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Design and development of poly -(3 -hexylthiophene) field effect transistors

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DESIGN AND DEVELOPMENT OF POLY-(3-HEXYLTHIOPHENE) FIELD EFFECT TRANSISTORS

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ABSTRACT

Organic field effect transistors (OFETs) with poly(3-hexylthiophene) (P3HT) as the active layer are developed and studied. The device characteristics are significantly affected by source/drain contact resistance, and P3HT-SiO_2 interface and the traps. These results are verified by the numerical device simulations. The temperature dependence of device mobility is studied, which indicates that the carrier transport is either heat-assisted or heat-limited at different temperature ranges. The on/off ratio and threshold voltage are found to be dependent on the temperature. Hysteresis effect due to gate electric stress is investigated. The silanol groups present at the SiO_2 surface are thought to be the key factor, which could trap the gate-induced electrons forming immobile negative ions, and shift the device threshold voltage.

Replacing gold with modified poly(3,4-ethylenedioxythiophene)-polystyrene sulfonate (PEDOT-PSS) for the source/drain electrodes, reduces contact resistance and leads to an improved device performance. The SiO_2 surface is also improved. Annealing the SiO_2 surface prior to the deposition of the P3HT layer is found to improve the performance of the device significantly. The device mobility is increased from 0.01 to 0.026 cm^2/Vs, the on/off ratio increased from 2.3×10^3 to 8.2×10^3, and subthreshold slope decreased from 3.6 to 2 V/dec. The enhanced device performance is attributed to the possible reduction of physically adsorbed water molecules and hydroxyl groups at the SiO_2 surface upon annealing.

Polymer heterostructure OFETs are also developed for establishing a method to fabricate new devices and the possibility to increase the device performance. This idea stems from the conventional inorganic modulation doped field effect transistors (MODFETs) that have shown strikingly high carrier mobility. The operation of conventional MODFETs is based on the technique of "modulation doping" which provides a good means of introducing carriers into the conduction layer without the adverse effects of donors. A polymer heterojunction structure is made of P3HT and poly(9,9-dioctylfluorenyl-2,7-diyl) (PFO) and is integrated into a field effect transistor. The resulting device characteristic shows the "modulation doping" effect. To our knowledge, the modulation doping effect with a polymer heterojunction has not been reported so far. This finding opens a potential pathway to improve the OFETs' device performance.

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CHAPTER ONE

INTRODUCTION

1.1 Organic Thin Film Transistor

Organic electronics have attracted tremendous research efforts over the last twenty years. It offers several advantages over the traditional inorganic semiconductor technologies for low cost, easy processing, good compatibility with a variety of substrates including flexible plastics and low temperature processing with little or no vacuum process involved. The interests in organic electronics are mostly driven by the demand for low cost, large area, flexible and lightweight devices. Organic light emitting diodes (OLEDs) and organic field effect transistors (OFETs) are two mainstream technologies in this area. OLED technology is now being commercialized, and there is a tremendous market for such devices. OLEDs have already been used in small displays in cellular phones, digital cameras, handheld computer games, and other consumer devices [1]. Meanwhile, OFET has also received considerable attention, although on a reduced scale. Since the first organic field effect transistor was reported in 1986 [2], there has been a very impressive progress both in the development of new fabrication techniques and the materials performance. OFETs have been demonstrated in applications, such as electronic paper, sensors, and memory devices including radio-frequency identifications tags [3-4]. Although they are not intended to replace conventional inorganic counterparts due to the

upper limit of the switching speed, they have a great potential for a wide variety of applications, such as electronic newspapers, low-end smart tags, and large-area drive circuits for flexible displays [5].

A field effect transistor (FET) with organic material as the semiconductor is normally called organic FET. An organic FET consists of materials ranging from conductors and semiconductors, to insulators. A typical device structure is shown in Figure 1-1. Here, the gate electrode, insulated from the semiconductor by an insulator, is used to control the current flow between the source and drain electrodes. A transistor is called p-channel device if the major charge carrier is hole, and on the contrary n-channel device when the major charge carrier is electron.

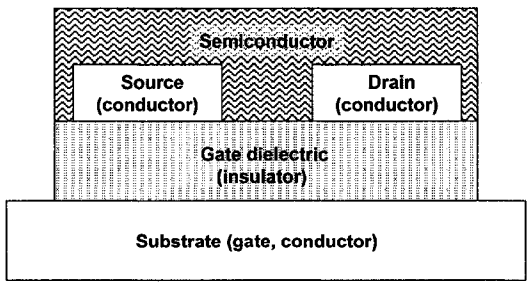


Figure 1-1 A schematic structure of a typical OFET.

1.1.1 Active Channel – Organic Semiconductor

One important feature that makes organic semiconductor attractive is the possibility for them to be deposited from solution for low-cost manufacturing. However, only a small number of soluble p-type organic semiconductors have been reported to show high performance, and a very few n-type organic semiconductors are soluble with reasonably high mobility. In order to build transistors with high mobility from solutions,

the materials should be soluble, and it should be possible to create large-area uniform films, in which the semiconducting molecules are desired to be well-ordered. The π-stacking between these molecules forms the conducting path for charge carriers to hop from one molecule to another molecule. However, with highly ordered materials it is usually difficult to form uniform films due to their high crystallinity. In contrast, polymers can easily form uniform films, but it is more difficult to obtain polymer films with high ordering. The polymer that gets around these two limitations is the regioregular poly (3-hexylthiophene) [6]. Therefore in our work, P3HT was selected for field effect transistor to demonstrate our strategies for improving OFET's performance.

1.1.1.1 Poly(3-hexylthiophene)

Poly(3-hexylthiophene) (P3HT) has been of particular interest due to its self-organizing properties to form a microcrystalline structure in films. Self-organization in P3HT results in a lamellar structure with two-dimensional conjugated sheets formed by interchain stacking [7]. Differences in the regioregularity in P3HT samples have been found to cause markedly different orientations relative to the substrate. As shown in Figure 1-2, the lamellae can adopt two different orientations: parallel and perpendicular to the substrate, the mobilities of which differ by more than a factor of 100. In samples with high regioregularity (96%) and low molecular weight, the preferential orientation of ordered domains is with the (100)-axis normal to the film and the (010)-axis in the plane of the film (Figure 1-2a). Here (100)-axis is with the lamella layer structure ("a" in Figure 1-2a) and (010)-axis is with π-π interchain stacking ("b" in Figure 1-2a). In contrast, in samples with low regioregularity (81%) and high molecular weight, the crystallites are

preferentially oriented with the (100)-axis ("a" in Figure 1-2b) in the plane and the (010)-axis ("b" in Figure 1-2b) normal to the film.

Charge modulation spectroscopy (CMS) has been used to study the charge carriers present in region-regular P3HT [8]. It was demonstrated that the CMS spectra of charge carriers in high-mobility region-regular P3HT FET's are independent of charge density, modulation frequency, and temperature. This was the evidence for the presence of a single, intrinsic charge carrier that was identified as a singly charged polaron.

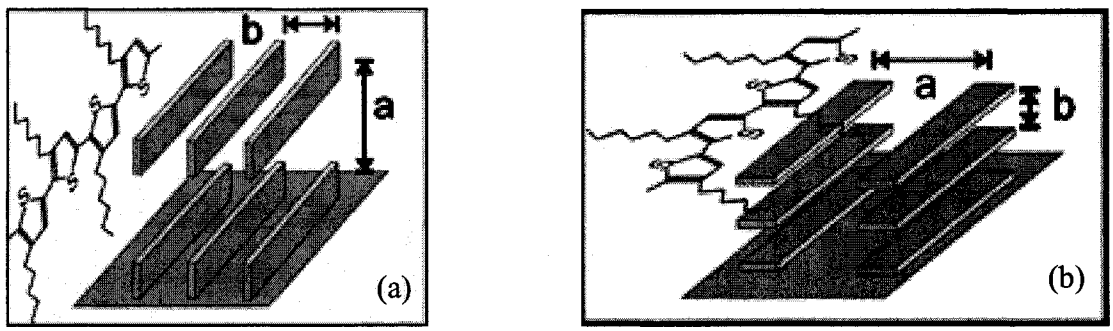


Figure 1-2 Packing orientation of P3HT films relative to substrate with (a) 95% and (b) 81% regioregularity, as determined by X-ray diffraction [7].

P3HT can be dissolved in a variety of solvents, such as chloroform, chlorobenzene, tetrahydrofuran, p-xylene and toluene, etc. It has been noted that the field-effect mobility can vary significantly with different solvents [9]. The mobility as high as 0.2 cm^2/Vs has been reported with P3HT film cast from chloroform solution and the SiO_2 gate dielectric covered with a hydrophobic self-assembly monolayer [10]. It was recently found that the dependence of mobility on the solvents could be related to the boiling points of the solvents [11]. Low boiling and rapid evaporation limit time for crystallization during spin coating process resulting in lower field effect mobility. Solution processes, such as drop casting, contact printing, Langmuir-Blodgett deposition,

dip coating, spin coating, and inkjet printing can be used to deposit P3HT films [12] [13] [14] [15]. One drawback of P3HT is that it is sensitive to moisture and oxygen when it is exposed to air, leading to the degradation of the device performance [16].

1.1.1.2 Other organic semiconductors

Examples of other organic semiconductors include p-type materials such as Cu-phthalocyanine [17], tetracene [18], phthalocyanine [19], α-sexithiophene [20], pentacene [21], α-ω-dihexyl-sexithiophene [22], poly[2-methoxy-5(2'-ethyl-hexyloxy)-1,4-phenylene vinylene] (MEH-PPV) [23], poly(9-9'-dioctyl-fluorene-co-bithiophene) [24], and dihexyl-anthradithiophene [25], etc., and n-type materials such as C_{60} [26], TCNQ [27], $F_{16}CuPc$ [28], and NTCDA [29]. It should be noted that most of the work to date has focused on p-type materials. The disproportionate development of p-type OFETs vs. n-type should be due to the inherent instability of n-type organic materials that react with water and oxygen under operating conditions, thus offering unstable devices [30]. Two methods have been proposed to improve the stability of n-type organic semiconductors in air. One is achieved by carefully tuning the electron affinity of n-type materials, since the stability of n-type doped materials depends strongly on the value of the overpotential associated with the chemical processes. The other is accomplished by kinetically inhibiting the undesired redox processes. For example, the incorporation of hydrophobic functionalities into the chemical structure of the organic semiconductor could thwart the penetration of water [30].

1.1.2 Gate Dielectric - Insulator

As compared to the extensive research efforts on organic semiconductors, there has not been much research on dielectric materials so far, even though they are extremely

crucial for high-performance and reliable organic devices. The basic requirements for such dielectric materials are their ability to form thin, pinhole-free films with a high breakdown voltage and good long-term stability. Additionally, the dielectric material should be compatible with organic semiconductors. For instance, the dielectric films must have low surface trapping density, low surface roughness, low impurity concentration and must not degrade the performance of ordered organic semiconducting films [6]. Silicon dioxide has been the most extensively used dielectric material so far, since it possesses most of the desired features and it offers a simple fabrication process for organic devices that are built on the silicon substrate. However, the natural hydroxyl groups present at the SiO_2 surface acted as surface traps reducing the hole mobility and quenching n-channel FET activity of organic semiconductors that do not have sufficiently large electron affinities [31] [32]. Pre-treatment of the Si-SiO_2 substrate with silylating agents replacing the hydroxyl groups with non-polar alkyl group has resulted in hole mobility of as high as $0.1 cm^2/Vs$ [31] and ambipolar activity [32] in P3HT FETs. A number of organic dielectric materials have also been found to give reasonable transistor performance. Examples are poly(methyl methacrylate) [33], poly(vinylphenol) [34], and polyimide [35]. From reliability and manufacturing yield considerations, a minimum dielectric layer thickness of 1000Å or more is necessary for large-area electronics [30]. Thicker dielectric layers are more suitable for large area applications since they suppress the formation of pinholes and the problems with step coverage. In this sense, a higher dielectric constant gate insulator is the more appropriate solution for low operation-voltage OFETs [36]. However, exceptional examples are known to exist. For example, recently, thin (2.3-5.5nm) self-assembled organic dielectric multilayers were integrated

into OFET structures to achieve sub-1V operating characteristics [37]. It was claimed that these thin dielectrics were smooth, nanostructurally well defined, strongly adherent, thermally stable, virtually pinhole-free, and with excellent insulating properties.

1.1.3 Electrodes – Conductor

Besides the organic semiconductor and gate dielectric, the conductor material, as the third component in an OFET's structure, has decisive impacts on the device electrical characteristics. The heavily doped silicon substrate is commonly used as the gate electrode for a simple fabrication process. Gate contact normally would affect the operation voltage of the OFET, but not at a significant level since organic devices normally operate at high voltages. For the source and drain electrodes, specific requirements need to be met. They have to be energetically well-matched with the organic semiconductor layer so that ohmic contact can be formed to allow efficient charge injection. For p-channel OFETs, charge carriers are holes. They are injected from or onto the highest occupied molecular orbital (HOMO) levels of the organic semiconductors. High work function conductors are usually preferred for an efficient injection due to a low injection barrier. On the other hand, n-channel OFETs, charge carriers are electrons. Conductors with low work function are normally required to achieve efficient injection of electrons from the lowest unoccupied molecular orbital (LUMO) levels of the organic semiconductors. Among those contact metals that have been employed in organic electronic devices, gold is the most frequently used one. It was found to form ohmic contact with many p-type organic semiconductors, resulting in good device performance. For n-type FET, electrode materials are usually metals of low work function, such as Ca, and Mg. However, they are very reactive in air and require a

vacuum or inert environment for device preparation. Since the inkjet printing emerged as a direct writing method for metallization, conducting polymers, such as PEDOT-PSS, have become promising electrode materials to achieve low-cost and high-performance devices [38]. Metals, such as gold [39] and silver [40], have also been deposited by printing for source/drain (S/D) electrodes giving good OFET performance.

1.2 Technology Computer Assisted Design

1.2.1 Overview

Technology Computer Aided Design, or TCAD, is the term used to describe a wide range of modeling and analysis activities that comprises detailed simulation of fabrication processes, electrical performance of single or multiple device and extraction of discrete parameters for equivalent circuit models. Numerical simulation of semiconductor device fabrication and operation is significant to the design and manufacturing of integrated circuits because it provides insights into complex phenomena that cannot be obtained through experimentation or simple analytical models. Simulation tools also provide a controlled and repeatable numerical experiment which can yield information that cannot be measured with present equipment. For the simulation tools to be useful in a practical environment, they should be physically accurate, computationally robust, and usable by those other than the software developers [41]. TCAD has been widely used by IC manufacturers during technology development. The software examples are SUPREM, PISCES, PROPHET, ATHENA, ATLAS, TSUPREM4, MEDICI, TAURUS, DIOS, and DESSIS, etc. Figure 1-3 shows schematically a typical TCAD flow. Starting from a process recipe and knowledge of the layout, a structure is created via process simulation. This structure is fed directly into the device simulator,

which produces I-V or C-V curves. One important benefit from simulation is a better understanding of how devices really operate. The simulation allows one to see inside the devices. For example, one can see how the electric field, and charge carriers distribute in the device structure; one can visualize where depletion regions are located. Apart from the flow information as shown in Figure 1-3, device simulation can also be performed without process simulation. In this case, doping profiles can be specified as Gaussian functions, which is suitable for many applications. This approach is very fast compared to process simulation. Another TCAD application is associated with the concept of inverse modeling. One starts with known device characteristics, and then searches for a structure that reproduces these curves.

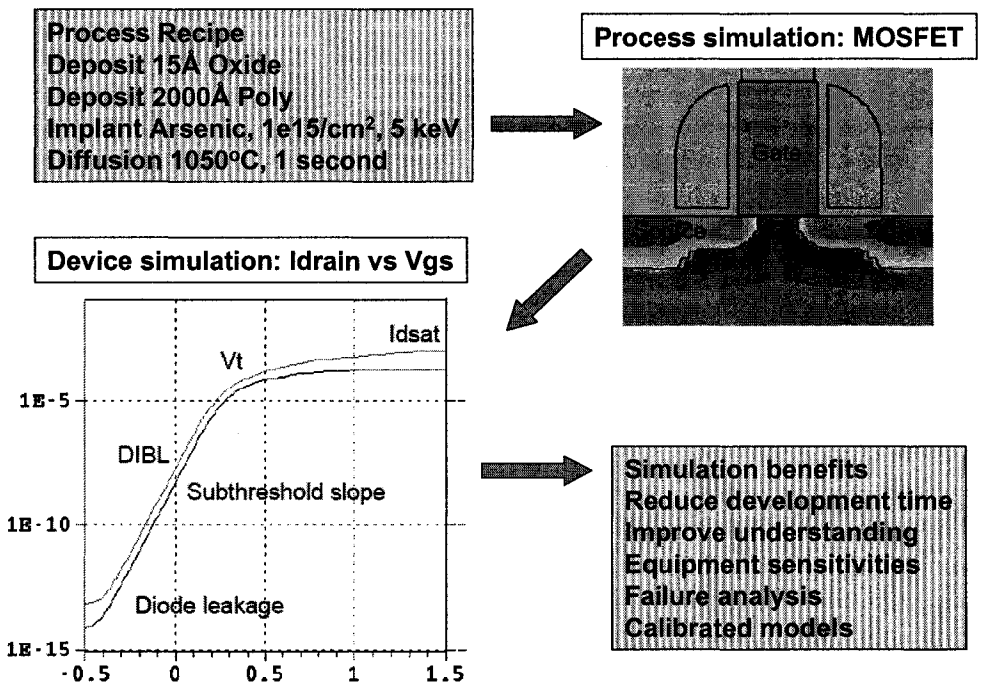


Figure 1-3 A typical TCAD flow [42].

However, examples can always be found where the simulation results do not match experimental results. The differences could arise from the insufficient physics for new materials, inaccuracies in metrology especially for gate length and oxide thickness, improper use of software tools such as models, and missing process details such as temperature ramp [42].

1.2.2 Device Simulation

Device simulation is usually done by employing the drift-diffusion (DD) model for electron transport. The equations for the flow of electrons and holes were given by Shockley consisting of three partial differential equations (PDEs) including electron and hole-current continuity equations and Poisson's equation [41]. Besides the DD model, there exists a density gradient (DG) model, which is an extension to the DD equations. It applies a quantum potential correction in the current density expression and is capable of calculating confined carrier concentrations and other quantum effects such as tunneling. Some of its advantages over other quantum models include the ability to handle complex geometries and to be readily applied in 1D, 2D and 3D [43].

1.3 Dissertation Objectives

The objective of this project is to present the previously discussed strategies to improve organic field effect transistors. First, poly(3-hexylthiophene) OFETs are fabricated and characterized based on a solution process. Then we will use TCAD simulations to gain better understanding of our devices and to identify the key factors that could limit the device performance. After that our device improvement strategies will be demonstrated. Based on our understanding of the inorganic and organic semiconductors and the gate insulated FETs, we will present polymer heterojunction modulation doped

field effect transistors, which could offer an alternative pathway for improving OFET's performance.

1.4 Organization of this Dissertation

Chapter One introduces organic field effect transistor as an ensemble of three components, namely, conductor, semiconductor and insulator. Related work that has been done and special requirements on these three components are briefly addressed in order to highlight the issues that could lead to high-performance OFETs. Then TCAD is introduced, highlighting the importance of the numerical simulation on the design and the understanding of the semiconductor devices. Finally, the objectives of our work are described.

Chapter Two covers the theoretical background that has been applied in this work. The conducting mechanisms of the organic semiconductors are introduced, followed by the operation principles of the OFETs. The conducting mechanisms include hopping transport, multiple trapping and release models, and field-dependent mobility. In the operation principles of the OFETs, we focus on the energy band diagrams, electric characteristics, contact resistance effects, trapping effects and gate bias dependent mobility.

Chapter Three introduces the fabrication and characterization techniques. Two solution processes, i.e. spin coating and inkjet printing, as well as the device characterization technique are emphasized.

Fabrication and analysis of poly(3-hexylthiophene) field effect transistors are given in Chapter Four. Device characteristics are investigated considering contact

resistance effect, gate voltage dependence of mobility, temperature dependence of mobility. The hysteresis effect of the fabricated devices is also explored.

In Chapter Five, we simulate the P3HT FET using 2-D Taurus-Device simulator in order to gain better understanding of device operation. The simulation is carried out based on drift-diffusion model. Traps and contact resistance are modeled.

With the knowledge of the fundamental issues that could affect P3HT device characteristics and performance, our strategies to improve P3HT device are demonstrated in Chapter Six, including improving S/D contact and semiconductor-insulator interface.

In Chapter Seven, instead of a single P3HT layer as the active channel, a polymer heterojunction involving P3HT is utilized as the channel material. The polymer heterojunction FETs show "modulation doping" effect analogous to that in conventional inorganic modulation doped field effect transistor (MODFET).

We will conclude our work in Chapter Eight and high-light some issues that should be done in the future.

CHAPTER TWO

THEORETICAL BACKGROUND

2.1 Charge Transport in Polymeric Semiconductors

2.1.1 Overview

The main element of conjugated polymers is the carbon atom, which has four electrons in the outer electronic level. The orbitals of these electrons could mix to create four equivalent degenerate orbitals called sp^3 hybrid orbitals around the carbon atom. These sp^3 hybrid orbitals arrange in a tetrahedral configuration. If only three chemical bonds are formed, three sp^2 hybridized orbitals will be created at an angle of 120° with each other in a plane. These bonds are called σ-bonds, associated with highly localized electrons in the plane of the molecule. The one remaining free electron per carbon atom is located in the p_z orbital, which is normal to the sp^2 plane. The p_z orbitals on the adjacent carbon atoms overlap to form π-bonds. A schematic representation of this hybridization is illustrated in Figure 2-1, for the simplest conjugated polymer polyacetylene [44]. Molecules with σ- and π-bonds are schematically represented by single and double alternating chemical bonds between the carbon atoms. They are called conjugated molecules. Due to the π-bonds, a delocalized electron density distributes above and below the plane of the molecule. It is the nature of these delocalized π-electrons that provide conjugated polymers interesting electrical and optical properties [44].

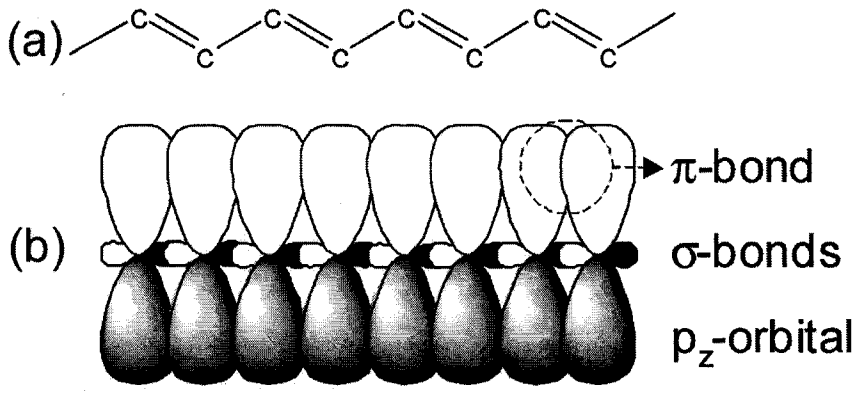


Figure 2-1 (a) The molecular structure of polyacetylene. The alternating single and double bonds indicate that the polymer is conjugated. (b) Schematic representation of the electronic bonds in polyacetylene [44].

There exist significant differences between the 3-dimensional crystal lattice of most inorganic semiconductors and the amorphous structure of conjugated polymers. Inorganic semiconductor crystalline lattices are characterized by long range order and strongly coupled atoms. Long-range delocalized energy bands are separated by a forbidden energy gap. Charge carriers added to the semiconductor can travel in these energy bands with a relatively large mean free path. The restrictive factor for this band transport is the scattering of the charge carriers due to thermal lattice vibrations, as illustrated by Figure 2-2a, where straight line represents a free carrier delocalized and moving freely in a perfect crystal [44]. Since lattice vibrations increases with increasing temperature, the mobility of the charge carriers decreases with increasing temperature. On the other hand, in conjugated polymers, the polymer chains are weakly bound by Van der Waals forces. These polymers generally have narrow energy bands. They can easily be disrupted by disorder. Although electric charge is delocalized along the π-conjugated segments of the polymer backbone, the length of such perfectly conjugated segments is generally limited to around several nm. These conjugated segments are separated by

chemical defects, such as a non-conjugated sp^3 hybridized carbon atom on the polymer backbone, or by structural defects, such as, chain kinks or twists out of coplanarity. Due to the disorder, the semiconductor can not be considered simply as having two delocalized energy bands separated by an energy gap. Instead, the charge transport sites, the segments of the main polymer chain, have a Gaussian distribution of energies [44]. The motion of the carriers in the amorphous conjugated polymers is thought to be via hopping process. The lattice vibrations are essential for a carrier to move from one site to another. The mobility normally increases with increasing temperature. The charge transport in these amorphous material system is schematically illustrated in Figure 2-2b.

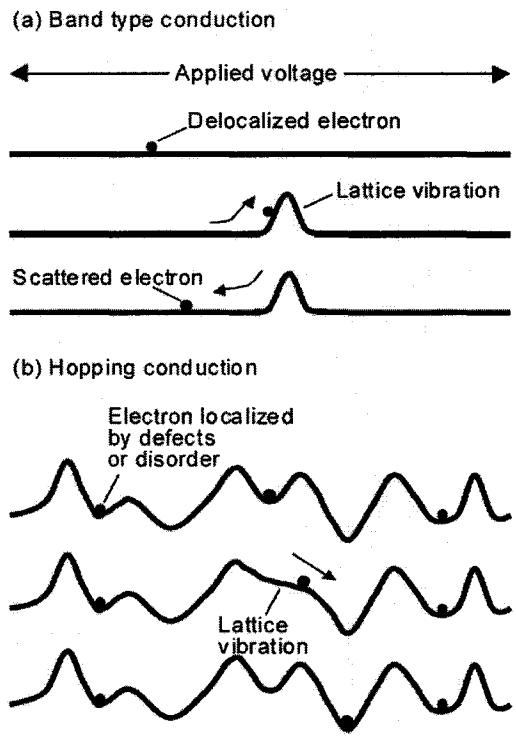


Figure 2-2 Charge transport mechanisms in solids: (a) band transport in a crystal structure, such as, silicon and (b) hopping transport in an amorphous structure such as conjugated polymer [44].

2.1.2 Hopping

As mentioned above, due to the disorder and localization of charges, the transport of charge carriers in polymeric semiconductors occurs by hopping between localized states. The transport is assisted by phonons, thus the mobility increases with increasing temperature. Several models have been developed for the hopping transport. In most cases, the temperature dependence of the mobility follows

$$\mu = \mu_0 \exp[-(T_0 / T)^{1/\alpha}] \tag{2-1}$$

where α is an integer ranging from 1 to 4 [2].

2.1.3 Field Dependent Mobility

In organic materials, the mobility generally becomes field dependent at high electric field, i.e., larger than ~10^5 V/cm. This effect is generally explained as follows: the coulombic potential near the localized levels could be modified by the applied electric field in a way that the tunnel transfer rate is increased between sites. The field dependence of the mobility is expressed by

$$\mu(E) = \mu(0) \exp(\frac{q}{kT} \beta \sqrt{E}) \tag{2-2}$$

$$\beta = (q / \pi \varepsilon \varepsilon_0)^{1/2} \tag{2-3}$$

where $\mu(0)$ is the mobility at zero electric field, β the Poole-Frenkel factor determined by Equation 2-3, E the magnitude of the electric field, ϵ permittivity of the semiconductor, and q electron charge [45].

2.1.4 Multiple Trapping and Release

Multiple trapping and release (MTR) model has been used to explain gate voltage dependent mobility in amorphous silicon. This model assumes that charge transport takes

place in extended states, and most of the carriers injected into the semiconductor are trapped in states localized in the band gap. Then by a thermally activated process, the trapped carriers are released to the extended states. The trapped-controlled drift mobility related to the mobility in the delocalized band can be expressed by Equation 2-4 [45] [46]

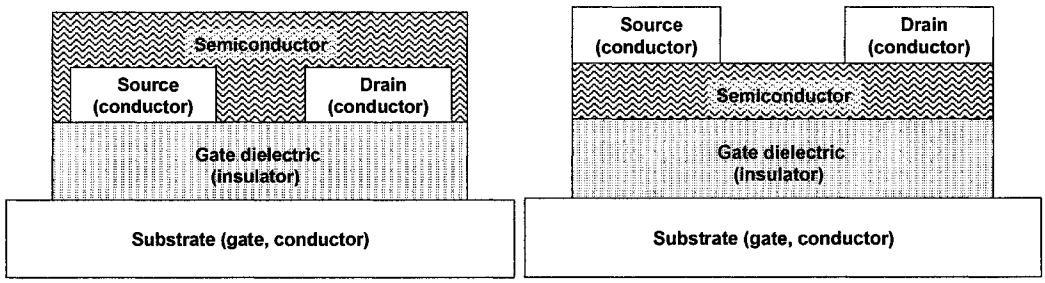
$$\mu_D = \mu_0 \lambda \exp(-\frac{E_t}{kT}) \tag{2-4}$$

where μ_D and μ_0 are effective drift mobility and the mobility in the delocalized band, respectively, E_t is the distance between the trap level and the delocalized band edge. In the case of single level of trapping states, λ is the ratio of the density of states at the delocalized band edge and the density of traps.

2.2 Operation of Polymeric Field Effect Transistors

Figure 2-3 shows schematic diagrams of thin film transistors (TFTs) based on bottom-contact and top-contact structure, respectively. Both structures have been widely used in organic field effect transistor with their own advantages. The operation mode of a TFT is different from that of a conventional metal-insulator-semiconductor field effect transistor (MISFET). The operation of a conventional MISFET is through a minority-carrier channel which forms in the strong inversion regime. The source and drain regions are oppositely doped as compared to the semiconductor channel. At zero gate voltage, structure from source to drain actually consists of two back-to-back p-n junctions, thus giving extremely low off-currents. In the TFT, source and drain electrodes have low contact resistance. The low source-drain current at zero gate voltage is simple due to the low conductivity of the semiconductor. Field-enhanced current occurs through majority-carrier injection in the accumulation layer. Organic (or polymer) field effect transistors

share the common features with the TFTs, in that, it also operates in the accumulation regime and not in the inversion region, and the low off currents are only guaranteed by the low conductivity of the organic semiconductors.



(a) (b)

Figure 2-3 Schematic structures of a TFT with (a) bottom-contact and (b) top-contact configuration.

2.2.1 Energy Band Diagrams

The energy band diagrams of a p-type MISFET at different operation conditions are schematically shown in Figure 2-4. Due to the work function potential difference between the semiconductor and the metal, a gate voltage is applied so that the Fermi levels of metal and semiconductor align, then no band bending will occur in the semiconductor as shown in Figure 2-4a. This gate voltage is called the flat band voltage V_{FB}

$$V_{FB} = \phi_{ms} = \phi_m - (\chi + \frac{E_g}{2q} + \phi_b) \qquad (2\text{-}5)$$

Here, ϕ_m is the metal work function, χ the electron affinity, E_g the semiconductor bandgap, q the electron charge, and ϕ_b the potential between the Fermi level and the intrinsic Fermi level E_i. If the work function of metal is similar to the Fermi level of semiconductor, the flat band voltage will be close to 0. Here we are not considering the

interface charges that also affect the flat band voltage. Applying a negative gate voltage will induce charges at the semiconductor-insulator interface. This causes band bending-up as shown in Figure 2-4b, indicating accumulation of holes at the interface. Under this condition, the p-channel transistor is turned on. When a positive gate voltage (or gate voltage higher than the flat band voltage) is applied, the mobile holes are depleted from the semiconductor-insulator interface due to the electric field, causing band bending down in the p-type semiconductor illustrated by Figure 2-4c.

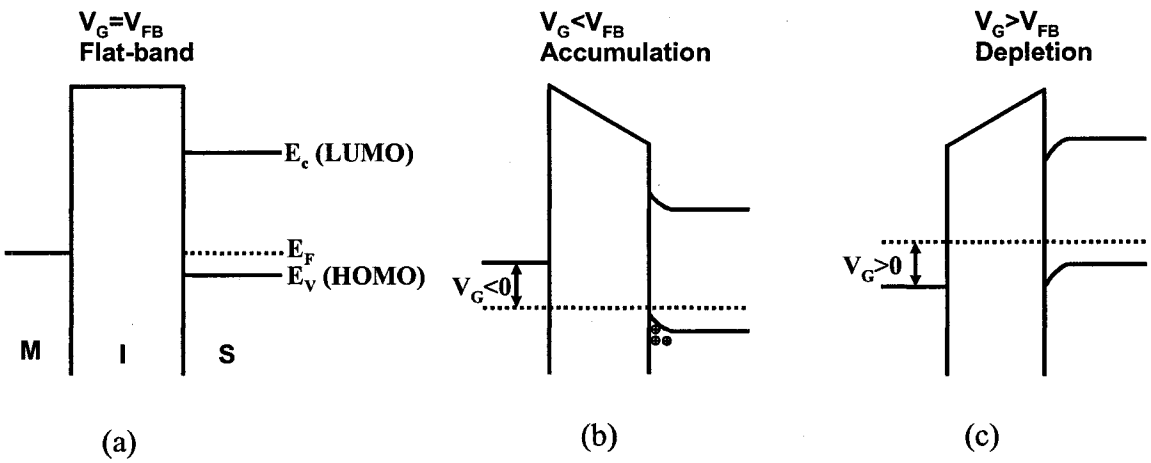


Figure 2-4 Energy gap diagram of a MIS structure with p-type semiconductor under (a) flat band condition, (b) accumulation, and (c) depletion. LUMO and HOMO apply for organic semiconductors.

2.2.2 Current-Voltage Characteristics

The drain current I_d up to the saturation point was predicted by a model derived by Borkan and Weimer [47]. An incremental section of length dx of a TFT, at an arbitrary distance x from the source, is shown in Figure 2-5, where the source is grounded, and the gate and drain are negatively biased. The charge at position x induced by gate is $C_i(V_g-V_x)$ per unit area, where C_i is the gate capacitance per unit area of the insulator, V_g is the gate potential, and V_x is the potential of the dx section relative to the source. The

potential V_x changes continuously along the semiconducting channel from zero at the source to V_d at the drain. If the initial free carrier concentration in the semiconductor is p_0 (p type) per unit area of surface, then the total conducting charge per unit area in the semiconductor is $p_0q + C_i(V_g-V_x)$. Then at low drain voltage, the current I_d is given by Equation 2-6[48]

$$I_d = w\mu[p_0 q + C_i(V_g - V_x)]\frac{dV_x}{dx} \tag{2-6}$$

where w is the width of the TFT, μ is the carrier mobility, and dV_x is the potential difference across the dx section. Having $V_T = -p_0q/C_i$, Equation 2-6 becomes

$$I_d \int_0^L dx = C_i w\mu \int_0^{V_d} [(V_g - V_T) - V_x]dV_x) \tag{2-7}$$

where L is the channel length, the distance from the source to drain. By integration, Equation 2-7 becomes

$$I_d = \frac{Cw\mu}{L}[(V_g - V_T)V_d - \frac{V_d^2}{2}] \tag{2-8}$$

V_T represents the applied gate voltage required for the onset of the conduction. If V_T is positive, the TFT is thought to operate in the enhancement mode, whereas the device is said to operate in the depletion mode if V_T is negative.

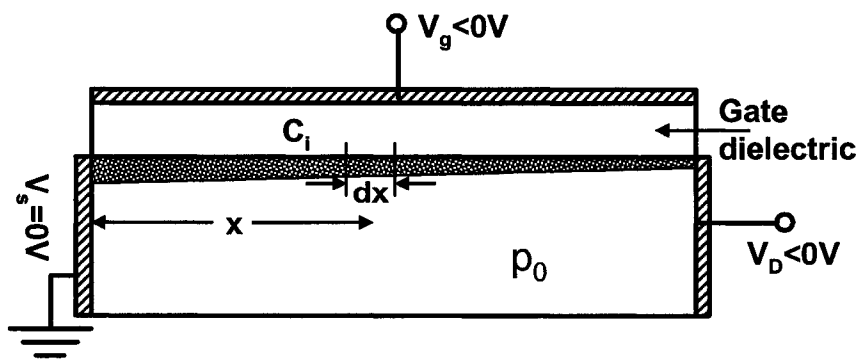


Figure 2-5 Channel formation in a TFT.

Equation 2-8 indicates that for a given Vg, the current increases with drain voltage and reaches a maximum value when V_d=Vg-V_T. At a low drain voltage and a large negative gate voltage, the quadratic term in Equation 2-8 could be ignored, and then Equation 2-8 could be simplified to

$$I_d = \frac{Cw\mu}{L}(V_g - V_T)V_d \tag{2-9}$$

Under this condition, there will be a uniform accumulated charge density throughout the channel. However, as the drain bias becomes increasingly negative, the voltage drop across the insulator and semiconductor will be a function of a position along the channel [49]. The accumulation charge density decreases along the channel from the source to the drain, as shown in Figure 2-5. When drain voltage reaches V_g-V_T, charge accumulation disappears near the drain, resulting in the so-called "pinch-off" of the channel. Then the TFT starts with a saturation region, where drain current remains substantially constant with increasing drain voltage. The saturation current is given by

$$I_{dsat} = \mu\frac{w}{2L}C_i(V_g - V_T)^2 \tag{2-10}$$

Equation 2-10 is obtained by simply substituting in Equation 2-8 with V_d=Vg-V_T. From the I-V characteristics, two important technological parameters viz. the channel conductance g_d and transconductance g_m can be determined. The channel conductance is obtained in the linear regime expressed by

$$g_d = \left|\frac{\partial I_d}{\partial V_d}\right|_{V_g=constant} = \frac{w}{L}\mu C_i(V_g - V_T) \tag{2-11}$$

The transconductance in the linear and saturation regimes are given by Equations 2-12 and 2-13, respectively,

$$g_m = \left|\frac{\partial I_d}{\partial V_g}\right|_{V_d=const} = \frac{w}{L}\mu C_i V_d \tag{2-12}$$

$$g_m = \frac{w}{L}\mu C_i (V_g - V_0) \tag{2-13}$$

Another significant technological parameter is mobility, which is normally taken as a measure of device performance. Higher mobility is preferred. For simplicity, mobility value can be derived from Equation 2-10 by plotting $I_D^{1/2}$ against V_G in the saturation regime. The x-intercept of the curve determines the threshold voltage. In the linear operation region, the mobility estimated using Equation 2-12 is usually gate-dependent, which is due to a nonlinear V_g~I_d relationship at low drain voltage. As addressed afterwards, this nonlinearity could be attributed to the source/drain contacts and the trapping effects in the organic field effect transistors.

2.2.3 Contact Resistance Effects

Source/drain contact resistance in OFETs have been investigated and found to strongly affect the overall device performance [50][51][52]. In the metal-organic semiconductor system, a large contact resistance normally arises from a Schottky contact between them. This non-ohmic contact is dependent on the gate electric field [53], resulting in the nonlinearity of V_g~I_d as mentioned above. By matching the energy levels between electrode and semiconductor, an ohmic contact could be reached. However, at the transition area between organic semiconductor and source/drain electrodes, the organic semiconductor could be poorly ordered forming a low-mobility region, resulting in a significant contact resistance. Accounting for the parasitic series resistance at source and drain R_p, Equation 2-9 could be improved to [51]

$$I_d = \frac{w}{L} C_i \mu (V_g - V_T)(V_d - I_d R_p)$$

$$= \frac{(w/L) C_i \mu (V_g - V_0) V_d}{1 + (w/L) C_i R_p (V_g - V_0)} \quad (2\text{-}13)$$

Since R_p can not be directly measured, estimating mobility from Equation 2-13 seems to be complicated. Nevertheless, R_p could be removed by some numerical manipulations [51]. First, we calculate the drain conductance g_d (Equation 2-14) and transconductance g_m (Equation 2-15) at low drain voltage

$$g_d = \frac{\partial I_d}{\partial V_d} = \frac{I_d}{V_d} = \frac{(w/L) C_i \mu (V_g - V_T)}{1 + (w/L) C_i \mu R_p (V_g - V_T)} \quad (2\text{-}14)$$

$$g_m = \frac{\partial I_d}{\partial V_g} = \frac{(w/L) C_i \mu V_d}{[1 + (w/L) C_i \mu R_p (V_g - V_T)]^2} \quad (2\text{-}15)$$

To eliminate the parasitic resistance, Equation 2-14 is divided by the square root of Equation 2-15 giving the following equation [51]

$$\frac{g_d}{\sqrt{g_m}} \sqrt{\frac{L}{w} \frac{V_d}{C_i}} = \sqrt{\mu} (V_g - V_T) \quad (2\text{-}16)$$

Therefore Equation 2-16 could be used to estimate field effect mobility, which is corrected for contact resistance and therefore it could describe the carrier mobility in organic semiconductor channel more accurately. The parasitic contact resistance could be derived from Equation 2-14 and has the following form

$$R_p = \frac{1}{g_d} - \frac{L}{w \mu C_i (V_g - V_T)} \quad (2\text{-}17)$$

Parasitic contact resistance could also be estimated by channel length series method, in which a set of devices with various channel lengths are characterized at low drain voltage [54] [55]. For each device at each gate voltage, the linear portion of I_d-V_d,

is used to find total source-to-drain resistance R_{total}, which is then plotted as a function of channel length. The extrapolated resistance corresponding to zero channel length gives parasitic contact resistance R_p. Then channel conductance R_{ch} can be obtained by subtracting R_p from the R_{total}. The mobility threshold voltage can be derived from the linear fit of sheet channel conductance as a function of gate voltage, with the slope and x-intercept of fitted line giving the intrinsic mobility and threshold voltage, respectively.

2.2.4 Trapping Effects

As described earlier in section 2.1 in this chapter, for the amorphous semiconductors, especially polymeric semiconductors, the material system is featured with a disordered structure having a significant density of defects that could trap carrier charges. The device behaviors of the OFETs, like the amorphous silicon TFTs [48], have been successfully explained by the trapping effects [56] [57] [58]. Proposed by Horowitz et al., [57], the trapping effect on the OFETs is divided into three regions.

(1) Region 1 extends from V=0 to V=V_1. V_1 corresponds to the surface potential where all traps are filled. The free and trapped carrier distribution can be approximated by the Boltzman distribution

$$n_f = N_v \exp(-\frac{E_v - E_F - qV}{kT}) = n_{f0} \exp\frac{qV}{kT} \tag{2-18}$$

$$n_t = N_t \exp(-\frac{E_t - E_F - qV}{kT}) = n_{t0} \exp\frac{qV}{kT} \tag{2-19}$$

where n_{f0} and n_{t0} are the bulk free and trapped carrier density. Bulk free/trap carrier-density ratio is introduced and expressed by

$$\theta_0 = \frac{n_{f0}}{n_{f0} + n_{t0}} \tag{2-20}$$

Taking into account the trapping effects, Equation 2-10 could be rewritten as

$$I_{dsat} = \theta_0 \mu_0 \frac{w}{2L} C_i (V_g - V_T)^2 \qquad (2\text{-}21)$$

where μ_0 could represent the intrinsic mobility of organic semiconductor.

(2) Region 2 extends from V_1 to V_2, where n_t is equal to n_f. This region corresponds to the so-called subthreshold regimes. The saturation current varies exponentially with the gate voltage.

(3) Region 3 extends beyond V_2. The free-carrier concentration is higher than the trapped carrier density. Therefore the total carrier concentration can be taken as the free carrier concentration resulting in θ_0 approximating 1. Then the intrinsic field effect mobility is approximately equal to the experimentally determined mobility.

Besides the above mentioned bulk traps that are associated with the organic semiconductor itself, interface traps at the insulator-semiconductor interface due to the defects on the insulator should not be neglected. The interface trapping effect could be significant due to the fact that the most of the charge transport occurs in one or two monolayers near the insulator-semiconductor interface. Recent reports [59] [60] suggested that the thermally grown SiO_2 surface carries SiOH silanol groups of a concentration up to (3–7) $\times 10^{13}$ cm^{-2}, which greatly exceeds the typical carrier concentration of 10^{13} cm^{-2}. These SiOH groups could trap induced electrons creating immobile SiO^- ions ($SiOH + e^- \rightarrow SiO^- + 1/2H_2$), which compensate or enhance gate electric field depending on the polarity of gate voltage, as illustrated in Figure 2-6, where $\ominus$ represents the immobile negative ions, E_1 gate electric field, E_2 the field due to the negative ions, E_1' the effective gate electric field. One can see that, for a negative gate

voltage, the effective electric field is enhanced by the negative ions, and vice versa for positive gate voltage.

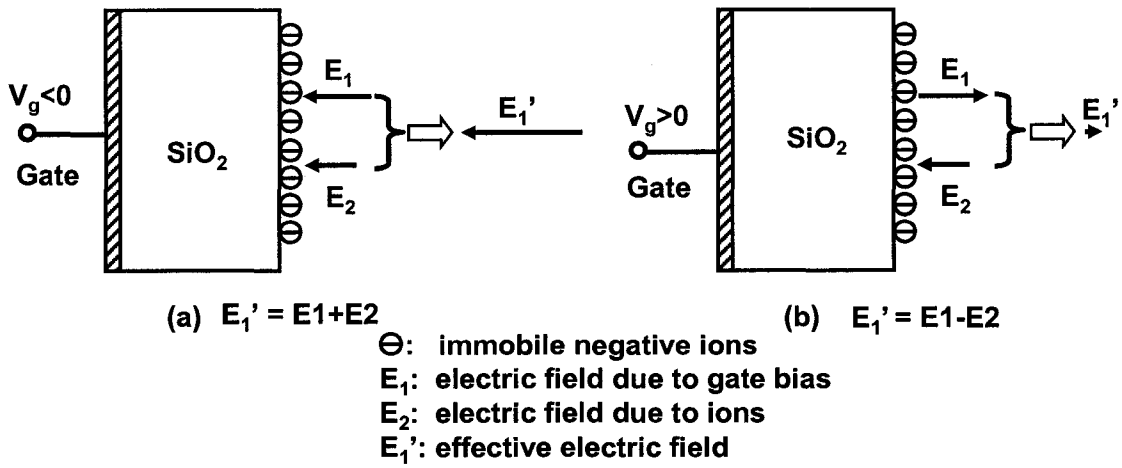


Figure 2-6 The effect of immobile negative ions on the electric field at the SiO_2 surface, (a) ions enhance the gate electric field and (b) ions compensate the gate electric field. The length of the arrows schematically represents the amplitude of the electric field.

2.2.5 Gate Bias-Dependence Mobility

As mentioned above in the section 2.2.4, the gate voltage dependent mobility is associated with the trapping effect. The gate voltage dependence of mobility simply comes from its dependence on mobile carrier density. Varying the gate voltage tunes the ratio between the densities of free carriers and trapped charge carriers, resulting in changing effective mobility. The gate dependence of mobility can be described by an empirical equation [61]

$$\mu = \alpha(V_g - V_0)^{\beta} \tag{2-22}$$

where α and β are fitting constants, V_g the gate voltage and V_0 the fitting threshold voltage.

CHAPTER THREE

FABRICATION AND CHARACTERIZATION METHODS

3.1 Introduction

In this work, several micro-fabrication processes and characterization techniques were used. They include metallization processes, such as thermal evaporation, sputtering, e-beam deposition, lithography, lift-off, etc.; polymer deposition processes, such as spin coating and inkjet printing; film characterization techniques such as atomic force microscope (AFM), scanning electron microscopy (SEM), Alpha step profilometer, Fourier transform infrared spectroscopy (FTIR), ellipsometer, roughness step tester (RST), etc.; device characterization system, such as Keithley probe station. Inkjet printing, spin coating, and device characterization techniques are most frequently used and thus are highlighted as follows.

3.2 Inkjet Printing

3.2.1 Introduction

Inkjet printers may operate in either continuous or drop-on-demand (DOD) mode. In continuous-mode inkjet printing, the ink is pumped through a nozzle to form a liquid jet. It is mostly used for high-speed graphical applications. In our work, drop-on-demand

mode is used. In a DOD inkjet printer, an acoustic pulse ejects ink droplets from a reservoir through a nozzle. The pulse can be generated either thermally or piezoelectrically (Figure 3-1). In a thermal DOD inkjet printer, ink is heated locally to form a rapidly expanding vapor bubble that ejects an ink droplet. Thermal DOD usually uses water as a solvent and may therefore impose restriction on the type of polymers that can be printed using this technique. Piezoelectric DOD inkjet printing, on the other hand, relies on the deformation of some piezoelectric material to cause a sudden volume change and hence generate an acoustic pulse. Piezo-electric DOD is suitable to a variety of solvents [62].

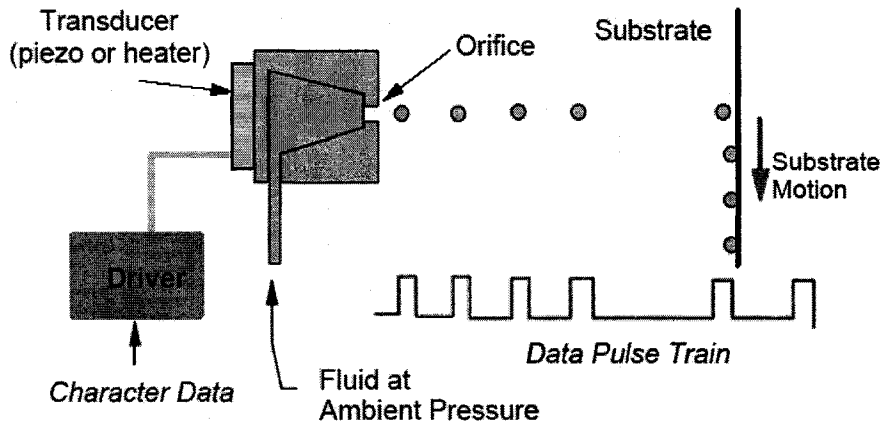


Figure 3-1 Schematic representation of a drop-on-demand ink-jet printing system [63].

3.2.2 Suitable Inks

The key part of inkjet printing technology is the ink. It must have specific physical properties particularly for the viscosity and surface tension. The viscosity should be suitably low, typically less than 20mPas. The polymer solution should therefore be sufficiently dilute. The surface tension is responsible for the spheroidal shape of the

liquid drop from the nozzle. Finally, the wetting behavior of fluid and nozzle material is of importance, as wetting of nozzle outlet face results in spray formation.

3.2.3 Coffee-Drop Effect

A serious problem with inkjet printing is the ''coffee-drop effect'': after evaporation of a printed solution droplet, most of the solute is accumulated as a ring that marks the original contact line [64]. This effect was explained by the pinning of the contact line of the droplet in combination with increased evaporation at the edges. However, to pin the contact line, liquid evaporated at the edges must be replenished by liquid from the interior. The resulting outward flow can carry virtually all the dispersed material to the edge [65] [66]. This "coffee-drop effect" could be overcome by the use of solvent mixtures to make polymer solutions, in which one solvent has a high boiling point and a low solubility for the polymer, and the other solvent has a low boiling point and a high solubility for the polymer. The dissolving potential of the solvent gradually decreases during evaporation and the polymer precipitates before a ring is formed. This method has been applied by Tekin et al., to avoid ring formation [67].

3.2.4 Microdrop Inkjet Printing System

All printing experiments are performed on a drop-on-demand (DOD) Microdrop Dispensing System (Microdrop GmbH, Germany, Figure 3-2). A printer head nozzle with an internal diameter of 50 μm and a 4 ml ink reservoir is used for our work. The printer is capable of simultaneously accommodating four printer head nozzles. The nozzle is driven by a voltage pulse signal, whose amplitude, pulse width, and frequency are determined by the printing program.

An MD-P-705 positioning system controls the movements of the nozzle in a XYZ station. The positioning accuracy is ±10 μm. The repetition accuracy is ±3 μm. The minimum step width of movement is 1 μm in X, Y and Z directions.

The substrate holder is a hotplate which is controlled by a PID (Proportional, Integral, and Derivative) regulator. The substrate holder can be heated up to 150 °C. A microscope connected with a monitor is used to accurately position printer head in order for the ejected droplets falling at the desired locations on the substrate.

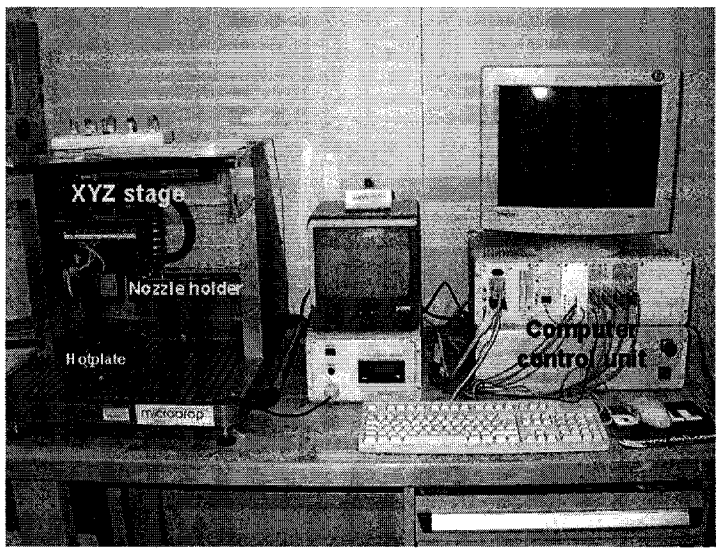


Figure 3-2 The Microdrop Dispensing System.

3.3 Spin Coating

Spin coating is a commonly used process in microfabrication to deliver solid films from solutions. Uniform film with desired thickness is achieved by controlling solution properties and spin coating parameters. A spin-coating process can be divided into three stages. Full knowledge of each stage is helpful for the formation of films with desired properties. The three stages are deposition and spin up, spin off, and film drying [68].

The first stage is the deposition and spin up [68]. At this stage, a liquid solution is first applied over the substrate. Next, the substrate is accelerated to its final rotational speed. At this stage, the majority of the liquid is sloughed from the substrate due to the overwhelming force of the centrifugal acceleration. Conversion to a thin, nearly uniform film takes place within the first second or two of spinning.

The second stage is the spin off [68]. During this stage the film is thinned due to a combination of convection and solvent evaporation. The centrifugal forces act to drive the fluid radially off the edge of the substrate impeded only by the viscous resistance. This radial flow quickly diminishes because the film has become exceedingly thin and evaporation of solvent has increased the viscosity by several orders of magnitude. During fluid flow, the film is also thinned by solvent evaporation. It is the trade-off between these two mechanisms that controls the film thickness, uniformity, and the success of the spin-coating process.

The third stage is the drying of the film [68]. In this final stage of spin coating, fluid flow has basically stopped and further shrinkage of the film arises from solvent loss alone. Concentration profiles depend on fluid convection flow through the cross terms in the solvent conservation equation [68]. However, as the velocity components drop to zero, this dependence becomes unimportant, and solvent conservation may be considered independently. It is at this point where the spin off stage ends and the film drying stage begins.

Figure 3-3 shows the dependence of final film thickness on the solution properties, rotational speed, and spin time. It indicates that increasing solvent weight fraction results in linearly decreased film thickness. A power-law dependence (see Figure 3-3b) is

predicted for the dependence of the final film thickness on the rotational speed. In the case of the dependence of film thickness on spin time (Figure 3-3c), it is shown that the film thickness first rapidly decreases within a short period of spin time, and then almost saturates with prolonged spinning time. These relationships will serve as an important guidance for spin coating work in our experiments.

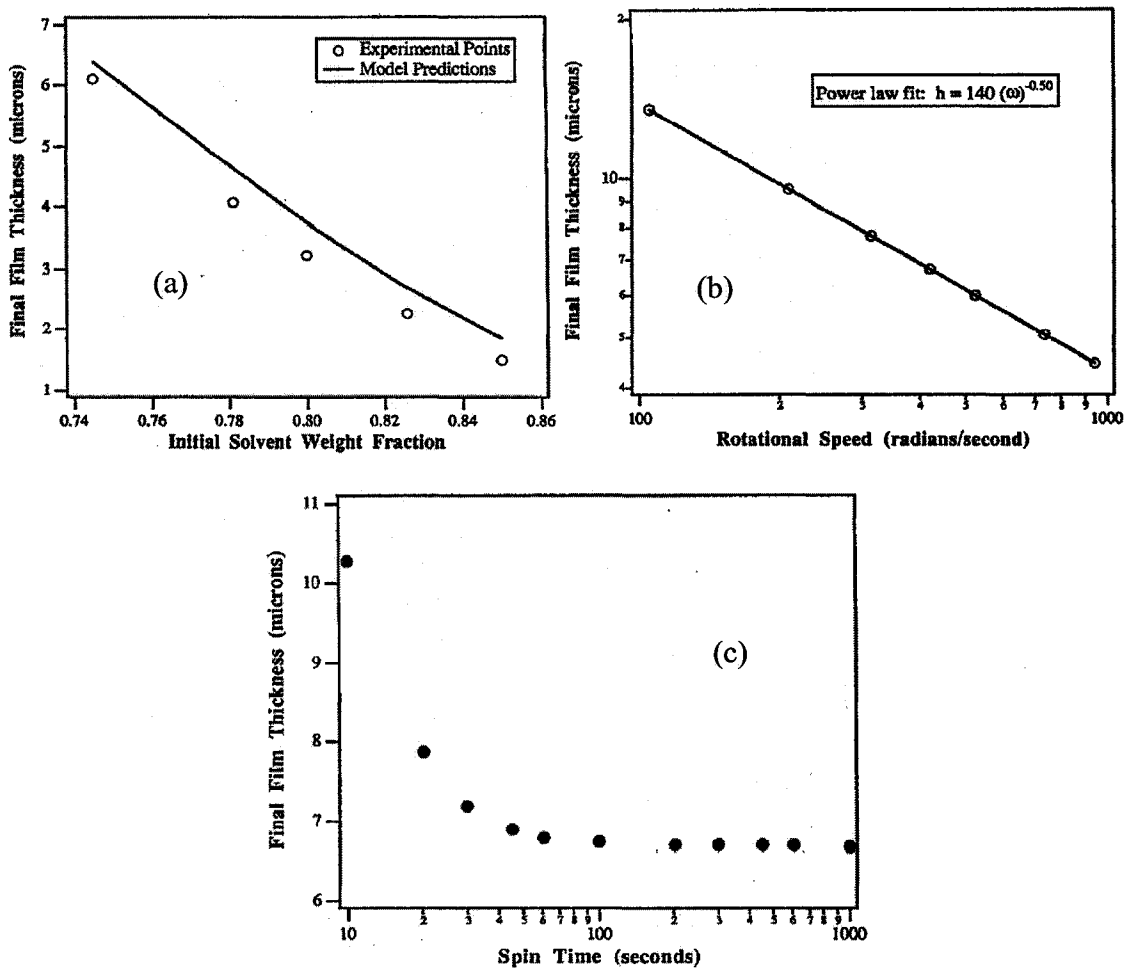


Figure 3-3 Dependence of final film thickness on the solvent fraction, rotational speed, and spin time (Du Pont PI2525 polyimide was used) [68].

3.4 Device Characterization

3.4.1 Keithley Probe Station

Device characterization is one of the most important steps in our work. In general, devices are tested for their current-voltage (I-V) and capacitance-voltage (C-V) characteristics. All electrical measurements are carried out on Keithley Probe station as shown in Figure 3-4, which is controlled by a computer via the IEEE-488 bus. The probe station includes three source measurement units for I-V characterization. Two-, three- and four-terminal devices, such as resistor, diode, capacitor, JFET, BJT, and MOSFET, can all be measured on this system. The measurable current is in the range of 1 PA to 100mA. The voltage could be applied to as high as 110V. Besides the I-V measurements, the probe station also allows to perform C-V measurements. It includes two additional source units for low frequency and high frequency capacitance measurements. The probe station is equipped with interactive characterization software (ICS) to remotely control the source units, allowing for fast and reliable measurements.

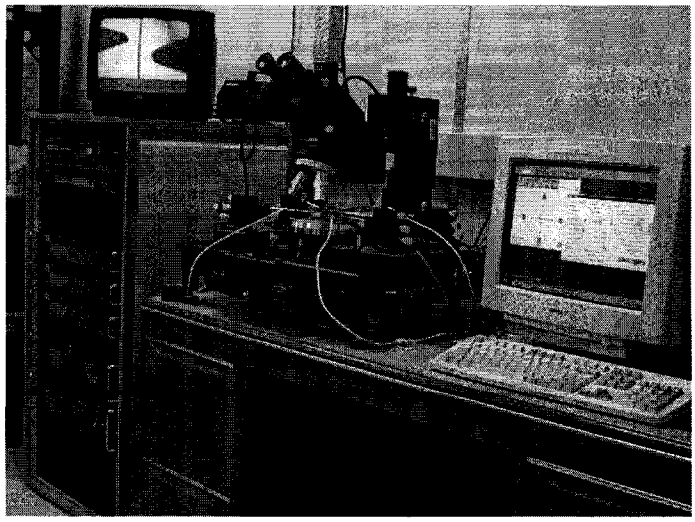


Figure 3-4 Photograph of Keithley probe station.

3.4.2 Required Measurements

Characterization of the organic transistor requires two primary sets of measurements. First, the transfer (I_{DS} vs. V_{GS}) curves that allow for determination of field-effect mobility, and threshold voltage and on/off ratio. These data are typically necessary for characterization of the semiconductor transport properties. Transconductance is also derived from this measurement. Second, the output characteristics (I_{DS} vs. V_{DS}) that provide channel conductance, current saturation and general electrical performance information. This curve is normally used to determine whether the device exhibits FET-like behavior [18].

3.4.3 Guidelines for OFET Characterization

Step size should be small enough to give a minimum of 10 data points per curve; 25 or more points are recommended. Increased number of data points results in more accurate curve fitting and greater noise/outlier tolerance, and therefore, more accurate parameter extraction [69].

Gate voltage values for V_{DS} vs. I_{DS} measurements are chosen to give a minimum of three curves; five or more curves are recommended. Values for gate voltage are to reflect the full expected operating range and/or demonstrate full device operating range.

A sufficiently long dwell time is required allowing organic materials to effectively respond to the electric signals. Minimum dwell time is 10 ms, but 100 ms or more is strongly recommended for each data point. Required dwell time is dependent on factors, such as device and instrument impedance values, field effect mobility, etc., and is selected sufficiently long so that transient effects do not affect measurement significantly.

Range of chosen values accurately represents full device operating range. These values are chosen so that device behavior is shown for the full expected operating range. Too high biases should be avoided to prevent damaging the devices under test.

CHAPTER FOUR

POLY (3-HEXYLTHIOPHENE) FET

4.1 Introduction

One key feature that makes organic semiconductors attractive is the possibility for them to be deposited from solution thus offering great potential for low-cost manufacturing. Semiconducting polymers provide good solubility in organic solvents enabling the formation of uniform film over large areas. However, compared with the OFETs made of the vacuum deposited small molecules, the polymer FETs normally have significantly lower field effect mobility thus reducing the possibility to put them into practical applications, such as drive circuits for organic displays. Semiconducting polymer poly(3-hexylthiophene) (P3HT) is an exception. It has good solubility in commonly used organic solvents, such as chloroform, chlorobenzene, p-xylene, and toluene, etc. Due to its high level of intrachain order, P3HT cast from solution self-assembles into regions of high-interchain order. Two-dimensional charge transport has been demonstrated in the film cast from regioregular P3HT solution. The 2-D nature of charge transport allows the charge carriers to spread over neighboring chains thus enhancing mobility. Field effect mobility as high as 0.2 $cm^2/V.s$ has been reported in OFETs with P3HT film cast on the hydroxyl free SiO_2 surface [10]. Remarkable properties of P3HT make it a material of choice to study OFET device physics and to

develop strategies for improving OFETs performance. In this work, field effect transistors composed of P3HT as the active layer are prepared and studied. Understanding of OFET device physics is achieved by analyzing the electrical characteristics of the device. This work serves as a base for further work that will be addressed in the next chapters.

4.2 Device Fabrication

Poly (3-hexylthiophene) (P3HT) thin film transistors were built on thermally oxidized heavily n-doped silicon wafers. The silicon oxide has a thickness of 1000Å for gate dielectric layer. The highly doped substrate serves as the gate electrode. A layer of 500Å Au/30Å Ti was deposited on the SiO_2 as the source/drain electrodes by sputtering and patterned by a lift-off process. Then a 20nm P3HT film, as the active semiconductor layer, was spin-coated on the SiO_2 surface, forming a bottom-contact structure as shown in Figure 4-1. The regioregular P3HT with head-to-tail linkages greater than 98.5% was obtained from Aldrich Chemical Company. The P3HT was used as received. The solution was made by mixing P3HT with p-xylene at a weight ratio of 0.5mg/ml.

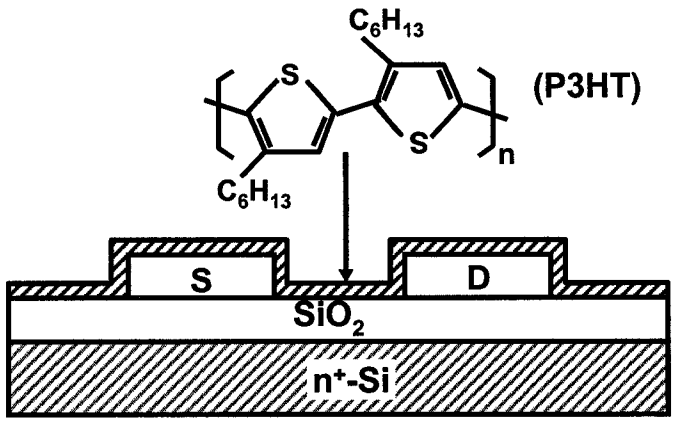


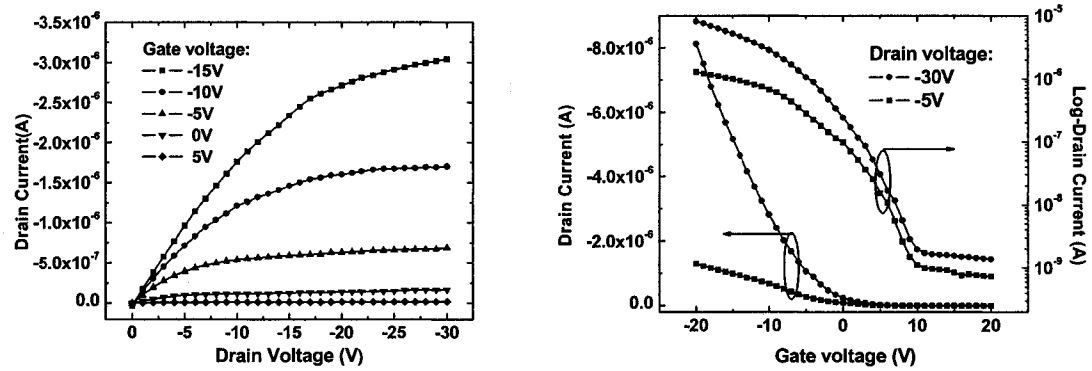
Figure 4-1 Schematic cross section of P3HT FET structure, above which molecular structure of P3HT is shown.

4.3 Results and Discussion

The fabricated devices were measured on a Keithley probe station in air at room temperature. The investigated devices have the channel length and channel width of 10μm and 500μm, respectively.

4.3.1 Device Characteristics

Figure 4-2 shows the output and transfer characteristics of the devices at room temperature.



(a) (b)

Figure 4-2 Output (a) and transfer (b) characteristics of poly(3-hexylthiophene) FETs.

These devices display the characteristics of a typical p-type thin film transistor: a negative gate voltage enhances while a positive gate voltage reduces the channel conduction; at a given gate voltage, the drain current linearly grows with the low drain voltage, then gradually saturates at high drain voltage regime. A substantial current level can be seen at zero gate voltage, which could be due to the unintentional doping of P3HT probably by oxygen [70]. As a result, a positive gate voltage has to be applied to turn off the device leading to a positive threshold voltage as determined afterwards. The residual doping level of P3HT can be estimated as follows, which was described in Ref [10].

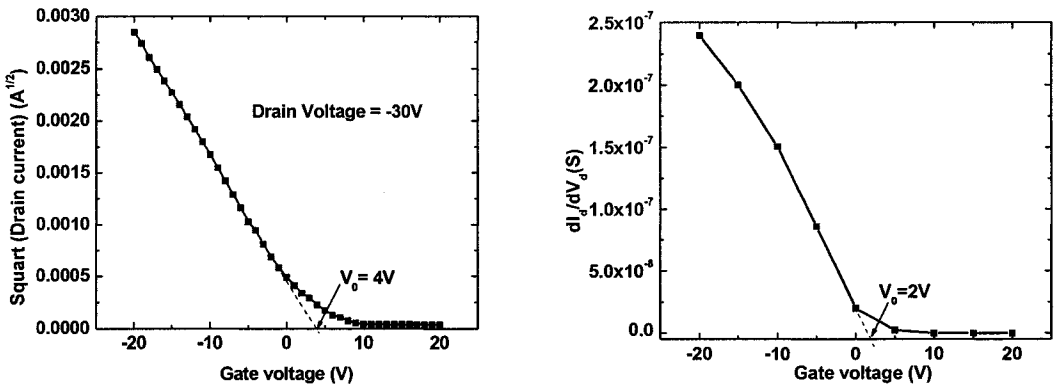
Given the gate capacitance of 34.5nF/cm^2, the injected charged density at V_g = -10V is 2.1 $\times 10^{12}$/cm^2 according to $Q = C_i V_g/q$, where Q is the charge number per cm^2, C_i is 34.5nm/cm^2 and q is the electron charge. Assuming the injected charges are confined to 20Å [10] , which is based on the fact that most of the accumulated charges are located within about one to two monolayers near insulator-semiconductor interface, the hole charge density is estimated to be 1.1 $\times 10^{19}$cm^{-3}. Next, from the ratio of the channel conduction in the linear region at V_g = -10V and V_g = 0V, the hole density at V_g = 0V, which approximately equals the residual doping concentration, is calculated to be approximately 2 $\times 10^{17}$cm^{-3} throughout the 20nm P3HT layer.

As described in Chapter Two, the mobility values in the saturation regime and the linear regime are obtained from Equations 2-10 and 2-11, respectively. In the saturation regime, $I_d^{1/2}$ is plotted against V_g in Figure 4-3a, giving rise to a threshold voltage and mobility of 4V and 0.016 cm^2/Vs, respectively. In the linear regime, the threshold voltage is 2V and the mobility is 0.007 cm^2/Vs, which are extrapolated from the dI_d/dV_d vs.V_g data as shown in Figure 4-3b. In the both curves shown in Figure 4-3, the slope determines the mobility, and the threshold voltage is read from the x-intercept.

The on/off current ratio and the subthreshold slope are the other two important device parameters, and can be determined from the device transfer characteristics. In the saturation region, the device has an on/off current ratio of 6 $\times 10^3$ and a subthreshold slope of 3.3V/dec.

One can see that a considerable difference exist between the threshold voltage V_t and the turn-on voltage V_{to}, which is the gate voltage where the drain current starts to increase exponentially. In the saturation regime, V_t is 4V and V_{to} 10V, giving $V_{tto}=V_t - V_{to}$

to be 6V. This difference was attributed to the trap states in the bandgap and therefore could serve to estimate the trap density N_{trap} [71]. Using the equation $N_{trap} = C_{ox}V_{tto}/q$, where C_{ox} is the oxide capacitance and q is the electron charge, one can obtain a trap density of $\sim 6 \times 10^{17} cm^{-3}$.



(a) (b)

Figure 4-3 (a) $I_d^{1/2}$ vs. V_g in the saturation regime and (b) dI_d/dV_d vs.V_g in the linear regime.

As noted in Chapter Two, the dependence of the field effect mobility on the gate voltage is quite typical in organic semiconductors due to the trapping effect, which has been studied in FETs with active layers of sexithiopene [72] and pentacene [73]. From the super linear $I_d - V_g$ characteristics in the linear region in our P3HT FETs, a gate-voltage dependence of mobility is expected according to Equation 2-9. However, this could not been identified using the above extraction method that assumes a constant mobility. Using Equation 2-12, the gate-voltage dependent mobility can be observed, as illustrated in Figure 4-4. We notice that the mobility grows with the increasing negative voltage and then become almost constant at high gate voltages. However, a clear relationship between gate voltage and mobility still can not be drawn before we take into

account of the contact series resistance that has been found to significantly affect OFETs' device characteristics.

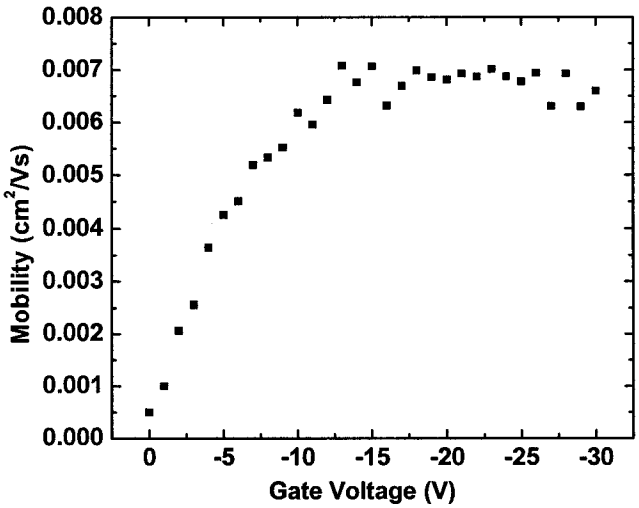


Figure 4-4 Mobility versus the gate voltage in P3HT FETs without considering the contact resistance.

Accounting for the contact series resistance, the field effect mobility can be corrected using Equation 2-16, which is rewritten as

$$\frac{g_d}{\sqrt{g_m}}\sqrt{\frac{L}{w}\frac{V_d}{C_i}} = \sqrt{\mu}(V_g - V_0) \qquad (4\text{-}1)$$

Then the corrected mobility is plotted as a function of the gate voltage V_g in Figure 4-5. For comparison, the uncorrected mobility curve is also presented. It can bee seen that the corrected mobility is larger than the uncorrected value by as high as 4 times and it has almost a linear relationship with the gate voltage. This will be described later.

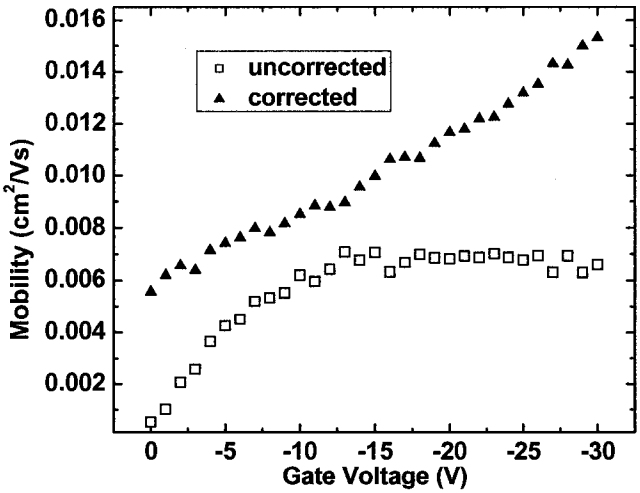


Figure 4-5 Mobility versus gate voltage corrected for the contact series resistance.

Based on the corrected and uncorrected mobility, the contact series resistance can be estimated according to the following equation

$$R_p = \frac{1}{g_d} - \frac{L}{w\mu C_i (V_g - V_0)} \tag{4-2}$$

which is recalled from Equation 2-17. Figure 4-6 shows the estimated contact series resistance as a function of the gate voltage. It suggests that the contact series resistance can be tuned by the gate voltage. This should be related to the bottom-contact structure. The injection of charge carriers occurs near the semiconductor-insulator interface, where the accumulated charges are located. A higher gate voltage induces a higher density of the accumulated charges, which in turn reduces the charge injection barrier at the S/D contact. Thus, we see the contact series resistance decreasing with the increasing gate voltage.

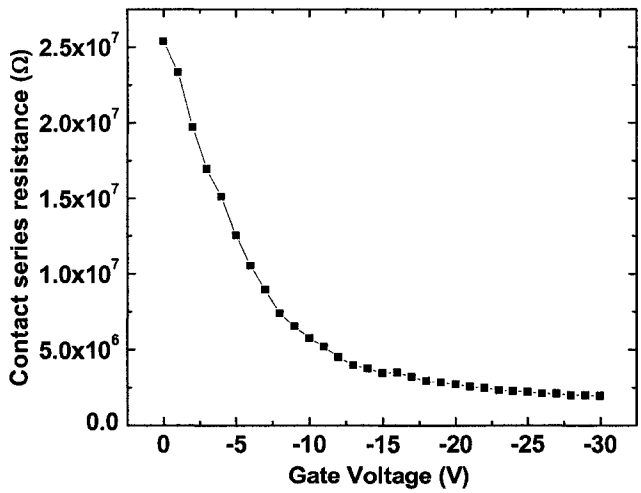


Figure 4-6 Contact series resistance as a function of the gate voltage.

4.3.2 Gate Voltage Dependent Mobility

As illustrated in Figure 4-5, the corrected mobility has almost a linear relationship with the gate voltage. It is consistent with the multiple traps and release (MTR) model, which splits the gate induced charges Q_{tot} into the trapped charges Q_f and the free charges Q_f [61]. The free charge is the effective portion that generates the channel conductance. The field effect mobility is thus related to the ratio $\theta=Q_f/Q_{tot}$. Increasing the gate voltages makes more traps to be filled and higher density of free charges. It leads to an increasing θ and thus an increasing mobility. When the gate voltage is so high that $Q_f >> Q_t$, then θ approaches unity and the mobility saturates. This has not been seen under the currently investigated biasing conditions. As mentioned in the second chapter, the gate voltage dependence of mobility could be expressed in a power law

$$\mu = \alpha(V_g - V_0)^{\beta} \tag{4-3}$$

where α is a constant, V_0 is the fitting threshold voltage. From the excellent fit as shown in Figure 4-7, we obtained $\alpha = 1.6 \times 10^{-4}$, $V_0 = 21V$ and $\beta = 1.15$.

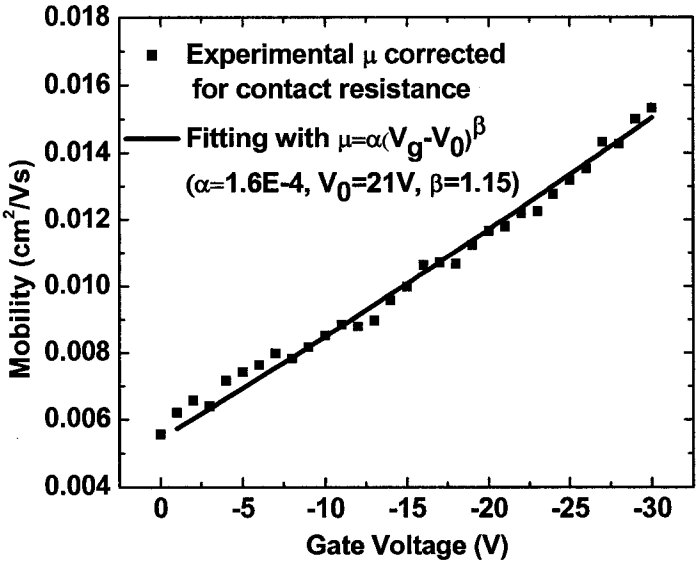


Figure 4-7 Mobility versus gate voltage.

4.3.3 Temperature Dependence of Mobility

The mobility of semiconductors is dependent on the operating temperature. As illustrated in Chapter Two, in a band-transport semiconductor such as silicon, the mobility is decreased by increasing temperature due to carrier scattering by thermal lattice vibrations. While in a polymeric semiconductor, the carrier transport is mainly through the hopping process assisted by thermal lattice vibrations, therefore the mobility normally increases with the increasing temperature. This temperature dependence of mobility has been investigated in organic semiconductor, such as, sexithiophene [8]. The mobility can vary up to three orders of magnitude from low temperature (30K) to room temperature (300K) [61]. In this work, our devices are studied over the temperature range from 300 to 560K. As illustrated in Figure 4-8, the temperature dependence of mobility

experiences two stages. First the mobility increases with the increasing temperature up to 380K, and then it decreases gradually with the further increasing temperature. Here, the mobility has been corrected for the contact series resistance. This temperature dependence of mobility can be explained as follows. In an amorphous semiconductor system, the lattice vibrations assist the charge carriers to move. Increase in temperature results in the increase of the mobility as illustrated by the first stage (T < 380K). In the meantime, we can imagine that when the lattice vibrations are so strong, due to a sufficiently high temperature, that carrier scattering could become important. Then we would see a decreasing mobility, for instance, when the temperature is higher than 380K in our study.

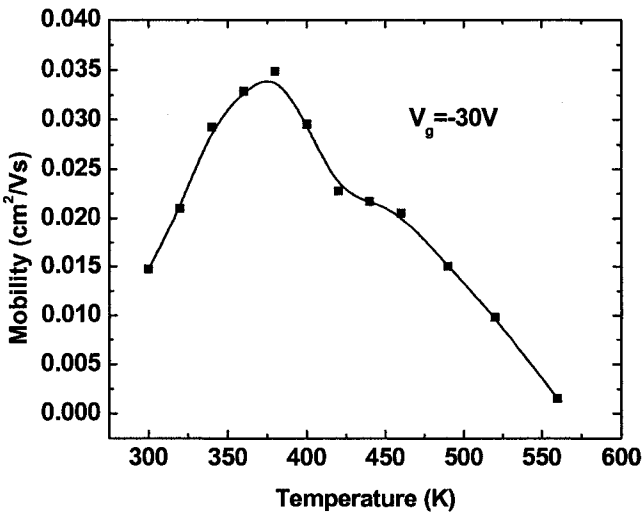


Figure 4-8 Mobility versus the operation temperature.

The other two important parameters, such as, the threshold voltage and on/off ratio are also investigated. Figure 4-9 (a) shows that the threshold voltage gradually shifts to the negative direction with the increasing temperature up to 440K. Figure 4-9(b) exhibits the temperature dependence of the on/off ratio, showing that a lower on/off ratio

corresponds to a lower temperature. These phenomena could be explained by the stability of the P3HT FETs in air, which has been extensively studied in terms of the effects of oxygen and the humidity. In the normal ambient (i.e. air), it is believed that oxygen reacts with P3HT increasing its doping level, and water molecules could form a dipole layer at the insulator-P3HT making the transistor harder to be turned off [16]. According to Ref [16], P3HT FETs are more sensitive to humidity than to oxygen. This could explain our results. When the temperature is increased, oxygen could more effectively react with the P3HT. On the other hand, the concentration of water molecules reduces with the increasing temperature. The effect of the later process is stronger, thus resulting in the negative shift of the threshold voltage and increasing on/off ratio. But as the temperature increases, the concentration of water molecules is decreasing, leading to a reducing effect on the P3HT FETs. At the same time, the effect of the oxygen becomes increasingly important with increasing temperature. This translates into the observation that when the temperature is higher than 440K, the threshold voltage shifts to positive direction and the on/off ratio decreases with the increasing temperature.

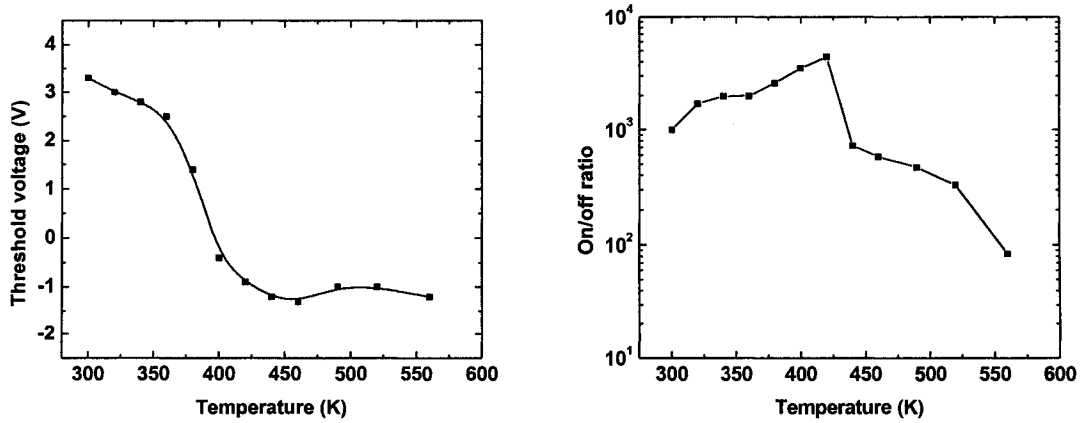


Figure 4-9 (a) Threshold voltage and (b) on/off ratio versus temperature in the linear region (V_d = -3V).

4.3.4 Hysteresis

The hysteresis is normally depicted by different threshold voltages for the sweep from positive to negative bias and in the reverse direction [74]. Although they have been ignored in most cases, the hysteresis effects occur usually in organic devices. The exact mechanism for the hysteresis effect is not certain yet. The hysteresis effect observed in MIS capacitors based on P3HT was attributed to carrier trapping and/or migration of dopants [8]. Scheinert et al. attributed the hysteresis effect to the interface charges arising from the possible oxidation of the active polymer [74]. All P3HT FETs under investigation demonstrated hysteresis effects in our experiments. By fixing drain voltage at -40V, the transfer characteristics of a P3HT FET with the gate voltage swept from -30 to 20V and from 20 to -30V are shown in Figure 4-10. A clear hysteresis window arising from a significant threshold voltage shift is observed.

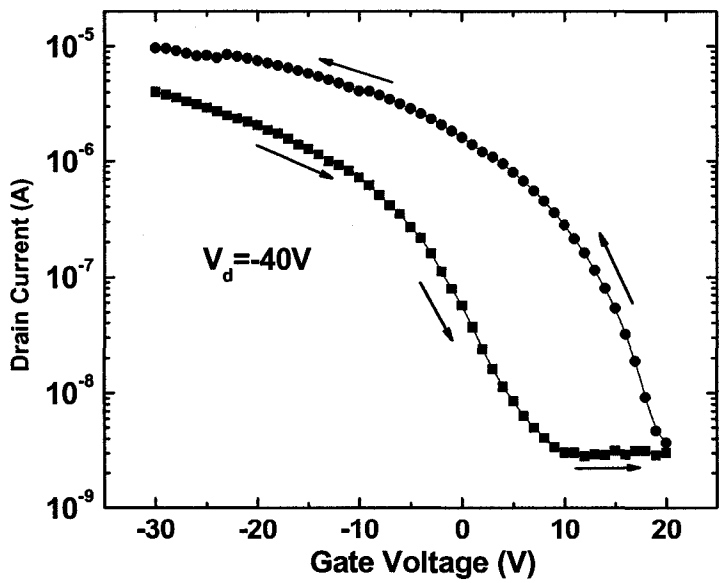


Figure 4-10 Hysteresis behavior in a P3HT FET. Arrows represent the gate voltage scan directions.

As depicted in Chapter Two, the hydroxyl groups (SiOH) present on the SiO_2 surface were suggested to be mainly responsible for this hysteresis effect. The SiOH groups could trap the electrons that are induced by positive gate biases, generating immobile SiO^- ions, equivalent to applying a negative gate voltage [32]. It results in a positive shift of the threshold voltage when the gate bias is swept from positive to negative as compared to the reverse sweep direction.

The above argument could be verified by the following experiments, where the starting gate voltages are varied when sweeping the transfer characteristics. For example, with the drain voltage fixed at -40V, we chose the starting gate voltages to be -10, 0, 5, 10 and 20V, respectively, and all sweeps ended at -30V. As illustrated in Figure 4-11, the first two curves almost overlap, but as the starting gate voltage increases to positive, the corresponding curves progressively shift to the positive direction.

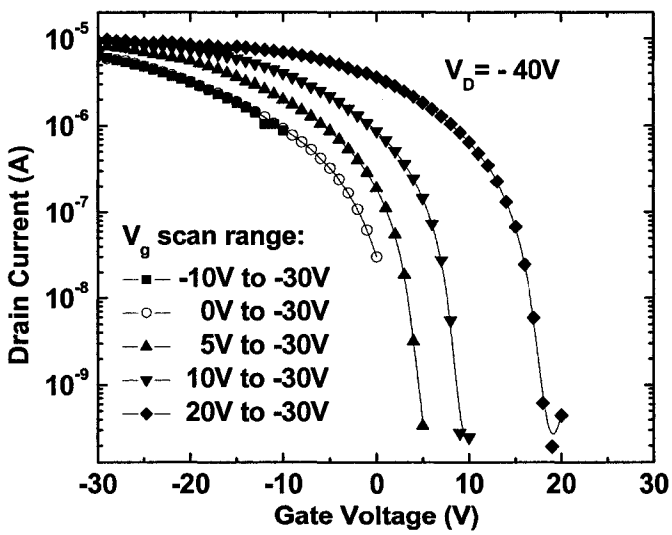
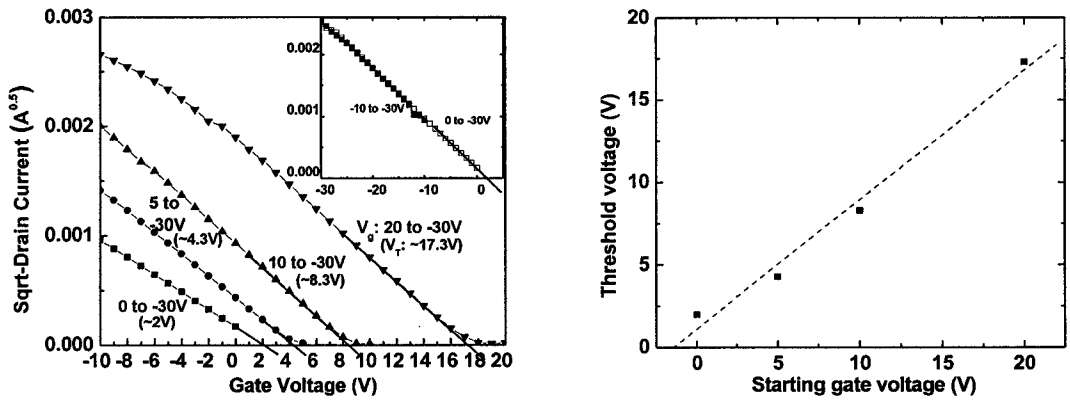


Figure 4-11 Transfer characteristics of a P3HT FET starting with various gate voltages.

By manipulating the data in Figure 4-11, the threshold voltages can be determined as illustrated in Figure 4-12. In the inset of Figure 4-12a, the sweeps that start from -10 and 0V have the same threshold voltage. However, when the starting gate biases are positive, the threshold voltage has a linear relationship with the amplitude of the starting gate biases. Therefore it could be assumed that hysteresis effect arises not from the negative but from the positive gate stress. The linear relationship demonstrated in Figure 4-12b is consistent with the above "electron-trapping" argument. When a sweep starts from a more positive gate bias, a higher density of electrons is induced near the P3HT-SiO_2 interface and trapped by silanol groups. Correspondingly, more immobile SiO^- ions are generated, moving the threshold voltage to more positive value. A slope of close to 1 in Figure 4-12b implies that the main part of the gate-induced electrons is trapped by the silanol groups. This is consistent with the phenomenon that P3HT FETs shows no n-channel activity, if no pretreatment is made on SiO_2 surface.



(a) (b)

Figure 4-12 (a) Square root of drain current versus gate voltage of the P3HT FET under various gate sweep conditions and (b) threshold voltage versus the starting gate bias.

4.4 Summary

P3HT deposited from solution offers great potential for low-cost manufacturing of organic electronics. The performance of the P3HT FETs not only depends on P3HT itself, but also significantly on other issues such as S/D contact, and P3HT-insulator interface, and optimizing them may lead to higher performance of the P3HT FETs. The temperature dependence of mobility implies that the charge transport in P3HT could be depicted by the hopping process. The mobility that has been corrected for contact resistance shows an approximately linear relationship with the amplitude of negative gate bias. It is the result of trapping effect, which could be explained by the MTR models. The hysteresis effect observed in the investigated devices can be attributed to the silanol (SiOH) groups that trap gate-induced electrons and form immobile negative ions at the P3HT-SiO_2 interface, leading to the positive shifts of the threshold voltages.

CHAPTER FIVE

MODELING AND SIMULATION OF P3HT FET

5.1 Introduction

As discussed earlier in Chapter One, OFETs technology has progressed very fast in recent years. Understanding of the device operation and the fundamental issues was important for the progress. An adequate understanding of the device operation normally relies on numerical simulation and modeling, by which the measured data were analyzed. Recently, numerical simulations using technology computer aided design (TCAD) simulator have been seriously carried out to describe the behaviors of OFETs with various emphasis such as, bulk traps effect [57] [75] [76] [77], field dependent mobility [78] [79], device structures (i.e. bottom contact or top contact) [80], S/D contact [81] [82] and channel length dependence [83], etc. Comprehensive study was conducted considering various effects simultaneously [84]. These numerical simulations were typically based on the drift-diffusion (DD) model, which does not depend on the type of the transport mechanism, and thus is also valid in the case of hopping transport in organic material system [85].

The P3HT thin films utilized in our work were deposited by the spin coating process. Despite the relatively well-ordered structure as a result of self-organization in P3HT, the polymeric thin film is basically of an amorphous or polycrystalline nature. A

great number of defects in this material could give rise to a large density of traps within the bandgap. These trap states exert strong effects on the OFETs' device characteristics by trapping mobile carriers located within the channel, which is evidenced by a significant difference between the turn-on voltage and threshold voltage as described in Chapter Four. Meanwhile, interfacial charges may also be introduced during the formation of P3HT thin film. They could have a similar role as the gate voltage to induce additional carriers in the channel, along with the unintentional doping of P3HT, generating a significant level of drain current even at zero gate voltage. The contact resistance was also found to be important as described in Chapter Six. In order to gain a comprehensive understanding of the P3HT OFETs made in our experiment, numerical simulation is carried out in the following section considering these effects. Taurus-device (Synopsys®) simulator is employed to simulate the device characteristics, and obtain results to compare with the experimental data.

5.2 Description of the Models

Our simulation of P3HT FET is based on the DD model. The Taurus-Device simulator self-consistently solves the two-dimensional Poisson's equation, together with hole and electron current continuity equations. The Poisson's equation is solved for the electrical potential

$$\varepsilon_r \varepsilon_0 \nabla^2 \varphi = -q(p - n + N_D^+ - N_A^-) - \rho_S \qquad (5\text{-}1)$$

where ϵ_0 and ϵ_r are the relative and vacuum permittivity, respectively, ϕ is the intrinsic potential, q the elementary charge, p and n are hole and electron density, respectively, N_D^+ and N_A^- are ionized donor and acceptor concentrations, respectively, and ρ_s is the surface charge density. The electron and hole continuity equations are

$$\frac{\partial n}{\partial t} = \frac{1}{q}\vec{\nabla}\cdot J_n - U_n \tag{5-2}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\vec{\nabla}\cdot J_p - U_p \tag{5-3}$$

where U_n and U_p are net electron and hole recombination, respectively. Both electron and hole current density, respectively, J_n and J_p, involve drift and diffusion current and are related to the quasi-Fermi potential ϕ_{Fn} and ϕ_{Fp}

$$\vec{J}_n = -qn\mu_n\vec{\nabla}\varphi_{Fn} + qD_n\vec{\nabla}n = qn\mu_n\vec{E}_n + qD_n\vec{\nabla}n \tag{5-4}$$

$$\vec{J}_p = -qp\mu_p\vec{\nabla}\varphi_{Fp} - qD_p\vec{\nabla}p = qn\mu_n\vec{E}_p + qD_p\vec{\nabla}p \tag{5-5}$$

where μ is the mobility and D the diffusivity, the electron and hole concentration n and p are given by

$$n = n_i \exp\frac{\varphi - \varphi_{Fn}}{\phi_T} \tag{5-6}$$

$$p = n_i \exp\frac{\varphi_{Fp} - \varphi}{\phi_T} \tag{5-7}$$

with

$$n_i = \sqrt{N_C N_V}\exp\frac{-E_g}{2kT} \tag{5-8}$$

where n_i is the intrinsic carrier concentration, ϕ_T is the thermal voltage, N_C and N_V are the effective density of states for the conduction band and valence band, respectively, and E_g is the energy band gap of the material. The mobility μ correlates with the diffusivity D by the Einstein relationship based on Boltzmann statistics

$$D_n = \frac{kT}{q}\mu_n \tag{5-9}$$

$$D_p = \frac{kT}{q}\mu_p \tag{5-10}$$

where footnotes n and p indicate electron and hole, respectively. Since the investigated P3HT FETs are not characterized for the n-type conductance, the observed drain currents are from mobile holes. Thus the electron current continuity equation could be ignored. As addressed afterwards in our investigations, trapping effect is first modeled and it is then coupled with contact resistance effect.

5.3 Device Structure

The investigated two-dimensional device structure is schematically shown in Figure 5-1. The dimensions of the device were chosen to approximate those of the real devices.

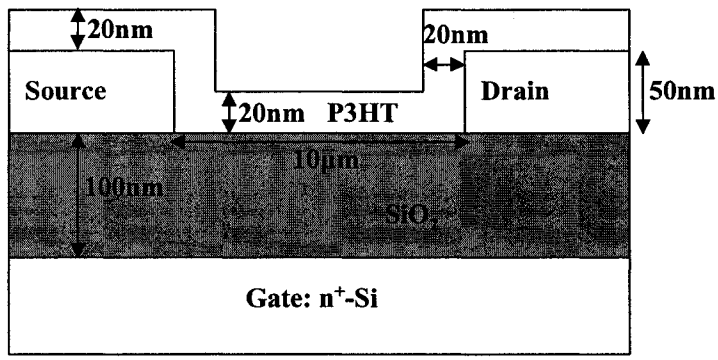


Figure 5-1 Schematic representation of the P3HT OFET structure.

The material parameters are shown in Table 5-1. Dielectric constant ϵ and effective density of states N_V and N_C of P3HT are from Ref [81], and the electron affinity (equivalent to LUMO level) and the energy bandgap are from Ref [86]. Mobility and doping concentration are obtained from the experimental results in Chapter Four. The S/D contacts are gold with work function of 5.1eV. The gate contact is n^+-Si with work

function of 4.2eV. For the mobility, the experimentally determined value is used, which is μ_p=0.016cm^2/Vs at V_d=-30V. The simulation input commands can be found in Appendix A.

Table 5-1 Basic material parameters used in simulation

	P3HT	SiO_2
ε	3.0	3.9
χ (eV)	3.0	
E_g (eV)	2.1	
N_C, N_V (cm^{-3})	2 ×10^{21}	
N_A^- (cm^{-3})	2 × 10^{17}	
μ_p (cm^2/Vs)	0.016	

5.4 Results and Discussion

In this study, all equations are solved based on the classical model (without considering quantum confinement effects).

The energy level diagram of the MIS structure under thermal equilibrium is shown in Figure 5-2, by solving the Poisson's equation. Here, E_C and E_V in P3HT are equivalent to the LUMO level and the HOMO level, respectively. E_F stands for the Fermi level. Being highly doped, n$^+$-Si as the gate electrode has a Fermi level close to E_C. Its electric property is thus similar to a metal. Due to the difference of the work function between n$^+$-Si (ϕ_m) and P3HT (ϕ_S) ($\phi_m < \phi_S$), the Fermi levels align under thermal equilibrium, leading to a slight depletion (band bending down) of the P3HT channel near the P3HT-SiO_2 interface.

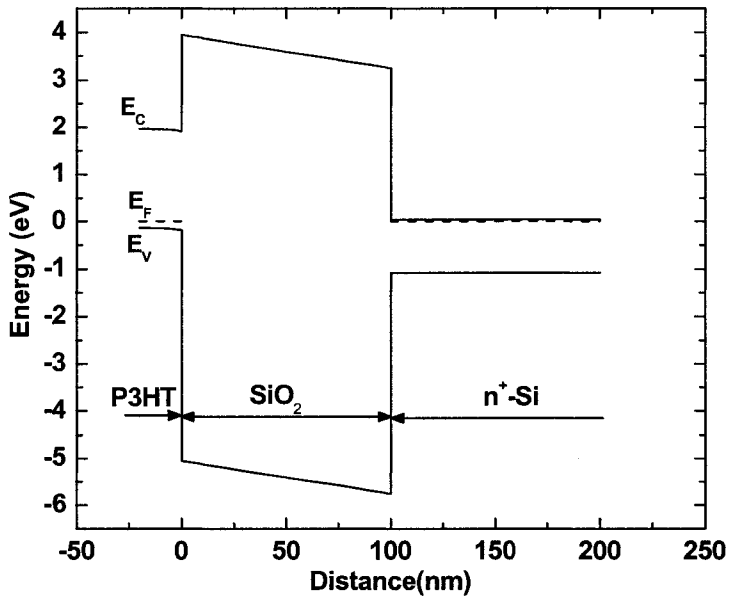


Figure 5-2 Energy level diagram of the MIS (n^+-Si-SiO2-P3HT) structure under thermal equilibrium. The cut line is chosen at the center of the device.

5.4.1 Channel Formation

Figure 5-3 shows the calculated hole concentration profiles in the P3HT layer, which is obtained from a cut-line at the middle of the channel starting from the P3HT surface. The gate voltage is -10V and both the source and drain voltages are 0V. The background doping profile is also shown. The right y-axis in Figure 5-3 shows a linear scale of the hole concentration. One can see that the charge carriers are predominately located within 2nm from the P3HT-SiO_2 interface where the carrier concentration reaches its maximum. This reveals the importance of the interface. Therefore, it is practically significant to improve the interface in order to enhance the electrical characteristics of the resulting devices.

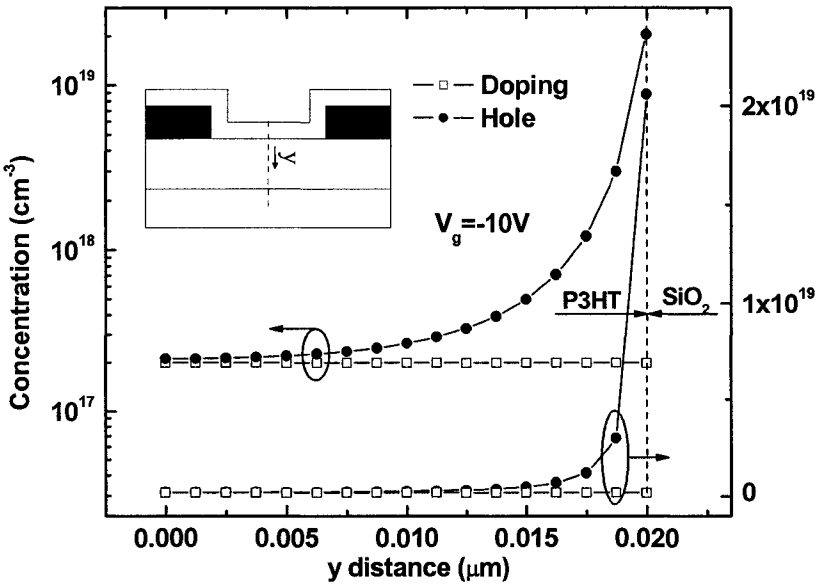


Figure 5-3 Hole concentration profile in the channel along the direction normal to P3HT-SiO_2 interface. The inset shows the cut line at the center of the channel. P3HT surface is the starting point.

The profiles of electric field and potential are shown in Figure 5-4. The cut line is also selected at the center of the device and the bias conditions are same as those in Figure 5-3. We can see that the electric potential curve is continuous when extended from SiO_2 to P3HT, while the electric field curve is discontinuous at the interface. This is due to the different dielectric constants of SiO_2 and P3HT. The distribution of electric field in P3HT channel is similar to that of holes, rapidly decreasing from the P3HT-SiO_2 interface into the bulk P3HT. This is consistent with Equation 5-1.

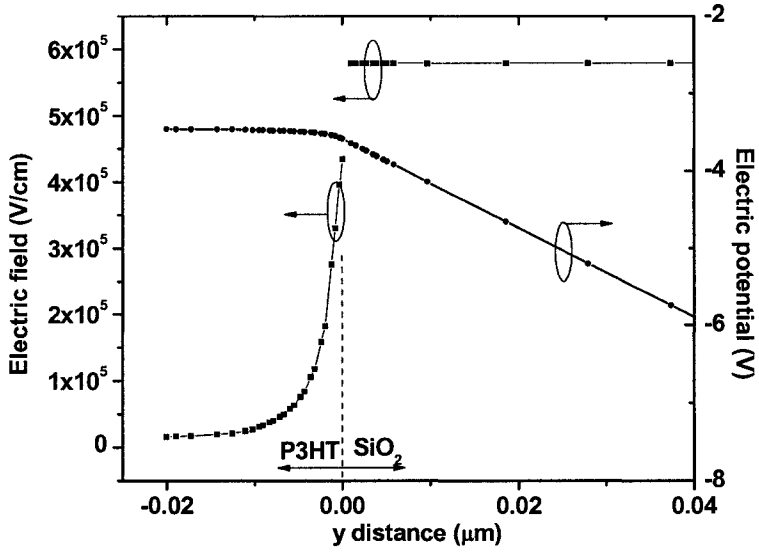


Figure 5-4 Electric field and potential profile in P3HT channel and part of SiO_2, the cut line is chosen at the center of the device. P3HT surface is the starting point.

5.4.2 Simulation with Trapping Effect

A model with a constant mobility coupled with traps is assumed. This model could be equivalent to the gate-voltage dependent mobility model, since the trapping effect, as described in Chapter Two, is responsible for the gate voltage dependent mobility. Trapping is modeled using Shockley-Read-Hall (SRH) model [43]. The trap density of 6×10^{17} cm^{-3} was estimated in Chapter Four. The knowledge of the trap distribution is not sufficient in the investigated P3HT. For simplicity, the trap level E_t (the distance from intrinsic Fermi level) was fixed at 0.5eV, approximately the half way between the valence band edge and the intrinsic Fermi level. This method was expected to give a reasonable accuracy. The detailed information and the input commands can be found in Appendix A. Figure 5-5 shows the simulation results, providing a comparison with the experimental data. A noticeable discrepancy between the simulation and experimental results is observed. We can see that all calculated values are higher than the

experimental ones. This may not mean invalid assumption of the trapping effect. It, however, led us to consider another important factor, the contact resistance, which has been identified in Chapter Four. The importance of contact resistance has also been numerically addressed for inorganic devices [87].

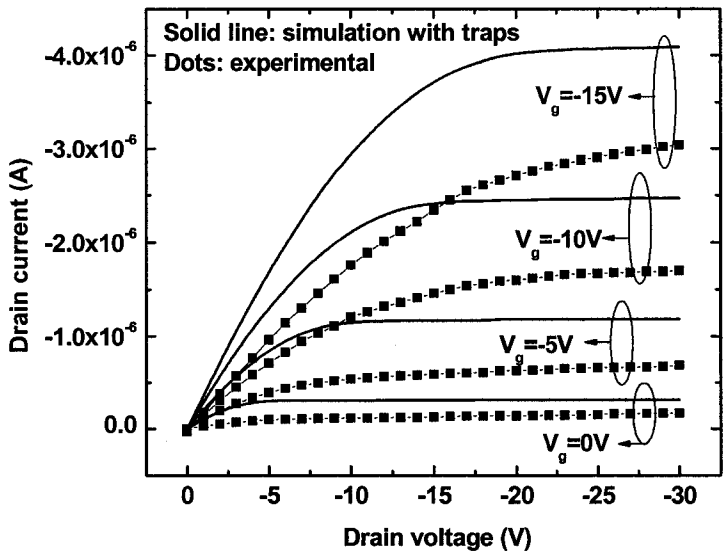


Figure 5-5 Output characteristics of OFETs including bulk traps of $6\times10^{17}cm^{-3}$ (E_t=0.5eV).

5.4.3 Simulation with Traps Coupled with Contact Resistance

Continuing with the above simulation, we additionally included the contact resistance in the model. The values of contact resistance are obtained from the results in Chapter Four (Figure 4-6). Figure 5-6 shows that a considerable voltage drop could be consumed due to the contact resistance, resulting in the effective channel voltage significantly lower than the total drain voltage. As shown in the inset in Figure 5-6, the percentage of the effective channel voltage as part of the drain voltage could be as low as 57% at V_g=-15V. Therefore, the inclusion of the contact resistance in device modeling is

important especially for devices with relatively short channel, which has resulted in a good match between the simulation and the experiment as shown in Figure 5-7.

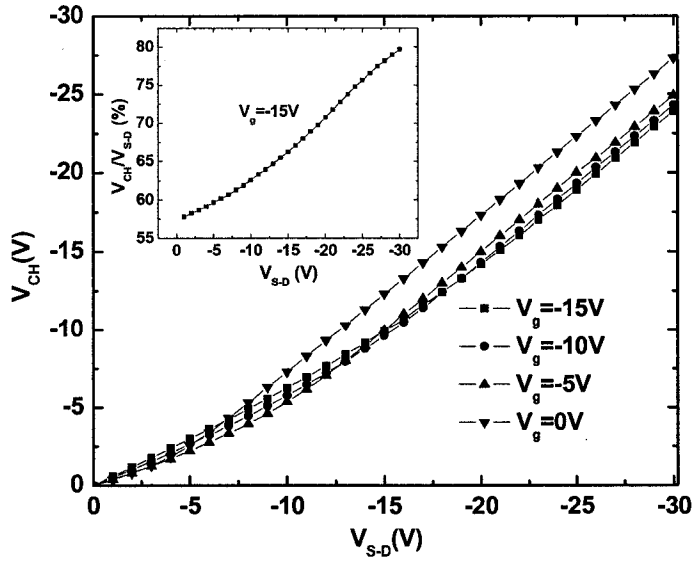


Figure 5-6 Effective channel voltage as a function of the applied S-D voltage with the effect of the contact resistance. The inset shows the percentage of channel voltage as a part of the total source-drain voltage at V_g=-15V.

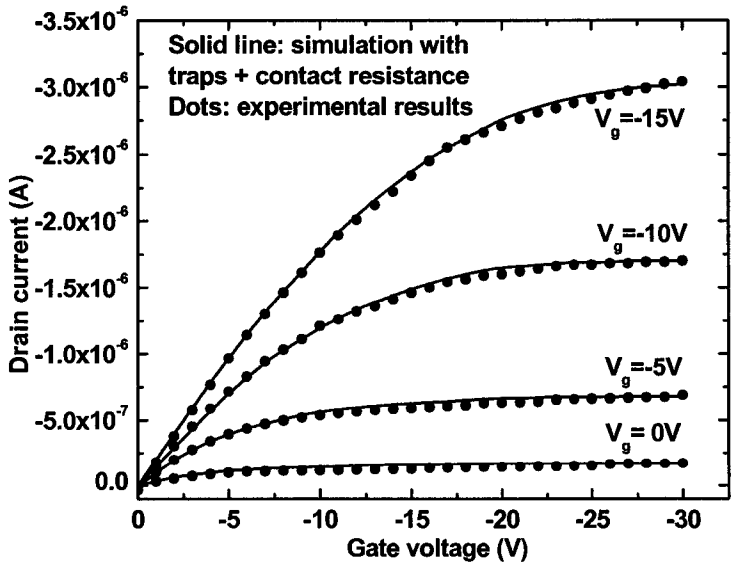


Figure 5-7 Output characteristics of OFETs including bulk traps and contact resistance.

5.4.4 Simulations on Devices with Low Contact Resistance Effect

The importance of the contact resistance effect could be verified from an opposite perspective, where a device is made with a lower contact resistance effect. The experimental work of the devices will be addressed in the next chapter [88]. Here, a brief description of this device is given. This device is made from improved S/D contact using modified PEDOT-PSS as the S/D contact material. The channel length is 20μm, which is almost two times longer than the previously simulated devices. Longer channel length, coupled with lower contact resistance results in a reduced contact resistance effect. In this simulation, trap model is included and the contact resistance is intentionally ignored. It is found that a good match has been reached between the simulation and experimental data as shown in Figure 5-8.

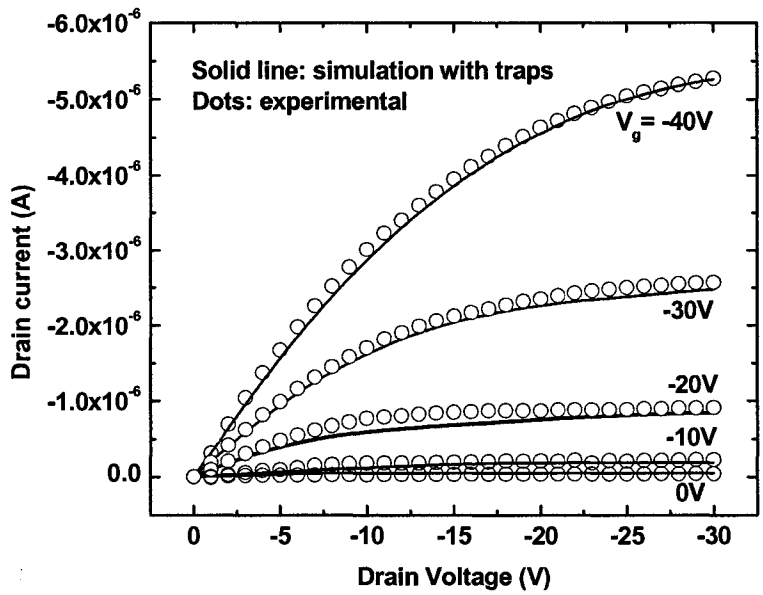


Figure 5-8 Simulation results of OFETs with low contact resistance effect including only traps model

5.5 Summary

Modeling and simulation is important for adequate understanding of the device operation. In this work, numerical simulation is carried out considering the effects of traps and contact resistance on the device characteristics. It is found that trapping effect coupled with the contact resistance could well describe the behavior of the P3HT FETs. The effect of contact resistance has been verified again from an opposite perspective, where simulation was carried out on a device with improved S/D contact and long channel length.

CHAPTER SIX

P3HT FET WITH ENHANCED PERFORMANCE

6.1 Introduction

As described in Chapter One, the improvement of OFET's performance is normally achieved through three approaches. First, create the organic semiconductor films with appropriate structures that can promote the charge transport. This can be done either by developing highly-ordered material or by optimizing deposition conditions for the organic semiconductors. For example, in the growth of pentacene fillms, the substrate temperature and deposition rate could significantly influence the grain size and crystallinity which tend to affect the carrier mobility [89]. For the solution-based P3HT, choice of solvents plays a significant role. A solvent with higher boiling point has a slower evaporation rate thus allowing the formation of P3HT films with increased crystallinity and mobility [11]. Second, optimize the electrode-semiconductor interface to increase the injection rate of the charge carriers. For instance, a metal with a high work function, such as Au, is typically used for p-channel FETs for ohmic source/drain contacts. Third, improve the characteristics of gate dielectric so that higher output currents are generated. For example, employment of high-k material is able to induce a higher density of accumulated charges in the semiconductor, and increase the output current. Treatments of gate dielectric surface could also improve the performance of the

resulting OFETs [90] [91]. In this chapter, we demonstrate simple methods for improving S/D contacts and the gate dielectric surface. As a result, the P3HT FETs' device performance is improved.

6.2 Improving S/D Contact

Since inkjet printing technique emerged as an attractive method to deposit solution based materials, solution based conducting polymers have become very promising electrode materials for high-performance OFETs. Poly(3,4-ethylenedioxythiophene) doped with polystyrene sulfonate (PEDOT-PSS) is an outstanding example [38] [92] [93]. Different from metals, which rarely form ohmic contact with the organic semiconductors [94], conducting polymer PEDOT-PSS was found to form ohmic contact with p-type organic semiconductor such as P3HT [28]. However, the performance of P3HT FETs is still limited by the relatively low conductivity of the commercial PEDOT-PSS. Therefore commercial PEDOT-PSS is modified in this work to increase its conductivity. Enhanced performance of P3HT FETs was achieved by using the modified PEDOT-PSS.

6.2.1 Experiments

The conducting polymer PEDOT-PSS (Baytron P) water solution obtained from H.C. Stack Company was mixed with polar solvent dimethyl sulfoxide (DMSO). The mixed solution was stirred continuously for 3 days at room temperature. The solution was spin coated on a glass substrate to form the film, which was then cured on a hot plate at 100°C for 60 minutes in air. The film conductivity was measured on Lakeshore Hall Effect measurement system. Controlled experiments were done on the original PEDOT-PSS.

The modified PEDOT-PSS solution was filtered through a 1μm membrane syringe filter. The original PEDOT-PSS was diluted with deionized (DI) water by a volume ratio of 1:1 to be suitable for inkjet printing. Both PEDOT-PSS materials were then patterned as S/D electrodes using inkjet printing technique. Gold (Au, 100nm thickness) in addition to titanium (Ti, 5nm thickness) was also used as S/D electrode material for comparison. All devices were made on a bottom contact structure as shown in Figure 6-1. The starting substrates are heavily n-doped silicon, which act as the gate electrodes. The gate insulator is 1000Å oxide thermally grown on silicon. The regioregular poly(3-hexylthiophene) with head-to-tail linkages greater than 98.5% (from Aldrich Chemical Company) was used as the semiconductor material. The P3HT film was deposited by spin coating technique from chloroform solution with a concentration of 1mg/ml. Film thickness was measured to be around 50nm by a Alpha-step profilometer. The FETs were completed after the P3HT films were deposited.

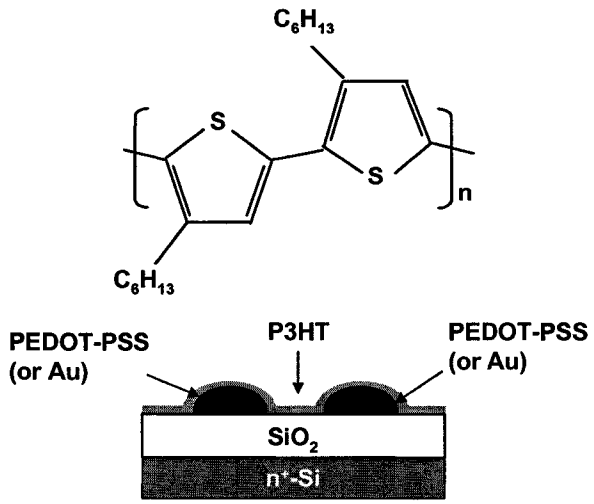


Figure 6-1 Schematic diagram of P3HT field effect transistor with inkjet printed PEDOT-PSS or gold as S/D electrodes. The chemical structure of P3HT is also shown.

Ink-jet printing work was carried out using a drop-on-demand Microdrop printer described in Chapter Three. The substrates were heated at 80°C during inkjet printing in order to enhance the evaporation rate of solvent and improve the S/D electrode patterns. Devices were characterized at room temperature in air using Keithley probe station.

6.2.2 Results and Discussion

The conductivity and stability of the electrode materials are investigated. The variations of conductivities of modified and original PEDOT-PSS as a function of time are shown in Figure 6-2. The conductivity of spin coated film from the original PEDOT-PSS solution was measured to be 0.072 S/cm. It decreased significantly within a day to 0.038 S/cm and saturated at 0.034 S/cm in a few days. The conductivity of modified PEDOT-PSS was 30 S/cm, which reduced slightly to 29.6 S/cm within a day. It further decreased at a slow rate, and almost saturated at 20.8 S/cm after 60 days.

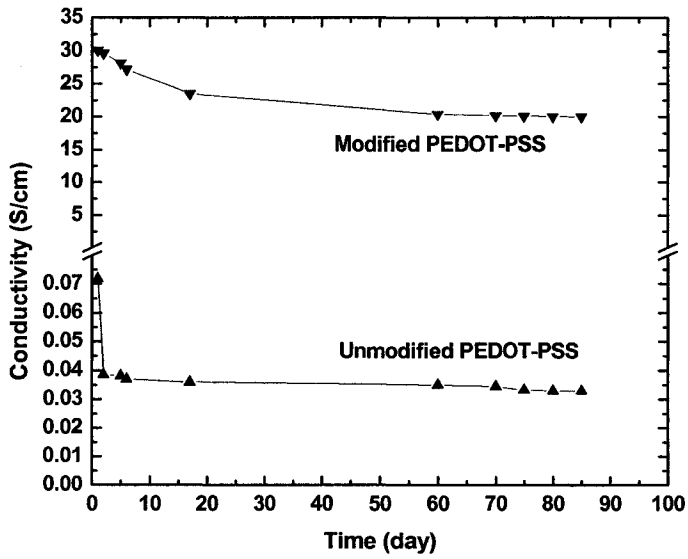


Figure 6-2 The variations of conductivities of the modified and unmodified PEDOT-PSS as a function of time in air at room temperature.

Inkjet printing of PEDOT-PSS solution requires the substrate to be heated at a temperature ranging from 80 to 100°C. Therefore, the aging of the conductivity of the modified PEDOT-PSS was investigated under thermal stress. It was monitored from a resistor made of the modified PEDOT-PSS film. Figure 6-3 illustrates that the resistance increases slowly with the time. The conductivity decreased 10% after heating at 100°C for 200 minutes in air.

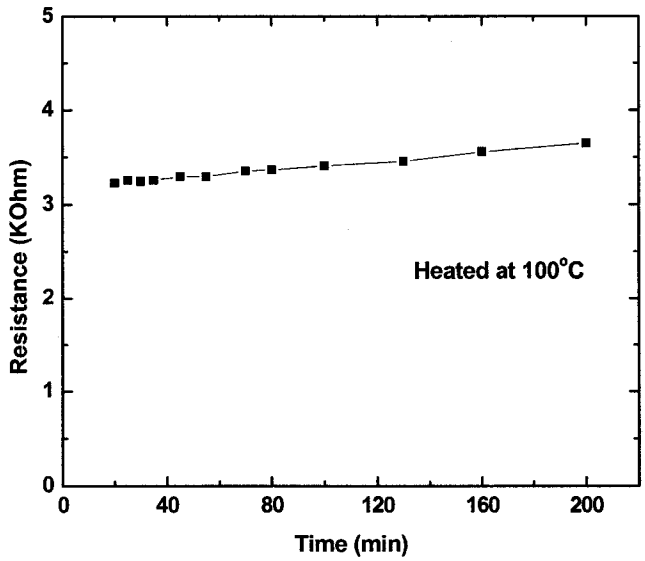


Figure 6-3 The variation of resistance of a modified PEDOT-PSS resistor as a function of time. The resistor was heated at 100°C in air.

To summarize, the enhanced conductivity of modified PEDOT-PSS exhibits long term stability at room temperature and short term stability at high temperature (100°C) in air. Both of these properties enable the modified PEDOT-PSS to be the material of choice for the S/D electrode contacts.

Figure 6-4 shows the output characteristics of P3HT TFTs with modified PEDOT-PSS S/D electrodes. The devices with gold electrodes show similar characteristic, while the curves from the devices with unmodified PEDOT-PSS are less smooth.

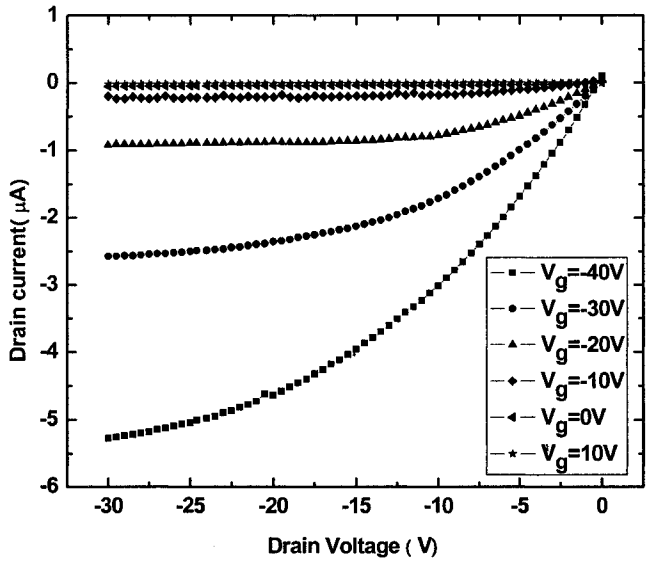


Figure 6-4 Output characteristic of P3HT TFT with modified PEDOT-PSS S/D electrodes.

Figure 6-5 shows the transfer characteristics of these devices in the saturation regime. Normalized drain currents are provided for comparison. They are obtained by dividing the actual device drain currents by the ratio of channel width to channel length (W/L). The ratios are 20, 24, and 18 for the devices with modified PEDOT-PSS, gold, and unmodified PEDOT-PSS electrodes, respectively. The on/off current ratios are found to be 46, 2.87×10^3 and 4.26×10^3 for the devices with unmodified PEDOT-PSS, modified PEDOT-PSS and gold, respectively, revealing the importance of improving PEDOT-PSS conductivity. The low on/off current ratio for the devices with unmodified PEDOT-PSS is related to the high electrode resistance as explained afterwards.

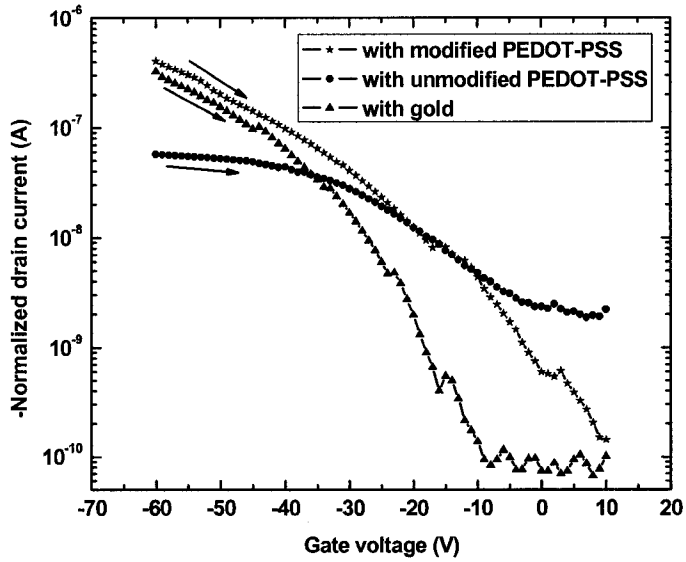


Figure 6-5 Normalized output characteristics of P3HT TFTs in the saturation regimes. Arrows represent the sweep direction of gate voltages.

The field effect mobility is first extracted using Equations 2-9 and 2-10, corresponding to the linear and the saturation regimes, respectively. As mentioned earlier in Chapter Two, the calculated mobility does not represent the intrinsic properties of materials. But it could serve for evaluating overall device performance. The threshold voltage is extracted from the (dI_{DS}/dV_{DS}) vs.V_{GS} data in the linear regime, and from the ($I_{Dsat}^{1/2}$ vs. V_{GS}) data in the saturation region as shown in Figure 6-6. Then the mobility can be determined by plugging the threshold voltage into both equations. This method is applied for all devices giving results summarized in Table 6-1. One can observe that the devices with modified PEDOT-PSS have the field effect mobility slightly higher than those with gold electrodes, and significantly higher than the devices with unmodified PEDOT-PSS.

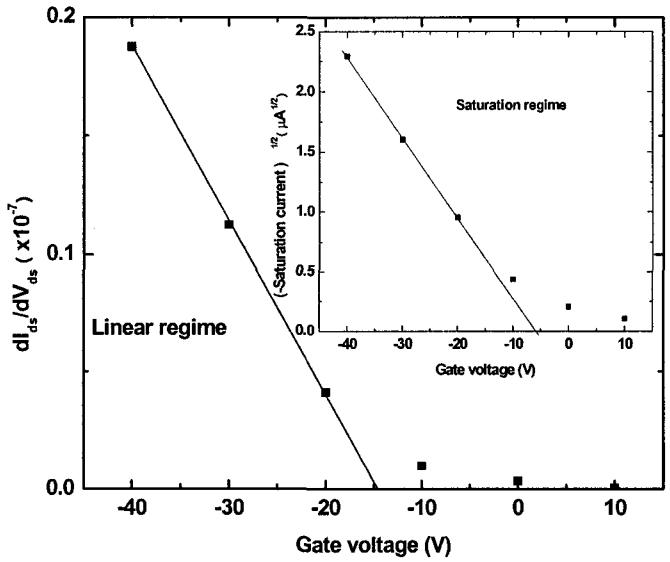


Figure 6-6 Plot of dI_{DS}/dV_{DS} as a function of gate voltage in the linear regime. The inset shows the square root of saturation current as a function of gate voltage.

Table 6-1 Extracted parameters using conventional MOSFET equations with and without considering the parasitic series resistance ('corrected' represents extraction taking into account parasitic series resistance)

	Device with modified PEDOT-PSS	Device with gold	Device with unmodified PEDOT-PSS
V_{Tlin} (V)	-15	-20	3
μ_{lin}(cm^2/Vs)	1×10^{-2}	9×10^{-3}	1.5×10^{-3}
V_{Tsat} (V)	-6	-10	8
μ_{sat}(cm^2/Vs)	1.2×10^{-2}	1×10^{-2}	1.7×10^{-3}
$V_{Tlin,}$ (V) (corrected)	-16	-22	-18
μ_{lin} (cm^2/Vs) (corrected)	1.6×10^{-2}	1.7×10^{-2}	1.5×10^{-2}
On/off ratio	2.9×10^{3}	4.3×10^{3}	46

As described in Chapters Two and Four, parasitic contact resistance has a significant effect on the OFET's behavior. Since all the investigated devices were made using the same device structures and fabrication conditions expect for the S/D electrodes. The difference in the examined device characteristics should mainly arise from the S/D

contacts. Here we use channel length series method [53] [54] [55] to extract the parasitic series resistance to verify its effect. Experiments included three groups of devices. All devices were prepared with channel width of 1000μm, while the channel lengths were varied. Figure 6-7 shows the relation between the overall resistance and channel length in the linear regime, for the devices with modified PEDOT-PSS. Y-intercepts of the fitted lines (solid lines) give the parasitic series resistance at various gate voltages. Same method is applied for the devices with gold and unmodified PEDOT-PSS. The parasitic series resistances at various gate voltages for all devices are summarized in Figure 6-8. We can see that although gold has much higher conductivity than modified PEDOT-PSS, the devices with modified PEDOT-PSS have slightly lower parasitic series resistance than the devices with gold. Parasitic series resistance difference between them changes with the gate bias. A lower difference is accompanied with a higher gate bias. This is attributed to the effect of the gate-dependent contact resistance. Lower parasitic series resistance could suggest a reduced contact barrier between modified PEDOT-PSS and P3HT. Alternatively, it might be because the contact-semiconductor transition region is probably of higher quality when using PEDOT-PSS contact. On the other hand, the parasitic series resistance in the devices with unmodified PEDOT-PSS is significantly higher than the devices with modified PEDOT-PSS. But the parasitic series resistance difference between them stays almost constant at different gate voltages. It might be due to the gate-independent electrode series resistance, which is originated from the unmodified PEDOT-PSS film with low conductivity (~0.07S/cm).

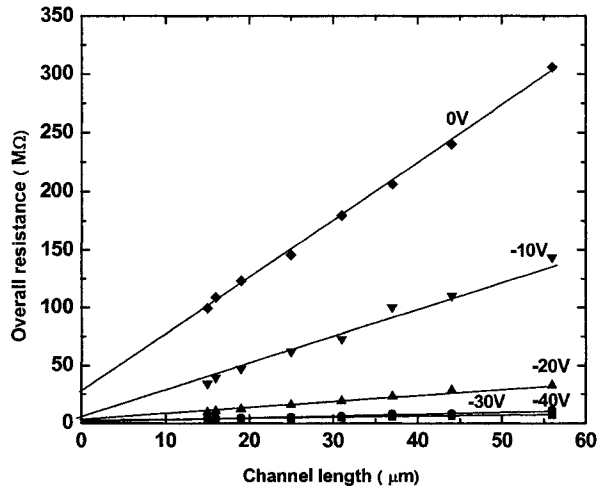


Figure 6-7 Overall device resistance as a function of channel length at gate voltages from 0 to -40V for the devices with modified PEDOT-PSS.

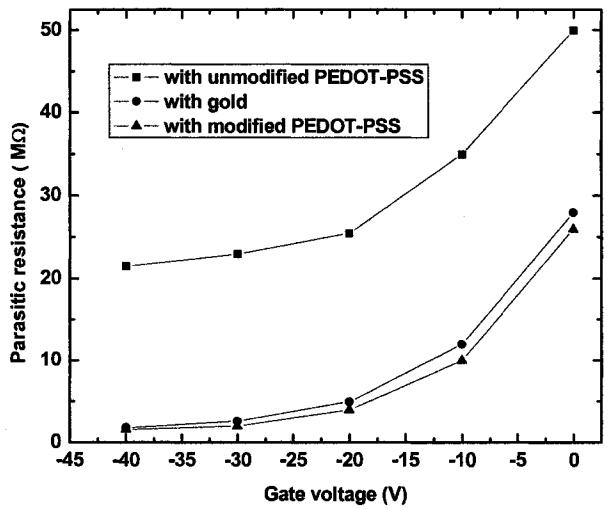


Figure 6-8 Parasitic series resistance as a function of gate voltage for the devices with modified PEDOT-PSS, gold, and unmodified PEDOT-PSS.

Taking into account the parasitic series resistance, in the linear regime, we use the following equation [54]

$$R_{on} = \frac{\partial V_{DS}}{\partial I_{DS}}\bigg|_{V_{DS}\to 0}^{V_G} = R_{CH} + R_p = \frac{L}{W\mu_i C_i (V_G - V_{T,i})} + R_p \qquad (6\text{-}1)$$

where R_{on} is the overall device resistance, R_{CH} is channel resistance, and R_p is parasitic series resistance. The intrinsic mobility μ_i and threshold voltage $V_{T,i}$ can be derived from the linear fit of sheet conductance as a function of gate voltage V_G. The slope and x-intercept of fitted line give the intrinsic mobility and threshold voltage, as shown in Figure 6-9, for the devices with modified PEDOT-PSS. The same method is also applied for the devices with unmodified PEDOT-PSS and gold. The results are presented in Table 6-1. We can see that the intrinsic mobility is quite similar for all three devices. Once parasitic contact resistances are taken into account, the corrected intrinsic mobility is increased by about 2 times in the devices with modified PEDOT-PSS and gold. While for devices with unmodified PEDOT-PSS the intrinsic mobility is nearly an order of magnitude higher than the uncorrected mobility, again indicating the significant effect of the electrode resistance.

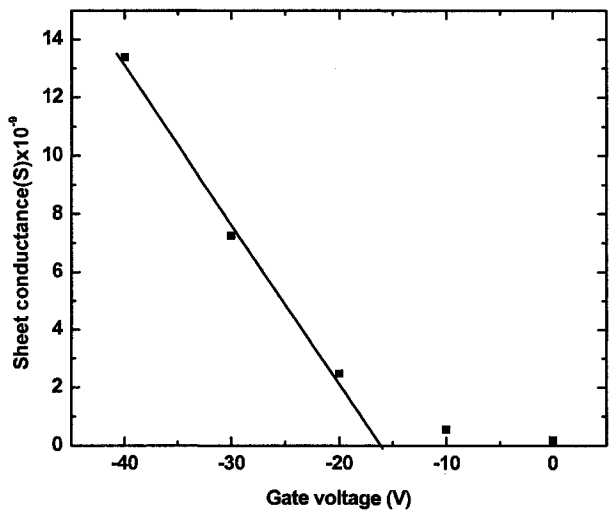


Figure 6-9 Sheet conductance of the active channel region as a function of gate voltage using Equation 6-1 for the devices with modified PEDOT-PSS.

The effect of the electrode resistance could be clearly illustrated by plotting the transfer characteristics in a linear scale as shown in Figure 6-10 for the devices with unmodified PEDOT-PSS. Sweeping the gate voltage, one can observe that the growth of the drain current is restricted at high gate voltages. This drain current restriction phenomenon could be understood when we consider overall source-to-channel resistance (R_{on}) as a function of the gate voltage. R_{on} includes three parts: electrode series resistance ($R_{S/D}$), contact resistance (R_C) and channel resistance (R_{CH}). R_{CH} and R_C are both gate-dependent and decrease with increasing negative voltage [53]. $R_{S/D}$ is gate-independent. In the devices with gold ($\sigma \sim 4.46\times10^5$ S/cm) and modified PEDOT-PSS (~30 S/cm), $R_{S/D}$ is negligible. R_{on} is strongly gate modulated at all gate voltages. Therefore no saturation phenomenon is observed. While for the devices with unmodified PEDOT-PSS (~0.07S/cm), $R_{S/D}$ is significant. At high gate voltage, R_{CH} and R_C are reduced to a relatively low level. $R_{S/D}$ becomes increasingly dominant, which results in the overall resistance decreasingly modulated by the gate voltage. Drain current grows at a decreasing rate as the gate voltage increases. Finally, it appears to saturate. This drain current restriction effect has resulted in the reduced on/off current ratio.

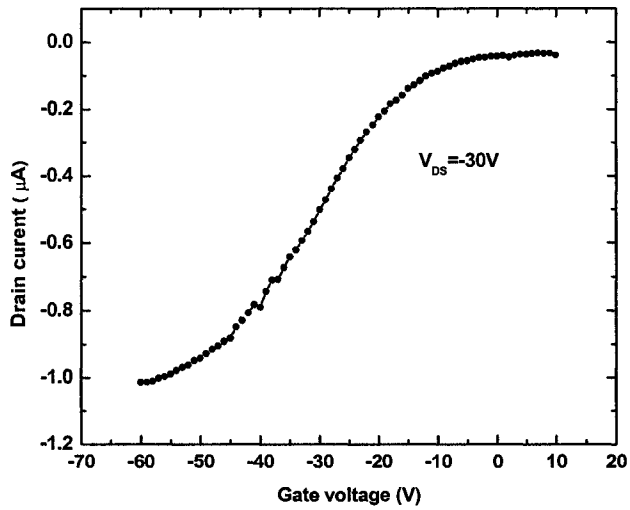


Figure 6-10 Transfer characteristics (in lin-lin scale) of P3HT TFT with the unmodified PEDOT-PSS source/drain electrodes at V_{DS}=-30V. The drain current appears to saturate at high negative gate voltage.

6.3 Improving the P3HT-SiO_2 Interface

The performance of OFETs depends largely on the gate dielectric-semiconductor interface. Treatment of SiO_2 gate dielectric prior to organic semiconductor deposition has been found to be an effective way of improving performance of OFETs [10] [95]. Most studies have focused on the growth of a self-assembly monolayer on the SiO_2 surface to passivate the SiOH groups, which were believed to be a key root cause limiting the OFET's characteristics [32]. The following work presents that significantly improved P3HT FETs can be obtained by simply annealing the gate dielectric SiO_2 before the P3HT film is deposited.

6.3.1 Experiments

The devices were made following a procedure similar to that described in Chapter Four. Highly n-doped silicon wafers having thermally grown 1000Å thick oxide

were used as the starting substrates. A layer of 500Å Au/30Å Ti was deposited by sputtering and then patterned by a lift-off process for S/D electrodes. The highly n-doped silicon acts as the gate electrode and SiO_2 as the gate dielectric. The prepared samples were then annealed at 300°C in vacuum for 4 hours, followed by the deposition of the P3HT films on SiO_2. The P3HT films having thickness of about 20nm were cast from a p-xylene solution (0.5mg/ml) using spin coating technique. A set of P3HT FETs were then finished. Without annealing the SiO_2 substrates, the other set of P3HT FETs were also prepared. All devices were measured on a Keithley probe station in air at the room temperature. These devices have a channel width of 500 μm and channel length of 50 μm.

6.3.2 Results and Discussion

Figure 6-11 shows the transfer characteristics of both devices. With the drain voltage fixed at -30V, where the devices operate in the saturation region, the gate voltages were swept from -20 to 20V, then swept back. Both devices show hysteresis effect. But an apparently wider hysteresis window is observed in the devices with the non-annealed SiO_2. Device parameters such as threshold voltage, field effect mobility, subthreshold slope, and the on/off ratio were extrapolated from the data in the reverse scan (20V to -20V). The results were summarized in Table 6-2. Annealing the SiO_2 was found to improve the device performance. The saturation mobility increases from 0.01 to 0.026 cm^2/Vs, the threshold voltage shifts closer to zero, subthreshold slope decreases from 3.7 to 1.9 V/dec and the on/off ratio increases by 4 times. The difference in the characteristics between the two investigated devices is related to the properties of SiO_2 surface. According to Sneh et al, the dehydroxylation ($2SiOH \rightarrow Si\text{-}O\text{-}Si + H_2O$) of the SiO_2 surface proceeded quickly when the SiO_2 was annealed [96]. At low temperatures

(<100°C), the SiO_2 surface rapidly loses physically adsorbed or bulk molecular water, and at about 150°C and higher temperature, the condensation of hydroxyl groups occurs on the silica surface [97].

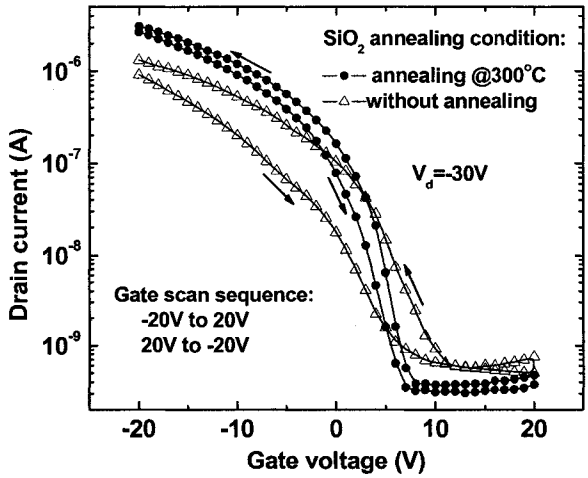


Figure 6-11 Transfer characteristics of P3HT FETs with annealed and non-annealed SiO_2

It has been described earlier in Chapter Four that the hysteresis effect is mainly attributed to the electrons trapped by the silanol groups forming immobile SiO^- ions. At the same time, the absorbed water molecules could form a dipole layer at the insulator-P3HT interface [16]. Both factors could contribute to a positive shift of the threshold voltage. Annealing SiO_2 at 300°C for 4 hours decreases both the silanol groups and the physically absorbed water molecules thus reducing the hysteresis effect, moving the threshold voltage closer to zero (see Table 6-2). The increased mobility could be due to the reduced scattering at the SiO_2 surface with less trapping sites. For the subthreshold slope, it is commonly known that its value is linked to the interfacial trap density [98]. A significantly smaller subthrehold slope in the devices with annealed SiO_2 is probably due to a smaller trap density. It should be noted that the annealing and device fabrication were carried out in air. These could lead to a reduced efficiency of dehydroxylation and

might introduce a certain level of rehydroxylation. Better device performance is possible if the device could be fabricated and characterized in vacuum. Higher annealing temperature is desirable for more complete dehydroxylation. It is possible that the P3HT FETs could be further increased.

Table 6-2 Comparison of device parameters between devices with annealed and non-annealed SiO_2.

	Without annealing SiO_2	SiO_2 annealed at 300°C (4 hrs)
Threshold voltage (V)	8.5	6
Saturation mobility (cm^2/Vs)	0.01	0.026
On/off ratio	2.3×10^3	8.2×10^3
Subthreshold slope (V/dec)	3.6	2

6.4 Summary

The performance of OFETs could be improved by various methods. In this work, improvements of S/D contacts and gate dielectric are considered. We used conducting polymer PEDOT-PSS as S/D electrodes, instead of commonly used metal such as Au. PEDOT-PSS was modified to be highly conductive leading to reduced contact resistance as compared to that of Au contacts. As a result, the performance of P3HT FETs is improved. The other improvement is achieved by simply annealing the SiO_2 gate dielectric. We attribute the device performance improvement to the reduced density of hydroxyl groups and physically absorbed water molecules on the SiO_2 surface as a result of annealing.

CHAPTER SEVEN

POLYMER MODULATION DOPED FET

7.1 Introduction

Conventional modulation doped field effect transistor (MODFET) technology provides a good approach to achieve high electron mobility of the device [99] [100] [101]. The high electron mobility is made possible by using a heterostructure which consists of two materials with different bandgaps. AlGaAs/GaAs structure is an outstanding example, which has been most extensively used and studied. AlGaAs has a wide bandagap as compared with GaAs. In AlGaAs/GaAS heterostructure, band discontinuity is present at both conduction band and valence band. Once n-doped, AlGaAs is put next to undoped GaAs, electrons will diffuse from the wide-band AlGaAs to the narrow-band GaAs, leaving behind a positive space charge region. The conduction band discontinuity and the accumulation of electrons setup a barrier to prevent the electrons from going back to AlGaAs. The diffused electrons are confined in a thin layer at GaAs side near the heterointerface and can freely move within the thin layer along the interface surface. Since the electrons are spatially separated from the donors, ionized impurity scattering is greatly reduced, resulting in field effect mobility in the thin layer almost only limited by lattice scattering. As a result, mobilities above 2×10^6 cm^2/Vs at 4K can be achieved in properly designed structures [98].

Ultrahigh speed devices made of GaAs/AlGaAs heterojunction have enabled themselves to be used for supercomputers [99].

It is worth noting that the striking device performance of MODFETs arises from the technique namely "modulation doping", which provides a perfect means of introducing electrons into conduction layer without the adverse effects of donors [99]. At present, OFET has become an extremely active research topic due to its potential for low cost manufacturing. However, they currently suffer from low carrier mobility, and therefore can rarely be used for practical applications. If the basic operation principle of the conventional MODFETs can be used for the OFETs, one may expect significantly improved device characteristics of OFETs. Here, a fundamental question needs to be answered: could "modulation doping" be valid in organic heterojunctions? As described in Chapter Two, the charge transport of an organic (or polymeric) semiconductor is described by a hopping process. Therefore, it is not clear whether the "modulation doping" as a phenomenon of band transport can still occur in organic (polymeric) semiconductor. Despite its importance, this issue has not been addressed so far. In this work, a polymer heterojunction is designed and integrated into a field effect transistor. Our observations indicate that "modulation doping" could exist in the poymer heterostructure.

7.2 Polymer Heterostructure

The polymer heterostructure is built and characterized in the configuration of a MOSFET. It is designed in such a way that "modulation doping" effect could be judged from the transistor characteristics. Two materials of different bandgaps are chosen that the one with wide bandgap has a low mobility and is intentionally doped, and the other

one with narrow bandgap has a relatively high mobility and low doping. This is analogous to AlGaAs/GaAs heterostructure. Two selected materials are P3HT for narrow band gap well layer, and Poly(9,9-dioctylfluorenyl-2,7-diyl) (PFO) for the wide band gap barrier layer. Both polymers are p-type conducting materials. The hole mobility of P3HT is normally 2-3 orders of magnitude higher than that of PFO. The highest occupied and lowest unoccupied molecular orbital (HOMO and LUMO) levels of P3HT are 5.1eV and 3.0eV giving a bandgap of 2.1eV [86], and those of PFO are 5.8eV and 2.6eV resulting in a bandgap of 3.2eV [102]. Following the work reported by Hwang et al., [102], organic molecules tetrafluorotetracyanoquinodimethane (F_4-TCNQ) is introduced to dope PFO through the co-solution method. The doping was achieved by means of charge transfer between two molecules, owing to a very high electron affinity of F_4-TCNQ (5.24 eV) [103]. The doping level, defined as the ratio between the density of F_4-TCNQ molecules and repeating units of PFO, was controlled to be around 10%. The energy level structures of two materials before contact are shown in Figure 7-1, indicating a 0.7eV of HOMO level offset between them.

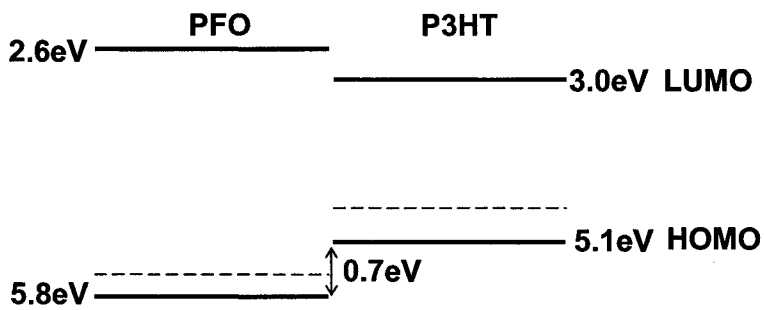


Figure 7-1 Energy level schematic diagram of PFO and P3HT before contact.

P3HT was dissolved in p-xylene at a weight ratio of 0.5mg/ml to form a solution for spin-coating. PFO and F_4-TCNQ are mixed and dissolved in chlorobenzene and ultra-sonicated overnight for complete mixing and dissolution.

7.3 Device Fabrication

As shown in Figure 7-2, devices were made on heavily n-doped silicon, which also acted as the gate electrode. A layer of1000Å thermally grown oxide served as the gate dielectric insulator. In addition, 500Å Au/30Å Ti metal layer was deposited on the SiO_2 as the S/D electrodes by sputtering and patterned by a lift-off process. Next, a 20nm thick P3HT layer was spin-coated on the SiO_2 surface and allowed to dry under vacuum at room temperature for 2 days. The P3HT FET was then finished. It was measured and recorded. Continuing on this device, a doped PFO layer was deposited over the P3HT film via a transfer method [104], which prevented the P3HT film from being attacked by the PFO solution. In this transfer method, a sodium poly(styrenesulfonate) (PSS-Na) sacrificial layer was first spin coated on a silicon wafer and dried by heating at 100°C for 1 hour, then the PFO was coated on the PSS-Na film. After drying in vacuum for 2 days, the PFO film was transferred onto the P3HT surface. Since both P3HT and PFO films were water insoluble and extremely hydrophobic, the samples were put in de-ionized (DI) water for 30 minutes to remove the PSS-Na sacrificial layer leaving the PFO film on the P3HT layer. The PFO film is about 40nm. Then the PFO/P3HT FET was finished. The PFO/P3HT FET was dried in vacuum at room temperature for 2 hours before measurement. Like the earlier measured P3HT FETs, the PFO/P3HT FETs were measured using Keithley probe station at room temperature in air.

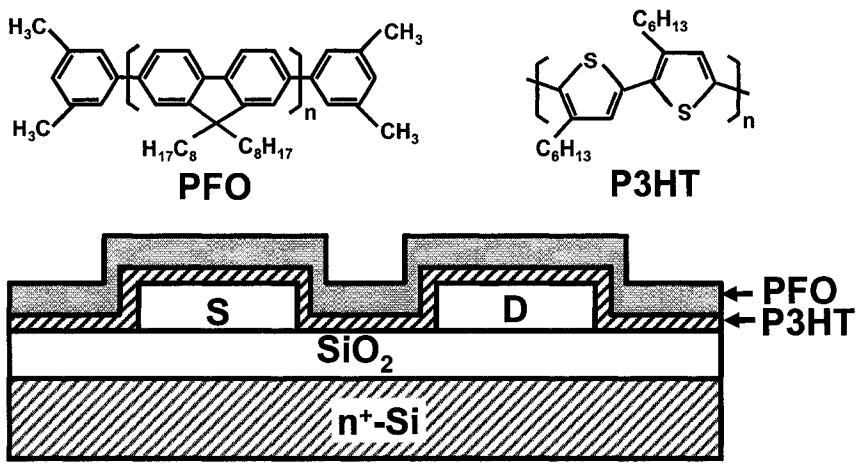


Figure 7-2 A schematic cross-section of a fabricated quantum-well polymer field effect transistor (SiO_2: 100nm, P3HT: 20nm, PFO: 40nm, S/D: 500Å gold/30Å titanium, channel length: 10μm, and channel width: 500μm). The molecular structures of PFO and P3HT are also shown.

7.4 Results and Discussion

Figure 7-3a shows the output characteristics of the P3HT FET as well as the PFO/P3HT FET. Noticeably higher drain currents are observed in the PFO/P3HT device at various gate voltages. The transfer characteristics of both devices are presented in Figure 7-3b, which also shows significantly higher drain currents in the PFO/P3HT device. The PFO layer conductance was found to be negligible, as illustrated in Fig 7-3b. The conductance was estimated from a PFO FET made in the same device configuration as the P3HT transistor.

It is apparent that the sum of drain currents from the separated P3HT and PFO layer is significantly lower than the drain current of stacked layers of P3HT and PFO. In other words, the heterojunction generates the enhanced current elements. This is a typical phenomenon of "modulation doping", which is explained as follows. The holes diffuse from the doped PFO into the P3HT where they are confined near the interface. Due to the significantly higher hole mobility of P3HT, the confined holes move much faster in the

P3HT. They accumulate at the interface leading to a high carrier density. Consequently, more current is generated than that if the carriers were transported in PFO, under the force of the source-drain electric field. Hence, the "modulation doping" translates into the observed increase of the drain current.

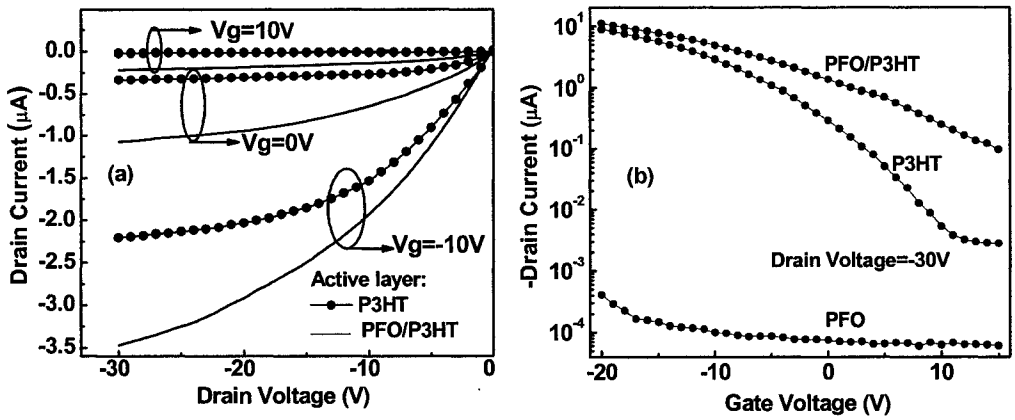


Figure 7-3 (a) Output characteristics and (b) transfer characteristics of the P3HT-only and the PFO/P3HT FETs. For comparison, the transfer characteristics of a PFO FET in the same device configuration are shown in (b).

To simplify the analysis of this polymer heterostructure, the "modulation doping" effect with the P3HT/PFO heterojunction is schematically depicted by the conventional energy band diagram as shown in Figure 7-4. The Fermi levels line up at thermal equilibrium resulting in discontinuity in the energy bands at the heterointerface. The discontinuity in the valence bands allows holes to spill over from the PFO layer into the P3HT layer, where they become trapped in the potential well. As a result, holes are confined on the P3HT side near the heterointerface. The inset in Figure 7-4 schematically shows the two dimensional hole gas in the potential well. It is these holes that result in the significantly increased current observed in the heterostructure OFETs.

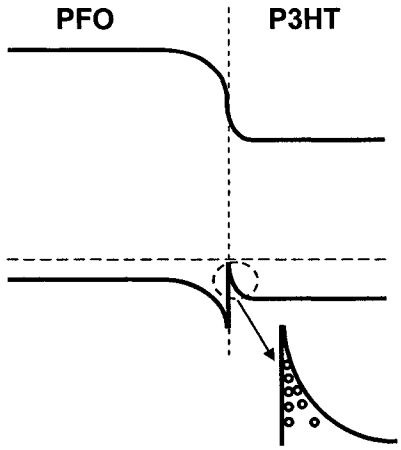


Figure 7-4 Schematic energy band diagrams of PFO and P3HT in the thermal equilibrium. The inset shows the confined holes.

Since the P3HT layer is sandwiched by the gate oxide and the PFO layer, two competing conducting channels exist in the P3HT layer. The one near the PFO/P3HT interface due to the confined holes will dominate at zero or positive gate voltages. The second one near the P3HT/SiO_2 interface arises from the injected holes induced by the gate electric field. In order to estimate the hole concentration profile in the P3HT channel under the effect of the PFO layer, two-dimensional Poisson's equation is solved by Taurus-Device simulator. The material parameters for P3HT have been described in Chapter Five; those for PFO can be seen in Figure 7-1, and the doping concentration of PFO is set at 1 $\times 10^{18} cm^{-3}$, estimated from the PFO FET results; dielectric constant used is 3, which is a typical value for a polymer material. The source and drain are grounded, and the gate is biased at -10V. The simulated results are shown in Figure 7-5. For comparison, the hole concentration profile for the device without the PFO layer is also shown. One can see that the effect of the PFO layer is mainly on the region near P3HT-PFO interface in our device. Under currently biasing condition (V_g = -10V), the hole

concentration due to the polymer hetero-junction is slightly lower than that due to the gate electric field.

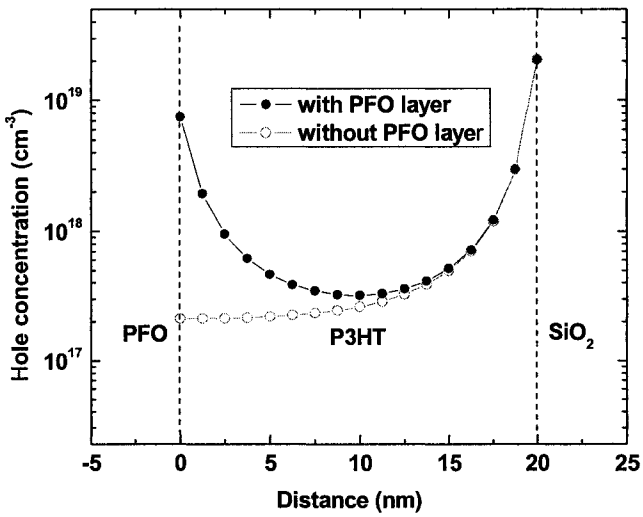


Figure 7-5 Simulated hole concentration profile in the P3HT layer with and without PFO layer in contact with it (at V_g=-10V). The cut line is chosen at the center of the device.

Figure 7-6 shows the simulated hole concentration profile in the P3HT layer as a part of the P3HT-PFO heterostructure, at V_g = 0V and -10V, and with the source and drain grounded. We can see that when a zero gate voltage is applied, the P3HT channel is dominated by the channel near the heterojunction interface, whereas, with a negative gate voltage, the gate-induced channel becomes to dominate. This indicates an increasing effect of the gate-induced channel when the gate voltage is increased in the negative direction. Therefore, we observe that the PFO/P3HT drain current gradually approaches to the P3HT drain current when the gate voltage is increased to be more negative, as shown in Figure 7-3b. It should be noted that all simulations in this study are based on the classical model. The simulated hole concentration profile and device characteristics could be different if the quantum confinement effects were considered.

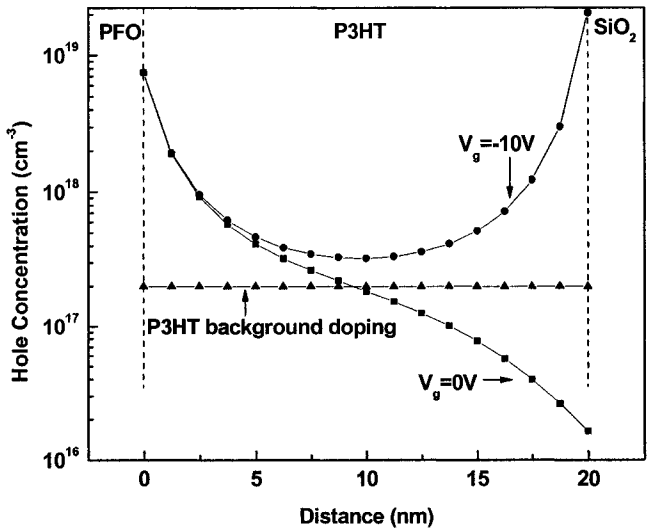


Figure 7-6 Simulated hole concentration profile in the P3HT layer in the P3HT-PFO heterojunction at different gate biases. The cut line is chosen at the center of the device.

Due to the confined holes, a higher threshold voltage was expected in the PFO/P3HT FET. From the x-intercept on the curve of ($I_D^{1/2}$ vs. V_G) in the saturation region (V_D=-30V), the threshold voltage was 11V in the PFO/P3HT FET and 6V in the P3HT FET. The field effect mobility in the saturation region was estimated using the following equation

$$I_D = \mu C_{ox} \frac{W}{2L}(V_G - V_T)^2 \qquad (7\text{-}1)$$

where I_D is the drain current, μ the mobility, C_{ox} the gate oxide capacitance per cm^2, W channel width, L channel length, V_G gate voltage, and V_T threshold voltage. The calculated field effect mobility is about 0.018 cm^2/Vs for both P3HT and PFO/P3HT FETs.

7.5 Summary

This study is to explore the potential possibility of enhancing OFET characteristics by using polymeric heterostructure as the active layer. Polymer heterojunction FETs were developed and characterized. The drain current was found to significantly increase in the PFO/P3HT transistors as compared to the P3HT devices. This increased drain current is likely from the charge carriers flowing from the wide bandgap PFO into the narrow bandgap P3HT. This phenomenon is called "modulation doping". The conventional heterojunction energy band theory is able to explain the operation of the polymer heterojunction FETs. Analyzing the fabricated devices, we found that PFO/P3HT FET showed a more positive threshold voltage than the P3HT FET. This was attributed to the confined holes in the potential well near the hetero-interface. These two devices have a similar field effect mobility of 0.018 cm^2/Vs. We expect our findings in this work could open an alternative approach for improving organic transistor's device performance.

CHAPTER EIGHT

CONCLUSIONS AND FUTURE WORK

8.1 Conclusions

In this thesis, field effect transistors composed of P3HT as the active layer have been fabricated and analyzed. Fundamental issues that could affect device characteristics, such as contact resistance, and the semiconductor-insulator interface were investigated. Hysteresis effect of the fabricated devices has been studied and possible explanation was given. Gate-voltage dependent mobility was fitted based on a reported model and explained in terms of the trapping effect. The devices have been studied with varying operation temperatures, implying hopping transport of the charge carriers.

To gain an adequate understanding of device operation, we carried out 2-D numerical simulations on Taurus-Device simulator, which self-consistently solved Poisson's equation, and current continuity equations. The simulations were implemented considering the contact resistance and traps, resulting in the simulation results to be in good agreement with the experimental data.

With the knowledge of the key issues that could limit device performance, corresponding improvements have been made. First, we aimed to improve the S/D contact. The commercial poly(3,4-ethylenedioxythiophene)-polystyrene sulfonate (PEDOT-PSS) was modified and studied. The modified PEDOT-PSS was utilized as the

source/drain electrode material in P3HT FETs, giving considerably lower contact resistance than the commonly-used gold electrodes. As a result, device characteristics were improved. Thus the modified PEDOT-PSS for S/D electrodes is a promising low-cost contacting technique. Second, we intended to improve semiconductor-insulator interface, which was done by simple annealing SiO_2 surface prior to the deposition of the P3HT layer. Consequently, device characteristics are significantly improved. The mobility is improved from 0.01 to 0.026 cm^2/Vs, on/off ratio from 2.3×10^3 to 8.2×10^3, subthreshold slope improved by approximately 2 times, from 3.6 to 2 V/dec. The hysteresis window is also reduced. The enhanced device performance could be attributed to the reduction of physically absorbed water molecules and hydroxyl groups at the SiO_2 surface upon annealing.

Polymer heterostructure OFETs have been also developed for establishing a method to fabricate new devices and the possibility to increase the device performance. The resultant device characteristics indicate the "modulation doping" effect at the P3HT/PFO heterjunction. It seems analogous to the conventional inorganic heterojunction MODFETs, which have shown strikingly high field effect mobility due to the "modulation doping" effect. This finding could open a potential way to achieve high-performance OFETs.

8.2 Future Work

8.2.1 Side Effects of Solvents

One key issue of using solution process in the fabrication of organic devices is the solvent compatibility problem. It has two aspects. First, the solvents from the subsequently layer may dissolve and damage the underlying layer. Second, the

subsequent solvents may not dissolve and damage the underlying layer, but could affect the properties of the underlying layer. The first aspect is apparent and easily identified. The second aspect is more complicated. It could result in misinterpretation of unusual device characteristics. In-depth investigation is required to find out the root causes and thus eliminate the side effects. For example, we have found that the solvent, isopropyl alcohol (IPA), did not dissolve P3HT but significantly affected the electrical properties of P3HT. Figure 8-1 shows the results from a P3HT FET before and after it is exposed to liquid IPA. It seems that IPA could dope P3HT layer and result in significantly increased current and reduced control capability of the gate on the P3HT channel.

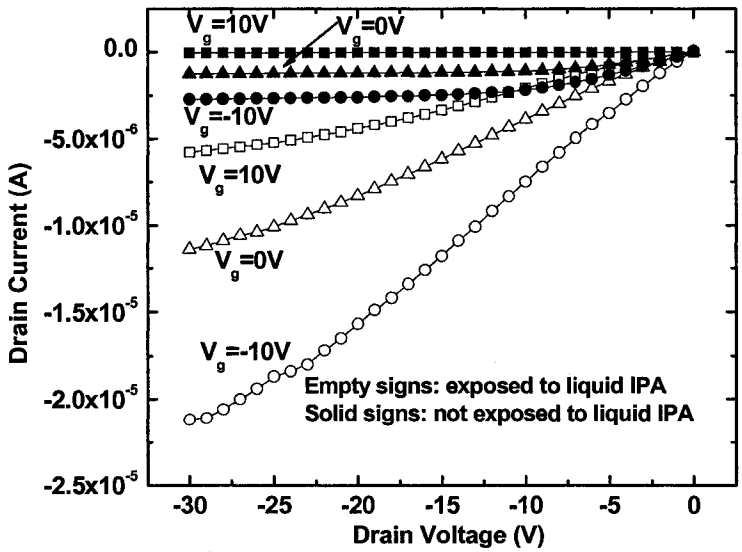


Figure 8-1 P3HT device characteristics showing the side effect of isopropyl alcohol.

This effect is very relevant in the fabrication of an all-polymer field effect transistor, in which gate dielectric is deposited from a solution process. For example, polymeric gate dielectric poly-4-vinylphenol (PVP) dissolved in IPA has strong side effect on P3HT properties. Figure 8-2 shows device characteristics of a P3HT FET before

and after PVP film was deposited on the P3HT layer. The striking difference in device characteristics should be mainly attributed to IPA. However, it is unknown so far what the exact root cause is. A systematic study on this issue is therefore technically and theoretically important and necessary.

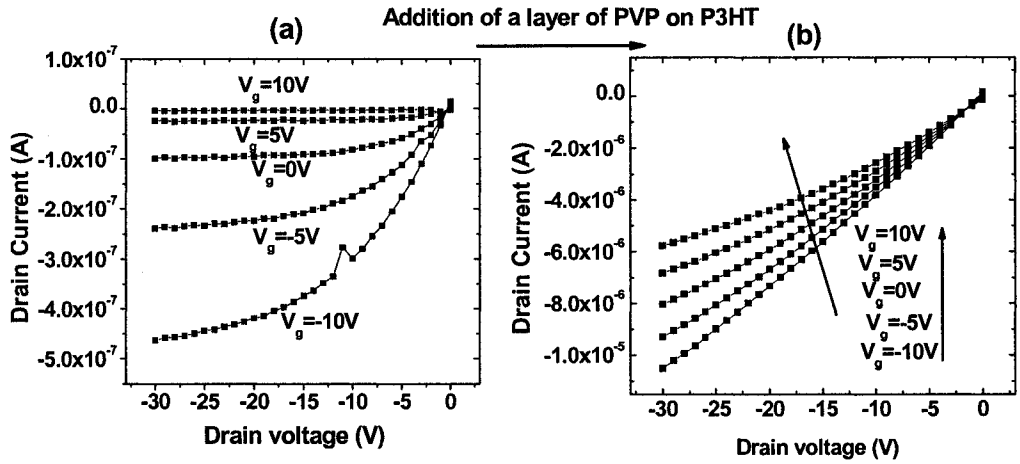


Figure 8-2 P3HT device characteristics showing the effect of PVP cast from isopropyl alcohol solution; (a) without PVP layer and (b) with PVP layer on P3HT.

8.2.2 Leakage Current

Currently fabricated P3HT FETs exhibit a significant level of leakage current. In order for practical applications, it should be reduced. We have found that the leakage current was sensitive to fabrication process, especially to gate oxide process conditions. For example, oxygen plasma or KOH treatments of SiO_2 surface prior to the deposition of P3HT layer was found to significantly increase the leakage current. Figure 8-3 shows that oxygen plasma treatments of oxide surface has led to leakage current up to several μA, which is almost two orders of magnitude higher than the device with gate oxide without oxygen plasma treatment. This high leakage current has very detrimental effect on device characteristics. Therefore, further study is necessary on this topic.

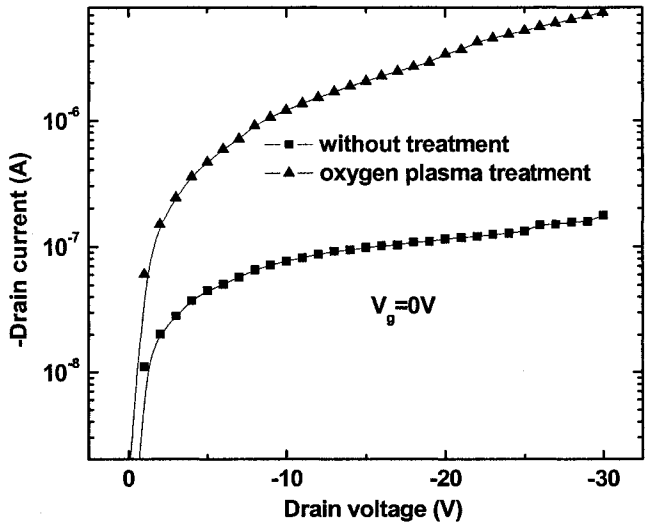


Figure 8-3 P3HT FET drain leakage current at V_g=0V.

8.2.3 Polymer Modulation Doped OFET

This is a very promising area, and our initial results have demonstrated the "modulation doping" effect in polymer heterojunction. It seems analogous to the conventional modulation doped field effect transistors that have shown strikingly high mobility. Further work could be focused on optimized designs of the polymer heterojunction stacked layers. The layer thickness, band discontinuity level and doping profile need to be studied. New models should be developed to describe the operation of the devices. This could be implemented with the help of numerical simulations. In this thesis, we had initial simulation results which described the operation of the polymer heterostructure. However, our simulation is based on the classical model. Part of the further work should be focused on modeling of polymer heterostructure by considering the quantum confinement effects. A systematic comparison should be made between the results from the classical model and the quantum effect model. By comparing the

simulation results and the experimentally observed device characteristics, a better understanding of the polymer MODFETs should be possible. The other issue that needs to be further addressed is the film-growth technique. Due to the solvent compatibility problem, we used a transfer method (see Chapter Seven). This is not technically preferred, since it does not allow growing thin film of high-quality (i.e. sufficiently dense, uniform film), which may introduce trapping and scattering centers for the carriers located within the well region.

8.2.4 Treatments of Gate Silicon Oxide

It has been shown that the P3HT device characteristics can be significantly improved by simply annealing the SiO_2 surface. It could be attributed to the reduced physically absorbed water molecule and a certain level of dehydration at the SiO_2 surface upon annealing. Due to the limitation of lab instruments, our annealing experiment was carried out at a moderate temperature (300°C) and FET devices were prepared in air. We expected that a higher curing temperature and a very dry environment for FET fabrication could further improve the device characteristics.

8.2.5 Inkjet Printing Technique

Inkjet printing technique has been explored in our work. It has enabled us to deposit and pattern electrodes from materials, such as, conducting polymers and metals, for high-performance devices. This technique allows for deposition of solution on selected areas, and therefore is very helpful to reduce leakage current if the active channel layer could be deposited by inkjet printing. However, we have not achieved satisfactory results in our efforts so far. Much work could be further done for optimizing

solutions and conditioning substrate surface in order to achieve uniform and highly-ordered films.

8.2.6 Other Issues

Stability of the devices in air is important. However, current devices show a certain level of degradation when exposed to air for extended time. It has been attributed to the diffusion of oxygen and water molecules into P3HT thin film as described earlier. Further work should be done on the passivation of these devices from air to prolong device's lifetime.

Furthermore, due to the low mobility of organic semiconductors, devices with short channel are desirable for high speed circuits. Vertical device structure seems to be promising [105]. Extended work could include structure designs and process optimizations. Full understanding of the key issues, such as, short-channel effect, and leakage current, etc., is necessary.

APPENDIX A

TAURUS-DEVICE INPUT SIMULATION COMMANDS

```
Taurus {device}
DefineDevice (
  name=devicemesh
  minX=0.0 maxX=20
  minY=-70nm maxY=200nm
  region(material=silicon, name=channel1),
  region(material=silicon, name=channel2),
  region(material=silicon, name=channel3),
  region(material=silicon, name=channel4),
  region(material=silicon, name=channel5),
  region(material=aluminum,name=source1),
  region(material=aluminum,name=drain1),
  region(material=oxide, name=oxide)
  region(material=polysilicon, name=gatematerial)
  region (material=Ambient name=ambient1)
  x=0.0 dx=200nm
  x=4   dx=200nm
  x=5   dx=10nm
  x=5.2   dx=200nm
  x=14.8   dx=10nm
  x=15  dx=200nm
  x=20 dx=200nm
  y=-70nm dy=10nm
```

```
  y=-20nm dy=10nm
  y=-10nm dy=5nm
  y=-5nm dy=1nm
  y=0nm dy=0.5nm
  y=5nm dy=5nm
  y=100nm dy=50nm
  y=200nm  dy=50nm
)
Defineboundary(
  region=gatematerial,
  polygon2d(
  point(x=0, y=100nm), point(x=20,y=100nm), point(x=20, y=150nm),
  point(x=0,y=150nm)))
Defineboundary(
  region=oxide,
  polygon2d(
  point(x=0, y=0nm), point(x=20,y=0nm), point(x=20,y=100nm), point(x=0,y=100nm)))
DefineBoundary(
   region=source1,
   polygon2d(
   point(x=0,y=-50nm), point(x=5,y=-50nm),point(x=5,y=0nm),point(x=0,y=0nm)))
 DefineBoundary(
   region=channel1,
```

```
  polygon2d(
  point(x=5,y=-50nm), point(x=5.02,y=-50nm),point(x=5.02,y=0nm),point(x=5,y=0nm)))
DefineBoundary(
   region=channel2,
   polygon2d(
   point(x=5.02,y=-20nm), point(x=14.98,y=20nm),point(x=14.98,y=0nm),
   point(x=5.02,y=0nm)))
DefineBoundary(
  region=channel3,
  polygon2d(
  point(x=14.98,y=-50nm), point(x=15,y=-50nm),point(x=15,y=0nm),
  point(x=14.98,y=0nm)))
DefineBoundary(
  region=drain1,
  polygon2d(
  point(x=15, y=-50nm), point(x=20, y=-50nm),point(x=20, y=0nm),
point(x=15, y=0nm)))
DefineBoundary(
   region=channel4,
   polygon2d(
   point(x=0,y=-70nm), point(x=5.02,y=-70nm),point(x=5.02,y=-50nm),
   point(x=0, y=-50nm)))
DefineBoundary(
```

```
 region=channel5,
 polygon2d(
 point(x=14.98,y=-70nm), point(x=20,y=-70nm),point(x=20,y=-50nm),
 point(x=14.98, y=-50nm)))
save (meshfile=FET0.tdf)
Regrid (
      MinX=4, MaxX=16, MinY=-60nm, MaxY=100nm,
      MaxDeltaY=50nm,
      Criterion (Name=AllInterfaces))
save (meshfile=FET1.tdf)
# Define contact regions
Definecontact (name=source, X (min=0, max=5) Y(min=-50nm, max=0nm))
Definecontact (name=drain, X (min=15 max=20) Y(min=-50nm, max=0nm))
Definecontact (name=gate, X (min=0 max=20) Y(min=150nm, max=151nm))
Regrid (minx=5, maxx=15, MinY=-10nm, maxY=0,  MaxDeltaY=2nm)
save (meshfile=FET3.tdf)
#---- semiconductor material definition and solve equations
Taurus {device}
DefineDevice(Name=tft, meshfile=FET3.tdf, areafactor=500)

#doping profile:
profile (name=ptype, region=channel1, uniform(value=2e17))
profile (name=ptype, region=channel2, uniform(value=2e17))
```

```
profile (name=ptype, region=channel3, uniform(value=2e17))
profile (name=ptype, region=channel4, uniform(value=2e17))
profile (name=ptype, region=channel5, uniform(value=2e17))
profile (name=ntype, region=gatematerial, uniform(value=5e18))
Physics(
Aluminum(
global (workfunction=5.1),
electricConductance(
electricConductivity(sigma0=5e6))))
Physics(silicon(holecontinuity(mobility(constant=true,mup0=0.016))))
Physics(Silicon(global(global
conductionDensityOfStates(AtRoomTemperature=2e21),
ValenceDensityOfStates(AtRoomTemperature=2e21)))))
Physics(Silicon(Global
(Permittivity=3, ElectronAffinity=3.0, Bandgap(Eg300=2.1))))
#contact(name=gate, workfunction=5.0)
#contact(name=source,type=schottky, workfunction=5.1)#to set contact
#                                                    barrier(optional)
#contact(name=drain, type=schottky, workfunction=5.1)
#contact(name=source,type=ohmic)#-----default: ohmic
#contact(name=drain, type=ohmic)
#setAttributes{Traps(material=silicon,
#trap(ilevel=0, dgen=2, et=-0.5, nt=-6e17,taup=1e-5))}
```

```
#interface (qf=-1e12, material(m0=silicon, m1=oxide))
SetBias (value=0.0) {Contact (name=source, type=voltage)}
SetBias (value=0.0) {Contact (name=gate, type=voltage)}
SetBias (value=0.0) {Contact (name=drain, type=voltage)}
# Specify zero-carrier solution
Symbolic (carriers=0)
numerics (iterations=100, relativeerror=1e-3)# to alleviate convergence
                                                # problem
# initialization that only solve poisson's equation
Solve {}
Save (meshfile=initial.tdf)
# solve poisson's equation and hole current continuity equation
Symbolic (carriers=1, holes)
# simulate output characteristics
ramp (
voltage (electrode=gate,endvalue=-15,nsteps=15)
Ramp (logfile=Id1.data
Voltage (electrode=drain, startvalue=0, endValue=-30, nSteps=30))
ramp (
voltage (electrode=gate,endvalue=-10,nsteps=5))
Ramp (logfile=Id2.data
Voltage (electrode=drain, startvalue=-30, endValue=0, nSteps=30))
ramp (
```

```
voltage (electrode=gate,endvalue=-5, nsteps=5))
Ramp (logfile=Id3.data
Voltage (electrode=drain, startvalue=0, endValue=-30, nSteps=30))
ramp (
voltage (electrode=gate, endvalue=0, nsteps=5))
Ramp (logfile=Id4.data
Voltage (electrode=drain, startvalue=-30, endValue=0, nSteps=30))
Save (meshfile=gateN15.tdf)
Stop

#---PMEI user defined field dependent mobility model-----
EquationDatabase{poissons.db,holecontinuity.db,electroncontinuity.db}
DefineEquation
(
 Name=Mobility,
 Material=Silicon,
 IsDeviceEquation,
 VariableName=Dummy,
 Parameter (Name=k, Default=8.62e-5), # eV/k
 Parameter (Name=T, Default=300),    #k
Model (Name=TempField
 Expression {"Sqrt(electricfield*electricfield)"}
)
Model (Name=Mu,
```

```
Parameter (Name=Mu0, Default=0.016)
Parameter (name=E0, default=1e5)
Expression {"Mu0*sqrt(Tempfield*KT/E0)"
#expression {"Mu0*sqrt(Tempfield/E0)"
}
)
Model
(
 Name=PmeiLowFieldMobility,
 Expression {"(Mu)"}
 ),
Expression {"dummy"}
)
```

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