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Delay line based passive radio frequency identification tags

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DELAY LINE BASED PASSIVE RADIO FREQUENCY IDENTIFICATION TAGS

by

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ABSTRACT

This work describes the concept, design, fabrication, and characterization of delay-based radio frequency identification (RFID) tags and RFID-based sensor tags, representing a novel RFID technology. The presented delay-based RFID concept is based on the LC-delay-line and transmission-delay-line based approaches. The proposed concept allows the realization of RFIDs and RFID-based sensor tags at any allowed radio frequency, with the limitation of realizing delay elements capable of producing required delays. The RFID configurations presented in this work are for operation at 915 MHz. Simulations are used to design and optimize components and devices that constitute the tags, and to integrate them to realize tags of different configuration. A set of fabrication processes has been developed for the realization of the tag. Characterization and field testing of these tags show that delay-based RFID approach can be used to make passive tags at ultra high frequency (UHF) and other allowed frequencies. Delay-based tags have the advantages of time domain operation, and the feasibility of complying with FCC regulations. However, size, need of isolators and circulator, and design constraints in producing higher number of bits are some of the concerns that need to be further addressed. In summary, this dissertation work presents a viable alternative RFID approach based on the delay line concept. The results obtained show great promise for further development and optimization of this approach for a wide range of commercial applications.

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DEDICATION

To my mother, Jayalakshmi, father, Kurmacharyulu, brother, Madhusudhan,

Sister, Santhi, uncle, Dr. Gopalacharyulu,

my beloved wife, Radhika,

my high school Jawahar Navodaya Vidyalaya,

India and the United States

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CHAPTER 1

INTRODUCTION

Radio Frequency Identification is a generic term for technologies that use radio waves to automatically identify individual items. There are several methods of identifying objects using RFID, but the most common is to store a serial number that identifies a product, and perhaps other information, on a microchip that is attached to an antenna. The chip and the antenna together are called an RFID transponder or an RFID tag. The antenna enables the chip to transmit the identification information to a reader. The reader converts the radio waves returned from the RFID tag into a form that can then be passed on to computers that can make use of the sent information (Figure 1.1).

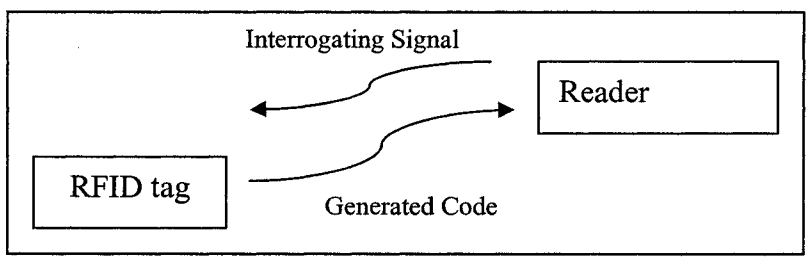


Figure 1.1 Schematic diagram showing a typical RFID system.

Even though tags in the form of RF transponders have existed for the last fifty years, bar codes have been the primary means of identifying products for the past twenty five years. However, bar codes require line of sight for them to be read by a scanner.

Moreover, if a bar code on an item is damaged, soiled or removed, it can not be scanned. Standard bar codes identify only the manufacturer and product and not the unique individual item. Recent inventions in fabrication and design techniques solved some of these problems and lead to the aggressive application of the RFID technology, where tags can be read even under an object or layer, do not require line of sight, and can be read simultaneously. RFIDs having read/write capabilities can be both read/written wirelessly, offering a lot more flexibility in their implementation to form networks that can make inventory and supply chain management an easy task. RFID-based sensor tags offer additional advantages like tamper proof capability and entity sensing such as, pressure, stress, temperature and vibration. These tags exist in different layouts, form factors, work in different bands of the radio spectrum, and constitute different design and fabrication technologies. Recent advances in the technology allow sensors to be incorporated in RFIDs called RFID-based sensors. The following gives an overview of the technology and details the challenges for its large scale implementation.

1.1 Overview of RFID Technology

RFID is one of the automatic identification (auto ID) technologies such as, bar codes, smart cards, voice recognition, biometric technologies, optical character recognition, etc. These technologies are used to help machines identify objects which are also called automatic data capture [1, 2, 3]. Companies and commercial entities want to identify items, capture information about them and somehow get the data into a computer without having employees type it in. This is to increase efficiency, reduce manual data entry errors, and free up staff for more value-added functions.

RFID technology had one of its first applications during World War II. "Identification Friend and Foe" (IFF) systems have been deployed in the military and commercial aircraft that emit a unique signal to identify one another. Over the years different derivative forms of tags such as, far-field/near-field, chip-based/chipless and low/high frequency have been used for applications from animal and bird tracking, to military surveillance, to present day smart systems and automatic inventory [4]. Most of the initial tags were powered by battery [5]. Until the 1960's, most tags were far-field devices. Reading distances of these tags are much greater than the wavelength and the size of the antennas involved. Chipless tags such as, harmonic-diode tags, surface acoustic wave (SAW) reflectors were some of the other technologies available during this time [6]. In the early 1970's Los Alamos National Laboratory and the Department of Energy developed chip-based RFID tags to track radioactive materials. Even though these tags were battery powered, they used back scattering modulation for the transmission, which will be explained later. This technology was further improved by companies such as, Identronix, Micron, Amtech, Motorola, and Intermec using the advances in silicon industry, and low power, ultra high frequency IC design [7]. During the 1970's the first low-cost electromagnetic tagging systems appeared for library and retail store applications, popularly known as Electronic Article Surveillance (EAS) systems. During the same period another chipless technology, based on LC-resonance arrays for swept-RF, has been developed for security access applications.

Other applications of chip-based tags such as, tagging cattle, horses, and laboratory animals and commercial and industrial access control systems were developed in the 1980's. Commercialization of chip-based tags overtook their chipless counterparts

in the 1990's and continued into the 21st century. Now RFID tags are used for a variety of applications from freight train car tagging, automated tracking and billing, automatic sorting of clothes at commercial laundry companies, navigation aid for vehicles or for the visually-impaired. RFIDs of grain size are now used as tags using credit card information embedded under the skin, identification aid on business cards and paper currency. By decreasing the cost of individual tags, demand by different types of applications can be met [8,9]. With the regulatory protocols already in place, there is a tough competition to produce reliable tags at low-cost.

1.2 Major Classifications

The present day RFID tags are the basic components that are bound to produce gigantic networks that can uniquely identify tagged items, obtain real time inventory data and generate a lot of information-technology-based applications. Most of the tags are passive and flexible and cost 50 cents or more if purchased in larger volumes. Wireless sensor technology, on the other hand, envisions large networks with millions of low-cost passive, semi-passive or active nodes that provide a real time sensed data that can be fed to the internet without human intervention. Different kinds of RFIDs and RFID-based sensor tags are available for such applications from a variety of unique RFID technologies. These tags are classified based on different criterion such as, the presence of battery, transmitter, and the presence of a chip and the frequency of operation. They are described below.

1.2.1 Passive, Semi-passive and Active Tags

Tags are classified as passive, semi-passive and active based on the source of energy and transmitter on board. Passive tags do not have either a battery or a transmitter on-board. They are energized from the interrogating signal of the reader. Active tags, on the other hand, have a battery and an active transmitter on the tag and can transmit and receive over longer distances. Semi-passive tags have an on-board power source, but no transmitter. Each type has its own market share characterized by the application requirements.

1.2.2 LF, HF, UHF and Microwave Frequency Tags

According to national and international communication regulatory authorities, 125 KHz (LF), 13.56 MHz (HF), 868 MHz and 915 MHz (UHF) and 2.45 GHz (microwave) frequency ranges are the allowed Industrial Scientific and Medical Applications (ISM) frequency bands for RFID purposes. RFIDs can be categorized based on these ISM bands and are designated as LF, HF, UHF and microwave tags. In general, the size of the tag decreases with the increasing frequency of operation.

1.2.3 Chip-based and Chipless Tags

Tags can be chip-based or chipless. A chip-based tag contains a silicon chip attached to an antenna on the substrate. A typical RFID chip contains 80,000 transistors and an Electrically Erasable and Programmable Read Only Memory (EEPROM) to do complex functions [2]. Chip-based RFIDs are main stream products with exponentially increasing markets. Chipless RFIDs are characterized by the absence of an integrated chip. These include SAW-based RFIDs, RFID based on domain wall kinetics, LC

resonators, magneto-elastic resonators and RFIDs based on harmonic generation. Besides the above mentioned technologies, RFIDs are fabricated using printable polymers and hybrid materials using cost effective printing techniques. In general, chipless technologies can not perform complex functions like their chip-based counterparts, but many of them offer cost-effective solutions in their application specific domains. Different present-day chipless technologies are described below.

1.2.4 Chipless RFID Technologies

Inventions involving chipless RFIDs have began as early as the 1940s, and resulted in commercially viable RFID technologies offering an option to silicon-chip-based RFIDs. Some of the chipless RFIDs such as, RFIDs based on domain wall kinetics, although producing an electronic signature of their own can not produce multi-bit codes and are not discussed below. The following will explain different chipless RFID technologies that are capable of producing multiple bit code generation.

1.2.4.1 SAW-based RFID tags

SAW-based RFID Tag uses a piezoelectric substrate in combination with an antenna and works on the surface acoustic wave phenomenon. The reader emits a radio wave pulse that is directly converted into a nano-scale surface acoustic wave on the substrate's surface by the inter-digital transducer (IDT). This wave travels past a set of wave reflectors to produce uniquely encoded acoustic wave pulses, which travel back to the IDT. The IDT converts those pulses into a radio wave reply signal that is sent back to the reader. The SAW-based substrate operates using the piezoelectric effect and is passive. These received pulses are then processed and interpreted as data. A variety of sensor elements can also be attached to these substrates as well, thus allowing the SAW

tags to function as wireless sensors. They have read range of hundreds of meters or so, depending on the reader power. However the process of depositing precise silver or gold lines on lithium niobate substrates to create the chip, packaging, and attaching the antenna, is not significantly cheaper than traditional semiconductor RFID chips. With recent improvements such as, anti-collision, SAW-based RFID tags are gaining commercial importance.

1.2.4.2 LC resonance swept RF tags

When a reader sweeps a range of RF frequencies, a response in the form of resonance peaks can be seen from a multi-bit LC resonance array tag in the frequency domain. Each LC resonance element is made to resonate at a particular frequency over the swept RF range. These resonances peaks are easy to interpret and process even in the presence of environmental noise. Moreover, capturing a frequency response of a material structure can be accomplished with very little transmitted energy. In order to exhibit a large amplitude response, low internal losses and weak coupling to the external environment are required. This RFID technology is commercially exploitable and lead to tags for applications such as electronic article surveillance.

1.2.4.3 RFIDs based on harmonic generation

Some materials generate harmonics when placed in an electromagnetic field having a particular frequency and amplitude. In the tags based on harmonic generation, harmonics generated by a soft magnetic material is used as the response of the object from the surrounding environment. These tags are commercially used as anti-theft tags for EAS and are known as harmonic tags. These tags can be detected over 100 meter

distances. Other applications include tracking people buried in an avalanche and tracking butterflies. This technology can be used to produce multi-bit tags.

1.2.4.4 Printable electronics-based RFIDs

The Advent of conducting and semi-conducting polymers which are thought to be solely insulators has paved the way for new type of electronic circuits and gadgets. Though they can not compete with solid-state electronic devices in performance they do offer low-cost alternative processes and are advantageous in producing inexpensive gadgets such as, RFIDs. Polymer electronics is seen as a promising alternative for RFID fabrication based on conventional solid-state electronic device logic. Chips made of synthetic polymers or mono-crystals can be less expensive than silicon chips, and may act as complementary sensors for detecting temperature and vibration [6]. It might take a few more years before polymer electronic circuits overcome issues such as, device stability and electronic performance and prove to be an alternative commercial technology for RFID fabrication for commercial applications.

1.3 Need for Low Cost RFIDs

Cost is the main factor among others such as, dimensional and mechanical flexibility and application customization, for the adoption of any RFID technology by the commercial market on a large scale. Conglomerates of academic institutions and companies around the world took the initiative to promote RFID technology and created exclusive research labs such as, Auto-ID labs. By the year 2003, Auto-ID labs have established the network protocols, language, and infrastructure required for a worldwide RFID based network and have assured the credibility and viability of RFID technology

by performing field tests of RFID attached items with newly developed protocols and infrastructure. This set of protocols and infrastructure developed by Auto-ID are flexible enough to adopt different types of tags and different technologies of the future. The only major obstacle still remaining in the adoption of RFID technology is cost. MIT's autoID center estimated the use of 555.3 billion RFIDs by its sponsors alone [7]. Figure 1.2 shows a schematic diagram of an information food-chain similar to the biological food-chain diagram.

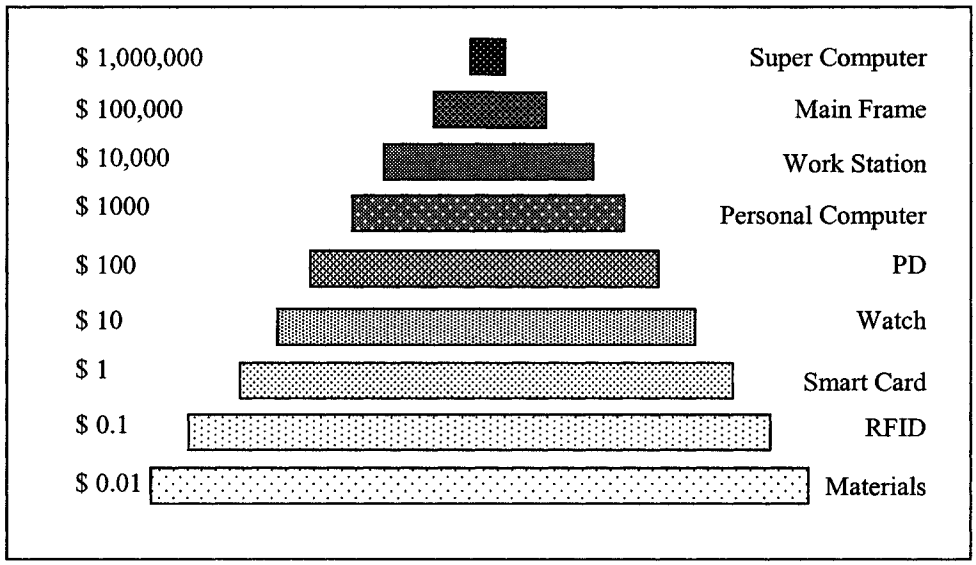


Figure 1.2 Information food chain [1].

From Figure 1.2, it can be appreciated that high end, high cost systems of information technology, such as super computers, are less in number but are high in cost. As we go down the hierarchy the price goes down and so does the performance of the systems at that level but the number of individual systems will increase. Each level in the diagram can be networked to the other through the internet. The lowest level in the diagram is labeled as materials which are generally used for electronic article surveillance

(EAS). As mentioned earlier, these materials can give unique response to an interrogating electromagnetic signal from the reader and cost one cent or less. But they can not provide a significant amount of data and requires interpreting devices to convert data into digital information bits. RFID technology is seen as a practical approach to form vast networks rather than materials even though the former costs more. Since tags are required in the billions, cost of the tag still remains the object of concern for their implementation into networks for both researchers and industry. There has been a tremendous effort to make tags for a few cents that can generate the maximum possible number of bits in response to an interrogating signal. Such low cost tags can be attached to each and every entity in the world making them readable from anywhere in the world through the internet which will influence the way we live.

1.4 Technology Options for Low Cost RFIDs

As mentioned in the earlier, different RFID technologies are available and can be applied to different applications. There is a great potential for RFIDs and cost is the main factor defining the versatility of applications and market reach. Evolving EPC global standards for RFID systems are reducing the cost of RFID readers and other equipment due to interoperability and competition. The following describe techniques and strategies available for chip-based RFIDs for the reduction of the individual tag price, and enhance the cost effectiveness of available chipless technologies.

1.4.1 Cost Reduction Techniques for Chip-based RFIDs

Chip-based RFIDs are predominant in the present market compared to their chipless counterparts. Commercial chip-based RFIDs of the present day have a silicon

chip assembled on a flexible substrate containing antenna(s). The chip is small enough not to affect the mechanical flexibility of the tag. Flexible circuit technology has a significant role in achieving this type of assembly [10]. Market demand for the RFIDs can be met by using some of the unused 35% potential of existing microprocessor chip manufacturing facilities. Even though researchers could produce ultra low power (a few microwatts) consuming chips for RFID applications, chip associated costs remained the main obstacle to the goal of reducing the price of an RFID down to five cents. Having a silicon chip on an RFID is expensive, because of silicon costs, and fabrication costs.

1.4.1.1 Minimizing chip size

It costs two billion dollars to set up a microprocessor manufacturing unit and it takes two weeks to complete microfabrication steps to produce a wafer. It costs $1000, on an average for fabricating chips on a wafer today. Therefore, it can be understood that silicon chip costs increase with an increase in the number of transistors on the chip. A 64 bit simplified standard would decrease the number of transistors from 80,000 to 8000 [2]. Another factor affecting the cost for fabricating chips on a wafer is the feature size. Processing costs increase linearly with the decrease in the feature size. Silicon chip costs can be decreased by increasing the throughput from each wafer. Even though the price of an 8-inch silicon wafer is relatively stable, chip yield depends on dicing. Today, most wafers are cut with a diamond saw which yields a maximum of about 15,000 microchips that are one millimeter square. A process called wet etching is becoming popular where a thin line of acid eats through the wafer and yields up to 250,000 chips that are about 150 microns square.

1.4.1.2 Statistical self-assembly techniques

It is time consuming to precisely assemble small chips on to the tag using sophisticated pick-and-place machines, thus limiting the throughput. Fluidic self-assembly and vibratory assembly are two promising techniques that differ from traditional pick and place machines and reduce the duration time of the assembly process considerably. The term 'statistical assembly' comes from the fact that it is not possible to achieve 100% precision in these processes and still have an edge with low variable costs.

In fluidic self-assembly, the wafer is diced through chemical etching into differently shaped units called nano-blocks. These dies, which have a three dimensional shape, are suspended in a fluid and flowed across the substrate, which has indentations that fit the nano-blocks. Finally, the blocks are later connected to contact pads using a standard metallization process. Vibratory assembly is a similar technique in which vibration is used, instead of a fluid, to act as a medium for the proper attaching of the nano-blocks to the tag's substrate.

1.4.1.3 Antenna fabrication costs

Antenna fabrication costs become significant when a tag costing five cents needs to be produced. An innovative technique where an antenna is printed using conductive ink followed by a layer of metal stamped on the top using a high-speed plating technology could produce antennas in high volumes, and can make tags costing around five cents. This method is different from the usual acid etching methods used to shape electroplated copper or aluminum antenna geometries that cost from 5 to 15 cents [9]. Other promising approaches are direct printing using nano-inks and synthetic polymers for antenna fabrication.

1.4.2 Cost Effectiveness of Chipless Technologies

Absence of a chip would result in a huge cost reduction of an RFID as it eliminates both chip and assembly costs. Printing synthetic polymers as explained earlier, will reduce the assembly costs but may result in new problems like poor resolution, low yield and high power requirements. SAW-based RFIDs have comparable characteristics with their chip-based RFID counterparts but cost more because of their piezoelectric substrate. The Performance of RFIDs, based on magnetic properties or resonance, are limited by either frequency domain operation or a limited ability to produce multi-bit code generation.

1.4.3 Hybrid RFID Tags

Some of the elements of the chip-based tags and chipless tags can be used together to create hybrid tags which is one of the ways to invent low-cost technologies. Some of the wireless sensor tags already have both chip-based and chipless components. This would allow one to eliminate the disadvantages of the two types of technologies and at the same time exploit the advantages of both. Therefore, chipless technologies in general, with derived advantages from silicon chip-based RFID technology, can provide the low-cost RFID solutions required for the present and future markets.

1.4.4 Need for Improved RFID Technology

It is clear that none of the above mentioned technologies, independently or in combination, can become a complete solution to the present day RFID problems. Polymer electronic technology has many inherent disadvantages for RFID fabrication. Even though polymer printing is promoted as a future RFID technology, printer

throughput decreases with increasing accuracy requirements. Soft lithography, which can be an alternative technique, is disadvantageous because the hard coded layout on the mold is not flexible for modifications. Soft lithographic techniques are not flexible for innovative custom-based designs and for different printing materials. The precise control of LbL and LB methods is affected by poor lateral contrast and thermal instability issues [10]. Moreover, the instability of polymers is one of the main issues that needs to be addressed for polymeric electronic devices. N-type semiconducting materials that have been so far reported have a charge mobility of 10^{-2} cm^2/Vs which is only one third compared to typical p-type conductivity. However, with the invention in recent years of more stable n-type polymers with improved conductivities, stable devices could be made using good packaging techniques and reliable protective coatings [11-12]. Still, polymer devices face the serious challenge of shorter life times compared to solid-state devices made by conventional technology. Impurities, thermal instability and sensitivity to moisture are some of the main causes that are attributed to the shorter life time of these devices. Polymer electronic devices can not reach the dimensions of typical silicon integrated chip devices because of material purity problems [13]. Large scale low-cost devices and rugged large-area devices and systems can be made using polymers.

Solid-state electronics on the other hand, is much more prominent with well established theory, predictable device characteristics, down-scalability and high mobilities, but still not a complete solution for a universally adaptable RFID technology due to cost and other problems discussed earlier. While LF and HF Tags have long been commercialized, UHF tags and readers are now expanding their market with the GEN-2 protocol in place, which regulates RFID performance at 915 MHz. However, companies

could not offer individual tags priced below 50 cents unless ordered in quantities of millions because of silicon chip and assembling costs. RFID-based sensor tags cost are too high. To make vast networks that can sense automatically and feed the data into the internet with out manual intervention, fabrication costs of the IC, and assembly costs of the RFID needs to be reduced.

While SAW-based devices are costly due to the substrate costs, multiple resonance swept RF tags are big in size. Therefore, a cost-effective solution for RFIDs and RFID-based sensors would be a hybrid technology platform that shall derive benefits from both the silicon and non-silicon technologies utilizing an intelligent design to eliminate some of the inherent disadvantages present in each of the materials and components used. The developed protocols and regulations are flexible enough for any new RFID technology as long as they communicate in the same language as the rest of the tags. An RFID/RFID -based sensor tag that is simple in layout, and easily fabricated using desktop and cost effective equipment and processes that reduces assembly costs is much more desirable.

1.5 Literature Review

The key milestones in the emergence of different technologies to realize RFIDs and RFID-based sensors have been presented here. Approaches taken by researchers to further lower the price lead to the development of low-cost alternative technologies such as, printed electronics RFID tags, SAW-based reflectors, and swept RF LC resonant array based tags. All these technologies are suitable for realizing multiple bit tags that can compete with silicon chip-based RFIDs. Other types of chipless tags mentioned in Chapter 1 that can be applied to single bit generation or unique signature, are not

reviewed in this chapter. The advancements in chip-based RFIDs such as, fabrication techniques, design improvements behind low-power ICs, and phenomenon such as back scattering have been explained below. The important milestones in the advancement of other chipless technologies and printed electronics in RFID realization have been presented later. Research done towards the design and low-cost fabrication of RFID-based sensors and applications of delay line concepts have been detailed in chronological order at the end of this section.

Silicon-chip-based RFID is a proven technology that has been around for more than fifty years. In the early 1970's, the most direct descendent of present day chip-based RFID originated in Los Alamos National Laboratory. These tags are semi-passive battery powered and function by back scattering. This technology is further developed by Identronix in the 1980's and later by Micron, Amtech and Intermec. During this time advances in semiconductor technology enabled low-power passive ICs to operate in the UHF range. This is achieved by reducing the chip size which resulted in lower silicon device cost. The cost for making an RFID chip can be estimated simply by knowing the required silicon area for the RFID chip. Assuming a typical modern-day fabrication plant with a 0.25 μm CMOS process and assuming a wafer of 10-inch diameter, this translates to between 10 to 40 thousand dies per wafer [2]. With the help of new technology called wet etching, a thin line of acid is laid that eats through the wafer, 250,000 chips or more can be obtained that are about 150 microns square. This would bring down the cost of each die from 3 to 10 cents each to around one cent each. But working with smaller chips requires more sophisticated pick-and-place machines that would increase the costs further. Alien Technology's fluidic self-assembly and MIT's vibratory assembly, are

some of the promising assembling technologies that can further lower the cost [9]. Rafsec, a subsidiary of Finland's UPM-Kymmene Corp., is developing an innovative antenna that will be attached to chips to make tags that, at high volumes, might cost around five cents. With its pioneered high-speed plating technology, an antenna is printed using conductive ink and then a layer of metal is stamped on top. This would decrease the cost of an antenna to a penny when manufactured in bulk. This price is very low compared with 5 to 15 cents for a typical antenna made with existing technology. Even with successful development and implementation of the above techniques, silicon chip-based RFIDs and RFID-based sensors would cost more due to the unavoidable silicon related costs and, therefore, can not be adapted to low end applications that in combination have a large market potential together. Since there are promising non-silicon technologies for RFIDs, silicon chip-based RFIDs and RFID-based sensors can either be augmented with the resulting technology or replaced if proven more commercially viable.

Since the discovery of conducting polymers by Alan J. Heeger, H. Shirakawa, and Alan G MacDiarmid in 1977 [14], which won them the Nobel Prize in chemistry for 2000, many new challenges and opportunities have been brought into the fields of physics, chemistry, electronics, and electromagnetics. With the later discovery of semi-conductivity in polymers, the notion that polymers are only insulators has changed and researchers envisioned that polymer electronics and hybrid electronics would complement solid-state electronics to meet the ever growing demands of hi-tech industry. Although polymer electronics offer advantages such as flexibility, reduced cost, processability by side-chain engineering and controllability of device characteristics, there are disadvantages such as instability, incomplete theory to support the material

behavior and relatively low conductivities. Processing techniques such as side-chain engineering can be used to modify electrical, mechanical, and chemical properties of polymers to suit the requirements of an electronic device. Organic polymers such as polythiophenes, polyaniline (PANI), polypyrrole (PPy) and their derivatives have gained much reputation as conducting and semiconducting polymers [15-20]. Maximum conductivities of 200-300 S/cm are reported to date in p-type conducting polymers, whereas the conductivities of metals are in the order of 10^5 S/cm and above. Low cost processing techniques such as printing, spin coating, and spray coating can be used to fabricate polymer electronic devices and thus can reduce the cost of their production [21, 23]. A group of researchers believe that printed electronics provides a potential pathway towards the realization of low-cost RFID tags for item-level tracking of consumer goods and other applications. The idea that the circuits can be printed over large areas and onto flexible substrates has gained momentum in the past decade. From the materials standpoint, the most convenient class of semiconductors to form the basis for such circuitry is organic or polymeric semiconductors. Such materials have properties that are inherently suited to this kind of processing; indeed, some of the best polymeric semiconductors are cast from solution at room temperature by ink-jet printing, resulting in devices that have performance characteristics similar to those of amorphous Si transistors. A ambi-polar behavior has been realized for an n- and p-type polymer dispersed layer, and for a single organic material with a low band gap, and thus providing a low barrier for electron and hole injection [0- 28]. RFID cards and RFID based sensors are made possible with this complementary circuitry for applications involving identification, verification, and tracking [29]. Redinger et al., [30] developed an all ink-

jet-deposited process capable of creating high-quality passive devices suitable for an RFID front-end. Gold nanocrystals are printed to create conductive lines with sheet resistance as low as 23 mΩ per square. Optimal printing conditions were found for creating polyimide dielectric films as thin as 340 nm. Using these techniques, spiral inductors, interconnect, and parallel plate capacitors are produced. Subramanian et al. [31], used inkjet printing of novel conductors, dielectrics, and organic semiconductors, to produce transistors with mobilities of 0.1 cm^2/V-s. Both pentacene and oligothiophene precursors are used for pMOS and ZnO nanoparticles for nMOS. These transistors, which are building blocks of an RFID, perform adequately for a 135 kHz RFID. They could print nanoparticle patterns that are subsequently sintered at plastic-compatible temperatures, and use them to realize low-resistance interconnects and passive components. With further optimization, these researchers are looking forward to fabricating transistors for 13.56 MHz RFIDs [32]. Baude et al. [33], have fabricated pentacene-based, eight-bit RFID transponder circuitry. The same group of researchers earlier created an AC powering scheme for a 1-bit pentacene transponder, which eliminates the need for a rectification stage that is typically employed in RFIDs to convert the absorbed RF energy into dc power to run the transponder's logic circuitry. They could reduce the overall area and the number of process steps and successfully powered the pentacene-based circuitry at carrier frequencies of 125 kHz and higher to 1MHz and above.

Chipless tags hold great promise where the circuitry required to generate an ID from the tag is printed, or patterned on the tag itself, thus avoiding expensive assembly processes. Polymers can be patterned using techniques such as, soft-lithography, layer by

layer (LbL), Langmuir-Blodgett (LB) method and drop on demand printing. The performance of devices made using such techniques, are improving significantly. Researchers at MIT have fabricated nanostructures using techniques other than printing such as, layer by layer (LbL) and Langmuir Blodgett (LB) methods. Soft lithography and conventional lithography are used for lateral patterning of the substrate on which polymers are then deposited using LbL and LB methods. But these techniques are not adaptable for making circuits for RFIDs. However, different printing techniques are already available and offer a reliable option for cost effective fabrication of electronic devices on large scale. This technique avoids using photolithography for patterning and thus reduces the number of steps in producing a device or a circuit. In any case, polymeric electronic circuits would certainly bring down the cost for bulk and rugged applications with RFIDs being touted as one of the viable applications. Chips made of polymers or single crystal materials may turn out to be less expensive than silicon chips. However, the predominance of chip-based RFID technologies over many years is still influencing the development of device fabrication techniques.

SAW-based RFIDs originated in the early 1960's and re-emerged as a commercial success after recent advancements in this technology. SAW tags were developed commercially by Seimens in the mid-1990's and are currently being developed by start-up companies such as i-Ray in Israel and RF-Saw in the USA. These tags have the inherent ability to measure tag position, direction of travel, and tag temperature, which are costly or difficult to implement with competing technologies. SAW-based tag is one of the viable RFID solutions for many applications, especially those where extended read range, reading tags on metal and liquid items, and reading tags in harsh

environments are important. A recent breakthrough by RFSAW enabled the development of an encoding algorithm and manufacturing processes capable of producing 128 bits of address space from the earlier 14 bits [34], which will comply with EPC encoding. Furthermore, SAW tags can withstand processes that involve elevated operating temperatures, high energy X-rays, or gamma rays. This technology claims to have lower power requirements and performance limitations, better overall cost-effectiveness, superior read range, speed and accuracy. However, passive SAW-based tags need precise layout of their components on a high cost substrate such as, lithium niobate, that might increase the cost. Therefore, SAW-based tags, even though offering an entirely different technology by themselves, are relatively costly. These can not be made on flexible substrates because bending of the substrate will result in output errors. This technology is not widely adaptable for all frequency ranges of ISM bands over which chip-based RFIDs are a commercial success already. Pressure and other ambient variations will creep into the output thus affecting the tag's performance. Therefore, these tags are not adaptable for all types of applications.

The concept behind multiple resonance, swept RF tags has been explained earlier in Section 1.2. In the late 1970's Schlage, a lock manufacturing company, while exploring electronic alternatives to the standard key, found a chipless multiple-resonance swept-frequency approach for storing information in the frequency domain. The swept frequency approach went on to be developed by Westinghouse for security access applications. The concept of multiple resonances of LC arrays over swept RF has been used by different companies to produce different types of tags. The simplest way to create multiple bit tags is to use LC circuit arrays with each tuned to particular part of the

swept frequency. In this way the presence/absence of a particular LC circuit would correspond to presence or absence of a peak in the frequency domain that could be interpreted as bit 1. 'CW Over Solutions' and Checkpoint Systems commercialized these tags. Another way of creating multiple LC arrays is to use a set of capacitors in connection with a single inductor. These were first commercialized by Schlage and Westinghouse and more recently a Japanese company named Navitas has managed to make a planar metal foil label using the same concept.

Until recently, RFIDs and wireless sensor nodes and modules were considered to be different entities. Incorporating sensing capabilities in the RFIDs led to a new generation of active and passive tags called RFID-based sensors. These are different from wireless sensor nodes which are predominantly active and are more similar to RFIDs in their structure and architecture. Some of the commercially available RFID-based sensors can sense parameters such as, pressure, stress, and vibration and gases like ammonia, carbon monoxide and ethylene oxide [28].

1.6 Research Objectives and Considerations

The main aim of the proposed research is to design, fabricate and develop low-cost chipless passive RFIDs and RFID-based sensor tags. Different strategies have been developed to make the tag simple to fabricate and yet produce reliable ID code. Silicon chip technology and the corresponding complexities and costs are to be avoided in fabricating the tag. One of the main objectives is to reduce the cost of the tags using low-cost, non-silicon fabrication techniques which include methods such as, xerographic printing, spray-coating, and electroless deposition. Different ID generation circuits are explored which are based on delay line concept and care is taken to avoid lumped, off-

the-shelf components that require assembly. A tag that is commercially exploitable and compatible with FCC regulations will be ideal and presents a viable option in the present RFID market. Additional capabilities such as, anti-collision, dynamic ID generation, back scattering communication and other performance enhancing circuits shall be considered in the future work.

The word 'Tag or Tags', is used in this dissertation to indicate both RFID and RFID -based sensor. Similarly the word 'RFID Technology' is coined to represent a technology that can realize both RFID tags and RFID-based sensors. This dissertation contains tags that are based on both the LC delay and transmission delay line concepts. Some of the individual components that have been designed under prior thesis works are modified with respect to process and device integration in this work. The design and fabrication of planar inductors, capacitors, and ID generation circuits based on LC delay are described in [35]; Meander antenna design and fabrication has been detailed in [36]; Fractal and Hilbert antennas have been presented and characterized in [37]; and quantum tunneling composite (QTC) and polyvinylidene fluoride (PVDF) sensor elements are tested and characterized in [38].

1.7 Organization of the Dissertation

Chapter 2 introduces the concept of delay-based RFID technology and different tag configurations that can be realized. Both the LC-delay-line-based and transmission-delay-line-based RFIDs and RFID-based sensors are presented with constituting models, and elements.

A set of low-cost fabrication processes, as well as conventional silicon-based processes, have been explained in Chapter 3 that can be used in the fabrication of the

proposed tag layouts. Process flow charts have been developed for the fabrication of the tags using either set of fabrication processes.

Individual elements of the proposed tags have been designed/modified using modeling and simulations, and fabricated using the processes discussed in Chapter 3 and presented in Chapter 4. Commercially available components have been used for some of the components to realize the tag. Significance is given to making the processes used for the realization of the individual elements of the tag compatible with the process hierarchy of the complete tag fabrication.

Tags based on LC-delay-line-based ID generation and transmission-delay-line-based ID generation is discussed in Chapter 5 and Chapter 6, respectively. Device integration, fabrication using the proposed process flow, and characterization and testing of the fabricated components and the tag they constitute, have been detailed in each of the corresponding chapters.

Chapter 7 is dedicated to the comparison of the delay-based RFID technology with other existing RFID technologies. Conclusions drawn from the design, processing, integration and compatibility issues of the tag and the RFID systems that they constitute, are summarized. Finally, recommendations are made for future work based on the conclusions drawn from the analysis of the presented work.

CHAPTER 2

DELAY-BASED CHIPLESS RFID SYSTEMS

2.1 Overview

Delay-based chipless RFID technology is introduced in this chapter. Simple layout is proposed for realizing low-cost RFIDs and RFID-based sensors using this technology. The concepts behind delay-based RFID systems, design equations, and communication schemes under consideration are presented below. LC-delay-line-based RFID systems and transmission-delay-line-based RFID systems that are subcategories of the delay-based RFID Technology are described in the later part of the chapter.

2.2 Proposed Generic Layout

The working principle of a typical RFID system has been explained in Chapter 1. The layout of the proposed delay-based tag is given in Figure 2.1. It consists of three main parts. (i) antenna/antennas to interact with an external transceiver or reader, (ii) a sensor switch that controls the generated output code of the ID generating circuit, and (iii) a delay-based ID generation circuit that converts the reader's query signal into a unique code that is characteristic of the tag and sent back to the transceiver through the on-board transmitting antenna. The presence or absence of a sensor switch makes the tag an RFID-based sensor or an RFID.

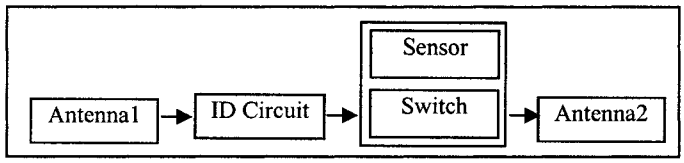


Figure 2.1 Schematic diagram of wireless sensor tag showing receiving antenna (Antenna1), sensor-switch, ID generating circuit and transmitting antenna (Antenna2).

The antenna can be of any configuration such as, Fractal, Hilbert, Triangular, Spiral or Meander. Different antenna designs can be considered for different applications. Transmitting and receiving antennas can be replaced by a single antenna to transmit and receive signals, if we use the back scattering mode for communication or an on board circulator.

The ID circuit (Figure 2.1) contains delay lines either in the form of LC arrays or transmission lines of different lengths. The ID circuit receives a signal from the receiving antenna on the tag when the sensor switch is on, and converts this signal into a time-domain binary code characteristic of the tag number, and sends it to the transmitting antenna on the tag for sending this information to the reader.

Adding a sensor on the RFID, will make the RFID into a simple sensing device defined as an RFID-based sensor. A simple on/off sensor switch has been proposed for our RFID-based sensor configuration and, therefore, the presented RFID-based sensors do not have a dynamic ID generation capability corresponding to different levels of sensed materials. A major obstacle in designing an RFID-based sensor is the power consumption by its sensor. Active/stand alone sensors would solve this problem if they are coupled with passive RFID tags thus making them power savvy. Therefore, our RFID-based sensors are based on a chipless ID code generation circuit and active/stand

alone sensors. The sensor is dormant until the sensed material exceeds the threshold of the sensor, and responds to the reader as long as the sensed level is above the threshold at which point the sensor switch will turn on the RFID. The concept of the proposed tag is elaborated in the schematic diagram shown in Figure 2.2.

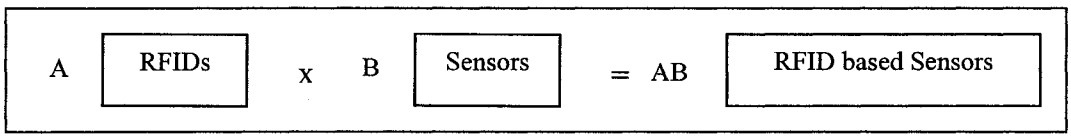


Figure 2.2 Effect of RFID-based sensors having sensor switch on the worldwide net.

If 'A' number of RFIDs are expected to be in use for different identification applications, then incorporating 'B' types of sensing capabilities on them would increase the number of applications about 'AB' times. The value of 'A' approximates to 550 billion, if the current sponsors of Auto-ID centers alone place RFID tags on every item they produce [7]. This above simple calculation justifies the application of the developed RFID systems and RFID-based sensors. If each tag can generate a dynamic ID for 'C' sensing levels, then there will be 'ABC' discrete data points that will be available for processing into useful information. The feasibility of dynamic ID generation corresponding to different sensing levels is discussed in Chapter 7.

2.3 Delay-based RFID Systems

The term delay-based RFID technology is coined because the proposed RFIDs and RFID-based sensors contain an ID generation circuit that generates the required ID code using the time delay present in either LC arrays or transmission lines. The delay-based RFID system, its components, and design equations of the tags have been

presented here. Each type of tag with different ID generation circuit has been dedicated to individual sections in this chapter. Two types of communication schemes are proposed for the operation of delay-based RFID system. They are communication between the tag and the reader using amplitude modulated continuous wave and using on-off-keying (OOK) modulated sinusoidal signal. Description of these schemes along with compatibility with communication regulations are presented in dedicated sections.

Figure 2.3 shows a typical RFID system with delay-based tag. The reader of a typical RFID system, as shown in Figure 1.1, is represented with discrete transmitter and receiver diagrams in this figure for clarity. A transmitter can be as simple as a signal generator connected to an antenna, and receiver can be an oscilloscope connected to receiving antenna. A signal from the transmitter is received by the tag through antenna1, converted into ID code in the delay-based ID generation circuit, and sent to an external receiver through RF switch and antenna 2. Absence of the sensor switch makes the tag an RFID.

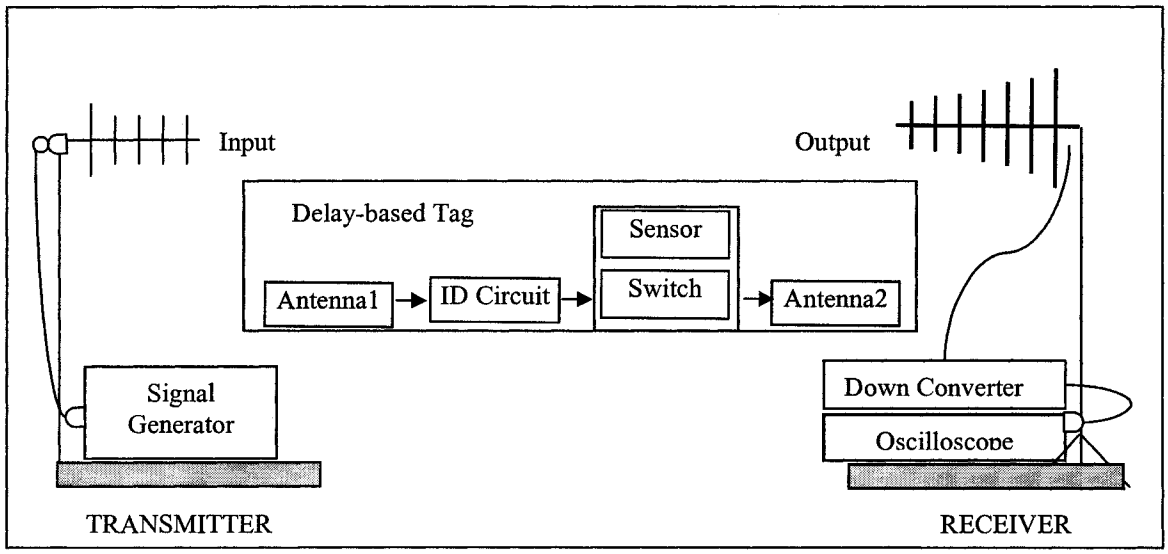


Figure 2.3 Schematic diagram of delay-based RFID system.

2.3.1 Delay Line Concept

It is a known fact that each circuit and element contains some inherent time delay which might or might not be a significant factor influencing their performance. Time delay can also be useful for different applications. Different delay-based circuits are used for filtering, pulse generation and modification, and in digital and mixed mode systems [39]. Optical delay circuitry is gaining significance in gigahertz frequency communications. The delay line concept can be explained as below.

A long transmission line can be represented by an equivalent circuit as shown in Figure 2.3. There exists a series inductance along the length of the transmission line in the conducting wires and capacitance exists across the live wire and the ground wire of the transmission line. These inductances and capacitances exist along the entire length of the transmission line and are the cause for the time delay. The equivalent circuit shown in Figure 2.4 applies to a properly terminated microstrip transmission line.

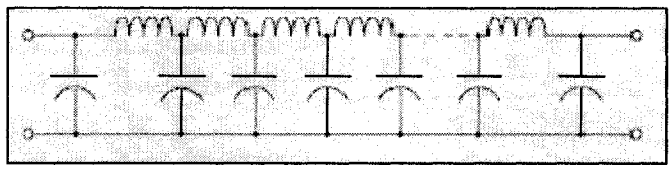


Figure 2.4 Equivalent circuit diagram of a transmission line.

Time delay can also be obtained from a circuit with lumped inductor (L) and capacitor (C) arrays in series with each other representing the above circuit. Since each LC array is capable of producing a fixed time delay and do so without any battery for biasing, these arrays are also known as passive delay lines. A passive delay line is a special purpose low pass filter designed to delay the input by a specified increment of time and is composed of series inductors and shunt capacitors (Figure 2.4) with values

dictated by characteristic impedance [40]. The time delay T_d and characteristic impedance Z_o are given by

$$T_d = \sqrt{LC} \tag{2.1}$$

and

$$Z_o = \sqrt{L/C}\,, \tag{2.2}$$

where T_d is the total delay in seconds, Z_o is the characteristic impedance in Ω, L is the series inductance in henries and C is the shunt capacitance in farads. Equation 2.1 holds good for an equivalent circuit with lumped LC arrays. Such a circuit should be terminated using a resistor of value given by Equation 2.2 so that it represents an infinite length transmission line. This concept is further detailed in Section 4.2.

In electronics and derivative fields such as, telecommunications, a delay line is rigorously defined as a single-input-channel device, in which the output channel state at a given instant, t, is the same as the input channel state at the instant $t-n$, where n is a number of time units, *i.e.*, the input sequence undergoes a delay of n time units, such as, n femtoseconds, nanoseconds, or microseconds. The delay line may have additional taps yielding output channels with values less than n. In other words, the device introduces a delay of a certain amount of time between its input and output [43].

2.3.2 Process of Delay-based ID Generation

Based on Equation 2.1 one can infer that a constant time delay of T_d can be obtained either after a unit length of microstrip transmission line or an LC array constituting an equivalent circuit of a transmission line. If an input signal of width T_d and time period T is sent through either the transmission line or the LC array, tapped at delays that are integral multiples of T_d and superimposed on one another, the resulting signal represent a binary code [44,45]. Different combinations of such codes can be obtained by

different tapping configurations. Figure 2.5 depicts the concept of ID generation using time delay. Generation of 4 bit code 1101 has been depicted in this picture. A half-wave rectified sinusoidal input is tapped at delays T_d, $2T_d$, and 4 T_d and superposed on one another. Any type of input signal will be delayed in the similar fashion. Care should be taken to see that the width of the signal is less than or equal to T_d to avoid overlapping of the signals.

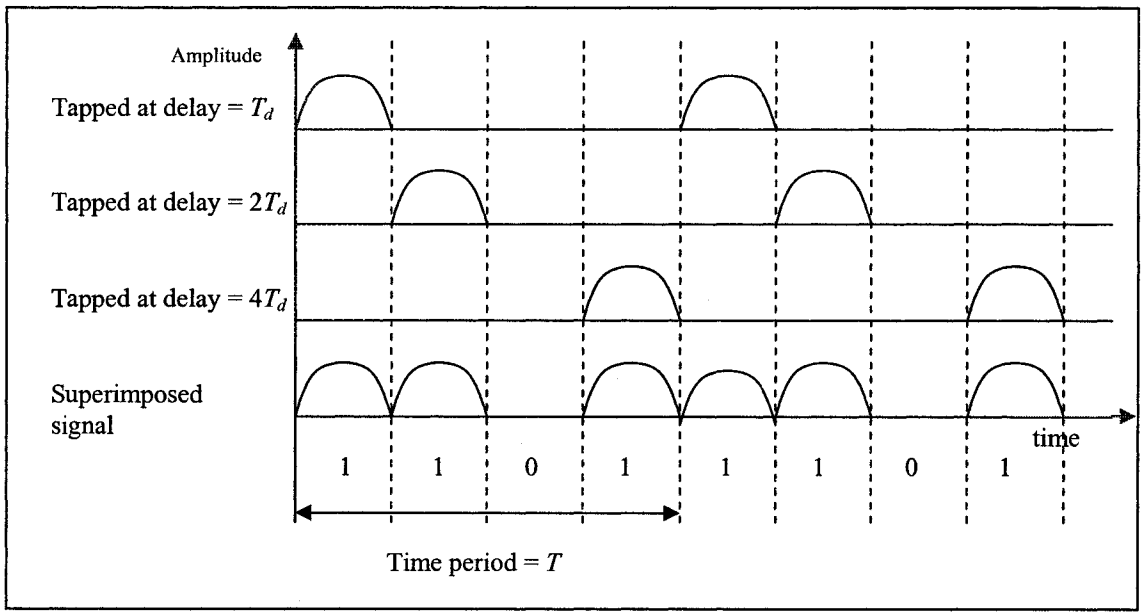


Figure 2.5 Delay-based ID generation by superposing tapped signals at different delay.

2.3.3 Design Equations for Delay-based Tags

As explained earlier, the width of the tag's input signal that represents a binary bit should be less than or equal to T_d, and should have a time period equal to T such that

$$T = nT_d, \tag{2.3}$$

where n is the number of bits required and T_d is given by Equation 2.1. In case of LC-delay-line-based RFIDs, the ID generation circuit shall contain n number of LC arrays each capable of generating T_d obeying Equation 2.1. Layout should be designed such that the signal after each LC array element can be routed on to a single point or a common trace. In case of RFID based on transmission-line delay, the ID generation circuit shall consist of two branches of microstrip transmission line connected to the input. One branch is long and capable of producing a delay of T given by Equation 2.3. This branch is Meandered to decrease the form factor and designed such that each point on the branch after a delay of T_d can be tapped on to the shorter straight branch. The ID generation circuits based on a transmission-line is explained in Chapter 6 while ID generation circuit based on LC delay line has been mentioned in this chapter [35].

Bandwidth of the communication signal is significant in the delay-based RFID systems. Bandwidth of a communication signal depends on the type of modulation and bit rate which in turn depends on T_d. The bandwidth allowed for communication between reader and tag is regulated by the International and regional authorities allocating the frequency bands of the radio spectrum. In the United States, Federal Communication Commission (FCC) regulates the spectrum. Therefore, care should be taken to design tags such that T_d, which corresponds to signal width and therefore, to bandwidth obeys these regulations and have a signal band width less than the limits prescribed. The regulations and different communication schemes are presented below.

2.3.4 Design Equations for the System

A typical delay-based RIFD system is shown in Figure 2.3. As mentioned earlier, the system includes transmitter, tag, receiver and the channels connecting them. The

distances between these components of the RFID system plays an important role in the characterization of the tag as a whole.

Microstrip antennas, whether Fractal, Meander, or Hilbert configurations, are the transducers on the tag that convert electromagnetic energy in their ambient environment to electrical energy in the tag's circuitry and vice versa. In order to accurately measure an antenna's far field performance, the phase of the field across its aperture must be constant to within $\pi/8$ radians. The distance of separation between external transmitting and receiving antennas should be more than $\pi/8$ radians. As the separation increases further, the radius of curvature of the spherical wave front is so large that, for all practical purposes, the phase front can be considered planar over the aperture of a practical antenna.

The variation of the field magnitude across the aperture of the tag's antenna needs to be limited. For a magnitude variation of 0.5 dB or less across the antenna under test, the error in the measurements will be negligible for most applications. It is essential that the external transmitting antenna be accurately directed so that the peak of its beam is centered on the aperture of the antenna under test. Improper alignment, which may not cause a noticeable loss of signal level, might result in erroneous directionality predictions.

Adequate separation (Equation 2.4) between antennas prevents excessive phase errors but increasing the separation to the other extreme might cause large reflections from the ground or other sources of reflection that can produce erroneous gain and pattern measurements. The usual method of minimizing the effects of fields caused by reflections are to (1) mount the transmitting antenna and test antenna sites on towers at a

height greater than or equal to 6D, where D is the maximum test antenna aperture dimension, (2) employ directive transmitting. Usage of linearly polarized directional antennas at the external transmitter and receiver will reduce unnecessary interference of signals to some extent.

For such distance of separation and tower heights, it is advisable to restrict the amplitude taper to the order of 1/4 dB or less by using the criterion [46]

$$d_t \leq \frac{\lambda R}{4D}, \tag{2.4}$$

where d_t is the transmitting antenna diameter, λ is the wavelength, R is the range length, and D is the maximum test aperture dimension. There are both losses and gains in the path of the signal propagation starting from the signal generator, to the transmitting antenna, to free space, through the tag circuitry and back to the oscilloscope. In the proposed delay-based tag system, the external transmitter consists of signal generator and the Yagi antenna. The distance vs. field relation in the far field is linear and inversely proportional to electric field intensity E or magnetic field intensity H.

The received power, P_r at a distance r from the source is given by [47]

$$P_r = \frac{(pqP_tG_t\lambda^2)}{(4\pi r)^2}, \tag{2.5}$$

where p is the polarization compatibility coefficient, P_t is the power transmitted by the external transmitter, G_t is the train of the transmitting antenna, λ is the wavelength of the signal, and q is a constant that depends on scattering effect. We let p as one as we intend to use similar antennas for uplink and down link. Besides the above mentioned values and equations defining the amplitudes and signal strengths, attenuation occurs in cables and adapters due to insertion losses.

2.3.5 Communication Schemes Under Consideration

Two different communication schemes have been considered for delay-based RFID tags. Amplitude modulated continuous wave is used for our initial design of LC-delay-line-based RFID systems. A more FCC compatible OOK modulated sinusoidal wave is used for tag-reader communications for the transmission-delay-line-based RFID system. Both schemes are explained below.

2.3.5.1 Communications using amplitude modulated continuous wave

In this mode of communication a sinusoidal signal of time period T (Equation 2.3) is half-wave-rectified using diodes on the tag or at the external transmitter (Figure 2.3). This signal is converted into binary code by superimposing the signals of delay equal to integral multiples of T_d given by Equation 2.1 and Equation 2.3. This mode of communication scheme will have a narrow bandwidth as there is no modulation of input signal. However, the output from the tag resembles an amplitude modulated continuous wave similar to that used in Morse coded telecommunication [47]. This communication scheme is further explained in Section 2.4 with respect to the LC-delay-line-based RFID system. Such a code can easily be transmitted through air because of the higher frequency but might not result in a reliable communication due to the noise present in the channel. Present stringent FCC regulations might not allow usage of such communication. However the signal obeys bandwidth, emission and other limits specified by the FCC.

2.3.5.2 Communications using on-off-key modulated sinusoidal wave

In communications using OOK modulated sinusoidal wave, a pulse of pulse repetition frequency (PRF) equal to T and width equal to T_d is used to control an RF switch that switches the output from a signal generator. The sinusoidal signal from the signal generator has a frequency in the UHF range. When transmitted from the external transmitter, the modulated envelop gets delayed in the ID generation circuit of the tag and superimposed to represent binary code. This scheme is explained further with respect to the transmission-delay-line-based RFID system in Section 2.5.

2.3.6 International and FCC Regulations

There are international, regional and national organizations to regulate the radio signals in the air. The International Telecommunication Union (ITU) consists of virtually all independent nations as members and manages the worldwide radio frequency spectrum and publishes a table of international frequency allocations. Even though ITU fosters cooperation between different regional and national bodies, it is the various regional and national bodies that set and administer actual band allocations and emission limits. Since immediate RFID markets exist in the United States, Europe and Japan, individual allocations and emission limits are presented here. The European Telecommunication Standard Institute (ETSI), established in 1988, is responsible for developing telecommunication standards in Europe (ESO), while Federal Communications Commission (FCC), and Association of Radio Industries and Businesses (ARIB) regulate the spectrum in the United States and Japan, respectively.

Table 2.1 Allowable frequency ranges for RFIDs in air.

Frequency	Bandwidth	Region
9-135 KHz		In most regions
6.765 – 6.795 MHz	+/- 15 KHz	Worldwide (approval required)
13.553 – 13.567 MHz	±7 KHz	Worldwide
26.975 – 27.283 MHz	± 163 KHz	Worldwide
40.66 – 40.70 MHz	± 20 KHz	Worldwide
433.05 – 434.75 MHz	± 870 KHz	European countries
865 - 868 MHz	± 125 KHz	European countries
902 – 928 MHz	± 13 MHz	Americas (250/500KHz FH)
2.4 – 2.5 GHz	± 50 MHz	Worldwide
5.725 – 5.785 GHz	± 75 MHz	Worldwide
24 – 24.25 GHz	± 125 MHz	Worldwide

RFID systems are considered as Short Range Devices (SRD) which means radio transmitters that provide unidirectional or bidirectional communications and which have low probability of causing interference to other radio equipment. These devices are allowed to operate in frequency bands known as Industrial, Scientific and Medical (ISM) bands designated by ITU. The principal ISM bands are given in Table 2.1. The 865-869 MHz band in Europe does not come under the ISM band but is proposed for the use of RFIDs and other SRDs.

Most of the RFIDs presented in this work have been designed at 915 MHz and with FCC regulations in mind. A 13.56 MHz RFID system is also designed and explained elsewhere. All the UHF tags work with far-field coupling. In the Americas, the UHF frequency band of 902 to 928 MHz 250 or 500 KHz channels can be used if Frequency Hopping (FH) communications is used. For most of the frequencies, the FCC specifies emission limits in terms of radiated power or far-field electric field. Besides allocating the frequency bands, the FCC also specifies radiation, and bandwidth specifications. Table 2.2 shows these specifications for the 915 MHz and 13.56 MHz bands.

Table 2.2 FCC regulations for 13.56 MHz and 915 MHz ISM bands.

Frequency Band	Electric Field Strength	Type of Detection
13.56 MHz ± 7 KHz	10,000 uV/m, at 30 m	Quasi – peak
13.56 MHz ± 7 KHz	30 uV/m at 30 m	Average
902-928 MHz	50 mV/m at 3 m	Quasi – peak
902-928 MHz	500 uV/m at 3 m	Average

FCC specifies that outside the 13.56 MHz band, emissions must not exceed 30 uV/m at 30 m. There is a restricted radio-astronomy band at and below 13.41 MHz where only spurious emissions are allowed. Similarly, for the 902-928 MHz band there is a limit of 500 μV/m at 3 m for harmonics detected using the quasi peak detector method. At UHF and microwave frequencies, limits are usually specified in radiated power as EIRP. This radiated power is called effective isotropically radiated power (EIRP) given by [47]

$$EIRP = G_t P_t, \tag{2.6}$$

where G_t is the gain of the transmitting antenna with respect to the isotropic antenna and P_t is the net input power. In the 915 MHz, 2.45 GHz, and 5.8 GHz regions, spread spectrum operation, including frequency hopping and direct sequence, may be permitted. Typically, both narrow band and spread spectrum are allowed by the administrations within these bands. There are a number of changes recently proposed in the 900 MHz and 2.45 GHz regions. Table 2.3 shows the FCC limits in terms of EIRP for the 902-928 MHz band. The proposed layouts for the delay-based tags can also be made for other frequencies and are discussed in Chapter 7.

Table 2.3 FCC Regulations for UHF frequencies in EIRP.

Frequency	Bandwidth (20dB)	Channels	Power (EIRP)
902-928 MHz	< 250 KHz	≥ 50	4W
902-928 MHz	< 250 KHz, ≤ 500KHz	≥ 25	1W

2.3.7 Compatibility of Communication Schemes under Consideration

The amplitude modulated continuous wave based communication scheme explained in Section 2.3 has many disadvantages. Even though such a scheme existed some time back, it is used in wired telecommunications only. Moreover, due to the usage of half-wave rectified sinusoidal wave as input to the tag, the rise and fall time of the signal can never be steep as compared to a digital pulse. Due to the overlap of signals, realization of intermediate zeros in the code becomes difficult as the required number of bits to be generated increases. Such a signal sent through wireless means might result in a low modulation index. Only half of the time period is used to generate bits, which further makes it complex to generate a greater number of bits.

The OOK modulation method obeys all the regulations specified by the FCC for the UHF range. Since a digital signal is made up of multiple signal pulses of the same duration and thus same frequency, its bandwidth is the same as the bandwidth of a single signal pulse. Therefore, the bandwidth of a digital signal is actually determined by the signal pulse it uses which are its pulse width and its shape. Since one pulse is used for one bit, the pulse width is proportional to the bit duration and inversely proportional to the bit rate. Therefore, in digital systems the bandwidth and bit rate and, therefore, the pulse width are proportional. The general expression which links bandwidth and bit rate of a digital system is given by

$$B = a \times R, \tag{2.7}$$

where B is the bandwidth required for relaying a digital signal with a bit rate of R bits per second and 'a' is a constant such that $0.5 < a < 1$, and depends on the pulse design [47]. Therefore, care should be taken while determining the width of the bit which is less than or equal to T_d such that it obeys the bandwidth regulations of the FCC.

2.4 LC-Delay Line Based RFID System

An LC-delay-line-based RFID system contains a reader, LC-delay-line-based RFIDs and/or RFID-based sensors. They communicate with each other in a similar way, as explained in Section 1.1. Figure 2.6 shows the external transmitter and receiver that constitute the reader and LC-delay-line-based RFID tag. The principle of operation of the LC-delay-line-based RFID system is explained in the following paragraph with the help of an amplitude modulated continuous communication wave.

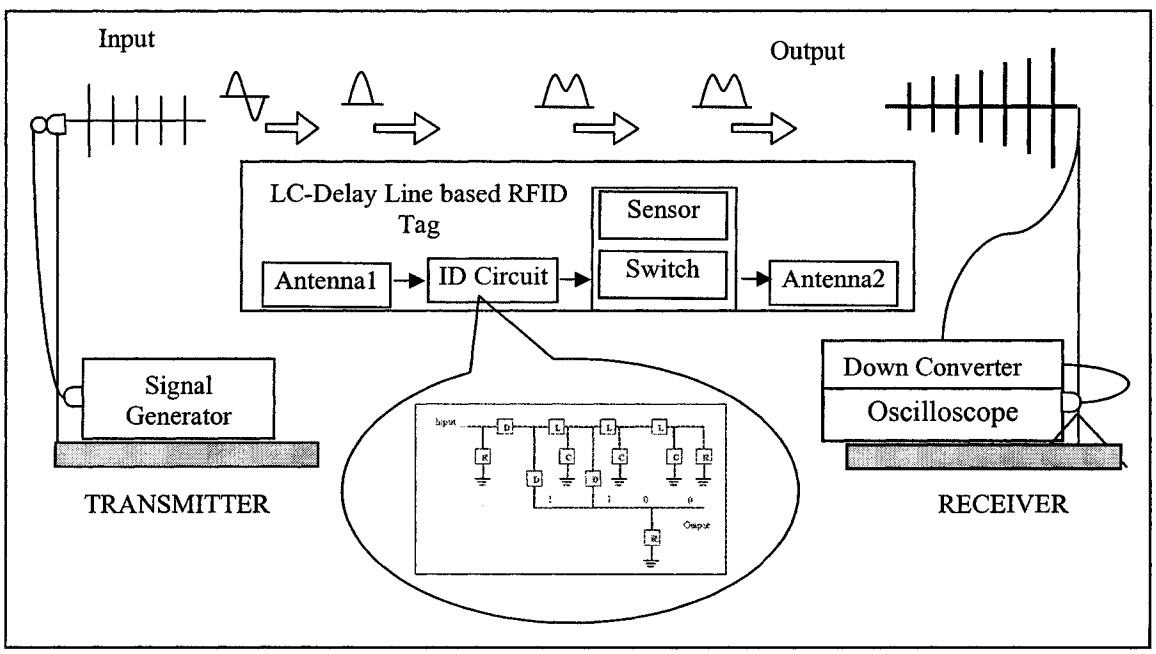


Figure 2.6 Schematic diagram of a typical LC-delay-line-based RFID system.

In the proposed system, a 915 MHz sinusoidal signal will be transmitted from an external transmitter. Antenna1 receives the signal and sends it to the ID circuit (Figure 2.6 and Figure 2.7) when the sensor switch is on for the case of the RFID-based sensor and directly to the ID circuit for the case of the RFID. The rectifying diode in the ID circuit rectifies the incoming sinusoidal signal and sends it to the LC arrays where the signal gets delayed [35].

The signal is tapped after the designated LC delay elements corresponding to the required bit code, and connected to the load through the diodes. In Figure 2.7, taps corresponding to the bit code 1100 are shown. The values of the delay elements L and C are determined based on the number of bits needed to be generated during one time period of the input sinusoidal signal. The generated output will be transmitted through tag's antenna2 to the external receiver which is connected to the oscilloscope to observe the output.

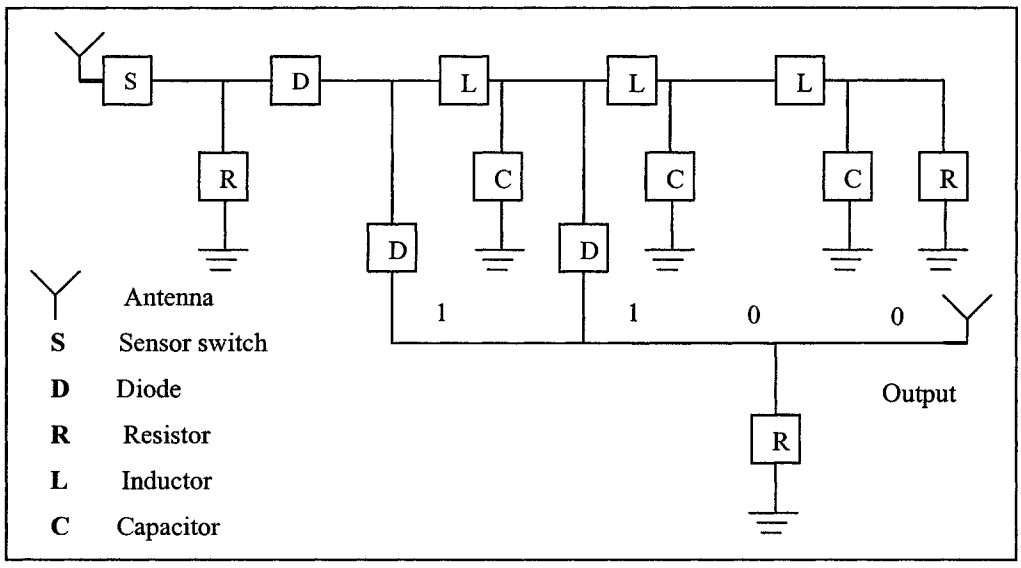


Figure 2.7 Circuit diagram of LC-delay-line-based RFID/RFID-based sensor [35].

2.4.1 LC Delay Line Based RFIDs and RFID Based Sensors

An LC-delay-line-based RFID has a receiving antenna, ID circuit and transmitting antenna all in series with each other as shown in Figure 2.6. The tag is similar to its chip-based counterpart and is always responding to the reader that is in the vicinity. This tag is passive and has no battery on board. Such tags can be used just like chip-based RFIDs for applications such as, supply chain and inventory management.

An LC-delay-line-based RFID-based sensor, on the other hand, contains a sensor switch in series with the rest of the RFID circuit, as shown in Figure 2.4. The switch turns 'ON' when the sensed material reaches above the sensing threshold of the sensor and acts as a short between the ID circuit and tag's transmitting antenna, thus making it operate like an RFID. The tag is still passive as the sensor placed on the tag requires no power from the tag and can stand alone. The sensor is either active or can stand alone as a switch, thus eliminating the need for input power from the tag for its operation.

2.4.2 Elements of LC-Delay Line Based Tags

The LC-delay-line-based RFID/RFID-based sensor contains mainly transmitting and receiving antenna/antennas, an LC-delay-line-based ID generating circuit, and/or sensor switch. Antennas can be of any model such as, Hilbert, Meander, Spiral and Triangular. As shown in Figure 2.7, the ID generating circuit based on the LC delay line concept [39] has passive elements such as, resistors, inductors and capacitors and diodes. Each set of LC circuits is designed to produce a delay corresponding to bit width. The sensor can be any active/stand alone component. The design fabrication and characterization of these devices and components are explained in Chapter 4.

2.4.3 Compatibility with Communication Schemes

Tags presented in this dissertation are made for the 915 MHz UHF range and with FCC regulations in mind. LC-delay-line-based RFID/RFID-based sensor can be made to operate on either amplitude modulated continuous wave communication signal or OOK modulated sinusoidal communication signal as explained in Section 2.3. Tags made for the former communication scheme are small in size as the planar inductors and capacitors under the proposed design are made for delays that are a fraction of the time period of the 915 MHz signal. Tags for LF and HF ranges can be realized for this scheme using lumped off-the-shelf components. LC-delay-line-based tags made for OOK communication, are large in size under the proposed design due to limits on maximum usable bit rate set by the FCC which, in turn, causes a limit on the usable bit width. Therefore, large planar inductors and planar capacitors are to be designed to obtain the required delays at 915 MHz. The size of the tag increases significantly as the frequency of operation goes down to LF and HF ranges. Off-the-shelf lumped components can be used for realizing LC-delay-line-based LF and HF tags of moderate size.

2.5 Transmission-delay-line-based RFID System

The transmission-delay-line-based ID generation circuit, when properly connected with antennas, can wirelessly receive the input signal from a reader, delay it and send it back to the reader. This can be considered as a simple transmission-delay-line-based RFID. When attached to a sensor switch, it acts as an RFID-based sensor where the tag works as an RFID only when the sensor switch is on. The proposed transmission-delay-line-based RFID system contains an external transmitter and receiver that constitute the

reader and transmission-delay-line-based RFIDs and/or RFID-based sensors (Figure 2.8). Either type of communication scheme explained in Section 2.3 can be implemented in this system. However, operation of the transmission-delay-line-based RFID system can be explained with the help of OOK modulated sinusoidal wave and by the Figure 2.8. A single antenna is used on the tag for transmitting and receiving the signal from the external reader.

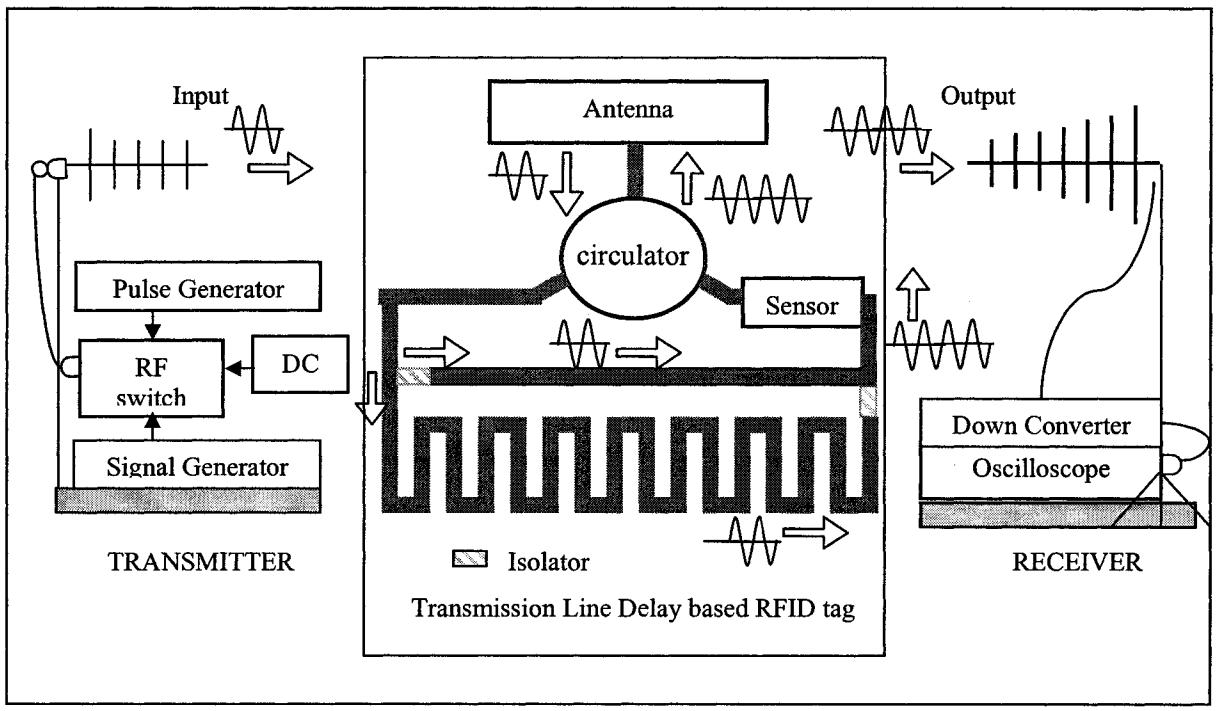


Figure 2.8 Schematic s ical transmission-delay-line-based RFID system.

The external transmitter for the communication scheme using OOK modulated sinusoidal wave, consists of a signal generator, RF switch, DC supply and a pulse generator. The signal generator supplies a carrier frequency at 915 MHz to the RF input of the RF switch. The DC supply needed by the RF switch is provided by the DC power supply. The on and off duration of the RF switch is controlled by supplying a pulse from

a pulse generator. In this way a train of sinusoidal signals are produced at the RF output of the RF switch known as the OOK scheme. This output is fed to the transmitting antenna.

When the sensor switch is 'ON', the modulated sinusoidal signal is received by the transmitting/receiving antenna on the tag. The received signal is sent to the ID generation circuit through a circulator. The input fed to the ID circuit travels along two parallel paths, as shown in Figure 2.9. One travels through a straight, relatively shorter transmission line and other along a lengthier transmission line that is meandered to reduce the form factor. The signals are taped along the Meander line via isolators connected to the shorter transmission line according to the required ID code. The generated code contains a modulated signal with new bits in the OOK scheme. Figure 2.9 shows the generation of 2 binary code bits 1 and 1 followed by zeros. This model is explained in Chapter 6 through simulations using Ansoft Designer electromagnetic simulation software [40].

2.5.1 Transmission-delay-based RFIDs and RFID-based Sensors

Figure 2.9 shows the schematic diagram of a typical RFID tag. The tag can be a transmission-delay-line-based RFID-based sensor or RFID based on the presence or absence of the sensor switch. Transmission-delay-line-based RFIDs contain antenna/antennas connected to the ID circuit which is based on transmission-line delay. A Circulator on the tag eliminates the possibility of signal interference at the antenna as the latter does both receiving and transmitting. Isolators are used to avoid interference between the transmission line branches of the ID generation circuit and are explained

earlier. Adding a sensor switch in between the tag antenna and the ID generation circuit results in an RFID-based sensor based on transmission-line delay. The RFID can always respond to the interrogation signal from the reader while the RFID-based sensor does so only when the switch is 'ON'.

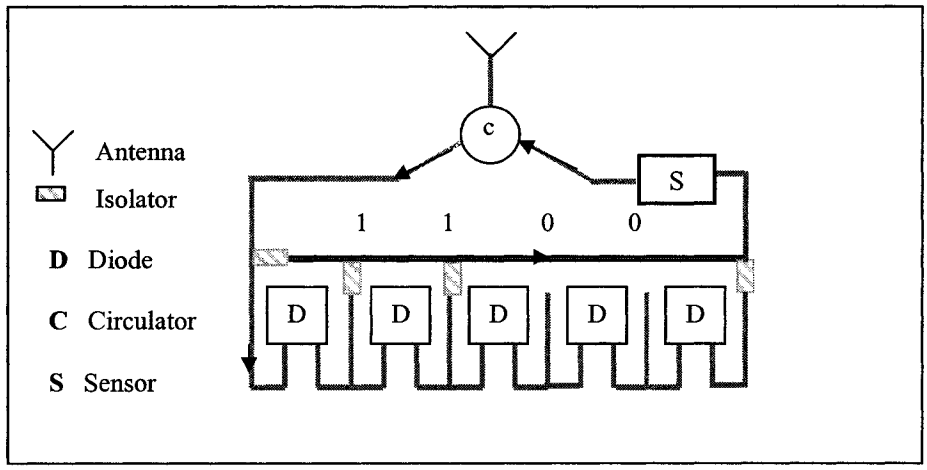


Figure 2.9 Circuit diagram of transmission-delay-line-based RFID tag.

2.5.2 Elements of the Transmission Delay-line-based RFID tags

All the elements of a typical transmission-delay-line-based RFID/RFID-based sensor are shown in Figure 2.9. The tag consists of an antenna such as, Fractal, Hilbert, Meander and Spiral, and an ID generation circuit based on transmission-line delay and/or a sensor switch. A terminating resistor of value equal to the characteristic impedance is required at the end of the Meandered branch (Figure 2.8) of the ID generation circuit to avoid reflections. The ID generation circuit can be matched to properly tuned antennas with input impedance equal to the characteristic impedance of the transmission lines. Isolators are used for tapping the signal for bit code generation as explained earlier.

Isolators and circulators can be replaced by diodes and FETs by modifying the modulation scheme, which is explained in Chapter 7.

2.5.3 Compatibility with Communication Schemes

Either type of the communication schemes considered in Section 2.3 can be implemented in a transmission-delay-line-based RFID system. Tag size will be a few square centimeters for implementing the communication scheme with amplitude modulated continuous wave. This is because time delays which are a fraction of 1.1 ns are required for bit generation. 1.1 ns is the time period that corresponds to a sinusoidal signal of 915 MHz. However, careful design is required so as not to populate the RFID tag with isolators that interfere with each other's performance.

Under the proposed tag design, tags of a few square inches are to be made to comply with the communication scheme with OOK modulated sinusoidal wave signal, and the FCC regulations for such scheme. These are relatively large compared to those implemented for the other communication scheme explained in the earlier paragraph. Tags of LF and HF frequencies can be fabricated in principle using off-the shelf passive chip delay elements.

2.6 Fabrication Processes for Delay-based Tags

The proposed delay-based RFID technology will not be successful if the manufacturing costs are high. This aspect is given prime importance during the design of RFID and RFID-based sensors based on LC-delay-line and transmission-delay-line schemes. The design is made simple to fabricate and, at the same time, capable of producing bits in the time domain as explained in this chapter. Much of the components are designed to be planar and realizable in the integrated form. Some components such

as, isolators, circulators, and diodes could not be eliminated in the present tags and are implemented by assembling off-the-shelf components on to the tag layout. While the proposed low-cost fabrication processes with which these tags are realized are not similar to the standard processes followed by the chip-based RFID industry, delay-based tags can also be manufactured using industry standard manufacturing methods. Both sets of processes are discussed in Chapter 3.

CHAPTER 3

PROPOSED FABRICATION PROCESSES

3.1 Overview

The need for low-cost manufacturing of RFIDs and RFID-based sensors has been discussed in Sections 1.3 and Section 1.4 of Chapter 1. This chapter describes the different low-cost fabrication processes considered to realize the tags, their merits, limitations, and compatibility to over all process integration. While cost is the main criterion in the selection of material and processes, reliability and stability of the materials and processes is given considerable importance. Conventional photolithography and other associated methods have also been implemented in the realization of the tag layout in order to assess the compatibility of delay-based tags with the fabrication technology of the present day silicon-based electronic industry. The materials and processes that are considered for the realization of the tags have been explained below.

3.2 Materials under Consideration

Different material options for building devices and components that are required for the fabrication of RFID tags and RFID-based sensors and their components, have been explained here. Each section includes experiments performed to characterize the materials and draws conclusions from the results. Both solid state and organic materials are considered with the cost and reliability of the materials as the main selection criteria.

3.2.1 Substrates

Polyimides and polyesters are well known for their RF performance while polyethylene-terepthalates (PET) are known to be successfully used as substrates for flexible electronic device fabrication [20, 48]. Polyimide substrates are known for their thermal stability and chemical inertness but are relatively high in cost. Polyester substrates, on the other hand, offer cost flexibility but are not stable above 200°C. Many researchers fabricated devices on PET and other transparency materials that have thermal stability comparable to Polyesters [49].

Table 3.1 Description of the different types of flexible substrates under test.

Sl No.	Identification Code	Description
1	C3834A/40/FF	Hewlett Packard Inkjet Transparency
2	CG6000	3M Multi-Purpose Transparency
3	CG5000	3M Laser Printer and Copier Transparency
4	PP2200	3M Normal Copier Transparency
5	CG3460	3M Color Ink Jet Transparency
6	CG3700	3M Laser Jet Printer Transparency
7	CG3480	3M Ink Jet Normal Printer Transparency
8	753-621	Office Depot Write-On Transparency
9	753-371	Office Depot Black & White Copier Transparency
10	753-381	Office Depot Ink Jet Transparency
11	200 E	Dupont Kapton Polyimide Sheet

Flexible substrates of different prices, and properties have been chosen to test the thermal stability and chemical inertness to commonly used solvents of the electronics industry. Table 3.1 gives a list of different flexible substrates chosen for tests on their thermal stability, surface roughness, and chemical inertness. The experimental results are explained in this section. Most of the substrates are predominantly PET with varying

degrees of thermal stability and chemical inertness. Kapton 200E, on the other hand, is a polyimide film used as a substrate in flexotronic applications. The properties of polyimide substrates are explained in detail in Section 3.5.

3.2.1.1 Surface characterization

There are many types of flexible substrates with varying barrier and thermal properties. Surface morphology of a substrate defines adhesion and interface properties with other materials. Using a Roughness-Step-Tester, (Wyko Inc., presently Veeco Inc.), flexible substrates under consideration (Table 3.1) are characterized for relative significance of their physical properties such as, surface roughness and waviness. Further experiments are done to modify the substrate's surface for controlling the roughness to meet required values. Figure 3.1 shows the relative average roughness of these substrates.

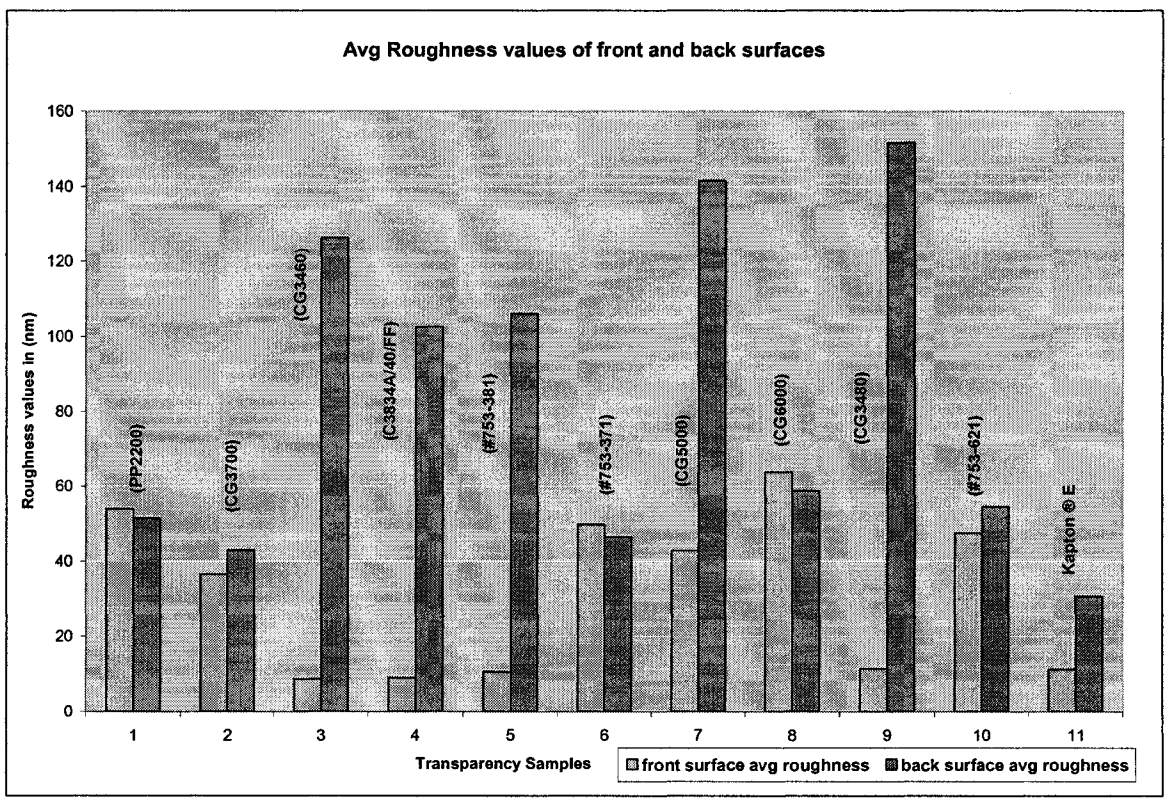


Figure 3.1 Average roughness values of the flexible substrates under consideration.

3.2.1.2 Thermal and chemical sensitivity tests

Flexible substrates can be successfully used for organic and metal deposition and processing for device fabrication. Organic polymer electronic devices consume more energy as compared to their silicon counterparts. Moreover, RF devices need substrates of higher thermal stability. With a goal to find a substrate that can withstand a minimum of 150-250°C without any physical deformation and suitable for device fabrication, thermal stability experiments were conducted on all eleven types of substrates (Table 3.1). Samples of each substrate one square centimeter in size are heated to their melting temperatures on a hotplate. Results obtained from the tests are tabulated in Table 3.2.

Table 3.2 Effect of common solvents and temperature on the flexible substrates.

Sl no.	Sample	thermal stability (°c)	DMF	NMP	VM652	water
1	Dupont Kapton® 200B	325				
2	3M hP Laser Jet Printer CG-3700	150				
3	HP color inkjet printers CG-3460	145				
4	normal copier PP2200	126				
5	3 M LP n Copiers CG 5000	156				
6	office depot color ink jet t 753-381	152				
7	office depot b&w copier 753-371	153				
8	3 M inkjet CG-3480	111				
9	3 M multipurpose CG-6000	154				
10	Office Depot Write on 753-621	141				
11	HP inkjet (c3834A/40/FF)	170				

No effect after 4 days White depostion after 4 days White deposition after 1 day Immediate attack

Both the polymers and the constituent solvents that are used for making polymer electronic device could have an effect on the substrate, and the substrate itself might affect the device material. Therefore, the substrates under consideration are tested for their chemical sensitivity to common solvents such as, dimethylformamide (DMF), N-methyl pyrrolidone (NMP), water, methanol and VM652. These tests would further help in choosing the substrates that can be used in the fabrication of polymer electronic devices. The solvent effect on the substrates was observed by optical microscopy and RST each day and the observed results are tabulated in Table 3.2.

3.2.1.3 Observations

From the above experiments, it is clear that Kapton 200E polyimide film has higher thermal stability and chemical inertness compared to the other films. However, the surface of Kapton 200E is too smooth and might need chemical or mechanical roughening for electroless deposition of copper or other metals, which is one of the proposed deposition methods for RFIDs. This is because the polyimide surface must be sensitized to adhere to the catalyst that initiates the electroless deposition. Kapton VN polyimide films have a rougher surface and almost similar characteristics of Kapton 200E. These polyimide films are analyzed at length later. Polyesters or other low cost substrates given in Table 3.1 can also be used for making RFIDs depending on the process and application requirements. We used polyimide films such as, Kapton 200E and Kapton 500VN, which are known to be good substrates for RFID and RFID-based sensor applications, as a precaution for optimal stability with respect to the tentative set of proposed processes. Polyesters, which are of low cost compared to polyimides and have moderate properties, can also used for RFID applications such as, our tag, once a

complete prototype is made and the power and thermal issues associated with it are resolved. Experiments have been carried out to coat the surface of the transparencies with polyimide to emulate the surface characteristics of a polyimide film. These experiments are explained in Section 3.3.1.

Kapton polyimide films are available in many forms. Researchers have been trying to improve adhesion between polyimide films and evaporated copper [50,51]. Kapton H, HN, E and VN films are used for metallization, particularly for copper. Kapton H and HN films are the original older versions of polyimide and have relatively less dimensional stability. A typical HN film changes by 1.4% of its dimensions at 400^0C while a VN film changes only by 0.25% [52]. They vary in texture compared to the E and VN films. Processes have been developed by the manufacturer to release the stress in the polyimide films and E and VN films are more stress free. Kapton E films are also known as TAB E films because they are used in TAB applications where fine copper lines are metalized on these films and they will not migrate at elevated temperatures such as, 400^0C. Because of the above mentioned reasons, Kapton VN films are chosen for the fabrication of RFIDs and RFID-based sensors. Kapton 500VN film of the Kapton VN family of substrates that corresponds to a five mil thickness can be easily loaded into a desk-jet printer with 'transparency' setting enabled and toner can be printed for device fabrication purposes which will be explained later.

3.2.2 Conducting Materials

Metals, metallic nanoparticle inks and conductive polymers are known to be suitable conducting materials for flexible electronic circuits and devices. These materials are used to fabricate antennas, wireless components, interconnects, contacts and devices

such as, planar inductors and capacitors. Gold and silver nanoparticle inks are expensive and their printing is a time consuming task. Conductive polymers are inexpensive but their printing still consumes a lot of time. Physical vapor deposition (PVD) is a process which gives good quality metal patterns but is expensive. Metals like copper can be deposited electrolessly which is simple and inexpensive.

Experiments have been done to deposit metals such as, aluminum, copper and conducting polymers such as, polyethylenedioxythiophene (PEDOT) and polypyrrole on flexible substrates. Copper is deposited on flexible substrate using PVD for comparing the quality with electrolessly deposited copper. The sheet resistances of the planar resistors patterned xerographically and deposited using electroless copper deposition resistor structures and direct printing of conducting polymers have been compared with that of elemental copper in Table 3.3. According to the available literature, sheet resistances of 350 Ω/square to 2000 Ω/square are common for PEDOT/PSS films and approximately 1.2 Ω/square are reported for electroless deposited copper.

Table 3.3 Sheet resistance values of conductive materials obtained through experiments.

Sl. No	Conducting Material	Sheet Resistance /square
1.	PVD Copper	8.4×10^{-3} .....[53]
2.	Electroless Copper	1.26
3.	PEDOT/PSS Conducting Polymer	3.8×10^{3}
4	Polypyrrole	45.7×10^{6}

The values reported in Table 3.3 are approximated because rough calculations were used to calculate the sheet resistance of printed conducting polymers. The printed patterns using a desktop printer (HP desk-jet 1200 Series) are rugged and vary in width

and thickness in the order of few microns. Therefore, average values of the measured dimensions and resistances are taken and the sheet resistance is calculated. The difference in the obtained sheet resistances values is attributed to the surface non-uniformity of the thermally untreated patterns. The change in the resistance with respect to the thickness of the pattern can be seen in Figure 3.2 for two coats and 15 coats of polypyrrole, printed using the desk-jet printer. Therefore, it was decided that electroless copper might be a better deposition choice in the fabrication of devices and interconnects with its sufficiently moderate conductivity and ease of fabrication.

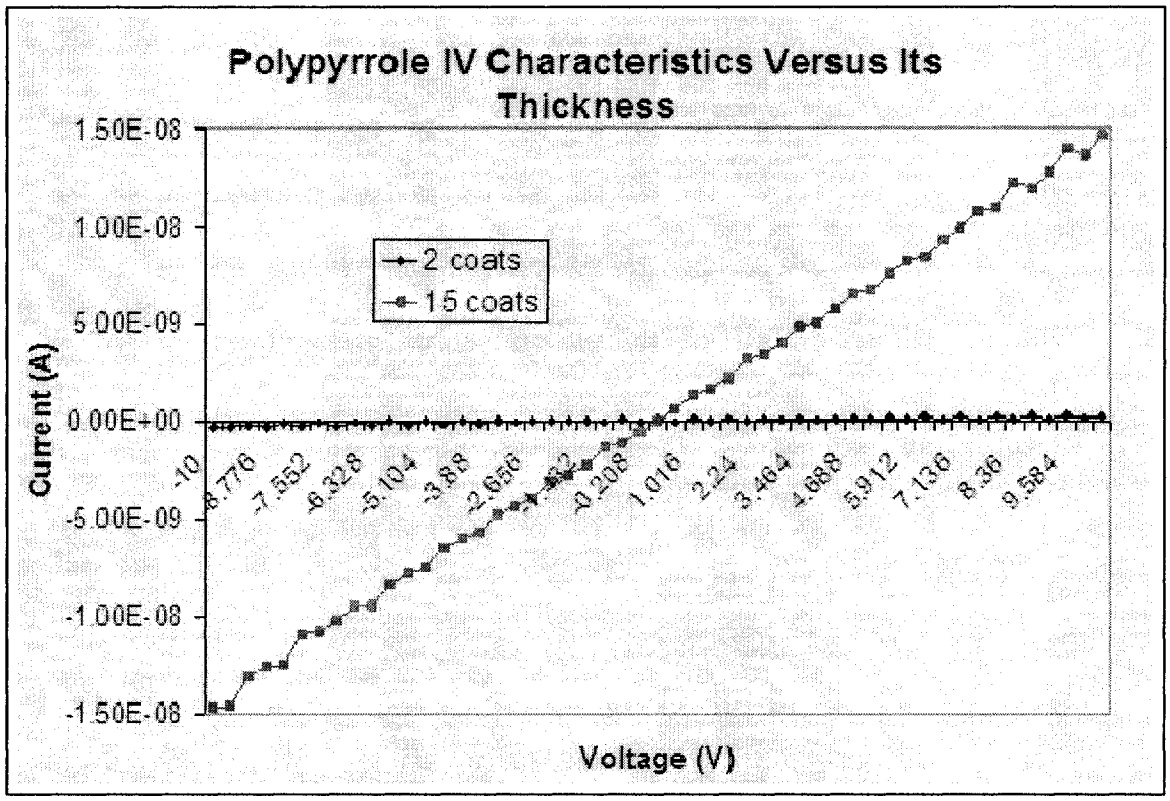


Figure 3.2 Measured current-voltage characteristics, indicating change in resistance with respect to the number of layers of printed polypyrrole.

3.2.3 Semiconducting Materials

Semiconducting polymers are required for the channel material of FETs and in the fabrication of devices such as, diodes. As explained in the earlier chapter n-type semiconducting polymer materials are very unstable in air and water and require a vacuum environment for their use in device fabrication and for stability of the fabricated devices, P-type semiconducting polymers are more stable. P-type materials such as, doped polypyrrole, PEDOT doped with PSS are considered for our device fabrication as they are stable in atmosphere and are commercially available at low cost. These polymers can be printed using a commercial desktop printer by replacing printer ink in the cartridge by PEDOT/PSS solution, a method which is explained later in this chapter.

3.2.4 Insulating Materials

Many polyimides and epoxies are available which can be either spin-coated or dip-coated or spray-coated on flexible substrates and are best known for their insulating properties. They can be cured thermally or with U.V light. Polyimide (PI6858) is used as an insulating intermediate layer in the microfabrication of devices and ultra fast epoxy encapsulant (Dymax 9008) is a general purpose product for encapsulating and sealing electronic components for chip-on-flex applications. They have similar thermal expansion coefficients compared to copper (Table 3.4), oxidation protection capabilities, and moisture resistance and are chosen as encapsulant and protective coatings for the proposed device components and the tag.

Table 3.4 Thermal expansion coefficients of insulating materials used in the experiments.

Sl. No	Insulating Material	TCE
1.	Polyimide	16
2.	Epoxy	15-100
3.	Copper	16-17

3.3 Fabrication Processes under Consideration

Different cost effective processes that can be applied to the fabrication of low-end RFIDs and RFID applications have been presented here. Different electroless copper deposition methods have been tried and are explained in detail. Some of the deposition techniques need surface conditioning. Surface conditioning is also required to control the adherence of polymers printed on the substrates. Other methods such as, spray coating and plate-through hole technique for the ground connections of the RFID circuit have been explained later. Reliability and compatibility with mass production strategies are some of the other criterion besides cost in the selection of the processes described below.

3.3.1 Surface Modification

Many of the substrates described in Section 3.2 are commercial ink-jet and laser-jet printer transparency films and they are readily attacked by commonly used polymer solvents such as, DMF and NMP (Table 3.2). A buffer coating on the surface that is inert to such solvents would help in eliminating this solvent attack. Further, the coating should ideally facilitate the printed patterns to adhere properly to the coated surface of the substrate and act as a barrier to the unwanted diffusion of molecules. Polyimides are proven to be chemically inert to the above mentioned solvents and a polyimide film of sufficient thickness coated on the transparency films should, therefore, make the

transparencies offer some chemical inertness to the common solvents. Commercially available liquid polyimide solution contains NMP as solvent and, therefore, the characteristics of the polyimide buffer film are controlled by varying the relative concentration of NMP in the solution. However, buffer coatings on some of the transparency films resulted in poor surface properties such as, non-uniformity and poor adhesion. Figure 3.3 shows the edge of a polypyrrole pattern printed on polyimide coated 3M laser printer transparency film. The high boiling point of some of the constituents of the liquid polyimide and low melting point of the transparency film demands a careful recipe for thermal treatment of the polyimide coated transparency film. The polyimide from Sigma Aldrich is in liquid form, and starts polymerizing at just 35°C (90 F). The NMP solvent of the polyimide solution has a boiling point of 202^0C. Since this high boiling point is unsuitable for transparencies, complete thermal treatment of the polyimide buffer layer on the transparencies could not be accomplished. This might be one of the reasons for the resulting poor surface characteristics. The improper recipe rendered the surface of the 3M laser printer transparency film hydrophobic and thus resulting in poor adhesion to water based polypyrrole patterns. It can be seen that the pattern is not continuous and cracks have developed after 20 days when left unprotected. The characteristics of printed patterns on other polyimide coated transparencies were also unsatisfactory. Moreover, this buffering will not help in increasing the melting point of the film.

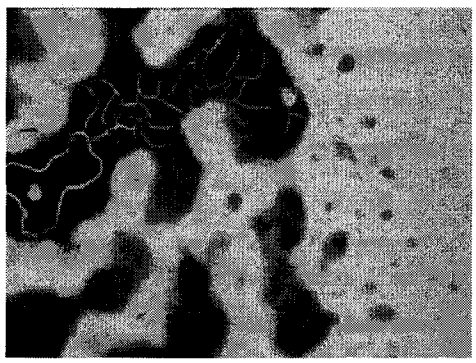


Figure 3.3 Edge of a polypyrrole pattern on the polyimide coated 3M laser jet printer transparency (picture taken using Optimus measurement system).

Thin film transistors that are made on glass substrates, Kapton films and clear polyimide films have all shown similar device characteristics. The similarities are attributed to similar surface parameters such as, roughness and waviness. Experiments with the coating polyimide on transparency films gave poor results, as explained earlier. But polyimide buffer solution can still be used to engineer the surface roughness of Kapton polyimide substrates themselves because devices of different scale require different surface characteristics.

Liquid polyimide has been coated on Kapton 500VN sheets using a spray coating technique and the coated substrates are thermally cured at 300^0C. Cured samples are coated with a thin layer of black gold to improve the reflectivity of the films for roughness measurements using an optical interferometer (Roughness and Step Tester, Veeko Inc). Figure 3.4 shows the change in surface parameters with an increasing number of polyimide coatings on the Kapton 500 VN substrate. Controlling the surface properties is also required for proper adhesion of the toner for xerographic printing techniques, which will be explained later in this chapter.

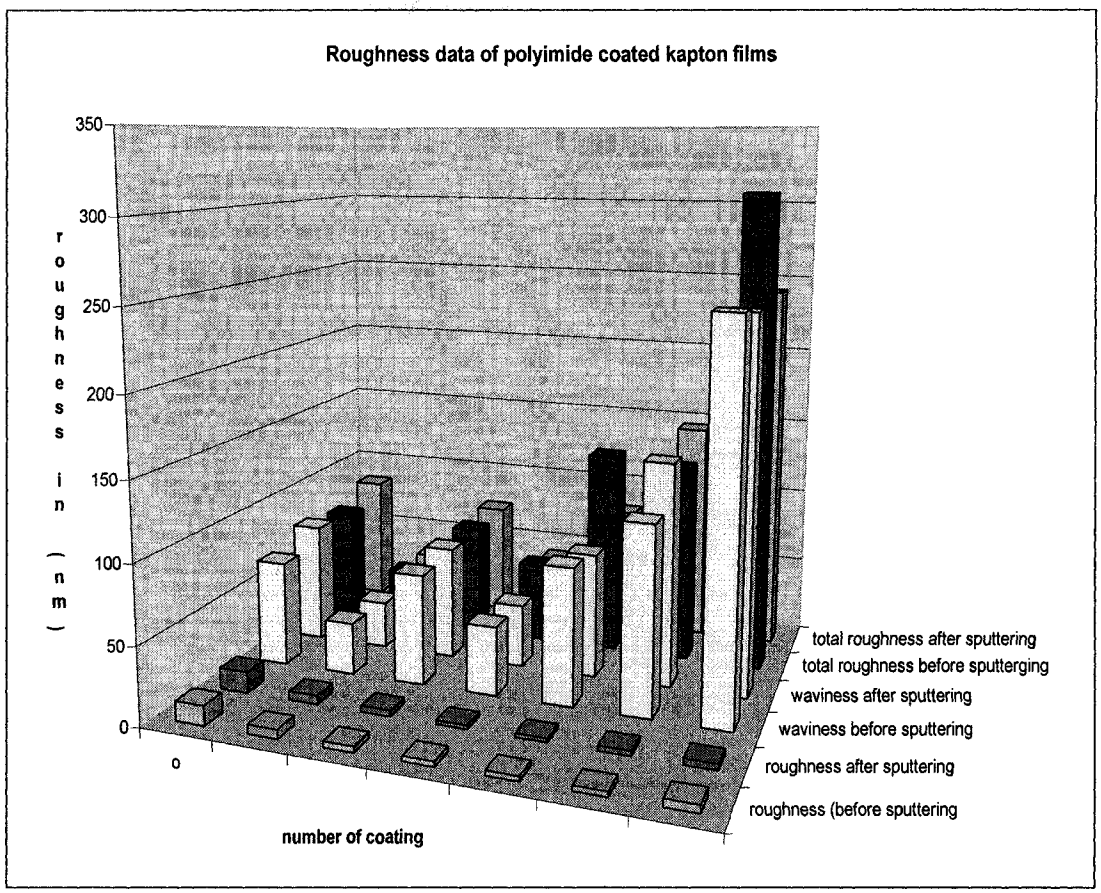


Figure 3.4 Roughness parameters of polyimide coated Kapton 500VN films.

3.3.2 Xerographic Processes

A black and white printout from a laser-jet printer or a copier on a transparency shows patterns or letters printed with toner material. Toner in a laser Jet printer is an electrically charged powder material made of pigment and plastic. The pigment is for the color as for example, black in a black and white laser printer. Plastic beads hold this pigment and melt when passed through heat. Once printed, the toner will not have any static electricity and acts as an insulator. Therefore, if a laser printer is used to pattern a transparency, then the toner material acts like an insulating shadow mask on the transparency. Metal or conducting polymer can be deposited on the patterned transparencies using different deposition techniques and the toner can be removed later

using sonication in acetone or toluene similar to a lift-off method [53]. We have chosen Kapton 500VN film as our substrate which has a thickness of 5mil, which is comparable to the thickness of a typical transparency, in order to avoid problems while loading the substrate into the printer. Kapton VN films of other thicknesses can also be used depending on the design requirements of the circuit and the printer capabilities. Figure 3.5 shows the IV characteristics of toner and electroless-deposited copper trace patterned using a laser printer. Electroless deposition of copper requires pre-conditioning of the substrate as well as other precautions which are explained later in this chapter.

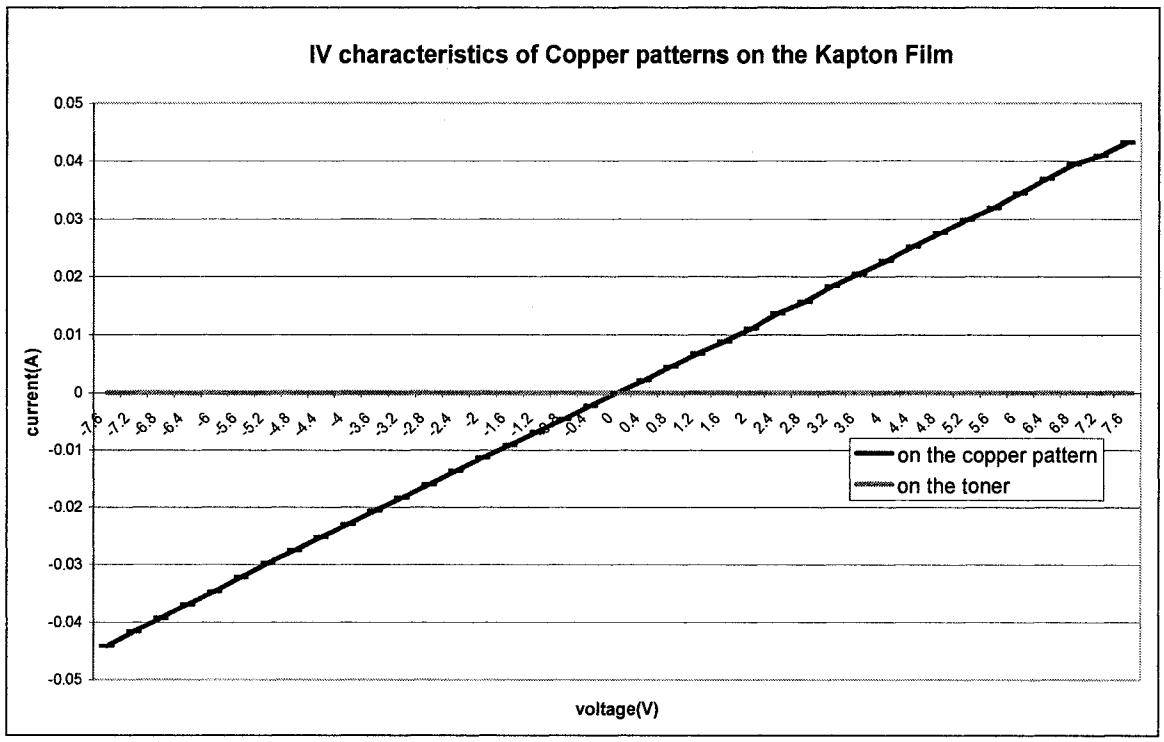


Figure 3.5 I-V characteristic curves of copper pattern and toner.

Figure 3.6 shows device patterns such as, Meander and Hilbert antennas, and other components printed on a polyimide substrate using a laser jet printer. Resolution of the printer is very important in determining the design approach for circuit patterning using

xerographic methods. A laser printer's resolution is given in dots per inch (dpi). A high end printer can have a resolution of 2400 X 2400 dpi or more which means each dot is a minimum size of 10.58 μm. Therefore, many of the circuits and elements, like inductors and interconnects, can be designed with high resolution laser jet printers. We have used 300 X 300 dpi resolution using an HP laser Jet 1200 series printer, which corresponds to a minimum patternable size of 84.6 μm.

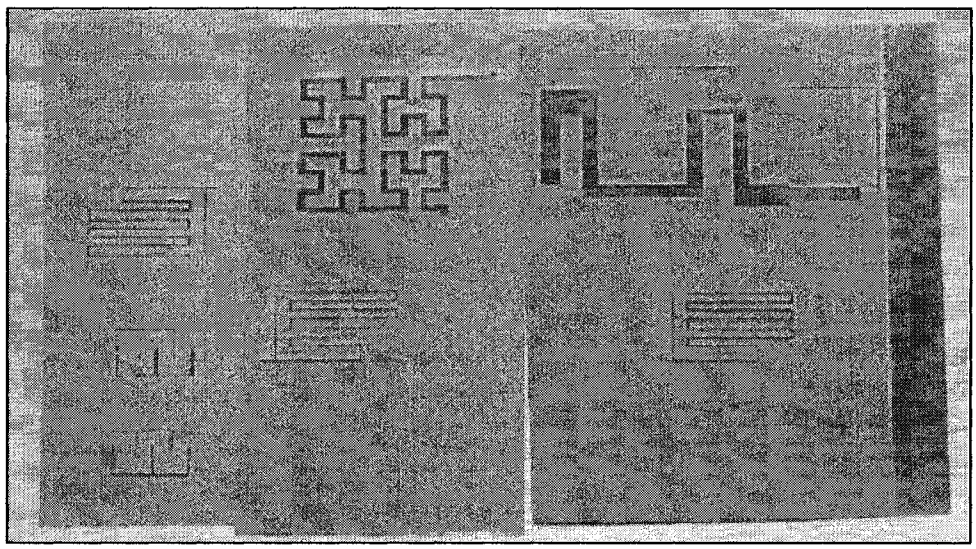


Figure 3.6 Different device patterns printed on a Kapton 500VN substrate using laser-jet printer.

Low end commercial printers might have higher tolerance to the width of the substrate that is fed and therefore result in alignment problems of the printed patterns. Careful adjustments must be made in the softcopies for the case of circuit patterns that need patterning of the substrate on both sides. Any drawing software based on AutoCAD can be used for making a soft copy of the design for the printer. Ansoft and Coventor and other similar CAD software packages have the capability to generate softcopy of micron sizes and below [40,41]. Figure 3.7 shows pictures of copper lines patterned by

the xerographic method as taken by using the Optimus measuring system. Under a high resolution microscope, one can see that the edges of the patterns are not straight and there are many unwanted toner particles on and around the copper patterns. This dust is removed after sonication and cleaning of the patterns but the edges remain non-uniform. This factor needs to be taken into account while designing components and circuits at high and ultra high frequencies because of the loss of signal at uneven edges. Pits on the copper patterns become negligible once sufficient deposition thickness is achieved and a minimum thickness is required because of skin depth requirements at the frequency of operation. Line patterning technique can be used to avoid some of these problems [54]. A copier can be used but this would add one more step to the patterning process and add alignment errors as the mask needs to be aligned accurately with the loaded transparency.

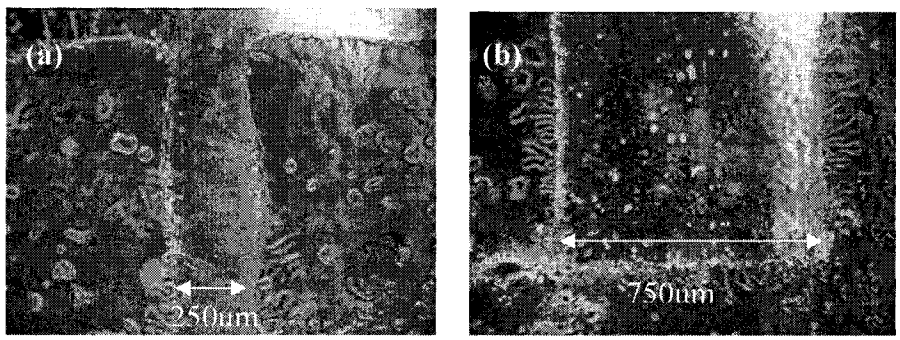


Figure 3.7 Deposited copper patterns with line-width of approximately (a) 250 µm (b) 750 µm printed using laser jet printer (pictures taken using Optimus measurement system).

3.3.3 Polymer Inkjet Printing

Some water-based conducting polymer solutions or solutions that are relatively neutral with pH around 7 can be printed directly on to the transparencies by using desk-jet printers. These polymers can be loaded into a cleaned cartridge instead of printer ink

using a syringe or a refillable kit. Many procedures are available online about cleaning and refilling of inks [55]. Strong acidic or basic solutions tend to etch away the cartridge walls and the nozzle and, therefore, are not adaptable to desk-jet printing. The size of the particles in the solutions also plays a significant role in the printability of the material as large size particles might block the nozzle. Unfortunately, many polymers will not produce a good continuous pattern unless they are printed one on the other several times thus requiring good alignment capabilities of the printer (Figure 3.8 (a)). Moreover, the printed patterns are rough and non-uniform at the edges (Figure 3.8 (b) and (c)). Thermal treatment is used to achieve good topography and morphology of the printed pattern. Viscosity is another factor to consider in determining whether a polymer is printable with a desk-jet printer or not. Polymers such as, PEDOT/PSS and polypyrrole are made highly aqueous in order to get a uniform continuous printable pattern on the transparencies. Some substrates such as, inkjet transparencies contain a special powder coated on the surface to give good adhesion to the printed aqueous ink. Patterns printed on Kapton 500VN have sufficient adhesion as the surface is rough and absorbs moisture up to 1% in humid conditions as compared to other types of polyimide substrates available in the market.

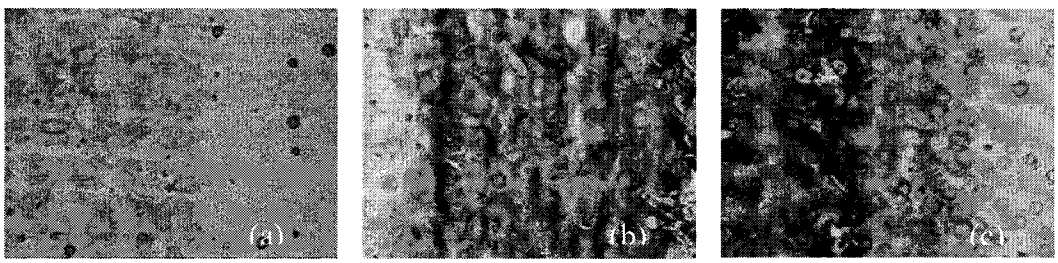


Figure 3.8 Inkjet printed polypyrrole patterns (a) two coats on the substrate (b) densely packed polymer structures of a pattern with 15 coats (c) non uniform edge of a pattern with 15 coats.

The minimum printable size is dependent on the resolution of the printer as discussed earlier. We have used a HP desk-jet 600 series printer that has a resolution of 600 dpi with a corresponding dot size of 42.3 micron. The printer resolution is one of the concerns while designing the devices. Devices of larger tolerance values can be made using this technique but might not be of much use for radio frequency device fabrication where the dimensions of the patterns become more critical at higher frequencies.

The IV characteristics of patterns of different dimensions measured using the 2-probe method of the Keithley electrical characterization system show that the resistance of the pattern is directly proportional to length and inversely proportional to width and thickness, thus confirming the ohmic nature of the patterns. Figure 3.9 shows the effect of thickness on the resistance of the PEDOT/PSS patterns. PEDOT/PSS is printed on a Kapton substrate, and the thickness is varied for the successive patterns by changing the number of coatings. The patterns have the same dimensions and have coatings from 11 to 28 layers. A clear trend line could be seen that shows a decrease in the resistance with an increase in the number of layers. A minimum of 10 layers are printed to ensure the continuity and uniformity of the structures.

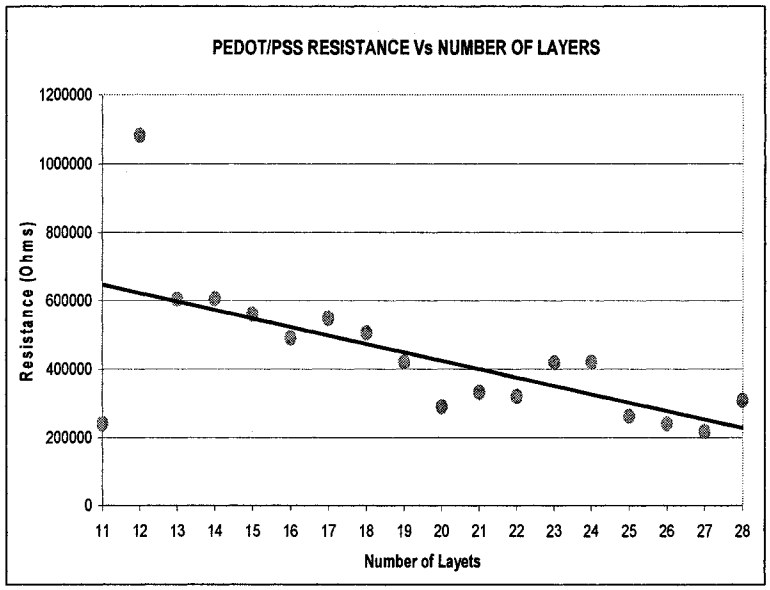


Figure 3.9 Resistance changes of PEDOT/PSS patterns with the number of printed layers.

The resistance of patterns with similar dimensions varied from each other suggesting discrepancies in the printer performance. Printers with better resolution and capabilities are available for a moderate price. Demand-on-drop printers can also be used to print liquids of varying viscosities, with more control of the dimensions and uniformity. Droplets of 30 μm diameter or less are possible but cost tens of thousands of dollars and are low in throughput.

3.3.4 Electroless Deposition

Copper is being considered as one of the best among the metals for interconnects and as a circuit material. Electroless copper deposition offers a low-cost option to sputtering and physical vapor deposition (PVD). Usually, electroless copper is used as a seed layer followed by electrolytic deposition of copper, but significant improvements have caused electroless copper to be used directly as the interconnecting metal in the

flexible electronics industry and other industries. Some companies offer ready-to-use solutions that can give up to 2.2 μm thickness depending on the substrate [56].

3.3.4.1 Preconditioning

Even though copper of sufficient thicknesses is obtainable from the electroless deposition method, the ambient conditions during the deposition need special consideration. Commercial copper baths that promise a deposition of 2.2 μm thickness specify bath conditions such as, continuous N_2 bubbling, mechanical agitation and type of substrate. The process should be continuous and requires frequent calibration and constant addition of required constituents to the bath to avoid a Cannezaro reaction that depletes the plating capability of the bath. Filtering should be done frequently to remove waste material that might favor deposition to also occur on these contaminants.

Besides the above mentioned requirements, surface treatment is necessary for many commercially available substrates such as, PETs and polyimides. This includes activation and acceleration. Palladium acts as a good catalyst for many polymeric substrates but Kapton polyimide substrates are relatively smooth and, therefore, do not react with chemicals used for activation. Thus, surface preconditioning is necessary for proper activation of the substrate.

Different methods were tried to modify the substrate roughness of the Kapton polyimide films. Literature suggests different strategies to alter the polyimide surface for proper copper deposition. Mechanical roughening initially helps to increase the surface roughness and therefore, increases the activation sites to enhance the deposition. This is followed by sonication in isopropyl alcohol and KOH etching of the polyimide substrate [57]. The steps mentioned above actually resulted in the reduction of the substrate's

roughness for the Kapton 500VN films rather than an increase as suggested by the literature (Figure 3.10). The difference in the subtypes of the polyimide substrates used and those suggested in the literature might be the reason for obtaining a completely different set of results.

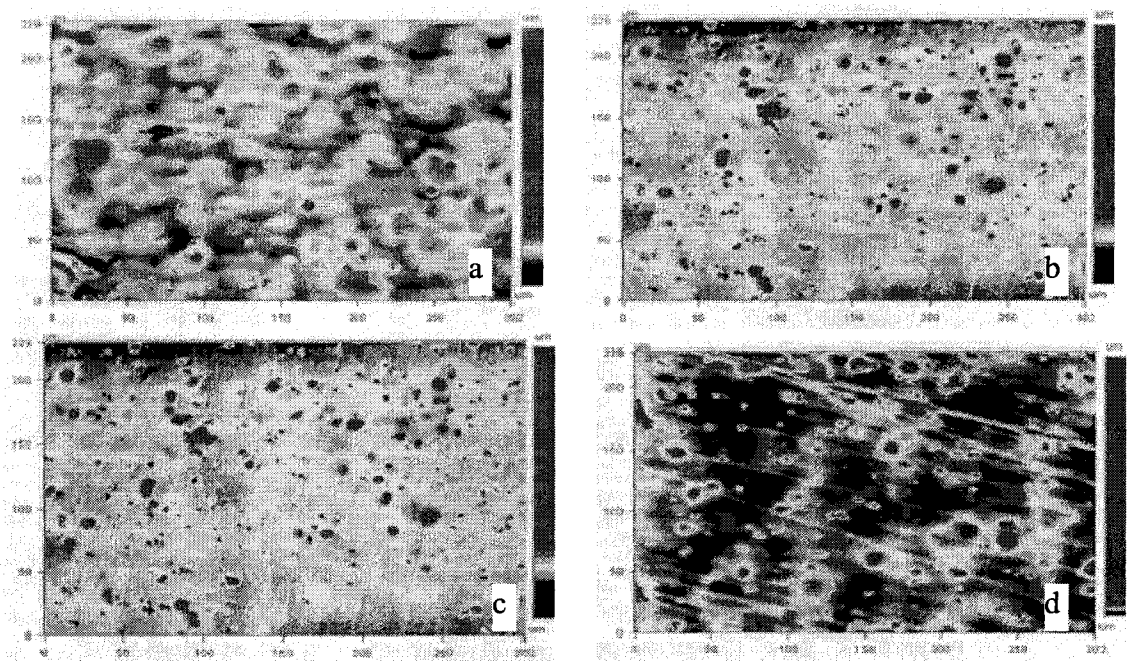


Figure 3.10 (a) Untreated Kapton VN500 (65 µm) (b) mechanically roughened (37 µm) (c) Sensitized with Isopropyl alcohol under sonication (37 µm) (d) KOH etching for 1 min (15 µm).

KOH etch time has been increased to see its effect on the substrate. It is observed that increasing the etching time resulted in an increase in the substrate's roughness but considerably less as compared to the original roughness of the substrate (Figure 3.11). A further increase in the etch time resulted in complete deformation of the polyimide into soften form. The smoothing effect of the substrates was further confirmed by poor adhesion of copper and toner material to the substrate.

Adhesion of copper to the polyimide substrate can also be increased by electroless deposition of a seed layer of copper on the polyimide substrate, heating at 400^0C for 30 seconds, etching the copper away using HNO_3 and using the substrate for final deposition of copper. Applying the same set of processes on Kapton 500VN did show significant improvement in the quality of the deposited copper patterns.

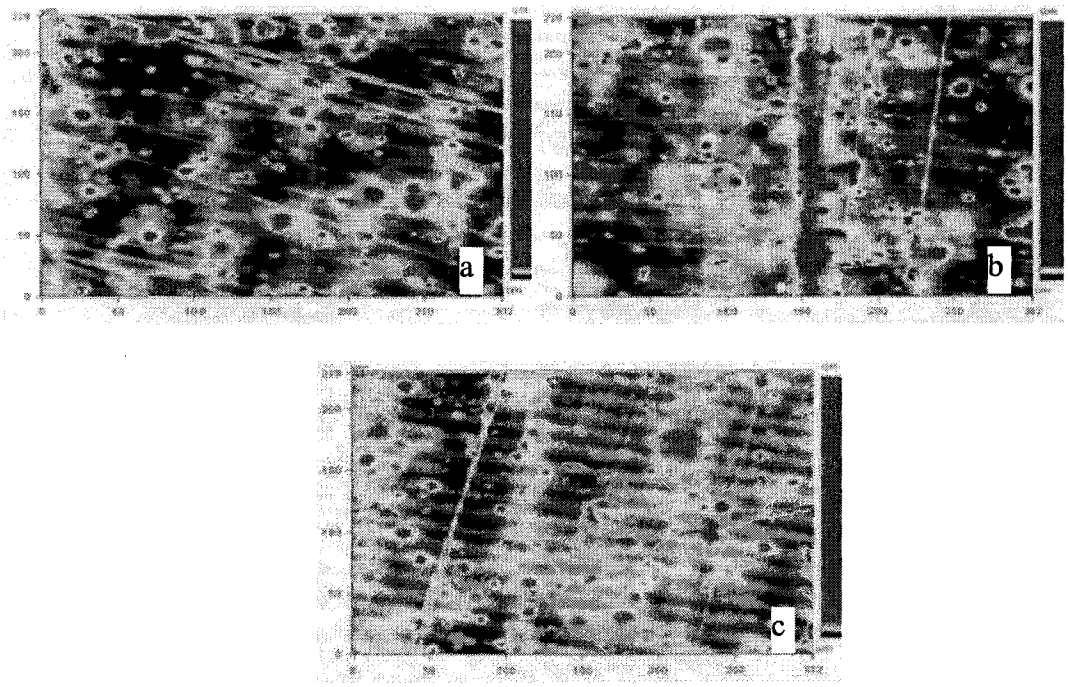


Figure 3.11 R.S.T measurements of KOH etched substrates. Etching is done for (a) 1 min (15 μm) (b) 2 min (19 μm) (c) 3 min (22 μm).

It was decided that based on the results obtained from the above experiments, that mechanical roughening of Kapton 500VN substrates followed by sonication in isopropyl alcohol are the processes of choice for good copper deposition. The roughening was achieved by manually rubbing the substrates with a smooth cloth. Even though there is a decrease in the surface roughness, these processes enhance the availability of molecules

to bond with molecules of catalyst and activation solution which further results in the good adhesion of copper molecules and a uniform coating.

3.3.4.2 Activation and acceleration

Table 3.5 describes the two methods used for activation and acceleration of the substrates for further deposition of copper. The activation step involves the coating of the non-catalytic surface with catalytic colloidal particles. Activation could be performed either in two steps or in one step [58].

Table 3.5 Types of preconditioning methods used in the experiments.

Preconditioning Method-1	Preconditioning Method-2
Step 1: Activate the substrate using the following solution for 2 to 4 minutes Preparation: 30ml water +2.5 g Tin Chloride (0.2 g instantly and 2.3 g after 24 hrs) + 0.05 g Pd chloride + 15 ml HCl.	Step 1: Activate the substrate using the following solution for 2 to 4 minutes Preparation: 30ml water +2.5 g Tin Chloride (0.2 g instantly and 2.3 g after 24 hrs) + 0.05 g Pd chloride + 15 ml HCl.
Step 2: Keep the substrate in the following acceleration solution for 2 to 4 minutes Preparation: 50ml of HCl (37%) + 50 ml Water	Step 2: Keep the substrate in the following acceleration solution for 2 to 4 minutes Preparation: 50mg of $PdCl_2$+ 200ml of water + 0.25ml of HCl
Remarks This procedure yielded moderate copper deposition with non-uniform coating over an area	Remarks This procedure yielded very good copper deposition along with uniform coating over an area

The metallic palladium on the surface after the activation step is surrounded by hydrolyzed stannous hydroxide. The excess of stannous hydroxide should be removed

before the palladium can act as a catalyst. The accelerator solution consists of an organic or mineral acid which removes the excess tin from the part while leaving the palladium sites intact for the deposition of the electroless copper. Immersion of the substrate in the accelerator solution for too short a time, or too long can result in skip-plating.

Figure 3.12 shows the top and bottom sides of the substrates patterned for high frequency and ultra high frequency tag layouts using the above mentioned preconditioning methods 1 and 2, respectively. Even though there is a thick deposition of copper on the 13.56 MHz tag layout (Figure 3.12 (a)) the inductor patterns in between the square capacitor plates did not get coated with copper because of the non uniformity of the applied catalyst and acceleration components on the surface. Adhesion of copper to the substrate is also very poor (Figure 3.12 (b)). On the other hand, the layout for 915 MHz tag was preconditioned using method 2 was coated uniformly with proper adhesion (Figure 3.12 (c) and (d)).

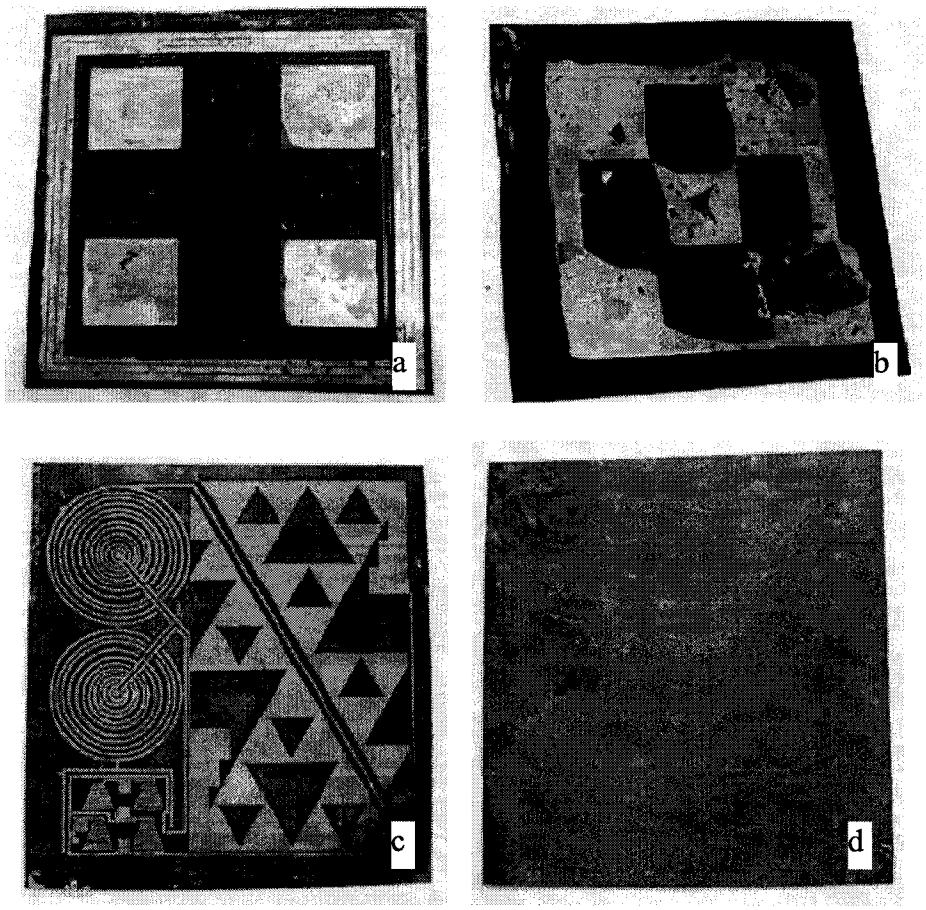


Figure 3.12 Effect of activation and acceleration preconditioning method-1 on copper deposition of 13.56MHz layout (a) front side (b) bottom side. Preconditioning method-2 on 915 MHz layout (c) front side (d) bottom side (note: dimensions are not to the scale).

3.3.4.3 Electroless copper solutions

An electroless bath has been successfully developed in our lab at IfM for the deposition of copper on a silicon substrate and is further optimized for copper deposition on flexible substrates [59, 60]. The bath solution did not yield thicknesses greater than a 100 to 150 nm. Therefore, Cuprothick 84 ready to use copper bath solution is used for our experiments which promises a 2.2 μm thickness under ideal conditions. This bath is well known and is promoted as one of the best for the plate-through-hole process. Table 3.6 describes the recipes for both of the solutions

Table 3.6 Recipes of electroless copper baths used in the experiments.

Copper Bath Optimized at IfM	Readymade Copper Bath –Cuprothick
Moderate Build solution for copper Operating Temperature = 50^0C to 55^0C Bath = 1000 ml of water + 3 g of $CuSO_4$ + 8 g of EDTA + 2 to 3 ml of HCHO + NaOH (till the pH becomes 12.5 to 12.6) + 100 mg of 2,2' pyridyl + 0.05 ml of Triton	High build solution for thick copper Operating Temperature = 36 to 38^0C Bath = 800 ml water + 100 ml of Cuprothick84 F + 40 ml of Cuprothick 84A + 30 ml of Cuprothick 84B + 30 ml of Cuprothick Alkaline additive
	low build solution for thick copper Operating Temperature = 25 to 30^0C Bath = 800 ml water + 100 ml of Cuprothick84 F + 40 ml of Cuprothick 84A + 20 ml of Cuprothick 84B + 40 ml of Cuprothick Alkaline additive

During electroless copper deposition, dissolved toner particles may cause pH changes and affect the physical properties of the deposition. Timely filtering of the bath solution and adjustment of the pH are necessary to avoid such problems. The operating temperature should be accurately maintained. Uniform nitrogen bubbling is necessary in order to avoid blistering. If the solution is not agitated a continuous reaction known as Cannezaro reaction takes place inside the bath depleting the copper deposition capability of the bath. Copper gets deposited on the bottom of the bath container because of this reaction. A properly plated copper pattern remains relatively inert for several days showing no signs of oxidation. Figure 3.13 shows a 915 MHz tag layout plated up using the Cuprothick 84 ready to use copper bath and precondition method-2 as explained earlier.

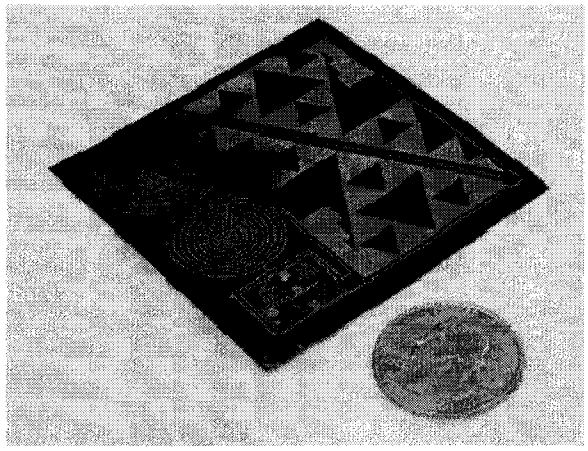


Figure 3.13 Cuprothick 84 deposited layout for 915 MHz tag using preconditioning method-2.

3.3.4.4 Characterization

A maximum of 0.3 μm to 0.4 μm thick copper is achieved using the preconditioning and deposition methods explained earlier. The specified thickness of 2.2 μm could not be achieved due to non-ideal bath conditions such as, non-uniform bubbling of N_2, absence of mechanical agitation and usage of a polyimide substrate rather than a typical printed circuit board (PCB) for which such high thickness is possible. The adhesion to the substrate is found to be good for the mechanically roughened pre-treated substrate followed by sonication in isopropyl alcohol. The roughness of the copper is found to be of the order of tens of nanometers (Figure 3.14). Toner particles and other dust particles shown in the RST plot demonstrate the need for proper cleaning of the substrate before and after the deposition of copper.

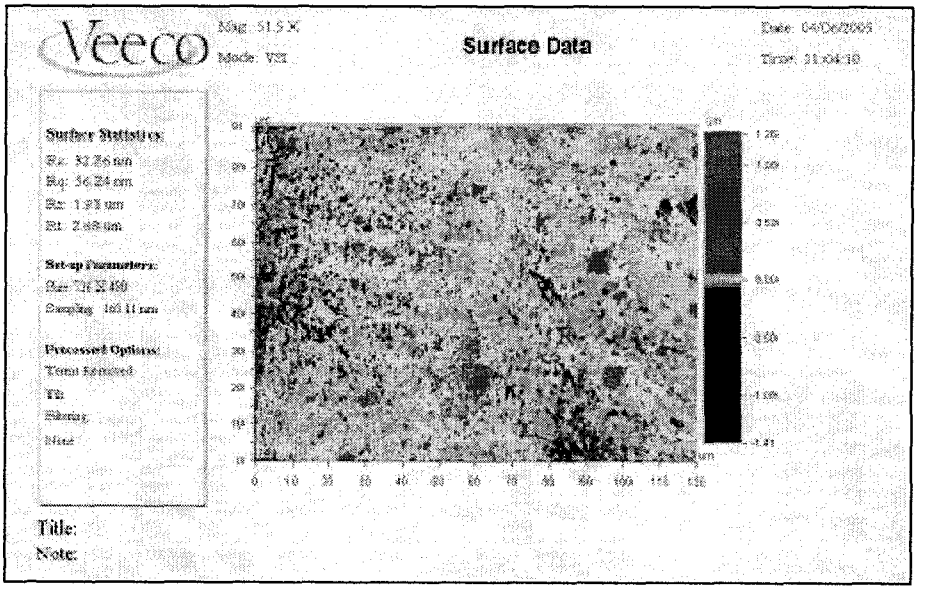


Figure 3.14 R.S.T diagram showing roughness of the electroless deposited copper.

3.3.5 Spray Coating

The Eclipse BCS bottom feed airbrush with 0.5mm needle and nozzle combination is used for manual spray coating liquid polyimide on to substrates. Figure 3.15 (a) shows the experimental set up and Figure 3.15 (b) shows the major parts of the air brush. The quality of the coated layer can be controlled by varying the viscosity of the polyimide by adding NMP and by controlling the nozzle size and the angle of the spray.

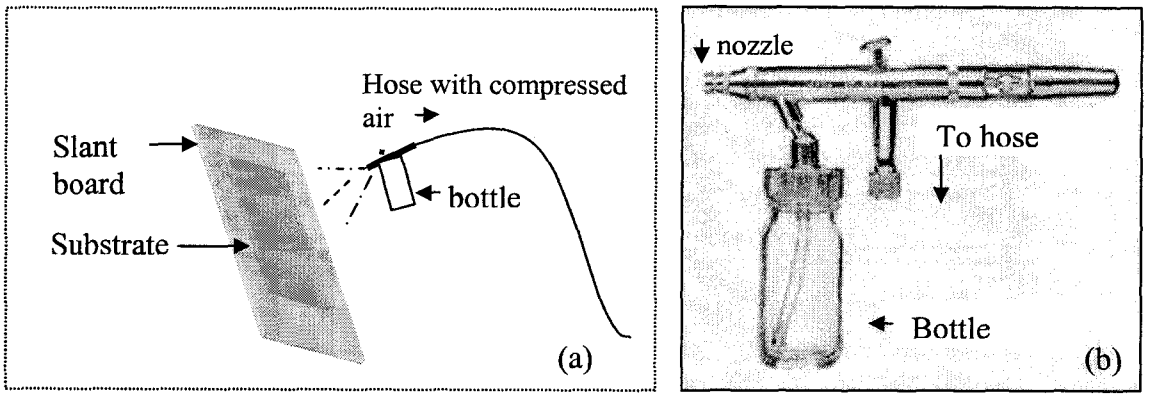


Figure 3.15 (a) Spray coating experimental set up (b) air brush used for spray coating technique.

A minimum of five coats is required to cover the whole surface of the substrate with out leaving any gaps. A typical coat of polyimide by air brush produces small liquid particles that merge with adjacent available droplets in successive coatings. This might cause liquid islands rather than a uniform coating. Therefore, a hot air dryer (VS Sassoon professional turbo dryer) is used in between two consecutive coats to partially evaporate the solvent. This would eliminate the merging together of adjacent droplets because each layer of droplets are evaporated by the dryer, which produces a temperature up to 80^0C, leaving semi solid polyimide particles behind. A final thermal treatment of the spray coated substrates in a vacuum thermal oven (Vacutherm, HERAEUS Instruments) will evaporate NMP a and polyimide layer of sufficient thickness is obtained. Figure 3.16 shows the effect of the polyimide protective coating on PANI resistor patterns and Figure 3.17 shows that for PEDOT/PSS patterns.

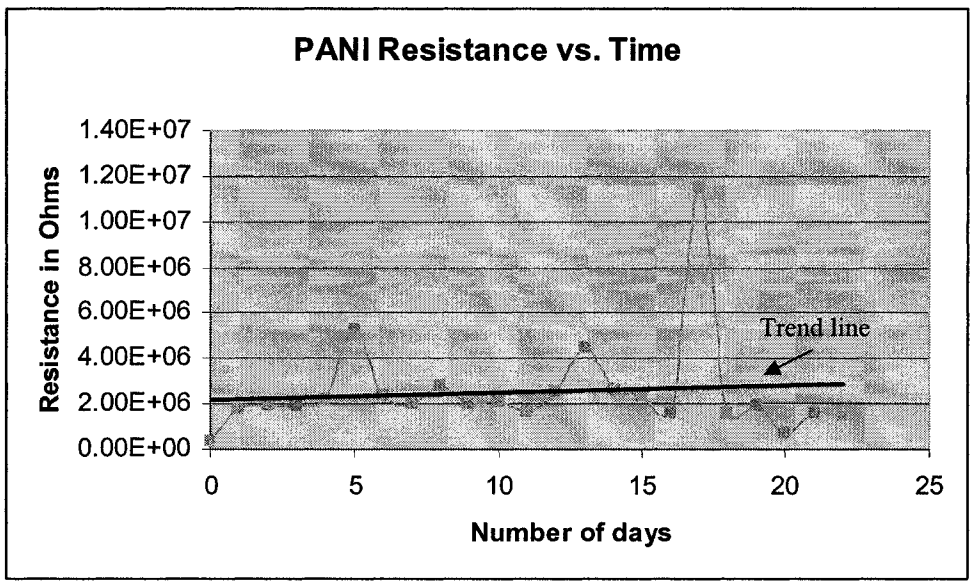


Figure 3.16 Resistance vs time graph of polyimide coated PANI resistor patterns.

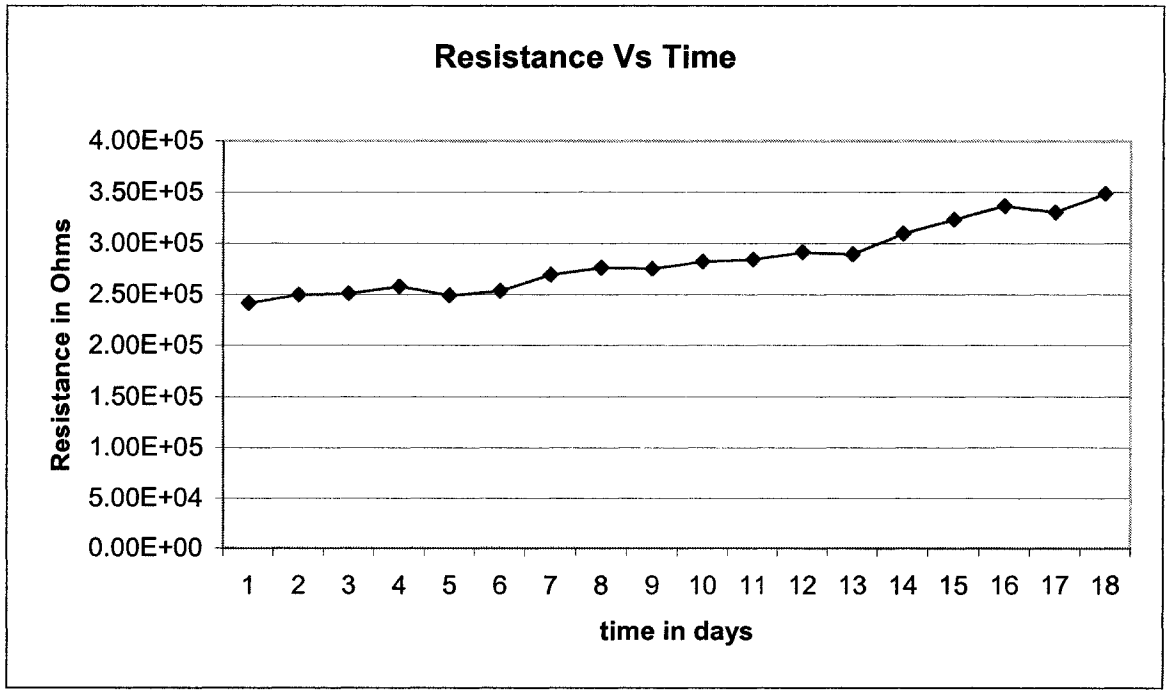


Figure 3.17 Resistance vs time graph of PEDOT/PSS resistor patterns protected by polyimide.

3.3.6 Plate-through-hole Process

Grounding might be required for some of the components of the tag. The wireless tag circuit needs to be grounded to the bottom metallic layer through a conducting via. The Cuprothick 84 process is good for the Plate-Through-Hole Process as mentioned earlier. A needle is used to manually drill a hole approximately 400 μm in diameter and is electroless copper plated for one minute. The quality of the deposition was observed under the scanning electron microscope. Figure 3.18 below depicts one of the plated vias at different magnifications. Manual drilling resulted in elevated edges near edge of the hole (Figure 3.18 (c)). The plated vias have been tested for their electrical continuity between top and bottom layers. An average resistance of 10 Ω was observed between the layers that are connected through the via including the contact resistances of the probes. The thickness of the plated copper can be increased by increasing the time of deposition.

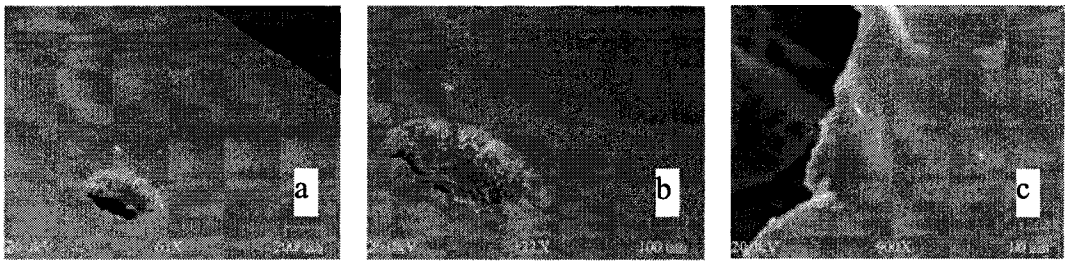


Figure 3.18 Via plated using Electroless Plate-Through-Hole process (a) at 61 x magnification (b) at 122 x magnification (c) edge of the Via at 900 x magnification.

3.3.7 Drop Casting

A simple syringe was used to drop cast PEDOT/PSS solution on the copper electrodes for making the resistors. Such processes are unreliable for fabricating resistors requiring precise values. However, the LC-delay-line-based tag requires a 10 MΩ resistor. Resistors ranging from a fraction of 1 MΩ to 10 MΩ have been fabricating using the drop casting method. Characterization of resistors made using drop-casting method is discussed in the next chapter.

3.4 Proposed Low-cost Fabrication Process Flow

Researchers are keen to develop methods and techniques to fabricate devices and circuits on flexible substrates with low-cost processes [61, 62]. As explained earlier, Kapton VN 500 polyimide substrates were chosen from all the flexible substrates under consideration (Section 3.3). Polyimide films are expensive but are thermally stable (up to 400^0C) as compared to Polyesters and have high mechanical stability, a less than 1% moisture absorption, and a compatible thermal expansion coefficient with respect to copper [63]. Copper has been used as the conductor material for interconnects, capacitors, inductors, antennas and the sensor switch layout. The electroless copper

deposition technique developed at IfM has repeatability, reliability and yields depositions of sufficient thickness and uniformity to fabricate the designed components and the tag layout. The combination of copper and polyimide for flexible electronic circuits has proven successful in the electronic industry. Copper can be deposited to form planar inductors, capacitors, antennas and interconnects. PEDOT/PSS, which is known for its stability, can be used to make resistors of the required values. Figure 3.19 shows set of materials chosen for the fabrication of the proposed passive RFIDs and RFID-based sensors based on delay-line concept.

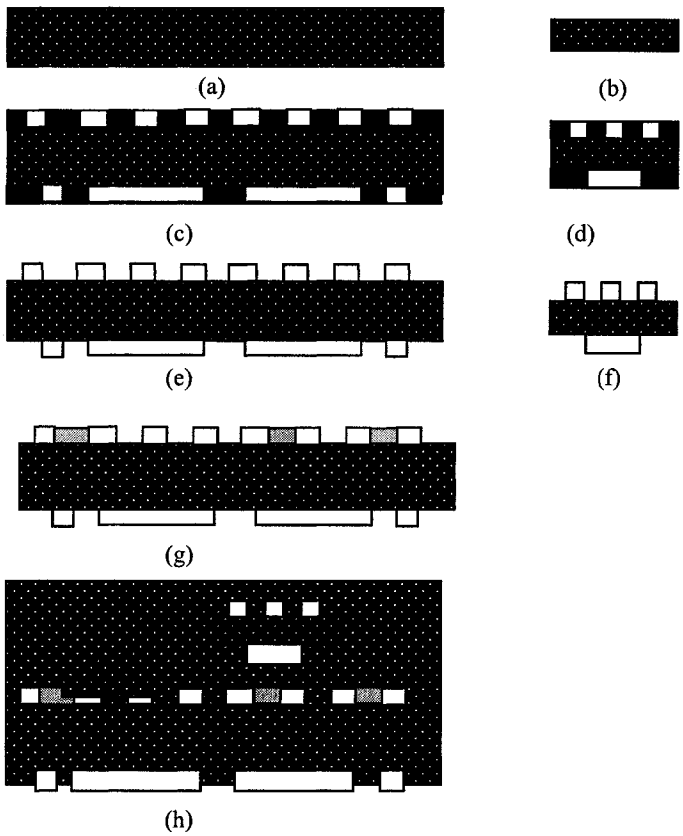


Figure 3.19 Schematic diagram depicting the proposed set of processing steps used in the fabrication of tag.

Epoxy has been established as a good encapsulant and protecting layer in the industry. It is compatible with the flexible circuits offering mechanical flexibility and

good adhesion properties with metal and polyimide [64]. Moreover, U.V curing is sufficient for the epoxy thus avoiding any heating during the packaging of the tag that might cause thermal damage to other components and layers.

The materials chosen for the fabrication does not imply that these are the optimum choice for the fabrication of our tag. Devices for low end applications such as, our tag, can be made rugged and reliable within the limits of their applications. As explained in the earlier chapter, researchers are searching for low-cost alternatives for conventional silicon-based technologies. Therefore, any of the other low-cost techniques such as, printing techniques, soft-lithography and line patterning, can be used for the fabrication of the tag depending on the requirements of the application and capability for mass-production [63-69].

A Kapton VN500 film is taken as the flexible substrate (step (a) in Figure 3.19) and is loaded into a laser printer. The layout of the tag is designed in simulation programs such as Coventor or Ansoft, and then converted into a soft copy. Depending on the design, the layout is printed on one or both the sides of the substrate using a desk top laser-jet printer. The substrate, with the toner acting as shadow mask, is then dipped in activation and acceleration solutions for three minutes (preconditioning method-2) each and then copper can be deposited using a ready to use electroless bath. Step (c) in Figure 3.19 shows the copper patterns on the toner covered substrate. The toner material can be removed using ultrasonic vibrations in acetone or toluene [54]. The substrate containing the copper patterns (step (e) of Figure 3.19) can now be loaded into an inkjet printer to deposit a PEDOT/PSS layer for the channel material of the switch (step (g) of Figure 3.19). With some modifications, diodes can be printed on the layout in a similar way. The

process steps depicted above are used to metalize and pattern the piezoelectric polymer sensor material for integration with the organic switch of the wireless tag (steps (b), (d), and (f) of Figure 3.19). The sensor element is now attached to the channel region of the switch by using an adhesive that acts as the gate insulation material (step (h) of Figure 3.19). Since the sensor material and the adhesive are transparent, the gate can be visually aligned with the channel with considerable accuracy. Processing temperatures have been taken into consideration in designing the fabrication process hierarchy. The materials are chosen such that there is no significant mismatch in the thermal expansion coefficients which, if large, results in poor device reliability. A polyimide spray coating can be administered for protection and packaging. U.V. cured epoxy encapsulant is also a reliable alternative for protection and packaging of the tag.

3.5 Silicon-based Fabrication Processes

One of the main objectives of this work is to fabricate RFIDs and RFID-based sensors at low-cost. However, non-silicon-based processing techniques explained earlier may not be immediately adopted by the mature silicon-based industry. Moreover, it is learned from the experiments that the vendor specified thickness of 2.2 μm for electroless copper could not be achieved at our lab for the reasons mentioned earlier. A lesser thickness means more surface losses because of the minimum skin depth requirements. In case of partial or complete failure of the proposed set of processes in the fabrication of devices, components, and integrated layout of the tags, an optional set of processes are employed to realize them. These are conventional silicon-based processes established in the chip-based industry and are more robust but expensive. The devices or components made using these optional silicon-based conventional processes will be used to compare

with those fabricated with the low-cost processes proposed in Section 3.4 and demonstrate the inter-compatibility of the proposed RFID design with silicon-based processing technology.

Figure 3.20 shows a schematic diagram of the proposed processes and the hierarchy for making RFIDs and RFID-based sensors. The substrate chosen is a double sided copper clad polyimide substrate (FR9151, Dupont Pyralux) (Figure 3.20) which is thermally stable up to 300^0C and has high dimensional stability and good peel strength [70].

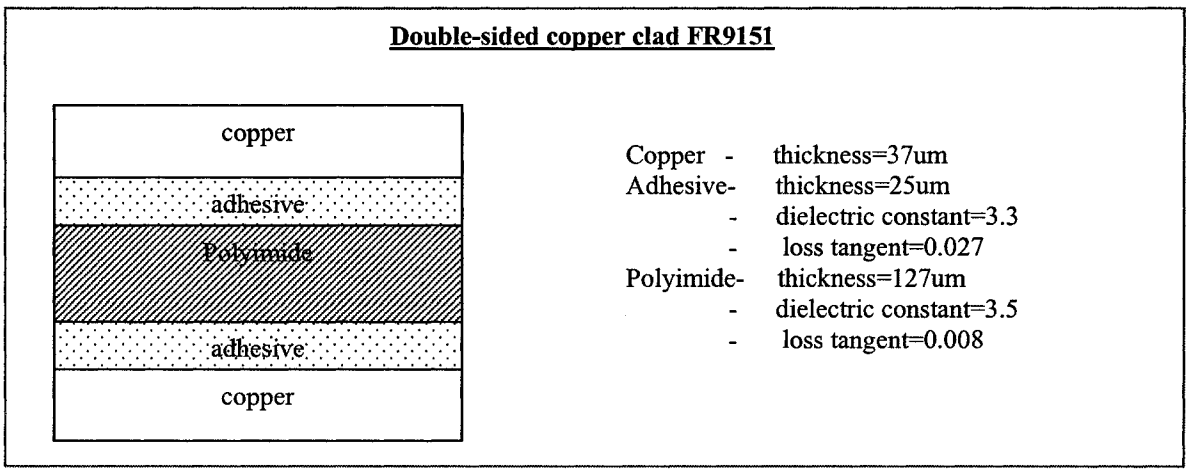


Figure 3.20 Substrate stack up of FR9151 for simulations.

The tag's layout has been designed using Ansoft Designer simulation software and soft copies of the masks have been printed either by using facilities at Louisiana Tech University (Linotronics 330 with 4000 dpi resolution) or at the University of Illinois with 5080 dpi resolution. Using the masks the substrate is patterned by a photolithography process that includes spin coating PR1813 photoresist (Shipley), U.V curing, and Ferric Chloride (MG Chemicals) etching for 20 minutes. Depending on the design layout, either

both sides or one side is patterned. Components such as, resistors, diodes and FETs are attached using conductive silver epoxy (Chemtronics Inc) or by soldering, which ever is suitable. In the case of the RFID-based sensors, the sensor material is placed on the sensor layout using insulating glue. U.V curable epoxy is used as the encapsulant and prevents oxidation of the copper. UV curing eliminates heating during the packaging of the tag that could cause thermal damage to other components and layers. Wherever necessary, grounding of the components is achieved by manually drilling a hole and filling it with conductive epoxy to make connection to the bottom ground plane layer. These steps are illustrated in Figure 3.21 and each step is explained in detail below.

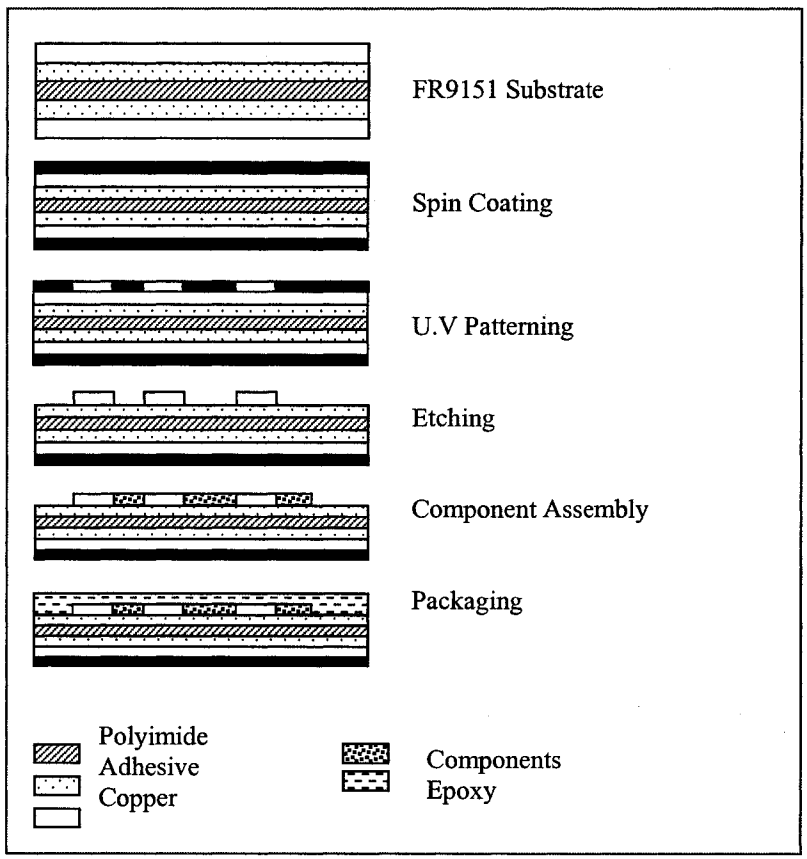


Figure 3.21 Schematic diagram showing the process steps used in the fabrication of piezoelectric RFID tag.

3.5.1 Substrate Cleaning

Double sided copper clad polyimide substrate (FR9151) is cut into square pieces to fit the tag layout. These pieces are cleaned with acetone and isopropyl alcohol to remove any organic or other dust particles on the surface. After drying in air, the pieces are kept at 100^0C for 2 minutes.

3.5.2 Photolithography

After thorough cleaning, each square piece was mounted on to a spinner using a piece of double sided tape for adhesion to the spin head and coated with positive photoresist (PR1813, Shipley) to cover the entire surface. A recipe with an initial speed of 200rpm for the first 30 seconds and 2000rpm for 2 minutes is programmed into the spinner (P 6204 A, Spin Coating systems). The photoresist coated piece is removed from the spinner and kept on a hot plate at 100^0C for 1 minute for pre-baking. After prebake, each piece is spin coated with PR1813 on the other side and kept on a hotplate at 100^0C for another one minute cycle. Then, each prebaked piece is placed in a U.V exposure chamber along with the contact mask having the tag layout on it for 30 seconds. The exposed patterns on the pieces are developed using photoresist developer (MF319, Shipley) for 2 minutes and post-baked on a hot plate at 100^0C for 5 minutes.

3.5.3 Etching

The copper etching solution (Ferric Chloride, MG Chemicals) is placed in a tray and the pieces on which photolithographic pattern has been completed are kept in the solution for 20 minutes with constant agitation. Once the patterns are realized, the samples are rinsed with DI water and dried thoroughly with N_2.

3.5.4 Component Assembly

Off the shelf components are used where possible for realizing the RFID concept and the tag. At radio frequencies, lumped resistors, capacitors or inductors behave differently due to undesirable resistances, capacitances, and inductances that are in addition to their true values. Surface mounted devices (SMDs) are used instead of lead components because the lengths of all component leads have losses due to lead inductance. A component's effective frequency increases with a decrease in its size. The smaller the package, the lower will be the harmful reactances and series or parallel resonances. Thus surface mount Schottky diodes such as, those requiring bias (MA4e1338A-114T, Macom.com) and zero bias diodes (HSMS 2850, Agilent) and resistors are used for the ID circuit of the tag. These components are attached to the copper lines either by using silver epoxy (Figure 3.22) or soldering. This figure also shows silver epoxy filled holes of 0.4mm diameter that are drilled manually using a syringe needle to connect the necessary devices to the ground plane.

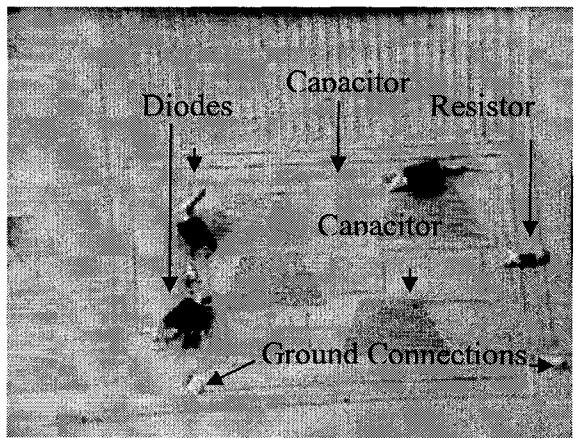


Figure 3.22 Layout showing ID circuit with silver epoxy assembled diodes and resistors.

CHAPTER 4

DEVICES AND COMPONENTS OF THE TAG

4.1 Overview

The two different delay-based RFID systems that consist of RFIDs and RFID-based sensors are described in Chapter 2 and different fabrication techniques through which these tags can be realized are discussed in Chapter 3. This chapter describes individual devices and components, their design, fabrication and characterization. Modeling and simulation of some of the devices and components such as, planar inductors, capacitors, and antennas required for the RFID tag were modeled independently by different members of our research group and were presented in Section 1.6. This chapter describes the modeling and simulation of the components of the LC-delay-line-based RFID/RFID based sensor such as, interconnects, resistors and diodes, and simulation/modification of the previously modeled components such as, inductors, capacitors, and antennas with respect to the low cost processes that constitute the proposed fabrication process flow (Section 3.5). Isolators and circulators are described later which are used in the fabrication of transmission-delay-line-based RFIDs and RFID based sensors. Complete layout design, integration and fabrication, and characterization of the UHF tags based on the LC delay line concept and transmission delay line concept are discussed in Chapter 5 and Chapter 6, respectively.

4.2 Component Design

All the devices and components are designed and modeled with overall tag layouts in mind. These models have been simulated using software packages such as, Ansoft Designer [40]. Component values of inductors, capacitors and other elements of the LC-delay-line-based RFIDs have been obtained from the reactance values of the simulated lumped ID circuit simulation [35]. Devices such as, diodes, isolators and resistors are represented in the simulations either by exact vendor components or their equivalents. In the case of the transmission-delay-line-based tag layouts, circuit level simulations have been implemented using lumped delay elements to assess the adaptability of the tags to different communication schemes. Figure 4.1 shows the stacked-up structures for the low-cost fabrication processes (Section 3.3) and conventional processes (Section 3.5).

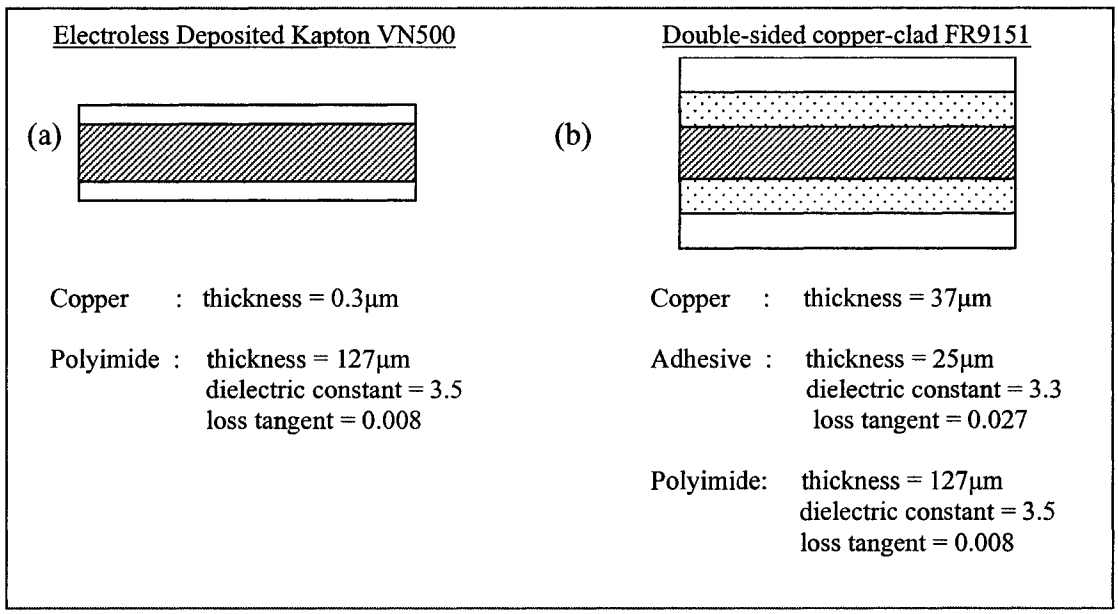


Figure 4.1 Layout architecture for modeling and simulations (a) substrate stack up for proposed low-cost fabrication on Kapton VN500 (b) substrate stack up for silicon-based processes on FR9151.

Low-cost fabrication processes are implemented on Kapton 500VN film and the FR9151 substrate is used for fabrication using conventional processes. The same stacked up layers are maintained for the simulation of all components corresponding to the type of processes used for fabrication.

A new adhesive layer material has to be defined in Ansoft Designer to simulate devices that need to be fabricated using conventional processes on FR9151. This adhesive layer is present in between the copper and polyimide layers on top and bottom of FR9151. The properties of the adhesive are obtained from the vendor [71]. Figure 4.2 shows the 'View/Edit Material window' of Ansoft Designer with the defined parameter values.

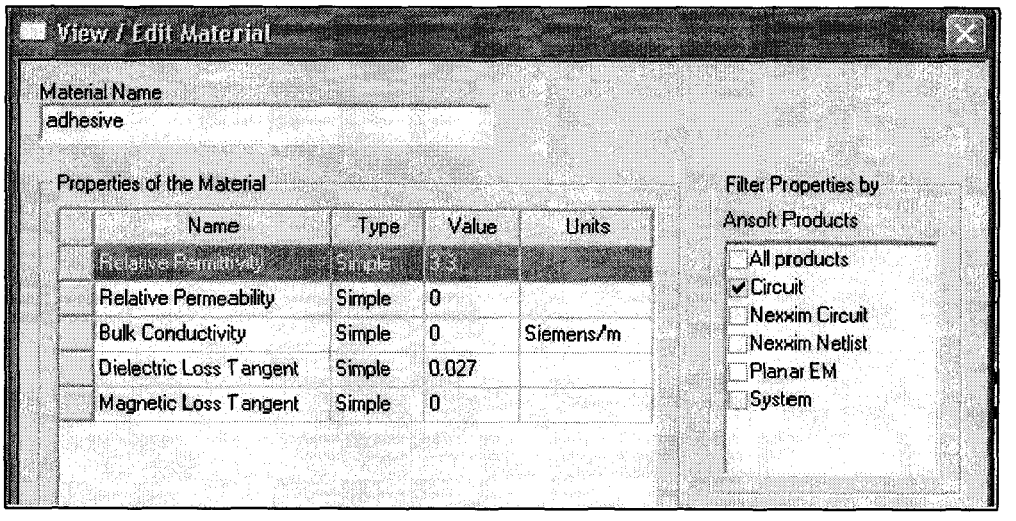


Figure 4.2 Ansoft View/Edit Material window showing parameters of the adhesive material for FR9151.

A thin layer of insulation is present on the copper layer of FR 9151 to protect it from oxidation. The stack-up can still be considered as a microstrip so long as the total thickness including substrate thickness, insulation thickness and the conductor thickness,

is less than 1.2 times the substrate thickness. If the ratio exceeds 1.2, then equations for an embedded microstrip should be considered. Once designed, component layouts are exported into*.dxf or *.gds formats and then converted into printer compatible formats such as, *.ps or *.pdf. These formats are also compatible with mask making for optional conventional process. Using these masks, devices are fabricated using the proposed low cost fabrication processes. The silicon-based fabrication processes explained in Section 3.7 are used whenever the proposed fabrication processes failed to yield devices of above average performance. Remedies and alterations required to the proposed process flow are discussed wherever necessary. However, individual components such as, inductors and capacitors are not fabricated using conventional processing on FR9151 because this research is reported in prior thesis work, as mentioned in Section 1.6.

4.2.1 Microstrip-based Modeling and Simulations

Both the layer stack-ups shown in Figure 4.1 can be viewed as microstrip structures. A microstrip is defined by a conducting trace line on a substrate with a ground plane on the opposite side (Figure 4.3). This trace line can be an interconnect, an electrode or a transmission line equivalent device. In general, each trace line can be viewed as a transmission line.

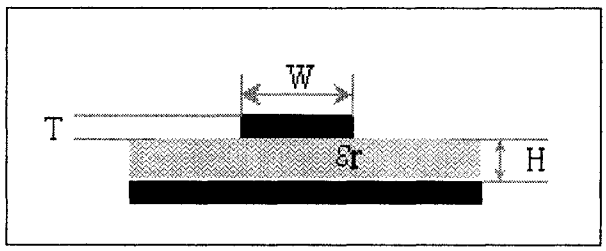


Figure 4.3 Schematic diagram of a microstrip.

A transmission line is characterized by its characteristic impedance. The width W, thickness T, substrate thickness H and dielectric constant ε_r determine the Characteristic Impedance of transmission lines, which is explained later in this chapter.

In a microstrip, the dielectric constant ε_r of the dielectric material will be different from the one that is seen by a microstrip transmission line of width W and thickness T. This is because of the flux leakage into the air above the transmission line, combined with the flux penetrating into the dielectric material. Thus, the effective dielectric constant is given by [46],

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \left(\frac{\varepsilon_r - 1}{2} \cdot \frac{1}{\sqrt{1 + \frac{12}{h}}} \right) \tag{4.1}$$

where ε_{eff} is the effective dielectric constant that the microstrip sees, ε_r is the actual dielectric constant of the substrate material, and h is thickness of the substrate material between the top conductor and bottom ground plane of the microstrip.

Microstrip equations are used to model the devices to be fabricated using the proposed low cost fabrication flow on Kapton 500VN and the dimensions obtained from the equations are used as initial values in the simulation. The same values are used for devices that need to be modeled on FR9151 with conventional processes. Initial values for devices based on FR9151 can also be obtained from the microstrip equations and using the equivalent dielectric constant of the substrate and adhesive materials of FR9151. Table 4.1 gives the effective dielectric constants for transmission lines of typical characteristic impedances as deposited using the proposed low cost fabrication processes on Kapton 500VN.

Table 4.1 Effective dielectric constants for different characteristic impedances.

Characteristic Impedance	Effective Dielectric Constant
30 Ω	1.51
50 Ω	2.75
100 Ω	0.60

The wavelength of the signal in the substrate will be different from the one that it has when traveling in vacuum. Thus λ, the effective wavelength is calculated using [46]

$$\lambda = V_p X(\lambda_{Vac}), \tag{4.2}$$

where λ_{Vac} is given by

$$\lambda_{Vac} = 11800/f \tag{4.3}$$

and V_p is the fraction of the speed of light compared to light in a vacuum and is given by

$$V_p = 1/\sqrt{E_{eff}}\ . \tag{4.4}$$

Here ε_{eff} is defined by Equation 4.1. These equations are to be kept in mind while designing microstrip-based components. These equations can be solved for any characteristic impedance traces required by the design. Table 4.2 gives the values of effective wavelength λ and velocity of propagation V_p for typical characteristic impedances.

Table 4.2 Effective velocity of propagation and equivalent wavelength for different characteristic impedances.

Characteristic Impedance	Velocity of propagation	Equivalent Wavelength
30 Ω	0.81 m/s	0.265 m
50 Ω	0.60 m/s	0.196 m
100 Ω	1.29 m/s	0.423 m

Devices and components such as, capacitors, inductors, interconnects and ID circuits can be designed using the above mentioned microstrip based rules. Inductors and capacitors can be either represented by equivalent microstrip transmission lines or planar lumped structures. Interconnects, on the other hand, are useful in impedance matching between the components and for interconnecting the different components of the system.

4.2.2 Copper Thickness Considerations

The thickness of copper achieved by a given process is another significant factor in determining the design of the components. High frequency signals are denser on the outer surface of a wire rather than with in the wire. Therefore, thinner transmission lines are sufficient as the frequency of operation increases. The phenomenon is known as skin effect and the depth to which these signals penetrate is called the skin depth and given by [46]

$$d = \sqrt{\frac{2\rho}{\omega\mu}}, \tag{4.5}$$

where ρ is the resistivity of the conductor, ω is the angular frequency of the current which equals to 2π times the frequency, and μ is the permeability of the conductor. This depth corresponds to 2.19 μm for a signal of 915 MHz and 18 μm for a 13.56 MHz signal below which losses start to appear. As explained earlier, even though Cuprothick ready-to-use copper bath promises a thickness of 2.2 μm on PCBs, it is hard to achieve the same on polyimide substrates due to poor adhesion and a relatively smooth surface. A thickness of 0.3 μm to 0.4 μm is achieved from electroless plating in our lab and experiments are continuing to optimize the process to further increase the thickness. Therefore, all simulations are done with 0.3 μm thick copper on the substrate in the simulation stack up.

Non-uniformity of the edge of the printed patterns is not considered for simulations and is attributed to differences in the simulated and practical results presented in this chapter.

4.3 Inductors

Due to the fabrication constraints, planar inductors are chosen to realize the inductor values of the simulated ID circuit. Planar Meander and triangular inductors are preferred over spiral inductors because of fabrication complexities involved in connecting the ends of the inductor to the rest of the circuit. Therefore, Meander and triangular Meander planar inductors are modeled and simulated [35] with the prime goal of achieving a reactance value of 574.9 Ω. These layouts are modified to make them printable with a laser printer and to simulate inductors with a copper thickness of 0.3 μm achieved using the electroless copper process. Theory, simulations, fabrication and other issues involved in the fabrication of inductors using the low-cost processes are explained below. Design and fabrication using conventional processes have also been done in order to compare the inductors made by both processes.

4.3.1 Design Considerations

A shorted microstrip transmission line of length less than λ/4 or an open microstrip transmission line of length greater than λ/4, act as an inductor. A microstrip transmission line can be designed to act as an equivalent inductor by decreasing the width to be less than the width that corresponds to a 50 Ω characteristic impedance. Equation 4.6 gives the required length L of a microstrip of characteristic impedance, $C.I$ and input reactance X_l for a signal of wavelength λ [46].

$$L = \frac{\left(\tan^{-1}\frac{X_l}{CI}\right)}{360}\lambda \qquad (4.6)$$

where λ is the equivalent wavelength for 100 Ω of characteristic impedance (Table 3.3). Therefore, a required inductance value of 0.1 μH would correspond to an X_L of 574.91 Ω. Equation 4.5 gives the corresponding length as 9.41cm which is more than the maximum allowed distributed component's length of λ/12, or 2.7 cm, for a 915 MHz signal. Rectangular and triangular Meander inductors are convoluted in the structure and, therefore, can fit a small form factor. These can be designed such that there is a minimum field canceling effect between adjacent lines of the inductor.

Planar inductors for HF and UHF frequencies, that can be patterned using a laser jet printer, need to be carefully designed due to resolution limitations. Inductance increases with a decrease in line width and decreases with decreasing metal thickness. These parameters certainly limit our capability of achieving inductors of values covering a broad range. The form factor should not be too large to avoid any interference with the incoming signal on electrically large components.

The inductor's dimensions are adjusted according to the printer resolution. It was observed that the inductance, and thus the reactance of the inductor, changes with respect to the thickness of the copper and number of turns (Figure 4.4).

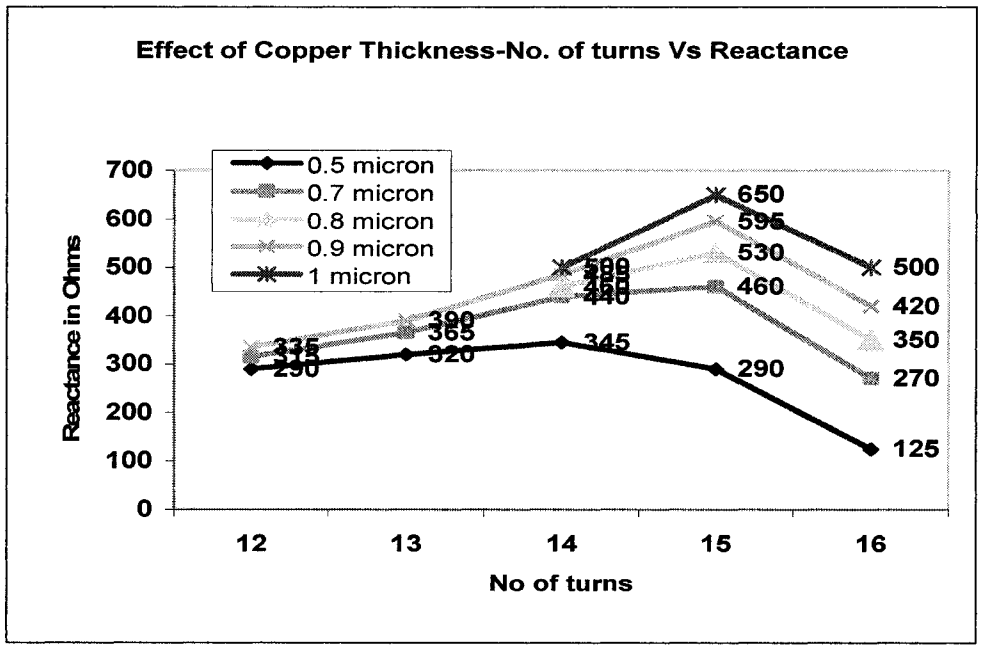


Figure 4.4 Reactance change in simulated triangular planar inductors with respect to thickness and number of turns.

A line width which is a third multiple of the minimum printable dot size of the laser-jet printer has been taken as the width of the planar inductor. This value is obtained based on the resolution experiments done with the printer. The distance of separation between the lines is also chosen to be a multiple of the minimum printable dot size. This strategy ensures that the designed layout can be printed without any discontinuities or breaks. This is very important to ensure the continuity of the copper after the electroless deposition step.

Our goal of designing an inductor with 574 Ω reactance could not be achieved for the ID circuit design. A trade off between a printer patternable structure, 0.3 μm thickness of electroless copper, form factor and maximum obtainable reactance value resulted in a design reactance of 190 Ω. It was decided that the decrease in the inductor's reactance

can be compensated for the design of the capacitor for the delay element of 0.275 ns for the four bit ID generation circuit for 915 MHz.

Inductors with sufficient copper thickness will certainly yield the required reactance value of 575 Ω. Therefore, previously modeled inductor layouts [35] are modified to emulate FR9151 stack up and silicon-based fabrication requirements (Figure 4.5). The inductor layout has been modified to accommodate an infinite metalized ground layer which represents the practical tag configuration. The inductor has its transmission coefficient S_{12} and reflection coefficients S_{11} as 0.98 and 0.034, respectively which is much less than the assumed tolerance value of 0.1 for the complete system. The inductor has a characteristic impedance of approximately 108.0 Ω. It was observed that inductors with a small form factor, compared to λ/12, will have good s-parameters.

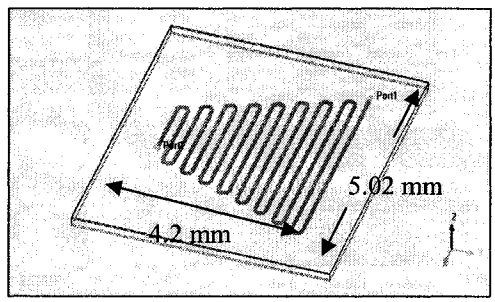


Figure 4.5 Modified inductor layout for photolithography on FR9151.

4.3.2 Fabrication and Characterization

Figure 4.6 shows the inductor patterns printed on a polyimide substrate using a laser jet printer. There are no discrepancies in the continuity of the pattern visible to the naked eye and a lot of unwanted toner material can be seen on the inductor pattern as viewed with the optical microscope. Electroless deposition yielded a seemingly

continuous inductor pattern but suffers with discontinuities due to unwanted particles. The toner can be removed by sonicating in toluene/acetone solution as explained earlier.

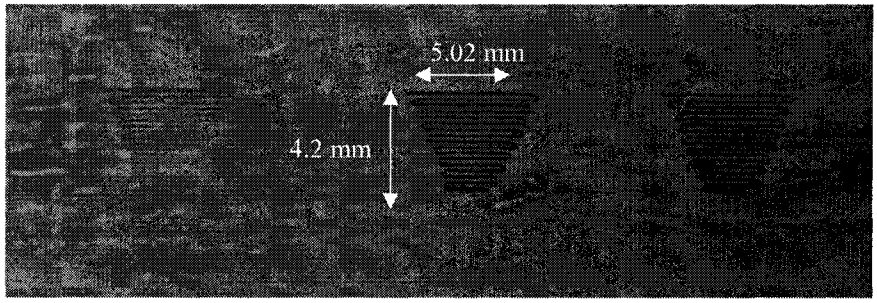


Figure 4.6 Inductor structures patterned with laser printer on polyimide substrate.

As explained earlier, individual inductors are not fabricated using conventional processes on FR9151 because the process is described in previous thesis work, as mentioned in Section 1.6. However, the modeled layout is used in the integrated tag layout, which is fabricated using the conventional process on FR9151.

4.4 Capacitors

Capacitors of different form factors can be made for the tag. For a given reactance, the length of the capacitor electrode increases when the line width is decreased. The modeled parallel plate capacitors [35] have been changed into capacitor equivalent microstrip transmission lines to meet the tag's requirements. This is done by placing a metalized ground on the bottom layer. The width of the capacitor has been adjusted to decrease the gamma or reflection coefficient below the assumed tolerance value of 0.1 or -10 dB.

4.4.1 Design Considerations

A microstrip transmission line can be used as an equivalent capacitor by increasing its line width more than a lossless interconnect corresponding to a 50 Ω characteristic impedance. Lumped component circuit level simulation of the ID circuit shows that the required value of the capacitor C is 0.756 pF which corresponds to a reactance X_c of 232 Ω. The length, L of such a capacitor equivalent of transmission line of characteristic impedance CI is given by [46]

$$L = \frac{\left(\tan^{-1}\frac{CI}{X_c}\right)}{360}\lambda \tag{4.7}$$

where λ is the equivalent wavelength. Equation 4.7 yields a length of 0.54 cm for a line width corresponding to 30 Ω characteristic impedance. Thus a distributed capacitor equivalent will not create real estate problem unlike a distributed inductor for the chosen inductance and capacitance values. Therefore, it is feasible to design capacitor equivalent of transmission line for the tag. If the circuit required values that correspond to larger capacitors, then n capacitors of smaller form factors corresponding to 1/n capacitance can be added in parallel such that the equivalent capacitance equates to the required value.

Capacitors are more easily fabricated as they are large in area and thus do not require high resolution printers. A 230.2 Ω reactance capacitor has been simulated using the low-cost process flow stack up. For simulating capacitor for conventional processes on FR9151, the gds layout obtained [35] has been imported intoAnsoft file to simulate its impedance and see its compatibility. The value of the capacitor from the lumped component simulation is 0.756 pF that corresponds to X_c of -230.2 Ω. Initial stack up has been changed to add the adhesive layer present in the FR9151 stack up. Parallel plate

capacitor has been changed to capacitor equivalent of transmission line by changing the dimensions of the plate on the top to accommodate infinite ground layer at the bottom. The capacitor along with the interconnect has a reflection coefficient of 0.17 and transmission coefficient of 0.98 (Figure 4.7). The capacitor has a characteristic impedance of approximately 16.30 Ω. This impedance mismatch should be taken care of while designing the circuit.

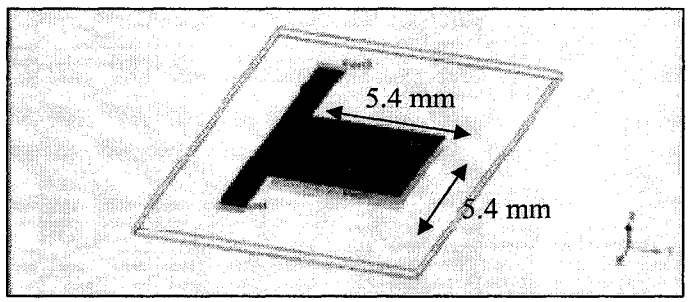


Figure 4.7 Modified capacitor layout for photolithography on FR9151.

4.4.2 Fabrication and Characterization

The same set of low cost fabrication steps discussed in Section 4.3 have been implemented to realize the copper patterns shown in Figure 4.8.

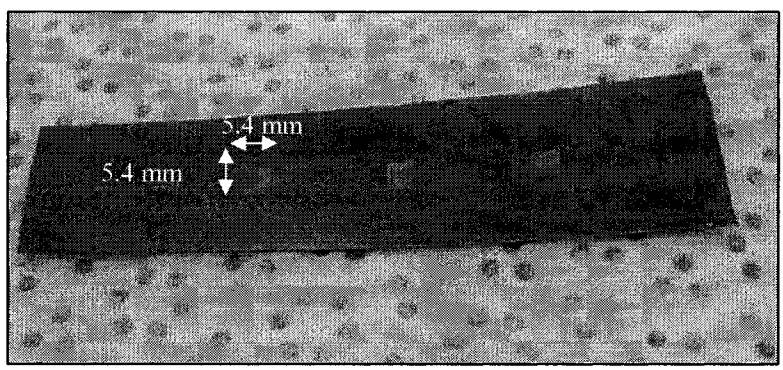


Figure 4.8 Capacitors patterned with laser printer and electroless plated on a polyimide substrate.

In the simulations interconnects should be attached to the sides of the electrode plate and not vice versa, because attaching the plate to the interconnect line will give an erroneous reactance value. Capacitor dimensions offer flexibility in the real estate design of the tag and in impedance matching. This is explained later in the next chapter.

4.5 Resistors

Optimization of the lumped component circuit level simulations of the ID tag resulted in three resistors of values 50 Ω, 244.9 Ω and 10 MΩ, respectively. Experiments have been conducted to realize these values using PEDOT/PSS solution on copper. Simulations are done to design layouts suitable for RF characterization.

4.5.1 Design Considerations

A simple resistor will present reactance in addition to its own resistance as the frequency of operation is increased. This is due to the parasitic capacitance that shunts the current across the resistor. The leads of the resistor present parasitic inductances and therefore, surface mount (SMT) resistors are used for high frequency circuits. Experiments have been designed to observe the performance of the planar resistor patterns fabricated using low cost processes and PEDOT/PSS as the main resistor material.

A set of ten pairs of 50 Ω characteristic impedance microstrip lines have been designed for the resistor electrodes, with varying distance of separation between them. Each electrode is simulated both separately and in proximity to each other to obtain their intrinsic parasitic reactances. This will help in determining the parasitic reactances during

the characterization of the resistor patterns. Figure 4.9 shows the schematic diagram of the electrode patterns made in the Ansoft simulation software.

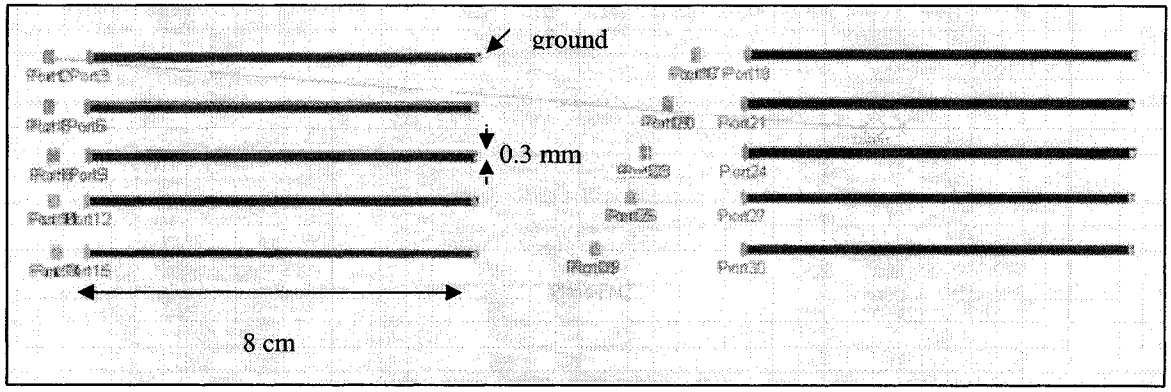


Figure 4.9 Modeled resistor patterns of different sizes on the simulation software screen.

4.5.2 Fabrication and Characterization

A Kapton 500VN film is loaded into a laser jet printer and a soft copy of the patterns for the copper electrodes that were designed using Ansoft, as earlier explained, was used to print the electrode patterns. Electroless copper has been deposited in the patterns and the toner is removed. PEDOT/PSS is drop cast to make the resistor patterns using a syringe. After heating the PEDOT/PSS patterns at 80^0C for 10 minutes, the patterns are analyzed using Keithley electrical characterization equipment and an impedance analyzer.

D.C characterization using the Keithley electrical characterization system shows that resistances varying from approximately 1000 Ω to 10 MΩ can be obtained using PEDOT/PSS patterned on copper electrodes, or a combination of varying concentrations of PEDOT/PSS and Ethylene Glycol. Figure 4.10 shows the IV characteristics of one such pattern.

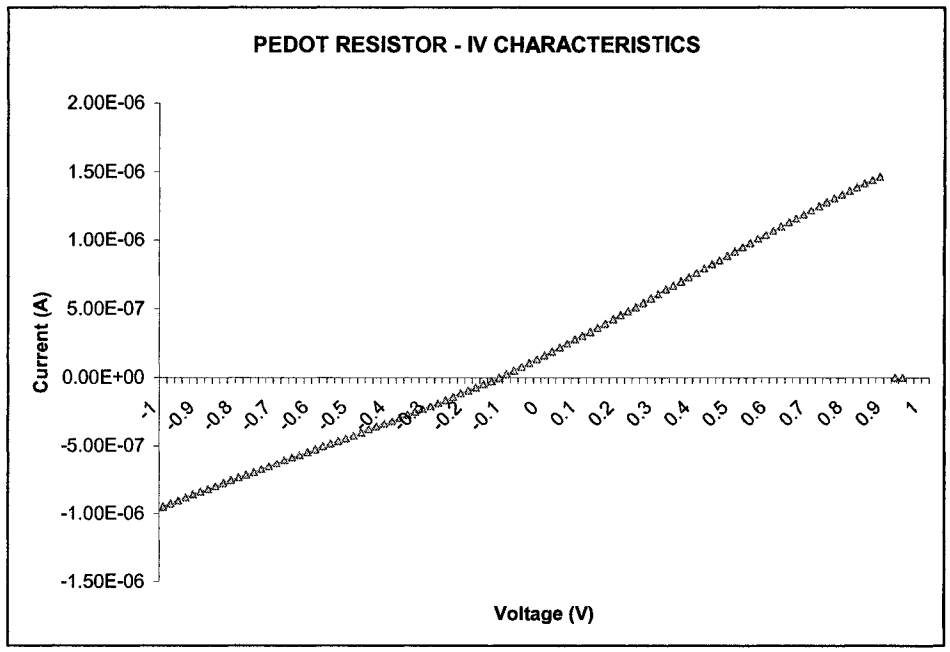


Figure 4.10 DC characteristics of PEDOT/PSS resistor.

4.6 Transmission Lines

Transmission lines of different characteristic impedance have been modeled for connecting the source to the load and as interconnects between different devices of the ID circuit. A 50 Ω characteristic impedance is generally used for connecting different components. For connecting an inductor to a capacitor the value of the characteristic impedance of the interconnect is chosen to be the mean of the characteristic impedances of inductor and capacitor. The interconnects inside the ID circuit are kept electrically small in length to reduce parasitic capacitances. The inherent capacitances of the interconnects are nullified by taking their value into consideration while designing the capacitors.

4.6.1 Design Considerations

Microstrip transmission lines are designed for 50 Ω constant impedance throughout its length which, in general, is known as characteristic impedance, and will

not add any inductance or capacitance. These transmission lines eliminate reflections, maximize power transfer and avoid mismatch losses between physically separated components over electrically long distances for the given frequency. The ideal microstrip transmission line will have only I^2R losses. The characteristic impedance Z_0 of the microstrip transmission line is given by [46]

$$Z_0 = \frac{377}{\left(\frac{w}{h}+1\right)\sqrt{\varepsilon_r + \sqrt{\varepsilon_r}}} \tag{4.8}$$

where w, h, and ε_r are defined in Equation 4.1. Different microstrip trace calculators are available on the internet that can calculate the width of the microstrip interconnects, given the thickness of the substrate, conductor and other values [72,73].

The line width of the microstrip transmission line for 50 Ω characteristic impedance has been calculated using Equation 4.8 and taken as the initial value for further refinement using Ansoft simulation software. As a design rule, interconnects should be as short as possible and straight. Curves, if required, should be smooth. Simulations with the metalized ground layer at the bottom showed that there is no change in the characteristic impedance out to two decimal places after the decimal point, even if the interconnect was bent or sharp. The simulated interconnects have been exported as the layout for fabrication using low-cost processes on the Kapton 500VN substrate. Simulations for the proposed processes and stack-up resulted in an interconnect of line width 289.65 μm and simulations of conventional processes on FR9151 resulted in 406.25 μm line width patterns.

4.6.2 Fabrication and Characterization

As explained earlier, different pairs of interconnects with varying distance of separation are designed using Ansoft and later patterned on the Kapton VN500 film using a xerographic process and then electroless copper is deposited. Values ranging from 500 kΩ to 10 MΩ have been obtained from these resistor patterns.

4.7 Diodes

Copper-PEDOT/PSS junctions show schottky behavior but are not of use at the RFID frequencies of operation. The efforts made to simulate, fabricate and characterize metal-polymer schottky junctions have been described here. Even though these junctions are easy to fabricate, researchers could not realize a polymer switching device that can operate satisfactorily at 1 MHz or more [74-81]. These junctions can not work at higher frequencies because of the low mobility of charge carriers in the polymer, and poor interface properties. Therefore, it was decided to use conventional solid state diodes for the tags. Different diodes can be used for the HF and UHF tags. PIN diodes work below 50 MHz and are useful for 13.56 MHz and 125 KHz applications. Schottky and Gun diodes having ranges up to 100 GHz can be used for UHF applications. Fast-Recovery Diodes switch within 200 ps or less and have appreciable performance up to 5 GHz or more. We have used Schottky diodes such as, MA4E1338A-1141T (Macom.com) and HSMS 2820/2850 (Agilent) for our HF and UHF circuit.

4.7.1 Design Considerations

Different commercially available schottky diodes and other radio frequency diodes have been tested for their performance in the tag. Most of the diodes chosen have

corresponding vendor components in the Ansoft Designer software, thus allowing circuit level and system level simulations that represent practical conditions. The MA4E1338A-1141T Schottky diode that we tested does not have a vendor component in Ansoft Designer and, therefore, necessitated the need for creating one. Table 4.3 shows the averaged vendor values for different spice parameters. The DC characteristics of the diode are determined by the parameters IS, N, and the ohmic resistance RS. Charge storage effects are modeled by a transit time, TT, and a nonlinear depletion layer capacitance which is determined by the parameters CJO, VJ, and M. The temperature dependence of the saturation current is defined by the parameters EG, the band gap energy and XTI, the saturation current temperature exponent. The nominal temperature at which these parameters were measured is TNOM. Reverse breakdown is modeled by an exponential increase in the reverse diode current and is determined by the parameters BV and IBV [82].

A .lib file is created by inserting the parameter values into Pspice Model editor (Orcad Demo Model Editor, Pspice Student version 9.1). The created file is imported intoAnsoft's system library and used in the ID circuit and system simulations. Figure 4.11 shows the ID generated with the spice modeled diode placed in the lumped circuit.

Table 4.3 Spice model parameters for MA4E1338A-1141T Schottky diode (Charge storage effects and thus TT considered negligible at 915 MHz for this 4GHz Schottky Diode, ** since the diode is made of silicon, * 3 for pn diodes and 2 for Schottky diodes, # from the data sheet).**

	Name	Parameter	Units	Default	Vendor values
1	IS	Saturation current	A	1.0e-14	24.04e-9
2	RS	Ohmic resistance	Ω	0	7.618
3	N	Emission coefficient	-	1	1.188
4	Tt	transit-time	Sec	0	0.04f*
5	CJO	Zero-bias junction capacitance	F	0	0.222pF
6	VJ	junction potential	V	1	0.296
7	M	Grading coefficient	-	0.5	0.5
8	EG	Band-gap energy	eV	1.11	1.11 **
9	XTI	Saturation-current temp.exp	-	3.0	2.0***
10	KF	Flicker noise coefficient	-	0	0
11	AF	Flicker noise exponent	-	1	1
12	FC	coefficient for forward-bias depletion capacitance formula	-	0.5	0.039
13	BV	Reverse breakdown voltage	V	Infinite	13.076
14	IBV	Current at breakdown voltage	A	1.0e-3	10^{-5}
15	TNOM	Parameter measurement temperature	Deg C	27	25#

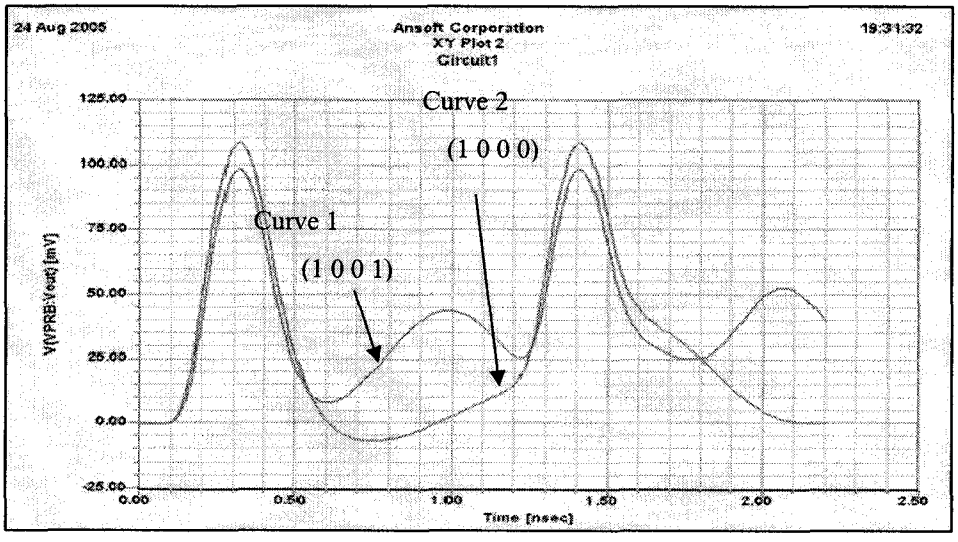


Figure 4.11 Different configurations of 4 bit codes generated using ID circuit with created spice model for MA4E 1338A-114T showing output signals representing 1000 and 1011.

Each curve shown in Figure 4.11 represents unique ID codes. If we take minimum threshold voltage for bit '1' around 30 mV and the sampling is done at the intervals of 0.275 ns, then it can be seen that the generated curves 1 and 2 represent 1001 and 1000 respectively.

4.7.2 Fabrication and Characterization

Copper is deposited on Kapton 500VN substrate through electroless deposition using laser jet printout as a shadow mask. PEDOT/PSS is deposited on the copper electrode using the drop cast method. I-V characteristics are obtained by keeping one of the Keithley electrical measurement system's probes on the copper and other on the polymer. Figure 4.12 shows the I-V curves obtained from one such PEDOT/PSS-copper junction by changing the position of the probe on the polymer region of the junction.

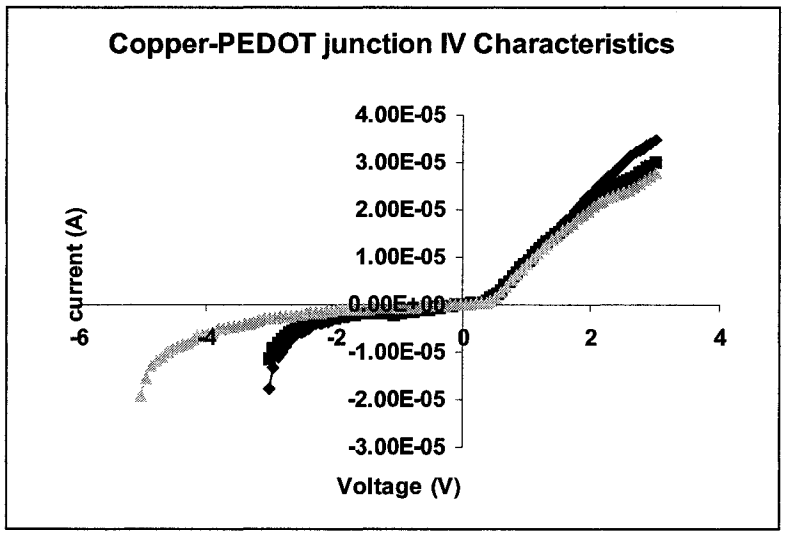
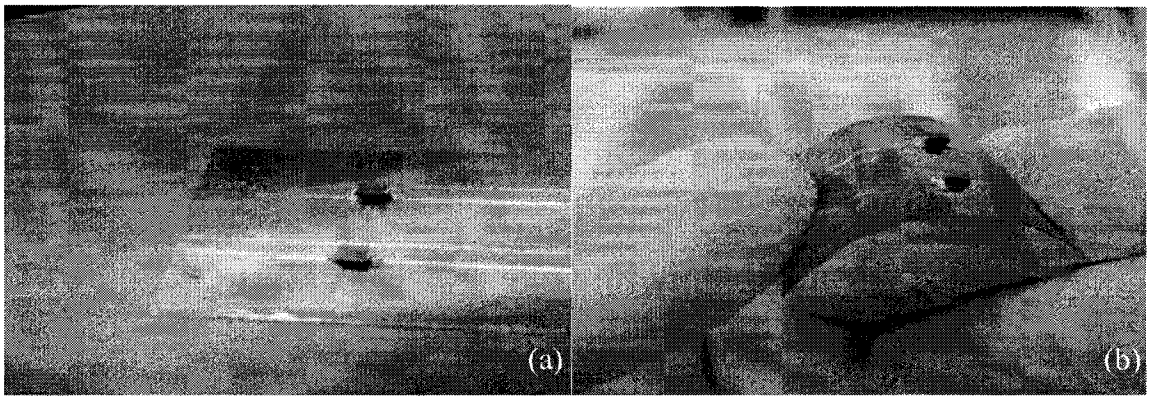


Figure 4.12 I-V characteristics of Copper-PEDOT/PSS junctions.

Diodes such as, MA4e1338A-114T, have been attached to the electroless copper patterns using conductive epoxy and I-V characteristics have been taken using the

Keithley Electric Measurement Station. Figure 4.13(c) shows the I-V characteristics of one such diode corresponding to the unstressed condition as shown in Figure 4.13(a) and after the application of bending stress as shown in Figure 4.13(b).



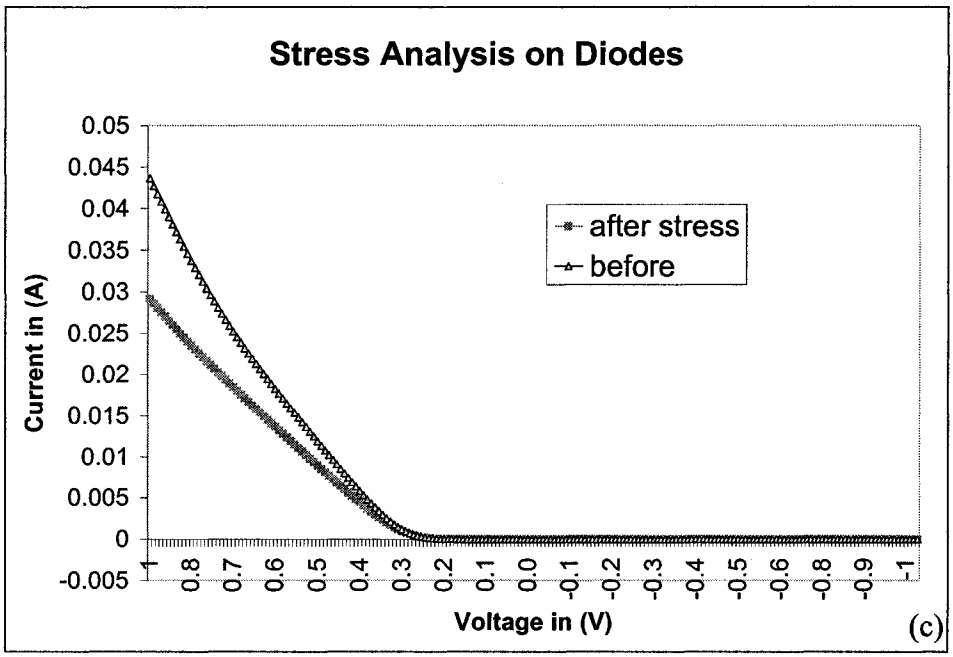


Figure 4.13 (a) Diodes attached to the copper patterns using epoxy before stress and (b) Diodes under stress (c) Effect of stress on the diode IV characteristics.

As described in the previous paragraph the polymer-metal schottky junction is compatible with the overall proposed hierarchy of fabrication processes but is not useful at HF and UHF ranges. Researches are able to make organic switching diodes that work

at speeds of a few megahertz. Once a properly-engineered processible polymer with stability and satisfactory switchability at the required radio frequencies is available, these diodes then can be easily integrated into RFIDs and RFID-based sensors thus eliminating the need for assembling components. It is noted that soldering is not compatible with electroless copper patterns due to the lifting off of the very thin copper by the solder. However, performance of off-the-shelf diodes could not be established beyond a 10 MHz operating frequency. Soldering technique and modifications of the circuit might solve this problem.

4.8 Antennas

The antenna serves as the transducer between the controlled energy residing within the system and the radiated energy existing in free space. Antennas of different design and configuration have been compared under similar conditions using simulations. Optimized antenna designs have been simulated with electric field in the ambient and the resulting current from the antennas has been calculated using HFSS software and Field calculator. Antennas made with low-cost processes and conventional processes gave satisfactory performance in the field tests.

4.8.1 Design Considerations

Typical metrics used in evaluating an antenna include the input impedance, polarization, radiation efficiency, directivity, gain and radiation pattern. These are explained below.

Input impedance is the parameter which relates the antenna to its transmission line. It is of primary importance in determining the transfer of power from the transmission line to the antenna and vice versa. The impedance match between the

antenna and the transmission line is usually expressed in terms of the standing wave ratio (SWR) or the reflection coefficient of the antenna when connected to a transmission line of given impedance. The reflection coefficient expressed in decibels is called return loss.

Polarization is defined as the polarization of the electromagnetic wave radiated by the antenna along a vector originating at the antenna and pointed along the primary direction of propagation. The polarization state of the wave is described by the shape and orientation of an ellipse formed by tracing the extremity of the electromagnetic field vector versus time. Although all antennas are elliptically polarized, most antennas are specified by the ideal polarization conditions of circular or linear polarization [83]. The ratio of the major axis to the minor axis of the polarization ellipse defines the magnitude of the axial ratio. The tilt angle describes the orientation of the ellipse in space. The sense of polarization is determined by observing the direction of rotation of the electric field vector from a point behind the source. Right-hand and left-hand polarizations correspond to clockwise and counterclockwise rotation, respectively.

Directivity is defined as 4π times the ratio of the maximum radiation intensity (power radiated per unit solid angle) to the total power radiated by the antenna [84]. The directivity of an antenna is independent of its radiation efficiency and its impedance match to the connected transmission line. The gain, or power gain, is a measure of the ability to concentrate in a particular direction the net power accepted by the antenna from the connected transmitter. When the direction is not specified, the gain is usually taken to be its maximum value. Antenna gain is independent of reflection losses resulting from impedance mismatch. The radiation efficiency of an antenna is the ratio of the power radiated by the antenna to the net power accepted at its input terminals. It may also be

expressed as the ratio of the maximum gain to the directivity. Antenna radiation patterns are graphical representations of the distribution of radiated energy as a function of direction about an antenna. Radiation patterns can be plotted in terms of field strength, power density, or decibels. They can be absolute or relative to some reference level, with the peak of the beam often chosen as the reference. Radiation patterns can be displayed in rectangular or polar format as functions of the spherical coordinates, θ and φ.

Four antenna designs have been considered for performance comparison. They are the Hilbert antenna, two types of Fractal antennas, Fractal-1 and Fractal-2 [36] and Meander antenna [37]. Since they are designed on different simulation software packages such as, Ansoft Designer and HFSS, performance comparison is almost impossible. Irrespective of the simulations software, all antennas have shown a directional balloon shaped radiation pattern with a metalized ground layer beneath them but in general suffered from low gain. On the other hand, there is a considerable increase in the gain, if the ground layer beneath the antenna is removed but causes a reduction in the directionality of the radiation pattern. Therefore, all four layouts have been imported into Ansoft Designer and simulated under two sets of approximately similar conditions namely, condition-1 and condition-2. Condition-1 includes a metalized ground around the antennas but not beneath the surface of the antennas. There are dissimilarities in the way the port is defined in the individual designs, and because there is a need for a ground layer under the port for proper simulations, a 0.01mm width ground layer has been left under the port for each individual antenna. Condition-2 includes a complete metalized ground layer beneath the antennas. The results obtained from the simulation are given in Table 3.5. These values are good for relative comparison and do not represent optimized

individual antenna parameters. Thus, Meander and Hilbert antennas have been chosen for further integration into the tag.

There is a way to extract current, and thus power, from the simulated antennas in the HFSS software and a special calculator and recipe provided by the software vendor did not give values close to the practical values obtained.

Table 4.4 Antenna parameters for different designs under similar conditions.

Sl.No	Antenna	Condition	Gain (dB)	Z_{11}	$\|S_{11}\|$	Remarks
1.	Meander	Condition1	-23.67	28.57+j131.90	0.95	Highly directional
		Condition2	-33.32	62.65-j160.85	0.93	Highly directional
2.	Fractal-1	Condition1	-65.00	05.10+j481.00	1.00	Omi directional
		Condition2	-66.38	1.67-j122.19	0.99	Directional
3.	Fractal-2	Condition1	-45.00	07.92-j783.80	1.00	Omni directional
		Condition2	-64.36	63.79+j0	0.99	Directional
4.	Hilbert	Condition1	-11.18	01.92-j30.61	0.94	Directional
		Condition2	-35.89	4.05+j34.06	0.89	Directional

It is also observed that antennas with copper thickness more than the minimum skin depth do not depend on the thickness of the copper. However, since the maximum deposition thickness achieved in our lab was approximately 0.3 μm, their antenna performance decreases. Electromagnetic waves of less than the allowed power specified by FCC are made incident on the simulated receiving antennas.

4.8.2 Fabrication and Characterization

Antennas are fabricated using low-cost material and processes explained in Section 3.3 and Section 3.4. Figure 4.14 (a) and (b) shows the fabricated Hilbert and Meander configurations.

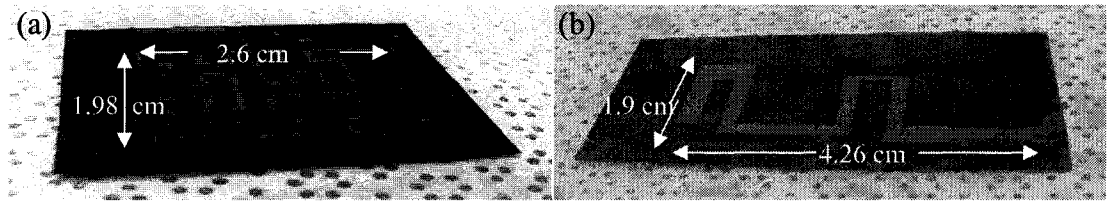


Figure 4.14 (a) Hilbert antenna and (b) Meander antenna, fabricated using low-cost processes on Kapton 500VN.

These antennas are simulated to observe the thickness of the copper on their performance. Antennas have also been simulated for conventional processes on FR9151. The obtained results are detailed in Table 4.5.

Table 4.5 Performance characters of Hilbert and Meander Antennas.

Sl. No	Stack Up	Copper Thickness	Gain in dB	VSWR	Input Impedance	S_{11}
Meander						
1.	FR9151	37 μm	-33.32	27.5	62.65-j160.8	0.93
2	Kapton 500 VN	2.2 μm	-35.52	28.68	12.38+j0	0.93
		0.8 μm	-37.81	16.91	12.38+j0	0.89
		0.4 μm	-39.98	10.31	12.38+j0	0.82
		0.3 μm	-40.99	8.21	12.38+j0	0.78
Hilbert						
Sl. No	Stack Up	Copper Thickness	Gain in dB	VSWR	Input Impedance	S_{11}
1.	FR9151	37 μm	-33.32	27.5	62.65-j160.8	0.93
2	Kapton 500 VN	2.2 μm	-35.52	28.68	12.38+j0	0.93
		0.8 μm	-37.81	16.91	12.38+j0	0.89
		0.4 μm	-39.98	10.31	12.38+j0	0.82
		0.3 μm	-40.99	8.21	12.38+j0	0.78

4.9 Sensor Switch

One of the main obstacles in the realization of RFID-based sensors is powering of the sensor. A sensor that would consume low power (few microwatts) or supplies power to the sensor would eliminate this problem. Solar cells, piezoelectric and pyroelectric

materials generate energy and can be used to turn on a switch such as, an FET. Materials like quantum tunneling composites and PANI change from insulating state to conducting state nonlinearly when they sensed quantity reaches a threshold value. Thus there is no battery in the proposed layout and the sensor switch operates either on its own with the generated energy or passively. Quantum Tunneling Composite (QTC), polyvinylidene fluoride (PVDF) and polyaniline (PANI) sensors are considered in particular. To simplify the fabrication, a simple switch model is chosen rather than a complex multilevel switch.

As explained earlier, the LC-delay-line-based RFID-based sensor is actually an LC-delay-line-based RFID with a sensor switch in series. Any material that has a non-linear behavior and has the capability to stand alone can be considered for the switch. The sensor switch is an interface between the sensor element and the RF path of the RFID circuit. Three different types of sensing material were considered for integration into our RFID-based sensors. They are 1. QTC, 2. PVDF and 3. PANI. The materials were first tested for their sensing capabilities [38,85] and initial experiments showed promising results. The sensor switch layout on the tag depends on the properties of the sensor material and its fabrication method.

4.9.1 Design Considerations

The resistance of a QTC material changes exponentially under pressure making it ideal for its use as a switching element for pressure sensing. In these materials, the metal particles are separated by a polymer lattice and never come into physical contact. They get very close under pressure and Quantum Tunneling occurs between the metal particles which are now separated by quantum scale distances. Quantum Tunneling is a phenomenon which is derived from Quantum Mechanics in which an electron is not

viewed as a solid particle but more like a wave which is the probability that the electron would happen to be at that location. When the wave meets a barrier, for instance a non-conductive material, the wave doesn't instantly go to zero, but decays exponentially. If the wave hasn't reached zero by the time it has reached the other side of the barrier, then it emerges on the other side which means that the electron has effectively "tunneled" through the non-conductive barrier. Moreover, QTC material is modeled as an RF resistor switch because it is known to conduct high frequency signals. QTC materials are new to the market and offer the potential new applications.

Piezoelectric materials such as, PVDF, generate a charge when a pressure is applied. The charge developed can be converted into a voltage, if a capacitor structure is used with PVDF between its electrodes. The charge developed is due to the aligning of the dipoles in the material and this polarization occurs only in the area where pressure is applied. The charge disappears once the pressure is removed and the material acts as any other dielectric material. These materials are not good as current sources but certainly are good voltage sources in the sense that any magnitude of the voltage can be obtained by the capacitive effect, given by the equation

$$V=Q/C \tag{4.9}$$

where Q is the charge developed by the piezoelectric material, C is the capacitance of the capacitor, V is the voltage developed. Certain types of polyaniline change their conductivity exponentially when they detect acidic fumes such as those that emanate from fruit and vegetable spoilage. Thus, polyaniline can be used to detect the freshness of the fruit, if carefully designed.

4.9.2 Modeling and Simulations

Both QTC and PVDF are pressure sensitive and change their properties only in the area where pressure is applied. Therefore, the layout should be such that the switch should respond whenever pressure is applied to the sensing area. The sensing area should be large in general compared to the other components of the tag. This is the same case as with the polyaniline sensor, because a larger sensing window would make the sensor accessible to a large sensing ambient. The modeling and simulation of the sensor switch layouts for all three types of sensor materials described above, have been described below.

4.9.2.1 Layout for quantum tunneling composite and polyaniline sensor switch

QTC material is available as film and pallets. Pallets are more pressure sensitive compared to film. An RFID-based sensor should have maximum on-board real estate for pressure sensing. Thus, film is chosen and the layout is modeled as an interdigited structure 1 cm x 1 cm in area as shown in the Figure 4.15 (a). This structure can be expanded over the required area on which the QTC film can be glued at the edges. When pressure is applied on the film, adjacent electrodes beneath the film are shorted thus turning 'on' the switch. But when the area of this layout has been increased, the open ended electrodes radiate considerably and act like antennas thus causing crossover and interference effects. Simulations show that a 2 cm x 3 cm interdigited structure (Figure 4.15 (c)) has a negligible change in its S-parameters when it is short circuited, thus making it unusable for a sensor switch. On the other hand, there is a clear change in the reflection and transmission coefficients for the layout with a 1 cm x 1 cm area. Table 4.6

shows the comparison of S-parameters for both form factors. The layout with a 1 cm x 1 cm area shown in figure 4.15 (a) can be used for freshness detection sensor by coating polyaniline on the interdigited layout. When polyaniline senses gases from spoilage the comb like structures of the layout will be shorted to one another.

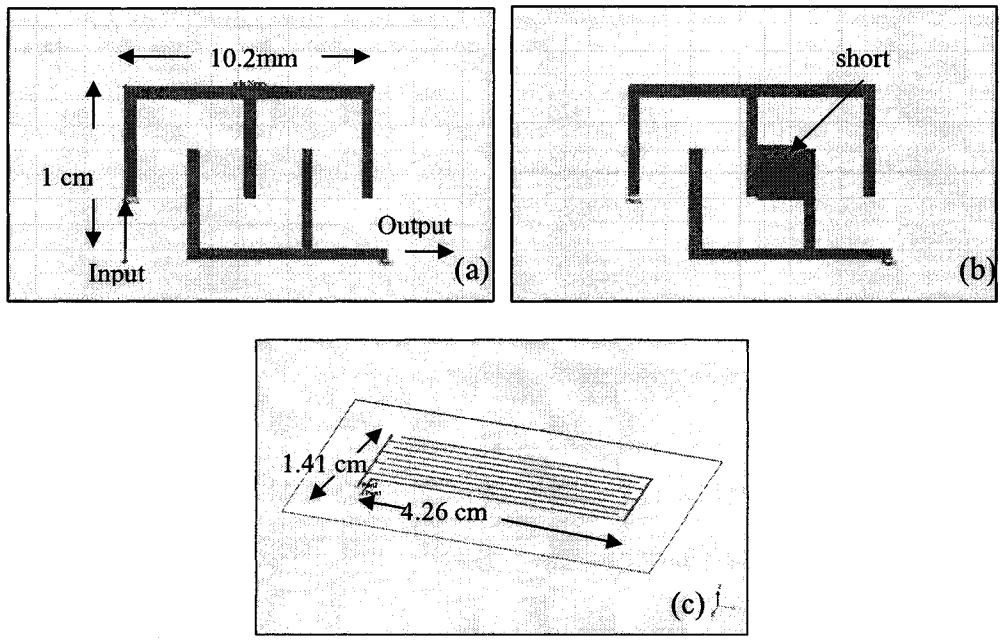


Figure 4.15 Sensor switch layout for QTC and freshness sensors (a) interdigited simulated structure (1.02 cm x 1 cm) (b) with short circuited electrodes (c) structure with large form factor (1.41 cm x 4.26 cm).

Table 4.6 S-parameters of sensor layouts of different areas.

Sl. No	Sensor Layout Area	Condition of Electrodes	$\|S_{11}\|$	$\|S_{12}\|$
1.	1.02 cm x 1cm	Open	0.98	0.00
		Shorted	0.30	0.90
2.	1.4 cm x 4.26 cm	Open	0.93	0.04
		Shorted	0.89	0.05

4.9.2.2 Layout for Polyvinylidene fluoride sensor switch

The voltage across a capacitor corresponding to the charge developed depends on the capacitance. The sensitivity of PVDF is in the range of a few pC /N. Therefore, a 1 cm x 1 cm area electrode with a PVDF film on it would produce enough voltage to turn on a commercially available FET (Figure 4.16). This model was based on the initial experiments conducted at lower frequencies. Since the voltage generated is DC and is of small area, it will not be electrically long to act as the antenna on the tag's layout.

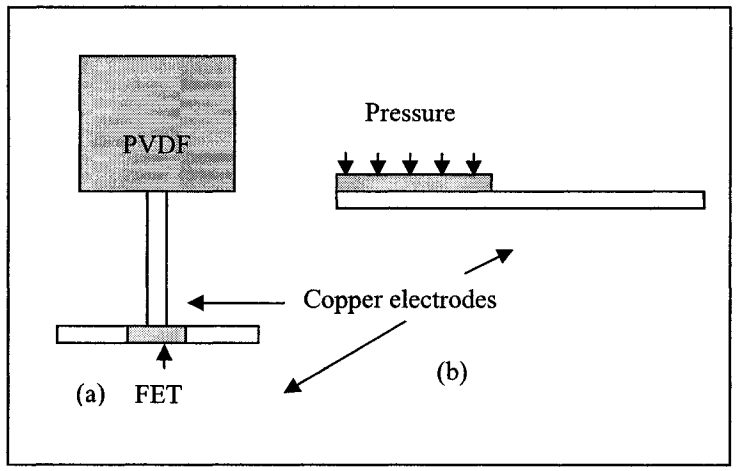


Figure 4.16 Layout for PVDF pressure sensor switch (a) top view (b) side view.

4.9.2 Fabrication and Characterization

The modeled layout for the QTC pressure sensor switch is fabricated using both low-cost and conventional processes. The difference in the layouts is the width of the transmission lines that constitute the switch layout. The difference in line widths is due to the difference in the layer stack-up for both cases and is explained earlier in Section 4.6. The QTC film will be attached on the periphery of the layout with dielectric or

conductive adhesive. Care should be taken not to short the interdigitated structures while attaching the film with the conductive adhesive. Figure 4.17 shows the fabricated sensor switch layout for the QTC film pressure sensor switch and Table 4.7 shows the switching characteristics. Simulations done on Coventor to model the PVDF material showed a maximum developed voltage of 13V when a force of approximately 6-8 N is applied [38]. This voltage is more than enough to turn on an off-the-shelf FET. Organic FETs with PEDOT/PSS or any other semiconducting polymer made by researchers [84-95] and used as channel material, requires 10 V to show significant switching behavior and can be employed along with the PVDF sensor to make the sensor switch. In this way, off-the-shelf components and the corresponding component assembly can be eliminated.

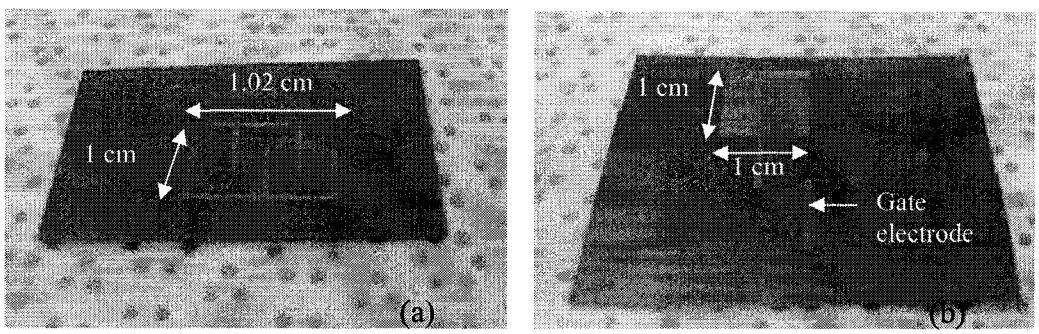


Figure 4.17(a) Switch layout for QTC pressure sensor (b) PVDF pressure sensor switch layout.

However, the radio frequency signal may get delayed due to the polymeric channel material of the FETs. This delay can be reduced by having a short channel rather than a long channel. Table 4.8 shows the switching characteristics of the PVDF sensor switch.

Table 4.7 Switching characteristics of QTC sensor switch.

Switch Condition	Type	S_{11}	R_{11}	X_{11}
Off	Simulated	0.98	0.64	-22.91
On	Simulated	0.3	105	-64.83

Table 4.8 Switching characteristics of PVDF sensor switch.

Switch	Condition	S_{11}	R_{11}	X_{11}
Off	Simulated	0.97	1.92	-63.98
On	Simulated	0.28	29.31	-9.22

4.10 Isolators and Circulators

RF isolators and circulators are passive devices that are used to control the propagation of RF signals. RF isolators are two-port units that allow signals to pass in one direction while providing high isolation for reflected energy in the reverse direction. Isolators are used to allow the delayed signal to flow to the common point or trace in the ID generation circuit and not vice versa. Figure 4.18 (a) shows the assembled isolator (CES 40925MECB000RAB, Murata, Inc) on the tag. These isolators are customized for a 925 MHz central frequency with sufficient band width. However, testing using a multi-meter showed a short among all the terminals of the isolator chip and the specified performance could not be established during the characterization. Isolators need careful assembly using a reflow oven. Manual soldering is not suggested by the vendor.

RF circulators have three or more ports and are used to control the direction of signal flow in a circuit. They allow the signal entering one port to pass to an adjacent port in either a clockwise or counter-clockwise direction, but not to any other port. Three port

or Y junction circulators are used in our experiments. In these devices, the signal flow is normally expressed as 1 to 2, 2 to 3 and 3 to 1. Figure 4.18 (b) shows assembled circulator (MAFRIN0497). These circulators are assembled using manual soldering and their performance could be verified.

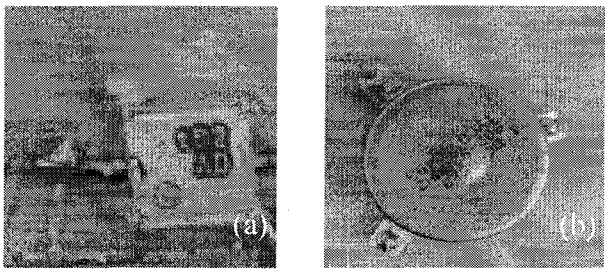


Figure 4.18 (a) assembled isolator (b) assembled circulator.

CHAPTER 5

LC-DELAY-LINE-BASED RFID SYSTEMS

5.1 Overview

The concept of LC-delay-line-based RFIDs and RFID based sensor tags, is explained in Chapter 2 along with a brief description of constituent devices and components. Different materials and processes that can be used for low cost fabrication are detailed in Chapter 3. Chapter 4 is devoted to the individual devices and components of the RFIDs and RFID-based sensors based on the LC delay line concept and transmission delay concept. This chapter describes integration of the devices and components that constitute LC-delay-line-based RFIDs and RFID-based sensors.

5.2 Integrated Layout Design

Figure 2.6 shows the schematic of the LC-delay-line-based RFID-based sensor tag. Individual devices and components that are modeled in Chapter 4 have been used for realizing the integrated tags. The layout of RFIDs/RFID-based sensor tag has been designed such that it minimizes the impedance mismatch between different components of the layout and cross over signals among the neighboring structures. A constant characteristic impedance of 50 Ω is maintained to avoid mismatches between different equipment and the tag and between almost all of the components in the tag itself. Stubs were used to tune the antennas and to connect them to the rest of the circuit with

microstrip transmission lines. The effects of antennas, sensor layout, and the ID circuit on one another have been studied using S-parameters and Z-parameters. As explained earlier, the layout design is based on the microstrip concept. Since diodes could not be fabricated for RF frequencies, off-the-shelf components are used. The mounting layout of these lumped components has been obtained from the data sheets and implemented into the tag layout. Wherever possible, models of the lumped components or equivalent circuits have been substituted in the layout simulations to emulate the real tag. The time delay effects of the interconnects are kept in mind while designing the layout. Table 5.1 shows typical values of the time delay, and the inductive and capacitive effects associated with transmission lines of different characteristic impedances.

Table 5.1 Time delay and L and C values corresponding to the characteristic impedance.

Z_0= Sqrt (L_0/C_0) (Ω)	Time Delay (nS/inch)	L_0 (in nH/inch)	C_0 (in pF/inch)
30	0.13	3.88	4.31
50	0.13	6.47	2.58
100	0.13	12.92	1.29

5.2.1 Impedance Matching

Impedance matching plays an important role in power consumption, noise, cross over signal effects and thermal effects in a tag. The S-parameters are very useful in determining matched components and their performance. The design aspects for matching different components of the tag have been explained below. A reflection coefficient of -10 dB is kept as a tolerance value for the ID circuit and antennas while a trade-off value of -5.2 dB is obtained for the sensor switch.

There are four different components that constitute a typical LC-delay-line-based RFID-based sensor. Impedance matching techniques need to be applied to address the unique nature of the layout. The receiving antenna is the source of the RF signal on board and its input impedance has been tuned to 50 Ω. Similarly the transmitting antenna's impedance is also tuned for 50 Ω. The input and output of the ID circuit are matched with a 50 Ωload and to transmission lines with 50 Ω characteristic impedance. This modular approach of impedance matching helped in matching every component of the tag to 50 Ω and then adding them together. The impedance matching of the individual components has been explained below.

5.2.1.1 ID generation circuit

The ID generation circuit layout contains three types of components. They are (1) off-the-shelf components such as, diodes, (2) capacitor and inductor equivalents of transmission lines and (3) transmission lines connecting other components such as, antennas. Capacitors and inductor equivalents are considered as lumped components and are connected to each other with the shortest possible interconnect lengths, thus eliminating the electrically long line effects of electromagnetic radiation. An electrically long line is one with a length equals to λ/4 or more where λ is given by

$$\lambda = \frac{V}{f} \tag{5.1}$$

where V is the velocity of the wave in the medium and f is the frequency of the circuit. The parasitic capacitance values of interconnects are a few femto farads and are considered during the capacitor design such that the equivalent capacitance is equal to the value required by the circuit level lumped component simulation. The reflection coefficient S_{11}, which is of one of the most important parameters, has been given with a

tolerance of -10 dB for the ID generation circuit. To achieve this value for the circuit, the line widths of different components should almost be equal if possible. The designed inductor has a line width approximately of 100 μm and a corresponding characteristic impedance of 102 Ω while the capacitor has a line width of 1.67 mm and of characteristic impedance approximately 16 Ω. Connecting them directly to one another would cause a large mismatch in their characteristic impedances. Because changing the inductor's width and, therefore, the characteristic impedance is a tedious job, the width of the capacitor has been decreased and compensating it with an increase in the length to keep the reactance the same at approximately 220 Ω. Furthermore, inductors and capacitors are interconnected with a line width that is mean value of the inductor and capacitor's line widths to minimize the mismatch. Because the interconnects are electrically small compared to the wavelength of the working frequency, the characteristic impedance of the intermediate interconnects need not be 50 Ω (Figure 5.1).

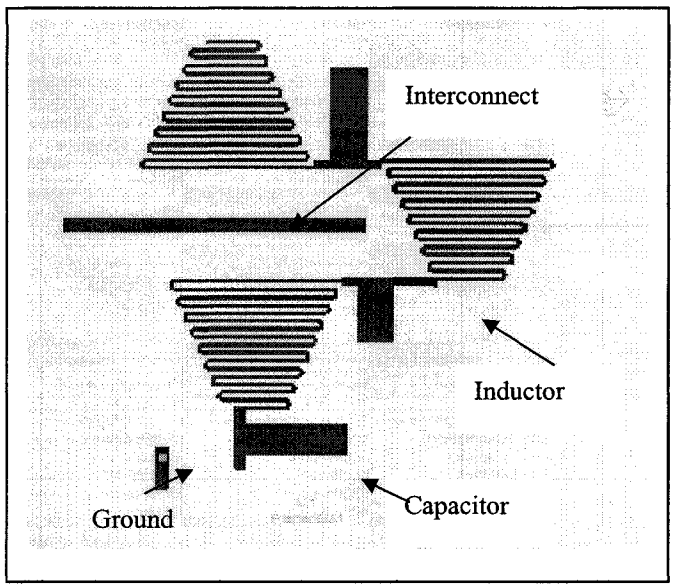


Figure 5.1 Modified layout of ID generation circuit.

From the point of design considerations the ID circuit has been designed with three LC delay lines with capacitor and inductor values adjusted to 220.1 Ω and 540.23 Ω, that is 0.791 pF and 0.094 μH, respectively. The design constitutes all the diodes connecting at the same point on the interconnect so that any time delay effects due to any interconnect variation lengths is eliminated. The output signals obtained after successive delay lines are shown in Figure 5.2 along with the input signal.

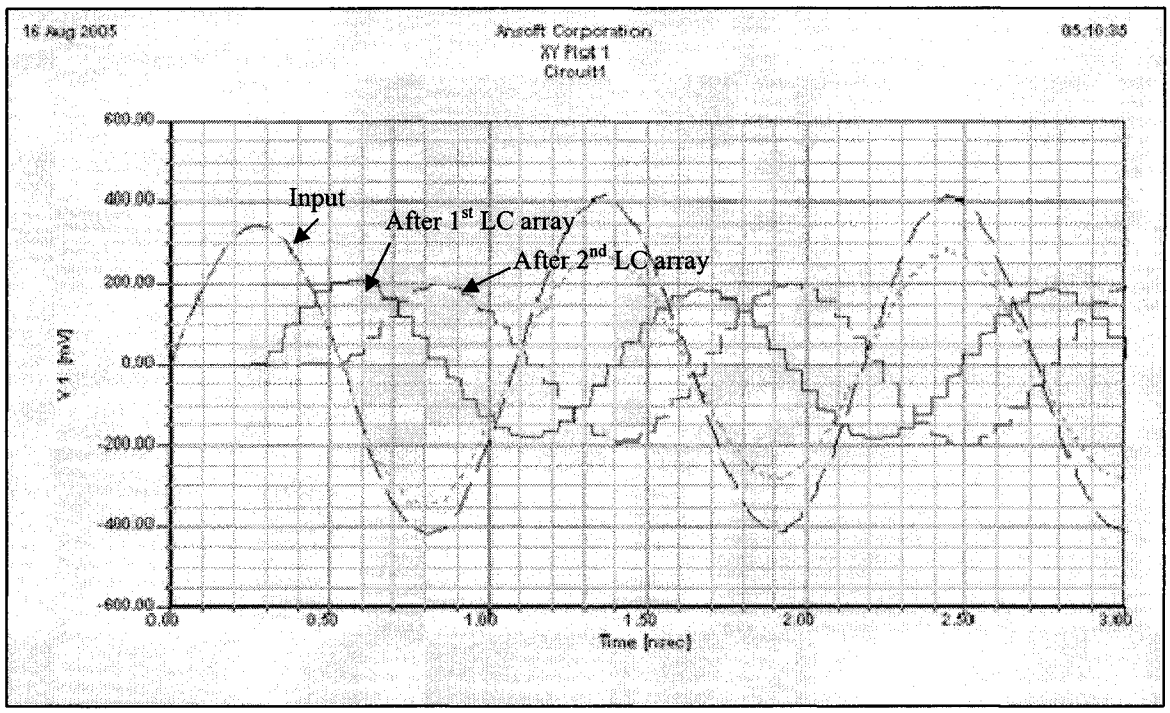


Figure 5.2 Input and output signals after 1st and 2nd delay lines of the ID circuit.

Reflection coefficients of -10.56 dB and -11.87 dB are obtained after the 1st and 2nd delay lines, which are below the tolerance value of -10 dB. Since the interconnects and the components themselves are designed to be electrically small, the electromagnetic effects of the tag radiations on these components, and thus on the ID circuit, are made negligible.

5.2.1.2 Antenna stub tuning

The 'Estimator' tool in the Ansoft Designer is used to calculate the stub location and the length. Meander and Hilbert antenna designs are chosen from the four available designs based on the analysis explained in Section 4.8. The estimator gives the length and location of an open stub that needs to be connected to a load and the expected real impedance value at a distance from the load. The receiving and transmitting antennas are taken as source and load, respectively, in our case. But, open stubs are electrically long and might act as radiating antennas (Figure 5.3 (a)). Therefore, each open stub is simulated separately to determine out the reactance value and then replaced by a short circuited stub of equal reactance. A short circuited stub would reduce the length of the stub, and not radiate. The microstrip transmission line to which the stub and load are connected is convoluted to adjust the form factor (Figure 5.3(b)).

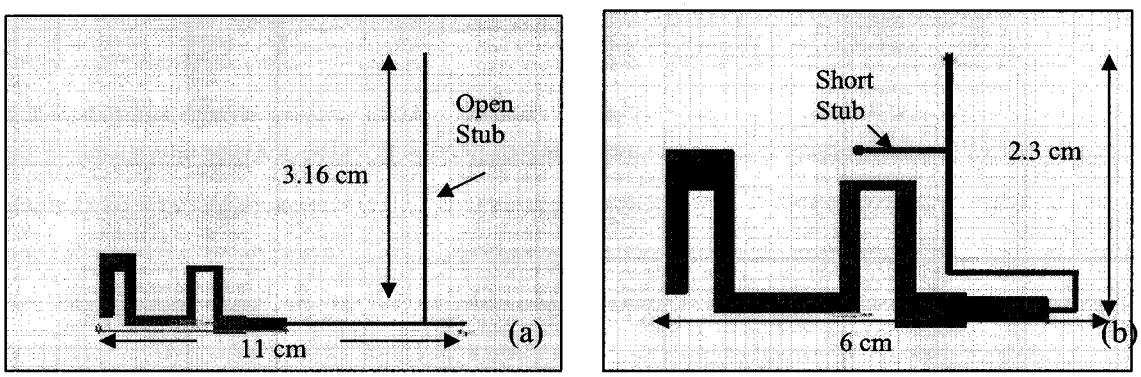


Figure 5.3 (a) An open stub connected to a Meander antenna (b) Impedance matched antenna after adjusting the form factor and with a shorted stub.

Table 5.2 Simulated stub matching parameters for Meander and Hilbert antenna designs.

Sl. No	Antenna	Z_{11}	Stub	Initial /final $\|S_{11}\|$	Location	Length
1.	Meander	62.65-j160.85	Open	0.93/0.30	31.76mm	60.42mm
			Short	0.93/0.27	31.76mm	10.11mm
2.	Hilbert	04.05+j034.06	Open	0.89/0.30	73.30mm	57.56mm
			Short	0.89/0.21	73.30mm	07.69mm

The lengths of open and short circuited stubs used for tuning, their location from the antenna, and initial and final reflection coefficients before and after tuning, are given in Table 5.2. The impedance matched ID circuit along with tuned antennas is shown in Figure 5.4.

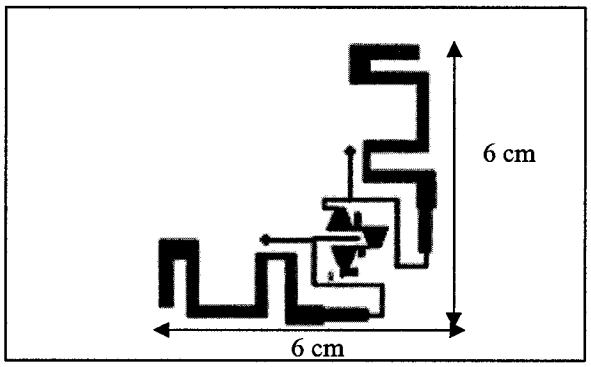


Figure 5.4 RFID tag with impedance matched ID circuit and tuned antennas.

5.2.1.3 Interconnect design

Interconnects play an important role in the tag layout design. 50 Ω characteristic impedance transmission lines have been designed to connect the different components and devices of the tag. A design rule that states that adjacent interconnects should be separated by at least three line widths, is maintained through out the design. To observe

the effect of adjacent structures, interconnects are simulated on board with other components of the tag (Figure 5.5 (a)) and as individual component (Figure 5.5 (b)). Considerable effects of adjacent conductors on the S and Z-parameters are observed.

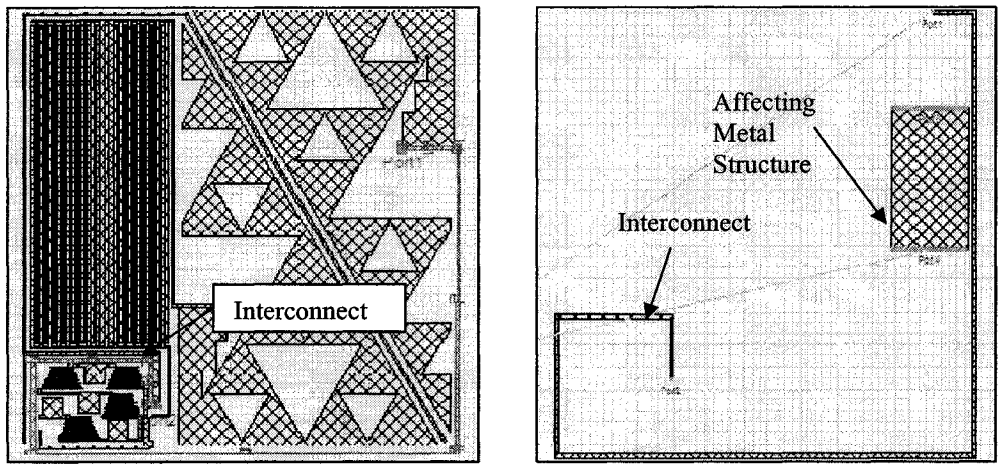


Figure 5.5 Schematic showing (a) interconnect under consideration (b) set up to measure the proximity effects of a capacitor near by an inductor.

5.2.2 Cross Talk Issues

The presence of components in the close proximity may cause crossover of signals known as "cross talk." Cross talk in the physical layout assumes significance at higher frequencies and can have varying impact on the output of the system. Practical knowledge prescribes a minimum distance of three line widths between adjacent interconnects, which is adhered to the layout design. Simulations of on-board interconnects show that their S-parameters did not change in value up to two decimal places after the decimal when another interconnect is placed in its vicinity that is less than a separation of two line widths. However, a considerable change in the reflection coefficients S_{11} and S_{22} is observed when a capacitive or inductive trace, with one of the ends open, was kept near the interconnect at a distance of less than three line widths.

Therefore, a design rule of a three line width minimum distance of separation between adjacent transmission lines, and near the ID generation circuit has been implemented in the layout model.

Simple simulation runs keeping both transmitting and receiving antennas on the tag area and simulating one of them gave an insight into the change in the radiation pattern. Meander antennas are more directional and their radiation pattern does not change much in the presence of a receiving antenna or other components of the tag (Figure 5.6(a)). This is not the same when Meander antennas are replaced by Fractal antennas (Figure 5.6(b)).

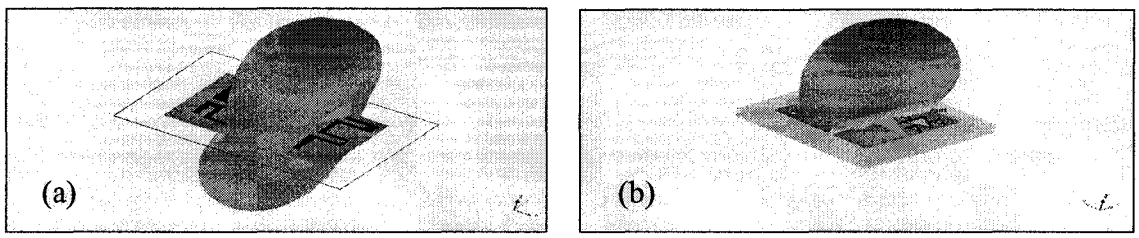


Figure 5.6 (a) RFID tag with Meander antennas (b) tags with Fractal antennas. (Note: the lighter colors correspond to lower electric field intensity and dark color correspond the high electric field intensity and the dimensions are normalized).

The radiation patterns shown in Figure 5.6 are not to scale. However, they give an idea of the antenna behavior on the tag. The ground plane at the bottom plays an important role in defining the radiation pattern. Both antennas showed a donut shaped pattern encircling the tag in the absence of a ground thus implying Omni-directionality. It is seen that when we decrease the conductor thickness below the minimum skin depth of the 915 MHz signal, the gain of the antenna decreases and maximum electric field strength in the z direction, Ez, is observed to be 22.2 μV/m for the antenna constructed using low-cost technology and 29.5 μV/m for the antenna with conventional technology.

5.3 Fabrication of LC Delay Line Based Tags

The feasibility of fabricating individual devices and components of the LC-delay-line-based RFIDs and RFID based sensors has been discussed in Chapter 3. Complete tags have been fabricated using both the proposed process flow (Section 3.3) and conventional silicon-based fabrication processes (Section 3.5). The implementation of each set of fabrication processes for the realization of LC-delay-line-based tags has been explained below.

5.3.1 Fabrication Using Low-cost Processes

As explained in Section 4.3, inductors can not be fabricated using low-cost processes without a high resolution printer for patterning the layout on the substrate. Therefore, working tags that constitute inductors can not be fabricated either. However , tags have been fabricated using low-cost technology to observe the feasibility of fabrication. Some modifications are done to the originally proposed processes. The Kapton 500VN substrate is mechanically roughened, and sonicated in isopropyl alcohol for 20 minutes. Then the substrate is cleaned with isopropyl alcohol and acetone. After drying in air and preheating, the substrate is loaded into the laser printer and the designed layout is printed from a pdf softcopy. Holes are manually drilled at the required grounding points on the layout using a syringe needle for the plate-through-hole process. The patterns are cleaned with air and cut into individual samples. These samples are kept in the activation solution for 4 minutes and acceleration solution for four more minutes to precondition the samples for electroless copper deposition. Preconditioned samples are cleaned with water and dried in air before immersing them in the ready-to-use Cuprothick 84 electroless copper bath which is maintained at a temperature of 32-35^{0}C and agitated

with an N_2 gas bubbler. One point of significance was the relative rate of electroless copper deposition on a tag containing components of different form factors. Blistering was observed on the components with large form factors while uniform deposition on components with small form factors was barely complete. This effect is particularly visible with the HF tag shown in 3.12 (a) and (b). This problem is not observed for 915MHz UHF tags where the relative difference in the form factors of the components is not large. Samples are removed from the bath just before the start of blistering. As explained earlier blistering can be avoided by improving the adhesion between the copper molecules and the substrate, by having continuous mechanical agitation of the substrate in the bath, and by adjusting the temperature and composition of the bath. By avoiding the blistering for a sufficient length of time copper of above 1um thickness can be achieved, which would solve the discontinuity problem in the inductors. After removal from the bath, samples are cleaned with water and dried in air.

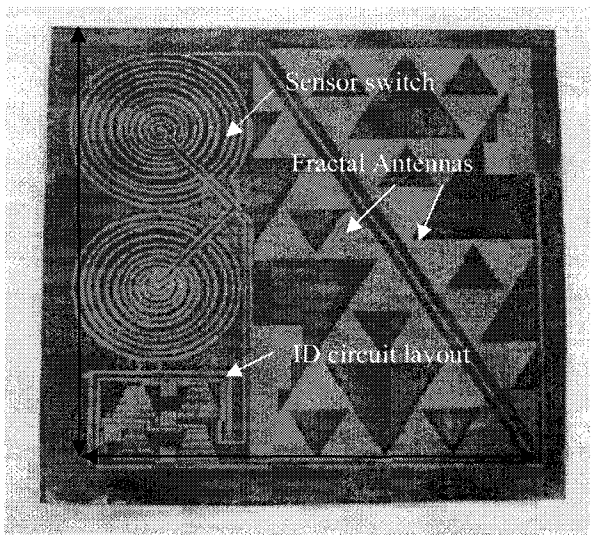


Figure 5.7 UHF Tag layouts fabricated using proposed low-cost technology

Off-the-shelf components such as, diodes are attached to the tag using conductive epoxy. This concludes the fabrication of RFID tags. These processes can be employed with slight modifications for the mass production of the tags. Figure 5.7 shows tag layout fabricated using low-cost fabrication processes.

5.3.2 Fabrication Using Conventional Processes

Figure 5.8 shows the LC-delay-line-based RFID-based sensor fabricated using the silicon-based fabrication processes explained in Section 3.6. After realizing the tag layout on the substrate, diodes and resistors are attached and a QTC sensor film is assembled using non-conductive glue.

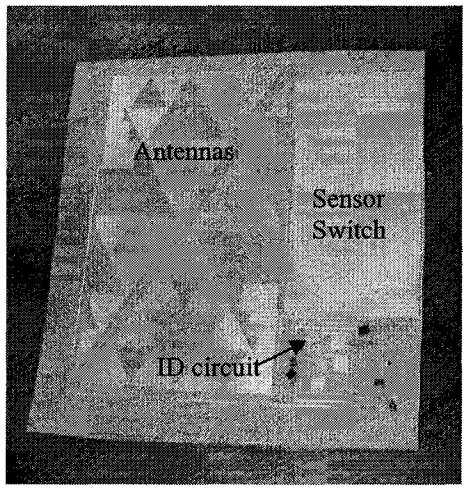


Figure 5.8 Tag fabricated silicon-based fabrication processes and assembling.

5.3.3 Packaging

Dymax 9008 series epoxy can be used as an encapsulant for the lumped components assembled on the tag. The same material can be coated on the tag and UV cured to package the tag. This material is flexible enough to allow the sensor film to perform normally. A window is needed, however, for the polyaniline based sensor tag

which may require an additional patterning step. This epoxy does not affect the flexibility of the tag in any way.

5.4 Characterization of LC-delay-line-based Tags

The method by which different components have been tested onboard of the tag to find out their performance has been outlined below. Experiments done with different parts of the tag that constitute these parts have been explained later. Finally, tag as a whole is tested and the results are presented.

5.4.1 On-board ID Circuit Tests

Figure 5.9 shows a test set up to measure the time delay in the LC arrays of the ID generation circuit. Off-the-shelf diode performance could not be established in our experiments, as mentioned in Section 4.7. Moreover, power consumed by the diodes is very high. Diode rectification is needed for the verification of the delay and the ID code generation. Experiments done to verify the ID generation circuit using amplitude modulated sinusoidal wave are explained in a prior thesis work, as mentioned in Section 1.6.

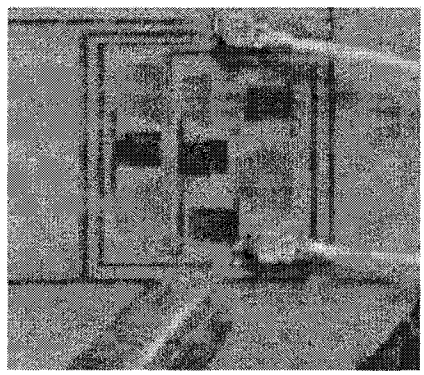


Figure 5.9 Fabricated LC-delay-line-based ID generation circuit with four LC arrays in series under test.

However, the time delay has been verified by feeding the OOK modulated signal as explained in Chapter 2. A modulated signal allows one to clearly observe the time delay compared to an unmodulated sinusoidal wave. Therefore, a pulse modulated OOK signal with a 915 MHz center frequency and an 8 ns envelop width has been applied as the input signal through a 3 GHz passive probe and the output is connected to an oscilloscope with equal length connectors. Figure 5.10 shows the observed results. The signal is observed after the first, third and fourth LC arrays each of which is capable of producing a delay of 0.275 ns. The produced delay might not be sufficient to produce the ID code in OOK communication scheme. However, time delays of tens of nanoseconds can be produced using planar inductor and capacitor arrays of large size, as explained in Chapter 7.

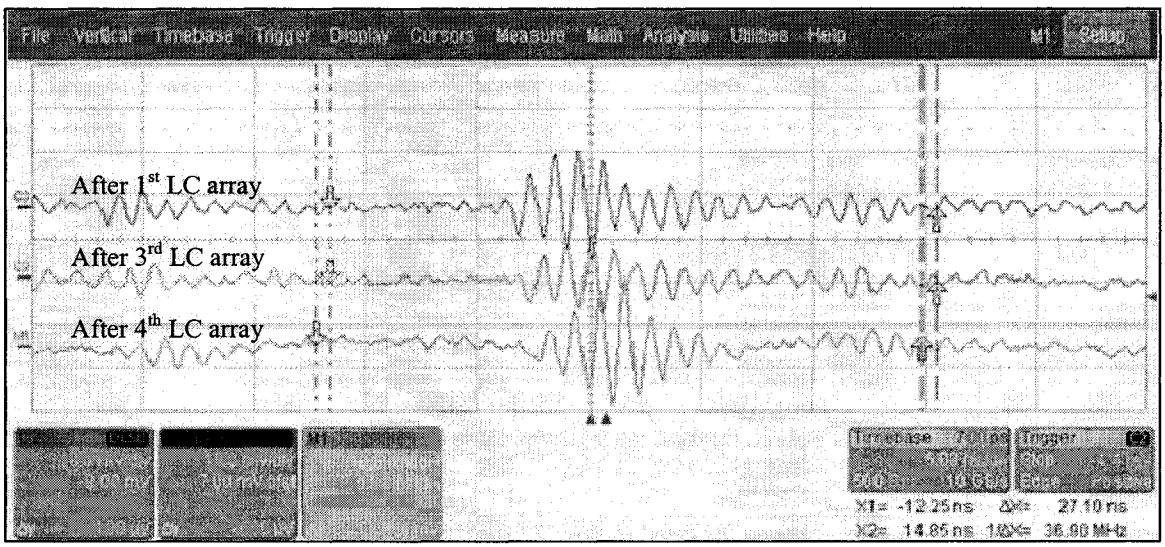


Figure 5.10 Oscilloscope display showing OOK modulated signal after first, third and forth LC array of the ID generation circuit (x axis = time (5 ns/div); y axis = voltage (10 mV/div)).

5.4.2 Antenna Tuning

Tuned and untuned Meander and Hilbert planar antennas fabricated using low-cost fabrication techniques (Figure 5.11) have been tested for their behavior using the test set up shown in Figure 5.12. Each fabricated antenna is tested in receiving mode with a Yagi transmitting antenna on the other side connected to a signal generator.

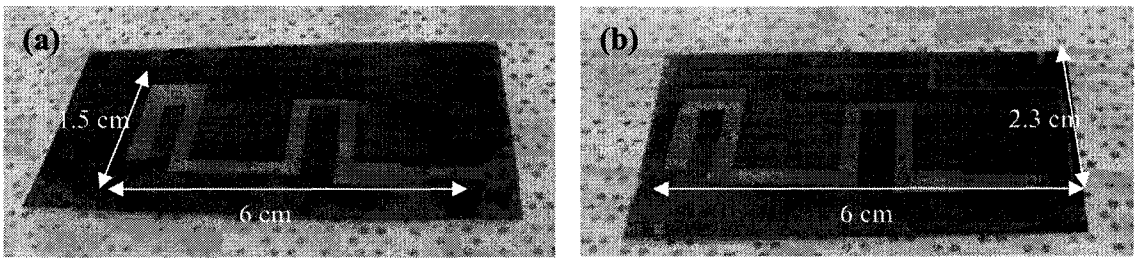


Figure 5.11 Fabricated Meander antennas (a) untuned (b) tuned.

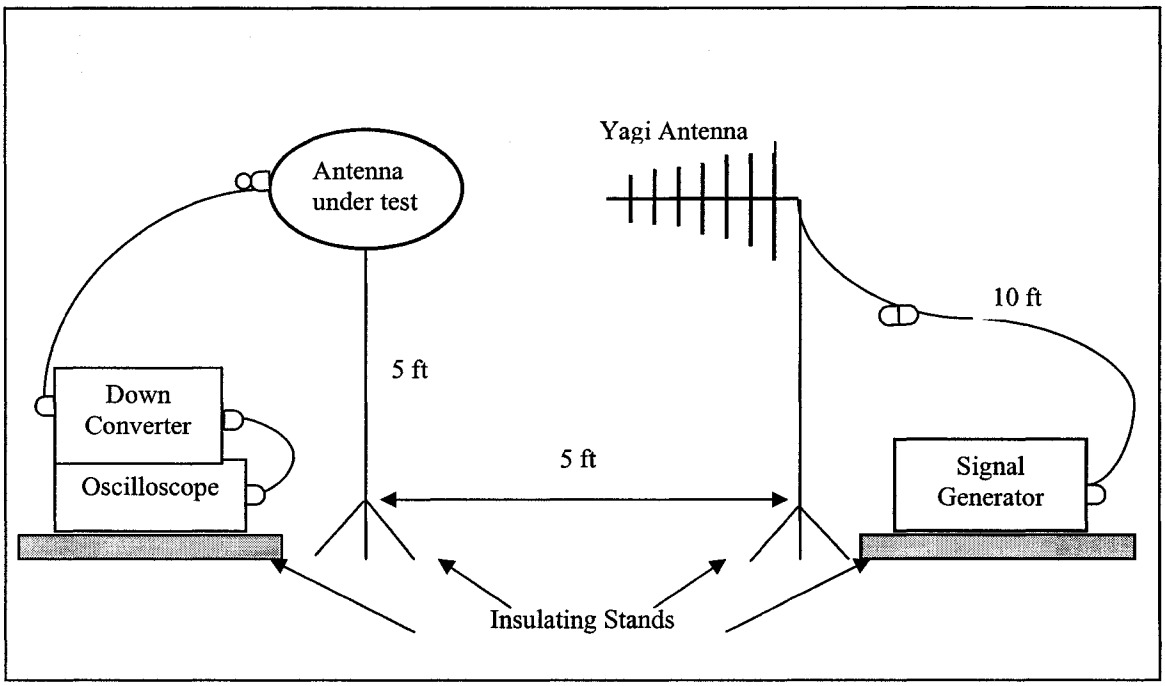


Figure 5.12 Dimensions and instrumentation of measurement and test setup.

The distances between the antennas and the height of each antenna from the ground obey the equations and regulations described in Section 2.3.4. The external transmitter consists of signal generator and the Yagi antenna. Our signal generator can produce a maximum of 20 mw into 50 Ω input impedance. The Yagi antenna has a power gain of 8.5 dBI. Therefore, the EIRP (Equation 2.6) of our system is 170 mw which is less than the EIRP of 1W allowed by the FCC. The power available at typical distances, for some of the tag's antennas, is given in Figure 5.13.

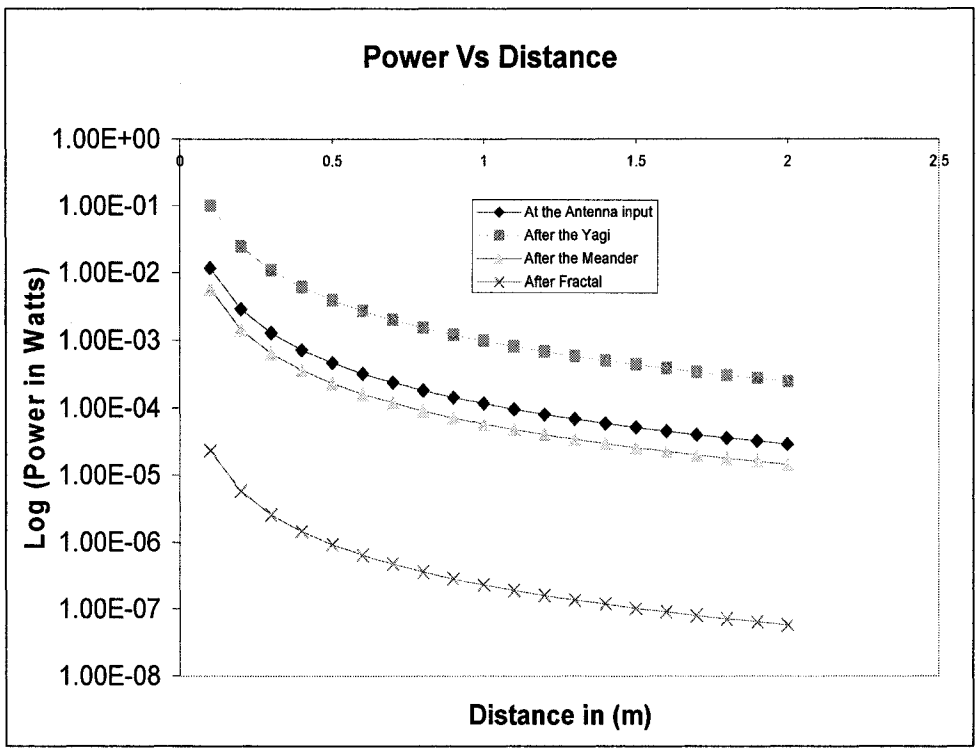


Figure 5.13 Power vs distance parameters for the experimental set up.

Any signal that is less than 2 mV in the oscilloscope has been interpreted as an unwanted signal because of the noise present in the ambient showing the same amplitude. All the antenna configurations performed satisfactorily in both transmitting and receiving

modes. Tuned antennas showed better performance over their untuned counterparts (Figure 5.14).

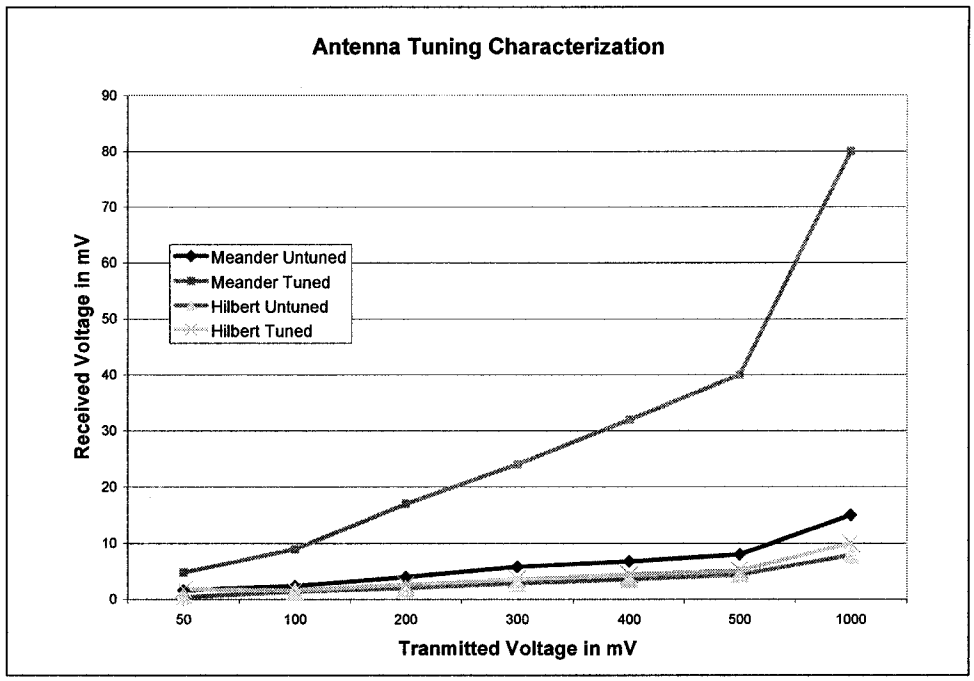


Figure 5.14 Effect of tuning on Meander and Hilbert antennas.

5.4.3 ID Circuit Along with Transmitting/ Receiving Antenna

Fractal antennas were used as the tag's transmitting antenna and external receiving antenna with a one meter distance of separation. The signal could be distinguished from the noise in the oscilloscope which is connected to the Fractal receiving antenna through the down converter. The down-converter is used with 0 dB attenuation, RF gain and zero automatic gain control settings. Fractal antennas are also used in this set up to observe the signal strength Vs distance. A maximum separation of two meter could be achieved with a distinguishable signal observed with the oscilloscope.

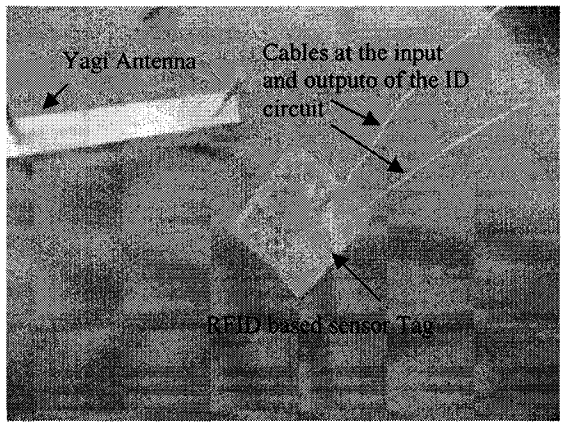


Figure 5.15 LC-delay-line-based RFID sensor tag receiving signal from the Yagi antenna wirelessly.

After the delay is observed in the LC array series of the ID generation circuit, the circuit connected to the receiving antenna of the tag is observed for the time delay. An external Yagi antenna is used to transmit the signal and the tag with Fractal receiving antenna (Figure 5.15) is set to receive the signal. Two w.fl cables are connected to the input and output of the LC series array of the ID generation circuit. An OOK modulated input similar to that mentioned in Section 2.3.5 is provided to the Yagi antenna. Figure 5.16 shows the observed delay of 1.1 ns in the 1 GHz oscilloscope, as expected.

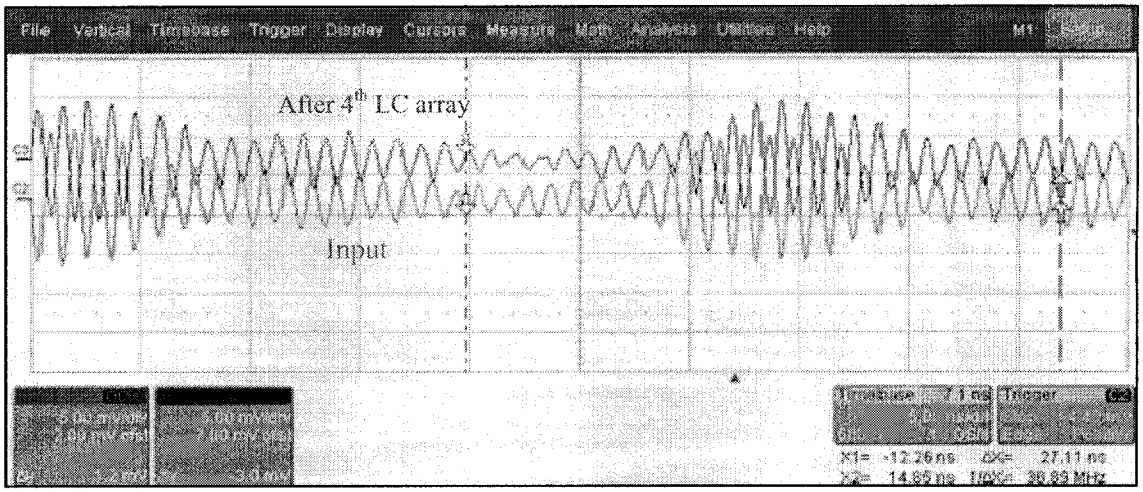


Figure 5.16 Signal at the input and output of four LC array series of the ID generation circuit showing the time delay in the oscilloscope (x axis = 5 ns/div; y axis = 5 mV/div).

5.4.4 Onboard Sensor Switch Tests

The Fractal antenna is used as the transmitting tag antenna along with the sensor switch connected in series with it. A voltage signal of -29.5 dBm (7.5mV) is applied and the output signal is observed in the oscilloscope connected to the down-converter equipped with a Yagi antenna. The following output levels are observed at a distance of 1 m (Table 5.3).

Table 5.3 Effect of different types of switch closing on the signal.

Type of Closing	Signal in the oscilloscope
Shorting with conductor	1mV
QTC Pellet	0.9mV
QTC film	0.4 mV

The above values confirm the working of the QTC film and pellet as sensors and show that the performance of the sensor switch layout is satisfactory. Experiments are also done to confirm the working of the PVDF switch layout and are discussed in prior thesis work [38], and as also explained in Section 1.6.

CHAPTER 6

TRANSMISSION DELAY LINE BASED RFID SYSTEMS

6.1 Overview

The concept behind transmission delay line based RFID/RFID-based sensors was explained in Chapter 2. Similar to a power transmission line, a microstrip transmission line contains inherent time delay due to the presence of distributed inductances and capacitances present along its length. Therefore, a microstrip transmission line can be used as a delay element for the ID generation circuit, as explained in Section 6.2, instead of the transmission equivalent structures of the inductors and capacitors, as explained in Chapter 5. This chapter describes the simulation, fabrication and characterization of the transmission delay line based RFIDs and RFID-based sensors. These tags incorporate rugged and easy to fabricate components are compared to those based on delay lines made of planar inductor and capacitor structures.

6.2 ID Generating Circuit Based On Transmission Delay Line

A simple and efficient ID generation circuit, based on the inherent delays of microstrip transmission lines has been designed, fabricated and characterized for realizing chipless RFIDs and RFID-based sensor tags. Results show that there are many advantages to the new ID generation circuit, one of which is the greater adaptability

to the proposed set of low-cost fabrication processes as compared to LC delay line based RFIDs and RFID based sensors. These advantages and limitations are discussed in the later sections of this chapter.

6.2.1 Theoretical Considerations

The distributed capacitance and inductance of a microstrip transmission line, that cause a time delay, depends on the width and thickness of the signal layer and the dielectric material of the microstrip. An approximate time delay of 0.13 ns per inch is present in the microstrip line based on the material stack up structure explained in Section 4.2. Therefore, by careful design, this delay can be used to create an ID code at UHF and higher frequencies by superimposing signals tapped at different lengths of the transmission line. Figure 6.1 shows the schematic of the proposed ID generation circuit based on the transmission delay lines.

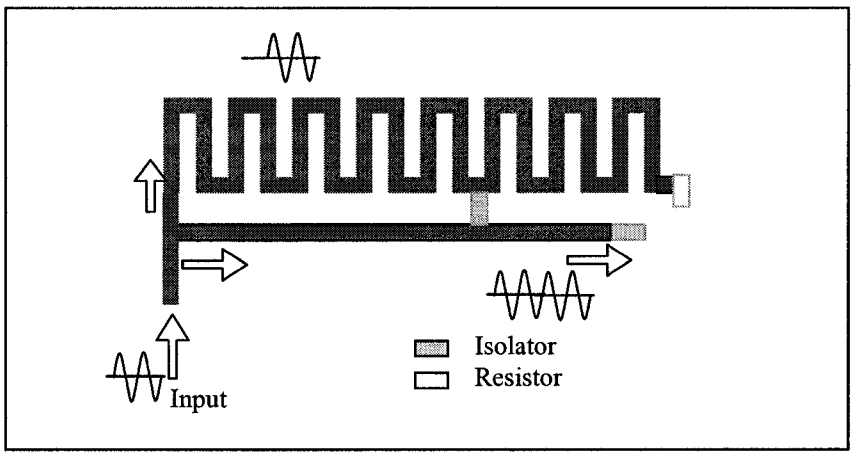


Figure 6.1 Schematic diagram of ID generation circuit.

An input signal, such as an OOK modulated signal, is fed into the ID generation circuit. The signal travels along two parallel paths as shown in Figure 6.1. One through a straight and relatively shorter branch and the other along a longer transmission line

meandered to reduce the form factor. The end of the meandered branch is terminated with a 50 Ω resistor. The signal delayed in the meandered transmission line is tapped via isolators on to the shorter branch according to the required binary code. The signal in the shorter trace and the tapped signal get superimposed on each other to produce the ID code.

6.2.2 Modeling and Simulations

Figure 6.2 shows the schematic diagram of the simulated ID generation circuit layout. A signal entering in port 1 travels in the two parallel branches as explained earlier. The meandered branch has a total length of 72 inches which corresponds to a time delay of 9.3 ns. As a general rule of thumb, adjacent lines of the layout are separated by a minimum gap equal to three line widths to avoid crosstalk. Isolators are then used to tap the signal from the meandered branch on to the straight branch. Ansoft Designer's EM level simulation is used to model the circuit

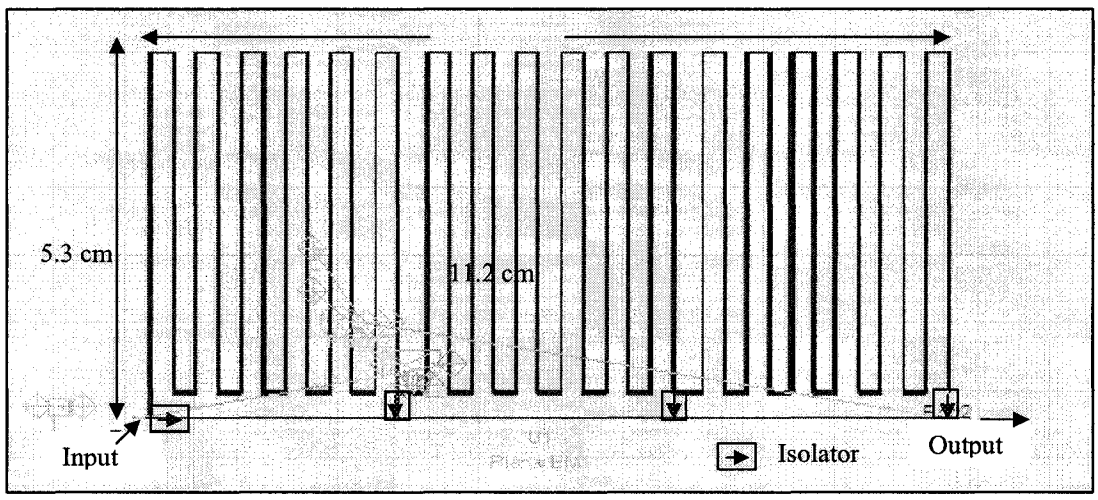


Figure 6.2 Schematic showing simulated 9.3 ns delay ID generation circuit.

Different types of input signals are fed into the ID generation circuit to analyze its response. Figure 6.3 shows the output response to typical waveforms such as, half wave sinusoidal, pulse signal, etc. Figure 6.3 (a) shows three different bit configurations generated for a half-wave rectified sinusoidal input at 915 MHz. Curve 1 corresponds to the code 1010, curve 2 to 0101 and curve 3 (not completely visible in the figure due to overlapping) to 1001. The limitations of using a half-wave rectified sinusoidal signal for communications are explained in Chapter 7.

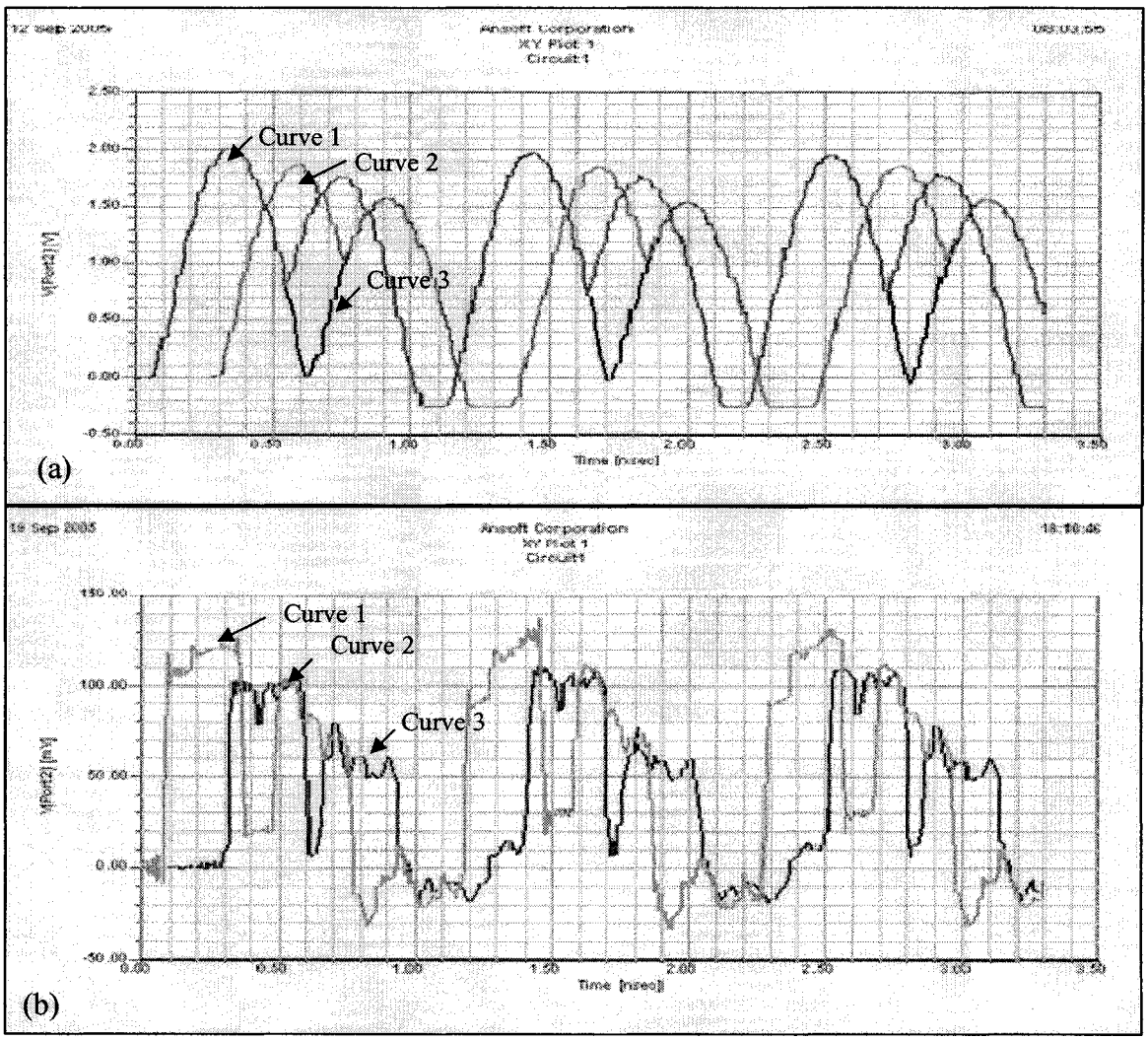


Figure 6.3 Different bit code generation by ID generation circuit response to (a) half wave rectified sinusoidal input (b) pulse input.

Figure 6.3 (b) shows the response of the ID generation circuit to an input pulse of 915 MHz pulse repetition frequency (PRF) and 25% duty cycle. The two different combinations of the four bit code generated correspond to 1010 and 0101 respectively. The effect of bit overlapping has been simulated and shown in Figure 6.3 (b) by taking a pulse width greater than T_d, the unit delay corresponding to the bit width. The bit overlap can be eliminated by carefully selecting the tapping points on the ID generation circuit. One can see that the voltage amplitude shown in this figure is in hundreds of millivolts and not in volts as shown in earlier simulations. This is due to the use of a 1 V voltage source at the input rather than a 100 mW power source. Figure 6.4 shows the input and output responses of the ID generation circuit for an OOK modulated input of 915 MHz center frequency using 31.3 MHz PRF, 0.25 duty cycle pulses.

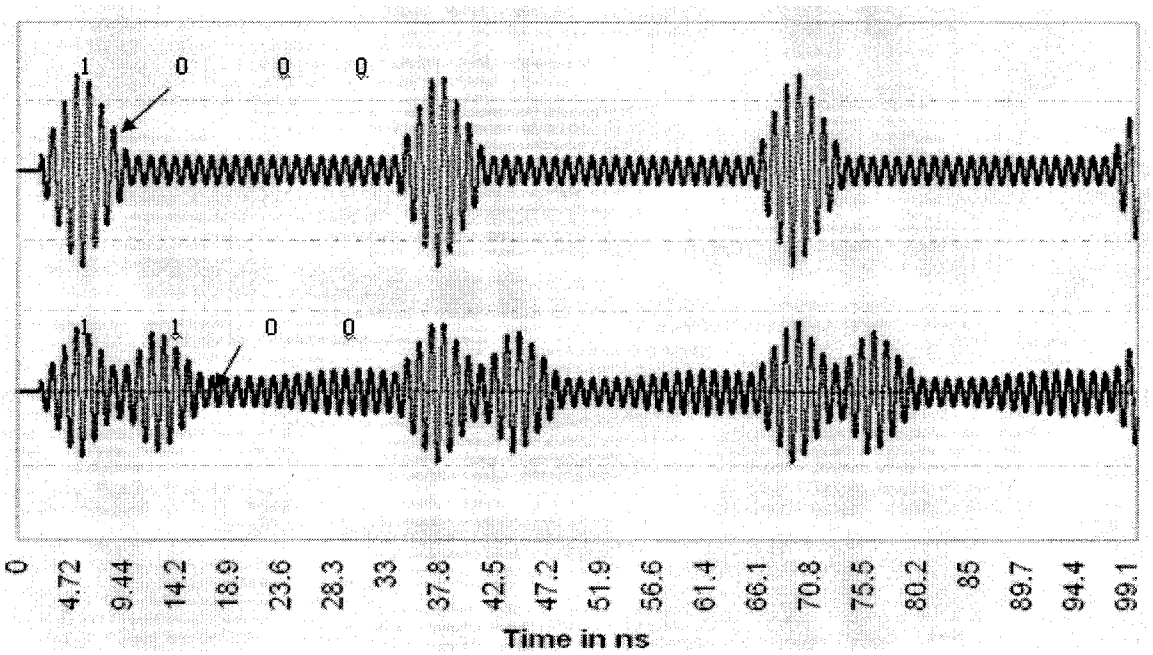


Figure 6.4 Different bit code generation by ID generation circuits for modulated digital input (x-axis = 4.72 ns/div; y-axis = 0.3V/div voltage).

The input signal is modified to emulate the practical conditions of the experimental set-up that are explained in the later sections. The generated output can be interpreted as a binary code 1100.

6.2.3 Fabrication and Characterization

Figure 6.5 (a) shows the layouts of a transmission delay line based ID generation circuits capable of producing 1 ns delay and fabricated using a low-cost fabrication processes. Figure 6.5 (b) shows the ID generation circuit capable of producing a maximum delay of 9.3 ns and made using conventional photolithography based fabrication processes.

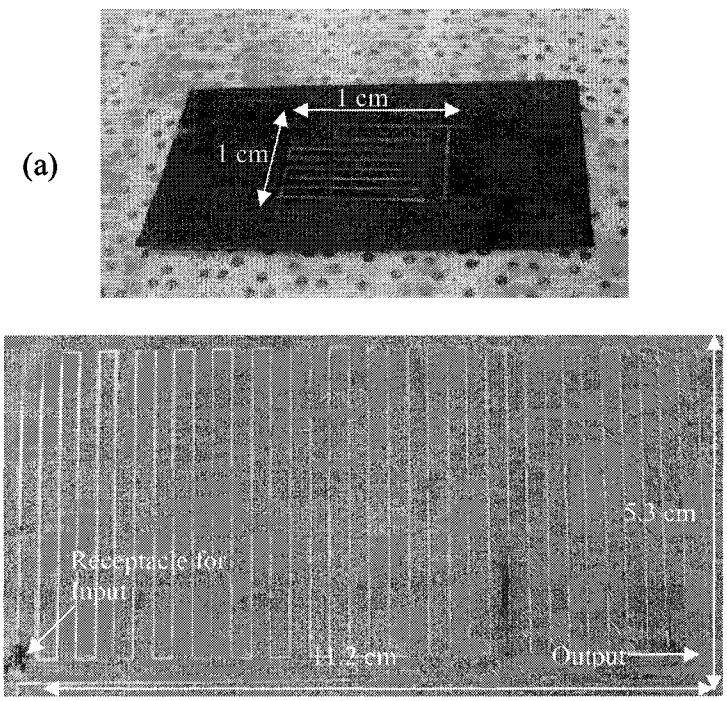


Figure 6.5 Transmission delay line based ID generation circuits fabricated using (a) proposed low-cost technology and (b) using conventional technology.

Since the layout contains 50 Ω characteristic impedance transmission lines that correspond to a line width of 408.65 μm, it can be easily printed using a commercial laser

jet printer of moderate resolution. This will also simplify the electroless copper deposition process because of the absence of structures of unequal form factors that require different plating times.

The delayed signal from the meandered branch is tapped using an isolator as described in Section 4. 10. Transmission line losses in the ID generation circuit based on low-cost fabrication techniques are high compared to the one fabricated using photolithography based processes. This is due to the thinner layer of copper obtained from electroless deposition which is less than the required value corresponding to the skin depth requirements at the 915 MHz frequency of operation. Simulations did not show the effect of copper thickness on the amplitude of the output waveform for the ID generation with 1 ns delay but showed a clear effect in the case of the ID generation circuits with 9.3 ns delay. The shown reduction in the signal could also be due to cross over effects in the long meandered transmission line branch.

The transmission delay line based ID generation circuit capable of producing 9.3 ns delay is characterized for its response to both pulse signal and OOK modulated input signals. An input pulse of 2 ns pulse width and 31.3 MHz PRF is fed from a pulse generator (Agilent 8133A) to the ID generation circuit capable of producing 9.3 ns delay, using W.FL cables and receptacles. Figure 6.6 (a) clearly shows delay of 9.3 ns in the meandered branch with respect to the pulse in the straight branch of the ID generation circuit. Figure 6.6 (b) shows the OOK modulated signals of 915 MHz center frequency and 4 ns envelops in the meandered and straight branches. All the responses are observed using a 1 GHz Lecroy digital oscilloscope capable of sampling at the rate of 10G samples per second.

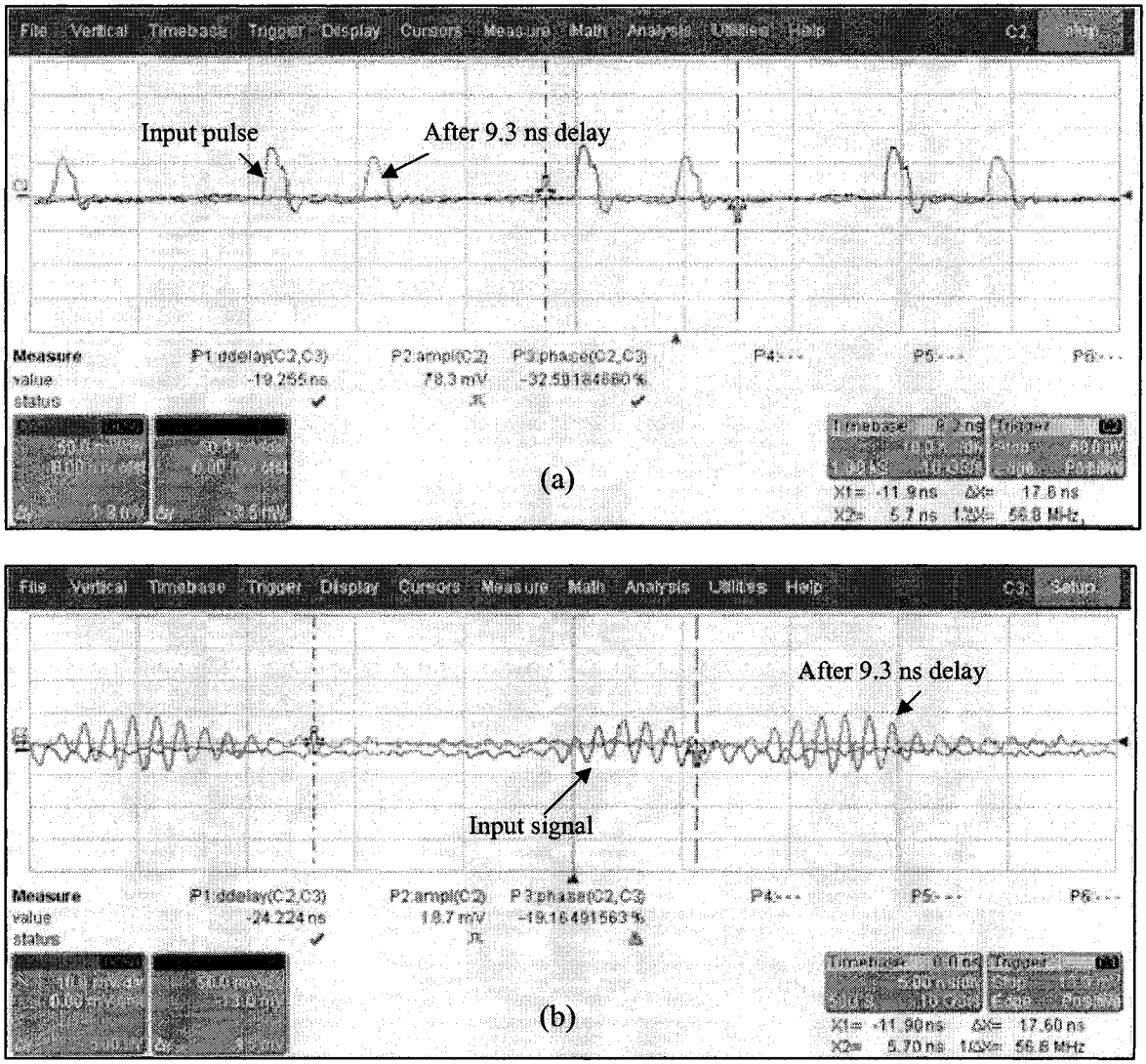


Figure 6.6 Delay observed in the 1GHz digital oscilloscope for (a) pulse input (b) OOK modulated signal of 915 MHz center frequency using 5 ns pulse, 31.3 MHz PRF.

Figure 6.7 shows different binary codes generated by the ID generation circuit shown in Figure 6.5 (b). Isolators obtained from the vendor could not be tested, as explained in Section 4.10. Therefore, a circulator is used to tap the signal from the meandered branch on to the straight branch of the circuit. In Figure 6.7 (a), a four bit code was generated using a OOK modulated signal with a 915 MHz center frequency generated using a signal generator and an RF switch controlled by a pulse width of 8 ns

and 31.3 MHz PRF. A six bit code was generated by decreasing the bit width and not changing the ID generation circuit. This confirms the feasibility of generating any number of bits and their combinations.

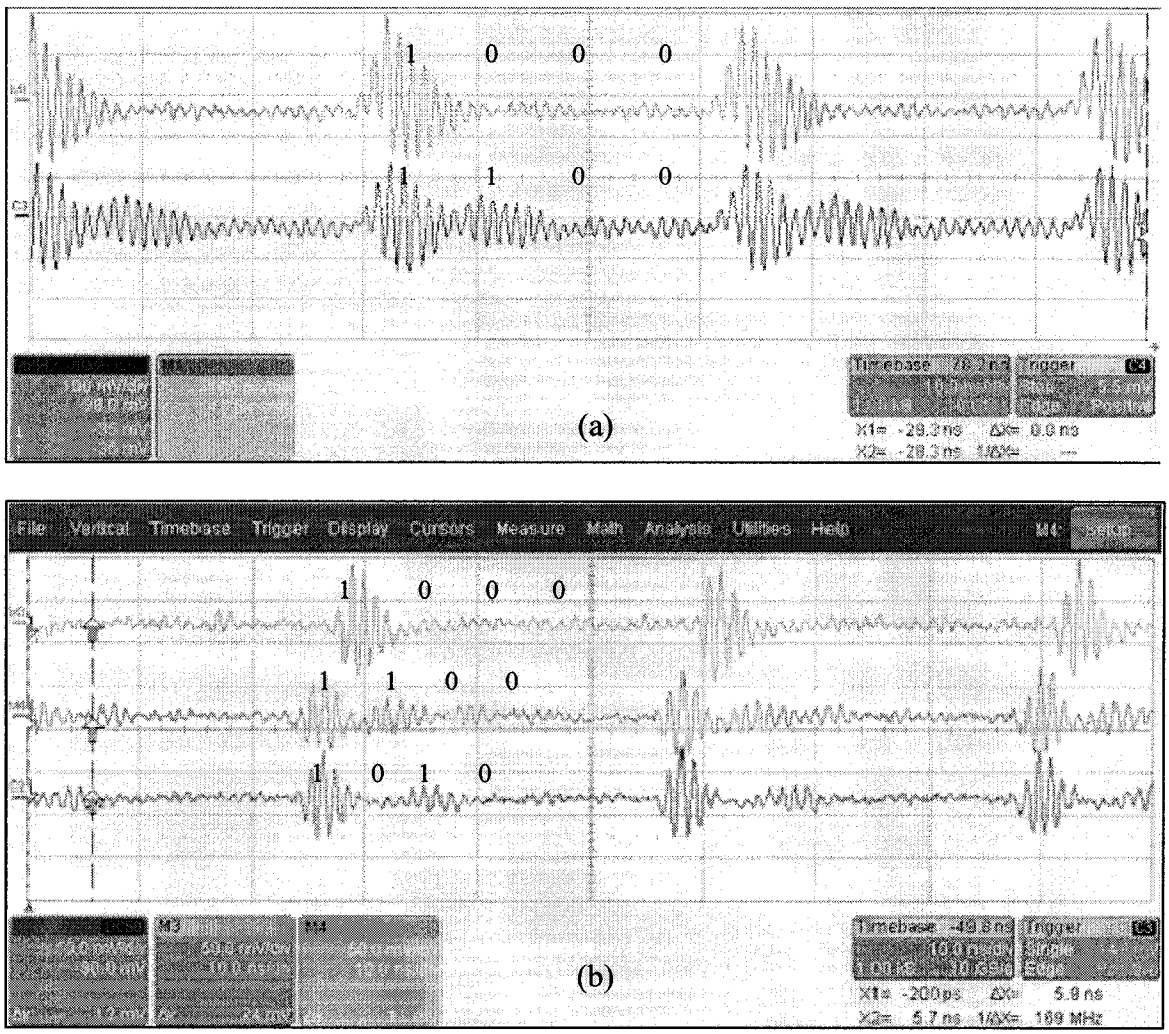


Figure 6.7 Output waveforms from the ID generation circuit (a) 4 Code generation (x axis = 10 ns/div, y axis= 100mV/div) with 8 ns bit length (b) Codes generated with 4 ns bit length (x axis = 10 ns/div, y axis = 50 mV/div).

6.2.4 Conclusions

It is clear from the above experiments that a distinct output code can be realized with input pulses as well as modulated digital signals. An ID generation circuit based on

transmission-line delay presents many advantages. The layout is rugged and the output is more repeatable as compared to an ID circuit with planar capacitors and inductors. Since the ID contains transmission lines of 50 Ω characteristic impedance it can be easily integrated with the rest of the tag which contains structures with the same impedance. The absence of planar devices of varying widths resulted in a very low coefficient of reflection. This circuit avoids using diodes, inductors, and capacitors which are required for LC-delay-line-based ID generation circuits. The numbers of resistors required for the circuit have also been reduced to only one resistor which may be required to terminate the delay branch of the ID generation circuit. This concept can be used to develop an ID generation circuit for any frequency so long as dimension and cross talk are with acceptable limits. By careful design and a larger number of tapping points, the same layout can be used to obtain a different number of bits without the need for redesign or re-fabrication. The circuit can be used to produce a large number of bits without significant loss at microwave frequencies, such as 2.45 GHz because the required delay for discrete output levels will be small. The duty cycle of the pulse can be adjusted to accommodate a large number of digits and be devoid of bit over lap because of sharp rise and fall times.

The ID generation circuit based on a transmission delay line can be used to generate dynamic code by incorporating sensor switches in series with isolators at the taps. In this way, bit 1 is generated corresponding to the 'ON' position of the switch. Isolators and circulators can be replaced by diodes and an extra antenna using unipolar signals for communications. This concept will be detailed in Chapter 7.

6.3 Component Integration of Transmission-delay-line-based Tags

The concept of a transmission-delay-line-based RFID system, and constituent tags that is RFIDs and RFID-based sensors has been explained in Chapter 2. The layout consists of a transmitting/receiving antenna, a circulator, an ID generation circuit and or a sensor switch. Antennas tuned to 50 Ω input impedance can be directly attached to the ID circuit and the required number of resistors used to terminate the Meandered branch of the ID generation circuit can be reduced to one or none. All interconnects, sensor switch layout and the ID generation circuit contains traces of 50 Ω impedance and thus reflections at the interfaces between the components are reduced. Modeling and simulations done for the integration, fabrication and characterization of transmission-delay-line-based RFIDs and RFID-based sensors are explained below.

6.3.1 Design and Simulation

Antenna tuning has been explained in Section 4.8. Different tuned antennas are connected to the ID generation circuit to make different RFID configurations. Similarly, tuned antennas are connected to the ID generation circuit in series with the sensor layout for realizing RFID-based sensors. Figure 6.8 shows one of the mask layouts prepared with transmission-delay-line-based RFIDs and RFID-based sensor tags, with Hilbert and Meander line antennas, 2.6 ns and 9.3 ns delay-ID generation circuits, and QTC, PVDF sensor switches. Masks have been printed using the equipment mentioned in Section 6.2. Other mask designed include masks for transmission-delay-line-based RFIDs and RFID-based sensors of Fractal, Spiral, and Triangular patch antenna configurations [36]. The layouts are designed with the required land patterns for the circulators and the isolators.

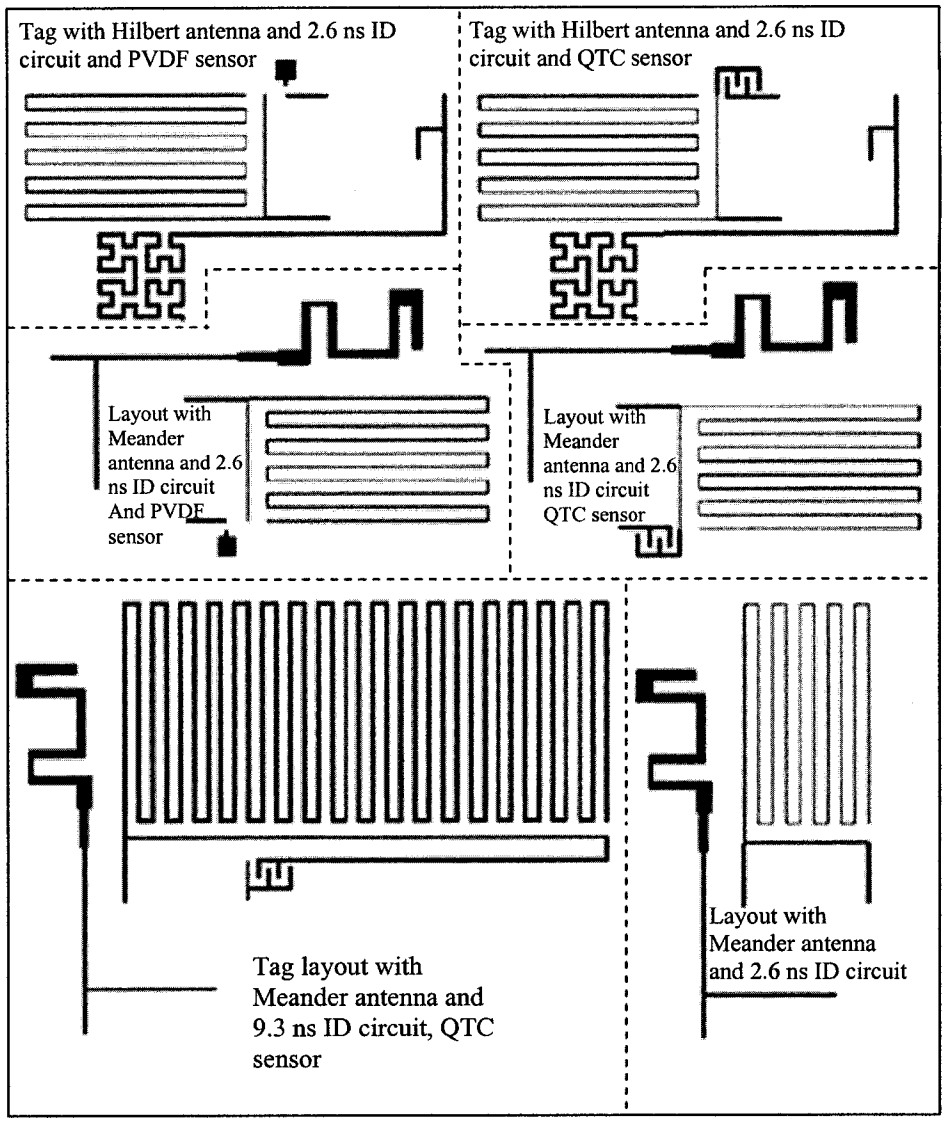


Figure 6.8 Mask layout with different RFID and RFID-based sensor configurations.

6.3.2 Fabrication

All the RFIDs and RFID-based sensor configurations are fabricated using conventional photolithography and other corresponding processes which are explained in Section 3.6. The UV lamp in the UV mask aligner could not be used for exposing the tag layouts because of the smaller circumference of the exposure area. Therefore, a conventional U.V lamp is used with a three minute exposure time to obtain a uniform

exposure. Circulators have been attached using manual soldering and silver epoxy is used for ground connections. Figure 6.9 shows the fabricated RFID-based sensor based on transmission-line delay with assembled on-board circulator.

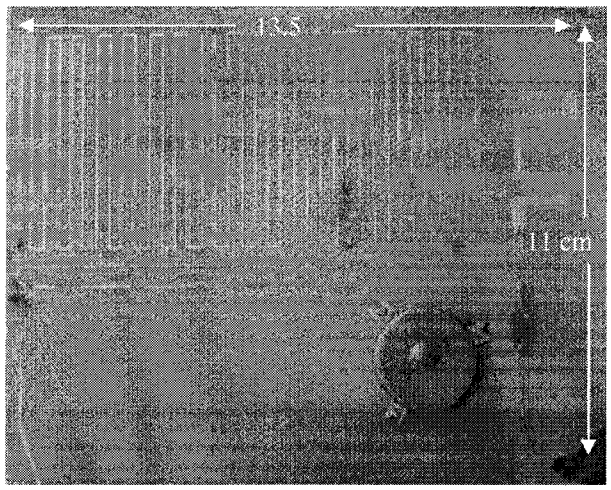


Figure 6.9 Fabricated RFID-based sensor with QTC sensor switch layout, 9.3 ns delay ID generation circuit and Meander transmitting/receiving antenna.

6.3.3 Characterization

As explained in Chapter 2, it was decided to use OOK for modulating the input signal of the transmission-delay-line-based RFID/RFID-based sensor. This type of modulation will be more compatible with respect to commercial standards and FCC regulations. To achieve such modulation, an RF switch is connected to the output of the signal generator and a D.C supply. The 'On/Off' of the switch is controlled by a pulse generated by a pulse generator. By changing the duty cycle and pulse repetition frequency of the pulse used for OOK, communication between the tag and reader can be designed such that there is a single signal present in the air for either input or output at a given time. This will eliminate directionality requirements for characterization and ease the testing procedure of the output signal since both input and output can be seen as

discrete signals as viewed at the oscilloscope. Figure 6.10 shows the simulated output at the receiver using a modulated signal of 228.75MHz PRF, and 10% duty cycle. The input signal (Curve 1) is clearly distinguished from the output codes (curve 2). This is achieved by delaying the input signal by one pulse width inside the RFID/RFID-based sensor and then using the remainder of the available delay in the ID generation circuit for ID code generation.

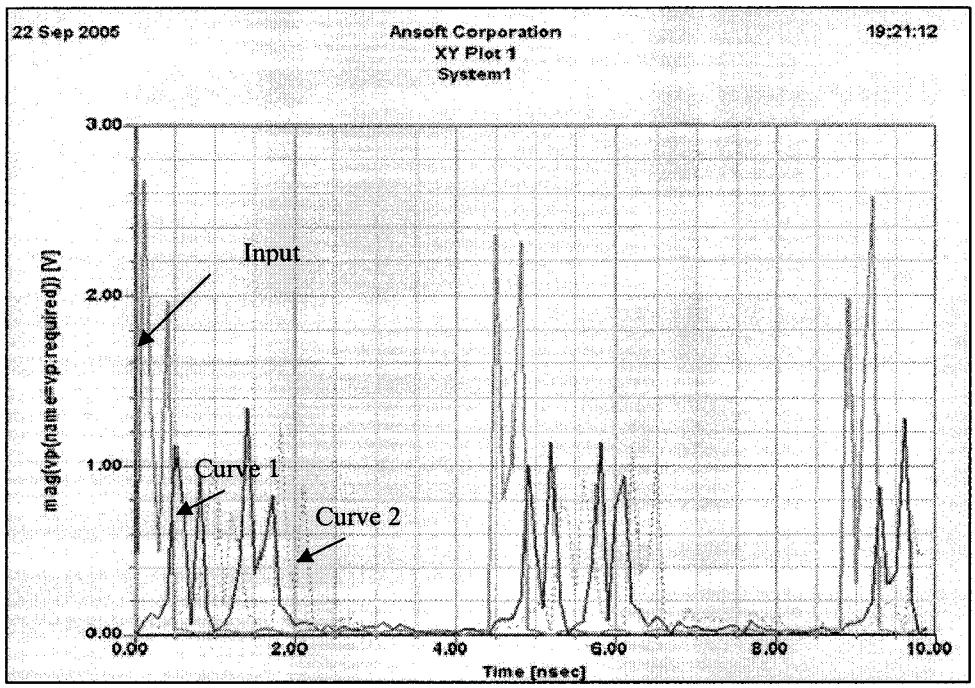


Figure 6.10 Simulated input and output waveforms at the receiver.

The experiments performed to test the RF switch, on-board antenna, individual components on the tag, signal integrity and complete tag performance are explained below.

6.3.3.1 RF switch performance tests

The RF switch (ADG 901, Analog Devices Inc) evaluation board obtained from the vendor is tested by connecting it to an RF input from the signal generator and control

logic from a pulse generator and DC input from the DC power regulator. This CMOS based SPST RF switch works for wide band applications, provides 40 dB isolation at 1 GHz and can be controlled by a LVTTL signal from the pulse generator [96]. A minimum pulse width of 10 ns with the required amplitude could be obtained from this pulse generator. Figure 6.11 shows the RF switch board with connections and the obtained OOK modulated signal. The slope in the modulated signal is attributed to the 'On/Off' delay times of the RF switch. It is observed that the RF switch can not give full amplitude unless it is supplied by a sufficient pulse width of 7 ns or more.

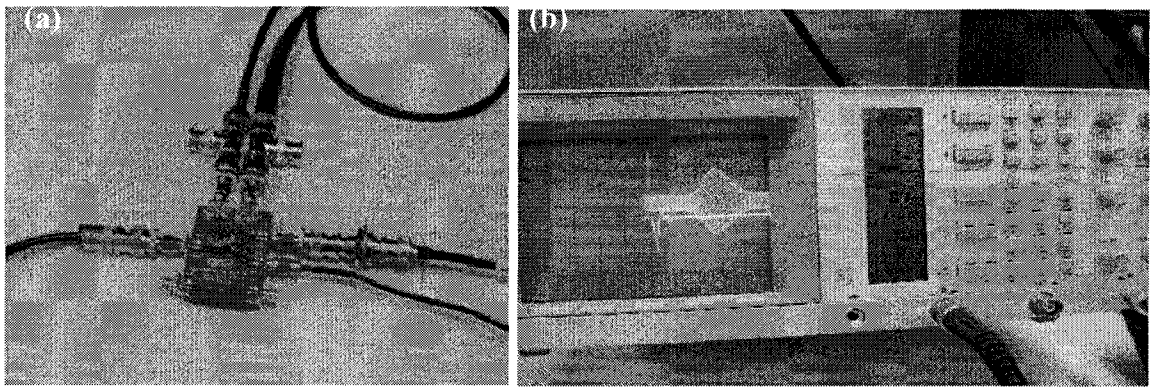


Figure 6.11 (a) RF switch with connectors (b) modulated output from the switch (x-axis = 20 ns/div and Y axis 2 V and 0.1 V /div).

6.3.3.2 On-board antenna performance tests

Tuned and un-tuned Hilbert, Meander, and Fractal antennas are tested for their received signal strengths at a distance of 10 ft from a Yagi Antenna. A modulated signal of 13 dB power input with 915 MHz carrier frequency is obtained from the RF switch using a control pulse signal of 20 ns pulse width and prf of 0.5 MHz. The distance is chosen such that antennas on the tag perform satisfactorily with minimum available signal strength in the ambient.

It is observed that all the configurations of the onboard antennas onboard could receive a modulated signal at 915 MHz (Table 6.1). The Hilbert antenna, which has the smallest form factor, performed satisfactorily and received 8 mV_{p-p} which is clearly above the noise level of 4 mV_{p-p} measured for in the lab environment ambient. However, none of the tags could receive signals properly with envelop widths of less than to 8 ns.

Table 6.1 On-tag antenna reception amplitudes.

Type of Antenna	V_{p-p}
Yagi	100 mV
Hilbert- tuned	8.0 mV
Meander- tuned	4.0 mV
Meander- untuned	5.6 mV
Fractal-untuned	29 mV

6.3.3.3 Signal integrity tests

Different experiments have been conducted on the fabricated transmission-delay-line-based RFIDs and RFID-based sensor layouts. The tag with Meander antenna, ID circuit capable of generating 9.3 ns delay and QTC sensor switch layout (Figure 6.8) has been selected for system level testing. Signal strengths have been estimated at various points of the proposed transmission-delay-line-based RFID system (Section 2.5) starting from the external transmitter to the RFID-based sensor to the receiver.

Figure 6.12 shows the block diagram of the test set up along with the voltage amplitudes measured at various test points for the RFID systems. First OOK modulated signal from the RF switch is observed in the oscilloscope at the required carrier frequency of 915 MHz with voltage amplitude of 1 V_{rms} from the signal generator. A pulse width 50 ns and 0.43 MHz PRF is fed to the control input of the RF switch and a DC voltage of

1.7 V is also applied. The modulated signal having an envelope with amplitude 140mV is fed to the Yagi transmitting antenna.

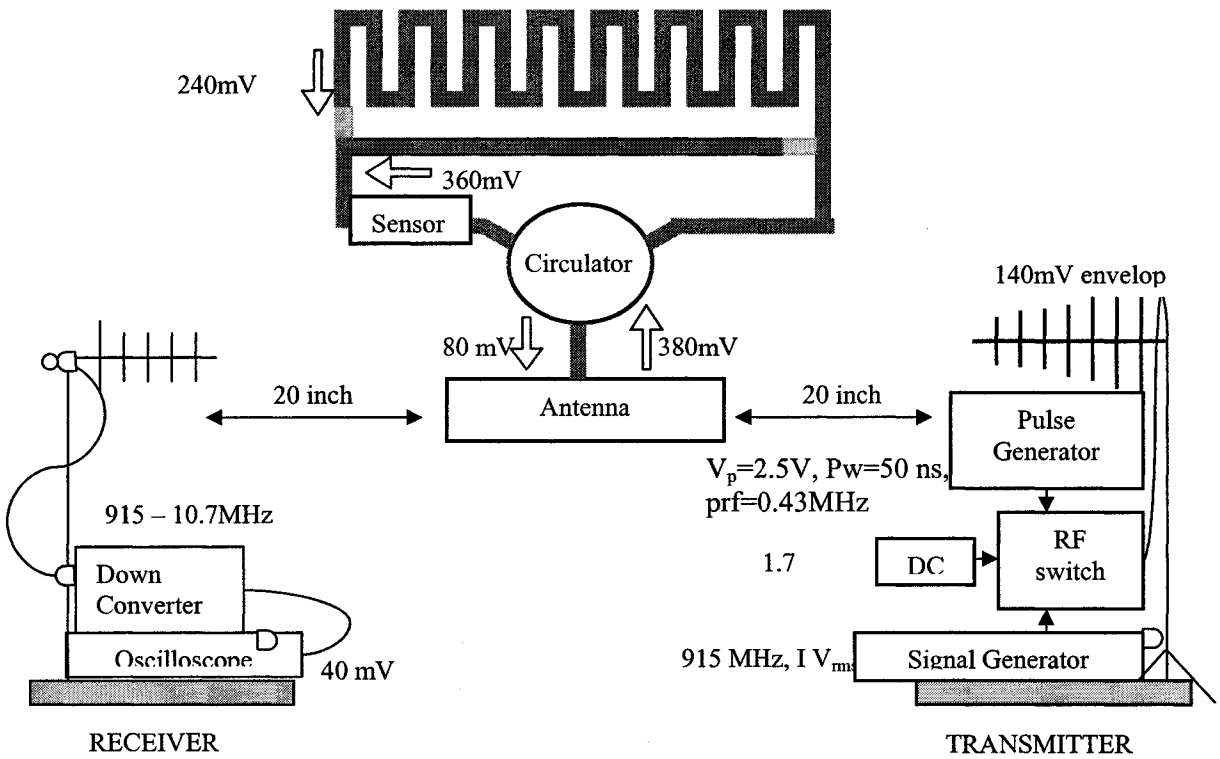


Figure 6.12 Schematic diagram showing the test set up with different signal levels observed.

The tag is kept at a distance of 20 inches where it could receive a maximum signal. The 380 mV amplitude that is observed at the output of the antenna is fed to the circulator. It is observed that there is no significant insertion loss for the circulator. Now the same 380 mV signal is fed to the input of the 3 ns transmission delay ID circuit and signal strength is measured at both branches of the circuit. Signal amplitudes of 360mV and 240 mV are observed at the straight and Meandered branches of the ID circuit respectively. A QTC pellet is now placed on the sensor layout and an amplitude of 80 mV is observed at the output of the sensor that is fed to the same Meander antenna

through the circulator. A minimum of 30 to 40 mV, which is well above the noise amplitude level, could be observed with an oscilloscope that is connected to the receiving Yagi antenna through the down converter. The oscilloscope is terminated with 50 Ω resistance to obtain accurate values. This experiment confirms the signal integrity in the proposed RFID system.

6.4 Tag Performance Test in Transmitting and Receiving Modes

The complete tag testing is done in successive steps. The external antenna is supplied with an OOK modulated signal of amplitude 1.5 V. However, antennas, including Yagi, could not receive the modulated signal if the signal is modulated using a pulse width less than 10 ns due to limited bandwidth. Below 10 ns, the amplitude of the received signal strength decreases drastically because of the RF switch limitations explained earlier. Therefore the tag is tested in receiving and transmitting modes first and the output is taken through w.fl cables and connected to the oscilloscope.

The experimental set up for the tag in receiving mode has been modeled through the simulations. Figure 6.13 shows the input, delayed and output signals from the tag taken after short and meandered branches of the ID generation circuit. It can be clearly observed that the signal strength decreases with the time delay and successive bits will have decreasing amplitudes which might set a limit to the maximum number of bits produced.

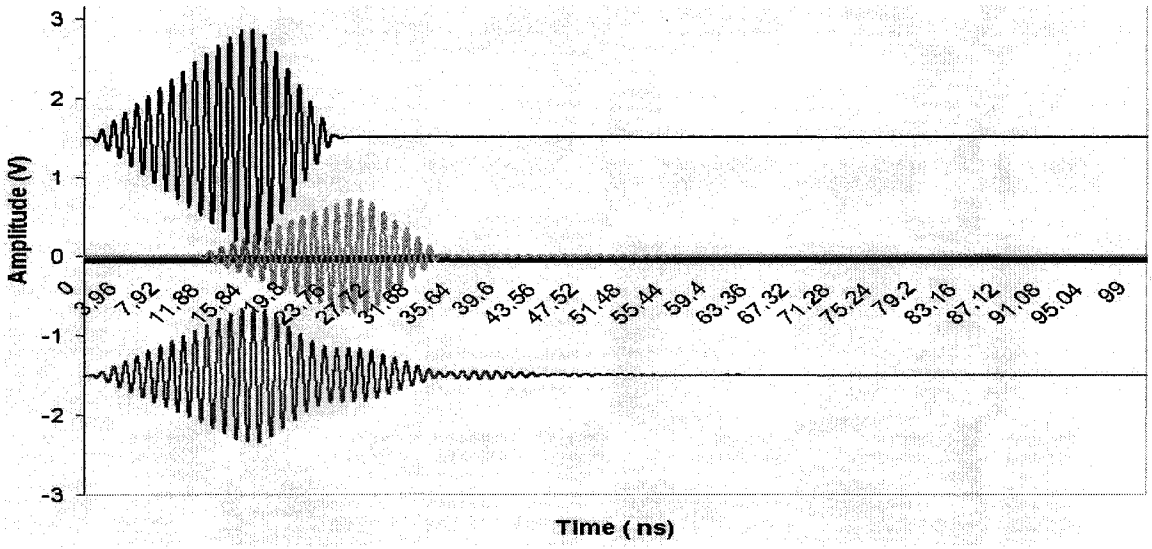


Figure 6.13 Simulated input signal, delayed signal and the output signal of the tag in receiving mode.

Figure 6.14(a) shows the input and delayed signal obtained from the tag from experimental data and Figure 6.14 (b) shows the combined output obtained when the delayed signal is tapped on to the input signal. The tag is wirelessly transmitted from the external Yagi transmitting antenna at a distance of 1 ft. Besides verifying the ID code, this experiment confirms the presence of delay in the ID circuit and the capability of receiving the signal using planar antennas.

Similarly the tag has been fed an input at the ID generation circuit and the generated output has been transmitted using the tag's antenna. The output obtained from the tag in the transmitting mode is shown in Figure 6.15.

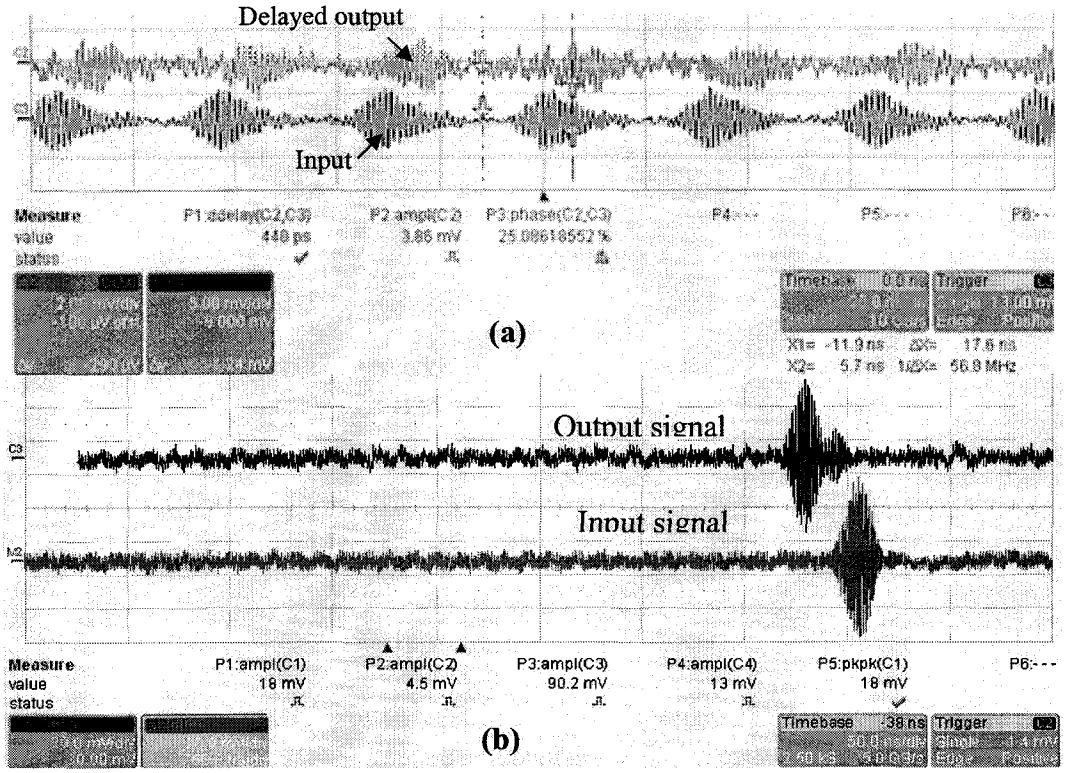


Figure 6.14 (a) Observed delay in the Meandered and straight branches of the ID generation circuit with the input signal received (b). Measured input and output signals from the tag in receiving mode (for maximum coupled signal).

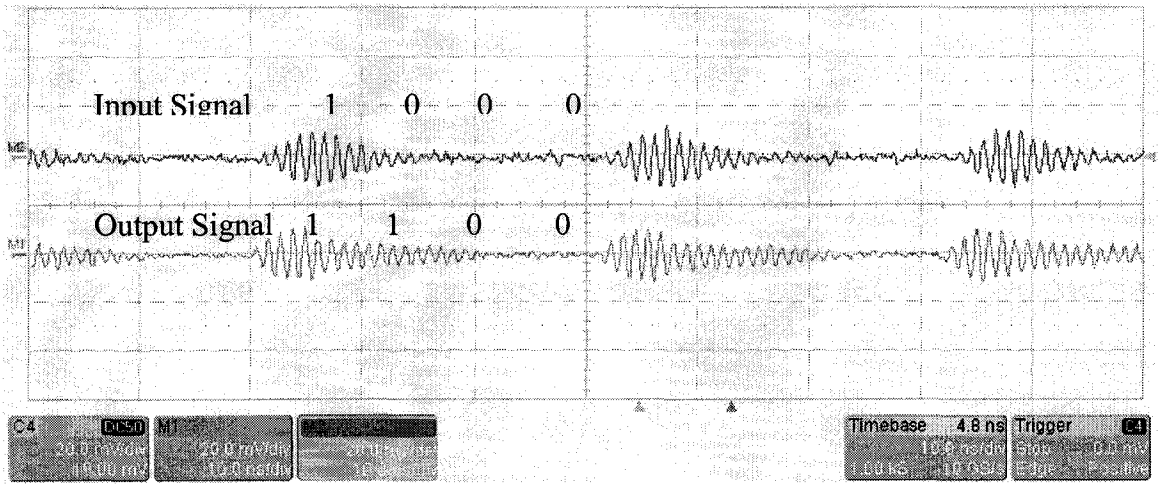


Figure 6.15 Practical input and output from the tag in transmitting mode (for maximum coupled signal).

6.5 Complete Tag Performance Tests

As mentioned earlier, maximum signal strength should be transmitted through the external transmitter so that the tag can receive and send back the signal to the external receiver. Different factors that are affecting the modulated signal strength are the characteristics of the RF switch, pulse generator and the signal generator. The signal generator (HP 8656B) has the capability of producing a maximum power of 20 mw or 13 dBm and the Yagi antenna has a gain of 8.5 dBi. From Equation 2.3, the EIRP of the transmitter, that consists of the signal generator and the Yagi antenna, is 0.17 W which is very low compared to the permitted 1 W. For the modulated signal, the 'On/Off' ratio of the signal is significantly affected by the RF switch. Even though the isolation is 40 dB between the input and output of the switch, there is a clear peak to peak signal voltage of 20 mV that can be seen when the output of the signal generator is at 13 dBm and the RF switch is off. Therefore, in order to see a clear and distinguishable output with the oscilloscope, the received signal from the tag should be greater than this amplitude. A maximum peak to peak voltage of 600 mV is measured at the output of the tag's antenna at a distance of 1 ft.

Figure 6.16 (a) shows the schematic diagram of the experimental setup for complete tag testing. External transmitting and receiving Yagi antennas and the tag are kept at 60^0 to each other at a distance of 0.1 m. This configuration confirms the proximity of each antenna to the other. Since Yagi antennas are directional, keeping them at 60^0, and not in front of each other, assures that there is a significant attenuation in the received signal coming directly from the transmitting antenna. This attenuation is required because it gives sufficient contrast between the directly coupled signal and the one from the tag.

As mentioned earlier, we need to get maximum signal from the tag. Therefore, the tag is kept at the third vertex of the equilateral triangle facing each of the Yagi antennas. The distances and the gains of the antennas and other parameters of the equipment have been modeled with an equivalent circuit and simulated using Ansoft Designer (Figure 6.16(b)).

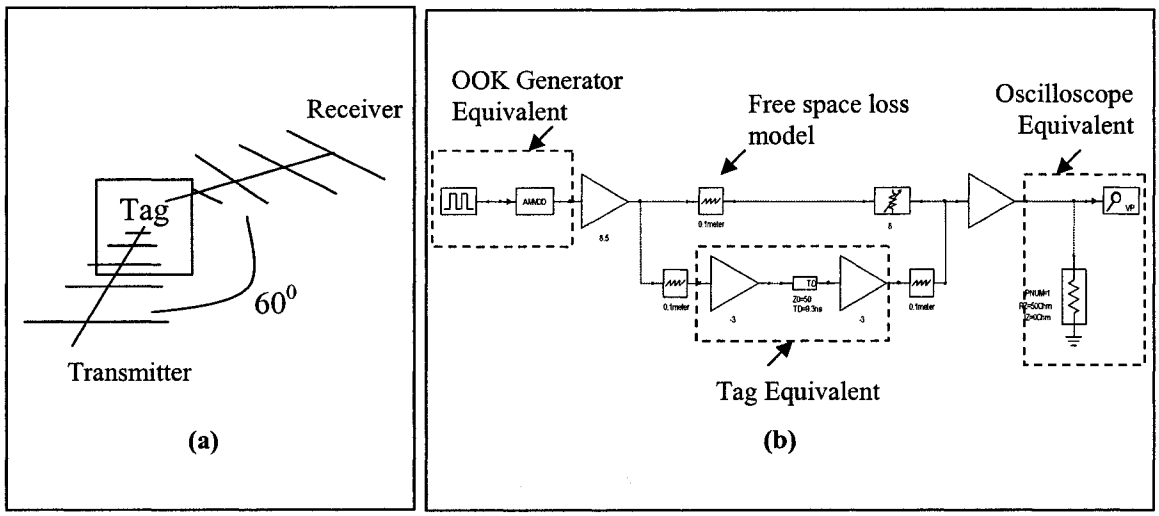


Figure 6.16 (a) Schematic diagram of the experimental setup for complete tag testing (b) circuit equivalent of the experimental setup.

Figure 6.17 (a) and (b) show the RFID simulated and practical outputs observed with the oscilloscope when the tag received the input from the external transmitter and sent it back to the receiver. Due to the overlapping widths of the modulated signals, there may be a peak or trough depending on the type of interference of the signals during the overlap.

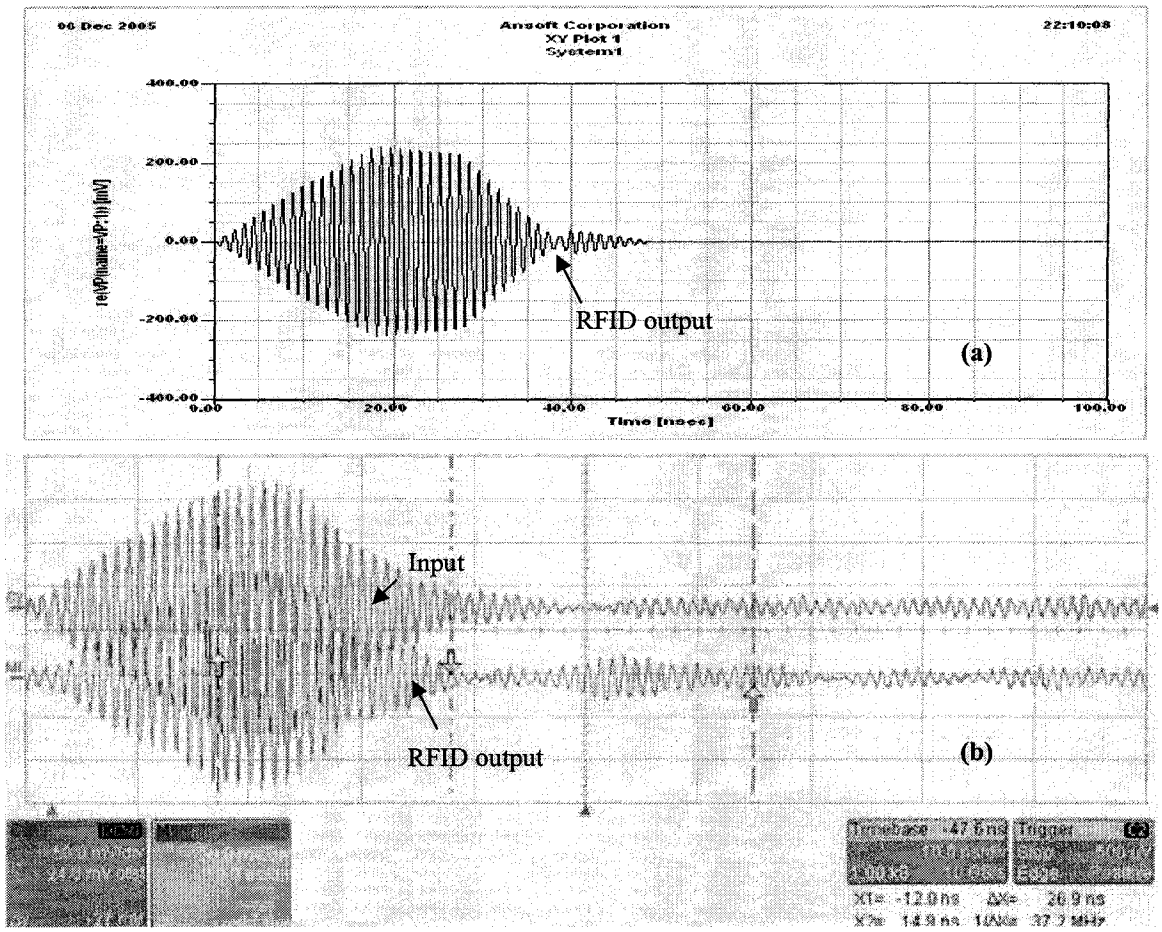


Figure 6.17 (a) Simulated tag output at the oscilloscope (b) Input signal received by the oscilloscope when the tag is communicating with the external antennas (x-axis, 10 ns/div; y-axis, 50 mV/div).

During the above measurements, there is a lot of noise in the ambient around the experimental setup due to the active RF equipment present in the lab. The overlap of the successive bits in the RFID output can be eliminated with a lesser bit width. A lesser bit can be achieved by antennas of sufficient bandwidth and an RF switch with faster rise and fall times (in picoseconds) and shorter turn-on and turn-off times. Filtering techniques can be used to further reduce the band width, if pulse widths around 1-2 ns are employed for OOK modulation.

A number of improvements were made to the experimental setup to obtain better results. Fig. 6.18 (a) shows the custom made anechoic housing, 2 ft^3 in volume, built with a type of polyurethane foam, capable of absorbing the 915 MHz signal. The anechoic chamber eliminates external reflections from the walls and the ambient noise. Figure 6.18 (b) shows the comparison between the received signal strengths inside and outside of the anechoic chamber.

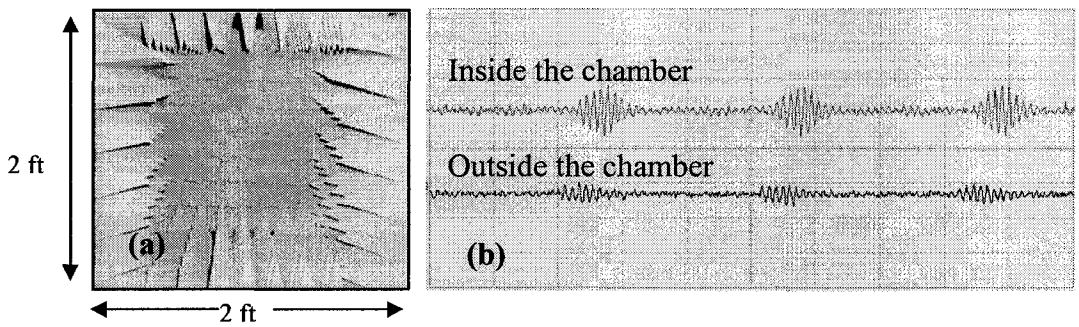


Figure 6.18 (a) Custom built anechoic housing for tag testing (b) Effect of anechoic housing on the signal strength (x-axis = time, y-axis= voltage).

Circular disc monopole (CDM) antennas are designed to improve the bandwidth of external transmitting and receiving antennas. These antennas and the tag to be tested are supported by triangular polyurethane posts inside the anechoic chamber. Figure 6.19 (a) and (b) show the schematic diagram and a picture of the original setup. All three objects, the tag and the two CDM antennas are placed in an equilateral triangular configuration, 6 cm apart, similar to the experimental setup without the anechoic chamber, as explained earlier in this section. The transmitting and the receiving CDM antennas are connected to coaxial cables that run through small openings in the corners of the anechoic housing.

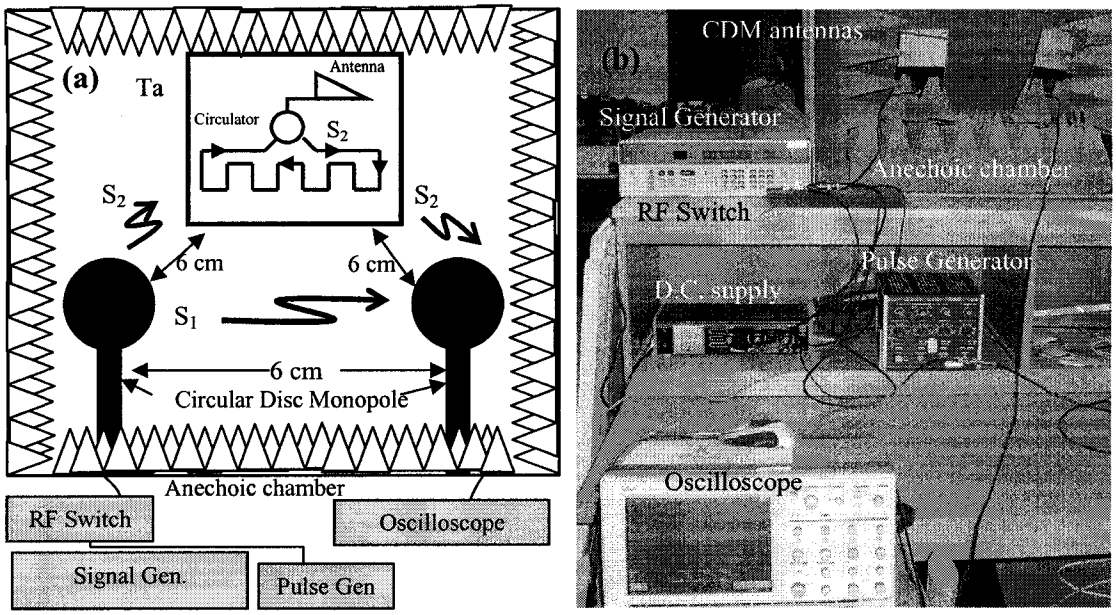


Figure 6.19 (a) Schematic diagram of experimental setup with Circular Disc Monopole antennas and the tag inside the anechoic chamber (b) Picture of original setup.

Figure 6.20 shows a clear improvement in the output signal under the present setup, compared to the earlier result (Figure 6.17) without the anechoic chamber. This figure shows the two output signals received from external transmitter in the presence and absence of the tag. It can be seen that, in the presence of the tag, the signal received at the oscilloscope is a combination of two signals. One is the signal received directly from the external transmitter and the other is the signal from the on-board tag antenna. The signal received at the oscilloscope from the tag has relatively less amplitude as compared to the one received directly from the external transmitter. This is because of the distance it has traveled from the external transmitter to the tag's antenna, through the ID circuit and from the tag's antenna to the external receiver. An OOK signal, having a center frequency of 915MHz, and 10 ns pulse width, is used as the input signal. The RF

switch has a rise and fall time of 3 ns and 6.3 ns respectively. A pulse of 31.3 MHz PRF and a 25% duty cycle is used to control the RF switch.

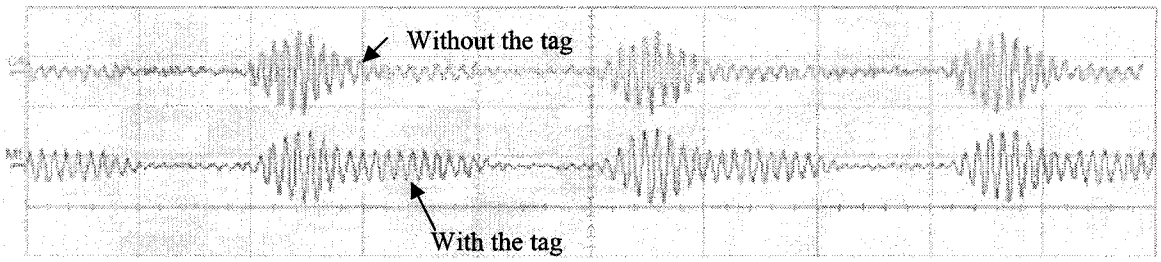


Figure 6.20 Signal received by the oscilloscope from the transmitter in the absence and presence of the tag (x-axis, 10 ns/div; y-axis, 100 mV/div).

Different combinations of the binary codes can be generated with an ID generation circuit capable of generating more delay. The codes can also be generated with a smaller bit width for the input signal but yet wide enough to be transmitted through the tag's antenna. The narrower the individual bit (the higher the bit rate), the more bandwidth is required for the antenna to transmit the signal. Therefore, to improve the response of the tag to input signals with narrower bit widths, new types of tag antennas were designed with CDM antennas being used for external transmitting and receiving antennas. Figure 6.21 (a) and (b) shows different output codes generated using tags with a triangular and spiral antenna respectively, and which have different time delays. Figure 6.21 (a), shows output signals received by the oscilloscope, when (i) there is no tag in the ambient, (ii) there is a tag with a 5 ns delay, and (iii) when there is a tag with 10 ns delay. The dotted lines show the limits of the noise signal and the continuous line the limits of the delayed signal. The high rise and fall times of the pulse is attributed to the slow switching of the RF switch. The lowest amplitude of the delayed signal is

found to be 26 mV and the amplitude of the noise is found to be 16.67 mV. Thus, a threshold of 20 mV can be set for the bit reading of 1110 or an 1111.

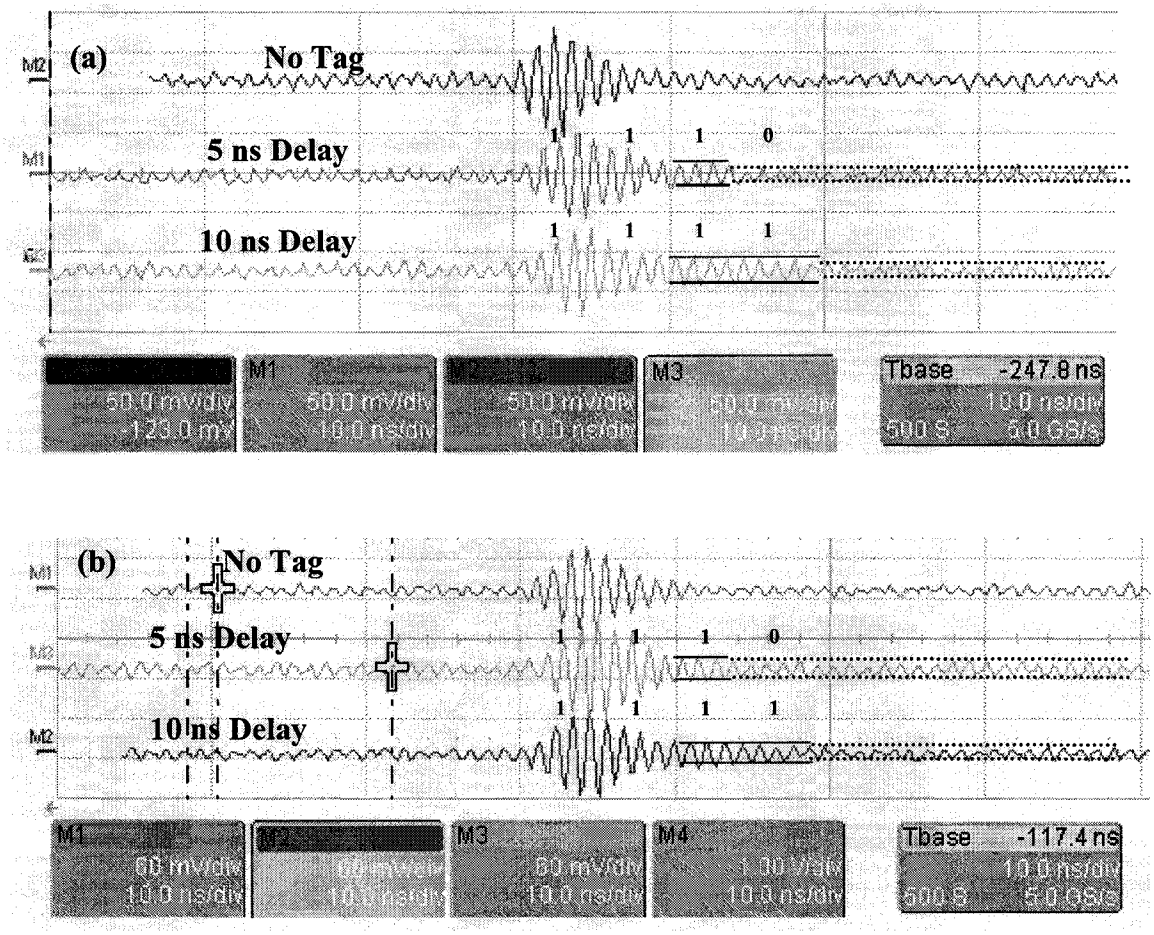


Fig. 6.21 (a) 5 ns and 10 ns delay deliverable using RFID tag with triangular antenna (b) using RFID tag with spiral antenna.

The spiral antenna used in the second tag which resulted in the output signals shown in Figure 6.21 (b), has less gain than that of the triangular antenna. It can be seen that for the tag with 5 ns delay, the noise level in the output signal is high. This is attributed to the solder connections in the tag. Also, the bandwidth of the spiral antenna is less than that of the triangular antenna and therefore, has the effect of reducing the amplitude of the delayed second bit of the output, which has to pass through two wireless

links before being captured by the receiving antenna of the oscilloscope. As explained earlier, the dotted lines show the limits of the noise signal and the continuous line shows the limits of the delayed signal. For the 10 ns delay measurement, the amplitude of the noise is found to be 15 mV and the minimum amplitude of the delayed signal is 21 mV. Thus, the threshold for bit reading could be placed in between the above values at 18 mV. For the 5 nsec delay measurement, the amplitude of the noise is found to be 24 mV and the minimum amplitude of the delayed signal is found to be 30 mV. Thus the threshold for bit reading could be placed in between the above values at 27 mV.

These output signals are measured when the external antennas and the tag are separated by 10 inches. The output can further be improved by decreasing this seperation distance. The bandwidth regulations and the bit rates are more flexible for other higher frequencies of operation that are allowed by the FCC.

CHAPTER 7

CONCLUSIONS AND FUTURE RECOMMENDATIONS

7.1 Conclusions

Conclusions are drawn from the experimental results presented in Chapters 2 to Chapter 6 in this chapter. Benchmarking of delay-based RFID technology has been done in Section 7.1. The future recommendations that have been presented in section 7.2 are based on the conclusions drawn. It is observed that there is considerable opportunity for improving the model and fabrication processes to make delay-based RFID technology more adaptable to the present RFID industry. Negotiations have been continuing to standardize/modify the present FCC regulations in the 900 MHz region and 2.45GHz ISM band width. However modifications need to be done to the present delay-based tags with respect to bit rates and bandwidths to comply with FCC regulations. Recommendations are given with respect to possible approaches and modifications of the tag to satisfy this aspect. Finally, different possible paths this novel technology can take in the future have been outlined in Section 7.2.

7.1.1 Materials and Fabrication Processes for Tag Implementation

Materials and processes presented in Chapter 3 have been studied with the designed delay-based RFID tags in mind. Though experiments have been done to test some of the materials and processes, they do not cover optimization and standardization of materials and processes for the realization of the tag. Different RFID materials have been considered in Section 3.2 with respect to the proposed delay-based tags. While polyimides and polyesters are known to be RFID substrate materials, researchers have also shown that RFID components and circuits can be made on materials, such as PET, as mentioned in Section 3.2.1. Experiments to test the chemical inertness and thermal stability of some of these substrates showed the available options for selecting the substrate for the proposed tag. However, a polyimide substrate is chosen as a safe side because of the flexibility of implementing any new process or technique other than the ones proposed in the two process-flows (Sections 3.4 and 3.5), if such a need arises.

Metals, polymers and hybrid materials such as colloidal solutions, can be used as conductors. As explained in Section 3.2.2, conducting polymers and colloidal solutions are printable using desk-top commercial printers. Antenna printing using conductive inks is becoming a popular practice in the RFID industry [97]. Techniques such as these will eliminate xerographic patterning techniques, the electroless plating of copper on polyimide and the problems associated with these methods (Sections 3.3.2 and 3.3.4). Processes, such as spray coating, the plate-through-hole technique, and drop casting have been implemented to assess the compatibility of the tag design to these rugged processes. Improving or replacing these processes with other standard practices will improve the

precision of the fabricated devices and components. Reduced cost and reliability should be the main criterion in choosing from the available options. Tag layouts are implemented using silicon-based and low-cost alternate fabrication processes to show the compatibility of the design to both process flows. In summary, tags based on LC-delay-lines and transmission-line delay can be fabricated using either one of the two process flows (Chapter 3) and either of two communication schemes considered in Section 2.3.4, such that they comply with communication regulations.

7.1.2 Realization of Delay-based Tag Elements

Planar devices, with layouts which can be integrated with one another and with other components of the tag, are preferred for implementation. Therefore, antennas, interconnects, delay elements, inductors and capacitors are chosen to be planar. The integrated layout is designed such that realization of the tag layout results in simultaneous realization of most of the planar devices mentioned above. The remaining lumped components, such as diodes, resistors, isolators and circulators, are attached to the tag layout later during component assembly.

It is observed from the simulations that planar inductor layouts without a ground show good performance characteristics. However, planar inductors are made as transmission line inductors with the ground on the bottom side of the microstrip because this eliminates both the need for another mask for patterning the ground layer and the alignment inaccuracies associated with general purpose laser-jet printers. Fabrication of the designed planar inductors using low-cost processes did not result in patterns with electrical continuity due to the inadequate resolution of the printer used. The copper thickness produced from the electroless deposition process is barely sufficient to cover

the irregular surface features of the preconditioned surface of the substrate. It is concluded that a high yielding electroless bath that would produce thicker copper and a printer with resolution of more than 600 X 600 dpi would result in inductors of satisfactory performance at 915 MHz. Inductors for the HF tag could successfully be fabricated using the low-cost processes because of broader line widths. Inductors of smaller reactance values can still be achieved using conventional lithographic processes. Capacitors are designed by modeling them as transmission-line equivalents, as explained in Section 4.4. The layouts are large enough to pattern using the xerographic processes explained in Section 3.3.2 as well as with conventional processes. Resistors with values in the range of mega-ohms are made with PEDOT/PSS, which is a water soluble conducting polymer. It can be deposited using different techniques, such as spin-coating, dip coating and spray coating with varying morphologies. Desk-jet printing and drop casting are some of the deposition techniques, but both methods are not efficient in producing patterns of high quality and accuracy. Line patterning in which a laser jet patterned transparency is deposited with a conducting polymer, such as PEDOT/PSS by spin coating or dip coating, eliminates some of these problems and produces films of good quality. For simulations, a circuit level general resistor component or a vendor component is used that represents a surface mount resistor for most of the initial prototypes.

Even though some polymer-metal junctions show schottky behavior and are compatible with proposed fabrication processes, they have high forward bias resistance and low switching speeds. Therefore, off-the-shelf diodes are used for the realization of the tags. Care is taken to insert corresponding vendor components representing the real

diodes for simulations. In the case of the non-availability of a simulation component in the software package, corresponding spice models are built from the vendor test data of the diode and inserted into the simulations. This ensured the correlation between the simulated and practical characteristics of the tag.

It is difficult to obtain antenna parameters from simulations and compare them with experimental results. This is because of the model limitations and complexities involved in the simulations. The shape of the ground at the bottom of the microstrip has an enormous effect on the impedance, gain and radiation pattern. These parameters change drastically and thus make it difficult to characterize the antennas. Therefore, care has to be taken with regard to proper grounding, soldering and ground patterning to obtain comparable results between practical and simulated results. Polarization, radiation patterns and other antenna parameters are measured and presented separately, as mentioned in Section 1.6.

Transmission lines can be easily fabricated using either low-cost fabrication processes or conventional processes. A line width of 289.65 μm is obtained for a transmission line of 50 Ω characteristic impedance corresponding to the Kapton 500 VN layer stack up (Figure 2.1 (a)) for the low-cost fabrication processes. The line width corresponding to silicon-based fabrication layer stack up (Figure 2.1(b)) is 406.26 μm. A transmission line can be used as a delay element in transmission-delay-line-based tags or as interconnect in LC-delay-line based tags. Impedance analyzer measurements of the fabricated transmission lines confirmed the 50 Ω characteristic impedance.

Section 4.9 describes the design and fabrication of the different sensor switch elements. QTC sensor film obtained from the vendor has insulating polymer on one side

and pressure sensitive material on the other side. Thus care should be taken during assembly on the layout. Since the film conducts only in the regions where pressure is applied, care should be taken to minimize the distance between interdigited electrodes. Polyaniline coated on the same layout would short circuit the electrodes when it react to acidic fumes and changes its conductivity. In both cases the maximum area is limited by the electrodes acting as antennas and receiving unwanted signals. PVDF material, on the other hand, can be attached to the electrode of 1 cm x 1 cm area can turn 'on' an FET when pressure is applied to any part of the film. PVDF material can be cut exactly to the size of the capacitor electrode and attached to it using either insulating or conducting glue. Insulating glue will add another capacitor of the same area in series with the piezoelectric capacitor while conducting glue should be conductive enough to allow the created charge to reach the capacitor electrode. In summary, all the elements of the delay-based tags can be designed within the limits of the proposed fabrication processes.

7.1.3 LC-Delay Line versus Transmission-delay-line-based Tags

The concept of LC-delay-line-based RFID is mainly based on using LC elements to produce the required delay in the input signal (Equation 2.1). The input signal should have discrete 'On-Off' times for the ID generation circuit in order to generate output bits in the provided off time using the delay line concept. In the initial proposed model this is achieved by half-wave rectification of the sinusoidal input signal which provides an 'Off' period of half the time period before the next positive half cycle is produced. Bit codes are generated within this small increment of time. The tag consists of two antennas, one for receiving the input signal and the other for transmitting the output of the ID circuit.

The ID circuit consists of power consuming diodes and resistors. These resistors are required for matching the impedances to obtain the correct delay. In the present set up, the external transmitter consists of a signal generator connected to a Yagi antenna and the external receiver consists of a Yagi antenna connected to an oscilloscope. Due to the low gains of the fabricated tag antennas, signal strength received by the tag's circuitry and the signal strength transmitted back from the tag to receiver are low.

The inherent delay present in the microstrip transmission lines is used for producing the required delay for the case of RFID systems based on transmission-line delay. The longer branch of the ID generation circuit that is based on transmission-line delay is meandered to reduce the form factor and tapped at the required time delay. This circuit is more rugged and different delays can be obtained from the same Meandered branch without the need to redesign the LC arrays.

Both RFID systems using OOK require isolators and circulators to tap the signal and to route the signal, respectively. Usage of a circulator will eliminate the second antenna and facilitate a single antenna to work as both a transmitting and receiving antenna. However, isolators and circulators are bulky in nature and require proper care during assembly. This would increase the assembly costs and diminish the chances of producing a viable technology with low-cost fabrication feasibility. However, by using a unipolar modulation scheme for the communications between the tag and the reader, isolators can be replaced by zero biased diodes.

Another big challenge for the tag is to efficiently receive the input from the tag and couple its output signal back to the reader. At UHF frequencies, interference from water, that absorbs radio waves, and metal, that reflects radio waves, can degrade the

signal, reducing the tag's readable range and, in extreme cases, prevent tag-to-reader communications. Backscatter modulation is more adaptable for passive tags and the same can be implemented in our delay-based RFID system. Initial experiments with simulations showed promising results and the circulator can be eliminated by using such a scheme.

In general, planar antennas made for the tag have a band width of tens of megahertz and can not receive signals with envelop widths less than 10 ns. Moreover, decreasing the envelop width less than this value will increase the band width significantly. This problem can be eliminated by finding out strategies to achieve more delay with a smaller form factor.

Both LC-delay-line-based RFID systems and transmission-delay-line-based RFID system can be made to be compatible with industry standards with a few modifications. The amplitude modulated sinusoidal wave that is proposed for communications in the LC-delay-line-based RFID system, even though having many advantages, is not allowed under present FCC regulation schemes. However, the OOK modulation scheme proposed for transmission-delay-line-based RFID system can be implemented with the LC-delay-line-based RFID system. This will increase the flexibility of producing the required number of bits and reduce the bandwidth problems associated with transmission-delay-line-based RIFD systems. Lumped planar LCs, even though possibly causing a certain amount of reflections due to varying line widths do have the capability of producing time delays over a wide range. Therefore, lower bit rates can be achieved to obey EPC global specifications (Gen-2) for the RFIDs. Implementing OOK will also eliminate the need of diodes which consume a lot of the power available at the tag. Unlike LC-delay-line-based

RFID systems, transmission-delay-line-based RFID systems are rugged in design and can be adapted to a varying number of bit generation methods without redesign and remanufacturing. These are simple in structure and with fewer reflections due to uniform line widths over the entire tag. Table 7.1 summarizes the characteristics of both the types of delay-based RFID systems with OOK modulation for communication.

Table 7.1 Comparison of LC-delay-line-based RFID system with transmission-delay-line-based RFID system.

Parameter (Compatible with present FCC Regulations)	LC-Delay Line Based RFID System	Transmission-delay-line Based RFID system
Design compatibility-Size		
13.56 MHz	Too big to realize using planar L C arrays	Too big to realize using transmission lines
915 MHz	Readily realizable with planar LCs ; a few square inches in size	Very large size, difficult to fabricate
2.45 GHz	A few square centimeters in size; small compared to transmission line-delay-based RFID system	Readily realizable with transmission lines, a few square inches in size
Process compatibility		
915 MHz	Compatible with low-cost and conventional processes	Compatible with conventional processes
2.45 GHz	Difficult to fabricate using low-cost processes; readily fabricated with conventional process	Easily fabricated using both low cost and conventional processes
Design flexibility		
Dynamic code generation	Difficulty in real design	Possibility of design
Multiple sensor Incorporation	Feasible	Feasible
Obtainable delay range	High	Limited
Code variations	Difficult to modify the layout for hard code	Easily adaptable layout for hard code

7.1.4 Comparisons with Other RFID Technologies

The similarities and differences between different RFID technologies are discussed below. Characteristics of the proposed delay-based RFID systems are considered for comparison rather than that of the implemented system.

7.1.4.1 Delay-based tags versus chip based RFID tags

Table 7.2 summarizes the similarities and differences between delay-based and chip-based technologies.

Table 7.2 Comparison between delay-based RFID technology and chip-based RFID technology.

Property	Delay-based RFID System	Chip Based RFID System
Size	Relatively big	Relatively small
Number of bits	Capable of generating any number of bits with bandwidth being the limit	Capable of 256 bits and more
Assembly Costs	Significant compared to price of an individual tag	Significant compared price of an individual tag
Material costs	Low	High
Fabrication Costs	Low	High
Industry- Adaptability	Can be adapted	Already adapted
Mechanical Flexibility	Moderate	Moderate
Cost	Low	Relatively high
Manufacturability	Requires desk top processes	Required billion dollar fab facilities
Feasibility of passive tags	Yes	Yes
Multiple sensor incorporation	Feasible	Feasible
Multiple sensing level detection	Feasible	Feasible
Domain	Time	Time
Frequency of operation	All ISM Bands	All ISM Bands
Network compatibility	Moderate	Low
Power consumption	Moderate	Low

It is to be noted that, while comparing the two technologies, the applicability of low-cost fabrication techniques in the manufacture of delay-based RFID, has been considered as feasible. However, as explained in Chapter 3, the low-cost fabrication processes need further development and optimization for their application in the manufacture of the delay-based RFID.

7.1.4.2 Delay-based tags versus swept RF tags

Table 7.3 summarizes the similarities and differences between delay-based RFID technology and swept RF LC resonant technologies. The conditions under which these comparisons are made, are outlined in Section 7.1.4.

Table 7.3 Comparison between delay-based RFID technology and swept RF LC resonant RFID technology.

Property	Delay-based RFID System	Swept RF LC resonant RFID system
Size	Relatively big	Relatively small
Number of bits	Any number of bits with bandwidth being the limit	Number of bits depend on the allowed frequency channels
Assembly Costs	Significant compared to price of an individual tag	No assembly costs
Material costs	Low	Low
Fabrication Costs	Low	Low
Industry- Adaptability	Can be adapted	Already adapted
Mechanical Flexibility	Moderate	Low
Cost	Low	Low
Manufacturability	Requires desk top processes	Simple fabrication processes
Feasibility of passive tags	Yes	Yes
Multiple sensor incorporation	Feasible	Not implemented
Reader complexity	Low	High
Domain	Time	Frequency
Frequency of operation	All ISM Bands	Some Bands
Network Compatibility	Moderate	Low
Power consumption	Moderate	Low

7.1.4.3 Delay-based tags versus SAW-based RFIDs

SAW-based RFID technology has gained prominence recently with the advent of new techniques. Table 7.4 summarizes the similarities and differences between delay-based and SAW-based RFID technologies. As explained in Section 7.1.4.1, the applicability of low-cost fabrication processes in the manufacture of delay-based RFID, and the possibility of eliminating the circulators and isolators, have been considered, while comparing the two technologies.

Table 7.4 Comparison between delay-based RFID technology and SAW-based resonant RFID technology.

Property	Delay-based RFID System	SAW-based RFID System
Size	Relatively big	Relatively small
Number of bits	Capable of 256 bits and more	Relatively less number of bits
Assembly Costs	Significant compared price of an individual tag	Significant compared to individual tag
Material costs	Low	Very high
Fabrication Costs	Low	High
Industry- Adaptability	Can be adapted	Already adapted
Mechanical Flexibility	Moderate	Moderate
Cost	Relatively low	High
Manufacturability	Requires desk top processes	Requires sophisticated equipment
Feasibility of passive tags	Yes	Yes
Multiple sensor incorporation	Feasible	Feasible
Multiple sensing level detection	Feasible	Unknown
Domain	Time	Time
Frequency of operation	All ISM Bands	Some ISM Bands
Network adaptability	Moderate	Moderate
Power consumption	Moderate	Low

7.1.4.4 Delay-based tags versus printable electronic based RFIDs

Polymer electronics promise easily printable electronic devices that offer mechanical flexibility and cost effectiveness at low end applications. However more research needs to be done before cheap reliable polymer electronic gadgets arrive in to market. Table 7.5 summarizes the similarities and differences between delay-based RFID technology and polymer-electronics-based RFID technology. The conditions under which the comparisons are made are briefly explained in Section 7.1.4.1.

Table 7.5 Comparison between delay-based RFID technology and swept RF LC resonant RFID technology.

Property	Delay-based RFID System	Polymer-electronics-based RFID System
Size	A few square inches	Similar in size
Number of bits	Capable of 256 bits and more	Capable of 32 bits and more
Assembly Costs	Moderate	No assembly costs
Material costs	Relatively High	Relatively Low
Fabrication Costs	Relatively High	Relatively Low
Industry- Adaptability	Can be adapted	Still needs research
Mechanical Flexibility	Moderate	High
Cost	Relatively high	Relatively Low
Manufacturability	Requires desk top processes	Requires desk top processes
Feasibility of passive tags	Yes	Not yet known
Multiple sensor incorporation	Feasible	Might be Feasible
Multiple sensing level detection	Feasible	Unknown
Domain	Time	Time
Frequency of operation	All ISM Bands	All ISM Bands
Power Consumption	Moderate	Very high

7.2 Future Work Recommendations

One of the main obstacles in making the delay-based RFID tag comply with FCC Regulations is the bandwidth. The size of the tag increases with an increase in the number of bits generated for delay-based RFID systems. The inherent delay of 0.13 ns present in the microstrip transmission lines is more or less constant and will not change with a change in the conductor or dielectric material of the microstrip, or by changing the architecture to embedded microstrip or strip line. Calculations done to observe the effect of a high dielectric material of dielectric constant around 10, resulted in an increase in the delay to 0.3 ns / inch. It was observed that there is a significant inherent time delay in the polymers due to their morphology but results in considerable power loss. Therefore, transmission-delay-line-based RFIDs at high frequencies, such as 13.56 MHz, are difficult to achieve using passive microstrip lines even though smaller and efficient tags can be made for RFIDs and RFID-based tags at a microwave frequency of 2.45GHz. Figure 7.1 shows simulated output of the delay-based tag at 2.45 GHz. This frequency band has the advantage of having 100 MHz FCC allowed bandwidth.

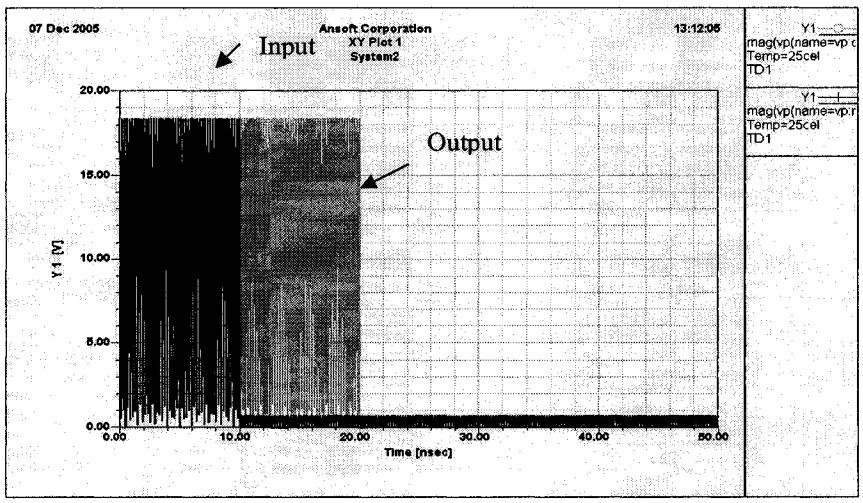


Figure 7.1 Simulated output for 2.45 GHz center frequency.

LC arrays of 13.56 MHz RFID system can produce a delay of 18 ns each which is sufficient to generate 4 bits at 915 MHz with the OOK modulation scheme without any band width problems. In any case materials and strategies need to be found in order to attain higher delays using a small area. From the simulations that are done for a 13.56 MHz signal, it can be deciphered that those LC combinations can be fabricated to be used at 915 MHz and produce larger delays (Figure 7.2).

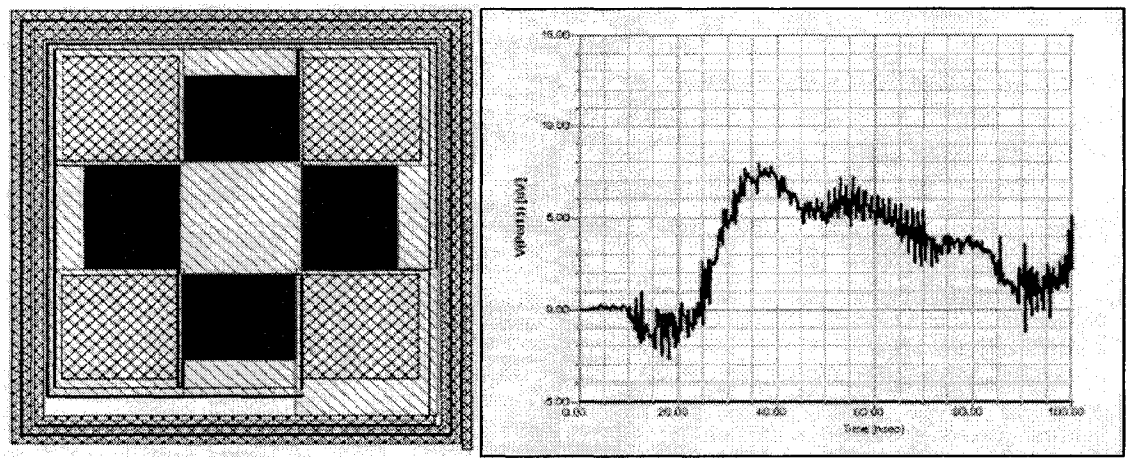


Figure 7.2 (a) 13.56 MHz LC-delay line based circuit layout and (b) Obtained output from delay lines.

Isolators and circulators on the tag make the layout complex and fabrication cumbersome. Unless these devices or their replacements can be printed or deposited in a low cost approach, assembly costs will remain high just like those for chip-based RFIDs and RFID-based sensors.

Increasing the power budget of the tag will make it readable from greater distance. Back scattering modulation is used for much of the passive RFID tag communications due to its power efficiency [98]. Initial simulation runs do show the

feasibility of implementing back scattering modulation in delay-based RFID tags (Figure 7.3). This will also eliminate the need for the circulator.

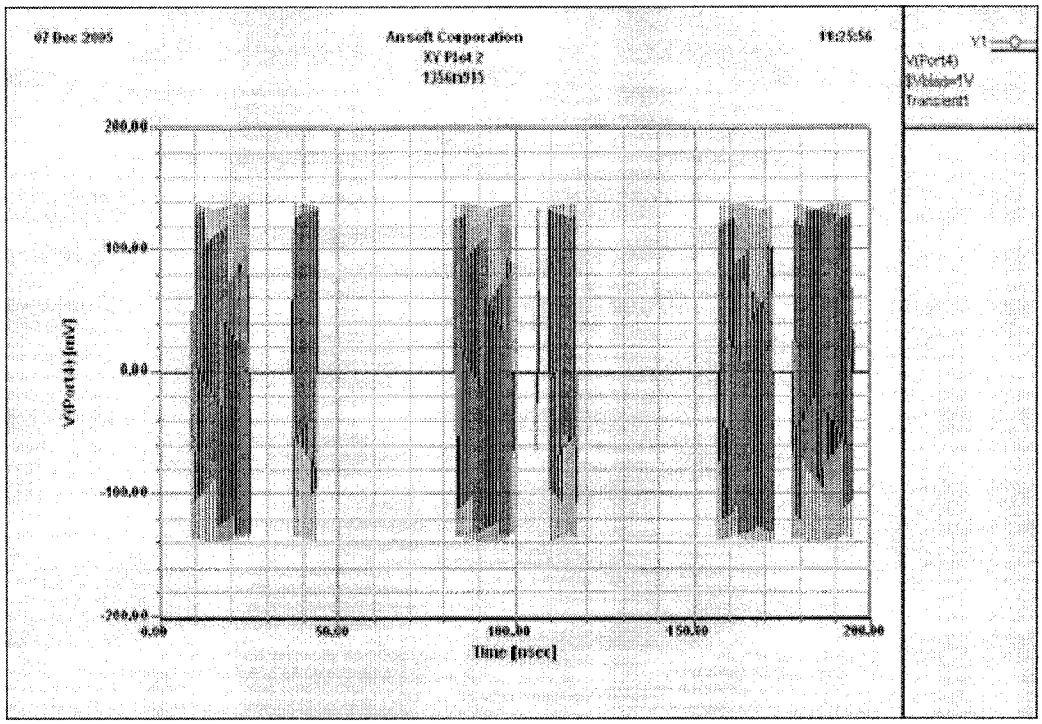


Figure 7.3 Output obtained from the simulated circuit representing the tag and back-scatter modulation circuit.

REFERENCES

1. F. Kreibel and T. Seidowski, "Smart Lables- High Volume Applications Using Adhesive Flip-Chip Technologies," *IEEE Flexible Systems,* (2001).

2. R. Fletcher, "Low-Cost Electromagnetic Tagging, Design and Implementation," Ph.D. thesis, Massachusetts Institute of Technology, Cambridge, (2002).

3. T. A. Scharfeld, "An Analysis of Fundamental Constraints on Low Cost Passive Radio-Frequency Identification System Design," M.S. thesis, Massachusetts Institute of Technology, Cambridge, (2001).

4. L. E. Larson, "Integrated Circuit Technology Options for RFIC's—Present Status and Future Directions", *IEEE Journal of Solid-State Circuits*, vol. 33, NO. 3, pp. 387, (1998).

5. U. Karthaus and M. Fischer, "Fully Integrated Passive UHF RFID Transponder IC With 16.7-μW Minimum RF Input Power," *IEEE Journal of Solid-State Circuits*, vol. 38, NO. 10, (October, 2003).

6. A. Dodabalpur, "Betting on organic CMOS," *Materials Today,* September (2004).

7. S. Sarma, "Towards the 5 cents tag, white paper, *MIT AutoID Center*," November (2001).

8. S. Gitanjali and S. Sarma, "Manufacturing Cost Simulations for Low Cost RFID Systems, whitepaper, *MIT Auto-ID Center*," (February, 2003).

9. "AutoID Technology Guide, whitepaper," *MIT Auto-ID Center*, (2002).

10. T. Li, M. Mitsuishi and T. Miyashita, "Photodegradable polymer LB films for Nano-lithographic imaging techniques," *Thin Solid Films*, vol. 389, (2001), pp. 267-271.

11. K.H. Chmil, D.M. de Leeuw, M.M.J. Simenon and A. J. W. Tol, "Synthesis and properties of n-type doped semiconducting materials," *Synthetic Metals*, vol. 84, no. 1-3, pt 1, (January, 1997), pp. 387-388.

12. H. Chatham, "Review- Oxygen Diffusion Barrier Properties of transparent coatings on Polymeric Substrates," *Surface and Coatings Technology,* vol.78, (1996), pp. 1-9.

13. K. Ziemelis, "Putting it on plastic," *Nature*, vol. 393, (1998), pp. 619-20.

14. A.J. Heeger, H. Shirakawa and A.G. Macdiarmid, "Conducting polymers, *Seminal paper for Nobel prize in chemistry*," http://www.nobel.se/chemistry/laureates/2000/adv.html, accessed on 11-01-2005.

15. A. Galatanu, M.I. Chipara, M.D. Chipara, and M. Toacsen, "Structural properties of conducting and semiconducting polymers," *Physica B: Condensed Matter*, vol. 234-236, (June, 1997), pp. 242-244.

16. U. Lemmer, A. Ochse, M. Deussen, R.F. Mahrt, E.O. Goebel, H. Baessler, P.H. Bolivar, G. Wegmann, and H. Kurz, "Energy transfer in molecularly doped conjugated polymers," *Synthetic Metals*, vol. 78, no. 3, (April, 1996), pp. 289-293.

17. N. Camaioni, G. M. Casalbore, A. Geri, and G. Zotti, "An investigation of the electronic properties of Poly(4,4'- dipentoxy -2,2'-bithiophene)," *Journal of Physics–D Applied Physics*, vol. 31, (1998), pp. 1245-1250.

18. S. Tagmouti, A. Outzourhit, A. Oueriagli, M. Khaidar, M. Elyacoubi, R. Evrard, and E. L. Ameziane, "Electronic Properties of poly(3-methylthiophene)," *Solutions Energy Materials and Solution Collusions.,* vol. 71, (2002), pp. 9-18.

19. A.W. Denie, Van Der Gon, J. Birgerson, M. Fahlman, and W.R. Salaneck, "Modification of PEDOT–PSS by low-energy electrons," *Organic Electrnonics,* vol. 3, (2002), pp. 111–118.

20. A. Elshabini, F. Barlow, and A. Lostetter, "Low cost flex substrates for miniaturized electronic assemblies," *Micro Electronic Reliability,* vol. 42, (2002), pp. 1091-1099.

21. P. Chandrasekhar, *Conducting Polymers, Fundamentals and Applications-a practical approach*, 1st ed. Boston: Kluwer Academic Publishers, (1999).

22. "A review of flexible circuit technology and its applications," *Prime Faraday Technolgoy Watch*, (June, 2002).

23. A.J. Heeger, "Semiconducting and Metallic polymers-The Forth generation of polymeric materials," *Synthetic Metals*, vol. 125, (November, 2001), pp. 23-42.

24. M.G. Kane, J. Campi, M.S. Hammond, F.P. Cuomo, B. Greening, C.D. Sheraw, J.A. Nichols, D.J. Gundlach, J.R. Huang, C.C. Kuo, L. Jia, H. Klauk, and T.N. Jackson, "Analog and digital circuits using organic thin-film transistors on Polyester substrates," *IEEE Electron Device Letters*, vol. 21, no. 11, (November, 2000), pp. 534-536.

25. B.K. Crone, A. Dodabalapur, R. Sarpeshkar, A. Gelperin, H.E. Katz, and Z. Bao, "Organic oscillator and adaptive amplifier circuits for chemical vapor sensing," *Journal of Applied Physics*, vol. 91, no. 12, (June, 2002), pp. 10140.

26. E.J. Meijer, D.M. De Leeuw, S. Setayesh, V.E. Van, B.-H. Huisman, P.W.M. Blom, J.-C. Hummelen, U. Scherf, and T.M. Klapwijk, "Solution-processed ambipolar organic field-effect transistors and inverters, *Nature Materials,* vol. 2, no. 10, (October, 2003), pp. 678-682.

27. Z. Rang, A. Haraldsson, D.M. Kim, P.P. Ruden, M.I. Nathan, R.J. Chesterfield, and C.D. Frisbie "Hydrostatic-pressure dependence of the photoconductivity of single-crystal pentacene and tetracene," *Applied Physics Letters*, vol. 79, no. 17, (October, 2001), pp. 2731.

28. C. Reese, M. Roberts, M.M. Ling, and Z. Bao "Organic thin film transistors," *Materials Today*, vol. 7, no. 8, (September, 2004), pp. 20-27.

29. Excess Adds Ammonia Detection Capability to RFID-based Sensor Tags, http://www.kasper-cdrom.com/499002.page, accessed on 11-01-2005.

30. D. Redinger, S. Molesa, S. Yin, R. Farschi, and V. Subramanian "An ink jet deposited passive component process for RFID," *IEEE Transactions on Electronic Devices*, vol. 51, no. 12, (December, 2004).

31. V. Subramanian, P.C. Chang,J.B. Lee, S.E. Molesa, and S.K. Volkman, "Printed Organic Transistors for Ultra-low-cost RFID Applications," *IEEE International Conference on Polymers and Adhesives in Microelectronics and Photonics,* (2004), pp. 67-71.

32. V. Subramanian, J.M.J. Frechet, P.C. Chang, D.C Huang, J.B. Lee, S.E. Molesa, A.R. Murphy, D.R. Redinger, and S.K. Volkman "Progress towards development of all printed RFID tags: Materials, Processes and Devices," *Invited paper, Proceedings of the IEEE*, vol. 93, no. 7, (July, 2005).

33. P.F. Baude, D.A. Ender, T.W. Kelley, M.A. Haase, D.V. Muyres, and S.D. Theiss "Pentacene Based RFID transponder circuitry," article, *3M company.*

34. The Global SAW Tag -a New Technical Approach to RFID, white paper *RFSAW, Inc.*, (2004).

35. S. Ramisetti, "Design and Development of an ID Generation Circuit for Low-cost Passive RFID-based Applications," M.S. Thesis, Louisiana Tech University, Ruston, (2005).

36. J.K. Vemagiri, "Design and Development of Triangular, Spiral, and Fractal Antennas for RFID applications," Ph.D. Dissertation, Louisiana Tech University, Ruston, (2006).

37. U.K. Dandgey, "Design and Development of a Microstrip Meanderline Antenna for an RFID-based Passive Wireless Sensor Platform," M.S. Thesis, Louisiana Tech University, Ruston, (2005).

38. W.A. Mohammad, "Design, Fabrication and Characterization of Sensor Elements for Wireless Sensor System," M.S. Thesis, Louisiana Tech University, Ruston, (2005).

39. B. Analui and A. Hajimiri "Statistical Analysis of Integrated Passive Delay Lines," *IEEE Custom Integrated Circuits Conference*, (2003), pp. 107-110.

40. Ansoft Designer software, http://www.ansoft.com, accessed on 11-01-2005.

41. Coventor MEMS software, http://www.coventor.com, accessed on 11-01-2005.

42. Passive Delay Line Design Considerations, *Rhombus Industries*, 1998.

43. Delay Line, http://en.wikipedia.org/wiki/Delay_line, accessed on 11-01-2005.

44. A. Chamarti, W. Mohammad, S. Ramisetti, J. Vemagiri, U. Dandgey, and K. Varahramyan, "A Low Cost Flexible Substrate Wireless Sensor Tag Based on Sensor Switch Element," *55th IEEE Electronic Components and Technology Conference,* 2005

45. A. Chamarti, and K. Varahramyan, "Transmission Delay Line Based ID Generation Circuit for RFID Applications," accepted for publication in IEEE Microware and Wireless Component Letters, 2006

46. C.W. Sayer, *Complete Wireless Design*, 1st ed. New York: McGraw Hill, (2001).

47. G. Kennedy and B. Davis, *Electronic Communication Systems*, 4th ed. Ohio: Macmillan/McGraw-Hill, (1993).

48. N. Santhanam, "Low Cost High Performance RF Substrates," *IEEE Transcations on Circuits and Systems,* (1999).

49. M.S. Shur, S. Rumyantsev, R. Gaska, B.Q. Wei, R. Vajtai, P.M. Ajayan, and J. Sinius, "Structural and transport properties of CdS films deposited on flexible substrates," *Solid State Electronics,*. vol. 46, (2002), pp. 1417–1420.

50. M. Strobel, *Plasma Surface Modification of polymers*, 1st ed. Netherlands: VS publications, (1994).

51. N. Inagaki, S. Tasaka, and K. Hibi, "Improved adhesion between plasma-treated Polyimide film and evaporated copper," *Journal of Adhesion Science and Technology*, vol. 8, no. 4 pt. 2, (1994), pp. 395-410.

52. Kapton Polyimide film – General Specifications, Bulletin-GS-96-7 http://www.dupont.com/kapton/general/H-38479-4.pdf

53. Copper Metallization: Non-contact Sheet Resistance and Film Thickness Mapping, http://www.lehighton.com/AppNotes/CuMetallization/cumetallization.html. accessed on 11-01-2005.

54. D. Hohnholz, H. Okuzaki, and A.G. MacDiarmid, "Plastic Electronic Devices Through Line Patterning of Conducting Polymers," *Advanced Functional Materials,* vol. 15, no. 1, (2005), pp. 51-56.

55. Technical Data Sheet, Ink Refill Kit, *StratiteK Inkjet Refill Kit Inc.*

56. Technical Data Sheets, *Cuprothick 84,* Technic. Inc.

57. Faster Caustic Etching of Kapton H, E, and KN Types, *Dupont Kapton® Technical Bulletin,* http://www.dupont.com/kapton/general/caustic-etching.pdf. accessed on 11-01-2005.

58. J. Vemagiri, "Electroless Deposition of Magnetic and Non-magnetic Ni Alloys for Microstructure Fabrication," M.S. Thesis, Louisiana Tech University, Ruston, (2002).

59. R. Aithal, "Electroless Copper Deposition for Non-catalytic Substrates with Single Titanium Seed Layer," M.S. thesis, Louisiana Tech University, Ruston, (2002).

60. S. Yanamandra, "Integration of Electroless Deposition and Inkjet Printing For Metal-polymer Schottky Diode Fabrication," M.S. Thesis, Louisiana Tech University, Ruston, (2002).

61. T.F. Guo, S. Pyo, and Y. Yang, "Vertically Integrated Electronic Circuits via a Combination of Self-Assembled polyelectrolytes, Ink-Jet Printing, and Electroless Metal Plating Processes," *Langmuir*, vol. 18, (2002), pp. 8142-8147.

62. A. Turut and F. Koeleli, "Semiconductive Polymer-based Schottky Diode," *Journal of Applied Physics,* vol. 72, (1992), pp. 818-819.

63. P. Gudmundson and A. Wikstrom, "Stresses in Thin Films and Interconnect Lines," *Microelectronic Engineering*, vol. 60, no. 1-2, (January 2002), pp. 17-29.

64. New Chip Encapsulant 9008 Passes Polyimide Bend Test even at -20^{0}C, http://www.dymax.com/pdf/press_release/p102_9008_chip_encapsulant.pdf accessed on 11-01-2005.

65. C.C. Clavijo, J. Seekamp, A.P. Kam, T. Hoffmann, S. Zankovych, C.M. SotomayorTorres, C. Menozzi, M. Cavallini, M. Murgia, G. Ruani, F. Biscarini, M. Behl, R. Zentel, and J. Ahopelto, "Nanoimprint Lithography for Organic Electronics," *Microelectronic Engineering*, vol. 61-62, (2002), pp. 25-31.

66. J. Steiger, S. Heun, and N. Tallant, "Polymer Light Emitting Diodes Made by Ink," Jet Printing, *Journal of Imaging Science and Technology*, vol. 47, no. 6, (2003), pp. 473-478.

67. T. Li, M. Mitsuishi, and T. Miyashita, "Photodegradable Polymer LB Films for Nano-lithographic Imaging Techniques," *Thin Solid Films*, vol. 389, (2001), pp. 267-271.

68. H. Meng and F. Wudl, "A Robust Low Band Processable n-Type Conducting Polymer Based on Poly(isothianaphthene), *Macromolecules*," vol. 34, (2001), pp. 1810-1816.

69. J.M. Shaw and P.F. Seidler "Organic electronics: Introduction," *IBM Journal of Research and Development.*, vol. 45, (2001), pp. 3-9.

70. Dupont Pyralux FR Copper-Clad Laminates, *Technical data sheet*, http://www.dupont.com/fcm/products/H-73233.pdf accessed on 11-01-2005.

71. Pyralux FR, LF and AP dielectric constants and dissipation factors, *Technical Data Sheet, Pyrex Inc.*

72. Microstip Trace Calculator, *http://www.emclab.umr.edu/pcbtlc/microstrip.html.* accessed on 11-01-2005.

73. SPICE Diode Model Parameters, http://www.acsu.buffalo.edu/~wie/applet/spice_pndiode/spice_diode_table.html. accessed on 11-01-2005.

74. S. Tagmouti, A. Outzourhit, A. Oueriagli, M. Khaidar, M. Elyacoubi, R. Evrard, and E.L. Ameziane, "Electrical Characteristics of W/P3MT/Pt Diodes," *Thin Solid Films.* vol. 379, (2000), pp. 272-278.

75. W. Geens, S.E. Shaheen, B. Wessling, C.J. Brabec, J. Poortmans, and N.S. Sariciftci, "Dependence of Field-effect Hole Mobility of PPV-based Polymer Films on The Spin-casting Solvent," *Organic Electronics*, vol. 3, (2002), pp. 105–110.

76. Y. Onganer, M. Saglam, A. Turut, H. Efeoglu, and S. Tuzemen, "High Barrier metallic Polymer/ p-type silicon schottky diodes," *Solid-State Electronics*, vol. 39, no. 5, (1995), pp. 667-680.

77. Aernouts T, W. Geens, J. Poortmans, J. Nijs and R. Mertens, "Analysis and Simulation of the IV-characteristics of PPV-oligomer Based Schottky Diodes," *Synthetic Metals,* vol. 122, (2001), pp. 153-155.

78. H.L. Gomes, G.W. Jones, and D.M. Taylor, "Influence of Fabrication Conditions on the Electrical Behavior of Polymer Schottky Diodes," *Synthetic Metals, v*ol. 85, (1997), pp. 1351-1352.

79. J.R. de Limaa, L.O. PeÂ resb, J.R. Garciab, J. Gruberc, and I.A. HuÈ Mmelgena, "A Poly(acetoxy-p-phenylene vinylene) Based Diode With a Soft Breakdown Behavior," *Solid State Electronics,* vol. 44, (2000), pp. 565-69.

80. T. Cassagneau, J.H. Fendler, S.A. Johnson, and T.E. Mallouk, "Self-Assembled Diode Junctions Prepared from a Ruthenium Tris -(Bipyridyl) Polymer, n-type TiO_2 Nanoparticles, and Graphite Oxide sheets," *Advanced Materials*, vol. 12, no. 18, (2000), pp. 1363-1366.

81. A.N. Chowdhury, Y. Kunugi, Y. Harima, and K. Yamashita, "Electrochemical Switching to p- ype and n-type Semiconductance with Poly (3-methyl thiophene) Film," *Thin Solid Films*, vol. 271, (1995), pp. 1-3.

82. S-parameter Data for MA4E1338-114T, Personal communication with Mr. Joe Bowinsky, Technical Expert, MACOM.com, (2005).

83. D. Kim, M.A. Ingram, and W.W. Smith Jr., "Measurements of Small-Scale Fading and Path Loss for Long Range RF Tags," *IEEE transactions on antennas and propagation*, vol. 51, no. 8, (August, 2003).

84. J. A. Fordham, "An Introduction to Antenna Test Ranges, Measurements and Instrumentation," *Microwave Instrumentation Technologies, LLC.*

85. S. Bharadwaj, "Polyaniline for Freshness Detection Purposes," Research Report, Louisiana Tech University, (2005), Ruston.

86. A. Babel and S. A. Jenekhe, "Electron Transport in Thin-Film Transistors from an n-type Conjugated Polymer," *Advanced Materials*, vol.14, no.5, (2002), pp. 371-374.

87. H. Klauk, D.J. Gundlach, J.A. Nichols, and T.N. Jackson, "Pentacene Organic Thin-Film Transistors for Circuit and Display Applications," *IEEE Transcations on Electronic Devices*, vol. 46, (1999), pp.1258-63.

88. S. Scheinerta, G. Paaschb, S. Pohlmanna, H.-H. HoÈ rholdc, and R. Stockmannc, "Field Effect in Organic Devices With Solution-doped Arylamino-poly-(phenylene-vinylene)," *Solid State Electronics,* vol. 44, (2000), pp. 845-53.

89. A. Kuntman and H. Kuntman, "Study on Dielectric Properties of A New Polyimide Film Suitable for Interlayer Dielectric Material in Microelectronics Applications," *Micro Electronics Journal*, vol. 31, (2000), pp. 629-34.

90. L. Herard, "Packaging Reliability," *Micro Electronic Engineering,* vol.49, (1999), pp. 17-26.

91. D.M. de Leeuw, M.M.J. Simenon, A.R. Brown, and R.E.F. Einerhand, "Stability of n-type Doped Conducting Polymers and Consequences for Polymeric Microelectronic Devices," *Synthetic Metals*, vol. 87, (1997), pp. 53-59.

92. A. Dodabalapur, J. Laquindanum, H.E. Katz, and Z. Bao, "Complementary Circuits with Organic Transistors," *Applied Physics Letters*, vol. 69, (December, 1996), pp. 4227-29.

93. C.D. Dimitrakopoulos, A.R. Brown, and A. Pomp, "Molecular Beam Deposited Thin Films of Pentacene for Organic Field Effect Transistor Applications," *Journal of Applied Physics*, vol. 80, (1996), pp.2501-08.

94. Y.Y. Lin, A. Dodabalapur, R. Sarpeshkar, Z. Bao, W. Li, K. Baldwin, V.R. Raju, and H.E. Katz,"Organic Complementary Ring Oscillators," *Applied Physics Letters*, vol. 74, (1999), pp. 2714-16.

95. M.J. Lee, C.P. Judge, and S.W. Wright, "Thin Film Transistors for Displays On Plastic Substrates," *Solid State Electronics,* vol. 44, (2000), pp. 1431-34.

96. Wideband 40 dB isolation at 1 GHz CMOS 1.65 V to 2. 75 V, SPST switches-ADG 901/ADG 902, *Application data sheet, Analog devices Inc.,*

97. J. Neilson, "Flexo Printing with Conductive Ink," presentation, *Printed Electronics Europe-2005,* (April 2005).

98. K. V. S. Rao, "An Overview of Back Scattered Radio Frequency Identification System (RFID)," *IEEE Proceedings*, (1999).