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Introducing porous silicon as a sacrificial material to obtain cavities in substrate of SOI wafers and a getter material for MEMS devices

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INTRODUCING POROUS SILICON AS A SACRIFICIAL MATERIAL TO OBTAIN CAVITIES IN SUBSTRATE OF SOI WAFERS AND A GETTER MATERIAL FOR MEMS DEVICES

by

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ABSTRACT

Microelectromechanical system (MEMS) resonators have been a subject of research for more than four decades. The reason is the huge potential they possess for frequency applications. The use of a MEMS resonator as the timing element has an experimental history and huge progress has been made in this direction. Vacuum encapsulated MEMS resonators are required for high precision frequency control. Hence, a device with a high quality factor and durability is needed. In this effort, a new process for producing a cavity in the substrate of Silicon on insulator (SOI) MEMS devices and augmenting it with a getter using porous silicon is developed. The process involves a mask-less, self-aligned cost effective electrochemical etching process.

A 10 μm cavity is introduced in the substrate of SOI dies. This helps in increasing the packaging volume of the SOI resonators along with mitigating the viscous damping effects. The stiction problem in MEMS devices is effectively eliminated and millimeter long slender MEMS structures do not get stuck to the substrate. It also helps in reducing the parasitic capacitance between the device side and the substrate.

The porous silicon getter is introduced as a getter material for vacuum encapsulated MEMS devices. This getter needs no external mask and is self-aligned. It requires no external heat or additional materials to operate. The highly reactive porous silicon can readily react with the oxygen gas and form an oxide layer that can trap other gas molecules. This helps in maintaining low pressures in the cavity of the bonded MEMS resonators.

A tuning fork resonator with a resonant frequency of 245 kHz was used to realize the benefits of the cavity and the getter. It was observed that the unpackaged device with the cavity in the substrate showed two times better quality factor at different pressures, than the device with no cavity. In order to understand the benefits of porous silicon as a getter, the MEMS devices (one with only a cavity in the substrate and the other with a cavity and getter) were anodic bonded and tested. The devices with a getter reported two times better quality factor than the non-getter devices.

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DEDICATION

To

My dear parents: Mr. Mubasheruddin Mohammed & Mrs. Saleha Begum

and

My Sheikh: Dr. Abdul Sattar Khan Mohammed

(Ex-Head of Arabic Dept, Osmania University, Hyderabad, India)

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CHAPTER 1

INTRODUCTION

Microelectromechanical systems (MEMS) are the micro sized (less than 1 mm and more than 1 μm) mechanically moving structures. MEMS devices are in a myriad of applications ranging from chemical sensing [1] to biomedical sensing [2] to clocking devices [3, 4]. One of the most famous MEMS devices is the Digital Mirror Device (DMD) by Texas Instruments. With the advent of DMD, the display screens have seen magnificent improvements in terms of cost versus quality. MEMS microphones are competing in price and performance with the traditional electret condenser microphones [5].

MEMS sensors have also been introduced in the automobile industry. The MEMS accelerometers in the crash sensing systems have reduced the number of components that were used, and henceforth, they increased the accuracy of the system. The performance of a positioning device, such as a GPS, is dependent on its ability to synchronize with the satellites, which is dependent on the internal clock [6]. Quartz oscillators have always proven to be the best timing devices. However, they are relatively large. MEMS oscillators offer a way to miniaturize clocks. One of the major issues with MEMS devices is their large temperature dependence. Quartz has proven to be stable over wide ranges of temperature. Immense research is being carried out to make the MEMS based oscillators stable over temperature. Whether or not the MEMS oscillators replace the quartz oscillators depends on solving the issue of temperature dependence of MEMS devices. Up until the past five years, the number of papers published in IEEE frequency control conference was 80% quartz based research and 20% MEMS based research [7]. In these past few years the trend has reversed, and more than 85% papers are published in MEMS based research and the rest in quartz based research. This indicates a major push for MEMS timing devices. Honeywell, in collaboration with the Defense Advanced Research Projects Agency (DARPA), is currently working on chip scale atomic clock (CSAC) devices to be used in wireless communication and precise positioning systems [8].

In an effort to enhance the performance of the MEMS devices, this dissertation presents results obtained by introducing a cavity and getter material using an electrochemical etching process. In this chapter, the motivation behind this project is discussed in detail.

1.1. Actuation in MEMS

The general actuation mechanisms in MEMS are electrostatic, electromagnetic, thermal, or magnetic. The advantage of the electrostatic actuation is that there is no current consumption but high actuation voltages are used [9]. Depending upon the actuation mechanism, the MEMS devices could be used for different applications [10]. The parameters involved in micro actuation are the force (F), displacement (x), volume (v), and response time. The formula that could be used to compare between the actuation mechanisms is the work output per unit volume given by

$$W = \frac{F\,x}{v}. \tag{1.1}$$

In this dissertation, the electrostatic actuation mechanism was used. The principle of electrostatic actuation is the attraction of the columbic charges. As the MEMS devices are micro-scaled, the electrostatic forces become significant at this level, unlike the macro-scaled devices. The displacement in any specifically designed structure could be obtained by the columbic attraction between the oppositely charged bodies [10]. Figure 1.1 shows the capacitor connected to a voltage (V) [11].

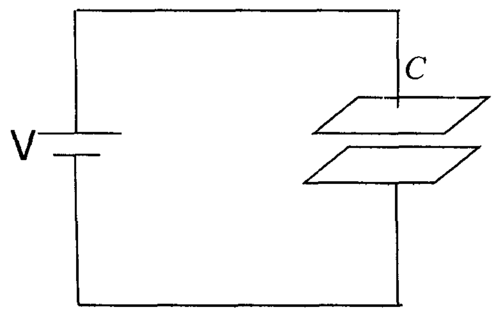

Figure 1.1 A capacitor connected to a voltage source V [11]

The energy stored in a capacitor (U_c) is

$$U_C = \frac{1}{2}CV^2 , \tag{1.2}$$

Where C is capacitance and V is the voltage applied.

The charge stored in a capacitor (Q_c) is

$$Q_c = CV . \tag{1.3}$$

Applying a derivative with respect to Cin Eq. 1.2, with voltage as a constant, obtains

$$dU_C = \frac{1}{2}V^2 dC . \tag{1.4}$$

The change in the charge stored in a capacitor is given by

$$dQ_C = VdC. \tag{1.5}$$

This charge is due to the voltage supply (Q_v), hence,

$$dQ_V = -dQ_C \quad . \tag{1.6}$$

The energy stored in the voltage supply changes by

$$dU_V = VdQ_v = -VdQ_C . \tag{1.7}$$

Hence, the total change in the stored energy is given by

$$dU_e = dU_C + dU_V = -\frac{1}{2}V^2 dC . \tag{1.8}$$

The force acting on the capacitor (F_e) is obtained by

$$F_e = \frac{dU_e}{dx} = \frac{1}{2}V^2 \frac{dC}{dx} . \tag{1.9}$$

From Equation 1.9 it can be inferred that the force is proportional to V^2, which means the force is independent of the polarity of the applied voltage. The force is in the direction of an increase in capacitance.

The most common capacitive resonators are the parallel plate and comb drives. A tuning fork resonator was used to exemplify the usage of porous silicon, in obtaining the cavity, and its use as a getter. This resonator uses differential capacitance detection of MEMS resonators. Chapter 6 deals with the results obtained with these resonators.

1.2. Motivation for the Dissertation

Many MEMS devices need vacuum to obtain a higher quality factor (Q). At atmospheric pressures, the air damping becomes prominent, hence lowering quality factor. In addition to the vacuum, the devices need to be encapsulated in order to avoid any particle contamination which can cause problems in MEMS sensing devices. Single crystal silicon (SCS) wafers are common in research and industry to fabricate MEMS devices. The SCS wafers need several deposition, lithography and etching steps to form a MEMS device. Also, these devices impose high parasitic capacitances. The use of silicon on insulator (SOI) wafers has addressed these issues to a greater extent: often times, one etch cycle followed by the lithography step is sufficient to define the movable structures. The buried oxide between the device side and the substrate offers electrical insulation between these two layers. As this separation is less than 2 μm, the parasitic capacitance from the device layer to the substrate is still possible. A small gap between the device side and the substrate results in a small packaging volume and poses a stiction problem between the MEMS device layer and the substrate. Both of these issues can be addressed to an extent by increasing the gap between the substrate and the device side. In Section 1.4, the technique that has been in use is discussed along with the drawbacks.

This dissertation presents an alternative technique that is easier to implement than prior methods. When the devices are anodically bonded, the pressure in the packaged device increases over a period of time because of the evolving gases, primarily oxygen. In order to counter this problem, getter materials are used. SAES getters are one of the commercial getter providers. In Section 1.7 the drawbacks of these getters are presented. This dissertation offers porous silicon as an alternative getter material. In the sections below, a literature review on MEMS resonators, SCS and SOI wafers, MEMS packaging techniques and getters is provided.

1.3. Resonators

MEMS resonators have been a subject of research for at least 40 years. The work of Nathanson et al. [12] on the resonant gate transistor is the oldest reported MEMS resonator. The reason that the MEMS resonators still remain the topic of research even today is the huge potential it possesses for frequency applications. The use of a MEMS resonator as the timing element has a long experimental history and huge progress has been made in this direction. In order for Si resonators to be used as oscillators, the resonant frequency should remain constant at all times and for all conditions. The main problems that Si resonators have in replacing the quartz resonators are the issues with packaging and the temperature dependency of silicon, causing the change in the resonant frequency. MEMS resonators need to be packaged in order to keep the dust particles away from the resonating structure. A detailed review of the literature on the packaging of MEMS devices is provided in the sections to follow. The temperature coefficient of silicon gives rise to a frequency error of ~30 ppm/C. This makes silicon unsuited for use as a timing element. Several techniques have been experimented on to compensate for the temperature effects of silicon. In the work presented here, a study is made on how porous silicon getter materials would benefit in compensating their effects of temperature.

Micromechanical resonators are used in many emerging high volume MEMS products. Gyroscopes [13] and reference oscillators [3, 4] have been successfully commercialized. Other applications include accelerometers [14], mass sensors [2], electrometers [15], temperature sensors [16], chemical sensors [1] and RF filters [17]. These applications benefit from high quality factors and low parasitic capacitances that are challenging due to the very small package size.

In this dissertation tuning fork resonators were used to exemplify the benefits of porous silicon in improving quality factor. The tuning fork has been used as the moving structure in oscillators [18], accelerometers [19], and gyroscopes [20]. This resonator design offers better isolation and capacitive readout of the movement of the tines.

1.4. SCS and SOI Wafers

Resonators have been fabricated in the single crystal silicon (SCS) or the silicon on insulator (SOI) wafers with resonant frequencies ranging from tens of kHz to MHz and GHz. When compared to polycrystalline silicon, SCS has a high mechanical quality factor, low internal stress, and it remains independent of other process parameters [21]. Siavash et al. [22] presented the results from a clamped-clamped beam and disk resonator. The spacing between the resonating structure and the electrodes was 90 nm. The beam was shown to resonate at 37.4 MHz and the disc resonators fabricated with a diameter of 29.5 μm and 50 μm were shown to resonate at 148 MHz and 87 MHz. These resonators were fabricated for operating frequencies in the HF (3-30 MHZ) and VHF (30-300 MHz) ranges.

SOI wafers offer many advantages compared to SCS wafers. First, the buffered oxide provides the electrical isolation between the device side and the substrate. Second, with the use of dry etching techniques, high aspect ratio devices can be fabricated with precision. Third, the transduction gaps can be obtained to their true physical limits. Grogg et al. [23] fabricated resonators that were defined on wafers of different thicknesses. It was shown that with varying thicknesses the resonant frequency changes significantly. Using the combination of UV-lithography and focused ion beam (FIB) milling, a transduction gap of 100 nm was obtained. The device side thicknesses of 350 nm and 1.5 μm were experimented on to evaluate the possibilities of future complimentary metal-oxide-semiconductor CMOS integration.

SOI wafers provide better process control and performance. In these wafers, the thickness of the buried oxide is the only separation between the device side and the substrate. This causes the problem of parasitic capacitance between the device side and the substrate. Also, this small separation poses the problem of stiction in the MEMS devices. In order to abate these problems, the cavities in the substrate have been effective. The cavity would increase the distance between the device side and the substrate and hence decrease the parasitic capacitance. Also, the increase in this distance helps in countering the problem of stiction. In a collaborative research effort of UC Berkeley and Stanford University, Noworolski et al. obtained etched cavities in the substrate wafer before bonding the structural and substrate wafers together [24]. In this method, thermal oxide is grown on the substrate wafer and patterned in order to etch the wafer to produce cavities. This wafer is then fusion bonded with the structural wafer which results in an SOI wafer with cavities in the substrate at the desired locations. This method has the following disadvantages: Firstly, a regular SOI wafer cannot be used. Secondly, the cavity size is limited by the structural rigidity, and lastly the device mask needs to be aligned with the buried cavity. Luoto et al. [25] has demonstrated MEMS on cavity-SOI. The process that was used was the same as that of Noworolski et al. [24]. The handle wafer with cavity and support pillars for MEMS structures was directly bonded to the device side. The results obtained show the misalignment between the handle wafer and the cap wafer. The misalignment was discussed to be a result of the double sided lithography of the handle wafer and the alignment mark transfer on the front surface. This misalignment led to displacements in the structures on the device side and the pillars in the substrate. This clearly shows the intricacies of pre-etched cavities in the substrate of SOI. As an alternate, this dissertation offers an electrochemical etching process to obtain cavities in commercial SOI wafers that neither needs a mask nor alignment.

1.5. Air Damping

Air damping is one of the factors that reduce the quality factor of the MEMS resonators. The air film that is trapped between the bottom of the resonating structure and the substrate damps the resonator, and hence decreases the quality factor of the resonator. The effect of damping is dependent on the thickness of this air film. The thicker it is, the less damped is the resonator, and the lesser the effect on the quality factor of the resonator. Several models have been presented to study the effect of air damping. The experimental results in [26] show the dependence of the quality factor to the gap between the resonating structure and the substrate. In this experiment two sets of similar resonators were fabricated in the experiments. One was in plane, parallel to the substrate and the other a self elevated resonator out of the plane of the substrate with a bimorph. The gap between the out of plane resonator and substrate was varied from 6 μm to 65 μm using the temperature, and the quality factor was noted. It was shown that with the increase in the gap the quality factor had increased. Theoretical models 1D [27] and 3D [28] have been proposed to study the effect of air damping. Although the 3D model proposed was in close agreement with the experimental results, the 1D model still provided an estimation of the quality factor dependence on the air damping. These theoretical models are based on the assumption of atmospheric pressures. The simulation of micro beam resonators resonating at low vacuum has also been presented [29-32]. In reference [33], a study of these models with their limitation is presented. A molecular dynamic simulation of the resonator in a low vacuum, and the effect of oscillating frequency and amplitude on the quality factor are presented.

The quality factor of the MEMS devices increases with the decrease in the pressure. The study made by Li et al. [34] show that the quality factor of MEMS devices is also dependent on the gas ambience. It is shown that a gas with low molecular weight has a higher quality factor than the high molecular weight gas. The MEMS resonator was tested with He, N_2 and CO_2 ambience. The experiments reveal that a MEMS resonator under He ambience has a better quality factor than a resonator in CO_2 ambience at the same pressures. Hence, with the low molecular weight gas, the need for external low pressure is excluded.

The experiments conducted in this dissertation used air ambience. The cavity is introduced to increase the distance between the device side and the substrate and limits the effect of air damping.

1.6. Packaging

The operation of MEMS devices in a vacuum improves their performance [35]. The vacuum helps in reducing the viscous and squeeze film damping effects and hence increases the quality factor [36]. Encapsulation of MEMS devices provides several benefits. It prevents the MEMS structures from being exposed to the external environment and provides the needed vacuum to the system. As the typical mass of the resonating structure is in the order of 10^{-9} to 10^{-13} kg, any micro/nano sized dust particle could significantly increase the mass and cause a major drift in the frequency [36]. Several encapsulation techniques have been discussed in [37], such as anodic, fusion, eutectic, solder, adhesive, and glass frit. Of these, anodic bonding has been seen to provide clean environments for some resonator types such as plate, beam and piston to operate and help in the applications, such as the oscillators [38]. Commercially available

Bosch airbag and yaw rate sensors are examples of mass produced wafer bonded devices [39]. Hermetic encapsulation is needed in different devices, such as accelerometers [40], radio frequency (RF) switches for controlled atmospheric damping, sensitive gears and gyroscopes for moisture control of drag and friction, IR MEMS for vacuum insulation [41].

Verheijden et al. demonstrated the use of HF permeable PECVD SIOC capping layer in wafer level encapsulation of MEMS devices [42]. Black diamond (BD), a low-k material, was used as the permeable layer, which is porous as deposited and also an insulator itself. The encapsulation was based on the deposition of the layers of the MEMS devices that seal the surface of the movable structures. The release of the movable structure was performed after the deposition of the encapsulation layer. Hydrogen Fluoride (HF) vapors permeate through the BD layer to etch the SiO_2 under the movable structures. The devices performed three times better at lower pressures. There are two drawbacks in this method. First, the process involves more than one layer deposition. Second, the devices cannot be used at atmospheric pressure.

Monajemi et al. demonstrated a low cost wafer level MEMS packaging technology which does not use the traditional wafer bonding to package the devices [43]. A sacrificial material was deposited through a polymer overcoat cap using the thermal decomposition process. The end component was hermetically sealed using the Al coating over the deposited cap. The pressure inside the encapsulated samples depends on the pressure in the chamber used for coating. Hence, it is difficult to obtain very low pressures in the sealed sample.

Apart from the above mentioned researchers, there are a few more who have suggested different ways of bonding MEMS devices. Y. C. Lee [44] presented three cases for MEMS and their packaging to advance the integration of MEMS devices to microelectronic, optoelectronic, and microwave devices. First, packaging for MEMS, that provide flexible circuits for MEMS, second, packaging of MEMS, that deals with wafer level packaging and integration with flip-chip assembly, third, MEMS for packaging, that deals with the active alignment for optoelectronic packaging. Duck-Jung Lee et al. [45], from the Material and Device Research Center in Korea, hermetically packaged the Field emission display (FED) panel glass with another glass wafer using interlayer of amorphous silicon. The combination of anodic bonding and emission characteristic of FED was used in this packaging. The different bonding techniques presented by far present the potential and scope of MEMS bonding.

Anodic bonding is a very common wafer bonding technique. Vacuum anodic wafer bonding is done by first lowering the pressure of the chamber, followed by heating the wafer, and applying a high voltage to bond the wafers. There are some problems encountered at different stages for different samples getting bonded. A. P. Malshe et al. [46], in collaboration with Sandia National Laboratories presented the challenges encountered in packaging the MEMS devices, and solutions for few of those challenges. In their paper they suggest some viable techniques to provide solutions to problems in releasing and stiction, dicing contamination, out gassing, die handling and stress on dies while bonding. Likewise, Blasquez et al. [47] in their paper suggest the solution for the problems in bonding silicon and glass in partial vacuum conditions. Their suggestions of time, pressure and voltages for bonding were applied in this research. In this dissertation the anodic bonding technique was used to bond glass to silicon in vacuum.

1.7. Getters

The main challenge in MEMS encapsulation is maintaining low pressure. In order for MEMS devices to operate at the fabricated resonant frequency after anodic bonding, the possible drift in the frequency from the emerging gases needs to be controlled. This is due to the small packaging volume that gets easily filled up by outgassing. The formation of a cavity in the substrate or cover helps in increasing the volume to surface ratio. Introducing the getter material either in the cup or cap wafers is another common technique to counter this problem.

Getters are widely used to lower the effect of out gassing and maintain the required vacuum needed. The beneficial effects of getter material for MEMS resonators have been studied and experimented before [41, 48]. Moraja et al. [41] in their paper presented a method to pattern the getter film named as High Porosity Thick Film (HPTF). The authors talk about the use of patterned getters on both the cap and cup wafers. The conventional method of using the getter films in ceramic and metallic packages has been discussed which uses a mixture of Ti and Zr getter alloys, deposited on the metallic substrates. The getter has high porosity that absorbs H_2O, O_2, CO, CO_2, H_2, and N_2. The paper shows the stability over time of the vacuum bonded MEMS devices that has getter layers integrated in the bonding process. The drawbacks of this approach are: 1.) an external layer needs to be introduced, 2.) it needs a mask to be aligned and patterned.

1.8. The Approach

The problems encountered in the fabrication of SOI wafers due to the small thickness of the oxide layer that separates the device layer from the substrate layer have been observed. It was discussed that the cavity in the substrate would increase the distance between the device and substrate layer and hence decrease the parasitic capacitance and air damping, and thereby increase the quality factor. In this effort, the use of an electrochemical etching process of silicon to obtain cavity in the substrate is presented. This is a self aligned, mask-less electrochemical etching process to etch cavities in the substrate of commercially available SOI wafers. Using the same technology, after the cavity is introduced, a layer of porous silicon getter was augmented in the substrate. This porous silicon getter needs no mask, is self aligned, and can capture the oxygen gas by readily forming silicon dioxide. Unlike other commercially available getters, this getter needs no activation temperature and no external material is introduced. The results obtained from these devices are presented in Chapter 6, which indicate that the device with the getter would perform two times better than the device without the getter.

1.9. Research Goals

This dissertation aims at obtaining better results from the SOI resonators that are now used in various applications as previously discussed. The following are the research goals that were met in the order they are listed:

- confirming the use of porous silicon to obtain a cavity in the substrate of SOI devices and its use as a getter material for encapsulated MEMS devices,
- comparison of quality factors of devices with only a cavity and cavity plus porous silicon, and
- suggestions on avoiding the reaction of the device side of SOI for P and N type silicon.

CHAPTER 2

FABRICATION OF MEMS

In this chapter, the designs and the fabrication steps of the beam resonators used in the dissertation are presented. The mathematical calculations used to calculate the resonant frequency are also presented

2.1. Generation 1 Resonators

Different resonator types (plate, comb drives and beam resonators) were fabricated in the generation 1 resonators. Figure 2.1 presents the microscopic image of these resonators. Among these, the beam resonators were chosen to exemplify the benefits of porous silicon because: 1) they are rugged structures with simple design 2) lateral movement involves capacitive sensing that provides excellent readouts.

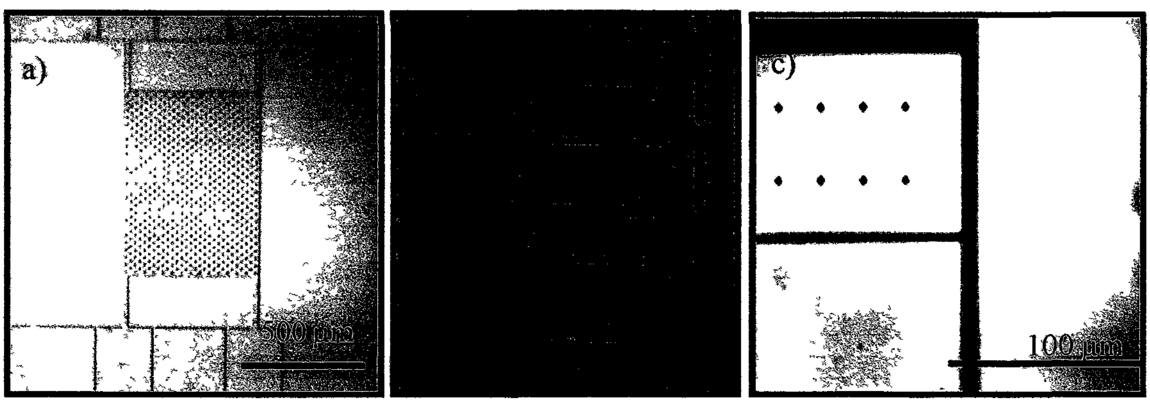

Figure 2.1 a) Plate resonator, b) Comb drive resonators, and c) Beam resonators

The design and the mask used for the beam resonators are shown in Figure 2.2. The Design A resonators use a differential capacitive sensing readout, and Design B uses a single ended capacitive sensing readout. The benefits of the Design B beam resonator are:

1) the wide etched space (the red area in Figure 2.2 (b)) in the device side exposes the substrate layer, and helps in the microscopic evaluation of the porous silicon formed,
2) this design helps in releasing the stuck MEMS devices:

   After the resonators were processed, CO_2 supercritical drying was used to release the devices. Some devices encountered stiction problems. The Design A beam resonator experienced stiction between the drive and sensing electrodes. The Design B resonators would get stuck either to the substrate or to the sensing block. In order to release the devices from stiction, ultrasonic treatment was used. The devices were kept in a glass tube filled with ethanol and stirred in the sonicator. The Design B resonators were more successfully recovered from stiction as compared to Design A. The reason was the large etched area in the device side allowed ethanol to move between the stuck surfaces and release them.

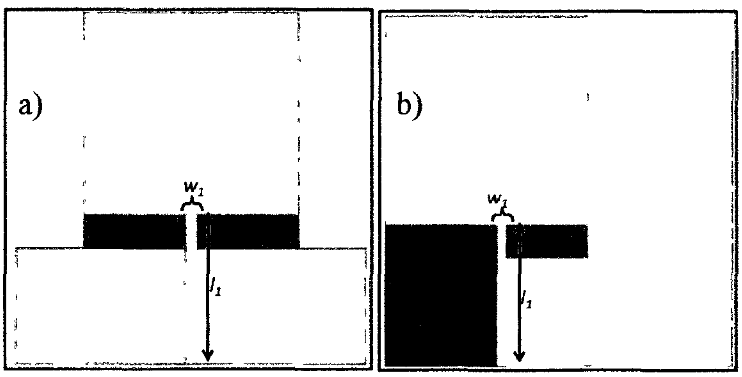

Figure 2.2 Beam resonators: a) Design A, and b) Design B

2.2. Calculation of Resonant Frequency

The dimensions of the resonating beam structure for both the designs in Generation 1 were kept the same (Figure 2.2). The length of the beam is $l_1 = 1500$ μm, width is $w_1 = 100$ μm, thickness $h_1 = 10$ μm. The Young's Modulus of the silicon (100 orientation) is $E = 130$ GPa, and the density is $\rho = 2330$ kg/m^3.

The moment of inertia is given by

$$I_1 = \frac{h_1 w_1^3}{12}, \tag{2.1}$$

and is calculated to be $I_1 = 8.33\times10^{-19}$ m^4.

The spring constant is given by

$$k_1 = \frac{12EI_1}{L_1^3}, \tag{2.2}$$

and is calculated to be $k_1 = 385$ N/m.

The mass of the resonating beam is given by

$$m_1 = \rho \times V, \tag{2.3}$$

and is calculated to be $m_1 = 3.5$ nkg.

The resonant frequency is given by

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k_1}{m_1}}, \tag{2.4}$$

and is calculated to be $f_0 = 52.83$ kHz.

The actual resonant frequency was measured to be 57 kHz, as presented in Chapter 6. The difference in the resonant frequency was due to the limitations in lithography (intensity of light, exposure and developing time) that caused changes in the device dimensions.

2.3. Generation 2 Beam Resonator

The second generation resonator was modified into a tuning fork resonator. This design is used in the gyroscopes. Figure 2.3 shows the design of the resonator. The green color is the mask for the contact pads. This design uses front side electrical probing for testing the resonator. Hence, no additional wire bonding process was needed for testing the uncapped resonators in vacuum, unlike the Generation 1 resonators.

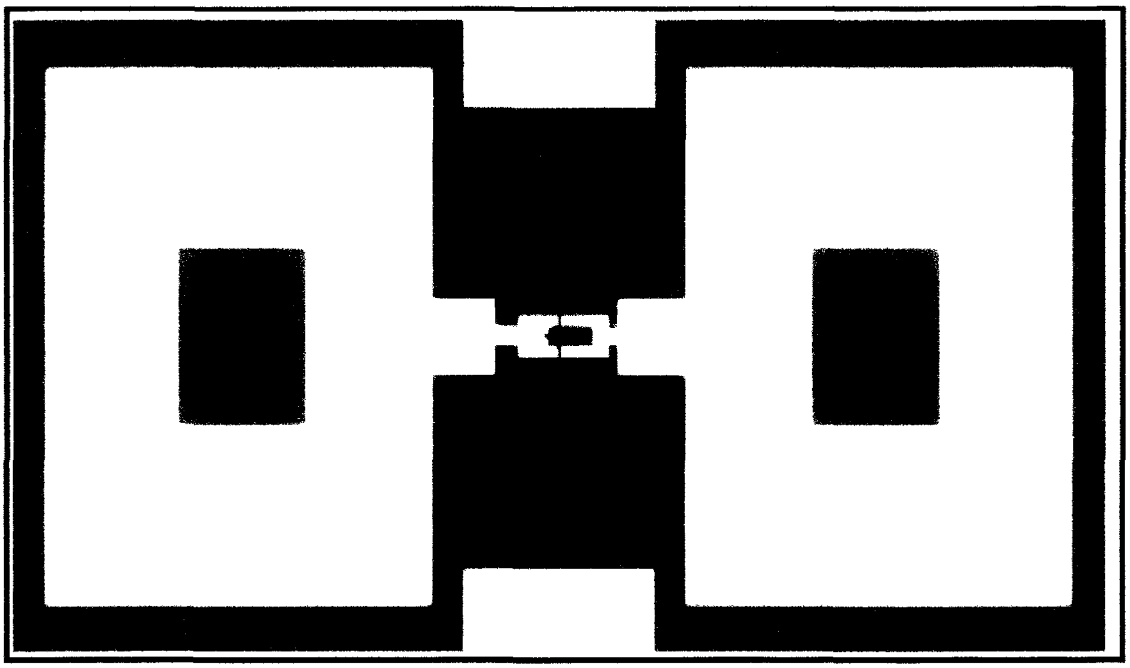

Figure 2.3 Generation 2 fabricated beams

2.4. Fabrication of Generation 2 Beam Resonator

The fabrication process of the tuning fork resonator is shown in Figure 2.4; 100 mm diameter SOI wafers were used for the process.

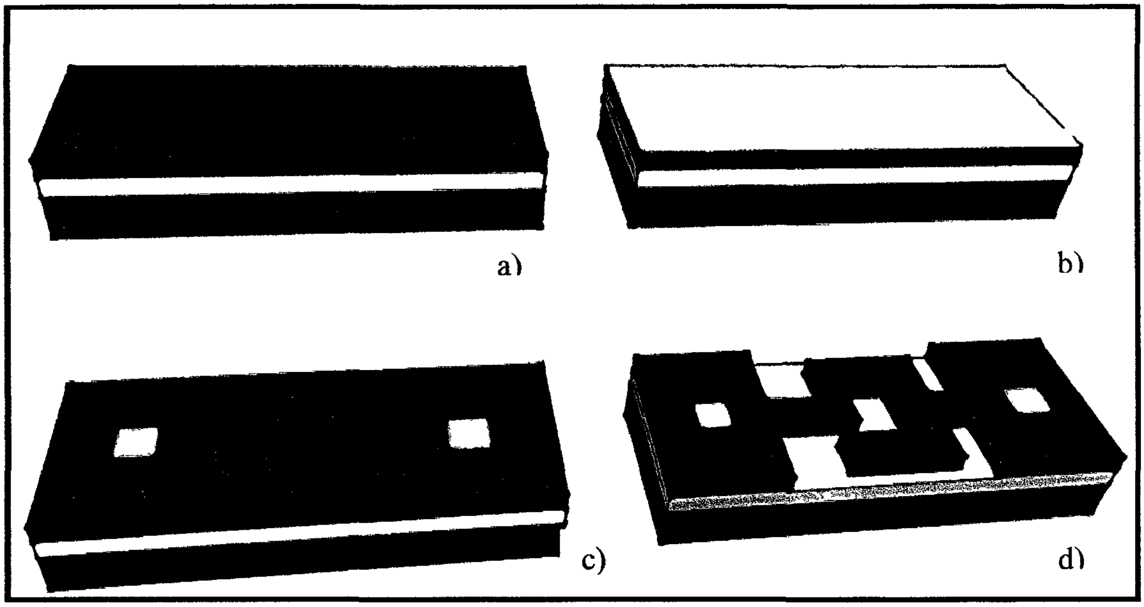

Figure 2.4 Process flow a) SOI wafer, b) Cr/Au deposition, c) Cr/Au patterned for the contact pads, and d) ICP etching on the device side to open the structural layer

The device side has a thickness of 10 μm and resistivity of 0.001 - 0.01 ohm·cm. The substrate layer is 500 μm thick and resistivity of 0.01 - 0.02 ohm·cm. After the wafers were etched in buffered oxide etch (BOE) (Figure 2.4 (a)) to remove native oxide, 10 Å chrome and 100 nm of gold was deposited on the wafer for the contact electrodes (Figure 2.4 (b)). Figure 2.4 (c) shows the gold layer patterned and etched to define the contact pads. The device side was then patterned and etched using inductive coupled plasma etching (ICP), as shown in Figure 2.4 (d). The tines of the tuning fork are perforated with holes of 3 μm diameter to provide faster and uniform oxide etches). Finally the wafers were diced. An SEM image of the resonator structure is shown in Figure 2.5 together with the device dimensions. This design of the resonator had a wide open area that helps in increasing the volume to surface ratio in packaged devices.

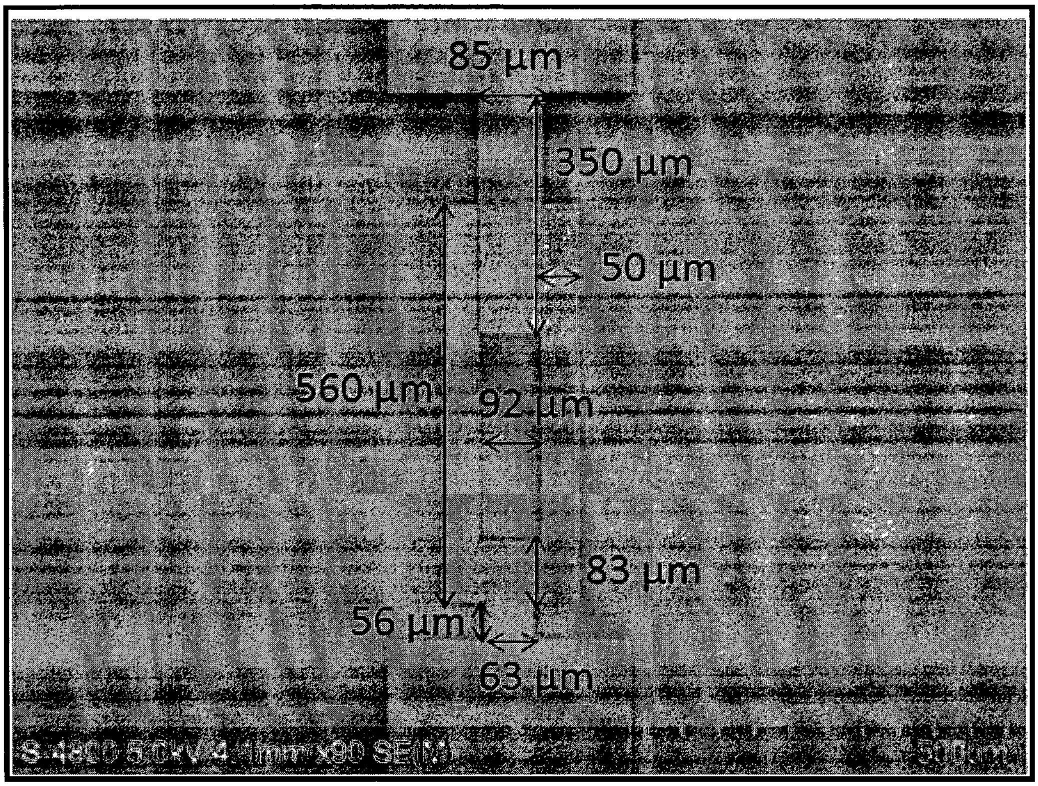

Figure 2.5 The dimensions of the tuning fork

2.5. Calculation of Resonant Frequency

The tuning fork can be divided into three sections as shown in Figure 2.6. Sections 1 and 3 are symmetric with Section 2 that connects the tuning fork to the electrode. Sections 1 and 3 are dimensionally equal. Hence, Section 1 is considered for the calculations.

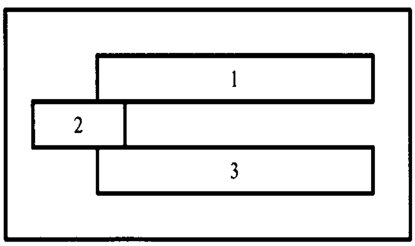

Figure 2.6 Sections in the tuning fork

Section 1:

The spring constant and mass for Section 1 was first calculated. The length of the beam is $l_1 = 560$ µm, width is $w_1 = 50$ µm, thickness $h_1 = 10$ µm. The Young's modulus of the silicon (100 orientation) is $E = 130$ GPa, and the density is $\rho = 2330$ kg/m^3. Using Equation (2.1) the Moment of inertia is calculated to be $I_1 = 1.04\times10^{-19}$ m^4. The spring constant according to Equation (2.2) is $k_1 = 0.9$ kN/m. The mass of the resonating beam according to Equation (2.3) is calculated to be $m_1 = 0.65$ nkg.

Section 2:

The length of this connecting block is $l_2 = 140$ µm, width is $w_2 = 63$ µm, thickness $h_2 = 10$ µm. The Young's modulus of the silicon is $E = 130$ GPa, and the density is $\rho = 2330$ kg/m^3.

Using Equation (2.1) the moment of Inertia is calculated to be, $I_2 = 1.04\times10^{-19}$ m^4. The spring constant according to Equation (2.2) is $k_2 = 118.5$ kN/m.

Comparing the spring constants k_1 and k_2, it can be seen that the latter is much stiffer than the former. Hence, the resonant frequency of the tuning fork is dependent on the tines of the tuning fork (Sections 1 and 3).

The resonant frequency is given by

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k_1}{m_1}} = 226 \text{ kHz.} \tag{2.5}$$

2.6. Probing Comparison between Generation 1 and 2 Beam Resonators

The probing mechanism for the Generations 1 and 2 beam resonators is as shown in Figure 2.7. The device side, buried oxide and the substrate along with the vias and contacts pads are shown.

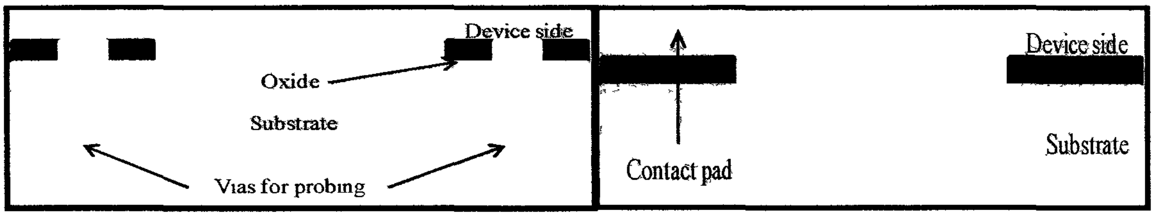

Figure 2.7 Comparison of probing for generation 1(left) and generation 2 (right)

As the Generation 1 beam resonators used back side probing, these resonators needed to be bonded to glass for testing. Bonding to glass would provide necessary back side support and the probes will not pierce the device side surface. To test the uncapped devices, they needed to be wire bonded on the surfboards and tested. As these devices needed several steps before they could be tested, a new design of a resonator was needed that can eliminate the problem of: 1) stiction between the electrodes, 2) electrical probing; and be a lot simpler in fabrication and processing. Hence, the Generation 2 design of a resonator was developed. For these resonators it was possible to test the uncapped devices in vacuum prior to encapsulation and study the response. The devices were then permanently sealed with glass bonding.

2.7. Outline of Experiments

The general outline of the experiments in this dissertation is presented in the Figure 2.8. Two types of devices, one with just the cavity in the substrate and the other with a cavity and porous getter were fabricated and compared for quality factor. The experimental process and the results obtained are discussed in Chapters 3-7.

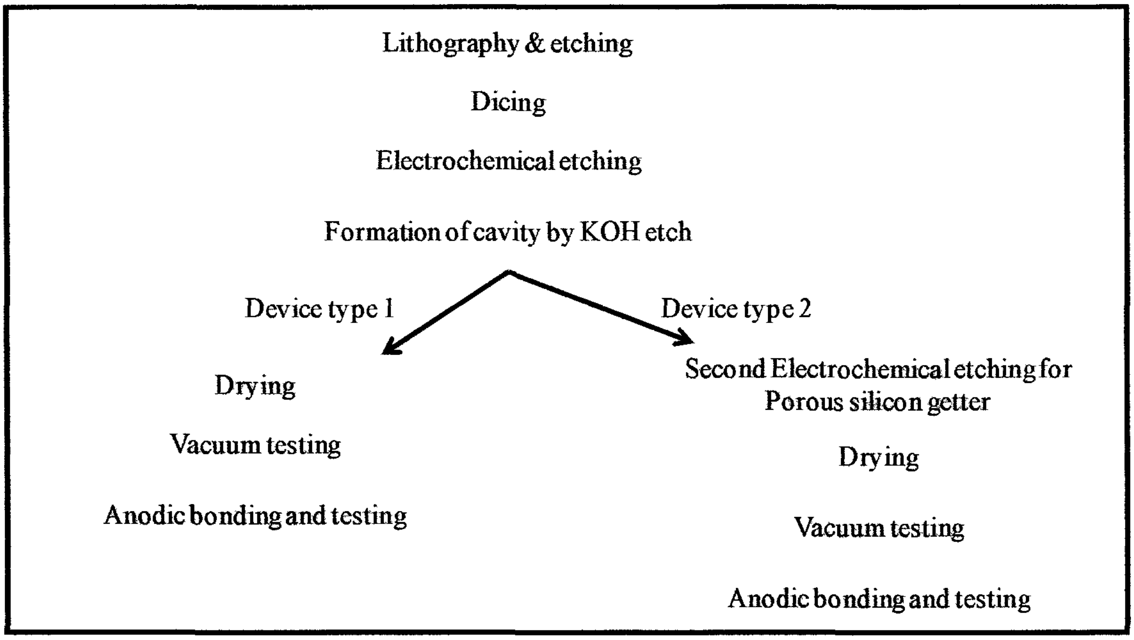

Figure 2.8 Outline of experiments

2.8. Summary

The design of the resonators used in this dissertation, along with the analytical calculations for resonant frequency, were shown in this chapter. A general outline of device types and a brief experimental procedure were also presented.

CHAPTER 3

POROUS SILICON

Electrochemical etching of silicon generates porous silicon. Depending on the concentration of Hydrofluoric Acid (HF), current density and etching time, the thickness and the porosity of porous silicon can be varied. This dissertation deals with the use of porous silicon as a sacrificial material to generate a cavity in the substrate of the SOI dies and its use as a getter material for encapsulated MEMS devices. Thicker porous silicon layers are needed in order to get thick cavities in the substrate when etched by KOH, and also to get a thick porous silicon getter. In this chapter, the porous silicon formation techniques are discussed along with the experiments conducted in the dissertation. The results of the devices obtained are presented. The solutions to the problems encountered in the porous silicon formation are also discussed.

3.1. Background on Porous Silicon

Porous silicon was discovered by Uhlir at Bell Laboratories in 1956 [49]. He was conducting an experiment on the electropolishing of silicon and discovered a porous layer on the silicon surface that was non soluble in an HF solution. The resulting material was named porous silicon. Following this discovery, many research groups started to experiment with the porous silicon formation mechanisms and its possible applications. Porous silicon is used in spectroscopic studies as a model of the crystalline silicon surface [50, 51] as an intermediate layer to form thick oxides on silicon to help make the SOI wafers [52], and as a dielectric material in capacitive based chemical sensors [53]. The porous silicon formation mechanism is explained by the current density vs. voltage curve in Figure 3.1 [54]. The porous silicon formation takes place until the current density J_{ep} is reached. Beyond this point, electro-polishing is observed. An important thing to observe is that the formation of porous silicon is a combination of electrical and chemical etching processes. Hence, when these two processes are balanced, a porous layer is formed. With an increase in voltage (electrical part) as indicated in Figure 3.1, the electro-polishing is observed.

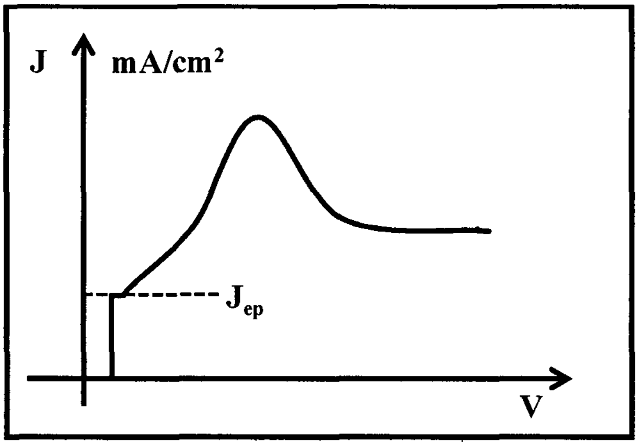

Figure 3.1 Current density vs. Voltage [54]

Various models have been proposed to explain the porous silicon formation. Beales model, diffusion limited model, and the quantum model are among the noted models proposed. The widely accepted phenomenon of the porous silicon formation process is as follows:

1) the application of voltage between the substrate of the SOI wafer (the anode) and the Pt electrode (the cathode) in the HF medium causes displacements in the valence and conduction bands of silicon,
2) these displacements lead to the movement of the holes from the silicon crystal to the Si-HF interface. This weakens the Si-Si bonds and lets F^- ions attack the Si surface. The removal of holes from the silicon surface causes pores to form on the surface,
3) with the passage of time, as more and more holes move to the Si-HF interface from the silicon crystal, the layer of porous silicon gets thicker and thicker.

The chemical reactions that govern the porous silicon formation, as found in the literature [55] are

$$Si + 2HF + 2H \rightarrow SiF_2 + 4H^+, \tag{3.1}$$

$$SiF_2 + 2H_2O \rightarrow SiO + 2HF + H_2 + O^-, \tag{3.2}$$

$$SiO + 6HF \rightarrow H_2SiF_6 + 2H_2O. \tag{3.3}$$

The Si molecules react with the HF medium to form silicon di-fluoride. This reacts with water to form silicon mono-oxide and HF. SiO reacts with HF to form H_2SiF_6 leaving behind the pores in the Si.

There are three experimental setups that are generally used to form porous silicon. First, the traditional beaker system, second, the single tank cell, and third, the double tank cell are used as shown in Figure 3.2.

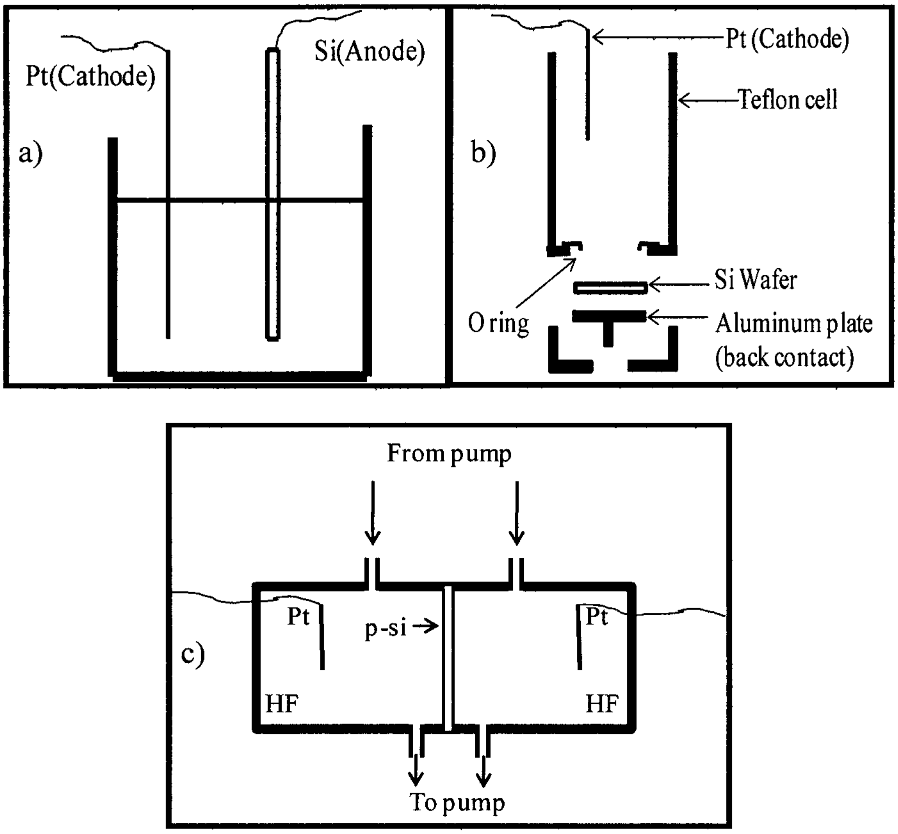

Figure 3.2 Experimental setups to form porous silicon a) traditional beaker system, b)single cell, and c) double cell [56]

In the first setup, the voltage is applied between the silicon wafer (anode) and the Pt electrode (cathode), as they are suspended in a beaker with HF as the medium. In the second setup, the wafer is sealed from the back side by an Al plate and O ring to expose only the portion of the Si wafer that is supposed to be made porous. In this kind of electrochemical etch setup, the back surface of the Si wafer is made electrically conductive which acts as an anode, and the cathode is the Pt electrode suspended in the cell. The third setup used is the double tank cell, in which the electrolyte is constantly pumped in the tank to keep away any bubble formation near the Silicon surface. The bubbles can block the current flow through the HF medium.

The porous silicon experiments were conducted in the following stages:

1) the SCS wafer was diced and each die was electrochemically etched using the traditional beaker etching setup,
2) after the optimized current density was established from former experiments, the SOI dies were processed to obtain porous silicon in the substrate. A single cell setup was used for these experiments.

3.2. Experiments with the SCS Dies

The SCS wafer was coated with a Cr/Au layer on the backside to provide electrical contact. The 32 AWG wire was soldered on the back side to provide necessary electrical connection. The backside was then coated with wax to prevent any reaction during the electrochemical etching process. Platinum mesh was used as the negative electrode and Si was the positive electrode during the process. A Keithley 2400 source meter was used to pass current through the die for the electrochemical etching. Various current densities were investigated at different time lengths. The schematic of the electrochemical etch setup is shown in Figure 3.3.

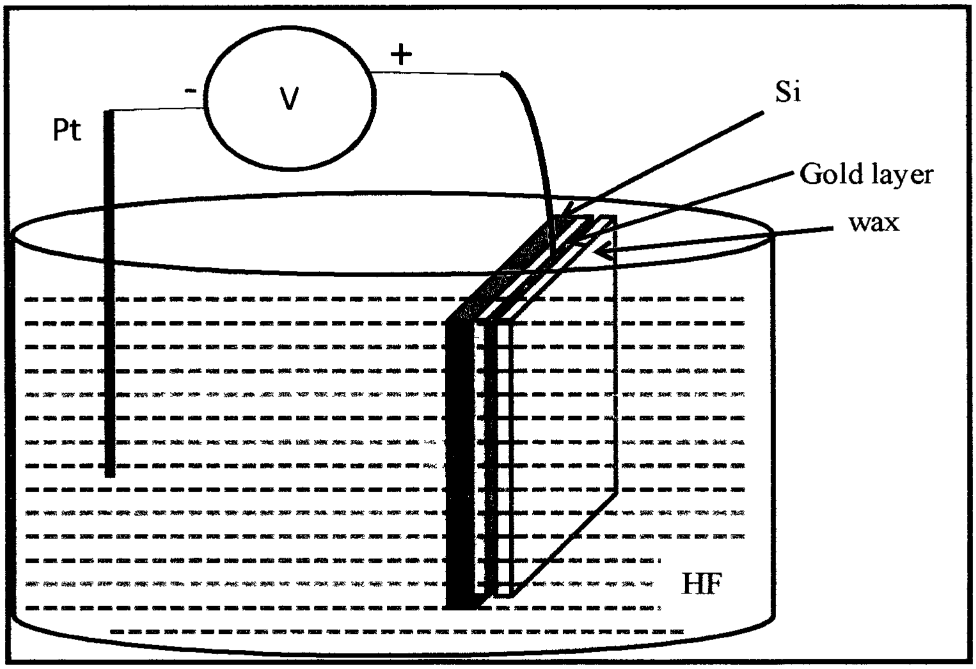

Figure 3.3 Electrochemical etching setup

An HF solution was used as the electrolyte. Porous silicon formation depends on the use of proper concentration of HF, the negative electrode, and the time for which the process is carried out [57]. Different current and time duration operations were carried out and finally a current density of 50 mA/cm^2, which gives the porosity of about 90%, [58] was adopted. This current density was chosen because the densely porous layer can quickly be etched in KOH. Experiments have proven that, if the time period of etching process was extended from 6 min to 90 min, thick layers of porous silicon can be obtained. The thick layers of porous silicon are needed: 1) to provide deep cavities in the substrate after being etched by KOH, and 2) to getter more gases in an encapsulated MEMS die. In the experiments conducted, it was seen that the samples exposed for 90 min of electrochemical etching led to cracks and were polished. In order to form the porous silicon layers, the experiments were alternated for low current and high current cycles. The low current forms a thin layer of porous silicon with less porosity, and then a high current cycle would harvest on this layer to form a highly porous layer. This alternation of current cycles eases the strain on the silicon die and prevents cracking. It was seen in the experiments that, with the alternation of current cycles, the porous layer formed on the surface of the substrate is clear and smooth.

The current density of the low current cycle was 10 mA/cm^2 and that of the high current cycle was 50 mA/cm^2. Several experiments were conducted at different time lengths for both low and high current densities. The table below shows several experiments conducted in a 10% HF solution. The LC and HC are the low current and high current cycles.

3.3. Summary of Electrochemical Etching Experiments Conducted

Several experiments were repeated with the same process parameters to authenticate the results on SCS dies. Table 3.1 presents the summary of these results.

Table 3.1 Summary of experiment conducted on samples

Sample #	Current (mA)	Time (min)	Remarks
1	2.5	6	Uniform porous layer
2	2.5	10	Uniform porous layer
3	2.5	20	Uniform and densely porous
4	5.0	20	Edges were polished but the surface was porous
5	10.0	20	Rough and polished surface with cracks
6	7.5	20	Rough surface, polishing starts here

7	6.5	20	Unpolished surface with cracks and rough edges
8	6.0	20	Uniform porous layer
9	6.0	30	Porous surface with cracks and polished edges
10	6.0	60	Polished surface
11	5.0	60	Rough and polished surface
12	5.0	30	$1/5^{th}$ of the surface was polished
13	5.0	45	Surface was completely polished

Deductions from Table 3.1:

1) Etching the sample for a moderately longer period of time with lower current densities increases the porosity of the porous silicon, but etching the device for a extremely longer period of time causes the surface to be polished.
2) Electropolishing of a sample starts from the edges and grows over the whole sample area.
3) Etching the sample with low current densities for a longer period of time or high current densities for a lesser period of time can both cause polishing.

The samples were then tested with alternation of low current and high current cycles of electrochemical etching to form thick porous silicon layers. Table 3.2 provides the summary of these experiments.

Table 3.2 Shows the different experiments conducted on the samples and the results obtained. The a's and b's in the bracket show the priority in which the current cycles were conducted

Sample #	Low current cycle		High current cycle		No of cycles each	Remarks
	I(mA)	T(min)	I(mA)	T (min)		
1	1.0(b)	15	5.0(a)	15	2	Surface was polished
2	1.0(a)	15	5.0(b)	15	3	Surface was porous with polished edges
3	1.0(a)	20	5.0(b)	15	6	Surface was highly porous and lost some layers of porous silicon in critical drying
4	1.0(a)	30	5.0(b)	15	6	Surface is uniformly etched but with cracks on the surface
5	1.0(a)	10	5.0(b)	7.5	6	Surface was porous and uniform
6	1.0(a)	10	7.5(b)	7.5	4	Surface is porous and uniform
7	1.0(a)	7.5	10.0(b)	4	22	Surface is densely porous with many fragile layers
8	1.0(a)	10	9.0(b)	3	15	Surface is densely porous with fragile layers
9	1.0(a)	10	8.5(b)	3	20	Surface is porous and robust
10	1.0(a)	10	9.0(b)	3	13	Surface is densely porous and soft

Deductions from Table 3.2:

1) the samples that were subjected first to a low current cycle and then to a high current cycle generated densely porous silicon and were less prone to polishing than the sample subjected to a high current cycle first and then a low current cycle,

2) it was also observed that it is possible to generate a densely porous silicon layer in comparison to the experiments tabulated in Table 3.1, but to be able to dry the sample and retain the layer was difficult even with the use of CO_2 critical point dryer (CPD).

3.4. Results Obtained by Electrochemical Etching on SCS Dies

Tables 3 1 and 3.2 showed the summary of results obtained on the SCS samples Figure 3.4 shows the sample with a current density of 42.5 mA/cm ^{2} . The surface of the sample is smooth and uniformly porous

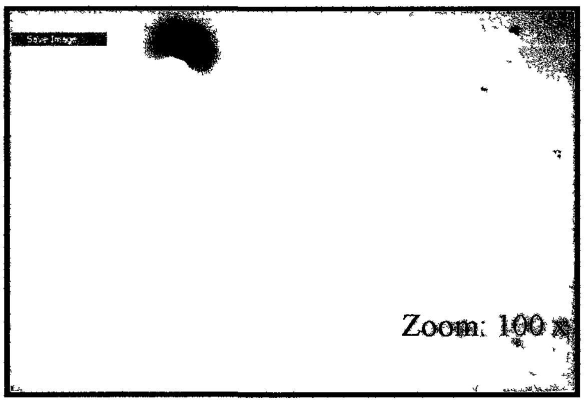

Figure 3.4 Surface of the sample with current density of 42.5 mA/cm ^{2}

Figure 3.5 shows the sample with a current density of 45 mA/cm ^{2} . The surface of the sample is uniform (Figure 3.5 (a)), and the edges show the signs of electro-polishing (Figure 3 5 (b)).

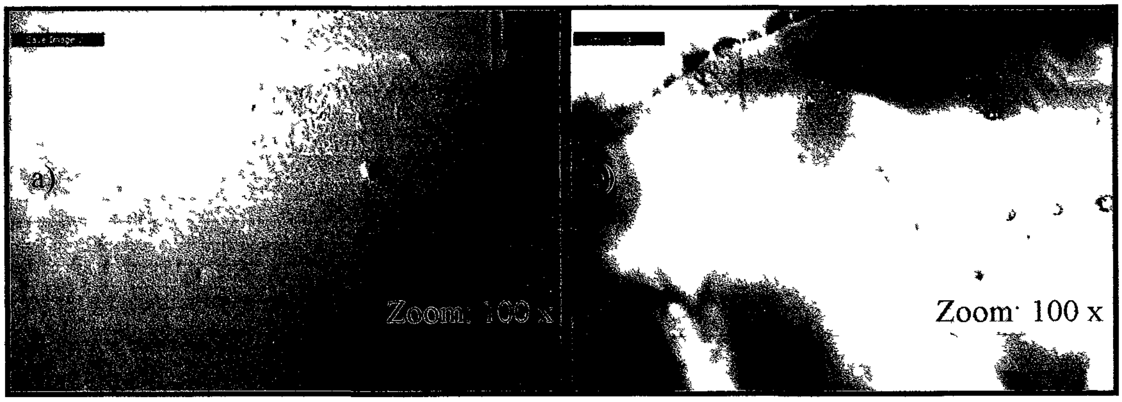

Figure 3 5 Sample with current density of 45 mA/cm^2 a) surface of the sample, and b) edges of the sample (100 x)

Figure 3 6 shows the sample with a current density of 50 mA/cm^2 The electro-polished surface of the sample is shown in Figure 3 6 (a). In Figure 3 6 (b) the edges of the sample show the layers of porous silicon peeling out after drying

Figure 3 6 Sample with a current density of 50 mA/cm ^{2} a) polished Si surface, and b) edges of the sample with porous silicon peeling out

Figure 3 7 shows the SEM image of an 80 µm thick porous silicon layer in the SCS die This sample was subjected to a current density of 10 mA/cm^2 for 45 min

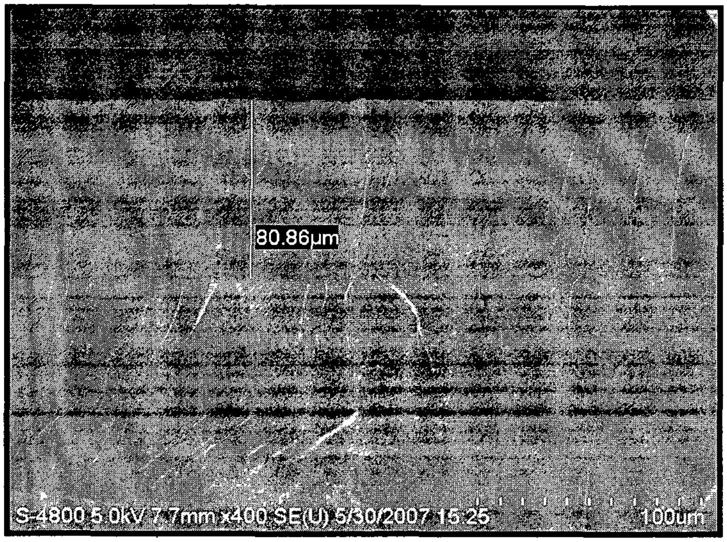

Figure 3.7 SEM image showing the porous silicon (80 µm) in the SCS die

After the experiments conducted on SCS dies, the optimized electrochemical etching parameters were deduced to be 10% HF, current density of 2-5 mA/cm^2 and time duration of the electrochemical etching process t = 20 min.

3.5. Electrochemical Etching of SOI Dies

The SOI dies were electrochemically etched using the one-sided etch jig, as shown in Figure 3.8. The sample was evaluated for different etching currents and time period. The substrate acts as the anode and the Pt wire acts as the cathode. The porous silicon is formed in the substrate of the SOI only in the area exposed to HF. Figure 3.8 indicates the area of porous silicon formation. The device side is insulated from the current flow by the buried oxide; hence, ideally it does not react to the etching process.

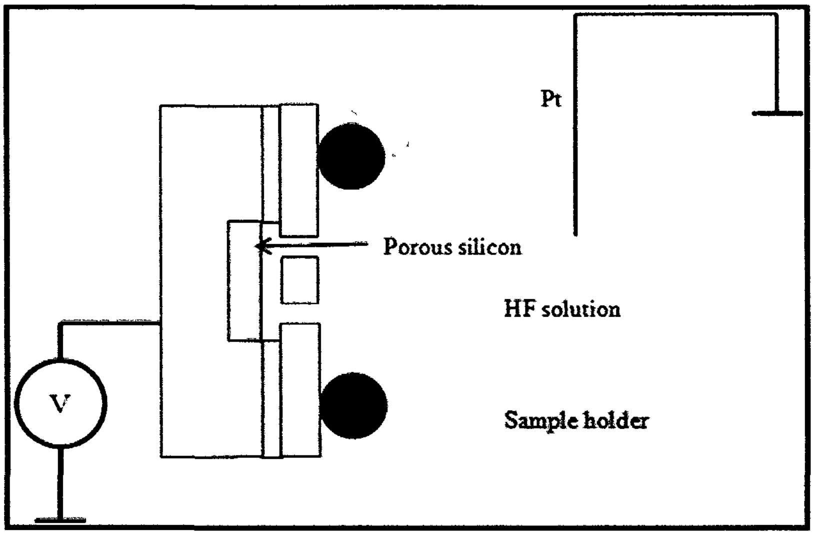

Figure 3.8 Electrochemical etch setup for SOI MEMS die

Figure 3.9 shows the SEM image of an SOI die before the electrochemical etching process. As indicated in Chapter 2, there were two designs in Generation 1. The area of the substrate that is exposed to HF, where the porous silicon can be formed in Design A is 6.3×10^{-7} m^2, and that in Design B is 2.5×10^{-7} m^2. The results presented in this chapter in the following sections are of the Generation 1 Design B beam resonators.

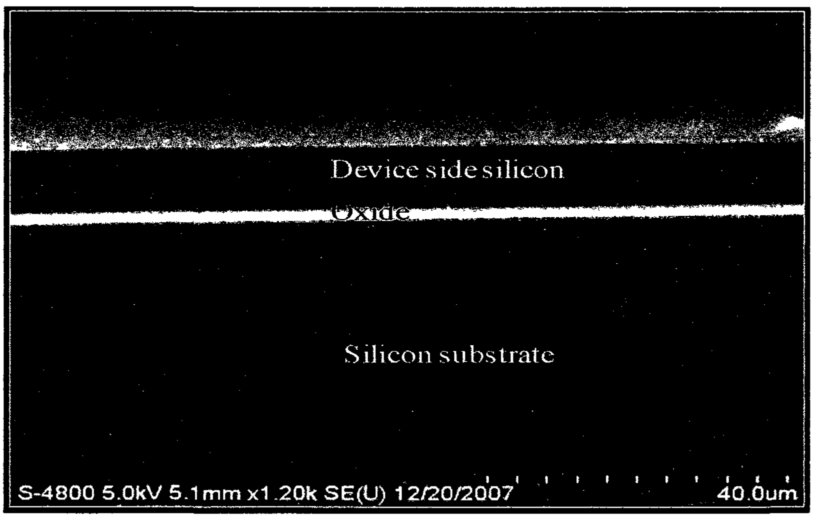

Figure 3.9 SEM image of SOI die

The Generation 1 Design B beam resonator, shown in Figure 3.10 was subjected to 0.52 mA of current (20 mA/cm^2) for 60 min. Figure 3.11 shows the microscopic image of the sample. The surface of the porous layer was uniform and densely porous.

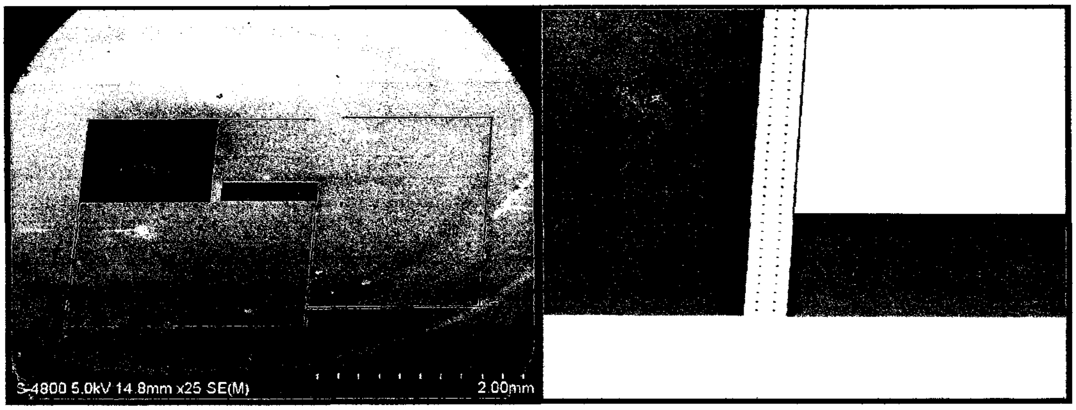

Figure 3.10 Generation 1 Design B beam resonator

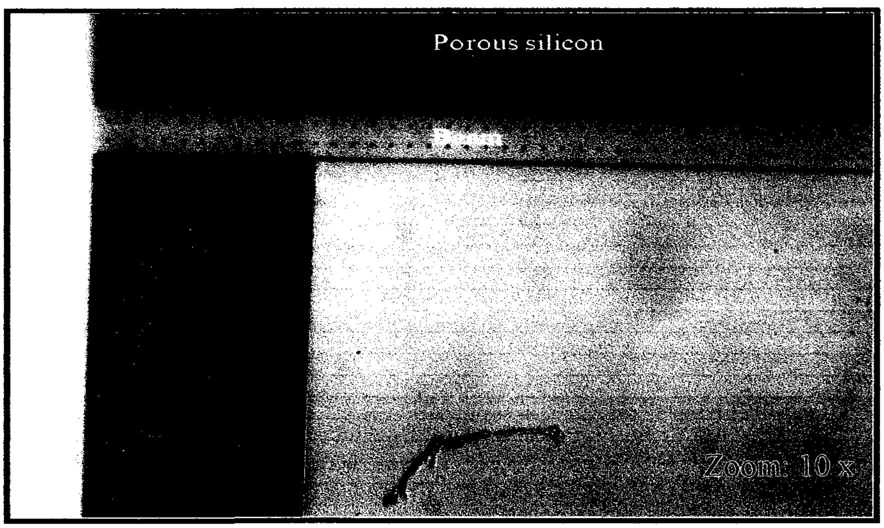

Figure 3.11 The sample which was subjected to 0.52 mA current for 1 hour

The porous layer is formed in the substrate of the SOI where the oxide layer is etched, as shown in Figure 3.12. It can be seen in Figure 3.13, that relatively thin porous layer grows in the substrate in the areas where the oxide is under etched. This is because the current flow between the silicon substrate and the Pt electrode is blocked to a certain extent by the device layer. The layer starts to grow thicker under the structural MEMS device where the device layer is largely etched except the structural device. This thick layer is because of the largely open device layer that allows the current to flow freely from the silicon substrate to the Pt electrode. With the etching parameters mentioned above, a 40 μm thick porous layer was formed, as shown in Figure 3.13 (b).

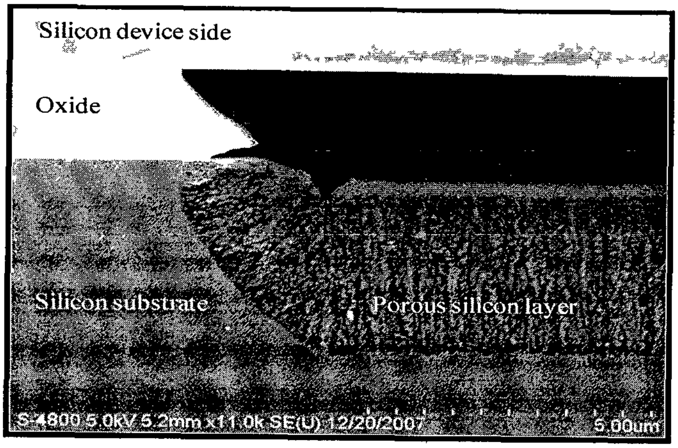

Figure 3.12 SEM of the SOI die showing porous silicon layer

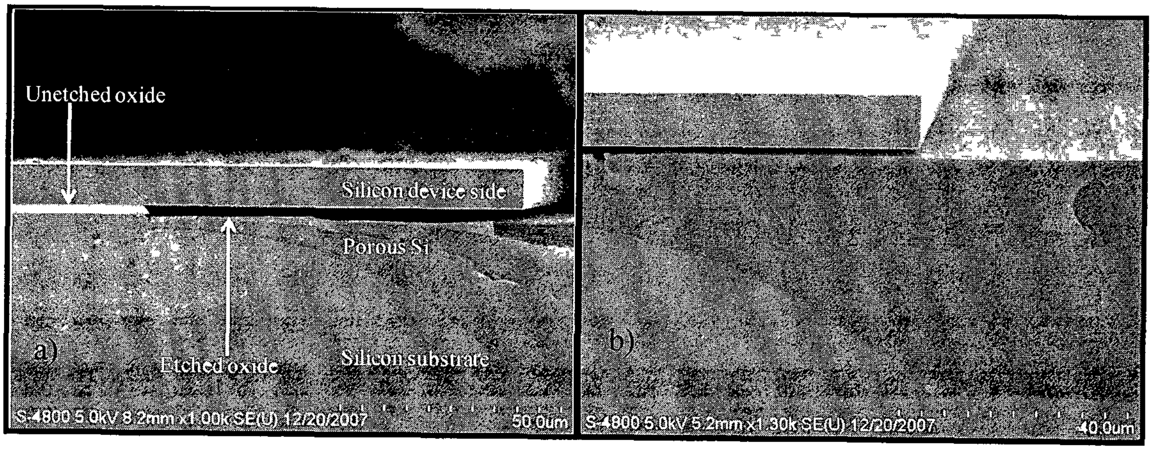

Figure 3.13 Porous layer in the substrate of the SOI die a) SEM image of the same sample shown in Fig 3.11 showing the different sections of the die, and b) 40 μm thick porous layer

When these dies are dipped in KOH for 40 to 60 s, the porous silicon can be etched off thus creating cavities in the substrate. Figure 3.14 shows the SOI die that was subjected to 50 mA/cm^2 for 60 min. It was observed that the surface of the substrate was polished.

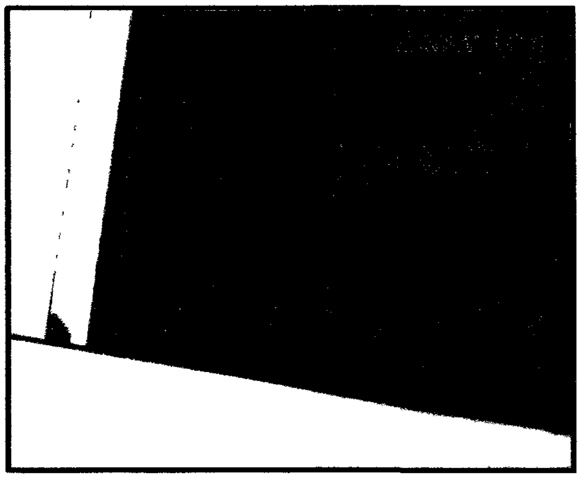

Figure 3.14 Electropolished substrate

3.6. Generation 2 Tuning Fork Resonator

The Generation 2 tuning fork resonator shown in Figure 3.15 (a) has a substrate area of 6.55×10^{-6} m^2. These resonators were subjected to an optimized current density of 3 mA/cm^2, in a 10% HF solution for a time duration of 20 min to obtain a 10 μm thick porous silicon layer in the substrate. The die was then dipped in 50% KOH solution for 40 s to etch the porous layer and create a cavity in the substrate. Figure 3.15 (b) shows the obtained 10 μm deep cavity in the substrate.

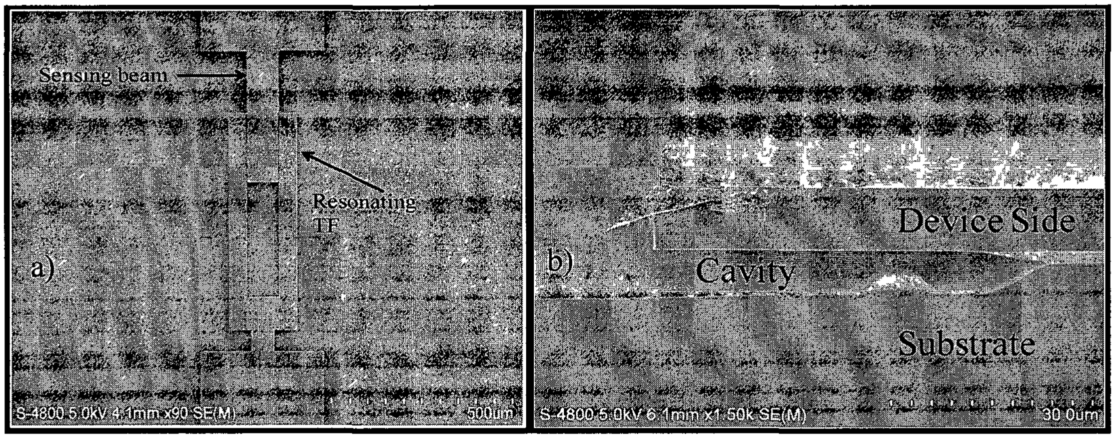

Figure 3.15 Tuning fork resonator a) design of resonator, and b) cavity obtained in the substrate

3.7. Augmenting Porous Silicon Getter to the Cavity

The benefits of the cavity and the getter have been discussed in Chapter 1. After obtaining a cavity in the substrate, it was augmented with a 10 μm thick layer of porous silicon that acts as a getter. The experimental setup is shown in Figure 3.16. The buried oxide of the SOI die is etched in 50% HF solution (Figure 3.16 (a)). The die with etched oxide is subjected to the electrochemical etching cycle with 10% HF (Figure 3.16 (b)). After 20 min of the process, a 10 μm porous layer is formed in the substrate, and is etched in 50% KOH for 40 sec to form a cavity (Figure 3.16 (c)). The SOI die with a cavity is subjected to another cycle of electrochemical etching, thus forming a porous silicon layer augmented to the cavity that acts as a getter material (Figure 3.16 (d)). Figure 3.17 shows the SEM of the SOI die with cavity and porous silicon in the substrate.

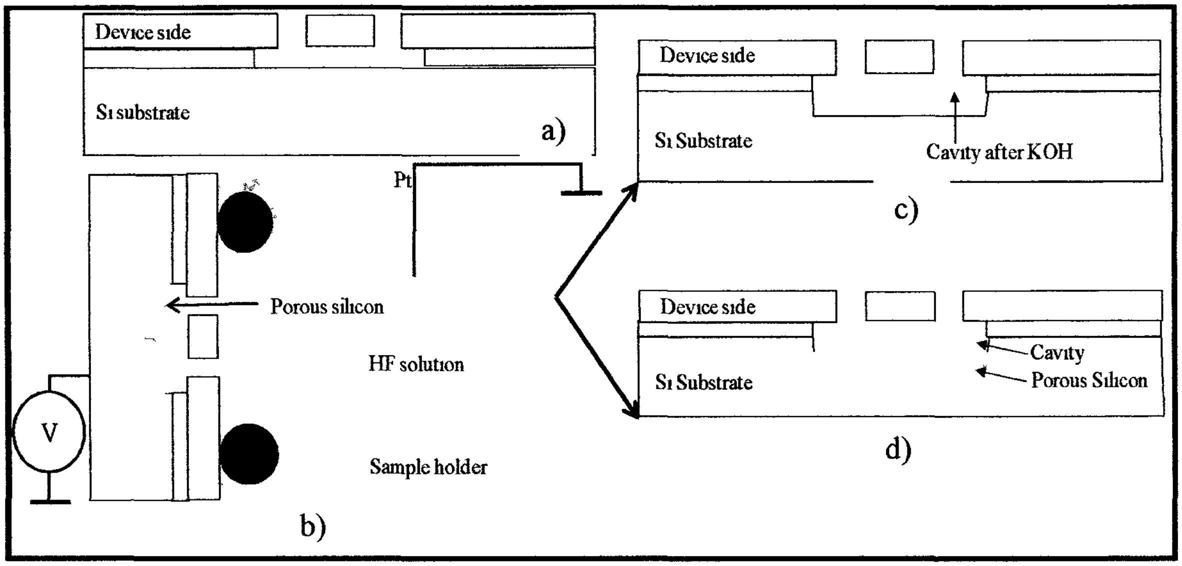

Figure 3 16 Electrochemical etching process to obtain cavity and getter in the substrate a) SOI die with etched buried oxide, b) HF etching jig, c) cavity after KOH etch, and d) porous silicon augmented to cavity after another electrochemical etch cycle

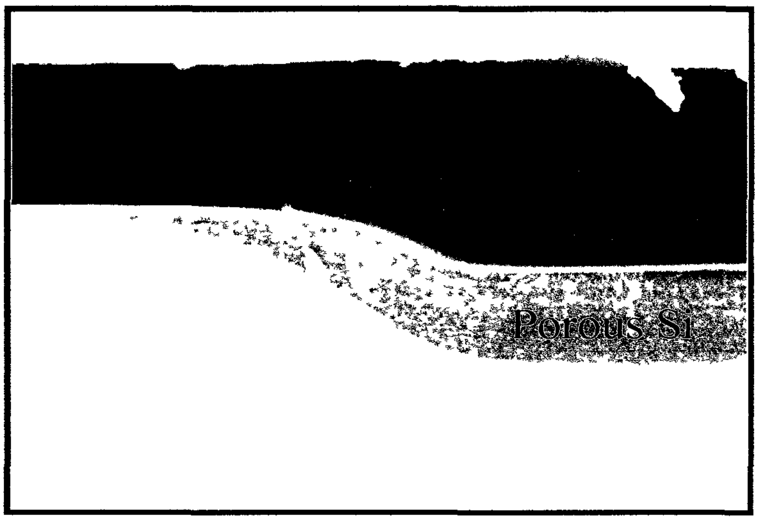

Figure 3 17 Porous silicon and cavity in the substrate

3.8. Obtaining Cavity with High Current Densities

In the results presented so far, it was seen that by using 3-10 mA/cm^2 current density, a thick layer of porous silicon can be formed in the substrate This layer was then etched using 50% KOH to obtain a cavity in the substrate. The SOI dies were subjected to a current density of 200 mA/cm^2 for 30 min and 60 min each. It was observed that the die with a 30 min process time showed an 80 μm etched cavity in the substrate, as shown in Figure 3.18. The die with a 60 min of process time showed a cavity of 200 μm, as shown in Figure 3.19.

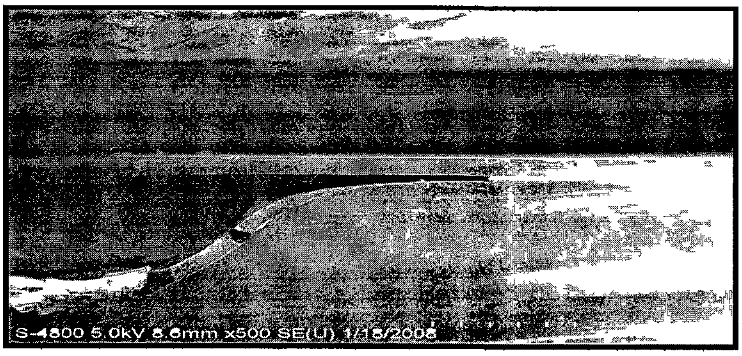

Figure 3.18 The SEM image of SOI device showing the cavity obtained in the substrate

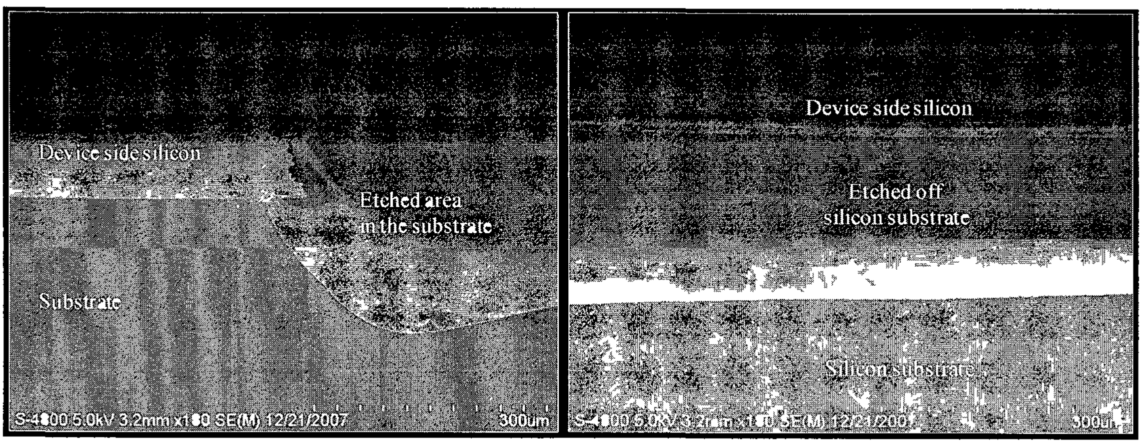

Figure 3.19 Images showing the device side and substrate with the etched surface obtained using the electrochemical etching

Although with the application of high current densities led to deep cavities in the substrate with any KOH etching required, the device layer was etched in this process. Figure 3.20 shows the device side of an SOI die with a polished surface. The resonating beam structure was also consumed in this etching process. It could be concluded that although the high current densities can etch deep cavities in the substrate, it affects the device side. Hence, in this dissertation, low current densities for moderately longer periods of time were used to obtain porous silicon in the substrate.

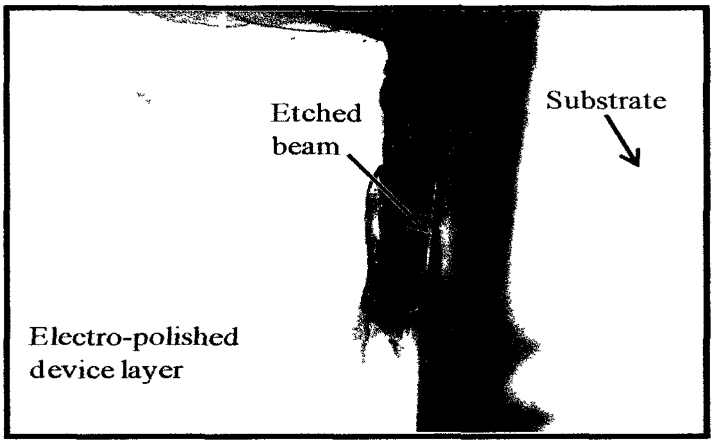

Figure 3.20 The die where the beam is etched out and the device side is polished too

Figures 3.21 and 3.22 show thick layers of porous silicon in the substrate of an SOI die bonded to a glass die. The layers seen in Figure 3.22 are due to the cleaving process.

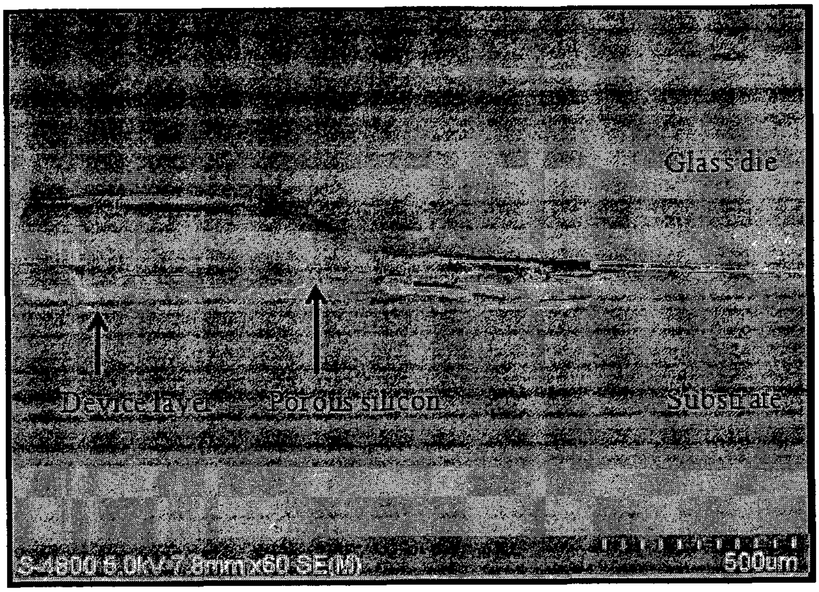

Figure 3.21 SEM shows the glass bonded to Si with the layers of porous silicon being clearly shown

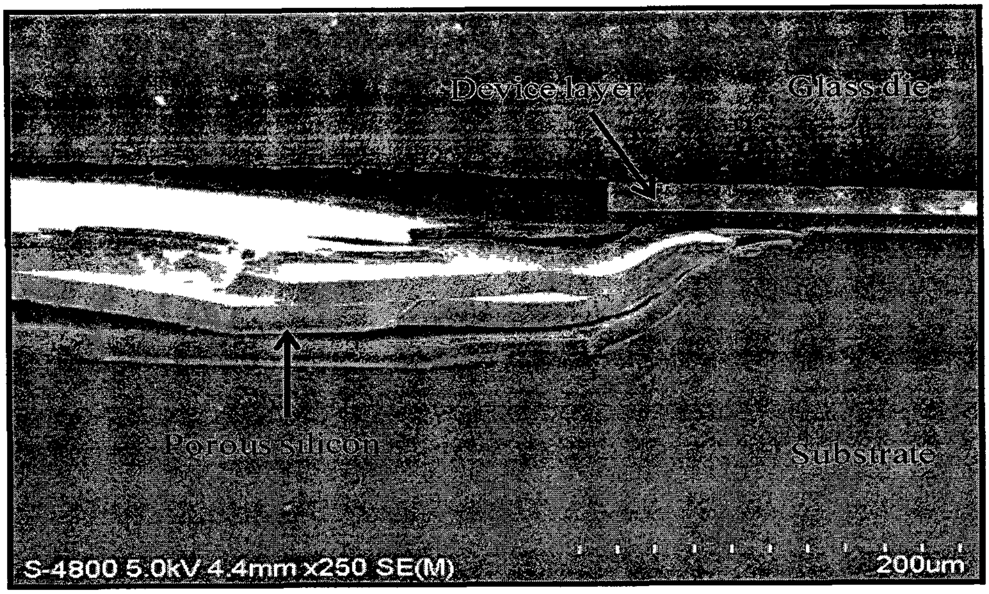

Figure 3.22 The zoomed image of the device in Figure 3.21

3.9. Problem Encountered: Reactive Device Side

Ideally, the porous silicon should only be formed in the substrate of the SOI die. With the experiments performed, it was seen that the porous silicon was formed in both the substrate wafer and the device layer. The rate of formation of porous silicon on the device side was indeed much slower. Figure 3.23 shows the microscopic image of the die showing the porous silicon on the device side. It was formed only in the area of the device side covered by the O ring and exposed to HF. In order to create the cavity in the substrate when the die was dipped in KOH, the depth of the etched surface in the device side silicon was measured to be 100 nm. Figure 3.24 shows the measured depth from the profilometer. Figure 3.25 shows the SEM of the reactive device side.

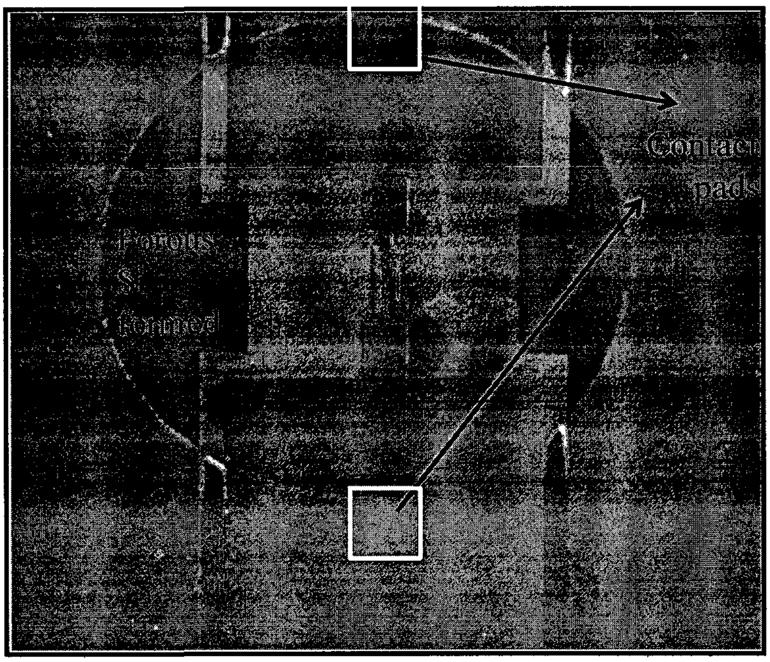

Figure 3.23 The microscopic image of the die showing porous silicon on the device side

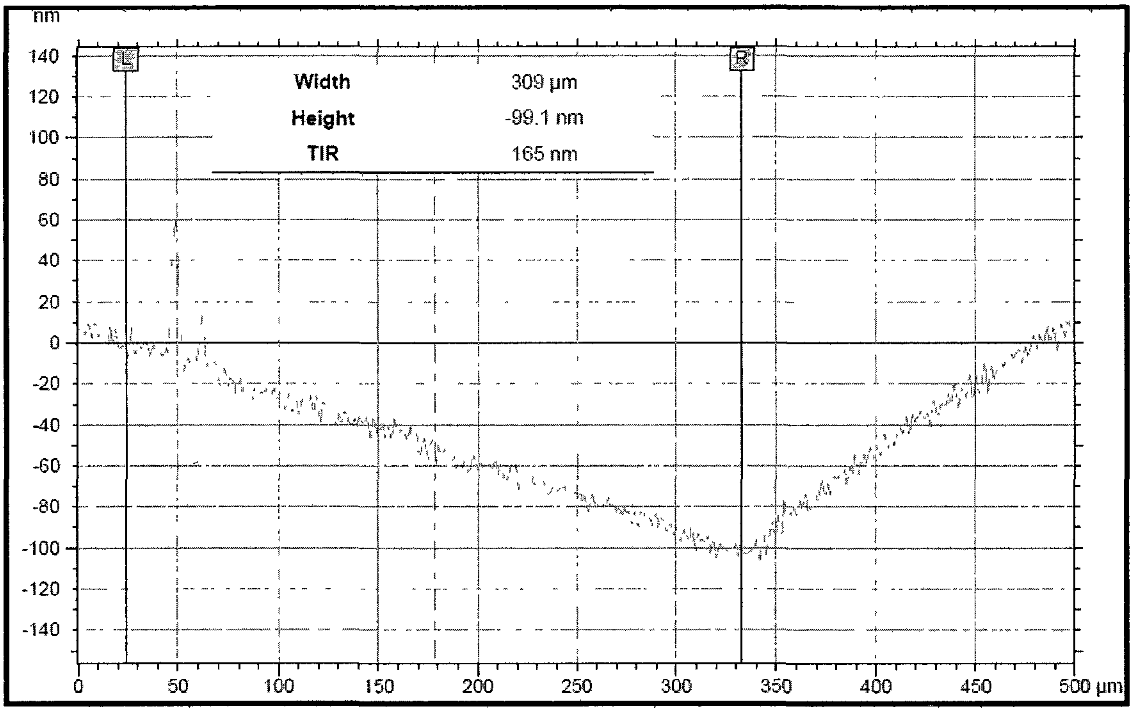

Figure 3.24 The tencor profile of the SOI die with 100 nm depth in the device side post KOH etch

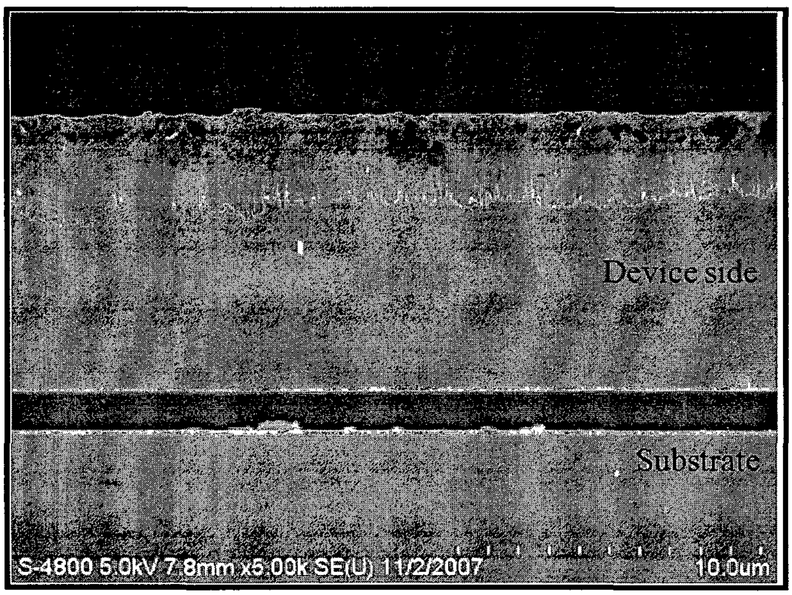

Figure 3.25 SEM of the die showing porous silicon on the device side

The reaction on the device side is highly undesirable, as the cavity formed in the device layer after KOH etching may prevent hermetic sealing with the glass cap. Figure

3.26 shows the schematic of the desired, perfectly sealed sample with no leaks, due to the absence of any undesired cavities formed in the device side. Figure 3.27 shows the cavity created in the device side by the porous silicon formed on the device layer extending to the contact pads leading to improper sealing of the sample.

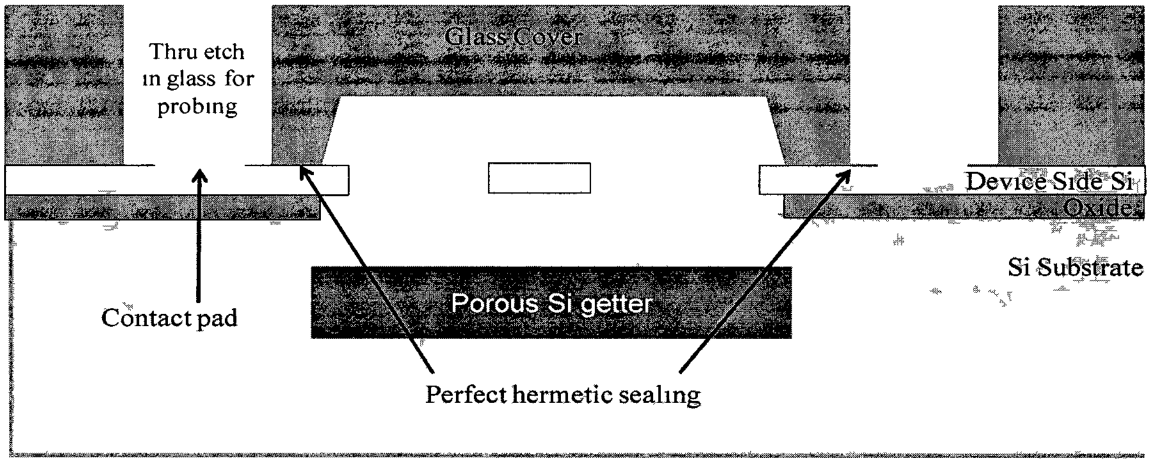

Figure 3.26 Schematic of a perfectly sealed SOI sample

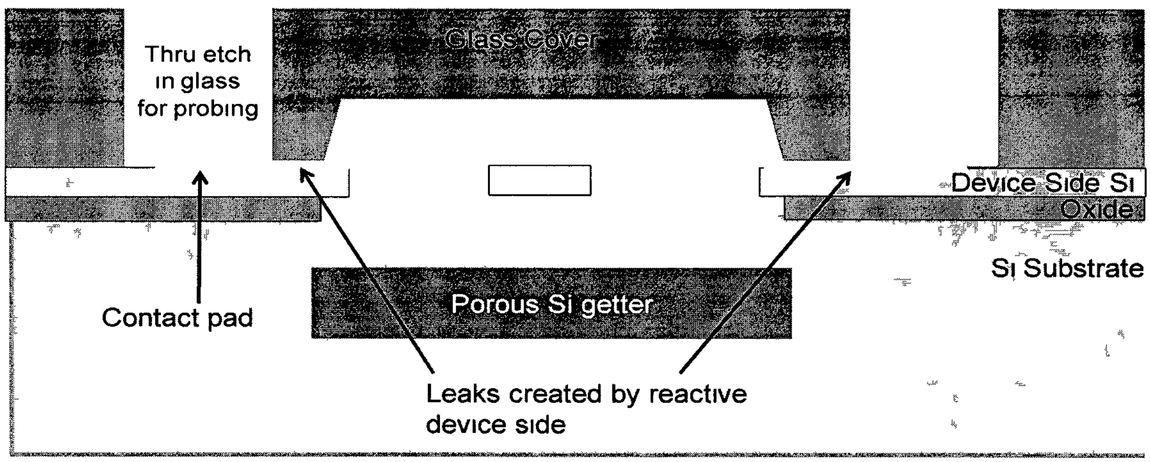

Figure 3.27 Schematic of a sample with leaks due to the undesired 100 nm cavity obtained in the device side

A possible explanation is shown in Figure 3.28. The current passes from substrate to the solution. Ideally, this current should not pass the device layer. However, if the solution resistance is higher than the device layer resistance, the current would conduct through the device side silicon and form a thin layer of porous silicon.

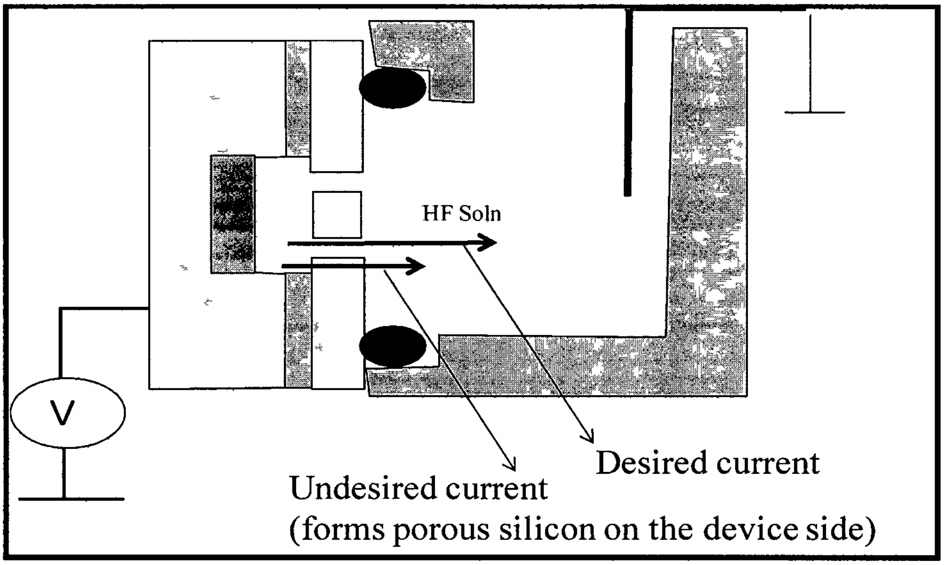

Figure 3.28 Current flow during the etching process

One of the possible reasons for the reactive side silicon could also be an undesired leak from the O ring that would make a contact between the device side and the substrate. In order to check the credibility of this reasoning, a new electro-chemical etch setup was designed, as shown in Figure 3.29. Instead of using the one-sided jig, the HF drops were placed on the device side using the pipette, and the electrical contact was provided using the probe (Figure 3.30). The die was placed on the stainless steel base that conducts the current through the substrate. In this process the possibility of the contact between the device side and the substrate was eliminated, but the results obtained showed the same affects of porous silicon on the device side.

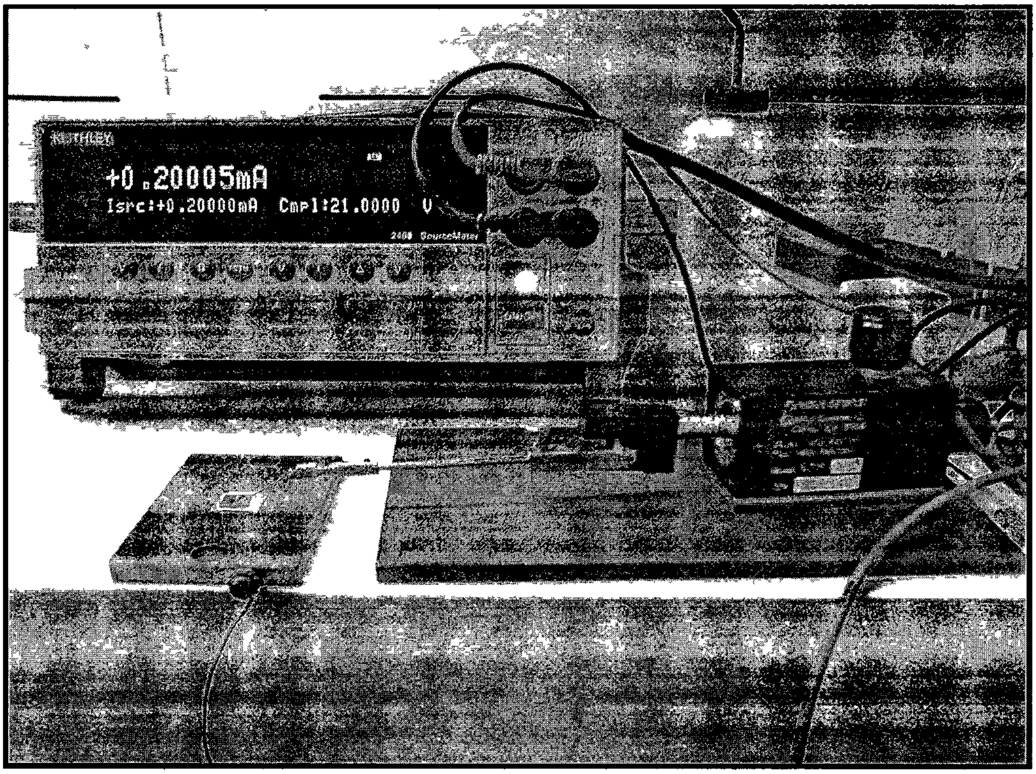

Figure 3.29 The setup showing one of the experiments carried out to counter the porous device side

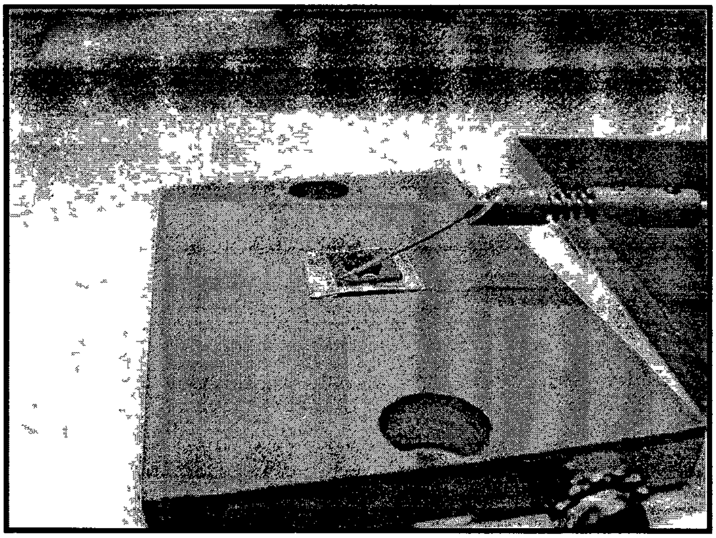

Figure 3.30 Zoomed in view of the contact on the device side

3.10. Steps to Avoid Porous Silicon in the Device Side

The following steps were taken to avoid the reaction on the device side silicon:

1) Changing the groove where O ring is placed, from conical to cylindrical:

   The schematic of the HF jig setup is shown in Figure 3.31. The gland in which the O rings sits was changed from conical to cylindrical. This would stop any leakage of HF from the groove and avoid any short-circuit between the device side and the substrate of the SOI die.

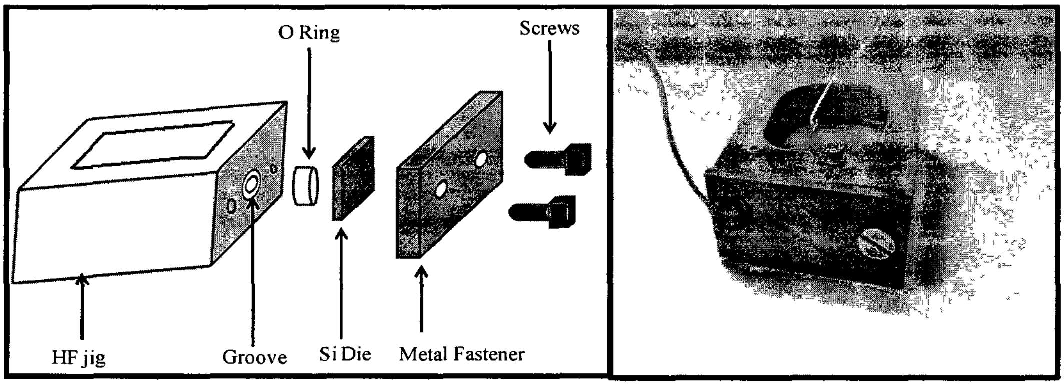

Figure 3.31Schematic of the assembly of etching setup and the actual jig

2) Using ethanol to dilute HF instead of iso-propanol:

   Ethanol was used instead of iso-propanol to dilute 50% HF to 10% HF. Ethanol acts as a surfactant and aids in uniform porous layer formation.

3) Wait period between the buried oxide etch and electrochemical etch:

   Once the Si die is fixed on the HF jig, 50% HF is used to etch the buried oxide and release the structure. This solution is then removed with a pipette and the jig is filled with 10% HF for electrochemical etching. The wait period between these two processes would help any remaining high concentration of HF to dilute into the low concentration solution and prevent any rapid etching of silicon.

3.11. Summary

This chapter presented the experiments conducted on the single crystal silicon (SCS) wafers to obtain porous silicon, and optimize the process parameters to be used on the SOI wafers. The chosen parameters were: 10% HF, current density of 2-5 mA/cm^2 and the time duration of the electrochemical etching process was 20 min. The steps used to counter the problem of the device side reacting during the etching process were also discussed.

CHAPTER 4

PACKAGING

Vacuum packaging the MEMS devices avoids any particle contamination on the micro-structures and also helps in improving the quality factor. A detailed literature review on MEMS packaging was presented in Section 1.6.

In this chapter, the silicon and glass bonding methodology, and the setups utilized in this dissertation are discussed in detail.

4.1. Preparation of Glass Dies and Si Dies

In this dissertation, the silicon wafers were diced, and the process of electrochemical etching and the introduction of a porous silicon getter were carried out on individual dies. Next, the silicon dies were bonded to the glass dies to package the MEMS resonator.

Two types of glass dies were fabricated, as shown in Figure 4.1. The Generation 1 resonators used back side electrical probing; hence, the glass die needed only a cavity to be structured over the moving resonator. The Generation 2 resonator used front side electrical probing; therefore, the glass die needed a cavity and through etched holes to be structured over the Si resonator and the contact pads, respectively. The cavity increases the volume to surface ratio in the bonded sample.

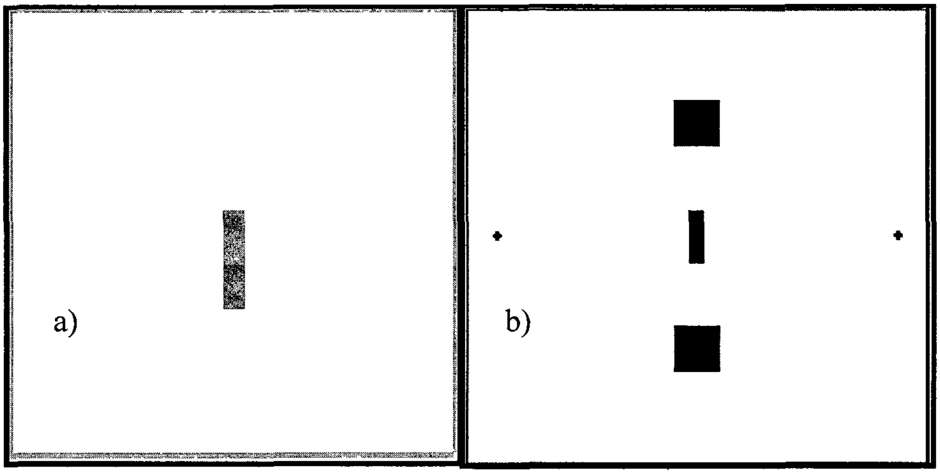

Figure 4.1 Masks for the glass caps for a) Generation 1 resonators, and b) Generation 2 resonators

After the glass dies have been patterned by lithography, they needed etching of cavity and contact pads. Various processes have been reported in the literature for etching glass.

Corman et al. [59] presented a wet etching process to etch the glass. A silicon wafer pre-structured in KOH was used as a mask. The silicon was anodic bonded to glass, and the assembly was etched in HF and H_2O solution. After the glass is structured, the assembly was placed in KOH solution to etch off the silicon. The glass wafer can be washed in H_2SO_4:H_2O (2.5:1) solution and re-bonded with silicon without any defects. This process of structuring the glass requires anodic bonding and multiple etching steps.

The traditional method of wet etching the glass is to use Cr/Au as the masking layer and HF as the etching solution. Iliescu et al. [60] presented a method of wet etching of glass using amorphous silicon/photoresist and amorphous silicon/silicon carbide/ photoresist as the mask. As these masking layers have less stress, the HF solution can be used to etch through the glass without any defects being generated. As per their work as presented, the defects in the glass are limited to the defects in the masking layer and the penetration of the etching solution through these defects. The etch rates of 7.5 μm/min have been reported for the process.

Dry etching has also been used to etch the glass wafers. This method becomes more prominent when the etch holes in the glass are required to be vertical [61]. Ni has been used as the masking layer and SF_6 as the gas medium to etch the glass. Another method used for dry etching the glass is by using SU8 as the masking layer as reported by [62]. It was shown in their work that 85° vertical etches were obtained.

Sand blasting is another method of etching glass. It is used for plasma display panels to etch 50 μm width channels [63]. Sand blasting is shown to have very high etch rates compared to RIE, ion milling and wet etching [64]. It produces conical etched shapes in the glass [65]. In this dissertation, flat glass surface was needed to bond and conical etch in the glass would not have been affected; hence, this method was used to etch the glass.

4.2. Methodology Used for Etching Glass

The Generation 1 resonators used back side probing to test the devices, and the Generation 2 used front side probing of the devices. The glass caps were structured according to the probing mechanism. The glass cap for the Generation 1 resonators was structured with only a cavity to be aligned above the resonator (Figure 4.2). The glass cap for the Generation 2 resonators was structured with a cavity to be aligned above the resonator and two thru-etched cavities aligned above the contact pads (Figure 4.3). In order to optimize the process steps, the bonding of glass and silicon was carried out in two stages. In stage one, the silicon die was bonded to the glass dies structured with a thru-etched cavity aligned over the resonator (Figures 4.4 and 4.5). In this stage, the process parameters (temperature, pressure, voltage and time) were optimized. In the second stage, using the optimized parameters from stage 1, the silicon die was bonded to the glass die structured with a cavity that aligns the resonator structure. Figure 4.6 shows the schematic of glass and silicon die aligned before bonding.

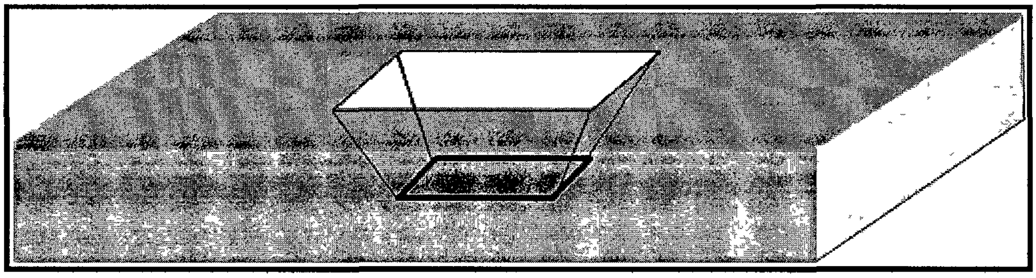

Figure 4.2 The schematic of glass die with cavity over the beam surface

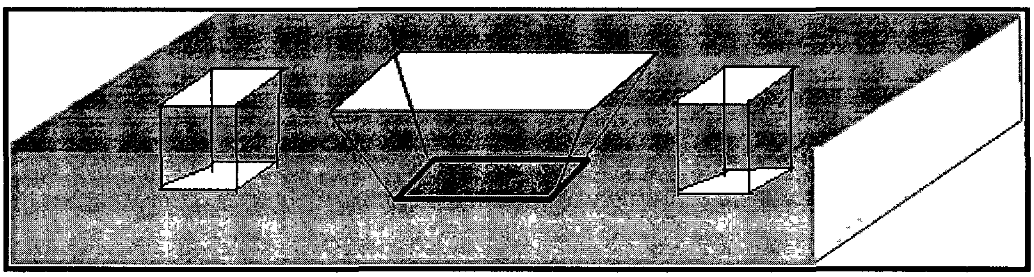

Figure 4.3 The glass cap with thru holes at the ends for the electrical connections and a 200 μm cavity aligned over the beam surface.

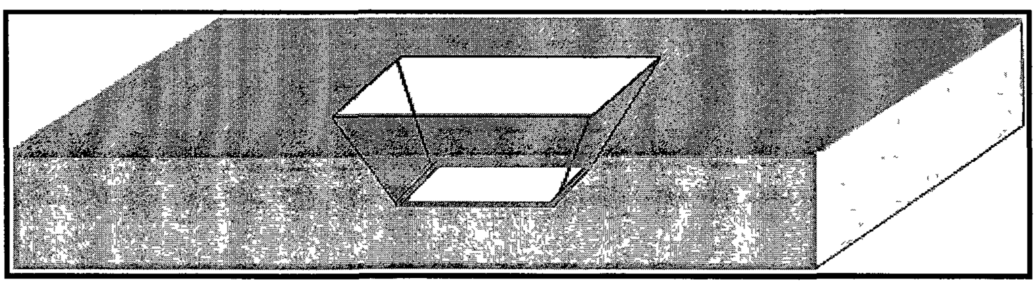

Figure 4.4 The schematic of glass die with through hole over the beam surface

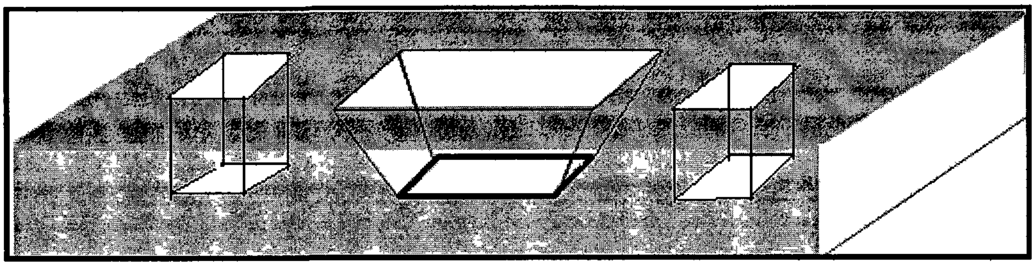

Figure 4.5 The glass cap with through holes at the ends for the electrical connections and a through etched cavity in the middle to cover the beam surface

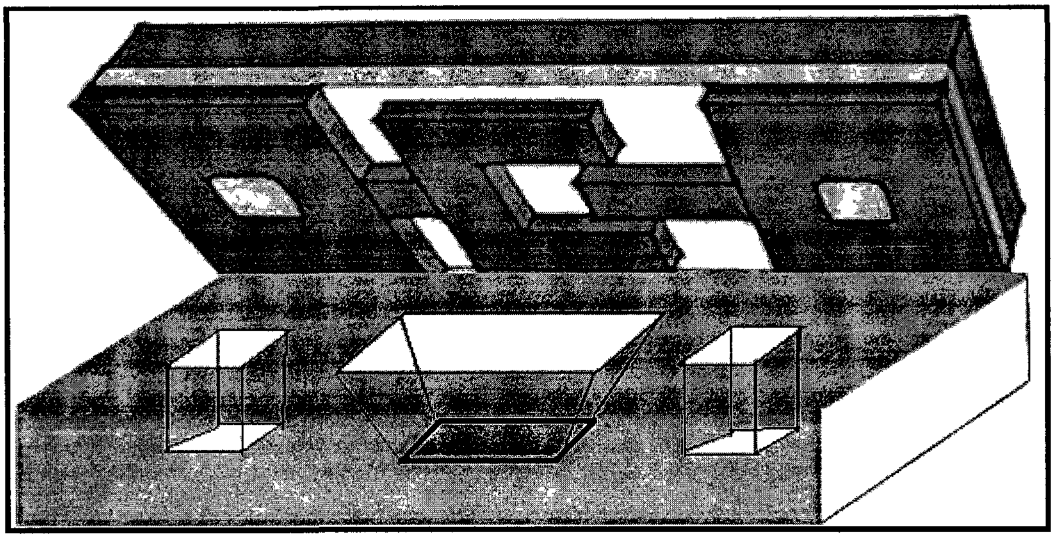

Figure 4.6 Schematic of the glass and silicon die for encapsulation

4.3. Experimental Process

In this dissertation, the individual glass dies were etched one at a time. The dies were required to have through etched contact pads in a 500 μm thick glass wafer and a cavity of 100-200 μm. Sand blasting was used to etch the glass. The contact pads and cavity were etched one at a time. Electrical tape was used as the masking layer for the glass dies. A sand blasting gun was aimed at the unmasked surface of the glass die to etch the glass. The glass dies were cleaned using acetone and isopropanol, followed by Piranha etch. A glass die structured with two thru-etches for contact pads, and a cavity, is shown in Figure 4.7. An SEM image of a bonded Si and glass assembly with a cavity in the glass and a through etched glass is shown in Figure 4.8.

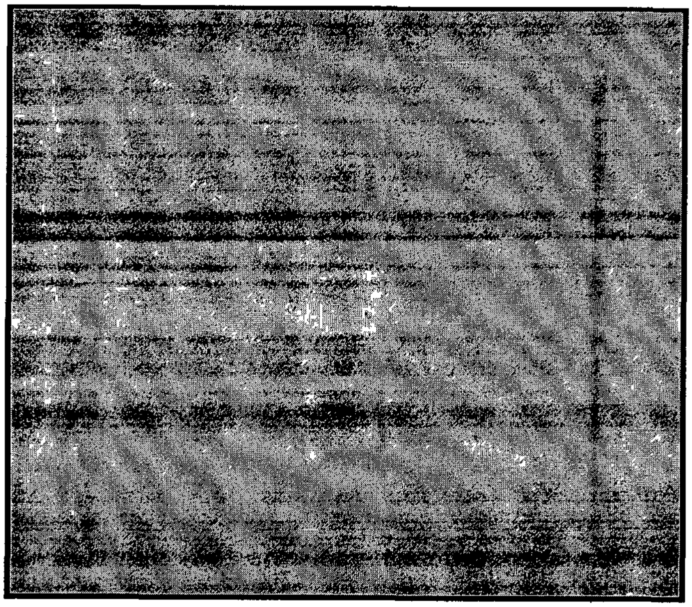

Figure 4.7 The microscopic picture of the glass die showing the through etched holes for the electrical connection and the cavity in the middle

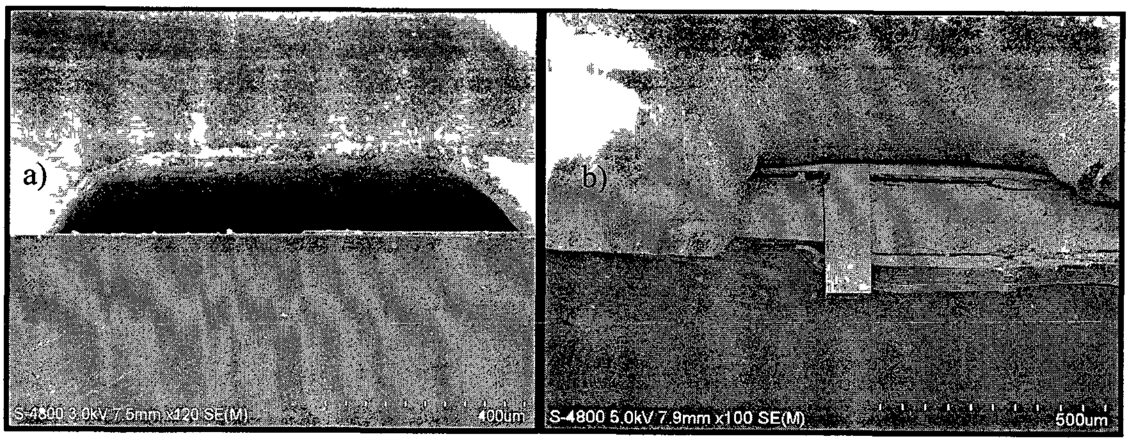

Figure 4.8 The SEM of the bonded die a) with the cavity in the glass structure, and b) with through etch hole in the glass die

Figure 4.9 shows the microscopic image of the bonded assembly of Si and glass. The thru-etched cavity in the glass structured over the resonator for Generations 1 and 2 along with the contact pads are shown. Figure 4.10 shows the contact pads etched from the backside in the substrate of the Si die for Generation 1 resonators.

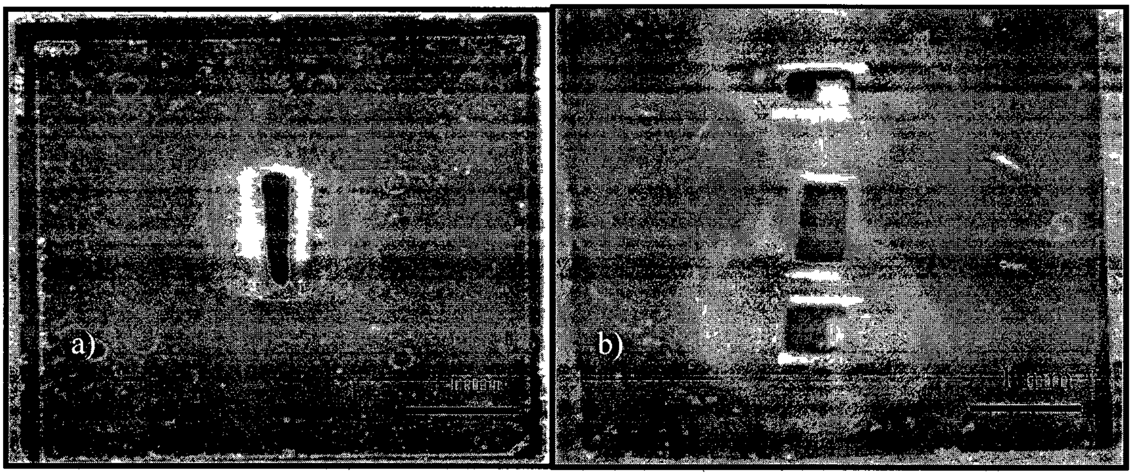

Figure 4.9 The microscopic image of bonded devices a) Generation 1 with the through etch aligned over the resonator, and b) Generation 2 with the contact pads on Si die and through etch in glass over the beam surface

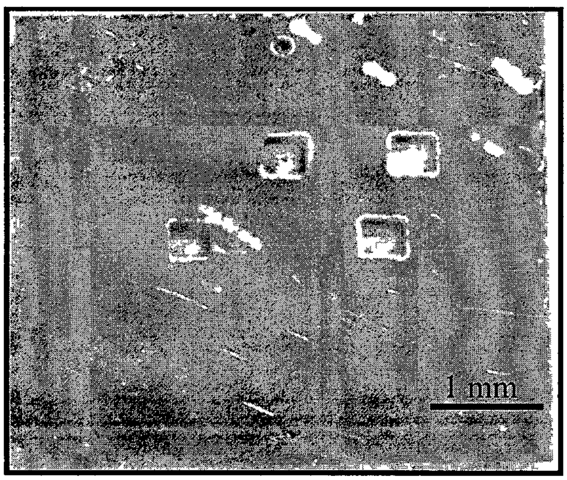

Figure 4.10 The ICP etched back side of the substrate for the electrical contact for Generation 1 resonator

4.4. Bonding Setups

In this dissertation, different bonding setups were investigated before finalizing the best suited one. Two of these setups are presented here:

Setup 1:

In this setup, shown in Figure 4.11, an external heater was used to heat the sample holder and the samples. The Si and glass dies were placed as shown, and the voltage was applied when the temperature reached 450° C. In this setup, the heat conduction takes place from the bottom of the sample holder to the glass dies. This process took 2-3 hours and had limited controllability. A setup was needed that could directly heat the holder and sample with better controllability. Hence, a new setup was built.

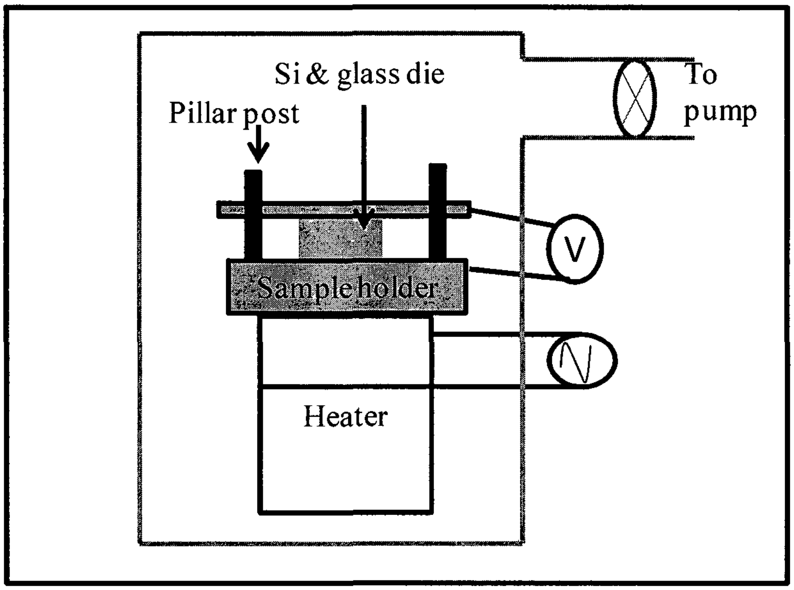

Figure 4.11 Bonding setup Design 1

Setup 2:

The final bonding setup is as shown in Figure 4.12. In this setup, a ring heater (120V, 500W, 4” dia, 4 amp) was sandwiched between two stainless steel discs. The Si and glass die assembly was placed on the upper disc as shown. The disc acts as one of the electrodes needed, and the second electrode is a stainless steel plate that provides the necessary weight on the sample. Si and glass dies were pre-aligned and placed in the vacuum chamber. After the sufficient vacuum is achieved, they were heated to 450° C and a voltage of 200 V is applied for 20 min to bond the surfaces. Figure 4.13 shows the final setup inside the vacuum chamber that was used to carry the bonding process on the silicon and glass dies.

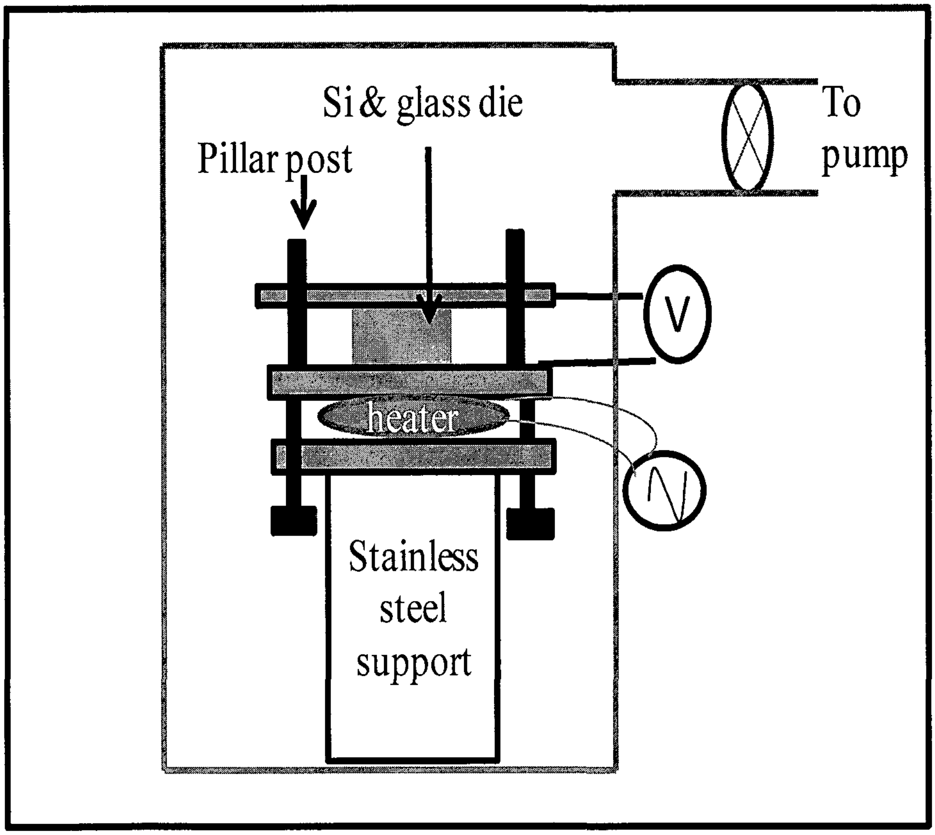

Figure 4.12 Bonding setup Design 2

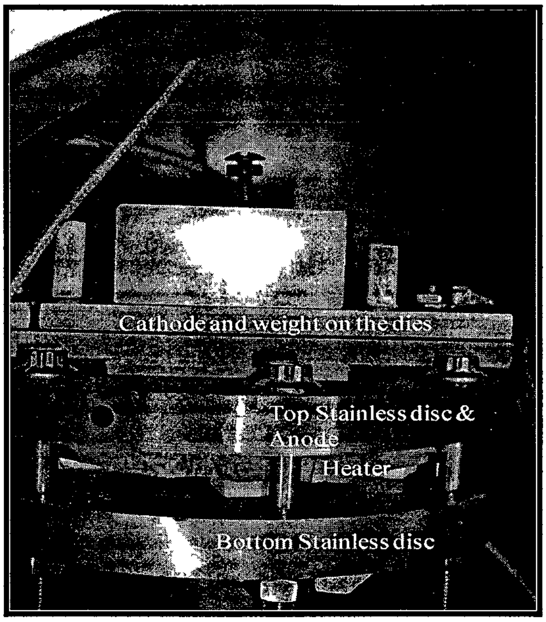

Figure 4.13 The actual setup of Design 2 inside the vacuum chamber

4.5. Summary

Different glass dies fabricated in this dissertation along with the process used were presented in this chapter. The bonding setups along with the process parameters used for anodic bonding were also presented.

CHAPTER 5

TESTING CIRCUITS

MEMS devices need an AC excitation signal and a DC bias voltage to operate. A test setup with proper connections is thus needed that can carry the excitation signal to the MEMS devices and read the output signal. In this dissertation, a printed circuit board (PCB) was custom designed, that uses the BNC (Bayonet Neil-Concelman) connectors, resistor (R) and capacitor (C) combinations, along with an operational amplifier (opamp) to: 1) provide the excitation signal to the MEMS devices, and 2) read the output at the Bode network analyzer. The PCB was also designed to cancel the parasitic capacitance that affects the measurement of quality factor of the devices.

This chapter presents the LTspice simulations of the circuits used in this dissertation, and hence there is no error value mentioned on the graphs.

5.1. RLC Representation of MEMS

The MEMS resonators need a combination of AC signal and DC bias voltage to resonate. The MEMS resonator can ideally be represented by the RLC circuit shown in Figure 5.1. The output of the resonator is measured at the output impedance of 50 ohm.

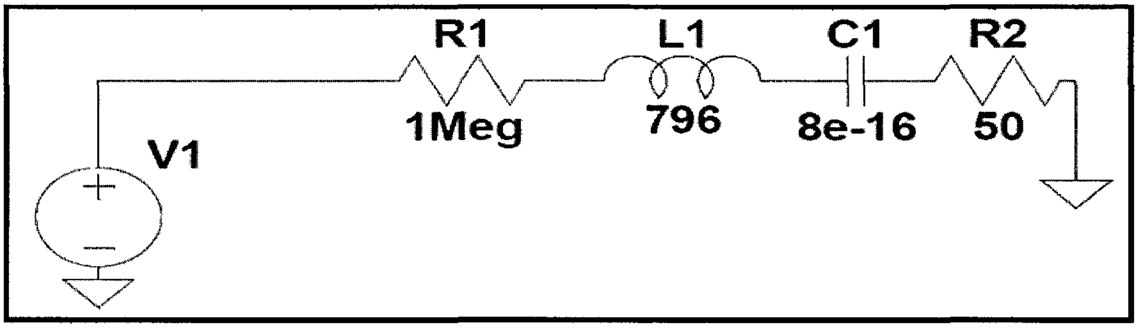

Figure 5.1 The RLC circuit representing the MEMS resonator

Figures 5.2 and 5.3 show the ideal case with no parasitic capacitance present. Hence, there is no lower peak in the resonance profile, and the phase shift is 180 °.

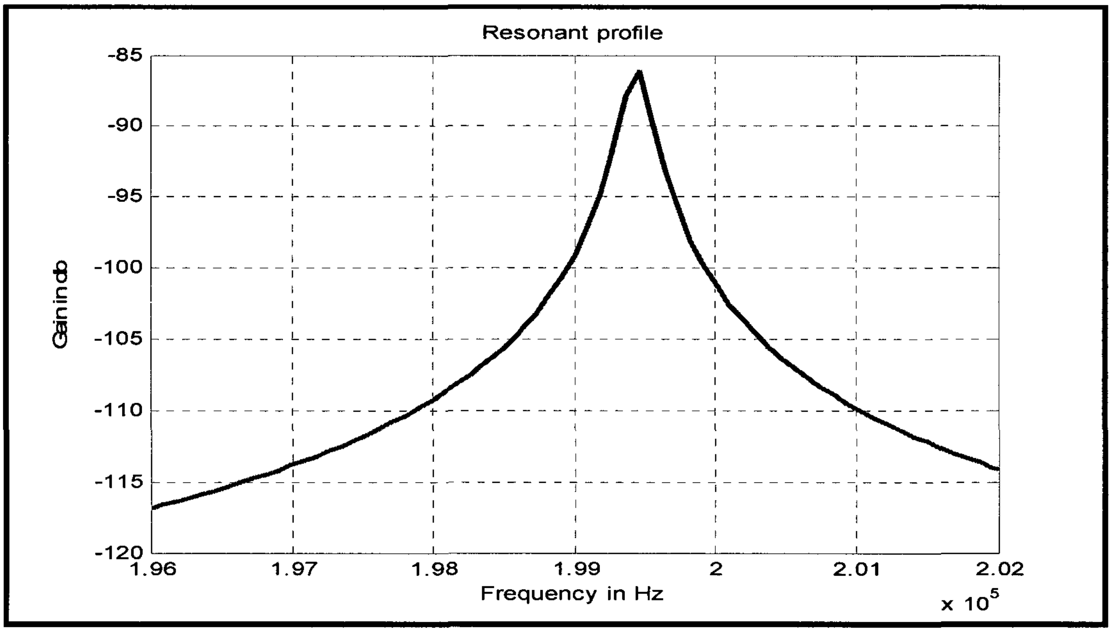

Figure 5.2 An ideal response of the ideal RLC circuit representation of the MEMS resonator

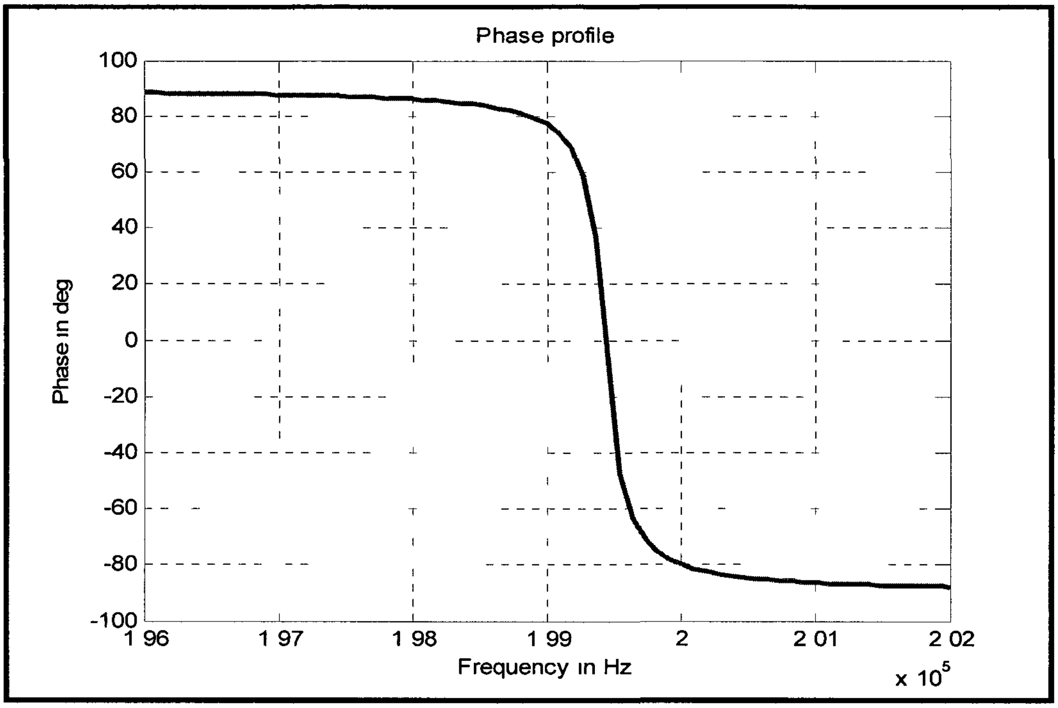

Figure 5.3 The phase response of an ideal resonator

In all MEMS resonators, parasitic capacitance exists parallel to the RLC representative MEMS resonator, as shown in Figure 5.4. This affects the signal strength and the quality factor. In order to get a readable signal strong enough to calculate the 3 dB quality factor, the output from the MEMS resonator was amplified using an opamp. The response of the MEMS device with the parasitic capacitance is shown in Figure 5.5. It can be seen that unlike Figure 5.2, the resonant profile now has a lower peak and the phase shift is not 180 °. In order to study the effect of parasitic capacitance, Spice simulations were run with different values of capacitance C2 in Figure 5.4. The summary of the results obtained are presented in Figure 5.6. It is seen that with the increase in the parasitic capacitance, the dynamic range of the resonant profiles is degraded and the apparent 3 dB quality factor is reduced, hence the need to cancel the parasitic capacitance and to improve the resonator behavior.

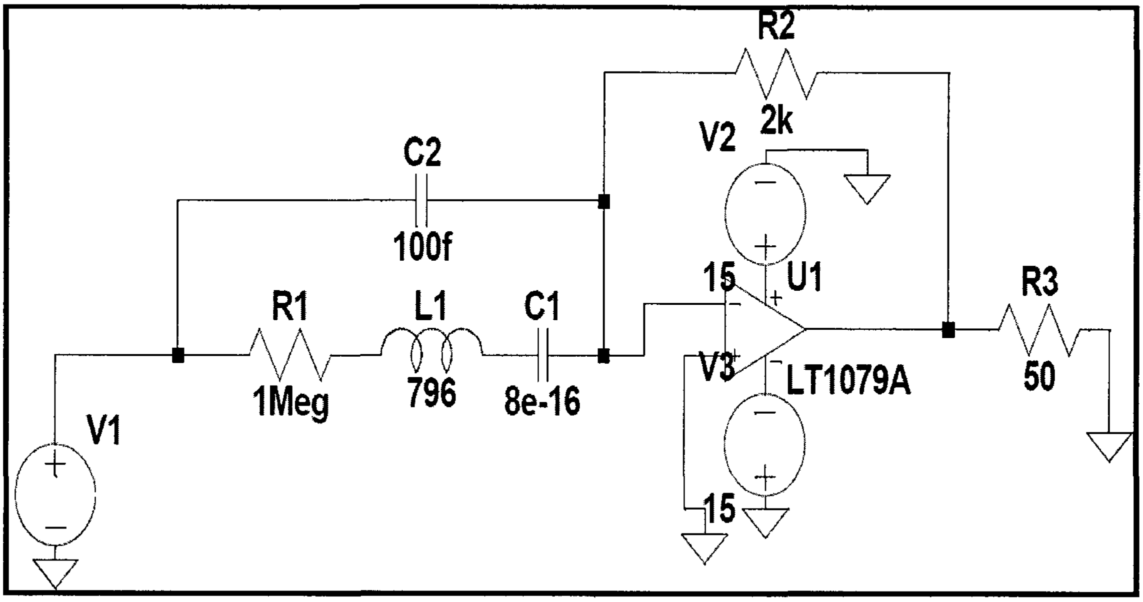

Figure 5.4 The actual resonator with calculated parasitic capacitance in parallel to the resonator

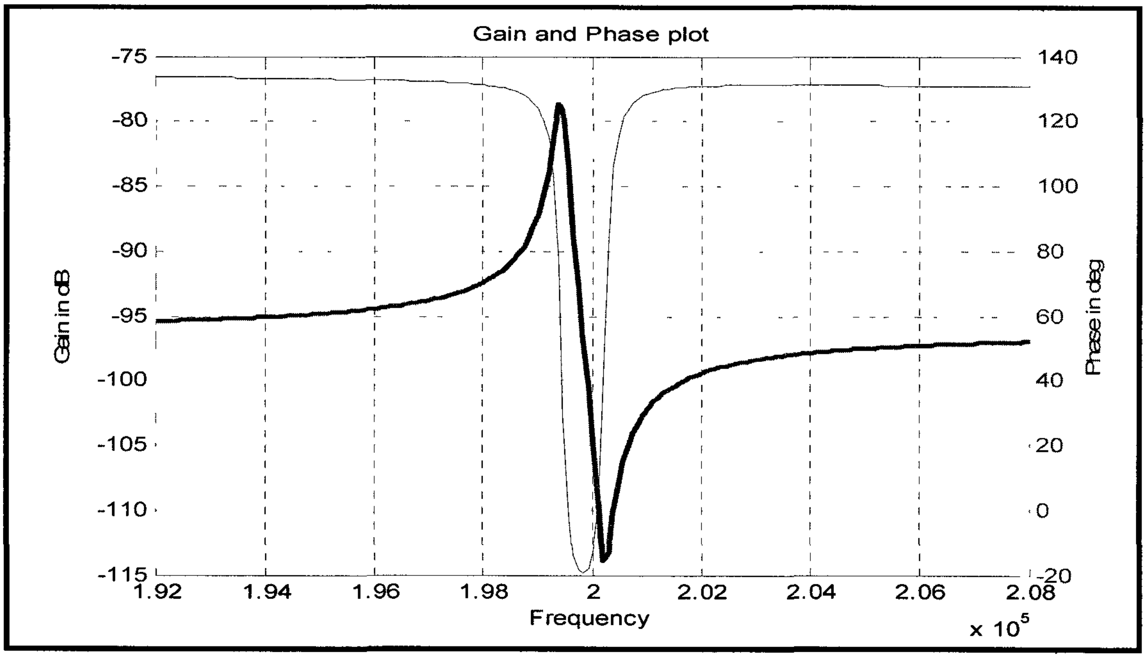

Figure 5.5 The output obtained from the MEMS resonator along with the phase profile of the resonator

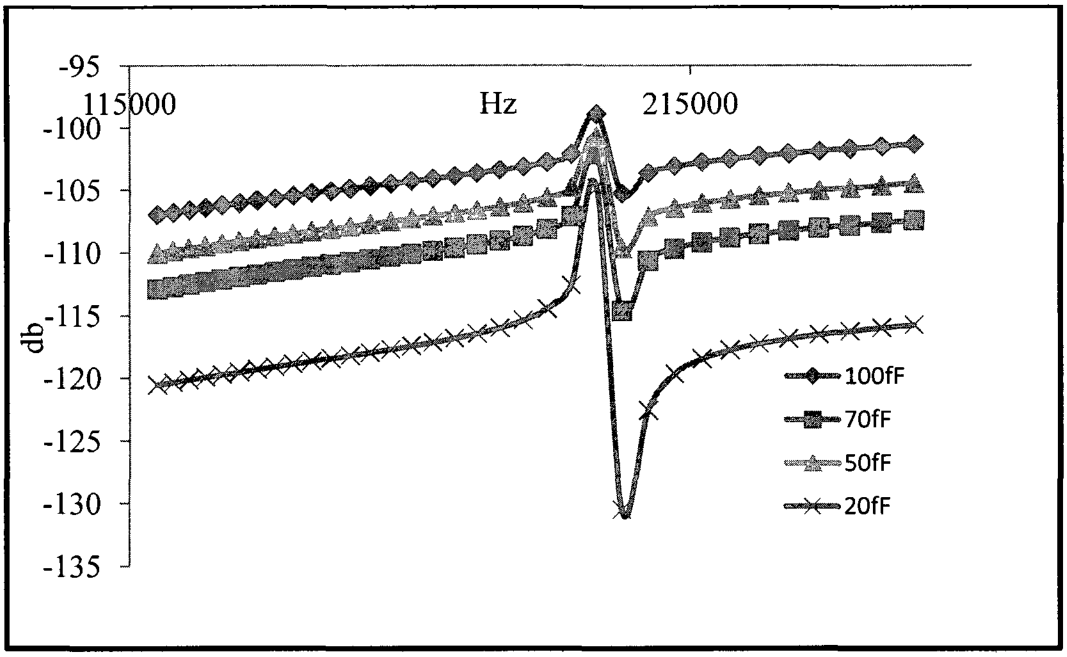

Figure 5.6 Effect of parasitic capacitance on the resonator

5.2. Calculation of Parasitic Capacitance

In order to cancel the parasitic capacitance, it was first needed to calculate the parasitic capacitance present in this resonator system. Figure 5.7 shows the circuit used to calculate the parasitic capacitance. R1, L1, and C1 represent the MEMS resonator, C0 represents the parasitic capacitance, C6 represents the 5 pF capacitor across the MEMS resonator, and the dotted line indicates the shorted MEMS device. As the parasitic capacitance cannot be measured directly, it was calculated by measuring the signal strengths for three cases. Case 1: for only the MEMS resonator (that has the inherent parasitic capacitance). Case 2: MEMS resonator shorted with a 5 pF capacitor. Case 3: MEMS resonator shorted (shown by the dotted line in Figure 5.7).

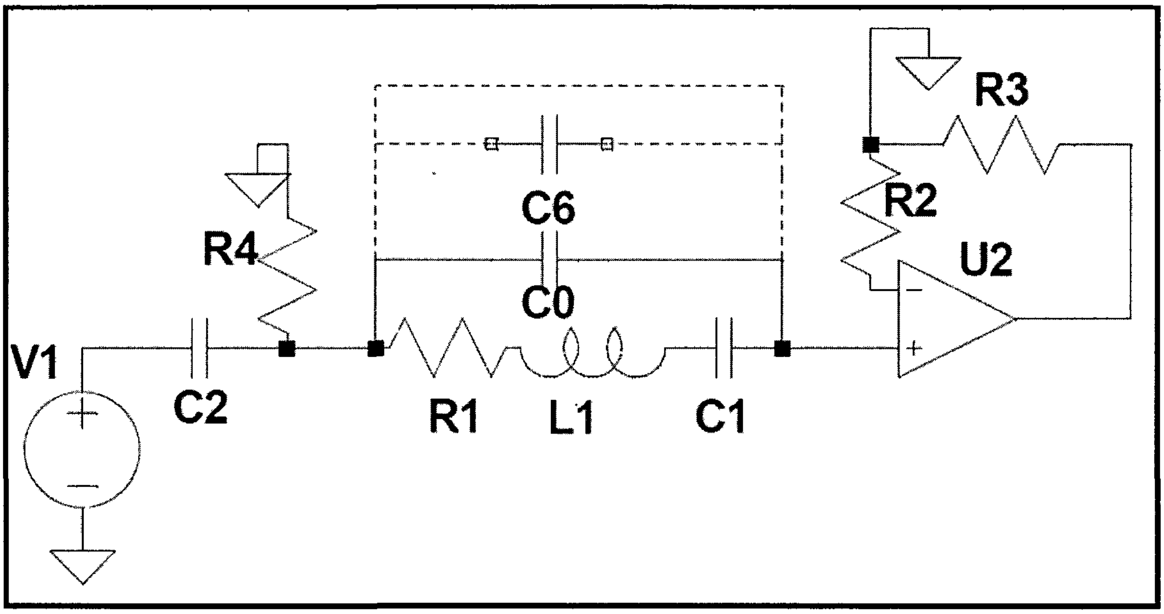

Figure 5.7 Circuit used to calculate the parasitic capacitance

In this dissertation, the signal strengths were measured by the Bode Analyzer that gives the signal strength in dB. Equations 5.1 and 5.2 were used to calculate the voltage gain / loss from S_{21}:

$$dB = 20log_{10}^{Vgain} \quad (5.1)$$

$$Vgain = 10^{\frac{dB}{20}} . \quad (5.2)$$

The S_{21} measured and converted to the voltage gain/loss are

- -8.27 dB for the 5pf i.e., the voltage gain V_c=0.38
- -43 dB with only the resonator i.e., the voltage gain V_R=0.007
- 20 dB when the resonator is shorted i.e., the voltage gain V_s=5.01

The operational amplifier has an unknown input capacitance. This can be calculated by comparing the signal strengths of the resonator in parallel with a 5 pF capacitor and when the resonator is shorted. Equation 5.3 represents the gain comparison for the resonator shorted and the resonator in parallel with a 5 pF capacitor. C_{in} is the input capacitance that was calculated as 60.92 pF.

$$\frac{V_c}{V_s} = \frac{C_c}{C_c + C_{in}} \tag{5.3}$$

$$\frac{0.38}{5.01} = \frac{5}{5 + C_{in}}$$

$$C_{in} = 60.92 \text{ pF}$$

Once the input capacitance of the operational amplifier is calculated, the dB gains for only the resonator, and the resonator shorted are compared, as shown in Equation 5.4 to calculate the parasitic capacitance. C_o represents the parasitic capacitance that was calculated to be 85 fF.

$$\frac{V_R}{V_s} = \frac{C_o}{C_{in} + C_o} \tag{5.4}$$

$$\frac{0.007}{5.01} = \frac{C_o}{60pF + C_o}$$

$$C_o = 85 \text{ fF}$$

5.3. <u>Parasitic Cancellation</u>

A custom circuit was designed and built to cancel the parasitic capacitance. Figure 5.8 shows the block diagram of the parasitic cancellation circuit used. The effective capacitance from the T-network of capacitors cancels the parasitic capacitance when it matches the MEMS capacitance C6 in Figure 5.8. The excitation signal is sent to the MEMS resonator and the T-network of the capacitors. Each signal from the MEMS resonator and T-network is passed to the single stage operational amplifiers and the output from each is fed to the differential amplifier with a gain of 10. When the parasitic capacitance is cancelled, the response of the MEMS resonator is amplified by 10.

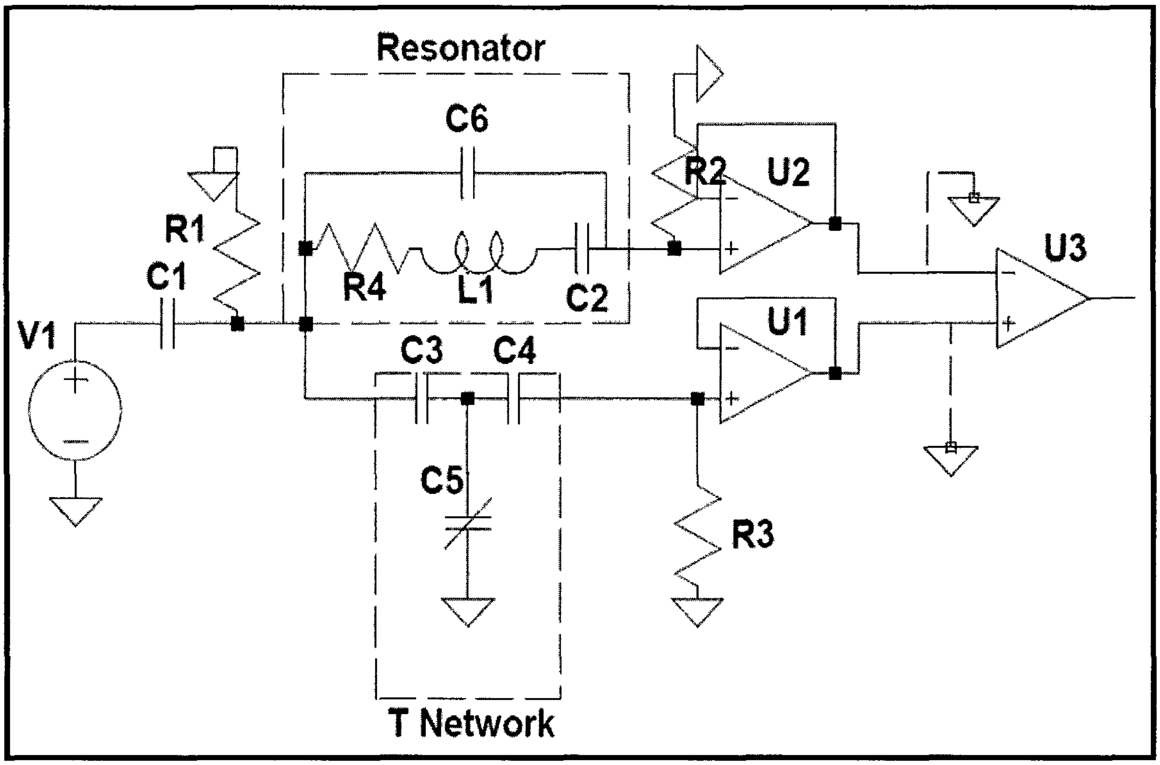

Figure 5.8 The block diagram of the parasitic cancellation circuit

As the parasitic capacitance is in femto Farads, and there is no commercial capacitor available in this range, a capacitive T-network is used that utilizes commercial capacitors in the pico Farad range, and the effective capacitance cancels out the parasitic capacitance. The capacitors C3 and C4 are non-variable but Capacitor C5 is the variable. The variable capacitor is varied so that the effective capacitance cancels out the parasitic capacitance.

In order to cancel out the parasitic capacitance using the external circuit, the following conditions have to be met:

1) when the input (+ve and –ve) of the differential amplifier (U3 in Fig 5.8) is grounded one at a time, and the output is measured, the signal level (dB level) should be the same,
2) the phase difference in the outputs, when the inputs are grounded one at a time, should be 180 ° for both the inverting and non-inverting mode of the op-amp.

Once these conditions are met, the signal level at the output of the differential amplifier with both inputs fed, drops 20 dB as the gain is 10 in Equation 5.1.

Figure 5.9 shows the LTspice schematic of the circuit tested for the parasitic cancellation. The op-amps are used in the inverting mode of this circuit. C3 in the circuit is the variable capacitance. It is varied until the point the output at the differential amplifier drops down by 20 dB. This drop indicates that the signal strength at the output of the differential amplifier for each input has the same magnitude. Figure 5.10 shows the response of the MEMS resonator when the negative input of the differential amplifier is grounded. Figure 5.11 shows the response of the MEMS resonator at the output of the differential amplifier when the positive input is grounded. As can be seen, the dB levels are at approx -49 dB for both the outputs and the phase difference between the outputs is 180 °. Figure 5.12 shows the resonant and phase profile of the MEMS resonator after the parasitic capacitance is cancelled.

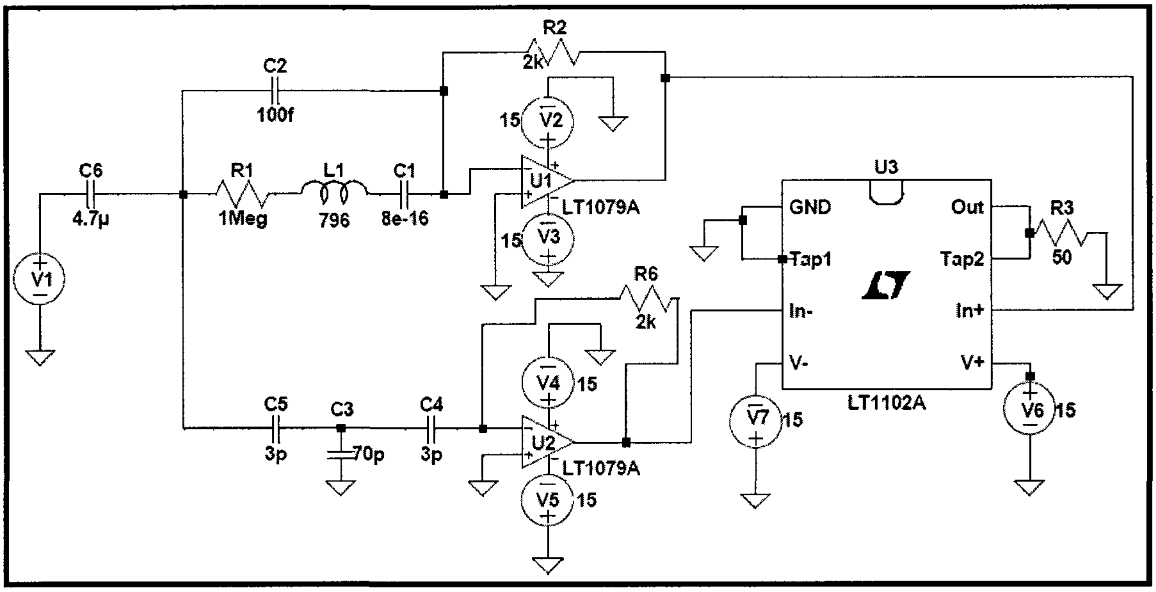

Figure 5.9 The parasitic cancellation circuit used and simulated in LT Spice

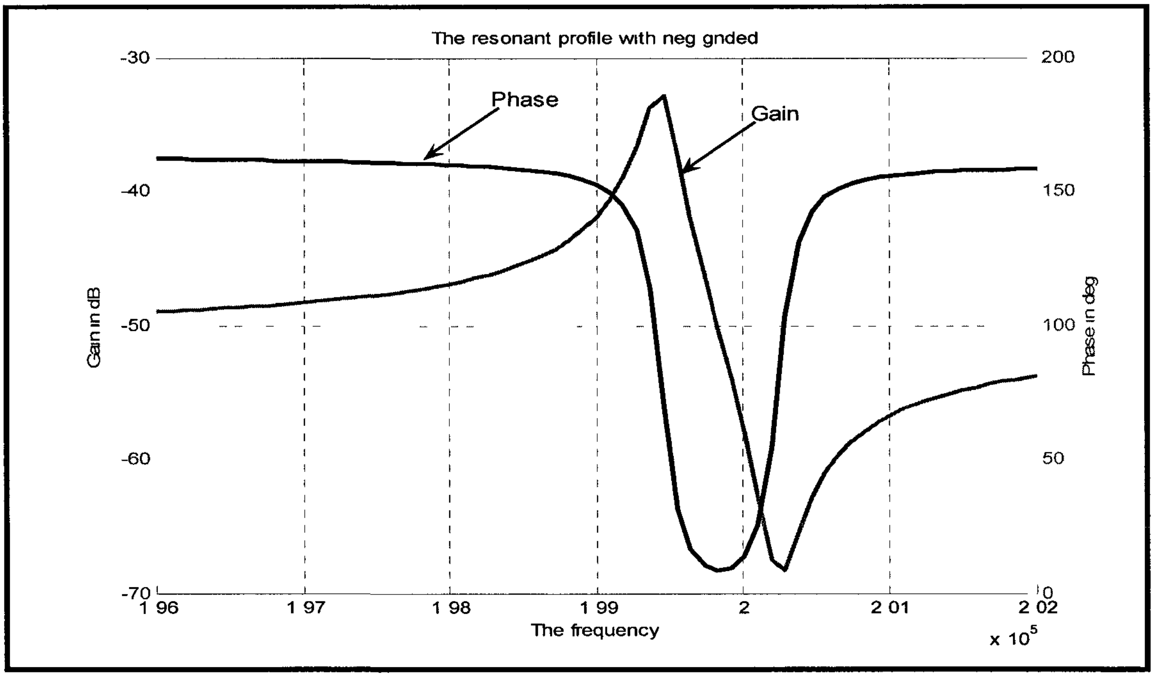

Figure 5.10 The resonant profile obtained at the output of the differential amplifier when its negative input is grounded

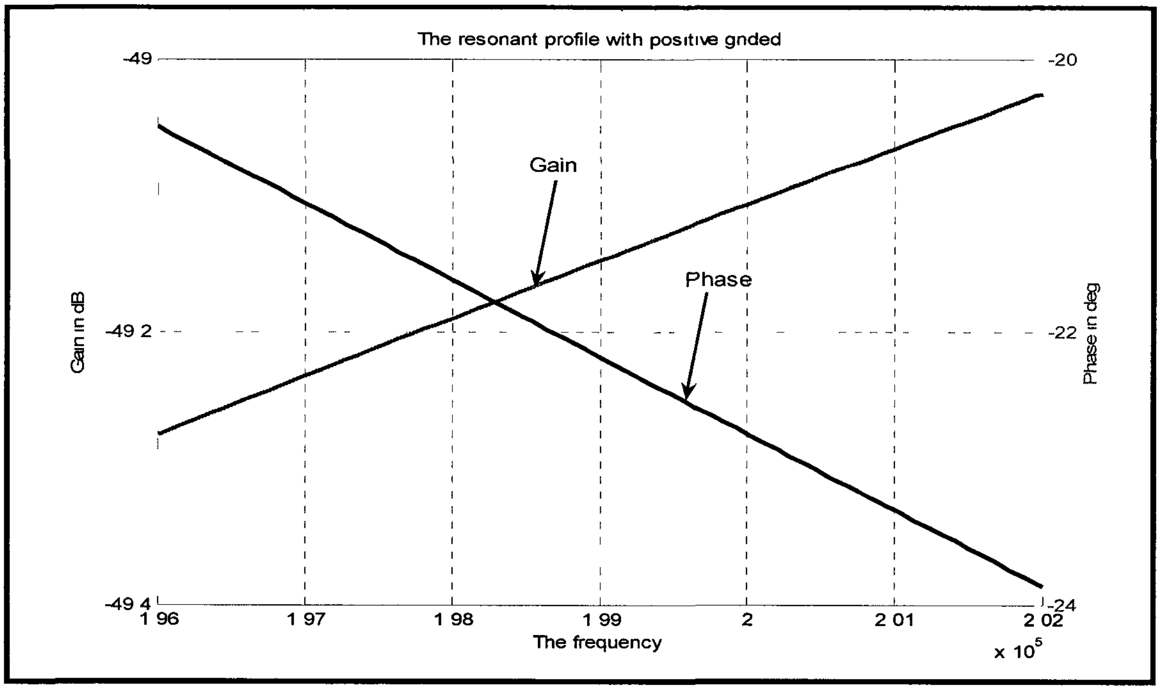

Figure 5.11 The resonant profile obtained at the output of differential amplifier when its positive input is grounded

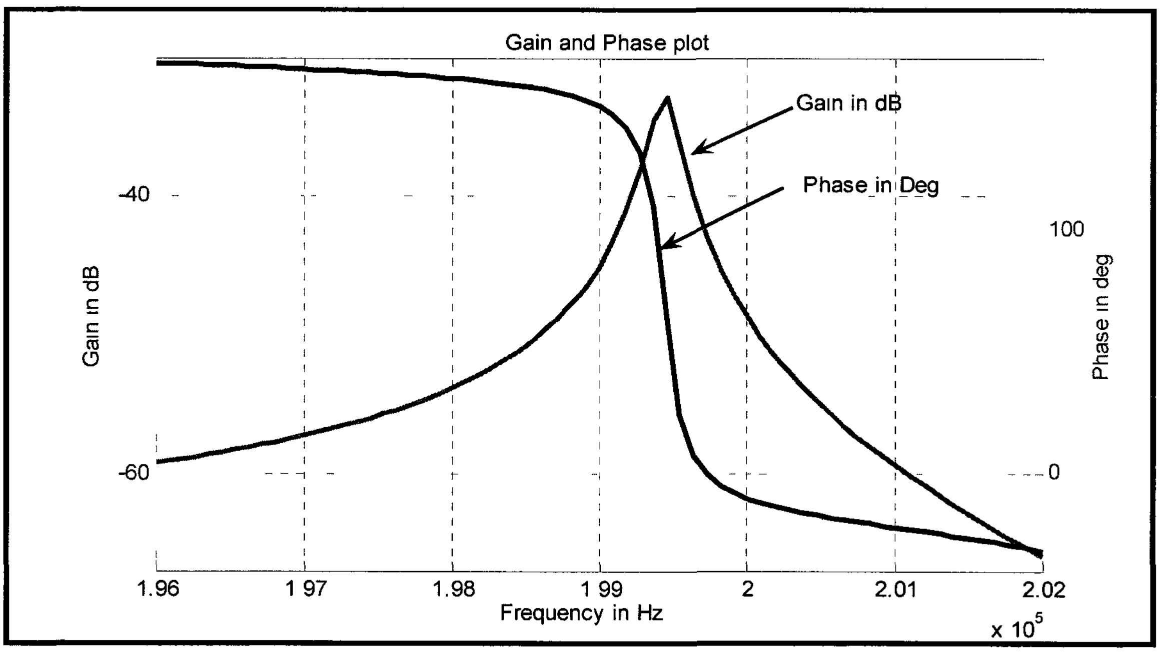

Figure 5.12 The gain and the phase profiles of the sample showing the perfect parasitic cancellation with 180 ° phase difference

The variable capacitor C3 has a primary role to play in cancelling the parasitic capacitance. In this dissertation, only one capacitor was kept as a variable, but if needed, more than one capacitor can be made a variable to increase the compensation range. In order to study the effects of the variable capacitance, the response of the MEMS resonators at different values of capacitance (20 pF, 50 pF, 100 pF and 300 pF) was simulated. Figures 5.13 and 5.14 show the gain and phase profile of the MEMS resonator with parasitic cancellation circuit. It can be seen that the dynamic range has increased from 20 pF to 50 pF, but, comparing it to others, the response of both signals is inverted. As the capacitance value was increased to 100 pF, the resonant profile showed the cancellation of parasitic capacitance. But, when the value was increased to 300 pF, the anti resonance shifted from being below the series resonance to being above.

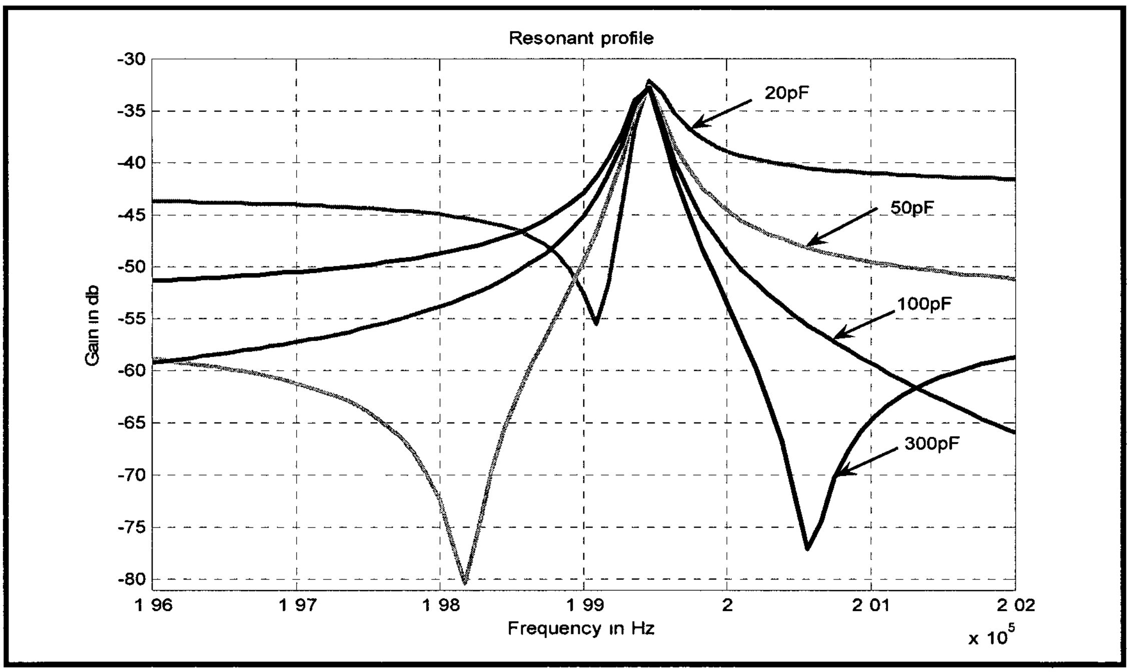

Figure 5.13 The resonant profiles obtained with different values of the variable capacitance

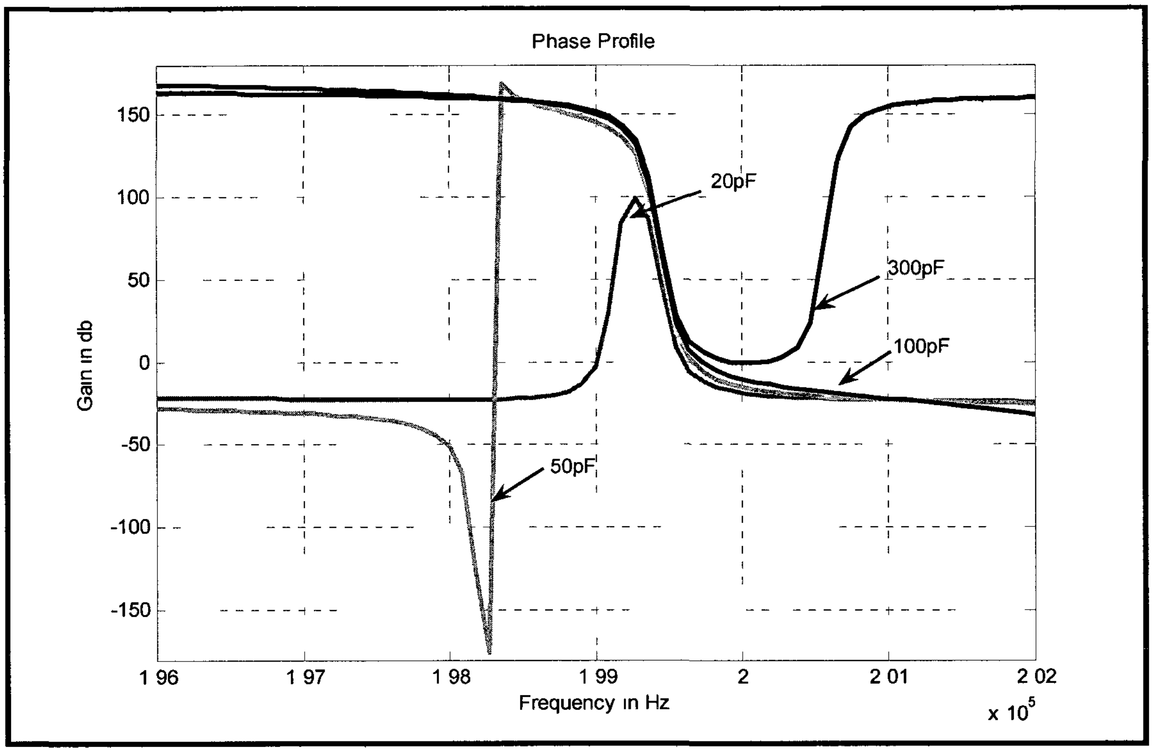

Figure 5.14 The phase profiles obtained with different values of the variable capacitance

It can be deduced from the pattern that if the value of the variable capacitance is less than 100 pF, (before the point when parasitic is cancelled), the negative input of the differential amplifier dominates and the response of the system is inverted. But, when the capacitance is more than 100 pF the positive input is dominant and the response of the signal shows the parasitic effect in the lower second half of the signal.

The parasitic cancellation circuits discussed above used the opamps in the inverting mode. Figure 5.15 shows the parasitic cancellation circuit with the opamps used in the non-inverting mode. The advantage of this mode is the infinite input impedance. Every other part of the circuit remained the same, and hence, the dependency of the parasitic cancellation on the variable resistor R7. This circuit was used in the dissertation to cancel the parasitic capacitance and the results are presented in Section 6.9. Figure 5.16 shows the gain and phase profile obtained using this circuit.

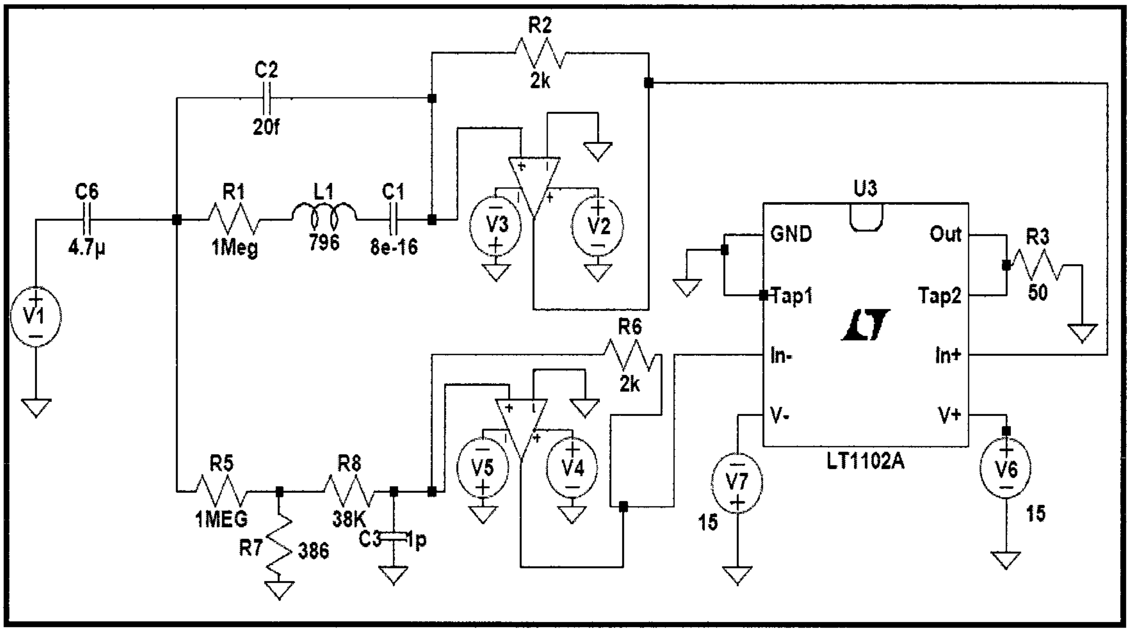

Figure 5.15 External parasitic cancellation with opamps used in non-inverting mode

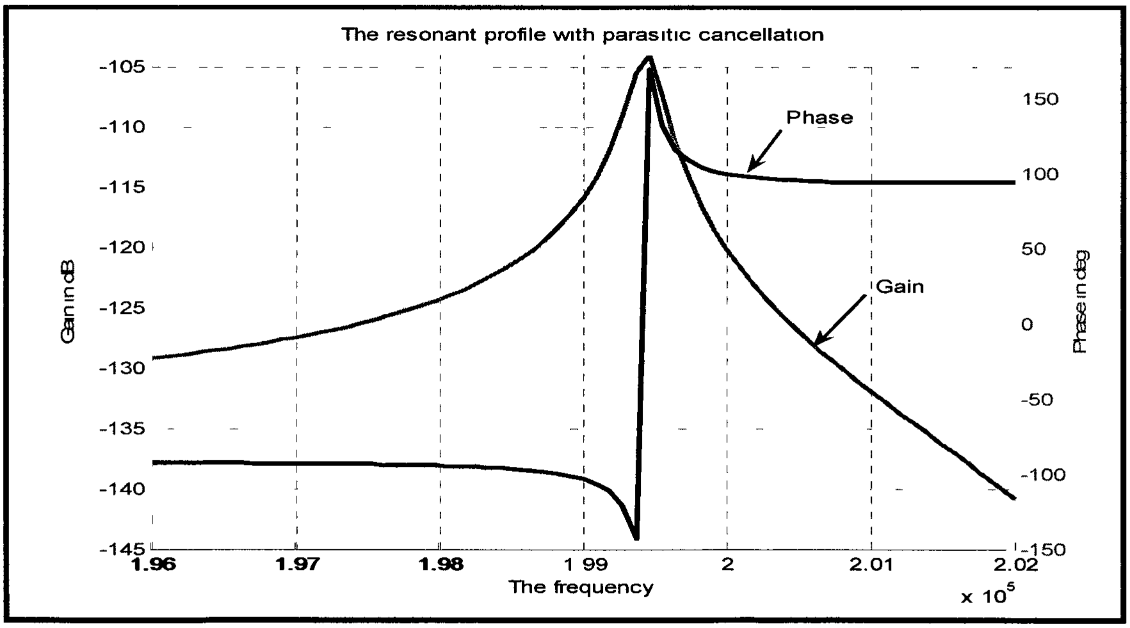

Figure 5.16 The gain and the phase profiles of the sample showing the perfect parasitic cancellation with 360 degrees phase difference

5.4. Calculation of dB Levels in the Circuits

Although it is shown in the circuits above that the perfect cancellation could be obtained with the T-network of capacitances, in some MEMS devices, this alone was insufficient. In testing the MEMS devices using the fabricated PCBs, it was seen that the dB levels at the inputs of the differential amplifier were not the same and the phase difference was not 180°. In this case, a combination of resistors was used to adjust the dB levels. The low pass filter (LPF) and high pass filter (HPF) circuits were used to adjust the phase difference. Figure 5.17 shows the only resistive network that provides the -40 dB gain, as calculated by Equation 5.5.

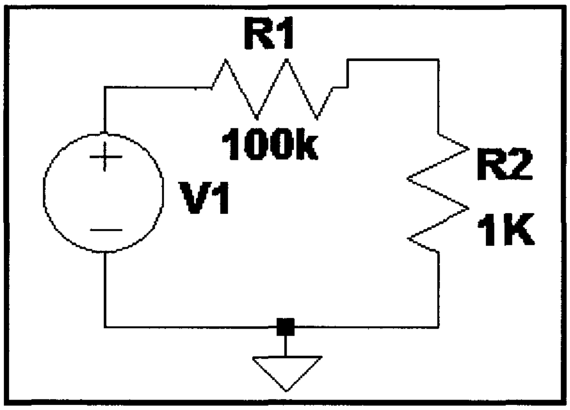

Figure 5.17 The circuit with simple voltage source and resistors

$$Gain = 20\log\left(\frac{R2}{R1}\right) \tag{5.5}$$

$$= 20\log\left(\frac{1e3}{1e5}\right)$$

$$= -40 \text{ dB.}$$

In order to obtain a -60 dB signal from the circuit given above that provides -40 dB signal otherwise, a combination of resistors (R3 and R4), as shown in Figure 5.18 can be used. When additional gain is needed, a combination of resistors can be used to increase the gain. Figure 5.19 shows the wide range of 1 MHz over which the signal remains stable.

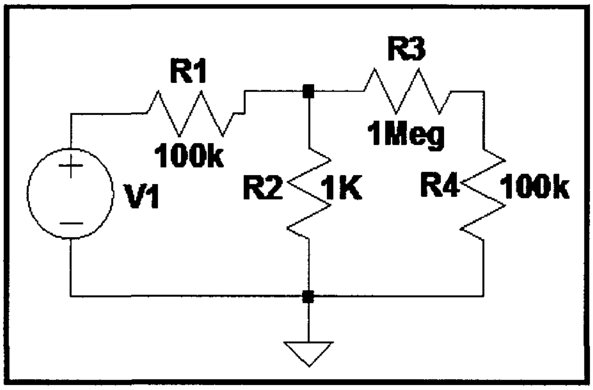

Figure 5.18 The circuit used to obtain the desired dB level of -60 dB

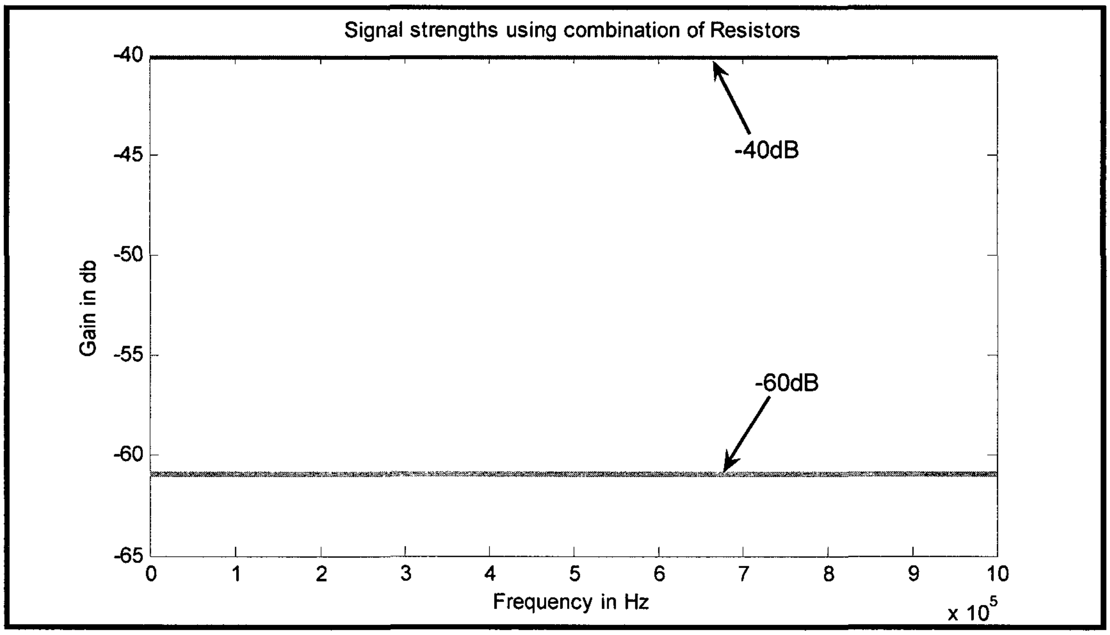

Figure 5.19 The signal strength of -40 dB at R2 and -60 dB at R4

As was mentioned before, the gain and the phase of the measured signal at the inputs of the differential amplifier should be the same in order to cancel the parasitic capacitance. But, when the inputs are out of phase by some degrees, it can be adjusted by using the LPF and HPF circuits. For example, if the phase difference is 136 °, then to get the phase difference of 180 °, 44 ° degrees is to be added to one of the inputs. As it requires a positive phase to be added to the circuit, a high pass circuit can be used, as shown in Figure 5.20. One of the disadvantages of using the HPF/LPF to adjust the phase is that there is a slight loss in the gain as shown in Figure 5.22. Using the resistive network, this loss in gain can be adjusted. Equation 5.6 shows the formula used to calculate the *R* and *C* values when the phase and the resonant frequency to be adjusted is known.

$$\phi = \tan^{-1}\left(\frac{1}{2\pi f RC}\right) \tag{5.6}$$

If, $f = 200$ kHz; $\phi = 44$ °,

Then $RC = 7.95\times10^{-7}$,

so $R = 2$ kΩ, $C = 0.4$ nF.

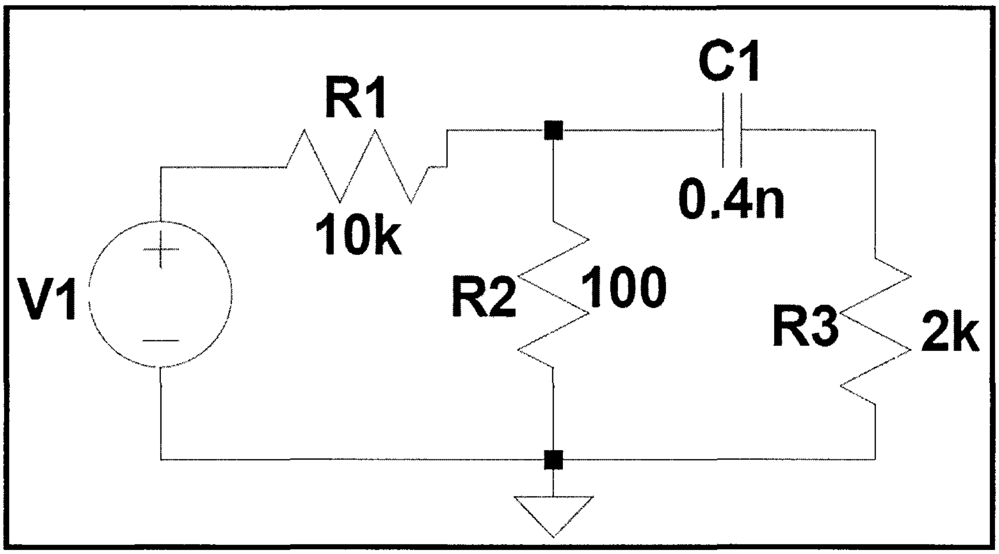

Figure 5.20 The circuit with RC combination for HPF setup

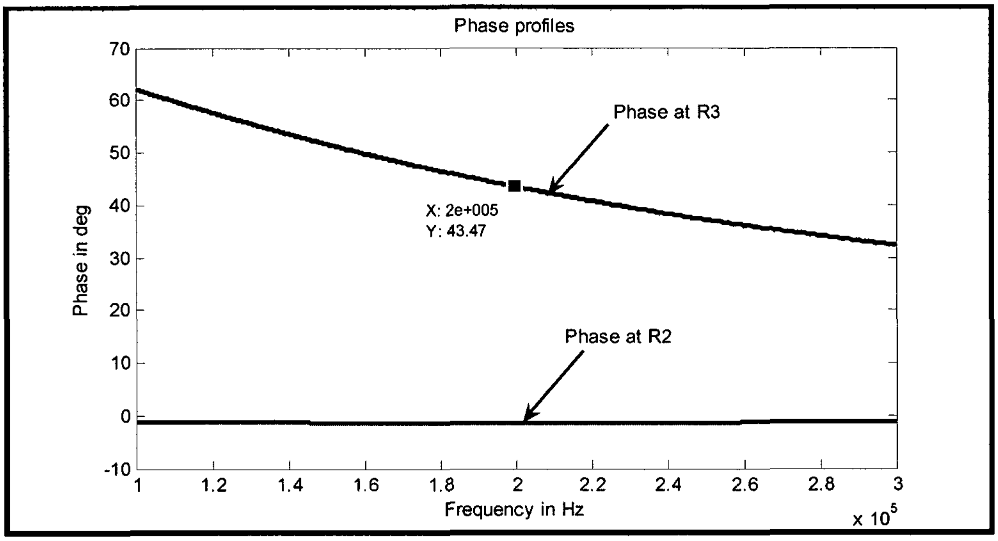

Figure 5.21 Phase profiles obtained with the HPF. The phase is 43.47 deg at 200 kHz

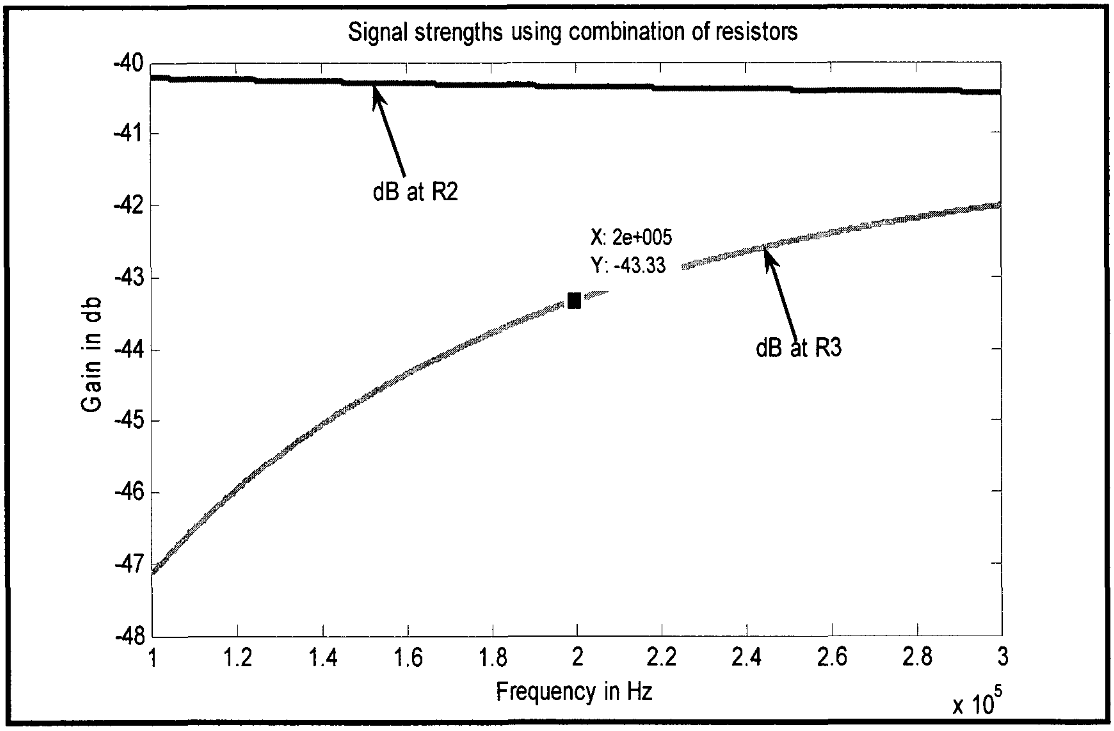

Figure 5.22 dB profiles obtained with the HPF. The dB value at 200 kHz is -43.33 dB

The 3 dB loss shown in Fig 5.20 can be adjusted using the variable resistor(s) for R1 and/or R2. It was observed that the number of degrees required for the phase difference to be 180 ° defer from device to device. Hence the variable resistor and/or capacitor were used at R3 and/or C1 to make the circuit compatible with all the devices.

If a device requires negative phase to be added to the circuit, then a low pass filter circuit, as shown in the Figure 5.23, can be used. For example, if the phase difference is 210 °, then 30 ° needs to be subtracted from one of the inputs to get a phase difference of 180 °. The value of *R*and *C* for a known phase difference of 30 ° is calculated using Equation 5.7. Figures 5.24 and 5.25 show the gain and phase profile obtained by appending the low pass filter to the circuit shown in Figure 5.17. It can be seen that the gain dropped by 1 dB when the phase was adjusted for 30 °. Again, this gain can be compensated using the resistive network shown in Figure 5.18.

$$\phi = \tan^{-1}\left(-2\Pi f\, RC\right) \tag{5.7}$$

If, $f = 200$ kHz; $\phi = 30$ °,

Then $RC = 4.59 \times 10^{-7}$,

so $R = 1$ kΩ, $C = 0.46$ nF.

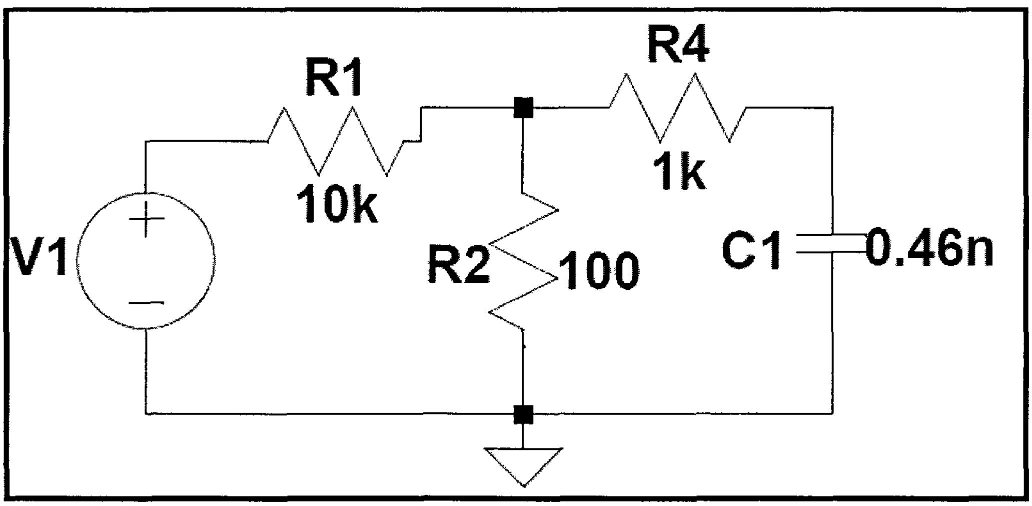

Figure 5.23 The circuit with the LPF assembly

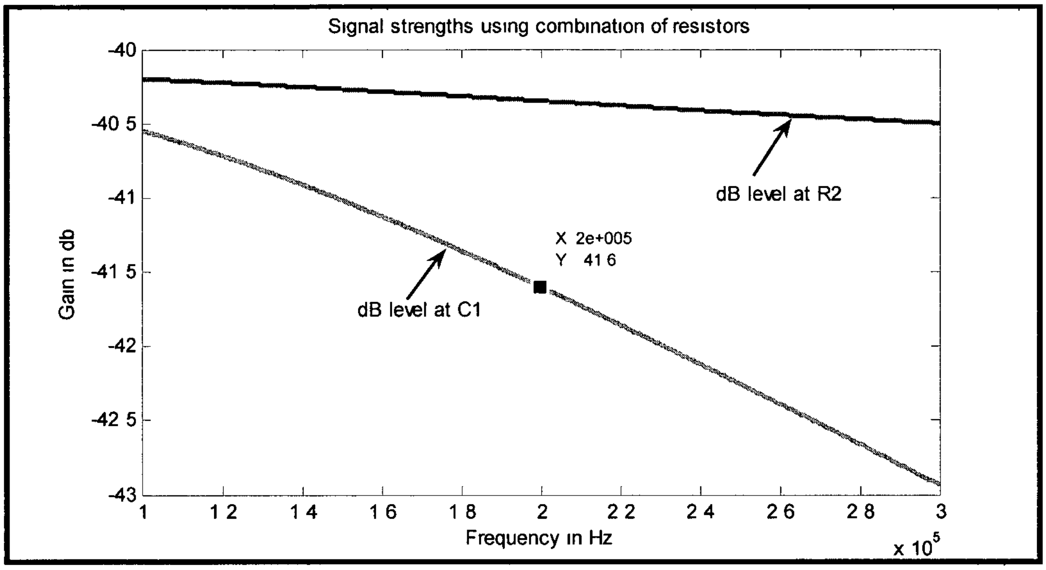

Figure 5.24 Gain profiles for the LPF

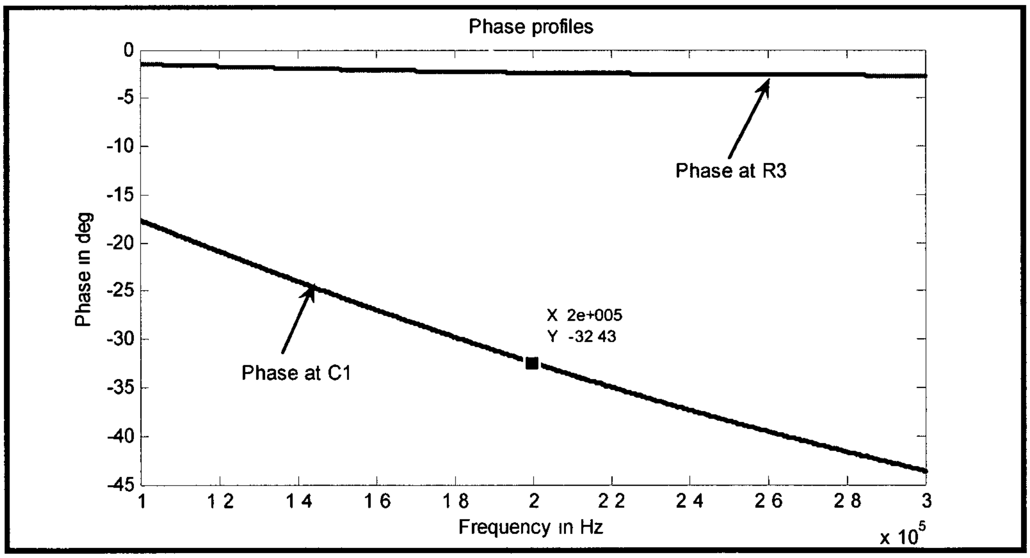

Figure 5.25 Phase profile for LPF

5.5. Summary

LT Spice simulations of the circuits used in this dissertation were presented in this chapter. Effects of parasitic capacitance on the MEMS response were analyzed and external parasitic cancellation circuits were simulated. It was found that for some devices, the use of a low pass and high pass filter may be needed to adjust the gain and phase on the individual inputs of the op-amp to obtain the same gain at the inputs and 180 ° phase shift between the inputs.

CHAPTER 6

RESULTS OBTAINED

The fabrication process of the different resonator types has been discussed in the previous chapters. The performance of a resonator is characterized by its quality factor and signal strength. In this chapter, the results obtained from the beam resonators with the introduction of the cavity and getter is presented along with a performance comparison. The porous silicon getter is also compared to the commercial SAES getter for the getter capacity. The Bode Network Analyzer was used to measure the resonant frequency and the error on this device was ± 0.1 dB on Gain scale and ± 1 Hz on frequency scale.

6.1. Beam Resonators

The beam resonators have the following advantages:

1) Robustness:

   The beams are simple designed long (in millimeters) and slender rectangular structures clamped at one or both ends. Each MEMS device may have a single beam structure or a combination of them depending upon the design and need. Because of the large spring constant and small area, they are less susceptible to stiction.

2) Lateral detection:

In surface micromachining, the beams are commonly actuated laterally, parallel to the substrate. This provides the advantage that the beam is subjected to a shear flow damping, which is less significant than squeeze film damping. The lateral movement lends itself to capacitive sensing with lateral electrodes that provides excellent noise performance and low power consumption.

6.2. Generation 1: Beam Resonator

The first generation of beam resonators was designed for a resonant frequency of 60 kHz. Figure 6.1 shows the schematic of the testing circuit. A sine wave input with a frequency sweep is fed to the resonator. In the presence of a bias voltage V_T and the sine wave input, the capacitance between the beam resonator and the sensing pad changes with the motion of the beam. The inset on the top shows the schematic of the lateral motion of the resonator and the change in capacitance with the motion. The bottom inset shows a metal plate (bronze in our case) with XYZ probe stages mounted on it using screws that connect to the contact pads on the resonator through the probes. The resonator is connected to the test circuit using the BNC connectors on the circuit and bronze plate. The signal from the change in capacitance is amplified by an operational amplifier. The output from the operational amplifier serves as an input to the Bode Network Analyzer that measures the resonant profile of the beam resonator. Figure 6.2 shows the measured transmission curve of the beam resonator. The peak point in the profile indicates the resonant frequency f_0 of 57 kHz. The signal height was 4.5 dB and the quality factor was approximately 2,900. The response of the beam resonator at different pressures for a constant bias voltage of 15 V is presented in Figure 6.3. The resonant profile of the resonator at a constant pressure of 6.0 mTorr at different voltages ranging from 3.0 - 15 V was measured and is presented in Figure 6.4. The 3 dB quality factor of the resonator at 15 V was measured at different pressures and is shown in the Figure 6.5. The change in the quality factor up to a pressure of 100 mTorr is smooth and not as rapid as from 100 mTorr to 1 Torr. This is because until 100 mTorr, it is the intrinsic regime where the air damping does not contribute significantly and other loss mechanisms dominate. However, beyond this pressure the molecular regime starts and the quality factor is dependent on the individual molecular interactions, and hence, the increase in pressure significantly affects the measured quality factor. Beyond 10 Torr the viscous regime starts where the mean free path for the air molecule is 65 nm. As this is small in comparison to the device's dimensions, the quality factor is unaffected by the molecular motion. In our case, this data is unavailable because the signal amplitude (gain) beyond 2 Torr was less than 3 dB, thus making it impossible to measure the quality factor.

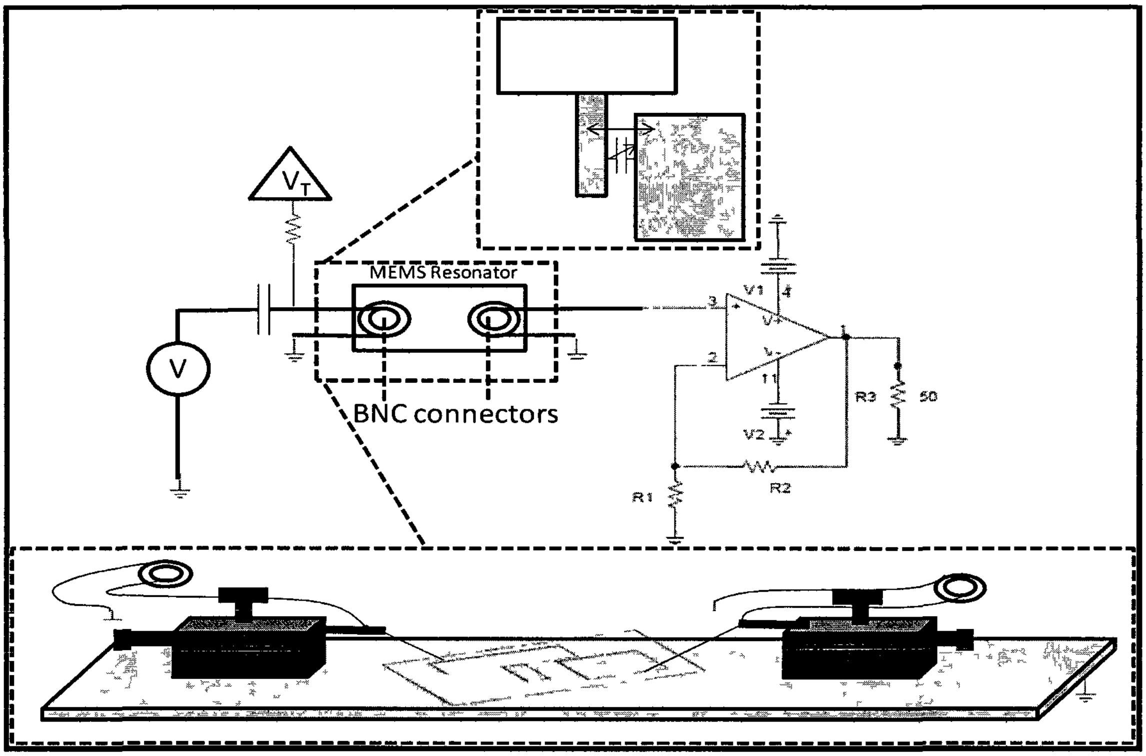

Figure 6.1 The schematic of the Generation 1 beam resonator test circuit

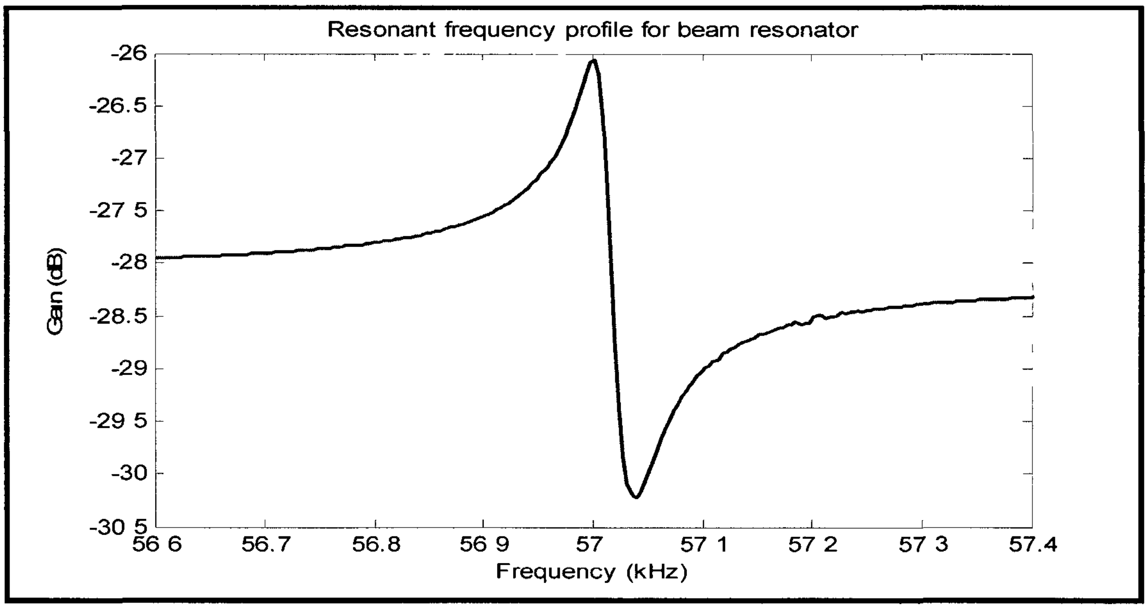

Figure 6.2 The resonant profile of the beam resonator at a pressure of 7 mT and a bias voltage of 15 V

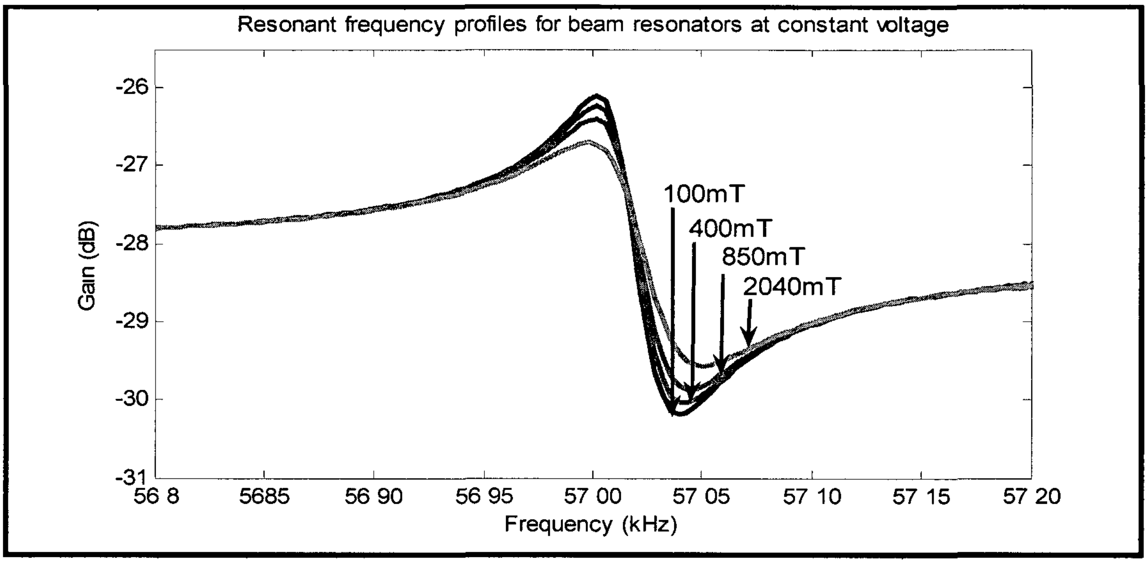

Figure 6.3 Resonant profiles of the beam resonator at constant voltage of 15 V at different pressures

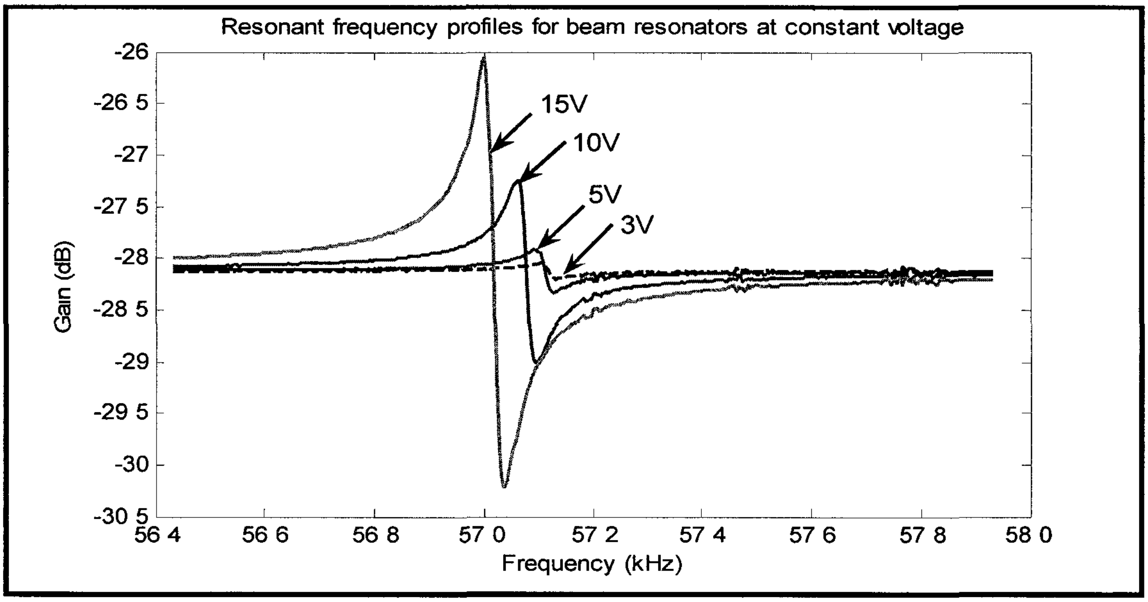

Figure 6.4 Resonant profiles for the beam at different voltages for a constant pressure of 6 mTorr

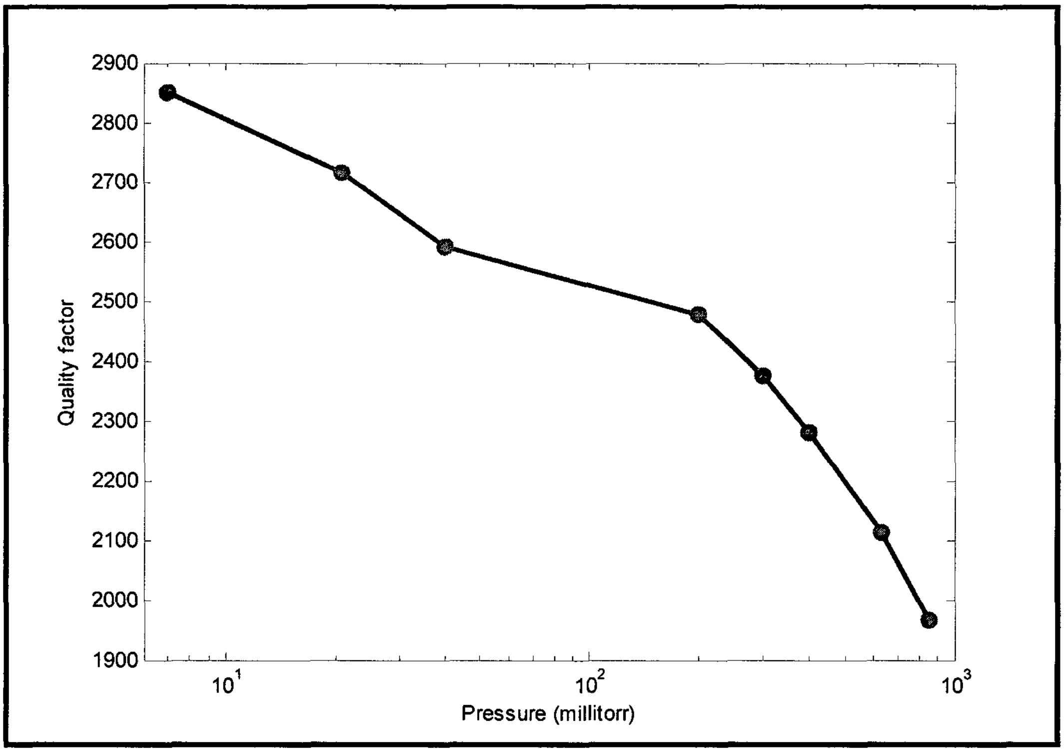

Figure 6.5 Quality factor profile of the beam resonator for different pressures at 15 V

6.3. Generation 2: Tuning Fork Resonator

The second generation resonators were modified into the tuning fork resonators. The motivation to use this resonator design is its wide use in gyroscopes, accelerometers and oscillators. Apart from this, the chosen design provides better isolation between the sense and drive electrodes. They were designed for a resonant frequency of 200 kHz. The test setup is similar to the Generation 1 beam resonators, as shown in Figure 6.6. The inset on the top shows the movement of the tines of the tuning fork. The capacitance between the tines of the tuning fork and the beam changes as per the motion of the tuning fork resonator. Hence, a differential change in capacitance is amplified by the operational amplifier and translated into a readable/recordable signal on the computer using the Bode Analyzer. The resonance profile obtained from the device is shown in Figure 6.7. The measured resonant frequency was 243.73 kHz and the dynamic range was approximately 6 dB. The quality factor at 20 V and 60 mTorr was recorded to be Q = 65,000. The response of the resonator for different pressures at 20 V is presented in Figure 6.8. The quality factor of the resonator at different pressures and a constant 20 V is presented in Figure 6.9. The behavior of the resonator in different pressure regimes has been discussed in Section 6.3. For this resonator, the ratio of length to thickness of the resonator is approximately 56 μm. As per the reference [66], for the *l/d* ratio of 56 μm the intrinsic regime is approximately 1 Torr and below, the molecular regime is from 1-10 Torr, and the viscous regime is from 10 Torr and higher. A better understanding of the behavior of the resonator in these pressure regimes can be obtained from Figure 6.9. It can be seen that, below 1 Torr (which is the intrinsic regime), the change (decrease) in the quality factor is slow compared to the change between 1 Torr to 5 Torr (the molecular regime). In the molecular regime, the quality factor is dependent on the individual molecule interactions, and hence, the increase in pressure significantly affects the measured quality factor. In the viscous regime (>5 Torr), the mean free path for the air molecule is 65 nm. As this is small in comparison to the device dimensions, the quality factor is unaffected by the molecular motion and hence the change in quality factor in this regime is almost constant.

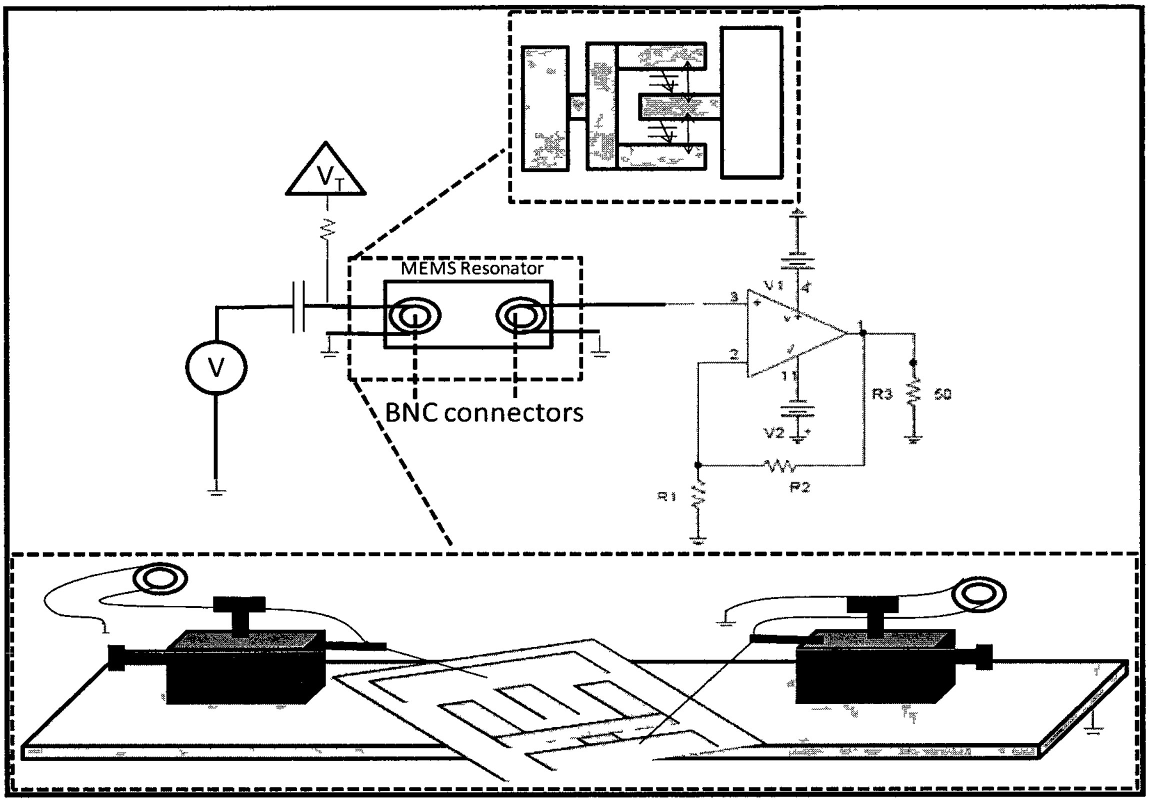

Figure 6.6 The schematic of the 2nd generation beam resonator test circuit

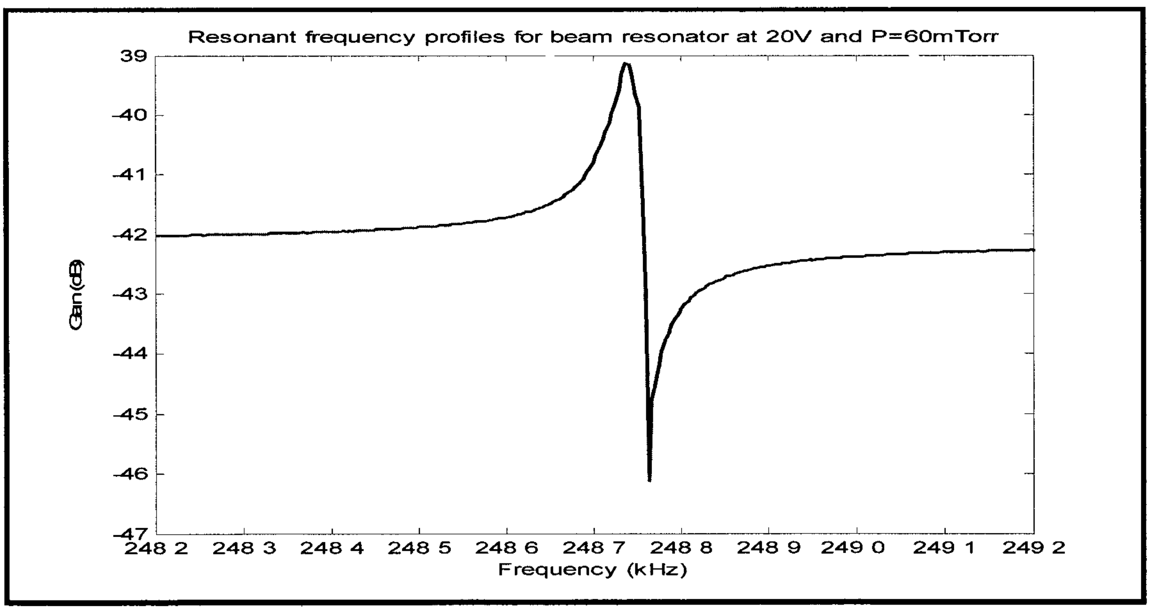

Figure 6.7 Resonant profile of a beam with f_0 = 248 kHz

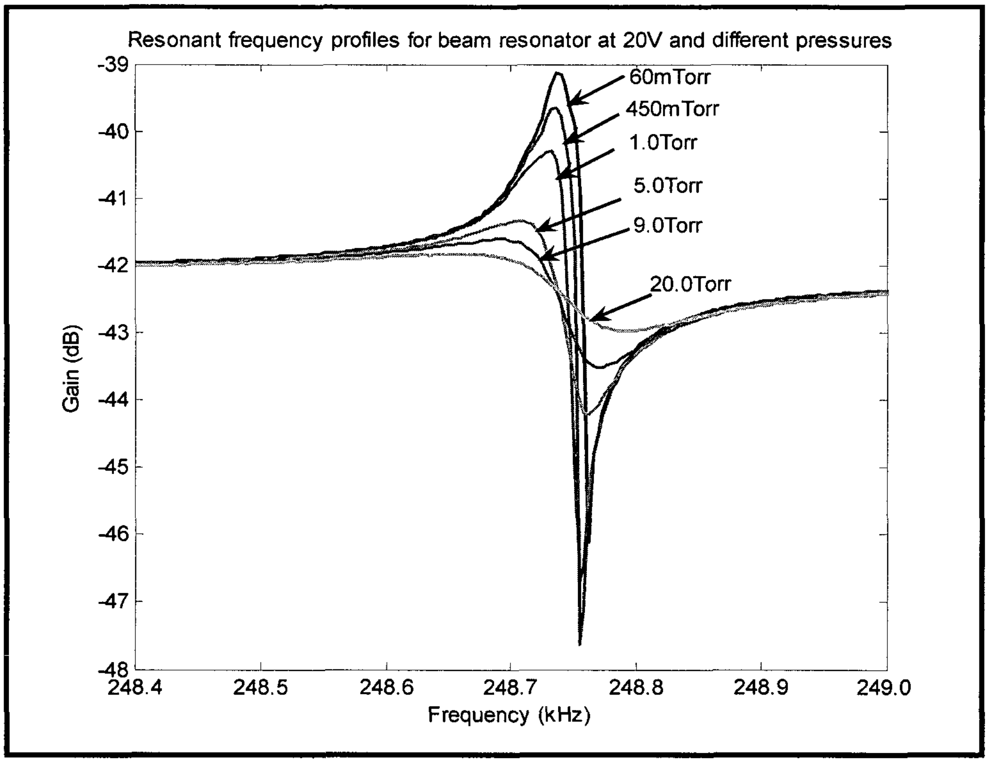

Figure 6.8 Resonant profiles of the beam at different pressures

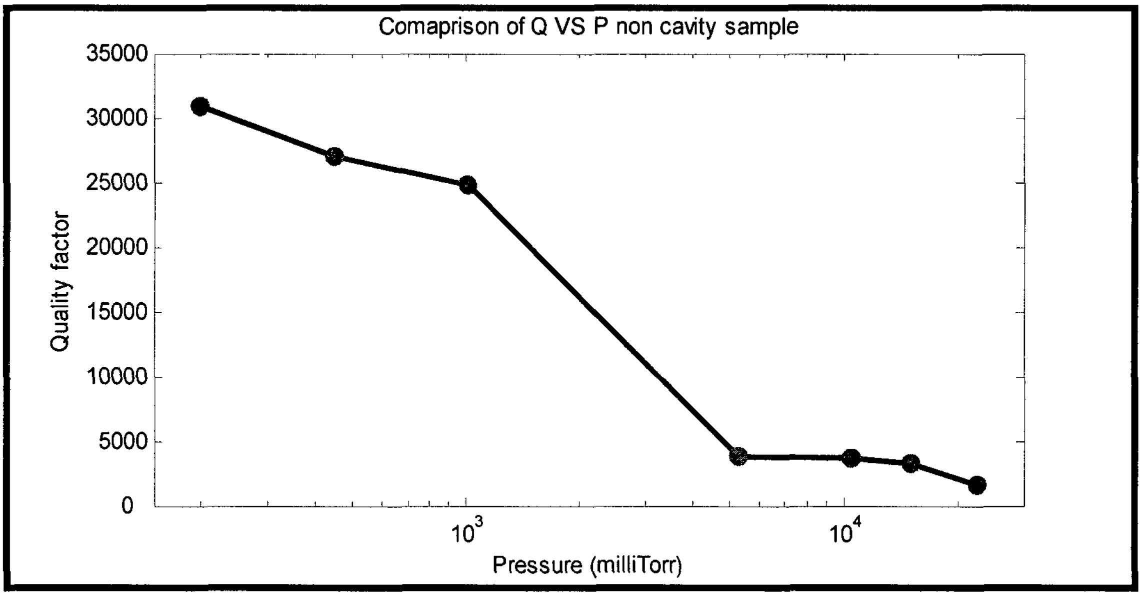

Figure 6.9 The quality factor of the beam resonator at different pressure for constant 20 V

6.4. Cavity in the Substrate of the SOI Die

The process used to obtain a cavity in the substrate has been discussed in Chapter 3. The results obtained by these devices are presented in this section. The test setup used is the same as shown in Figure 6.6. The resonant profile of the device with a cavity is shown in Figure 6.10. The resonant frequency is 247.25 kHz, dynamic range of approximately 7 dB and a quality factor of 85,000 at 20 V and 36 mTorr of pressure. The response of the resonator for different pressures at a constant voltage of 20 V is presented in Figure 6.11. It is seen that with the increase in pressure from 36 mTorr to 1.2 Torr, the change in the response of the resonator is almost gradual and similar to the sample without a cavity. The reason for this linear change in both kinds of devices is their having the same length to the thickness ratio and, hence, the same range of intrinsic pressure regime. The quality factor of the device at a constant voltage of 20 V and different pressures ranging from 35 mTorr to 20 Torr, is presented in Figure 6.12. It can be seen that the intrinsic regime ends at approximately 1 Torr, just as the device without the cavity, but the molecular regime is extended from 5 Torr to 11 Torr and the viscous regime starts from 11 Torr onwards. The extended molecular regime is due to the cavity in the substrate. In the molecular regime, the interaction between the individual gas molecule and the device structure is the cause of damping. With the introduction of a cavity in the substrate, these interactions can be reduced and the effect of air damping is decreased. A more detailed description of advantages of a cavity is presented in Section 6.5.

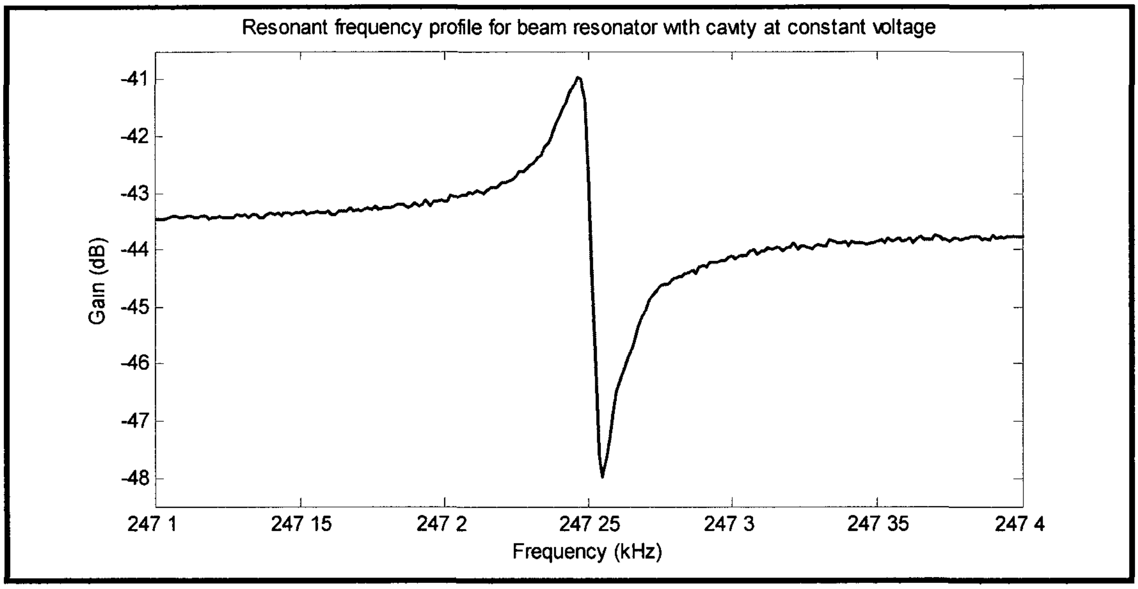

Figure 6.10 Resonant profile of the device with a cavity in the substrate

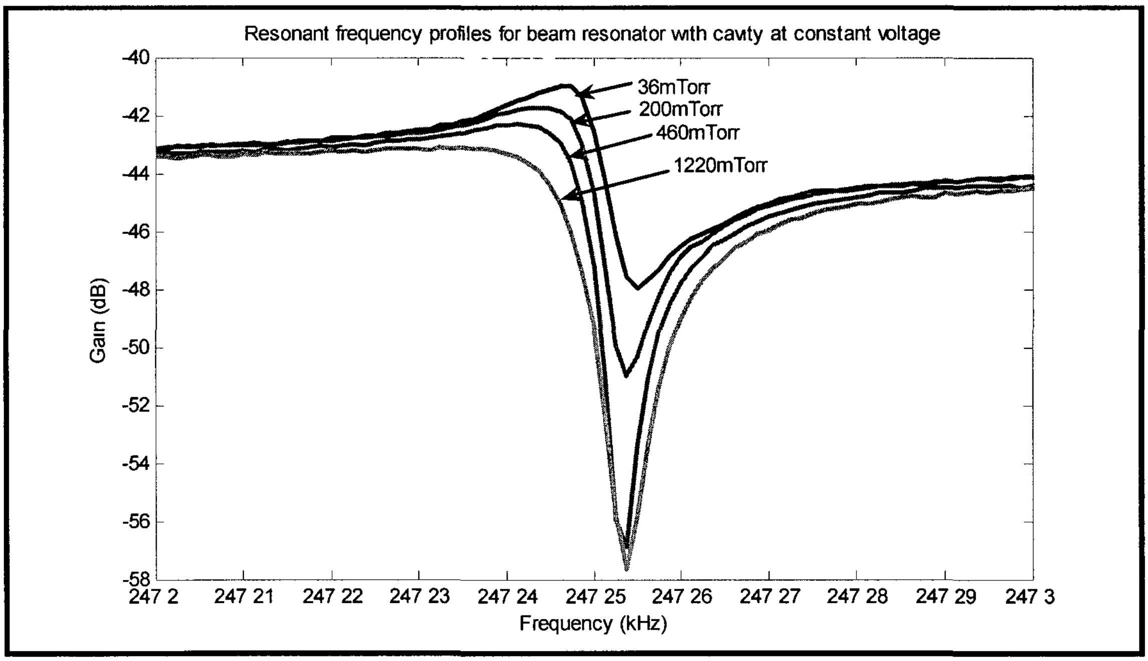

Figure 6.11 Resonant profiles at different pressures for device with a cavity in the substrate

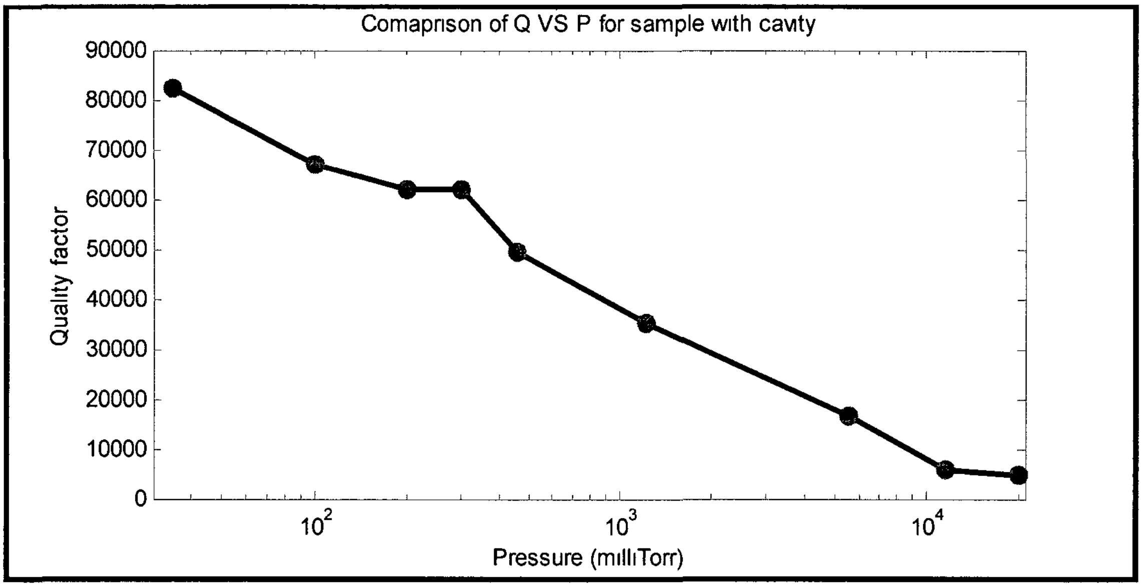

Figure 6.12 Quality factor of the beam resonator with a cavity in the substrate at different pressures

6.5. Comparison of Quality Factors of Devices With and Without a Cavity in the Substrate

The quality factor measured as a function of pressure for the devices with and without cavity was presented individually in the previous sections. Figure 6.13 presents the comparison of these devices in one graph. It can be seen that the device with a cavity had a quality factor 2-3 times higher than the device without a cavity at the intermediate pressures. At low pressures (less than 100 mTorr), the intrinsic mechanical quality factor dominates and hence the quality factors converge. Therefore, the cavity increases the quality factor of the devices significantly.

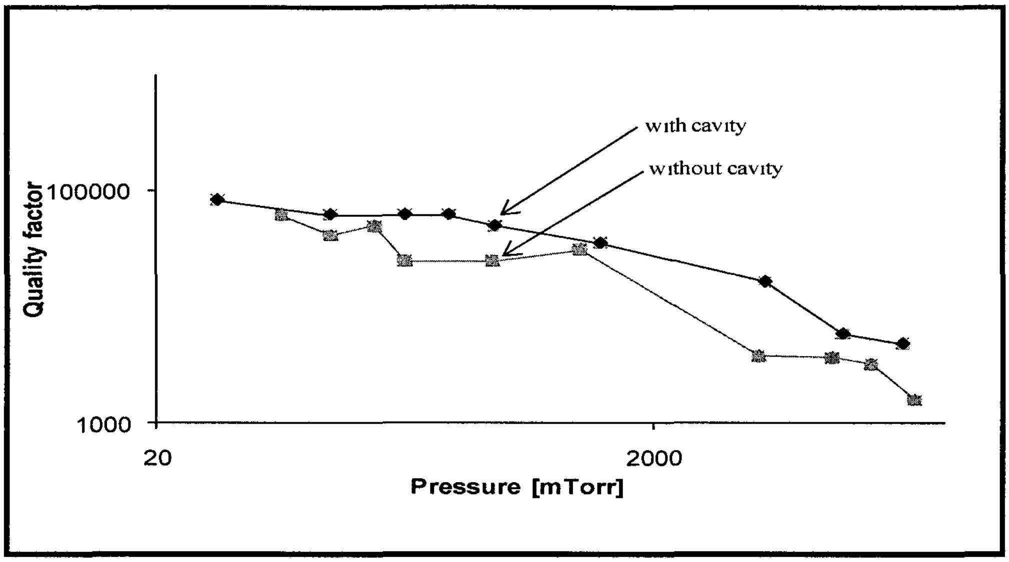

Figure 6.13 Comparison of quality factors at different pressure for the device with and without a cavity

6.6. Discussion on Benefits of the Cavity

The benefits of a cavity in the substrate of the MEMS devices are:

1. The parasitic capacitance to the substrate is reduced. The parasitic capacitance C_P is related to the device-substrate gap d by

$$C_P = \frac{\varepsilon_o A_{el}}{d} \tag{6.1}$$

where A_{el} is the area and ε_0 is the permittivity of free space. Hence, with an increase in the depth of the cavity, the parasitic capacitance C_P shown in Figure 6.14 is decreased.

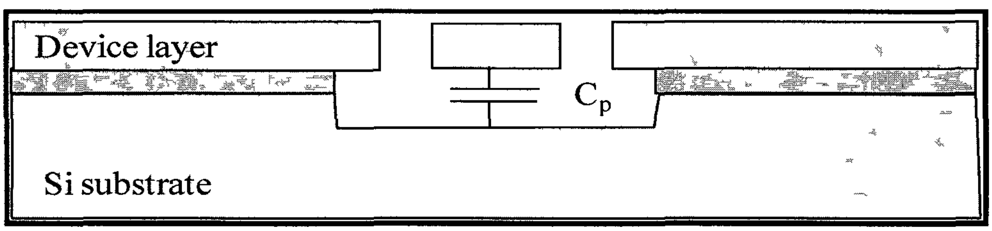

Figure 6.14 Schematic of device with cavity showing the parasitic capacitance between the device side and the substrate

According to Equation (6.1), the increase in distance of movable structure to the substrate from 2 to 10 μm reduces the parasitic capacitance by a factor of five.

2. The air damping is reduced. The main damping mechanism are the squeeze film damping between the moving resonator and the fixed electrode caused by the air flowing from the gap to the empty space above the device and the shear damping between the device and the substrate. By providing additional space under the device, the travel length for the air in between the electrodes is effectively reduced by half with air escaping above and below the structure. In theory, this reduces the air damping by a factor of six. If shear damping (Couette damping) dominates, the quality factor is related to the distance between the movable structure and substrate [67, 68] by

$$Q = \frac{d\sqrt{mk}}{\mu A} \quad , \tag{6.2}$$

where d is the distance between the device layer and the substrate, m is the resonator mass, k is the spring constant, μ is the viscosity, A is the device area. According to Equation (6.2), a 5x the improvements in the quality factor is expected. The obtained increase in the quality factor was less, about 2-3x, which is probably due to the edge effects in gas flow.

3. The cavity under the resonator essentially eliminates the stiction problem where the device gets stuck to the substrate. It was found that with the 10 μm cavity, even a millimeter long and slender, structures never get stuck to the substrate.

6.7. Bonded Cavity Sample

The benefits of MEMS encapsulation have been previously discussed. After achieving a 2x better quality factor with the cavity device in comparison to a non cavity device, the device was hermetically encapsulated to study the behavior of the resonator. The resonant profile obtained by a vacuum bonded sample is presented in Figure 6.15 (a). The measured dynamic range is only 0.12 dB, thus making the quality factor calculation impossible. There are two possible reasons for this low signal strength: One, very high pressure in the bonded sample (in the order of hundreds of Torr) and second is a very high parasitic capacitance that makes it difficult to measure the original signal. Although pressure in the bonded sample cannot be reduced to improve the resonator response, the parasitic capacitance can be cancelled using an external circuit. The external parasitic cancellation circuit (discussed in Section 6.3) was used to cancel the parasitic capacitance. The signal obtained after the use of the cancellation circuit is shown in Figure 6.15 (b).

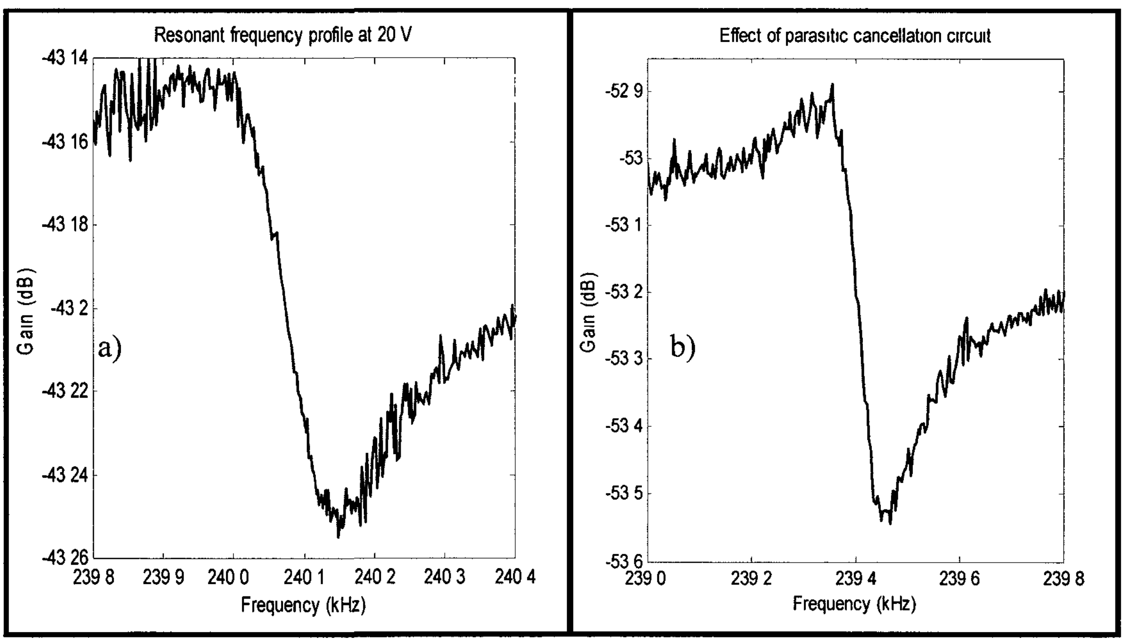

Figure 6.15 Resonant profiles of the bonded device with cavity at 20 V a) Without parasitic capacitance cancellation, and b) After parasitic capacitance cancellation

It can be seen that the dynamic range improved from 0.12 dB to 0.7 dB, but it was still not possible to measure the 3 dB quality factor. It was found that the reason was due to the chrome metal that was used to ground the substrate. It was found that chrome did not make a good contact to silicon, making measurements impractical. As a solution to this, the electroless Ni deposition process was chosen to coat the substrate and the contact pads of the bonded device with Ni.

6.8. Results from Ni Deposition

The 1:1 volume combination of Solution A ($NiSO_4.6H_2O$, $Na_4P_2O_7.10H_2O$, 58% NH_4OH) and Solution B ($((CH_3)_2NHBH_3)$) was used to deposit Ni on the substrate of the bonded SOI die and the contact pads. The composition of each solution is as follows:

Solution A:

$NiSO_4.6H_2O$ → 50 gm/l

$Na_4P_2O_7.10H_2O$ → 100 gm/l

NH_4OH (58%) → 45 cc/l

Solution B:

$((CH_3)_2NHBH_3)$ → 3 gm/l

An equal volume of Solutions A & B was prepared in a petri dish just prior to the deposition. The deposition rate for this combination is approximately 35 nm/min [69]. The experiment was carried out for 5 min and a Ni layer of 150 nm was obtained.

The bonded device was now tested for resonance using the Bode Network Analyzer. The resonant profile obtained from the device at 20 V, without using the parasitic cancellation circuit, is presented in Figure 6.16 (a). The dynamic range was measured to be 0.8 dB. It can be seen that the Ni deposition had made a significant change by increasing the dynamic range to 0.8 dB from 0.12 dB of non parasitic signal pre-Ni deposition. The resonant profile obtained from the device, after using the parasitic cancellation circuit at 20 V, is presented in Figure 6.16 (b). The dynamic range measured was 1.8 dB. It was still not possible to measure the 3 dB quality factor. In order to obtain high signal strength from a bonded device, the pressure in the device needs to be very low and the grounding of the substrate needs to be good with low impedance. The pressure in the bonded device is dependent on the device processing and the bonding process. In order to increase the vacuum in the bonded device, the bonding process was carried out by cleaning the vacuum chamber and its accessories before every use.

As the Ni deposition was post device fabrication and bonding processes, it did not serve the purpose of providing a strong grounding contact to the substrate. Hence, a new wafer was fabricated with an Au layer deposited on the Cr layer for strong grounding.

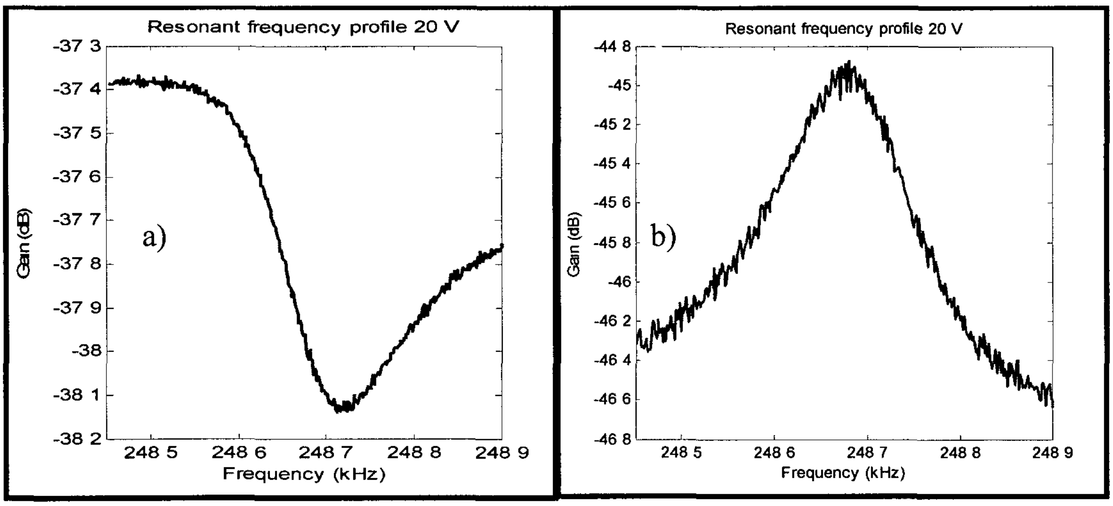

Figure 6.16 Resonant profiles of bonded device with Ni deposited over chrome a) Before parasitic capacitance cancellation, and b) After parasitic cancellation

6.9. Bonded Devices with Au as the Grounding Metal Layer

The device fabrication process of the gold deposited samples has been discussed in the section above. The devices were then anodic bonded with glass. In this section, the results obtained from these devices are presented. Figure 6.17 (a) shows the resonant profile of the resonator at 20 V. The signal strength of the resonator was measured to be 2.6 dB. The phase profile of the resonator is presented in Figure 6.18 (a) which shows the phase difference of only 22 °. In an ideal resonator where the parasitic capacitance is cancelled, the phase difference in the resonator profile is 180 ° when the signal is amplified using the non-inverting amplifier. The external parasitic cancellation circuit was used to cancel the parasitic capacitance. Figure 6.17 (b) shows the measured resonant profile after the parasitic capacitance is cancelled. Figure 6.18 (b) shows the phase profile obtained after using the parasitic capacitance. The phase difference of the resonator was measured to be 180 °, therefore indicating a complete parasitic capacitance cancellation. The signal strength is 7 dB and the quality factor is Q = 8,000. Hence, the deposition of the Au as the grounding metal and the use of the parasitic cancellation circuit had been successful in obtaining better results for the bonded MEMS resonators with a cavity in the substrate.

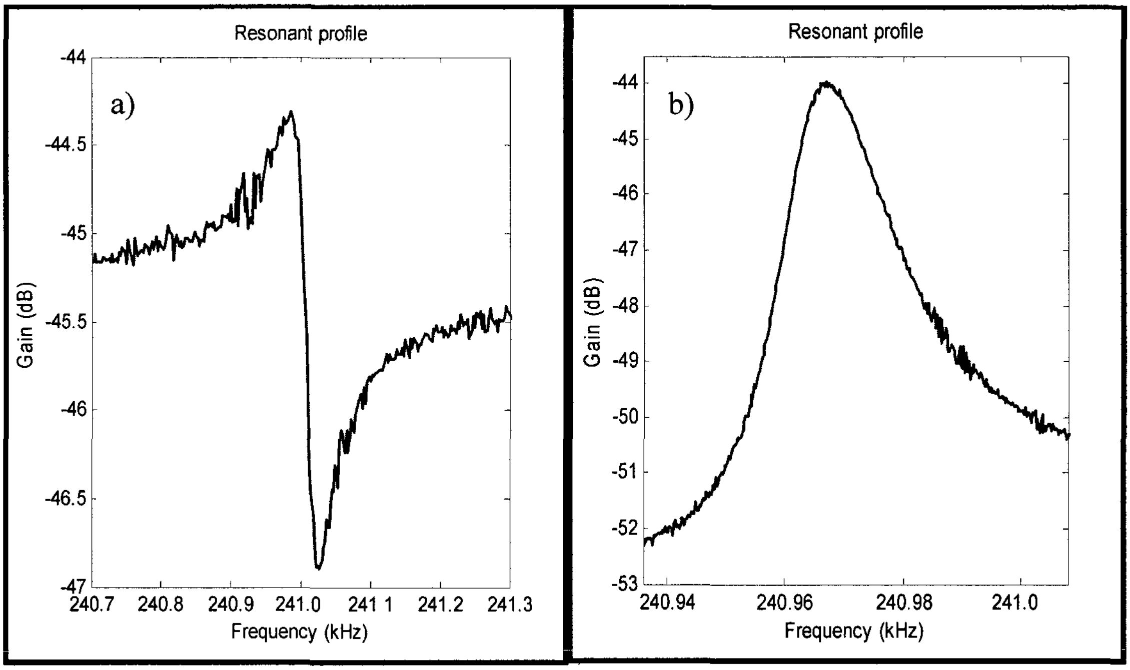

Figure 6.17 Resonant profiles at 20 V of the bonded device with cavity a) Before parasitic capacitance cancellation, and b) After parasitic cancellation

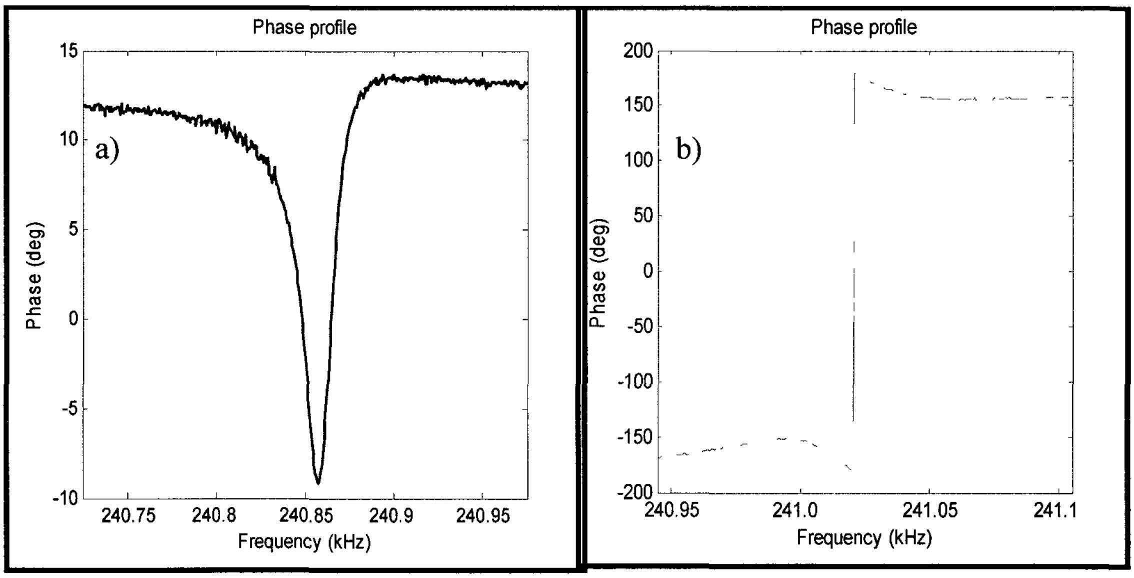

Figure 6.18 Phase profiles at 20 V of the bonded device with only cavity a) Before the parasitic cancellation, and b) After the parasitic cancellation

6.10. Bonded Device with Porous Silicon Getter

So far the benefits of a cavity in the substrate over a non-cavity sample and the advantage of using the Au layer in parasitic capacitance cancellation have been seen. In this section, the results obtained by augmenting the porous silicon getter layer to the cavity in the substrate are presented. The process of obtaining the porous silicon getter in the substrate was discussed in detail in Chapter 3. The resonant profile obtained by the bonded device with cavity and porous silicon getter in the substrate at 20 V is presented in Figure 6.19 (a). The signal strength was measured to be 6 dB with a 3 dB quality factor of 13,000. The phase profile of the device is shown in Figure 6.20 (a), which shows the phase difference of 36°. This clearly indicates the presence of parasitic capacitance. The external parasitic capacitance cancellation circuit was used to cancel the capacitance. The resonant profile obtained after using the cancellation circuit is presented in the Figure 6.19 (b). The dynamic range was 7 dB and the 3 dB quality factor measured was 14,000. The phase profile of the device is shown in Figure 6.20(b), which shows the phase difference of 180°, therefore indicating perfect parasitic capacitance cancellation.

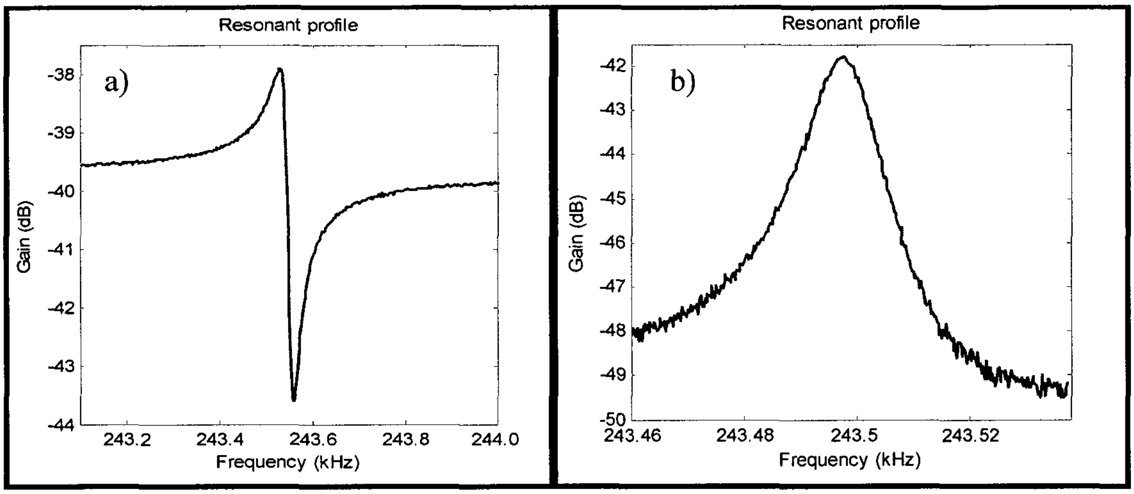

Figure 6.19 Resonant profiles at 20 V of the bonded device with cavity and porous silicon getter in the substrate a) Without parasitic capacitance cancellation, and b) After parasitic cancellation

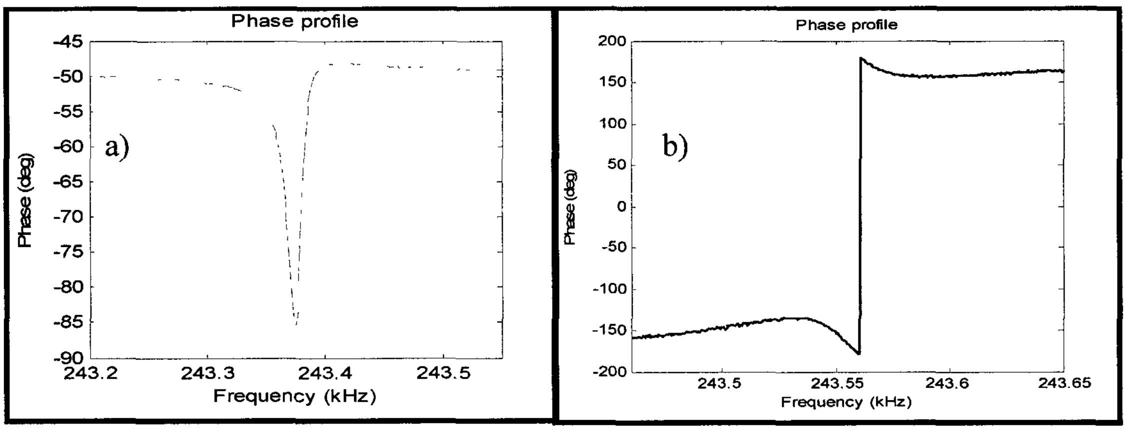

Figure 6.20 Phase profile at 20 V of bonded device with cavity and porous silicon getter in the substrate a) Without parasitic capacitance cancellation, and b) After parasitic cancellation

6.11. Comparison of the Getter and Non Getter Devices

The resonant profiles obtained by the devices with and without a getter have been individually presented in the Sections 6.2, 6.3, 6.4 and 6.10. In Figure 6.21, the resonant profiles obtained by the devices were compared in one graph. The quality factor at 20 V for the device with a getter was measured to be 14,000 and the one without a getter was measured to be 8,000. Hence, the device with a getter had a quality factor approximately two times higher than a device without a getter. As the device fabrication steps are the same for both the devices, the better performance of the device with a getter is due to the presence of porous silicon. Multiple samples were fabricated to confirm the performance of the porous silicon. The results are tabulated in Table 6.1. Figures 6.22-24 show the resonant profiles obtained by different samples.

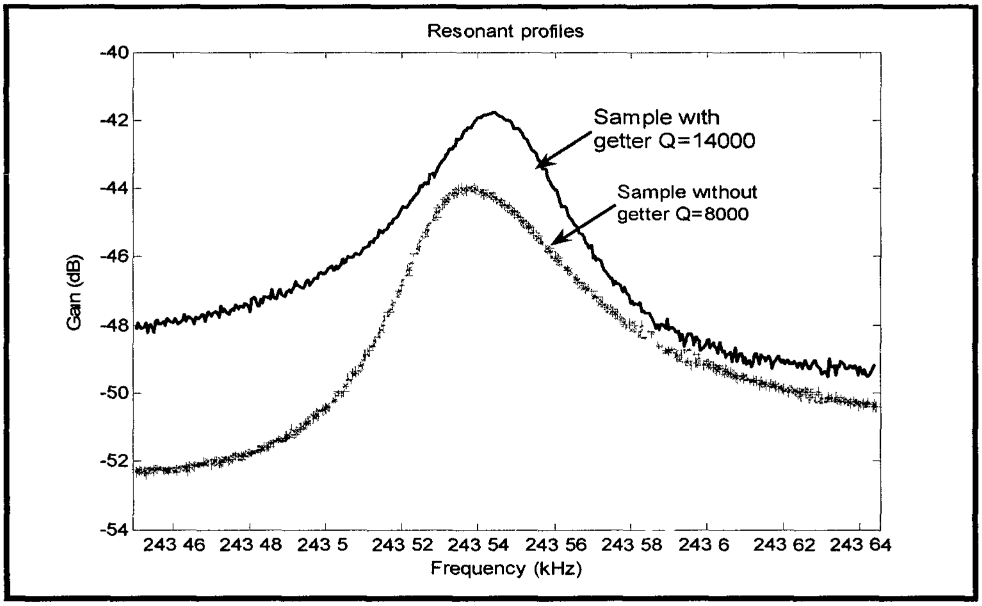

Figure 6.21 Comparison of resonant profiles of devices with and without a porous silicon getter

Table 6.1 Summary of quality factors obtained from different devices

	Q of devices with only a cavity	**Q of devices with a cavity and getter**
Batch 1	7,000	13530
Batch 2	5873	16083
Batch 3	2410	6701
Batch 4	1350	1600

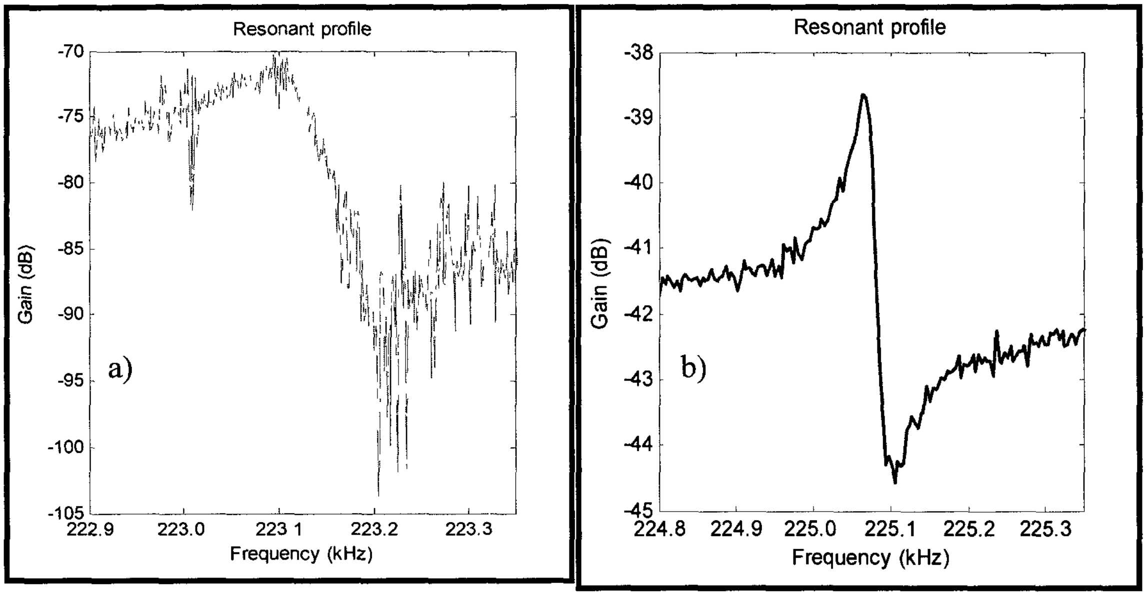

Figure 6.22 Resonant profiles of batch 2 bonded devices a) sample without getter Q = 5,900, and b) sample with getter Q = 16,000

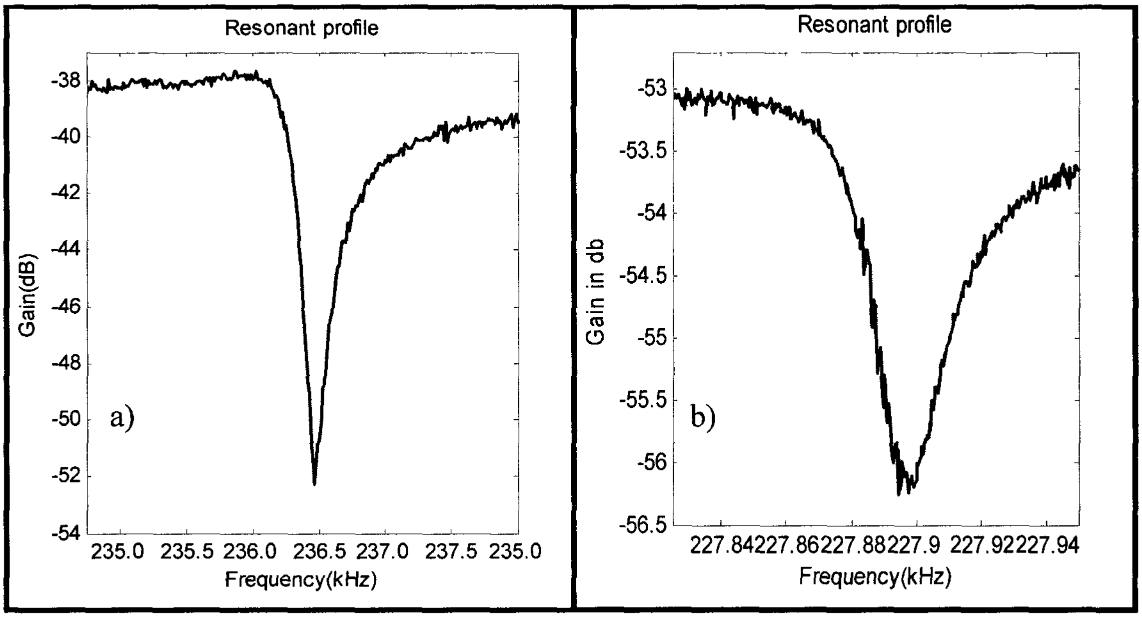

Figure 6.23 Resonant profiles of batch 3 bonded devices a) sample without getter, and Q = 2,400 b) sample with getter Q = 6,700

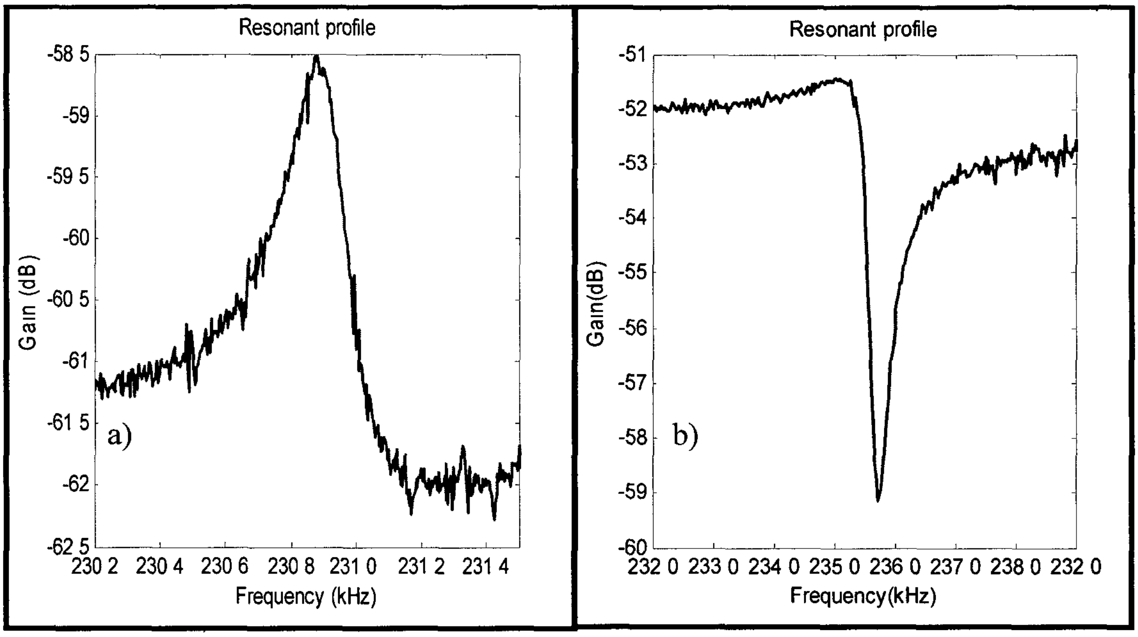

Figure 6.24 Resonant profiles of batch 4 bonded devices a) sample without getter Q = 1,350, and b) sample with getter Q = 1,600

6.12. Estimation of Pressure in the Bonded Sample

In order to estimate the pressure inside the bonded MEMS device, an uncapped die was tested in vacuum at different pressures. The quality factor of the device at different pressures is measured and graphed, as shown in Figure 6.25. The pressure in the cavity was back calculated to be 5 Torr in the sample with cavity only and 1 Torr in the sample with cavity and getter. As the process parameters remained the same in bonding both types of devices, the low pressure in the sample with a cavity and getter could be accorded to the presence of the getter in the device.

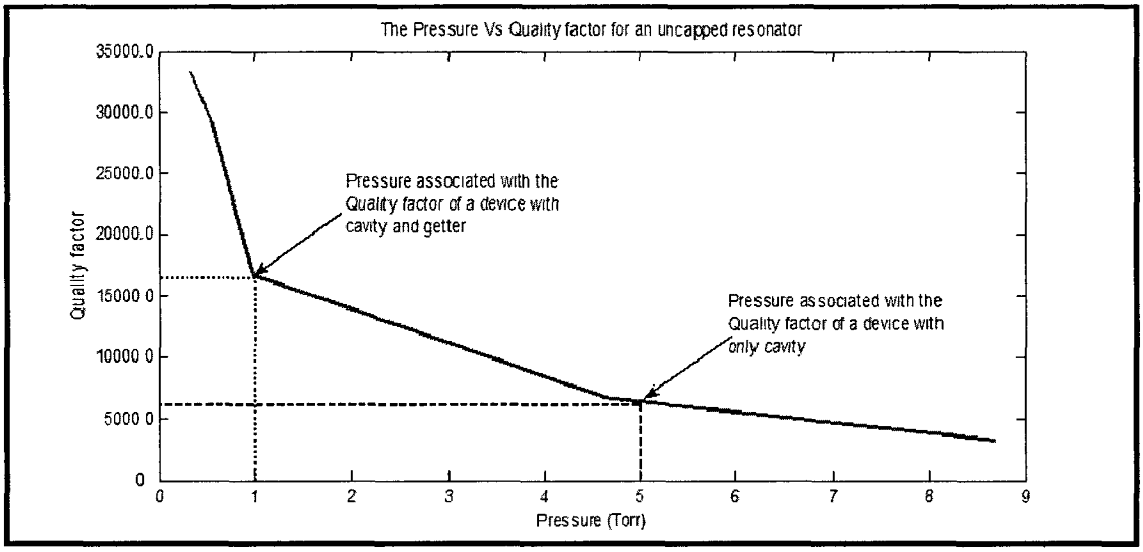

Figure 6.25 Quality factor vs. pressure of an uncapped device

6.13. Porous Silicon as a Getter Material

Porous silicon has a large internal surface area (for this work 200 m^2/cm^3). This surface is highly chemically reactive silicon that can absorb gases. Thus, the porous silicon layer can readily oxidize to form the oxide layer. The thickness of the layer is dependent on time and temperature. The decrease in the inherent matrix elements of F and H causes the impurity elements, such as C, B, S and N to deposit on the resulting oxide [70, 71]. Figure 6.26 shows the reaction between the porous silicon and the O_2 gas to form the oxide layer. The pores of the porous silicon are magnified and the oxide layer deposited everywhere in these pores is shown. As could be seen, the O_2 gas is gettered by the porous silicon. The advantages of introducing porous silicon getter along with a cavity are:

1. the cavity and porous layer reduces the parasitic capacitance and air damping, which helps resonators perform better,

2. the porous layer needs no mask and is self aligned,
3. the porous getter material needs no external heat to be activated.

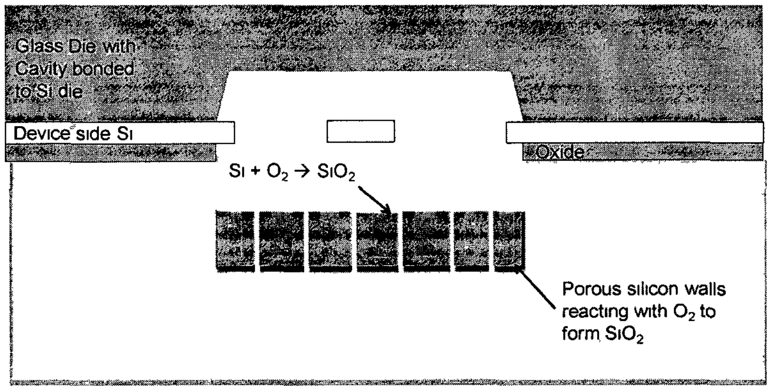

Figure 6.26 Schematic of the bonded SOI die that shows the reaction of silicon with oxygen resulting in the formation of silicon dioxide

6.14. Calculation of the Number of Active Sites in the Porous Silicon Sample

Active sites are the available locations on the porous layer that reacts with the gases to form a layer and getter them. The number of active sites depends on the area of silicon substrate available for the formation of porous silicon. Figure 6.27 shows the design of the tuning fork resonator with the dimensions of the available area for porous silicon formation.

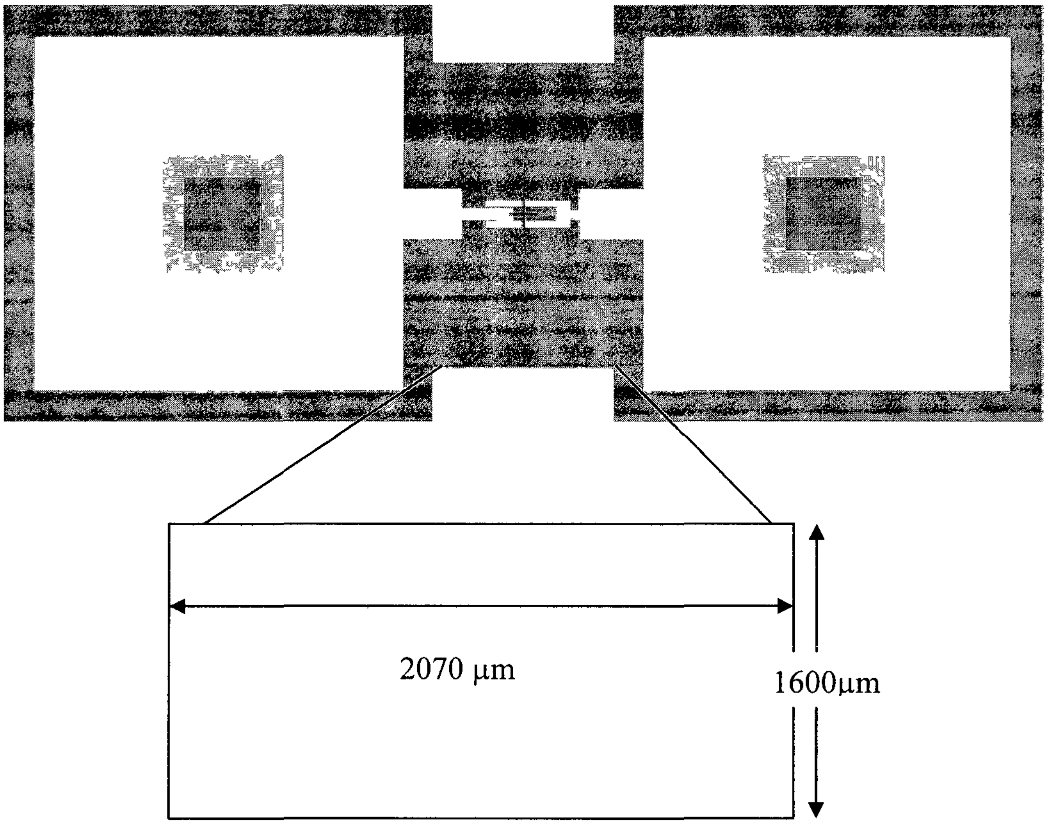

Figure 6.27 Porous silicon formation area

The SOI die size is 8 mm × 8 mm and the area where porous silicon can be formed is 3.3×10^{-7} m^2. The volume of the porous silicon (V_{PoSi}) in the die is 3.3×10^{-11} m^3. The BET (Brunauer, Emmett and Teller) [9] surface area (A_{BET}) for the electrochemical etching parameters used is 200 m^2/cm^3 [10]. The surface area of the porous silicon (A_{PoSi}) is

$$A_{PoSi} = A_{BET} \times V_{PoSi} = 6.6 \text{ m}^2. \tag{6.3}$$

The number of active sites (N_{AS}) present on the surface of the porous silicon that can react to the gases present are

$$N_{AS} = A_{PoSi} / CA_{Si} = 22 \times 10^{18}. \tag{6.4}$$

In Equation (6.4), the CA_{Si} represents the area of the crystalline Si. The number of moles of gas molecules (n) present in the bonded devices can be calculated using the ideal gas law equation

$$n = \frac{PV}{RT}. \tag{6.5}$$

Table 6.2 summarizes the values of pressure (P), volume (V), gas constant (R), and temperature (T) used to calculate the number of moles of gas present in the sample with cavity only and in a sample with a cavity and getter.

Table 6.2 Values used for computing the number of moles of gas molecules

	Cavity only	**Cavity and getter**
P	5 Torr = 666 Pa	1 Torr = 133 Pa
V	33×10^{-12} m^3	33×10^{-12} m^3
R	8.314JK^{-1}mol^{-1}	8.314JK^{-1}mol^{-1}
T	300 K	300 K
n	8.8×10^{-11}	1.8×10^{-11}

The difference between the number of moles of gas present in the sample with cavity only ($n1$) and the number of moles of gas present in the sample with a cavity and getter ($n2$) gives us the number of moles of gas molecules absorbed by the porous silicon getter, which is

$$\Delta n = n1 - n2 = 7.0\times10^{-11} \text{ mol.} \tag{6.6}$$

Hence, the number of molecules of gas molecules absorbed is estimated to be 4.3×10^{13}.

6.15. Comparison of Porous Silicon Getter with the Commercial Getter

In this section, the porous silicon getter is compared to the commercially available SAES getters. SAES produces two getter materials which are application selective. One is the Page wafer getter for wafer-wafer bonding and the other is the Page lid getter for discrete MEMS packages and ceramic packages. Figure 6.28 shows the sorption curve of the Page lid getter provided by SAES. The highest sorption capacity shown for CO is 0.2 cc.mbar/cm^2. The datasheet provided by the SAES also shows that for 1 molecule of CO absorbed, three molecules of O_2 are absorbed. To get the number of molecules of O_2 absorbed, the number of molecules of CO is calculated and multiplied by three.

The sorption capacity (*SC*) is normalized over an area, so let us assume the area to be 1cm^2. Hence,

$$(SC) \times \text{Area} = 0.2 \text{ cc.mbar/cm}^2 \times 1 \text{ cm}^2 = 0.2 \text{ cc.mbar} = PV. \tag{6.7}$$

The number of moles of CO (n_{co}) is given by

$$n_{CO} = \frac{PV}{RT} = 8.018 \times 10^{-5} \text{ mol.} \tag{6.8}$$

In Equation (6.8) the PV can be used from Equation (7.7), R=8.314 JK^{-1}mol^{-1} and T=300 K. The number of molecules of O_2 absorbed are three times that of the CO and is

$$n_{O_2} = n_{CO} \times 3 = 2.405 \times 10^{-4} \text{ mol.} \tag{6.9}$$

The number of molecules is

$$N_{O_2} = n_{O_2} \times N_A = 1.45 \times 10^{20}, \tag{6.10}$$

where N_A is the Avogadro's number. The number of molecules per unit area would be

$$1.45 \times 10^{20} / \mathrm{cm}^2. \qquad (6.11)$$

The number of molecules per unit area for porous silicon:

Equation (6.4) presents the number of molecules absorbed by the porous silicon getter. The area of the porous silicon is 3.3×10^{-3} cm^2. The number of moles per unit area of porous silicon is

$$n_{O_2} = \frac{\Delta n}{3.31\times10^{-3}} = \frac{7.0\times10^{-11}}{3.31\times10^{-3}} = 2.13\times10^{-8} \text{ mol.} \qquad (6.12)$$

The number of molecules per unit area is

$$N_{O_2} = n_{O_2} \times N_A = 1.28\times10^{16} \ . \qquad (6.13)$$

Table 6.3 presents the comparison of the commercial getter and the porous silicon getter.

Table 6.3 Comparison of getters

Number of molecules of oxygen absorbed by getter(per unit area)	**SAES getters**	**Porous silicon getter**
N_{O_2}	1.45×10^{20}	1.28×10^{16}

The number of molecules absorbed by commercial getters is four orders higher than the ones absorbed by the porous silicon getter. The experiments were partly conducted in a cleanroom environment (the wafer fabrication) and partly in a non-cleanroom environment (processing of the MEMS die to etch the oxide and introduce a cavity and porous silicon in the substrate) which affected the efficiency of the getter. In addition to this, the university setup limits the efficiency in comparison to the commercial getters. Hence, it is possible that if these experiments were conducted in an industrial setup the efficiency could be comparable to the available commercial getters.

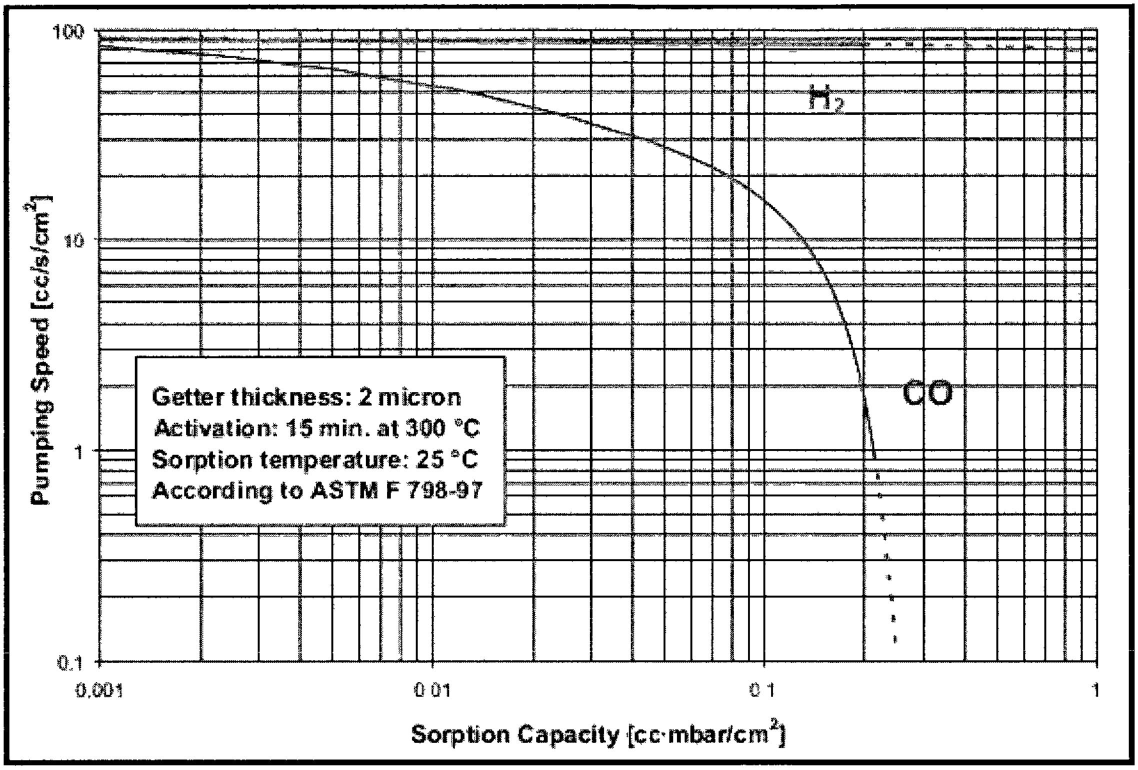

Figure 6.28 Page film sorption curve [72]

6.16. The Benefits of Porous Silicon Getter

1. The highly reactive porous silicon can readily react to the oxygen gas and form the oxide layer that can trap other gas molecules and hence maintain low pressure in the cavity. This benefit is realized without additional materials or masks in the process.

2. The thickness of the porous silicon getter can be increased based on the electrochemical etching parameters used. Hence, the getter material of 100-200 μm can easily be formed that has proven to be more effective in use.

3. One of the major gases that are emitted after the anodic bonding is O_2, which increases the cavity pressure to about 400 mT. At this pressure the number of O_2 molecules could rise to 1.04×10^{15} which is still four orders less than the 2.23×10^{19} active sites of the porous silicon that are available to react.

4. Bonded MEMS devices require high volume to surface ratio to accommodate any outgassing from the surface. Porous silicon has a very high surface area. Ideally, this surface would outgas more and decrease the quality factor of the device. But, it is seen that the device with porous silicon has two times better quality factor than the non-porous device. This proves the performance of porous silicon as a getter for MEMS devices.

6.17. Resonator with Cavity in Glass Lid Coated with 100 nm Ti

The porous silicon getter was compared to the Ti getter. Using e-beam evaporation, a 100 nm Ti layer was deposited on the cavity of the glass die. This die was then bonded with the resonator that has a cavity in its substrate. During bonding the Si and glass assembly is heated to 450 °C that helps to activate the Ti getter. Figure 6.29 shows the resonant profile obtained from this resonator. The signal strength was measured to be 4.5 dB and the quality factor was 1,000 at 35 V. The quality factor is comparable to the quality factor of the batch 4 resonators with only a cavity in the substrate, which indicates that the effect of the Ti getter was insignificant. Hence, the porous silicon getter has proven to be an effective getter.

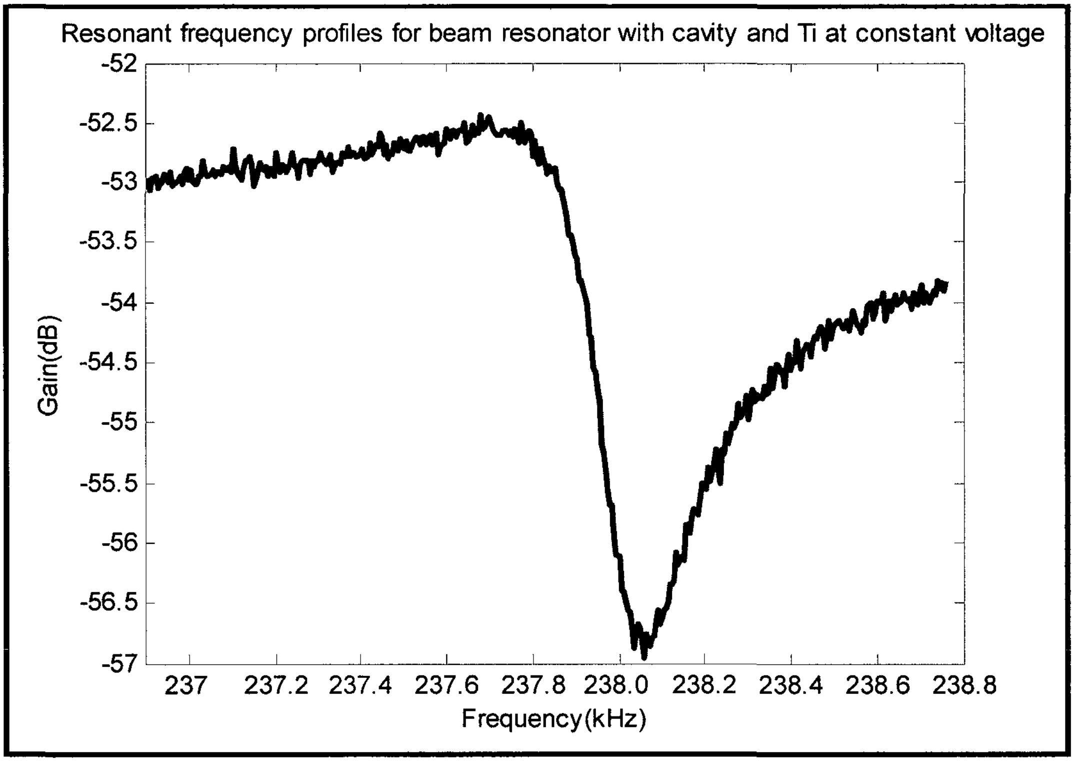

Figure 6.29 Resonant frequency profile of resonator with 100 nm Ti deposited on glass

6.18. Summary

In this chapter the results obtained by the uncapped devices without any cavity and with a cavity were compared and it was shown that the latter has two times better quality factor than the former. The encapsulated devices that have a cavity augmented with porous silicon were shown to perform 2-3x better in terms of quality factor than the devices with cavity only. It was also shown, that after introducing the porous silicon, the pressure level in the bonded sample can be reduced up to 5x.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

This chapter presents the outcome of the work presented in this dissertation along with suggestion for future work. An explanation of results obtained is also presented.

7.1. Conclusions

This dissertation presents the following:

- Successful use of porous silicon as the sacrificial material to obtain cavities in SOI die substrates of and its benefit to improve the quality factor:

  It was shown that, with the electrochemical etching of silicon, thick layers of porous silicon can be obtained in SOI die substrates. This layer can be etched with a KOH dip leaving a cavity in the substrate. The process is mask-less, self aligned and low cost. It was seen that the devices with a cavity showed two times better quality factor than the non cavity devices.

- Steps to prevent the reaction on the device layer during the electro-chemical etching process:

  It was shown that the device layer reaction can be prevented by: the use of ethanol to dilute the 50% HF; changing the groove for the O ring from conical to cylindrical; and increasing the wait time between the etching of the buried oxide using 50% HF and electrochemical etching using 10% HF.

- Successful augmentation of porous silicon getter to the cavity in the SOI die substrate:

  It was shown that by using another electrochemical etching cycle, thick layers of porous silicon getter can be obtained to augment the cavity in the substrate. Again, this process is a mask-less, self-aligned process and hence eliminates the use of any special process to introduce the getter material in the MEMS devices.

- Construction of a vacuum chamber that can host both testing and bonding process:

  A customized vacuum chamber was assembled that can house the MEMS bonding process and test the MEMS devices one at a time in vacuum. The chamber was equipped with both a mechanical and a turbo pump that can obtain pressure of 0.01-0.1 mTorr in the chamber.

- Comparison of getter and non getter devices:

  The vacuum encapsulated MEMS devices, with and without a getter in the substrate, was compared. It was shown that the devices with a getter had 2-3 times better quality factor in comparison to non getter devices. The device with a getter was shown to achieve 5 times less pressure than the non-getter device.

7.2. Explanation on the Results Obtained

The experiments in this dissertation were carried out sequentially in three different labs one after the other. First, in the class 1,000 clean room where the MEMS devices are fabricated on the SOI wafer. Second, in a semi-clean room where the MEMS devices were released and the electrochemical etching process was carried out. Third, in a general lab where the MEMS devices were encapsulated in vacuum and tested. In the experiments performed, after the porous silicon getter was introduced in the substrate, the processed die was then taken into a general lab to bond the Si die to glass. During this time, as the porous silicon had been exposed to non-cleanroom conditions, it may have had some of its pores contaminated with micro/nano sized dirt particles. It also takes some time to manually align the glass and silicon dies before starting the bonding process. During this time, the reactive nature of porous silicon is degenerating. Because of these reasons, it can be seen that the number of molecules of O_2 absorbed by the porous getter is four orders less than the SAES getters. Ideally, the number of gas molecules absorbed should be same as the available 22×10^{18} active sites on the surface of porous silicon, but in our case, 1.28×10^{16} gas molecules were absorbed. The reason for this is because the Si tangling bonds/active sites get occupied before bonding. Hence, to avoid this problem, the entire process can be conducted in the clean room from fabrication to bonding. Due to the lab space limitations, in this dissertation, the experiments needed to be spread out in three labs, as mentioned above.

Ideally, the bonded MEMS devices need high volume to surface ratio to accommodate any outgassing from the surface of the MEMS die. The surface area of the porous silicon in the device was calculated to be 6.6 m^2. With the introduction of this high surface area in the sample, the volume to surface ratio is reduced magnificently. Hence, the devices with a porous silicon getter should have a low quality factor. However, it was seen that the devices with porous silicon performed two times better than non-porous samples. This proves the significant advantage porous silicon offers as a getter material for MEMS devices. This dissertation proves the benefits of porous silicon as a getter material that requires no mask, lithography, or special heat treatment and is self aligned.

7.3. Future Work

- Extend the process to wafer level: this enables the mass production of MEMS devices with porous silicon to benefit industrial applications
- Experiment on the effects of getter thicknesses: ideally the greater thickness should provide better gettering of gases because of deeper pores and increased surface area
- Investigating the benefits of porous silicon on the reactive device side for bio sensing: the pores in the porous silicon can be used to store or sense bio fluids
- Extending the experiments to different MEMS structures, such as plates, comb drives for confirmation of theory

APPENDIX A

EXPERIMENTAL VACUUM SETUP

MEMS resonators need vacuum to obtain a high quality factor. In this dissertation, a vacuum chamber was custom made with required accessories to test and bond the MEMS resonators.

A vacuum chamber typically has a container that holds vacuum, a mechanical and turbo pump that creates the vacuum, and a pressure gauge to measure the vacuum. Each of these parts is presented in detail in the following paragraphs.

A.1. Vacuum Chamber

Any container held at a pressure less than 760 Torr is loosely defined to be a vacuum chamber. Stainless steel is most widely used for high-vacuum and ultra high vacuum apparatus. The types 304 and 316 stainless steel are more commonly used than 303 as it contains the added volatile materials for better machinability. The advantages of using stainless steel in the vacuum chamber building are [73]:

- The type 304 and 316 are non magnetic and have magnetic permeability less than 1.01.
- It is easy to join stainless steel parts using brazing, silver soldering or welding; hence, any desired chamber size or shape can easily be made. Tungsten inert gas (TIG) welding is a process commonly used for joining stainless steel metal parts. It uses non consumable tungsten electrode in argon atmosphere to arc weld the parts. TIG produces very strong joint, and the surface of the joint parts can be cleaned easily, as it does not use any flux or welding rod.

A.2. Mechanical Pump

In this dissertation, the combination of oil sealed mechanical pump and turbo molecular pump was used to achieve the needed high vacuum. The turbo pump needs the pressure of the chamber to be below a certain pressure (stall pressure) before it starts to operate. The mechanical pump maintains pressure lower than the stall pressure, for the high vacuum pump to start its operation. The mechanical pump is called the roughing pump in this function.

In this work the mechanical pump had a pumping speed of 20 L/sec. This pump was able to obtain a pressure of 8-5 mTorr in the chamber. In order to obtain higher vacuum, a turbo molecular pump was attached to the vacuum chamber. The stall pressure for the turbo pump was 200 mTorr. The mechanical pump was operated first to obtain a pressure of 150 mTorr. As a safety precaution, the pressure of the vacuum chamber was kept 50 mTorr less than the stall pressure. Once this pressure is reached, the turbo pump was put in operation to achieve the needed high vacuum. The type of mechanical and turbo pump used and the principle involved in their operation is discussed below.

A.3. Oil Sealed Rotary Vane Pump

In order to obtain pressures in the order of a few millitorr's, the most commonly used pump is the oil sealed rotary vane pump. In this pump, the internal chamber is divided into two sections. One is the inlet and the other is the outlet. The oil used in these pumps is good quality low vapor pressure hydrocarbon oil, and it acts as a differentiating layer between the vanes of the rotor and the stator. As the high vapor pressure fraction is removed from the oil used, there are no voids created in the differentiating layer. Also, there is no condensing that takes place inside the pump. These pumps are also available as two stage operating pumps with rotors on a common shaft operating in series.

The oil sealed rotary pumps can operate for a long time with minimal maintenance. If the oil is changed periodically, then there would be no condensation inside the pump. If the lowest pressure obtained by the mechanical pump changes drastically, it is an indication of the presence of the volatile materials inside the oil that contaminates the pump and hence increases the pressure. The pump oil thus needs to be drained out and new oil be filled. As these pumps act as the backing pump for high vacuum pumps, they are designed for continuous long time operation. It was observed with the continuous operation of the pump that the body of the pump starts to leak oil because the nuts and bolts that hold the pump start to loosen. But with little care, the pump can be well maintained and its use be maximized. Single stage pumps are useful to obtain a pressure of 50 mTorr or higher and the two stage pumps help in obtaining the pressures of 5 mTorr. A two stage pump is preferred as a backing pump [73].

The oil sealed pumps tend to exhaust gases with the mist of fine droplets of oil. These droplets are very dense above 100 Torr. With these heavy droplets, there is a layer of dirt that tends to condense and contaminate the inside of the pump. Inhaling this kind of exhaust over a long period of time is unhealthy for the person operating the pump. Hence, a filter is attached to the exhaust of the pump. The exhaust is recommended to be connected to an air exhaust line to pass the gases out of the lab. Figure A.1 shows the vacuum chamber with all the accessories attached. In the lab space used for the work in this dissertation, the gases were vented using the suction pipe as shown in the Figure A.2.

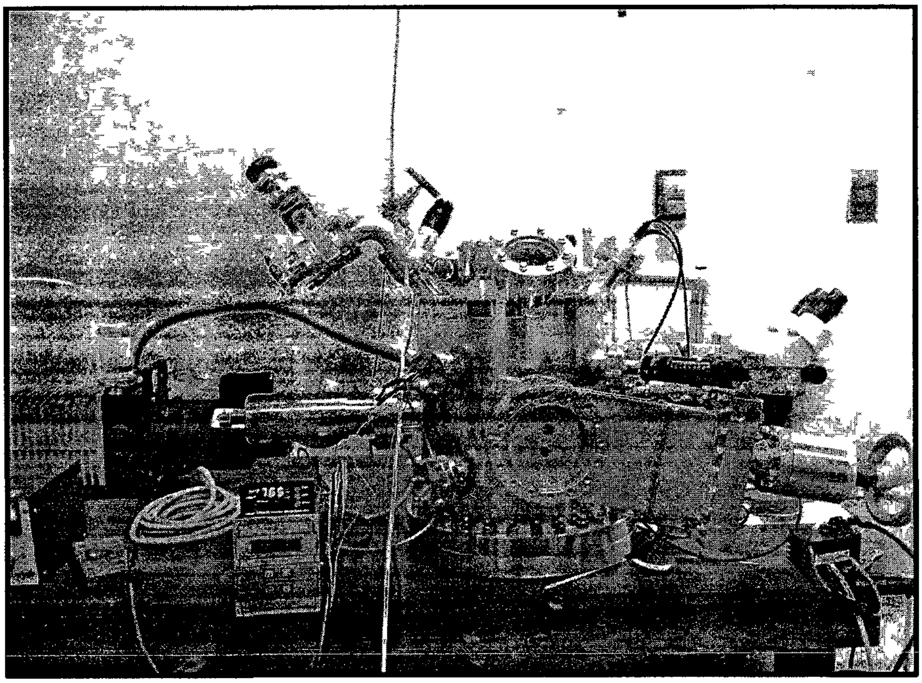

Figure A.1 The vacuum pump with the mechanical pump, pressure indicator clearly shown

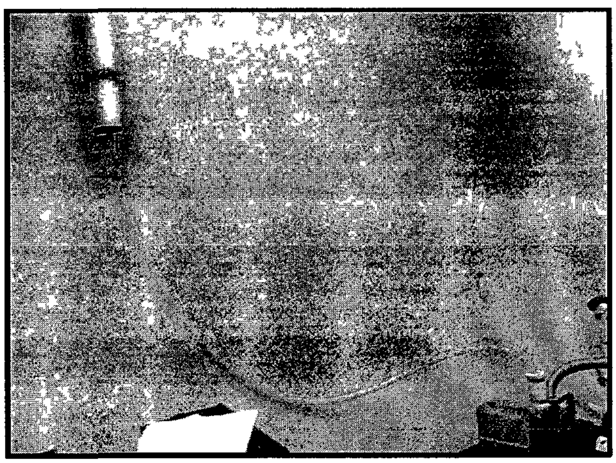

Figure A.2 The outlet of the pump being connected to exhaust

With the use of filters at the exhaust of the pump, the oil may coalesce down to the pump and be reused. If the filter is not used and the oil evaporates, within a period of time, it may cause the oil level to drop, and, if unmonitored, it may cause damage to the pump's mechanical components.

The time taken by the pump to bring the pressure in the pump from a pressure P_0 down to P is given by

$$t = \frac{V}{S} ln\left(\frac{P_0}{P}\right), \tag{7.1}$$

where V is the volume of the vacuum chamber, S is the pumping speed of the pump, P_0 is the initial pressure of the chamber and P is the desired pressure of the chamber [73].

The time taken by a chamber to reach a certain pressure depends on the pump that is used. A mechanical pump has a pumping speed lower than a turbo molecular pump. Hence, it takes more time for a mechanical pump to reach the stall pressure. Hence, in calculating the time it takes to create a suitable vacuum in the chamber, the pumping system needs to be considered.

A.4. <u>Outgassing</u>

Outgassing is one of the limiting factors to obtain a high vacuum (in the range of 10^{-7} torr) in a chamber. It is the evolution of gases from the surface of the chamber or any part present in the chamber. Hence, after a certain pressure, the rate at which the pressure drops in the chamber is not just limited to the speed at which the pump operates, but also at the rate of out gassing in the chamber. A porous or a rough surface adsorbs the gases from the chamber and causes a decrease in the rate of vacuum in the chamber. An aluminum surface outgases at a rate ten times higher than a stainless steel surface. Plastics are ten times worse in out gassing than aluminum and rubber is ten times worse than plastic. As rubbers and plastics are not vacuum friendly, their use is avoided.

The in-house vacuum chamber designed in this dissertation had a brass plate, PCB, electrical tape and wires in it to aid in the testing of MEMS devices. The rate of out gassing was kept under control with the combined operation of mechanical and turbo pump.

A.5. Pirani Gauge

We used the convection enhanced Pirani gauge (CVT-275-101). It can measure the pressure down to 0.1 mTorr. The Pirani gauge uses the change in thermal conductivity from one pressure to another as an indication of pressure in the chamber. A wire filament is heated in the Pirani gauge which forms one arm of the Wheatstone bridge. Depending on the rate of heat loss to the surrounding gases, the temperature of the filament changes. The change in temperature changes the resistivity in the arm, hence changing the voltage drop in the arm and causing an imbalance in the bridge. This imbalance of voltage is the indication of pressure. An equivalent voltage is then applied to the bridge to create a balance in the bridge. This applied voltage is the measurement of the pressure in the chamber. In the Figure A.3 the enhanced convection gauge and the pressure indicator are shown.

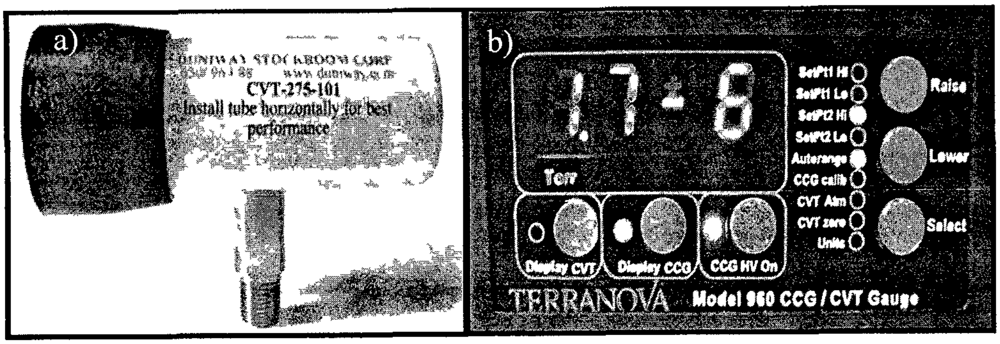

Figure A.3 a) Pirani gauge, and b) Pressure indicator

The convection enhanced pressure gauge has a special structure that responds to convection cooling at higher pressures. This gives a wide range of measurement, as compared to a simple pirani gauge.

A.6. Turbo Pump

Turbo molecular pumps operate in the molecular-flow regime [74]. The schematic of the turbo molecular pump, also called the turbo pump for simplicity, is shown in Figure A.4.

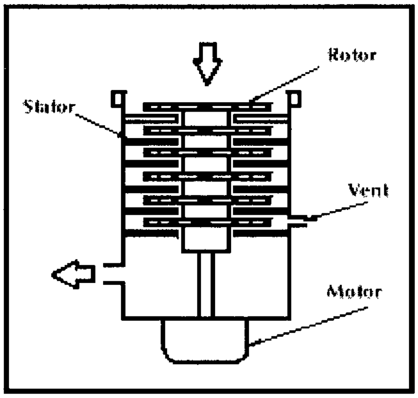

Figure A.4 The schematic of the turbo pump showing the multiple stator and rotor pairs [73]

The motor rotates the rotor with a speed of 20,000 to 90,000 rpm and the canted rotor pushes the gas molecules with high speed to the next rotor assembly, thus making it approach the exhaust. The rotors are canted to let the air molecule gain a velocity component in the direction of the exhaust. At atmospheric pressure, the flow of gases is viscous. The mean free path of the molecules at atmospheric pressure is 70 nm. The molecules interact with each other more often than with the walls of the chamber. Because of these collisions, the rotor blades would not be able to impart as much force on the molecules to move them towards the exhaust. Hence, a rotary pump is used to bring the pressure down so that the molecules could now be in the molecular regime and respond to the high rotor speeds. After the turbo pump is turned on, because of the high rotor speeds, the pressure starts dropping off rapidly. As there are multiple stages of rotor and stator assembly present, the gas molecules are sent from one set to the other and they get compressed at the exhaust. Although the pumping speed remains the same for all the gases, the compression ratio at the exhaust changes with the gas. After a certain pressure is reached the rate at which pressure drops becomes significantly low. This is because:

1) the out gassing from the seals and vacuum parts become significant at very low pressures, and
2) the turbo pump will have achieved the maximum compression possible for the gas in the chamber.

Special care was taken in the project to avoid any kind of out gassing. The vacuum chamber was cleaned with acetone periodically and was constantly pumped down to keep the chamber clean.

A.7. <u>Summary</u>

This chapter presented a description of the vacuum chamber with the accessories attached to obtain a high vacuum. The principle of operation of mechanical and turbo pump is also presented.

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