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Bulk micromachining of silicon for MOEMS prototype

Sung-Dong Suh

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BULK MICROMACHINING OF SILICON

FOR MOEMS PROTOTYPE

by

SUNG-DONG SUH, B.S., M.S.

A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
PhD in Engineering

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Head of Department

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ABSTRACT

In this dissertation, the optical application of silicon micromachining technology was investigated in order to create the three-dimensional microstructures that can be used as the components for the MOEMS prototype. These microstructures were designed and fabricated by utilizing corner compensation techniques and silicon bulk micromachining technologies. The fabricated microstructures are silicon mirror arrays that have a 1250 μm etch depth and through-holes across the OE-MCM substrate that has sixteen-fan-out OCDN on front side and a 1mm thickness.

Guided-wave OCDN on MCMs are designed and fabricated to meet the high-speed clocking requirements of next-generation digital systems through a realization of superior network bandwidth, low power consumption, and large fan-out capabilities.

Two fabricated components were assembled to build the MOEMS prototype. From the fiber-to-waveguide butt coupler, the light signal is launched on the waveguide core, and the signal travels and splits along the waveguide. Then, the light signals reflect at the micromachined silicon mirrors which are located in the sixteen fan-out nodes. This device was characterized by measuring the excess loss at the sixteen fan-out nodes at the wavelengths of 1310 nm and 1550 nm. The results show low loss signal propagation and signal uniformity.

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CHAPTER 1

INTRODUCTION

Background

Silicon Micromachining

Silicon micromachining is the process of creating microstructures in silicon by means of photolithography and chemical or physical etch. There are three technologies in micromachining: bulk micromachining, surface micromachining, and LIGA process.

Bulk micromachining, used to selectively remove silicon from substrates, has been applied in the fabrication of micromachined sensors, actuators, and microstructures [1]. Since the silicon can be micromachined precisely by anisotropic etchants, whose etching rates depend on the crystal orientation, bulk micromachining utilizes the etching selectivity between {111} planes and {100} or {110} planes [2-4]. There are two types of bulk micromachining techniques depending on the state of the etchants: chemical wet etching and dry micromachining. In dry micromachining, chemically active species collide with the substrate. This collision removes the substrate ion, atom or molecule. It even produces delicate microstructures, but it requires an expensive facility. Dry micromachining is particularly amenable to single-wafer processing, and for practical reasons etching depth is usually limited to depths of less

than 20 μm [5]. Therefore, traditional bulk micromachining (wet chemical etching) is preferred for the fabrication of thick and high aspect ratio microstructures.

Surface micromachining is the fabrication process of the micromechanical structures by deposition and etching of thin structural and sacrificial films. There are several advantages and trade-offs between surface micromachining and bulk micromachining technologies. Compared to the bulk micromachining technique, the surface micromachining method does not have enlargement effects so the improvement of device density is expected. The increased throughput reduces the cost of individual devices and makes the development of merged integrated sensor/microelectronic systems economically feasible [6]. In addition, the optical applications of the surface micromachining have been reported recently [7]. However, the biggest disadvantage of surface micromachinng is that it is limited to thin films.

A variety of high aspect ratio microstructures can be fabricated by using the LIGA process that utilizes a combination of surface micromachining and metal electroplating. The fabrication method of the LIGA process for micro-optical elements has been presented by many researchers [8,9].

MEMS

The most important goal of micromachining technologies is the ability to create higher performance with smaller and more functional measurement, instrumentation, and control systems. These systems may include sensors, actuators, and electronics or a combination of them,

implemented using batch fabrication technologies typically used in integrated circuits [10-12].

Micro-electro-mechanical-systems (MEMS) are integrated micro-scale devices or systems that utilize both electrical and mechanical components. Two main categories of MEMS are sensors and actuators. Both of these are special types of tranducers, which are devices that convert one physical quantity to another. Therefore, the sensor is considered to be a device that converts a physical quantity to an electric signal, and the actuator is considered to be a device that converts an electric signal to a physical quantity. In Table 1-1, types of sensors are listed. Electrostatic actuators such as comb drives and micromotors, piezoelectric actuators, thermal actuators, hydraulic actuators and microstimulators, are all considered actuators.

Optical Applications of Silicon Bulk Micromachining

When MEMS technology is applied to optics, it can extend the functionality of optical devices and miniaturize the optical systems. The miniaturization and integration of optical and optoelectronic systems can improve the performance of these systems with a reduction in size and cost, very similar to IC fabrication technology in the recent technological revolution. Since micro-optical elements such as mirrors and actuators can be monolithically integrated on the same substrate using a batch process, micromachining technology brings many opportunities for the application of optoelectronic systems [13-16].

Table 1-1. Microsensors

Sensor Types	Examples
Thermal Sensors	Thermocouples
	Thermoresistors
	Thermal flow-rate sensors
Radiation Sensors	Photodiodes
	Phototransistors
	Charge coupled devices (CCDs)
	Pyroelectric sensors
	Integrated Optics
Chemical Sensors	ISFETsensors
	Enzyme-based biosensors
	Microelectrods for neurophysiology
Mechanical Sensors	Piezoresistors
	Piezoelectric sensors
	Capacitive sensors
	Optical sensors
	Resonant sensors
	Accelerometers
	Pressure sensors

* Available from internet: http://www.dbanks.demon.co.uk/ueng/

The basis for the MEMS technologies is micromachining, which involves the fabrication of mechanical structures in the micron to millimeter range. Wet chemical anisotropic etching of silicon is one of the key technologies of silicon micromachining, and it is also referred to as "bulk micromachining" since significant amounts of silicon are removed from a substrate in this technology [1,17].

Wet chemical anisotropic etching was used to create the microstructures in this dissertation. Two different microstructures were fabricated. These are the silicon micromachined mirror array and the through holes across the optoelectronic multichip module (OE-MCM). The silicon mirror array, which has a convex structure, is used for optical signal distribution. The fast etching planes determine the shape of the silicon micromachined mirrors. The through-hole is a concave structure, and its final form after etching is determined by the slow etching planes [17-21].

There is an optical waveguide network on the MCM substrate. Figure 1-1 shows the optical waveguide network and the locations of input/output (I/O) couplers on the front side of the MCM substrate. The optical waveguide network is composed of bending sections and branches such as Y-splitters, even though it looks like it consists of all straight lines in Figure 1-1. The back side of the substrate is patterned with oxide openings at the same location of the I/O pads on the front, but the openings for bulk micromachining have larger dimensions than those on the front side. The through-holes are formed by etching both sides simultaneously to accommodate the silicon mirror array. Figure 1-2 shows a diagram of the micromachined silicon mirror array.

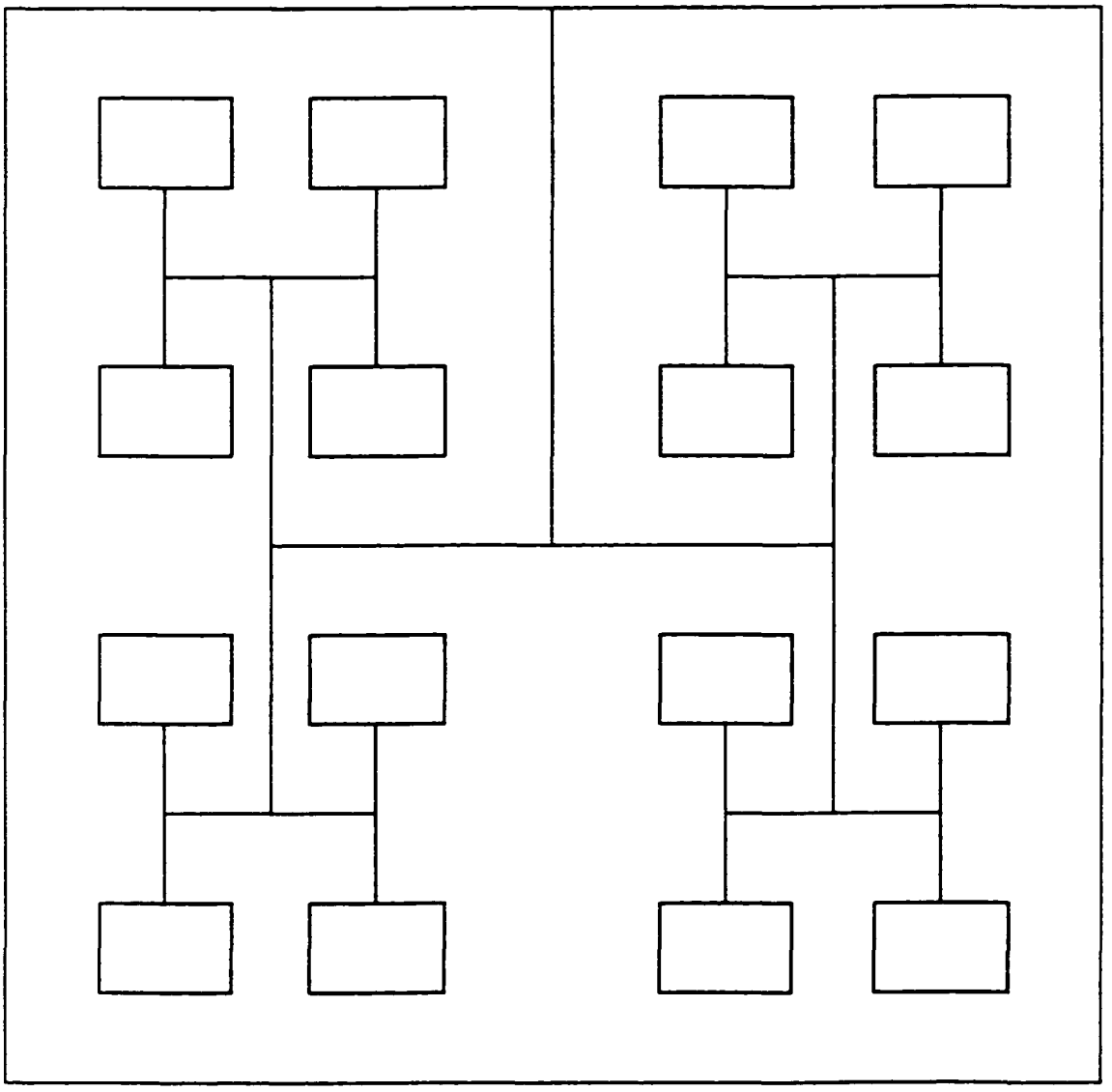


Figure 1-1. Front Side of The OE-MCM Substrate

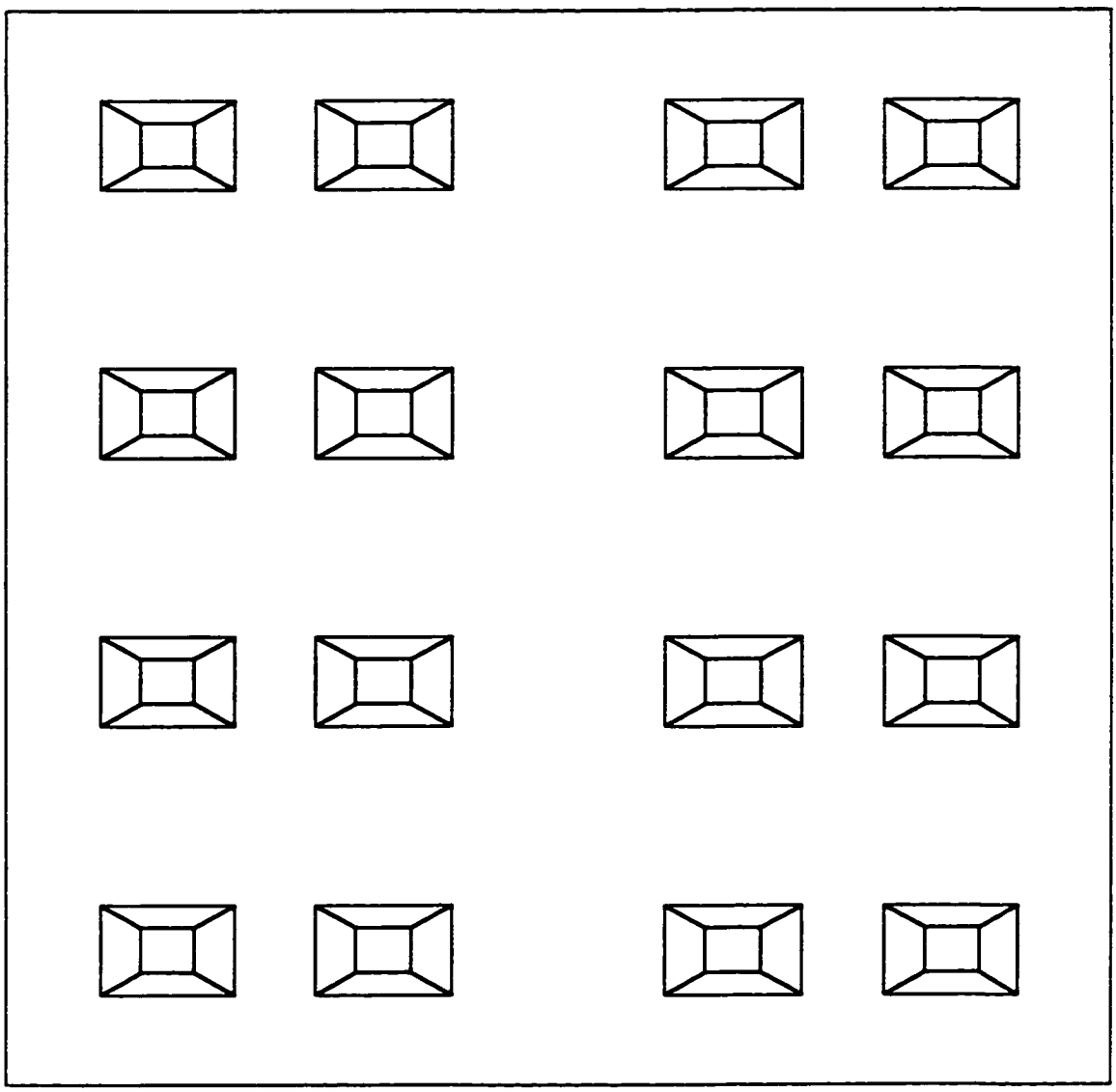


Figure 1-2. Micromachined Mirror Array

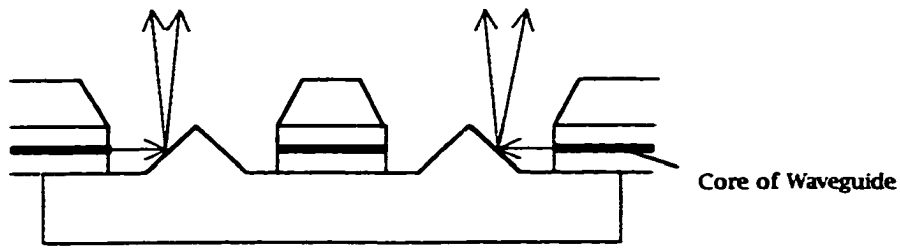


Figure 1-3. MOEMS Prototype after Assembly.

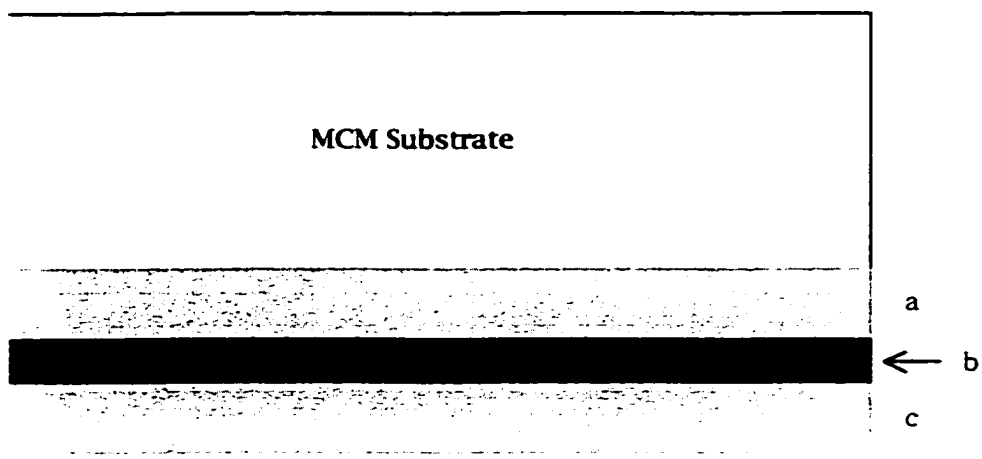


Figure 1-4. Silica Glass Waveguide Layers (a: Upper Buffer Layer, b: Core of The Waveguide, c: Under Buffer Layer).

The micromachined silicon mirror array and the through-holes across the OE-MCM are combined and used for I/O couplers on the OE-MCM [22-25]. Figure 1-3 shows a side view of the micro-opto-electro-mechanical-systems (MOEMS) prototype after assembly. The beam comes from the core of the waveguide, and reflects at the mirror's surface, and then goes to the detector.

The optical waveguides are composed of symmetric, three layers, and the structure of the layers is shown in Figure 1-4. The photonic integrated circuits (PIC) for the optical clock distribution network (OCDN) have been designed by considering the following requirements: PIC sizes determined by the minimum bending rules, waveguide and coupling excess losses, and distribution of equivalent powers at the clock fan-out nodes.

OE-MCM

The multichip module (MCM) is a new packaging approach in which multiple bare chips are mounted and interconnected on a substrate. Some of the problems such as propagation delay, packaging, and power dissipation can be solved by using MCM technology [26-28]. But other problems such as electromagnetic interference, number of chip I/O pads, and maximum interconnection density remain even in the MCM environment for high speed digital applications. Optical interconnects are a potential solution to these problems [29-33]. There are two types of optical interconnections: guided-wave type and free-space type. The guided-wave type is superior to the free-space type in coupling efficiency, compactness and mechanical stability [34,35]. In this project, high silica glass guided-waves are used as optical interconnections for the global

signal distribution [36,37].

Research Objectives

The objective of this research is to build a MOEMS prototype by using bulk micromachining technologies. The fabricated MOEMS prototype is a guided-wave optoelectronic clock distribution network on MCMs, which utilizes silica glass waveguides and micromachined silicon microstructures.

The micromachined microstructures include a silicon mirror array and the through-holes across the MCM substrates. Since these microstructures require very deep etch depths (1000 - 1300 μm), the design of a mask layer that prevents the corner undercutting is the main objective. These micromachined silicon microstructures are used as optical I/O couplers on the OE-MCM.

The optical waveguides are used for optical interconnection within the MCM. The optical waveguide networks contain many components, such as bending sections and branching waveguides. Therefore, the investigation of these waveguide components is also an objective of this research.

Outline of the Documents

Chapter 2 presents the mask layer designs for high mirrors that need corner compensation techniques, and for deep through-holes. The fabrication method of the 45° mirror is also introduced. Chapter 3 describes the waveguide network on MCM substrate, including the bending loss theory and branching components. In Chapter 4 experimental procedures for the fabrication of the silicon mirror array and through-

holes across MCM substrate are explained in detail. The measured experimental data, assembled structure, excess loss measurements and characterizations are also covered. Finally, Chapter 5 contains conclusions and recommendations for future work.

CHAPTER 2

BULK MICROMACHINING OF SILICON

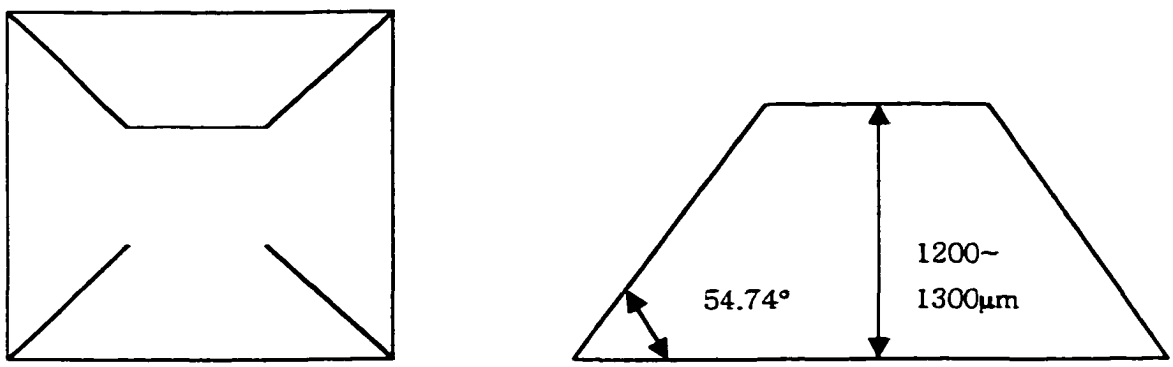
Silicon micromachining technology has been used to create three-dimensional microstructures on silicon substrate in order to form V-grooves for optical fiber alignment and construct micro-optical elements such as mirrors and through-holes. Through-holes and tall mirrors are fabricated to build MOEMS through this dissertation. And Tetramethylammonium hydroxide (TMAH) is chosen as an etchant for bulk micromachining. Since TMAH is an organic material, it is a potentially IC-compatible etching agent as well as a nontoxic material. Some potential drawbacks of TMAH are high undercutting ratios, surface roughness on the (100) plane, and limited published results [38-40]. Another popular etchant is an aqueous solution of potassium hydrixide (KOH) with concentration ranging from 10 to 50%. However, the selectivity over silicon dioxide is less than 500 at various concentrations, which is not quite enough for masking during long etches [6].

In this chapter, the mask layer design of microstructures and the 45° mirror fabrication method are explained, and wafer preparation, fabrication procedures and results are covered in chapter 4.

Mask Layer Design for Mirrors

It is known that there is corner undercutting at the convex corner in the anisotropic etching of (100) oriented silicon wafers [2,4,41,42]. There are two methods that can be used to correct for corner undercutting [43]. The first one is the addition of compensation patterns to the mask corners, and the second one is the tilting of the mask side with respect to the wafer flat by a small angle.

Since the second method is not the efficient way for a given facility with limited functionalities, the first method is chosen to fabricate the mirrors that have mesa structures, and it can be used for guiding the optical signal. Figure 2-1 shows the desired shape of mirror. The required etch depth is 1200 ~ 1300 μm, and N-type, 3-inch, 2mm thick wafers are used to create these particularly tall structures.



(a) Top View (b) Side View

Figure 2-1. Diagrams for Mirrors

Many types of corner compensation design have been presented. All of the different compensation structures were created based on the fast-etching planes [17]. Several methods to compensate corner undercutting have been presented by many researchers. M.M. Abu-Zeid added rectangles to the corner of the square mask pattern and Xian-Ping Wu and Wen H. Ko used triangles, and H. Sandmaier and H.L Offerins attached <110> oriented beams and <110> oriented squares to make the sharp corners [43-47]. But these designs were devised only to use a specific etchant (usually KOH), not for other etchants. Since different etchants show different characteristics such as different lateral etch ratio, their designs could not be adopted directly for our bulk micromachining, which uses TMAH as an etchant. Therefore, a mask that has several test structures was prepared for obtaining the information required to design a corner compensation structure. Figure 2-2 shows the mask layer with different structures. Using the below test structures, the silicon wafer etched at 70°C. This experiment shows the high lateral etch ratio and relatively slow etch rate into the <100> direction. After several experiments, we concluded that 85°C is an optimum etching temperature for our mirror fabrication, considering both surface quality and etch rate. At this particular temperature, the etch rate is 25 ~ 27 μm/hr and the lateral etch ratio is 6.8 ~ 7.2.

It has been reported that the main beveling planes at undercut corners are all {212} planes, whether KOH or hydrazine or EPW solutions are used as etchant [44]. That means the fastest etching planes do not depend on the etchant but on the atomic density. Therefore, the lateral etch ratio and target etch depth can be the main design parameters

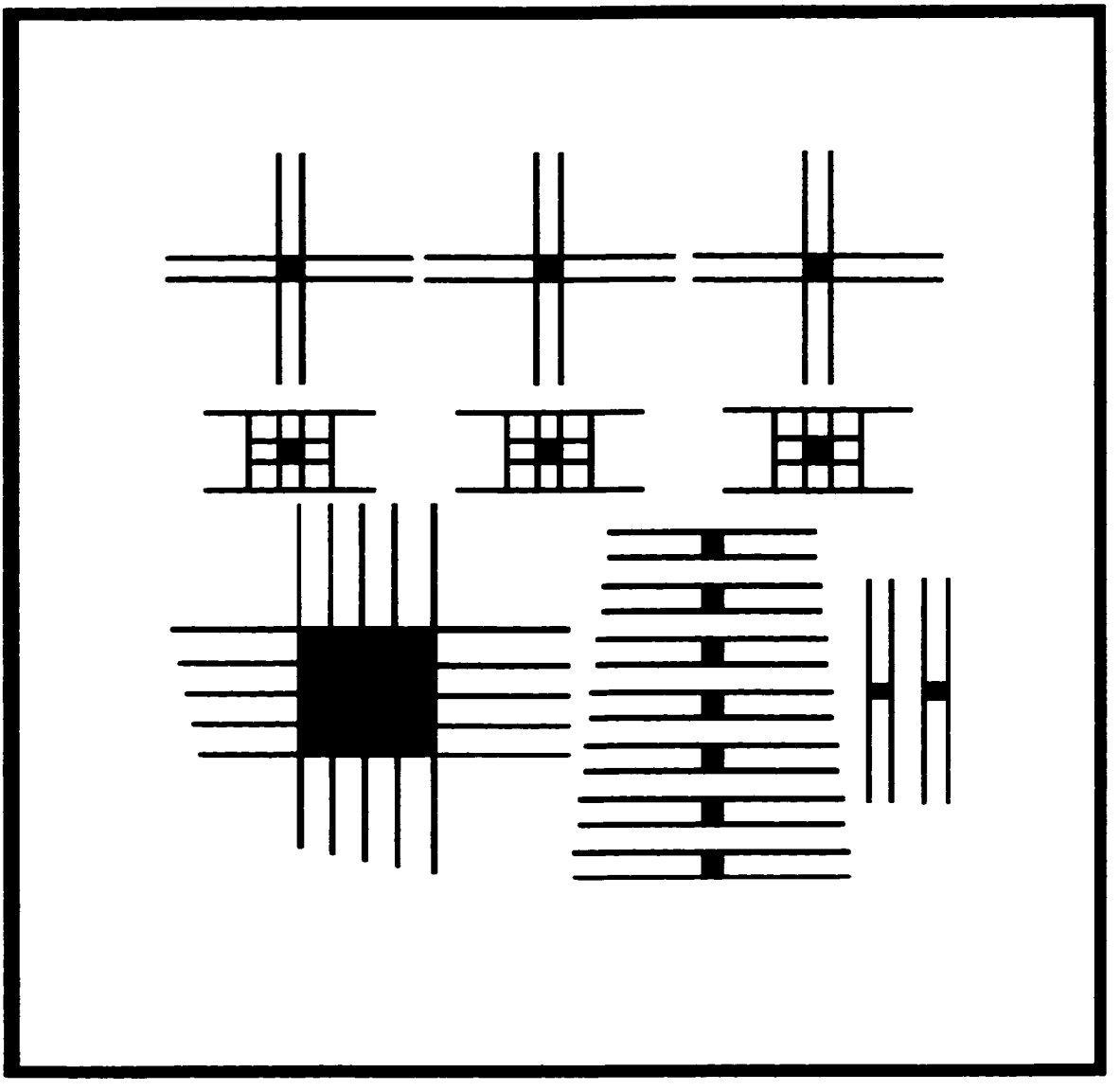


Figure 2-2. Mask Layer for Test Structures

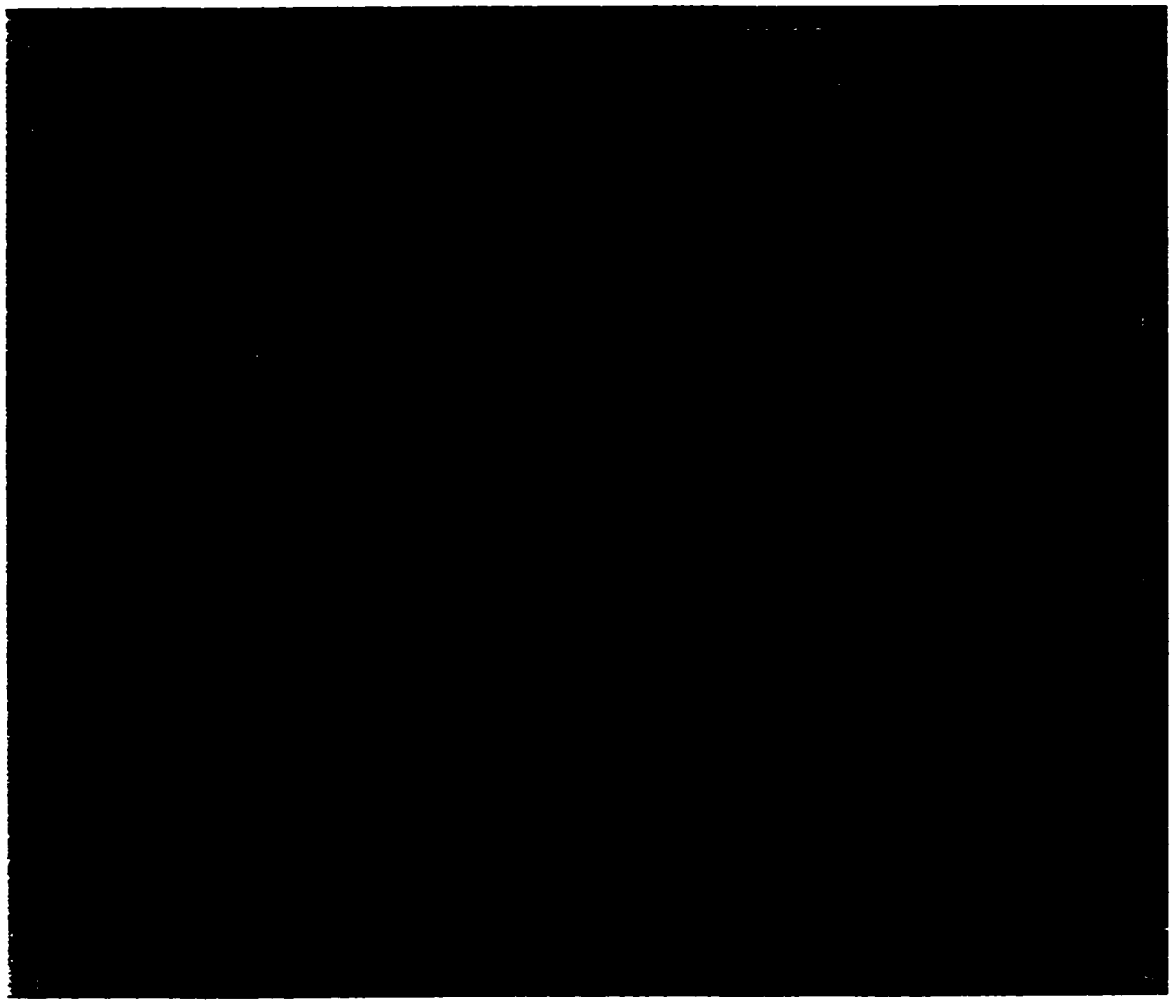


Figure 2-3. Corner Compensation Structure

regardless of the etchants used. The first designed corner compensation structure is showed in Figure 2-3. In this design, square patterns are added to the mask corners to correct the corner undercutting. The corner compensation structure is based on M. M. Abu-Zeid's model [43].

But the above model did not work exactly for our case because of the alignment error and imperfect flatness of the silicon wafer. The maximum attainable etching depth was 400 μm with this mask layer design for our case, because of the each mirror's location in the silicon mirror array. Figure 2-4 shows the photograph (by using stereo microscope) of the fabricated mirror. It shows the top plane in mesa structure, and it shows the hillocks on the (100) plane. This is one of the disadvantages of TMAH. Since TMAH produces smooth side the {111} planes that are used as mirrors, the quality of (100) surface has nothing to do with the mirror usages.

To obtain the 1200 ~ 1300 μm height mirror, the design shown in Figure 2-3 was changed. Simply speaking, the length of the beam should be longer to get the target etch depth. But, the wafer has a limited area for the 16-mask opening with 8 beams each to be located. Therefore, 4 beams per mask opening were removed to prevent the overlapping of beams due to each mirror's location for the alignment with the through-holes. To simplify the design, the width of the beam was changed to narrow and the beam length was decided to have value of around lateral ratio times target etch depth. Figure 2-5 shows the corner compensation structure for the mirror that is supposed to be used in the dissertation. Four beams are attached to the squares.

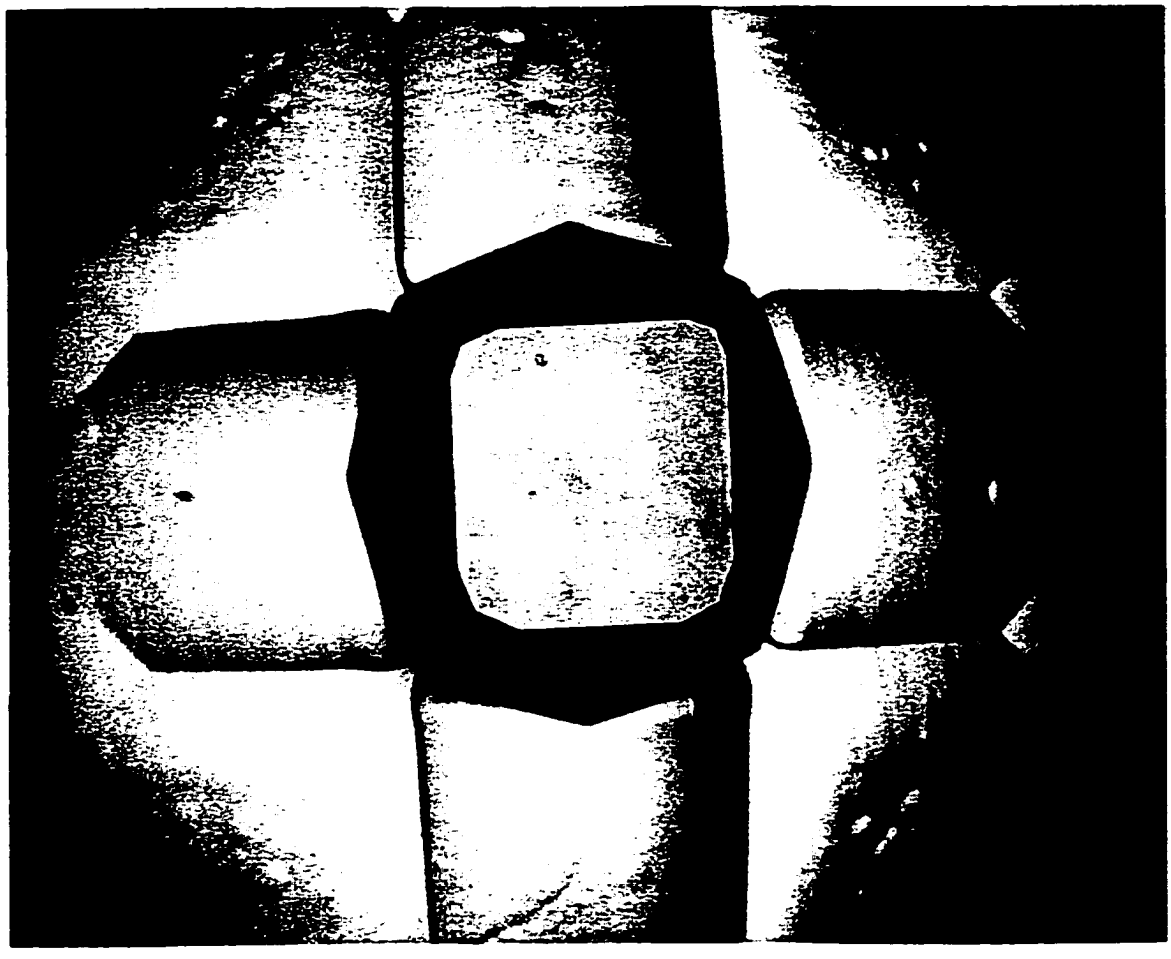


Figure 2-4. Fabricated Mirror

Stopping the etching process properly before the corner structures start to collapse is one of hardest jobs in mirror fabrication. Thus to easily find the stopping point of etching, the left side of the arms are designed longer than the right hand side arms. The etching process is stopped when the short-arm side of the corner structure begins to collapse. Since only one side plane of the four side planes in the mirror structure is used for the guiding optical signal, this design pattern was possible.

a. 1800 μm
b. 1100 μm
c. 975 μm
d. 350 μm
e. 9315 μm
f. 8615 μm

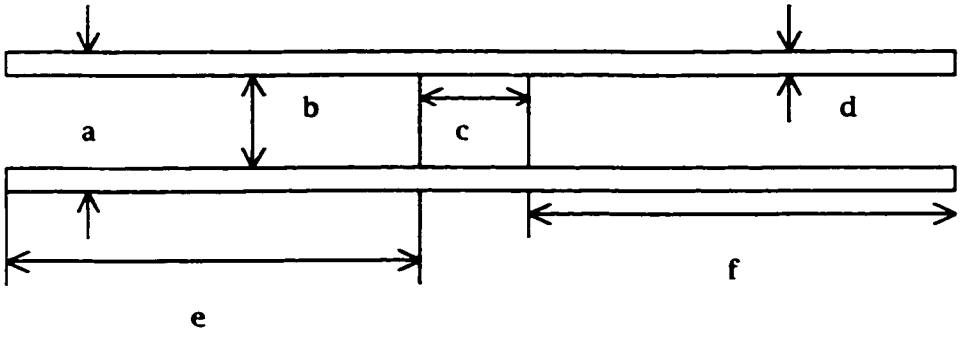


Figure 2-5. Corner Compensation Design

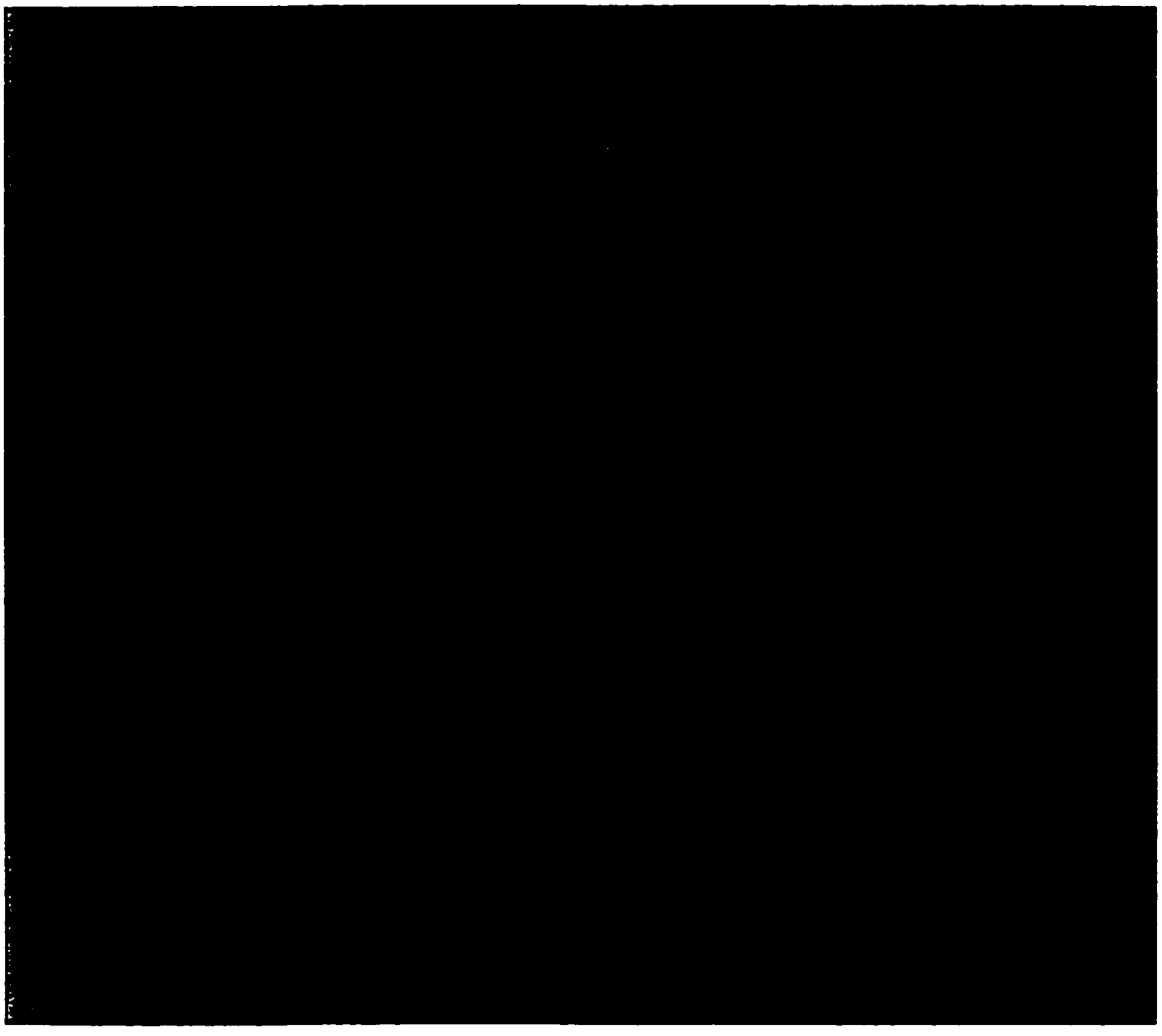


Figure 2-6. Mask Layer for Symmetric Sixteen Mirrors

Mask Design for Through-Holes

As opposed to a convex structure such as a mirror structure, a through-hole is a concave structure. The forms resulting from concave structures are dominated by slowly etching planes [17]. Since silicon belongs to the diamond cubic crystal structure, the (111) plane has a very high atomic packing density, and (100), (110) planes have low atomic packing densities. Therefore, micromachined structures are bounded by high atomic density planes. Figure 2-7 shows the {111} planes after micromachining of silicon.

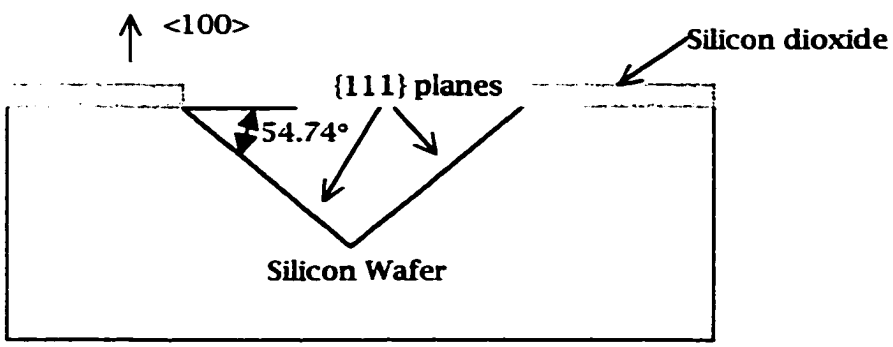


Figure 2-7. Micromachined Silicon Substrate

In the above figure, a mask opening is aligned to the <110> direction, and 54.74° has come from the following simple vector algebra:

$$\theta = COS^{-1}\left[\frac{(111)\bullet(100)}{|(111)|\times|(100)|}\right] = COS^{-1}\left(\frac{1}{\sqrt{3}\times 1}\right) = 54.74^{\circ}$$

where θ is the angle between (111) plane and (100) plane.

If the silicon substrate is immersed in an anisotropic etchant such as TMAH, etching will proceed in the <100> direction until the etch front hits the {111} planes, intersecting the (100) plane at the edge of mask opening, and the etching will stop as in Figure 2-7 [41]. In bulk micromachining, the required area on the silicon wafer surface is larger than actual device size because of the anisotropic wet chemical etching characteristics. The diagram in Figure 2-8 explains this characteristc.

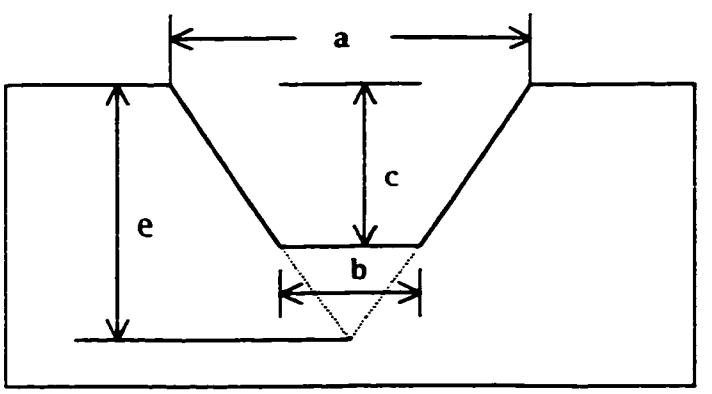


Figure 2-8. Geometry of an Etched Pit

In Figure 2-8, a is the mask opening, b is the width after some amount of etching, c is the etching depth after some amount of etching, and e is the etching depth when the etching ceases. The etch depth to oxide opening ratio is 0.707. And the relation between a, b and c can be driven as follows:

$$\frac{c}{(a-b)}=\frac{\tan\theta}{2} \quad where\ \theta\ is\ 54.74^{\circ}.$$

$$a-b=\frac{2c}{\tan\theta}=\sqrt{2}c$$

$$\frac{c}{a}=\frac{c}{b+\sqrt{2}c} \qquad \frac{c}{a}=0.707,\ if\ b=0$$

From the above equations, we know the enlargement effect of bulk micromachining. Therefore, the width of the oxide opening should be 1.414 times larger than the actual device feature size. With this concept, a mask layer for back side opening squares was designed, and special alignment marks were used for minimizing the alignment error. Because the front side of the substrate is covered with silica glass, it is hard to see the alignment mark on front side of the substrate even though the IR aligner is used for the back side lithography. Figure 2-9 shows the dimensions and shape of the mask layer design.

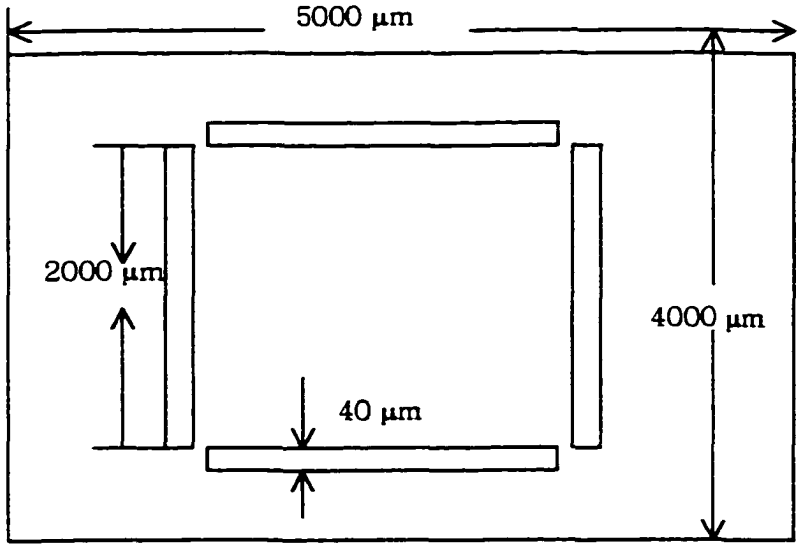


Figure 2-9. Mask Layer for Through-Holes

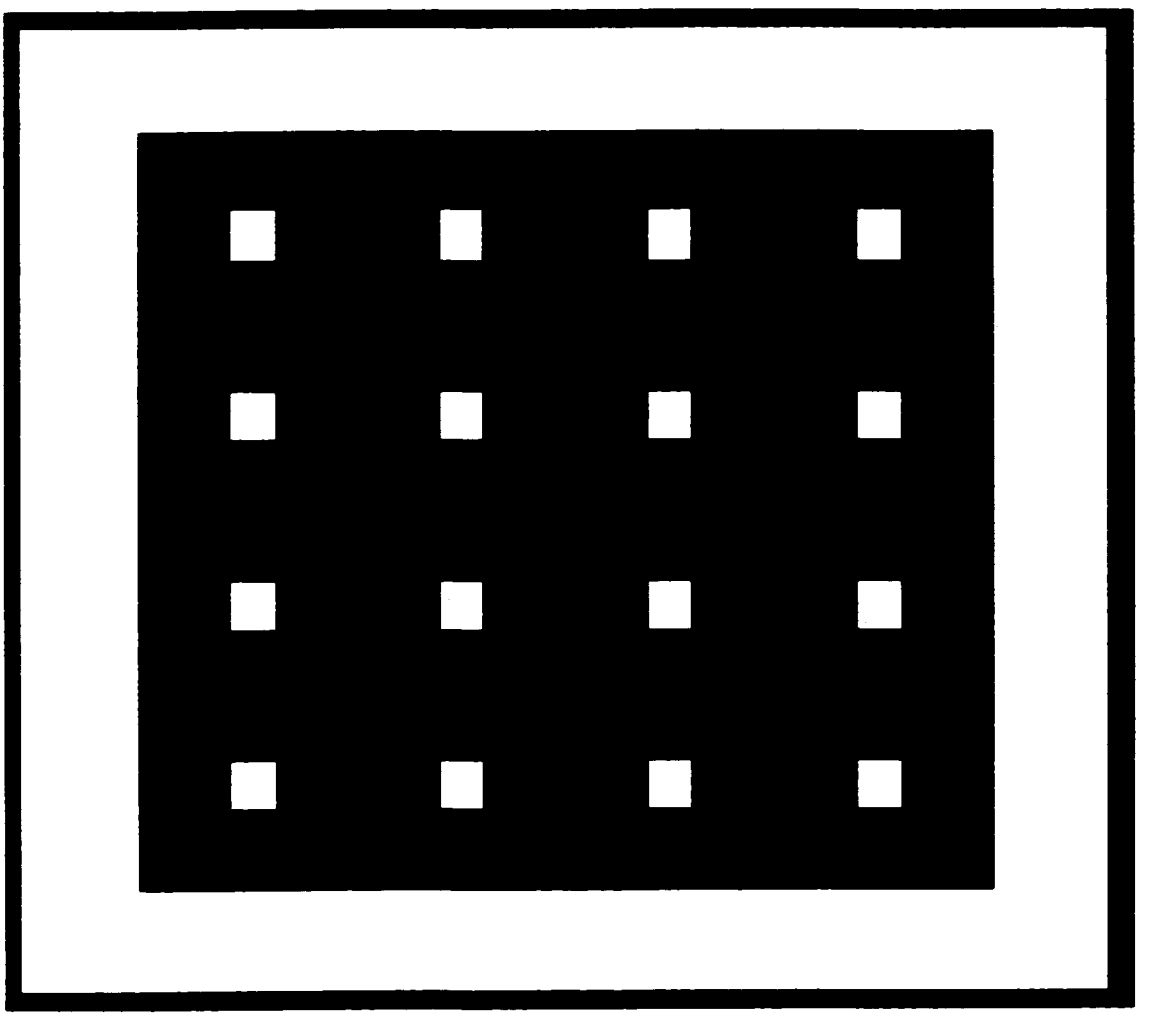
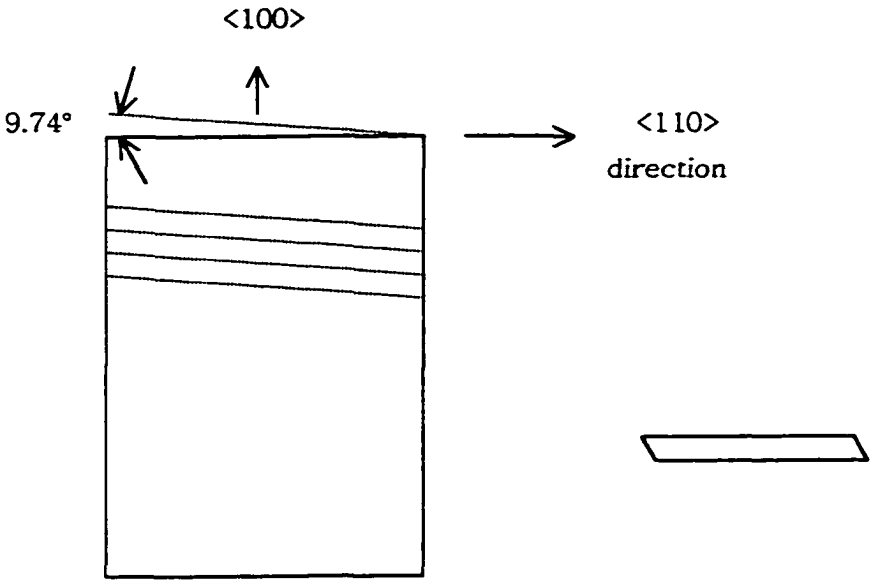


Figure 2-10. Mask Layer for Sixteen Through-Holes

Fabrication of 45° Mirrors

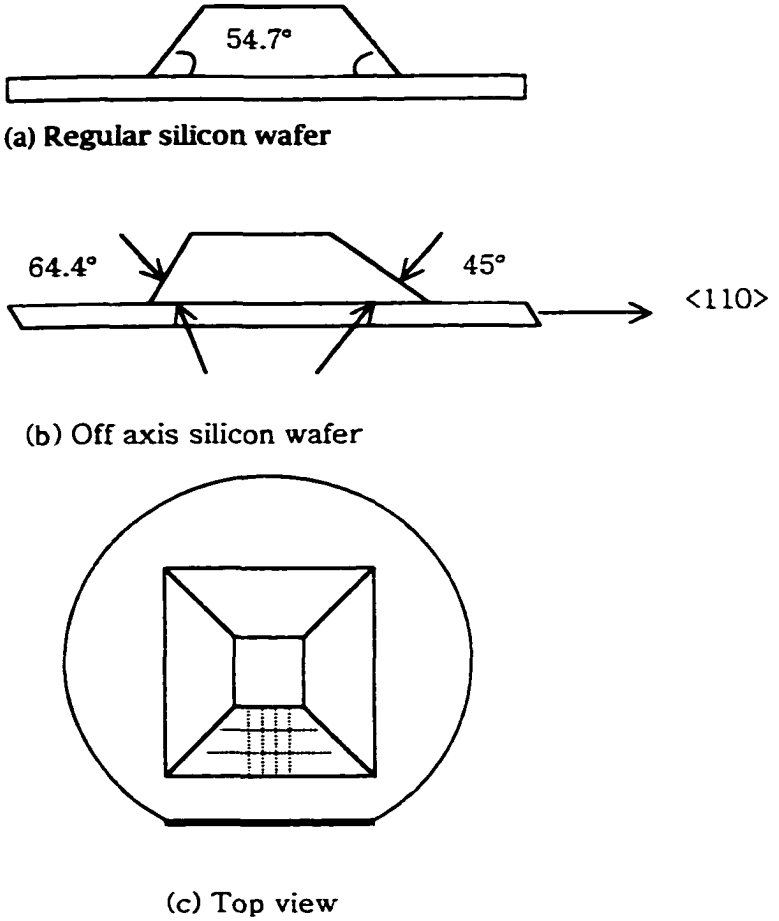
In integrated optic devices, the purpose of the mirror is to change the direction of the guided beam. Compared to the 54.74° mirror, the 45° mirror provides more accuracy in guiding the beam. There are two methods to fabricate the 45° mirror. One is to reveal the {110} planes on (100) silicon wafer, and the other is to use a 9.7° off axis (100) silicon wafer [48,49]. In our project, the second method was used to create the 45° mirror. Figure 2-11 shows the geometry of the off axis (100) silicon wafer.



(a) Cutting direction (b) Side view of a off axis wafer

Figure 2-11. Geometry of Off Axis Silicon Wafer

The dot lines, which are slanted 9.7° to <110>, indicate the wafer cutting direction. From the above figure, the front surface can be easily recognized by investigating the edge side. Since there is no mark on the silicon surface, determining which one is the front side is very important for designing the 45° mirror. Figurer 2-12 shows the angle of mirror plane with (100) surface.



(a) Regular silicon wafer

(b) Off axis silicon wafer

(c) Top view

Figure 2-12. Location of 45° Mirror

The hatched region on the above figure is the plane that has a 45° to the (100) surface. The opposite side has a 64°. The figure shown below displays the necessary location of the 45° mirrors and the direction of the incident beam.

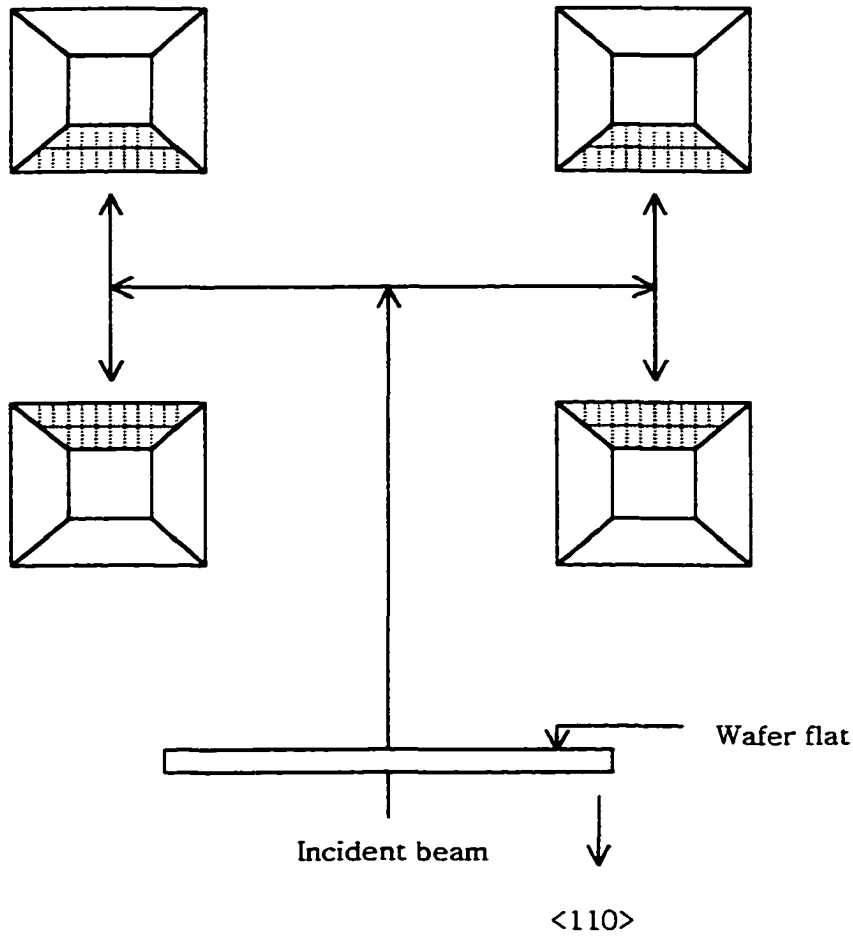


Figure 2-13. Direction of Incident Beam to 45° Mirrors

To achieve the desired location of the 45° mirrors, the wafer should be cut and flipped over parallel to the flat, and each piece of wafer should be bonded to the pyrex glass. Figure 2-14 shows the 45° mirror on the topside and 64° mirror on the bottom. It also shows the attatched corner compensation beams, which are slanted.

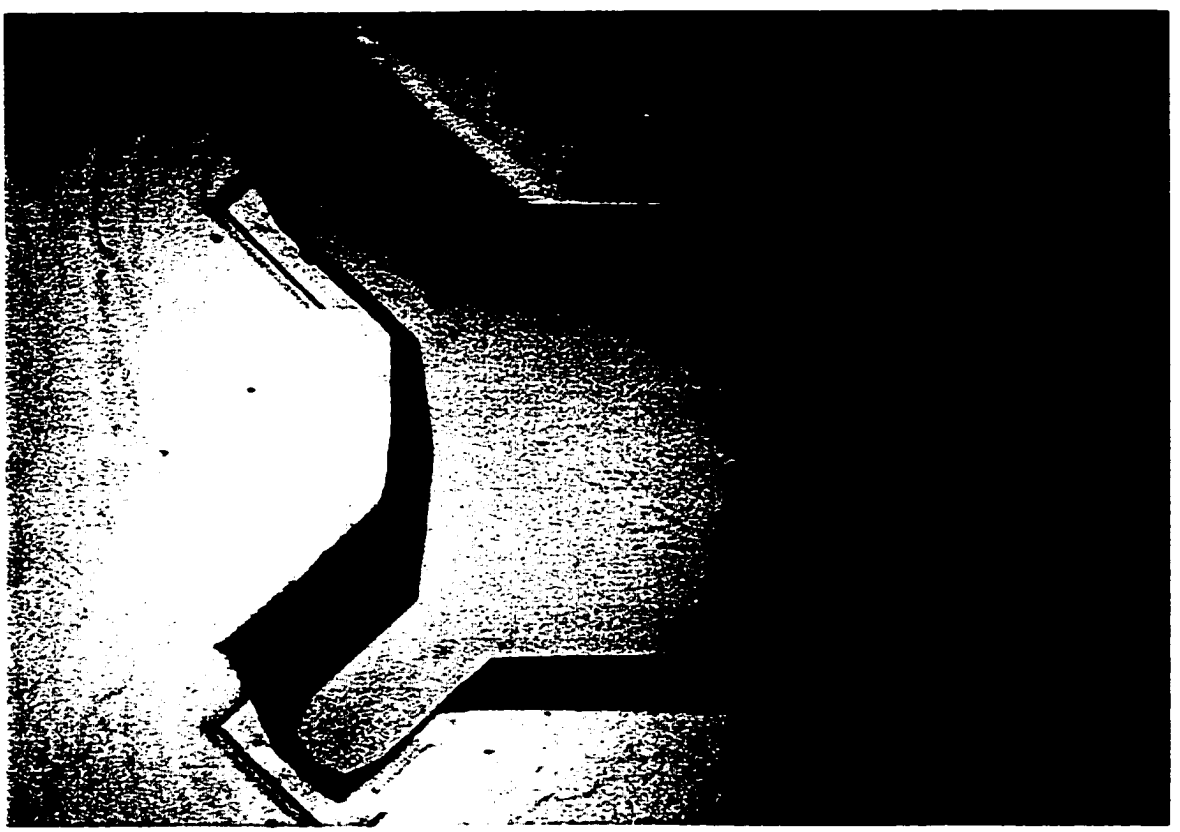


Figure 2-14. 45° Mirror During Bulk Micromachining

CHAPTER 3

INTEGRATED OPTIC WAVEGUIDE

To distribute the global signal within the multi chip module (MCM), guided-waves using a silica glass optical waveguide were designed, fabricated and characterized. The single-mode, step-index, buried-type silica glass waveguide networks were designed by utilizing H-tree network configuration and 3 dB Y-branching beam splitters to minimize the propagation losses and clock skew [50-53]. The Y-branching for 3 dB coupling has been selected due to its polarization and wavelength insensitive characteristics.

The silica glass optical waveguide networks are deposited on the silicon wafers using flame hydrolysis deposition (FHD) processes. The photonic integrated circuits are composed of three layer silica glasses and the waveguide is designed to be symmetric, single-mode, step-index, and buried type. The waveguide is formed, using silica glass layers with the varying refractive indices, by differing impurity doping levels in the silica glass. The channel waveguide has been formed using the reactive ion etching (RIE) process. The cross-sectional dimension of the waveguide is 6 μm by 6 μm, and the I/O coupling sidewall has been designed to be 1200 μm by 1200 μm to accommodate the silicon mirror arrays. The fabricated optical waveguide network is characterized by measuring the excess losses at the wavelength of 1550 nm.

Planar Waveguide

The channel waveguide, which is symmetric, and has a single-mode, was used as an optical interconnection within the MCM. Channel optical waveguides differ from planar waveguides in that they have additional transverse direction field confinement. But the investigation of planar waveguide theories is necessary to understand the wave propagation phenomena. In this section, cutoff frequency and cutoff thickness of the waveguide core at different wavelengths are calculated based on the planar waveguide theories. The design parameters and structures are shown in Figure 3-1.

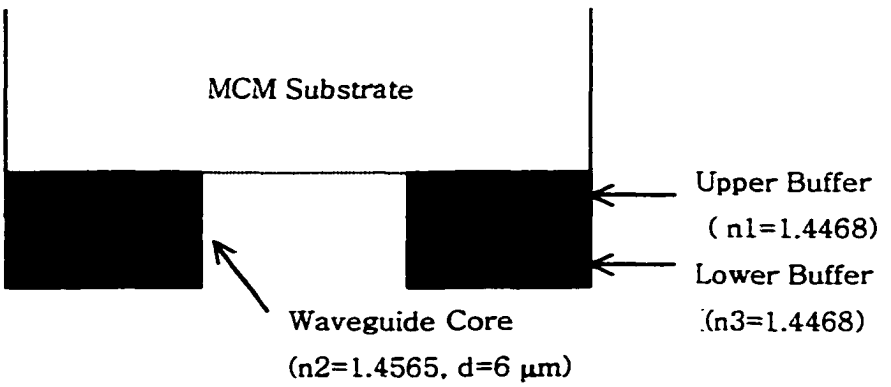


Figure 3-1. Silica Glass Waveguide Substrate

The space between waveguides shows the I/O coupling side wall and reveals that the core diameter is 6 μm. This waveguide network is used at the wavelength 1550 nm. Using the above parameters and a guidance condition for a symmetric waveguide, propagation mode is found graphically.

$$\tan(\frac{k_{2x}d}{2}) = \frac{\alpha_x}{k_{2x}} \qquad (3\text{-}1)$$

where $k_{2x} = \sqrt{\omega^2 \mu_0 \varepsilon_2 - k_z^2}$, d is a diameter of the core, and α_x is decay coefficient. The above guidance condition was drived under the assumption: (1) z is the direction of propagation, (2) the waveguide core is located between x = -d/2 and x = d/2, and (3) there is no field variation along the y direction. Figure 3-3 shows the graphical solution to the above equation.

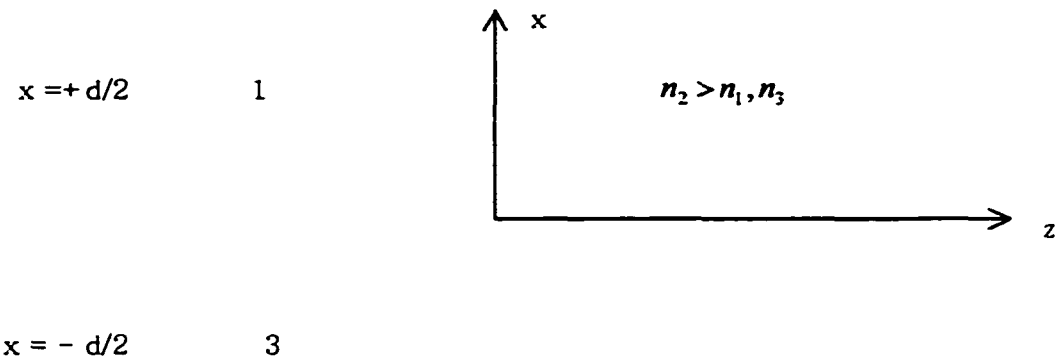


Figure 3-2. Three Layer Waveguide.

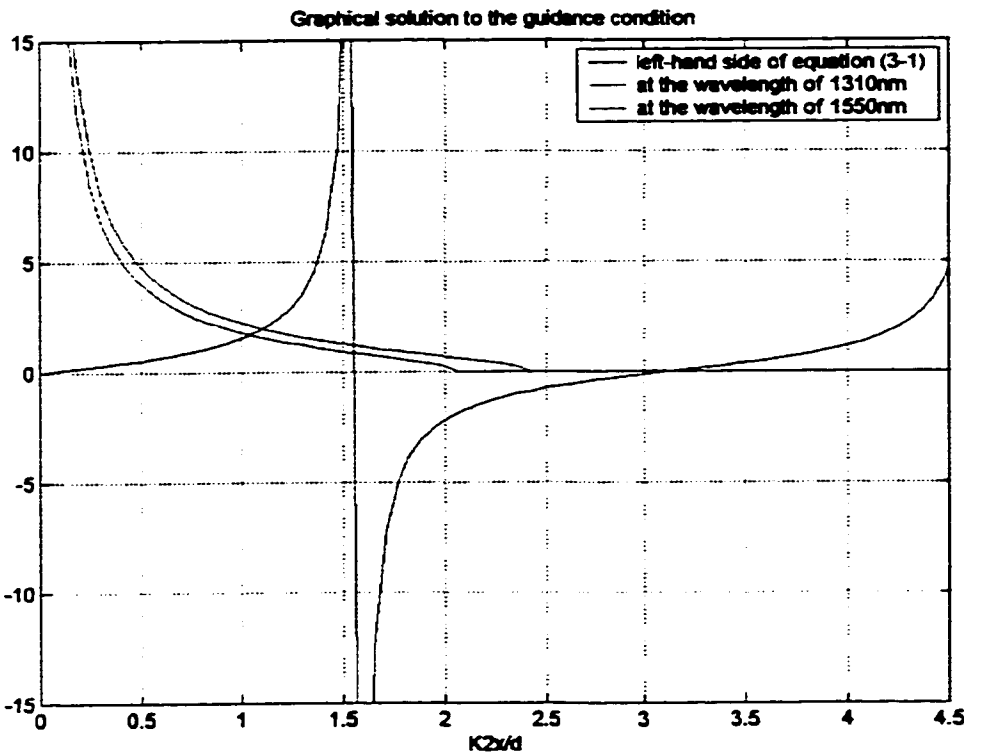


Figure 3-3. Graphical Solution of the Guidance Condition

The intersection point in Figure 3-4 represents the allowed solution. According to the graphical solution, only one mode is propagating in the optical waveguide network at two different wavelengths. But Figure 3-3 shows that the plot of the right-hand side of the equation (3-1) at 1310 nm wavelength is placed to right of the plot at 1550 nm. This means increasing frequency can introduce more propagating modes. Tables 3-1 and 3-2 show the cutoff thickness of core and the effective refractive index at two wavelengths for given refractive indices (n1 and n2) and core diameter (d).

Table 3-1. Cutoff Thickness

wavelength	n1	n2	Cutoff thickness
1.31 μm	1.4468	1.4565	3.9031 μm
1.55 μm	1.4468	1.4565	4.6182 μm

Table 3-2. Effective Refractive Index

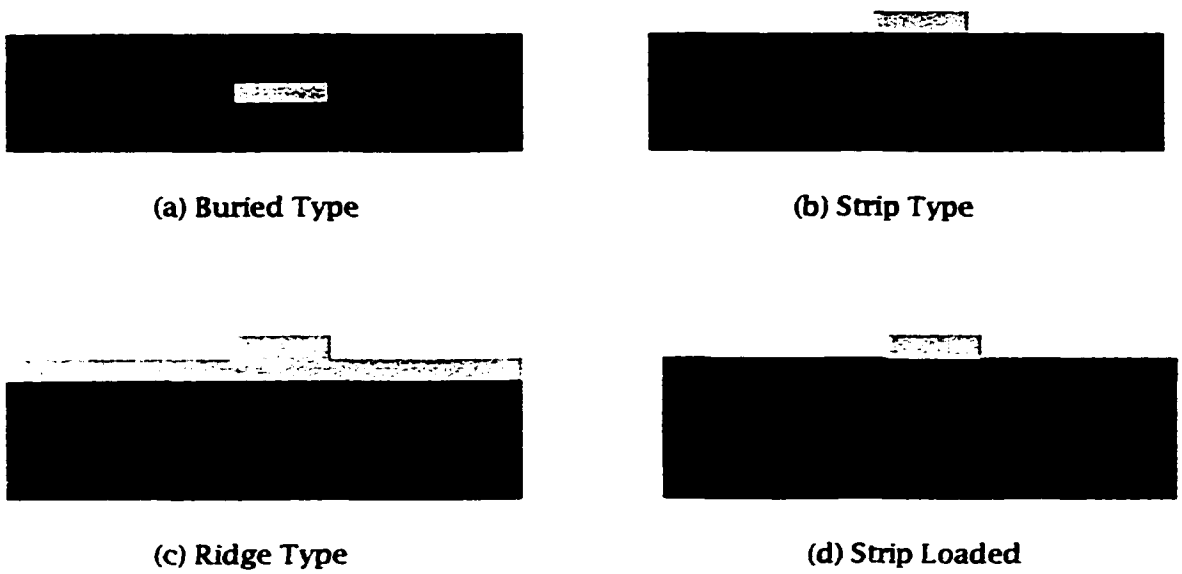
wavelength	n1	n2	Effective Refractive Index
1.31 μm	1.4468	1.4565	1.4545
1.55 μm	1.4468	1.4565	1.4540

Channel Waveguide

Channel waveguides have additional confinement in the transverse direction, so they give the desirable device characteristics. Channel waveguides are used in many active and passive devices of integrated optics, including lasers, modulators, switches and directional couplers [54].

Channel Waveguide Types

Generally, there are four types of channel waveguides. Figure 3-4 shows channel waveguide structures.



(a) Buried Type

(b) Strip Type

(c) Ridge Type

(d) Strip Loaded

Figure 3-4. Various Types of Channel Waveguides

The analysis of a channel waveguide is generally a complicated problem, and different approaches are used for each type. Since the analysis of the channel waveguide requires solutions of partial differential equations, powerful computers are necessary to obtain numerical solutions such as finite element (FE), finite difference (FD), method of lines (MoL) [55]. Although numerical methods are required to obtain the solutions, there are several approximations such as effective index method and Marcatili's method [56,57].

Radiation Bending Loss

When guided wave optoelectronic interconnections are designed on a single chip or multichip to make the signal distribution, sometimes bending sections are required. In this region, power loss happens because there is a change in propagation. In this section, the theory of bending loss and a new design for the bending section are introduced. Many bending loss theories and improved structures have been presented [58,59]. In this section, we followed Donald Lee's approach.

Changes in propagation direction within a waveguide cause a portion of the power to be radiated away from the guiding layer. Figure 3-5 shows the bending section of the waveguide. If the phase velocity ($V_p = \omega / k_z$) is measured along the axis of the bend under the approximation of $R \rightarrow \infty$, this would be equal to the tangential velocity at R from the center of the curvature.

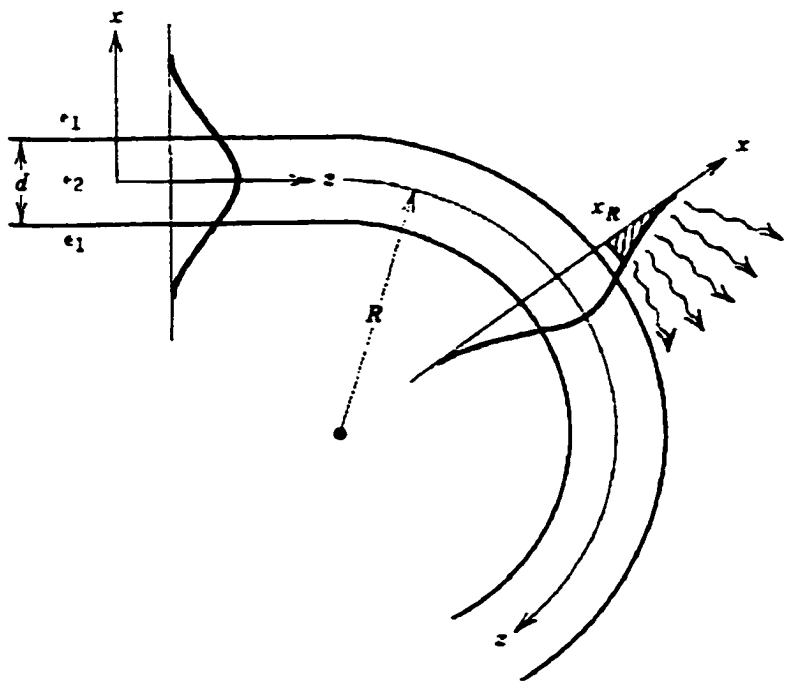


Figure 3-5. Bending Section of the Waveguide [58]

$$\frac{\omega}{k_z} = R\frac{d\theta}{dt} \tag{3-2}$$

In the upper buffer layer, the above equation changed as follows:

$$\frac{\omega}{k_1} = (x_r + R)\frac{d\theta}{dt} \tag{3-3}$$

where $k_1 = \omega\sqrt{\mu_0\varepsilon_1}$

By combining the equation (3-2) and (3-3), x_r is given in terms of the waveguide parameters by

$$x_r = \left(\frac{k_z - k_1}{k_1}\right)R \tag{3-4}$$

As the guided mode enters the bending section, the portion of the evanescent tail beyond x_r cannot travel as fast as the guided mode and so it splits away from the guide and radiates into upper buffer layer. If we assume that the rate of loss of total power contained in the waveguide at z is proportional to the power contained in the mode at that point, then

$$\frac{-dP(z)}{dz} = \alpha P(z) \tag{3-5}$$

where P(z) is the total power contained in the mode at any point z along the bend, α is the proportionality constant.

The above equation has the solution

$$P(z) = P(0)e^{-\alpha z} \tag{3-6}$$

and α is identified as the exponential decay constant. To compute the attenuation, equation (3-6) is solved for α.

$$\alpha = \frac{dP(z)/dz}{P(z)} \tag{3-7}$$

If the amount of power lost between the z and z + Δz is defined as P_L, then for small Δz, α is approximated as

$$\alpha \cong \frac{P_L(z)}{\Delta z P(z)} \tag{3-9}$$

And the quantity $\frac{P_L}{\Delta z}$ can be obtained following way:

$$\frac{P_L}{\Delta z} = \frac{power\ contained\ in\ tail\ at\ z}{distance\ for\ power\ in\ tail\ to\ radiate\ away} \tag{3-10}$$

Δz can be estimated by treating the portion of the waveguide field beyond $x = x_r$ radiating aperture as shown in figure 3-6.

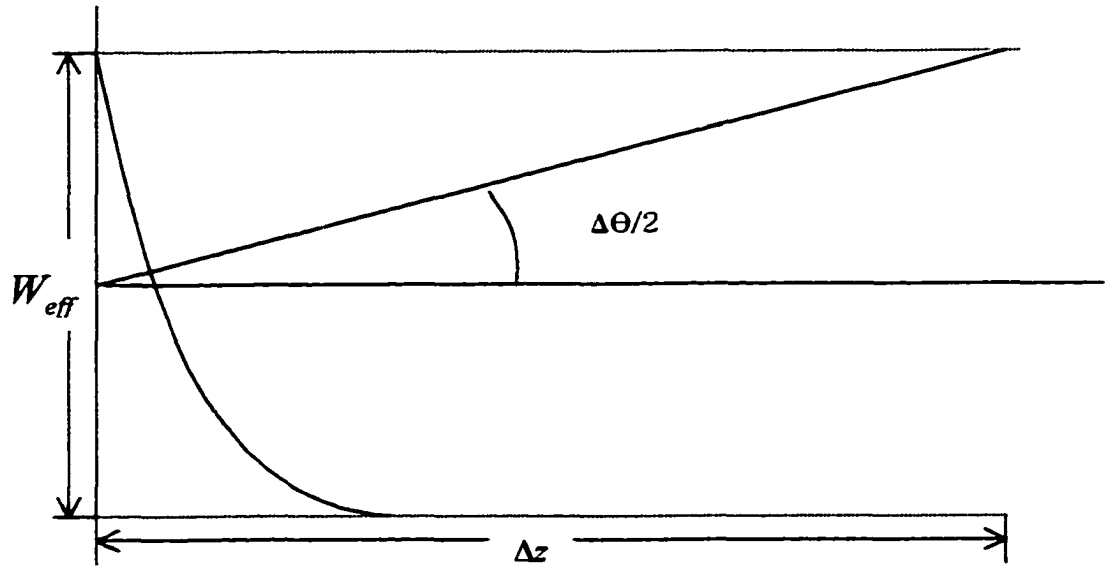


Figure 3-6. Radiation Aperture for Fields on a Curved Waveguide [58]

In upper buffer layer, the dispersion relationship is

$$k_x^2 + k_z^2 = k_1^2 \tag{3-11}$$

If $k_x << k_1$, the corresponding angular spread ΔΘ is given by

$$\tan\frac{\Delta\theta}{2} \cong \frac{\Delta\theta}{2} = \frac{k_x}{k_1} = \frac{\alpha_x \lambda_1}{2\pi}$$

therefore,

$$\Delta z \cong \frac{\pi W_{eff}}{\alpha_x \lambda_1} = \frac{\pi}{\alpha_x^2 \lambda_1} \tag{3-12}$$

Since the field at the aperature varies as $e^{-\alpha_x x}$, the aperature width can be approximated as $W_{eff} \cong \frac{1}{\alpha_x}$.

To find the exponential decay constant, P_L (amount of power lost between the arbitrary planes z and z + Δz) and P (z) (total power contained at any point z along the bend) should be derived. The power radiated away per unit length along z is

$$P_L = \frac{1}{2}\mathrm{Re}\int_{x_r}^{\infty}\left(\bar{E}\times\bar{H}^*\right)\cdot\hat{z}\,dx \tag{3-13}$$

And the total power is

$$P = \frac{1}{2}\mathrm{Re}\int_{-\infty}^{\infty}\left(\bar{E}\times\bar{H}^*\right)\cdot\hat{z}\,dx \tag{3-14}$$

For the fundamental mode on the symmetric slab waveguide,

$$\frac{1}{2}\mathrm{Re}\left(\bar{E}\times\bar{H}^*\right)\cdot\hat{z} = \frac{k_z}{2\omega\mu_0}|E_y|^2 \tag{3-15}$$

Using an equation (3-15), P_L and P expressed as follow.

$$P_L = \frac{k_z}{a\omega\mu_0\alpha_x}|A|^2\cos^2(k_{2x}d/2)e^{\alpha_x(d-2x_r)} \tag{3-16}$$

$$P = \frac{k_z}{4\omega\mu_0}|A|^2(d+2/\alpha_x) \tag{3-17}$$

where A is the amplitude coefficient. Therefore α is expressed as

$$\alpha = \frac{\alpha_x^{\,2}\lambda_1}{\pi(\alpha_x d+2)}\cos^2(k_{2x}d/2)e^{\alpha_x d}\exp[-2\alpha_x(k_z-k_1)R/k_1] \qquad (3\text{-}17)$$

The above equation can be written as the functional form

$$\alpha = C_1 e^{-C_2 R} \qquad (3\text{-}18)$$

where C_1 and C_2 are independent of radius R. When only a single-mode is guided, the propagation constant k_z can be approximated as follows.

$$k_z = \left(k_1^{\,2}+\alpha_x^{\,2}\right)^{1/2} = k_1\left(1+\alpha_x^{\,2}/k_1^{\,2}\right)^{1/2} \cong k_1 + \frac{1}{2}\frac{\alpha_x^{\,2}}{k_1} \qquad (3\text{-}19)$$

In this case, C_1 and C_2 are expressed as

$$C_1 = \alpha_x^{\,2}/k_1$$

$$C_2 = \alpha_x^{\,3}/k_1^{\,2}$$

The quantity α_x can be obtained in terms of the waveguide parameters.

$$\alpha_x d = \sqrt{v^2+1}-1 \qquad (3\text{-}20)$$

where v is the frequency parameter that is related to the normalized film thickness.

$$v = k_1 d\left(\frac{n_2^{\,2}}{n_1^{\,2}} - 1\right) \tag{3-21}$$

Figure 3-7 shows the attenuation as a function of bending radius at two different wavelengths. From the figure 3-7, it is noted that radiation loss increases exponentially with decreasing bending radius. In integrated optic devices there are limited available spaces, so a bending radius cannot be increased beyond a specific point to further reduce the radiation loss. To solve this problem, a new bending design was suggested. Figure 3-8 shows the bending section of the waveguide, which consists of many segments [59].

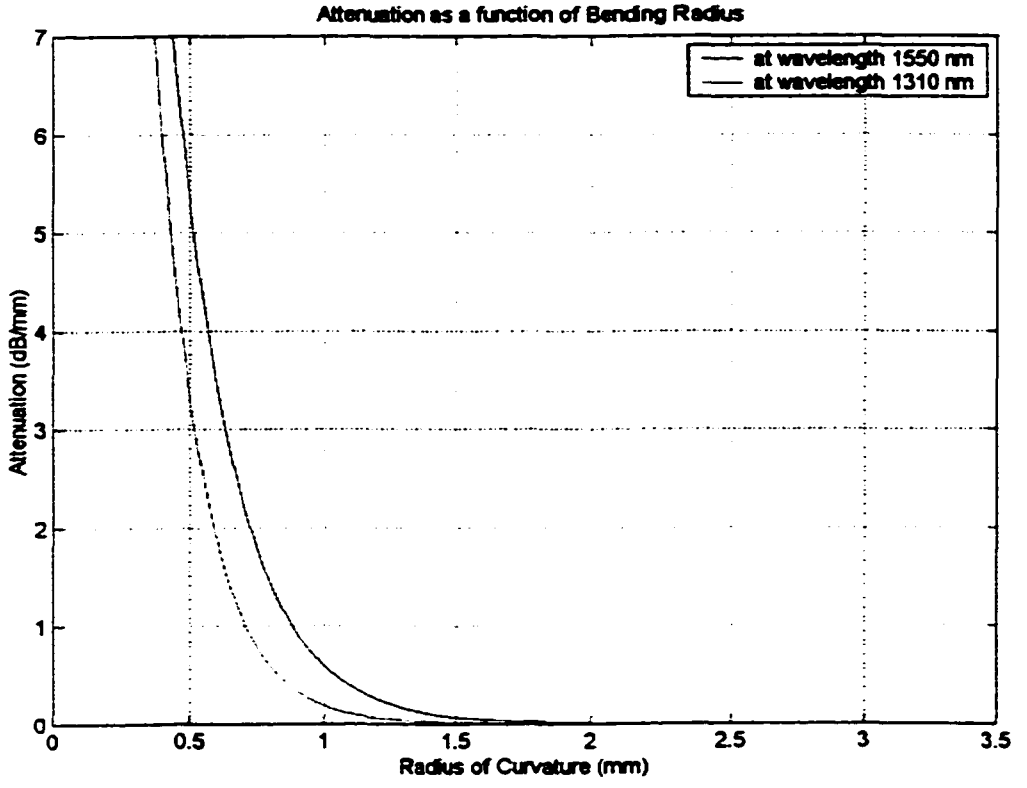


Figure 3-7. Attenuation as a Function of Bending Radius

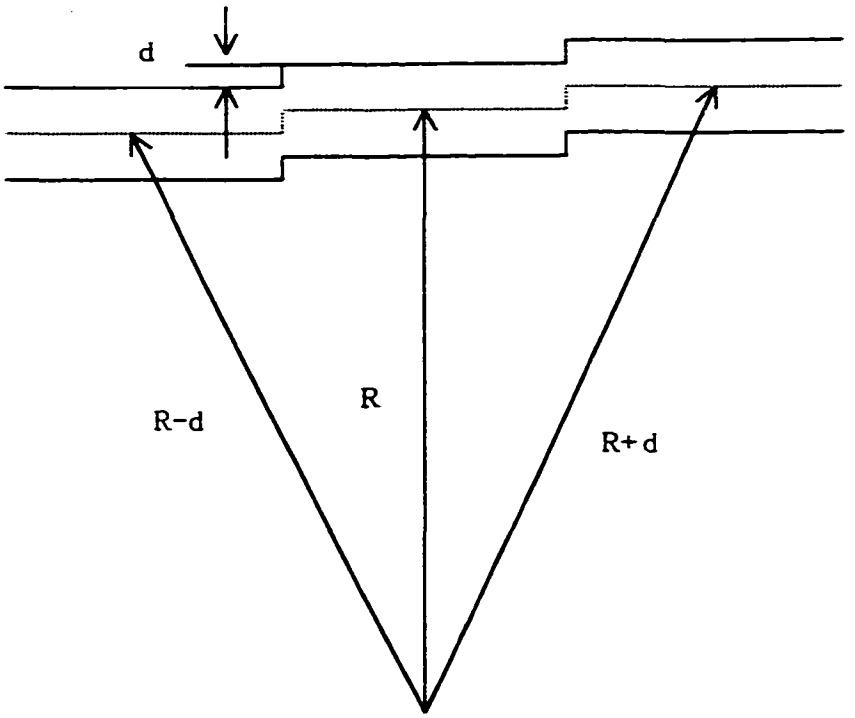


Figure 3-8. New Bending Section Design

Y-Branching Waveguide

A single-mode Y-branching waveguide is used as a power divider or combiner [60-64]. Figure 3-9 shows the structure of the Y-branching waveguide.

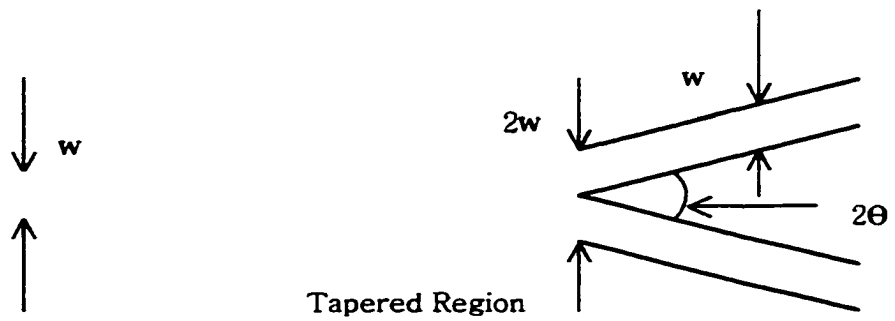


Figure 3-9. Y-Branching Waveguide Structure.

A Y-junction consists of a single-mode input guide that is gradually separated by a tapered region into two similar single-mode ouput guides. When light is incident from the one-waveguide end, the gradual taper of the waveguide width causes the light to spread with most of the power staying in the lowest-order mode of the waveguide. As this light is incident on the two-waveguide section, the incident light is divided and equal amounts of power propagate in the two branches with some scattering loss at the junction [61].

Since the operation of this device is complicated, it is useful to see the characteristic modes of the entire structure at each end [62].

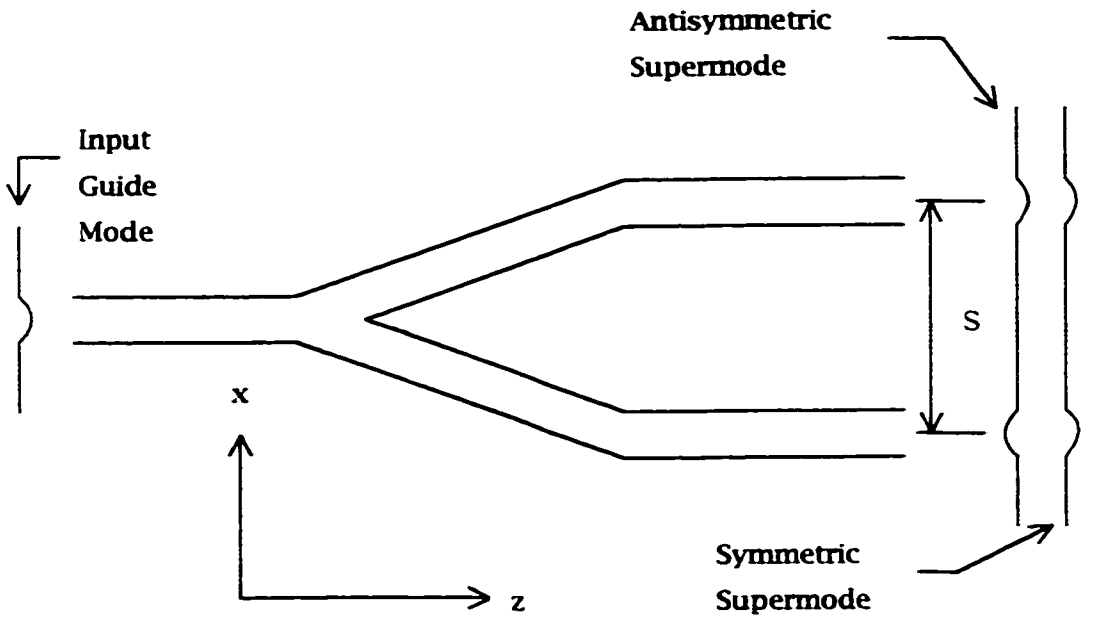


Figure 3-10. Characteristic Modes of a Symmetric Y-Junction [62]

The left side of the structure consists of one single-mode guide that supports a characteristic mode with a transverse field distribution

$$E_L(x,y) = E(x,y) \tag{3-22}$$

The right end of the device consists of two similar single-moded guides separated by a distance S. The transverse field patterns are

$$E_{RU}(x,y) = E(x-S/2,y) \quad \text{and} \quad E_{RL}(x,y) = E(x+S/2,y) \tag{3-23}$$

where E_{RU} and E_{LU} are transverse patterns of the upper and lower guides. The combined structure at the right hand end can be thought of as

a composite guide that supports its own characteristic modes, known as supermodes. Since the structure is symmetric, we shall assume that the supermodes are symmetric and anti-symmetric field patterns. These patterns are labeled E_{RS} and E_{RA}. Therefore, at the right-hand end of the device, we assume that the combined structure can support two guided supermodes of the form:

$$E_{RS}(x,y) = E_{RU} + E_{RL}$$
$$E_{RA}(x,y) = E_{RU} - E_{RL} \qquad (3\text{-}24)$$

Figure 3-10 shows the response to an input to the single guide at the left end. At some reference point near the input, the transverse field can be taken as

$$E_{in} = a_{in} E_L(x,y) \qquad (3\text{-}25)$$

where a_{in} is the input mode amplitude. According to the theory of local normal mode, the single input gradually converts into the symmetric supermode in the tapered region. Because the taper itself is symmetric, no anti-symmetric modes can be excited. At some reference point near the output, the transverse field can be written as

$$E_{out}(x,y) = a_{out} E_{RS}(x,y) \qquad (3\text{-}26)$$

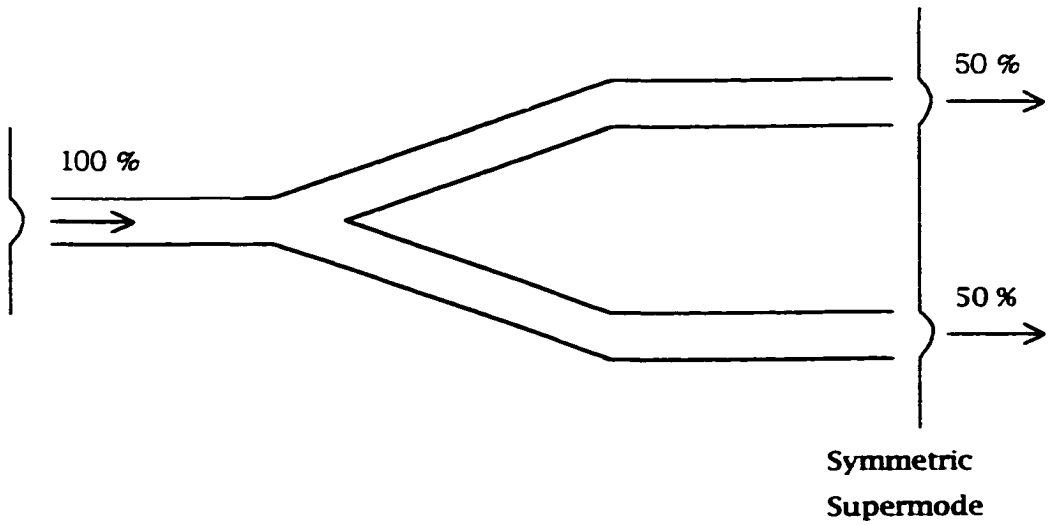


Figure 3-11. Excitation of a Y-Junction at the Left End [62]

Assuming 100% efficiency, the field amplitude can be calculated. The input power is given by

$$P_{in} = (\beta / 2\omega\mu_0) a_{in}^2 \langle E, E \rangle \tag{3-27}$$

where β is propagation constant and $\langle E, E \rangle = \int_{-\infty}^{\infty} E^2 dx$. While the output power is

$$P_{out} = (\beta / 2\omega\mu_0) a_{out}^2 \langle E_{RS}, E_{RS} \rangle \tag{3-28}$$

If the two output guides are sufficiently far apart, equation (3-28) can be approximately written as follows:

$$P_{out} = (\beta / 2\omega\mu_0) a_{out}^2 \{\langle E_{RU}, E_{RU} \rangle + \langle E_{RL}, E_{RL} \rangle\}$$
$$= 2(\beta / 2\omega\mu_0) a_{out}^2 \langle E, E \rangle \quad (3\text{-}29)$$

where we have assumed that $\langle E_{RU}, E_{RU} \rangle \approx 0$. From equation (3-27) and (3-29),

$$a_{out} = \frac{a_{in}}{\sqrt{2}} \quad (3\text{-}30)$$

Equation (3-26) can be reexpressed as

$$E_{out}(x,y) = (a_{in} / \sqrt{2}) E_{RU}(x,y) + (a_{in} / \sqrt{2}) E_{RL}(x,y) \quad (3\text{-}31)$$

The equation implies that the Y-junction divides the input equally between the two output guides. The derivation of equation (3-31) follows Richard Syms and John Cozens's book. The operation as a power combiner was described by these researchers [62,65].

Directional Coupler

Directional coupler is a fundamental element in optical integrated circuits (OIC) and forms the basis of many distribution networks [66-68]. Figure 3-12 shows the typical four-port directional coupler.

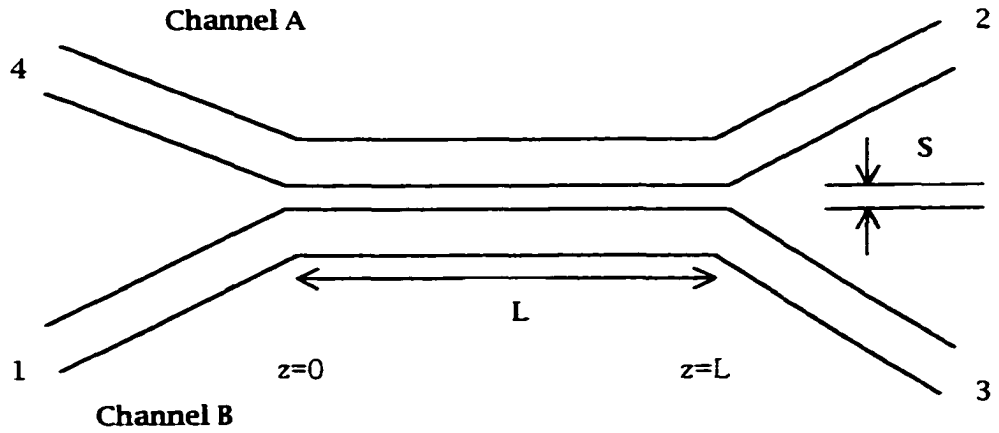


Figure 3-12. Directional Coupler

The coupling of light between two channel waveguides A and B occurs when light propagates as long as the separation between two channels is small. By using coupled mode theory, output powers at port 2 and port 3 can be expressed as [58]

$$P_A = P_{in}\frac{|C_{BA}|^2}{S^2}\sin^2(Sz) \tag{3-32}$$

$$P_B = P_{in}\left[\left(\frac{\Delta k}{2S}\right)^2 \sin^2(Sz)+\cos^2(Sz)\right] \tag{3-33}$$

where C, P_A , P_B. P_{in} and S are the coupling efficiency, output power at port 2, output power at port 3, input power and the separation between two identical channel waveguides, respectively.

Δk and S are given as

$$\Delta k = k_{zA} - k_{zB}$$

$$S = \sqrt{\left(\frac{\Delta k}{2}\right)^2 + C_{BA}C_{AB}}$$

Under phase-matched conditions ($\Delta k = 0$ and $C_{AB} = C_{BA} = C$),

$$P_A(z) = P_{in}\sin^2(Cz) \tag{3-34}$$

$$P_B(z) = P_{in}\cos^2(Cz) \tag{3-35}$$

Equations (3-34 &3-35) indicate that the length L_{dc} required for total power transfer under phase-matched condition. From equation (3-34)

$$\sin(CL_{dc}) = 1$$

$$L_{dc} = \frac{\pi}{2C} \tag{3-36}$$

Light will completely couple from one waveguide to the other at integral multiples of L_{dc} . For making 3 dB couplers, coupling length is adjusted as follows:

$$L_{3dB} = \frac{\pi}{4C} \tag{3-37}$$

For non-phase-matched condition ($\Delta k \neq 0$), complete power transfer cannot occur.

The maximum power transfer to channel A occurs when $Sz = \frac{\pi}{2}$.

$$P_{A\_max} = P_{in} \frac{|C_{BA}|^2}{C_{AB}C_{BA} + \Delta k^2/4} \tag{3-38}$$

From the above equation, we know that power transferred to channel A depends on phase mismatch (Δk). The appreciable power transfer requires that [38]

$$|\Delta k| < 2\sqrt{C_{AB}C_{BA}} \tag{3-39}$$

Fiber-to-Waveguide Couplers

One of the key elements of an integrated optic system is the coupler that transfers the optical waves between a fiber and a waveguide of the OIC [69]. The coupling efficiency depends on the overlap integral between the field profile of the incident wave and the modal profile of the guided mode [70]. In this section, the discussion of butt coupling, and grating couplers is presented.

Butt Coupling

Butt coupling is the process of forming the junction between entirely different guides. The fiber may be directly butted in contact with

the waveguide, without any interfacing device, in an end-on alignment [69]. Fiber-to-waveguide butt coupling has a high efficiency coupling, if the numerical aperture, the field profile, and fiber-to-waveguide alignment are matched. Since both optical fiber core and channel waveguide core have the dimensions around few micro-range, it is very difficult to align them.

The silicon V-groove technique has been introduced to align a channel waveguide with a single-mode optical fiber [71]. Sheem and Giallorenzi showed the alignment between 3 μm channel waveguide core and 4.5 μm fiber core using two-dimensional groove pattern on a silicon wafer. Figure 3-13 shows the schematic diagram of the alignment.

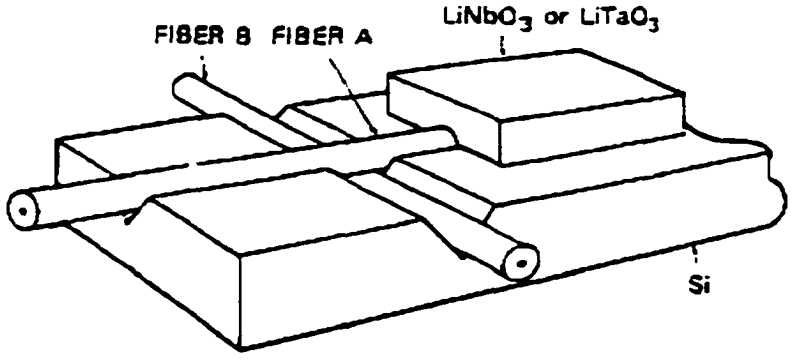


Figure 3-13. Fiber-to-Channel Waveguide Using Silicon Grooves [71]

Grating Coupler

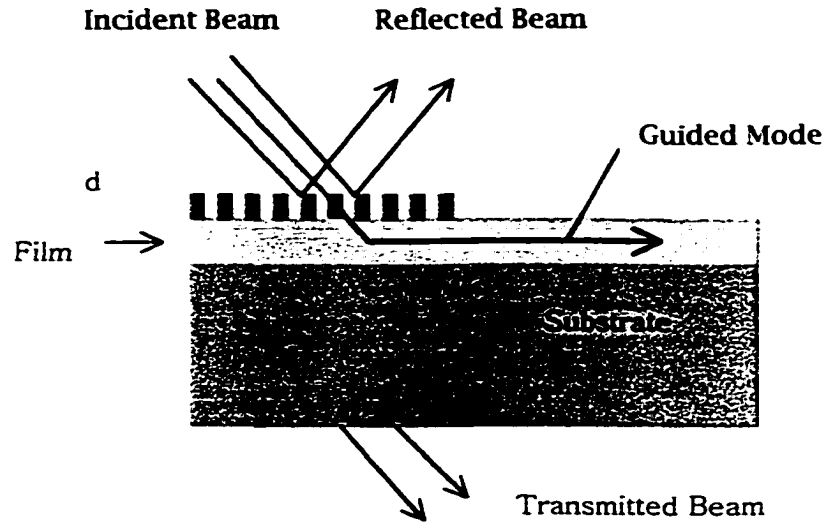


Figure 3-14. Grating Coupler

The structure of the grating coupler is shown in figure 3-14. The grating coupler produces a phase matching between a particular waveguide mode and unguided optical beams which is incident at an oblique angle to the surface of the waveguide [69]. The operation of the grating coupler is understood on the basis of the coupled mode theory. But there is an additional aspect because of its periodic nature. Therefore, the propagation wave vectors in the grating have the form [72]

$$\beta_{gr} = \beta_0 + \frac{2\pi\nu}{d} \tag{3-40}$$

where and $\nu = 0, \pm 1, \pm 2, \pm 3, \ldots\ldots$, d is the periodicity of the grating. The fundamental factor β_0 is approximately equal to the propagation in the

guide. The phase matching condition between grating-waveguide region and the air is given by [72]

$$k_a \sin\theta = \beta_{gr} \tag{3-41}$$

where k_a is the wavevector in air and θ is the incidence angle.

The main advantage of the grating coupler is that it can be the integral part of the waveguide structure, however its coupling efficiency is not as good as the prism coupler because of the transmitted beams.

Test Results and Characterizations

The actual power available to the detector is determined by the source power and the losses throughout the distribution system [25]. In this system, the power is required to be split equally and transferred to sixteen-fan-out. Input coupling to sixteen-fan-out OCDN is shown in Figure 3-15. Table 3-3 shows the optical power loss and signal uniformity. The test structures with one-to-sixteen beam splitters have shown a positive results with an average excess loss of 3.69 dB and signal uniformity of 1.44 dB at the wavelength of 1550 nm.

Table 3-3 Total Excess Losses for 1-to-16 Splitter Test Structure.

Channels	1	2	3	4	5	6	7
Power(dB)	-3.44	-3.49	-3.89	-3.96	-3.13	-3.52	-3.20
Channels	8	9	10	11	12	13	14
Power(dB)	-4.05	-3.30	-3.79	-3.88	-3.41	-3.38	-3.61
Channels	15	16	Average		STD	Uniformity	
Power(dB)	-4.35	-4.57	-3.69		0.41	1.44	

* The signal wavelength is 1550 nm and the total excess losses include losses from fiber to-waveguide coupling, waveguide propagation, waveguide bending, Y-branch, and waveguide-to-fiber coupling.

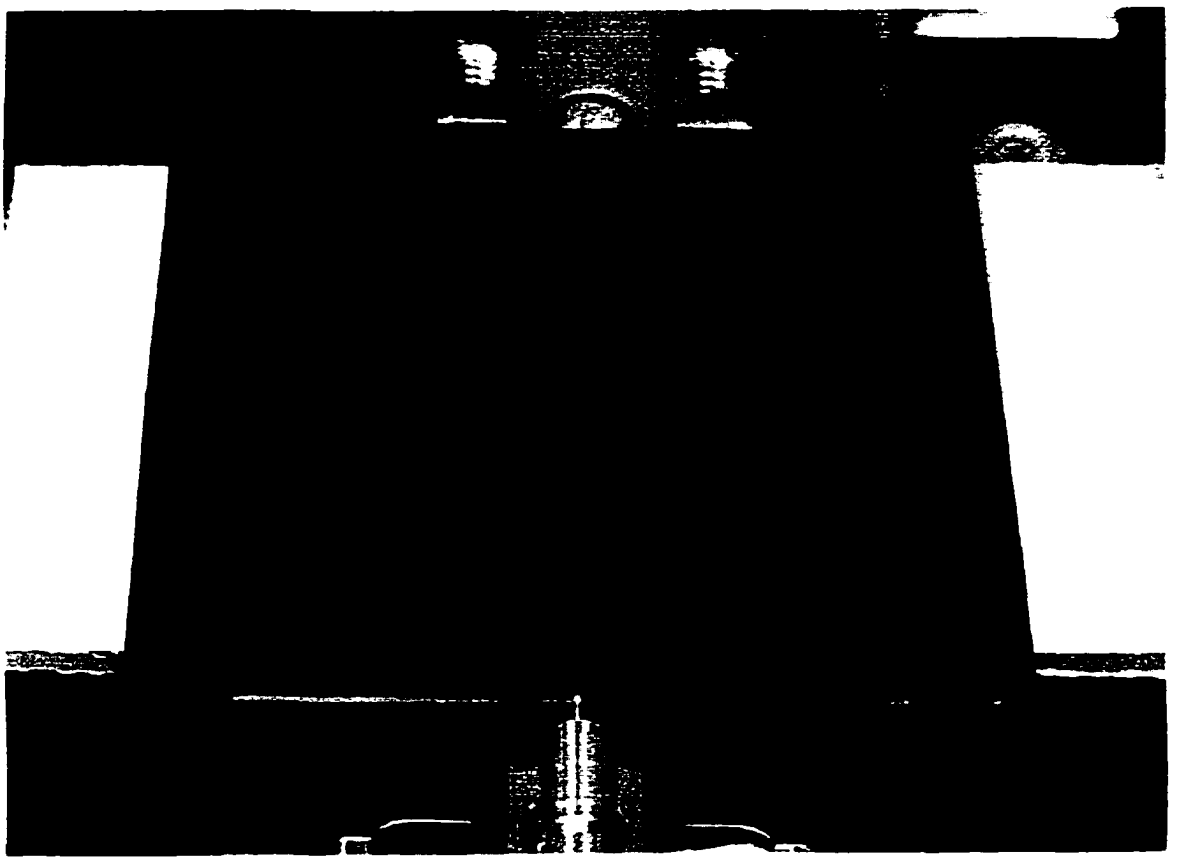


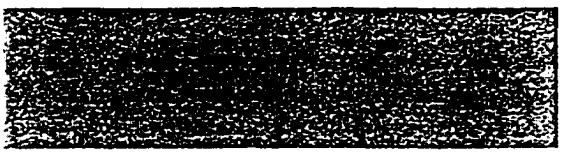
Figure 3-15. Sixteen Fan-Out OCDN Prototype Input Coupling

CHAPTER 4

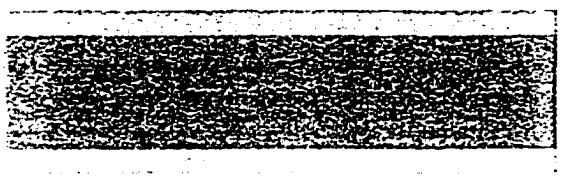
PROTOTYPE FABRICATION AND CHARACTERIZATION

Prototype Fabrication and Procedures

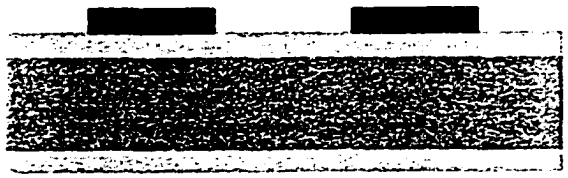
In this section, the procedures of the fabrication process are described. Figure 4-1 and Figure 4-2 show the overall fabrication procedures for mirrors and through-holes. The difference between the fabrications of these two microstructures is a lithography process.



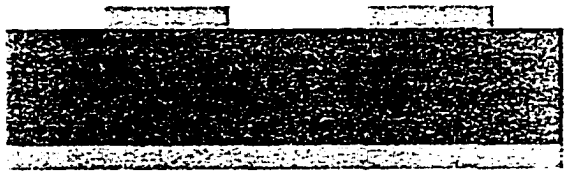
(a) Base Clean



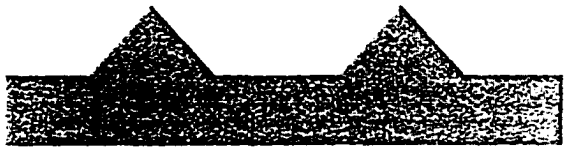
(b) Oxidation



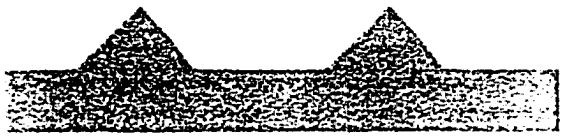
(c) Spin Coating, Exposure and Development



(d) Oxide Etch and Photoresist Removal

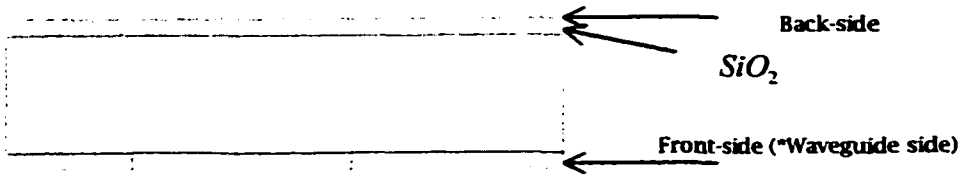


(e) Silicon Etching on Back Side
& Front Side Oxide Removal

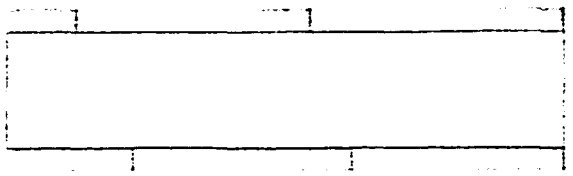


(f) Aluminum Coating

Fig 4-1. Fabrication Process of Silicon Mirror



(a) OE-MCM Substrate



(b) Back-side Lithography and Oxide Etching

(c) Bulk Micromachining

Figure 4-2. Fabrication Process of Through-Holes

*Detailed waveguide layers are shown in figure 1-4.

Based on the schematic diagrams shown above, each procedure is described here along with skillful tips.

Base Clean

The purpose of this procedure is to remove all the organic dirt from the surface of the silicon wafers prior to processing. To prepare the base cleaning solution, ammonium hydroxide (NH_4OH 27% aqueous solution) and deionized water (DI H_2O) are mixed in a beaker. Then slowly, the solution is heated on a hot plate to between 75°C and 80°C, and then the beaker is removed from the hot plate, and hydrogen peroxide (H_2O_2 30% aqueous solution) is added. The solution will bubble after 1~2 minutes when it is ready for use. After submerging the wafers into the solution for 15 minutes, the beaker containing the solution and wafers is placed under running DI H_2O for 3 minutes. During the base cleaning, contaminants tend to float to the top of the solution; therefore, during the DI H_2O rinse, it is important to flush the water in the beaker several times without allowing the wafers to break the surface of the liquid.

Oxidation

To mask the regions we do not want attacked by anisotropic (wet) silicon etchant when the microstructures are formed, we need to grow a silicon dioxide layer on our silicon substrate. There are two main chemical mechanisms for the growth of oxide by this process. If the oxide grows in the presence of molecular oxygen, a high-quality oxide would be generated, but fairly slowly:

$$Si + O_2 \rightarrow SiO_2$$

If we bubble the oxygen through water (in our case at a flow rate of 0.3 L/min. at ~ 99°C) we can increase the rate of growth. We then form oxide via the following reaction, with hydrogen as a by-product:

$$Si + H_2O \rightarrow SiO_2 + H_2$$

This so-called wet oxide is typically not as high quality as that grown by dry oxide as far as adhesion and other properties are concerned. However, it is generated at a much faster rate. Since the etching time required for creating the mirrors is more than 40 hours, enough thick oxide layers were grown on the silicon surface. Using a quartz-tube oxidation furnace, oxide was grown on both sides of the wafers. Typically, there is a 'flat zone' from 10 - 16" somewhere along the length of the furnace where the temperature remains approximately constant. With the help of the push rod, a quartz boat where wafers are loaded is inserted into this region of the furnace very slowly to prevent sudden thermal shock. The procedure for growing the oxide is to use 30 minutes of dry oxidation, 15 hours of wet oxidation, and 30 minutes of dry oxidation in order to obtain good quality oxides at the surface and silicon interface and still grow the oxide in an efficient manner. The oxide thickness was measured by using a Gaertner ellipsometer.

Table 4-1. Oxide Thickness

	Oxide Layer Thickness (μm)	
Wafers	Front Side	Back Side
1	1.69	1.69
2	1.72	1.73
3	1.71	1.73
4	1.72	1.72
5	1.73	1.73

Photoresist Spin Coating

In order to perform optical lithography (transferring layered patterns across the wafer to mask certain regions), we must employ a material that changes its solubility when exposed to this type of radiation. Photoresists (PRs) are organic, polymer-based molecules that either become more or less susceptible to dissolution in a developing solution when exposed to radiation (meaning any portion of the material exposed to UV radiation would be dissolved away by the developer, in our case S-351). This allows us to generate patterns by selectively removing or leaving parts of the PR layer on top of the substrate. The photoresist employed was a micro-positive S 1800 series photoresist manufactured by Shipley. S 1800 series are sensitive to light in the UV range and were used to protect the silicon dioxide mask layer from the buffered oxide etching (BOE or BHF) solution when it was used for opening a window in order to form the microstructures in the next step.

Before doing the photoresist spin coating, there is a preparation step for increasing the adhesion of the photoresist. It is a dehydration bake. The wafers are baked in the oven at $200°C$ for 30 minutes and then

cooled down at room temperature. After this step, the wafers are ready for a spin coating. If the photoresist is stored in the refrigerator, it is necessary for it to warm up to room temperature. HMDS (hexa-ethyl dislazane) was used as an adhesion promoter, and a micro-positive S 1800 series photoresist was used for spin coating. The table below relates specific S 1800 series products to corresponding film thickness at 3000 to 6000 rpm. The standard product name is derived from the coating thickness at 4000 rpm spin speed.

For this project, 3-inch thick silicon wafers were used. Because of the heavy weight, a high enough rpm could not be reached to obtain the thin layer of photoresist. Therefore, S 1805 photoresist was chosen, and spinning time was increased to obtain uniformly covered thin film. Table 4-3 shows the photoresist spin coating speed and times for 3 inch-thick silicon wafers.

Next, the photoresist was hardened by soft baking so sticking or smearing would not occur during the mask-wafer alignment necessary for exposure. This was done in an oven at 90°C for about 30 minutes.

Table 4-2. Photoresist Thickness vs RPM

Micro-Positive 1800 Series Photoresist				
Product Type	Photoresist Thickness (μm)			
	3000 rpm	4000rpm	5000rpm	6000rpm
1805	0.54	0.46	0.41	0.36
1811	1.23	1.06	0.93	0.83
1813	1.51	1.28	1.14	1.02
1815	1.78	1.53	1.34	1.22
1818	2.10	1.82	1.59	1.45
1822	2.58	2.20	1.95	1.77

Table 4-3. HMDS/PR Spin RPM and Times

	HMDS		Photoresist	
Cycle	Spin Speed (rpm)		Time (secs)	
Spread	10	400	10	400
Spin	60	1200	60	1200

Alignment, Exposure and Development

Alignment is the most important of all the steps because we can not fabricate the precise microstructures if the alignment error is too big. During the soft bake, the aligner must be warmed up to stabilize the UV (ultra violet) light. Once the soft bake is finished, the wafers are cooled down at room temperature, and a mask and a wafer are loaded into the chamber. Then a wafer edge is aligned to the alignment marks on the mask. The exposures take place in the spectral output range of 350 - 450 nm for nine and half seconds. The next procedure is development of S 1805 photoresist. Its purpose is to remove the area of the photoresist film exposed to UV light from the wafers. The preparation and procedures are as follows:

a. Mix 5 parts of DI water with Shipley 351 developer.
b. Immerse the wafer into the developer solution for 1 minute.
c. Rinse the wafer under running DI water for 1 minute.
d. Blow dry with filtered nitrogen.

After this step, inspection with a microscope is required. If any mistakes are found, every step after the oxidation should be repeated. Figure 4-3 shows the patterns after development.

Hard Bake and Back Side Protection

After the lithography, a hard bake is necessary to harden the photoresist and to remove the solvent to make it etch resistant. The hard bake procedure is the same as the soft bake procedure, except for the temperature setting.

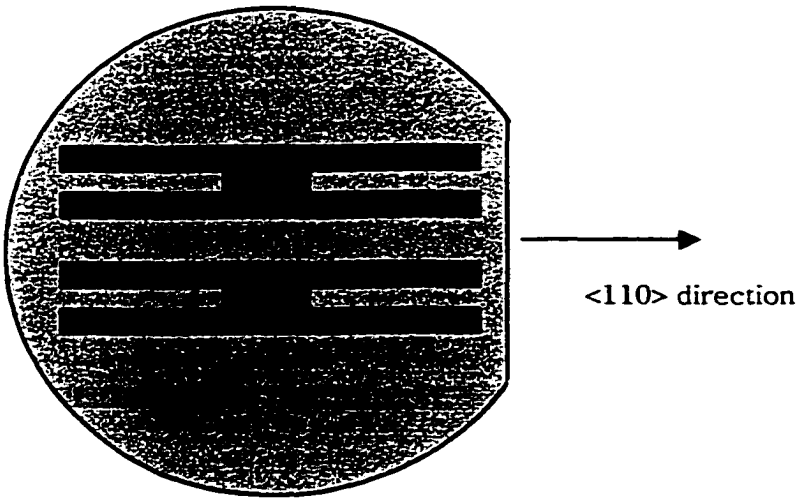


Figure 4-3. After Development

The hard bake is done at $105°C \pm 5°C$. Now, the wafers are ready for oxide etching, but sometimes photoresist stripping can occur during this process if the wafer is not dry enough or clean enough [3]. Since this project requires a long wet anisotropic etching, the back sides of the wafers should be protected perfectly. In addition, back side spin coating is not desirable because the vacuum pressure between a wafer and a chuck may cause damages on the front side (patterned side) of the wafer. The other problem is protecting the edge. Since the edge side of the wafer is rough compared to the polished surface, the oxide growth rate is low, and this condition makes it hard to cover the edge with photoresist. To solve these problems, the method used to protect an edge and back side of the wafer is as follows:

a. Prepare 4-inch glass wafers and AZ photoresist.
b. Spread photoresist on the glass wafer.
c. Put the silicon wafer on the glass wafer.
d. Bake at $60°C$ for 12 hours.

Isotropic Etching

One of the most frequently encountered photolithographic processes in monolithic integrated-circuit fabrication is the selective etching of thermally grown SiO_2 on silicon substrates. Wet chemical etching using HF or buffered HF is the most popular means for accomplishing this process. SiO_2 is readily attacked by room temperature HF, while silicon is not. It is therefore possible to selectively remove SiO_2 with HF solutions. As supplied by the manufacturers of electronic grade chemicals, the HF concentration is 49% aqueous solution. This is too strong a concentration for a controlled pattern definition. The HF can be diluted to 5 to 10% with DI water for a more controlled etch. Diluted HF loses its acidity during the etched process and must be replaced frequently. A more common etchant contains a buffering agent like ammonium fluoride (NH_4F), which helps maintain a constant acid-base ratio. In this project, the silicon dioxide was etched in BOE (Buffered Oxide Etching) solution. Since the measured oxide thickness with the ellipsometer was 1.8 μm, etching time was 18 minutes.

The etchant of the BOE is a mixture of 6 parts of NH_4F and one part of HF (49% aqueous solution). One interesting fact is that silicon is hydrophobic and silicon dioxide is hydrophilic. So the end point of etching can be easily seen. It is recommended, however, to check the etch result under the microscope because there may be little residual oxide spots. After this step, the photoresist is stripped using acetone, and the wafers are base cleaned to remove any organic dirt.

Anisotropic Wet Chemical Etching of Silicon

Anisotropic wet chemical etching requires careful attention. Even though TMAH etchant is a nontoxic material, it is very harmful to skin. To obtain the best results, careful measurements of the etch rate and temperature control of the etchant are required. Figure 4-4 shows the etching system for the bulk micromachining of silicon.

Etching of the silicon wafer is processed at different temperatures to measure the etch rate and investigate the surface quality. Since the target etch depth is 1200 ~ 1300 μm, both a higher etch rate and a good surface quality are needed to obtain the best reults. Table 4-4 shows the etch rate of silicon at various temperatures. The data reveals that the etch rate increases as the temperature increases. The surface quality, however, degrades at 90°C or higher. Thus it is concluded that 85°C is the optimum temperature for the etching process. After finishing the wet etching process, the residual oxide thicknesses of the wafers are measured. Only 0.3 μm is etched in TMAH, and this value is negligible compared to the 1250 μm silicon etch. So, the oxide layer on the silicon wafer acts as a good mask layer for the TMAH etching process.

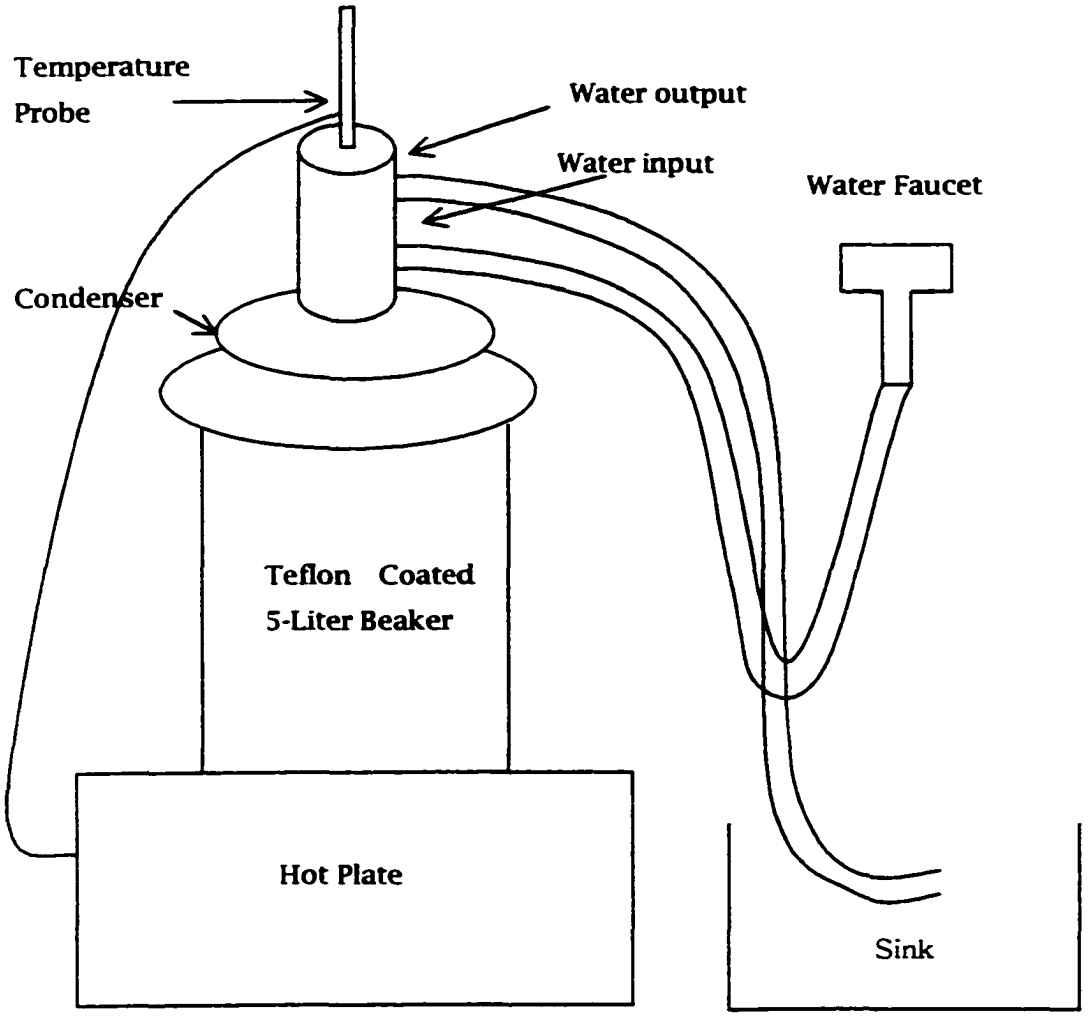


Figure 4-4 Anisotropic Etching System

Table 4-4 Etch Rate of Silicon Mirror

Temperature (°C)	Etch Rate (μm/hr)
70	14.3
75	17.0
80	19.8
85	25.6
90	35.5
95	45.5

The final step after anisotropic wet etching is a base clean of the silicon wafers to remove any organic etchant. This process is described in previous pages, and the residual oxide is removed by using BOE. After all fabrication steps, the aluminum is coated by using a sputtering machine to increase the reflectivity. The reflectivity of the silicon micromachined mirror array was 30%, but it was increased to 94% after the aluminum coating. This is shown at figure 4-6.

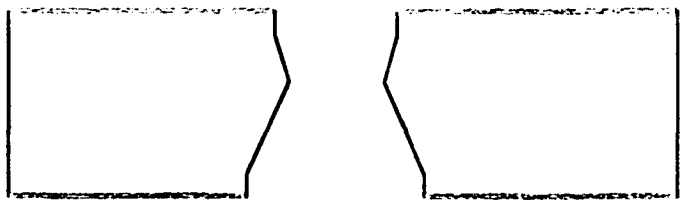
Through-Holes

The process of making through-holes on MCM substrate is very similar to the process of mirror fabrication steps. The only difference is the lithography process. Infrared (IR) aligner is used for back side alignment and exposure. In this process, etching takes place on both the front side and back side simultaneously. However, there is a slight etch rate difference between the front side and the back side of the MCM substrate.

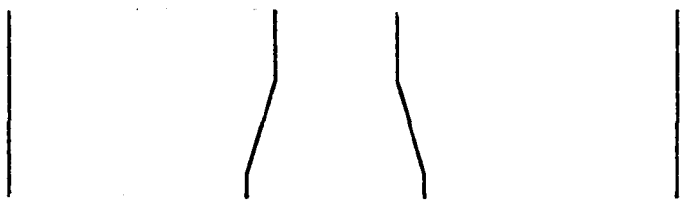
Table 4-5. Etch Rate of the MCM Substrate

	Etch Rate per Hour (μm/hr)	
Temperature (°C)	Front Side	Back Side
85	19.28	22.15
90	23.8	27.3

In Figure 4-5, (a) shows the substrate when the through-hole has just been created, and (b) shows the through-hole after the complete etching process.



(a) When through-hole is created



(b) After Complete Etching

Figure 4-5 Fabrication of Through-Hole

From Table 4-5 and Figure 4-5, it is shown that the back side of the substrate has a faster etch rate. This is because the back side opening has larger areas that interact with etchant. The dimensions of the openings are shown in table 4-6.

Table 4-6. Dimensions for Opening Squares on MCM Substrate

	Size of Opening Squares
Front Side	1200 μm × 1200 μm
Back Side	5000 μm × 4000 μm

Measurement Results and Characterizations

Bulk micromachining of silicon using a TMAH provided good etching selectivity and a well-controlled etch rate. Only 0.3 μm of the silicon dioxide layer was etched away during more than 40 hours of etching at 85°C. When this value is compared to the 1250 μm etch of silicon, it is negligible, and the selectivity is more than 4000. With a determined etch rate and etch selectivity of the TMAH etchant, deep and high quality silicon micromachined structures were fabricated. One interesting fact is that the fabricated structure shows the shape of a table cloth on the corner intersections, even though there is no under cutting. The fabricated silicon mirror prototypes have uniform and repeatable beam guiding performances at the wavelength of 1550 nm. Figure 4-6 shows the beam reflectivity of the silicon micromachined mirror. Aluminum was coated on the silicon mirror arrays to improve the I/O coupling efficiencies of the mirror arrays. Also, Figure 4-6 gives the comparison of the silicon mirror array reflectivity before and after the aluminum coating. It shows that the

reflectivity increased from 30% to 94% after the aluminum coating.

Micromachined silicon mirrors array substrate and the sixteen-fan-out optical clock distribution network (OCDN) with through-holes were assembled to build an MOEMS prototype. Figure 4-7 shows the assembled OE-MCM prototype and displays the laser beams of 635 nm wavelength at the sixteen fan-out nodes. This OE-MCM has a silicon mirror substrate underneath the optical waveguide layers, which are on the top surface of OE-MCM substrate. The laser signals are coupled into the OE-MCM by using the fiber-to-waveguide butt coupler. In addition, the total excess loss of sixteen-fan-out OE-MCM protype was measured at the wavelength of 1550 nm. Table 4-7 shows the total excess loss for assembled sixteen-fan-out OCDN signal propagation. The total loss includes fiber-to-waveguide coupling, waveguide propagation, waveguide bending, Y-branch, and through-hole output coupling losses. In this situation, the through-hole output coupling loss includes the losses due to mirror reflectivity,and waveguide-to-mirror coupling efficiencies associated with mirror size. The through-hole output coupling losses also include separation between waveguide end-facet and micromachined silicon mirrors.

Table 4-7 Excess Losses at 1-to-16 Fan-Out

Channels	1	2	3	4	5	6	7
Power(dB)	-13.4	-13.6	-13.2	-13.0	-13.2	-13.0	-13.6
Channels	8	9	10	11	12	13	14
Power(dB)	-13.4	-13.8	-13.4	-13.2	-13.2	-13.6	-13.4
Channels	15	16	Average		STD	Uniformity	
Power(dB)	-13.6	-13.4	-13.4		0.21	0.76	

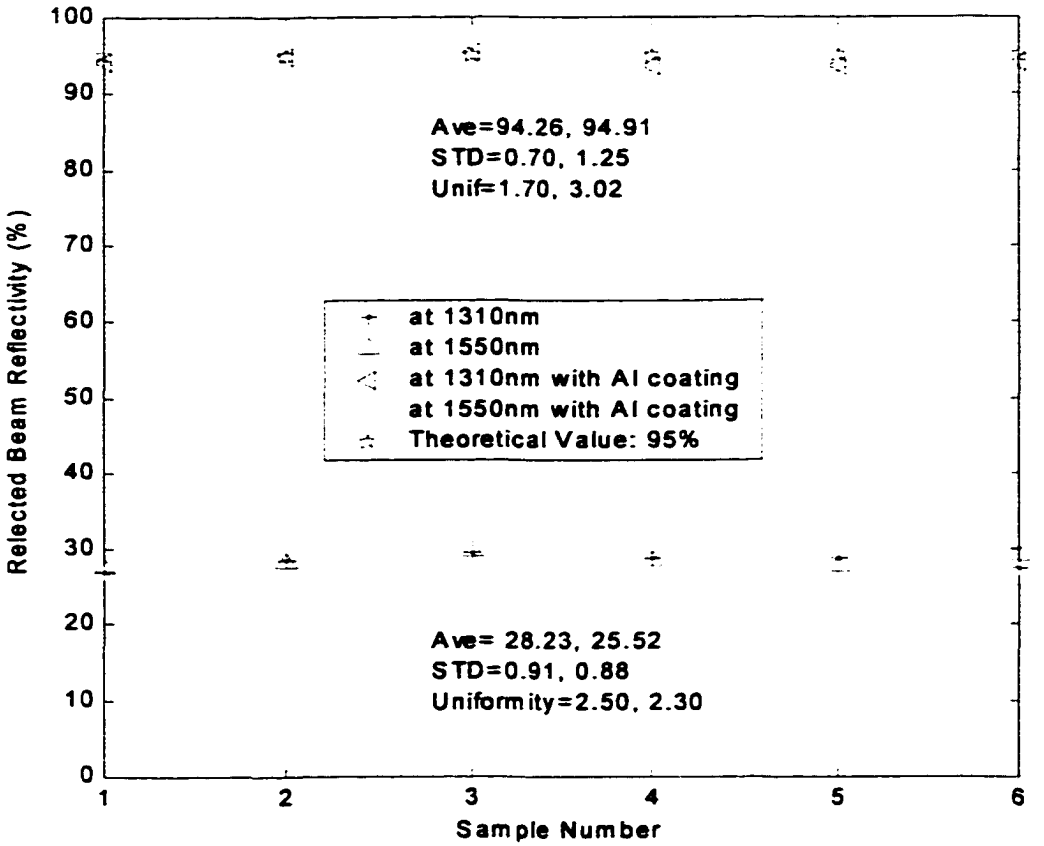


Figure 4-6. Beam Reflectivity of Silicon Mirror

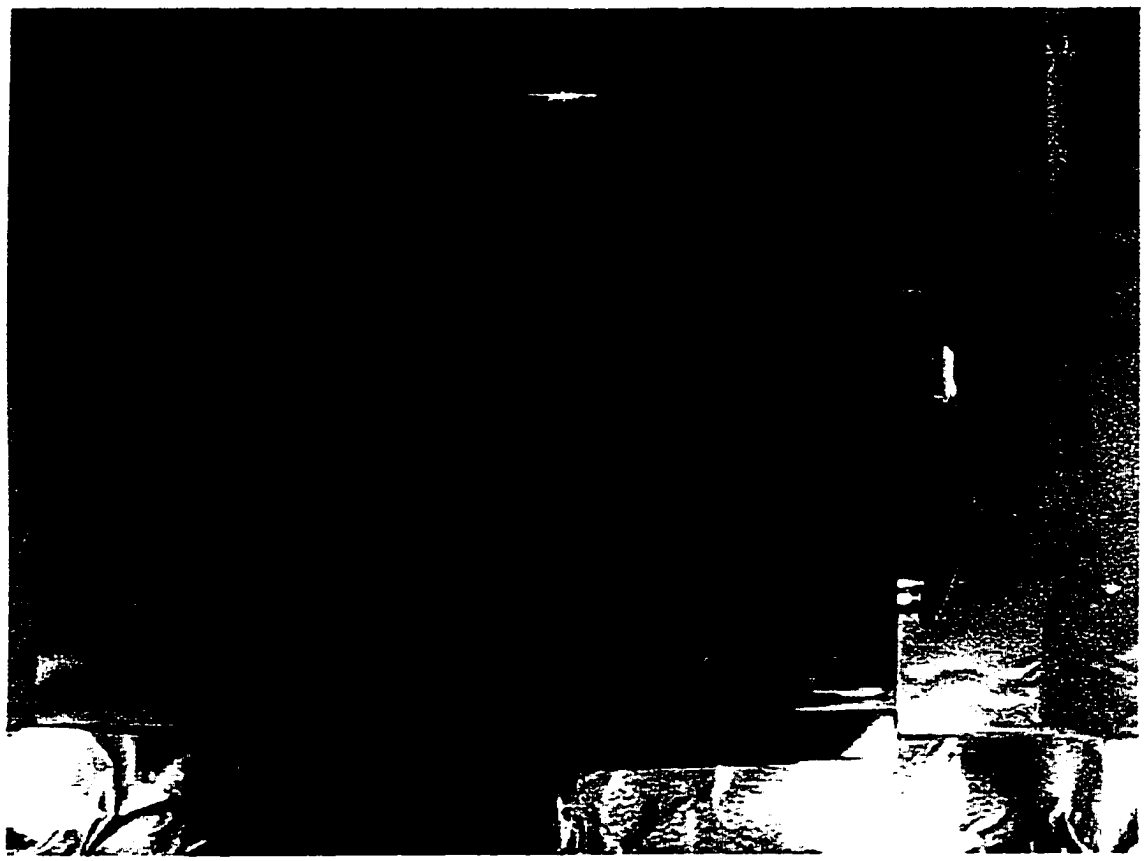


Figure 4-7. Assembled OE-MCM Prototype

CHAPTER 5

CONCLUSION AND FUTURE WORK

Conclusion

Throughout this dissertation, the main effort was the design and fabrication of the micromachined silicon mirror array that has an etching depth of around 1250 μm. Since the mirror has the form of a convex structure, many possible structures were tested at various temperatures to obtain the proper design parameters for a mask layer design that prevented corner undercutting during a long etching process. The fabricated mirrors have a smooth surface quality and are coated with aluminum. The beam reflectivity measurement shows 94%.

Fabrication of through-holes across MCM substrate was easily accomplished compared to the fabrication of the silicon mirror array. Because the through-hole has a concave structure, we could calculate the exact dimensions of the etched shape.

The MOEMS prototype, which contains the sixteen-fan-out OCDN on the OE-MCM and the micromachined silicon mirror array, was built by utilizing the silicon bulk micromachining technology. In addition, the fabricated prototype was characterized by measuring the optical power losses and signal uniformity. It was demonstrated that the OCDN itself distributed the signal uniformly and split the power equally to each sixteen fan-out node.

After assembly with the micromachined silicon array, the prototype still provided the uniform signal distribution with low excess loss. Figure 5-1 shows these results. From these facts, we concluded that fabricated silicon microstructures were very successful.

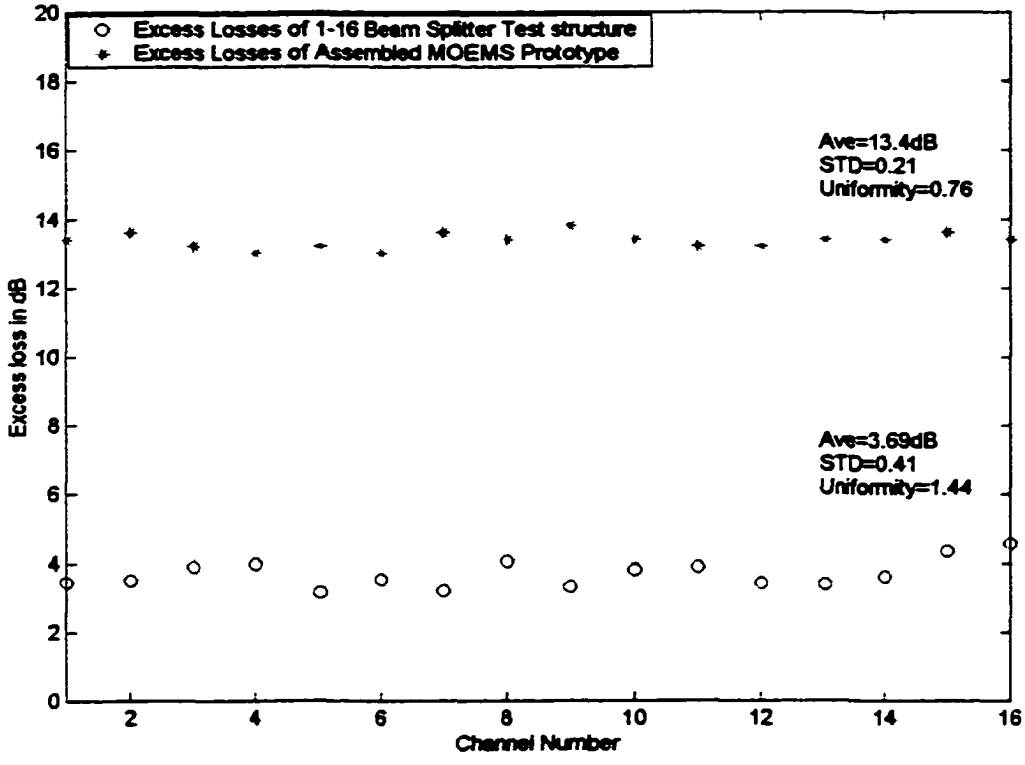


Figure 5-1. Excess Losses at Sixteen Fan-Out Nodes

* Plotted Using Table 3-3 and Table 4-7

Future Research

In MOEMS prototype, 54.74° micromachined silicon mirror array was used as a beam guiding device. To improve the OCDN signal output coupling efficiency, design and fabrication of 45° mirror array that has to have a etch depth of around 1250 μm is required.

In this dissertation, the passive optical elements were designed and fabricated. The optical applications of MEMS can also be extended to the fabrication of the movable structures such as microhinges and free-space microoptical benches, which include microlenses, micropositioners, microactuators, and actuated microstages. Therefore, the design and fabrication of systems that utilize the active components such as laser diodes, photodiodes and optical switches by the use of various micromachining technologies will be the focus of future work.

BIBLIOGRAPHY

[1] G. T. A. Kovacs and K. E. Petersen, "Bulk Micromachining of Silicon," *Proceedings of the IEEE*, Vol. 86, No. 8, pp. 1536-1551, 1998.

[2] K. E. Petersen, "Silicon as a mechanical material," *Proceedings of the IEEE*, Vol. 70, No. 5, pp. 420-457, 1982.

[3] K. E. Bean and P. S. Gleim, "The Influence of Crystal Orientation on Silicon Semiconductor Processing," *Proceedings of the IEEE*, Vol. 57, No. 9, pp. 1469-1476, 1969.

[4] S. Lee, S. Park, and D. Cho, "The Surface/Bulk Micromachining Process: Anew Method for Fabricating Released MEMS in Single Crystal Silicon," *Journal of Microelectromechanical Systems*, Vol. 8, No. 4, pp. 409-416, 1999.

[5] S. A. Campbell, and H. J. Lewerenz, "Semiconductor Micromachining," John Wiley & Sons, 1998.

[6] S. M. Sze, "Semiconductor Sensors," Wiley - Interscience, 1994.

[7] R. S. Muller and K. Y. Lau, "Surface-Micromachined Microoptical Elements and Systems," *Proceedings of IEEE*, Vol. 86, No. 8, pp. 1705-1998.

[8] W. Ehrfeld, P. Bley, F. Gotz, P. Hagmann, A. Maner, J. Mohr, H. O. Moser, D. Munchmeyer, W. Schelb, D. Schmidt, and E. W. Becker, "Fabrication of Microstructures Using The LIGA Process," *IEEE Micro Robots and Teleoperators Workshop*, pp. 623-633, 1987.

[9] M. Gerner, T. Paatzsch, L. Weber, H. Schift, I. Smaglinski, H-D. Bauer, M. Abraham, and W. Ehrfeld, "Micro-optical Components for Fiber and Integrated Optics realized by the LIGA Technique," *Proceedings of IEEE*, pp.328-333, 1995.

[10] K. Najafi, "Silicon Micromachining Technologies: Future Needs and Challenges," *SPIE*, Vol. 2879, pp. 206-215, 1996.

[11] K. Skrobis, J. Christenson, S. Staller, J. Freman, and P. Gadgil, "Material Structure and Process Required for The Manufacture of Micromechanical Devices," *SPIE*, Vol. 3223, pp. 230-236, 1997.

[12] H. Fujita, "Microactuators and Micromachines," *Proceedings of IEEE*, Vol. 86, No. 8, pp. 1721-1732, 1998.

[13] M. C. WU, "Micromachining for Optical and Optoelectronic Systems," *Proceedings of IEEE*, Vol. 85, No. 11, pp. 1833-1997, 1997.

[14] G. Trott, L. Yang, K. Carey, R. Ratowsky, J. S. Kallman, "Optical Application of Silicon Micromachining Technology," *SPIE*, Vol. 3223, pp. 120-129, 1997.

[15] W. Ehrfeld, H. Bauer, "Application of Micro-and Nanotechnologies for The Fabrication of Optical Devices," *SPIE* Vol. 3276, pp. 2-14, 1998.

[16] J. Clerc and P. Mottier, "MOEMS - A new European Competence Center: Core Competencies, Additional Technologies and Industrial Objectives," *SPIE* Vol. 3276, pp. 176-184, 1998.

[17] M. Elwenspoek and H. Jansen, "Silicon Micromachining," Cambridge University Press, 1998.

[18] H. Seidel, L. Cspregi, A. Heuberger, and H. Baumgartel, "Anisotropic Etching of Crystalline Silicon in Alkaline Solutions," *Journal of Electrochemical Society*, Vol. 137, No. 11, pp. 3612-3625, 1990.

[19] K. Ssato, M. Shikida, Y. Matsushima, T. Yamashiro, K. Asaumi, Y. Iriye, and Masaharu Yamamoto, "Characterization of Orientation-Dependent Etching Properties of Single-Crystal Silicon: Effects of KOH Concentration," *Sensors and Actuators*, A-64, pp. 87-93, 1998.

[20] C. R. Tellier, "Anisotropic Etching of Silicon Crystals in KOH Solution," *Journal of Materials Science*, Vol. 33, pp. 117-131, 1998.

[21] L. Cheng, M. Chen, C. Wan, T. Tasur, and Chenhsin, "Selective Etching of Silicon in Aqueous KOH," *Materials Science and Engineering*, B34, pp. 180-187, 1995.

[22] S. Koh, and C. Ahn, "Novel Integrated Optical I/O couplers on MCMs using MEMS Techniques," *SPIE*, Vol. 2686, pp. 121- 130, 1996.

[23] S. Koh, S. Suh, D. Wu, and D. J. Sadler, "High-speed low-loss and large-fanout optoelectronic clock distribution networks on multichip modules by using silica glass waveguides and silicon microstructures," *SPIE*, Vol. 3952, 2000.

[24] S. Koh, S. Suh, D. Wu, and M. Lantz, "Guided-wave optoelectronic clock-distribution networks on multichip modules using MEMS fabrication techniques," *SPIE* Vol. 3288, pp. 79-84, 1998.

[25] G. T. Valiath and K. W. Jelly, "Low skew chip-to-chip interconnects for high speed digital applications," *Journal of Miroelectronic Systems Integration*, Vol. 1, No. 1, pp. 79-84, 1993.

[26] N. Sherwani, Q. Yu, and S. Badida, "Introduction to Multichip Modules," John Wiley & Sons, 1995.

[27] M. Pecht, "Integrated Circuit, Hybrid, and Multichip Module Package Design Guidelines, " Wiley Interscience, 1994.

[28] J. T. Buttler, V. M. Bright, P. B. Chu, and R. J. Saia, "Adapting Multichip Module Foundries for MEMS Packaging," *Proceedings of International Conference and Exhibition on MCM and High Density Packaging–MCM*, pp. 106-111, 1998.

[29] P. Cinato, and K. C. Young, Jr, "Optical Interconnections within Multichip Modules," *Optical Engineering*, Vol. 32, No. 4, pp. 852-860, 1993.

[30] C. Tocci, and H. J. Caulfield, "Optical Interconnection," Artech House, 1994.

[31] P. R. Haugen, S. Rychnovsky, A. Husain, and L. D. Hutcheson, "Optical Interconnects for High Speed Computing," *Optical Engineering*, Vol. 25, No. 10, pp. 1076-1084, 1986.

[32] J. W. Goodman, S. Kung, and R. A. Athale, "Optical Interconnections for VLSI Systems," *Proceedings of the IEEE*, Vol. 72, No. 7, pp. 850-866, 1984.

[33] S. Koh, "Performance driven low skew clock distribution on multichip modules," PhD. Dissertation; University of Cincinnati (1994) 76 pages.

[34] M. Kobayashi, M. Yamada, Y. Yamada, A. Himendo, and H. Terui, "Guided-Wave Optical Chip-to-Chip Interconnections," *Electronics Letters*, Vol. 23, No. 4, pp. 143-144, 1987.

[35] L. Y. Lin, S. S. Lee, M. C. Wu, and K. S. J. Pister, "Micromachined Integrated Optics for Free-Space Interconnection," *Proceedings of the IEEE*, pp. 77-82, 1995.

[36] Y. Yamada, T. Miya, M. Kobayashi, S. Sumida, T. Miyashita, Tokai, and Ibaraki-ken, "Optical Interconnections using silica baase waveguide on Si Substrate," *SPIE*, Vol. 991, pp. 4-11, 1988.

[37] T. Miyashita, S. Sumida, and S. Sakaguchi, "Integrated Optical Devices on Silica Waveguide Technologies," *SPIE*, Vol. 993, pp. 288-294, 1988.

[38] L. M. Landsberger, S. Naseh, M. Kahrizi, and M. Paranjape, "On Hillocks Generated During Anisotropic Etching of Si in TMAH," *Journal of Microelectromechanical Systems*, Vol. 5, No. 2, pp. 106-136, 1996.

[39] O. Tabata, R. Asahi, H., Funabashi, K. Shimaoka and S. Sugiyama, "Anisotropic Etching of Silicon in TMAH Solutions," *Sensors and Actuators* A. 34, pp. 51-57, 1992.

[40] S. Tan, H. Han, R. Boudreau and M. L. Reed, "Process Induced Hillock Defects on Anisotropically Etched Silicon," *Proceedings of the IEEE*, pp. 229-234, 1994.

[41] K.E. Beans, "Anisotropic etching of silicon," *IEEE Trans. ElectronDevices*, Vol. ED-25, pp. 1185 - 1193, 1978.

[42] M. Elwenspo, U. Lindberg, H. Kok and L. Smith, "Wet Chemical Etching Mechanism of Silicon," *Proceedings of the IEEE*, pp. 223-228, 1994.

[43] M. M. Abu-Zeid, "Corner undercutting in anisotropically etched isolation contours," *Journal of Electrochemical Society*, pp. 2138-2142, 1984.

[44] X. P. Wu and W. Ko, "A study on compensation corner undercutting in anisotropic etching of (100) silicon," *The 4th International Conference on Solid-State Sensors and Actuators*, pp. 126 - 129, 1987.

[45] H. sandmaier, H.L. Offereins, K. Kuhl, and W. Lang, "Corner Compensation Techniques in Anisotropic Etching of (100) Silicon Using Aqueous KOH," *Proceedings of the IEEE*, pp. 456-459, 1991.

[46] D. R. Ciarlo, "Corner Compensation Structures for (110) Oriented Silicon," *Proceedings of the IEEE*, Micro Robots and Teleoperators Workshop, pp. 570-573, 1987.

[47] G. K. Mayer, H. L. Offereins, H. Sandmaier, and K. Kuhl, "Fabrication of Non-Underetched Convex Corners in Anisotropic Etching of (100)-Silicon in Aqueous KOH with Respect to Novel Micromechanic Elements," *Journal of Electrochemical Society*, Vol. 137, No. 12, pp. 3947-3951, 1990.

[48] C. A. Strandman, and L. Rosengren, "Fabrication of 45° mirrors together with well-defined v-grooves using wet anisotropic etching of silicon," *Journal of microelectromechanical systems*, Vol. 4, No. 4, pp. 213-219, 1995.

[49] C. Strandman, and L. Rosengren, "Fabrication of 45° optical mirrors on (100) Si using wet anisotropic etching," *Proceedings of the IEEE*, Microelectromechanical Systems Workshop, pp. 244-249, 1995.

[50] S. Koh, and D. Wu, "Prototyping of Optoelectronic Clock Distribution Networks on Multichip Modules by Using Silica Glass Waveguides and Silicon Microstructures," *SPIE*, Vol. 3632, pp. 115-122, 1999.

[51] S. Koh, D. J. Sadler, and C. H. Ahn, "Optoelectronic Multichip Modules for High Speed Computer Sysems and Communication Networks," *Optical Engineering*, 36, pp. 1319-1325, 1997.

[52] S. Koh, H. W. Carter, and J. T. Boyd, "Performance Comarison of Global Clock Distribution Networks on Multichip Modules Based on Electrical and Optical Interconnect Technologies," *SPIE*, Vol. 2400, pp. 259-266, 1995.

[53] S. Koh, H. W. Carter, and J. T. Boyd, "Synchronous Global Clock Distribution on Multichip Modules Using Optical Waveguides," *Optical Engineering*," Vol. 33, No. 5, pp. 1587-1595, 1994.

[54] T. Tamir, "Guided-Wave Optoelectronics," Spring-Verlag, 1990.

[55] R. Marz, "Integrated Optics: Design and Modeling," Artech, 1995.

[56] D. Marcuse, "Theory of Dielectrical Optical Waveguides," Academic Press, 1991.

[57] C. R. Pollock, "Fundamentals of Optoelectronics," Irwin, 1995.

[58] D. L. Lee, "Electromagnetic Principles of Integrated Optics," John Wiley & Sons, 1986.

[59] V. Subramaniam, G. N. De Brabander, D. H. Naghski, and J. T. Boyd, "Measurement of Mode Field Profiles and Bending and Transition Losses in Curved Optical Channel Waveguides," *Journal of Lightwave Technology*, Vol. 15, No. 6, 1997.

[60] H. Nishihara, M. Haruna, and T. Suhara, "Optical Integrated Circuits," McGraw-Hill, 1989.

[61] J. T. Boyd, "Photonic Integrated Circuits," Photonic devices and systems ed. R. G. Hunsperger, pp. 313-375, 1994.

[62] R. Syms, and J. Cozens, "Optical Guided Waves and Devices," McGraw-Hill, 1992.

[63] M. Kuznetsov, "Radiation Loss in Dielectric Waveguide Y-Branch Structures," *Journal of Lightwave Technology*, Vol. LT-3, No. 3, 1985.

[64] K. Liou, U. Koren, E. C. Burrow, M. Young, M. J. R. Martyak, M. Oron, and G. Raybon, "Y-Junction Power Divider in InGaAsP-InP Photonic Integrated Circuits," *Proceedings of The IEEE*, pp. 1376-1383, 1990.

[65] T. J. Gullen and C. D. W. Wilkinson, "Radiation Losses from Single-Mode Optical Y-Junctions Formed by Silver-Ion Exchange in Glass," *Optics Letters*, Vol. 10, No. 4, 1984.

[66] J. C. Palais, "Fiber Optic Communications," Prentice Hall, 1992.

[67] M. T. Kauffman, C. J. Radens, and J. T. Boyd, "Length Minization in Integrated Optical Circuits Incorporating Directional Couplers and Curved Sections," *Journal of Lightwave Technology*, Vol. 8, No. 10, pp. 1504-1508, 1990.

[68] B. A. Saleh, and M. Carl Teich, "Fundamentals of Photonics," Wiley Interscience, 1991.

[69] R. G. Hunsperger, "Integrated Optics: Theory and Technology," Springer-Verlag Berlin Heidelberg, 1982.

[70] S. L. Chuang, "Physics of Optoelectronic Devices," Wiley Interscience, 1995.

[71] S. K. Sheem and T. G. Giallorenzi, "Two-Dimensional Silicon Grooves for Altitudinal alignment in Fiber End-Butt Coupling," *Optics Letters*, Vol. 3, No. 3, 1978.

[72] J. Singh, "Optoelectronics," McGraw Hill, 1996.