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#### Realization of optical multimode TSV waveguides for Si-Interposer in 3D-chip-stacks

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#### ABSTRACT

Optical connectivity has the potential to outperform copper-based TSVs in terms of bandwidth at the cost of more complexity due to the required electro-optical and opto-electrical conversion. The continuously increasing demand for higher bandwidth pushes the breakeven point for a profitable operation to shorter distances. To integrate an optical communication network in a 3D-chip-stack optical through-silicon vertical VIAs (TSV) are required. While the necessary effort for the electrical/optical and vice versa conversion makes it hard to envision an on-chip optical interconnect, a chip-to-chip optical link appears practicable. In general, the interposer offers the potential advantage to realize electro-optical transceivers on affordable expense by specific, but not necessarily CMOS technology. We investigated the realization and characterization of optical interconnects as a polymer based waveguide in high aspect ratio (HAR) TSVs proved on waferlevel.

To guide the optical field inside a TSV as optical-waveguide or fiber, its core has to have a higher refractive index than the surrounding material. Comparing different material / technology options it turned out that thermal grown silicon dioxide (SiO<sub>2</sub>) is a perfect candidate for the cladding ( $n_{SiO_2} = 1.4525$  at 850 nm). In combination with SiO<sub>2</sub> as the adjacent polymer layer, the negative resist SU-8 is very well suited as waveguide material ( $n_{SU-8} = 1.56$ ) for the core. Here, we present the fabrication of an optical polymer based multimode waveguide in TSVs proved on waferlevel using SU-8 as core and SiO<sub>2</sub> as cladding. The process resulted in a defect-free filling of waveguide TSVs with SU-8 core and SiO<sub>2</sub> cladding up to aspect ratio (AR) 20:1 and losses less than 3 dB.

Keywords: optical interconnects; polymer optical waveguides, through-silicon VIAs,

#### **1. INTRODUCTION**

The continuously increasing demand for higher bandwidth and evolution towards to 5G makes the application of an optical chip-to-chip interconnect system conceivable. Based on the assumption of a 3D-chip-package an essential ingredient of such a system is the availability of a vertical interconnects. Through-silicon vias (TSVs) are the key technology for chip-stack intraconnects [1]. Copper-based solutions for electrical connections are the traditional approach [2]. Ultra-thin TSVs have been presented as well [3]. Usually, for electrical communication copper-filled through-silicon-vias (TSV) are used. A high bandwidth is the major performance indicator of the communication in a 3D-chip-stack.

Optical connections have the potential to outperform copper-based connections in terms of bandwidth at the cost of more complexity due to the required electro-optical and opto-electrical conversion. Once converted, the transmission distances in the optical domain are far less critical than in the electrical domain. The advantage of optical interconnects as optical waveguides or fibers is well established for long distance communication. The continuously increasing demand for higher bandwidth pushes the breakeven point for a profitable operation to shorter distances. Hence, first optical systems for chip-to-chip and chip-stack-to-chip-stack communication have been proposed [4]. Multiprocessor configurations are the driver for optical networks that connect chips [5], [6], [7]. While the required effort for the electrical/optical and vice versa conversions makes it hard to envision an on-chip optical interconnect, a chip-to-chip optical link appears practicable. Until this will have been realized, one has to consider a 3D-chip package based on silicon interposers. In

Micro-structured and Specialty Optical Fibres V, edited by Kyriacos Kalli, Jiri Kanka, Alexis Mendez, Pavel Peterka, Proc. of SPIE Vol. 10232, 102320T · © 2017 SPIE CCC code: 0277-786X/17/\$18 · doi: 10.1117/12.2265168 general, the interposer offers the potential advantage to realize electro-optical transceivers on affordable expense by specific, but not necessarily CMOS technology. To integrate an optical communication network in a 3D-chip-stack vertical optical TSV interconnect are required. Here, we present the fabrication of an optical polymer based waveguide in TSVs proved on waferlevel using SU-8 as core and  $SiO_2$  as cladding.

#### 2. OPTICAL INTERCONNECTS

To guide the optical field inside a TSV as optical-waveguide or fiber, its core has to have a higher refractive index than the surrounding material. Having a comparably high refractive index, silicon has to be shielded from the TSV filling using a lower refractive index material. Comparing different material / technology options it turned out that silicon dioxide (n = 1.46) is a perfect candidate for the cladding, because it can be manufactured as a very conformal layer by thermal oxidation, a well-known and controllable process. In combination with SiO<sub>2</sub> as the adjacent polymer layer, the negative resist SU-8 is very well suited as waveguide material (n = 1.56) for the core [8] (see Figure 1).



Figure 1. Schematic illustration of a Waveguide TSV.

In [9] we introduced three options of optical TSV: air-filled TSVs with silicon walls, air-filled TSVs with copper liner, and waveguide TSVs with SU-8 core and silicon dioxide cladding. The modeling and characterization of air-filled TSVs and polymer-filled optical TSVs was investigated in [10]. In [11], we presented results on the realization of optical interconnects and horizontal optical waveguides made by SU-8 as well using special imprint lithography technique on Si interposer. This TSV waveguide concept requires a SiO<sub>2</sub> surface as waveguide cladding and additionally a waveguide material with a higher refractive index in the core (e. g. SU-8). In this paper, we briefly report the realization and characterization of optical interconnects as a polymer based waveguide in high aspect ratio TSVs with SU-8 as core and 1.8 to 2  $\mu$ m SiO<sub>2</sub> layer as cladding and demonstrate a waferlevel proved polymer filling process for optical TSV (diameter 10 - 40  $\mu$ m) in 200 – 380  $\mu$ m thick Si interposer.

For producing an optical connection through a silicon wafer an optical waveguide must be created in high aspect ratio TSVs as shown in Figure 2. To realize it, the cylindrical TSVs were etched by an optimized deep reactive ion etching process (DRIE) through the substrate (a, b). Afterwards, a 2  $\mu$ m SiO<sub>2</sub> cladding is grown by thermal oxidation of Si (c). Next, the wafer-backside is covered with a temporary bonded PDMS-membrane (d). The SU-8 resist acting as waveguide-core material is deposited on the wafer frontside as a thin film by spin-coating (e). Homogeneous filling of TSVs is achieved by vacuum and temperature. A spin-off step reduces the SU-8 residual layer (f). Next, a maskless exposure from wafer backside of the SU-8 layer to UV light is performed in order to achieve a cross-linked SU-8 inside the TSV (g) followed by a resist development which dissolves the unexposed SU-8. After this, the backside membrane is removed. The following subchapters describe the process sequence in detail.



Figure 2. Process scheme for the realization of polymer based optical waveguides in high aspect ratio TSVs

#### 2.1 TSV etching

The TSVs were etched by deep reactive ion etching using a high-rate-etching tool (STS Pegasus). The optimized etching process with etching rates up to  $4 \mu m/min$  consists of a combination of passivation layer deposition and isotropic etching. Thus, we succeeded in generation of high aspect ratio TSVs (up to 30:1) with tapered profiles.

The integration scheme for the fabrication of the optical TSV (diameter: 20  $\mu$ m or 40  $\mu$ m) on 200  $\mu$ m or 380  $\mu$ m thin wafers enables the manufaction of through-hole vias without additional wafer thinning. Thus, no grinding, polishing, temporarily bonding or etch back processes have to be applied later as it is required in blind hole via integration schemes. Therefore, the TSV-hole etching process must be reliably stopped on a thin membrane as stop layer on the wafer backside. The etch-stop on the silicon wafer backside is realized by depositing a 50 nm aluminum layer via physical vapor deposition (PVD) and mechanical stability is provided by applying an additional photoresist layer (AZ4562) of 5  $\mu$ m thickness onto the aluminum layer. The etching process was optimized regarding the bottom of the holes to achieve a notching free shape. Inherent to the Bosch process are undercuts which arise at the top and the bottom of the holes. To remove them and to create tapered profiles at the mouth, an additional etching step is required to widen the holes at both sides.

After photoresist stripping and selective etching of aluminum, fluoropolymer residues remaining on the TSV walls were fully removed by dry plasma-enhanced process or wet chemical method (the latter used 1-methyl-pyrrolidone, NMP, at 55 °C). The developed optimal parameters of the subsequent smoothing process guaranteed a TSV sidewall surface roughness below 20 nm. The previous rough inner surface of the vias (<100 nm) was smoothed by a subsequent plasma-enhanced step using oxygen ( $O_2$ ), argon (Ar), and nitrogen trifluoride (NF<sub>3</sub>). Thus, cylindrical holes with high aspect ratios from 5:1 to 20:1 were successfully realized.



Figure 3. SEM-cross-section a) of etched TSV (40 µm diameter, 380 µm length; AR 10:1): b) etch-stop layer after DRIE, detailing minimal notching on 50 nm Al and 5 µm resist-stop layers.

#### 2.2 SiO<sub>2</sub> waveguide cladding

As cladding of the optical waveguide a 1.8 to 2  $\mu$ m thick SiO<sub>2</sub> layer with an optical refractive index of n = 1.4525 (wavelength  $\lambda_0 = 850$  nm) is required. Indeed, the production of high aspect ratio TSV requires a deposition process enabling the deposition of homogeneous layers on high aspect ratios. A simple method to achieve this is thermal oxidation, which is dependent on temperature and time. So, a 2  $\mu$ m thick SiO<sub>2</sub> waveguide cladding was performed in 8 h at 1.100 °C resulting in a conformal layer with satisfying uniformity over the wafer scale as shown in Figure 4.



Figure 4. SEM cross-section of an uniform  $SiO_2$  layer grown by thermal oxidation with a thickness of about 1.900 nm as cladding of the TSV waveguide; a) TSV side wall top (40  $\mu$ m diameter, 380  $\mu$ m TSV length); right: details of the 1.940 nm thermal SiO<sub>2</sub> layer

#### 2.3 Polymer filling of the core

To guide the optical field inside a TSV, the filling needs a higher refractive index than  $SiO_2$  cladding. The core of the optical waveguide was a polymer filling of SU-8. The latter is an epoxy-based negative UV resist with a refractive index n of about  $n_{SU-8}=1,56$ . Due to its unique properties, it is widely used as a structural material on several fields of MEMS. It is very well suited as waveguide material with excellent optical transparency beyond 400 nm, which makes it a preferred material for the fabrication of optical components and systems [8].

Here, for the suggested filling procedure a *MicroChem NANO*<sup>TM</sup> *SU-8* in formulation 50 was used. Its viscosity can specifically be reduced to formulations 25, 10, 5 by diluting with the solvent  $\gamma$ -butyrolactone (GBL).

To obtain maximum process reliability, substrates should be cleaned and dried before applying the SU-8 resist. The pretreatment of the TSV wafer started with solvent cleaning, clean water water rinse and  $N_2$  drying, followed by  $O_2$  plasma treatment. For the applied vacuum filling process of TSV blind holes are required. To obtain this, the TSV wafer backside was covered with a temporary bonded polydimethylsiloxane (PDMS) membrane. To dehydrate the surface, a bake at 200 °C for 5 minutes on a hotplate was applied.

A sufficient amount of SU-8 solution was deposited on the wafer front side as a thick film via spincoating as waveguide material. Homogeneous filling of the TSVs was achieved by applying 10 mbar in a vacuum oven.

A high solvent concentration of GBL in the SU-8 produced gaps, voids and bad adhesion on inner surface of the TSV during development (Figure 5a); its reduction during the following development of SU-8 could be achieved by vacuum pre-treatment, drying, and additional pre- and soft-bake on different levels of vacuum and temperature. After the resist had been applied by vacuum into TSV, it must be soft baked to evaporate the solvent and to condense the film under vacuum in an oven at 55 °C to 95 °C. This diminishes gaps, voids, blisters and shrinking of the material and improved the adhesion as well (Figure 5b). The filling process resulted in a defect-free filling of waveguide TSVs with SU-8-core and SiO2 cladding up to AR 20:1 (Figure 5c,d).



Figure 5. SEM cross-section of a SU-8 polymer filled TSV with a 1.900 nm SiO<sub>2</sub> cladding: a) gaps, voids and bad adhesion in SU-8 filling due to a not well adjusted process; b) details of a defect-free filling by vacuum pre-treatment, drying, additional pre- and soft-bake; c) defect-free filling of a 20  $\mu$ m TSV in bulk Si, 220  $\mu$ m length; d) defect-free filling of a 40  $\mu$ m TSV, 380  $\mu$ m length.

For the TSV filling process a large amount of SU-8 was needed, so, a thick SU-8 residual layer on top of the wafer remained. A subsequent spin-off step reduced this SU-8 residual layer on top of the wafer. To achieve this, the SU-8 residual layer was wetted with GBL. During an application time of 20 sec the GBL liquified the soft baked SU-8 and could be removed via spin coating. The thickness of the SU-8 residual layer as could be controlled by the rotation speed during the spin-off and application time of GBL. If required, the SU-8 residual layer thickness after the spin-off can be adjusted by an additional coating with a low viscosity SU-8 (formulation 10 or 5) to the desired value shown in Figure 6. After filling of TSV and adjustment of residual layer thickness, again a pre- and soft-bake (65 °C / 5 min and 95 °C / 20 min) was applied to evaporate the solvent and to establish the density of the film.



Figure 6. SEM cross-section of the adjustment of the SU-8 residual layer in top of the wafer thickness by a spin-off process: a) 30 μm SU-8 residual layer; b) 8 μm SU-8 residual layer; c) 2 μm SU-8 residual layer

#### 2.4 Exposure and development

In the following step, an exposure (contact mode with vacuum contact) of the SU-8 layer was conducted to cross-link the polymer. The optimal exposure dose depends on film thickness (thicker films require higher dosage) and other process parameters. In order to achieve a cross-linked SU-8 inside the TSV an exposure energy of 1.200 mJ/cm<sup>2</sup> to 1.500 mJ/cm<sup>2</sup> was applied (smaller TSV diameter require higher dosage). We performed an exposure from wafer backside through the temporary bonded PDMS membrane in order to achieve a cross-linked SU-8 inside the TSV since the TSV without residual layer. For pattern transfer into the SU-8 residue layer an exposure was performed from the wafer frontside.

Following this exposure, a post expose bake (PEB) had to be performed to selectively cross-link the exposed SU-8. This PEB was carried out either on a hotplate or in a convection oven. Optimum cross-link density was obtained through careful adjustments of the exposure and PEB process conditions to avoid highly stressed films. To minimize film stress and resist cracking, a 3 STEP contact hot plate process with slow heating and cooling ramp was used (50 °C / 3 min; 65 °C / 3 min; 95 °C / 15 min).

As a next step, unexposed SU-8 was developed in 6 minute application of *MicroChem SU-8 Developer*. In case of exposure from wafer backside, the SU-8 residual resist layer on the top surface was removed in the development step, it remained only in the cross-linked TSV. The SU-8 residues on top of the SU-8 are related to the residual thickness.

Following the development, the optical TSV wafer was rinsed with isopropyl alcohol and clean water. Finally, a removal of the temporary bonded PDMS-membrane uncovered the wafer backside. To improve the mechanical properties of the SU-8 an additional ramped hard baked at 200 °C for 15 min was applicated.

The process enabled a defect-free filling of waveguide TSVs with SU-8 core and SiO<sub>2</sub> cladding up to AR 10:1 or more. Figure 7 shows a cross section of a uniformly filled optical waveguide TSVs with 40  $\mu$ m in diameter and 380  $\mu$ m in length, a approximately 2  $\mu$ m thermally grown SiO<sub>2</sub> was used as cladding.



Figure 7. Uniformly filled optical waveguide TSV. a) SEM cross section of TSVs (40  $\mu$ m diameter, length 380  $\mu$ m) with 2  $\mu$ m thermally grown SiO<sub>2</sub>; b) microscopy cross section of waveguide TSVs (20  $\mu$ m diameter, length 380  $\mu$ m); c) details of the SU-8 core filling and the SiO<sub>2</sub> cladding; d) microscopic topview on optical waveguide TSV, with backside illumination, e) microscopic topview using differential interference contrast mode

#### 3. CHARACTERIZATION

In order to provide a simple characterization setup that can be realized on existing wafer probers, only one optical probe fiber shall be used. This reduces the workload during the test procedure and also the requirements on the required hardware.

The setup consists of a laser source (CW laser at 1550 nm for the measurements carried out in this paper), an optical circulator to distinguish between the ongoing and back-reflected optical signals, an optical probe (SMF as probe fiber connecting directly to the fiber-coupled equipment) and an optical power meter. A reflector has been placed underneath the TSVs wafer under test. The aim of this characterization experiment is to measure and investigate the power loss due to round trip inside the TSV. Therefore, the reflectivity has to be known. First, the setup has been calibrated by connecting it without optical probe and TSV structure under test to a fiber-coupled mirror as can be seen in Figure 8. For 2.82 dBm optical power of a laser source, the measured power losses in paths  $(1 \rightarrow 2)$ , and  $(2 \rightarrow 3)$  from the optical circulator are 0.78 dB and 1.22 dB, respectively.



Figure 8. Schematic illustration of the calibration setup.

When replacing the mirror with optical probe and the wafer including TSV under test stacked from backside with reflector as shown in Figure 9, the influence of the circulator, laser and power meter is canceled by the first calibration. Probing without TSV wafer directly on the reflector plane gives a hint on the quality of this reflector.

Two different set of optical TSVs, based on the pitch size (100  $\mu$ m, 200  $\mu$ m) as illustrated in Figure 10, are measured, the measured attenuation range is between (0.8-3) dB. The deviations are not only caused by the manufacturing process of the TSVs but also by variations in the reflector plane. The realized setup used in this paper outperforms a previous one with two fibers aligned in a vertical configuration [9] in terms of simplicity and stability. The measurement results matched the values predicted by the models very well.



Figure 9. Schematic illustration of the TSV characterization setup



Figure 10. Microscopy cross section (backside illumination) of optical TSV with different pitch: a) 200 µm; b) 100 µm



Figure 11. TSV characterization setup

#### **4. CONCLUSION**

This paper presents a promising fabrication technologies and the successful realization of multimode waveguides for integrated optical interconnect system on a silicon interposer. We present the fabrication of an optical polymer based waveguide in TSVs proved on waferlevel using SU-8 as core and SiO2 as cladding. Individual TSV process and filling parameter setups were identified for different diameters and aspect ratios and for producing either optical TSV waveguide. The process resulted in a defect-free filling of waveguide TSVs with SU-8 core and SiO<sub>2</sub> cladding up to AR 20:1. The measurement results matched the values predicted by the models very well. SU-8-filled waveguide TSVs have the potential for low losses measured in the range between (0.8-3) dB.

#### 5. ACKNOWLEDGMENT

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