A 30 Gb/s High-Swing, Open-Collector Modulator Driver in 250 nm SiGe BiCMOS

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***Abstract*—This paper presents a modulator driver realized as a breakdown voltage doubler which can provide a high output swing of 7.6 $V_{pp,diff}$ for load impedances as low as 30 Ω, thus overcoming the limitation imposed by the collector-emitter breakdown voltage. The open-collector design gives an important degree of freedom regarding the modulator load to be driven, while significantly reducing the circuit's power consumption. The driver is capable of running at 30 Gb/s while dissipating 1 W of DC power. Thanks to the inductorless design, the active area occupied by the circuit is only 0.28 mm × 0.23 mm. The driver was realized in a 250 nm SiGe BiCMOS technology.**

I. Introduction

With the rapid growth of intra and inter data center networks, high speed and low loss transport of data becomes a critical requirement for modern transceivers. Optical communications proved to be a reliable technology to satisfy these demands, as optical fibers are superior to the conventional copper-made cables or to wireless channels in terms of bandwidth and loss [1].

A common way to realize the electro-optical interface is to modulate the signal onto a continuous-wave light source provided by a laser. To this end, voltage-dependent modulators are used. Mach-Zehnder modulators (MZM) are one of the most reliable modulator types employed due to their high speed, wide optical spectrum and low thermal sensitivity [2].

The principle of operation for a basic, one-arm driven MZM is explained based on Fig. 1. The input light wave is split at point A on two arms of equal length. If no modulation is applied, the two light waves will combine constructively at point B resulting in a logical "1". However, if on one of the arms a 180° phase shift is applied, the light waves will combine destructively resulting in a logical "0". The phase shift is obtained by means of a voltage controlled pn-junction, called phase shifter. For a push-pull operation, which is the standard today, phase shifters on both arms are driven

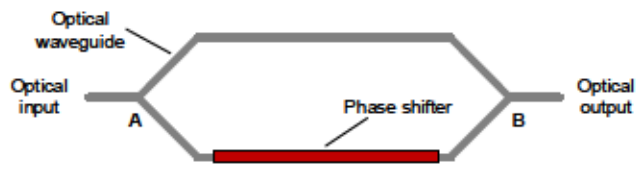

Fig. 1. Basic, one-arm driven MZM.

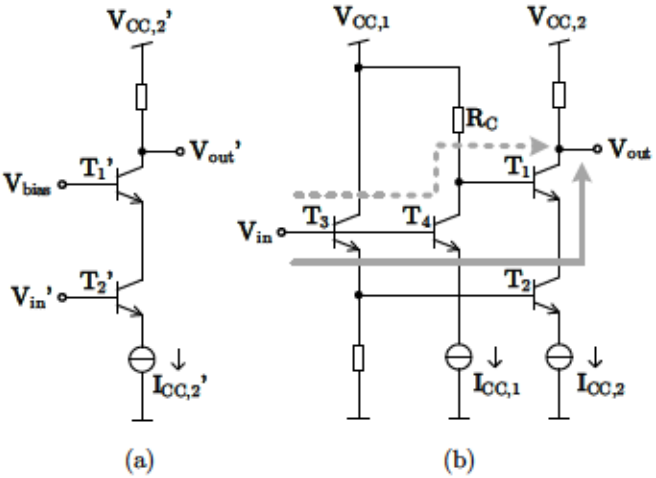

Fig. 2. (a) Simple cascode; (b) BV-doubler [3].

differentially, thus halving the required voltage to achieve a 180° phase shift.

The modulation efficiency of an MZM is given by the product $V_\pi \times L$ [4], where V_π is the necessary voltage swing to reach a 180° phase shift and L is the length of the phase shifter. In order to have a short phase shifter length and therefore a low capacitive loading of the driver, a large V_π is required. This poses however a challenge to the driver design because the maximum achievable voltage swing is limited by the collector-emitter breakdown voltage (BV_{CE}) of the output differential pair.

In this paper, a modulator driver featuring a breakdown voltage doubler topology (BV-doubler) is presented that allows to overcome the breakdown voltage limitation imposed by the technology. The particularity of the circuit is represented by its open-collector design, making it highly adaptable with regard to the load impedance that is to be driven. Depending on the application, the proposed circuit is able to drive both short length and high speed or long length and high extinction ratio modulators for short and long distance communications, respectively. Moreover, not having a load in the output stage saves a considerable amount of DC power, as it will be shown in the comparison with the state of the art at the end of this paper.

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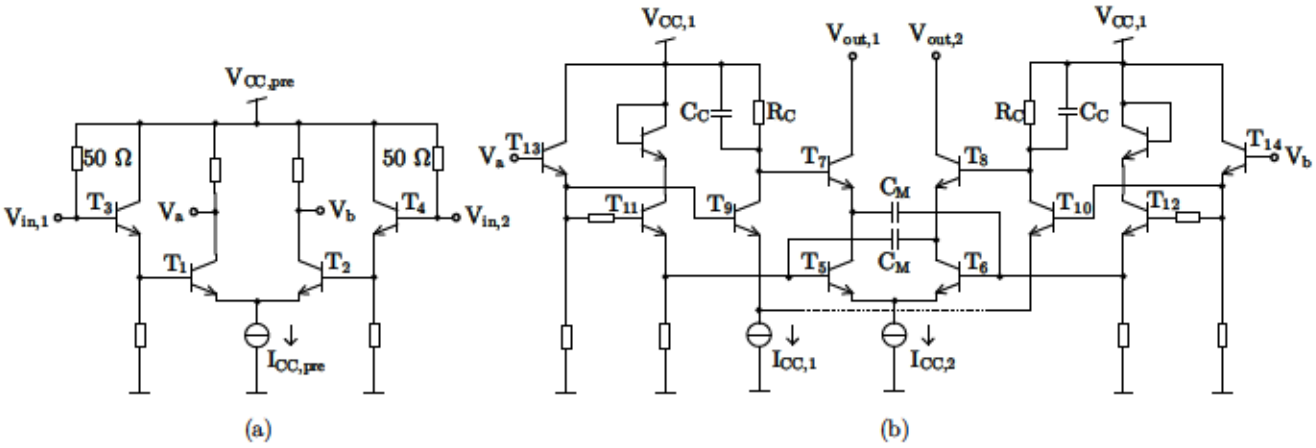

Fig. 3. (a) Preamplifier; (b) Output stage.

II. Circuit Concept

In order to double the maximum achievable voltage swing of a modulator driver, one needs to cascade two transistors in the output differential pair. However, a simple cascode topology, as shown in Fig. 2(a), would not be adequate for this purpose. As the bias voltage of transistor T_1' is constant, its base potential and therefore its emitter potential remain nearly constant during the entire operation of the circuit, which means that the whole voltage swing falls over the upper transistor T_1' [3]. It is thus necessary that the base of T_1' varies synchronously with the output of the circuit. This can be realized by using a common-emitter stage to drive the base of T_1 as shown in Fig. 2(b) [3]. In this way, transistors T_3 and T_4 and thus T_1 and T_2 are turned on and off simultaneously. By carefully dimensioning the resistor R_C, the supply voltage $V_{CC,1}$ and the tail current $I_{CC,1}$, an equal distribution of the output voltage swing over the transistors T_1 and T_2 can be achieved.

For the current design, considering both the minimum value of the collector-emitter voltage below which the transistor enters the saturation region as well as the upper boundary imposed by the breakdown voltage [5], a swing of 1.9 V per transistor (from 0.6 V to 2.5 V) has been chosen. This leads, for the two cascaded transistors, to a total of 3.8 V single-ended output swing, or 7.6 V when considered differentially.

III. Circuit Design

The modulator driver presented in this paper consists of two stages, namely a preamplifier and an output stage. The preamplifier, which is depicted in Fig. 3(a), operates under switching condition, thus behaving like a limiting amplifier. In this way, the sensitivity of the driver's output to input variations and distortions is considerably diminished.

The output stage, shown in Fig. 3(b), was designed to get the highest possible voltage swing while not exceeding the breakdown limitations. As it was discussed in the previous section, it consists of a modified cascode circuit that enables the swing to be equally distributed over the two output transistors $T_{5/6}$ and $T_{7/8}$. Designed as an open collector, the load is solely the impedance of the modulator itself that the circuit is supposed to drive. During measurements, the 50 Ω impedance of the sampling oscilloscope served as a load. In order to reach the desired swing regardless of the connected load, the tail current $I_{CC,2}$ was made tunable.

As it can be noticed in Fig. 2(b), there are two different paths from the circuit's input to its output, one that goes through the transistors T_2 and T_1 (solid line) and another one that goes through T_4 and T_1 (dashed line). Because the signal propagation velocity through the former path is slower than through the latter [3], it is necessary to equalize the delays in the two paths in order to avoid distortions in the output signal. Referring to Fig. 3(b), this is done by employing a capacitor C_C at the collector of $T_{9/10}$ in order to slow down the signal through this transistor and thus match the speed in the two aforementioned paths.

Even though the Miller effect is reduced due to the cascode topology, compensation capacitors C_M are still needed to cancel the effects of the collector-base parasitic capacitances of transistors T_5 and T_6 and hence improve the bandwidth. Also, resistors were added at the bases of T_{11} and T_{12} in order to increase the stability of the circuit.

IV. Measurement Results

The circuit was fabricated in a 250 nm SiGe BiCMOS electronic-photonic integrated technology. The transit frequency of the NPN transistors used in this design is 190 GHz. The technology incorporates a module for optical components, enabling the realization of fully-integrated electro-optical systems. Such co-designs offer important advantages in terms of production costs, compactness and low-loss connections between the electrical and optical modules.

The chip micrograph is shown in Fig. 4. The chip size is 0.8 mm × 0.8 mm, whereas the driver's active area (excluding the pads) is only 0.28 mm × 0.23 mm, thanks to its inductorless design. The chip has two RF input pads, two RF output pads, DC pads both for the supply voltages, namely

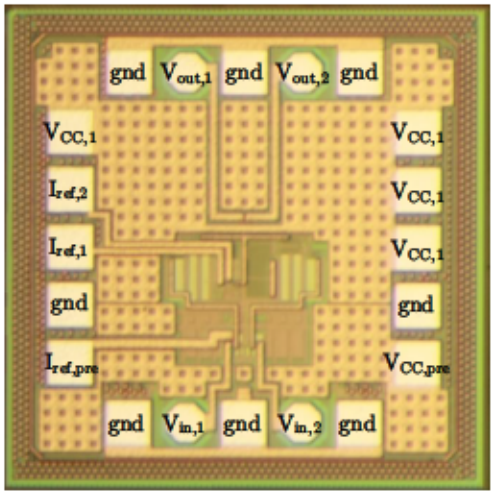

Fig. 4. Chip Micrograph. Size is 0.8 mm × 0.8 mm.

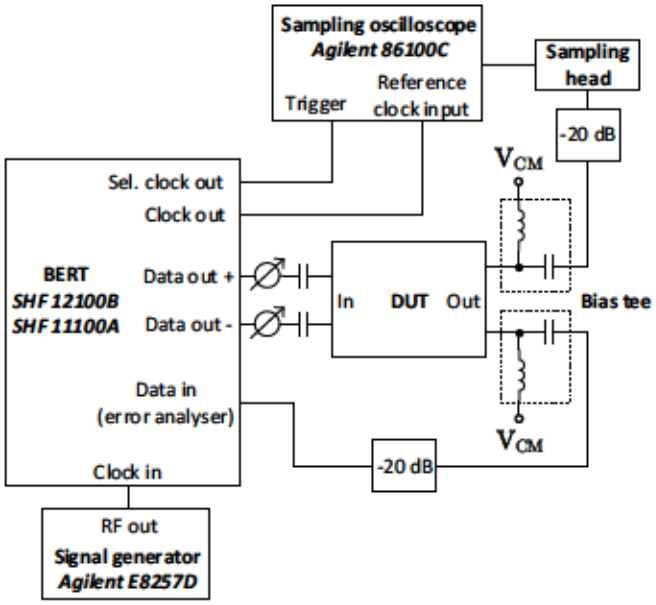

Fig. 5. Measurement setup.

$V_{CC,pre}$ and $V_{CC,1}$ (4 V and 4.5 V, respectively) and for the reference currents of the three current mirrors that provide $I_{CC,pre}$, $I_{CC,1}$ and $I_{CC,2}$, as well as several ground pads. By tuning the reference currents, additional corrections can be made in order to counterbalance process variations or other error sources and attain the desired output swing.

The setup for the large-signal measurement is depicted in Fig. 5. The input signal was a $2^7 - 1$ long pseudo random bit sequence (PRBS) with a 330 mV amplitude generated by a bit error rate tester (BERT). Phase shifters were used in order to align the phases of the two input signals. One output of the circuit was fed into a sampling oscilloscope to measure the eye diagram, while the other output was fed back into

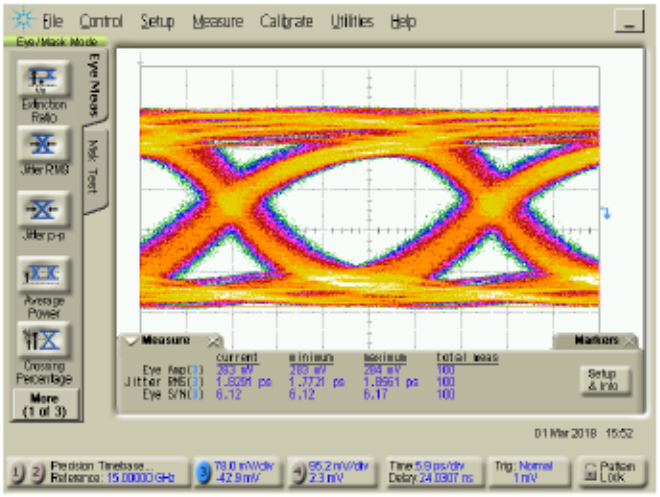

Fig. 6. Single-ended output eye diagram at 30 Gb/s. Horizontal scale is 5.9 ps/div and the equivalent vertical scale considering the 20 dB attenuator is 0.78 V/div.

the BERT to measure the bit error rate (BER). The BERT and the driver's output were connected using a 0.8 m RF cable. The measurement equipment including probes, cables and connectors was not de-embedded and thus impacted the measurement results.

As the circuit is an open collector, the 50 Ω impedances of the oscilloscope and the BERT were acting as a load during the measurements. In order to achieve the desired 7.6 V differential swing, a tail current $I_{CC,2}$ of 76 mA was needed, attained by tuning the corresponding reference current. The common mode voltage V_{CM} = 4.5 V of the output signal was provided by means of a bias tee. Additional 20 dB attenuators at both circuit outputs were used to protect the measurement devices from the high voltage swing.

The single-ended output eye diagram measured at 30 Gb/s is shown in Fig. 6. The maximum achievable output voltage swing is the targeted value of 7.6 $V_{pp,diff}$, while the vertical

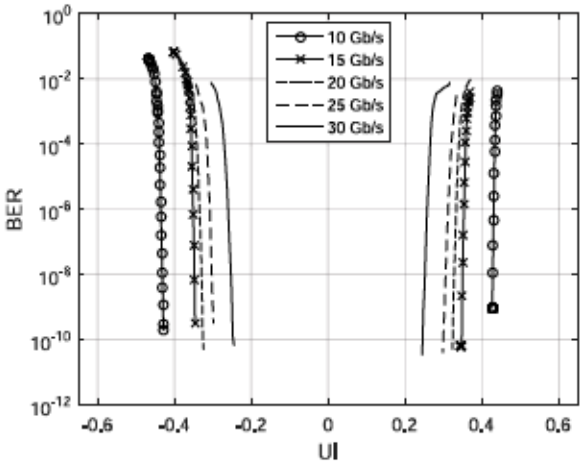

Fig. 7. BER for different data rates measured with a $2^7 - 1$ PRBS.

eye opening at the specified data rate is 4 $V_{pp,diff}$. The RMS jitter amounts to 1.8 ps and the eye signal-to-noise ratio is 6.1. The total DC power consumption of the circuit is 1 W.

The measurement results of the BER are displayed in Fig. 7 for data rates from 10 Gb/s up to 30 Gb/s. The input signal settings were the same as for the eye diagram measurement.

TABLE I
PERFORMANCE SUMMARY OF SILICON HIGH SWING MODULATOR DRIVERS

	Speed (Gb/s)	Output Swing, Diff. (V)	DC Power (W)	Technology
[3]	10	8	3.7	180 nm SiGe BiCMOS
[6]	23	7	2.5	SiGe Bipolar
[7]	25	6.4	0.52	65 nm CMOS
[5]	40	6	1.35	250 nm SiGe BiCMOS
[8]	40	7.2	3.6	180 nm SiGe BiCMOS
[9]	50	5.4	1.7	55 nm SiGe BiCMOS
This Work	30	7.6	1	250 nm SiGe BiCMOS

V. CONCLUSION

In this paper we have presented a modulator driver featuring a breakdown voltage doubler topology capable of providing a maximum output voltage swing of 7.6 $V_{pp,diff}$. Such a high swing allows a shorter phase shifter length, thus reducing the capacitive loading of the driver and increasing the overall bandwidth of the electro-optical transmitter. The open-collector topology offers a high degree of flexibility in the design of the MZM while significantly decreasing the amount of power dissipated. The proposed circuit can run at a data rate of 30 Gb/s while consuming 1 W of DC power.

Compared to the first breakdown voltage doubler topology reported in [3], the driver presented in this paper reaches a three times higher data rate while dissipating 73 % less DC power. Furthermore, the absence of a load in the output stage saves 26 % DC power in comparison with the driver in [5], realized in a similar technology.

To the best of the authors' knowledge, the proposed circuit is the first implementation of a breakdown voltage doubler as an open-collector topology, offering the lowest power consumption among high-swing drivers at data rates above 25 Gb/s.

ACKNOWLEDGMENT

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