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Integrated Distributed Amplifiers for Ultra-Wideband BiCMOS Receivers Operating at Millimeter-Wave Frequencies

Paolo Valerio Testa

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Vorsitzender: Jun.-Prof. Dr.-Ing. KAMBIZ JAMSHIDI
Gutachter: Prof. Dr. sc. techn. habil. Dipl. Betriebswiss. FRANK ELLINGER
Prof. Dr.-Ing. MATTHIAS RUDOLPH

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Zusammenfassung

Die beiden Hauptanwendungsgebiete der Millimeterwellentechnik sind die Telekommunikation und die Bildgebung. Für beide Anwendungen muss die Bandbreite bestehender Systeme erhöht werden, um größere Datenraten und feinere Bildauflösungen zu erreichen. In dieser Arbeit wurden monolithisch integrierte Millimeterwellenschaltungen mit sehr hoher Bandbreite entwickelt. Der Fokus der Untersuchungen lag auf Verstärkern, sowie der Integration dieser Verstärker mit Antennen auf einem Chip. Ein kommerziell erhältlicher 130 nm Silizium-Germanium (SiGe) Bipolar-Complementary-Metal-Oxide-Semiconductor Prozess wurde eingesetzt, um die Prototypen der Schaltkreise herzustellen und zu validieren. Im Bereich der verteilten und konjugiert-komplex angepassten Verstärker, sowie für Verstärkersysteme mit kointegrierten Antennen, wurde der Stand der Technik u.a. in folgenden Bereichen verbessert:

- Eine neuartige Kaskoden-Verstärkerzelle mit drei Transistoren wurde entwickelt. Durch eine Transkonduktanz-Erhöhung bei hohen Frequenzen konnten die Verluste der synthetischen Leitung auch bei höheren Frequenzen kompensiert werden. Dieses Verhalten wurde analytisch hergeleitet und erklärt. Die Messungen der realisierten Schaltung bestätigen, dass ein Traveling-Wave Amplifier (TWA) mit dieser Technik 10 dB Verstärkung in einem 170 GHz breiten Frequenzband erzielt.

- Zwei Cascaded Single-Stage Distributed Amplifier (CSSDA) wurden aufgebaut. Der erste Verstärker, welcher für einen geringen Leistungsverbrauch optimiert wurde, benötigt weniger als 20 mW DC-Leistung, um eine Verstärkung von 10 dB in einem 130 GHz breiten Frequenzband zu erreichen. Der zweite Verstärker wurde für den Hochfrequenzbetrieb optimiert und arbeitet bei bis zu 250 GHz. Diese Operationsfrequenz stellt für verteilte Verstärker in SiGe-Technologie einen Rekord dar.

- Die erste vollständige CSSDA-Schaltungsanalyse wurde als Funktion aller Schlüsselparameter vorgestellt. Die typische Verschlechterung der CSSDA-Ausgangsanpassung in Richtung hoher Frequenzen wurde analytisch quantifiziert. Eine symmetrische Architektur wurde verwendet, um die Vorteile des CSSDA im Frequenzgang beizubehalten und dennoch den Verstärker über das gesamte erwünschte Frequenzband anzupassen. Diese Erkenntnisse wurden experimentell verifiziert.

- Die ersten Traveling-Wave-Leistungskombinierer und -teiler wurden entworfen, die für den Betrieb im Frequenzbereich von wenigen MHz bis zu 200 GHz geeignet sind. Die Schaltungen verbessern den Stand der Technik hinsichtlich der maximalen Betriebsfrequenz und der Bandbreite um den Faktor fünf.

- Es wurde ein resonant-angepasster symmetrischer Verstärker mit einer Mittenfrequenz von 185 GHz, einer –3 dB-Bandbreite von 55 GHz und einer Verstärkung von 10 dB realisiert. Die Leistungsaufnahme des Verstärkers beträgt nur 16,8 mW, was eines der besten Ergebnisse in dieser Schaltungsklasse ist. Dieser Verstärker hat das breiteste Frequenzband unter den bisher veröffentlichten resonant-angepassten Verstärkern in SiGe Technologie.

- Die erste Stufe eines ultrabreitbandigen Empfängers für Sub-THz Anwendungen wurde entwickelt. In dem System wurden eine Vivaldi-Antenne und ein CSSDA integriert. Die beschriebenen Entwurfstechniken und die Systemanalyse ermöglichen eine Maximierung der Bandbreite und verbessern den Stand der Technik hinsichtlich dieser Eigenschaft um den Faktor zwei.

Abstract

Millimetre-wave technology is used for applications such as telecommunications and imaging. For both applications, the bandwidth of existing systems has to be increased to support higher data rates and finer imaging resolutions. Millimetre-wave circuits with very large bandwidths are developed in this thesis. The focus is put on amplifiers and the on-chip integration of the amplifiers with antennas. Circuit prototypes, fabricated in a commercially available 130 nm Silicon-Germanium (SiGe) Bipolar Complementary Metal-Oxide-Semiconductor (BiCMOS) process, validated the developed techniques. Cutting-edge performances have been achieved in the field of distributed and resonant-matched amplifiers, as well as in that of the antenna-amplifier co-integration. Examples are as follows:

- A novel cascode gain-cell with three transistors was conceived. By means of transconductance peaking towards high frequencies, the losses of the synthetic line can be compensated up to higher frequencies. The properties were analytically derived and explained. Experimental demonstration validated the technique by a Traveling-Wave Amplifier (TWA) able to produce 10 dB of gain over a frequency band of 170 GHz.

- Two Cascaded Single-Stage Distributed Amplifiers (CSSDAs) have been demonstrated. The first CSSDA, optimized for low power consumption, requires less than 20 mW to provide 10 dB of gain over a frequency band of 130 GHz. The second amplifier was designed for high-frequency operation and works up to 250 GHz leading to a record bandwidth for distributed amplifiers in SiGe technology.

- The first complete CSSDA circuit analysis as function of all key parameters was presented. The typical degradation of the CSSDA output matching towards high frequencies was analytically quantified. A balanced architecture was then introduced to retain the frequency-response advantages of CSSDAs and yet ensure matching over the frequency band of interested. A circuit prototype validated experimentally the technique.

- The first traveling-wave power combiner and divider capable of operation from the MHz range up to 200 GHz were demonstrated. The circuits improved the state of the art of the maximum frequency of operation and the bandwidth by a factor of five.

- A resonant-matched balanced amplifier was demonstrated with a centre frequency of 185 GHz, 10 dB of gain and a 55 GHz wide –3 dB-bandwidth. The power consumption of the amplifier is 16.8 mW, one of the lowest for this circuit class, while the bandwidth is the broadest reported in literature for resonant-matched amplifiers in SiGe technology.

- The first stage of a receiver for Ultra-Wide-Band (UWB) sub-THz applications was developed integrating a Vivaldi antenna with a CSSDA. Design techniques and system analysis ensured the maximization of the bandwidth and improved the corresponding state of the art by a factor of two.

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1 Introduction

1.1 Motivation

Science and technology improved through the centuries our way of communication, leading at the time of writing to compact and portable systems able to code messages into electromagnetic signals.

Mobile phones are the best example of such devices. The ever-increasing request for data transmission pushed the capability of cellular networks over the years. The first commercial cellular network (first generation – 1G), launched in 1979 in Tokyo, was based on analog standards and capable of a two Kilobits-per-second (Kbps) data rate [1]. In the early nineties, the 2$^{\mathrm{nd}}$ generation of mobile network – 2G – introduced digital-based coding increasing the communication capability up to 14.4 Kbps [1]. Since then, a new standard appeared roughly every ten years culminating in the actual fourth generation 4G. This standard can support a maximum data rate of one gigabit per second (Gbps), and it operates at frequencies up to 6 GHz. An example of fourth generation technology is the LTE advanced, which is capable of 100 Mbps data rate. Fig. 1.1 shows the evolution of telecommunications standards in the past years. Mobile devices capable of huge data-rates had an impact on our daily life comparable to only a few other technologies. This lead in just three decades to move from zero to more than seven billion devices in use worldwide, turning them into the fastest growing human-made phenomenon ever [2]. In prevision of an increased sharing of data, communications in the order of multi-gigabits-per-second have to be established. The next standard 5G, planned to operate from 2020, is expected to fulfill such expectations. The main difference between the new standard and the previous generations will be the use of signals in the millimeter-wave band, which covers the frequency range from 30 GHz to 300 GHz. The key advantage of millimeter-wave (mm-wave) signals is the availability of broad frequency-bands, which can be used to establish communications with high data rate. An example of the capability of millimeter-wave communications can be found in [3], which demonstrates data rates up to 65 Gbps over a distance of 1 m, and in [4] where a 120 Gbps transceiver is realized exploiting two carriers located at 70 GHz and 105 GHz. Although mm-wave systems are promising, they are indeed more challenging to be designed than with their counterparts operating at lower frequencies. One critical point in mm-wave designs is the interconnection between front-ends and antennas. This issue is partly compensated by the fact that at mm-wave frequencies the dimensions of antennas reduce enough to allow their integration with the transceiver hardware, improving, in turn, the quality of the interconnection. Several front-ends integrated with antennas demonstrated operating frequencies up to 350 GHz [3, 6–8]. The main drawback of the state of the art is the relatively narrow frequency-band of operation. For example, in [8] a bandwidth of 24 GHz is demonstrated for a center frequency of 220 GHz. This bandwidth limitation arises from the use of narrow-band amplifiers and antennas. Instead, the mm-wave band offers still unexploited hundred-GHz wide frequency bands, which can enable communications with data rates of hundreds of Gbps. As stated in fact by the Hartley-Shannon theorem, one fundamental approach to increase the data rate of communication consists in enlarging the bandwidth of the radio channel in use. In addition, these efforts align well with the adjacent area of imaging, sensing applications, and positioning, which share similar requirements. In detail, an Ultra-WideBand (UWB) is necessary to achieve imaging or positioning applications with a fine resolution.

All these considerations motivate the interest in millimeter-wave UWB communications, which ultimately lead to this Ph.D. research project. The development of UWB mm-wave transceivers directly translates into the need of UWB amplifiers. In fact, the amplifier is the basic block of front-ends as it can be modified to obtain mixers, oscillators, and other components. This thesis then aims to increase the bandwidth of operation of UWB mm-wave receivers with the use of Distributed Amplifiers (DAs), and it investigates as well on the co-integration of on-chip antennas and amplifiers. A state of the art 130 nm Silicon-Germanium (SiGe) Bipolar Complementary Metal-Oxide-Semiconductor (BiCMOS) process has been used for the experimental verification of the presented research.

1.2 Scope of the Project

This Ph.D. research project has been performed in the frame of the Deutschen Forschungsgemeinschaft (DFG) priority-program named Wireless Ultra high-speed Communication for Mobile Internet Access – SPP-1655 – which targets the development of wireless systems with data rates above 100 Gbps. At state of the art, such high data rates are obtained mostly with guided optical systems such as fiber optics, and they are employed in data centers and high-performance computing facilities. The accomplishment of the SPP-1655 goals requires a multidisciplinary approach embracing system architectures, coding algorithms, and

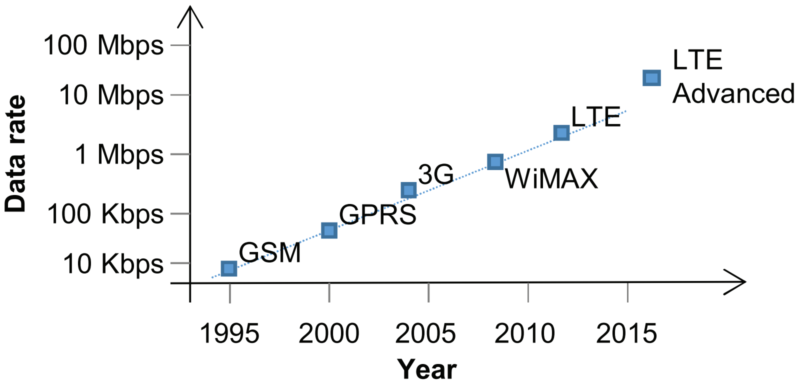


Figure 1.1: Data-rate increase over the years of telecommunications standard [5].

technological methods. The SPP-1655 program is formed by different projects to perform research with close interaction between semiconductor technology, radio-frequency engineering, and information theory, such as:

- DAAB – On-chip integrated distributed amplifier and antenna systems in locally-backside-etched SiGe BiCMOS for receivers with ultra-large bandwidth – Technische Universität Dresden;
- LP100 – Optimization of 100 Gbps near field wireless transmitters under consideration of power limits – RWTH Aachen University and University of Kaiserslautern;
- SPARS – Development of novel system and component architectures for future innovative 100 Gbps communication systems – University of Stuttgart, Technische Universität Dresden, and Friedrich-Alexander-Universität Erlangen Nürnberg;
- W-Band CMOS-PA – W-band high efficiency power amplifier in CMOS-technology – Berlin Institute of Technology;
- Tera50 – A 10-1000 GHz wireless measurement system with 50 GHz bandwidth – University of Duisburg-Essen;
- maximumMIMO – Maximum spectral efficiency by parallel multiple-input-multiple-output transfer using high-density 3D-antenna-topology – Technische Universität Dresden, Humboldt Universität zu Berlin, and Universität der Bundeswehr München;
- M4 – Ultra-wideband communications based on massive MIMO and multimode antennas suitable for mobile hand-held devices – Kiel University;
- PolyData – Integrated active antenna arrays with polarization multiplexing for broadband communications at W-band – Hamburg University of Technology;
- Real100G.COM – Mixed-mode baseband for 100 Gbps wireless communication – University of Stuttgart, Brandenburg University of Technology Cottbus Senftenberg, and Universität Paderborn;
- Real100G.RF – Fully integrated radio-front-end for wireless 100 Gbps communication – Bergische Universität Wuppertal and Karlsruhe Institute of Technology;
- End2End100 – MAC and PHY protocols to support 100 Gbps communications – Brandenburg University of Technology Cottbus Senftenberg.

This thesis mainly presents the results of the project "On-chip integrated Distributed Amplifier and Antenna systems in locally-backside-etched SiGe BiCMOS for receivers with ultra-large Bandwidth" – DAAB. In detail, the DAAB project investigates novel distributed amplifier and antenna concepts to massively improve the relative bandwidth of wireless receivers operating at frequencies above 100 GHz and up to 250 GHz. The project aims to achieve relative bandwidths up to 50%, corresponding to an improvement by at least a factor of 2 compared to the state-of-art. This will pave the way to communications with data rates beyond 100 Gbps. Furthermore, the integration of antennas and amplifiers into the same semiconductor die aims to minimize the interconnection parasitics. The fastest commercially available BiCMOS technology, with a maximum frequency of oscillation (f_{max}) of 450 GHz has been employed for experimental validation. The Chair for Circuit Design and Network Theory and the Chair for Radio Frequency and Photonics Engineering, both from the Technische Universität Dresden, led the project. Profound interdisciplinary competencies have been applied, involving – among the others – knowledge in the high-frequency domain and integrated circuits.

1.3 Objective and Structure

This thesis presents the research results in the field of distributed amplification techniques for UWB mm-wave circuits, and it discusses the integration on a single chip of UWB antennas and amplifiers for receiver hardware. In particular, the research goal is the maximization of the frequency band of operation of these systems. The frequency band of interest spans from 1 GHz to 250 GHz, while the crucial points of the research are in the field of:

- Circuit analysis, such as the investigation of novel approaches for signal amplification in the frequency band of interests. Different distributed architectures have been investigated pursuing to improve the maximum working frequencies and the bandwidths of amplification;
- Circuit design, for mm-wave and UWB purposes. Topics such as the estimation and the modeling of parasitics, which limit the operation at high frequency, received the primary focus;
- System analysis and design of antenna-amplifier receiver systems. Novel techniques have been used to evaluate the response of co-integrated antenna-amplifier systems.
- Experimental validation of the proposed design solutions and approaches.

The focus of the thesis is on the amplifier design, while the antennas are discussed only where necessary for the overall understanding. This thesis has eight chapters and two appendices, and it is structured as follows. This introduction highlights the motivations and the scope of the work. The second chapter provides an overview of the 130 nm SiGe BiCMOS technology used for the prototype fabrications, and it illustrates the general techniques employed for the design of millimeter-wave and ultra-wideband circuits. Chapter 3 presents the distributed amplification approach and the demonstrated amplifiers. In particular, the circuit design sought the maximization of the usable bandwidth to support the broadest set of antennas. Within the frame of this thesis, a novel gain-element has been conceived to boost the bandwidth of operation of DAs. The first appendix contains the detailed circuit analysis of this gain cell. Beside traveling-wave amplifiers, which are a subset of DAs, Chapter 3 also presents the Cascaded Single-Stage Distributed Amplifiers (CSSDAs), which are formed by a cascade of single-cell distributed amplifiers. The available literature has been then enlarged presenting in this chapter, and in the second appendix, the first complete circuit analysis for this class of amplifier. This analysis has been used to design three CSSDAs: one optimized for low power, one for high speed, whereas the last targeted improved input and output matching, which was still an open issue of the state of the art. The amplifier optimized for high speed demonstrated a maximum frequency of operation of 250 GHz, which sets a record result for SiGe distributed amplifiers. Chapter 4 describes the development of UWB combiners and dividers formed by independent distributed amplifiers physically sharing part of their circuitry. These components demonstrated to be functional from 1 GHz to 220 GHz, being this as well record results for their circuit category. Chapter 5 describes the design of UWB mm-wave amplifiers based on resonant matching techniques. A UWB response has been demonstrated thanks to a multi-stub approach, while the introduction of a balanced architecture ensured robustness against fabrication mismatches and model inaccuracies, which are particularly severe at high frequencies. The research interest in these circuits originated from the need of a benchmark between distributed and resonant matched amplifiers. The designed circuit demonstrated one of the broadest bandwidth of operation for SiGe mm-wave amplifiers and yet confirmed the superiority of DAs in establishing amplification over broad bands but at price of more considerable dissipated power and silicon footprint. Chapter 6 presents the integration of amplifiers and antennas, and an on-chip antenna-amplifier system is demonstrated. The component consists of a multi-stacked Vivaldi antenna integrated with a CSSDA. A frequency band of operation from 140 GHz to 220 GHz is achieved. This result constitutes the research goals of the DAAB project demonstrating a relative bandwidth of operation approaching the 50%. Finally, Chapter 7 discusses possible UWB mm-wave transceivers concerning the complete system architecture (including mixers, filters, ADC), highlighting advantages and possible bottlenecks of real applications. The conclusions of the work are given in Chapter 8 together with an outlook on future investigations of UWB transceivers based again on distributed amplification.

2 Introduction to Wideband and High-Speed Circuit Design

This chapter presents the manufacturing technology and the design techniques used to develop the circuits and the systems covered by this thesis. A BiCMOS silicon-germanium process has been used for the experimental validation. This technology is provided by IHP under the name of *SG13G2*.

The first part of this chapter describes the main features of SiGe BiCMOS processes listing the active and passive devices offered by the *SG13G2* Process Design Kit (PDK), while the second part of the chapter covers the components used in microwave integrated-circuits such as transmission lines and networks for the distribution of the bias signals.

2.1 IHP *SG13G2* SiGe BiCMOS Fabrication Process

Silicon-germanium BiCMOS technologies are widely employed for the development of mm-wave circuits due to their high performances regarding speeds and the compatibility with Complementary Metal-Oxide-Semiconductor (CMOS). SiGe Heterojunction Bipolar Transistors (HBT) are based on the same working principle as Bipolar Junction Transistors (BJT), but make use of a heterojunction for the emitter-base interface to increase the transistor performance. The HBTs emitter is made of silicon, while a silicon-germanium alloy realizes the base. Fig. 2.1 illustrates the energy band diagram of a SiGe HBT. The lower energy band-gap of the SiGe alloy reduces the potential barrier seen by the electrons on the emitter side, resulting in an enhanced collector-current and hence a higher gain than conventional BJTs [9, 10]. Furthermore, the reduction of the

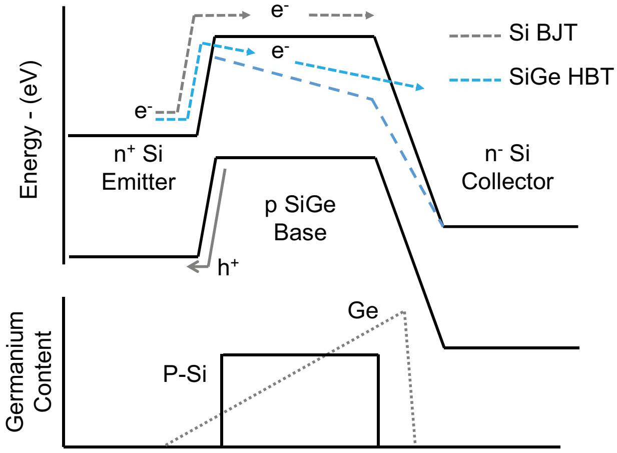


Figure 2.1: Band-gap diagram of a SiGe n-type transistor: the energy level of the conduction band of the base reduces (top graph) for increasing germanium doping (bottom graph). The band-gap diagram of SiGe HBT is also compared against that of a conventional silicon BJT [9].

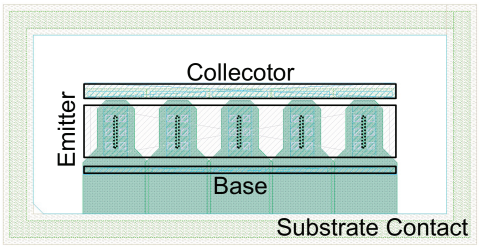


Figure 2.2: Layout top-view of the HBT offered by the *SG13G2* process.

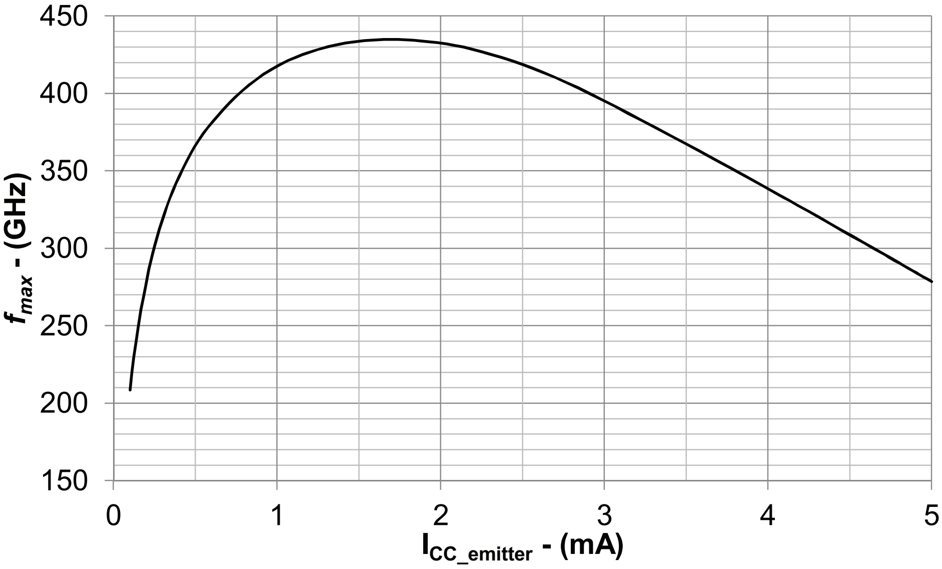


Figure 2.3: *SG13G2*-HBT f_{max} simulated for fixed V_{CE} of 1.6 V, and sweeping the collector bias current per emitter $I_{CC\_emitter}$.

base band-gap creates a drift electric-field which accelerates the electrons reducing their transit time in base. The diminution of the transit time, in turn, leads to an enhancement of the transistor transit frequency f_t and maximum oscillation frequency f_{max} [9, 10].

The idea of exploiting heterojunctions to ameliorate common BJTs is as old as the BJT itself. It was in fact patented in 1951 by W. Schockley [11, 12], while the use of alloys to guide carriers in semiconductors was first presented by H. Kroemer in 1954 [13]. On the other hand, due to technological issues, it took almost thirty years to demonstrate the first operative HBT device [9, 10].

The components available in the SiGe *SG13G2* process are briefly illustrated in the next sections to prepare the description of the circuits demonstrated in this thesis.

2.1.1 HBT - *npn13G2*

The transistor with highest f_{max} offered by the *SG13G2* technology is the SiGe npn-HBT, with PDK name *npn13G2*. The feature size of the process is 130 nm, and at the time of writing it is the fastest SiGe BiCMOS process commercially available [14]. As demonstrated in [15], the process f_{max} sets the upper limit on

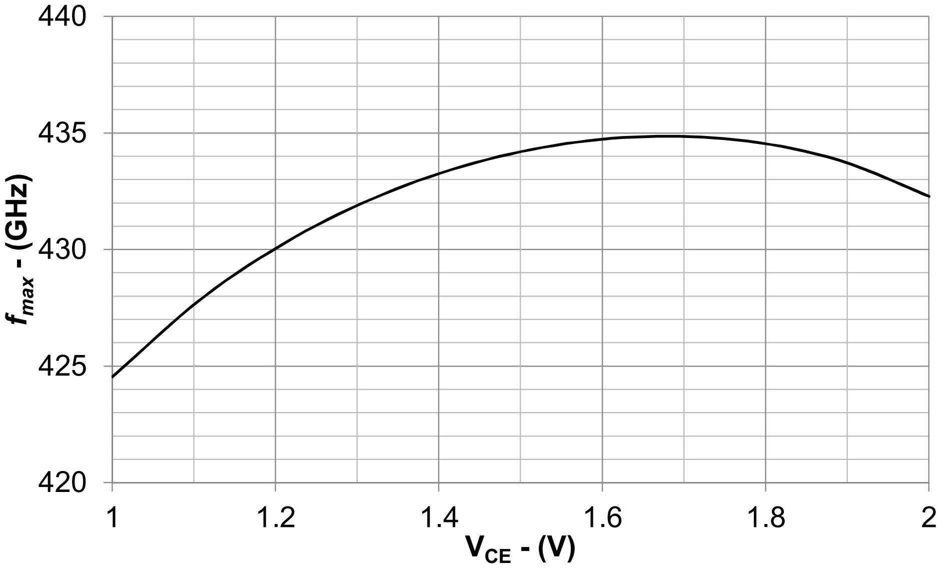


Figure 2.4: *SG13G2*-HBT f_{max} simulated for fixed $\mathrm{I_{CC\_emitter}}$ of 1.8 mA, and sweeping $\mathrm{V_{CE}}$.

the highest possible frequency of operation of DAs. Therefore, the transistor biasing targeted to maximum f_{max}, which for the *SG13G2* is 450 GHz [14]. Achieving circuits operating at the highest possible frequency has been crucial in this research to minimize the silicon footprint, and hence the cost, of the antennas co-integrated with the amplifiers in the final demonstrator (Chapter 6).

The approximated expressions of transit and maximum oscillation frequencies are:

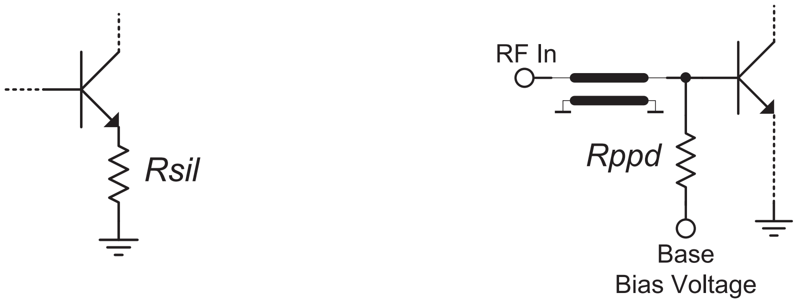
$$f_t = \frac{g_m}{2\pi C_{be}} \tag{2.1}$$

$$f_{max} = \sqrt{\frac{f_t}{8\pi r_b C_{bc}}} \tag{2.2}$$

where $\mathrm{g_m}$ is the small-signal HBT transconductance, $\mathrm{C_{be}}$ and $\mathrm{C_{bc}}$ the small-signal HBT base-emitter and base-collector capacitances respectively, and $\mathrm{r_b}$ is the small-signal HBT base-resistance. Since several second-order RC constants are neglected, these simple equations yield rather optimistic values, and they represent upper limits for f_t and f_{max} [1].

Despite the simplifications, eq. (2.1) and (2.2) relate the transistor speed to its small-signal parameters, which depend on bias conditions, layout geometry, process variations and temperature. An example of a transistor layout modeled in the PDK is illustrated in Fig. 2.2. This particular HBT has five emitters but the PDK offers configurations with up to ten emitters. The area of single emitter is $0.9\times0.07\,\mu\mathrm{m}^2$.

Fig. 2.3 and 2.4 show the simulated f_{max} for different bias collector-currents per emitter $\mathrm{I_{CC\_emitter}}$, and collector-emitter voltages $\mathrm{V_{CE}}$. As illustrated, the highest f_{max} is reached for $\mathrm{I_{CC\_emitter}}$ of 1.8 mA and $\mathrm{V_{CE}}$ of 1.6 V. This translates in static power dissipation ($\mathrm{P_{DC}}$) of 2.88 mW per emitter. In general, high bias



(a) (b)

Figure 2.5: Typical circuital employments of (a) *Rsil* and (b) *Rppd* resistors.

collector-currents and collector-emitter voltages increase the complexity of the integrated systems since each of their parts has to sustain more dc-bias levels. High current densities are of particular concern for metal layers and integrated resistors that can fuse due to thermal dissipation, or experience electromigration. High voltages can destroy the gate-oxide of Metal-Oxide-Semiconductor (MOS) structures. Due to these considerations, V_{CE} and $I_{CC\_emitter}$ have been reduced in most of the designs presented in this work to 1.2 V and 1.5 mA, respectively.

2.1.2 MOS Transistors

The n- and p-MOS transistors offered by the process have lower performances regarding speed if compared to the HBT counterpart. In general, these MOS transistors realize the digital parts integrated in BiCMOS technologies. Their minimum channel length is 130 nm. In this work, these transistors have been employed only as MOS capacitors to shunt to ground unwanted Radio-Frequency (RF) signals.

2.1.3 Bulk Resistors - *Rsil* / *Rppd*

The process offers salicided *Rsil* and unsalicided *Rppd* gate-polysilicon resistors. Due to technological reasons, salicided resistors typically have square resistances of two orders lower than that of unsalicided counterparts.

Rsil resistors have been therefore preferred when resistances up tens of Ohm were needed, while *Rppd* devices have been chosen in case of resistances with values higher than hundreds of Ohm. This guideline is motivated by the need to minimize the resistor silicon footprint and parasitics, and yet to have devices with a width large enough to sustain the bias currents. In particular, when resistors with large dimensions where necessary, then electromagnetic simulations as in [16] have been used to predict their parasitics.

Fig. 2.5 shows an example of the use of these resistors within this thesis: *Rsil* is employed as emitter degeneration in Fig. 2.5a, since resistance in the order of Ω is required; whereas in Fig. 2.5b *Rppd* feeds a small base-bias current (µA) to

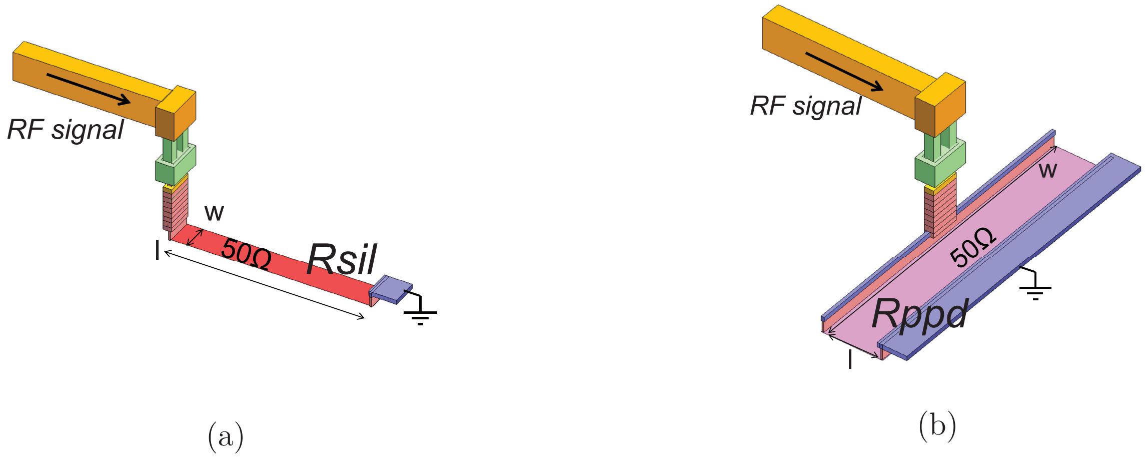


Figure 2.6: 3D view of 50 Ω (a) *Rsil* and (b) *Rppd* resistors interconnected between a transmission line and ground.

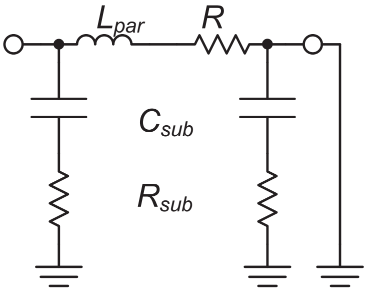


Figure 2.7: Equivalent circuit of *Rsil* and *Rppd* resistors for the configuration in Fig. 2.6 where one terminal of the device is shorted to ground: C_{sub} and R_{sub} are the substrate capacitance and resistance, L_{par} is the parasitic inductance of the component plus that of the attached via stack.

the HBT via its kΩ resistance. This large resistor prevents the leakage versus the supply line of RF signals, which are also applied at the HBT base.

In case of 50 Ω resistors, *Rsil* and *Rppd* have almost same footprint but opposite width and length: the first is narrow and long, while the second is wide and short, as Fig. 2.6 shows. 50 Ω resistors are of particular interest in this work since they are used in DAs as termination resistance (Chapter 3). The equivalent circuit, valid for both the resistors, is given in Fig. 2.7: for *Rsil* the dominant parasitic is the inductance L_{par}, while for *Rppd* it is the capacitance to ground, due to the distinct device shapes. The different dominant parasitic leads to divergent frequency-trends of the components equivalent resistance, as Fig. 2.8 shows.

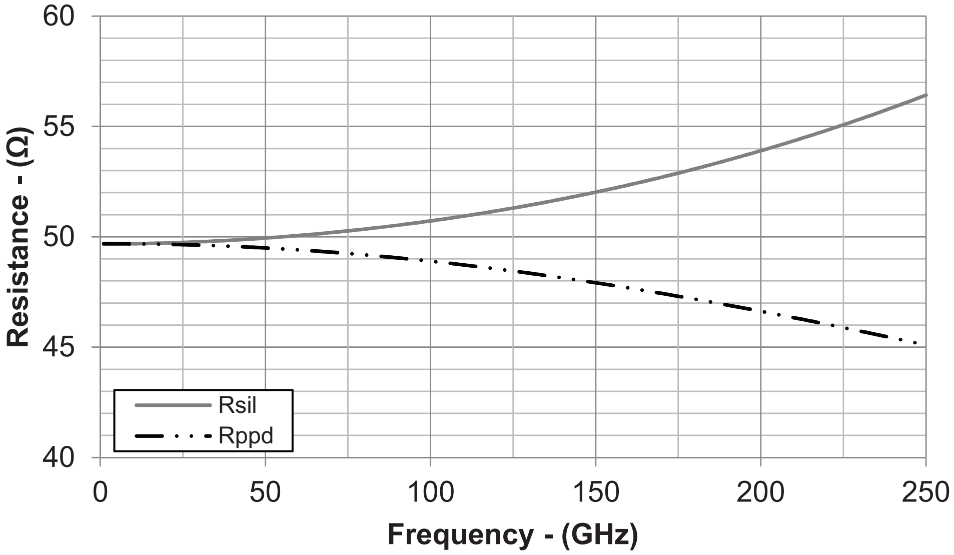


Figure 2.8: Simulated equivalent resistance of the resistors in Fig. 2.6.

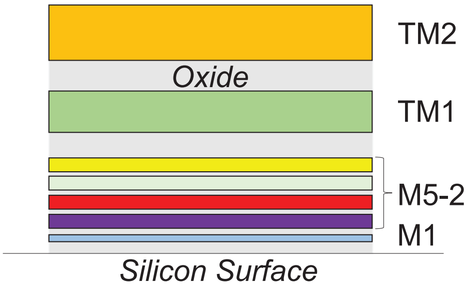


Figure 2.9: Simplified metal-stack of the *SG13G2* process. The MIM layer between TM1 and M5, and the passivation above TM2 are not shown.

2.1.4 Metal Stack

The *SG13G2* technology supports the design of mm-wave circuits with a suited back-end-of-the-line. Fig. 2.9 shows the metal stack: seven levels of metallization are available, two of them are thick top metals ($TM_{1,2}$) to sustain high current densities and be reliant against electromigration, while the other five ($M_{1,5}$) are lower layers for dense interconnections. The tick dielectric between the highest metal and the active silicon enables the design of transmission lines with high characteristic impedance, as it will be shown in Section 2.2. More in detail, altogether, the metal layers allow designing coplanar, microstrip and stripline transmission lines with a high degree of freedom for the dielectric thickness. Finally, the silicon substrate of the process is 300 µm thick, but the foundry offers also mechanical thinning and etching of the back side to reduce the substrate losses.

2.1.5 MIM Capacitors - *Cmim*

The *SG13G2* process offers Metal-Insulator-Metal (MIM) capacitors with high quality-factors and high resonance frequencies. The MIM capacitors are formed

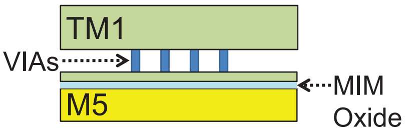


Figure 2.10: Cross-section view of a *Cmim* capacitor: the MIM structure is formed between M5, an oxide with high dielectric constant, and a metal plate connected with vias to TM1.

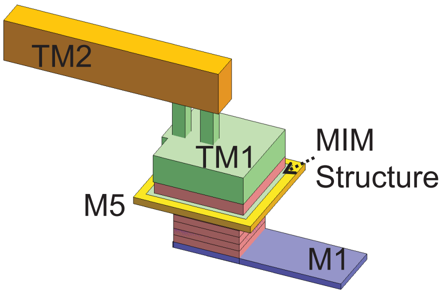


Figure 2.11: 3D view of a *Cmim* capacitor connected between TM2 and M1 layers.

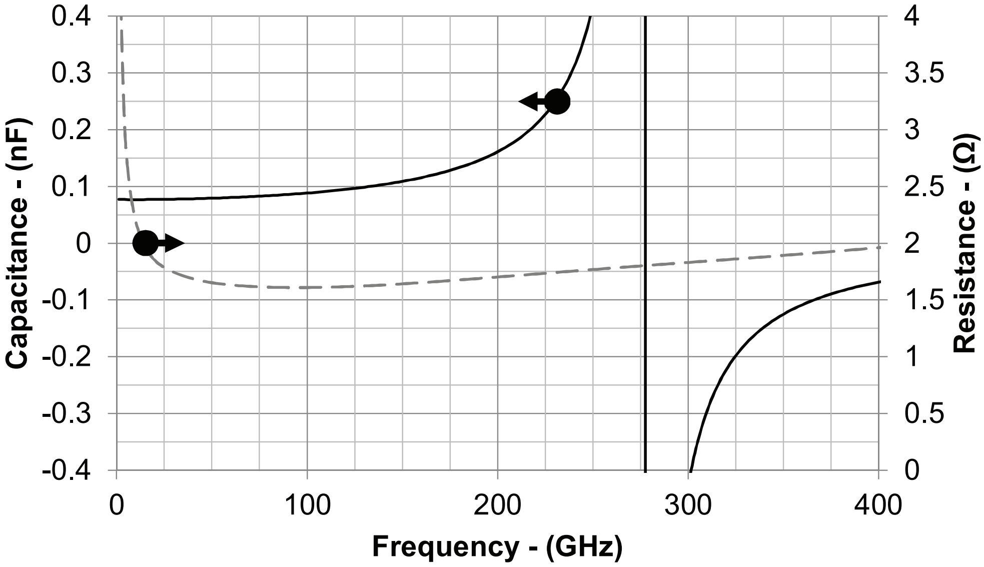


Figure 2.12: Simulated capacitance and parasitic resistance of the structure in Fig. 2.11 assuming a series capacitor-resistor equivalent model.

between M5 and a metal plate attached to TM1 and moved close to M5 to increase the capacitance of the structure. An oxide with a high dielectric constant is also used with the same aim. Fig. 2.10 shows the cross-section of the structure.

Due to their high self-resonance frequency, *Cmim* capacitors have been used in the networks guiding the RF signals. Fig. 2.11 illustrates the typical usage of this component: one plate of the capacitor is attached to the signal conductor of a transmission line, which is fabricated in TM2, while the other side is connected to M1 where the transistor contacts are available. A crucial aspect of the behavior of these components at mm-wave frequencies is that the via interconnections have

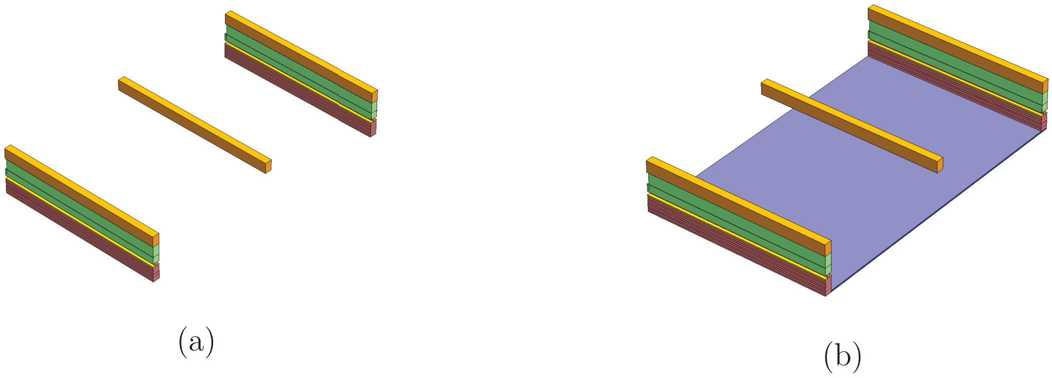
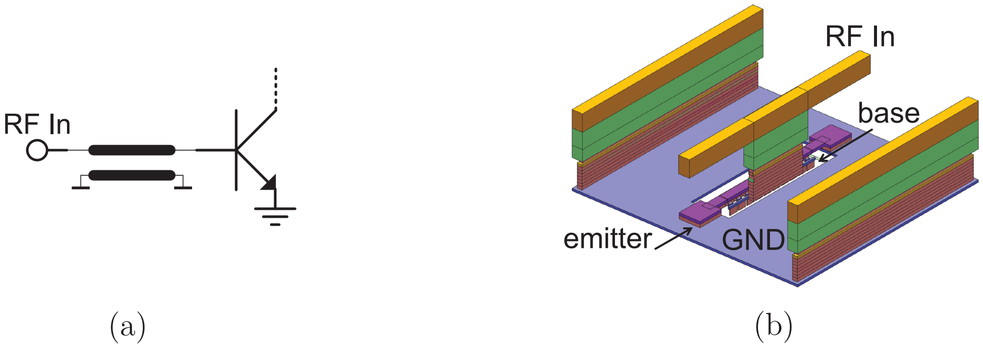

(a) (b)

Figure 2.13: (a) CPW and (b) microstrip transmission-lines used in this thesis.



(a) (b)

Figure 2.14: Connection example between TL and transistor, where the signal conductor of the TL is attached to the base of the device while the ground conductor to its emitter. (a) Schematic, (b) 3D view.

non-negligible parasitics. Fig. 2.12 shows the simulated equivalent capacitance of the *Cmim* in Fig. 2.11: the capacitance increases toward the frequency from its low-frequency value till the self-resonance with its parasitic inductance. After the self-resonance, the component behaves as an inductor. For this particular device, the capacitance raises from 70 fF to 400 fF over the frequency range 1 GHz – 250 GHz.

The significant impact of parasitics on the PDK components motivated the use of EM simulations to predict their behavior. Fig. 2.12 also shows the simulated parasitic resistance of the wired capacitor, which is below 2 Ω.

2.2 Integrated Transmission Lines

To meet the needs of the circuit design, Transmission Lines (TL) with low attenuation constant (α), and short guided wavelength are required. The first in fact determines the percentage of attenuation experienced by a signal traveling into the line along a certain distance, while the latter has a direct impact on the physical size of the system, and hence on its cost. Furthermore, transmission lines with high characteristic-impedance Z_0 are also beneficial to reduce the silicon footprint of mm-wave circuits. As a possible example, TLs with high Z_0, due

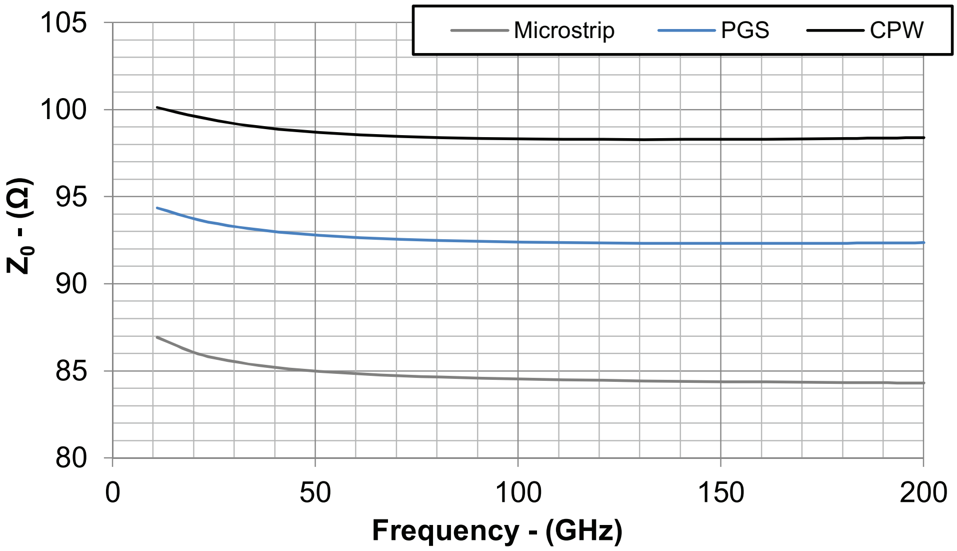


Figure 2.15: Simulated characteristic impedance of CPW, microstrip, and PGS-microstrip lines for same physical dimensions, which are annotated in Fig. 2.17.

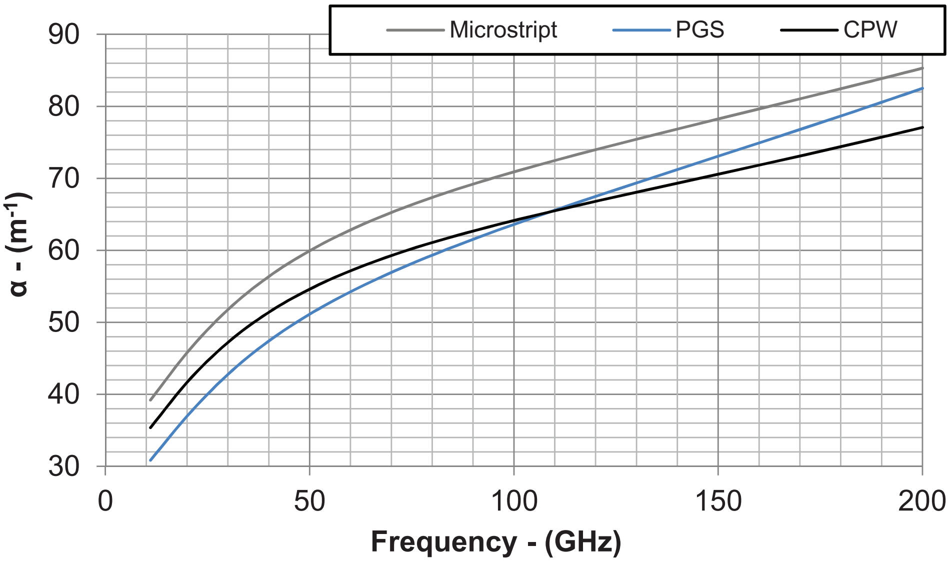


Figure 2.16: Simulated attenuation constant of CPW, microstrip, and PGS-microstrip for same physical dimensions, which are annotated in Fig. 2.17.

to large inductance per unit of length, have been used in the past to reduce the silicon footprint of TWAs [Testa1]. Section 3.3 will discuss the impact of Z_0 on the TWAs dimensions.

Within the frame of this thesis integrated microstrip and Conventional Pseudo-coplanar Waveguide (CPW) transmission-lines have been investigated. Fig. 2.13 shows their 3D view. The pseudo-coplanar design differs from the coplanar waveguide for the lateral ground side-walls. These are required to fulfill the process metal-density rules. Nevertheless, simulations showed that these side-walls have minimal impact on the performance of the line. From the circuit design point-

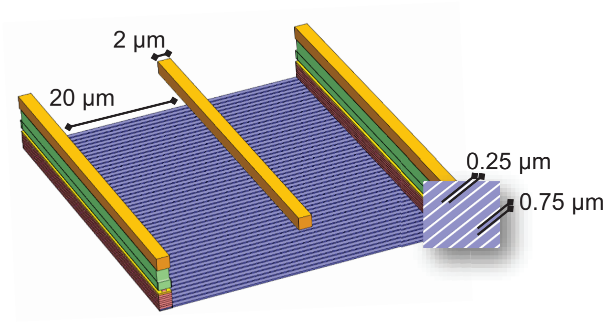


Figure 2.17: PGS microstrip line employed to enhance the performance of conventional microstrips (Fig. 2.13b). All the physical dimensions of the structure are annotated.

of-view, microstrips are advantageous offering a ground plane which reduces the parasitic to the ground of the devices connected to the line. Fig. 2.14 shows an example of transistor attached to a microstrip line. On the other hand, CPWs have higher Z_0 and lower α, as it can be seen in Fig. 2.15 and 2.16.

The performance of microstrip lines can be improved with Patterned-Ground-Shields (PGS) [17], as it is shown in Fig. 2.17. The simulated Z_0 and α of this line are also shown in Fig. 2.15 and 2.16: Z_0 is increased, and α is lowered in comparison to the microstrip. These improvements are enabled by the PGS, which force the backward current to flow in the ground side-walls rather than in the thin bottom metal-layer of the process. The flowing of the backward current into the side walls reduces the losses since these structures have higher conductance than the lower process metal layers. At the same time, Z_0 increase due to the increasing infuctance per unit of length of due line due to a larger return path of the backward traveling currents, that cannot flow anymore below the signal conductor [17].

2.3 Wideband Bias-Distribution Networks

The distribution of supply voltages and currents within the chips is a challenging task when high frequencies and wide frequency-bands of operation are involved. In fact, the bias signals reach the circuit cores after passing through pads, and electrically-long interconnections, which suffering from parasitics and coupling effects can deviate the operation of the devices leading to systems with poor performances. Wideband bias-distribution networks have been designed in this thesis to ensure the proper operation of the developed circuits. The following sections illustrate these structures.

2.3.1 Zero-Ohm Lines

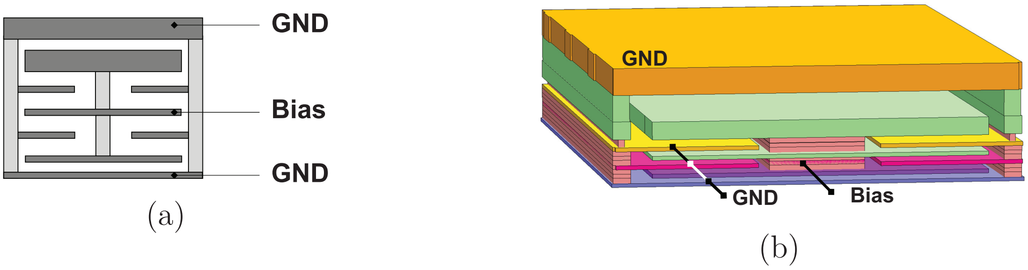
Zero-ohm lines are transmission lines with extremely low characteristic impedance, typically below $10\,\Omega$, which allows to ac-ground every signal propagating within them [18].

As every transmission line, zero-ohm lines are easy to model and offer a robust approach to the simulation of the supply distribution networks [19]. Fig. 2.18 shows the cross-section and the 3D view of the zero-ohm line used in this thesis: here the first, the fifth and the seventh metal layers of the process have been used as ground, while the sixth, the forth and the second carry the dc-bias signal. Fig. 2.20 and 2.21 show the simulated characteristic line impedance and attenuation constant: Z_0 is close to $0\,\Omega$ and this, as demonstrated in [18], implies an elevate attenuation constant, that in turn dissipates any ac-signal traveling in the structure. The attenuation constant of the line can be in fact expressed as [18]:

$$\alpha = \frac{R'}{2Z_0} + \frac{Z_0 G'}{2} \approx \frac{R'}{2Z_0} \tag{2.3}$$

where R' and G' are the resistance and conductance per unit-of-length of the line, and Z_0 is its characteristic impedance. Eq. (2.3) holds under the condition that R'G' is small compared with 2ωL'C', where L' and C' are the line inductance and capacitance per unit of length. Since G' is due to the losses of the metal-stack dielectric oxide, which are usually negligible for integrated circuit technologies, the attenuation of the line is dominated by the series metal-loss R' [18]. As eq. (2.3) predicts, for a decreasing Z_0 it corresponds an increase of the propagation losses, in agreement with the simulation results shown in Fig. 2.20 and 2.21.

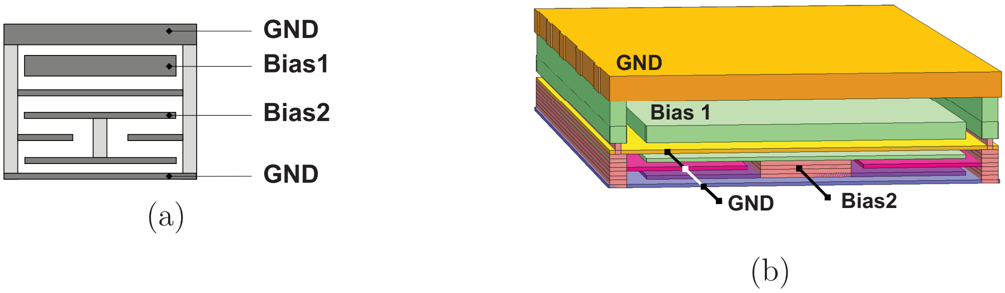
Besides, to save the chip area, multi-conductor zero-ohm lines have been designed, as Fig. 2.19 shows: here the first, the fifth and the seventh metal layers



(a)

(b)

Figure 2.18: Zero-ohm line: (a) cross-section, (b) 3D view.



(a)

(b)

Figure 2.19: Multi-conductors zero-ohm line: (a) cross-section, (b) 3D view.

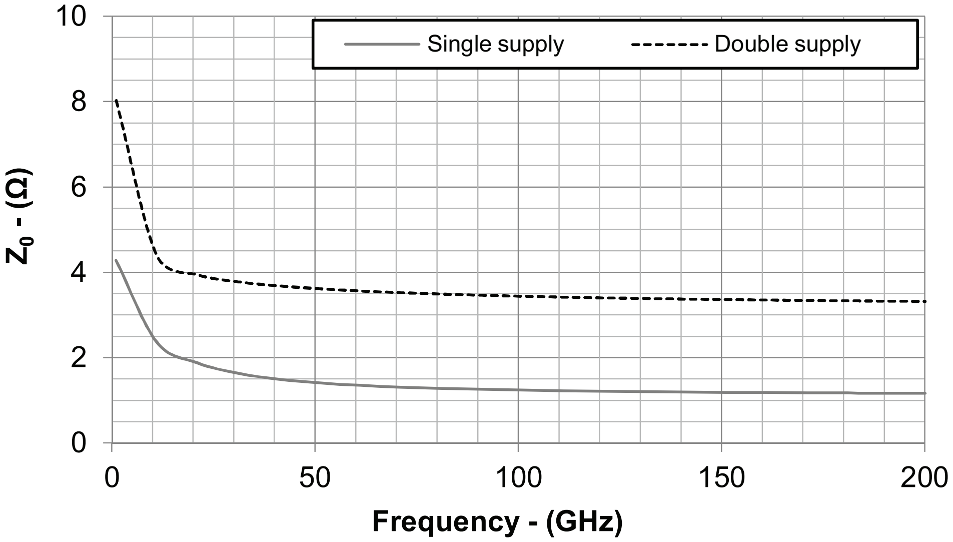


Figure 2.20: Simulated characteristic impedance of the zero-ohm lines in Fig. 2.18 and 2.19.

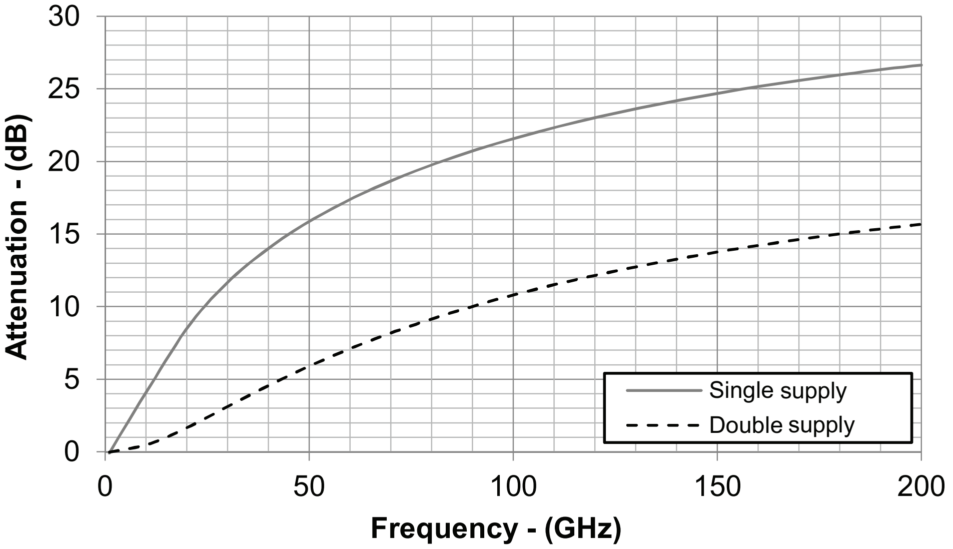


Figure 2.21: Simulated attenuation over 100 µm of the zero-ohm lines in Fig. 2.18 and 2.19.

of the process have been used as ground, while the sixth delivers a bias signal, whereas the forth and the second carry a second independent bias-signal supply. Fig. 2.20 and 2.21 present also the simulated features of the multi-conductor zero-ohm line.

2.3.2 Blocking Cap

The second component used in this work to deliver bias signals is the blocking cap. In first analysis the use of large capacitors allows obtaining low impedance to ground at low frequencies but, on the other hand, due to the parasitic inductance of the device, a Self-Resonance Frequency (SRF) has to be taken in account. After the SRF, the capacitors have an inductive behavior, and their impedance

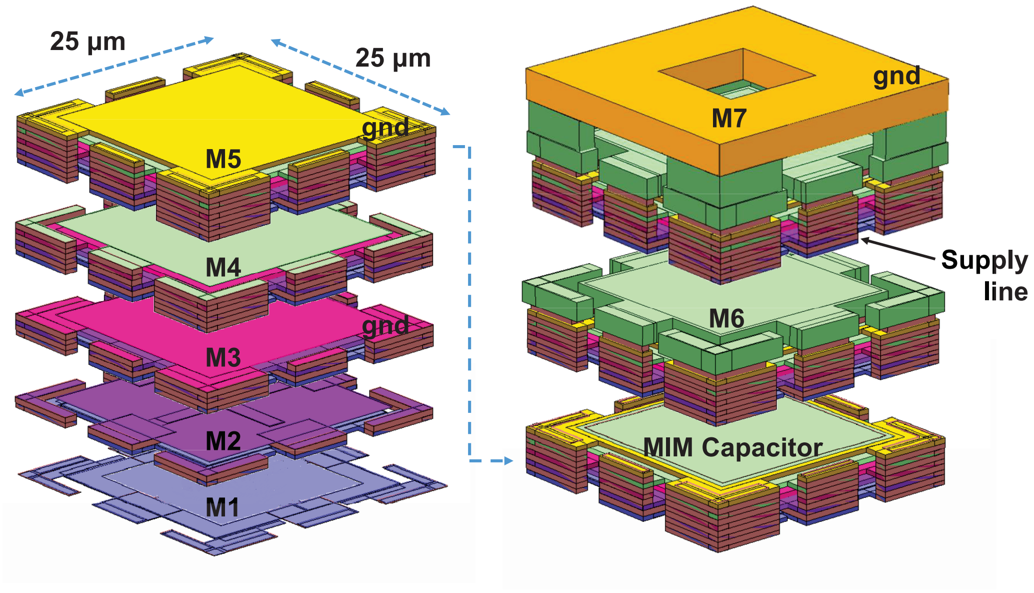
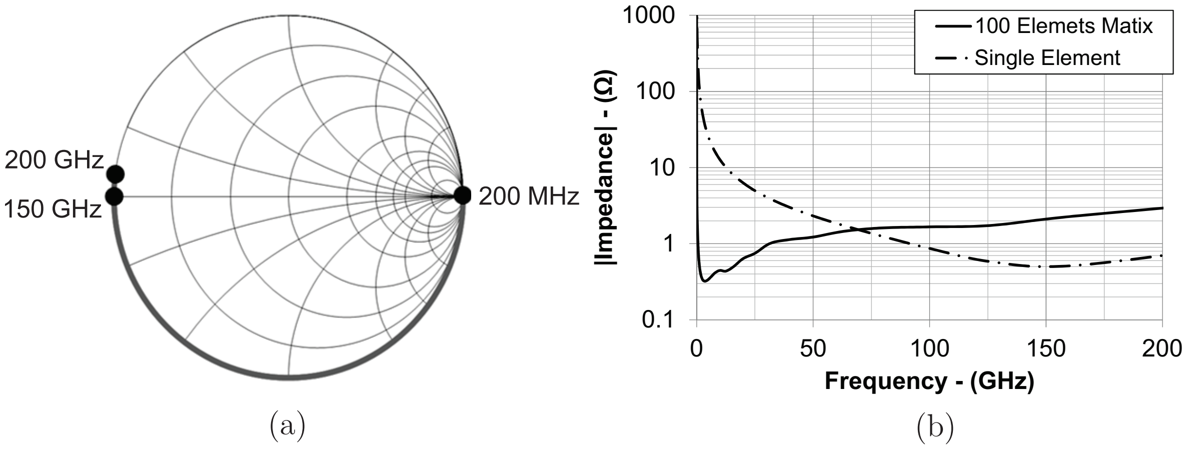

25 µm
25 µm
gnd
M5
M4
gnd
M3
M2
M1
gnd
M7
Supply line
M6
MIM Capacitor

Figure 2.22: Multi-plate capacitor used in the bias distribution networks [Testa1].



(a) (b)

Figure 2.23: (a) Impedance representation of the multi-plate capacitor of Fig. 2.22 in the Smith chart. (b) Impedances magnitude of the multi-plate capacitor of Fig. 2.22 and of a 10-by-10 array of elements of the same type [Testa2].

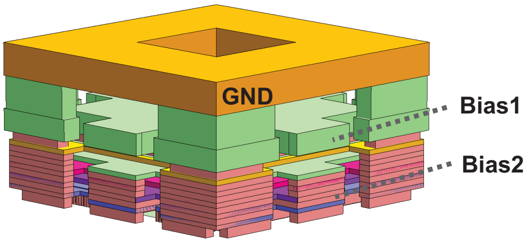

GND
Bias1
Bias2

Figure 2.24: Multi-plate capacitor able to simultaneously distribute two bias signals.

has the same magnitude of that associated with the parasitic inductance. The minimization of the parasitic inductance is, therefore, necessary to maximize the SRF and to minimize the inductance of the component at frequencies beyond the SRF. Multi-plate capacitors have been designed to offer several parallel current paths resulting in a reduced parasitic inductance.

Fig. 2.22 illustrates the component. For the annotated dimensions, this particular device offers a capacitance of 1.25 pF and parasitic inductance of just 0.9 pH. These values correspond to an SRF around 150 GHz. Due to the low parasitic inductance, even after its SRF, the blocking cap can be approximated with an ac-ground, as Fig. 2.23a shows. Furthermore, to ac-ground the bias distribution networks also at the lowest frequencies of operation, such as 1 GHz, array of these multi-plate capacitors are employed in a parallel connection. The comparison between the impedance to ground offered by one multi-plate capacitor and an array made of one hundred elements of this type is illustrated in Fig. 2.23b. As it is shown, the use of large matrices of these components lowers the impedance to ground toward low frequency. Finally, to enable the simultaneous distribution of two dc-signals, a variant of this device has also been used. The connection between M6 and M4 has been removed, creating two separate supply lines, as Fig. 2.24 illustrates: the sixth metal has been employed for the first dc supply, while the second and fourth for the second bias signal. Again, the first, third, fifth, seventh metal layers are used to realize the ground.

3 Distributed Amplifiers

3.1 Introduction

Wideband amplifiers are essential for several applications at mm-wave frequencies, such as radar imaging, optoelectronics, plasma diagnostics, space radiometry, high-frequency transceivers, ultra-fast measurements, security, and defense systems. The shared requirement of these applications is the necessity to amplify short pulses to probe the environment or the objects under examination or to transmit and receive information at very high data rates. These capabilities are strictly associated with the bandwidth of the signals relevant for the target systems. For this motivation, amplifiers with bandwidths in the order of hundreds of GHz are necessary.

A popular approach to the design of such amplifiers is the exploitation of distributed amplification techniques, first proposed by Percival in 1937 [20] with later widespread awareness provided by the paper of Gizton in 1948 [21]. From their early demonstration with solid-state devices in 1969 [22], many research groups studied distributed amplifiers, including the subset of Traveling-Wave Amplifiers (TWAs) and Cascaded Single-Stage Distributed Amplifiers (CSSDAs).

In the last forty years, implementations of TWAs and CSSDAs have been reported in all the most relevant technologies: Indium Phosphide (InP) High-Electron-Mobility Transistor (HEMT) [15, 23–25], bulk-silicon CMOS [26–29], Silicon-on-Insulator (SOI) CMOS [30, 31], and Gallium Arsenide (GaAs) HBT [32, 33]. Additionally, distributed amplifiers fabricated in SiGe technologies with bandwidth exceeding 100 GHz have been recently demonstrated [Testa1, Testa19, 34–36].

In any of their possible implementations, the operation of distributed amplifiers relies on synthetic transmission-lines, which are formed by loading conventional transmission lines with the input and output capacities (C_{in} and C_{out}, respectively) of the attached amplifiers, as Fig. 3.1 shows. These amplifiers are called

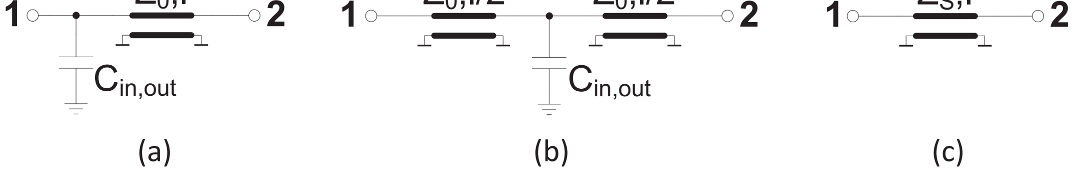


Figure 3.1: (a) Two-ports formed by the capacitor $C_{in,out}$ and the transmission line of impedance Z_0 and length ℓ, (b) two-ports formed by $C_{in,out}$ interposed between two lines of impedance Z_0 and length $\ell/2$, (c) equivalent synthetic transmission-line of the two two-ports obtained with eq. (3.1) and (3.2).

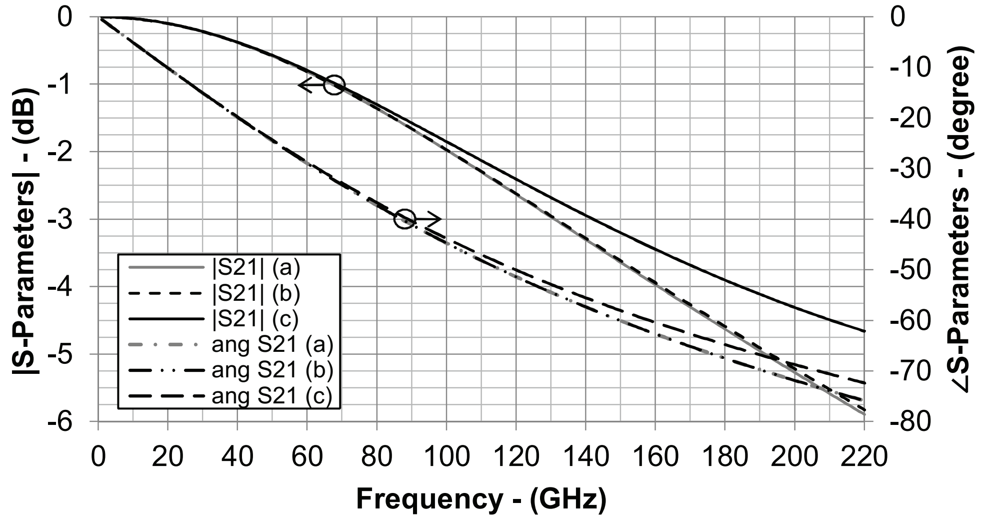


Figure 3.2: Comparison of the simulated transmission parameters for the circuits of Fig. 3.1a, 3.1b, and 3.1c.

gain cells or gain elements [37]. The guiding structures so formed inherently offer broad frequency bands of operations like the original transmission lines.

The general assumptions for the modeling of distributed amplifiers are here summarized to set aside the preliminary equivalences that will be used in the following sections to recall the circuit analysis of TWAs [37], and to present the first complete circuit analysis of CSSDAs valid for the whole frequency band of amplification. As their physical counterparts, the synthetic transmission-lines are described by their characteristic impedance Z_S [37]:

$$Z_{\mathrm{S}} = \sqrt{\frac{L'}{C' \ + \frac{C_{\mathrm{in,out}}}{\ell}}} \tag{3.1}$$

and propagation constant β_{s} [37]:

$$\beta_{\mathrm{s}} = \omega\sqrt{L' \ (C' \ + \frac{C_{\mathrm{in,out}}}{\ell})} \tag{3.2}$$

where ω is the angular signal frequency, L' and C' are the inductance and capacitance per unit-of-length of the physical lines, and ℓ the distance between the gain cells.

The fundamental assumption in distributed amplification is the equivalence between the transmission lines loaded by a capacitor (Fig. 3.1), and their equivalent synthetic transmission-line obtained with eq. (3.1) and (3.2). Fig. 3.2 shows the simulated behaviors of these networks. For the sake of this example and the practical relevance within this thesis, the properties of the line and attached capacitance are chosen in the same order of those of the presented designs: $C_{\mathrm{in,out}}$ is 50 fF, ℓ is 25 µm, and L' and C' are 0.42 µH/m and 92.5 pF/m, respectively. From 1 GHz to 220 GHz the circuits in Fig. 3.1 have negligible difference in the

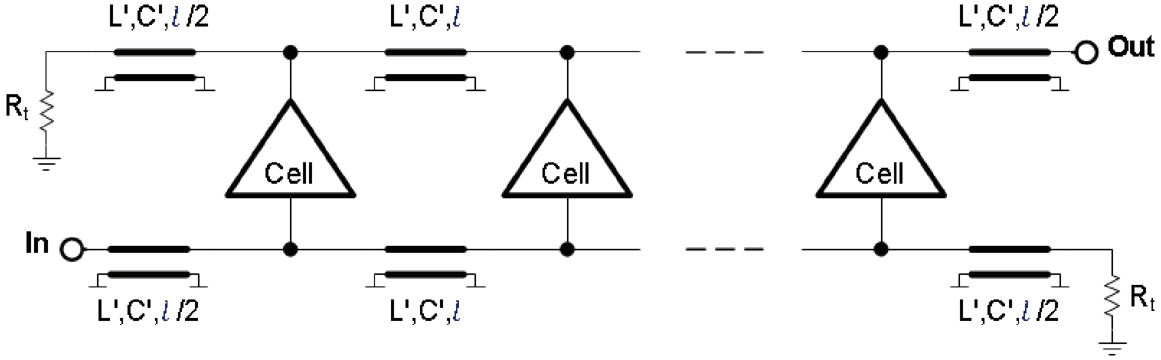

L',C',l/2
L',C',l
L',C',l/2
Out
Rt
Cell
Cell
Cell
In
L',C',l/2
L',C',l
L',C',l/2
Rt

Figure 3.3: Circuit schematic of traveling-wave amplifiers.

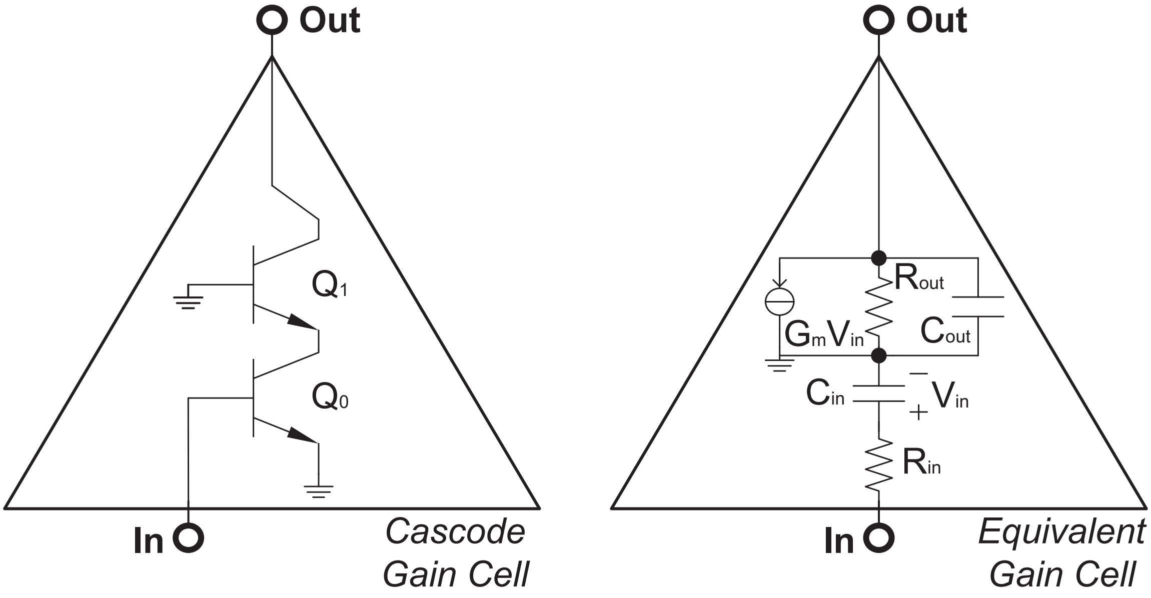

Out
Q1
Q0
In
Cascode Gain Cell
Out
Rout
GmVin
Cout
Cin
Vin
Rin
In
Equivalent Gain Cell

Figure 3.4: Cascode gain-cell and equivalent small-signal circuit.

response: for the insertion-phase below 1° at 100 GHz, and below 6° at 220 GHz; while for the insertion-loss below 0.2 dB at 100 GHz, and 1 dB at 220 GHz.

The synthetic-line model is thus an approximation of the circuits of Fig. 3.1a and Fig. 3.1b, which provides a compact description for these *line-capacitor* configurations. Indeed, for increasing frequency the mismatch between the response of the three circuits increases. Finally, the synthetic-line model loses validity approaching the Bragg cutoff frequency of the network [30]:

$$f_{\text{Bragg\_Synthetic}} = \frac{1}{\pi\sqrt{L_{\text{line}}\cdot\left(C_{\text{line}} + C_{\text{in,out}}\right)}} \tag{3.3}$$

where L_{line} is the line inductance $(\mathrm{L}' \cdot \ell)$, and C_{line} is the line capacitance $(\mathrm{C}' \cdot \ell)$.

3.2 Traveling-Wave Amplifiers (TWAs)

Fig. 3.3 depicts the general TWA circuit-topology: several gain elements or cells are enclosed between two transmission lines, which guide input and output signals. As discussed above, the fundamental idea is to embed the input and output cell capacitances within the guiding structures to realize synthetic transmission-lines. The gain elements transfer and amplify the signal traveling within the input line into the output line with different phase delays, while a suitable design ensures their coherent combination at the amplifier output.

3.2.1 Circuit Analysis

With the symbols defined in the previous section, the input and output characteristic synthetic-line impedances $\mathrm{Z_{Sin}}$ and $\mathrm{Z_{Sout}}$ are [38]:

$$Z_{Sin} = \sqrt{\frac{L'}{C' + \frac{C_{in}}{\ell}}} \tag{3.4}$$

$$Z_{Sout} = \sqrt{\frac{L'}{C' + \frac{C_{out}}{\ell}}} \tag{3.5}$$

The values of $\mathrm{Z_{Sin}}$ and $\mathrm{Z_{Sout}}$ set the quality of the TWA matching with load ($\mathrm{Z_L}$) and the generator ($\mathrm{Z_G}$) impedances.

In the ideal case of loss-less systems, a signal can propagate in the input line, be amplified by the gain elements and transmitted at the amplifier output for frequencies up to the synthetic-line cutoff defined in eq. (3.3). In practical TWA implementations, the losses of the synthetic transmission-line originating from the insertion of the gain cells have to be considered. Fig. 3.4 shows the equivalent small-signal circuits of the cells. Form this circuit it can be seen that the losses of the cell are attributable to its input and output resistances. If gain cells based on cascode configuration are in use, the output-parallel resistance $\mathrm{R_{out}}$ is large enough to be neglected. Therefore, $\mathrm{R_{in}}$ is the main loss contributor of the system that attenuates the signal propagating in the input lines [15, 30, 37]. The attenuation constant α_{in} is defined to model the reduction of the input signal by a factor $e^{-\alpha_{in}}$ over the line length ℓ. The analytic formulation of α_{in} is [15, 37, 38]:

$$\alpha_{in} = 2\pi^2 f^2 C_{in}^2 R_{in} Z_{Sin} \tag{3.6}$$

where f is the working frequency. Since the synthetic input-line losses increase with quadratic frequency dependence, α_{in} easily reduces the $-3\,\mathrm{dB}$ upper-corner frequency of TWAs to values smaller than the Bragg cutoff of eq. (3.3). Hence, the TWAs response is limited at high frequency by these two mechanisms. In detail, it is therefore essential to design the distributed amplifiers having the cutoff frequency of the synthetic-lines and the −3 dB corner frequency due to synthetic losses both above the desired maximum frequency of operation.

Under the assumption of input and output signals propagating with synchronous phases, output line losses negligible, and that $\mathrm{Z_S} = \mathrm{Z_L} = \mathrm{Z_G} = \mathrm{Z_{Sin}} = \mathrm{Z_{Sout}}$, the TWA power gain is approximated by [38]:

$$G_{TWA} = \Big(\frac{nG_mZ_S}{2}\Big)^2\Big(1 - \frac{n\alpha_{in}}{2}\Big)^2 \tag{3.7}$$

where n is the number of gain cells, and $\mathrm{G_m}$ their equivalent transconductance. This simple formula is very accurate for frequencies below the Bragg cutoff, while it gradually loses its validity when moving in frequency closer to it.

The limit of $\mathrm{G_{TWA}}$ for α_{in} approaching 0 corresponds to the ideal case of losses TWA, which is expressed as:

$$G_{TWA,ideal} = \frac{n^2G_m^2Z_S^2}{4} \tag{3.8}$$

Eq. (3.8) shows that the gain of an ideal TWA could be indefinitely increased with the number of cells, while the bandwidth would be limited by the cutoff frequency of the synthetic lines (eq. (3.3)). Conversely, in case of real TWAs, α_{in} is multiplied by n, representing that the losses of the single cell have a higher impact on the TWA response for an increasing number of cells. The losses, thus, not only limit the bandwidth but also set the optimal number of gain elements for the maximum Gain-Bandwidth Product (GBP). Reducing or compensating the losses allows increasing n without a corresponding bandwidth reduction, improving thus gain and GBP of the TWA.

3.3 170 GHz Loss-Compensated TWA

Within the frame of this thesis, a novel gain-cell has been demonstrated to increase the GBP and the maximum frequency of operation of TWAs with respect to conventional approaches based on cascode cells [Testa1]. The conceived cell produces a peak in its equivalent transconductance, this effect has been employed to compensate the synthetic-line losses at high frequency. The following sections describe in detail the designed $\mathrm{G_m}$-boosted cell. Therefore, circuit analysis, simulation and measurement results will be presented to validate the proposed technique.

3.3.1 Analysis and Design

As addressing directly the synthetic propagation-losses can improve the amplifier performance significantly, a TWA has been designed with the following purpose:

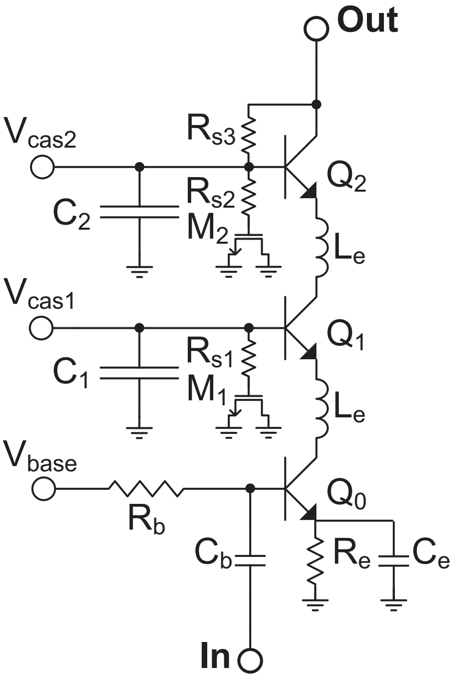


Figure 3.5: Circuit schematic of the G_m-boosted triple-cascode gain-cell developed in this thesis.

α_{in} is compensated by enhancing the equivalent transconductance of the cells, extending in this way the amplifier bandwidth up to higher frequencies [Testa1].

Another critical drawback of the state-of-art of DAs is the large area required for integration. PGS transmission-lines, like the one presented in Section 2.2, have also been employed to reduce the amplifier dimensions [29, 39–41]. The details of the presented TWA are provided below.

Gm-Boosted Gain-Cell Fig. 3.5 shows the schematic of the designed cell. The circuit is based on a cascode stage ($Q_0 - Q_1$), followed by an additional common-base amplifier (Q_2). The gain element so formed will be referred to as *triple cascode* within this manuscript. Among the important advantages of the cascode topology, it is possible to list high reverse isolation between output and input of the cells, which simplifies analysis and design of the circuit [15]; high output resistance, which reduces the synthetic losses of the output line (α_{out}) [30]; and low input capacitance thanks to the reduced Miller effect over the input stage. Contained input capacitances are a significant advantage of cascode-based TWAs because the reduction of C_{in} produces also that of α_{in} (eq. (3.6)) [30]. These essential features are also available with the gain cell presented here, where a common-base amplifier is stacked on top of a conventional cascode-cell. The three stacked transistors, together with inductive elements, produce a sharp peak in the transconductance of the cell. The inductive elements are realized with the collector-emitter connections between $Q_0 - Q_1$ and $Q_1 - Q_2$. In detail, bridge-shaped metal lines are used to obtain the inductors L_e shown in Fig. 3.5. The peaking of cell transconductance is shown in Fig. 3.6, where it is also compared

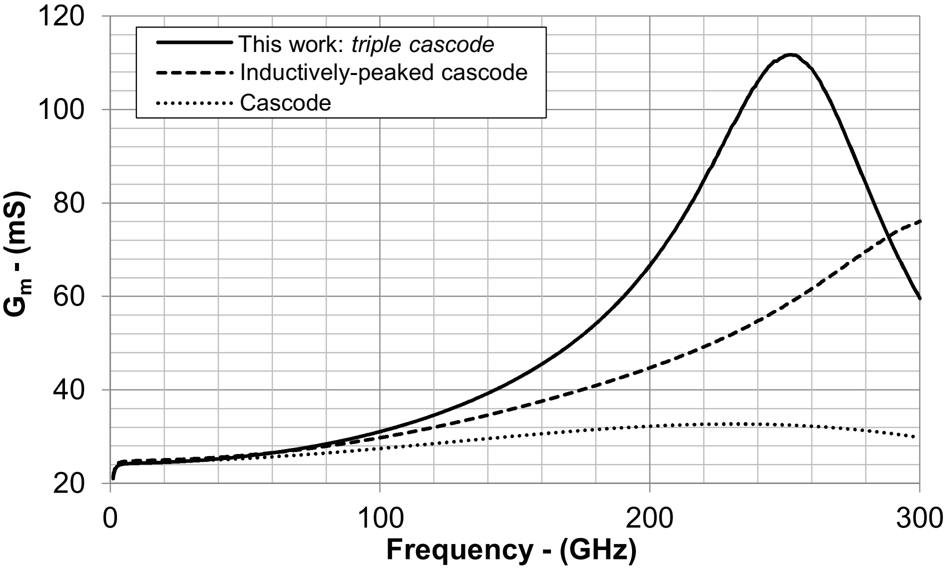


Figure 3.6: Simulated transconductance of the presented triple-cascode cell (Fig. 3.5) against those of conventional and inductively-peaked cascode. The three circuits have same emitter degeneration $R_e - C_e$, input series capacitor C_b, and L_e inductor. I_{CC} and V_{CE} per transistor are also the same.

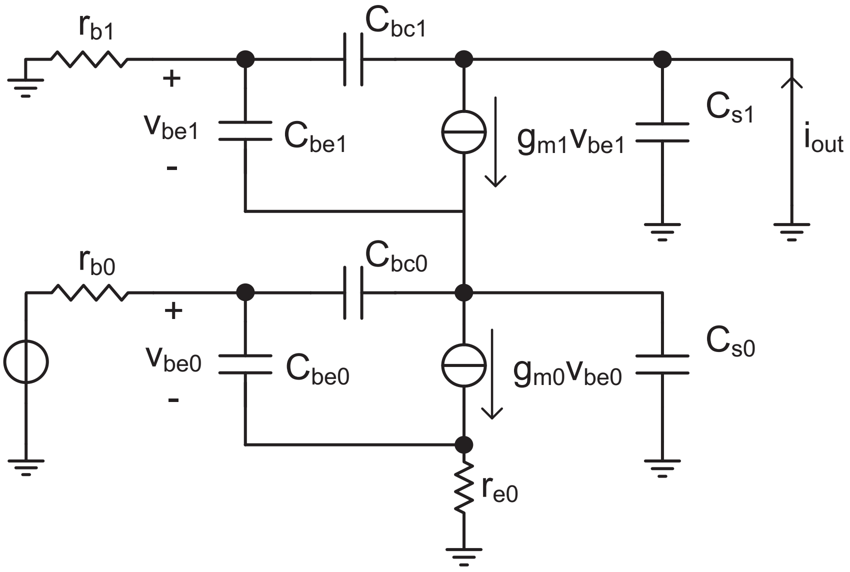
Table 3.1: Small-signal values of the circuits in Fig. 3.7 for the following bias conditions.

C_{be0-2}	C_{s0-2}	C_{bc-2}	g_{m0-2}	r_{b0-2}	r_{e0}
48 fF	6 fF	8 fF	152 mS	15.25 Ω	7.7 Ω

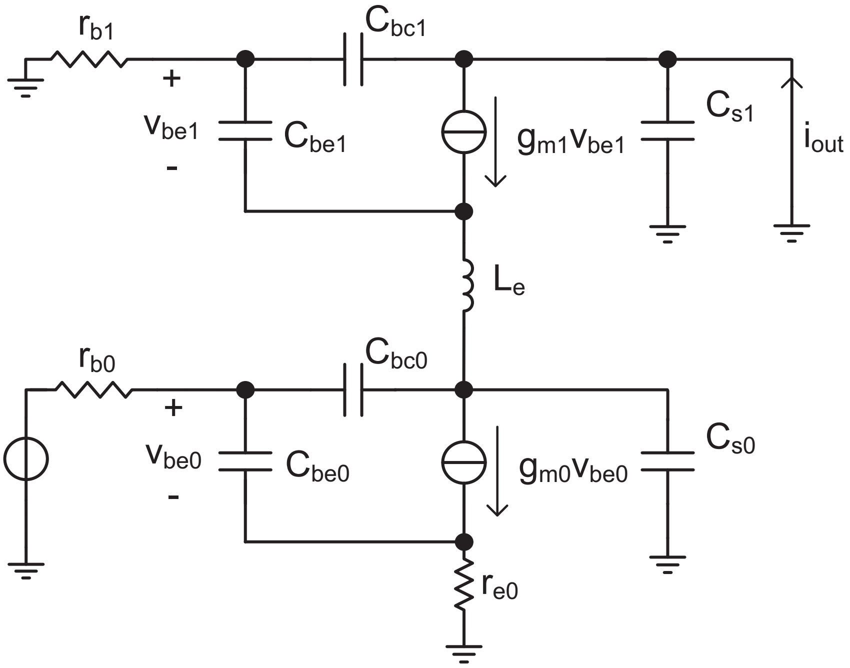
I_{base}	V_{cas}	V_{cas2}	V_{CC}
16 µA	2.1 V	3.3 V	3.6 V

for same technology and bias conditions (I_{CC} = 6 mA, V_{CE} = 1.2 V) against those of conventional and inductively-peaked cascode. As illustrated, the G_m of the presented cell has the steepest increment for increasing frequency. Since the TWA gain is proportional to ${G_m}^2$ (eq. (3.7)), its rapid increase has been exploited to compensate the losses (eq. (3.6)) improving the bandwidth of the amplifier.

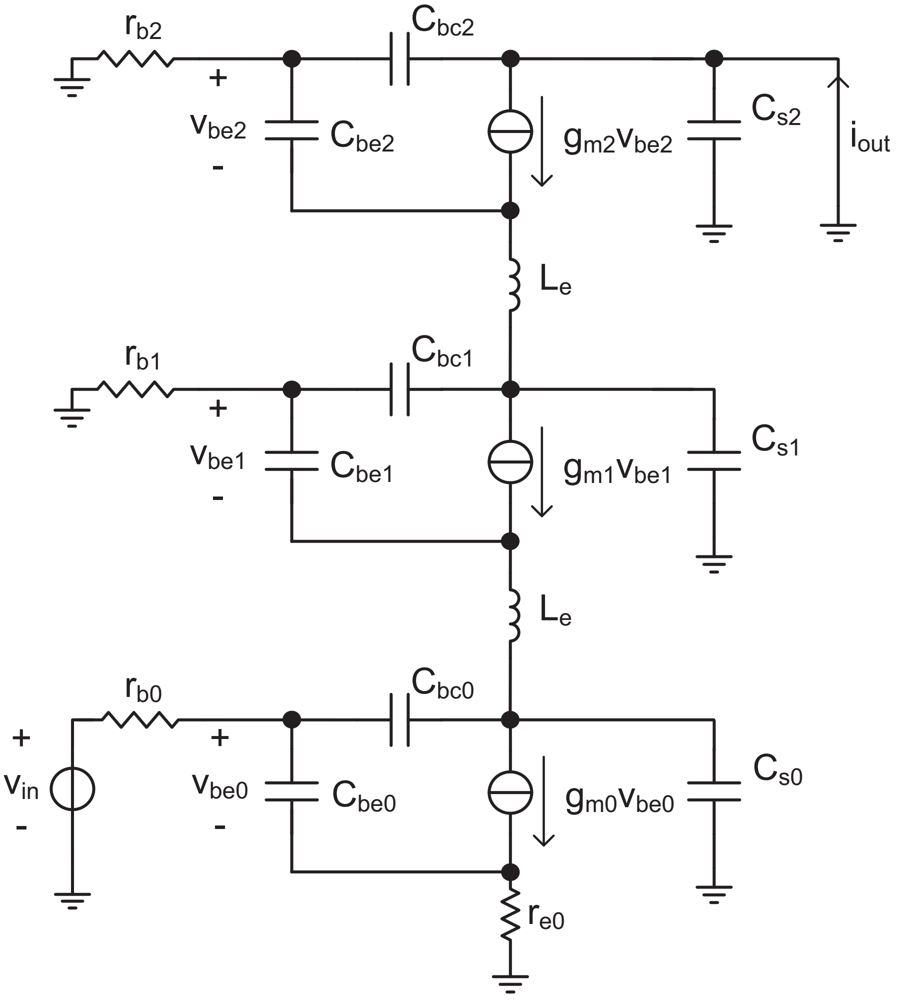
To illustrate more in detail the effects of the inductors L_e, Fig. 3.7 presents the simplified small-signal circuit of cascode, inductively-peaked cascode and proposed triple-cascode gain-cell, all without R_e, C_e and C_b for simplicity. The small-signal values of these equivalent circuits at the given operating point are in Table 3.1. V_{CC}, V_{cas}, and V_{cas2} are the bias voltages of the circuit in Fig 3.5, while I_{base} is the base bias-current of Q_0. The small-signal base-emitter voltages $v_{be0\text{-}2}$ and output currents i_{out} of these circuits are shown in Fig. 3.8. Fig. 3.8a shows that for a conventional cascode cell v_{be0}, v_{be1} and i_{out} decrease toward high frequency. This is due to the parasitic capacitances of the transistors. On the


r_{b1}
C_{bc1}
+
v_{be1}
-
C_{be1}
$g_{m1}v_{be1}$
C_{s1}
i_{out}
r_{b0}
C_{bc0}
+
v_{in}
-
+
v_{be0}
-
C_{be0}
$g_{m0}v_{be0}$
C_{s0}
r_{e0}

(a)


r_{b1}
C_{bc1}
+
v_{be1}
-
C_{be1}
$g_{m1}v_{be1}$
C_{s1}
i_{out}
L_e
r_{b0}
C_{bc0}
+
v_{in}
-
+
v_{be0}
-
C_{be0}
$g_{m0}v_{be0}$
C_{s0}
r_{e0}

(b)


rb2
Cbc2
+
vbe2
Cbe2
-
gm2vbe2
Cs2
iout
Le
rb1
Cbc1
+
vbe1
Cbe1
-
gm1vbe1
Cs1
Le
rb0
Cbc0
+
vin
-
+
vbe0
Cbe0
-
gm0vbe0
Cs0
re0

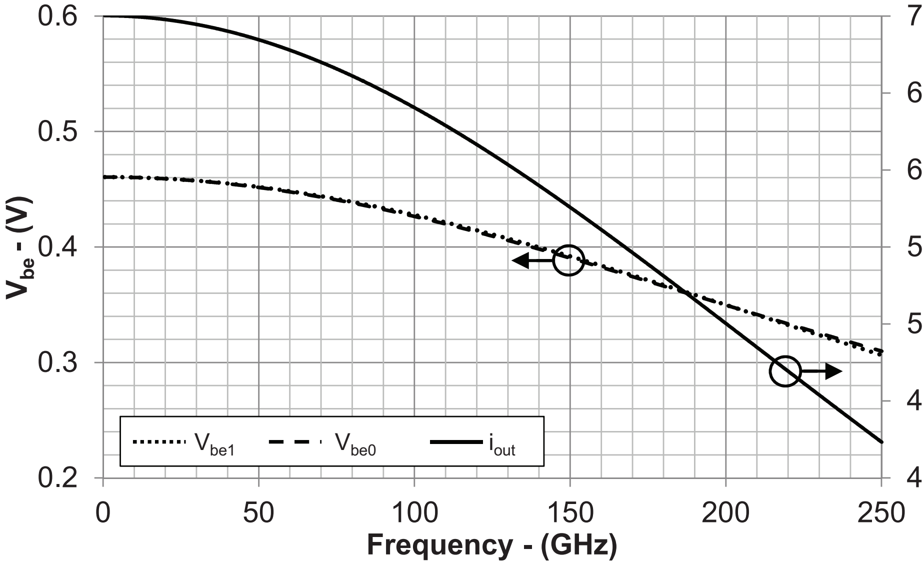
(c)

Figure 3.7: Small-signal circuits for the G_m evaluation of (a) cascode gain-cell, (b) inductively-peaked cascode gain-cell, (c) triple-cascode gain-cell which is presented in this thesis (Fig. 3.5).

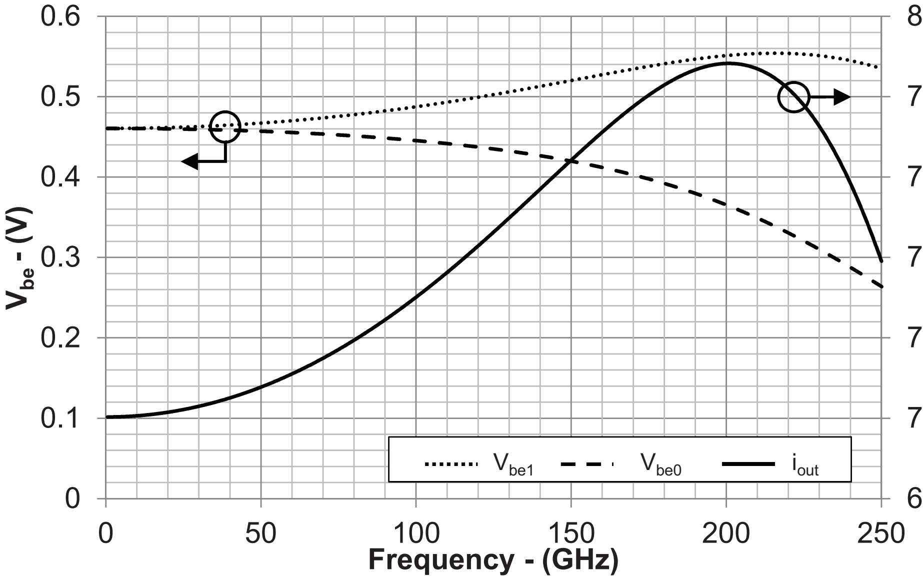
other hand, Fig. 3.8b shows that for an inductively-peaked cascode despite the decrease over the frequency of v_{be0}; v_{be1} and i_{out} have a peaked behavior toward high frequencies, which is due to the inductor L_e. Since these simulations are based on constant input voltages, the peaking in i_{out} directly translates into the peaking of G_m, as Fig. 3.6 shows. Finally, for the proposed gain-cell (Fig. 3.8c), the peaking of i_{out} is further enhanced by the additional common-base stage (Q_2) stacked over the cascode.

The analytic expression of G_m for the inductively-peaked cascode – Fig. 3.7b – is:

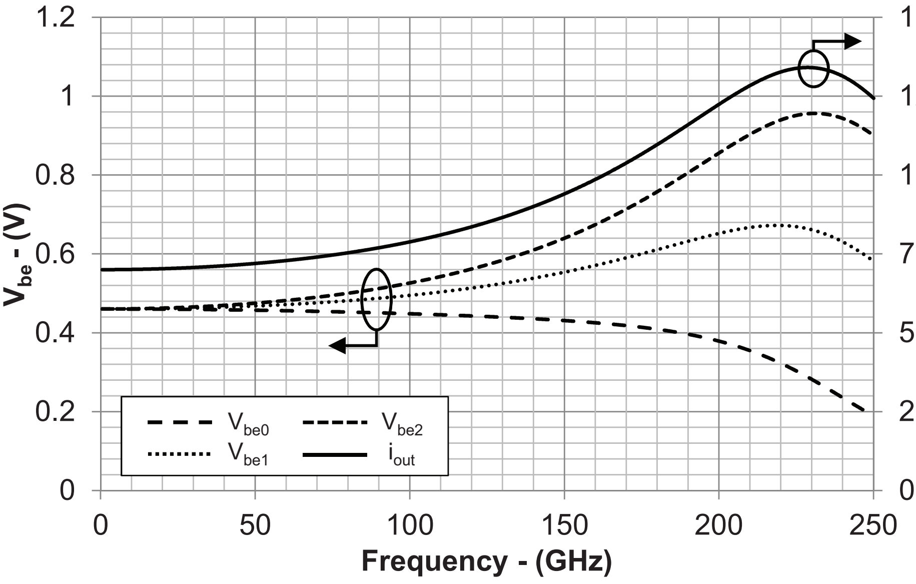
$$G_m = \frac{g_m(g_m - j\omega C_{bc})}{g_m\left[1 - \omega^2 L_e(C_{bc} + C_s)\right] + j\omega\left[C_s + C_{bc} + C_{be} - \omega^2 L_e C_{be}(C_s + C_{bc})\right]} \tag{3.9}$$


0.6
0.5
0.4
0.3
0.2
V_{be} - (V)
70
65
60
55
50
45
40
i_{out} - (mA)
0
50
100
150
200
250
Frequency - (GHz)
V_{be1}
V_{be0}
i_{out}

(a)


0.6
0.5
0.4
0.3
0.2
0.1
0
V_{be} - (V)
80
78
76
74
72
70
68
i_{out} - (mA)
0
50
100
150
200
250
Frequency - (GHz)
V_{be1}
V_{be0}
i_{out}

(b)



(c)

Figure 3.8: Simulated small-signal collector-currents and base-emitter voltages of the circuits of Fig. 3.7: (a) cascode gain-cell, (b) inductively-peaked cascode gain-cell, (c) triple cascode gain-cell proposed in this thesis.

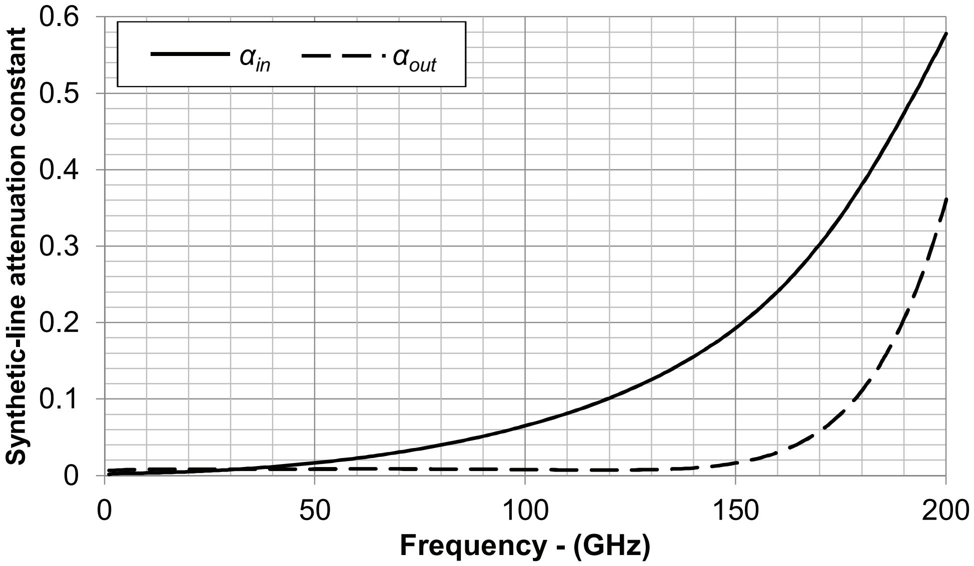


Figure 3.9: Simulated input and output synthetic-line attenuation constant over the frequency of the fabricated TWA.

where the resistances r_{e0}, r_{b0} and r_{b1} are neglected, and the small-signal values of the transistors $Q_0 - Q_1$ are assumed identical, to simplify the analysis into a compact and practical expression. With the same simplifications, the analytic expression of $\mathrm{G_m}$ for the proposed triple-cascode cell – Fig. 3.7c – is:

$$G_m = \frac{g_m^2(g_m - j\omega C_{bc})}{\{g_m\left[1-\omega^2 L_e(C_{bc}+C_s)\right] + j\omega\left[C_s + C_{bc} + C_{be} - \omega^2 L_e C_{be}(C_s + C_{bc})\right]\}^2} \tag{3.10}$$

The derivation of equations (3.9) and (3.10) is given in Appendix I. The circuit analysis confirms that the peaking of the cell transconductance is due to the resonances between the inductors $\mathrm{L_e}$ and the capacitances of the transistors. Furthermore, from the analytic expression of the $\mathrm{G_m}$ of the triple-cascode cell, it is possible to understand that the proposed design achieves the peaking with higher steepness than the inductive-peaking approach since the denominator of eq. (3.10) is elevated at the power of 2 precisely due to the second stacked transistor $\mathrm{Q_2}$.

Besides being compensated by the presented approach, the synthetic-line losses are also minimized making use of already reported techniques. In fact, to improve the frequency response of the TWA, the resistor $\mathrm{R_e}$ and the capacitor $\mathrm{C_e}$ are employed as emitter degeneration [36]. A value of 9 Ω has been chosen for $\mathrm{R_e}$: this is a good compromise to have at the same time low input capacitance without scarifying $\mathrm{G_m}$ excessively, or the power consumption [36]. Moreover, $\mathrm{R_e}$ stabilizes $\mathrm{G_m}$ against process variations. $\mathrm{C_e}$ has been set to 75 fF. This capacitor extends the amplifier bandwidth adding a zero in the system transfer function. Also the capacitive division technique has been used to reduce the losses of the input line [15, 42]: the MIM capacitor $\mathrm{C_b}$ of 75 fF decreases $\mathrm{C_{in}}$, hence α_{in}, at the cost of a slightly lower gain. Fig. 3.9 shows the frequency behaviors of α_{in} and α_{out} for the fabricated TWA, confirming α_{in} as the dominant one. Finally, the emitter area of the transistors $\mathrm{Q_0} - \mathrm{Q_2}$ was chosen of $4\times0.9\times0.07\,\mathrm{\mu m^2}$ to have a good trade-off between gain and dissipated power.

The gain-cell bias point is controlled in current through the 40 kΩ $\mathrm{R_b}$ resistor, while the MIM capacitors $\mathrm{C_1}$ and $\mathrm{C_2}$, respectively of 40 fF and 50 fF, are employed to ac-ground the $\mathrm{Q_1}$ and $\mathrm{Q_2}$ bases. The resistors $\mathrm{R_{s1}}$, $\mathrm{R_{s2}}$, and $\mathrm{R_{s3}}$ are used to ensure the gain-cell stability [43]. These two resistors are decoupled from dc through the MOS capacitors $\mathrm{M_1}$ and $\mathrm{M_2}$.

Transmission Lines Electrically short transmission lines, as the one shown in Fig. 2.17, have been employed to realize lumped inducances and connect the TWA gain cells. All the seven metal layers offered by the process have been used to achieve a characteristic line impedance close to 100 Ω. The width of the signal conductor is 2 µm, while its distance from the side walls is 20 µm. Slots orthogonal to the direction of propagation are applied to the ground conductor. Their width is 0.75 µm, while their relative spacing is 0.25 µm. As demonstrated in [29, 39–41] and discussed in Section 2.2, patterned ground shields reduce the propagation losses, while at the same time increasing the line inductance. Fig. 3.10 shows

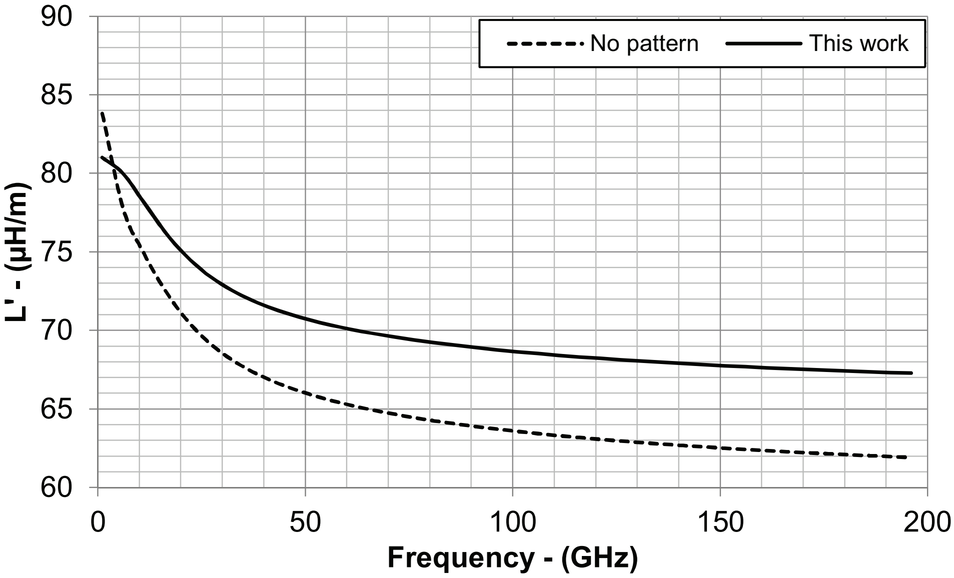


Figure 3.10: Simulated inductances per unit-of-length of conventional microstrip and of the PGS microstrip transmission lines used in this work, for same geometrical dimensions and materials.

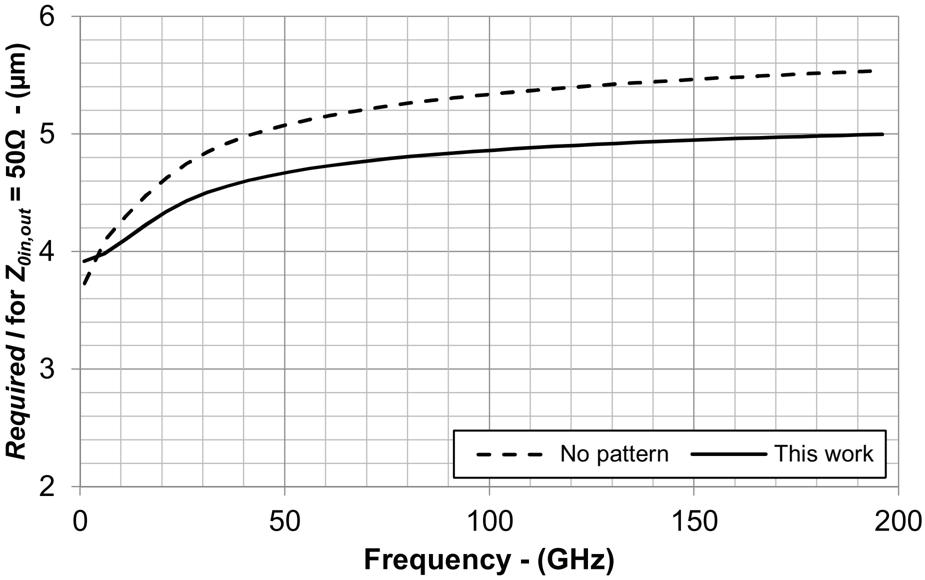


Figure 3.11: Required distance between the gain elements (ℓ) to achieve a synthetic transmission line impedance ($Z_{\mathrm{Sin,out}}$) of 50 Ω, with $C_{\mathrm{in,out}}$ of 1 fF, for conventional microstrip (dashed) and PGS microstrip (solid) transmission lines.

a comparison between the inductances per unit-of-length L' of a conventional microstrip and the PGS which was used in this work. For the same geometrical dimensions and materials, the slots increase L' by 8%. In this way, it is possible to reduce the distance between the gain cells ℓ required for $Z_{\mathrm{Sin,out}}$ of 50 Ω [29].

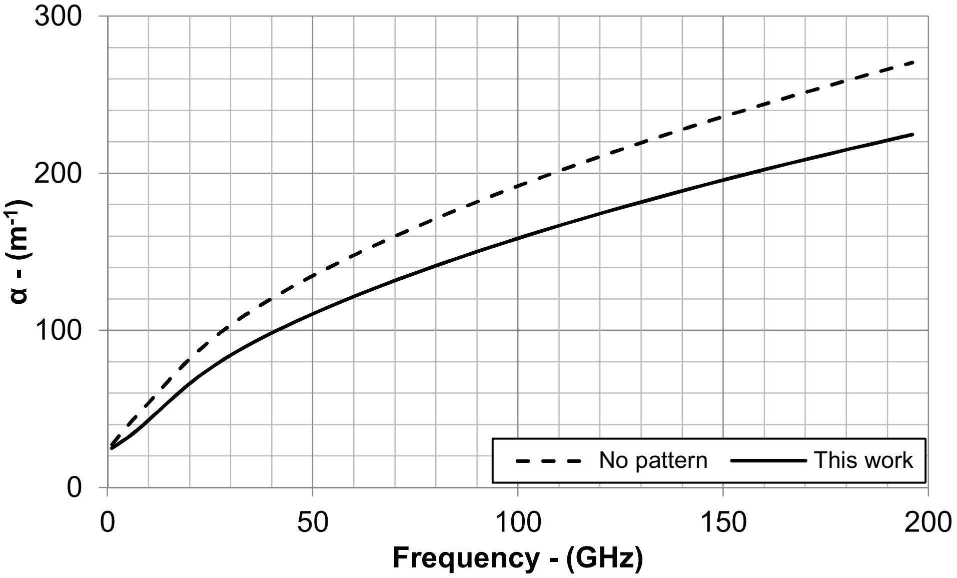


Figure 3.12: Simulated attenuation constant of conventional microstrip (dashed) and PGS microstrip (solid) transmission lines.

From eq. (3.4) and (3.5) the ℓ required for a certain $Z_{\mathrm{Sin,out}}$ is:

$$\ell = \frac{Z^2_{Sin,out} C_{in,out}}{L' - Z^2_{Sin,out} C'} \tag{3.11}$$

Fig. 3.11 shows the needed ℓ for $Z_{\mathrm{Sin,out}}$ of 50 Ω, when C_{in} and C_{out} are set to 1 fF to normalize the comparison: at 150 GHz, the PGS structure requires an ℓ of 4.9 µm, whereas 5.6 µm are needed with the conventional transmission line. This results in a 12.5% decrease of the distance between the cells ℓ, reducing in this way the silicon footprint of the TWA. Moreover, Fig. 3.12 shows that the patterned ground decreases by 17% the propagation losses of the line.

TWA Design Fig. 3.13 presents the schematic of the amplifier, while its microphotograph is shown in Fig. 3.14. The TWA is composed of five gain elements, placed at a distance ℓ of 130 µm, which resulted in a total chip area of 0.38 mm^2.

The main supply voltage V_{CC} is provided through the output of the amplifier with a bias tee. Thanks to the capacitors C_{t}, there is no dc current in the termination resistor R_{t}, and the size and parasitics associated with this resistor are minimized. R_{t} has a value of 50 Ω, and it is fabricated with a silicided gate-polysilicon resistor *Rsil* (Section 2.1). The bias signals V_{base}, V_{cas}, and V_{cas2} reach the gain elements being distributed by blocking caps (Section 2.3.2). Finally, electromagnetic simulations have been used to model transmission lines, interconnections within the gain cells, junctions between lines and termination resistors, and input and output RF pads as described in [44, 45].

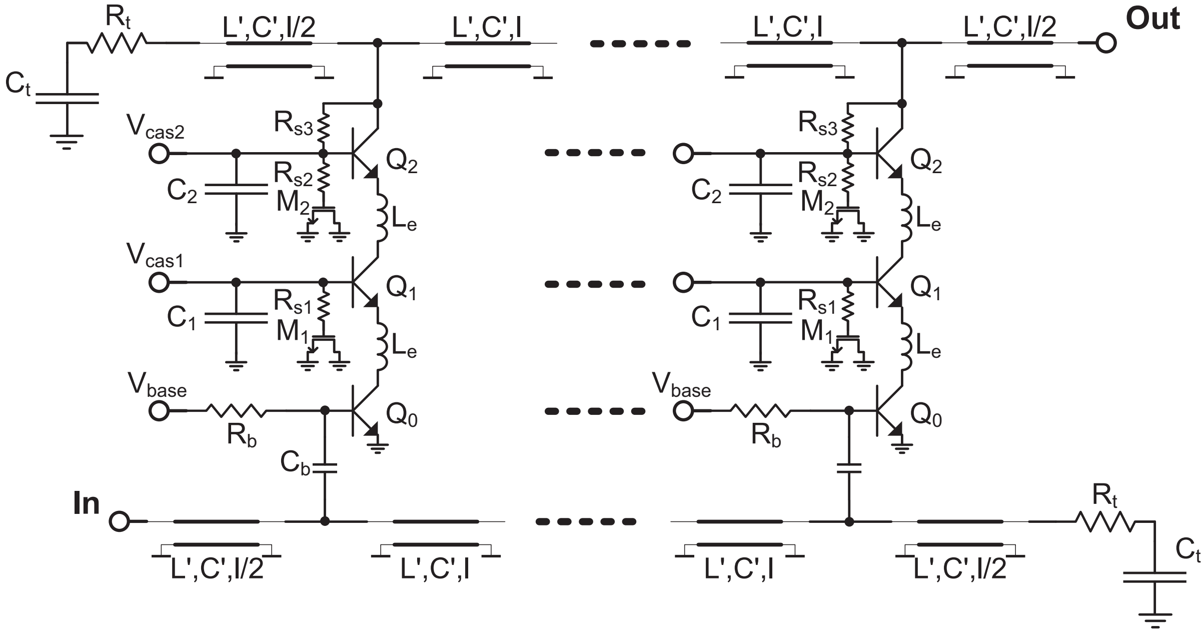

R_t
L',C',l/2
L',C',l
L',C',l
L',C',l/2
Out
C_t
V_cas2
R_s3
Q_2
C_2
R_s2
M_2
L_e
V_cas1
Q_1
C_1
R_s1
M_1
L_e
V_base
R_b
Q_0
C_b
In
L',C',l/2
L',C',l
L',C',l
L',C',l/2
R_t
C_t

Figure 3.13: Circuit schematic of the designed TWA. The blocking capacitors (Section 2.3.2) used to distributed the bias signals V_{base}, V_{cas1} and V_{cas2} are omitted.

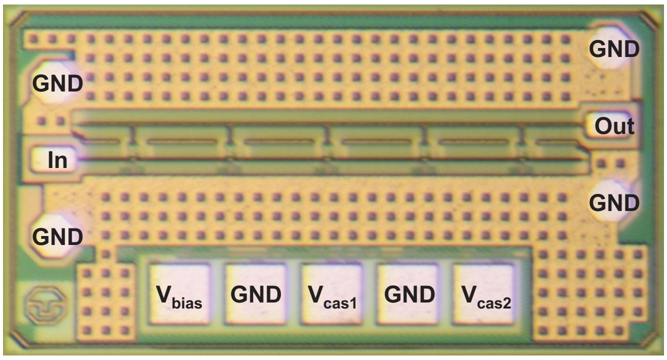

GND
GND
Out
In
GND
GND
V_bias
GND
V_cas1
GND
V_cas2

Figure 3.14: Chip micro-photograph of the fabricated TWA [Testa1]. The chip dimensions are 0.85 mm×0.45 mm, while the chip area is 0.38 mm^2.

3.3.2 Experimental Characterization

The presented novel architecture has been tested with a circuit prototype fabricated in the *SG13G2* technology. As described in Section 2.1, the nominal f_{max} of the process is 450 GHz, but it reduced to 370 GHz in the tolerance corner of the actual fabrication run. The characterization of the amplifier was performed on-chip with wafer probes when the circuit was biased at I_{CC} = 30 mA and V_{CC} = 3.6 V. The pad parasitics have been taken into account during the design through electromagnetic simulations. For this reason, they have not been de-embedded from the measurement results. A Vector Network Analyzer (VNA)

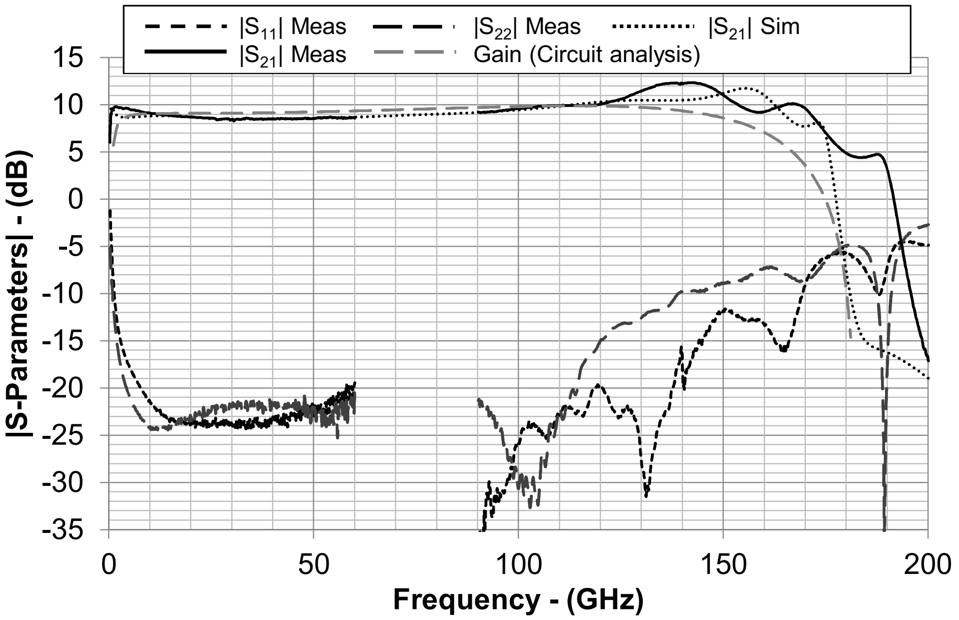


Figure 3.15: Measured S-Parameters magnitude of the TWA in Fig. 3.14, and comparison with its simulated $|S_{21}|$, and power gain as calculated in eq. (3.7) using the simulated values of G_m presented in Fig. 3.6 and of α_{in} in Fig. 3.9.

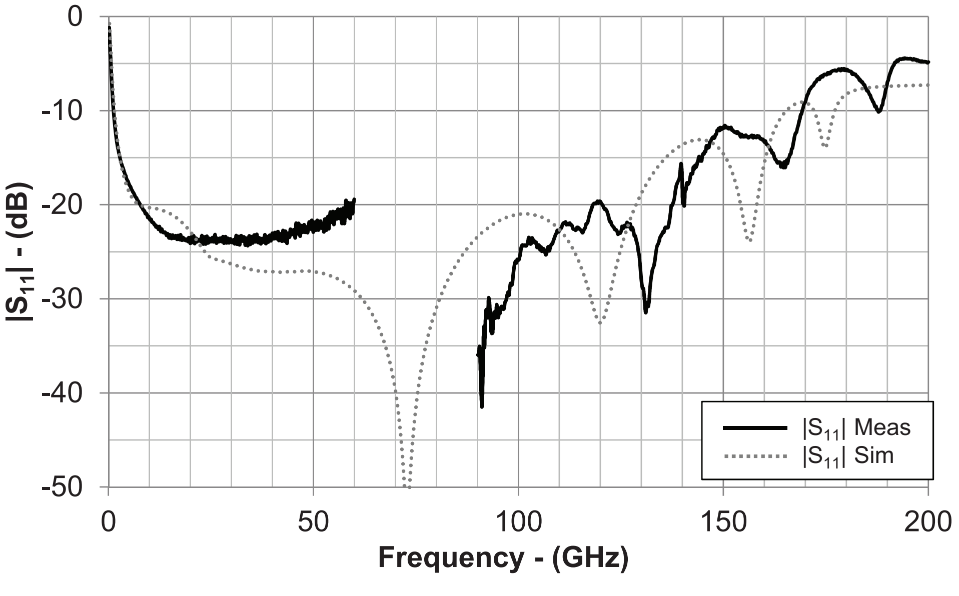


Figure 3.16: Measured and simulated $|S_{11}|$ of the TWA in Fig. 3.14.

has been used to measure the S-Parameters. Three different measurement setups characterized the ultra-wide spectrum of amplification: from 200 MHz to 67 GHz, from 90 GHz to 140 GHz, and from 140 GHz to 220 GHz. All except the first required the use of extender mixer modules, while the absence of experimental results between 67 GHz and 90 GHz is due to the lack of measurement instrumentation for this band at the time of characterization. Fig. 3.15 shows the measured S-Parameters magnitude and the simulated $|S_{21}|$. The amplifier provides an average gain of 10 dB with -3 dB corner frequency at 1 GHz and

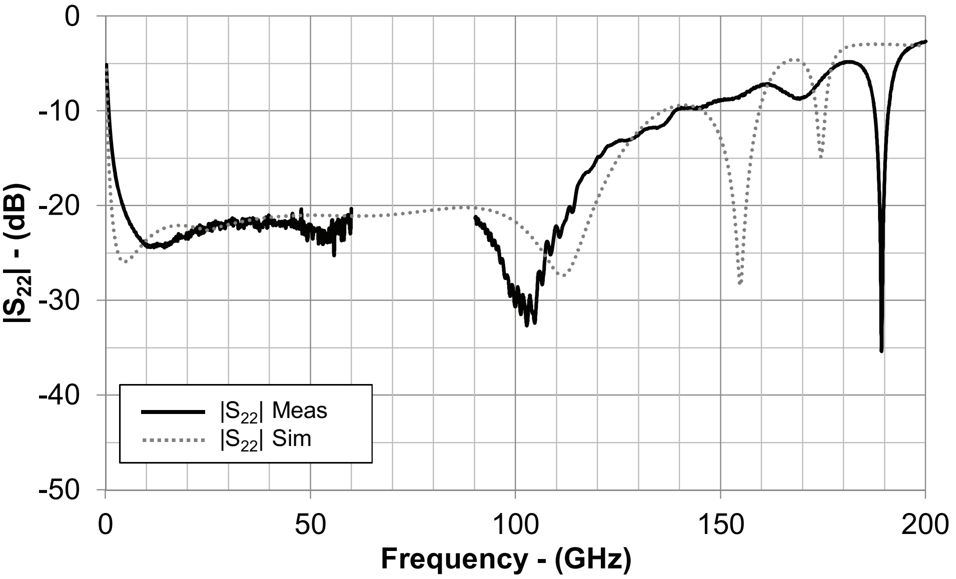


Figure 3.17: Measured and simulated $|S_{22}|$ of the TWA in Fig. 3.14.

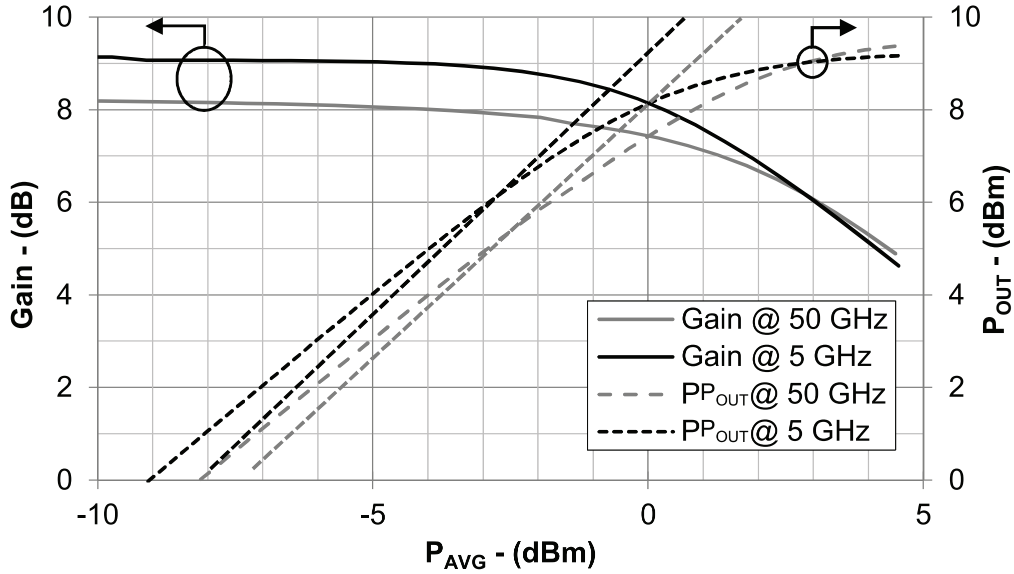


Figure 3.18: Measured gain and output power versus the available generator power, for 5 GHz and 50 GHz of the TWA in Fig. 3.14.

170 GHz. The resulting GBP is 537 GHz. Fig. 3.15 also shows the gain calculated as in eq. (3.7) with the simulated values of G_m and α_{in} presented in Fig. 3.6 and Fig. 3.9, respectively. The absolute value and frequency behavior predict well the measurement results, and this further validates the assumptions made in the circuit analysis of Section 3.3.1.

Fig. 3.16 and 3.17 show the comparison between the measured and simulated return losses. S_{11} and S_{22} magnitudes are below -10 dB and -8 dB over the entire bandwidth of the amplifier. The excellent agreement between measurements and simulations presented in Fig. 3.15, 3.16 and 3.17 validates the employed simulation techniques.

Fig. 3.18 shows the measured power gain and output power plotted versus the

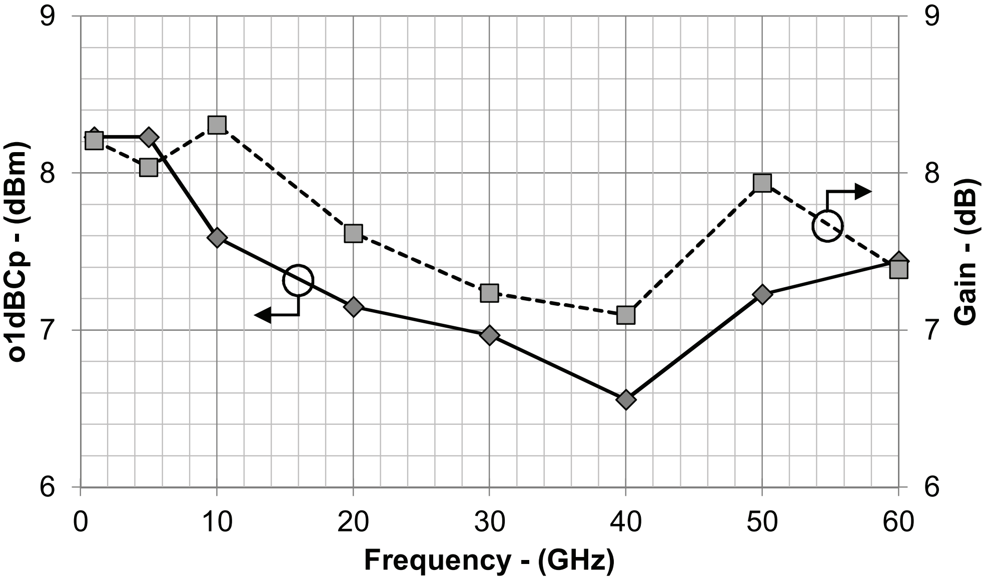


Figure 3.19: Measured o1dBCp and large signal gain (o1dBCp – i1dBCp) over the frequency range 1 GHz – 60 GHz of the TWA in Fig. 3.14.

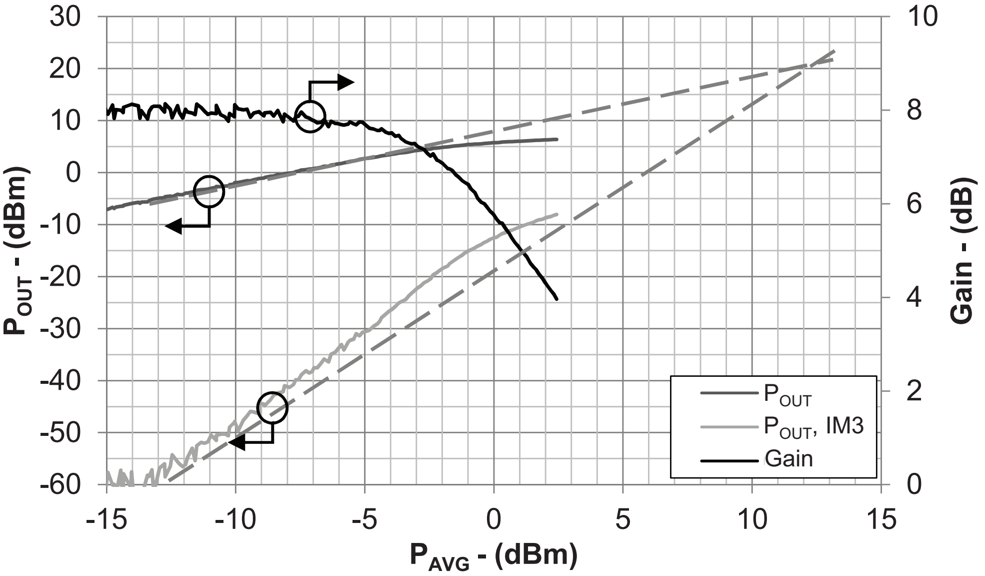


Figure 3.20: Measured third-order intercept point at 30 GHz of the TWA in Fig. 3.14.

available power of the generator P_{AVG} for 5 GHz and 50 GHz, while Fig. 3.19 reports the measured output-referred 1 dB compression point (o1dBCp) and large signal gain, defined as the o1dBCp minus the input-referred 1 dB compression point (i1dBCp), for the frequency range 1 GHz – 60 GHz. The maximum o1dBCp over this band is 8.2 dBm. An additional two-tone test at 30 GHz was also performed and the results are shown in Fig. 3.20. For 30 GHz the measured input-referred third-order intercept point (IIP3) is 13 dBm. The corresponding output-referred third-order intercept point (OIP3) is 20 dBm.

The simulated and measured noise figure (NF) are shown in Fig. 3.21. From 10 GHz to 67 GHz the simulated NF is 6 dB, while for higher frequencies it in-

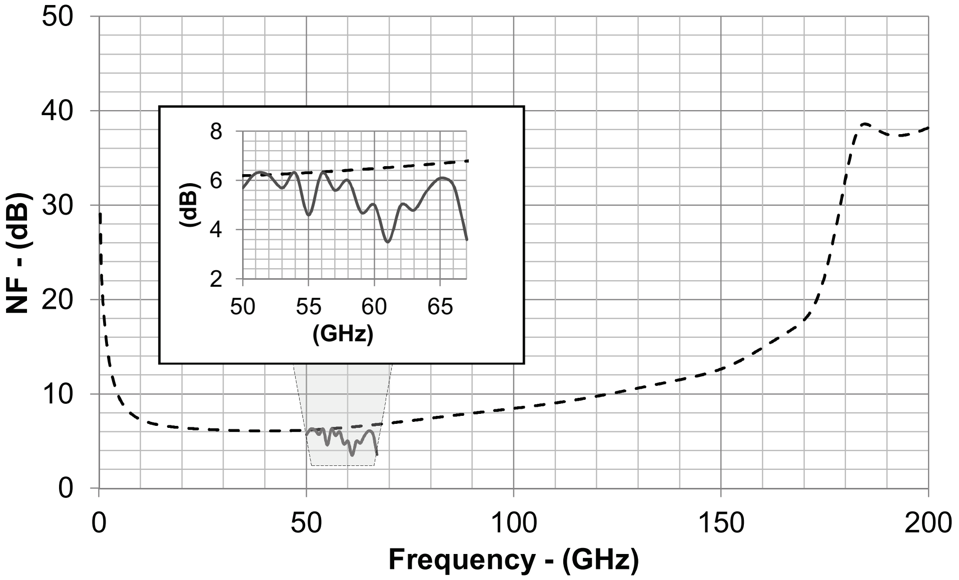


Figure 3.21: Measured and simulated noise figure of the TWA in Fig. 3.14. The inset shows in detail the measured and simulated noise figure from 50 GHz to 65 GHz.

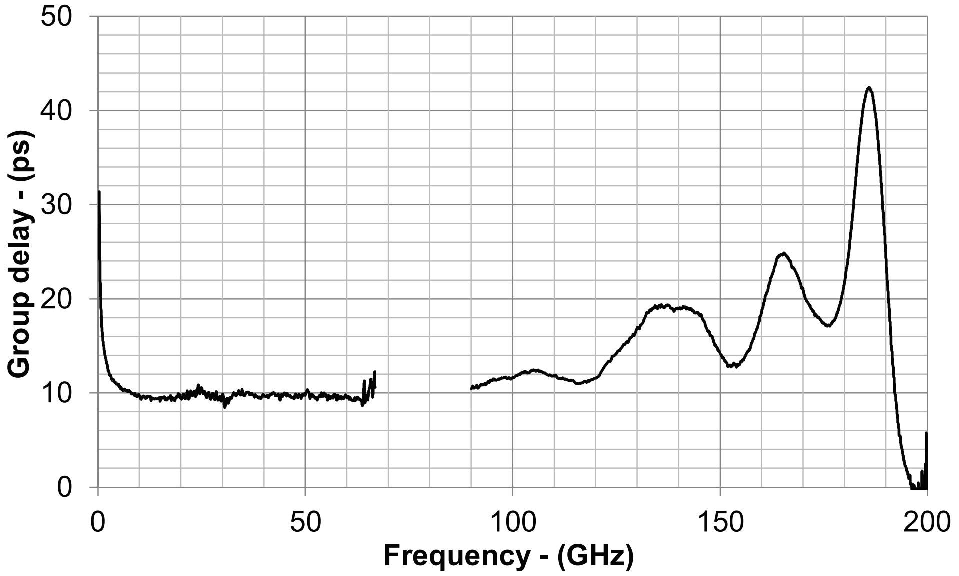


Figure 3.22: Group-delay of the TWA in Fig. 3.14 calculated as in eq. (3.12) from the measured S_{21}.

creases up to 18 dB at 170 GHz. The simulated NF is validated through a comparison with the measurement result in the frequency band from 50 GHz to 67 GHz, where the equipment was available.

Wideband and high-speed communications systems require components with constant group delays. The group delay t_p of the amplifier has been derived from the phase ϕ_{21} of the forward transmission coefficient S_{21} as [46]:

$$t_p = -\frac{d\phi_{21}}{d\omega} \tag{3.12}$$

Table 3.2: State of the art of single-stage TWAs.

FoM	**BW** [GHz]	**Gain** [dB]	**Technology**	**GBP** [GHz]	**Area** [mm^2]	**P$_{\text{DC}}$** [mW]	**o1dBCp** [dBm]	f_{max} [GHz]	**Ref.**
N/A	1-180	5	InP HEMT	320	2.1	N/A	N/A	300	[15]
0.51	5-110	11	50 nm InGaAs HEMT	390	1.68	450	7	500	[46]
0.76	dc-95	21	InP DBHT	1065	2.00	700	16	300	[24]
1.10	dc-120	21	InP DBHT	1346	2.00	610	N/A	370	[25]
1.25	dc-52	10	0.13 µm Si CMOS	164	1.56	84	N/A	N/A	[28]
1.47	4-82	7.8	0.12 µm SOI CMOS	201	1.05	130	10	N/A	[31]
1.70	dc-44	3	0.5 µm AlGaAs HEMT	61.5	1	36	0	70	[47]
2.56	5-73	14	90 nm Si CMOS	370	1.72	84	3	200	[29]
3.74	dc-59	8	90 nm Si CMOS	148	0.3	132	12	150	[30]
9.34	15-110	24	0.13 µm SiGe	1500	0.65	247	16	450	[34]
13.8	1-170	10	0.13 µm SiGe	537	0.38	108	7	340	This work

Fig. 3.22 shows the measurement results. The group-delay variations are less than 10 ps from 5 GHz to 160 GHz and less than 13 ps up to the 170 GHz −3 dB-corner-frequency.

3.3.3 Discussion of the Results

The presented traveling-wave amplifier occupies an area of 0.38 mm^2 and consumes 30 mA from a 3.6 V voltage supply. The circuit provides 10 dB gain over a bandwidth of 170 GHz. This behavior results from the design of the gain cell: a novel topology is introduced to compensate the signal attenuation in the synthetic input line [Testa1].

Table 3.2 presents a comparison with recently-published single-stage TWAs. At expenses of chip area and power consumption (P$_{\text{DC}}$), the gain can be increased using more gain cells. The following Figure of Merit (FoM) can be used to account for this design trade-off and ease the comparison [48]:

$$FoM = \frac{GBP}{Area \times P_{DC}} \quad [\frac{GHz}{mm^2 \cdot mW}] \tag{3.13}$$

The presented design solution achieves the highest GBP per power consumption and area, as well as the highest reported bandwidth for silicon implementations. The performance improvements presented are enabled by the introduction of a crucial circuit-design innovation: the compensation at high frequencies of the synthetic-line losses with a frequency-dependent increase of the gain-cell transconductance.

3.4 Cascaded Single-Stage Distributed Amplifiers (CSSDAs)

In the last decades different solutions have been reported to minimize or compensate the gain-cell losses [Testa1, 15], which, as described in the previous section, are the primary limiting factor toward operation at high frequencies of TWAs. However, the most straightforward approach to minimize the impact of the losses is the reduction of the number of cells, as predicted by eq. (3.7).

The single-cell configuration is, therefore, the one with the frequency response less penalized by the synthetic losses and, thus, the fastest distributed architecture. On the other hand, using just one gain element results in low amplifier gain. Cascading several single-cell DAs [49, 50] achieves gain levels comparable to TWAs, while still reaching the high frequency of operation. Amplifiers with such structure are referred to as Cascaded Single-Stage Distributed Amplifiers (CSSDAs) in literature and by the scientific community [Testa19, Testa21, 23, 26, 27, 32, 51–53]. Fig. 3.23 illustrates their circuit schematic. As it will be shown in next section, and in Appendix II, although only one cell is in use in each CSSDA stage, the concept of distributed amplification is still present since the cell capacitances attached to the transmission lines can be again described with the synthetic-model presented in the introduction of this chapter.

CSSDAs and TWAs have some advantages and disadvantages when compared to each other. As an example, CSSDAs require less power and chip area than TWAs to generate a certain gain since the input signal distribution is different: while all the cells of TWAs receive the same input signal with different phase-delays, in CSSDAs the output of each cell is fed to the input of the following one. For the same reason, CSSDAs are less linear than TWAs, resulting in lower input and output power levels in 1 dB compression of the gain.

A second and more serious drawback of CSSDAs is the poor output matching: this results from features inherent to the circuit topology, which renders the conventional configuration of CSSDAs unmatchable at the upper edge of the frequency band of operation [Testa19, Testa21, 23]. While several implementations of CSSDAs have been demonstrated [Testa19, Testa21, 23, 26, 27, 32, 52, 53], all

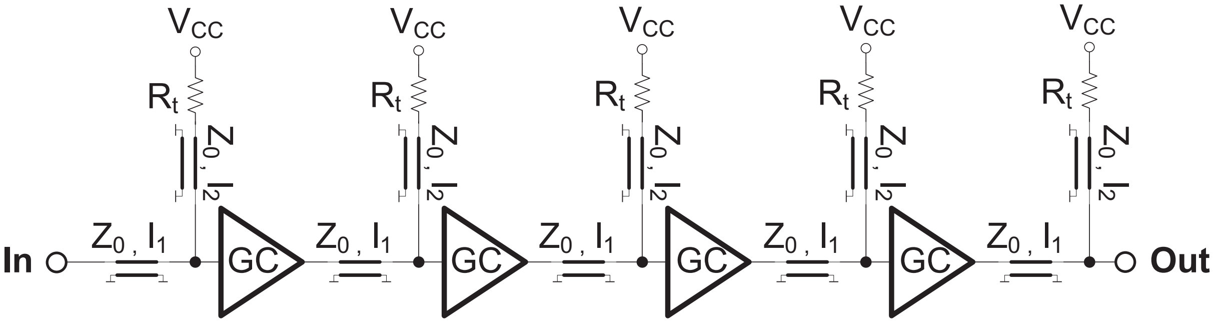


Figure 3.23: CSSDA circuit schematic. The gain-cells are labeled with GC.

of them present poor output-matching at the highest end of their amplification band, ranging from $|S_{22}| = -5\,\mathrm{dB}$ below 100 GHz [26, 27, 32], toward 0 dB for designs above 200 GHz [Testa19, 23]. This effect appears to be associated with the circuit topology, as it is independent of the fabrication technology.

Despite the fundamental principle of operation is well understood, a compact and general expression for the frequency response of the circuit has not been reported so far. In particular, no suitable description of the unmatched behavior at high frequency is available. In this thesis, the first complete circuit analysis for CSSDAs as the function of all key parameters is presented [Testa6]. In particular, the circuit analysis can serve as the design guideline, and it quantitatively explains the typical limitations of the output matching. As the analysis will show, the poor matching toward high frequency is a characteristic of the circuit topology itself. The balanced architecture will be then introduced to retain the frequency response advantages of CSSDAs and yet match the amplifier over the full band of interest.

In detail, a CSSDA optimized for low-power consumption and one for maximum frequency of operation, plus a balanced CSSDA targeting improved input and output matching, have been developed in this thesis. The following sections describe circuit analysis, design, and characterization of these amplifiers.

3.4.1 Circuit Analysis

Fig. 3.23 illustrates the CSSDA schematic. This distributed amplifier consists of a cascade of single-cell DAs, where the capacitances of the gain elements are embedded between transmission lines as in the configuration of Fig. 3.1b. Fig. 3.24 shows the equivalent circuit of the CSSDA obtained with the representation of the cell presented in Fig. 3.4. The input signal propagates into the synthetic line formed by ℓ_1, ℓ_2 and C_{in} as in Fig. 3.1b. ℓ_1 and ℓ_2 are assumed equal. The characteristic impedance of this synthetic line is Z_S, calculated as in eq. (3.1) with $\ell = \ell_1 + \ell_2$. Finally, the line is terminated with the resistor R_t, of the same value as Z_S, to ensure the matching condition. Hence, only forward-propagating waves are present in this CSSDA section.

The CSSDA input-impedance Z_{IN} is thus equal to Z_S, and it is also assumed to be identical to the generator impedance. The input-voltage v_{in} propagates till section A in Fig. 3.24 accumulating a phase-delay of $\beta_S\ell/2$. It is, in fact, possible to model the configuration of Fig. 3.1b as the cascade of two circuits of Fig. 3.1a with half the length and half attached capacitance. The voltage across the input capacitance of the first gain cell v_1, calculated as in [37], is then:

$$v_1 = \frac{v_{\mathrm{in}}}{1 + j\omega R_{\mathrm{in}} C_{\mathrm{in}}} \cdot e^{-\mathrm{j}\beta_S \ell/2} \tag{3.14}$$

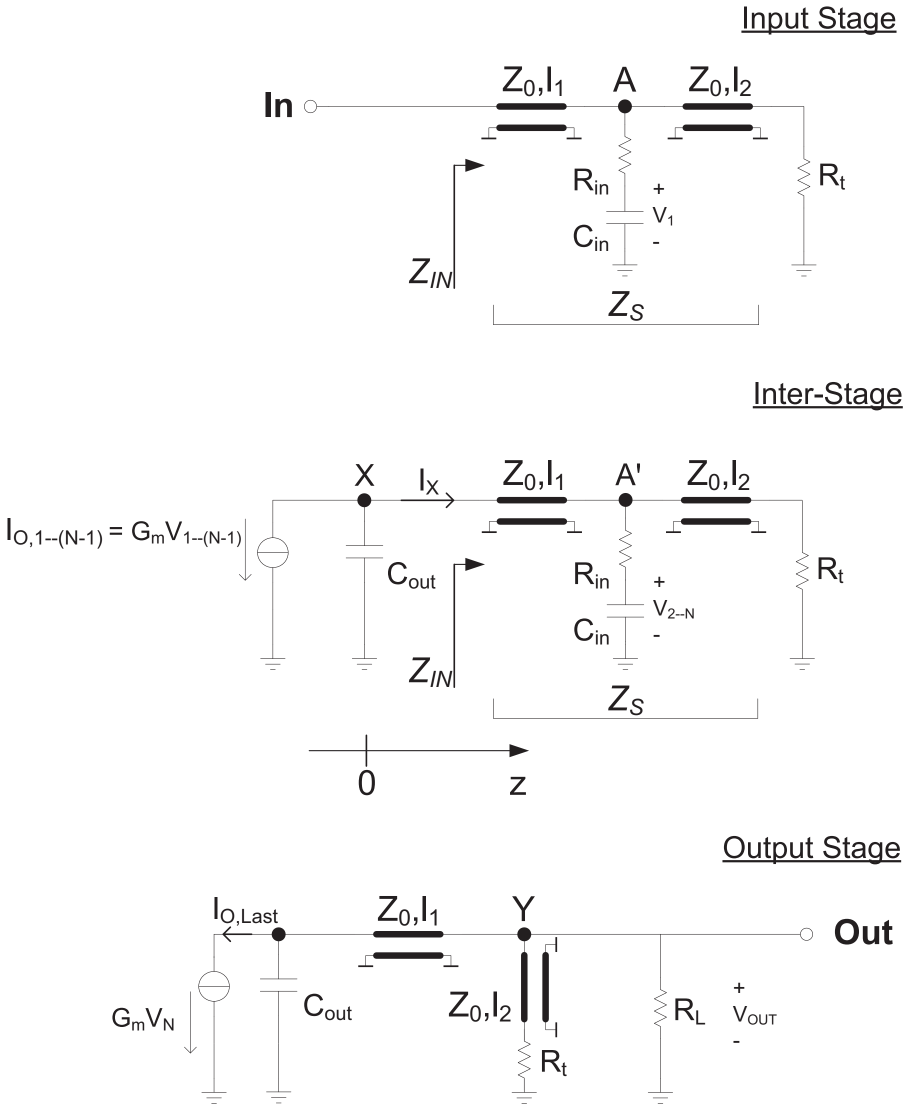

Input Stage
In
Z0,l1
A
Z0,l2
Rin
Cin
+
V1
-
Rt
ZIN
ZS
Inter-Stage
IO,1--(N-1) = GmV1--(N-1)
X
IX
Z0,l1
A'
Z0,l2
Cout
Rin
Cin
+
V2--N
-
Rt
ZIN
ZS
0
z
Output Stage
IO,Last
Z0,l1
Y
Out
GmVN
Cout
Z0,l2
Rt
RL
+
VOUT
-

Figure 3.24: Equivalent small-signal circuit of the CSSDA in Fig. 3.23.

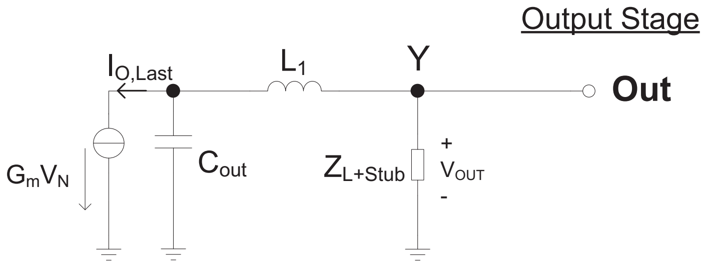

Output Stage
IO,Last
L1
Y
Out
GmVN
Cout
ZL+Stub
+
VOUT
-

Figure 3.25: Equivalent small-signal circuit of the last CSSDAs stage. The line with length ℓ_2 and the resistors R_t and R_L have been replaced with the impedance $Z_{L+\mathrm{Stub}}$, while the line with length ℓ_1 has been approximated with a lumped inductance L_1.

The resulting output-current of the first gain-cell i_{O1} is:

$$i_{\mathrm{O1}} = \frac{G_{\mathrm{m}} v_{\mathrm{in}}}{1 + j\omega R_{\mathrm{in}} C_{\mathrm{in}}} \cdot e^{\text{-j}\beta_{\mathrm{S}}\ell/2} \tag{3.15}$$

Concerning Fig. 3.24, i_{O1} is the input source of the first inter-stage and it is attenuated by the output cell-capacitance $\mathrm{C_{out}}$ placed between node X and ground. The actual input current and voltage of the second stage are i_{X} and v_{X}, which can be expressed as:

$$i_{\mathrm{X}} = \frac{-G_{\mathrm{m}} v_1}{1 + j\omega Z_{\mathrm{IN}} C_{\mathrm{out}}} \quad v_{\mathrm{X}} = i_{\mathrm{X}} \cdot Z_{\mathrm{IN}} \tag{3.16}$$

i_{X} travels in the second stage along the loop consisting of $\mathrm{Z_S}$ and $\mathrm{R_t}$. At section A' it accumulates a phase-delay of $\beta_{\mathrm{S}}\ell/2$, as in the first section. The impedance seen at A' toward $\mathrm{R_t}$ is still $\mathrm{Z_S}$, approximating the circuit of Fig. 3.1b again with two circuits of Fig. 3.1a with half the length and half the attached capacitance. Combining eq. (3.16) with these considerations, for v_1 and v_2 defined as in Fig. 3.24, it follows:

$$v_2 = \frac{-Z_{\mathrm{IN}} G_{\mathrm{m}} v_1}{(1 + j\omega Z_{\mathrm{IN}} C_{\mathrm{out}}) \cdot (1 + j\omega R_{\mathrm{in}} C_{\mathrm{in}})} \cdot e^{\text{-j}\beta_{\mathrm{S}}\ell/2} \tag{3.17}$$

Eq. (3.17) can be generalized as in eq. (3.18) to express the relation between the voltage across the $\mathrm{C_{in}}$ of the $(\mathrm{N}\text{-}1)^{\mathrm{TH}}$ stage, and that across the $\mathrm{C_{in}}$ of the $(\mathrm{N})^{\mathrm{TH}}$ stage.

$$v_{\mathrm{N}} = \frac{Z_{\mathrm{IN}} G_{\mathrm{m}} v_{\text{N-1}} (-1)^{N-1}}{(1 + j\omega Z_{\mathrm{IN}} C_{\mathrm{out}}) \cdot (1 + j\omega R_{\mathrm{in}} C_{\mathrm{in}})} \cdot e^{\text{-j}\beta_{\mathrm{S}}\ell/2} \tag{3.18}$$

The relation between the output current of the last cell $i_{\mathrm{O,Last}}$ and the output voltage v_{out} can be calculated with the equivalent circuit of Fig. 3.25: the impedance $\mathrm{Z_{L+Stub}}$ represents the network consisting of $\mathrm{R_L}$, $\mathrm{R_t}$ and the transmission line of length ℓ_2; while ℓ_1 and ℓ_2 have been replaced with lumped inductances $\mathrm{L_1}$ and $\mathrm{L_2}$ of values $\mathrm{L'} \cdot \ell_1$ and $\mathrm{L'} \cdot \ell_2$, under the assumption that these two lines are small compared to the wavelength of the guided signal. As a result, v_{out} is expressed as:

$$v_{\mathrm{out}} = \frac{-i_{\mathrm{O,Last}} Z_{\mathrm{L+Stub}}}{1 - \omega^2 L_1 C_{\mathrm{out}} + j\omega C_{\mathrm{out}} Z_{\mathrm{L+Stub}}} \tag{3.19}$$

where the impedance $\mathrm{Z_{L+Stub}}$ is:

$$Z_{\mathrm{L+Stub}} = \frac{R_{\mathrm{L}}(R_{\mathrm{t}} + j\omega L_2)}{R_{\mathrm{L}} + R_{\mathrm{t}} + j\omega L_2} \tag{3.20}$$

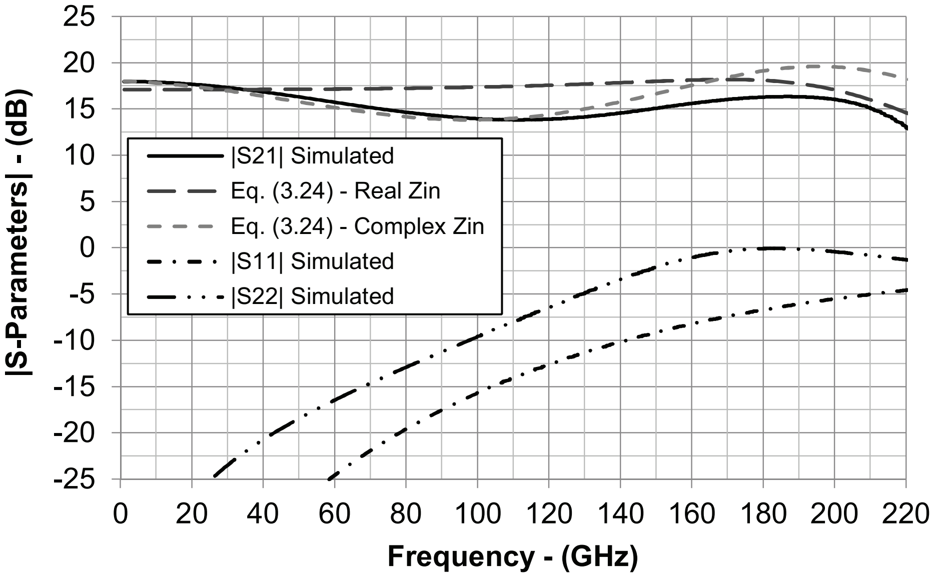


Figure 3.26: Comparison between the CSSDA gain simulated with the circuit in Fig. 3.24 and calculated as in eq. (3.24). The calculated gain is evaluated for the transmission-line and cell parameters gathered in Tab 3.3 and 3.4. Furthermore, the gain is calculated one time using a real value of Z_{IN}, using eq. (3.1) and neglecting thus the loss of the accuracy of the synthetic model toward high frequency; while the second calculation of the gain includes the imaginary part and the frequency variation of the input impedance of the CSSDA using the simulated value of Z_{IN} shown in Fig. 3.28.

Eq. (3.19) can be expressed in a compact form such as:

$$v_{\text{out}} = -i_{\text{O,Last}} \frac{A}{B} \tag{3.21}$$

where A and B are defined as follows:

$$A = R_{\text{L}}(R_{\text{t}} + j\omega L_2) \tag{3.22}$$

$$\begin{aligned} B = R_{\text{L}} + R_{\text{t}} - \omega^2 \left[L_1 C_{\text{out}}(R_{\text{L}} + R_{\text{t}}) + R_{\text{L}} L_2 C_{\text{out}}\right] \\ + j\omega \left[L_2 + C_{\text{out}}(R_{\text{L}} R_{\text{t}} - \omega^2 L_1 L_2)\right] \end{aligned} \tag{3.23}$$

The combination of the equations from (3.14) to (3.23) leads to the *analytic expression of the frequency response of a N-stage CSSDA:*

$$\frac{v_{\text{out}}}{v_{\text{in}}} = \frac{{Z_{\text{IN}}}^{N-1}(-G_{\text{m}})^N e^{\text{-j}\beta_{\text{S}}\ell \text{N}/2}}{(1 + j\omega R_{\text{in}} C_{\text{in}})^N \cdot (1 + j\omega Z_{\text{IN}} C_{\text{out}})^{\text{N-1}}} \cdot A/B \tag{3.24}$$

This expression of the gain is compared in Fig. 3.26 against the circuit simulation of the model in Fig. 3.24, evaluated with the values of the line parameters in Table 3.3, of the gain-cell in Table 3.4, and for R_t and Z_S of 25 Ω. Eq. (3.24)

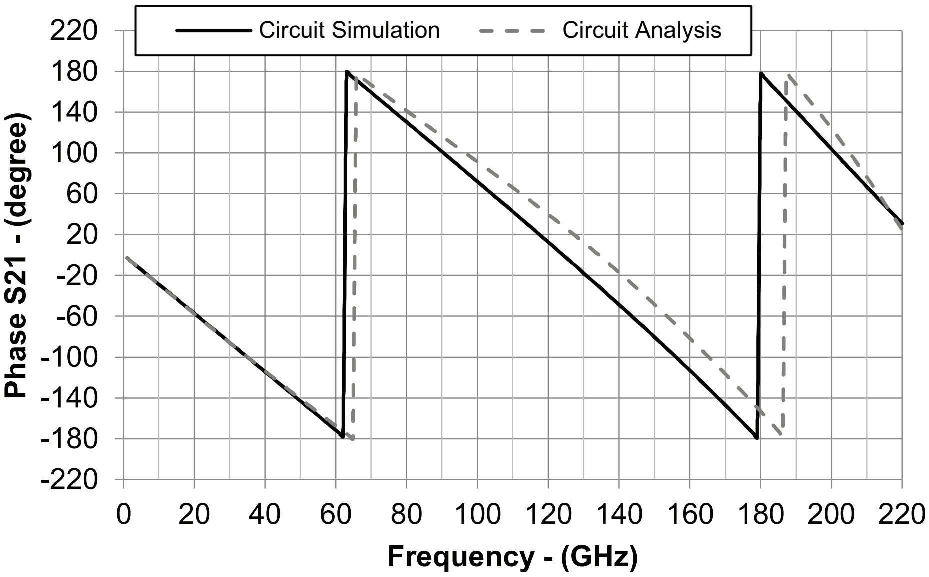


Figure 3.27: Comparison between the simulated CSSDA insertion-phase of the circuit in Fig. 3.24, and its calculation with eq. (3.24) using the transmission-line and cell parameters gathered in Tab 3.3 and 3.4, and Z_{IN} estimated with eq. (3.1).

Table 3.3: Transmission-line parameters of the circuit in Fig. 3.24.

ℓ_1	ℓ_2	L'	C'	Z_0
50 μm	50 μm	0.42 μH/m	92.5 pF/m	65 Ω

Table 3.4: Gain-cells small-signal parameters of the circuit in Fig. 3.24.

C_{in}	C_{out}	R_{in}	R_{out}	G_m
61.5 fF	23 fF	6.7 Ω	0.5 KΩ	80 mS

predicts the gain with good accuracy in the lower and higher part of the spectrum of amplification, while it deviates marginally in the intermediate region. At low frequency, in fact, the synthetic-line model fits with negligible error the line-capacitor circuit of Fig. 3.2b, while it starts to deviate from it for increasing frequency, as it is shown at 100 GHz in the simulation of Fig. 3.26. On the other hand, the error between the circuit simulation and eq. (3.24) reduces toward 200 GHz. The same frequency trend can be seen in Fig. 3.27 where the simulated CSSDA insertion-phase (of the circuit in Fig. 3.24) is compared against the circuit analysis in eq. (3.24). The real and imaginary parts of the CSSDA input-impedance Z_{IN} are plotted in Fig. 3.28. As discussed before, if Z_S is equal to R_t, Z_{IN} is real and equal to them. On the other hand, as Fig. 3.28 shows, since the synthetic model loses accuracy toward high frequency, Z_{IN} decreases in the real part and increases in the imaginary one. Due to the periodic structure of the amplifier, Z_{IN} is also equal to the input impedance of the intermediate stages (Fig. 3.24). Fig. 3.26 shows then the gain re-calculated with eq. (3.24) and taking into consideration the frequency variations and the imaginary part of

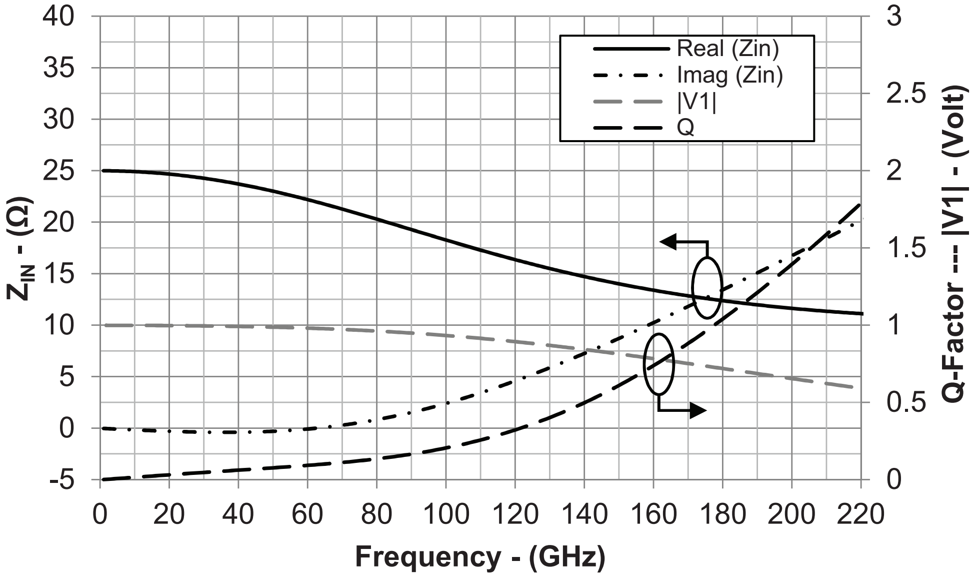


Figure 3.28: Simulated input impedance Z_{IN} and voltage v_1 of the circuit Fig. 3.24.

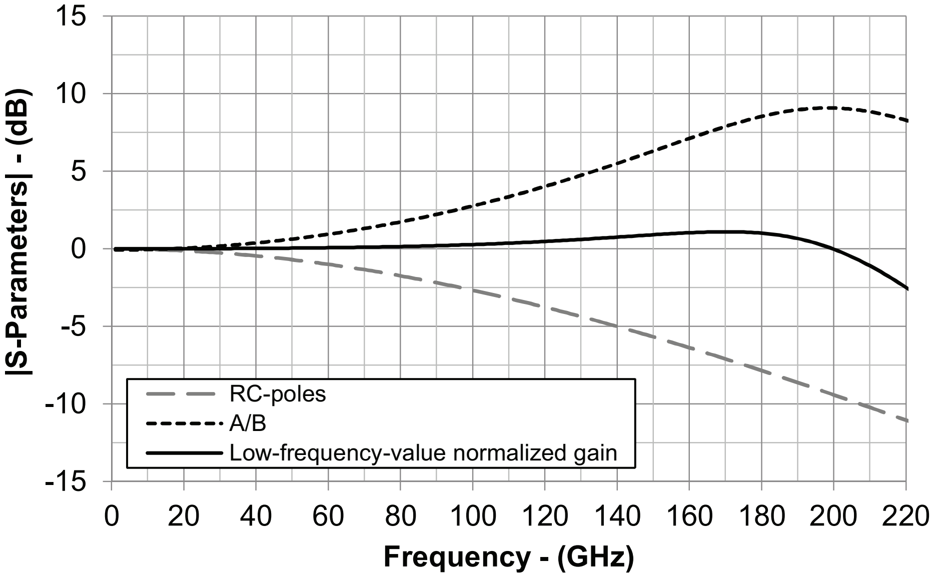


Figure 3.29: Contributions of the terms in eq. (3.24) to CSSDA frequency response.

Z_{IN}. Eq. (3.24) now predicts with better accuracy the circuit simulation, while it deviates only in the upper part of the band due to the approximation of the output transmission lines ℓ_1 and ℓ_2 with lumped inductance L_1 and L_2.

With its close approximation of the complete circuit behavior, eq. (3.24) is a powerful tool for important *considerations on the CSSDA response.* Fig. 3.29 shows the frequency trend of the terms in eq. (3.24). The limiting factors at high frequency are the frequency poles associated with $R_{in} \cdot C_{in}$ and $Z_{IN} \cdot C_{out}$. The gain roll-off for increasing frequency is compensated by the term A/B, which is introduced by the output network. In particular, the inductor L_2 can be approximated as a short at a low frequency of operation. Hence it divides the current $i_{O,Last}$

between R_t and the load. On the contrary, for rising frequency, this inductor offers a large impedance, which directs more and more current to the load rather than in R_t. As it is shown in Fig. 3.29, the CSSDA gain is constant up to the resonance frequency $f_{\text{R-OUT}}$ of the term A/B representing the output network, and it drops past that. $f_{\text{R-OUT}}$ is expressed as:

$$f_{\text{R-OUT}} = \frac{1}{2\pi}\sqrt{\frac{1}{C_{\text{out}}(L_1 + L_2\frac{R_L}{R_L+R_t})}} \tag{3.25}$$

For the presented simulation $f_{\text{R-OUT}}$ occurs at 190 GHz, and it can be used to approximate the -3 dB upper-corner frequency of the amplifier, and its bandwidth. The CSSDA gain-bandwidth product is then expressed as:

$$GBP_{CSSDA} = \left(\frac{P_{DC}}{NV_tVcc}\right)^{2N} \cdot \left(\frac{{Z_{\text{S}}}^N R_{\text{L}}}{Z_{\text{S}} + R_{\text{L}}}\right)^2 \cdot f_{\text{R-OUT}} \tag{3.26}$$

which is obtained assuming $Z_S = R_t$, and substituting G_m with $\frac{P_{DC}}{NV_tV_{CC}}$, where P_{DC} is the dissipated power, V_{CC} the voltage supply and V_t the thermal voltage. Eq. (3.26) shows that the GBP grows with ${P_{\text{DC}}}^{2\text{N}}/N$, where N is the number of cells. This is a crucial advantage with respect to TWAs, where the GBP is proportional to ${P_{\text{DC}}}^2$ [Testa4].

The equivalent CSSDA circuit presented in Fig. 3.24 can be also used for *considerations on the matching.* The resonant network used for gain peaking at high frequency deteriorates the output matching of the amplifier. The output impedance of the CSSDA consists of two admittance connected in parallel: Y_T' from the series of the transmission line with length ℓ_2 and R_t, and Y_{CO}' from the series of the transmission line with length ℓ_1 and C_{out}. The circuit can be simplified again replacing the lines ℓ_1 and ℓ_2 with the equivalent lumped inductors L_1 and L_2. Fig. 3.30 illustrates the equivalent circuit of the output stage. As a result, the output admittance of the circuit is expressed as:

$$Y_{\text{OUT}} = \frac{1 - \omega^2 C_{\text{out}}(L_1 + L_2) + j\omega C_{\text{out}} R_{\text{t}}}{(R_{\text{t}} + j\omega L_2)(1 - \omega^2 C_{\text{out}} L_1)} \tag{3.27}$$

Conjugate matching, $Y_{OUT} = 1/R_L$, can be reached only at low frequency, when the lines are approximated as a short, and C_{out} as an open, and for the special case of $R_t = R_L$. For increasing frequency of operation the line inductance and the C_{out} capacitance gradually deteriorate the matching at the output. Finally, a resonance occurs at $f_{\text{R-OUT}}$ and the output is severely un-matched, as Fig. 3.26 shows around 200 GHz. This behavior is an open problem of the CSSDAs state of the art [Testa19, 23], which can be addressed with the balanced architecture, as it will be shown in Section 3.7. It can be further seen in Fig. 3.26 that also $|S_{11}|$

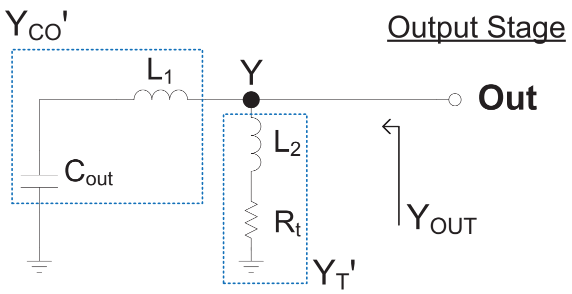


Figure 3.30: Equivalent circuit for the calculation of the CSSDA output impedance. The lines with length ℓ_1 and ℓ_2 have been replaced with equivalent inductors L_1 and L_2.

degrades toward high frequency. As explained in the introduction of this chapter, this is due to the input characteristic synthetic-line impedance which deviates from the values predicted by eq. (3.1) for frequencies of operation approaching the Bragg resonance [30]:

$$f_{\text{Bragg\_Synthetic\_Input}} = \frac{1}{\pi\sqrt{L_{\text{line}}C_{\text{in}}}} \tag{3.28}$$

where L_{line} is the line inductance L' $\cdot(\ell_1+\ell_2)$, while the line capacitance has been neglected with respect to the cell input-capacitance. For the simulation of Fig. 3.26 this occurs at 219 GHz.

In the next sections the presented CSSDA circuit analysis will be used to explain the design of three CSSDAs developed in this work. The first amplifier is optimized for low-power dissipation [Testa21], while the second targets a high −3 dB corner frequency leading to amplification capability up to 250 GHz [Testa19]. Furthermore, to overcome the issue of poor matching at the upper end of the CSSDA amplification band, the balanced architecture is adopted by the third circuit demonstrating a Balanced CSSDA (BCSSDA) [Testa6].

3.5 180 GHz Low-Power CSSDA

According to Moore’s law, the density and speed of integrated circuits have dramatically increased over the last decade. On the other hand, energy storage technologies, required in portable applications, have not yet undergone the same improvements. These two different trends fix the bottleneck of lifetime and speed of portable electronic systems.

Hence, hand in hand with Moore’s law, demanding for and research on low power-design solutions have continuously grown. Moreover, low power consumption is not the only features required for electronics employed in telecommunications and sensing systems. High speeds, high gains, and broad frequency band of operation are also critical design goals that must be reached to create innovative

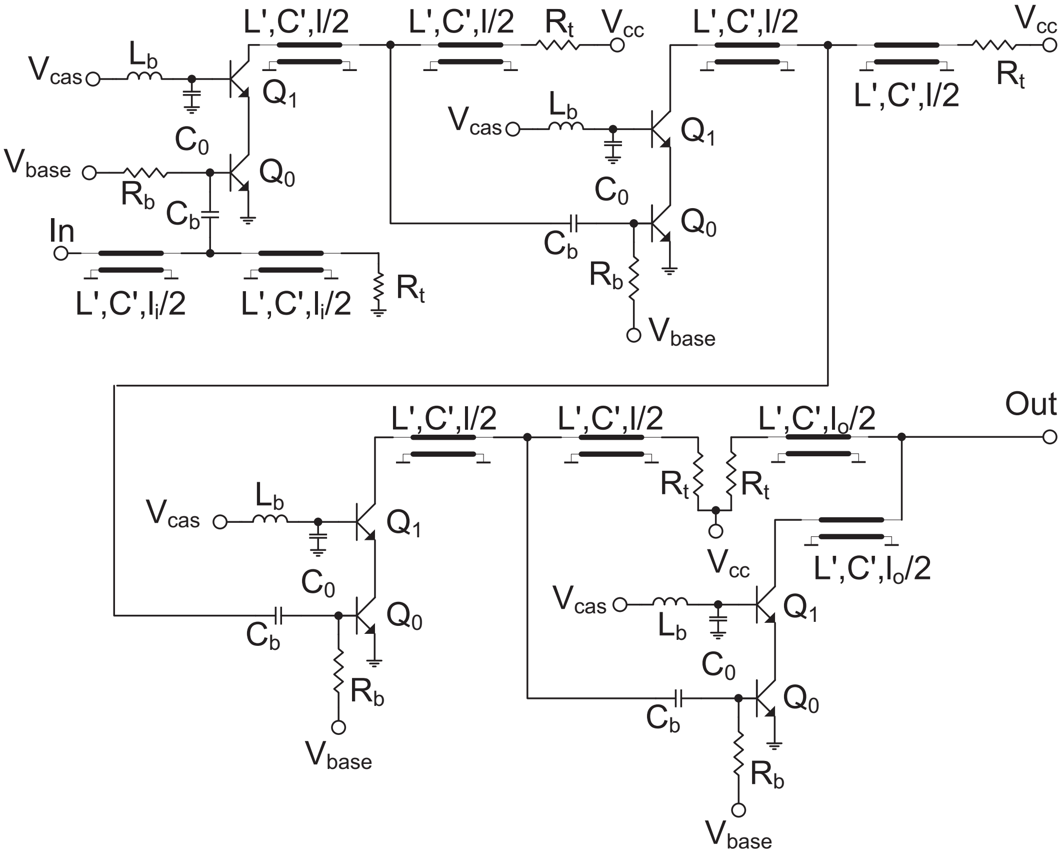

L',C',l/2
L',C',l/2
R_t
V_{cc}
L',C',l/2
V_{cc}
V_{cas}
L_b
Q_1
R_t
L',C',l/2
V_{cas}
L_b
Q_1
C_0
V_{base}
Q_0
R_b
C_b
C_0
Q_0
In
C_b
R_b
L',C',l_i/2
L',C',l_i/2
R_t
V_{base}
L',C',l/2
L',C',l/2
L',C',l_o/2
Out
R_t
R_t
V_{cas}
L_b
Q_1
V_{cc}
L',C',l_o/2
C_0
V_{cas}
Q_1
C_b
Q_0
L_b
C_0
R_b
Q_0
V_{base}
C_b
R_b
V_{base}

Figure 3.31: Circuit schematic of the CSSDA optimized for low power consumption.

systems.

Considering a first-order analysis, the performance of the electronics have to be traded off with the dissipated power, since the gain and speed of transistors are directly dependent on it. Conversely, it is possible to find design solutions that limit the power consumption while maintaining acceptable performance. In fact, this is the case of CSSDAs, where, as shown in the previous section, gain levels comparable to TWAs are achieved using a reduced number of cells and dissipated powers [Testa19, Testa21, 23, 27, 48, 50, 52].

Within this thesis, a CSSDA has been designed for low power consumption and implemented in the *SG13G2* process [Testa21]. In particular, gain and bandwidth of the amplifier have been improved thanks to inductive-peaking techniques. The next sections will present the design of this low-power CSSDA together with the experimental results.

3.5.1 Circuit Design

Fig. 3.31 and 3.32 show the schematic and micro-photograph of the designed CSSDA. The circuit consists of four cells based on an inductively-peaked cas-

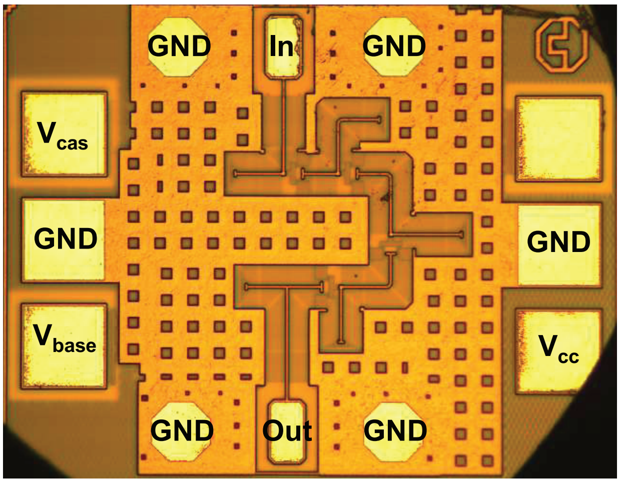


Figure 3.32: Micro-photograph of the CSSDA optimized for low power consumption [Testa21]. The die size is 0.28 mm^2.

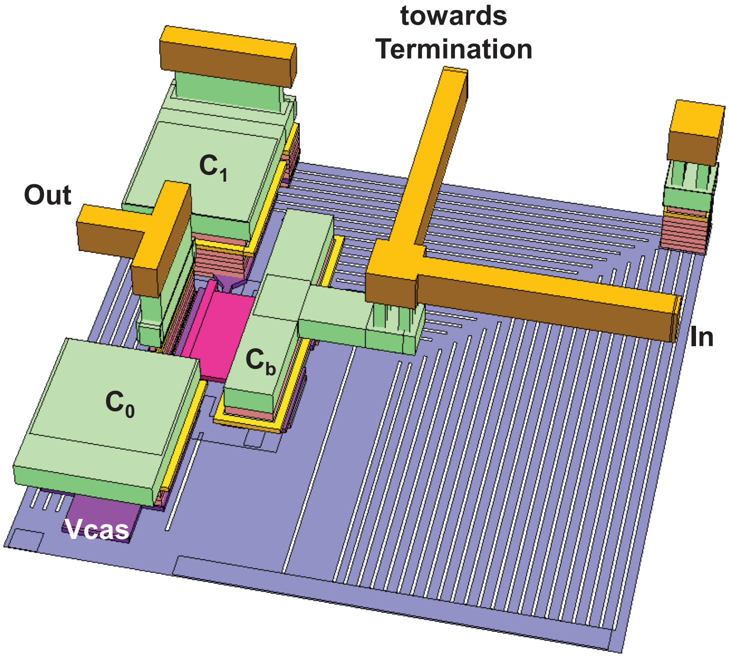


Figure 3.33: 3D view of the cell. One lateral ground-wall has been removed to offer a better view.

code topology. Fig. 3.33 shows their 3D view.

The advantages of cascode cells are listed in Section 3.3.1. Inductive peaking has been used to partially compensate the synthetic losses by boosting the gain-cells transconductances and improve the CSSDA gain and bandwidth, as presented in Section 3.3 and in [Testa1, 47]. The inductor L_b has been employed for the peaking creating positive feedback at the base terminal of the transistor Q_1. The value of L_b is 6 pH, and it is obtained with the parasitic inductance of the interconnections between the blocking caps (Section 2.3.2), used to distribute the bias signal V_{cas}, and the base of Q_1. The discussion of this peaking-technique is presented in detail in [47]. Fig. 3.34 shows the 3D view of the blocking-cap

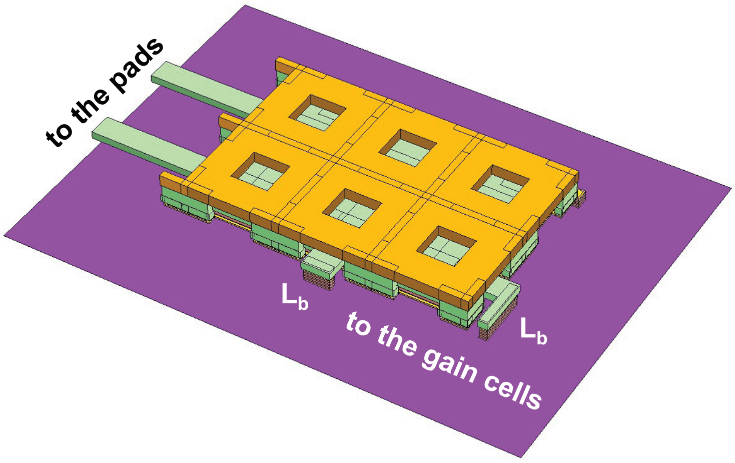


Figure 3.34: Blocking caps in the center of the CSSDA shown in Fig. 3.32. The two metal lines connecting the structure to the pads are used to de-embed the EM simulation, while via pillars from TM_1 to the bottom metal (M_2) realize the L_b inductors.

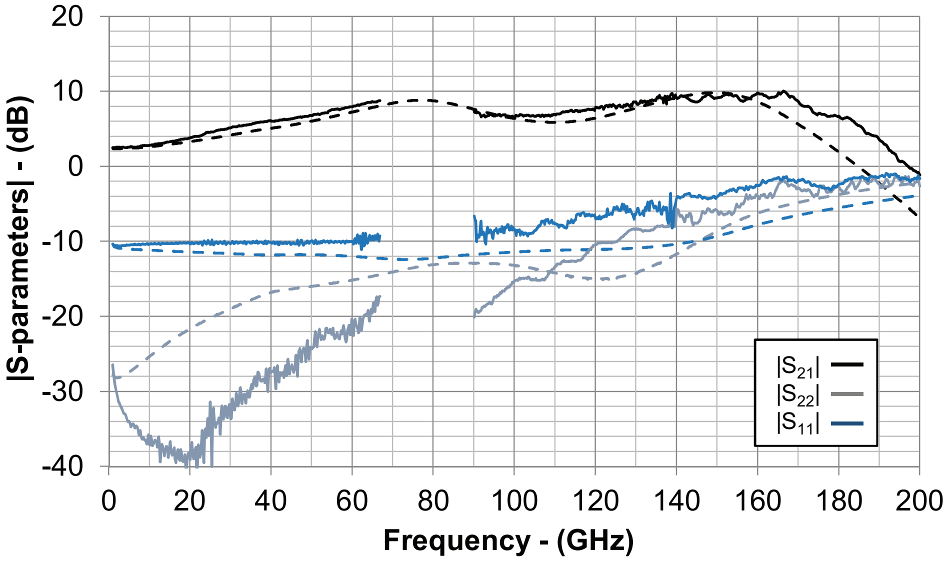


Figure 3.35: Measured (solid) and simulated (dashed) S-Parameters magnitude of the CSSDA in Fig. 3.32, for I_{CC} = 13 mA and V_{CC} = 1.5 V.

array and attached L_b inductors. As it is shown in Fig. 3.32, the gain elements are placed around this grid of capacitors located at the center of the circuit.

Besides being partially compensated, the losses were also minimized with the capacitance-division technique [15, 34]. For this purpose, a capacitor C_b of 125 fF has been placed in series to the base of the transistor Q_0. Finally, the emitter areas of Q_0 and Q_1 were chosen of $5\times0.9\times0.07\,\mu m^2$ to have a good trade-off between gain and dissipated power.

Table 3.5: CSSDAs state of the art.

$\mathbf{P_{DC}}$ [mW]	**Area** [mm^2]	**FoM**	**BW** [GHz]	**Gain** [dB]	**GBP** [GHz]	$f_{\mathbf{UP,3dB}}$ [GHz]	**Technology**	**Ref.**
120	0.72	3.6	70	13	312	70	90 nm CMOS	[52]
90	0.31	28	90	20	800	80	40 nm CMOS	[53]
60	0.36	9.2	25	9	199	25	0.18 µm CMOS	[27]
46	0.54	59	235	16	1480	235	InP DHBT	[23]
74	0.22	46	170	13	760	250	0.13 µm SiGe	CSSDA optimized for High Speed
20	0.28	71	130	10	388	180	0.13 µm SiGe	CSSDA optimized for Low Power

3.5.2 Experimental Characterization

A VNA together with extender modules has been employed to characterize the circuit in the frequency ranges from 200 MHz to 67 GHz, from 90 GHz to 140 GHz, and from 140 GHz to 220 GHz. The S-Parameters measurement for the operation point $I_{CC} = 13\,mA$ and $V_{CC} = 1.5\,V$ are shown in Fig. 3.35. For a power consumption of just 20 mW, the CSSDA provides 10 dB of gain, over a 130 GHz-wide −3 dB frequency-band, which spans from 50 GHz to 180 GHz. The resulting GBP is 388 GHz.

Particular attention has been devoted to the level of V_{cas} to minimize the power consumption. V_{cas} has been set to 1.6 V, which forced the Q_0 collector-emitter bias-voltage V_{CE} to 0.7 V, 0.1 V above the V_{CE} of saturation, while the V_{CE} of Q_1 was 0.8 V. This partition of the V_{CC} ensured an acceptable trade-off between the frequency response of the amplifier and its power consumption.

3.5.3 Discussion of the Results

A CSSDA for low power and wideband applications has been implemented in the *SG13G2* process. The amplifier dissipates just 20 mW and occupies an area of 0.28 mm^2 to provide 10 dB gain over a −3 dB-bandwidth of 130 GHz [Testa21]. The −3 dB upper-corner frequency $f_{UP,3dB}$ is 180 GHz.

Table 3.5 presents a comparison with recently-published CSSDAs in both Silicon and InP technologies. Since the amplifier gain can be increased using more cells at expenses of chip area and power consumption (P_{DC}), the FoM introduced in Section 3.3 is here recalled [48]:

$$FoM = \frac{GBP}{Area \times P_{DC}} \quad [\frac{GHz}{mm^2 \cdot mW}] \tag{3.29}$$

The designed CSSDA achieves the lowest lower power consumption and the highest figure of merit for CSSDA implementations, confirming that the circuit is well suited at the same time for low power, high speed, and broadband applications.

3.6 250 GHz CSSDA

The second CSSDA developed in this thesis targeted high frequencies of operation, demonstrating a response with a −3 dB upper-corner frequency of 250 GHz [Testa19]. The following sections present the design of this amplifier and the achieved experimental results.

3.6.1 Circuit Design

Fig. 3.36 shows the schematic of the CSSDA, while its micro-photograph is illustrated in Fig. 3.37. The circuit consists of four gain cells based on cascode topology, which advantages are listed in Section 3.3.1. Fig. 3.38 presents the 3D view of the structure.

As discussed in Section 3.4.1, the cell input-pole due to $R_{in} \cdot C_{in}$ is one of the factors that limit the CSSDAs operation at high frequencies. The design targeted, therefore, its minimization. A wide transistor Q_0 has been then used to reduce the cell input-resistance R_{in}. The emitter area of the device is $6 \times 0.9 \times 0.07\,\mu m^2$. Indeed, the larger the emitter area, the bigger is the input capacitances of the cells. The C_b capacitor in series with the base of Q_0 the reduced C_{in}, as usually done in the capacitive-division technique [15]. The capacitor C_b dc-decoupled also the gain elements. Its value is 125 fF.

The central sections of the CSSDA have been designed with synthetic characteristic impedance Z_S lower than $50\,\Omega$. This had no impact on the input and output matching, which depends on the Z_S of the first and last sections. In agreement with eq. (3.24), the low value of Z_S in the middle stages minimized the frequency pole due to $Z_{IN} \cdot C_{out}$. In detail, the three intermediate stages have been designed with Z_{IN}, Z_S and R_t of $10\,\Omega$, meanwhile the input and output synthetic lines, as well as $R_{t,1}$ and $R_{t,3}$, are equal to $40\,\Omega$. This value of resistance represents a good compromise between the necessity of matching with the $50\,\Omega$-based measurement setup and the design goal of operation at high frequency. The $25\,k\Omega$ R_b resistor has been used to feed the bias current to the Q_0 base, while the Q_1 base was ac-grounded with the capacitors C_1 and C_2. The supply voltages V_{base}, V_{cas}, and V_{CC} reached the transistors via distribution networks made of blocking caps (Section 2.3.2).

3.6.2 Experimental Characterization

Fig. 3.39 shows the S-Parameters measurements. They were acquired when the circuit was biased at $I_{CC} = 23\,mA$ and $V_{CC} = 3.2\,V$, resulting in 74 mW of power consumption. Due to its ultra-wide frequency band of amplification, four different setups have been employed in the following frequency ranges: from 200 MHz to 67 GHz, from 90 GHz to 140 GHz, from 140 GHz to 220 GHz, and from 220 GHz to 300 GHz. All except the first required the use of extender mixer modules. In

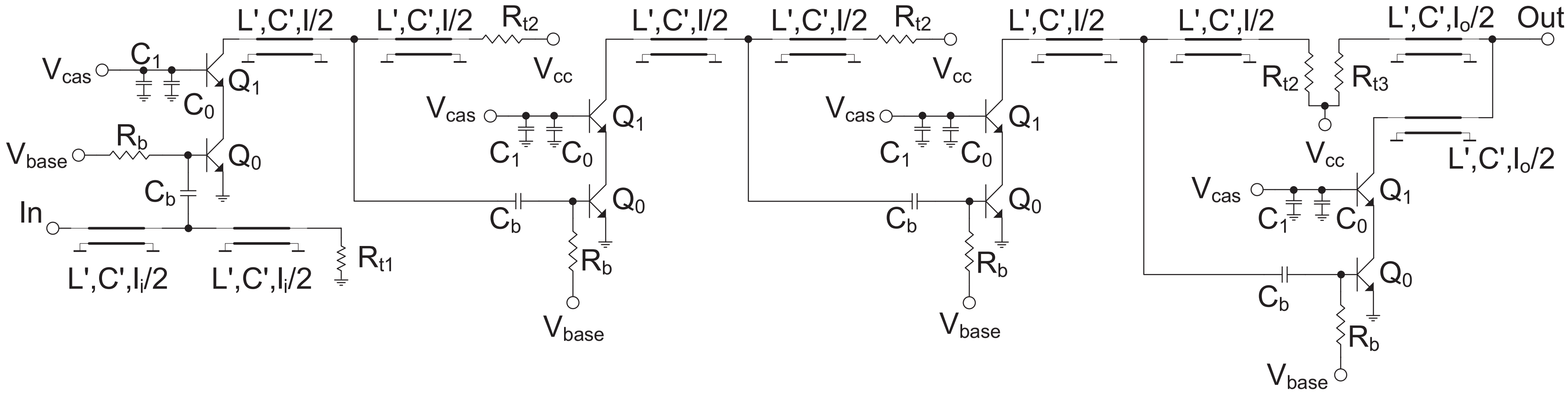

V_cas
C_1
C_0
Q_1
V_base
R_b
Q_0
C_b
In
L',C',l_i/2
L',C',l_i/2
R_t1
L',C',l/2
L',C',l/2
R_t2
V_cc
V_cas
C_1
C_0
Q_1
C_b
Q_0
R_b
V_base
L',C',l/2
L',C',l/2
R_t2
V_cc
V_cas
C_1
C_0
Q_1
C_b
Q_0
R_b
V_base
L',C',l/2
L',C',l/2
R_t2
R_t3
V_cc
V_cas
C_1
C_0
Q_1
C_b
Q_0
R_b
V_base
L',C',l_o/2
L',C',l_o/2
Out

Figure 3.36: Schematic view of the CSSDA optimized for high speed.

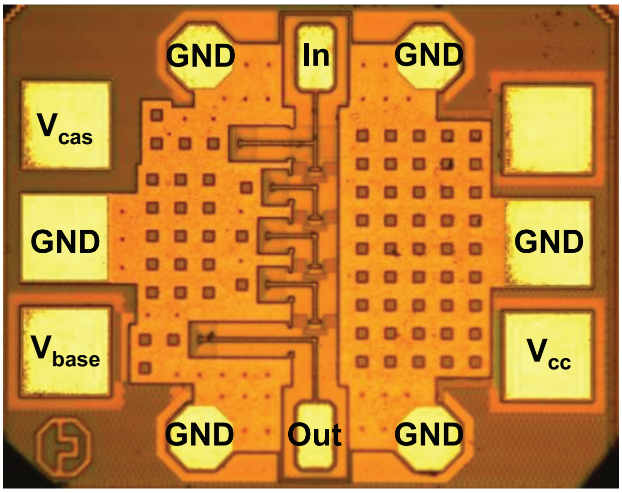

GND
In
GND
V_{cas}
GND
GND
V_{base}
V_{cc}
GND
Out
GND

Figure 3.37: Micro-photograph of the CSSDA optimized for high speed [Testa19]. The die size is 0.23 mm^2.

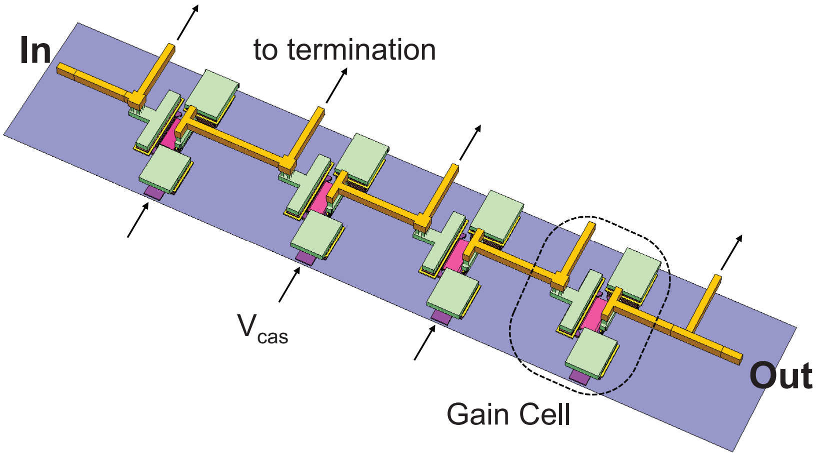

In
to termination
V_{cas}
Gain Cell
Out

Figure 3.38: 3D view of the four gain-cells embedded in the CSSDA of Fig. 3.37.

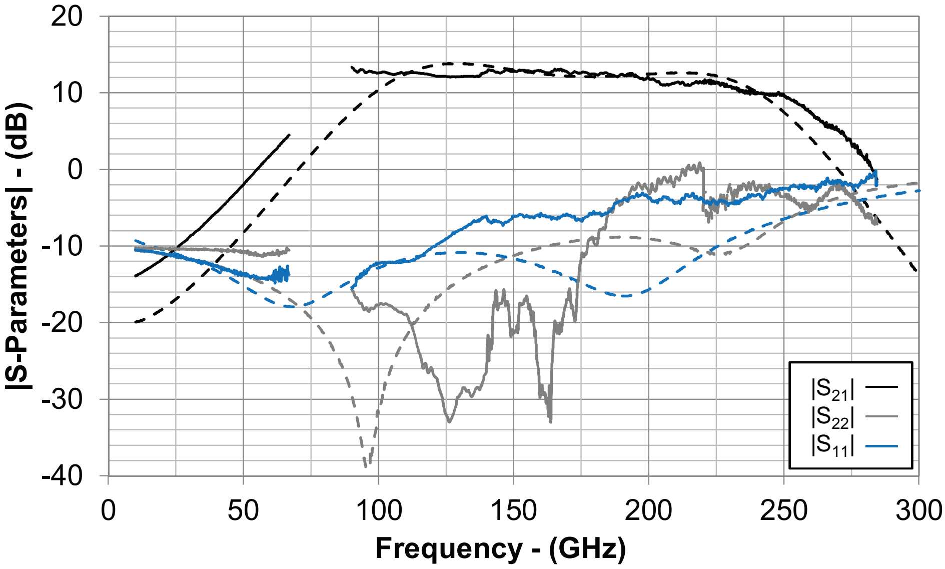


Figure 3.39: Measured (solid) and simulated (dashed) S-Parameters magnitude of the CSSDA in Fig. 3.37 for $I_{CC} = 22\,\text{mA}$ and $V_{CC} = 3.2\,\text{V}$.

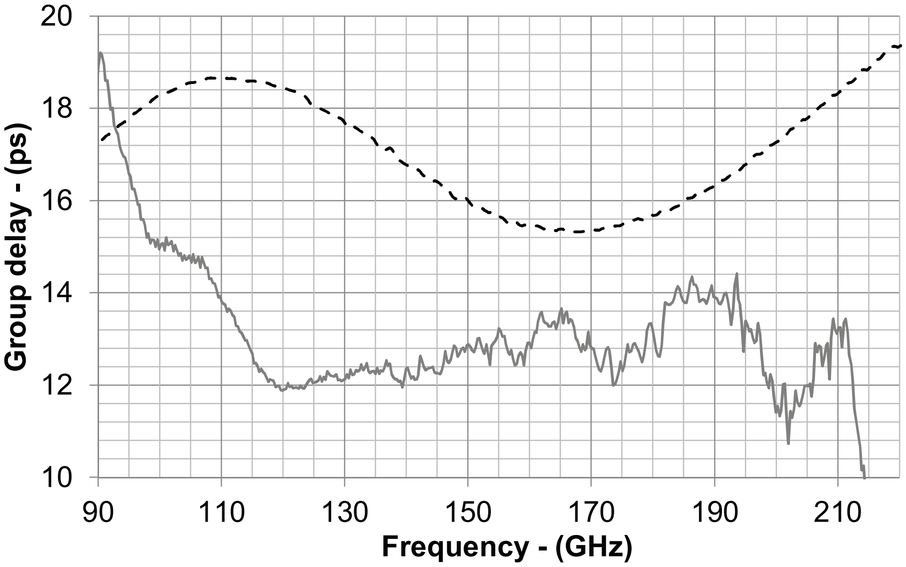


Figure 3.40: Measured (solid) and simulated (dashed) group delay of the CSSDA in Fig. 3.37 for I_{CC} = 22 mA and V_{CC} = 3.2 V.

the selected operation point, the amplifier provides a gain of 13 dB with a −3 dB bandwidth of 160 GHz, which spans from 90 GHz to 250 GHz. The resulting GBP is 715 GHz.

The input and output matching are also shown in Fig. 3.39. The magnitude of the input reflection coefficient is below −6 dB for the whole amplifier bandwidth, whereas $|S_{22}|$ is below −10 dB up to 180 GHz. At higher frequencies, the output matching degrades as predicted by the circuit analysis presented in Section 3.4.1.

Fig. 3.40 shows the measured and simulated group delay. The group delay variations are less than 3.5 ps from 110 GHz to 210 GHz, and less than 6.5 ps from 90 GHz to 210 GHz.

3.6.3 Discussion of the Results

A CSSDA for wideband applications optimized for high-frequency operation has been implemented in the *SG13G2* process [Testa19]. The chip area of the amplifier is 0.23 mm^2, and it requires 74 mW to generate 13 dB gain. The frequency band of operation is 160 GHz wide, while the −3 dB upper-corner frequency is 250 GHz.

Table 3.5 presents a comparison with recently-published CSSDAs in both silicon and indium-phosphate technologies. The CSSDA presented in this work achieves the highest −3 dB upper frequency, the smallest chip-area, and one of the highest GBP normalized to area and power consumption (FoM in eq. (3.29)) for silicon implementations. These improvements result from the set of presented design solutions, which can help to exploit at best the capabilities of the available integrated circuit technology.

3.7 220 GHz Balanced CSSDA

This section presents the third CSSDA developed in this thesis. The amplifier has been optimized for a high degree of input and output matching, which is an open issue in CSSDAs. A balanced architecture has been employed to overcome this limitation. The circuit so formed is here referred to as Balanced CSSDA (BCSSDA) [Testa6]. The following sections will present circuit analysis, design, and experimental characterization of this amplifier.

3.7.1 Analysis and Design

This section is divided into several parts to ease the description of the circuit, focusing on the benefits of the balanced approach, the gain-peaking techniques employed to extend the bandwidth of operation of the BCSSDA, and the gain cell used in this amplifier.

Balanced Approach Fig. 3.41 shows the circuit schematic of the BCSSDA. It consists of input and output on-chip Lange couplers, which enclose two CSSDA modules in a balanced configuration. Four gain-cells, connected via microstrip transmission-lines, form the two CSSDAs.

Good input and output matching are required to maximize power gain and mitigate stability issues. Especially at high frequencies, the optimization of $|S_{11}|$ and $|S_{22}|$ is complicated by the model inaccuracies of the employed devices, and by the process variations. Moreover, as discussed in Section 3.4.1, CSSDAs suffer of poor matching at the higher end of their band. The balanced architecture, achieved with integrated Lange couplers, overcomes these limitations and offers a robust matching to the load and generator impedance.

Fig. 3.42 shows the designed coupler. It splits the power fed at port 1 to ports 2 and 3, inserting a relative phase-shift between them of 90°, while port 4 is isolated and terminated with a matched resistance R_{TC} of $50\,\Omega$. Fig. 3.43 shows the simulated S-Parameters of the component with the port definition of Fig. 3.42. $|S_{31}|$ and $|S_{21}|$ are -3.8 dB at 200 GHz: for this frequency, the coupler divides the power at port 1 in half while inserting 0.8 dB of losses.

The two orthogonal input signals provided by the coupler are applied to the CSSDAs (Fig. 3.41), whose input and output impedances are represented with the reflection coefficients $\Gamma_{IN,CSSDA}$ and $\Gamma_{OUT,CSSDA}$. The waves reflected at their inputs are combined by the coupler, and the total phase shift between the two waves accounts now to two times 90°, hence 180°. This phase difference results in a destructive interference which always matches the input port to the generator impedance. The same mechanism is also exploited at the amplifier output. An ultra-wideband input and output matching, which covers the whole circuit bandwidth, is thus established as it will be later confirmed by the measurement results in Section 3.7.2. The matching, being independent of $\Gamma_{IN,CSSDA}$ and $\Gamma_{OUT,CSSDA}$,

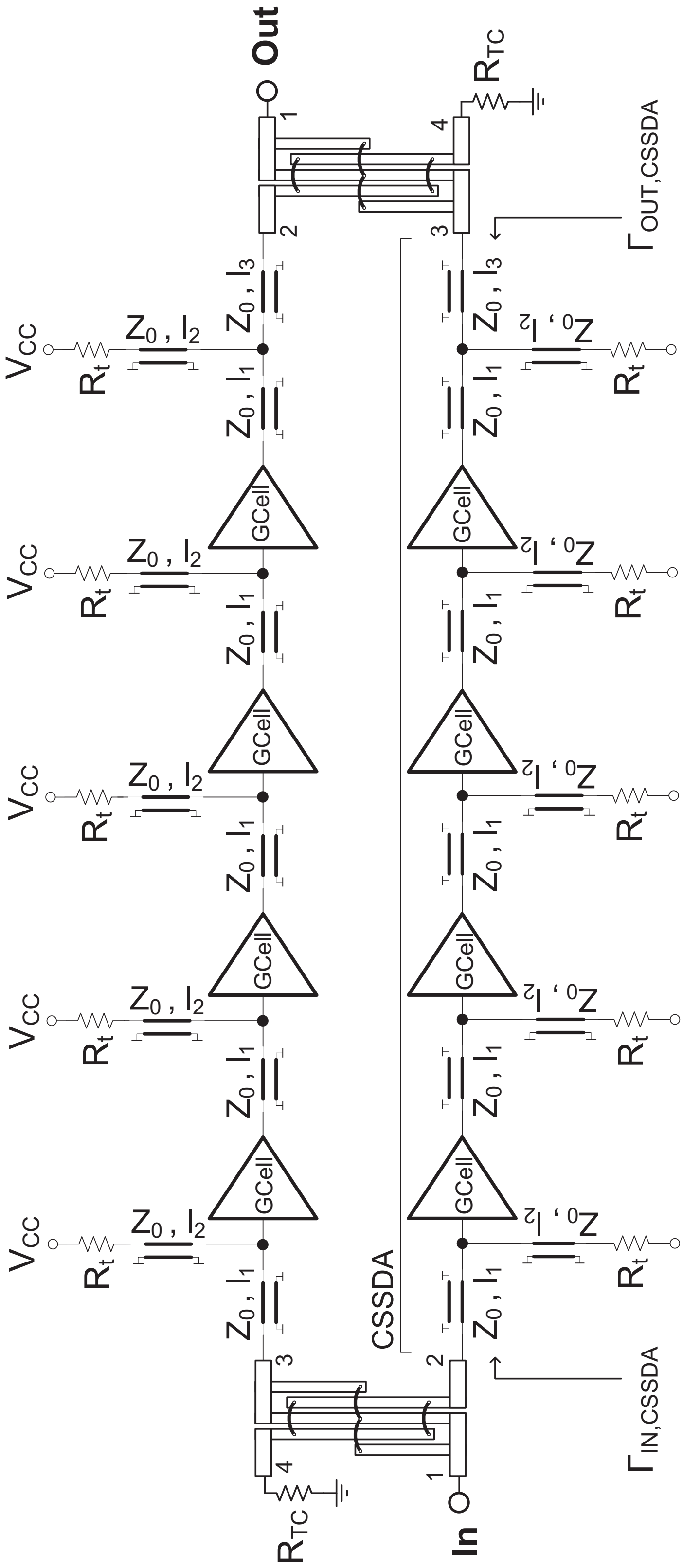

In
Out
R_TC
R_TC
1
2
3
4
1
2
3
4
V_CC
R_t
Z_0 , l_2
Z_0 , l_1
Z_0 , l_3
GCell
CSSDA
Γ_IN,CSSDA
Γ_OUT,CSSDA

Figure 3.41: Circuit schematic of the developed balanced CSSDA.

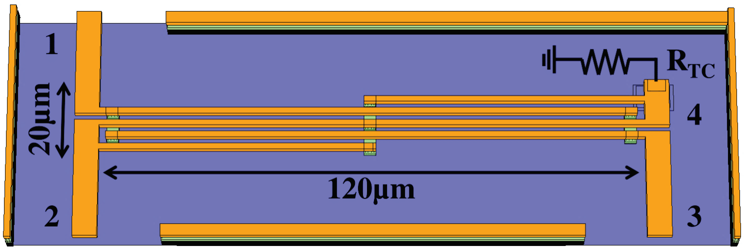


Figure 3.42: 3D view of the Lange coupler used in the circuit of Fig. 3.41 with terminals and physical dimensions annotated. The ground metal plate underneath is realized with the lowest metal of the stack (M1), while the signal conductors with the highest (TM2).

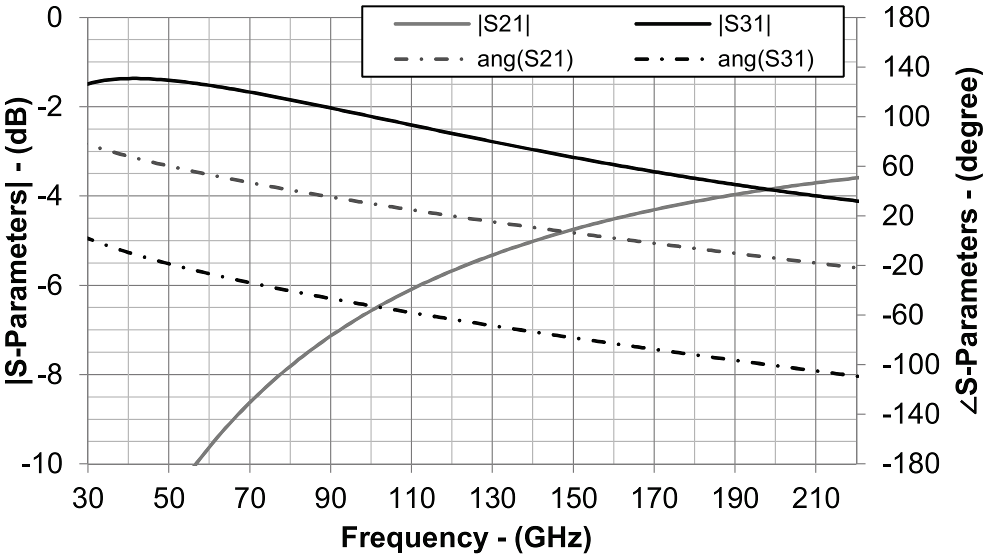


Figure 3.43: Simulated S-Parameters of the Lange coupler used in the BCSSDA.

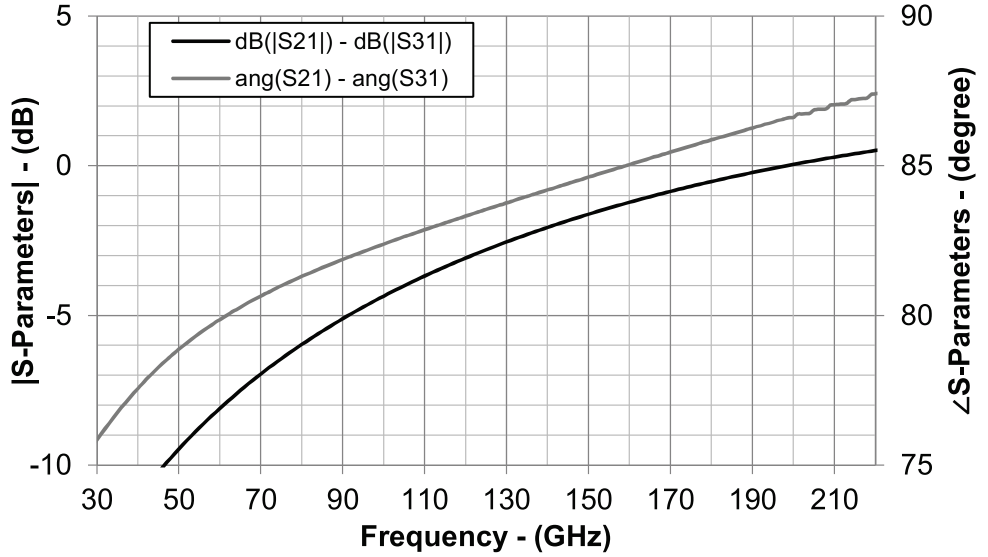


Figure 3.44: Simulated phase and amplitude imbalance of between the paths of the Lange coupler used in the BCSSDA.

is robust against process tolerances, model inaccuracies, and – most importantly – is independent of the output impedance of the CSSDAs. The trade-off between gain and output matching originating from the resonant output network of the amplifier (Section 3.4.1) is thus broken by the solution developed within this thesis [Testa6].

In Fig. 3.43 and Fig. 3.44 it can be seen that toward low frequencies the path from port 1 to 2 suffers from increasing insertion-losses, while the amplitude and phase imbalances between the path responses increase. This trend translates into the fact that the balanced architecture is not able anymore to improve the matching. In this condition, the matching of the system is dominated by the matching of each of the individual CSSDAs, which, as Fig. 3.26 shows, is satisfactory at low frequency: below $-10\,\mathrm{dB}$ for frequencies below 100 GHz. Above 100 GHz the output matching of the CSSDAs gradually deteriorates for increasing frequency, but at the same time, the response imbalance between the coupler paths gradually decreases, improving, in turn, the matching of the balanced CSSDA. This effect results in a $|S_{22}|$ constant over frequency which is achieved tailoring the coupler response to the matching degradation of the stand-alone CSSDAs.

Furthermore, at low frequency, the input-signal propagates mostly from port 1 to 3 of the input coupler (Fig. 3.41), while being highly attenuated at port 3. At the output, since the coupler is now rotated by 180°, the attenuation is on the previous un-attenuated input signal. The couplers are then a limiting factor for wideband operation, considering the CSSDAs capability of amplification from dc up to hundreds of GHz [Testa19, 23]. As it will be shown in the next section, to compensate this effect and extend the bandwidth of the whole amplifier, the CSSDAs have been optimized with a peaking of the gain toward low frequency.

Another essential feature of balanced amplifiers is the improved linearity. In balanced amplifiers, in fact, the input signal is divided between two identical amplifiers (the CSSDA modules in this work) improving by a factor 2 the input linearity. Similarly, the two amplified signals are combined at the output increasing as well by a factor 2 the output linearity. Depending on the actual design, the stand-alone CSSDAs will compress first at the input or the output, but the balanced architecture is beneficial in either case, resulting in an improvement by a factor of 2 for the overall amplifier linearity. Once again this comes at the cost of higher power consumption.

CSSDA Modules The two CSSDAs, which form the presented balanced amplifier, are an evolution of the conventional architecture presented in Section 3.4.1. For these circuits, in fact, two gain-peaking techniques are introduced in the low and high part of the amplifying spectrum.

The *peaking of the gain toward low frequency* is used to fit at best the balanced architecture, compensating the increasing insertion losses of the couplers (Fig. 3.43). To achieve the peaking, the synthetic-line impedance Z_S is designed

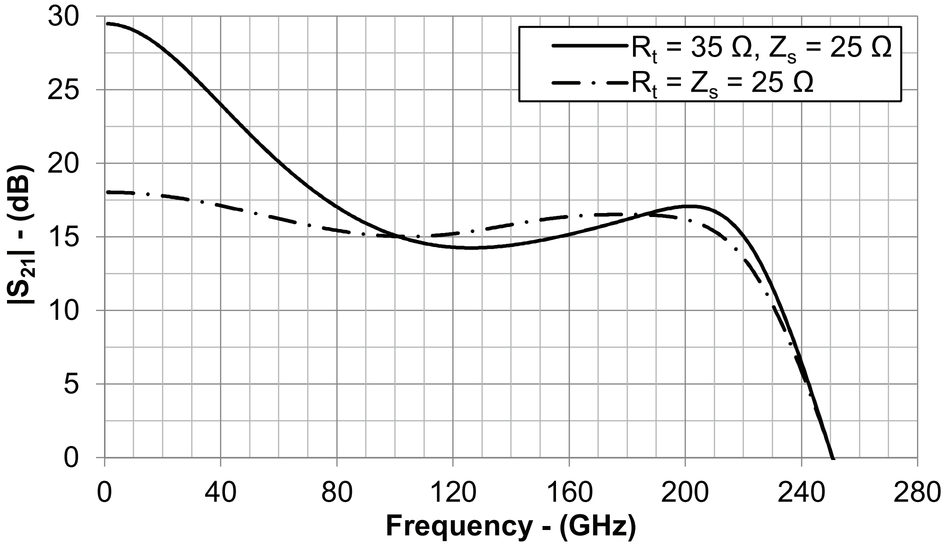


Figure 3.45: Circuit simulation of the CSSDA response for equal and different values of $\mathrm{R_t}$ and $\mathrm{Z_S}$. A gain-peaking toward low frequency has been achieved using $\mathrm{Z_S}$ lower than $\mathrm{R_t}$.

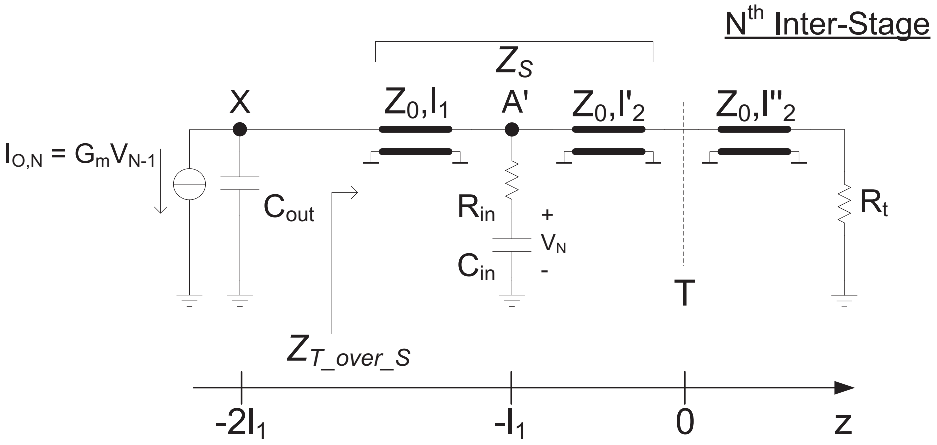


Figure 3.46: Equivalent small-signal circuit of the generic N^{th} stage of a CSSDAs with ℓ_2 longer than ℓ_1. ℓ_2 has been divided into ℓ_2', which is equal to ℓ_1, and ℓ_2'' which is the remaining part.

lower than $\mathrm{R_t}$, as well ℓ_1 is shorter than ℓ_2. The effect over the gain of these design choices is illustrated in Fig. 3.45 against the response of conventional CSSDA.

Fig. 3.46 presents the intermediate $\mathrm{N^{th}}$ section of the CSSDA for this case. The length of ℓ_2 is divided into ℓ_2' equals to ℓ_1, and ℓ_2''. This extra length is in series with the termination resistor $\mathrm{R_t}$, and the two form together the termination-impedance $\mathrm{Z_T}$:

$$Z_{\mathrm{T}} = Z_0 \frac{R_{\mathrm{t}} + jZ_0 \tan\left(\beta_0 \ell_2''\right)}{Z_0 + jR_{\mathrm{t}} \tan\left(\beta_0 \ell_2''\right)} \tag{3.30}$$

Since $\mathrm{Z_T}$ is different from $\mathrm{Z_S}$, the forward-propagating wave will be partially

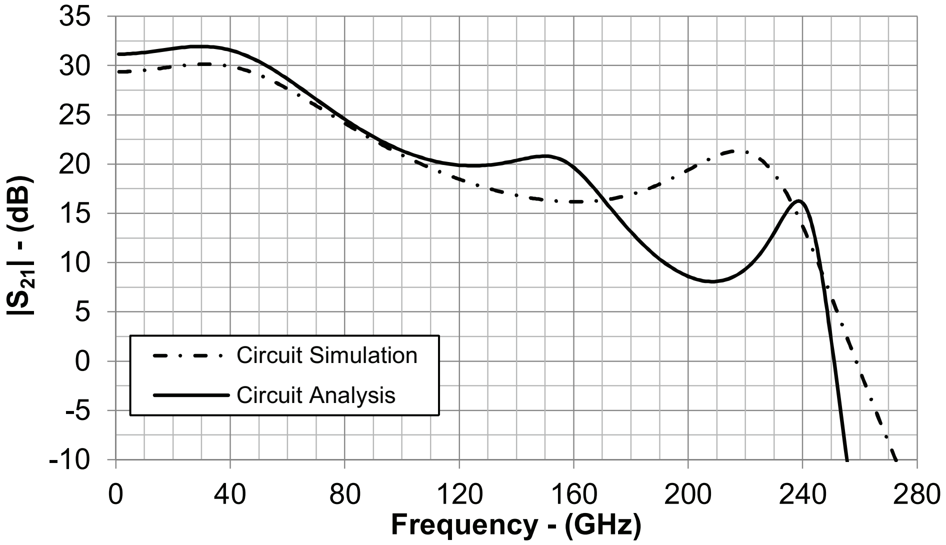


Figure 3.47: Comparison between simulation and circuit analysis (eq. (3.34)) of the CSSDA gain with peaking toward low frequency.

reflected at the interface T. A reflection coefficient Γ_{T} is thus defined:

$$\Gamma_{\mathrm{T}} = \frac{Z_{\mathrm{T}} - Z_{\mathrm{S}}}{Z_{\mathrm{T}} + Z_{\mathrm{S}}} \tag{3.31}$$

The voltage at section A' in Fig. 3.46 is the sum of the waves propagating forward and backward:

$$v_{\mathrm{A}}{}' \;= v_{\mathrm{X}} \cdot D, \quad D = \frac{1 + \Gamma_{\mathrm{T}} e^{-j\beta_{\mathrm{S}} 2\ell_1}}{1 + \Gamma_{\mathrm{T}} e^{-j\beta_{\mathrm{S}} 4\ell_1}} e^{-j\beta_{\mathrm{S}} \ell_1} \tag{3.32}$$

with v_{X} as in eq. (3.16) but with $\mathrm{Z_S}$ replaced by the impedance seen at section X toward the load (Fig. 3.46). This impedance is indicated with $\mathrm{Z_{T\_over\_S}}$ and is equal to:

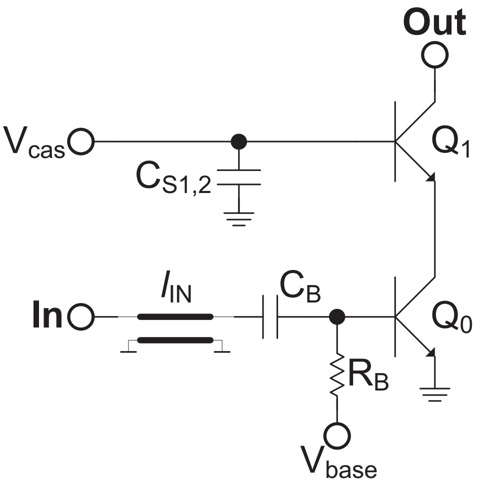
$$Z_{\mathrm{T\_over\_S}} = Z_{\mathrm{s}} \frac{Z_{\mathrm{T}} + jZ_{\mathrm{S}} \tan(2\beta_{\mathrm{S}}\ell_1)}{Z_{\mathrm{S}} + jZ_{\mathrm{T}} \tan(2\beta_{\mathrm{S}}\ell_1)} \tag{3.33}$$

Using eq. (3.32) and (3.33) to modify the circuit analysis presented in Section 3.4.1, the gain can be formulated for the general case of $\mathrm{Z_T} \neq \mathrm{Z_S}$, and $\ell_1 \neq \ell_2$:

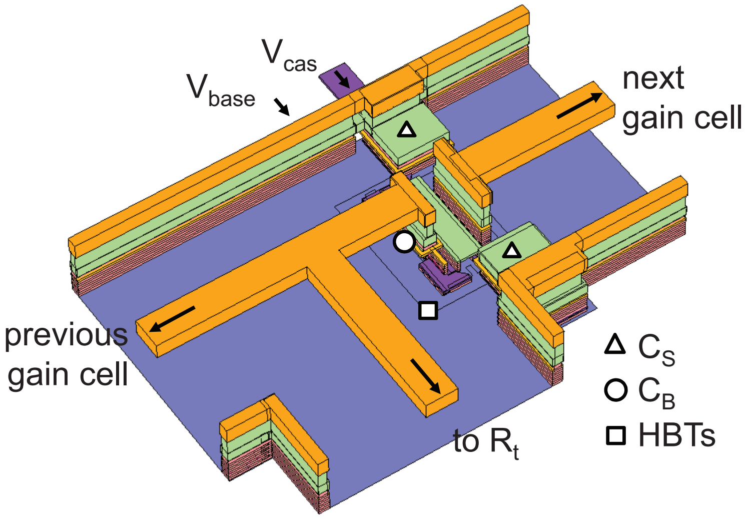
$$|\frac{v_{\mathrm{out}}}{v_{\mathrm{in}}}| = |\frac{(Z_{\mathrm{T\_over\_S}})^{N-1}(-G_{\mathrm{m}} \cdot D)^N}{(1 + j\omega R_{\mathrm{in}} C_{\mathrm{in}})^N \cdot (1 + j\omega Z_{\mathrm{T\_over\_S}} C_{\mathrm{out}})^{\mathrm{N\text{-}1}}} \cdot \frac{A}{B}| \tag{3.34}$$

with A and B as in (3.22) and (3.23) but with $\mathrm{Z_T}$ in place of $\mathrm{R_t}$, and $\mathrm{Z_S}$ replaced by $\mathrm{Z_{T\_over\_S}}$.

The comparison between circuit simulation and eq. (3.34) is shown in Fig. 3.47 for the actual design values of $\ell_1 = 50\,\mu\mathrm{m}$, $\ell_2 = 170\,\mu\mathrm{m}$ and $\mathrm{R_t} = 35\,\Omega$. The presented analysis fits in the low part of the spectrum, while it deviates from the simulation for increasing frequency of operation where the synthetic-line model



(a)



(b)

Figure 3.48: (a) Schematic and (b) 3D view of the gain cells used in the BCSSDA.

loses accuracy. In particular, the gain of the CSSDA is, in this case, more dependent upon Z_S than respect the case $Z_T = Z_S$. This is formalized in eq. (3.34) by the term D, which is dependent on Z_S and elevated to the power of N. This term reduces to 1 if $Z_T = Z_S$ (eq. (3.24)).

The peaking of the gain toward high frequency targeted to extend further the bandwidth of operation of the system. The peaking has been achieved with the line-segment ℓ_{IN} placed at the input of the cell, as shown in Fig. 3.48. The length of this line is 15 µm, which is short compared to the signal wavelength, and it can be replaced with an equivalent inductor of 6.3 pH. This value is calculated as the product between the line length and its inductance per unit-of-length. ℓ_{IN} boosts the equivalent gain-cell transconductances for increasing frequency, which results in the peaking of the amplifier gain. The resulting effect is shown in Fig. 3.49

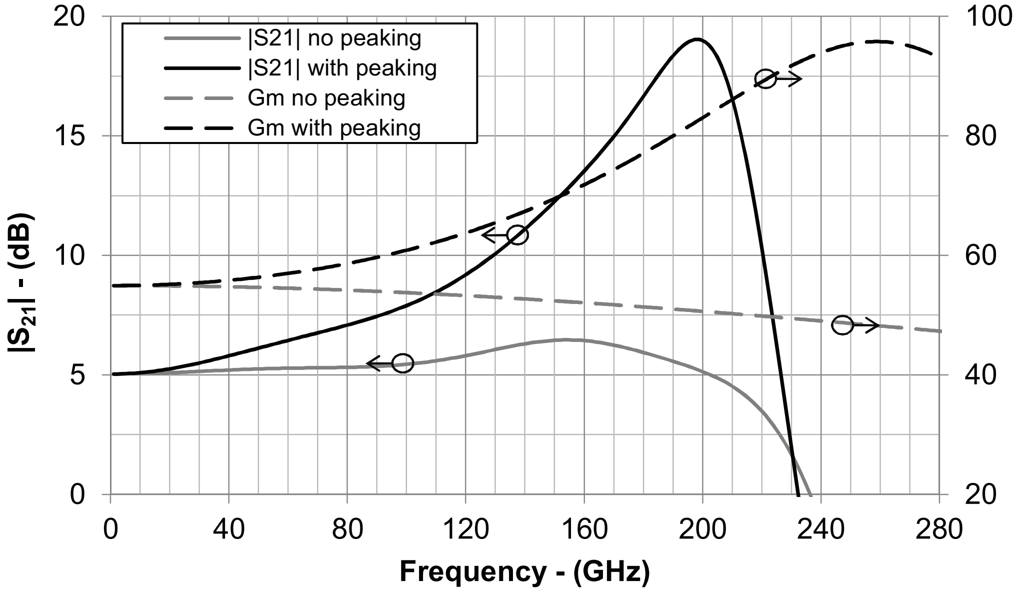


Figure 3.49: Simulated gain-peaking of the CSSDA established with ℓ_{IN} (Fig. 3.48). The result is compared to the case of no peaking for same design parameters. The simulated equivalent gain-cell transconductances are also illustrated for both cases.

against the conventional case, and also the cell G_m is presented.

The design of the cell targeted the minimization of its input pole originating from $R_{in}{\cdot}C_{in}$ to pursue the highest frequency of operation. The schematic and the 3D view of the gain element are in Fig. 3.48a and 3.48b. The main contribution to R_{in} is the base resistance of Q_0. Hence, the widest available HBTs from the model library have been used to reduce this parasitic resistance. The emitter area of the transistor Q_0 has been set to $10{\times}0.9{\times}0.07\,\mu m^2$. This produced a R_{in} of $6.7\,\Omega$. In turn, the use of large emitter-area resulted in a large input capacity. C_{in} has been then lowered with the capacitive-division approach [15] by the capacitor C_b of 120 fF (Section 3.3).

As mentioned above, the line segment ℓ_{IN} is used to boost the cell equivalent transconductance. Its length is 15 µm, while its characteristic impedance Z_0 is equal to that of the other lines used in the circuit. The cell G_m has been raised from 55 mS at 1 GHz, up to 95 mS at 260 GHz.

The cells are decoupled by C_b, while the base-current of Q_0 is supplied through the R_b resistor of 25 kΩ. The bases of the transistors Q_1 are ac-grounded with the capacitors $C_{S1,2}$ of 150 fF. Finally, blocking caps (Section 2.3.2) are used to create the distribution networks of the bias signals.

3.7.2 Experimental Characterization

The presented novel architecture has been tested with a circuit prototype fabricated with the *SG13G2* technology. As described in Section 2.1, the nominal f_{max}

Table 3.6: Design parameters of the fabricated BCSSDA.

ℓ_1 [μm]	ℓ_2 [μm]	**L' [μH/m]**	**C' [pF/m]**	**Z_0 [Ohm]**
50	170	0.42	92.5	65
ℓ_{IN} [μm]	**C_{in} [fF]**	**C_{out} [fF]**	**R_{in} [Ohm]**	**G_m [mS]**
15	50	23	6.7	55

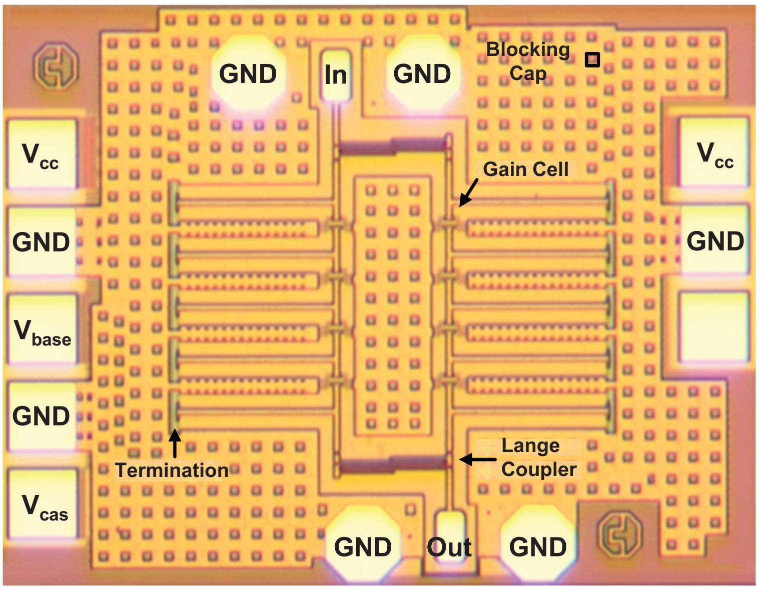


Figure 3.50: Micro-photograph of the BCSSDA [Testa6]. The die area is $0.38\,\text{mm}^2$.

of the process is 450 GHz, but it reduced to 370 GHz in the tolerance corner of the actual fabrication run. Fig. 3.50 shows the picture of the fabricated hardware. The total chip area is $0.38\,\text{mm}^2$. All the measurements were acquired on-chip for $I_{CC} = 121\,\text{mA}$ and $V_{CC} = 3\,\text{V}$. A vector analyzer with converter modules was used to perform the *S-Parameters characterization* in the following frequency ranges: from 200 MHz to 67 GHz, from 90 GHz to 140 GHz, and from 140 GHz to 220 GHz. Fig. 3.51 shows the measurement results, and the simulated $|S_{21}|$ for nominal and worst-case f_{max}. The gain is predicted well at low frequency by the worst-case process-corner model, while in the proximity of 200 GHz the amplifier behaves within the gain region defined by the two models. The amplifier provides an average of 16 dB gain, with a peak value of 20 dB, while the frequencies where it drops by $-3\,\text{dB}$ from its average value are 45 GHz and 220 GHz. Fig. 3.51 also shows the gain calculated using eq. (3.34) with the design values gathered in Table 3.6, in conjunction with the simulated response of the couplers. The gain absolute value and frequency behavior predicted by eq. (3.34) match the measurement results, validating the presented circuit analysis. Fig. 3.52 shows

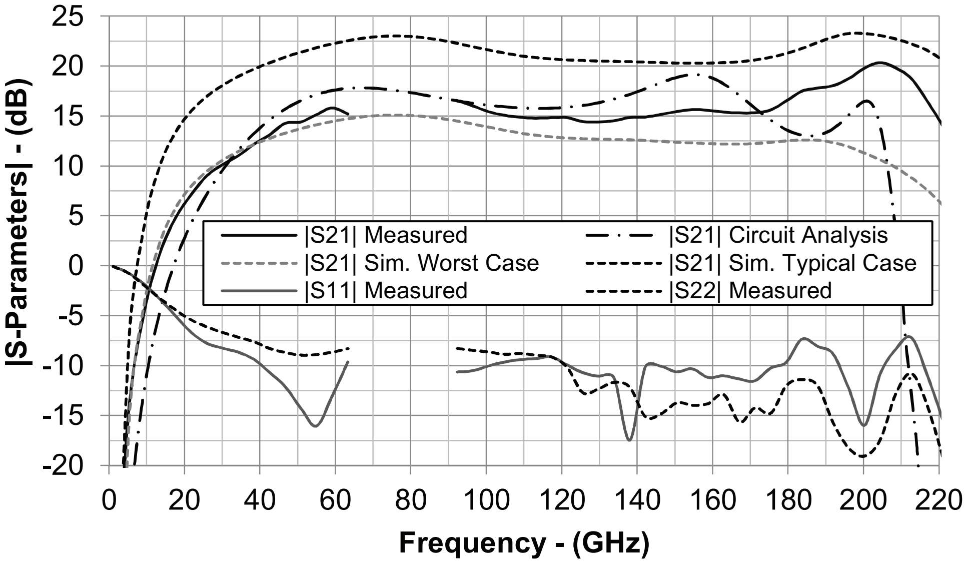


Figure 3.51: Measured S-Parameters magnitudes of the BCSSDA in Fig. 3.50, and simulated $|S_{21}|$ of this amplifier for worst and typical process-corner. The gain is also calculated as in eq. (3.34) using the values of Table 3.6.

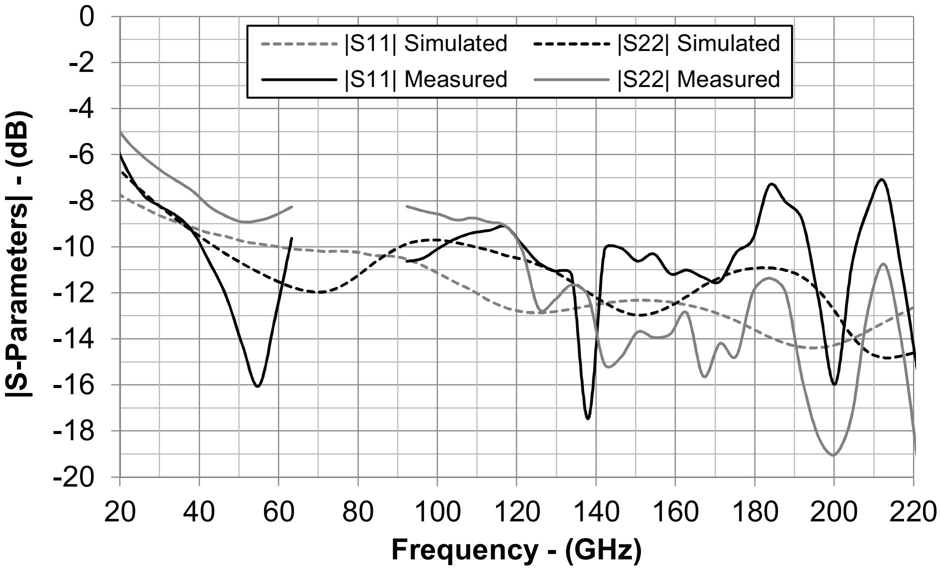


Figure 3.52: Measured and simulated $|S_{11}|$ and $|S_{22}|$ of the BCSSDA in Fig. 3.50.

measured and simulated $|S_{11}|$ and $|S_{22}|$ proving also agreement between them.

The *large-signal measurements* are presented in Fig. 3.53 and 3.54 as the function of frequency in the range from 30 GHz to 60 GHz and from 90 GHz to 140 GHz. The measured i1dBCp at 50 GHz is −16 dB, corresponding to an o1dBCp of −0.5 dBm. The measured i1dBCp at 130 GHz is −10.5 dBm, corresponding to an o1dBCp of 4.5 dBm. The measured output power versus the available power of the generator is shown in Fig. 3.55 for test frequencies of 180 GHz, 200 GHz, and 220 GHz. For these frequencies, the i1dBCp cannot be reached due to the limited output power of the available equipment. Nevertheless, it is possible to see a linear behavior of the amplifier up to an input power

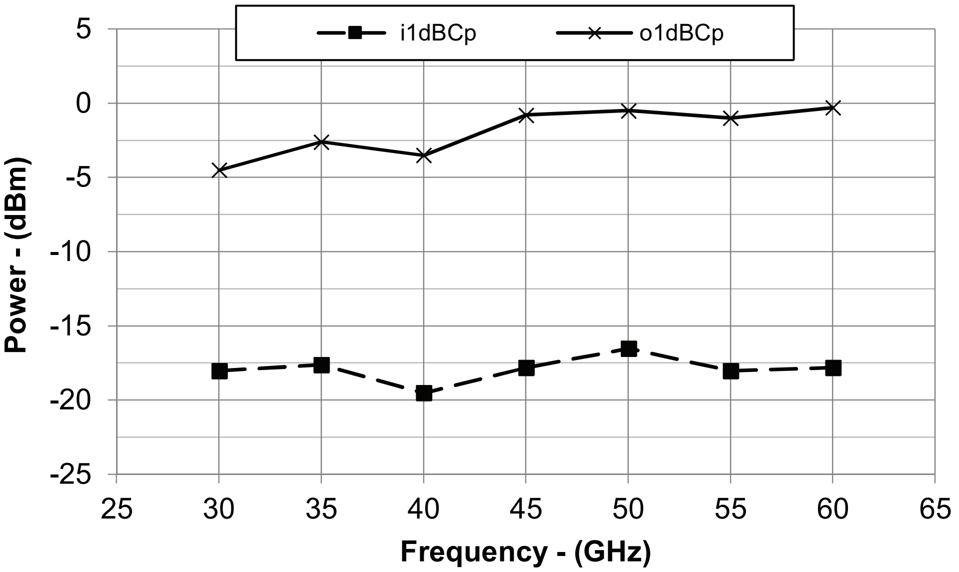


Figure 3.53: Measured input and output power in 1 dB compression of the gain of the BCSSDA in Fig. 3.50, for the frequency range 30 GHz to 60 GHz.

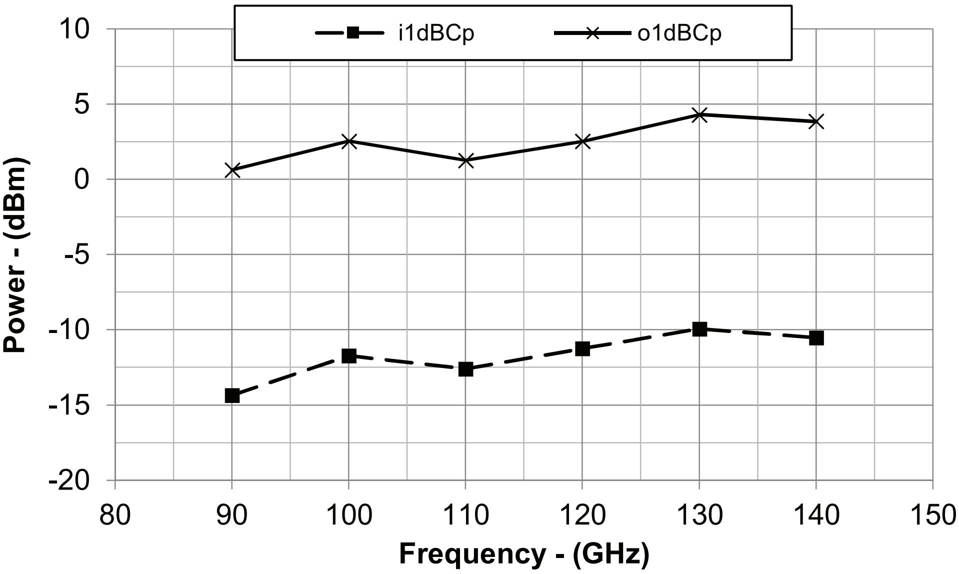


Figure 3.54: Measured input and output power in 1 dB compression of the gain of the BCSSDA in Fig. 3.50, for the frequency range 90 GHz to 140 GHz.

of −16.5 dBm, corresponding to an output power of −1.28 dBm. The presented characterization of the amplifier linearity highlights how for increasing frequency of operation the o1dBCp increases. This trend is due to the couplers, which for raising frequencies feed more uniformly the input signal to the CSSDA modules making both of them contribute to the output power, as confirmed by the reduction of the amplitude unbalance shown in Fig. 3.44.

The *group-delays measurements* and simulations are presented in Fig. 3.56. The simulated group delay variation is below 10 ps in the frequency range from 20 GHz to 220 GHz, while the measured group delay variation is below 20 ps in

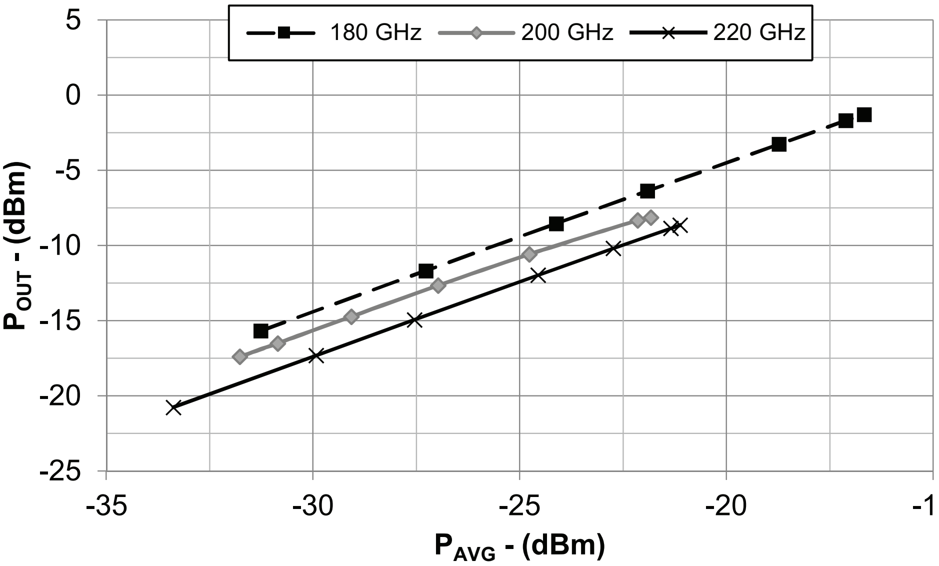


Figure 3.55: Measured output power of the BCSSDA in Fig. 3.50 versus the available power of the generator P_{AVG} at 180 GHz, 200 GHz, and 220 GHz.

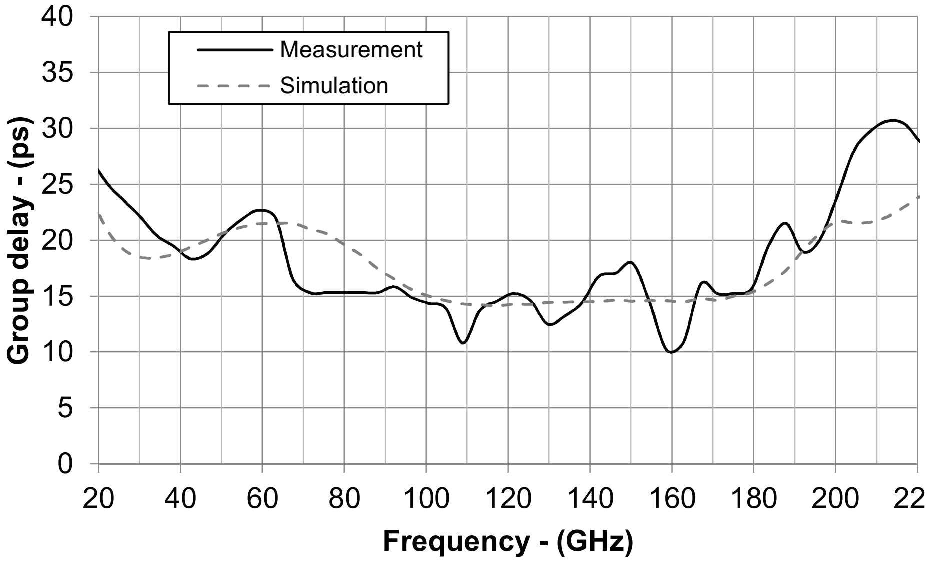


Figure 3.56: Measured and simulated group delay of the BCSSDA in Fig. 3.50 over the frequency.

the same range.

The *noise figure measurements* and simulations are presented in Fig. 3.57. The available equipment allows characterization up to 55 GHz. At this frequency, the measured noise figure is 14 dB in agreement with the simulation. The simulated noise figure reaches the minimum value of 9.5 dB at 110 GHz.

3.7.3 Discussion of the Results

A novel amplifier topology is proposed to address the shortcomings of CSSDAs with the use of two Lange couplers in a balanced configuration [Testa6].

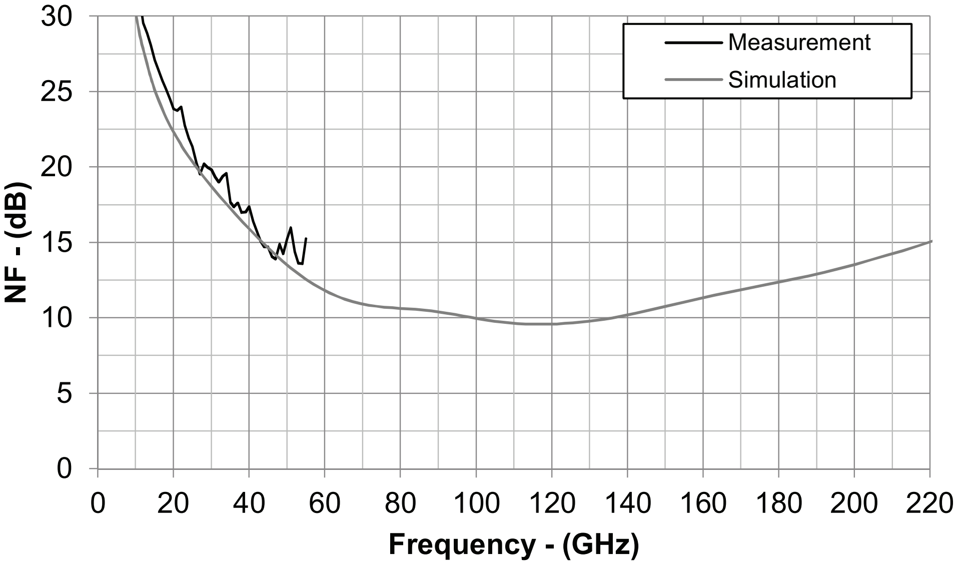


Figure 3.57: Measured and simulated noise figure of the BCSSDA in Fig. 3.50 over the frequency.

The presented solution solves the two main issues of CSSDAs, i.e., the degradation of the matching in the upper part of the frequency spectrum of amplification [Testa19, Testa21, 23], and the reduced input and output power in 1 dB compression of the gain.

The claim is supported by extended circuit analysis, and detailed description of which inherent features of the circuit network cause the difficulties in the matching. Furthermore, the first compact and general analytic expression has been presented for the prediction of the CSSDA gain versus the frequency of operation.

The experimental validation has been presented with a circuit prototype fabricated in the 130 nm SiGe BiCMOS process used in this thesis. The prototype gain peaks at 20 dB, and its average in-band value is 16 dB. The frequencies where the gain drops by −3 dB from the average value are 45 GHz ($f_{\mathrm{DOWN,3dB}}$) and 220 GHz ($f_{\mathrm{UP,3dB}}$), which is the highest observable frequency with the available measurement equipment. Compared against the state-of-art gathered in Table 3.7, the amplifier shows one of the largest reported gain-bandwidth products, the highest output-power in 1 dB compression of the gain, while still being functional above 200 GHz, and despite the lower f_{max} than the fastest reported designs. The demonstrated group delay variations over frequency (Δtp/BW) is also one of the best reported so far for distributed amplifiers, therefore validating the usefulness of the proposed techniques for broadband applications. The balanced configuration also enabled the best input and output matching at $f_{\mathrm{UP,3dB}}$, solving the issue of poor matching at the highest end of the band typical of CSSDAs.

Table 3.7: Extended CSSDAs state of the art.

Ref.	**GBP** [GHz]	$f_{\mathbf{DOWN,3dB}}$ [GHz]	$f_{\mathbf{UP,3dB}}$ [GHz]	**BW** [GHz]	**Gain** [dB]	**Peaking** [dB]	f_{max} [GHz]	**o1dBCp** [mW]	$\mathbf{P_{DC}}$ [mW]	$\lvert\mathbf{S_{11}}\rvert$, $\lvert\mathbf{S_{22}}\rvert$ [dB]*	**Area** [mm^2]	**Δtp/BW** [ps/GHz]	**NF** [dB]	**Technology**
[27]	199	dc	25	25	9	6	n.a.	n.a.	60	-5, -5	0.36	50/30	n.a.	65 nm Si CMOS
[32]	260	25	65	65	16.5	3	n.a.	n.a.	333	-5, -5	1.31	n.a.	n.a.	150 nm GaAs
[52]	312	dc	70	70	13	4	200	1	85	0, -2	0.78	75/70	n.a.	90 nm Si CMOS
[53]	900	dc	90	90	20	5	n.a.	1	90	-5, -5	0.31	80/100	n.a.	40 nm Si
CSSDA Sec. 3.6.1	759	80	250	170	13	0	450	n.a.	74	-4, 0	0.22	10/110	n.a.	130 nm SiGe
[23]	1514	2	240	240	16	2	650	n.a.	117	-5, 0	0.41	24/200	$10^{\dagger}$	250 nm InP
This Work	1102	45	220^{**}	175^{**}	16	4	370	4.5	360	-7.5, -11	0.38	20/200	$9.5^{\dagger}$	130 nm SiGe

*: Measured in the higher part of the spectrum of amplification, **: Limited by the available equipment, †: Minimum value.

4 Distributed Power Combiners and Dividers

4.1 Introduction

The millimeter-wave spectrum is of interest for the availability of un-allocated wide bands, while its main drawbacks are the severe free-space path losses. As an example, a signal propagating in the air at 200 GHz over 5 cm experiences more than 50 dB of attenuation is antennas with 0 dBi gain are in use. Millimeter-wave UWB systems are therefore usually connected with limited signal powers at the receiver end, which can reduce the data rate or the distance of the communication.

Antenna arrays are used to overcome this limitation focusing the transmission toward specific directions and increasing, in turn, the power at the receiver end. UWB combiners and dividers are needed to form the signal-distribution networks required by the antenna arrays. Passive components have limited bandwidth since they are usually based on quarter-wave (Wilkinson divider) and half-wave (Gysel divider) structures. On the contrary, active combiners and dividers exploiting distributed amplifications can operate over broad frequency bands as the amplifiers described in the previous Chapter.

In this thesis, a combiner [Testa2] and a divider [Testa9] have been developed using distributed amplification techniques. The analysis, design, and characterization of these circuits will be presented in the following sections.

4.2 220 GHz Distributed Power Combiner

Distributed amplifiers can achieve uniform gain, flat group delay, and good input and output matching over wide frequency bands of operation. Furthermore, distributed amplifier techniques can also be employed for designing active power combiners. In fact, as illustrated in Fig. 4.1, two distributed amplifiers sharing

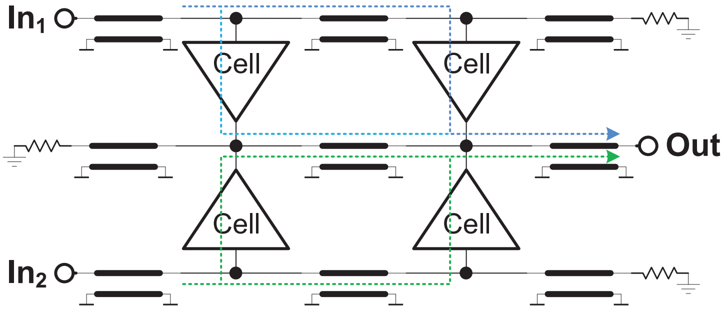


Figure 4.1: General architecture of traveling-wave combiners.

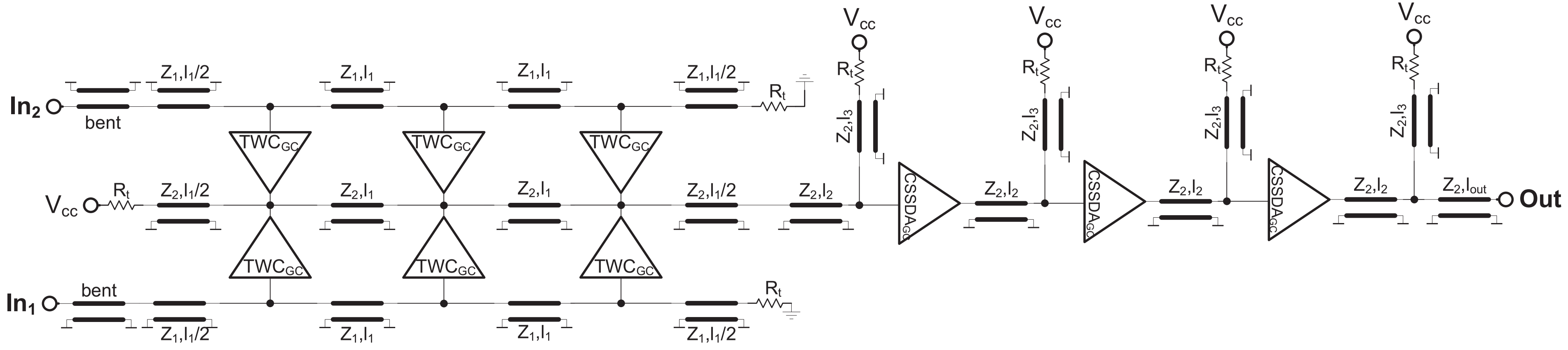

In$_2$
bent
$Z_1,l_1/2$
Z_1,l_1
Z_1,l_1
$Z_1,l_1/2$
R_t
V_{cc}
R_t
$Z_2,l_1/2$
Z_2,l_1
Z_2,l_1
$Z_2,l_1/2$
Z_2,l_2
TWC$_{GC}$
In$_1$
bent
$Z_1,l_1/2$
Z_1,l_1
Z_1,l_1
$Z_1,l_1/2$
R_t
V_{cc}
R_t
Z_2,l_3
CSSDA$_{GC}$
Z_2,l_2
Z_2,l_{out}
Out

Figure 4.2: Schematic of the distributed combiner designed in this thesis. The TWC and CSSDA gain cells are indicated by TWC$_{\mathrm{GC}}$ and CSSDA$_{\mathrm{GC}}$ respectively.

the same output line perform the signal combination [54–57].

Within the frame of this thesis, a UWB distributed combiner has been implemented in the *SG13G2* technology [Testa2]. The next sections present circuit analysis, design, and experimental characterization of the demonstrated combiner.

4.2.1 Circuit Analysis

Fig. 4.2 shows the circuit schematic of the developed distributed combiner. The circuit consists of two stages. The first one is formed by two TWAs, which share the output line and are used to perform the signals combination. This part of the system is referred to as Traveling-Wave Combiner (TWC). The second section of the circuit is composed of a CSSDA (Section 3.4), which is employed to provide high amplification while requiring reduced chip area and power consumption [Testa19, Testa21, 23, 49].

At first glance, the main difference between the circuit analysis of TWCs and TWAs is the double capacitive-loading of the cells on the shared output line. To account this, the combiner output synthetic-line impedance $\mathrm{Z_{S,out}}$ is expressed as:

$$Z_{S,out} = \sqrt{\frac{L'}{C' + \frac{2C_{out}}{\ell}}} \tag{4.1}$$

where the symbols are defined as in eq. (3.1). The whole power-gain of the combiner $\mathrm{G_C}$ can be expressed using equations (3.7), (3.34), and (4.1) as:

$$G_C = G_{TWC} \cdot G_{CSSDA} \tag{4.2}$$

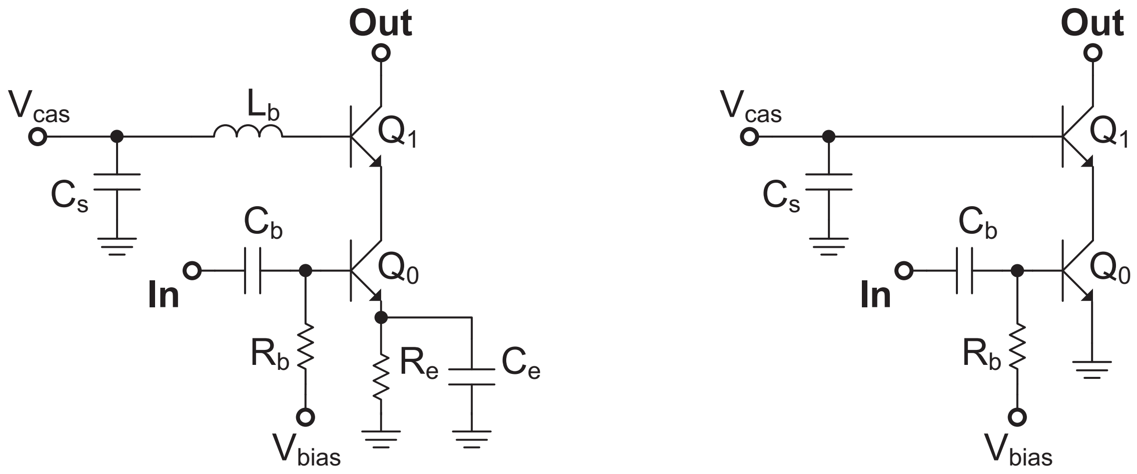
where,

$$G_{TWC} = (\frac{nG_m Z_{S,out}}{2})^2 (1 - \frac{n\alpha_{in}}{2})^2, \tag{4.3a}$$

and

$$G_{CSSDA} = |\frac{(Z_{\mathrm{T\_over\_S}})^{N-1}(-G_{\mathrm{m}} \cdot D)^N}{(1 + j\omega R_{\mathrm{in}} C_{\mathrm{in}})^N \cdot (1 + j\omega Z_{\mathrm{T\_over\_S}} C_{\mathrm{out}})^{\mathrm{N\text{-}1}}} \cdot \frac{A}{B}|. \tag{4.3b}$$

The symbols of these expressions are defined in eq. (3.7) for the TWC, and in eq. (3.34) for the CSSDA. Thanks to the distributed nature of TWAs and CSSDAs, very wideband matching can be obtained when these circuits are cascaded. The combiner gain is therefore calculated as the product of the amplifications provided by the single modules. In the next section eq. (4.2) will be compared against the simulation of the combiner response showing agreement, while in Section 4.2.3 the experimental results will validate in turn the circuit simulation.


Out
Vcas
Lb
Q1
Cs
Cb
In
Q0
Rb
Re
Ce
Vbias
Out
Vcas
Q1
Cs
Cb
In
Q0
Rb
Vbias

(a) (b)

Figure 4.3: (a) Schematic of the TWC gain-cell, and (b) of the CSSDA gain-cell.

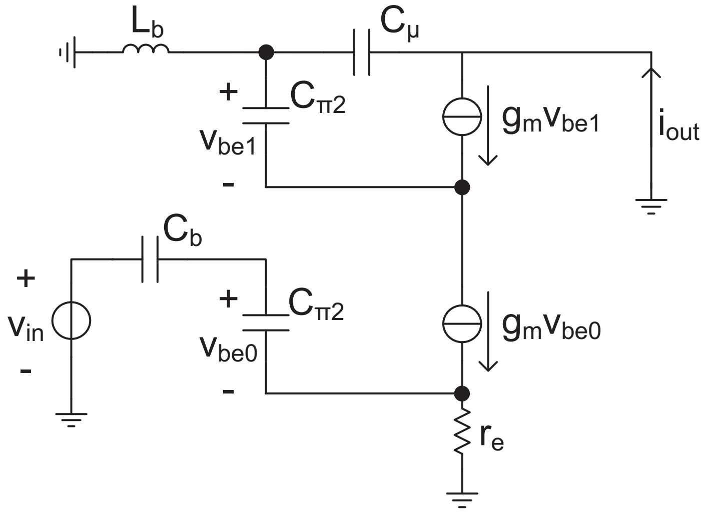

Lb
Cμ
+
Cπ2
vbe1
-
gmvbe1
iout
Cb
+
vin
-
+
Cπ2
vbe0
-
gmvbe0
re

Figure 4.4: Simplified small-signal circuit of the TWC cell (Fig. 4.3a), employed for the calculation of its transconductance in eq. (4.4).

4.2.2 Circuit Design

The core function of the TWC is the signal combination, while the CSSDA is devoted to the amplification of the combined signals. As it can be seen in Fig. 4.2, the TWC consists of only three gain cells to reduce the impact of the synthetic-line losses on the bandwidth of the combiner. On the other hand, the limited number of cells reduces the TWC gain to only 3 dB. Higher amplification is provided by the CSSDA, which increases the signal level by 17 dB employing only three cells as well. The details of the TWC and CSSDA gain-elements are

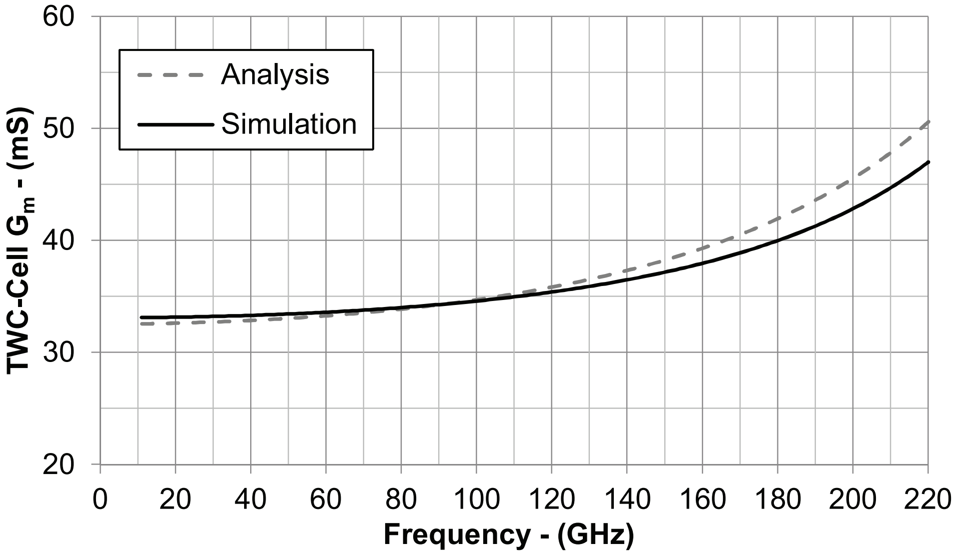


Figure 4.5: Comparison between the simulated G_m of the TWC cell, and its estimation as in eq. (4.4) evaluated for the values in Table 4.1.

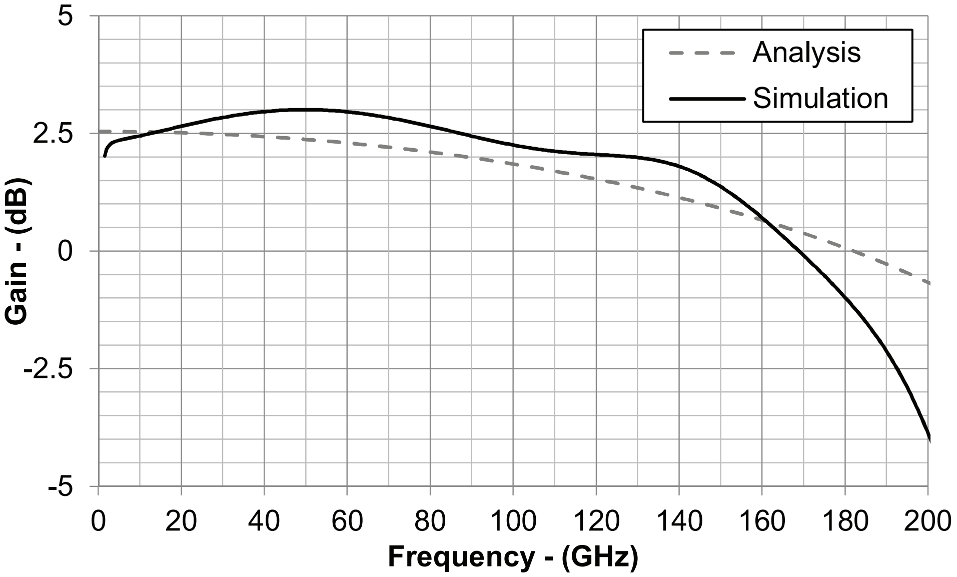


Figure 4.6: Comparison between the simulated gain of the TWC used in the combiner of Fig. 4.2, and its estimation with eq. (4.3a) evaluated for the values in Table 4.2.

presented below.

TWC Gain-Cell The cell schematic is shown in Fig. 4.3a. The gain element is based on the cascode configuration; the advantages of this topology are discussed in Section 3.3.1.

The capacitive division technique through the C_b capacitor of 50 fF [15] and the series feedback $R_e - C_e$ are employed to reduce the cell input-capacitance [34]. A value of 5 Ω has been chosen for R_e: this is a good compromise, which offers at the same time low R_{in} and C_{in} without scarifying G_m excessively, or the power consumption [34]. Moreover, R_e stabilizes G_m against process variations. C_e has

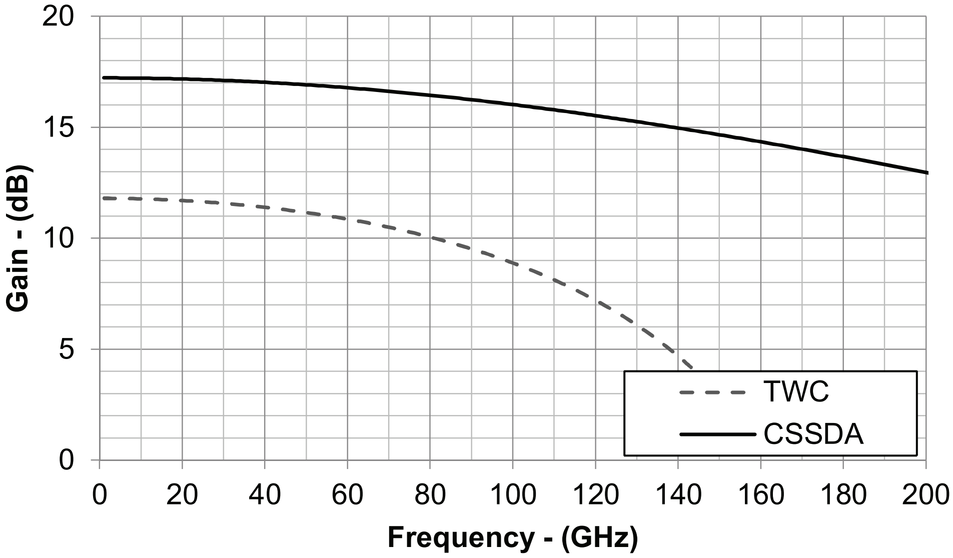


Figure 4.7: Simulated gain of the CSSDA used in the combiner of Fig. 4.2, and comparison against that of a hypothetical TWC based on the same design parameters such as type and number of cells and synthetic-line impedance.

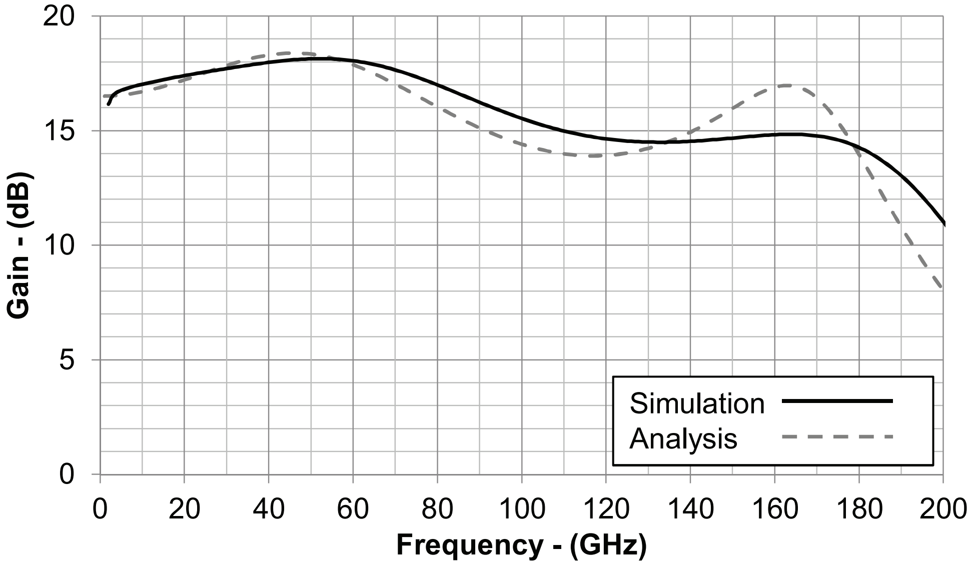


Figure 4.8: Comparison between the simulated gain of the CSSDA in Fig. 4.2, and its estimation with eq. (4.3b) evaluated with the values in Table 4.3.

been set to 90 fF. The inductance L_b (Fig. 4.3a) provides a partial compensation of the synthetic-line losses, increasing the cell G_m at high frequencies with a technique similar to that presented in Section 3.3.1. The simplified circuit of Fig. 4.4 has been used to calculate the cell transconductance. Its expression is:

$$G_m = \frac{A \cdot B}{C} \tag{4.4}$$

Table 4.1: Small-signal parameters of the circuit in Fig. 4.4.

$\mathbf{g_m}$ [mS]	$\mathbf{C_\mu}$ [fF]	$\mathbf{C_{\pi 1,2}}$ [fF]	$\mathbf{C_b}$ [fF]	$\mathbf{r_e}$ [Ω]
125	8	45	50	15

Table 4.2: Gain-cell and transmission-line parameters of the TWC used in the combiner of Fig. 4.2.

$\mathbf{G_m}$ [mS]	$\mathbf{C_{in}}$ [fF]	$\mathbf{C_{out}}$ [fF]	$\mathbf{R_{in}}$ [Ω]	$\mathbf{Z_1}$ [Ω]	$\mathbf{l_1}$ [µm]	**C'** [fF/m]	**L'** [µH/m]
Eq. (4.4)	22	12	19.5	90	80	70	0.60

where,

$$A = g_m(1 - \omega^2 L_B C_\mu) - j\omega^3 L_B C_\mu C_{\pi 2} \tag{4.5a}$$

$$B = \frac{1}{1 - \omega^2 L_B C_\mu} \tag{4.5b}$$

$$C = \left[1 + \frac{C_{\pi 1}}{C_b} + r_e(g_m + j\omega C_{\pi 1})\right](1 + \frac{j\omega C_{\pi 1}}{g_m}) \tag{4.5c}$$

Eq. (4.4) illustrates how the shaping of G_m at high frequency is due to the resonance of L_b with the capacitances of the transistors. The behavior of the simplified model in Fig. 4.4 is compared in Fig. 4.5 against the simulation of the cell demonstrating agreement. Table 4.1 lists the small-signal values of the simplified model.

To validate the circuit analysis presented in the previous section, the gain of the TWC has been calculated with eq. (4.3a) using the small-signal parameters gathered in Table 4.2 and then compared in Fig. 4.6 against the circuit simulation. The two evaluations of the TWC response are in agreement.

CSSDA Gain-Cell The schematic of the cell is illustrated in Fig. 4.3b. The circuit is based on a cascode architecture, while the capacitive division through C_b is used to reduce the synthetic-line losses. Since for CSSDAs the synthetic-line losses are less critical than for TWAs and TWCs, other loss-minimization techniques have been not necessary to match the bandwidth of the TWC stage. Fig. 4.7 compares the gain of the designed CSSDA with that of a hypothetical TWC based on the same design parameters such as type and number of cells and synthetic-line impedance: the CSSDA bandwidth is 170 GHz, while the TWC one is 100 GHz. Moreover, Fig. 4.7 shows that for same conditions, the CSSDA generates higher gain than the TWC. The CSSDA gain expression in eq. (4.3b)

Table 4.3: Gain-cell and transmission-line parameters of the CSSDA used in the combiner of Fig. 4.2.

$\mathbf{G_m}$ [mS]	$\mathbf{C_{in}}$ [fF]	$\mathbf{C_{out}}$ [fF]	$\mathbf{R_{in}}$ [Ω]	$\mathbf{Z_2}$ [Ω]	$\mathbf{l_2}$ [µm]	$\mathbf{l_3}$ [µm]	**C'** [fF/m]	**L'** [µH/m]	$\mathbf{R_t}$ [Ω]
60	45	15	15	100	60	160	70	0.68	50

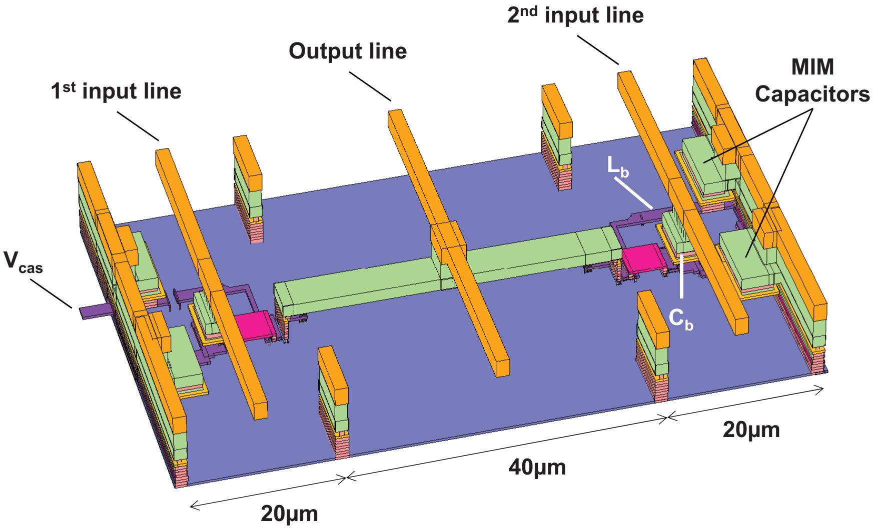


Figure 4.9: 3D view of the gain cells (Fig. 4.3a) and transmission lines employed in the TWC.

has been plotted for the simulated parameters of the designed cell in Table 4.3, and compared in Fig. 4.8 against circuit simulation, proving agreement. The presented circuit simulations will be validated by the measurement results in Section 4.2.3.

Microstrip transmission-lines have been used to connect the gain cells. Since the capacitive loading of the cells is not homogeneous between TWC and CSSDA, the characteristic impedance of the lines has been therefore adjusted to ensure a Z_S of $40\,\Omega$ in the whole circuit. This value is a compromise between gain, bandwidth, and matching. The characteristic impedance of the unloaded lines is Z_1 equal to $90\,\Omega$, while Z_2 is $100\,\Omega$ (Fig. 4.2). The distances between the cells are ℓ_1 of $80\,\mu\text{m}$, ℓ_2 and ℓ_{out} of $60\,\mu\text{m}$, and ℓ_3 of $160\,\mu\text{m}$. Electromagnetic simulations allowed the precise evaluation of the L_b inductance. Fig. 4.9 shows a 3D view of the TWC cell and transmission lines.

4.2.3 Experimental Characterization

Fig. 4.10 shows the micro-photograph of the distributed combiner. The total chip area is $0.57\,\text{mm}^2$. The *S-Parameters measurement* of the combiner is presented in Fig. 4.11. They were acquired when the system was biased at $I_{CC} = 58\,\text{mA}$ and

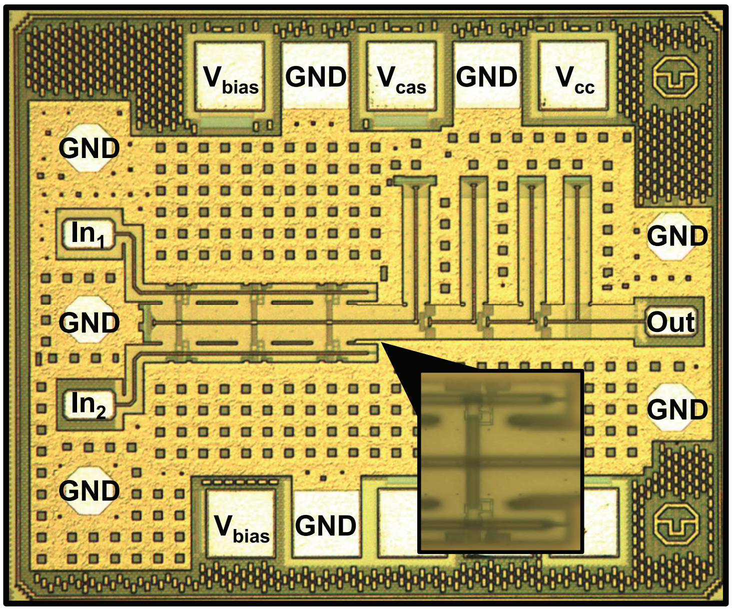


Figure 4.10: Micro-photograph of the fabricated distributed power combiner [Testa2]. The chip dimensions are 0.7 mm×0.8 mm, while the chip area is 0.56 mm^2. The TWC gain-cell is illustrated in the inset.

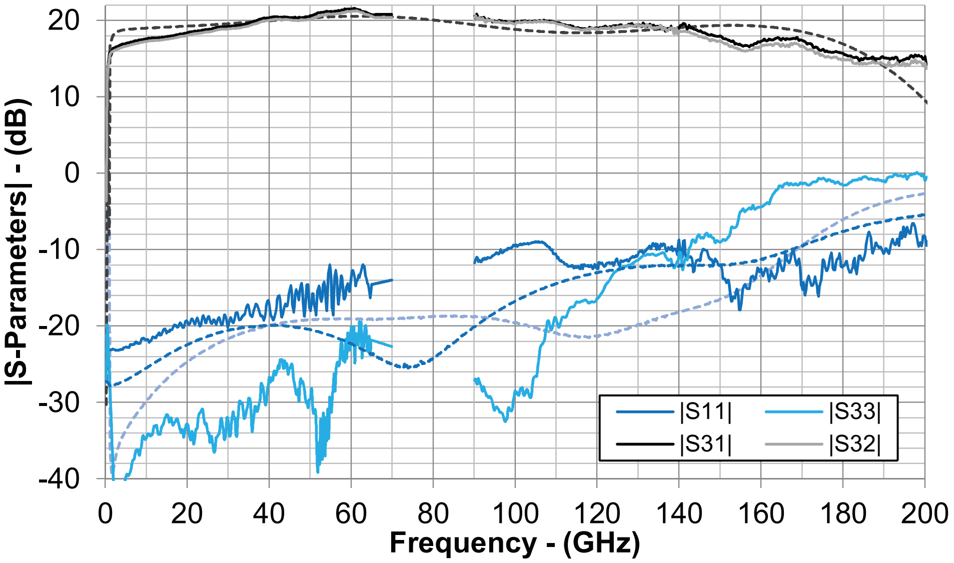


Figure 4.11: Measured (solid) and simulated (dotted) S-Parameters of the combiner in Fig. 4.10. The input ports are I and II, while the output is port III.

$V_{CC} = 3.5$ V, resulting in 203 mW of power consumption. A VNA was employed for the characterization. Due to its ultra-wide frequency band of operation, three different setups have been employed. They operate in the following frequency ranges: from 200 MHz to 67 GHz, from 90 GHz to 140 GHz, and from 140 GHz to 220 GHz. All except the first required the use of extender modules. In the selected operation point, the circuit provides a gain of 20 dB over the −3 dB bandwidth from 1 GHz to 170 GHz. From 170 GHz to 220 GHz, the gain is still above 15 dB, demonstrating the combiner capabilities with significant gain even

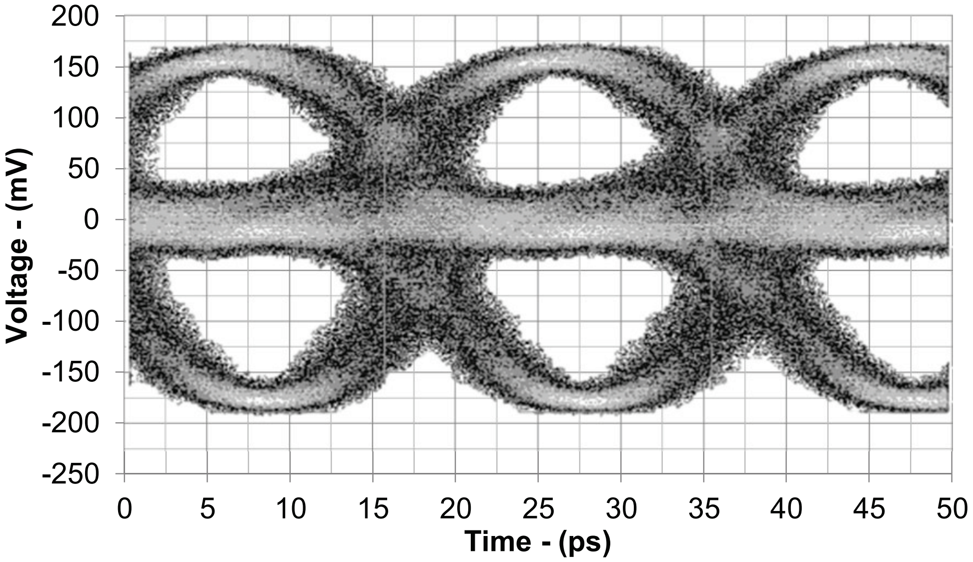


Figure 4.12: Output of the combiner in Fig. 4.10 for eye-diagram measurement when two input digital-signals of amplitude 32 mV peak-to-peak at 50 GHz are applied .

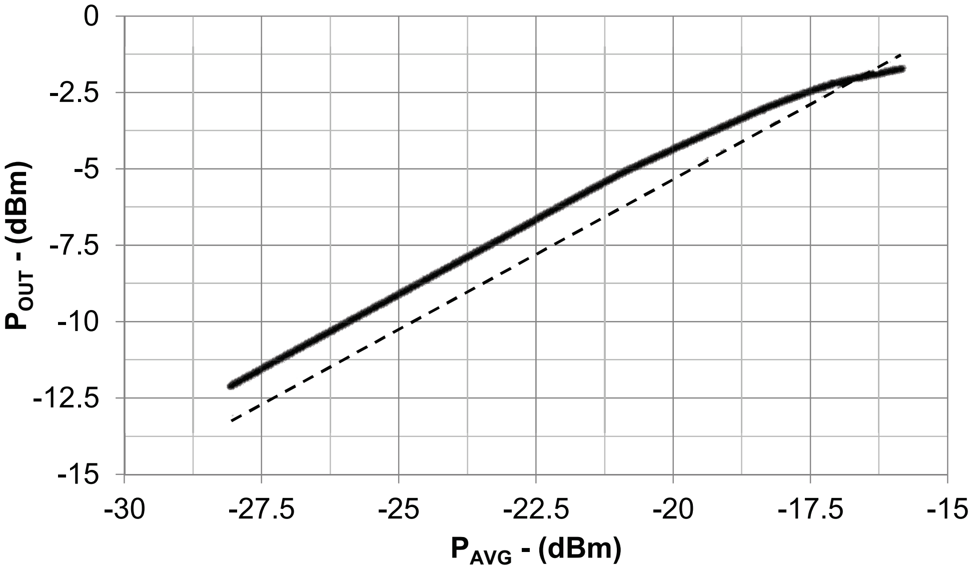


Figure 4.13: Measured gain-compression curve of the combiner in Fig. 4.10 for an input signal at 20 GHz.

at this frequency. The agreement between measurements and simulations shown in Fig. 4.11 validates the circuit analysis and design presented in Sections 4.2.1 and 4.2.2. The measured input return loss is above 10 dB for the whole −3 dB bandwidth of the combiner. $|S_{33}|$, which is the scattering parameter of the output port, is below −10 dB up to 150 GHz, while it deteriorates toward higher frequencies. The degradation of the combiner output matching is due to the CSSDA, which, as discussed in Section 3.4.1, suffers of poor matching at the highest end of the frequency band of operation.

Time-domain tests have been also performed to validate the signal combination

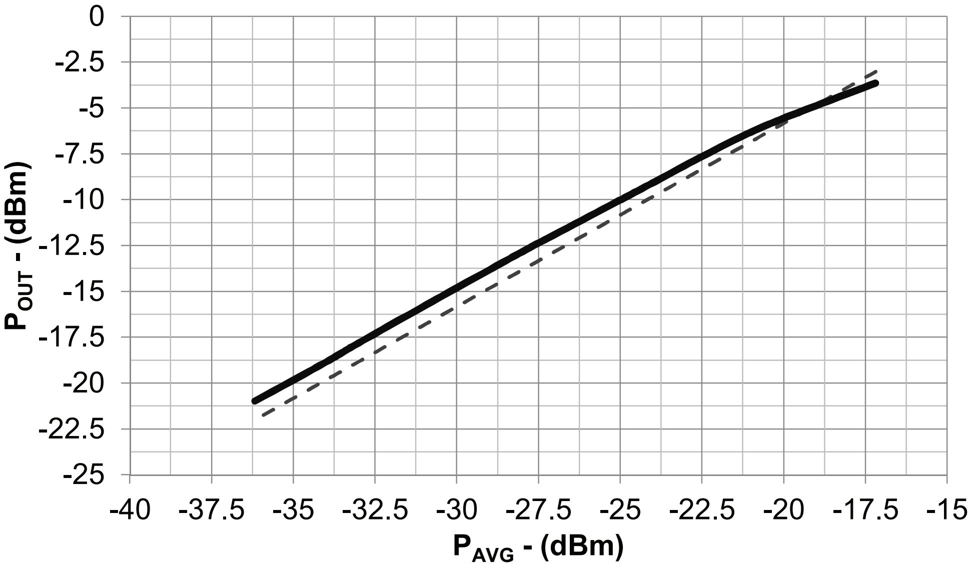


Figure 4.14: Measured gain-compression curve of the combiner in Fig. 4.10 for an input signal at at 180 GHz.

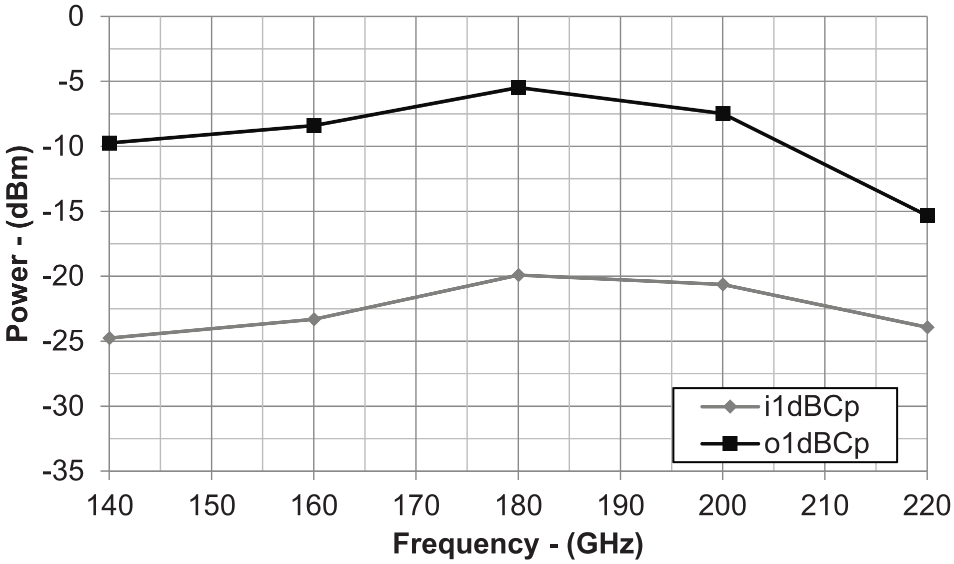


Figure 4.15: Measured input and output power in 1 dB-compression-of-the-gain of the combiner in Fig. 4.10 plotted over frequency.

capability. Two input digital signals have been applied to the combiner with a clock frequency of 50 GHz and a peak-to-peak amplitude of 32 mV. The two input signals have been generated with a bit pattern generator. The output eye diagram has been then captured with a sampling oscilloscope and synchronized with an external signal. An off-the-shelf phase shifter ensured the phase synchronization between the input signals. The experiment results are shown in Fig. 4.12. As expected the combination of two input signals with same frequency and amplitude generates three output levels: the lowest and highest outputs correspond to the combination of the lowest and highest inputs, while the intermediate output level is due to the addition of different inputs levels. The peak-to-peak voltage of the

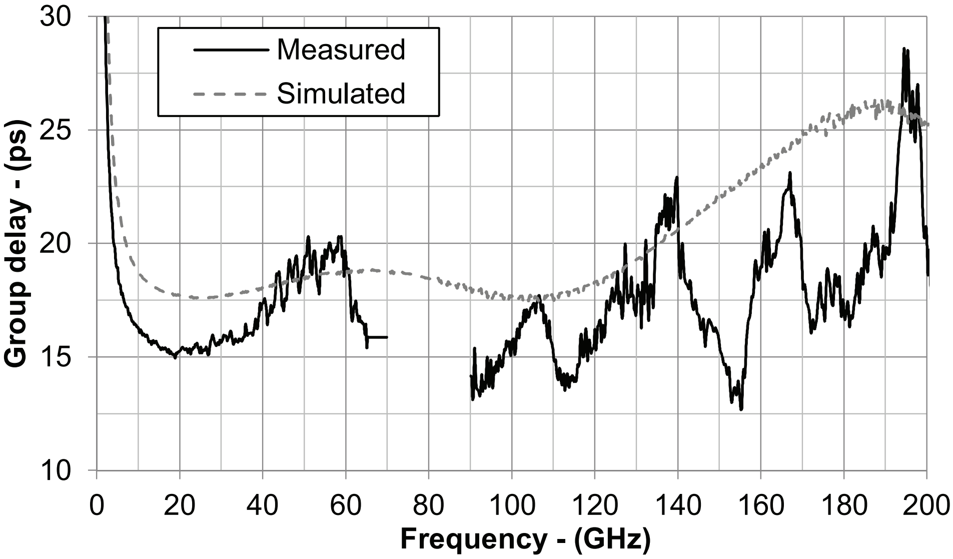


Figure 4.16: Measured and simulated group delay of the combiner in Fig. 4.10.

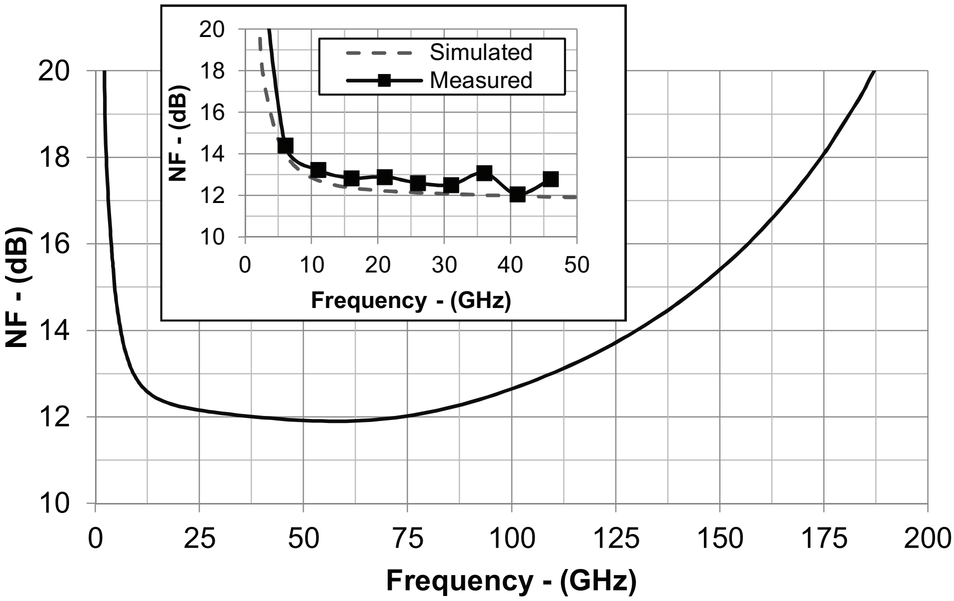


Figure 4.17: Simulated noise figure of the combiner in Fig. 4.10 for the frequency range from 1 GHz to 200 GHz. The inset shows the measured and simulated noise figure from 1 GHz to 50 GHz.

output is 343 mV. This value is the double of the output voltage swing of each of the combined signals. Hence, the output voltage swing for every output is 171 mV. Being the input swing 32 mV, the measured voltage amplification per combining path is 5.32, which corresponds to a power amplification of 14.6 dB, if referred to 50 Ω generator and load impedance. After de-embedding the 0.8 dB and 3 dB losses of probes and cables, respectively, the combiner gain reaches 19.4 dB, which is close to the measured small-signal power-gain of 20 dB at 50 GHz (Fig. 4.11).

Fig. 4.13 presents the *circuit linearity at low frequency* measured at 20 GHz. The input power at 1 dB compression of the gain is −17.7 dBm, which correspond an output power of −1.8 dBm.

Table 4.4: State of the art of distributed power combiners.

Ref.	**Gain** [dB]	**BW** [GHz]	$\mathbf{P_{DC}}$ [mW]	**Area** [mm^2]	$\mathbf{\Delta t_p}$ [ps/GHz]	**Technology**
[54]	6	1-10.6	15	1	10/10	0.13 µm CMOS
[55]	8	2-8	300	7.59	NA	0.5 µm GaN HEMT
[57]	3	2-18	NA	9	NA	GaAs
[56]	3	4-40	46	1	NA	0.25 µm InP HEMT
This work	20	1-170	203	0.56	10/170	0.13 µm BiCMOS

Fig. 4.14 presents the *linearity at high frequency*. The i1dBCp at 180 GHz is −19.2 dBm corresponding to a measured o1dBCp of 5.5 dBm. Fig. 4.15 presents the measured frequency behavior of i,o1dBCp in the band 140 GHz – 220 GHz. The measured variations of i,o1dBCp are within 5 dB in this frequency range.

Fig. 4.16 shows the measured and simulated group delay derived as in eq. (3.12). The group-delay variation is less than 10 ps over the combiner −3 dB bandwidth, and less than 15 ps over the 6 dB one. The small variations of the group delay result from the CSSDA which does not need equalization of phase-velocity of the currents, as TWAs require [37]. Moreover, just three cells are employed for the TWC, and this also reduces the variations of the group delay.

The measured and simulated *noise figure* is shown in Fig. 4.17. From 25 GHz to 75 GHz the simulated NF is 12 dB, while for higher frequencies it raises up to 18 dB at 170 GHz. The simulated data are validated through a comparison with the measurements in the frequency band from 10 GHz to 50 GHz, where the equipment was available.

4.2.4 Discussion of the Results

The developed distributed combiner has a silicon footprint of 0.57 mm^2 and consumes 203 mW to provide 20 dB of small-signal gain over the −3 dB frequency-band 1 GHz – 170 GHz [Testa2].

Table 4.4 presents the state of the art of distributed power combiners. The presented circuit shows the highest −3 dB upper frequency, as well as the broadest bandwidth of operation and gain. In detail, $f_{\mathrm{UP,3dB}}$ is improved from 40 GHz to more than 200 GHz, which amounts to a factor 5 of advancement.

The presented results are supported by the *SG13G2* process, in conjunction with the described design techniques. In particular, the primary system features such as signals combination, gain, and bandwidth, have been accomplished by the integration of TWC and CSSDA. The TWC has been optimized for a large bandwidth of operation, while the CSSDA increased the combiner gain above the highest demonstrated for this category of circuits.

4.3 200 GHz Distributed Power Divider

Fig. 4.18 shows the architecture of the distributed power divider presented in this thesis as Traveling-Wave Divider (TWD) [Testa9]. In a symmetric way of what described for TWCs in the previous section, the input transmission line feeds two sets of gain cells, which are attached to two independent output lines. Excited by the input signal, the cells feed same signal currents to the output lines, effectively providing the power-divider functionality while amplifying the signal. As for TWAs, the dominant effect limiting the performance of this architecture is the capacitive load that the cells impose on the input line: this is twice as large as in the corresponding TWA since two sets of cells are now attached at the input lines.

For this reason, despite the progress in IC technologies, TWD operating above 50 GHz have been not demonstrated yet [58–64], while TWAs have been reported with cutoff frequencies in excess of 170 GHz [Testa1]. The research community has acknowledged and approached this problem, with novel solutions being introduced recently to extend the operation band toward high frequency. In [58] the gain cells are arranged in interleaved rather than conventional parallel style to reduce the capacitances attached to the input line. The drawback of this approach is the difference in the response of the paths, which increases with the frequency of operation. In [59] a single-cell configuration has been adopted, minimizing the capacitive loading using just one cell, as it is done for CSSDAs (Section 3.4). Although in both works state-of-the-art technologies have been used (130 nm SiGe, and 90 nm CMOS), the maximum frequency of operation demonstrated is below 40 GHz.

Within the frame of this thesis, the first TWD operating from the MHz range up to 200 GHz is presented. Such high frequency and broadband operation has been achieved by shaping the gain-cell transconductance with the triple cascode topology described in Section 3.3. In addition, the synthetic lines have been designed with a tapering architecture, which, as described in the following sections, further increases the maximum operating frequency. To demonstrate experimen-

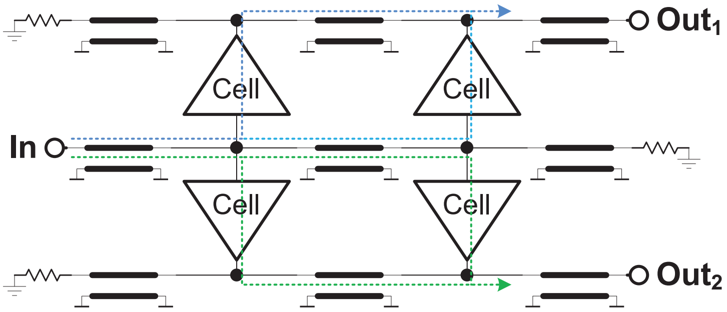


Figure 4.18: General architecture of traveling-wave dividers.

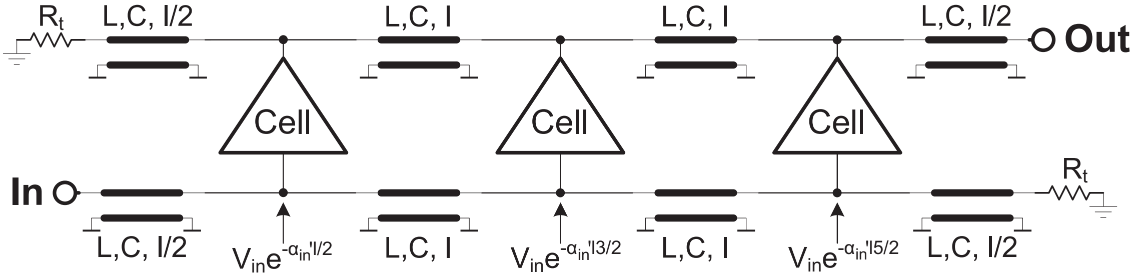

R_t
L,C, l/2
L,C, l
L,C, l
L,C, l/2
Out
Cell
Cell
Cell
In
R_t
L,C, l/2
$V_{in}e^{-\alpha_{in}' l/2}$
L,C, l
$V_{in}e^{-\alpha_{in}' l3/2}$
L,C, l
$V_{in}e^{-\alpha_{in}' l5/2}$
L,C, l/2

Figure 4.19: TWA schematic with synthetic propagation-losses in the input line annotated.

tally this novel approach, a circuit prototype has been fabricated in the *SG13G2* process. The next sections will present the circuit focusing on its analysis, design, and experimental characterization.

4.3.1 Circuit Analysis and Design

The general structure of TWDs – shown in Fig. 4.18 – is at its core a double traveling-wave amplifier, where the input line is shared between two identical amplifiers. As in TWAs, the input synthetic transmission-line is characterized by an attenuation constant equal to [15, 30, 37, 38]:

$$\alpha_{\text{in}}{}' = \frac{\omega^2 C_{\text{in}}{}^2 R_{\text{in}} Z_{\text{S}}}{2\ell} = \frac{\omega^2 C_{\text{in}}{}^2 R_{\text{in}}}{2\ell}\sqrt{\frac{L'}{C' + \frac{C_{in,out}}{\ell}}} \tag{4.6}$$

where the symbols have been defined in Section 3.2.1, and the distance between the cells ℓ is made explicit. Due to the synthetic losses, the voltage signal propagating over ℓ is attenuated by a factor L:

$$L = e^{-\alpha_{\text{in}}{}'\ell} \tag{4.7}$$

Furthermore, the input signal meets each cell after traveling different distances in the input line, as sketched in Fig. 4.19. The last cells of the TWA then receive less power than the one closer to the input of the amplifier. As discussed in Section 3.2.1, the dependence of α_{in}' from ω^2, and from the features of gain cells and transmission lines, sets the upper operating frequency of distributed amplifiers. This problem is even more severe for TWDs since the capacitive load on the input line is twice that of TWAs being two sets of cells attached. As predicted by eq. (4.6), this translates in an increase of α_{in}' by a factor of 4 for same cells and transmission lines. α_{in}' can be lowered with the reduction of Z_{S} but at the price of lower gains. Equation (3.7) quantifies this trade-off for TWAs. The gain of distributed amplifiers is here presented again isolating the low-frequency

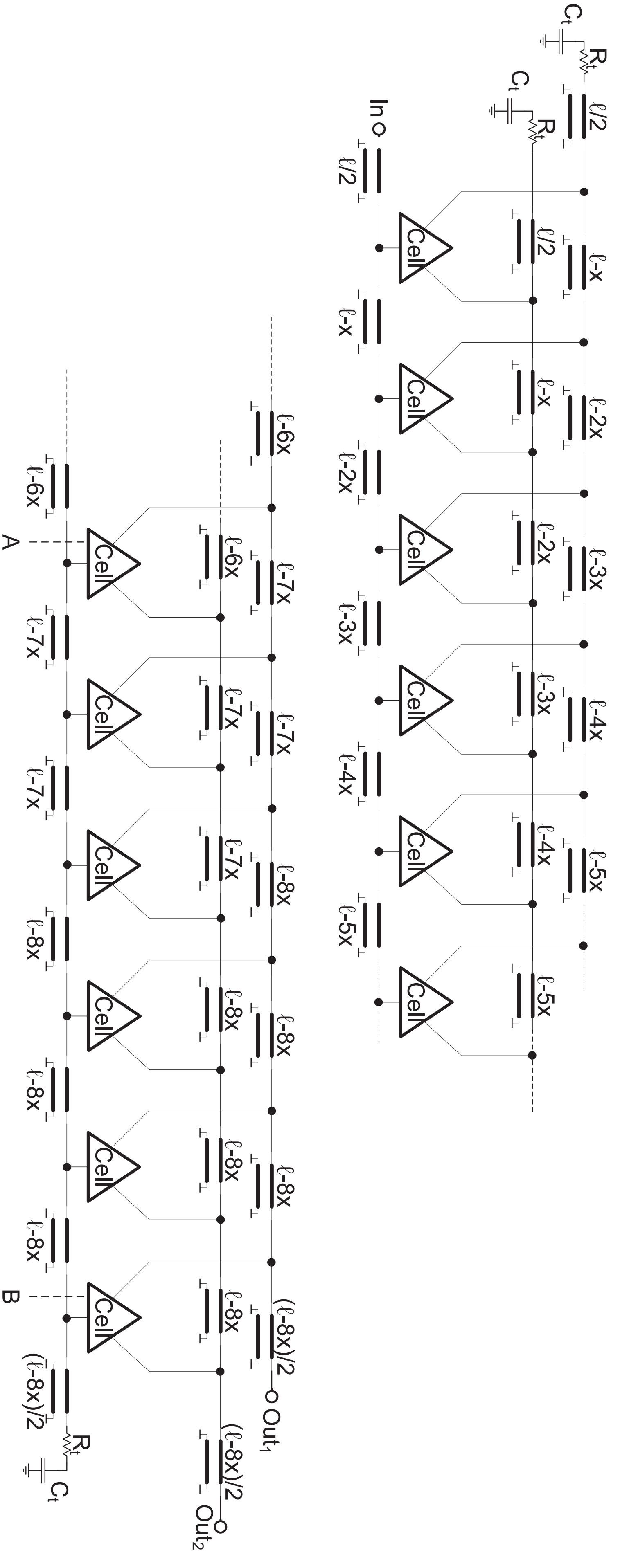

C_t
R_t
ℓ/2
C_t
R_t
In
ℓ/2
ℓ/2
Cell
ℓ-x
ℓ-x
ℓ-x
ℓ-2x
ℓ-2x
ℓ-2x
ℓ-3x
ℓ-3x
ℓ-3x
ℓ-4x
ℓ-4x
ℓ-4x
ℓ-5x
ℓ-5x
ℓ-5x
ℓ-6x
ℓ-6x
ℓ-6x
A
ℓ-7x
ℓ-7x
ℓ-7x
ℓ-8x
ℓ-8x
ℓ-8x
B
(ℓ-8x)/2
(ℓ-8x)/2
(ℓ-8x)/2
Out_1
Out_2
R_t
C_t

Figure 4.20: Circuit schematic of the developed traveling-wave divider: 12 gain cells are embedded in a tapered architecture.

part [15, 30, 37]:

$$G_{TWA,LF} = \Big(\frac{nG_{\mathrm{m}}Z_{\mathrm{S}}}{2}\Big)^2 \tag{4.8}$$

and highlighting the distance between the cell ℓ [15, 30, 37]:

$$G_{TWA} = G_{TWA,LF}\Big(1 - \frac{n\alpha_{\mathrm{in}}{}'\ell}{2}\Big)^2 \tag{4.9}$$

The solution employed in the developed TWD to reduce α_{in}' without sacrificing the gain excessively, is the tapering of the synthetic impedance consisting of a progressive reduction of $\mathrm{Z_S}$ in the direction of propagation of the input signal. To further reduce the impact of the synthetic-line losses on the TWD response, they have also been compensated by increasing an $\mathrm{G_m}$, as done in the TWA presented in Section 3.3. The two techniques are described in the following paragraphs.

Tapering of the Synthetic-Line Impedance Fig. 4.20 shows the complete schematic of the divider. It consists of 12 gain cells connected with on-chip microstrip lines. Their inductance and capacitance per unit-of-length are 0.5 µH/m and 80 pF/m, respectively, which corresponds a characteristic line impedance of 79 Ω.

The tapering of the synthetic-line impedance is achieved, as quantified in eq. (3.4), reducing the distance between the cells in the direction of propagation of the input signal. The length of each line is annotated on the circuit schematic in Fig. 4.20. The initial length *ell* of the lines is 100 µm, while the tapering parameter x has been set to 8 µm. Indeed, the tapering is also beneficial for the silicon footprint of the circuit, which is reduced due to the smaller distance between the gain cells.

The response of the TWD in case of tapering can be still approximated by eq. (4.9) with suitable adjustments. The term $n\alpha_{\mathrm{in}}{}'\ell$ indicates that at each section of the TWA the input signal sees an attenuation constant $\alpha_{\mathrm{in}}{}'$. In the case of tapering, on the other hand, for each section the attenuation constant is different. This can be taken into account by modifying eq. (4.9) inserting the summation of the attenuation in each section in place of the term $n\alpha_{\mathrm{in}}{}'\ell$:

$$\Big(1 - \frac{n\alpha_{\mathrm{in}}{}'\ell}{2}\Big) \rightarrow \Big(1 - \frac{1}{2}\sum_{i=k}^{n} \alpha_{in,k}{}'\ell_k\Big) \tag{4.10}$$

The attenuation in the k^{th} section $\alpha_{\mathrm{in,k}}$' is calculated taking into consideration the synthetic-line characteristic impedance of the section, which is expressed as:

$$Z_{\mathrm{S,k}} = \sqrt{\frac{L'}{C' + \frac{C_{\mathrm{in}}}{\ell - k\cdot x}}} \tag{4.11}$$

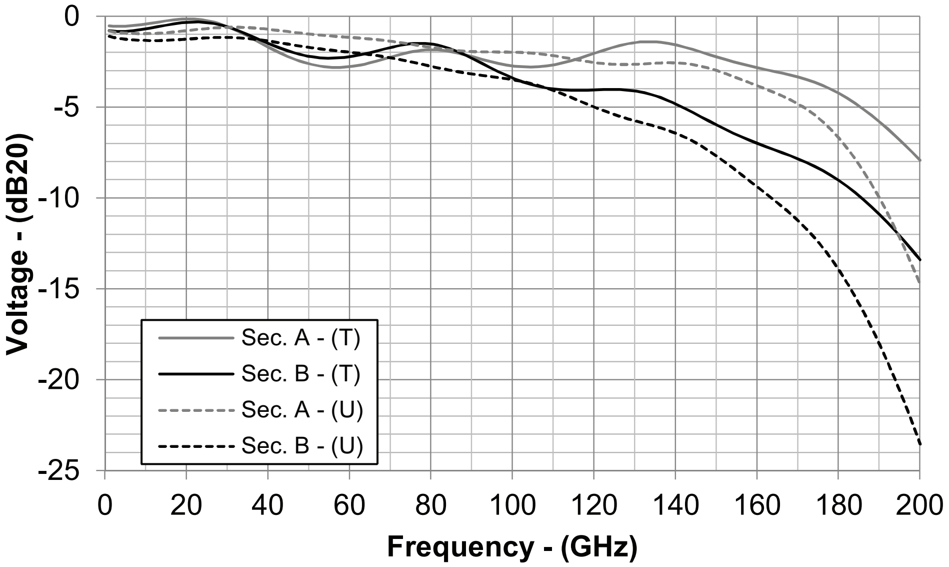


Figure 4.21: Voltage probed at section A and B of the presented TWD (Fig. 4.20) for the case of tapering (T) and uniform length (U) of the transmission lines.

The impact of the tapering on the amplifier response is illustrated in Fig. 4.21, where the input voltages of the cells, probed at different points, are shown for the presented design, and also compared against the case of no tapering. As it can be seen, the attenuation in the input line for the case of tapering is reduced against the conventional case. This effect is enhanced where the synthetic losses are more significant, i.e., toward high frequency and for the cells further away from the amplifier input.

Furthermore, the tapering increases the output power of the system redirecting more current to the output. In fact, since the impedance of the synthetic lines decreases toward the output, the current injection into the lines is favored in the direction of the final load rather than that of the termination resistor. In literature, several works have reported analytical expressions of the gain of tapered distributed amplifiers [65, 66]. The theory of small reflections must be used to calculate the load seen at the output of each cell [65]. The estimation of this impedance is required to determine the amount of cell output-current $\mathrm{i_{out}}$ directed toward the load $i_{\mathrm{out,L}}$, and toward termination resistor $i_{\mathrm{out,T}}$. In case of uniform distributed amplifiers i_{out} splits equally in the two directions leading to the term 1/2 in eq. (4.9). In case of tapering the calculation of $i_{\mathrm{out,T}}$ and $i_{\mathrm{out,L}}$ leads to bulky equations, which are not practical as design guidelines. An approximate, yet sufficiently accurate, and compact calculation of these currents can be done assuming that each cell sees at the output only the parallel between the two synthetic-line impedances of the section k^{th} and $(\mathrm{k}+1)^{th}$ where the cell is attached. With the help of eq. (4.11) then the relation between $i_{\mathrm{out,L}}$ and i_{out} can be calculated as:

$$i_{\mathrm{out,L}} = i_{\mathrm{out}} \cdot T(k) \tag{4.12}$$

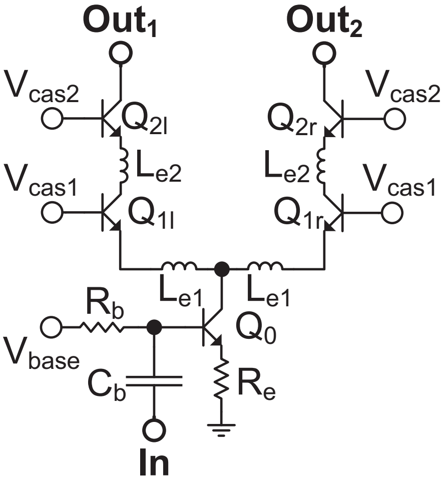


Figure 4.22: Circuit schematic of gain cell used in the TWD of Fig. 4.20.

$$T(k) = 1 - \frac{(1+k)\cdot x - \ell + \sqrt{(\ell - kx)(\ell - kx - x)}}{x} \tag{4.13}$$

which reduces again to 1/2 for x approaching 0. The gain of the non-tapered distributed amplifier expressed in eq. (4.9) can be then generalized to the case of tapering with eq. (4.10), (4.11) and (4.13) as:

$$G_{TWD} = \left(1 - \sum_{k=1}^{n} T(k) G_m Z_{S,k}\right)^2 \cdot \left(1 - \frac{1}{2}\sum_{k=1}^{n} \alpha_{in,k}\ell_k\right)^2 \tag{4.14}$$

Indeed eq. (4.14) is an approximated evaluation of the gain of tapered distributed amplifiers, but its compact expression makes it a useful tool in the design phase. Section 4.3.2 will validate eq. (4.14) with measurement results.

Gm-Boosted Gain Cell Fig. 4.22 presents the schematic of the cell employed in the TWD. The circuit consists of an input transistor $\mathrm{Q_0}$ in the common-emitter configuration, with one pair of two stacked transistors $\mathrm{Q_{1\text{-}2,l\text{-}r}}$ in the common-base arrangement. The advantages of the conventional cascode listed in Section 3.3.1 are retained by this gain element. The power-divider capability is provided by the cell via the $\mathrm{Q_{1\text{-}2,l\text{-}r}}$ transistors, which split the signal-current of $\mathrm{Q_0}$ in two, and redirect them toward the two outputs of the cell.

Additionally, the proposed gain element is conceived to compensate and minimize the synthetic-losses. The compensation is achieved via positive feedback between the inductors $\mathrm{L_{e,1\text{-}2}}$ and the parasitic transistor capacitances. The resonance between these elements produces the increase of the cell $\mathrm{G_m}$ toward high frequency, as already discussed in Section 3.3. Fig. 4.23 shows the effect of the peaking on the transconductance of the cell and on the divider gain for the de-

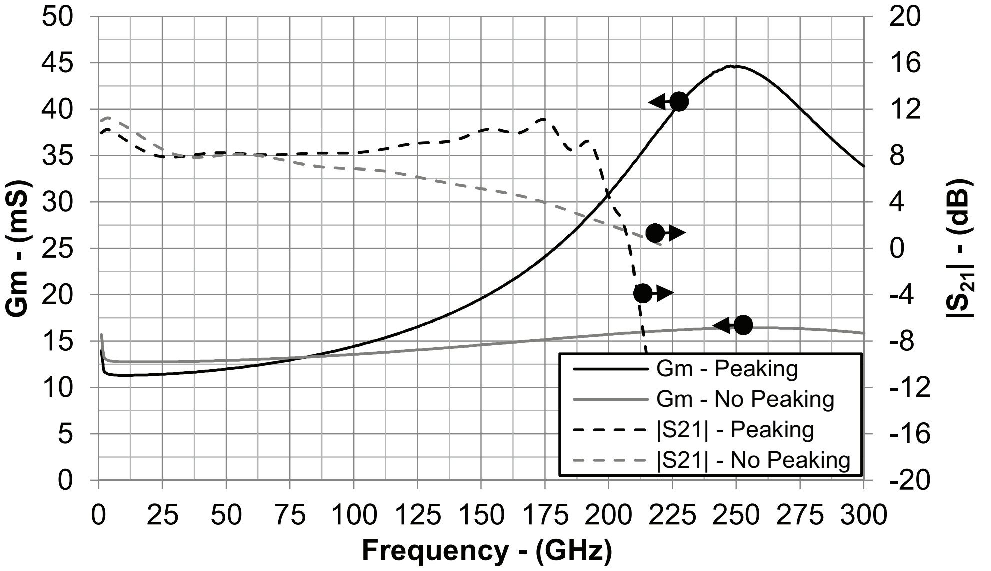


Figure 4.23: Simulated G_m and TWD response for the presented cell, compared against the conventional approach with equal design parameters but without inductive peaking.

sign values of this work, and it compares them against the conventional approach without peaking. The G_m increases with frequency from 40 GHz to 260 GHz. Since the TWD gain is proportional to ${G_m}^2$, this trend has been engineered to compensate the synthetic-line losses α_{in} and to extend toward higher values the maximum frequency of operation of the system. To minimize α_{in} the capacitive division technique has been employed: the capacitor C_b of 40 fF is in series with the base of Q_0 to lower the equivalent input capacitance of the cell [15].

The transistors of the cell have an emitter area of $5\times0.9\times0.07\,\mu m^2$, while the inductor $L_{e,1}$ is 9 pH, and $L_{e,2}$ is 14 pH. Finally, the resistor R_e is used to stabilize the cell transconductance against process variations. Its value is $10\,\Omega$. With this design choices, the input equivalent cell resistance and capacitance R_{in} and C_{in} are $12\,\Omega$ and 21 fF, respectively. These values, in conjunction with the simulated cell-transconductance presented in Fig. 4.23, will be used in Section 4.3.2 to validate the gain approximation of eq. (4.14) with the measurement results.

4.3.2 Experimental Characterization

Fig. 4.24 shows the micro-photograph of the fabricated TWD. The total area of the die is $0.8\,mm^2$, while the active area of the circuit is $0.1\,mm^2$. All the measurements presented in this section have been acquired on-chip with bias operation point $I_{CC} = 100\,mA$ and $V_{CC} = 3\,V$.

The *S-Parameters characterization* of the divider was performed with a vector network analyzer from 200 MHz to 67 GHz; extender modules were required from 90 GHz to 140 GHz, and from 140 GHz to 220 GHz. Due to the lack of equipment for the differential S-Parameter measurements above 60 GHz, the divider path-gain was measured with a single-ended setup, which probes contacting the die

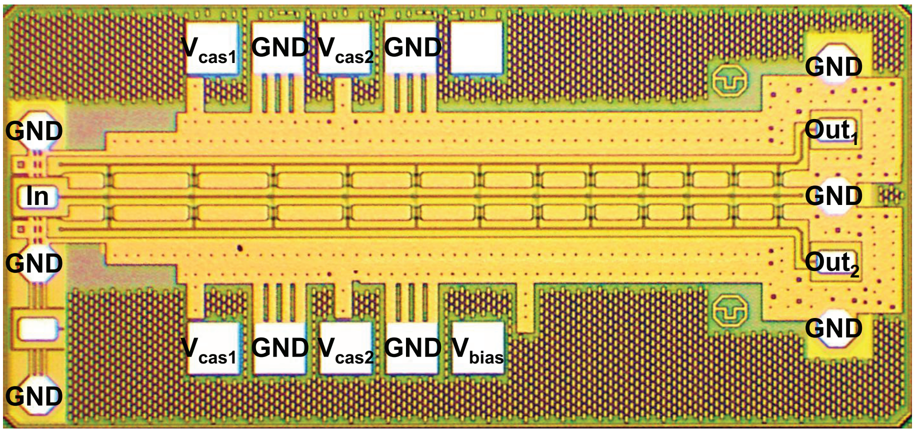

V_{cas1}
GND
V_{cas2}
GND
GND
GND
Out$_1$
In
GND
GND
Out$_2$
GND
V_{cas1}
GND
V_{cas2}
GND
V_{bias}
GND

Figure 4.24: Micro-photograph of the fabricated TWD [Testa9]: the dimensions of the chip are 0.6 mm×1.3 mm, while the chip area is 0.8 mm^2.

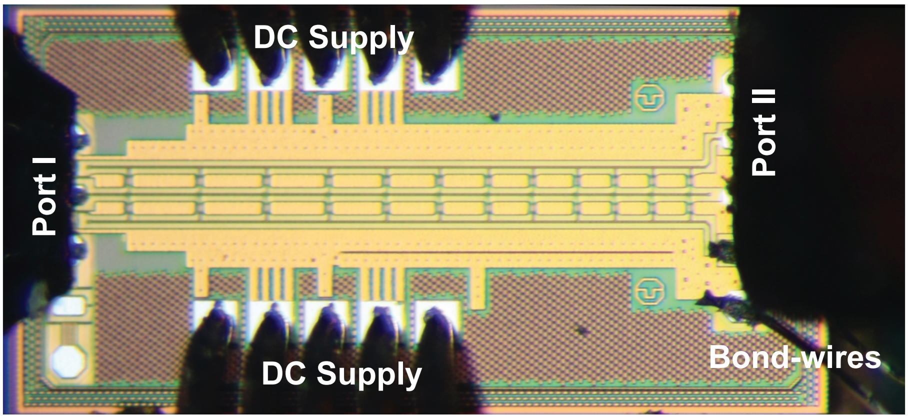

DC Supply
Port I
Port II
DC Supply
Bond-wires

Figure 4.25: Micro-photograph of the TWD contacted with single-ended probes. The divider input port is contacted with the first port of the measurement system, while one of the outputs of the divider is attached to port II of the setup.

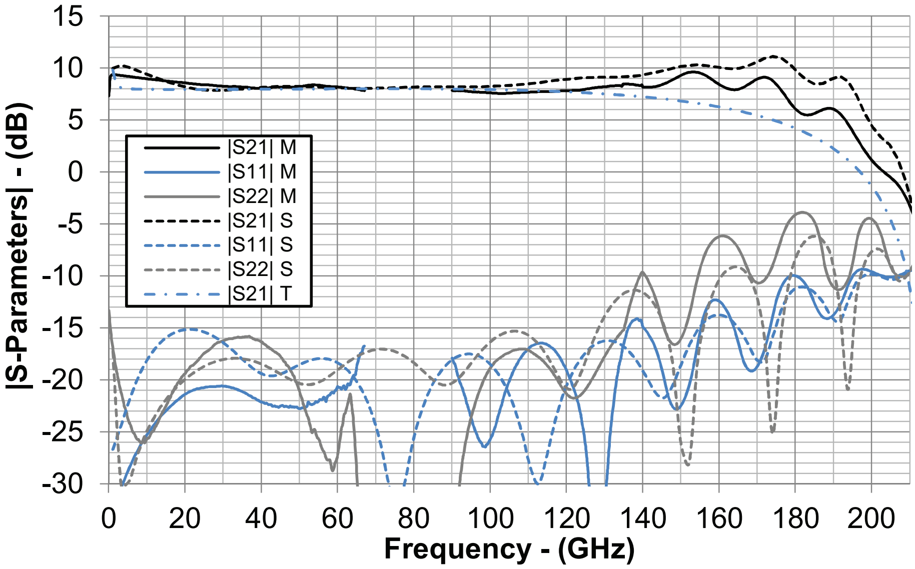


Figure 4.26: Measured (M), simulated (S) and calculated with eq. (4.14) (T) S-Parameters of the TWD in Fig. 4.24.

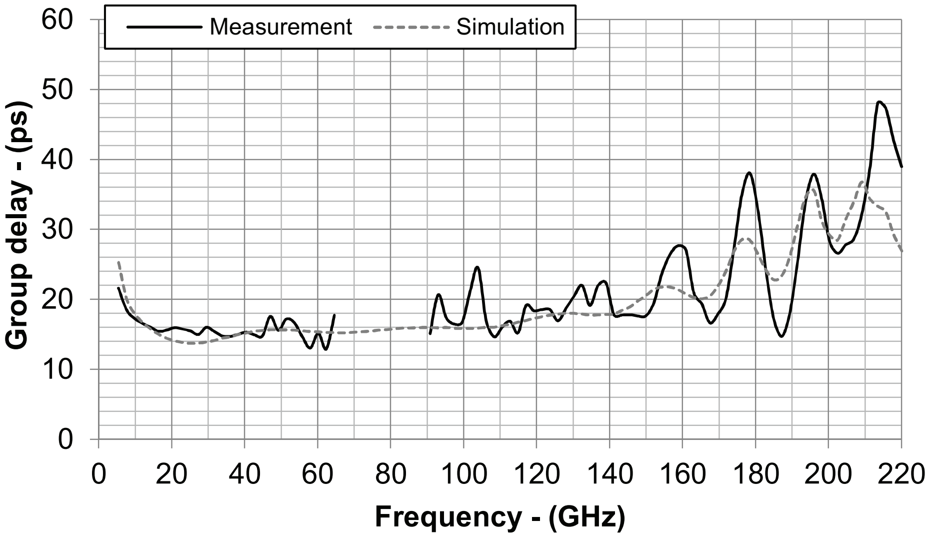


Figure 4.27: Measured and simulated group delay of the TWD in Fig. 4.24.

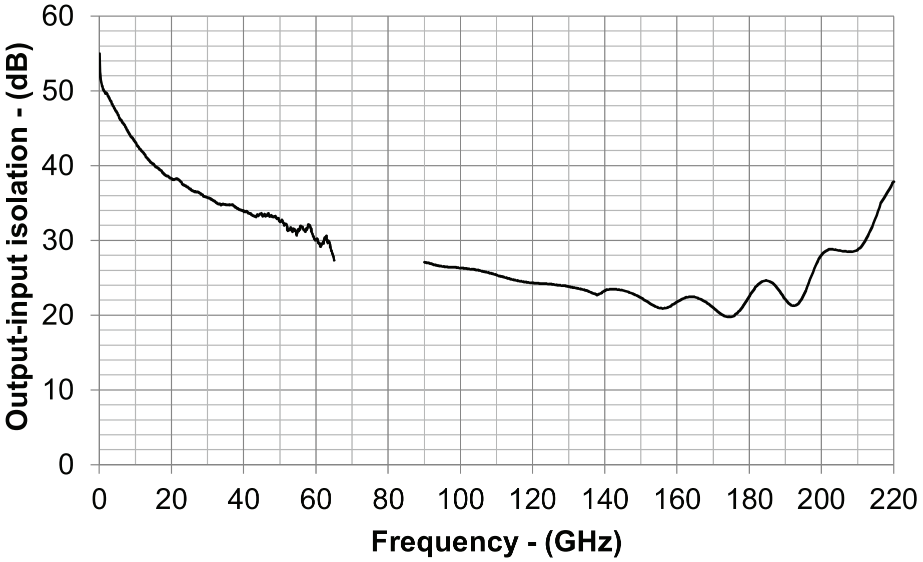


Figure 4.28: Measured output to input isolation of the TWD in Fig. 4.24.

are shown in Fig. 4.25. Fig. 4.26 shows the S-Parameters of the TWD as measured, simulated and calculated with eq. (4.14) with all the three in agreement. The divider provides a gain with a maximum value of 10 dB and a −3 dB bandwidth from 300 MHz to 180 GHz. The circuit analysis predicts the gain and the −3 dB upper-corner frequency correctly. The useful frequency band of the component, defined as the band where the gain is above 0 dB, spans from 100 MHz to 200 GHz. Fig. 4.26 also shows the measured and simulated input and output matching: $|S_{11}|$ is below −10 dB for the whole −3 dB frequency band, while $|S_{22}|$ is below −10 dB up to 155 GHz, and it reaches −5 dB at 200 GHz.

The *group delay characterization* has been derived from the phase ϕ_{21} of the measured S_{21} as expressed in eq. (3.12). Fig. 4.27 shows the comparison between measurement and simulation: the group-delay variations are less than 26 ps over the 180 GHz-wide −3 dB-frequency-band of the divider.

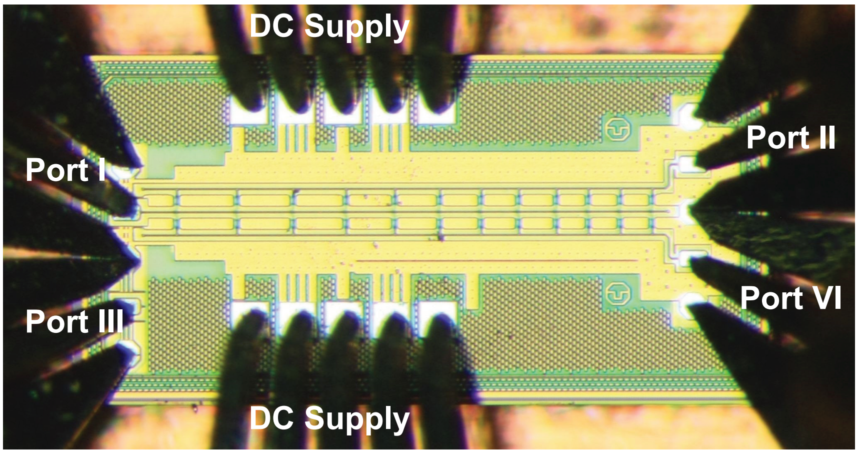


Figure 4.29: Micro-photograph of the TWD contacted with differential probes. The ports of the measurement system are also annotated. Port III contacts a dummy pad required for the landing of the differential probe on the input side of the divider.

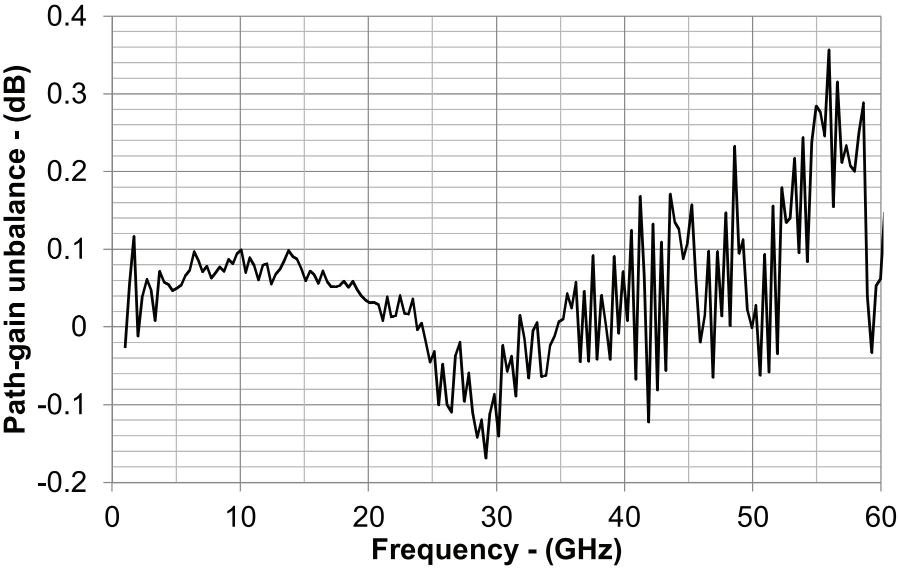


Figure 4.30: Measured gain-unbalance between the two paths of the divider in Fig. 4.24.

The *output to input isolation* has been also characterized, and the measurement result is shown in Fig. 4.28. The isolation is above 30 dB up to 60 GHz, while it decreases down to the minimum value of 20 dB at 175 GHz.

Of particular interest for this class of circuits is the *balance between the response of the output paths*. A differential S-Parameters measurement has been performed to experimentally characterize the balance between the two outputs of the components. Fig. 4.29 presents the micro-photograph of the divider contacted with differential probes. As it is shown, port I of the measurement systems feeds the input of the divider, while port II and IV acquire the outputs. Port III contacts a dummy pad required by the input differential-probe to land on the chip surface. Furthermore, although port III is not used for the measurement,

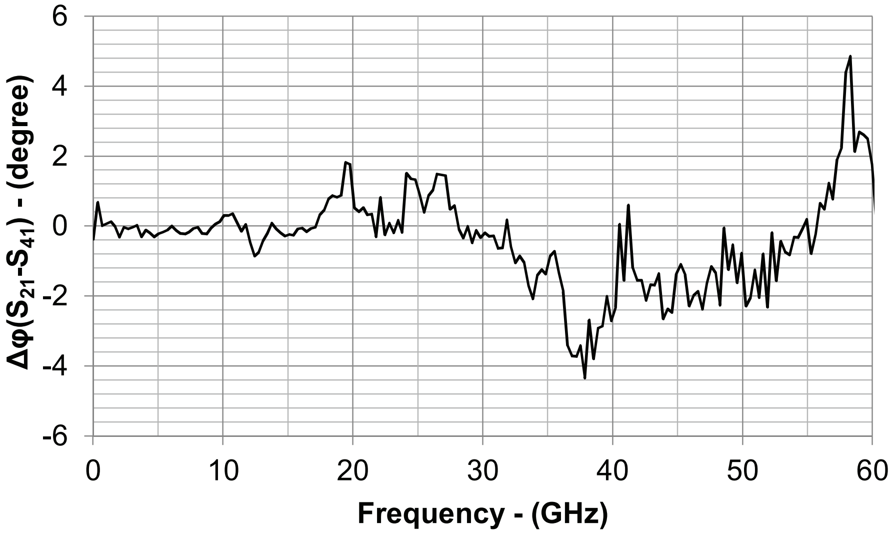


Figure 4.31: Measured insertion-phase unbalance between the two paths of the divider in Fig. 4.24. Fig. 4.29 illustrates the configuration of the measurement-system ports.

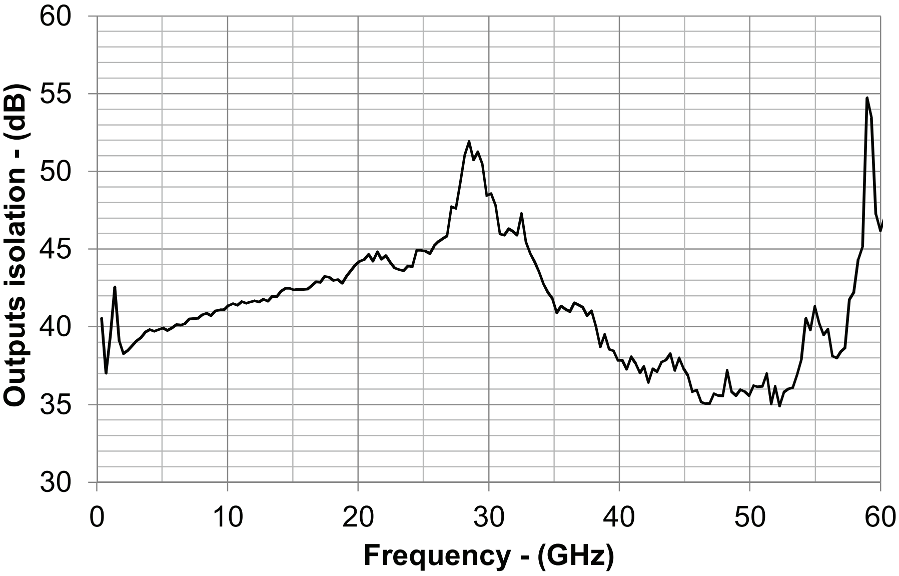


Figure 4.32: Measured isolation between the output ports of the divider in Fig. 4.24.

this port was necessary for the differential S-Parameter calibration. The measured gain and insertion-phase unbalances are presented in Fig. 4.30 and 4.31, respectively. From 200 MHz up to 60 GHz the measured path-gain unbalance is below 0.3 dB, while the measured insertion-phase unbalance is below 4°. Such marginal asymmetries between the responses of the outputs result from the symmetric divider architecture, which this work proves superior to other approaches such as interleaved dividers [58].

The differential S-Parameters measurement setup was also employed to characterize the *isolation between the output ports* of the divider, which is referred to as output isolation in this manuscript. The experimental results are in Fig. 4.32.

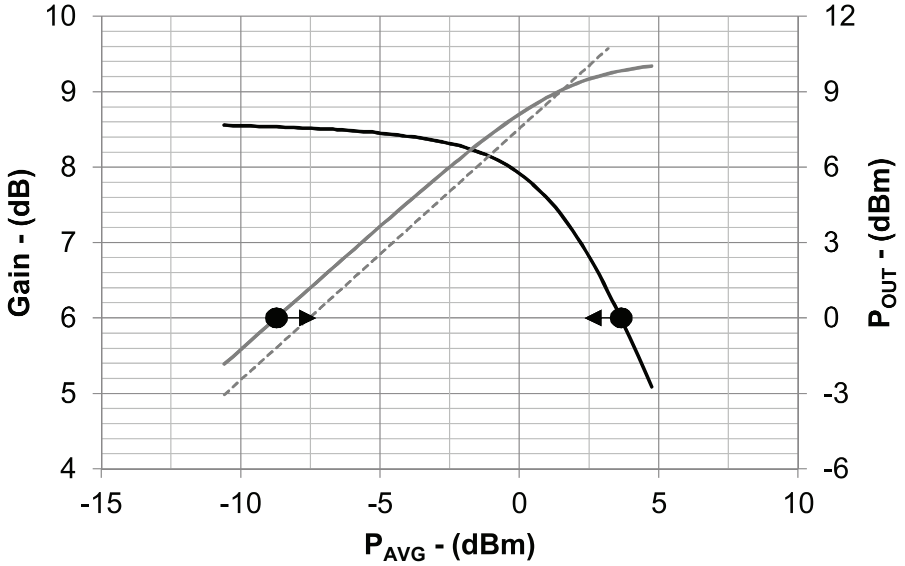


Figure 4.33: Measured gain-compression curve of the divider in Fig. 4.24 for a working frequency of 20 GHz.

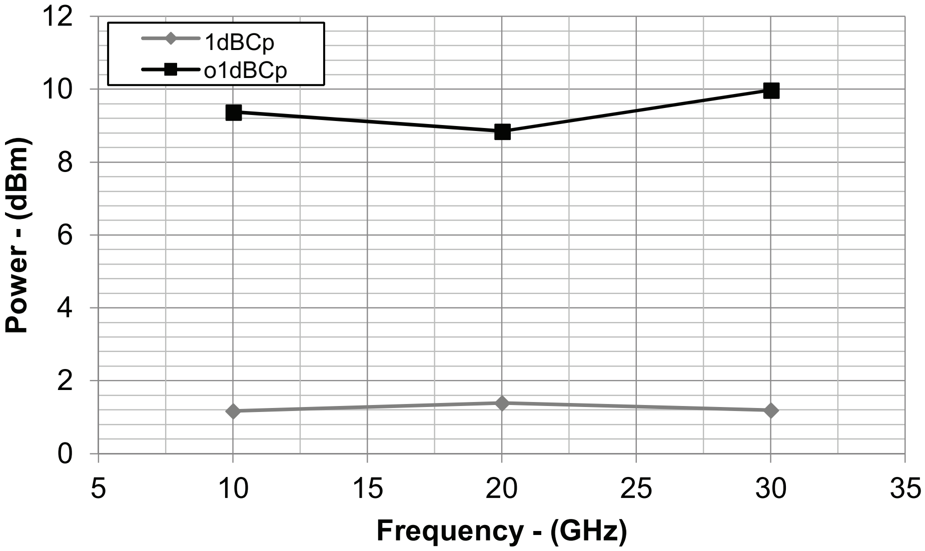


Figure 4.34: Measured input and output power in 1 dB compression of the gain of the divider in Fig. 4.24 plotted versus the frequency.

The output isolation is better than 35 dB from 200 MHz to 60 GHz. The differential measurements, which enabled the characterization of the output isolation and the unbalance between the path responses, are presented only up to 60 GHz that is the highest observable frequency with the available equipment.

The *large-signal characterization* has been performed using the same setups of the small-signal characterizations with the addition of a power meter to calibrate and measure the input and output power of the component. The measured gain-compression curve is presented in Fig. 4.33 for a frequency of operation of 20 GHz, while Fig. 4.34 shows the i1dBCp and o1dBCp as the function of the frequency in the band from 10 GHz to 30 GHz. The maximum measured i1dBCp and o1dBCp are 1.2 dBm and 10 dBm at 30 GHz. Such relatively good linearity

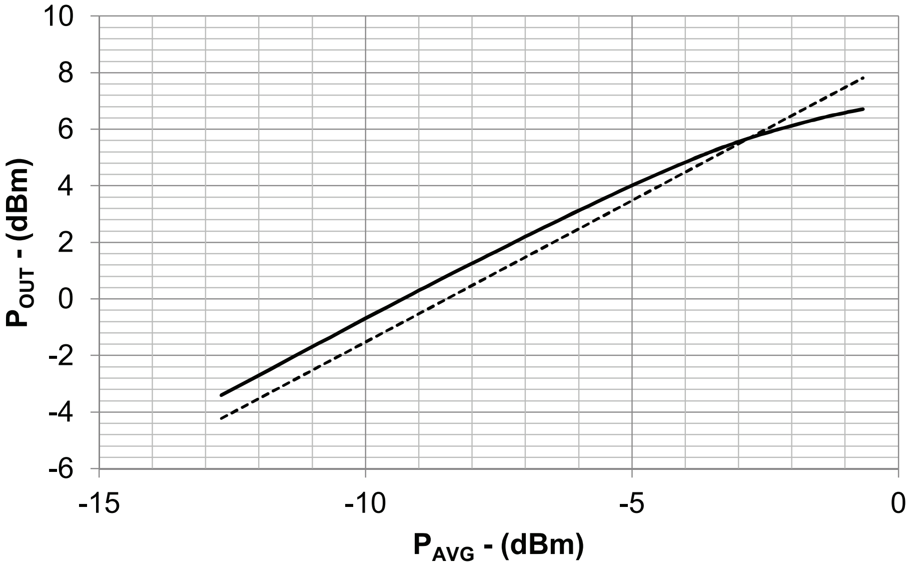


Figure 4.35: Measured gain compression-curve of the divider in Fig. 4.24 for a working frequency of 140 GHz.

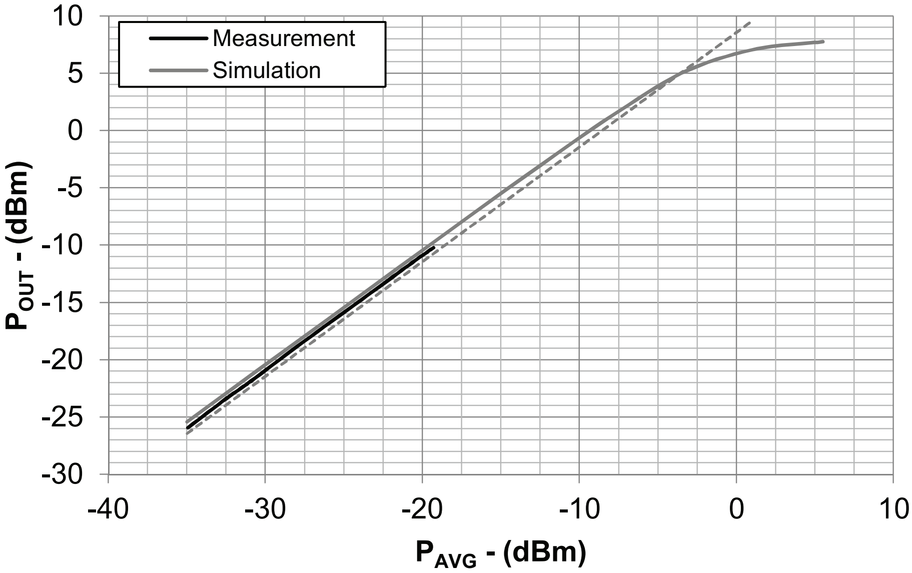


Figure 4.36: Simulated gain compression-curve at 160 GHz of the divider in Fig. 4.24, and measured output power at the same frequency versus the available generator power P_{AVG}.

performance is achieved by the triple-stacked cascode gain-cell, which allows increasing V_{CC} enabling, in turn, an output swing larger than the common-emitter or cascode cells. The high values of i1dBCp and o1dBCp prevented their measurement above 30 GHz, as the available equipment was not able to provide enough power to compress the gain by 1 dB. The same issue also limited the setups used for characterize the bands 90 GHz – 140 GHz and 140 GHz – 220 GHz. In the first frequency range, the converter module was able to generate enough power to compress the gain only at 140 GHz. At this frequency, an i1dBCp of −3 dBm and an o1dBCp of 5.6 dBm were observed, as Fig. 4.35 shows. For the frequency range of characterization 140 GHz – 220 GHz, it was not possible to compress the divider gain with the power generated by the extender module. Fig. 4.36 shows the simulated gain-compression curve for a working frequency of 160 GHz. This simulation result is also compared against measurement, showing good agreement in the range where it was possible to characterize the linearity of the circuit. Moreover, the simulation enabled to estimate an o1dBCp of 5 dBm at 160 GHz.

4.3.3 Discussion of the Results

A distributed power divider for wideband applications has been designed and fabricated with the *SG13G2* technology in an active area of 0.1 mm^2 [Testa9]. Consuming 300 mW, the circuit provides a gain of 10 dB over the −3 dB-bandwidth from 300 MHz to 180 GHz, which crosses 0 dB at 100 MHz and 200 GHz. The circuit analysis has been provided to express the path gain with an approximate, yet compact and accurate, formula suited for tapered distributed-amplifiers. The design of the divider has been presented in detail, focusing on the $\mathrm{G_m}$-boosted gain-cell, based on a triple-stacked cascode topology. This type of gain element was used for the first time in this work to compensate the synthetic-line losses and extend the upper frequency of operation of distributed dividers.

Table 4.5 presents an overview of the state of the art for this class of circuit. The presented design shows the highest frequency of operation, as well as the widest bandwidth of amplification. In fact, for BiCMOS processes [59, 60], the state of the art is improved by a factor of 10 from 20 GHz to 200 GHz for the highest operation frequency, which is defined as the frequency where the divider gain crosses 0 dB. Extending the comparison to other technologies, the highest frequency of operation reported is 40 GHz [58], which this work improves by a factor 5. The presented advancements are enabled by the $\mathrm{G_m}$-boosted gain cell and the tapered design technique, which compensate and minimize the input synthetic-line losses, identified as the main limiting factor toward applications at high frequency of distributed power dividers. These techniques also enabled a higher supply voltage, resulting in an improved divider linearity and in the highest o1dBCp so far reported. Finally, the symmetric layout and architecture of the divider ensured low unbalance between the responses of the divider paths, with superior performance compared to asymmetric approaches [58].

Table 4.5: State of the art of distributed power dividers.

Ref.	[64]	[63]	[62]	[61]	[60]	[59]	[58]	**This work**
Gain>0 dB‡ (GHz)	1-10.6	1-20	2-18	0-20	2-30	2-30	0-40	0.1-200
3-dB BW (GHz)	8	18	16	10	20	21.5	25	180
Supply (V)	1.8	5	NA	2.5	2.5	NA	3	3
P_{DC}(mW)	20.5	NA	NA	160	100	66	NA	300
Gain (dB)	9.5	10	4	5	9.6	11	6	10
Gain Stages	2	5	2	2	2	1	5	12
o1dBCp (dBm)	7.5@5GHz	n.a.	4@6GHz	0@15GHz	2@10GHz	-5.4@12GHz -8.9@22GHz	5@40GHz	10@30GHz 5.6@140GHz
O-iso* (dB)	n.a.	n.an	n.a.	30@10GHz	22@2GHz	25@20GHz	30	35
OI-iso** (dB)	n.a.	60@10GHz	40@12GHz	n.a.	30@2GHz 35@25GHz	n.a	n.a.	30@60GHz 25@170GHz
Δtp/BW (ps/GHz)	n.a.	n.a.	n.a.	100/25	20/25	16/18	n.a	26/180
ΔGain† (dB)	n.a.	n.a.	n.a.	1@18GHz	0.8@15GHz	0.2@15GHz	2@40GHz	0.35@55GHz
ΔPhase† (°)	10/10	n.a.	n.a.	1@18GHz	3.5@15GHz	1.6@15GHz	14@40GHz	5@55GHz
Technology	130 nm CMOS	150 nm GaAs	200 nm GaAs	180 nm CMOS	130 nm SiGe	130 nm SiGe	90 nm CMOS	130 nm SiGe

‡: Frequency region where the divider provides gain, *: Output isolation, **: Output to input isolation, †: Unbalance between the path responses.

5 Wideband Amplifiers based on Resonant Matching

5.1 Introduction

In the last years, Resonant-Matched Amplifiers (RMAs) have been demonstrated at millimeter wave frequencies with low dissipated powers and compact occupation areas [19]. These two characteristics are fundamental advantages with respect to DAs, which, conversely, enjoy wider frequency bands of operation since the matching does not require resonance phenomena.

Indeed, low power dissipation is beneficial for portable systems that cannot access to an abundant source of energy. Portable solutions, moreover, are expected in the next years to make extensive use of millimeter waves and UWBs. Best examples are the internet of things and industry 4.0. Typical portable applications require not only transceivers and sensing hardware, but also digital circuitry for data processing. SiGe BiCMOS technologies are good candidates for the integration of such systems since – as bulk and SOI CMOS – they allow embedding large digital blocks, and, in addition, they offer SiGe-HBTs suited explicitly for millimeter-waves. Antennas, front-ends and digital components can be then integrated reducing interface losses and packaging costs. Finally, the low-power requirement usually imposes low-voltage designs, thereby limiting the performance of sub-systems operating at millimeter waves.

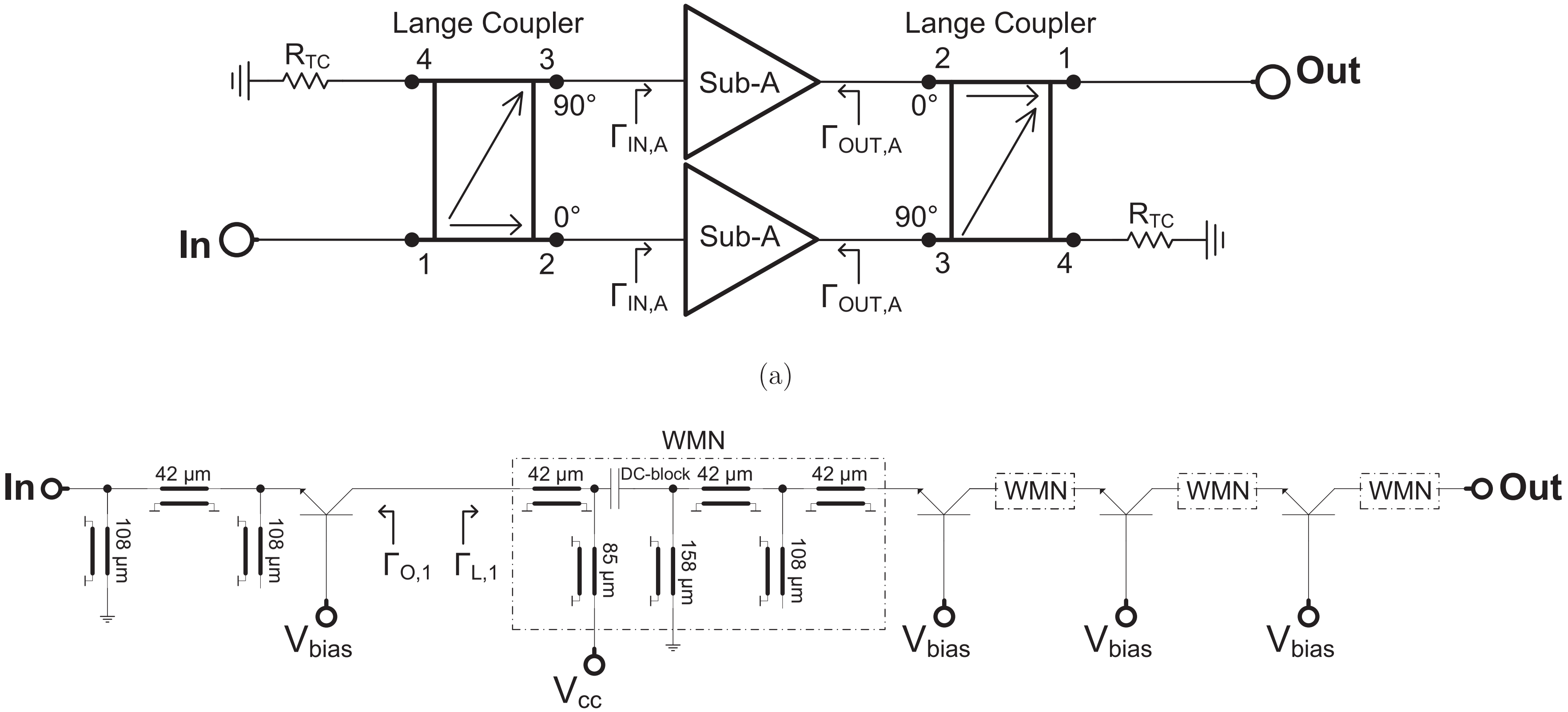
For all these motivations there is a keen research interest for low-power and low-voltage RMAs operating at millimeter waves with suitable performance. Furthermore, within this thesis, the need of a benchmark for the DAs capabilities motivated the development of RMAs. This chapter presents the obtained results.

5.2 210-GHz Low-Power Amplifier

This recearch produced a UWB RMA for operation at 200 GHz [Testa3]. The Common-Base (CB) configuration has been adopted since at millimeter-wave frequencies CB amplifiers demonstrated performance comparable to cascode circuits but requiring just half of the power and voltage supply [Testa3, 67]. The following sections describe the design of the circuit and the achieved experimental results.

5.2.1 Circuit Design

Fig. 5.1a shows the schematic of the amplifier. The circuit consists of two Lange couplers, at the input and output, and two amplifiers driven in quadrature to form a balanced configuration. The two amplifiers, named here sub-amplifiers


Lange Coupler
R_{TC}
4
3
90°
0°
1
2
In
$\Gamma_{IN,A}$
$\Gamma_{IN,A}$
Sub-A
Sub-A
$\Gamma_{OUT,A}$
$\Gamma_{OUT,A}$
Lange Coupler
2
1
0°
90°
3
4
R_{TC}
Out
WMN
In
42 µm
108 µm
108 µm
V_{bias}
$\Gamma_{O,1}$
$\Gamma_{L,1}$
42 µm
DC-block
42 µm
42 µm
85 µm
158 µm
108 µm
V_{cc}
V_{bias}
WMN
V_{bias}
WMN
V_{bias}
WMN
Out

(a)

(b)

Figure 5.1: (a) Schematic of the developed RMA, (b) schematic of the Sub-Amplifiers (Sub-A) embedded in the balanced architecture.

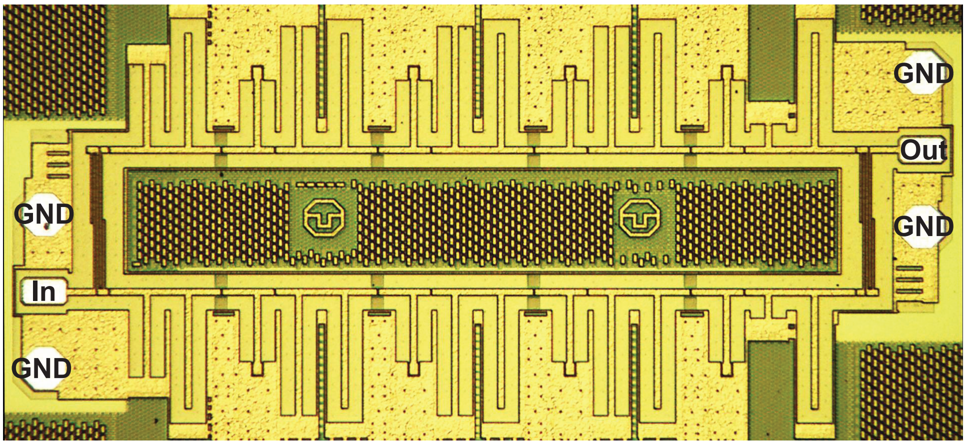


Figure 5.2: Micro-photograph of the fabricated RMA [Testa3]. The chip size is $0.8\,\text{mm}^2$.

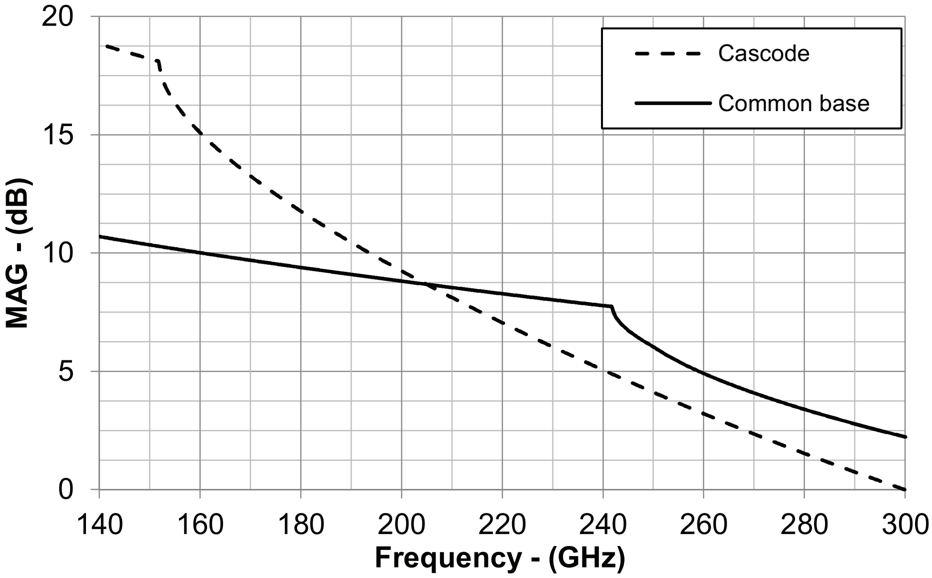


Figure 5.3: MAG comparison between cascode and common-base configurations for equal transistor size ($4{\times}0.9{\times}0.07\,\mu\text{m}^2$) and operating-point per device ($I_{CC} = 6\,\text{mA}$, $V_{CE} = 0.8\,\text{V}$).

(Sub-A), are formed by four cascaded common-base stages. Wideband Matching Networks (WMN in Fig. 5.1b), implemented with multiple stubs, provide the inter-stage connections and dc distribution. The chip is fabricated with the *SG13G2* technology presented in Section 2.1, and each HBT emitter has an area of $4{\times}0.9{\times}0.07\,\mu\text{m}^2$. A micro-photograph of the circuit is shown in Fig. 5.2. The main features of the amplifier are listed below.

Common-Base Approach Common-base amplifiers offer at the same time operation at high frequency and low dissipated power. To highlight this, the MAG (Maximum Available Gain) of CB and cascode amplifiers are compared in Fig. 5.3 for equal transistor size and operating-point per device ($I_{CC} = 6\,\text{mA}$, $V_{CE} = 0.8\,\text{V}$). Despite requiring half V_{CC} and P_{DC}, the MAG of the common base is equal to

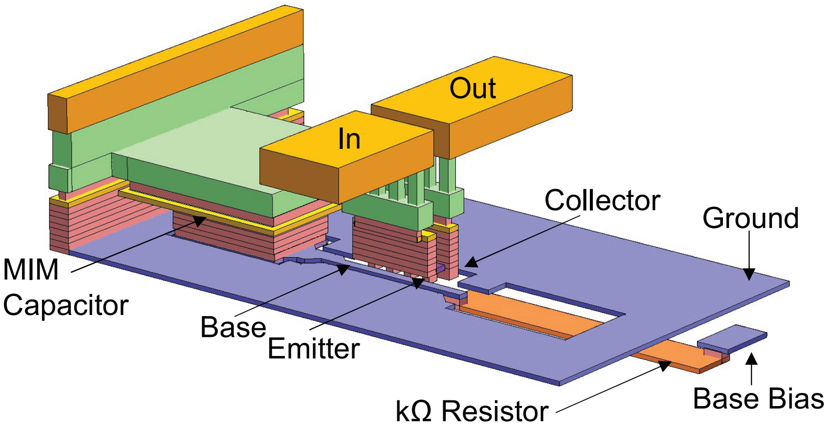

Out
In
Collector
Ground
MIM
Capacitor
Base
Emitter
kΩ Resistor
Base Bias

Figure 5.4: 3D view of one of the common-base stages embedded in the RMA of Fig. 5.2. To simplify the view only one of the MIM capacitors used to RF-shunt the transistor base is shown.

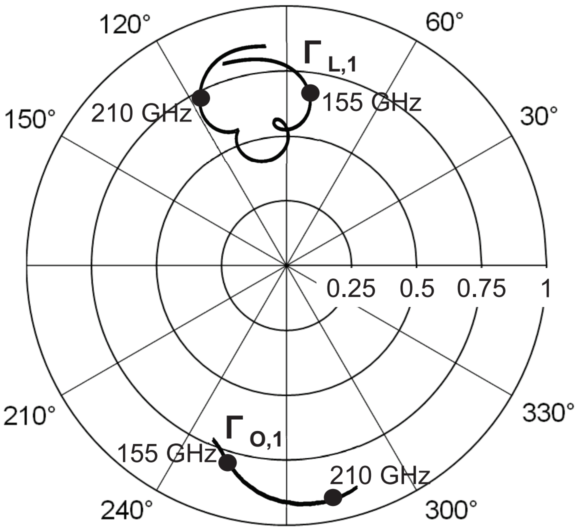


Figure 5.5: Polar plot representation of $\Gamma_{\mathrm{L},1}$ and $\Gamma_{\mathrm{O},1}$ of the designed RMA (Fig. 5.1) for the frequency range 140 GHz – 220 GHz.

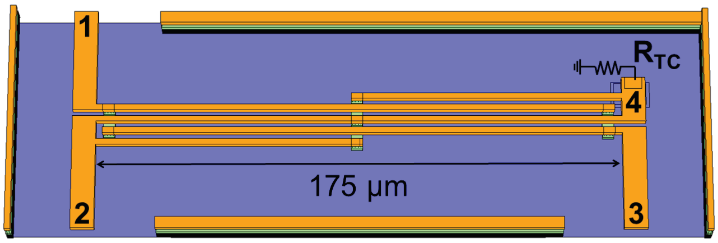

1
2
3
4
R TC
175 µm

Figure 5.6: 3D representation of the Lange coupler embedded in the RMA of Fig. 5.2. The ports are labeled, and also the physical dimension is annotated.

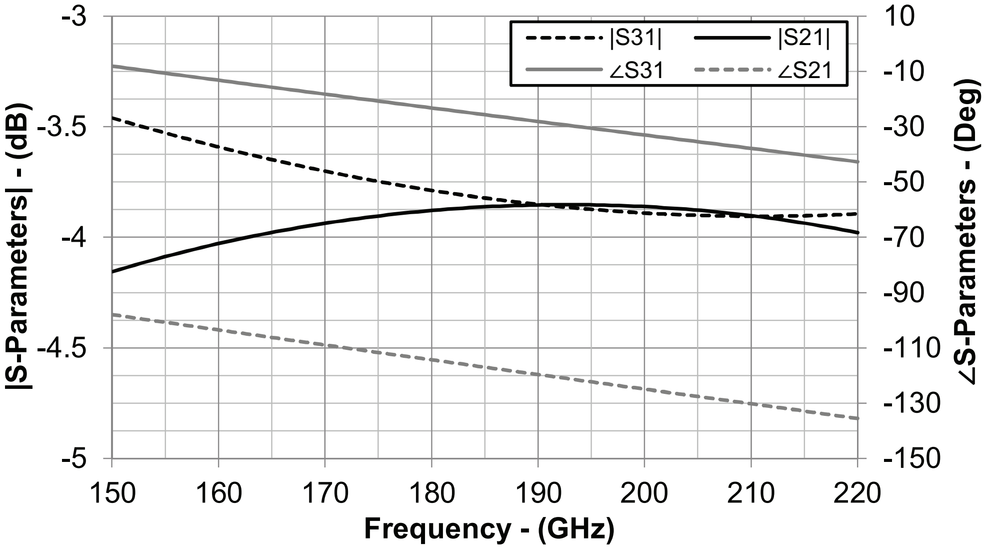


Figure 5.7: Simulated S-Parameters of the Lange coupler in Fig. 5.6.

the cascode one at 200 GHz and even bigger at higher frequencies. As a result, common-base amplifiers are preferable if high speed, low power, and low voltage applications are desired.

Other key points of CB circuits are the reduced Miller effect due to the positive transmission phase compared to the common emitter. At the same time, common base circuits also enjoy high isolation thanks to the small capacitance between emitter and collector, which results in little feedback from the output back to the input, providing therefore high stability. The layout of the transistor interconnections for the designed common-base stages is shown in Fig. 5.4.

Wideband Inter-Stage Matching Unlike cascode configuration, the impedances shown by common-base amplifiers are inductive at the input and capacitive at the output, easing the inter-stage matching of the sub-amplifier in Fig. 5.1b.

A multi-stub approach has been employed to maximize the amplifier bandwidth. $\Gamma_{\mathrm{L},1}$ and $\Gamma_{\mathrm{O},1}$ (Fig. 5.1b) are the load and the output reflection coefficient of the first CB stage. The designed matching networks ensured $\Gamma_{\mathrm{O},1}$ and $\Gamma_{\mathrm{L},1}$ close to the condition of conjugate matching over the whole amplifier band, as the polar plot in Fig. 5.5 shows. Similar considerations can be made for the other stages.

Balanced Architecture Good input and output matching are required to maximize the power gain and mitigate stability issues. When dealing with high frequencies, the optimization of $|S_{11}|$ and $|S_{22}|$ is particularly challenging due to the model inaccuracies of the employed devices and process variations. To offer robust matching to both load and generator impedance, a balanced architecture has been employed for the RMA including two Lange couplers at either side of the amplifier.

The 3D view of the couplers is shown in Fig. 5.6. The designed couplers split

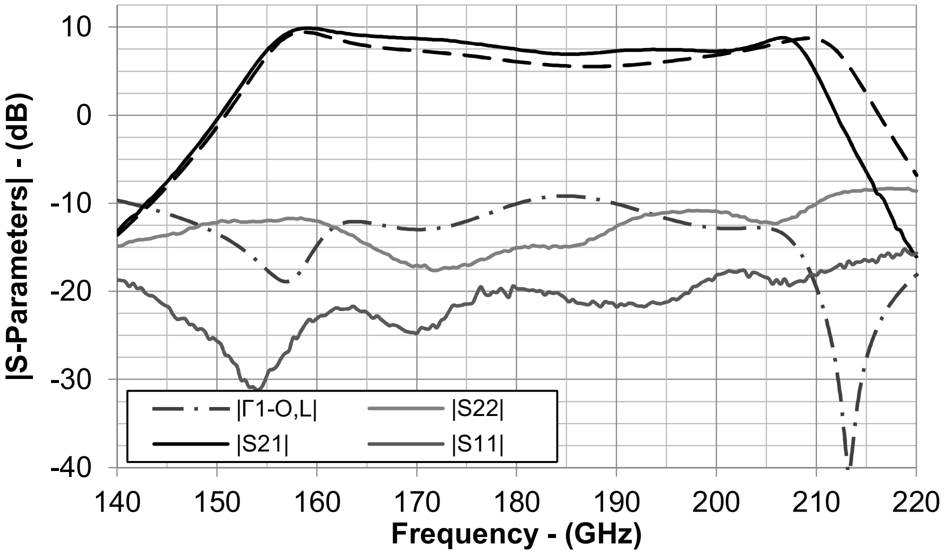


Figure 5.8: Measured S-Parameters, and comparison with the simulated $|S_{21}|$ (dashed) of the RMA in Fig. 5.2. $|\Gamma_{\text{1-O,L}}|$ calculated as in eq. (5.1) is also shown.

the power of port 1 to ports 2 and 3, and insert a relative phase-shift between them of 90°, while port 4 is isolated and terminated with a matched resistance R_{TC} of $50\,\Omega$. Fig. 5.7 shows the simulated S-Parameters of the coupler with the ports definition of Fig. 5.1. $|S_{31}|$ and $|S_{21}|$ are both $-3.8\,$dB at 200 GHz, hence at this frequency, the couplers divide the power at port 1 in half while inserting 0.8 dB of path losses.

As it is explained in detail in Section 3.7.1, the balanced architecture provides ultra-wideband input and output matching, which in this design covers the whole operating band of the amplifier. Section 5.2.2 will validate the technique with measurement results.

5.2.2 Experimental Characterization

The S-Parameters characterization was performed on-chip with wafer probes. A vector analyzer with frequency extension modules has been used for the experiment. The measurement results are shown in Fig. 5.8 for the bias point $I_{CC} = 21\,$mA and $V_{CC} = 0.8\,$V, resulting in a power consumption of 16.8 mW. The amplifier provides a gain of 10 dB over the $-3\,$dB-frequency-band 155 GHz – 210 GHz. This corresponds to a 30% relative bandwidth centered at 182.5 GHz. The power reflection coefficient $\Gamma_{\text{1-O,L}}$ between first and second common-base stages (Fig. 5.1) is defined as:

$$\Gamma_{\text{1-O,L}} = \frac{Z_{L,1} - Z_{O,1}*}{Z_{L,1} + Z_{O,1}} \tag{5.1}$$

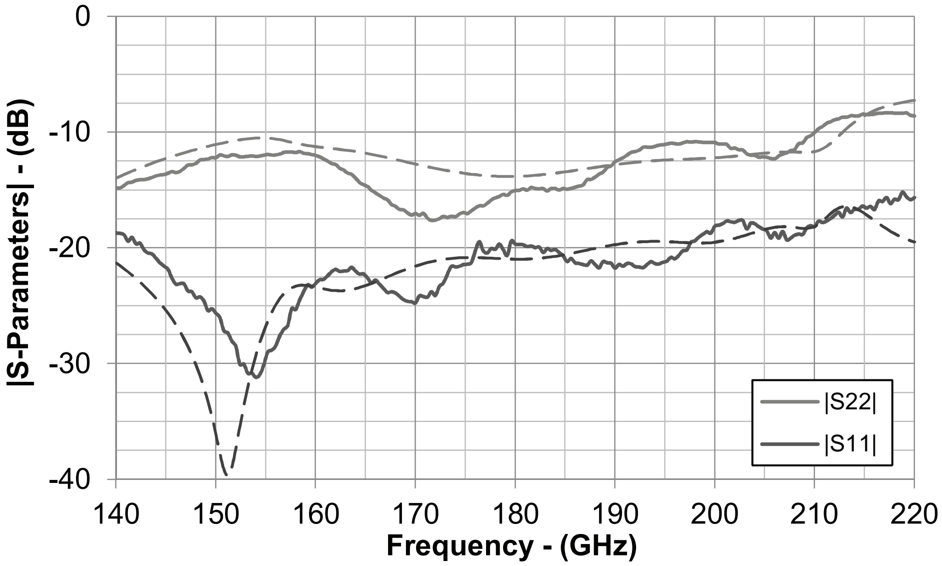


Figure 5.9: Measured (solid) and simulated (dashed) $|S_{11}|$ and $|S_{22}|$ of the RMA in Fig. 5.2.

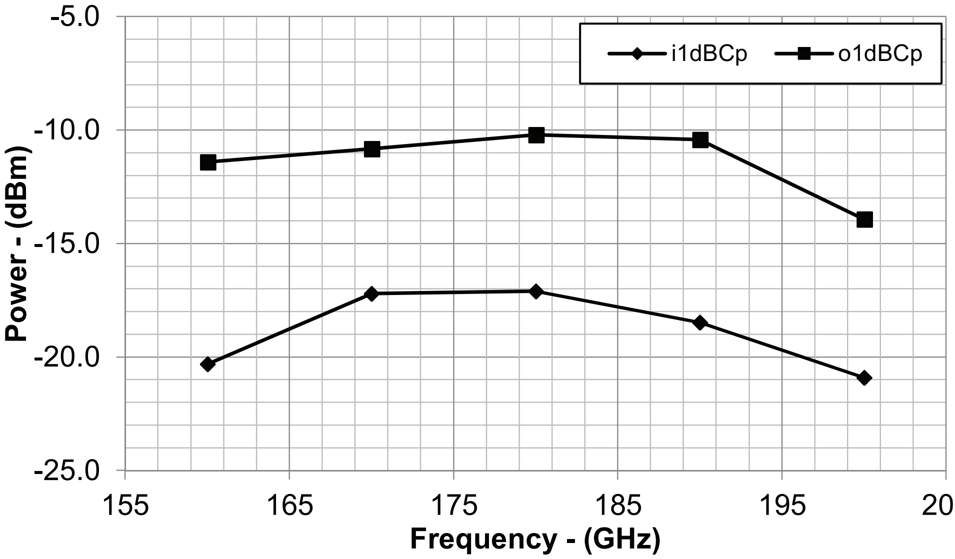


Figure 5.10: Input and output power in 1 dB compression of the gain of the RMA in Fig. 5.2 measured over the frequency.

where $Z_{L,1}$ is the load seen by the first stage, and $Z_{O,1}$ is its output impedance. Fig. 5.8 shows that $\Gamma_{1\text{-}O,L}$ is below −10 dB over the frequency band of interest. Therefore, the power transfer between the cascaded stages is constant and almost unitary over the frequency, explaining then the UWB behavior of the RMA.

Thanks to the balanced structure the RMA is matched over an ultra-wide band with return loss always above 20 dB and 10 dB at input and output, as it is shown in Fig. 5.9 together with the simulations. Good agreement is demonstrated. For the chosen operation point, the reverse isolation is better than 40 dB (not shown), and the circuit is unconditionally stable.

Fig. 5.11 presents the compression curve at 160 GHz: the measured i1dBCp is −20.3 dBm, corresponding to an o1dBCp of −11.1 dBm. The measured frequency

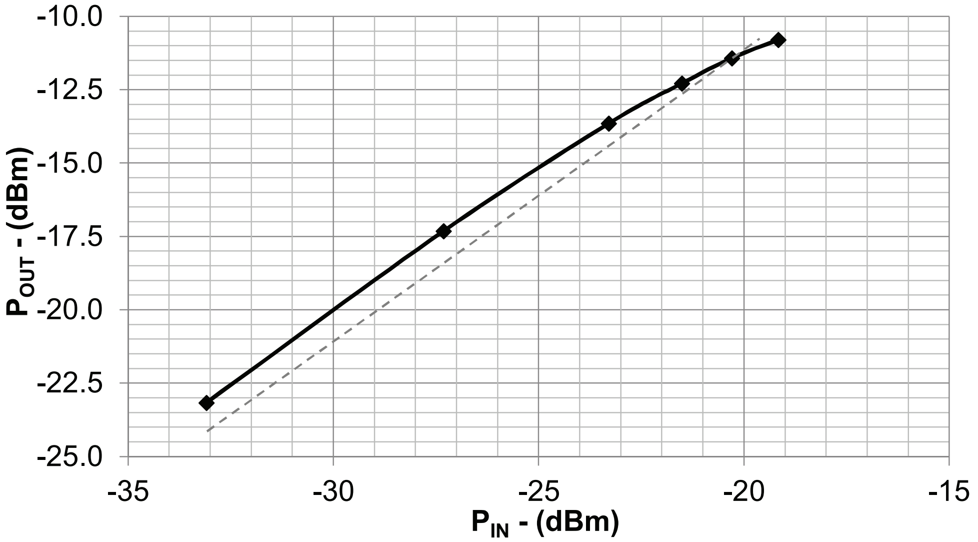


Figure 5.11: Compression gain-curve of the RMA in Fig. 5.2 for a working frequency of 160 GHz.

Table 5.1: State of the art of solid-state amplifiers operating at 200 GHz.

Ref.	**GBP** [GHz]	f_{Center} [GHz]	**BW** [GHz]	V_{CC} [V]	P_{DC} [mW]	**Gain** [dB]	**NF** [dB]	**o1dBCp** [dBm]	**Tech.**
[68]	70	265	10	1.5	52	17	-	-	In DHBT
[69]	67	230	12	-	-	15	-	1	40 nm CMOS
[70]	356	240	40	5	260	19	6	-	GaAs HEMT
[19]	307	190	44	2	18	16.9	9.4	-5	0.13 µm SiGe
[71]	223	230	10	4	68	27	12.5	-	0.13 µm SiGe
[67]	160	245	40	2	28	12	13.3	-	0.13 µm SiGe
This Work	173	180	55	0.8	16.8	10	10.5	-10	0.13 µm SiGe

behaviors of i1dBCp and o1dBCp are shown in Fig. 5.10: variations within 3 dB from 150 GHz to 195 GHz are observed with maximum i1dBCp of -17.1 dBm and o1dBCp of -10.2 dBm at 180 GHz.

5.2.3 Discussion of the Results

The UWB RMA developed in this thesis [Testa3] has been presented. The amplifier is based on a balanced architecture and common-base configuration. Dissipating only 16.8 mW from a 0.8 V supply, the RMA generates 10 dB of gain over the -3 dB-frequency band 155 GHz – 210 GHz, with central frequency of operation f_{Center} at 185 GHz.

A comparison with the state of the art of amplifiers operating at 200 GHz is reported in Table 5.1. The common-base topology enabled a reduction of the supply voltage to the lowest demonstrated for millimeter-wave designs, as well as the lowest required P_{DC}. One of the widest -3 dB-band ever reported in any process operating at 200 GHz has also been demonstrated thanks to multi-stub

Table 5.2: Comparison between DAs and RMAs developed in this thesis.

Ref.	**GBP** [GHz]	**BW** [GHz]	f_{Center} [GHz]	$\mathbf{V_{CC}}$ [V]	$\mathbf{P_{DC}}$ [mW]	**Gain** [dB]	**o1dBCp** [dBm]	**Area** [mm^2]	**Tech.**
CSSDA Section 3.6	760	160	170	2.4	74	13	n.a.	0.23	0.13 µm SiGe
TWA Section 3.3	537	170	75	3.6	108	10	7	0.38	0.13 µm SiGe
RMA Chapter 5	173	55	180	0.8	16.8	10	-10	0.8	0.13 µm SiGe

matching approach. In addition, input and output matching over the amplifier frequency-band of operation have been provided with the balanced architecture.

The RMA performance is briefly compared in Table 5.2 against those of the TWA presented in Section 3.3, and of the CSSDA described in Section 3.6, which are representative of the state-of-art for SiGe distributed amplifiers. The RMA requires lower dissipated power but at price of a narrower bandwidth of operation than the distributed amplifiers. These, in fact, use several gain cells to form synthetic lines, which in turn are functional from dc up to 200 GHz and beyond, for the employed fabrication technology. Since the goal of this research was the maximization of the bandwidth of antenna-amplifier co-integrated systems, then the distributed amplifiers have been chosen for the implementation of the receiver demonstrator, as it will be discussed in the next chapter.

6 On-Chip Antenna-Amplifier Receivers

6.1 Introduction

As introduced in Chapter I, the use of millimeter waves has two significant advantages: the availability of wide frequency bands, and the compact dimension of the antennas, which in turn enables their integration and reduces the interconnection losses with the transceivers. Co-integrated antenna-amplifier systems have been demonstrated with a central frequency of operation up to hundreds of GHz [6], while the fundamental limit of the state of the art is the narrow relative frequency-band of operation, whose maximum demonstration is 15% [7]. Causes of the so far reported narrow bands are indeed the RMAs integrated into the transceivers. For this reason, DA techniques have been used in this thesis to enlarge the operating frequency band of co-integrated antenna-amplifier systems.

This chapter presents the obtained results. A co-design method for antenna and amplifier maximized the frequency band of operation, while the characterization of the co-integrated system is discussed.

This know-how enabled the demonstration of a co-integrated system to be used as the first stage of sub-THz receivers. In detail, a three-time-stacked Vivaldi antenna has been integrated with the CSSDA presented in Section 3.6, and capable of operation from 140 GHz to 220 GHz. Design, characterization, and obtained measurement results are discussed in the following sections.

6.2 140–220 GHz Vivaldi Antenna integrated with CSSDA

This section presents the first stage of a sub-THz receiver demonstrated in this thesis [Testa5, Testa11]. The system consists of an on-chip stacked Vivaldi antenna, which was developed by the Chair for Radio Frequency and Photonics Engineering of the Technishe Universität Dresden [72], and integrated with the CSSDA described in Section 3.6. The concept of distribution is therefore present in the two part of the system: the antenna makes use of three Vivaldi radiating elements integrated into different metal levels and operating in adjacent bands to broaden the frequency response, while the amplifier is based on distributed techniques.

Among the amplifiers developed, the CSSDA of Section 3.6 was chosen for the integration since it has the highest frequency of operation, that is 250 GHz. This high-frequency operation was crucial to make the fullest use of the antenna bandwidth. Moreover, the compact footprint of the CSSDA was also beneficial to the reduce fabrication cost of the co-integrated antenna-amplifier system.

6.2.1 Analysis and Design of the Co-Integrated Antenna-Amplifier System

The schematic of the antenna-amplifier receiver system is illustrated in Fig. 6.1, while its chip micro-photograph is shown in Fig. 6.2. The system includes a cascade of a three-time stacked Vivaldi antenna, a connecting transmission line, and a CSSDA.

The transmission line prevents the metal structures of the amplifier from disturbing the radiation characteristic of the antenna, spacing the two apart. EM simulations have been used to find the minimum separation where the impact of the amplifier metal-structures on the radiation pattern of the antenna is negligible. The design goal has been to minimize the chip size and the losses associated with the transmission line. For UWB operation the frequency variations of the antenna and amplifier gains have to be taken into account to obtain a flat receiver-gain. The solution adopted describes antenna, amplifier, and interposed line, in terms of two-port scattering matrices [Testa10, Testa11]. These matrices, once transformed in transfer matrices, are multiplied to calculate the system response. Fig. 6.3 illustrates the physical positions of the ports of the matrices. The S-Parameters matrix of the antenna $[S_{Ant}]$ has as input port the physical port of a second antenna, labeled test antenna, located in the far field with respect to the on-chip antenna. Matching is assumed at this port ($S_{Ant,11} = 0$) to simplify the analysis. $S_{Ant,12}$ and $S_{Ant,21}$, which are equal for reciprocity, are the root square of the ratio between the power entering in one antenna and leaving the other when both antennas are matched. $S_{Ant,12}$ and $S_{Ant,21}$ are then normalized with respect to test-antenna gain and Free Space Path Losses (FSPL) to model the on-chip antenna as a stand-alone component independent of the radio-link budget. The normalized $S_{Ant,12}$ and $S_{Ant,21}$ are thus the square root of the gain of the on-chip antenna (G_{Ant}). $S_{Ant,22}$ is the S-Parameter of the on-chip antenna

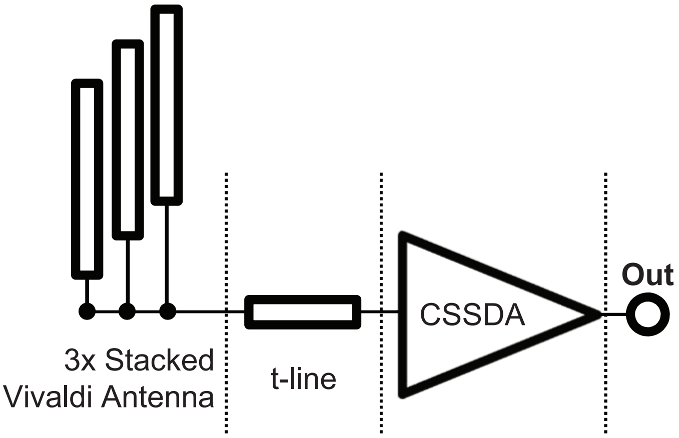


Figure 6.1: Schematic diagram of the demonstrated antenna-amplifier system composed of a three-time stacked Vivaldi-antenna connected to a CSSDA via transmission line.

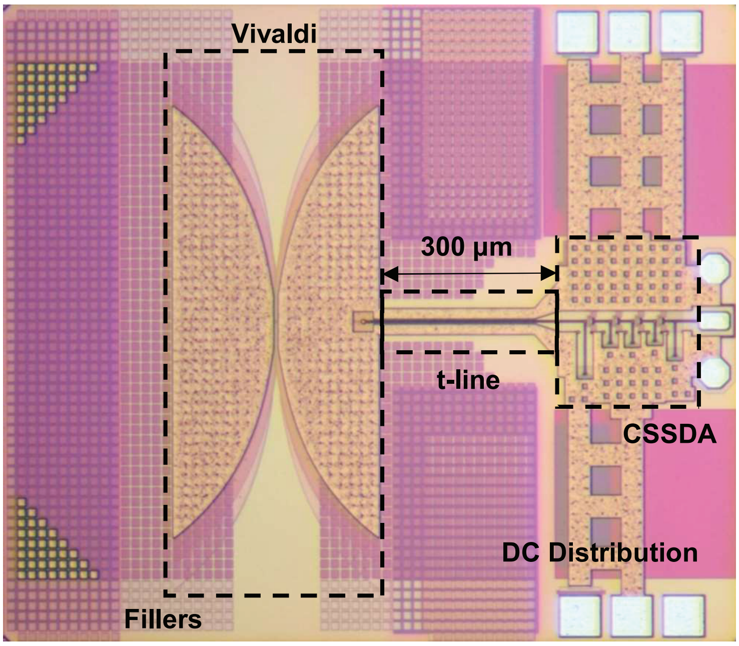


Figure 6.2: Chip micro-photograph of the demonstrated antenna-amplifier system [Testa5, Testa11]. The output is on the right, while the bias-signal pads are on top and bottom of the die.

impedance (Γ_{Ant}). $[S_{Ant}]$ is then expressed as:

$$[S_{Ant}] = \begin{pmatrix} 0 & \sqrt{G_{Ant}} \\ \sqrt{G_{Ant}} & \Gamma_{Ant} \end{pmatrix} \tag{6.1}$$

A coplanar transmission line with 50 Ω characteristic impedance, propagation constant γ, and length l_{Line} has been chosen to interface the antenna with the amplifier. The S-matrix of the transmission line, assuming its characteristic impedance equals to the 50 Ω reference impedance is:

$$[S_{Line}] = \begin{pmatrix} 0 & e^{-\gamma l_{Line}} \\ e^{-\gamma l_{Line}} & 0 \end{pmatrix} \tag{6.2}$$

with γ equals to 180 + j7600 m^{-1} at 180 GHz for the actual design.

The amplifier S-Parameters matrix is $[S_{Amp}]$. Finally, the system gain $S_{Rec,21}$ is obtained from its S-Parameters matrix calculated from the cascade of the transfer matrices of the three blocks. $S_{Rec,21}$ is presented in eq. (6.3): its close analytic formulation models the complete system. This formula has been used for the optimization toward flat and broadband frequency response.

$$S_{Rec,21} = \sqrt{G_{Ant}} S_{Amp_{21}} e^{-\gamma l_{Line}} \frac{1 + \frac{S_{Amp_{22}}}{S_{Amp_{21}}} - \frac{S_{Amp_{11}} S_{Amp_{22}}}{S^2_{Amp_{21}}}}{1 - \Gamma_{Ant} S_{Amp_{11}} e^{-2\gamma l_{Line}}} \tag{6.3}$$

Besides the impact on the receiver response of antenna and amplifier gains,

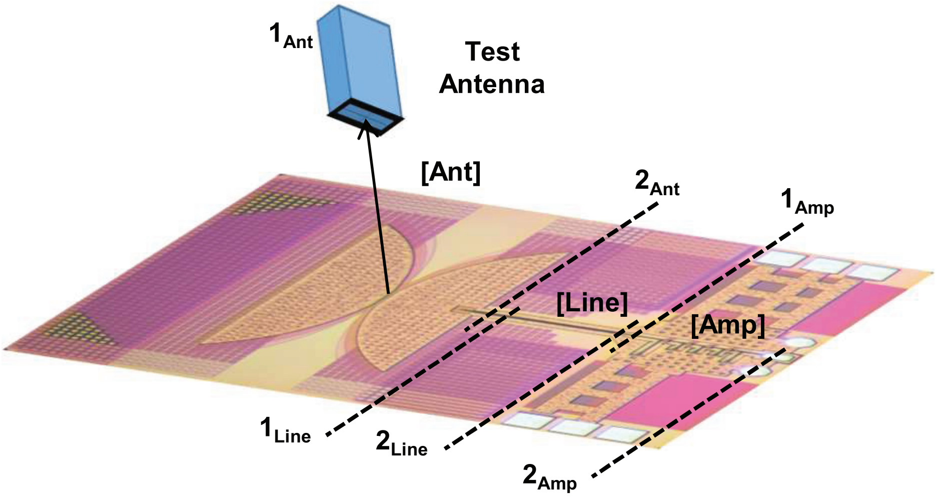


Figure 6.3: 3D representation of the S-Parameters–matrices ports used to describe the blocks forming the system in Fig. 6.1.

also the interface between them has a non-negligible effect on $S_{Rec,21}$. The term $1 - \Gamma_{Ant_R} S_{Amp_{11}} e^{-2\gamma l_{Line}}$ in eq. (6.3), which analytically quantify the relation, can be used to optimize the receiver for a narrow band response with peaked gain, or toward a wideband behavior which is of interest in this thesis.

The peaked response is obtained at the frequency where $\Gamma_{Ant} S_{Amp_{11}} e^{-2\gamma l_{Line}} = 1$, which corresponds to:

$$|\Gamma_{Ant}||S_{Amp_{11}}||e^{-2\gamma l_{Line}}| = 1 \tag{6.4}$$

and

$$\angle\Gamma_{Ant} + \angle S_{Amp_{11}} - 2\gamma l_{Line} = 2\pi k \tag{6.5}$$

with k integer number. This mathematical relation describes the fact that the signal traveling in the transmission line between antenna and amplifier is reflected at the two discontinuities, and the generated reflected waves sum up in phase producing a constructive interference, as in a Fabry-Perót interferometer. The peaking of $S_{Rec,21}$ is shown in Fig. 6.4 for values of $|\Gamma_{Ant_R}||S_{Amp_{11}}||e^{-2\gamma l_{Line}}|$ approaching the unity when the condition of eq. (6.5) is satisfied at 180 GHz. For clarity $S_{Rec,21}$ is normalized to antenna and amplifier gains in the presented simulation.

Although the peaking of the receiver response is interesting from a theoretical point of view, this thesis sought to obtain a broadband behavior for the receiver. The most direct way to achieve this is to have power matching between amplifier and antenna and to design their gains constant in the frequency band of interest, or with opposite frequency roll-offs. In case of matching the receiver gain reduces to:

$$S_{Rec,21-Matched} = \sqrt{G_{Ant}} S_{Amp_{21}} e^{-\gamma l_{Line}} \left(1 + \frac{S_{Amp_{22}}}{S_{Amp_{21}}}\right) \tag{6.6}$$

The CSSDA selected for integration (Section 3.6) has a −3 dB-frequency-band extending from 90 GHz to 250 GHz when the process f_{max} is close to the 450 GHz nominal value. On the other hand, in the case of lower f_{max} due to process variations, the −3 dB upper-corner frequency, and the gain roll-off, is reduced to lower frequencies. Finally, these two quantities can be further tuned through the bias operating point. Conversely, the gain of the Vivaldi antenna increases with frequency in the frequency band of interest [72]. Fig. 6.5 shows the simulated gains of these components for the process corner of the actual wafer run of the fabricated prototype, and the chosen bias operating point. Since the increment toward frequency of the antenna gain is steeper than the gain roll-off of the amplifier gain, the resulting receiver response in case of matching (eq. (6.6)) is narrow band, centered at 190 GHz, and with a −3 dB-bandwidth from 170 GHz to 200 GHz.

In addition to these issues, also the hypothesis of antenna and amplifier impedance constant to 50 Ω over the full operation frequency-band is not verified by the actual design. As discussed in Section 3.4, CSSDAs suffer from a worsening of matching for frequencies approaching the highest end of the spectrum of amplification, while the multi-stacked design of the Vivaldi antenna produces an impedance which is not constant in frequency [72], as it is illustrated in Fig. 6.6.

The receiver has been then modeled with eq. (6.3) taking into account both the mismatch between transmission line, amplifier, and antenna plus the variations of the gains of these components. In particular, starting from their simulated stand-alone performance, the line length has been adjusted to ensure uniform frequency-response through the tuning of the denominator in eq. (6.3). Fig. 6.7 shows that with a line length ranging from 100 µm to 500 µm it is possible to create a second peak in the receiver response, while Fig. 6.8 presents the equalization of the receiver gain effect with different line lengths. With a chosen line length of 300 µm, the −3 dB frequency band of the receiver broads from 155 GHz to 220 GHz, which is more than the double of the case of power matching in Fig. 6.5. This line length is also sufficient to physically separate the antenna from the amplifier metal-layers to avoid perturbations of the receiver radiation pattern. The electromagnetic compatibility between antenna and amplifier, as well as the design of the antenna, are outside the frame of this thesis, and they will not be discussed.

6.2.2 Measurement Technique and Results

The characterization of the system gain has been performed with the measurement setup sketched in Fig. 6.9, whose photograph is also shown in Fig. 6.10. The test signal generated at low frequency with a VNA operating up to 67 GHz, is upconverted with extender modules in the band 140 GHz – 220 GHz. A horn antenna with an average gain of 20 dBi in the frequency range of interest is used

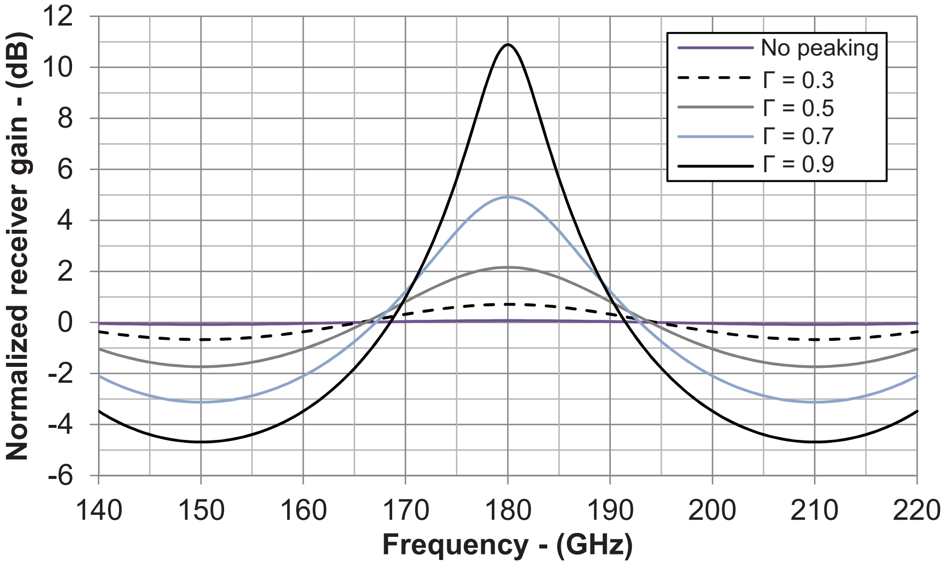


Figure 6.4: Peaking of the receiver gain, normalized to antenna and amplifier gain, when the conditions of eq. (6.5) are satisfied at 180 GHz, while $\Gamma = |\Gamma_{Ant} S_{Amp_{11}} e^{-2\gamma l_{Line}}|$ approaches 1.

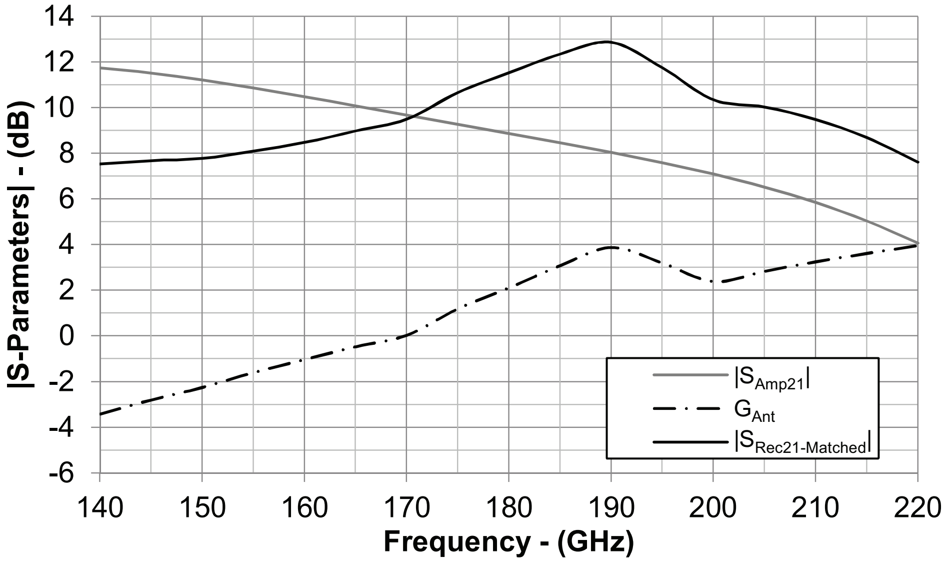


Figure 6.5: Simulated $|S_{Amp_{21}}|$, $|G_{Ant}|$, and receiver gain of the system in Fig. 6.2 in case of matching between antenna and amplifier.

as test antenna to radiate the signal generated by the VNA. A robotized arm ensures fine alignment between test and on-chip Vivaldi antenna. The separation between the two components is above 5 cm to ensure operation in far-field conditions. The VNA has been set in frequency-sweeping mode: in this configuration, the instrument uses a measurement bandwidth down to the kilo-Hertz range, thereby drastically lowering the noise floor. Simultaneously, the instrument sweeps the test signal at low frequency and the local-oscillator signal used for the frequency conversion, characterizing the target band at the intermediate frequency. As illustrated in Fig. 6.9 and 6.10, port I of the measurement equipment generates the test signal, while port II acquires the output of the

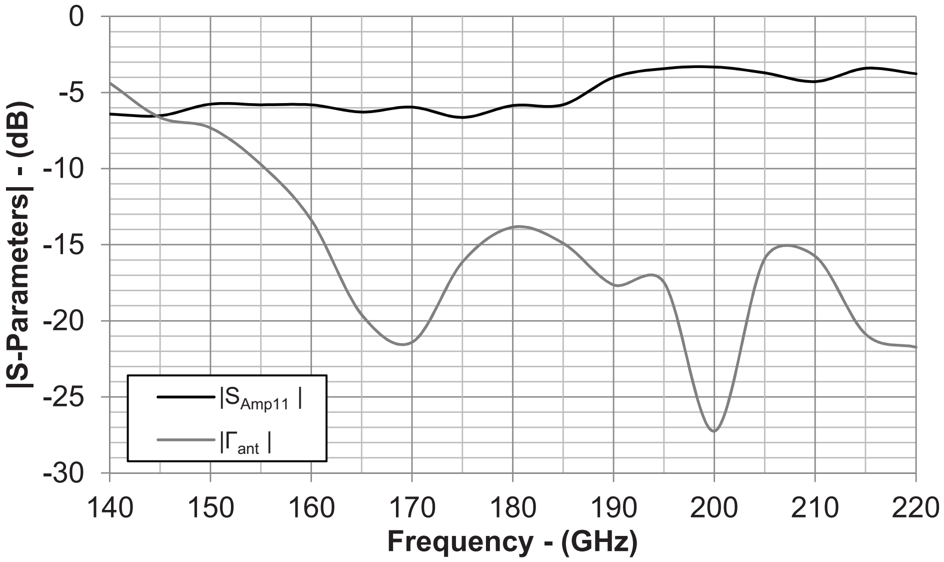


Figure 6.6: Simulated $|S_{Amp_{11}}|$ and $|\Gamma_{Ant}|$ of the system in Fig. 6.2.

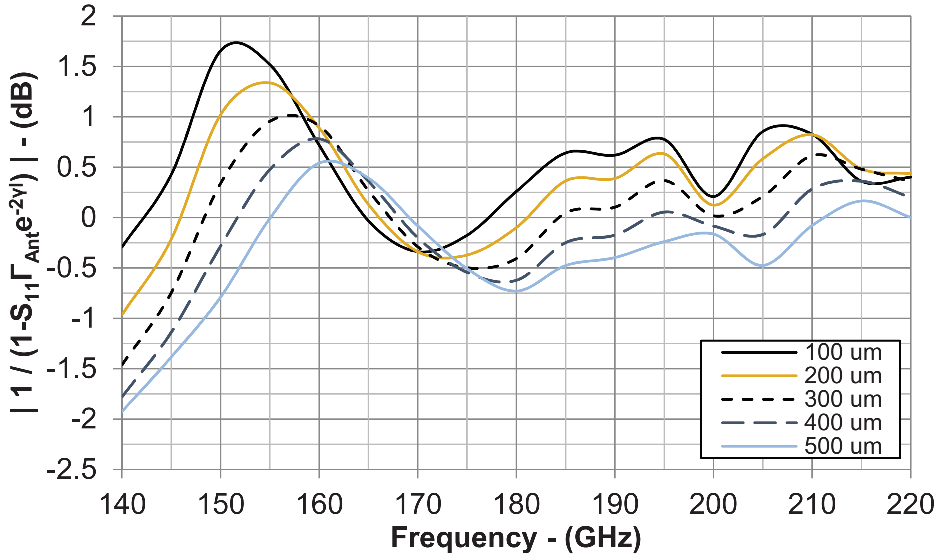


Figure 6.7: Simulated inverse of the receiver-gain denominator (eq. (6.3)) for different values of line length l_{Line}.

co-integrated antenna-amplifier receiver system. The overall gain of the receiver system $|S_{Rec,21}|$ is derived from the measured $|S_{M,21}|$ as:

$$|S_{Rec,21}| = \frac{|S_{M,21}| \times FSPL \times L_{Probe}}{G_{\text{Test-Antenna}}} \tag{6.7}$$

where $G_{\text{Test-Antenna}}$ is the test antenna gain, while FSPL and L_{Probe} are the free-space path losses and the losses of the probe used for contacting the circuit, respectively.

Fig. 6.11 presents the measurement results acquired for distances between the antennas of 5 cm, 10 cm, and 15 cm after de-embedding FSL, $G_{\text{Test-Antenna}}$ and

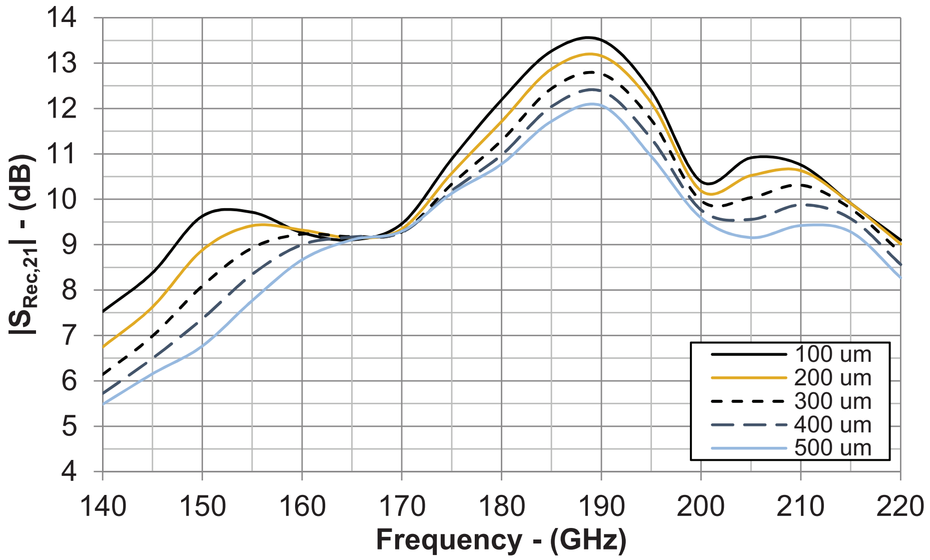


Figure 6.8: Simulated receiver-gain of the system in Fig. 6.2 (eq. (6.3)) for different values of line length l_{Line}.

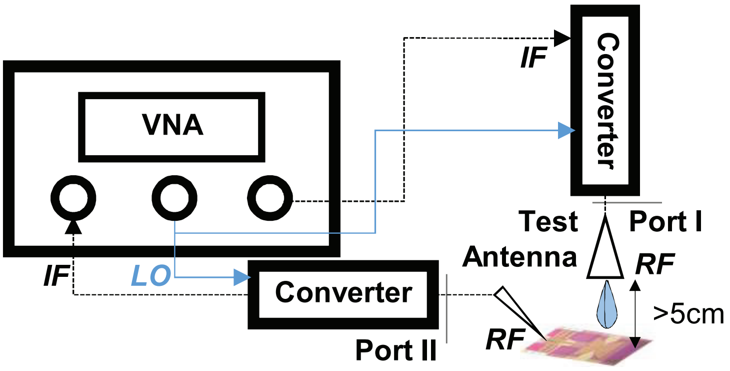

VNA
IF
LO
Converter
Port II
IF
Converter
Test
Antenna
Port I
RF
>5cm
RF

Figure 6.9: Schematic representation of the measurement setup used to characterize the co-integrated antenna-amplifier system of Fig. 6.2.

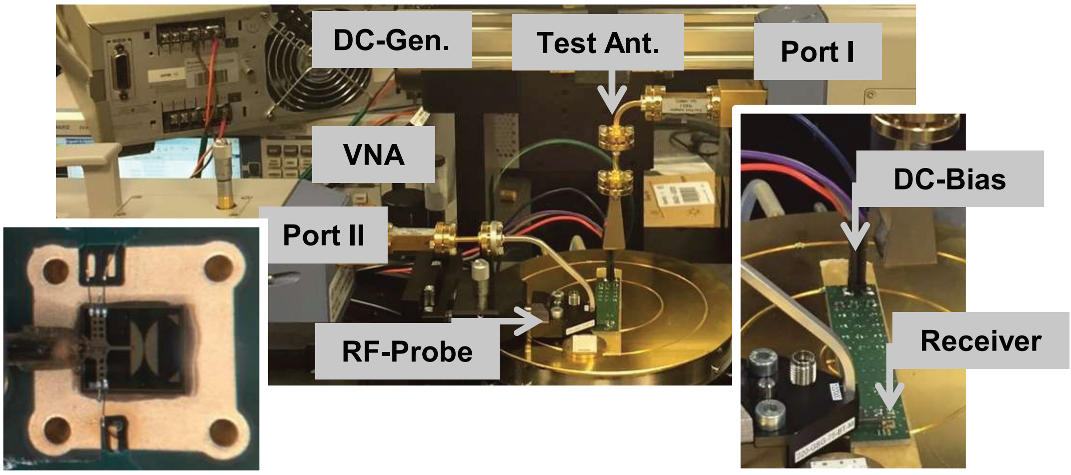

DC-Gen.
Test Ant.
Port I
VNA
Port II
RF-Probe
DC-Bias
Receiver

Figure 6.10: Photograph of the measurement setup sketched in Fig. 6.9. The left inset shows the probe and the bond-wires contacting the circuit in Fig. 6.2, while the right inset illustrates the receiver mounted on PCB.

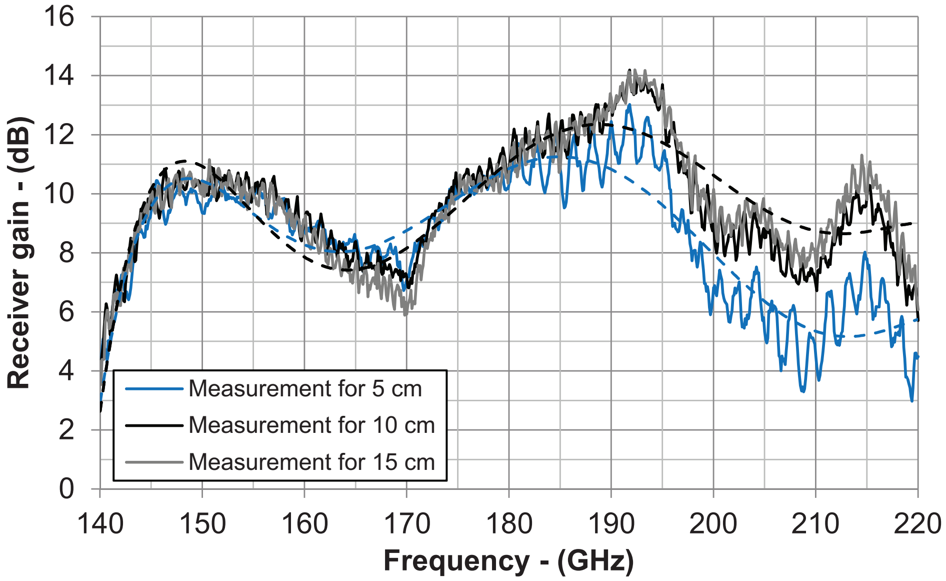


Figure 6.11: Measured (solid) and trend-line (dashed) gain of the receiver in Fig. 6.2 ($|S_{Rec,21}|$), for different distances from the test antenna.

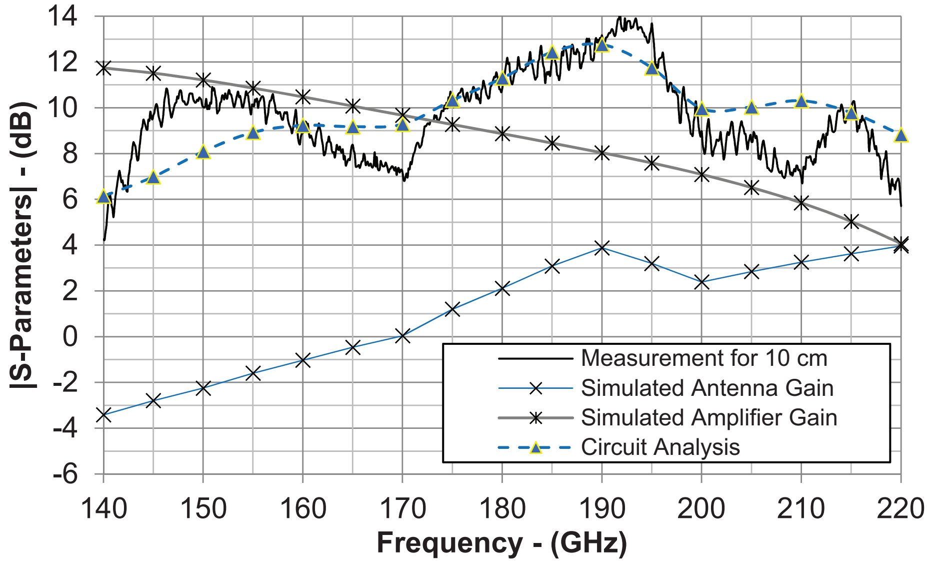


Figure 6.12: Gain of the receiver in Fig. 6.2 predicted as in eq. (6.3), evaluated with simulated data of amplifier and antenna, and comparison against measurement result for a distance of 10 cm.

L_{Probe}. The measurements show same absolute values and frequency trends; it is possible to observe that the ringing of the gain reduces at higher distances thanks to a focusing of the antenna beams, which in turn reduces the multipath effects. A maximum gain of 13 dB is demonstrated over a 6 dB bandwidth of almost 80 GHz, covering the full spectrum of characterization. The measured gain is compared in Fig. 6.12 against eq. (6.3) evaluated with the simulated features of the amplifier, transmission line, and antenna. The amplifier gain is lower than that reported in Section 3.6 since the f_{max} of the actual fabrication run was reduced to 370 GHz. Agreement between measurement result and presented

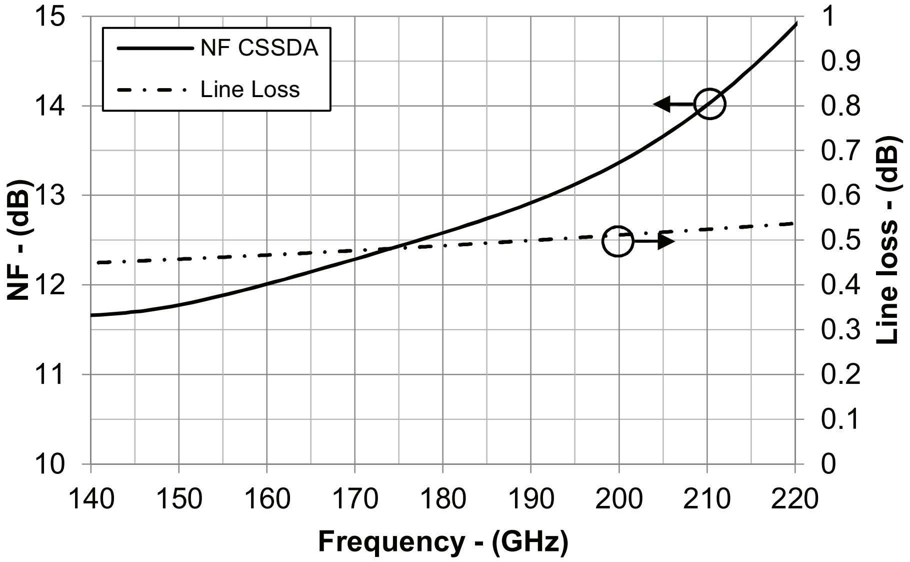


Figure 6.13: Simulated noise figure of the CSSDA, and attenuation of the 300 µm line interposed between this component and the Vivaldi antenna.

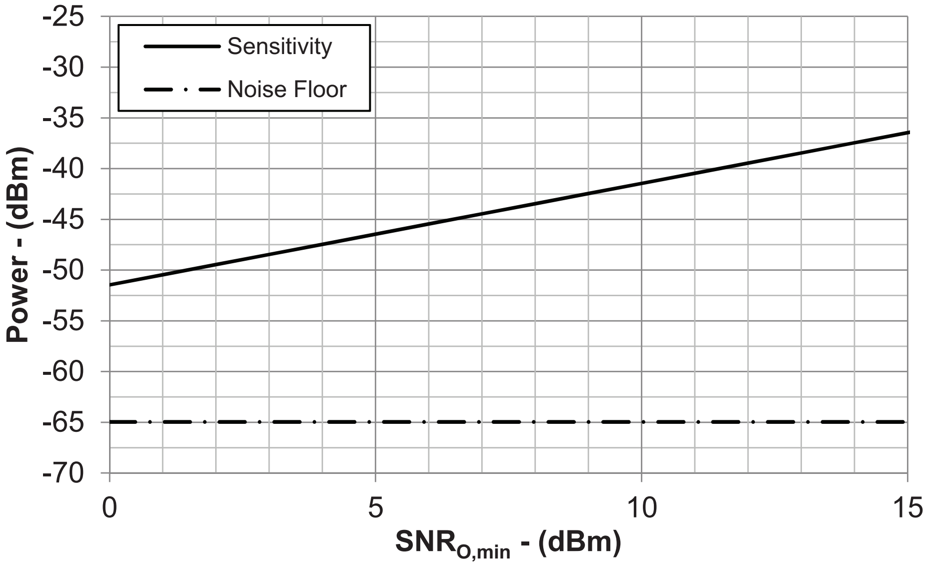


Figure 6.14: Calculated sensitivity of the co-integrated amplifier-antenna system plotted against the minimum acceptable SNR at the receiver output. The value of the noise floor is also reported for an antenna temperature of 290 K and bandwidth of the system of 80 GHz.

system-analysis is demonstrated within 3 dB tolerance, where the source of error can be identified in neglecting the effect of bond-wires used for feeding the dc supplies, and in the finite shape of the PCB upper metal layer that is used as antenna back-reflector. Finally, Fig. 6.12 shows how eq. (6.3) has been useful to optimize the receiver toward a broadband frequency response.

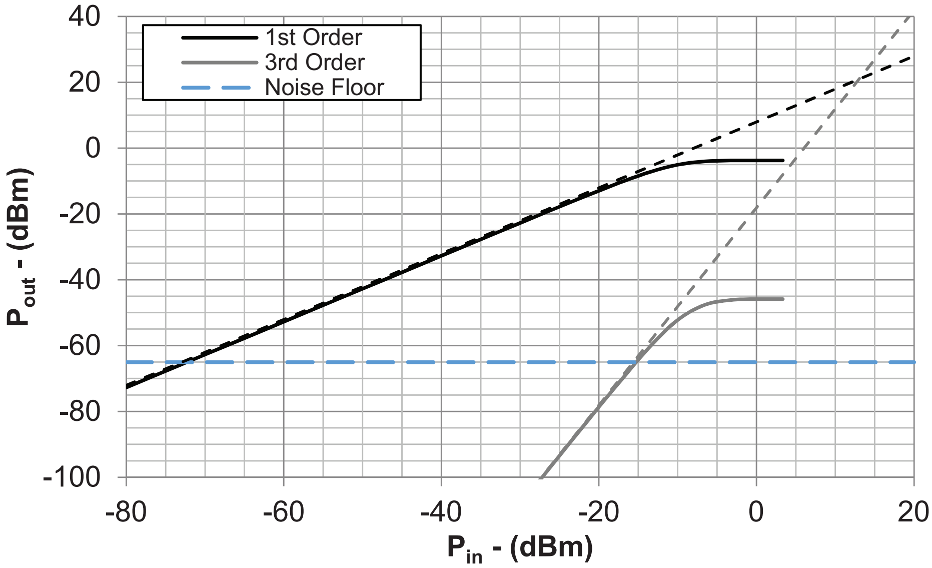


Figure 6.15: Simulated IIP3 of the CSSDA employed in the co-integrated antenna-amplifier system of Fig. 6.1. The intercept point between the noise floor and the third harmonic is the maximum input power of the spurious free dynamic range.

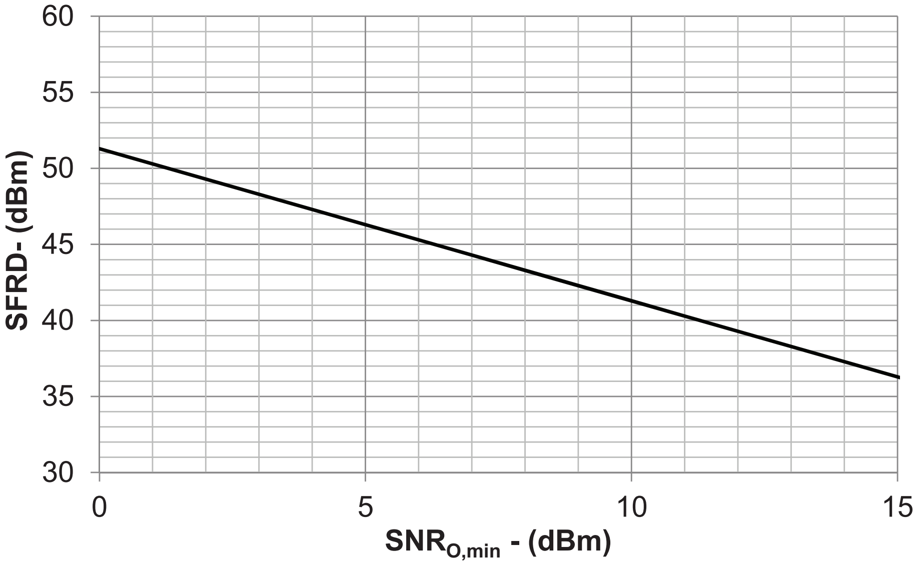


Figure 6.16: SFDR calculated as in eq. (6.11) for the co-integrated antenna-amplifier system in Fig. 6.1.

6.2.3 Considerations for Receiver Applications

Since the hardware developed in this thesis is designed to be the first stage of a UWB receiver for sub-terahertz applications, it is important to characterize other features in addition to the frequency band of operation and gain.

Receivers can collect electromagnetic signals in the form of radio waves and convert the information contained in them into a usable form. The antenna-amplifier system demonstrated in this thesis certainly has an impact on the *Sensitivity* of the receiver, which by definition is the weakest signal that can be received generating the minimum SNR acceptable for the final use [73]. The sensitivity of a receiver is calculated as [73]:

$$S_\mathrm{i} = k \cdot T_a \cdot BW \cdot F_{RX} \cdot SNR_{O,min} \tag{6.8}$$

where $\mathrm{S_i}$ is the power of the minimum detectable signal, k is the Boltzmann constant, $\mathrm{T_a}$ the equivalent noise temperature in Kelvin of the source at the receiver input (which is the antenna in this work), BW the working bandwidth of the receiver which coincides with the bandwidth where the input noise power is calculated, $\mathrm{F_{RX}}$ is the receiver noise-factor, and $\mathrm{SNR_{O,min}}$ is the minimum SNR at the receiver output acceptable for a specific application.

The antenna noise temperature $\mathrm{T_a}$ is the noise temperature at which a resistor should be to generate the same noise that is produced by the antenna in the operating environment.

The noise figure of the presented antenna-amplifier system can be then calculated with the Friis equation for the noise factor, as:

$$F_{RX} = F_{Line} + \frac{F_{CSSDA} - 1}{G_{Line}} + \frac{F_{FollowingStage} - 1}{G_{Line} G_{CSSDA}} \tag{6.9}$$

Under the assumption that the noise factor of the following stage $\mathrm{F_{FollowingStage}}$ is suppressed by the gain of the CSSDA, and considering that the noise figure of the line $\mathrm{F_{Line}}$ is the reciprocal of its gain and hence equal to its attenuation $\mathrm{A_{Line}}$, eq. (6.9) reduces to:

$$F_{RX} = A_{Line} F_{CSSDA} \tag{6.10}$$

The noise figure of the CSSDA is plotted in Fig. 6.13 together with the line attenuation for the frequency region of interest. Their average values are 13 dB and 0.5 dB for the CSSDA noise figure and the line attenuation, respectively. For the presented design, the remaining values in eq. (6.8) are 80 GHz for BW, while $\mathrm{T_a}$ is assumed to be 290 K. Fig. 6.14 shows the calculated sensitivity for these values plotted against the minimum acceptable SNR at the receiver output. Finally, the Minimum Detectable Signal (MDS), defined as the one which corresponds a $\mathrm{SNR_{O,min}}$ of 0 dB, is −52 dB.

Another essential feature of receivers is the *Dynamic Range*, which is the ratio between the maximum and minimum input power that the receiver can handle. As discussed above, the minimum input power manageable by the receiver is the sensitivity, while the maximum input power $\mathrm{P_{IN,max}}$ can be defined in several forms. In this work, $\mathrm{P_{IN,max}}$ is defined as the one that generates a third order harmonic at the output with power equal to the noise floor. With this definition, the dynamic range is called Spurious Free Dynamic Range (SFDR) [74]. Another possible metric for $\mathrm{P_{IN,max}}$ is the 1 dB compression point. Nevertheless, it is not considered in this work since it is less stringent than the SFDR. The analytical expression of the SFDR is [74]:

$$SFDR = \frac{2\,(IIP3 - P_{nf})}{3} - SNR_{O,min} \tag{6.11}$$

where IIP3 is the Input-Referred Intercept Point of Third-Order of the CSSDA, whose simulation is shown in Fig. 6.15; whereas $\mathrm{P_{nf}}$ is the noise-floor power (Fig. 6.14). The SFDR of the co-integrated antenna-amplifier receiver system is finally shown in Fig. 6.16. The maximum SFRD is 51 dB, which corresponds an $\mathrm{SNR_{O,min}}$ of 0 dB.

6.2.4 Discussion of the Results

A Vivaldi antenna has been integrated on-chip with a CSSDA to realize the first stage of a UWB receiver for sub-THz applications [Testa5, Testa11]. The circuit has been fabricated with the *SG13G2* technology described in Chapter 2. A novel design technique maximized the system bandwidth modeling antenna, amplifier and connecting transmission lines with S-Parameters matrices to predict the frequency dependency of the system gain, and the optimum impedance-interface between antenna and amplifier. The presented system demonstrated an average 10 dB of gain over the frequency band 140 GHz – 220 GHz. The design shows the broadest reported frequency band of operation, with an improvement of more than a factor 2 against the state of the art presented in Table 6.1.

Table 6.1: State of the art of antennas integrated with receiver hardware.

Ref.	**Tech.**	**System Type**	$\boldsymbol{f}_{\mathbf{Center}}$***** (GHz)	**BW** (GHz)	**ΔBW**** (GHz)	**Ant. Gain** (dBi)	**Antenna**	$\mathbf{P}_{\mathbf{DC}}$ (mW)	**Gain***** (dB)	**Area** (mm^2)
[6]	40 nm CMOS	Mixer+Osc.	340	0.5	0.14%	-5.5	Patch	53	-10	0.26
[8]	100 nm GaAs	LNA+Mixer	220	10	4%	0	Slot Square	110	3.5	4.80
[3]	130 nm SiGe	LNA+Mixer	240	20	4%	>15	Ring + Lens	1000	21	1.68
[7]	65 nm CMOS	Mixer+Amp.	260	42	16%	-5.6	SIW	18.2	-2	0.45
This work	130 nm SiGe	CSSDA	180	80	44%	-4.5 to 4	Vivaldi	74	10	1.68

*: Center Frequency, **: Relative bandwidth, ***: Of the complete system.

7 UWB Transceivers

This chapter presents the capabilities and bottlenecks of communication systems making use of the hardware developed in this thesis.

The chapter is organized as follows: the first part discusses the impact of the channel bandwidth on the communication data-rate; the second section describes the design approaches for UWB transceivers; finally, the last section shows how the results of this thesis could be embedded in future UWB communication systems.

7.1 Channel Capacity of UWB Systems

Information theory is the framework within study the performance and the limiting factors of the telecommunication. The unit of measure to characterize an exchange of data is the capacity of the channel, which is the highest speed of information transfer for an arbitrary probability of data loss. According to the Shannon-Hartley theorem, the capacity C through an Additive White Gaussian Noise (AWGN) channel, is [75]:

$$C = BW \cdot log_2(1 + SNR) \tag{7.1}$$

where BW is the channel bandwidth and SNR the signal-to-noise ratio. Eq. (7.1) can be used as a benchmark for evaluating the performance of the communication systems in relation with the basic resources available in the channel without going into the details of specific modulation used [75]. The SNR can be expresses as:

$$SNR = P_R/(BW \cdot N_0) \tag{7.2}$$

with $\mathrm{P_R}$ the received power, and $\mathrm{N_0}$ the spectral power-density of the noise. $\mathrm{N_0}$ can be further expressed as $k{\cdot}\mathrm{T_{REC}}$, where k is the Boltzmann constant in joules per kelvin, and $\mathrm{T_{REC}}$ the receiver-system noise-temperature in kelvins. Eq. (7.1) is then formulated as:

$$C = BW \cdot log_2\left[1 + P_R/(BW \cdot\ k \cdot\ T_{REC})\right] \tag{7.3}$$

Eq. (7.3) shows the relation between C and BW, and it is of particular interest within this thesis, which aims the maximization of the achievable data-rate via that of the transceiver bandwidth. Fig. 7.1 shows the evaluation of eq. (7.3) a received power of 0.1 nW, and a receiver noise-temperature of 297 °C, which corresponds to an $\mathrm{N_0}$ of $4.1{\cdot}10^{-21}$ J. From the plot, it can be seen that the capacity increases rapidly for enlarging of the channel bandwidth when this is small. In the frequency region where this applies, C is therefore in a bandwidth-limited regime. On the contrary, the channel capacity approaches an asymptotic value as the bandwidth tends toward infinity. The limit of C as BW approaches infinity is:

$$C = P_R/N_0 \cdot log_2(e) \tag{7.4}$$

that is achieved in practice for $\mathrm{BW} \gg \mathrm{P_R/N_0}$. In this circumstance, the capacity increases linearly with the SNR at the receiver, while it shows slow dependency with the channel bandwidth. For this reason, the capacity is indicated in this case as in signal-to-noise power limited-regime, or briefly power-limited regime [75]. A simplified sketch of transceiver system is illustrated in Fig. 7.2 with annotated power levels and gains compatible with the hardware presented so far. The FSL are calculated over a distance d of 1 cm, and for a frequency of operation of 200 GHz, as in case of short-distance high-speed data links. Considering an input power of −30 dBm, amplifier and antenna gains of 10 dB and 5 dB respectively, a received power of −40 dBm is expected. Fig. 7.3 shows the capacity of the system calculated with eq. (7.1): maximum data-rates above 500 Gbps are predicted for channel bandwidth equal or wider than 100 GHz, and receiver noise-temperature up to 1000 °C.

Indeed, in real applications only complicate modulation schemes enable to reach data rates close to the Shannon limit. On the other hand, the proposed simplified analysis highlights the benefits of using ultra-wide frequency bands at mm-wave frequencies. Starting from these considerations, the next section summarizes the usual design approaches for UWB transceivers.

7.2 Design Approaches for UWB Transceivers

Ultra-Wideband communications were first demonstrated by Heinrich Hertz in 1893 with the spark-discharge experiment. Since then, UWB systems have been employed for military purposes such as imaging, radar, and stealth communica-

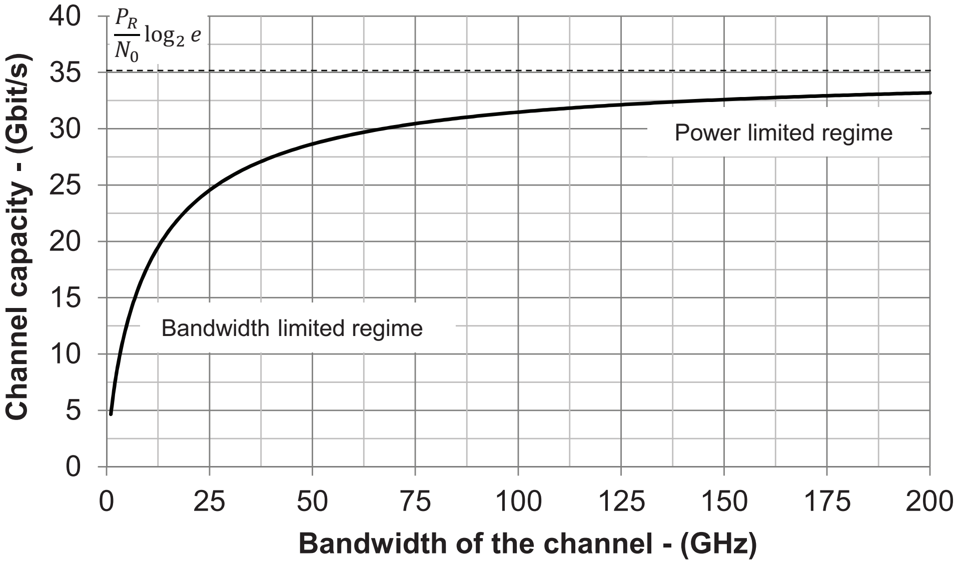


Figure 7.1: Simulated channel-capacity with eq. (7.3).

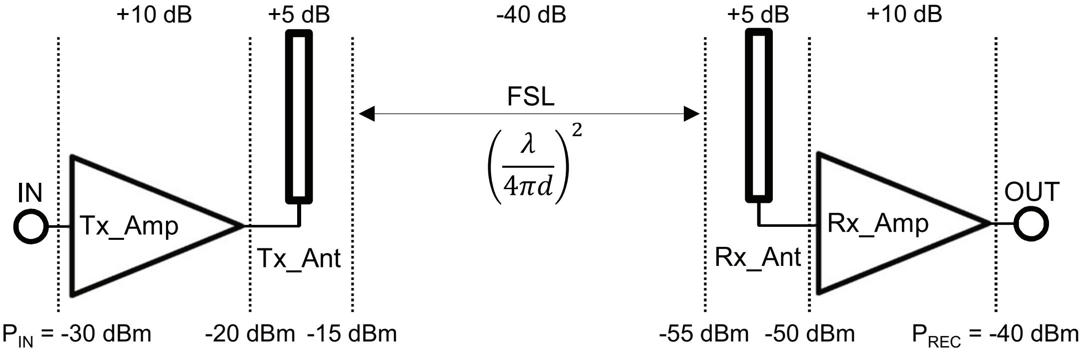


Figure 7.2: Power-link budget for a transceiver operating at 200 GHz and communicating over a distance d of 1 cm. The performance of the hardware forming the transceiver are compatible with those of the components demonstrated in this thesis.

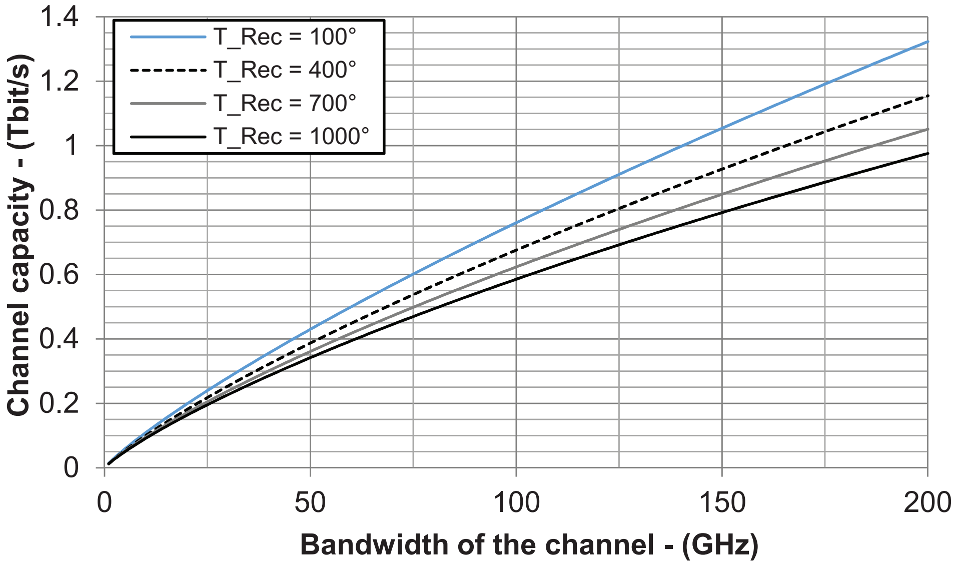


Figure 7.3: Channel-capacity calculated with eq. (7.3) and evaluated for the P_{REC} of the system in Fig. 7.2.

tions. Starting from the last two decades also the consumer market found interest in UWB approaches thanks to their low cost and energy-consumption [77].

In 2002 the first regulation of UWBs for commercial purposes has been introduced by the Federal Communications Commission (FCC) of United States. It has been defined UWB as any communication having a fractional bandwidth greater than the 20% or occupying at least 500 MHz of the spectrum [78]. The FCC has also regulated the maximum allowed Spectral Power Density (SPD) to −41.3 dBm per MHz to minimize interference with existing narrow-band communications, and it has allowed license-free UWB communications in the band from 3.1 GHz to 10.6 GHz [77]. In 2005, Japan and Europe approved similar rules allowing UWB systems operating from 3.1 GHz to 4.8 GHz and from 7 GHz to 10 GHz, and again with limited permitted power [78]. UWB signals with such low SPDs can be considered as noise by narrow-band standards. In fact, the aim

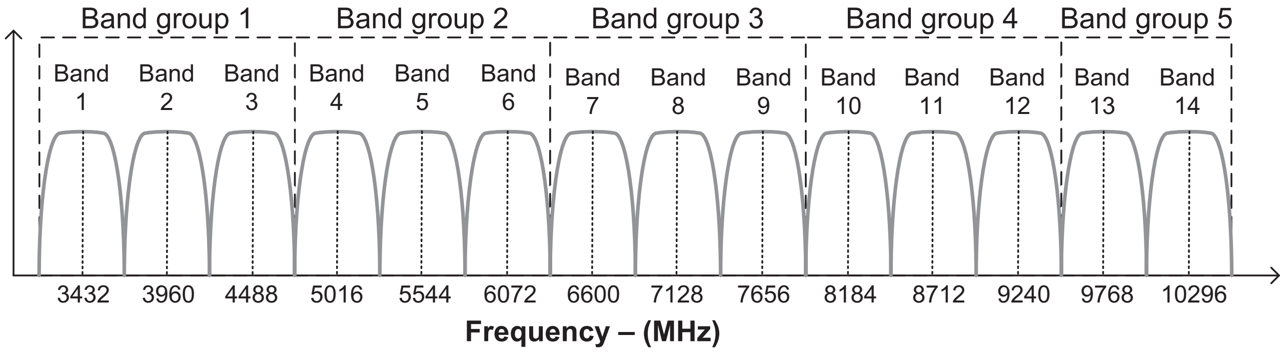


Figure 7.4: MB-OFDM frequency bands and their partitioning [76].

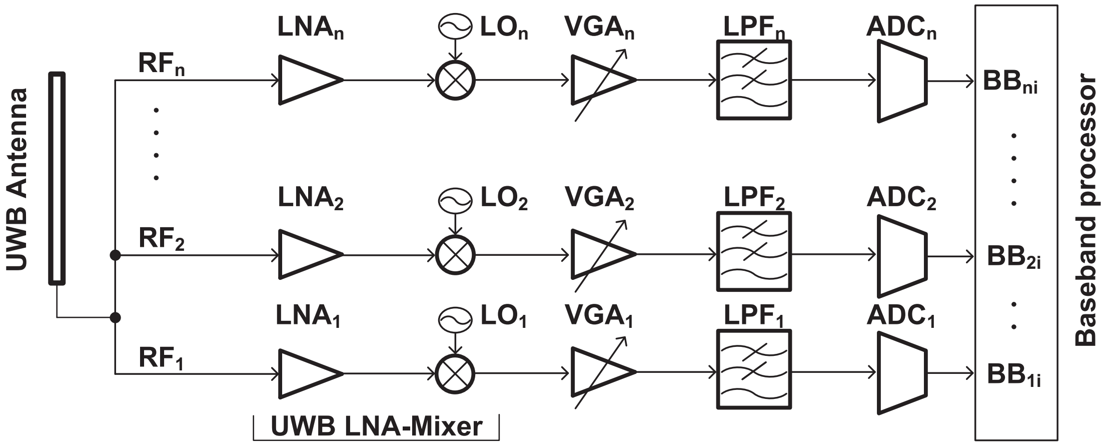

UWB Antenna
RFn
RF2
RF1
LNAn
LNA2
LNA1
LOn
LO2
LO1
VGAn
VGA2
VGA1
LPFn
LPF2
LPF1
ADCn
ADC2
ADC1
BBni
BB2i
BB1i
UWB LNA-Mixer
Baseband processor

Figure 7.5: Simplified example of a receiver for MB-OFDB.

is to make UWB technologies overlap with existing protocols of communications.

Two main approaches have emerged to exploit at best the UWB license-free spectrum. The first is the Multi-Band Orthogonal Frequency-Division Multiplexing (MB-OFDM), while the second is the Impulse Radio UWB (IR-UWB). The next subsections describe the two techniques discussing their advantages and bottlenecks.

7.2.1 Orthogonal Frequency-Division Multiplexing

The MB-OFDM approach consists of coding the information in several interleaved parallel low-rate streams, each of them modulating different sub-carriers forming the ultra-wide frequency band of the channel [76].

The standard currently in use for the MB-OFDM is based on the subdivision of the available bandwidth in sub-bands of 528 MHz, as it is shown in Fig. 7.4. Communications up to 0.48 Gbit/s can be demonstrated with this technique over distances in the order of meters [79].

In [80] a direct-conversion transceiver for band-group 1 (Fig. 7.4) is presented, while in [81] one for the band-groups from one to three. The two designs share a

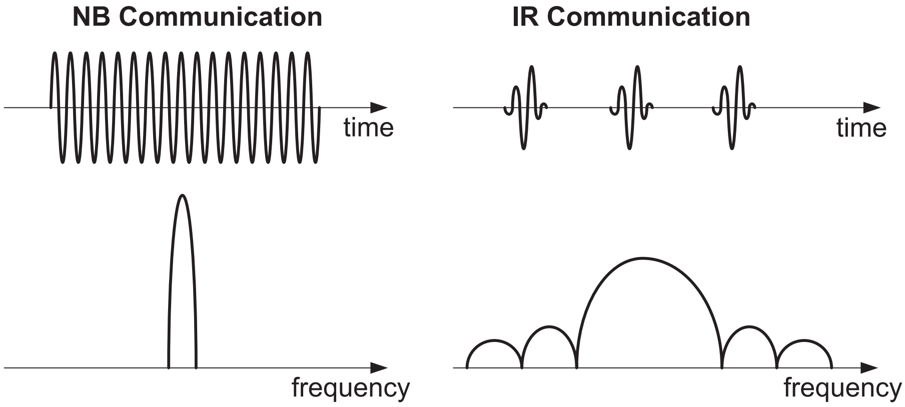


Figure 7.6: Narrow-band continuous-wave signal and impulsed-radio signal in time and frequency domain.

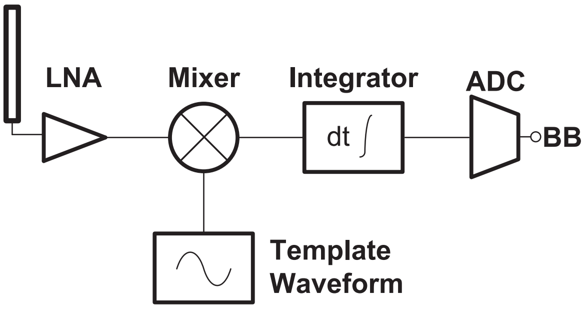


Figure 7.7: Impulsed-radio coherent receiver.

simple architecture, whose the receiver part is illustrated in Fig. 7.5: one of LNA, mixers, Variable Gain Amplifier (VGA), Low-Pass Filter (LPF) and analog-to-digital converter are used to receive each sub-band of the standard. Although LNAs and Mixers can be merged using a frequency hopping of the Local Oscillator (LO) signals, the complexity of the system, as well as its power consumption and silicon footprint, remains high. These drawbacks are further stressed by the requirement of circuitry for the generation of the LO signals. In [80] one Phase-Locked Loop (PLL) per LO signal is used, while in [81] a frequency synthesizer is employed to generate all the required LOs. These issues are resolved by the IR-UWB approach presented in the next section.

7.2.2 Impulse Radio

The second communication protocol used for UWBs is the impulse radio. In this approach, the information is encoded in carrier-free pulses. The technique was first conceived for time-domain electromagnetics in the 1960s when it was discovered that the description of some microwave networks could be easier quantified via its impulse response rather than in frequency domain [80].

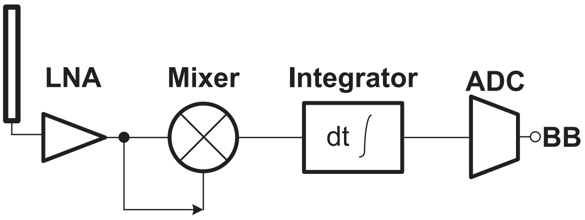


Figure 7.8: Impulsed-radio non-coherent receiver.

During the years, wireless short-pulses signals became quickly popular in military and radar applications, primarily due to their stealth properties, if used for telecommunications, or fine spatial resolution if employed in radars.

On the contrary of traditional radio systems, where the baseband information modulates continuous-wave signals, in IR-UWB the data is encoded in pulses in terms of amplitude, polarity, or other schemes. As it is shown in Fig. 7.6, the IR-signal bandwidth is spread over a broad frequency spectrum, which is the largest for decreasing duration in time of the pulses.

The principal advantage of this type of telecommunications is to enable transceiver implementations with low power and complexity. An example of IR receiver is outlined in Fig. 7.7. It consists of an antenna, LNA, correlation circuitry and ADC. After amplification, the received signal is correlated with an impulse template-waveform same as that of the received signal through a mixer. The output signal of the mixer is integrated to maximize the received signal-level with respect to the power of the noise. A simpler variant of this IR receiver is shown in Fig. 7.8. Now the received pulse is correlated with itself, and the approach is referred to as non-coherent. The main disadvantage of this solution is that the noise and the signal are both amplified at the receiver. Conversely, the advantage is to avoid the generation of a local pulse as well as its synchronization with the received signal.

Nevertheless, both IR coherent and non-coherent systems have the great benefit of extremely simple architectures since frequency synthesizer, PLL, voltage controlled oscillator and mixers are not required.

7.3 Applications to UWB Transceivers of the Thesis Results

The previous section illustrated the design approaches for transceivers operating in the frequency band 3.1 GHz – 10.6 GHz. The hardware presented in this thesis, on the other hand, is capable of operation from the MHz range till and above 200 GHz. This ultra-wide band paves the way for new opportunities regarding the maximum data-rates, as discussed in Section 7.1.

The first part of this section describes the integration of the demonstrated

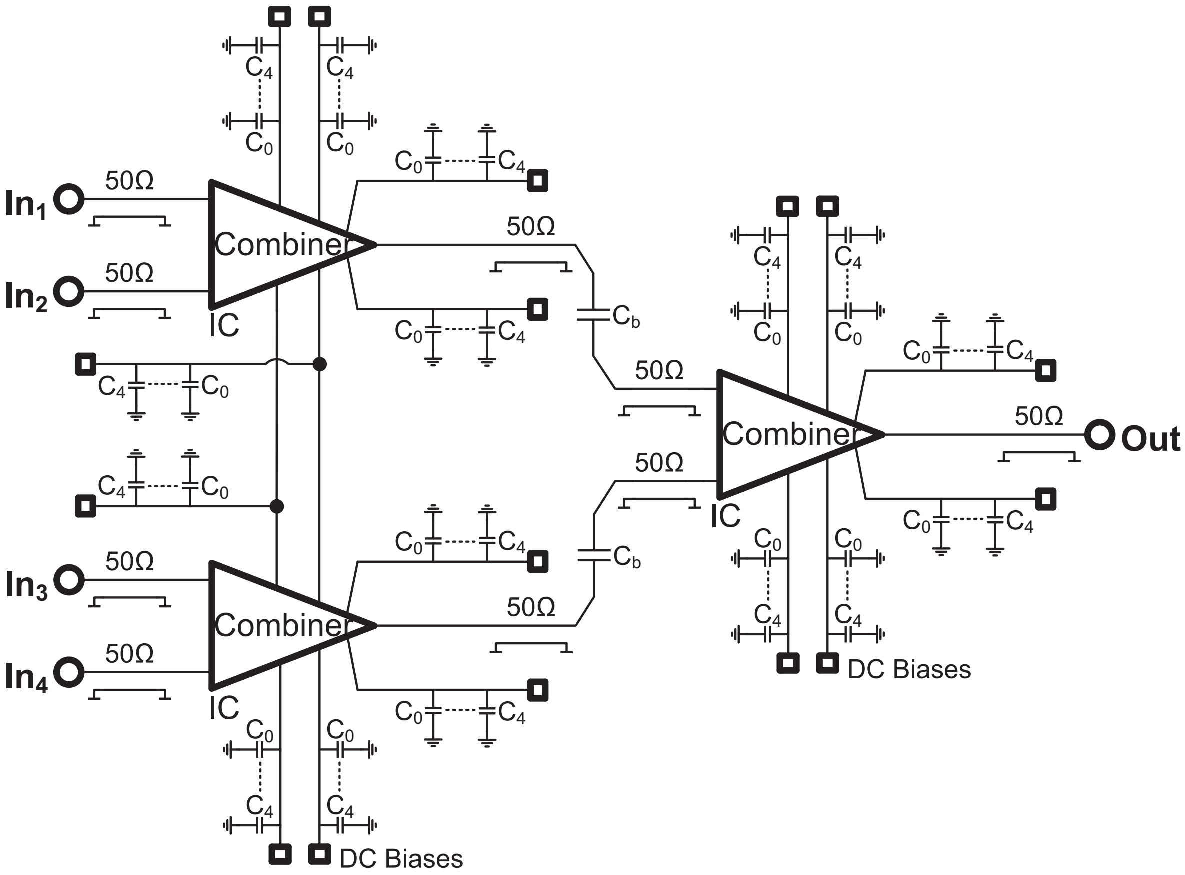


Figure 7.9: Schematic of the 4-to-1 combiner. The schematic of the ICs is shown in Fig. 4.2.

hardware with existing UWB protocols, while the second part discusses the employment of the thesis results for communications with a bandwidth approaching 100 GHz.

7.3.1 Integration with the 3.1–10.6 GHz UWB Protocols

The existing 3.1 GHz – 10.6 GHz UWB protocols set stringent constraints on the SPD, which translates in low powers at the receivers. Received low signal levels, in turn, limit the achievable data-rate at a given distance of the communication.

Beam-forming techniques can solve this limitation [82], increasing the received SNR focusing the transmitted power toward a favored direction, meanwhile not violating the limit on the effective isotropic radiated power.

UWB combiners and dividers are therefore required to route the signals in the multi-antenna architectures. For this reason, within the frame of this research, the combiner and divider discussed in Chapter 4 have been packaged in PCB boards with SMA interface to test their integration in existing UWB systems operating in the 3.1 GHz – 10.6 GHz band [Testa4].

The next paragraphs will present design and characterization of these boards.

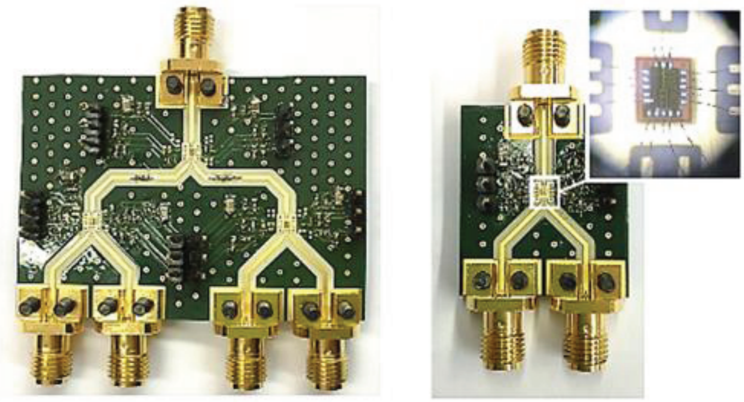


Figure 7.10: Photographs of the fabricated combiner PCBs [Testa4].

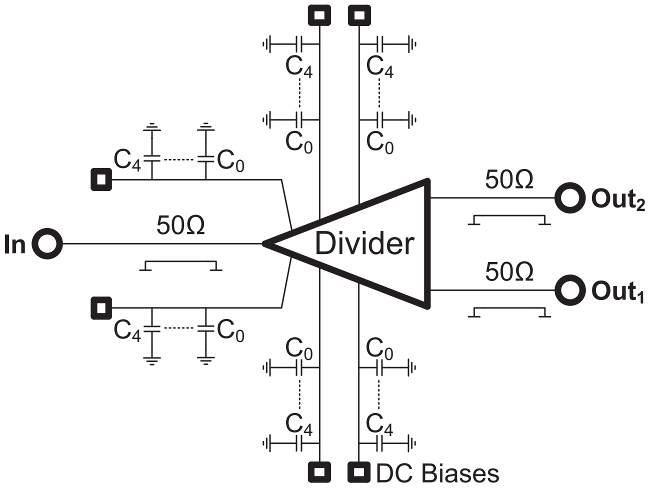


Figure 7.11: Schematic of the presented 2-to-1 divider board. The schematic of the divider IC is shown in Fig. 4.20.

PCBs Design A 2-to-1 and a 4-to-1 combiner PCBs have been developed. Fig. 7.9 shows the schematic of the 4-to-1 combiner, while its PCB photograph is illustrated in Fig. 7.10. The combiner ICs presented in Section 4.2 are mounted on PCB and connected to SMA interfaces with 50 Ω transmission lines. The routing of the bias signals is performed on PCB. Arrays of discrete capacitors $C_{0\text{-}4}$ (Fig. 7.9) have been used to ac-ground the supply distribution-networks. All the capacitors have values from 470 pF to 10 µF, ensuring for the frequency range of interest that at least one of them does not self-resonate, or does not resonate with the inductance of the distribution networks of the supplies.

The divider PCB has been designed complementary to the distributed combiners. Fig. 7.11 shows the circuit schematic, while the photograph of the PCB is presented in Fig. 7.12. The divider is based on the TWD IC presented in Section 4.3. Again, the IC is mounted on the PCB, and 50 Ω transmission lines are used to connect it with SMA connectors.

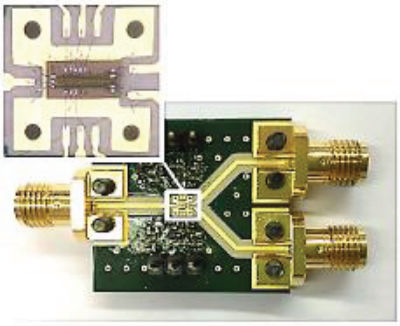


Figure 7.12: Photograph of the fabricated PCB divider [Testa4].

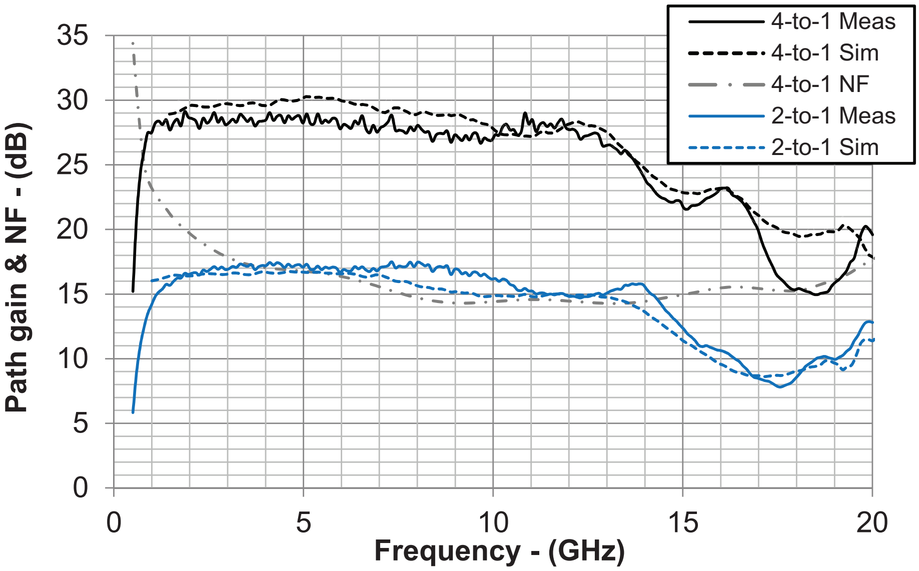


Figure 7.13: Measured and simulated path gains, and NF of the combiners presented in Fig. 7.10.

PCBs Characterization The combiner boards have been characterized with S-Parameters measurement. Fig. 7.13 presents the experimental results and their comparison against simulations. The tests have been performed with a 2-port measurement setup, calibrating a VNA up to the SMA-interface of the boards. The 2-to-1 combiner gain is 17 dB over the −3 dB-band 0.5 GHz – 15 GHz, while it decreases to 10 dB at 20 GHz. The 4-to-1 combiner gain is 30 dB over the −3 dB-band 700 MHz – 14 GHz, while its value at 20 GHz is still 20 dB.

The presented results are primarily limited by SMA connectors, transmission-line, and bond-wires losses. The combiner ICs are in fact functional up to 220 GHz (Chapter 4.2). To highlight the impact on the frequency response of the PCB parasitics, Fig. 7.14 shows the comparison between the gain of the 2-to-1 combiner PCB against the on-wafer measurement of the combiner IC, plus the simulated effect of bond-wires, transmission lines, and connectors. As it can be seen, the SMA connectors are the main limitation toward high frequencies.

Fig. 7.13 shows the noise figure of the 4-to-1 combiner. A minimal value of 14 dB is reached at 10 GHz, while a gradual increase is observed toward low

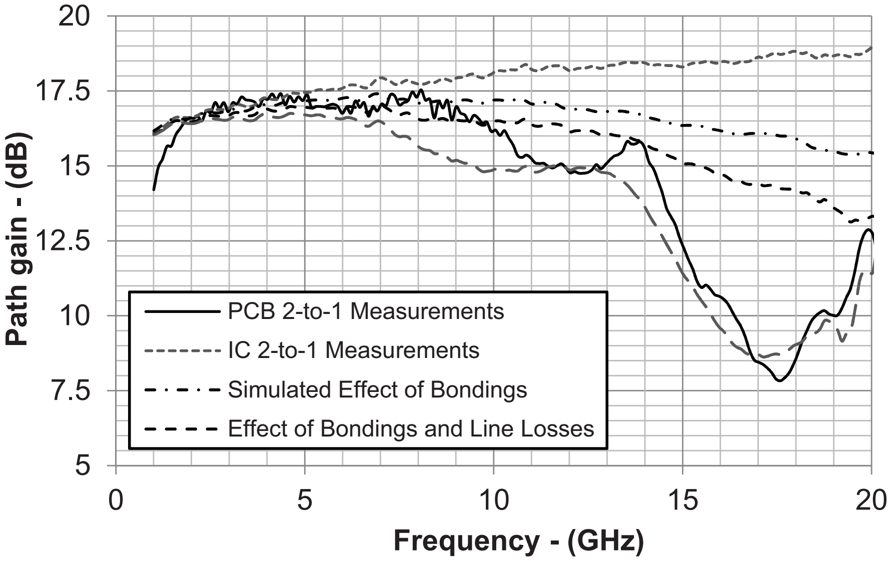


Figure 7.14: Gain comparison of the 2-to-1 combiner PCB in Fig. 7.10 against that of the 2-to-1 combiner IC in Fig. 4.10, and simulations of the impact of SMA connectors, transmission lines, and bond wires.

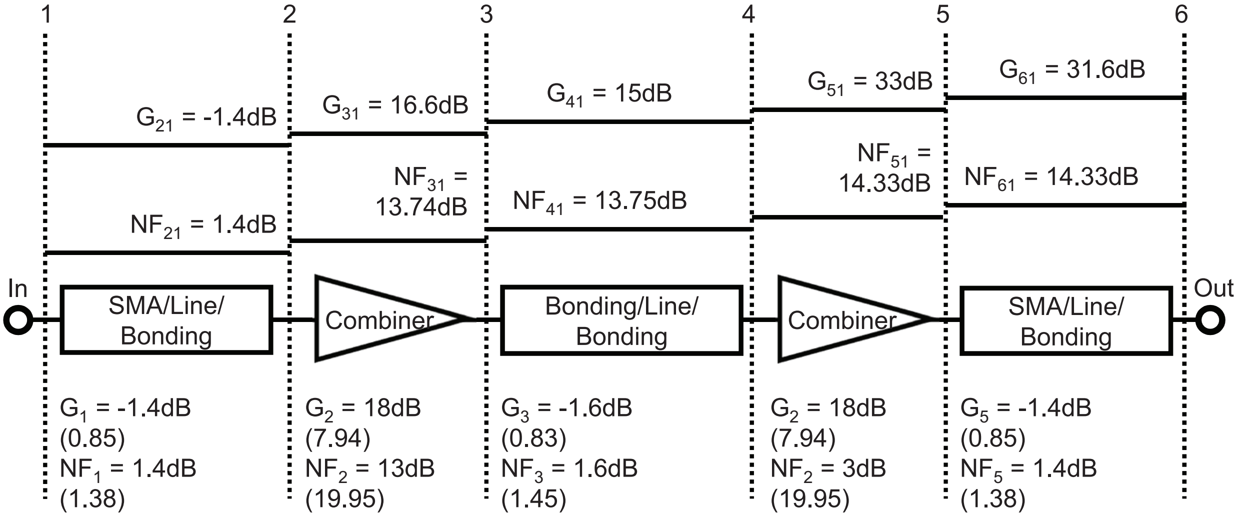

1
2
3
4
5
6
G_{21} = -1.4dB
G_{31} = 16.6dB
G_{41} = 15dB
G_{51} = 33dB
G_{61} = 31.6dB
NF_{21} = 1.4dB
NF_{31} = 13.74dB
NF_{41} = 13.75dB
NF_{51} = 14.33dB
NF_{61} = 14.33dB
In
Out
SMA/Line/ Bonding
Combiner
Bonding/Line/ Bonding
Combiner
SMA/Line/ Bonding
G_1 = -1.4dB (0.85) NF_1 = 1.4dB (1.38)
G_2 = 18dB (7.94) NF_2 = 13dB (19.95)
G_3 = -1.6dB (0.83) NF_3 = 1.6dB (1.45)
G_2 = 18dB (7.94) NF_2 = 3dB (19.95)
G_5 = -1.4dB (0.85) NF_5 = 1.4dB (1.38)

Figure 7.15: Noise figure and gain of the cascaded stages which form the PCB of the 4-to-1 combiner in Fig. 7.10. Numbers in brackets denote values in linear scale. The link-budget is calculated for 10 GHz.

frequency. The calculation of the equivalent noise of the board has also been performed for this frequency, and it is sketched in Fig. 7.15 annotating the gain and the NF at each section of the PCB. For all the sections, the signal-level referred to the input and the NF are calculated. The first stage is the cascade of SMA connector, transmission line, and bond wire. The losses of these components add up to 1.4 dB. The 2-to-1 combiner provides 18 dB gain and has an NF of 13 dB. The other stages behave similarly. The total NF of the 4-to-1 combiner calculated with the noise Friis equation is 14.3 dB, while its gain is 31.6 dB.

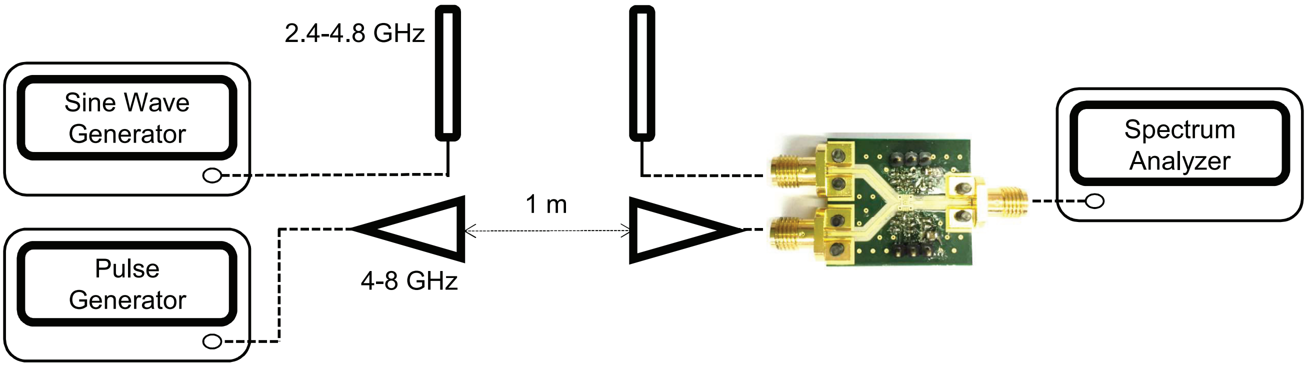


Figure 7.16: Setup for receiving narrow-band and wide-band communications with the 2-to-1 combiner board of Fig. 7.10 simultaneously.

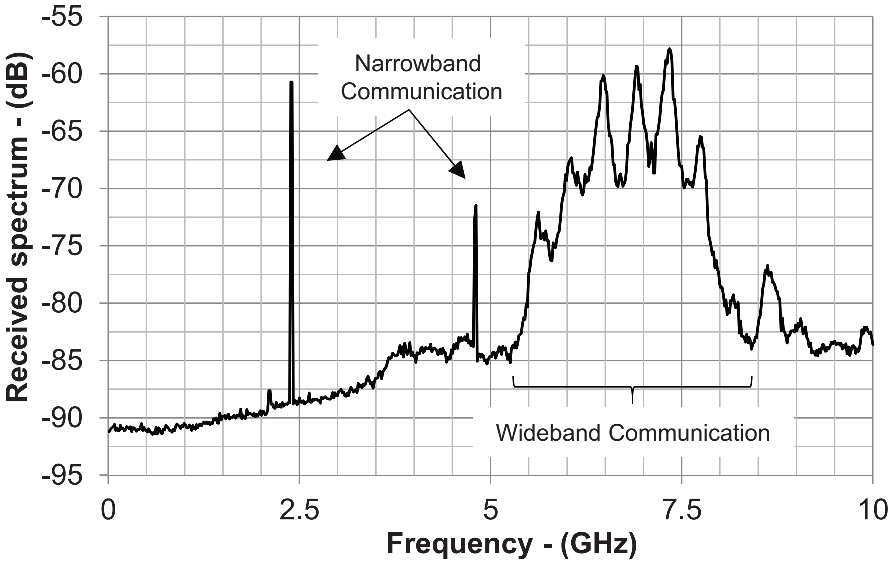


Figure 7.17: Measured received spectrum for the setup in Fig. 7.16.

Integration with 3.1–10.6 GHz UWB Systems The boards have been tested in multi-antenna radio links. Fig. 7.16 shows the setup for testing the reception of simultaneous narrow-band and wide-band communications. A Gaussian pulse with a spectrum from 5.3 GHz to 8 GHz is generated with a commercially available radar and transmitted with a horn antenna operating from 4 GHz to 8 GHz. A dual-band dipole antenna radiates a single-tone signal at 2.4 GHz, and its first harmonic at 4.8 GHz. At a distance of 1 m, two antennas, identical to the ones on the transmitter side, receive the signals which are then combined by the presented PCB. Fig. 7.17 shows the combined output spectrum: the input signals can be identified without relevant distortions and inter-modulation products.

Also the 4-to-1 combiner has been tested in a multi-antenna system. Fig. 7.18 shows the setup used to demonstrate the capability of the board to support narrow-band and UWB standards simultaneously. Two narrow-band dipole antennas resonating at 2.4 GHz, and two wideband horn antennas operating from 4 GHz to 8 GHz have been connected to the combiner inputs. A UWB horn antenna operating from 2 GHz to 18 GHz has been employed on the transmitter

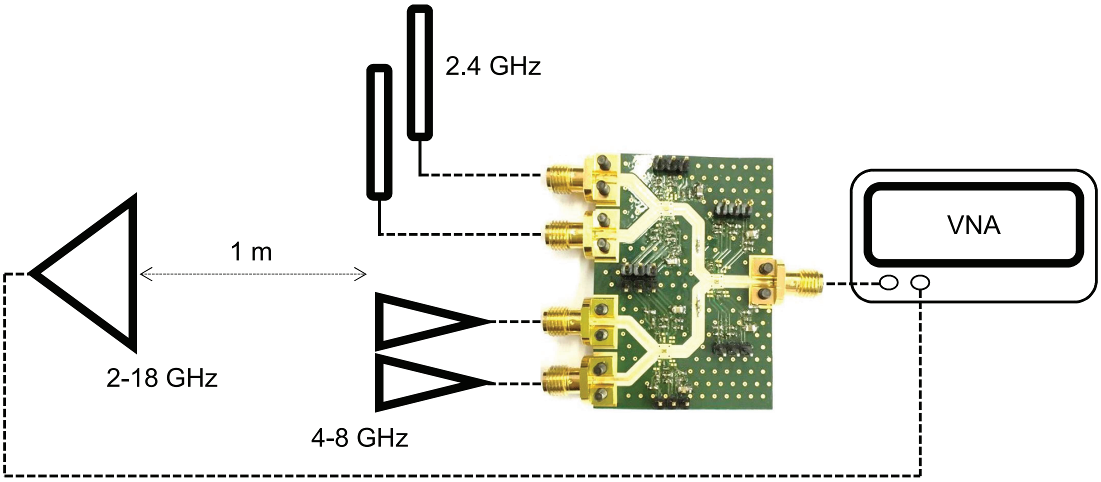


Figure 7.18: Setup for receiving narrow-band and wide-band communications with the 4-to-1 combiner board of Fig. 7.10 simultaneously.

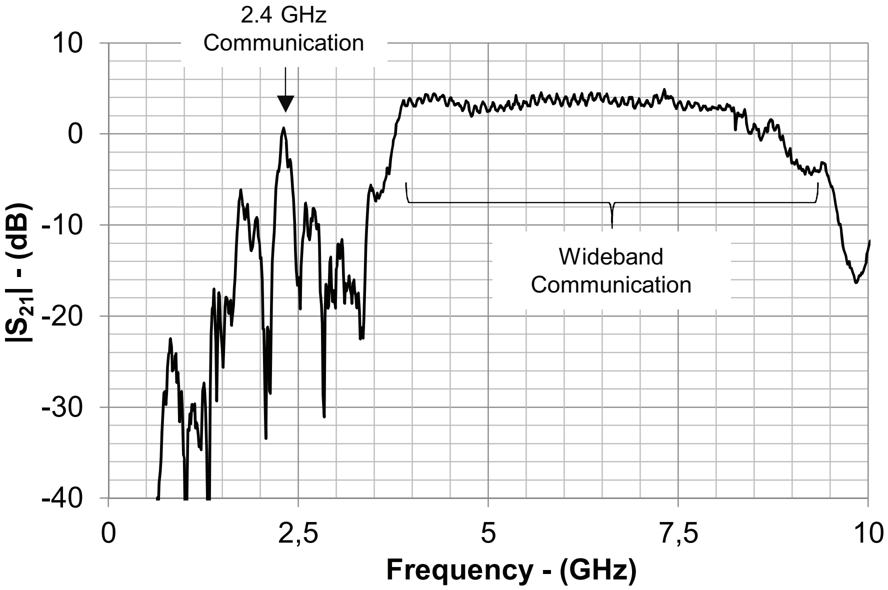


Figure 7.19: Measured $|S_{21}|$ for the setup of Fig. 7.18.

side and placed at 1 m of distance. A VNA is used to evaluate the scattering parameter from the input of the source antenna to the output of the combiner. The frequency behavior of the $|S_{21}|$ is shown in Fig. 7.19: both narrow-band and wide-band antenna arrays are supported simultaneously by the combiner. A quantitative analysis is performed for the wideband array to relate the measured $|S_{21}|$ to the combiner gain G_C (Fig. 7.13), and using the Friis' transmission equation:

$$|S_{21}| = \frac{G_C}{\alpha_C} \cdot G_{T,ant} G_{R,ant} (\frac{c}{4\pi d f})^2 \tag{7.5}$$

where $G_{T,ant}$ is the gain of the transmitting antenna, $G_{R,ant}$ the gain of the receiving array, d the transmitter-receiver distance, f the frequency, c the speed of light, and α_C the attenuation of the cables used to connect the combiner to the antennas at the receiver side. Table 7.1 gathers $|S_{21}|$ and G_C (from measurements),

Table 7.1: Values used for validation of eq. (7.5) with the setup in Fig 7.16.

f (GHz)	$\lvert S_{21} \rvert$ (dB)	G_C (dB)	$G_{T,ant}$ (dB)	$G_{R,ant}$ (dB)	α_c (dB)
6	4	28	11	15	2

$G_{T,ant}$ (from datasheet), and $G_{R,ant}$ simulated from the data-sheet information of the stand-alone antennas used in the array. The values in Table 7.1 are relative to a working frequency of 6 GHz, and if substituted in eq. (7.5) show good agreement between measurements and analysis.

Indeed a large number of tests can be performed combining the presented PCBs to form the signal distribution networks connected to multi-antenna systems. The simplest of such networks is the direct connection between a 2-to-1 power divider and combiner. This test is useful to isolate the behavior of the circuits from the propagation medium and antennas. Fig. 7.20 shows the block representation of the setup. The power-divider outputs are directly connected to the inputs of the combiner PCB. The measurement results are shown in Fig. 7.21. The total path gain is 27 dB. This test is equivalent to the case of ideal medium and antennas with 0 dBi gain. The −3 dB band spans from 0.5 GHz to 10.5 GHz. At 15 GHz the total-path gain is still 17 dB. This result is of particular interest since it covers the full UWB standard, as defined by FCC and other regulations.

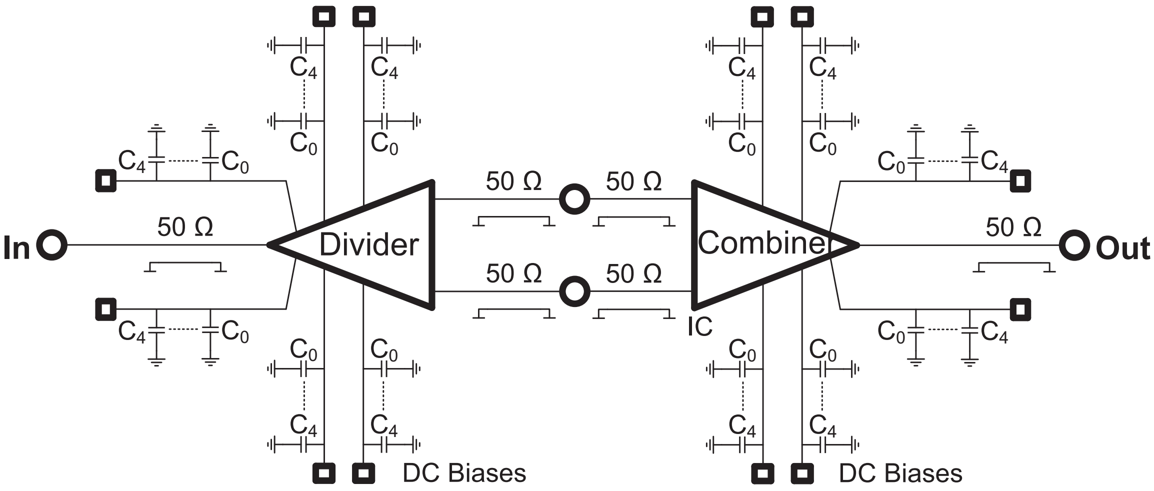


Figure 7.20: Direct connection between the 2-to-1 combiner and divider of Fig. 7.10 and 7.12 to measure the total insertion gain.

7.3.2 Communications using 100-GHz-wide Channels

The majority of the actual systems of telecommunication operate in the radio spectrum located below 30 GHz. As discussed in the previous section, several

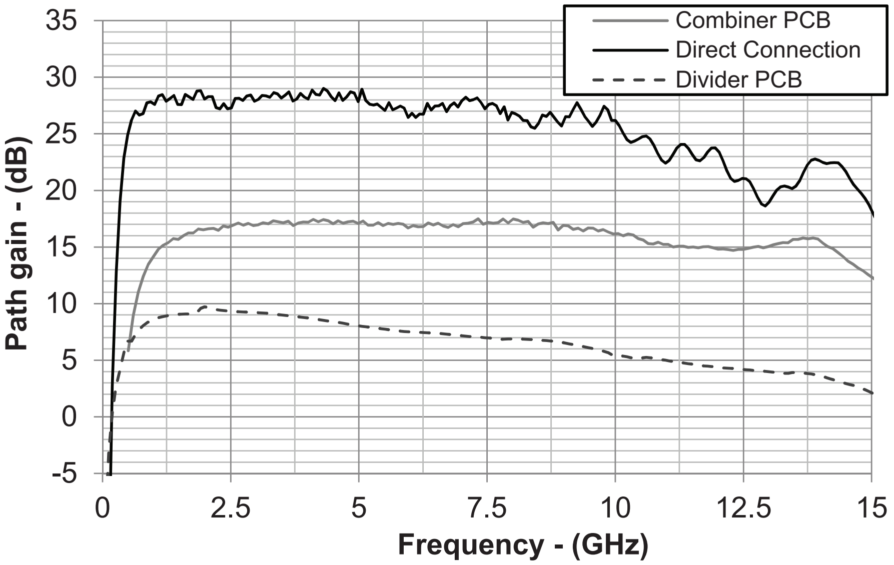


Figure 7.21: Measured gain of the circuit of Fig. 7.20, and comparison against the gains of the combiner and divider PCBs in Fig. 7.9 and 7.11 respectively.

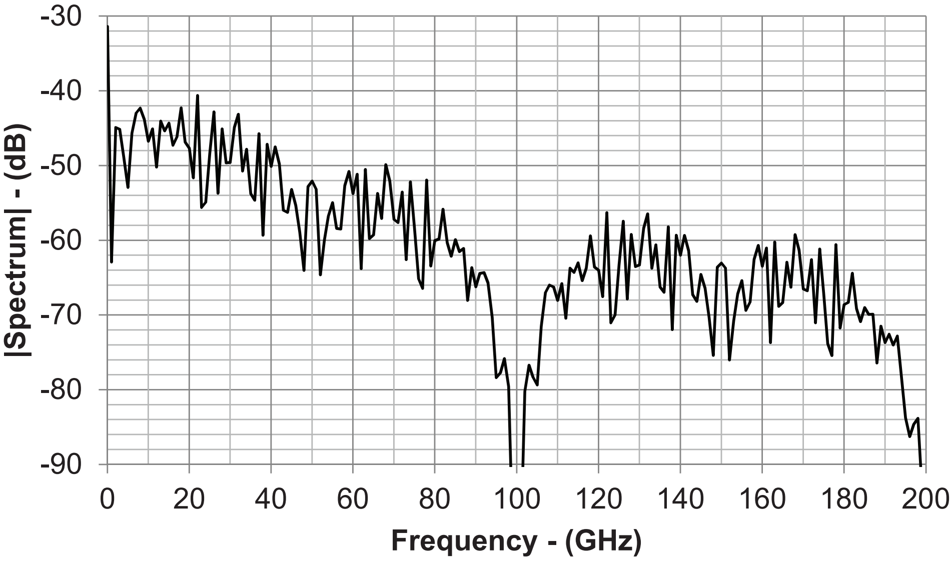


Figure 7.22: Simulated spectrum of a 100 Gbps pseudo-random non-return-to-zero bitstream.

regulations are imposed in accessing this crowded frequency region. On the other hand, in the last decade front-ends capable of operation at the millimeter-wave frequencies have been demonstrated [3, 4]. In particular, there is a keen research interest for the frequency bands above 95 GHz, which at time of writing remain unallocated and unlicensed [83].

The hardware presented in this thesis has been designed to be employed in future transceivers operating between 100 GHz and 300 GHz. A simulation test is here described to show the capability of the demonstrated circuits. A transmission of a pseudo-random non-return-to-zero bitstream with a data rate of 100 Gbps is considered. The signal is shown in the frequency domain in Fig. 7.22: its single-

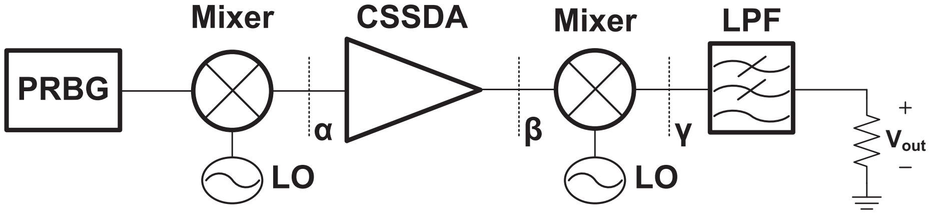


Figure 7.23: Simulation setup to evaluate the response of the CSSDA of Section 3.6 to the 100 Gbps bitstream of Fig. 7.22 modulated at 180 GHz.

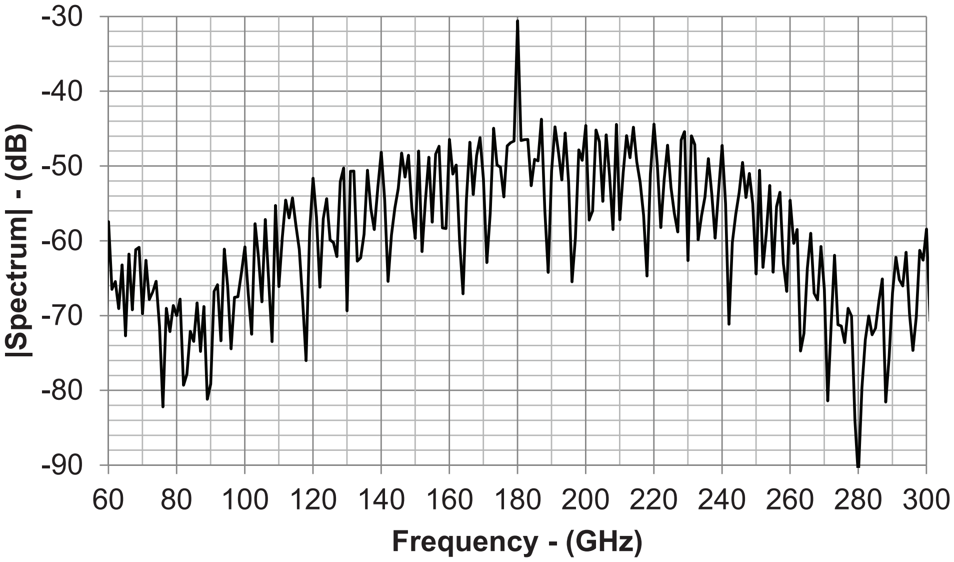


Figure 7.24: Simulated spectrum of a 100 Gbps pseudo-random non-return-to-zero bitstream (Fig. 7.22) modulated at 180 GHz, as the signal at the interface α in Fig. 7.23.

sideband is 100 GHz. Fig. 7.23 shows the simulation setup. The pseudo-random bit generator with period 10 ps is connected to a mixer, modeled in Verilog-A, which provides 0 dB gain, 50 Ohm input and output matching and 50 dB isolation between its ports. The LO signal is a sinusoid at 180 GHz. The modulated signal is applied to the CSSDA presented in Section 3.6. The model used for the CSSDA also considers its noise and linearity. A second mixer, identical to the first one, is employed for the down conversion. Finally, a Butterworth low-pass filter of the second order, also modeled with a Verilog-A code, and with -3 dB corner frequency of 100 GHz is used to integrate the signal. The filter has 0 dB losses and 50 Ohm input and output matching. The simulation aims to show the capability of the CSSDA to amplify input signals with 100 Gbps data rate and 100 GHz bandwidth.

Fig. 7.24 shows the spectrum of the modulated signal: the majority of its energy is concentrated between the first notches of its envelope which occur at

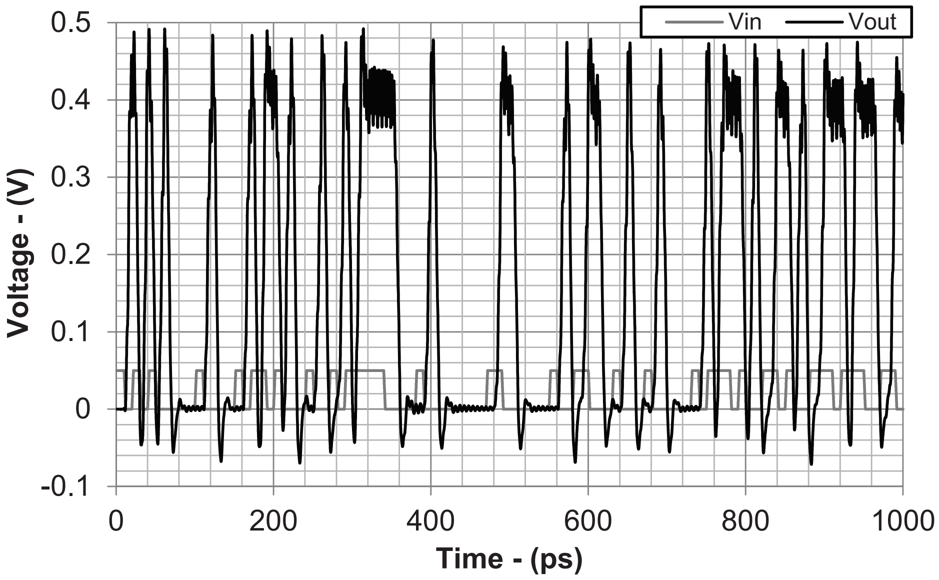


Figure 7.25: Simulated 100 Gbps pseudo-random non-return-to-zero bitstream used as input of the setup in Fig. 7.23, and relative output.

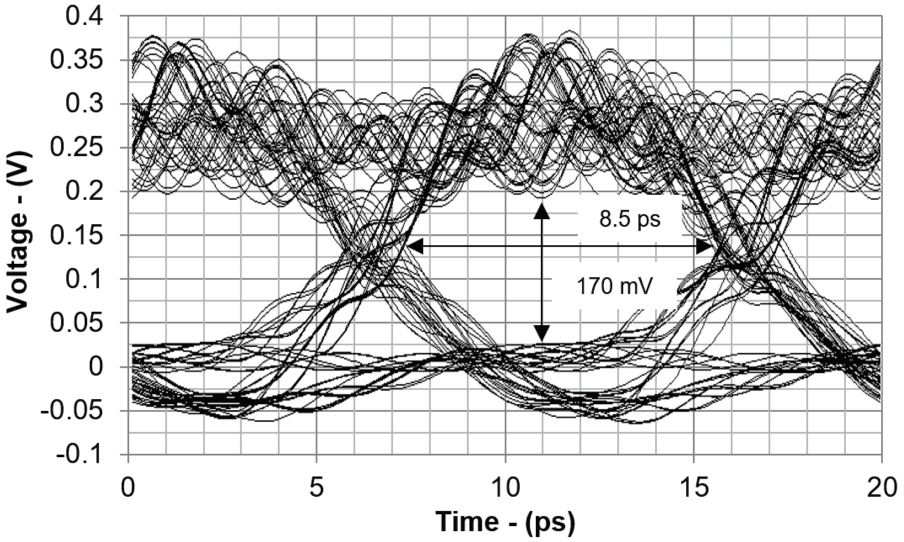


Figure 7.26: Simulated eye diagram of the output signal of Fig. 7.25.

80 GHz and 280 GHz. This frequency range is mostly covered by the spectrum of amplification of the CSSDA, which spans from 90 GHz to 250 GHz (Fig. 3.39). Fig. 7.25 presents the input and output bitstreams of the simulation setup, while the eye diagram of the output is given in Fig. 7.26. The opening of the eye is 170 mV in voltage and 8.5 ps in time confirming the suitability of the amplifier for 100 Gbps and 100-GHz-wide communications.

8 Conclusions

8.1 Summary

In this thesis, novel ultra-wideband amplifiers operating at millimetre-wave frequencies have been presented. The demonstrated components are based on distributed and resonant-matching techniques, while their primary application is in receiver front-ends where also antennas are integrated on the chip.

As shown in Chapter 3, the high frequency operation of distributed amplifiers is mainly limited by the synthetic-line losses. This work proposed as solution to this limitation a novel cascode gain cell with three transistors which is able to compensate the synthetic losses of TWAs up to higher frequencies.

Furthermore, distributed amplifiers with a reduced number of cells have been found suitable for high-frequency operation. This concept is used in CSSDAs, where single-cell distributed amplifiers are cascaded to increase the gain. The available knowledge on CSSDAs has been extended by this work presenting the first complete circuit analysis for this kind of amplifiers. Based on the improved understanding of CSSDAs, three amplifiers of this class have been developed. The first CSSDA targets low-power consumption, while the second is capable of useful amplification up to 250 GHz, establishing a record result for silicon-germanium distributed amplifiers. The third CSSDA uses a balanced approach to compensate the input and output matching degradation toward high frequency, which is an intrinsic limitation of CSSDAs.

This thesis embraced also the development of ultra-wideband distributed combiners and dividers demonstrating the first components of this class operating from the MHz frequencies until 200 GHz. As Chapter 4 illustrated, these results improve the state of the art by a factor of five in terms of maximum frequency of operation and bandwidth. Ultra-wideband amplifiers based on resonant matching have been also investigated, and the results are discussed in Chapter 5. A resonant-matched amplifier with centre frequency of 185 GHz and the broadest bandwidth for SiGe implementations has been demonstrated. A multi-stub-matching approach enabled this result.

Finally, a CSSDA capable of operation till 250 GHz has been integrated with an on-chip Vivaldi antenna to realize the first stage of an ultra-wideband sub-THz receiver. The high-frequency operation reduced the antenna physical dimensions minimizing the overall fabrication costs. The antenna-amplifier sub-system demonstrated useful amplification from 140 GHz to 220 GHz. This result is the ultimate goal of the presented research: the bandwidth of the antenna-amplifier systems, to be used as the first-stage of receiver front-ends, has been improved by a factor of two against the state of the art. Chapter 6 discussed in depth the antenna-amplifier integration, as well as the employment of this sub-system in a complete receiver chain. The results achieved within the frame of this thesis have been published in eight prestigious journals and thirteen conferences.

8.2 Outlook

At the writing time, the investigation on ultra-wideband amplifiers based on distributed techniques is still in progress. Therefore, future works will cover the development of complete receiving and transmitting front-ends, as well as the demonstration of wireless communications over ultra-wideband channels.

To develop the amplifiers used in the transmitter side, distributed amplification techniques will be adopted in conjunction with power combining approaches to increase the transmitted power. This, in turn, will extend the maximum communication distance and the obtainable data rate. Other challenges to be faced are the realization of ultra-wideband up- and down-conversion mixers, and baseband amplifiers. Also here distribution techniques can be applied as the possible solution.

Power combiners and dividers with very broad frequency-band of operation will pave the way for multi-antenna systems providing high antenna-array gain and thus larger communication distances when compared to single-antenna approaches.

9 Appendix I: Calculation of the Triple-Cascode Cell Gm

This appendix presents the calculation of the transconductances of inductively-peaked cascode (Fig. 3.7b) and triple-cascode (Fig. 3.7c) gain-cells presented in Section 3.3.1.

Fig. 9.1 shows the small signal circuit used for the $\mathrm{G_m}$ calculation of the inductively-peaked cascode cell (Fig. 3.7b). The resistances $\mathrm{r_{e0}}$, $\mathrm{r_{b0}}$ and $\mathrm{r_{b1}}$ of the circuit in Fig. 3.7b are neglected, and the small-signal values of the transistors $\mathrm{Q_0}$ – $\mathrm{Q_1}$ are assumed identical, in order to simplify the analysis. The equivalent cell transconductance is defined as the ration between short output-current i_{out} and input voltage v_{in} of the cell:

$$G_m = \frac{i_{out}}{v_{in}} \tag{9.1}$$

The capacitor $\mathrm{C_{bc1}}$ is suspended between ground nodes, and it does not contribute to the response of the system. The current i_{out} can be then related to v_{be1} as:

$$i_{out} = g_m v_{be1} \tag{9.2}$$

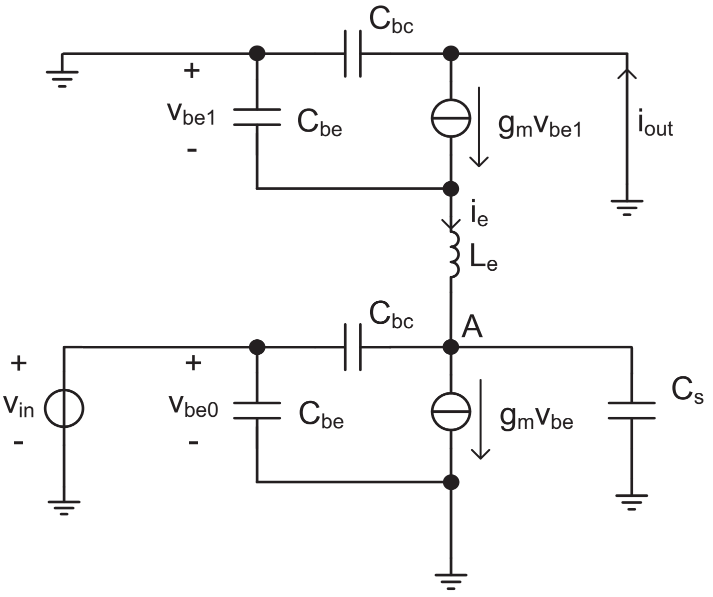


Figure 9.1: Small-signal circuit used for the $\mathrm{G_m}$ calculation of inductively-peaked cascode gain-cell (Fig. 3.7b), where the resistances $\mathrm{r_{e0}}$, $\mathrm{r_{b0}}$ and $\mathrm{r_{b1}}$ are neglected, and the small-signal values of the transistors $\mathrm{Q_0}$ – $\mathrm{Q_1}$ are assumed identical to simplify the analysis.

while the current i_e is related to v_be1 and i_out as:

$$i_e = i_{out} + j\omega C_{be} v_{be1} = i_{out}\left(1 + j\omega\frac{C_{be}}{g_m}\right) \tag{9.3}$$

and to v_be1 and v_A as:

$$i_e = -\frac{v_{be1} + v_A}{j\omega L_e} \tag{9.4}$$

Combining equations (9.2), (9.3) and (9.4) the relation between v_A and i_out is derived as:

$$v_A = -\frac{i_{out}}{g_m}\left(1 + j\omega L_e g_m - \omega^2 C_{be} L_e\right) \tag{9.5}$$

Applying the Kirchhoff current-law at node A (Fig. 9.1) the following relation between v_A, v_in and i_e is derived:

$$j\omega C_s v_A + g_m v_{in} + j\omega C_{bc}\left(v_A - v_{in}\right) = i_e = i_{out}\left(1 + j\omega\frac{C_{bc}}{g_m}\right) \tag{9.6}$$

which isolating v_in and v_A becomes:

$$\left(g_m - j\omega C_{bc}\right) v_{in} + j\omega\left(C_s + C_{bc}\right) v_A = \left(1 + j\omega\frac{C_{bc}}{g_m}\right) i_{out} \tag{9.7}$$

Combining equations (9.5) and (9.7) the relation between v_in and i_out is:

$$\left(g_m - j\omega C_{bc}\right) v_{in} - \frac{i_{out}}{g_m}\left(1 + j\omega L_e g_m - \omega^2 C_{be} L_e\right) j\omega\left(C_s + C_{bc}\right) = \left(1 + j\omega\frac{C_{bc}}{g_m}\right) i_{out} \tag{9.8}$$

The G_m of the inductively-peaked cascode gain-cell can be then calculated as:

$$G_m = \frac{i_{out}}{v_{in}} =$$
$$\frac{g_m\left(g_m - j\omega C_{bc}\right)}{g_m + j\omega C_{be} + j\omega\left(C_s + C_{bc}\right) - \omega^2 L_e g_m\left(C_s + C_{bc}\right) - j\omega^3 C_{be} L_e\left(C_s + C_{bc}\right)}$$

which can be reorganized as:

$$G_m = \frac{g_m(g_m - j\omega C_{bc})}{g_m\left[1 - \omega^2 L_e(C_{bc} + C_s)\right] + j\omega\left[C_s + C_{bc} + C_{be} - \omega^2 L_e C_{be}(C_s + C_{bc})\right]} \tag{9.9}$$

as presented in eq. (3.9) in Section 3.3.1.

The calculation of the transconductance of triple-cascode (Fig. 3.7c) gain-cells is also here presented. The small-signal circuit used for the circuit analysis is shown in Fig. 9.2. Same simplifications apply as above. The current i_out is related to v_{be2} as:

$$i_{out} = g_m v_{be2} \tag{9.10}$$

while the current i_{e2} is related to v_{be2} and i_{out} as:

$$i_{e2} = i_{out} + j\omega C_{be} v_{be2} = i_{out}\left(1 + j\omega\frac{C_{be}}{g_m}\right) = v_{be2}\left(g_m + j\omega C_{be}\right) \tag{9.11}$$

and to v_{be2} and v_{B} as:

$$i_{e2} = -\frac{v_{be2} + v_B}{j\omega L_e} \tag{9.12}$$

Combining equations (9.10), (9.11) and (9.12) the relation between v_{B} and v_{be2} is calculated as:

$$v_B = -v_{be2}\left[1 + j\omega L_e\left(j\omega C_{be} + g_m\right)\right] \tag{9.13}$$

Applying the Kirchhoff current-law at node B (Fig. 9.2) the following relation

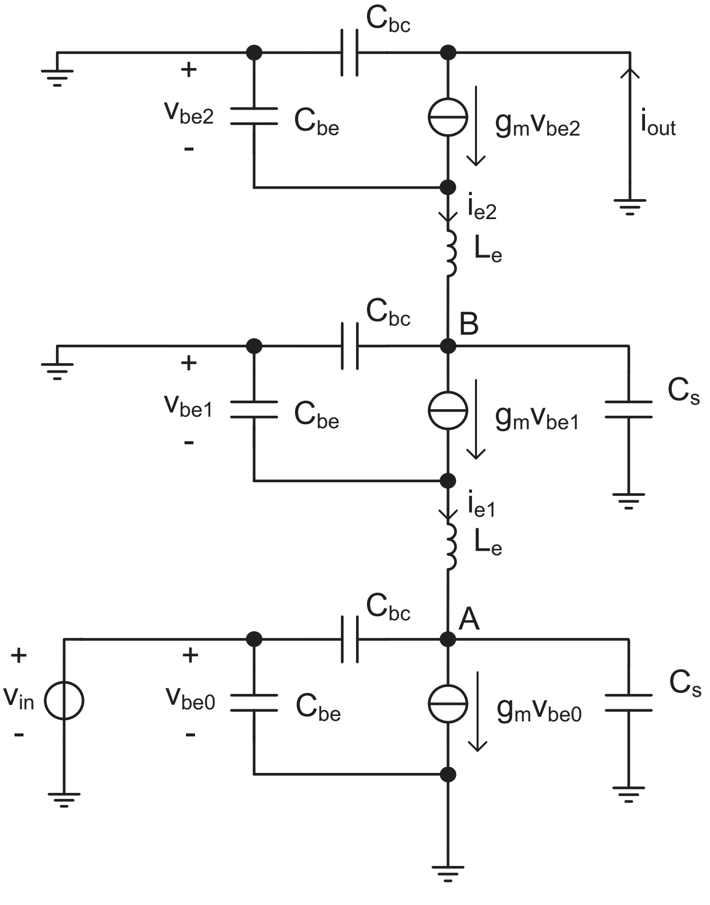

Cbc
+
vbe2
-
Cbe
gmvbe2
iout
ie2
Le
Cbc
B
+
vbe1
-
Cbe
gmvbe1
Cs
ie1
Le
Cbc
A
+
vin
-
+
vbe0
-
Cbe
gmvbe0
Cs

Figure 9.2: Small-signal circuit used for the G_m calculation of the triple-cascode cell (Fig. 3.7c), where the resistances r_{e0}, r_{b0} and r_{b1} are neglected, and the small-signal values of the transistors Q_0 – Q_1 are assumed identical to simplify the analysis.

between v_{B}, v_{be1} and i_{e2} is derived:

$$j\omega\left(C_s+C_{bc}\right)v_B+g_m v_{be1}=i_{e2} \tag{9.14}$$

which substituting the expression of v_{B} (eq. (9.13)) becomes:

$$-v_{be2}\left[1+j\omega L_e\left(j\omega C_{be}+g_m\right)\right]j\omega\left(C_s+C_{bc}\right)+g_m v_{be1}=i_{e2}=v_{be2}\left(g_m+j\omega C_{be}\right) \tag{9.15}$$

$$g_m v_{be1}=v_{be2}\{g_m+j\omega C_{be}+\left[1+j\omega L_e\left(j\omega C_{be}+g_m\right)\right]j\omega\left(C_s+C_{bc}\right)\} \tag{9.16}$$

The current i_{e1} is related to v_{be1} as:

$$i_{e1}=g_m v_{be1}+j\omega C_{be}v_{be1}=v_{be1}\left(g_m+j\omega C_{be}\right) \tag{9.17}$$

Applying the Kirchhoff current-law at node A (Fig. 9.2) the following relation between v_{A}, v_{in} and i_{e1} is derived:

$$j\omega C_s v_A+g_m v_{in}+j\omega C_{bc}\left(v_A-v_{in}\right)=i_{e1} \tag{9.18}$$

which isolating v_{in} and v_{A} becomes:

$$\left(g_m-j\omega C_{bc}\right)v_{in}+j\omega\left(C_s+C_{bc}\right)v_A=i_{e1} \tag{9.19}$$

The relations between i_{e1}, v_{A} and v_{be1} are:

$$i_{e1}=-\frac{v_{be1}+v_A}{j\omega L_e}\qquad i_{e1}=v_{be1}\left(g_m+j\omega C_{be}\right)\qquad v_A=-v_{be1}\left[1+j\omega L_e\left(j\omega C_{be}+g_m\right)\right]$$

Substituting these relations in eq. (9.19) the relation between v_{in} and v_{be1} is:

$$\left(g_m-j\omega C_{bc}\right)v_{in}=\{g_m+j\omega C_{be}+j\omega\left(C_s+C_{bc}\right)\left[1+j\omega L_e\left(g_m+j\omega C_{be}\right)\right]\}v_{be1} \tag{9.20}$$

Combining equations (9.10), (9.16) and (9.20), the relation between v_{in} and i_{out} is:

$$G_m=\frac{i_{out}}{v_{in}}=$$
$$\frac{g_m^2\left(g_m-j\omega C_{bc}\right)}{\{g_m+j\omega C_{be}+j\omega\left(C_s+C_{bc}\right)-\omega^2 L_e g_m\left(C_s+C_{bc}\right)-j\omega^3 C_{be}L_e\left(C_s+C_{bc}\right)\}^2}$$

which can be reorganized as:

$$G_m=\frac{g_m^2(g_m-j\omega C_{bc})}{\{g_m\left[1-\omega^2 L_e(C_{bc}+C_s)\right]+j\omega\left[C_s+C_{bc}+C_{be}-\omega^2 L_e C_{be}(C_s+C_{bc})\right]\}^2} \tag{9.21}$$

in the same manner as it is presented in eq. (3.10) of Section (3.3.1).

10 Appendix II: Considerations on Single-Stage DAs

This appendix describes the use of the single-stage distributed-amplifier as the base building block of CSSDAs and TWAs. In the available literature, the expressions *distributed amplifier* and *traveling-wave amplifier* are often misused to indicate the same broadband-amplifier topology. The misuse of terminology originates from the fact that the first demonstrated distributed amplifiers were traveling-wave amplifiers [20, 21]. On the other hand, in a broader context, distributed-amplifier techniques can be classified as the ones where the input and output capacitances of active devices – electron tubes or transistors – are combined with inductors to form synthetic transmission-lines. These synthetic transmission-lines enjoy wideband frequency responses: from dc up to the cutoff frequency of the synthetic-lines themselves. The technique does not necessarily require multiple stages and is still viable for single-cell implementations.

A simulation example is presented in Fig. 10.1 to illustrate how the core equations of distributed amplifiers hold independently from the number of cells involved, and hence the number of load capacitors connected along the transmission lines. Considering a cell input or output capacitance $C_{\text{in,out}}$ of 20 fF, a distance between the cells ℓ of 50 µm, line inductance and capacitance per unit-of-length L' and C' equal to 1 µH/m and 1 fF/m, respectively; then the resulting synthetic transmission-line will have a characteristic impedance Z_S of 50 Ω, and the synthetic line will be functional up to the Bragg cutoff frequency $f_{\text{Bragg\_Synthetic}}$ of 318 GHz. The analytic expressions of Z_S and $f_{\text{Bragg\_Synthetic}}$ are reported in eq. (3.1) and (3.3).

Fig. 10.1 shows the simulation setup used to emulate the input or output lines of distributed amplifiers formed by one, two, and four cells. The results regarding $|S_{11}|$ and $|S_{21}|$ are presented in Fig. 10.2. Two important considerations can be made: the simulated $|S_{21}|$ shows that a signal can propagate into the synthetic-

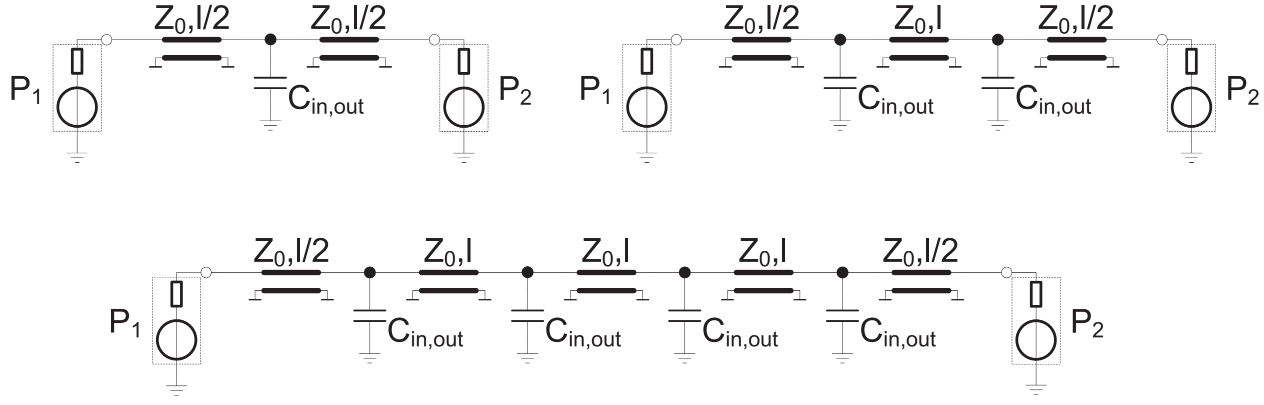
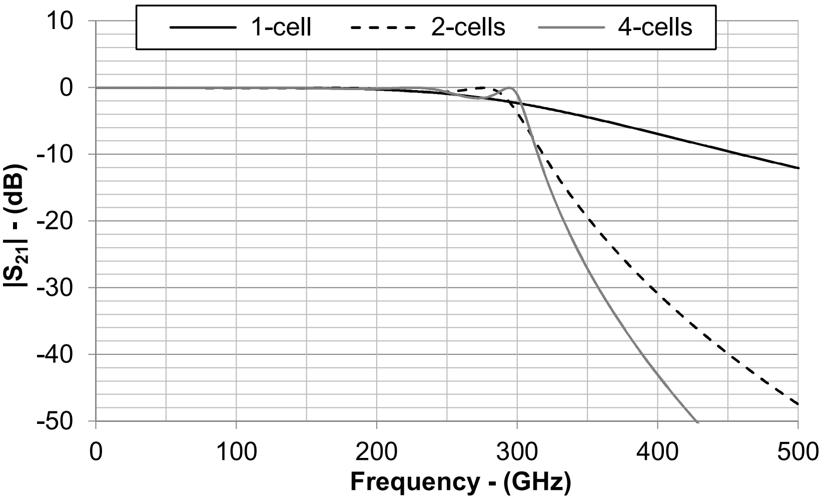
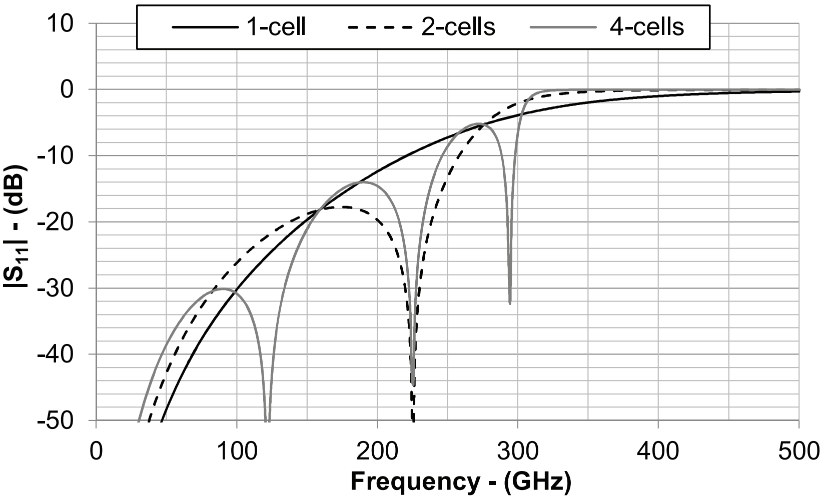


Figure 10.1: Simulation setup used to emulate the input or output lines of distributed amplifiers formed by one, two, and four cells.

line for frequencies up to $f_{\mathrm{Bragg\_Synthetic}}$ independently from the number of cells in use; the simulated $|S_{11}|$ shows that the characteristic impedance of the synthetic line deviates from eq. (3.1) for frequencies approaching $f_{\mathrm{Bragg\_Synthetic}}$, and with a trend whose envelope is independent of the number of employed cells. In this sense, the single-cell configuration is the basic block of distributed amplifiers, and CSSDAs or TWAs can be assembled depending upon its arrangement. In fact, CSSDAs are obtained cascading the single-cell blocks, while TWAs using them in a parallel-like connection.



(a)



(b)

Figure 10.2: Simulation results of the setup in Fig. 10.1: (a) S_{21} magnitude, (b) S_{11} magnitude.

Another observation which can be made is on the terminating resistance R_t. In TWAs, matched loads terminate the synthetic line on both sides. This could also be the case in CSSDAs as Fig. 10.3 illustrates. However, a significant drawback of this configuration is that half of the cell output-current i_{out} is dissipated in the termination resistor of the left side. For this reason, CSSDAs can be im-

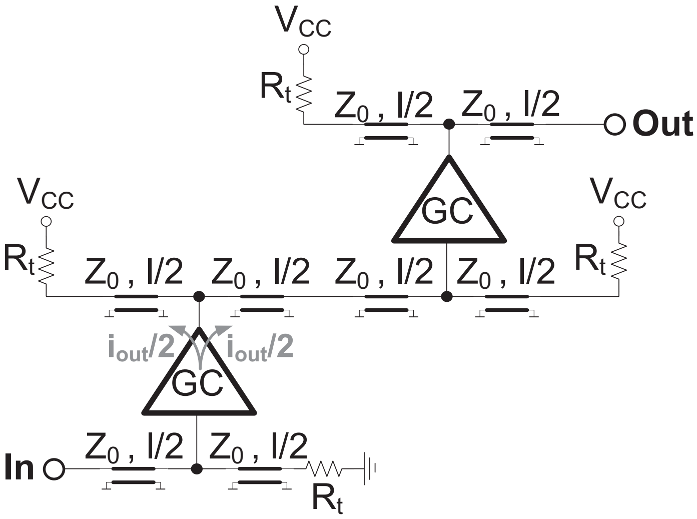

VCC
Rt
Z0 , l/2
Z0 , l/2
Out
VCC
VCC
GC
Rt
Z0 , l/2
Z0 , l/2
Z0 , l/2
Z0 , l/2
Rt
iout/2
iout/2
GC
In
Z0 , l/2
Z0 , l/2
Rt

Figure 10.3: CSSDA with termination resistors on both sides of the synthetic lines.

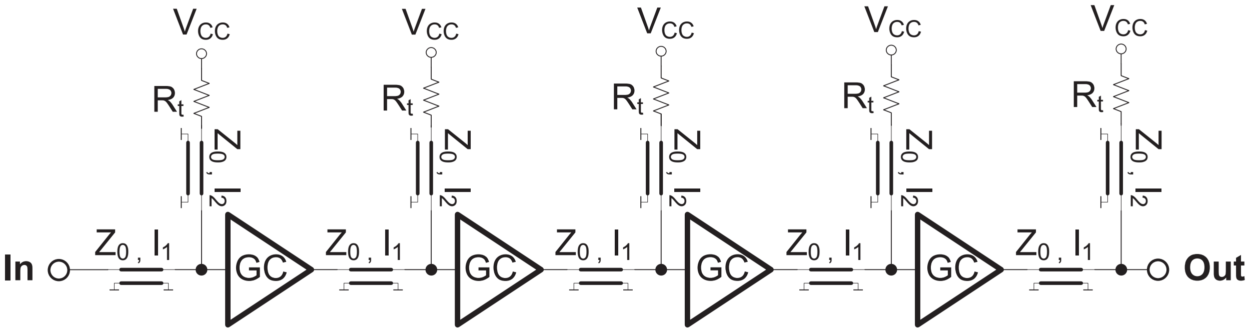

VCC
VCC
VCC
VCC
VCC
Rt
Rt
Rt
Rt
Rt
Z0 , l2
Z0 , l2
Z0 , l2
Z0 , l2
Z0 , l2
In
Z0 , l1
GC
Z0 , l1
GC
Z0 , l1
GC
Z0 , l1
GC
Z0 , l1
Out

Figure 10.4: Conventional CSSDA schematic.

proved by removing the left half of the output lines of each stage, resulting in the more-efficient structure presented in Fig. 10.4. In fact, in the conventional architecture of CSSDAs, shown in Fig. 10.4, the cell output-current feeds the next cell without partitioning. In this case, then, the output line of one stage is also the input line of the following one, hence the termination resistors $\mathrm{R_t}$ have the double function of terminating both lines. Finally, the output stage is also modified to achieve the resonant peaking and improve the response at the highest end of the amplification band, as discussed in Section 3.4.

11 Publications

Journal Articles

[Testa1] P. V. Testa, G. Belfiore, R. Paulo, C. Carta, F. Ellinger, "170 GHz SiGe-BiCMOS Loss Compensated Distributed Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 10, pp. 2228-2238, Oct. 2015.

[Testa2] P. V. Testa, C. Carta, F. Ellinger, "Analysis and Design of a 220 GHz Wideband SiGe BiCMOS Distributed Active Combiner," *IEEE Trans. Microw. Theory Tech.*, vol. 64, no. 10, pp. 3049-3059, Oct. 2016.

[Testa3] P. V. Testa, C. Carta, B. Klein, R. Hahnel, D. Plettemeier, F. Ellinger, "A 210 GHz SiGe Balanced Amplifier for Ultrawideband and Low-Voltage Applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 3, pp. 287-289, March 2017.

[Testa4] P. V. Testa, C. Carta, M. Barahona, F. Ellinger "0.5–20 GHz UWB distributed combiners for multi-antenna transceivers," in *IEEE Trans. Microw. Theory Tech.*, vol. 65, no. 9, pp. 3087-3098, Sept. 2017.

[Testa5] P. V. Testa, B. Klein, R. Hahnel, C. Carta, D. Plettemeier, F. Ellinger "On-Chip Integrated Distributed Amplifier and Antenna Systems in SiGe BiCMOS for Transceivers with Ultra-Large Bandwidth," *De Gruyter Frequenz*, vol. 71, no. 4, pp. 473-484, Sept. 2018.

[Testa6] P. V. Testa, C. Carta, U. Jörges, F. Ellinger, "Analysis and Design of a 30-220 GHz Balanced Cascaded Single-Stage Distributed Amplifier in 130 nm SiGe BiCMOS," in *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1457-1467, May 2018.

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[Testa9] P. V. Testa, C. Carta, F. Ellinger "200 GHz SiGe-BiCMOS Loss-Compensated Distributed Power Divider," in *IEEE Trans. Microw. Theory Tech.*, vol. 66, no. 9, pp. 3927-3936, Sept. 2018.

Conference Proceedings

[Testa10] P. V. Testa, V. Riess, C. Carta, F. Ellinger "Distributed Power Combiner and On-Chip Antennas for Sub-THz Multi-Band UWB Receivers," accepted at *IEEE International RF and Microwave Conference (RFM)*, Penang, Malaysia, Dec. 2018, pp. 1-4.

[Testa11] P. V. Testa, B. Klein, R. Hahnel, C. Carta, D. Plettemeier, F. Ellinger "140-220-GHz Distributed Antennas and Amplifiers Integrated in SiGe BiCMOS for UWB Receivers," accepted at *IEEE International Microwave Symposium (IMS)*, Philadelphia, Pennsylvania, USA, June 2018, pp. 1-3.

[Testa12] P. V. Testa, V. Riess, C. Carta, F. Ellinger "200 GHz Chip-to-Chip Wireless Power Transfer," in *Proc. IEEE Radio Wireless Week (RWW)*, Anaheim, California, USA, Jan. 2018, pp. 1-4.

[Testa13] P. V. Testa, D. Fritsche, S. Schumann, W. Finger, C. Carta, F. Ellinger "110 GHz Travelling-Wave Amplifier in 22 nm FD-SOI CMOS," in *Proc. IEEE Asia-Pacific Microwave Conference (APMC)*, Kuala Lumpur, Malaysia, Nov. 2017, pp. 1-4.

[Testa14] P. V. Testa, C. Carta, F. Ellinger "200 GHz SiGe-BiCMOS Loss-Compensated Distributed Power Divider," in *Proc. IEEE Asia-Pacific Microwave Conference (APMC)*, Kuala Lumpur, Malaysia, Nov. 2017, pp. 1-4.

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[Testa18] P. V. Testa, C. Carta, F. Ellinger, "220 GHz wideband distributed active power combiner," in *Proc. Asia-Pacific Microwave Conference (APMC)*, Nanjing, China, Dec. 2015, pp. 1-3.

[Testa19] P. V. Testa, R. Paulo, C. Carta, F. Ellinger, "250 GHz SiGe-BiCMOS Cascaded Single-Stage Distributed Amplifier," in *Proc. IEEE Compound Semiconductor IC Symposium (CSICS)*, New Orleans, Louisiana, USA, Oct. 2015, pp. 1-4.

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13 List of Abbreviations

AWGN	Additive White Gaussian Noise
BCSSDA	Balanced CSSDA
BJT	Bipolar Junction Transistor
BW	Bandwidth
CB	Common Base
CMOS	Complementary Metal-Oxide-Semiconductor
CPW	Conventional Pseudo-coplanar Waveguide
CSSDA	Cascaded Single-Stage Distributed Amplifier
BiCMOS	Bipolar Complementary Metal-Oxide-Semiconductor
DA	Distributed Amplifier
DC	Direct Current
DRC	Design Rule Check
EIRP	Effective Isotropic Radiated Power
Eq.	Equation
FCC	Federal Communications Commission
Fig.	Figure
FoM	Figure of Merit
FSPL	Free Space Path Losses
GCR	Gain Control Range
GaAs	Gallium Arsenide
GBP	Gain Bandwidth Product
$\mathrm{GBP}_{\mathrm{CSSDA}}$	CSSDA Gain-Bandwidth-Product
Gbps	Gigabits per second
GND	Ground
Kbps	Kilobits per second
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
i1dBCp	Input-Referred 1 dB Compression Point
ICs	Integrated Circuits
IIP3	Input-Referred Third-Order Intercept Point

IP3	Intercept Point of Third-Order
IR-UWB	Impulse Radio UWB
InP	Indium Phosphide
LC	Inductance Capacitance
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low-Pass Filter
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuit
mm-Wave	Millimeter Wave
MAG	Maximum Available Gain
MB-OFDM	Multi-Band Orthogonal Frequency-Division Multiplexing
MDS	Minimum Detectable Signal
MOS	Metal-Oxide-Semiconductor
NF	Noise Figure
npn	negative-positive-negative
o1dBCp	Output-Referred 1 dB Compression Point
OIP3	Output-Referred Third-Order Intercept Point
PDK	Process Design Kit
PGS	Patterned Ground Shields
PLL	Phase-Locked Loop
SFDR	Spurious Free Dynamic Range
Si	Silicon
SiGe	Silicon Germanium
SNR	Signal-to-Noise Ratio
SOI	Silicon On Insulator
SPD	Spectral Power-Density
SRF	Self Resonance Frequency
RC	Resistance Capacitance
RF	Radio Frequency
RMA	Resonant Matched Amplifier
SNR	Signal to Noise Ratio

SOLT	Short Open Load Through
SFR	Self Resonance Frequency
Sub-A	Sub-Amplifier
TL	Transmission Lines
Tab.	Table
TRL	Transmission Reflection Line
TWA	Traveling-Wave Amplifier
TWC	Traveling-Wave Combiner
TWD	Traveling-Wave Dividers
UWB	Ultra-Wide Band
VGA	Variable Gain Distributed Amplifiers
VNA	Vector Network Analyzer
WMN	Wideband Matching Networks

14 List of Symbols

α	Attenuation constant of transmission lines
α_C	Attenuation of cables
α_in	Attenuation constant of the input synthetic line multiplied by the cells distance
$\alpha_\mathrm{in}{}'$	Attenuation constant of the input synthetic line
A_Line	Attenuation of a transmission line
α_out	Attenuation constant relative to the output synthetic line
β_s	Phase constant of synthetic transmission lines
c	Speed of light capacity
C	Channel capacity
$\mathrm{C'}$	Capacitance per unit-of-length of transmission lines
C_bc	Small-signal base-collector capacitance
C_be	Small-signal base-emitter capacitance
C_in	Small-signal input capacitance of the gain-cell
C_line	Transmission-line capacitance
Cmim	MIM capacitor offered by the *SG13G2* process
C_out	Small-signal output capacitance of the gain-cell
C_s	Small-signal collector-substrate capacitance
C_sub	Substrate capacitance
d	Transmitter-receiver distance
f	Signal frequency
ϕ_{21}	Phase of the forward transmission coefficient
f_{Cin}	Cutoff frequencies for the input line
f_Center	Central frequency of operation
f_{Cout}	Cutoff frequencies for the output line
$\mathrm{F}_\mathrm{CSSDA}$	CSSDA noise factor
$f_\mathrm{DOWN,3dB}$	$-3\,\mathrm{dB}$ lower frequency corner of operation
$\mathrm{F}_\mathrm{FollowingStage}$	Noise factor of the following stage
$f_\mathrm{LC\_Synthetic}$	Cutoff frequency of a synthetic transmission-line
$f_\mathrm{LC\_Synthetic\_Input}$	Cutoff frequency of a input synthetic-line in a DA
F_Line	Transmission line noise factor
f_{max}	Maximum oscillation frequency
$\mathrm{f}_\mathrm{R\text{-}OUT}$	Resonance frequency of the output network of a CSSDA
F_RX	Receiver noise factor

f_t	Transit frequency
$f_{\mathrm{UP,3dB}}$	$-3\,\mathrm{dB}$ upper frequency corner of operation
γ	Propagation constant of a transmission line
G'	Transmission-line conductance per unit-of-length
$\Gamma_{\text{1-O,L}}$	Reflection coefficient between first and second common base stages in Fig. 5.1
$\mathrm{G}_{\mathrm{Ant}}$	Antenna gain
Γ_{Ant}	Reflection coefficient of the antenna impedance
G_{C}	Combiner gain
$\mathrm{G}_{\mathrm{CSSDA}}$	CSSDA gain
$\Gamma_{\mathrm{IN,A}}$	Amplifier input reflection-coefficient
$\Gamma_{\mathrm{IN,CSSDA}}$	CSSDA input reflection-coefficient
$\Gamma_{\mathrm{L,1}}$	Load reflection coefficient of the first CB stage in Fig. 5.1b
g_{m}	Small-signal transconductance
G_{m}	Small-signal gain-cell equivalent transconductance
$\Gamma_{\mathrm{O,1}}$	Output reflection coefficient of the first CB stage in Fig. 5.1b
$\Gamma_{\mathrm{OUT,A}}$	Amplifier out reflection-coefficient
$\Gamma_{\mathrm{OUT,CSSDA}}$	CSSDA out reflection-coefficient
$\mathrm{G}_{\mathrm{R,ant}}$	Receiving antenna-gain
$\mathrm{G}_{\mathrm{T,ant}}$	Transmitting antenna-gain
$\mathrm{G}_{\text{Test-Antenna}}$	Test-antenna gain
$\mathrm{G}_{\mathrm{TWA}}$	TWA gain
$\mathrm{G}_{\mathrm{TWA,ideal}}$	TWA gain for the ideal case of no losses
$\mathrm{G}_{\mathrm{TWA,LF}}$	TWA gain at low frequency
$\mathrm{G}_{\mathrm{TWC}}$	TWC gain
I_{CC}	Collector bias-current
$\mathrm{I}_{\mathrm{CC\_emitter}}$	Collector bias-current per emitter
i_{O1}	Small-signal output current of the first CSSDA gain-cell
$\mathrm{i}_{\mathrm{O,Last}}$	Small-signal output current of the last CSSDA gain-cell
$\mathrm{i}_{\mathrm{out}}$	Small-signal output current of a gain cell
$\mathrm{i}_{\mathrm{out,L}}$	Small-signal cell output-current directed to the load
$\mathrm{i}_{\mathrm{out,T}}$	Small-signal cell output-current directed to the termination
i_{X}	Small-signal current leaving node X in Fig. 3.24
k	Boltzmann constant
ℓ	Distance between gain cells
l_{Line}	Length of a transmission line

$\mathrm{L'}$	Inductance per unit-of-length of transmission lines
$\lambda_{\mathrm{Guided}}$	Guided wavelength
ℓ_{IN}	Transmission line in series with the input of the cell in Fig. 3.48
$\mathrm{L_{line}}$	Transmission-line inductance
$\mathrm{L_{par}}$	Parasitic inductance
$\mathrm{L_{Probe}}$	Attenuation of the probe
M1	First metal layer of the *SG13G2* fabrication process
M2	Second metal layer of the *SG13G2* fabrication process
M3	Third metal layer of the *SG13G2* fabrication process
M4	Fourth metal layer of the *SG13G2* fabrication process
M5	Fifth metal layer of the *SG13G2* fabrication process
n	Number of gain cells
Ne	Number of the emitters
$\mathrm{N_0}$	Spectral power-density of the noise
ϕ_{21}	Phase of the forward transmission
$\mathrm{P_{AVG}}$	Available power of the generator
$\mathrm{P_{DC}}$	Dissipated power in continuous current-mode
$\mathrm{P_{IN}}$	Input power
$\mathrm{P_{IN,max}}$	Maximum input-power for a receiver
$\mathrm{P_{nf}}$	Noise-floor power
$\mathrm{P_{OUT}}$	Output power
$\mathrm{P_R}$	Received power
$\mathrm{R'}$	Transmission-line resistance per unit-of-length
$\mathrm{r_b}$	Small-signal base resistance
$\mathrm{r_e}$	Small-signal emitter resistance
$\mathrm{R_{in}}$	Small-signal gain-cell input-series resistance
$\mathrm{R_L}$	Load resistance
$\mathrm{R_{out}}$	Small-signal gain-cell output resistance
Rppd	Unsalicided resistor offered by the *SG13G2* process
Rsil	Salicided resistor offered by the *SG13G2* process
$\mathrm{R_{sub}}$	Substrate resistance
$\mathrm{R_t}$	Termination resistor
$\mathrm{R_{TC}}$	Termination resistor of Lange coupler
$[S_{Amp}]$	Amplifier scattering matrix
$S_{Amp_{ij}}$	Amplifier s-parameter at port i feeding power at port j

$[S_{Ant}]$	Antenna scattering matrix
$\mathrm{S_i}$	Power of the minimum detectable signal
$[S_{Line}]$	Transmission-line scattering matrix
$S_{M,21}$	Measured scattering parameter at port 2 feeding power at port 1
$\mathrm{SNR_{O,min}}$	Minimum acceptable SNR at the receiver output
$S_{Rec,21}$	Receiver scattering parameter at port 2 feeding power at port 1
$S_{Rec,21-Matched}$	$S_{Rec,21}$ in case of matching between antenna and amplifiers
ω	Signal angular frequency
$\mathrm{T_a}$	Antenna noise-temperature
TM1	Sixth metal layer of *SG13G2* process
TM2	Seventh metal layer of *SG13G2* process
$\mathrm{T_{REC}}$	Receiver noise-temperature
t_p	Group delay
$\mathrm{v_1}$	Small-signal voltage across the first gain-cell $\mathrm{C_{in}}$ in a CSSDA
$\mathrm{v_2}$	Small-signal voltage across the second gain-cell $\mathrm{C_{in}}$ in a CSSDA
$\mathrm{v_{be}}$	Small-signal base-emitter voltage
$\mathrm{V_{CE}}$	Collector-emitter bias voltage
$\mathrm{V_{CC}}$	Voltage-supply
$\mathrm{v_{in}}$	Small-signal input voltage
$\mathrm{v_N}$	Small-signal voltage across the $\mathrm{(N)^{TH}}$ gain-cell $\mathrm{C_{in}}$ in a CSSDA
$\mathrm{v_{N\text{-}1}}$	Small-signal voltage across the $\mathrm{(N\text{-}1)^{TH}}$ gain-cell $\mathrm{C_{in}}$ in a CSSDA
$\mathrm{v_{out}}$	Small-signal output voltage
$\mathrm{V_t}$	Thermal voltage
$\mathrm{v_X}$	Small-signal voltage at node X in Fig. 3.24
$\mathrm{Y_{CO}'}$	Admittance defined in the output-stage of CSSDAs in Fig. 3.25
$\mathrm{Y_{OUT}}$	Output admittance of CSSDAs
$\mathrm{Y_T'}$	Admittance defined in the output-stage of CSSDAs in Fig. 3.25
$\mathrm{Z_0}$	Characteristic impedance of a transmission line
$\mathrm{Z_{Sin}}$	Input characteristic synthetic-line impedance

Z_{Sout}	Output characteristic synthetic-line impedance
Z_{G}	Generator impedance
Z_{IN}	Input impedance
Z_{L}	Load impedance
$Z_{\mathrm{L+Stub}}$	Impedance defined in the circuit presented in Fig. 3.25
Z_{S}	Characteristic synthetic-line impedance
Z_{T}	Impedance defined in Fig. 3.46
$Z_{\mathrm{T\_over\_S}}$	Impedance defined in Fig. 3.46

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17 Curriculum Vitae

Paolo Valerio Testa, Ph.D. Candidate
born on 10th August 1987, in Nocera Inferiore – Italy
paolo_valerio.testa@tu-dresden.de
paolovalerio.testa@libero.it

Professional Experience

Since 06/2018	Group leader of the 5 G research team within the Chair for Circuit Design and Network Theory (CCN) of the Technische Universität Dresden, Dresden, Germany.
Since 12/2015	GWT-Contractor for GlobalFoundries as millimeter-wave circuit designer for 22 nm FD-SOI CMOS technology, Dresden, Germany.
Since 07/2013	Research Engineer within the Chair for Circuit Design and Network Theory (CCN) of the Technische UniversitätDresden, Dresden, Germany, contributing to public and private founded projects *DAAB, DAAB-Tx, SPARS, Prosecco, FAST-Spot, AutoSWIFT.*
09/2012 - 07/2013	Researcher within the Photonics and Semiconductor Nanophysics (PSN) group of the Technische Universiteit Eindhoven, Eindhoven, The Netherlands, focusing on *Integrated Plasmon-Polaritons Nanolasers.*
02/2012 - 07/2012	Research Engineer within the Fraunhofer-Institut für Hochfrequenzphysik und Radartechnik (FHR) in Bonn, Germany, contributing to the development of *A multi GPU implementation of SAR Back-Projection system for real-time processing.*
09/2011 - 11/2011	Internship at DiBET of the Università degli Studi di Napoli Federico II, Naples, Italy, focusing on *CUDA algorithms for digital signal processing.*
09/2009 - 11/2009	Internship at ST Microelectronics Arzano, Naples, Italy, on *Thermographic System and Analysis for Defect Detection in Flash NAND Memories.*

Education

07/2013 - 07/2017	Ph.D. Studies in Millimeter-Wave and Ultra-Wideband Circuit Design within the Chair for Circuit Design and Network Theory (CCN) of the Technische Universität Dresden, Dresden, Germany, with thesis title *Ultra-Wideband BiCMOS Receivers based on Integrated Distributed Antenna-Amplifier Architectures.*
01/2010 - 01/2012	Master Degree Studies in Electrical Engineering at Università degli Studi di Napoli Federico II, Naples, Italy, final mark *110/110 Full Marks and Honours* with thesis title *A multi GPU implementation of SAR Back-Projection.*
10/2006 - 12/2009	Bachelor Degree Studies in Electrical Engineering at Università degli Studi di Napoli Federico II, Naples, Italy, final mark *110/110 Full Marks and Honours* with thesis title *Bragg Gratings in Microstructured Optical Fibers.*
09/2001 - 06/2006	High School of Science within the National Plan for Informatics (PNI), Nocera Inferiore, Italy, final mark *100/100.*

Awards

11/2017	Best Student-Paper Award at IEEE Asia-Pacific Microwave Conference (APMC) 2017.
06/2017	Gold Leaf Award (top best 10%) for conference paper at IEEE PRIME 2017.
04/2009	Among the Best 2^{nd}-year students in Electronic Engineering for the academic year 2006-2007 at Università degli Studi di Napoli Federico II, Naples, Italy.
02/2008	Best 1^{st}-year student in Electronic Engineering for the academic year 2006-2007 at Università degli Studi di Napoli Federico II, Naples, Italy.

Languages

English
German
Italian
Spanish

Leisure

Sports	Chess, Basket, Kung Fu, Modeling.
Reading	I. Asimov, P. Cohelio, V.M. Manfredi.
Travels	