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Characterization and Evaluation of a 6.5-kV Silicon Carbide Bipolar Diode Module

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CHARACTERIZATION AND EVALUATION OF A 6.5-KV SILICON CARBIDE BIPOLAR DIODE MODULE

Felipe Filsecker

DISSERTATION

Referee
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CONTENTS

NOMENCLATURE

A	Area of the device
C	Cost function
C_{CA}	Diode's cathode-anode capacitance
$C_{CA,ref}$	Diode's reference cathode-anode capacitance
C_{dc}	DC-link capacitance
C_j	Junction capacitance
C_s	*RC* snubber capacitance
c_{sw}	Cost factor that evaluates the switching events in the MPC algorithm
D	Diode symbol in the equivalent circuits
D_{in}	Inner diodes in an NPC converter
D_{np}	Neutral point diodes in an NPC converter
D_{out}	Outer diodes in an NPC converter
di_{rr}/dt	Diode's reverse recovery current change rate after I_{rrm}
E	Electric field
E_C	Critical electric field strength
E_{Cs}	Stored energy in the snubber capacitor C_s
$E_{D,int,off}$	Turn-off losses in the diode itself (no additional *RC* snubber losses)
$E_{D,int,on}$	Turn-on losses in the diode itself (no additional *RC* snubber losses)
$E_{D,off}$	Turn-off losses in the diode (including *RC* snubber if present)
E_g	Band gap
E_{sw}	Switching losses
f_c	Cut-off frequency
f_r	Resonant frequency in *RLC* circuit
f_s	Sampling frequency of the MPC algorithm
f_{sw}	Switching frequency (carrier signal frequency in PWM)
G	Time-continuous transfer function
h	Harmonic of order h
h_{max}	Maximum harmonic order considered for the WTHD calculation
I_D	Diode current

i_D	Diode current (time dependent)
$i_{D,int}$	Diode current excluding the *RC* snubber current (time dependent)
i_E	Electron recombination current
I_F	Diode forward current
i_H	Hole recombination current
$\mathbf{i}_L$	Load current (space vector)
I_L	Load current
i_L	Load current (time dependent)
I_{out}	Converter output current (rms value)
i_{ph}	Phase current
$\mathbf{i}_{ref}$	Reference current in the MPC algorithm (space vector)
I_{rrm}	Diode's reverse recovery current maximum value
i_s	*RC* snubber current (time dependent)
i_T	IGBT current (time dependent)
J_F	Diode forward current density
k	Current sampling instance in the MPC algorithm
k_B	Boltzmann constant (1.38066×10^{-23} J/K)
k_{drift}	Proportionality constant relating V_{drift} and J_F
L	Load inductor
L_σ	Stray inductance
$L_{\sigma,D}$	Stray inductance inside the diode module
m	Number of switching states in a converter
m_a	Modulation index
N	Time horizon in model predictive control
n	Electron density
N_D	Donor doping density
n_i	Intrinsic carrier density
n_R	Electron density near the nn^+ junction in a PiN diode
$\overline{p}$	Average hole density
p	Hole density
p_L	Hole density near the p^+n junction in a PiN diode
$P_{tot,sc}$	Total semiconductor device losses (conduction and switching)
P_{cond}	Conduction losses
q	Elementary charge (1.60218×10^{19} As)
Q	Charge
Q_F	Stored charge of the PiN diode
R	Load resistor
R_{ho}	High-ohmic resistance for the estimation of C_j
$R_{g,on}$	IGBT's gate drive unit turn-on resistance
R_p	Parallel resistance for static voltage balancing of series-connected IGBTs
R_s	*RC* snubber resistance
$R_{th,ch}$	Thermal resistance, case to heat sink
$R_{th,ha}$	Thermal resistance, heat sink to ambient

$R_{th,jc}$	Thermal resistance, junction to case
$R_{th,jh}$	Thermal resistance, junction to heat sink
s	Laplace variable
S_C	Converter power
T	IGBT symbol in the equivalent circuits
T_{in}	Inner IGBTs in an NPC converter
T_{out}	Outer IGBTs in an NPC converter
t	Time
t_{rr}	Diode's reverse recovery current duration
V_B	Breakdown voltage
v_C	Voltage of the snubber capacitor (time-dependent)
$\mathbf{v}_{conv}$	Converter output voltage (space vector)
V_D	Diode's anode-cathode voltage
$v_{D,int}$	Diode's anode-cathode internal voltage in the device simulation model (time dependent)
v_D	Diode's anode-cathode voltage (time dependent)
V_{dc}	DC-link voltage
v_{dc}	DC-link voltage (time dependent)
$v_{D,probe}$	Diode's anode-cathode voltage at the module terminals, including internal stray inductance (time dependent)
V_{drift}	Drift zone voltage
V_F	Diode forward voltage
v_F	Diode forward voltage (time dependent)
V_j	Junction voltage
V_L	Voltage of the p^+n junction in a PiN diode
V_{out}	Converter output phase voltage
V_R	Voltage of the nn^+ junction in a PiN diode
V_{RRM}	Reverse repetitive maximum voltage
v_T	IGBT collector-emitter voltage
w_B	Width of the lightly doped, middle region in a PiN diode (base)
w_{SCR}	Width of the space charge region
ϵ_0	Vacuum permittivity (8.854×10^{-12} F/m)
ϵ_r	Relative permittivity
μ_n	Electron mobility
μ_p	Hole mobility
φ	Phase angle between the fundamental components of voltage and current
τ_H	Carrier lifetime at high-level injection
ϑ	Temperature
ϑ_h	Heat sink temperature
ϑ_j	Junction temperature
$\vartheta_{j,max}$	Maximum junction temperature
ξ	Damping factor in *RLC* circuit

ACRONYMS

3L three level

AMB active metal brazing

BJT bipolar junction transistor

BPD basal plane dislocation

DBC direct bonded copper

EMI electromagnetic interference

ESL equivalent series inductance

ESR equivalent series resistance

FEM finite element method

GDU gate drive unit

IEGT injection-enhanced gate transistor

IGBT insulated-gate bipolar transistor

IGBT3 third generation IGBT

IGCT integrated gate-commutated thyristor

JBS junction barrier Schottky

JFET junction gate field-effect transistor

JTE junction termination extension

MOSFET metal-oxide-semiconductor field-effect transistor

MPC model predictive control

MPD micropipe density

NP neutral point

NPC neutral point clamped

NPT non punch through

NTC negative temperature coefficient

OP operating point

PCB printed circuit board

PEBB power electronics building block

PEEC partial element equivalent circuit

PP press-pack

PT punch through

PWM pulse width modulation

RRSOA reverse recovery safe operating area

SB Schottky barrier

SF stacking fault

SiCGT SiC commutated gate turn-off thyristor

SOA safe operating area

SSPS solid state power substation

TED threading edge dislocation

TSD threading screw dislocation

VSC voltage-source converter

WTHD weighted total harmonic distortion

ABSTRACT

This work presents a 6.5-kV 1-kA SiC bipolar diode module for megawatt-range medium voltage converters. The study comprises a review of SiC devices and bipolar diodes, a description of the die and module technology, device characterization and modelling and benchmark of the device at converter level. The effects of current change rate, temperature variation, and different insulated-gate bipolar transistor (IGBT) modules for the switching cell, as well as parasitic oscillations are discussed. A comparison of the results with a commercial Si diode (6.5 kV and 1.2 kA) is included. The benchmark consists of an estimation of maximum converter output power, maximum switching frequency, losses and efficiency in a three level (3L) neutral point clamped (NPC) voltage-source converter (VSC) operating with SiC and Si diodes. The use of a model predictive control (MPC) algorithm to achieve higher efficiency levels is also discussed. The analysed diode module exhibits a very good performance regarding switching loss reduction, which allows an increase of at least 10% in the output power of a 6-MVA converter. Alternatively, the switching frequency can be increased by 41%.

1 INTRODUCTION

Medium-voltage, adjustable-speed drives are essential for industry (e.g. oil and gas, chemistry, metals, marine, mining, etc.), traction and energy systems. The majority of them are based on a voltage-source self-commutated converter. Compared to load-commutated converters, they combine a high energy conversion efficiency and a highly dynamic control of the energy flow. Furthermore, compliance with grid standards is simplified. The rising energy costs have led to higher efficiency requirements in industrial processes, triggering a steady improvement of the medium-voltage converter technologies.

In the megawatt-range, the efficiency of the converter is higher than 96% [1]. The heat generated by the power semiconductors is the main source of losses in the converter. These losses also determine the maximum output power of the converter, as the junction temperature of the power devices cannot exceed the maximum temperature specified by the manufacturer (125...175 °C). Over time, the progress in power semiconductor device technologies has allowed the development of new converter topologies that take advantage of the properties of the new devices. Improvements in the power rating and density, efficiency levels, reliability, cost and performance of medium-voltage converters in the last decades are a consequence of this.

Power semiconductors have experienced a fast development towards higher blocking voltages and current ratings, more reliable packages and extended safe operating area (SOA) during the last years. The type of power semiconductor devices strongly depends on the converter voltage and current rating, as well as the specific application requirements. Today three different device types are applied in medium-voltage converters: IGBTs, integrated gate-commutated thyristors (IGCTs) and thyristors. IGBTs clearly dominate in converters with a power rating of S_C = 300 kVA...3 MVA. At very high power ratings (e.g. $S_C \geq 30$ MVA) load or grid commutated converters with thyristors are commonly applied. In the range of S_C = 3 MVA...30 MVA, IGBTs and IGCTs compete with thyristors. [1, 2]

But not only the switches are important in a converter: The power diodes can be as influential as the power switches in the performance of a converter. In self-commutated VSCs they are used in antiparallel connection to the switches to provide a freewheeling path for the current. In some multilevel VSC topologies, such as the NPC, also single diodes are required. Due to the high current and voltage change rates experienced during each commutation, these diodes need to be specially designed for this type of application (fast-recovery diodes). One of the major drawbacks of current Si-based diodes is their reverse recovery behaviour: The higher the voltage rating of a diode, the higher the commutation losses during turn-off. These losses also affect the switch involved in the commutation and increase for faster current change rates (*di/dt*). Since the maximum *di/dt* is determined by the diode, the switching speed of the switches is also restricted. Although 6.5-kV diodes for medium voltage converters have been developed, their performance is still not as good as the one achieved with two series-connected

3.3-kV devices [2]. However, a series connection requires extra passive components for static and dynamic voltage sharing.

Because of the problems experienced by fast high voltage diodes mentioned above, there are efforts to develop new diode technologies that have a better performance in medium-voltage converters. Among them, the use of new wide band gap materials, such as SiC, seems to be a promising alternative. SiC allows the fabrication of thinner diodes with improved voltage blocking characteristics and a very low base charge. Hence, the reverse recovery behaviour does not limit the switching speed and voltage ratings as high as 20 kV can be achieved without the need of a series connection [3].

The work presented here comprises the characterization and evaluation of a newly developed SiC PiN diode module, with a rating of 6.5 kV and 1 kA. For this purpose, the thesis is divided in three main chapters. The first part of Chapter 2 covers the state of the art of SiC devices. The different structures available nowadays are reviewed. The work of other research groups focused on SiC power devices for medium-voltage, high-power converters is presented. This part is completed with a brief summary of the main hurdles from the material point view to develop reliable PiN diodes. The second half of Chapter 2 focuses on medium-voltage power diodes and their properties. This section should give the reader all the basic information needed to understand the way a PiN diode operates. Also information regarding module packaging is included.

Chapter 3 presents the electrical characterization of the diode module prototype. It consists of the electrical characterization of the diode's static and dynamic behaviour, including a comparison to an equivalent Si diode and a study of the oscillations caused by the fast switching transient. With this data, an electrothermal model of the diode is elaborated.

In Chapter 4 the model of the diode module is used to evaluate the advantages of the inclusion of SiC diode technology in a medium-voltage, high-power converter. For this purpose, a simulation of the diode in a 3L-NPC VSC is carried out and its benefits and drawbacks are discussed. With the converter simulation it is possible to determine the increase of the output power or switching frequency that is achieved in a converter equipped with SiC diodes. Calculations regarding converter efficiency are also included. Furthermore, the use of a MPC algorithm to reduce the losses in the semiconductor devices was also investigated. For this purpose, the algorithm takes into account the reduced switching losses associated with the commutations that involve a SiC diode. The conclusions of this work can be found in Chapter 5.

During the time this investigation took place, several papers were published in international conferences and journals [4–8]. The contents of Chapters 3 and 4 are based on the published work.

2 STATE OF THE ART OF SIC DEVICES AND MEDIUM-VOLTAGE DIODES

2.1 SILICON CARBIDE DIODES AND MEDIUM-VOLTAGE MODULES

There has been an ongoing interest in mastering wide band gap materials for the application in power semiconductors. Devices made of wide band gap materials have a better performance at high temperatures and can block higher voltages than traditional Si-based devices. Out of the possible materials for power devices, SiC, in its polytype 4H, and recently GaN reached a commercial status. Some of their key parameters are listed in Tab. 2.1. The band gap of SiC and GaN is about three times that of Si, positioning these materials closer to the insulator category. Due to the stronger chemical bonds, as reflected by the higher E_g value, the electric field required for entering the avalanche mode, namely the critical field strength E_C, is one order of magnitude higher in SiC and GaN. This has a direct impact on the breakdown voltage V_B, as both are related by [9]:

$$V_B = \frac{1}{2} w_{SCR} E_C \tag{2.1}$$

where w_{SCR} represents the width of the space charge (depletion) region. This means that for an equal breakdown voltage, SiC or GaN devices can be 10 times thinner than Si. The width of the depletion region w_{SCR} is directly related to the doping density N_D of the semiconductor, as described by the following equation for an n-doped semiconductor [9]:

$$N_D = \frac{\epsilon_0 \epsilon_r E_C}{q w_{SCR}} \tag{2.2}$$

where q stands for the elemental charge, ϵ_0 and ϵ_r for the vacuum and relative permittivity, respectively. Considering the values provided in Tab. 2.1, a 10 times higher E_C combined with a 10 times lower w_{SCR} allows doping densities 100 times larger than in Si for devices with equal V_B values.

The material properties of Si have lead to commercial devices limited by a maximum reverse voltage of 6.5 kV and junction temperatures below 200 °C. Due to charge dynamics, the switching performance of these high voltage devices is limited (high switching losses). To overcome these limitations, the development of devices based on wide band gap materials has been the aim of many research and development efforts in the last two decades. In spite of that, commercial devices nowadays are mostly offered for the low-power range, with maximum ratings of around 60 A for 1.2-kV discrete devices. Modules with larger current capability are also available, but a considerably higher cost. There are still many technological hurdles particular to SiC that need to be overcome before all the advantages of this material can be translated

Table 2.1: Selected material properties of Si, 4H-SiC and GaN [9, 10]

	Si	4H-SiC	GaN
Band gap E_g (eV)	1.170	3.263	3.47
Intrinsic carrier con. n_i at 300 K (cm^{-3})	1.4×10^{10} [11]	6.7×10^{-11} [11]	2.25×10^{-10} [12]
Critical field E_C (MV/cm)	0.23	2.2	3.3
Permittivity ϵ_r	11.8	9.7	9.0

into functional devices [13–15]. SiC devices, in order to have a strong market presence, need to offer an attractive alternative to Si devices, which now profit from a widespread use, mature technology and very low prices.

Material defects and manufacturing problems are also an important issue, because they limit the yield and maximum die size. Restrictions like these, higher material costs, and the capability of SiC devices to operate at a high current density without thermal problems, lead to devices operating at a higher power density than common Si device. As a consequence, there are several reliability issues that become critical for long term operation. The higher thermal conductivity of SiC is usually referred as an advantage for operation at higher current densities, because it would theoretically allow a better heat conduction. However, this characteristic is not a critical factor in high current operation. Only 3% of the overall thermal resistance from the junction to the heat sink is dependent on the material used in the die [14]. For this reason, packaging technology plays a crucial role in enabling wide band gap technologies such as SiC to become a real alternative [16]. The higher current and voltage change rates during the switching instances of the devices have been reported as the source of electromagnetic interference (EMI), as most of the newly developed devices generate high frequency oscillations [17–22]. This is an issue that demands a careful design of the semiconductor devices, their housing, the gate drive loop and the current commutation loop.

The progress in the commercialization of SiC devices has been relatively slow. However, there are many technologies and manufacturers currently in the market. An overview of some of the available discrete devices as of the first half of 2015 can be seen in Fig. 2.1. A clear focus on the 1200-V class and a variety of structures for active switches can be observed. These are divided into metal-oxide-semiconductor field-effect transistor (MOSFET), junction gate field-effect transistor (JFET) and bipolar junction transistor (BJT). As for the diodes, Schottky barrier (SB) diodes are a mature alternative among SiC devices and at this voltage level superior than the PiN diode type. These were the first devices to be commercialized one decade ago and have found a market niche in high switching frequency, high efficiency applications. Despite all the technological and economical hurdles that still need to be overcome, there are studies that predict a 15-fold increase in the global SiC power market, from about USD $200{\times}10^6$ in 2013 to $3{\times}10^9$ in 2020, which would equal 9% of the total market of power switching devices [15]. This development implies that the high prices of current devices will eventually drop.

2.1.1 DIODES

SiC power diodes are divided into three different structures: SB, junction barrier Schottky (JBS) and PiN, as depicted in Fig. 2.2. Out of these three diode types, the first one to be commercially available was the SB [23], which in Si devices is known for its good performance in high frequency applications, usually related to switch-mode power supplies. Schottky rectifiers rely on the non-linear contact between semiconductor and metal to achieve unidirectional current flow. Si devices using this technology are limited to blocking voltages of around 150 V, because at higher voltage levels the resistance of the drift region becomes too high, increasing the conduction losses to intolerable levels. With SiC it is possible to design devices with a thinner

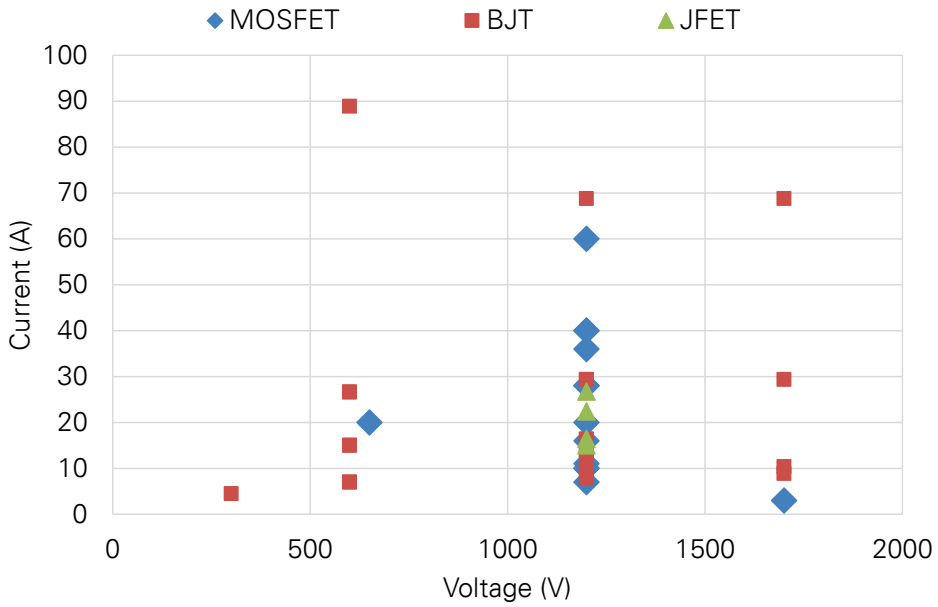


Figure 2.1: Selection of discrete SiC-based switches available as of the first half of 2015 for voltages up to 1700 V. The current rating represents the continuous current for a case temperature of 100 °C.

drift region for the same breakdown voltage, thus, allowing a 400 times smaller resistance for the same breakdown voltage or a 20 times higher breakdown voltage for the same resistance value [24, 25].

In forward bias mode, the electrons flow from the cathode to the anode; the on-state voltage drop depends on the resistance of the drift region and of the metal-semiconductor interface. For normal operation conditions, the current depends on majority carriers. This allows the device to go into reverse bias mode quickly, as no minority carriers need to be evacuated from the drift region. Thus, switching losses are minimum and the device can operate at high switching frequencies. The absence of stored charge can be appreciated in Fig. 2.3, where the current of the turn-off transient for a 3.3-kV SB diode is plotted and compared with the other SiC rectifiers types at a junction temperature ϑ_j of 25 and 300 °C.

Since Schottky diodes with voltage ratings above 200 V with low on-state resistance values are possible with SiC, new fields of applications are open to them. Some advantages of 1200-V devices are [27]:

- Low turn-off losses: reverse recovery current almost absent
- Electrical characteristics with a low temperature dependency
- Lower on-state losses than Si PiN diodes
- Lower leakage currents than comparable fast recovery Si PiN diodes

In the first development phase of SiC SB diodes, one of the main drawbacks encountered were the high levels of leakage currents observed, higher than the model predictions. An electric field crowding at the contact peripheries was identified as the main cause for an increased leakage current at the contact edge, which eventually leads to a premature device failure [26]. A proposed solution to this was the use of sophisticated contact termination techniques, such as

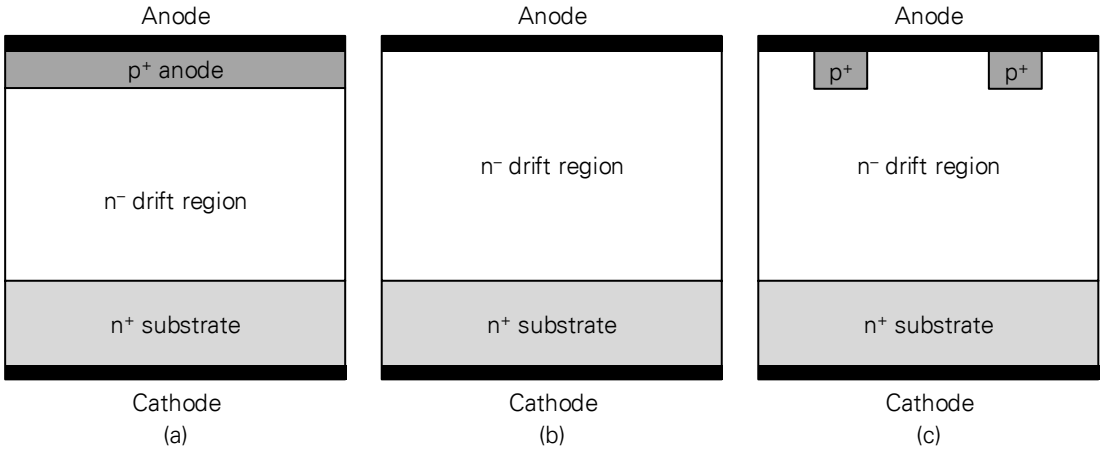


Figure 2.2: Cross-section of three SiC diode structures: (a) PiN, (b) SB and (c) JBS.

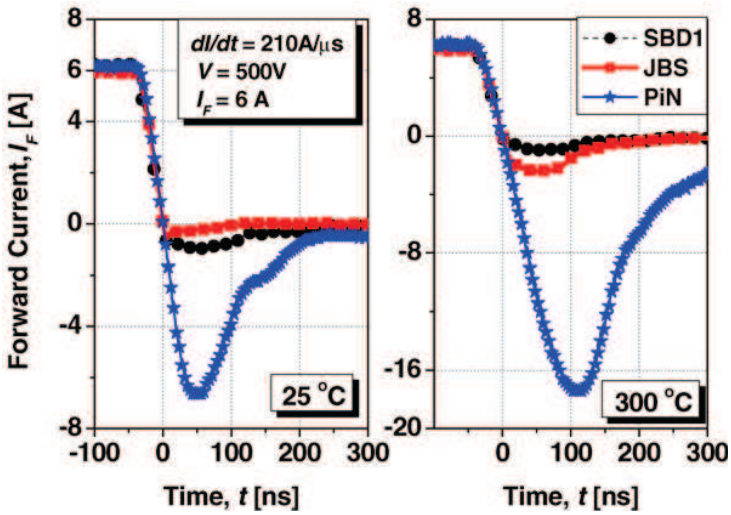


Figure 2.3: Comparison between the turn-off current waveforms for SB, JBS and PiN 3.3-kV diodes, ϑ_j = 25 and 300 °C. [26] © *IOP Publishing. Reproduced with permission. All rights reserved.*

junction termination extensions (JTEs). Using this principle, a 4H-SiC diode with a breakdown voltage of 10.8 kV could be demonstrated [28].

High temperature operation of SiC SB diodes is also of interest, especially for applications in harsh environments, e.g. aerospace and space missions, as in [29], where a 300-V, 5-A diode with a temperature operation range between −170 and 300 °C was presented. Nowadays, a commercial high temperature device family is available, with maximum ratings of 1200 V, 10 A and a maximum junction temperature of 250 °C [30].

JBS diodes are basically Schottky diodes with an n^- drift layer that incorporates p^+ *floating islands*, see Fig. 2.2. This structure was known from low-voltage Si Schottky devices, where it was used to reduce the leakage current through shielding of the Schottky interface. Besides that, in the case of SiC diodes, it offers a bipolar conduction path in the case of surge current conditions. This path is activated as soon as the threshold voltage of the pn junction is reached, thus, increasing the surge current capability of the device. For nominal currents, the diode behaves as an SB diode. It has also been found that this structure leads to an homogeneous avalanche breakdown throughout the active area of the chip, which means that the diode is able to withstand larger currents at breakdown condition without failing [31]. This type of technology

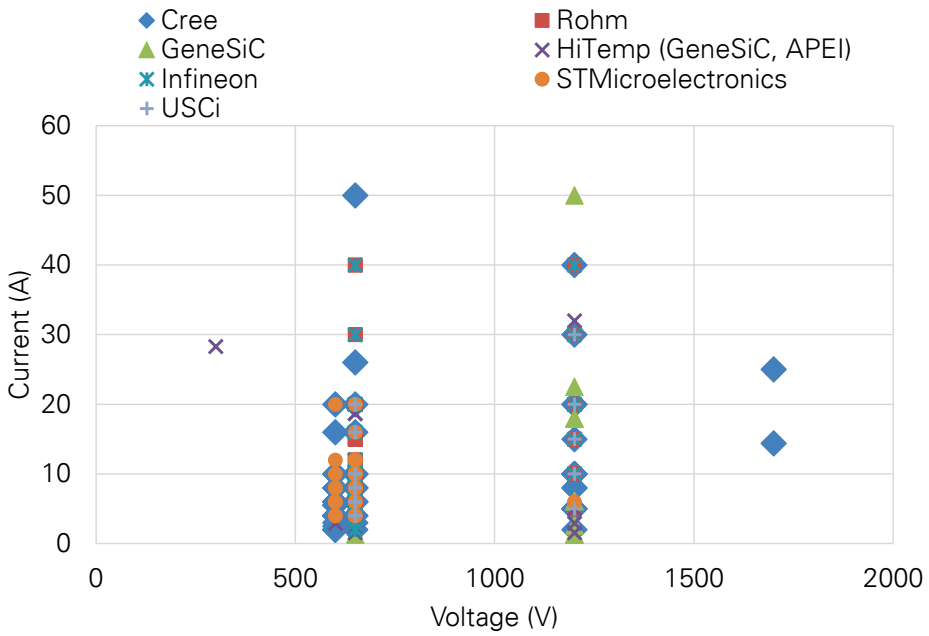


Figure 2.4: Selection of discrete SiC diode devices available as of the first half of 2015 for voltages of 300…2 kV. The current rating represents the continuous current for a case temperature of 130±15 °C. $\vartheta_{j,max}$ = 150…175 °C (normal), 225…250 °C (HiTemp).

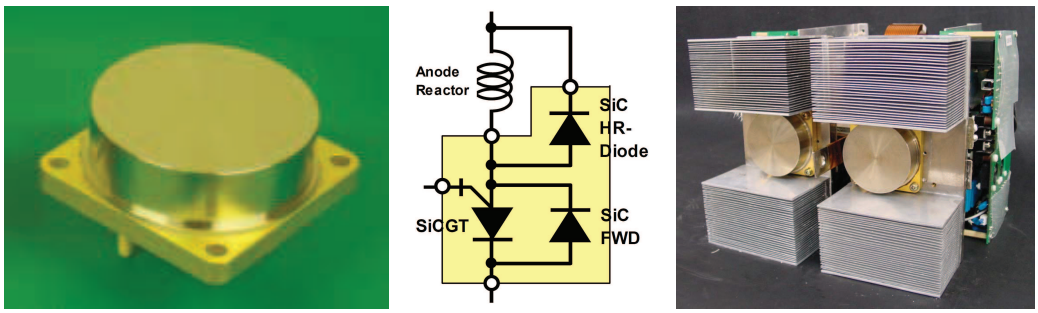
is being applied by two major SiC Schottky diodes manufacturers: Infineon and Cree [31, 32]. The latter has even demonstrated a JBS device with a breakdown voltage of 10 kV [33].

PiN diodes, due to their vulnerability to SiC material defects have not been developed to a commercial level, see Sec. 2.1.3. A detailed explanation of the working principle of this diode structure can be found in Sec. 2.2.1. This structure is only competitive for breakdown voltages over 2–3 kV [3], as there is a relatively high knee voltage associated with SiC (≈ 3 V). For breakdown voltages over 10 kV, they offer the best trade-off between on-state voltage drop, switching losses and high-temperature performance [34]. At chip level, diodes with very high voltages ranging from 10 to 26.9 kV have been reported [34–39]. These show that JTE structures are critical for the design of devices with very high breakdown voltages.

The development of PiN diode modules for voltages ranging from 4.5 to 6.5 kV has also been reported [40–43]. In these cases, the aim is to develop high power modules with current ratings ranging from a few hundred amps up to more than 1 kA. Since the main subject of this dissertation is the analysis of such a module, a section has been dedicated to review some of the power modules based on this technology, see Sec. 2.1.2.

Figure 2.4 shows most of the commercial SiC Schottky diodes available by the first half of 2015. The devices are offered for voltages of 600/650 V and 1200 V. Some of them achieve a high current rating through the paralleling of two dies, but the majority are single-die diodes. Schottky diodes can be either of the SB type, or in some cases of the JBS type, the manufacturers' catalogues do not make a clear distinction between both of them. All diodes have a maximum junction temperature of 150…175 °C, which is limited by standard packaging technology, e.g. TO-247. GeneSiC and APEI also have a high temperature family of Schottky diodes which allow a maximum case temperature of 225…250 °C by using advanced packaging technologies.

SiC Schottky diodes have also found acceptance as antiparallel diodes in All-SiC and Si/SiC hybrid modules. They are combined with Si IGBT switches, such as the QID12100 family from Powerex, or the GB100XCP12-227 from GeneSiC [44], both with ratings of 1200 V and 100 A.



(a) (b) (c)

Figure 2.5: 4.5-kV power module developed by Kansai Electric: (a) packaged SICGT module (Ø 56 mm) [52] © *2012 IEEE*, (b) equivalent circuit of the module [52] © *2012 IEEE*, (c) one phase leg of the 100 kVA converter [51] © *2009 IEEE*.

The FF600R12IS4F module from Infineon, also for the 1200-V class, is offered with a higher nominal current of 600 A. The maximum operating temperatures of these devices are limited by the high temperature performance of the Si IGBT, which can operate at junction temperatures up to 150...175 °C, depending on the manufacturer. Still on a prototype level, modules for higher voltages have been presented. For example, in [45], a hybrid module targeting traction applications equipped with 3-kV, 200-A Si IGBTs and JBS diodes. Takao *et al.* introduced in [46] a hybrid 4.5-kV module based on IGBTs and SiC PiN diodes, refer to Sec. 2.1.2 for details. The main advantage of this type of modules is the reduction of the switching losses in both the diode and the IGBT, which allows the design of converters working at higher switching frequencies.

2.1.2 MEDIUM-VOLTAGE HIGH-POWER MODULES

The inclusion of SiC devices in medium-voltage converters, where usually power modules with voltage ratings of at least 3.3 kV and a current capability of a few hundred up to a couple of thousands amps are used, is an important development towards higher efficiency and higher power density [47]. However, no commercial devices are available so far and only a few modules with the required voltage and current ratings have been reported by research groups. This section is focused on the published work presented by a selection of four groups, whose work is in a comparable level to the diode module analysed in this dissertation.

KANSAI ELECTRIC POWER COMPANY (JAPAN)

This research group has published many papers regarding the development of a SiC commutated gate turn-off thyristor (SiCGT)-based power module. They have developed so far:

- 5-kV SiC PiN diode die [48]
- 12-kV SiCGT die [49]
- 4.5-kV PiN diode module [50]
- 4.5-kV SiCGT + PiN diode module [51, 52]
- 3-phase, 900-V, 100-kVA converter with 300 kVA overload capability [51, 52]

The SiC PiN diode die [48] is made out of a 4H-SiC substrate, with dimensions of 8×8 mm^2 and a blocking voltage of 5 kV. The results published in [48] focus on the forward voltage recovery. Regarding the SiCGT die, information about the development of early dies can be found in [49]. The current die size used for the SiC modules is 10×10 mm^2 with a blocking voltage of 5 kV.

Using the 5-kV diode dies, two diode modules were built and presented in [50]. The first one consists of a ceramic flat package rated at 4 kV, 1200 A containing 9 dies, with on-state voltages between 4.2 V at room temperature and 3.7 V at 300 °C (1000 A). In the second module a resin-mold package rated at 4 kV and 1000 A was used. For this one, due to improved thermal properties, only 5 dies were required to achieve the 1000 A current rating. The module dimensions are 62×62×35 mm^3. It exhibits a low leakage current, 200 µA at 300 °C, and on-state voltages between 4.5 V at room temperature and 4.2 V at 300 °C (1000 A). In the turn-off commutation included in [50], a current snap-off is present. The corresponding very high *di/dt* causes voltage spikes which can even lead to device destruction. This is a critical issue for the device application. After this paper, the modules where not further developed and the focus of module development shifted to smaller modules with a SiCGT and an antiparallel diode.

The 4.5-kV SiCGT and PiN diode module are presented in [51, 52]. This module contains one SiCGT chip, one SiC PiN diode for freewheeling purposes and a highly resistive diode for the SiCGT snubber circuit, it has a diameter of 56 mm, see Fig. 2.5 (a) and (b). The results shown prove that no degradation effect in the forward characteristic is present in the semiconductors. The packaging technology allows operation at high temperatures capable of withstanding 400 °C for 3 s. The snappiness problem of the diodes previously reported is still present, but the *di/dt* chosen is lower, which helps keeping the voltage spikes under control. With the SiCGT modules a 100-kVA converter with 300-kVA overload capability was built, see [51, 52]. The full converter has dimensions of 110×48×55 cm^3, which amount to a reduction by about 87 % when compared to an equivalent Si converter, see Fig. 2.5c for one phase leg. It is operated at a dc-link voltage of 2 kV, and includes a capacitance of 500 µF. A successful continuous operation of 1000 h was demonstrated [52].

SiC bipolar devices suffer from degradation problems, as it is explained for the case of diodes in Sec. 2.1.3. The SiCGT is not exempt of this problem, as reported in [53]. Stacking faults that are present in the epitaxial layer cause unwanted carrier recombination at the pn junction, reducing the carrier injection from the anode to the gate. This affects the minimum gate current required to turn-on the device, which can experience a 10-fold increase after a few hours of dc current stress. Degradation of the forward voltage of the PiN SiCGT is also a problem and it is stronger in the devices with a high minimum gate trigger current degradation.

TOSHIBA (JAPAN)

Toshiba has focused on the development of SiC PiN diodes to be used with a 4.5-kV injection-enhanced gate transistor (IEGT) previously developed. The research includes diode dies, modules and converter design. Details about the PiN diode developed for this purpose can be found in [41]. The last version reported [46] is based on a 4H-SiC 4°-off substrate. The diodes are designed for a blocking voltage of 4.5 kV. Each die has a current capability of around 25 A, the die size is 5.2×5.2 mm^2 with an anode area of 4×4 mm^2, 50 % smaller than the Kansai diodes. The on-state voltage at 100 A is 4.08 V at room temperature and 3.99 at 125 °C. The SiC PiN diodes are also affected by forward voltage degradation, as reported in [54], refer to Sec. 2.1.3 for more details.

The 4.5-kV, 400-A power module contains two 200-A hybrid pair subunits connected in parallel, each with 4 IEGT and 8 SiC PiN diode dies, see Fig. 2.6a [46]. Instead of the conventional solution for high-power modules, consisting of an AlN direct bonded copper (DBC) substrate attached to an Al/SiC base plate, see Sec. 2.2.2, a SiN active metal brazing (AMB) substrate with a copper base plate was used for the prototype. The copper heat sink, as the cross-section in Fig. 2.6b indicates, is not a regular one. It features direct water cooling integrated into the copper base plate. To enhance the heat removal capability, the base plate includes pin fins, which are submerged into the water flow channels. With this technology, the maximum power dissipation in the module amounts to 3 kW, considering a water temperature of 40 °C and a maximum junction temperature of 125 °C for the semiconductors. The last results presented

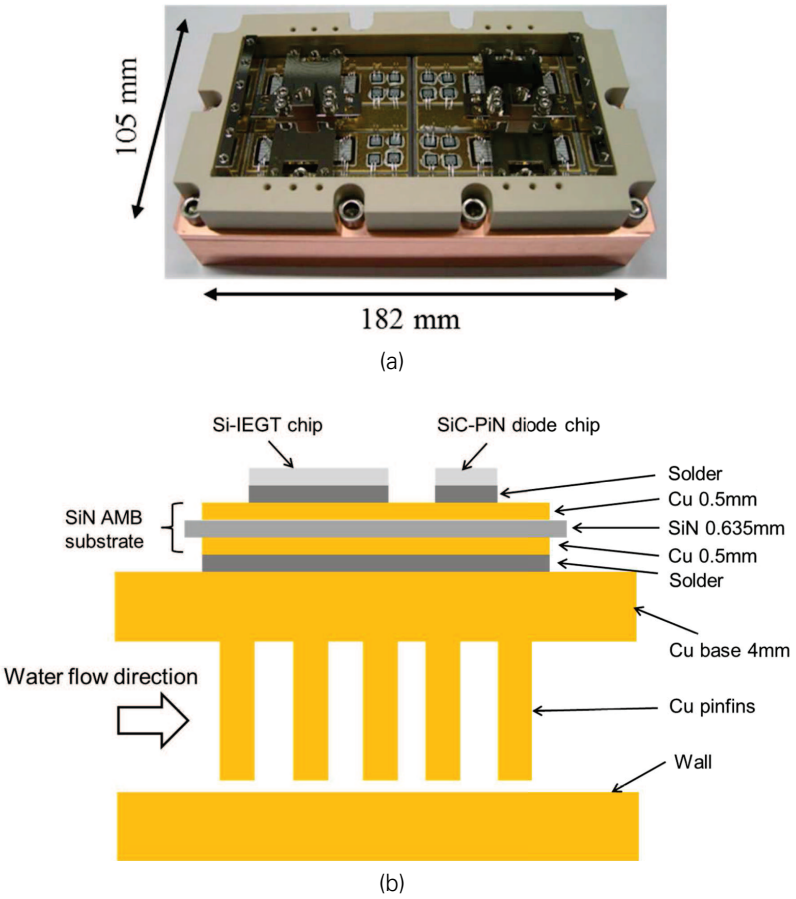


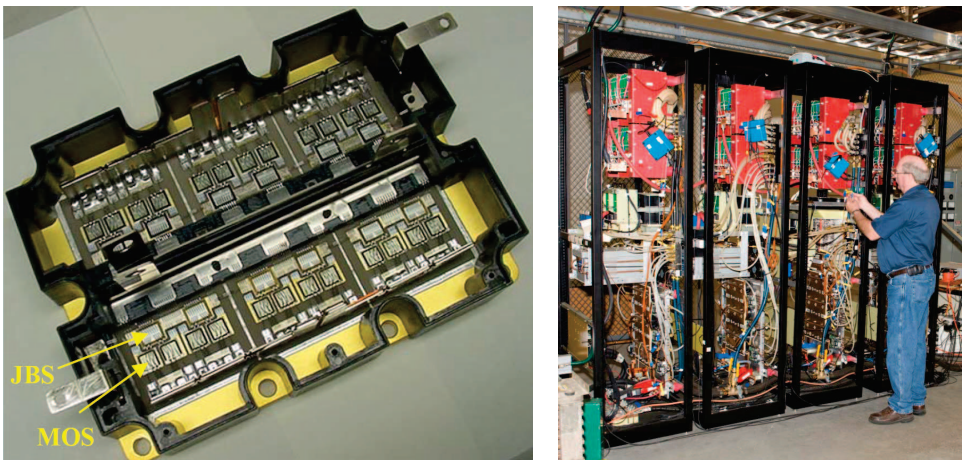
Figure 2.6: 4.5-kV, 400-A Si IEGT, SiC PiN diode power module developed by Toshiba: (a) top view, (b) cross-section. [55] © *2013 IEEE*

include operation of the module in a single-phase 2-level converter working at a dc voltage of 2.5 kV and currents up to 200 A in continuous mode operation at switching frequencies of 5 and 10 kHz [55, 56].

Two converter concepts using these modules were introduced in [57, 58], although no full converter has been presented yet. In [58], a 2-level, 3-phase converter of 1 MVA with a dc-link voltage V_{dc} of 5 kV and an output voltage of 2.8 kV, 210 A is introduced. To achieve this voltage level, each switch consists of two 4.5-kV modules connected in series. Another concept introduced in an earlier paper [57] is a 3-level, 378 kVA water-cooled converter with a dc link voltage of 10 kV and an output of 6.3 kV and 60 A, operated at a switching frequency of 2 kHz. However, this alternative has not been considered in subsequent papers.

CREE, POWEREX, GENERAL ELECTRIC, VIRGINIA TECH (USA)

The power module presented in [59] is an interesting approach to take advantage of the properties of SiC devices at voltage levels that single Si devices cannot reach. It consists of a 10-kV, 120-A, All-SiC half bridge power module. To achieve these ratings, 12 MOSFET and 6 JBS diode dies are required per switch. Each MOSFET has an area of 8.1×8.1 mm^2 with a yield of 55%; the JBS diodes exhibit and area of 8.3×10.6 mm^2 with a yield of 65% by the time of publication (2011). The 10-kV, 10-A MOSFETs features a specific on-resistance of 127 mΩ·cm^2. Due to the unipolar nature of both types of devices, they have a positive temperature coefficient, which facilitates the parallel connection inside the module. The losses of this module compared to a series connection of two 6.5-kV IGBTs are considerably lower and should allow an opera-



(a) (b)

Figure 2.7: 10-kV, 120-A half bridge power module developed by Cree, Powerex and GE: (a) top view of the module including SiC MOSFETs and JBS diodes, (b) photo of the 13.8 kV to 465/$\sqrt{3}$ V, 1-MVA solid state power substation. [59] © *2011 IEEE*

tion at switching frequencies up to 20 kHz, whereas the Si configuration cannot operate over 1 kHz [60].

The 10-kV, 120-A module housing is based on the standard 140×190 mm^2 footprint for high-voltage high-power Si IGBTs. For the cooling, standard liquid-cooled heat sinks are considered. To overcome the degradation problem in SiC MOSFETs when the body diode turns on, low voltage Si Schottky diodes are connected in series to the switches, preventing reverse conduction. The structure of the module is based on the traditional AlN DBC substrate; wire bonds are used for the top contacts.

A test at converter level is also included in [59], where a single-phase solid state power substation (SSPS) is equipped with the module prototypes. This converter consists of a 4-stage, ac-ac soft-switched converter that steps the voltage from 13.8 kV to 465/$\sqrt{3}$ V at 20 kHz using a small-sized nano-crystalline transformer. An efficiency of 97% at 855 kVA was achieved with the SiC power module. The concept has been further developed to a 4-kV, 100-A power electronics building block (PEBB), which consists of two 10-kV SiC MOSFET dual power modules connected in an H-bridge configuration. Besides the modules, gate drive units (GDUs), decoupling capacitors and heat sinks are also included in the PEBB. [61]

MITSUBISHI ELECTRIC (JAPAN)

The medium-voltage All-SiC power module with the highest switch power rating is a 3.3-kV, 1.5-kA SiC MOSFET module with SiC SB diodes developed by Mitsubishi Electric [62]. To achieve these ratings 16 MOSFETs and 16 SB diodes were connected in parallel. The conduction losses are comparable to 3.3-kV IGBT modules, but the switching losses are considerably lower. These modules were applied in a traction inverter with a dc-link voltage of 1500 V, where a volume reduction of 65% compared to a standard Si IGBT-based converter was possible [63].

2.1.3 DEFECTS IN SIC BIPOLAR DIODES

Some of the main hurdles for SiC technology have been wafer size, quality and costs. In the beginning of the '90s, the main concern was focused on micropipe density (MPD). 4H-SiC wafers, which are the most relevant for SiC power devices, had a diameter of only 25 mm and an MPD > 10^3 cm^{-2} [47]. Micropipes can be described as hollow tubes of about 1 µm

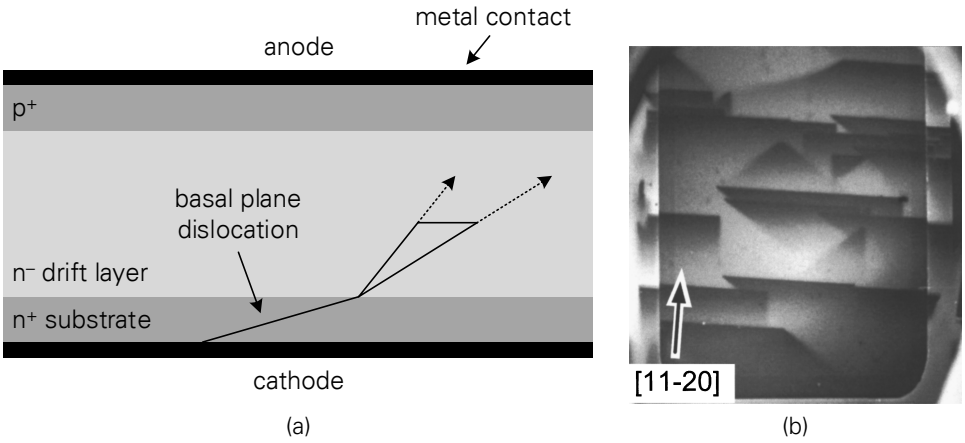


Figure 2.8: (a) Schematic drawing of a basal plane dislocation in a PiN diode [67]. (b) Low-temperature panchromatic cathodoluminescence image of a stressed 4H-SiC diode without the top metallization. The darker rectangle with rounded corners corresponds to the diode chip limits, the dark triangular and rectangular shapes correspond to stacking faults after the device had been stressed with current. *Reproduced with permission of Trans Tech Publications Ltd. from [74] in the format Thesis/Dissertation via Copyright Clearance Center.*

in diameter that originate during the bulk crystal production. The devices with a micropipe in its active area have a considerably lower blocking voltage capability [64]. After two decades substantial improvements in wafer quality and size have been achieved. 100-mm wafers are now standard, with median MPDs below 0.1 cm^{-2} [65].

After micropipes, the next issue to solve in SiC crystals are the basal plane dislocations (BPDs). These defects in the crystalline structure are critical for the development of bipolar devices, such as PiN diodes, as they have a direct influence on the forward voltage drift [64]. The mechanism can be described as follows: BPDs in the SiC substrate propagate through the epitaxial layers during the growth process. Under electrical conduction, these faults expand into triangular shaped stacking faults (SFs) in the buffer and drift layers of the device [66, 67], a process known as *radiation-enhanced dislocation glide* [68]. This phenomenon is schematically depicted in Fig. 2.8. Since SiC devices are made using substrates with 4°or 8°off-axis orientation, these SFs start at the substrate epitaxy interface and grow with the off-axis orientation of the crystal, which means that the higher the inclination of the off-axis, the larger the device area that is covered by the fault. As a consequence, the SFs reduce the minority carrier life time and active area of the device. Both cause a permanent increase of the forward voltage. BPD densities have been reduced from 10^4–10^5 cm^{-2} to 300–400 cm^{-2} in 100-mm wafers [65]. This has been achieved mainly through techniques where the BPDs are converted to threading edge dislocations (TEDs) —whose effect is less severe than BPD— and the reduction of the offcut angle of the SiC wafer from 8° to 4° [66, 69–72]. This angle is needed to assure that the epitaxial layers maintains the polytype of the seed, 4H-SiC in this case. A different approach has been reported in [73], where an on-axis 10-kV PiN diode was developed. This fabrication method could be an alternative to avoid device degradation problems due to BPDs.

As pointed out in [66, 75], forward degradation can be triggered by current densities as low as 1 mA/cm^2, higher densities lead to a larger voltage drift, as more BPD can be converted to SF. Temperature does not influence the voltage change, but accelerates the process of reaching a final state by about 5 to 8 times per 100 K. Besides forward degradation, it has also been reported that BPDs have an influence on leakage current levels [71]. However, it has been pointed out by Ota *et al.* [54] that even diodes made of BPD-free substrates showed degradation, which suggests an additional mechanism that triggers degradation in bipolar devices. An initial

analysis indicates that this could be caused by Shockley SFs and combined etch-pits arrays.

There are other defects besides micropipes and BPDs that also limit the yield in SiC wafers. Some attention has been directed to threading screw dislocations (TSDs) and carrot defects, which can be the reason for an increased reverse leakage current. Because this current flows concentrated through the defect area, the device may, over time, fail due to local power dissipation at the defect [33, 65, 71, 76]. Another possible source of failure that has been reported is particulate contamination, which can cause a local concentrated electric field [33]. Since no further improvement in reducing the density of TSDs and TEDs, commercial devices contain many of these non-micropipe defects. The consequences these defects might have in the device performance have not been documented yet, but they might have an impact on wafer yield, reduced voltage and current ratings, and reliability issues, which are not as easy to detect e.g. as a lower breakdown voltage [15]. As the SiC device quality improves, more efforts will be dedicated to investigate this area.

2.1.4 SUMMARY

This section summarized the development stage of SiC devices at commercial as well as at research level. SiC material has clear advantages over Si. However, there are many issues that need to be addressed before the devices reach a maturity level comparable to the one of Si-based devices. Two decades of intensive R&D efforts have lead to a first generation of commercial devices. Available devices comprise voltage classes up to 1700 V and current ratings up to 54 A (1200 V), which is still low compared to the palette of Si devices, which reaches up to voltage ratings of 6.5 kV (8 kV for thyristors) and several kiloamperes. Besides the limitation in power handling capability of the new devices, the prices are high —about 10 times higher for a 1200-V, 40-A switch— and the packaging used limits the maximum junction temperature the device can be operated at.

The lack of devices with higher voltage and current ratings in the market is mainly related to reliability issues. As pointed out in [15], for example, commercially available SiC power diodes, which have been in the market for over one decade, are significantly derated (by a voltage/current factor of 2 or greater) to achieve a high reliability. This leads to devices that do not take full advantage of the SiC material. However, as long as the material defects in SiC are not considerably reduced, this will not be possible. Even though defects such as micropipes and basal plane dislocations have been reduced by several orders of magnitude, there are still many defects present in SiC substrates. The consequences of them are more difficult to observe, as their impact in the device performance is not as evident as e.g. with micropipes, but it is believed that they play an important role in the field-reliability of SiC devices [77].

Notwithstanding that, there are ongoing efforts in improving the quality of SiC substrates, device fabrication and packaging technologies. As an example, 150-mm wafers of 4H-SiC are now commercially available [15], first devices allowing 250 °C junction temperature have also appeared in the market [30, 78]. On research level, many different device structures with attractive characteristics and very high blocking voltages (up to 20 kV) have been reported [3, 79]. The development of power modules is a technologically demanding task, as the electrical and thermal operating conditions of SiC drive the traditional technology developed for Si devices to new levels [16].

2.2 MEDIUM-VOLTAGE POWER DIODES

Medium-voltage power diodes are an essential component of modern VSCs. The diode design is optimized depending on the application, which can be divided in two main groups:

- *Rectifier diodes* are needed in classical diode-bridge rectifier systems, which are used to obtain dc current and voltage out of a three-phase grid. The grid-side rectifiers usually

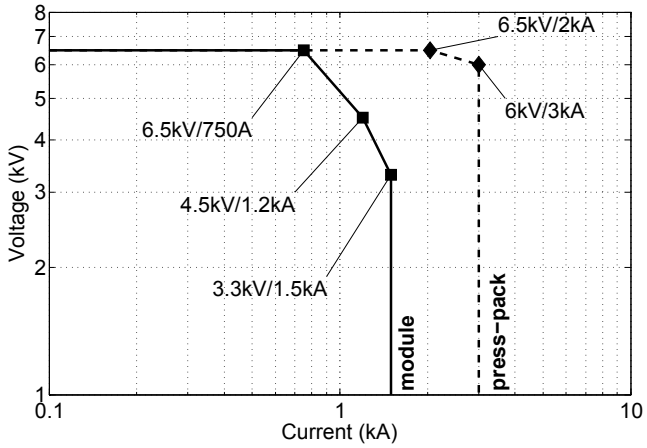


Figure 2.9: Maximum repetitive voltage vs. nominal current rating of commercially available high power diodes for hard switching applications ($V_{RRM} \geq 3$ kV). The diode modules include two independent diodes per module, the dc current rating is based on a single diode.

feed a capacitor bank (dc-link) and are operated at grid frequency (50, 60 Hz). Because of this, they are optimized for low conduction losses.

- *Fast recovery diodes* are used as freewheeling diodes in pulse-width modulated VSCs together with active switching devices, e.g. IGBTs and IGCTs. In this case, the diodes are switched at a higher frequency, which, depending on the application and voltage and current levels, can vary between a few hundreds and a few thousands hertz. For this reason, the reverse recovery behaviour is critical. Since switching and conduction losses cannot be minimized at the same time, a trade-off between them has to be accepted. Moreover, a soft-recovery behaviour is a must in these type of diodes, as a high *di/dt* during the reverse recovery process can cause high overvoltages that endanger the device and its surroundings [80].

Special attention is given in this section to the latter, as the SiC diode characterized and evaluated in this dissertation is a potential replacement for this type of diodes. Currently, commercial Si diodes with blocking voltages up to 6.5 kV can be found in module as well as in press-pack (PP) housing, as shown in Fig. 2.9. For this diagram only diodes for switching applications (*di/dt* $\geq$ 1 kA/µs) with a blocking voltage $\geq$ 3.3 kV were considered. Module packaging is the preferred alternative for traction and other applications where mechanical vibrations are present. In these cases they are used in combination with IGBT modules. PP devices, on the other side, are mainly used in IGCT-based converters and recently, together with PP-IGBTs [2, 81]. A short review of both packaging technologies is included in Sec. 2.2.2.

For voltages over 3 kV, Si PiN diodes are exclusively used. Unipolar devices such as Schottky diodes are not suitable, due to their high leakage current levels. However, as mentioned in Sec. 2.1.1, there are some SiC devices that achieve high blocking voltages of 10 and 15 kV using the hybrid structure known as *JBS rectifier* [32, 82, 83]. In this type of diode, a PN junction is included next to the Schottky metal contact with the purpose of reducing the electric field at the metal-semiconductor contact. This way, the leakage current under reverse bias can successfully be suppressed. The device is still a majority carrier, i.e. unipolar device, which means that it does not have losses related to stored charge during commutation [83, 84], refer to Sec. 2.1.1 for details.

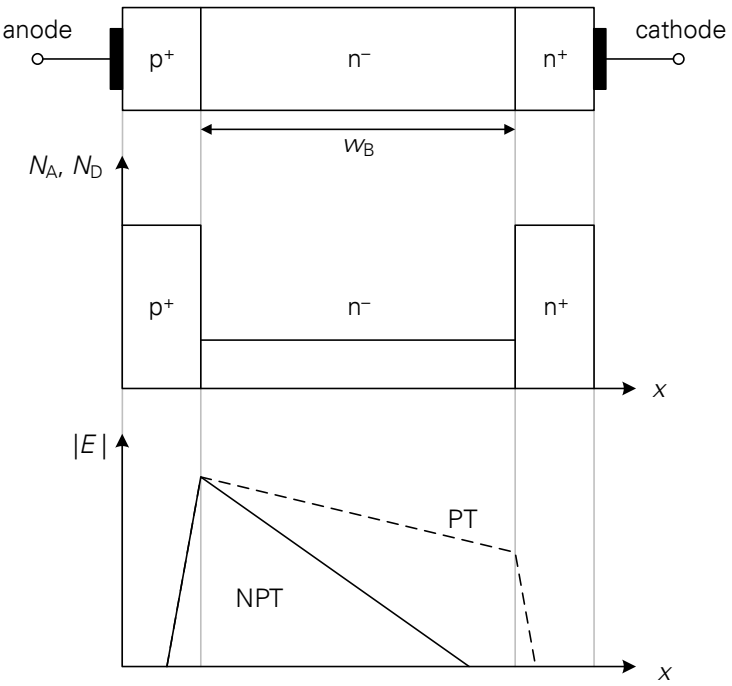


Figure 2.10: PiN diode structure (top), doping profile (middle, logarithmic) and electric field magnitude (bottom) for PT and NPT types.

2.2.1 PIN DIODE PROPERTIES

PiN diodes are used in applications where a large blocking voltage is required. Their structure is based on two highly doped p^+ and n^+ regions with a lightly doped n^- region between them, see Fig. 2.10. The middle, lightly doped n^- region, also known as *drift* or *base* region, is the key for realizing high breakdown voltages, as the blocked voltage principally falls across this part of the diode. During forward bias state, the n^- region is flooded with carriers from the adjacent regions (high injection mode). As a consequence, the doping of this region can stay low, close to the one of an undoped, i.e. *intrinsic*, material. The letter *i* in the *PiN* term stands for this feature.

Because of the high injection of carriers, the resistance of the relatively poor conductive drift region can be reduced. This effect is known as *conductivity modulation*, which allows the semiconductor to mitigate the high conduction losses related to a thick drift region. With PiN technology it is possible to achieve high breakdown voltages with relatively moderate on-state voltages.

A typical current-voltage characteristic of a PiN diode can be appreciated in Fig. 2.11. The diode has two modes, blocking and conduction. During blocking mode, a small reverse leakage current flows through the diode. Usually, it has a relatively low contribution to the total semiconductor losses and can be neglected in the power loss calculations. The reverse repetitive maximum voltage V_{RRM} is the maximum allowable voltage specified by the manufacturer for safe operation. A safety margin separates V_{RRM} from the breakdown voltage V_B. During the conduction mode, the diode forward voltage V_F is determined by the device forward current I_F.

REVERSE BLOCKING MODE

When the PiN diode is reverse biased, a space charge region with a corresponding electric field strength E is formed. If the critical field strength in the depletion layer (material property, related to its band gap) is not exceeded, the device will be able to block that voltage. The gradient of this field strength is directly proportional to the doping concentration. Depending on the width of

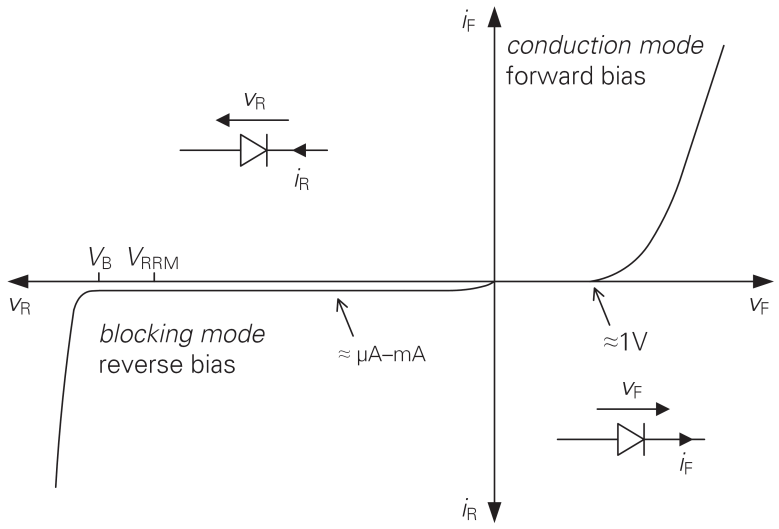


Figure 2.11: PiN diode characteristic, typical values according to Si devices for medium-voltage, high-power applications. Axes for forward and reverse bias have different scales.

the middle region w_B, the electric field distribution can be classified in two types. If w_B is long enough, so that the electric field reaches zero inside the drift layer, the electric field strength has a triangular form; this design is denominated non punch through (NPT). A shorter w_B leads to a trapezoidal electric field, where part of it reaches the n^+ region, which is known as punch through (PT) design. Figure 2.10 depicts these two possibilities. An ideal NPT design will aim for an electric field reaching zero as close to the n^+ region as possible, to avoid unnecessary thickness in the base.

As the electric field strength curves in Fig. 2.10 show, the doping density in the base is lower for the PT case. This is given by the slope of E, as stated in Poisson's equation for an n-doped material [11]:

$$\frac{dE}{dx} = -\frac{d^2V}{dx^2} = \frac{qN_D}{\epsilon_0\epsilon_r}. \tag{2.3}$$

Considering that the reverse voltage V is given by the area below the E curve, for an equal length w_B the maximum reverse voltage is higher in PT diodes. In other terms, for the same voltage, the thickness w_B of the diode is lower than the minimum NPT width; in the case of Si about 30% less [80]. This, in turn, has a direct influence on the forward voltage drop V_F, which increases with the thickness of the base. However, a PT design also has some drawbacks, especially regarding the reverse recovery behaviour, an effect which is discussed at the end of this section, see p. 32.

Temperature dependency of the breakdown voltage is an important aspect of device design. Since the breakdown voltage increases with temperature, it is of interest to study the device behaviour at its lowest specified temperature. The reason for this dependency can be explained by the *avalanche multiplication* effect. This mechanism is responsible for a sudden increase in the device leakage current which eventually leads to the loss of the blocking capability. At high field strengths, the carriers (electrons or holes) gain kinetic energy that can lift a valence electron by impact into the conduction band *(impact ionization)*, creating an electron-hole pair. These process can be repeated by the newly generated carriers, giving place to an avalanche effect, which is responsible for the high leakage current. At high temperatures, the lattice vibration in the semiconductor crystal increase, which raises the probabilities of a collision. This reduces the mean free path. For the particle, this means that a higher field strength is needed in order to gain enough kinetic energy to be able to create a new electron-hole pair. As a consequence, the device critical field strength and breakdown voltage increase. [11]

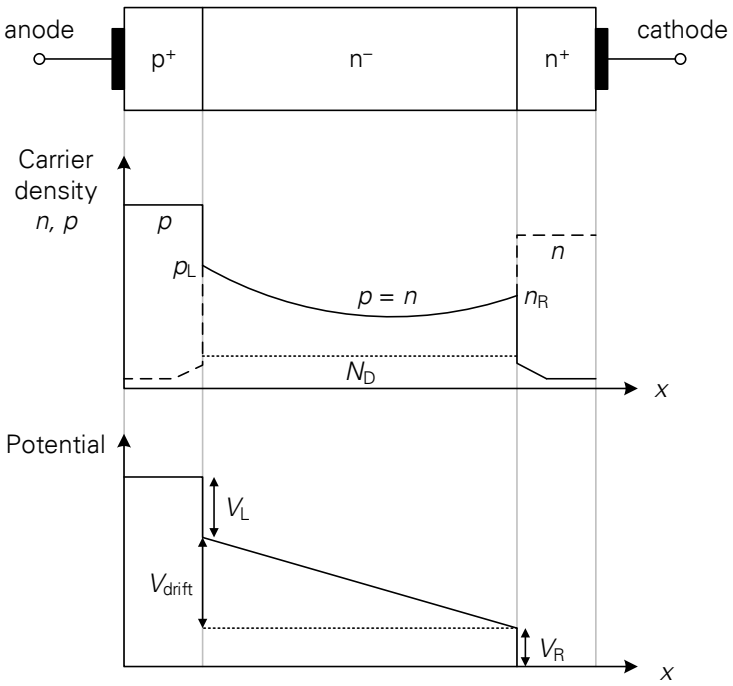


Figure 2.12: PiN diode in conduction mode with simplified carrier density (logarithmic scale) and potential diagrams.

As a reference, for a PT device with a doping density $N_D = 1{\times}10^{14}\,\mathrm{cm}^{-3}$, the breakdown voltages varies around 2.2 V/K. In other words, from room temperature to 125 °C, the breakdown voltage increases by 275 V. Conversely, at −25 °C the blocking capability is reduced by 110 V. In the case of NPT diodes, the influence of temperature is weaker, around 1.3 V/K. [85]

The same principles apply for SiC-based semiconductors. However, the material properties give SiC an advantage over Si regarding reverse blocking capability. Due to the higher band gap, the energy required to move one electron to the conduction band is higher, which is reflected in a higher critical field strength E_C. Leaving aside the dependency on the thickness of the depletion region and the doping density, E_C is $2{\times}10^6$ V/cm in the case of 4H-SiC, whereas for Si it is one order of magnitude lower, namely $2{\times}10^5$ V/cm [10]. Considering an abrupt p^+n-junction as a rough approximation, the breakdown voltage V_B can be expressed as

$$V_B = \frac{\epsilon_0 \epsilon_r {E_C}^2}{2qN_D}, \tag{2.4}$$

ϵ_0 and ϵ_r are the absolute and relative permittivity values and q the elementary charge. The breakdown voltage increases with the square of E_C. The effect of ϵ_r, which is 21% higher in Si, can be neglected. [10]

FORWARD CONDUCTION MODE

As mentioned before, the PiN diode relies on high injection for conduction mode. Basically, this means that the highly doped p^+ and n^- regions inject holes and electrons into the middle region, as shown in Fig. 2.12. Since this carrier injection is several orders of magnitude higher than the doping N_D of this region, the electrons and holes are approximately equal and depend on the adjacent regions. The enhancement of the conductivity through this carrier injection is called *conductivity modulation*.

When a forward voltage V_F is applied to the diode, part of it is used to reduce the built-in voltages at the two junctions, the rest falls across the drift region. Hence, it can be divided in

three components:

$$V_F = V_j + V_{drift} = V_L + V_{drift} + V_R, \tag{2.5}$$

where V_L is the voltage in the p^+n junction and V_R in the nn^+ junction of the PiN diode. V_{drift} represents the voltage of the drift zone. According to [80],

$$V_j = \frac{k_B \vartheta}{q} \ln \frac{p_L n_R}{{n_i}^2}, \tag{2.6}$$

with p_L as the hole density near the p^+n junction and n_R the electron density near the nn^+ junction, see Fig. 2.12. It is important to note that this voltage is independent of the current the diode is conducting and of the doping concentration in the middle zone N_D.

When using SiC as the material for a PiN diode, the junction voltages increase considerably. The carrier concentrations p_L and n_R are not essentially different. The most significant difference lies in the intrinsic carrier concentration n_i. At 300 K, it is in the order of $10^{-11}\,cm^{-3}$, compared to the 10^{10} in Si [11]. This is a direct consequence of the larger band gap of SiC, which leads to a higher V_F in SiC PiN diodes. According to (2.6), for an equal carrier concentration of $1{\times}10^{17}\,cm^{-3}$, V_j changes from 0.82 V (Si) to 3.24 V (SiC). That is one of the main drawbacks for the SiC PiN technology, which is also why other technologies, such as JBS diodes, are also catching some attention for devices over 3 kV [32, 82, 83]. Under that limit, SiC Schottky diodes have a superior performance [47]. Very high voltage bipolar SiC diodes (>10 kV) have also attractive properties and are currently being investigated, as mentioned in Sec. 2.1.1.

The calculation of V_{drift} is not an easy task, as it depends on many different parameters and oversimplified models do not yield accurate results. Grouping the constant terms in the equation for V_{drift} presented in [86] under k_{drift}, which depends on the drift zone length w_B, electron and hole mobilities μ_n, μ_p, carrier lifetime during high injection τ_H and hole and electron recombination currents i_H, i_E,

$$V_{drift} = k_{drift}\sqrt{J_F}, \tag{2.7}$$

where J_F is the current density of the diode in conduction mode and

$$k_{drift} = \frac{{w_B}^2}{(\mu_n + \mu_p)\cdot \tau_H} \cdot \frac{{i_H}^2}{i_E}. \tag{2.8}$$

Replacing (2.7) in (2.5) and solving for J_F,

$$J_F = \left(\frac{V_F - V_j}{k_{drift}} \right)^2. \tag{2.9}$$

This expression is valid for voltages $V_F > V_j$ and is a good approximation for the parabolic forward characteristics observed in fast recovery diodes, like the measured I-V characteristics of the diodes presented in Fig. 3.31, p. 65.

A resulting positive or negative temperature coefficient in the diode's forward characteristic depends on the behaviour of the voltages in the junctions V_j and in the drift zone V_{drift} and their contribution to the total voltage V_F, see (2.5). In the case of the junction voltages V_j, these decrease for higher temperatures, since the term ${n_i}^2$ in (2.6) increases with temperature.

In the case of V_{drift}, it is dependent on the carrier mobilities μ_n, μ_p, which decrease with increasing temperature, and of carrier lifetime τ_H, which increases with increasing temperature. By looking at (2.8), both have opposing effects on the drift voltage V_{drift}. If V_{drift} increases or decreases with temperature will depend on the diode technology used, especially of the role recombination centres play in the design [80]. A usual property of Si power diodes is a negative temperature coefficient for low current densities (V_j predominates) and a positive one for high current densities (V_{drift} predominates), as shown in Fig. 3.31.

At first glance, an negative temperature coefficient (NTC) might seem advantageous, as the conduction losses are reduced when the device heats up and offers a negative feedback that

should help avoiding overheating. This is true for single-chip devices and some of them exhibit this behaviour [87]. In the case of diode modules, however, the diode chips are connected in parallel to reach the desired current rating. If one of the chips inside the module has a higher temperature, this will lead to a higher current, which in turn will increase the losses and heat in the die. Eventually, this could lead to the so called *thermal runaway* effect and to device failure. This does not mean that any device with NTC will experience thermal runaway. If the coefficient is not strong enough, the change in the forward characteristic of each die due to temperature will not lead to failure. Also, each die is thermally coupled through the module base plate, which helps to minimize this effect. In general terms, an NTC < 2 mV/K is usually tolerable for parallel connection [80].

In the case of SiC PiN diodes, most of the samples that have been characterized show an NTC between 0.7 and 3.3 mV/K [34, 35, 40–42, 88]. The reason for this behaviour can be explained by a change in the junction built-in voltages V_j, where the intrinsic carrier concentration n_i is critical, see (2.6) [34, 89]. In these cases, the knee voltage of the forward characteristic is reduced with increasing temperature. The slope (differential on-resistance) remains unchanged or experiences only minor changes, refer to Fig. 3.7 for an example. Another mechanism for NTC that has been reported is the influence of the carrier recombination lifetime during high-level injection, τ_H in (2.8) [35, 90]. As stated in [90], conductivity modulation of the base of the bipolar device determines its on-state resistance, and hence, the forward voltage drop. This resistance is highly dependent on the recombination lifetimes. Some solutions to achieve a positive temperature coefficient have been reported, such as the inclusion of a *patterned ballast resistance* into the anode [91] and Al^+ ion implantation [92].

STORED CHARGE

One of the most well-known advantages of SiC over Si bipolar devices is the very low stored charge, which helps reducing the switching losses. In a PiN diode the stored charge is related to the density of carriers n, p in the base during conduction mode, see Fig. 2.12. Analytically, the charge Q_F can be expressed as [80]

$$Q_F = q \cdot A \cdot w_B \cdot \overline{p}, \tag{2.10}$$

where $\overline{p}$ represents the average hole density in the base and A is the area of the device, assuming equal carrier distribution ($n = p$). This charge needs to be evacuated before the device is able to block, which produces a reverse current in the diode during commutation. This process is called *reverse recovery*. Analogue to this, there is a voltage overshoot during the diode turn-on transient, known as *forward recovery*, discussed after this topic.

Expressing the charge Q_F as a function of the forward voltage V_F,

$$Q_F = \frac{{w_B}^2 I_F}{(V_F - V_j)(\mu_p + \mu_n)}, \tag{2.11}$$

the hyperbolic relation between both variables states that it is not possible to optimize a diode of a given technology to have a low charge Q_F and a low forward voltage V_F at the same time. The base width w_B has to be kept as short as possible, since both Q_F and V_F increase with it. In the case of SiC diodes, the critical field strength E_C is one order of magnitude larger than that of Si, as mentioned before when discussing the reverse blocking mode. As a consequence, the width w_B of the drift region can be much thinner in SiC devices. This does not mean, however, that the forward voltage is lower, because in this case, the junction voltages V_j of the PiN diode are considerably larger than in Si, due to the larger band gap, see (2.6).

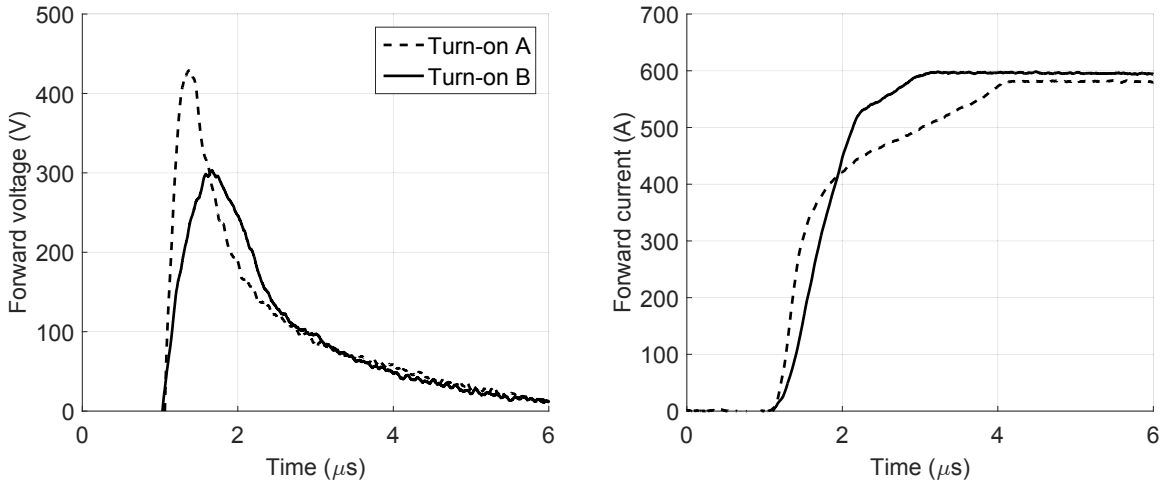


Figure 2.13: Forward recovery behaviour of the 6.5-kV PiN diode DD600S65K1 under two different *di/dt* conditions (V_{dc} = 3.5 kV, I_F = 600 A, ϑ_j = 125 °C).

FORWARD RECOVERY

The *forward recovery* effect occurs when the diode changes from reverse blocking to forward conduction mode. In terms of the device current and voltage, the forward recovery is associated to the overvoltage seen in PiN diodes when they start conducting current, as seen in Fig. 2.13 for a 6.5-kV Si PiN diode switching the same current with two different turn-on current slopes.

As mentioned before, PiN diodes rely on high injection of carriers into the middle region for conduction. The problem in this case is related to the time the base region needs in order to achieve conductivity modulation (steady state). During the turn-on transient, the carriers flood the middle region, but if the current increases at a high rate, some regions of the drift layer might remain without conductivity modulation. Due to its low doping concentration, the resistance will be higher than in steady state, which is the reason for the overvoltage [11]. This is confirmed by the waveforms of Fig. 2.13. The turn-on B has a lower *di/dt*, that gives the diode more time to go into conductivity modulation. In the case of A, the current experiences a higher *di/dt* during the first instants of current conduction, which causes an increase of the overvoltage from 300 to 400 V. The power losses due to forward recovery are usually low and negligible. In the case of the 6.5-kV diode used as an example, they stay under 200 mJ, about 10 times lower than turn-off losses, refer to Sec. 3.5.3 for details. This voltage overshoot has to be kept low also because of the reverse voltage stress of the semiconductor device which might be used together with the diode. For example, IGBTs and IGCTs have restricted reverse voltage blocking capabilities.

REVERSE RECOVERY

As mentioned before, the free carriers that the PiN diode needs during conduction mode for conductivity modulation have to be evacuated from the base before the diode is able to enter the reverse blocking mode. The *reverse recovery* behaviour of a diode describes the way this charge is dynamically removed from the diode. For the output circuit, this carrier removal process is seen as a reverse current in the diode, as exemplified in Fig. 2.14.

For the following qualitative description of this process, the simplified model presented in [11] is used. The carrier concentration in the diode drift region can be approximated by an average value $\overline{p}$, assuming charge neutrality $p = n$. The current-dependent part of the carrier concentration is represented by a higher value p_L next to the p^+n junction ($x = 0$) that decreases linearly to $\overline{p}$, as shown in Fig. 2.15.

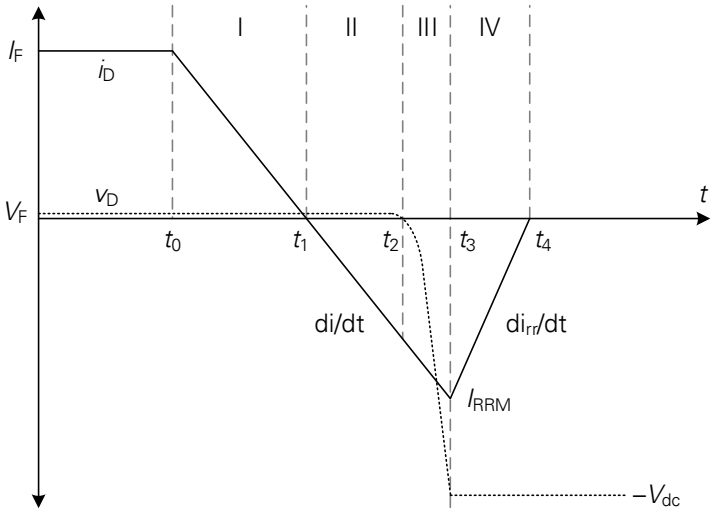


Figure 2.14: Simplified current and voltage waveforms during the diode turn-off transient.

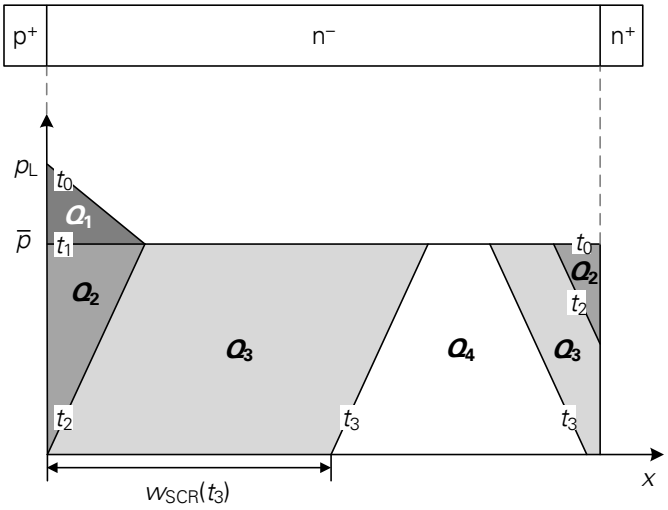


Figure 2.15: Time-dependent charge removal process during the diode turn-off transient.

During the commutation phase I, $t_0 < t < t_1$, the current in the diode changes from the on-state current to zero at a constant rate di/dt; the charge removed during this phase corresponds to Q_1 in Fig. 2.15. In the second phase, $t_1 < t < t_2$, after the device current reaches zero, a reverse currents flows through the diode. The charge that is removed by this current drops the carrier density next to the p^+n junction to zero, which then increases linearly as the separation from the junction increases, until the average density $\overline{p}$ is reached, see Fig. 2.15. For $t > t_2$, a space charge region w_{SCR} next to the p^+n junction starts expanding towards the cathode, which means that the device can support a reverse voltage. As the space charge region expands, the reverse voltage increases until reaching its final value $-V_{dc}$ (phase III). At t_3, the reverse recovery current peak occurs, see Fig. 2.14, and phase IV of the commutation begins. It is in this phase that most of the reverse recovery losses take place, as the diode is blocking the full supply voltage V_{dc} and a reverse recovery current flows simultaneously. As Fig. 2.14 illustrates, during this phase the current decreases towards zero with a slope di_{rr}/dt. The remaining charge in the drift region Q_4 is removed during this phase. The commutation transient is completed when the current reaches zero at t_4.

Special attention needs to be paid to the dynamics of the last commutation phase, which depends on the diode design. If the space charge region w_{SCR} is so wide that the remain-

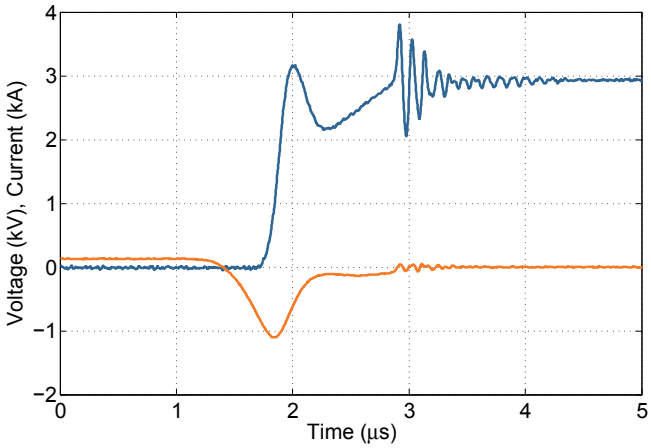


Figure 2.16: Snappiness in a 4.5-kV, 1.7-kA PP diode at 3 kV, 130 A and 125 °C.

ing charge Q_4 is low, it could happen that this charge is evacuated before t_4 is reached. As a consequence, the reverse current *snaps off* and decays with a very high *di/dt* to zero. Even though the losses are lower, the overvoltage caused by the commutation inductance and this *di/dt* could lead to device failure. This phenomenon, as exemplified in Fig. 2.16, is called *snappiness*. Diodes without this problem are referred as *soft recovery* diodes. These diodes are the preferred choice in hard-switching, medium-voltage applications. As a drawback, the lower di_{rr}/dt and the higher charge needed have a negative impact on the switching losses.

The previously discussed PT diode design (p. 27), where the space charge region during blocking mode at the rated voltage expands through the whole n^- region, is not advantageous if a soft recovery is sought. For this purpose, an NPT design is preferred, since the remaining carriers at rated voltage are enough to avoid snappiness. One of the consequences of this design type is a wider drift region w_B and, hence, a higher on-state voltage and reverse recovery charge. More complex structures that achieve a better performance are available under current commercial devices [80, 93]. Alternatively, the development of semiconductor devices and, particularly, diodes based on other materials such as SiC are drawing more attention.

2.2.2 MODULE PACKAGING

Medium-voltage, high-power diodes are available in two types of housing: press-pack and module. The application requirements define which type is needed, although in some cases both types can be applied; the decision is left to the converter manufacturer. Press-pack devices traditionally consist of a semiconductor wafer or, more recently, of paralleled dies in the case of IGBTs, mounted between two metal discs. To establish the electrical connections pressure is applied from both sides of the device. For a uniform pressure distribution molybdenum discs are used as an interface between the metal plate and the semiconductor. These devices are commonly used in applications where a high thermal cycling capability is needed, as no bond wires are required for the electrical connections. The cooling can be applied to both sides of the semiconductor. Some of the drawbacks of this approach are the need of a mechanically stable, vibration-free environment, a well defined pressure during the device operation and non-isolated cooling plates [94]. This section will outline the main characteristics of standard module packaging technology, as this is the packaging form selected for the diode presented in this dissertation.

In module devices the semiconductor chips are soldered on a DBC substrate which goes on top of an isolated base plate, as illustrated in Fig. 2.17 for a standard module. The substrate is made of ceramic material and provides an isolating layer between electrical and thermal

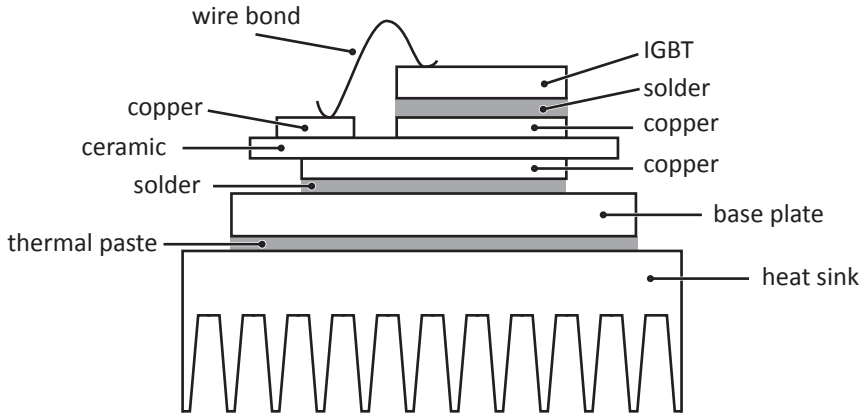


Figure 2.17: Cross section of the mechanical design of a standard module.

connections. Hence, it is possible to attach modules operating at a different potential to the same heat sink. A standard substrate material is Al_2O_3 with a thickness of 0.38 mm. A copper layer of around 0.3 mm is added on both sides of the substrate through the DBC-process: A pre-oxidized copper sheet is placed on the ceramic surface and heated up to a few degrees under the melting point of copper. This high-temperature oxidation process bonds the copper and the substrate oxides together. The mechanical strength of this type of union is high and gives good results at the operating conditions of power modules. After the top and bottom layers have been successfully bonded, the top copper layer is etched to form the tracks with the desired module functionality, in an etching process similar to the one used in printed circuit board (PCB) manufacturing. The next step is to solder the semiconductor dies directly to the top layer, whereas the top terminal of the semiconductor is connected to the desired copper track through bond wires. The bottom part of the DBC substrate is soldered to a base plate, and the power and control terminals are mounted. Once all these steps have been completed, the plastic housing is added and the free space is filled with silicone gel, which acts as an electrical insulator between the connections of the module internal components ($\approx$ 25 kV/mm) and also keeps the device protected from the environment. Finally, the top part is added and the module is sealed, although not hermetically, and the terminals are bent. Even though the gel is an effective barrier against particles such as dust, humidity cannot be kept easily away and can be an important factor in device reliability. [95]

Regarding the semiconductor dies, these are in practice limited to sizes of 20×20 mm^2; high-current capability is achieved by the parallel connection of the dies inside the module. In the case of active switches with antiparallel diode (e.g. IGBT), the area used by the diodes usually corresponds to half of the area dedicated to the active switch. This might limit the device operating capability in applications that use the antiparallel diodes intensively.

Power modules with high current requirements use AlN for the ceramic substrate instead of Al_2O_3, because of its improved thermal conductivity. However, due to the larger difference in the thermal expansion coefficients between AlN and a Cu base plate, the metal-matrix-composite Al/SiC is preferred instead. The expansion coefficient of this compound, made of porous SiC infiltrated with molten aluminium under pressure, can be fine-tuned to match the substrate by regulating the volume ratio of SiC to Al. Through this, a higher thermal cycling capability is achieved at the cost of a higher thermal resistance, as the thermal conductivity of Al/SiC is around 50% higher than Cu. Last but not least, the thermal paste layer between base plate and heat sink plays a major role in determining the thermal capabilities of a power module. This layer is responsible for an important fraction of the total thermal resistance, even though it is specified with a thickness of 40–50 µm. This paste is needed to fill the air gaps between base plate and heat sink. Although its thermal conductivity is better than air, it is 100 times

worse than that of most metal layers. [94, 95]

The description above gives the main characteristics of power module design for devices of at least 3.3 kV. For voltage classes below this level there are several new approaches, such as modules without base plate to reduce the total thermal resistance, use of pressure contacts to avoid thermal expansion issues and intelligent modules with integrated logic signal input. Moreover, efforts are being made to develop the next generation of packaging technology, in order to satisfy the requirements of new fields, such as hybrid electric vehicles, wide band gap semiconductor devices and optimized Si-based power modules. The current technological difficulties and some possible solutions are:

- The silicone gel that is used as an encapsulating material, cannot operate over 175 °C. Some alternatives for operation at 200 °C and more have been reported [96].
- The use of traditional soldering techniques as die attach technology has a temperature limitation based on its melting point between 180 and 220 °C. To replace this interface, silver diffusion sinter technique (a.k.a. low temperature joining) has already been successfully applied in some commercial devices [97]. The interconnection is made with a paste made of silver flakes embedded in a semi-fluid matrix instead of solder paste. By applying high pressure (e.g. 30 MPa) and moderately increased temperature (200–250 °C) simultaneously, the particles are densified and diffuse together. The melting point of this layer is close to 1000 °C. [98–100]
- Another alternative to soft soldering is the diffusion bonding technology, which consists of a bond based solely on intermetallics. As in soft soldering, a Sn-based solder is also used here. The difference is that in traditional soldering, only a small fraction of the Sn is transformed into Cu-Sn intermetallics. In diffusion bonding, by applying pressure ($\leq$6 MPa) and controlling the solder thickness ($\leq$ 10 µm) the whole volume of melting solder is consumed by the solidification process. As a result, a more reliable bond with a melting temperature over 400 °C is achieved. [98]
- Aluminium bond wires are a weak point of current module technology. New methods for interconnection include changing the wire material from Al to Cu, which should provide a tenfold increase in reliability [101], and replacing wire bonds by layer contacts [102] or metal foil [100]. Besides reliability issues, low-inductance module design that allows high *di/dt* switching is also one of the aims.
- Higher power densities make the thermal management of the module critical. A new step towards reducing the thermal resistance between chip and ambient is the use of a base plate with pin fins and integrated liquid cooling [46]. Another more complex approach is to integrate micro-channels in the bottom side of the DBC substrate for enhanced liquid cooling [103].

A good example of the potential of these improvements is the new SKiN module technology presented by Semikron [104], where a module (dual IGBT module, 600 V / 400 A) completely based on sinter technology was developed. This comprises the attachment from die to substrate, substrate to pin fin heat sink, and die to flexible circuit board.

3 CHARACTERIZATION OF THE SIC PIN DIODE MODULE

3.1 INTRODUCTION

The module here characterized is based on a 6.5-kV SiC PiN diode die rated at 12.5 A for a current density of 176 A/cm^2. This module prototype is the result of previous research work regarding 6.5-kV bipolar diodes done by SiCED and Siemens [105, 106]. The development of the diode has been addressed in [42] and a characterization of the device up to 300 °C can be found in [107]. The 6.5-kV, 1-kA power module was firstly introduced in [108]. The device characterization presented in this chapter was preliminarily published in [4], and the comparison to a Si diode module in [6], both of which are also included in [7]. A discussion of the high-frequency oscillations present in the turn-off transient —also treated in this chapter— was presented in [6].

The diode cross-section and top view is shown in Fig. 3.1. Low MPD wafers provided by Cree were placed in a hot wall reactor for the epitaxial growth. These consist of an n-type 4H-SiC substrate with 4° off-axis orientation, which is currently preferred over 8° due to a better material utilization and reduced BPD in the epitaxial layer [72]. BPDs are critical in bipolar devices, as they reduce the device performance and reliability [64, 75], refer to Sec. 2.1.3 for details. A blocking voltage of 6.5 kV was achieved through a 60 µm-thick n-base. [42]

Each die has a size of 3.5 × 3.5 mm^2 with an anode area of 7.1 mm^2, see Fig. 3.1b. The small size of each die is determined by yield limitations in the manufacturing process. As a consequence, to achieve a current rating of 1 kA per module, 80 dies in parallel operating at a high current density level of 176 A/cm^2 are needed. This level is considerably higher than the 50 to 75 A/cm^2 at which equivalent Si diodes are operated. Considering an on-state voltage of 4 V, the power losses can reach 700 W/cm^2 at the rated current. This demands a very careful thermal management in the module, without neglecting reliability, circuit parasitics and isolation requirements. [94, 109]

The diodes are packaged in a standard industrial module for 6.5 kV with dimensions of 130 × 140 × 48 mm^3, see Fig. 3.2 [110]. It contains two diode systems of 500 A each that can be used independently or connected in parallel to achieve a current rating of 1 kA. Inside the SiC diode module there are 4 DBC substrates, each with 20 SiC diode chips. 80 SiC chips equal an active area of 5.68 cm^2 per module. A commercial Si diode with the same package is rated at 6.5 kV and 1.2 kA per module [111].

A cross section of the module, indicating the different layers of the assembly, is presented in Fig. 3.3. Each DBC substrate is made of AlN, which is soldered to an Al/SiC base plate, a common combination used in high-power Si modules. Even though Al/SiC does not have such a good thermal conductivity as Cu, it is preferred due to its thermal expansion coefficient,

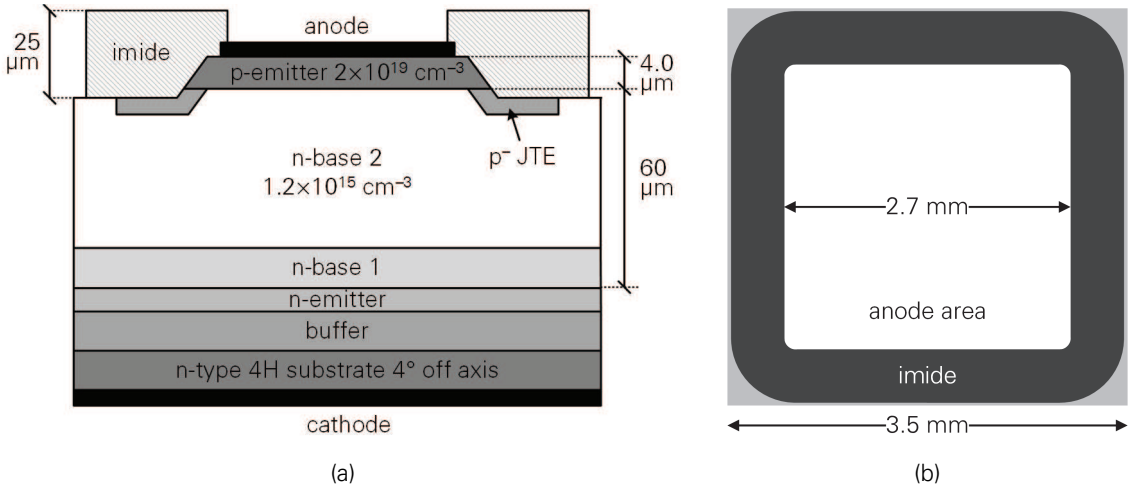


Figure 3.1: SiC diode chip design (a) cross section and (b) top view. [42]

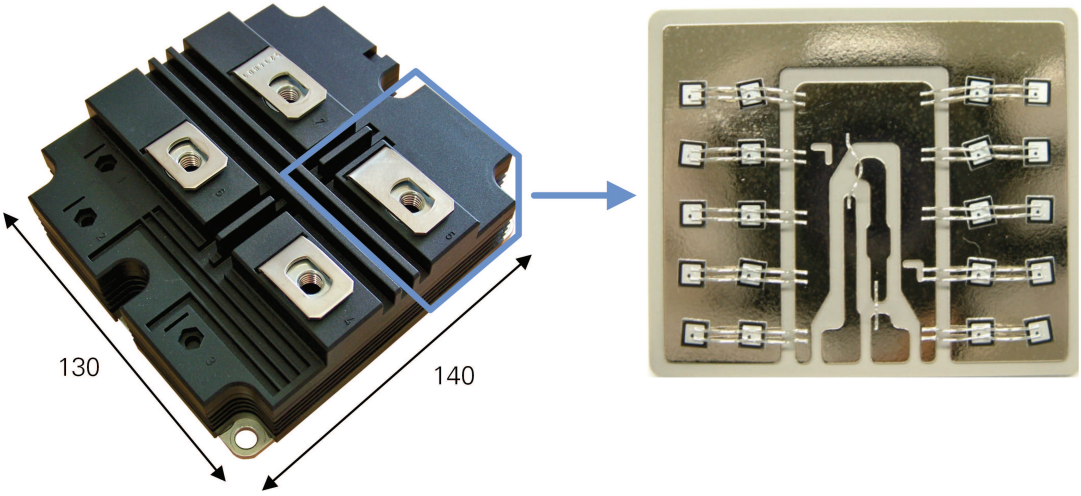


Figure 3.2: 6.5-kV 1-kA SiC diode module prototype and internal DBC substrate with SiC dies.

which is closer to the one of AlN [94, 112]. To simplify the prototype design, traditional Si module technology was adapted to these new dies, which is the reason for considering only temperatures up to 125 °C in the characterization. This first approach is of course not optimal, but it is useful to gain experience with the new device. As stated in [109], a SiC device will induce a higher stress level into the package as a Si device. The reason behind this is the higher thermal conductivity of SiC (3×) and the higher Young's modulus (also 3×), which represents the material stiffness. This leads to a 3.5× faster propagation of cracks in the solder layer, shortening the power cycle lifetime of the device. The higher current densities at which SiC devices operate put also a higher stress in the thermal management of the module. With the applied packaging technology, the maximum junction temperature is limited to 125 °C. It is clear that the development of these type of high-voltage, high-power modules demands a careful redesign of traditional packaging solutions.

As a new device, extensive testing is needed before a mature development stage can be reached. The characterization presented in this chapter includes the forward characteristic (on-state voltage), reverse characteristic (leakage current) and dynamic behaviour (switching transient, losses). The tests were conducted in a temperature range of −25 to 125 °C. In the case of the dynamic behaviour, the module was switched with a 6.5-kV IGBT module [113] as well as with two series-connected 3.3-kV IGBT modules [114]. Besides the temperature variation,

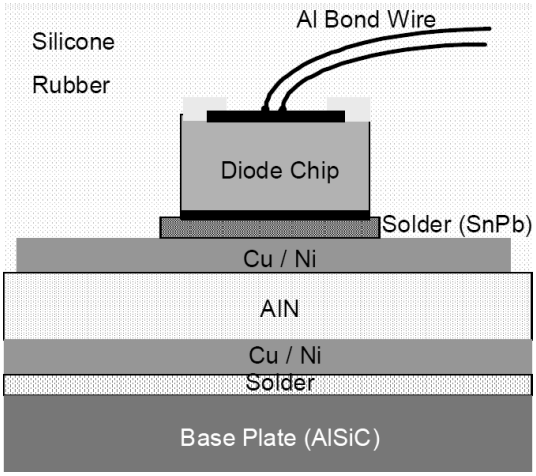


Figure 3.3: Single chip cross section of the SiC diode module assembly. *Reproduced with permission of Trans Tech Publications Ltd. from [108] in the format Thesis/Dissertation via Copyright Clearance Center.*

different current commutation speeds *di/dt* and commutation voltages were tested. Furthermore, a benchmark of the SiC module and a 6.5-kV Si diode [111] is included. Complementary to these tests, measurements on single SiC diode chips were carried out to evaluate the forward voltage drift degradation effect [64].

Needless to say, there are many aspects that need to be properly investigated and optimized before a module is fully qualified for normal operation, the electrical characterization is only a fraction thereof. Some of them are:

1. Module reliability [94, 109]
    - Static current/temperature distribution among the dies, layout optimization for minimum temperature spreading
    - Power cycling (DBC, bond wires, solder joints fatigue)
    - Long term stability
    - Partial discharges
    - Surge current capability
    - Optimal edge passivation
    - DBC optimization (materials, copper edge termination)
2. Chip design
    - Process stability and optimization (epitaxy, mesa-etching, imide, metallization)
    - Reduction of critical electric field strength (device edge termination) [109]

With the information gathered in this chapter it is possible to get a picture of the technological advantages and drawbacks of SiC diodes for the selected application.

3.2 EXPERIMENTAL SETUP

For the characterization of the SiC diode module the static and dynamic behaviour were investigated. This comprises the forward and reverse characteristic at different temperatures for the static measurements. The effect of forward degradation —see Sec. 2.1.3— was also studied. The switching behaviour was characterized in a double-pulse test. The IGBT modules and

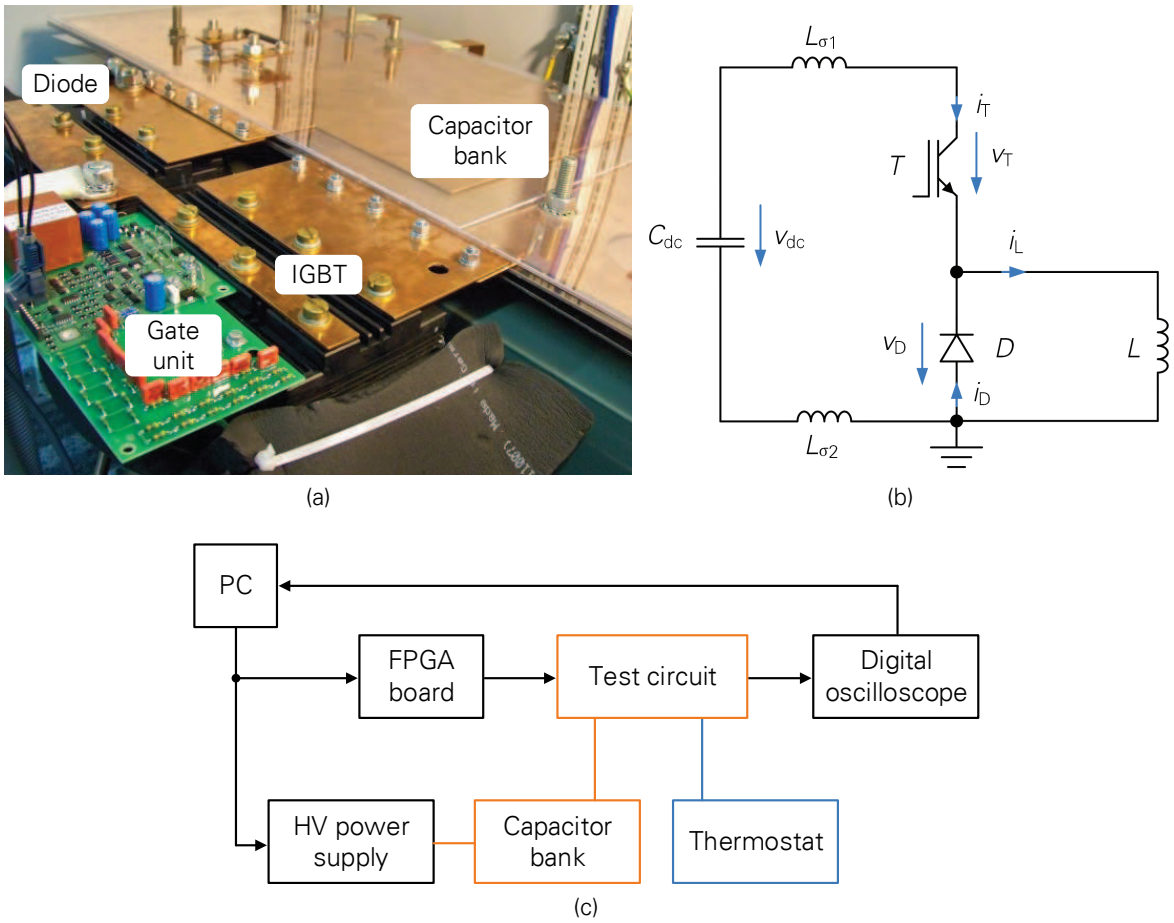


Figure 3.4: Test bench for the investigation of on-state and switching behavior. (a) Experimental setup photo for a 6.5-kV IGBT, (b) schematic diagram of the test circuit and (c) block diagram of the laboratory setup.

the GDU used to drive them in the switching tests are briefly presented. Each test bench is described in this section.

3.2.1 SWITCHING BEHAVIOUR

DOUBLE-PULSE TEST

The aim of the switching behaviour characterization is to analyse the switching transients of the diode D when commutating with an IGBT T at a defined voltage V_D, current I_D and junction temperature ϑ_j. This can be realized with a double-pulse test, see Fig. 3.5a. After the temperature ϑ_j has been externally adjusted and the capacitor C_{dc} charged to a voltage V_{dc}, the device T is turned on and the current flows through the inductor L until the desired commutation current I_D is reached ($t_0 < t < t_1$). In the instant t_1, T is switched off and the current commutates to the diode D. After a some microseconds, T is turned on and the diode switches off (t_2). Finally, T is turned off (t_3) and the current commutates back to the diode and slowly decays to zero. The commutation waveforms are acquired during t_1 and t_2.

A robust mechanical design was accomplished using 2 mm-thick planar bus bars connecting the dc-link capacitor bank C_{dc} and the modules, see Fig. 3.4a. It consists of layers of copper and dielectric (polycarbonate) stacked on top of each other. The capacitor bank is made of an array of 2×2 metallized polypropylene film capacitors (2 mF, 2.8 kV, Vishay ESTAdry-DC-Capacitor DCMKP 2.8/4.0mF/2). The load L is an air-core inductor of 1 mH. The stray inductance of the

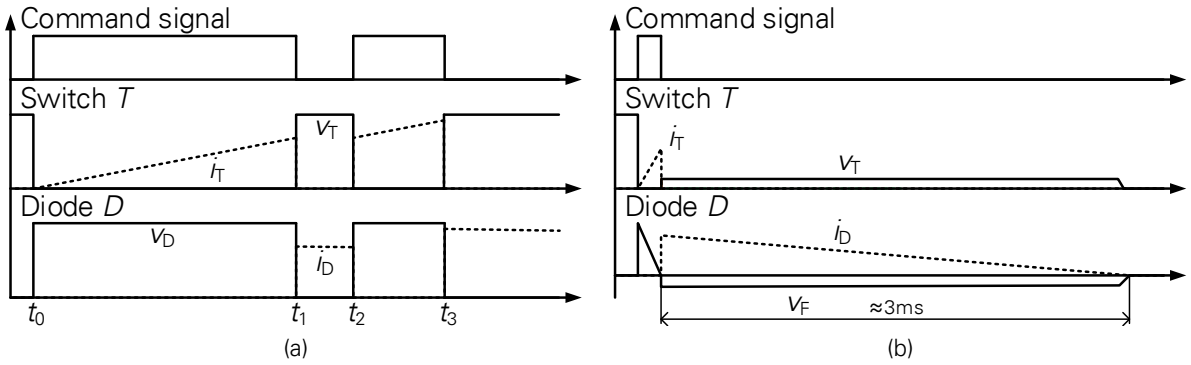


Figure 3.5: Double- (a) and single-pulse (b) patterns for device characterization

Table 3.1: Laboratory equipment

Oscilloscope	LeCroy 24MXs-B	8 bit, 200 MHz, 2.5 GS/s
HV capacitor charger	FuG 1000M – 15 000	15 kV, 120 mA
Thermostat	Lauda Proline RP845	3.50 kW (heating), 0.80 kW (cooling)

Table 3.2: Measurement instrumentation

Variable	Type	Model	BW (MHz)	Atten.
v_D, v_{dc}	Passive probe	PPE6KV	400	1000:1
v_T	Differential probe	TTSI9010	70	1000:1
i_D	Rogowski coil	CWT30B	10	1000:1
i_T, i_L	Rogowski coil	CWT15B	17	500:1
v_F	Differential probe	TTSI9002	25	200:1

commutation circuit (C_{dc}, T, D) has a value that varies from 235 to 255 nH, depending on the semiconductor configuration tested (1× 6.5-kV IGBT vs. 2× 3.3-kV IGBTs). Its relatively high value is caused mainly by the capacitors used for these tests. For simplicity, this inductance is represented by two concentrated inductors $L_{\sigma 1}$, $L_{\sigma 2}$ in Fig. 3.4b.

The junction temperature of the devices is controlled by a thermostat, which sets the temperature of the liquid that flows through the plate where the modules are attached to. Due to the maximum temperature limitation of the liquid used, temperatures over 80 °C were set with resistors attached to the heat sink. The dc-link capacitor is charged by a high-voltage power supply before the measurements are carried out. A partially automated measurement system was used. The values of V_{dc} and I_L are set using a graphical user interface on a computer connected to the test bench. The measurements are captured by two 8-bit 200-MHz four-channel digital oscilloscope, capable of working at a sample rate of 2.5 GS/s. A block diagram of this setup can be found in Fig. 3.4c, the laboratory equipment is listed in Table 3.1, the instruments used for measuring the voltage and current waveforms are summarized in the Table 3.2.

IGBT MODULES AND GATE DRIVE UNIT

As mentioned before, two different switch configurations were considered for the diode characterization: a 6.5-kV IGBT and two series-connected 3.3-kV IGBTs. In the case of the 6.5-kV IGBT a FZ600R65KF2 was used, an NPT fast switching IGBT which has a nominal current rating of 600 A and can switch up to 1200 A (repetitive peak) [113]. The 3.3-kV IGBT is a FZ1500R33HL3, which is a third generation IGBT (IGBT3) with Trench + Field-Stop technology and has a nominal current rating of 1500 A. Both IGBTs are packaged in a 130×190 mm^2 module.

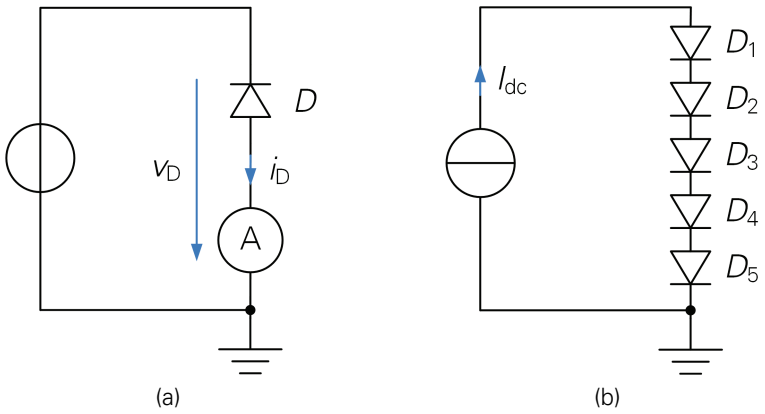


Figure 3.6: Test setup for the measurement of (a) leakage current and (b) forward degradation effect.

The 6.5-kV IGBT was driven with a fully digitally-controlled GDU with a voltage of −10/+15 V, refer to [115] for details. Instead of using gate resistors for controlling the switching speed of the device, a reference gate-emitter voltage waveform defined by the user is given to the output amplifier. Additional functions such as active *dv/dt* control, active clamping during switch off and active balance of collector-emitter voltage for series-connected IGBTs are included in the device. The parameters can be easily changed by the user and loaded in the GDU, without any hardware adjustments.

For the series-connected 3.3-kV IGBTs, a classical analogue GDU for industrial inverters was used, where the *di/dt* during the IGBT turn-on and turn-off transients is adjusted through gate resistors. This GDU also operates at −10/+15 V gate-emitter voltages. The dynamic balancing of the series-connected IGBTs is achieved by active gate voltage control [116]. For the static balancing, resistors in parallel to each device are used. More details to the setup are given in Sec. 3.4.3.

3.2.2 STATIC BEHAVIOUR

FORWARD AND REVERSE CHARACTERISTIC

Regarding the measurements for the on-state voltage, these were conducted using the same circuit presented in Fig. 3.4b. The voltage probe was changed to one with lower attenuation, see Table 3.2, v_F. Instead of a double-pulse, a single-pulse measurement was conducted, see Fig. 3.5b. The decaying current ramp through the diode during the freewheeling phase was captured together with the voltage waveform. In order to minimize the self-heating effect, the time of the free-wheeling phase was limited to 3 ms. To achieve this, the load inductance was reduced to $L = 58\,\mu H$.

The leakage current was measured using a 6½-digit multimeter (Keithley 2100). This allowed an accurate measurement of currents above 1 µA. Exceptionally, an alternative setup for leakage current measurements with higher accuracy was used for the 25 °C measurements of the SiC diode and for the whole measurement set of the Si diode. This comprised the aforementioned digital multimeter for the voltage measurement and a Keithley picoammeter model 6485. With this improved setup, currents of at least 20 nA could be measured. The simplified schematic diagram of the test setup can be found in Fig. 3.6a.

FORWARD DEGRADATION

The stability of the forward voltage was studied in a low voltage test bench using single-chip diodes packaged in a TO-220 housing. As mentioned in Sec. 2.1.3, the forward degradation effect of the on-state voltage occurs when the diode is stressed with current for the first time. If defects are present in the tested die, degradation can occur within a few minutes up to a couple of hours.

The tests were carried out in the following way:

1. Five diodes mounted on individual heat sinks and connected in series were stressed with 15 A dc current, equivalent to a current density of 211 A/cm^2. Forced air cooling was used to keep the devices under 120 °C.

2. After a stress interval of some minutes (2...20), the diodes were cooled down and the on-state voltage was measured.

3. Steps 1. and 2. were repeated until the total current stress time reached 80...90 min.

The test setup is schematically represented in Fig. 3.6b. With this simple test it was possible to obtain some insight into the total percentage of samples affected by this problem and the time needed for a diode to reach a final stable on-state voltage. The case temperature was kept high ($\approx$ 80 °C), as it helps to accelerate the degradation progress (5–8× per 100 K) [75].

3.3 EXPERIMENTAL RESULTS: STATIC BEHAVIOUR

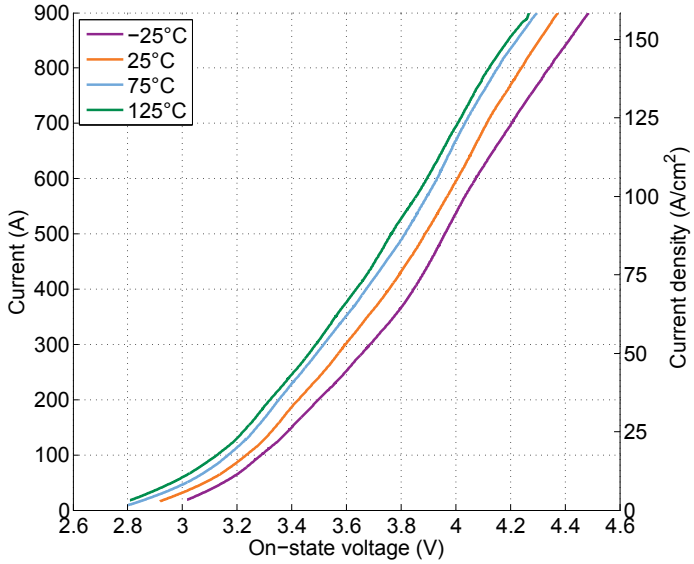
The on-state voltage curve for the SiC diode measured at four junction temperatures can be seen in Fig. 3.7a. The on-state voltage at 100 A/cm^2 (578 A) varies between 4.05 V at –25 °C and 3.87 V at 125 °C. A NTC with an average of –1.3 mV/K over the full current range can be observed, see Fig. 3.7b. The thermal coefficient decreases as the temperature increases, going from –1.7 mV/K between –25 and 25 °C to –0.8 mV/K between 75 and 125 °C. This behaviour was also observed in previous work [105]. It was attributed out to an unsuitable ohmic contact formation, which at high temperatures does not have a major influence.

One of the drawbacks of bipolar devices made out of wide band gap materials, such as SiC, is a higher junction voltage drop. As explained before, this voltage is given by (2.6), p. 30. The variable that causes this higher voltage drop is the intrinsic carrier concentration n_i. Table 2.1 indicates an n_i difference of 20 orders of magnitude compared to Si. Assuming a carrier concentration in the drift zone of 10^{15} cm^{-3}, as in the SiC diode analysed, a junction voltage V_j of 3.0 V is obtained. In the case of Si, V_j would amount to 0.6 V, which is only 1/5 of SiC.

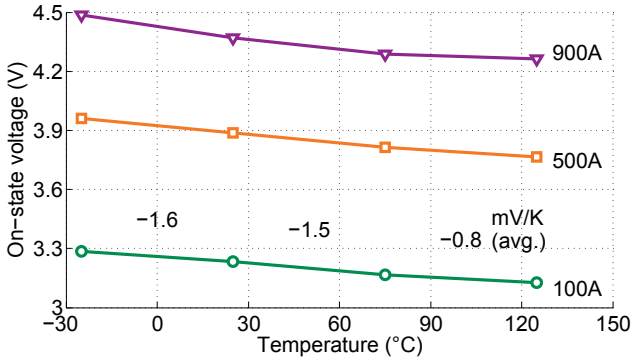
It is well known that NTC can lead to thermal runaway in parallel-connected chips [117]. No thermal runaway was observed after conducting tests under continuous load conditions (100 A/cm^2 dc, 2 h long). The average temperature variation in the measured chips was less than –1 K, with a maximum increase of 7 K in one chip. After 90 min the temperature remained stable.

Fig. 3.8 shows the leakage current for different temperatures. Due to limitations in the current measurement equipment, only the 25 °C was performed with high accuracy (currents starting from 200 nA) and error estimation. The results indicate that the leakage current is kept low in the whole temperature range. The dissipated power at 4 kV and 125 °C—*worst case* operating conditions— amounts to less than 8 mW, which is one of the advantages of SiC devices compared to Si devices. The leakage current stays under 250 µA.

Regarding forward voltage degradation, see Sec. 3.2.2, 20 single-chip diodes in TO-220 package were tested. The results showed that 20% had a considerable on-state voltage increase (more than 20%) after being exposed to 15 A for 80...90 min. Fig. 3.9 shows the forward characteristics of the 20 diodes before and after the current stress test. It can be appreciated that



(a)



(b)

Figure 3.7: On-state voltage (a) as a function of current and (b) as a function of junction temperature, including average temperature coefficients, full SiC diode module.

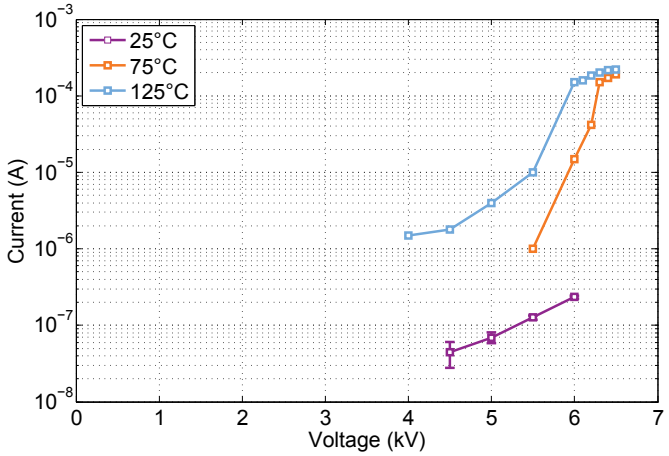


Figure 3.8: Leakage current of the SiC diode module for different junction temperature values. (Only the measurement at 25 °C includes error bars, 99,7% confidence.)

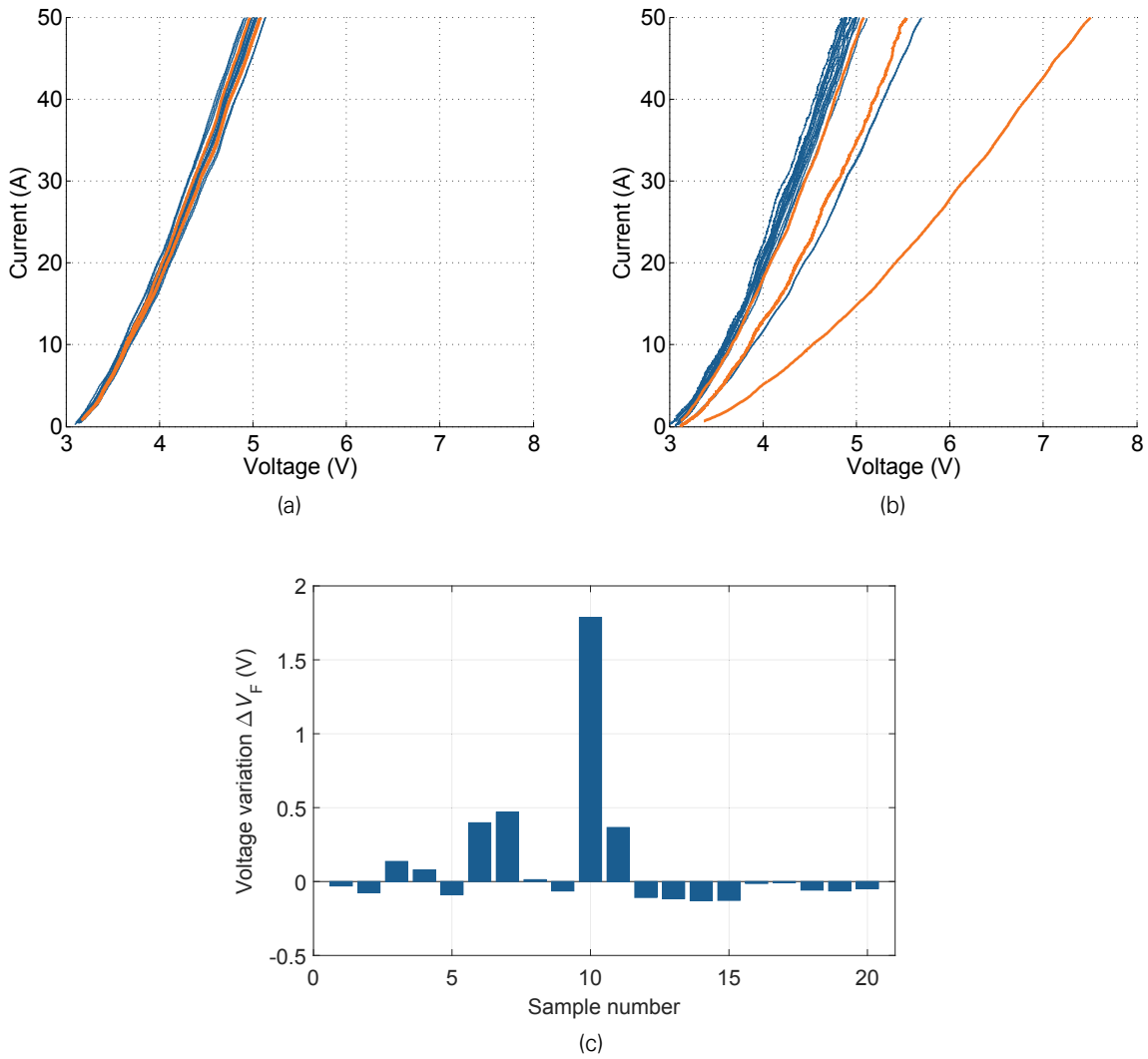


Figure 3.9: Forward degradation effect for 20 diode single-chip samples: (a) initial characteristics, (b) characteristics after 90 min of continuous conduction, (c) voltage variation at a constant current of 30 A. In orange the V-I characteristics of the three exemplary diodes shown in Fig. 3.10. Maximum case temperature 120 °C.

besides the evident on-state voltage variation in four diodes, the rest stay stable or within the boundaries given by the fabrication tolerances. The voltage variation at a constant current of 30 A has been plotted for each sample in Fig.

The characteristics of three exemplary diodes are plotted in Fig. 3.10 in the V-I plane and as a function of time for I_D = 30 A. Diode A does not experience any forward degradation, diode B has a moderate drift, and diode C is the sample with the highest voltage variation. Fig. 3.10b shows that the voltage increase is gradual during the first hour. In some cases, e.g. diode C, the voltage increases rapidly during the first 20 min, whereas in other cases, like the diode B, the increase is gradual over the first 60...70 min.

A good method for die screening on wafer-level that is able to detect defective diodes in an early stage would provide an effective way of sorting defect dies out. Since current stress capability on wafer level is limited, current work is focused on other principles of detection, e.g. low-current characteristics (nA-, µA-range), opto-electrical imaging. Some methods for reducing the impact of BPD have been reported, refer to Sec. 2.1.3. As shown in the measurements, this

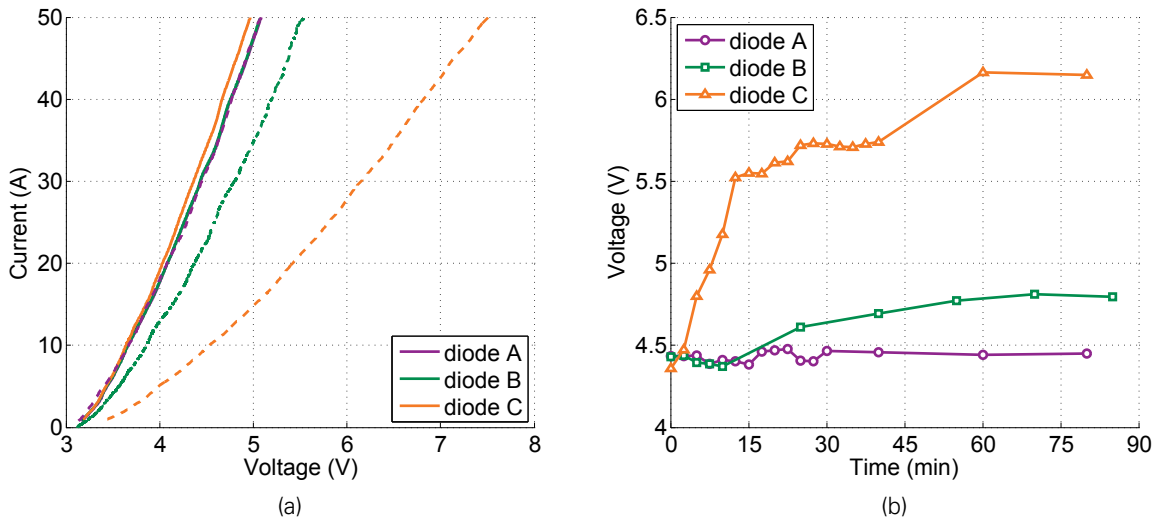


Figure 3.10: Forward degradation effect for three selected diodes: (a) V-I plane, segmented lines indicate the characteristic after the current stress test, (b) as a function of time for I_D = 30 A.

is a critical issue for future SiC bipolar device development. The final solution to this problem lies solely in the availability of defect-free wafers. If the current trend is kept, that should be possible within a few years. Meanwhile, alternatives to deal with devices which exhibit degradation of the forward characteristic have been proposed, such as operating the device at high temperature, heating it up if necessary. By doing so, the degradation effect can be reversed [118].

3.4 EXPERIMENTAL RESULTS: SWITCHING BEHAVIOUR

3.4.1 DEFINITIONS AND ADJUSTMENTS

In order to evaluate the results presented in this section it is mandatory to define the way the current and voltage slopes and switching energies are calculated. As a basis for the switching loss calculations, the definitions contained in Infineon's application note AN 2011-05 were applied [119], which are summarized in Fig. 3.11. The voltage polarities as well as the current directions can be extracted from Fig. 3.12. The points for current and voltage slope calculation during the diode turn-off transient are indicated with a ∘ symbol in Fig. 3.11a. The definition of the loss calculation for the IGBT turn-off transient, although not relevant for the diode characterization, is also included in Fig. 3.11, since it is used in the electrothermal models presented in Chap. 4.

As the photo of the module in Fig. 3.2 reveals, the prototype tested does not include an auxiliary terminal to have access to the internal diode voltage $v_{D,int}$, see Fig. 3.13a. This means that the voltage measurement $v_{D,probe}$ has to be carried out at the power terminals. As a consequence thereof, in presence of a current variation in time (di/dt), the module's internal stray inductance $L_{\sigma,D}$ will affect the measured voltage $v_{D,probe}$. This effect can be appreciated in Fig. 3.13b by looking at the voltage rise in $v_{D,probe}$ during the negative current slope of i_D. The measured diode current i_D corresponds to the current of the module and of the RC snubber.

To calculate the switching losses it is necessary to cancel out the effect of $L_{\sigma,D}$, which is given by

$$v_{D,int} = v_{D,probe} + L_{\sigma,D}\frac{di_{D,int}}{dt}. \tag{3.1}$$

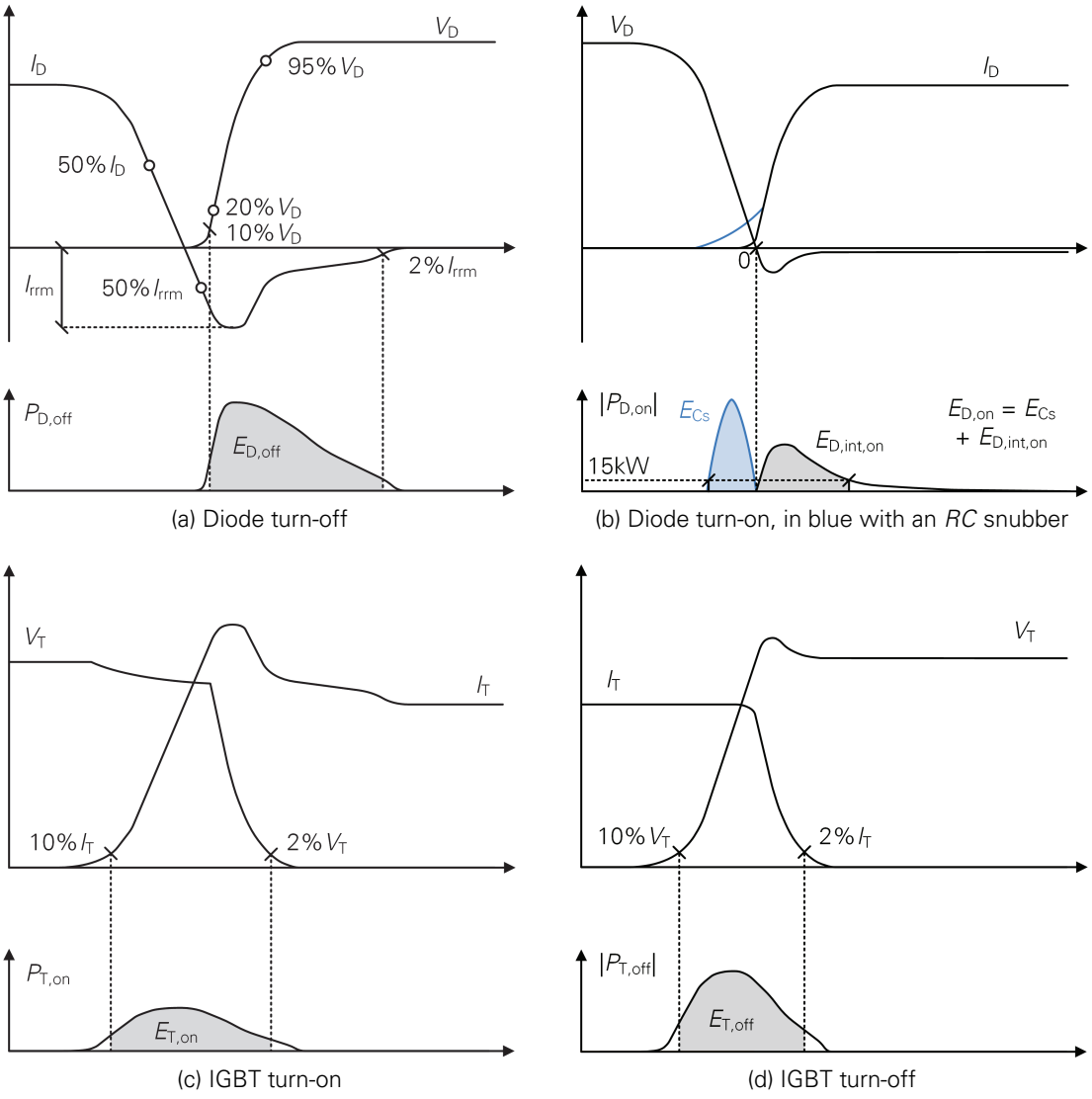


Figure 3.11: Definition of the limits for calculating the current and voltage slopes (∘ symbol) and the switching losses during a commutation, according to [119] with the exception of (b).

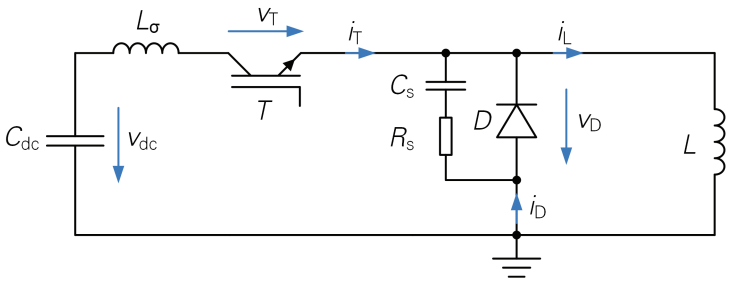
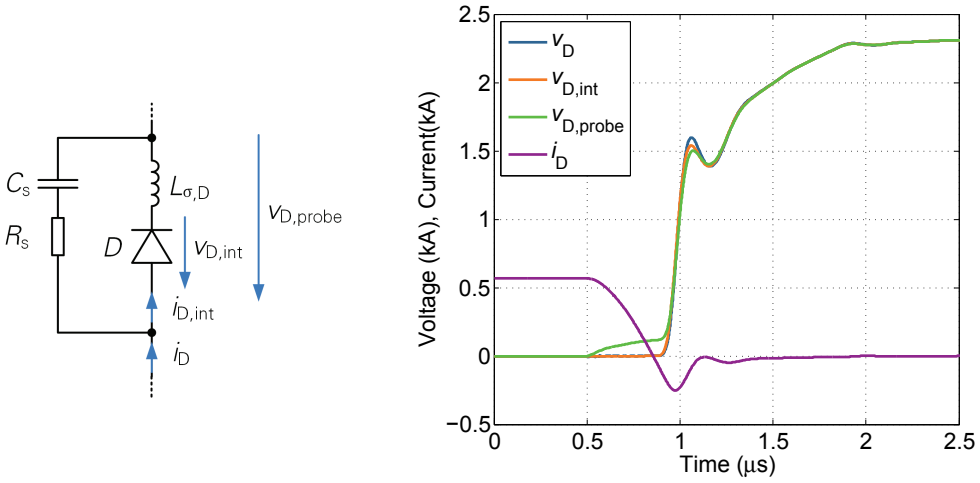


Figure 3.12: Test circuit diagram for diode switching characterization with added *RC* snubber (*di/dt1-2*: 4.7 Ω, 9.4 nF; *di/dt3*: 4.7 Ω, 14.1 nF).



(a) Equivalent circuit of the diode module and *RC* snubber

(b) Simulated diode turn-off waveforms

Figure 3.13: Explanation of the method for cancelling the diode module's internal stray inductance.

However, due to constraints in the experimental setup, the current $i_{D,int}$ could not be directly measured. Instead, the current i_D, which also includes the snubber current, was measured. Considering that the *RC* snubber is not active until the device starts to block voltage (shortly before the reverse recovery peak is reached), it is possible to use following equation to approximate the voltage $v_{D,int}$, which will be referred as v_D in this text.

$$v_{D,int} \approx v_D = v_{D,probe} + L_{\sigma,D}\frac{di_D}{dt} \tag{3.2}$$

The waveforms v_D and $v_{D,int}$ start to differ from each other only after the diode starts to block voltage, as the simulation results in Fig. 3.13b show. In this plot, the calculated voltage waveform v_D, as well as the measured and internal waveforms $v_{D,probe}$, $v_{D,int}$ were included. The calculated voltage v_D cancels the effect of the stray inductance in the initial phase of the commutation. Due to the *RC* snubber, the reverse recovery voltage peak is overestimated by v_D (compare to $v_{D,int}$). This is not critical, since the losses do not differ from each other in more than 3%. The voltage waveforms presented in this section and the ones used for the calculation of the switching losses correspond to v_D, as calculated by (3.2).

The next step in order to estimate the losses in the diode out of v_D and i_D is to substract the effect of the energy stored in the snubber capacitor C_s. The losses calculated with the current i_D are useful to understand the implications at system level, such as efficiency, or when comparing the diode to other devices. To calculate the losses in the semiconductor itself, which are important for the estimation of the junction temperature, the energy of the capacitor C_s has to be subtracted from the total losses. For the diode turn-off transient, the following relation was used in the calculations:

$$E_{D,off} \approx E_{D,int,off} + \frac{1}{2}\cdot 0.8C_s \cdot {V_D}^2 \tag{3.3}$$

To not underestimate the diode semiconductor losses $E_{D,int,off}$, the minimum possible capacitance value of the capacitor considering ±20% tolerance was used ($0.8C_s$). In the case of the diode turn-on losses, a more accurate alternative can be used to calculate the diode semiconductor losses $E_{D,int,on}$. As Fig. 3.11b shows, there are two phases that can be easily separated from each other. The first phase (blue colour) —the diode is reverse biased and a positive current i_D flows— corresponds to the discharge of the capacitor C_s. The losses that take place

after the diode has been forward biased correspond mainly to the losses in the semiconductor itself $E_{D,int,on}$.

In (3.3) the symbol ≈ was used to indicate that it is an approximation of the real value. The energy term corresponding to the reverse recovery current peak I_{rrm} and the stray inductance ($1/2 L I^2$) [25] was not considered, as simulations of the commutation cell showed that its influence is around 5% of the total losses $E_{D,off}$, which is negligible considering the tolerance of the capacitor C_s (±20%).

3.4.2 SWITCHING BEHAVIOUR WITH A 6.5-KV IGBT

The switching behaviour of the new SiC diode module was investigated using the test setup introduced in Sec. 3.2.1, with an IGBT FZ600R65KF2 as switch *T* and half of the SiC diode module (40 dies in parallel) as the diode *D*. Currents between 50 and 600 A at a dc-link voltage V_{dc} of 2.3, 2.9 and 3.5 kV were switched. The average junction temperatures ϑ_j tested were 25, 75 and 125 °C. Preliminary results of the device characterization were presented in [4]. Although the IGBT and diode are the same in this work and in [4], the GDU used here is a digitally controlled one instead of a classic analogue model, see Sec. 3.2.1.

Since the GDU does not rely on resistors for adjusting the current slope, the different *di/dt* configurations used to turn on the IGBT are labelled as *di/dt1*, *di/dt2* and *di/dt3*. Fig. 3.14 shows average and peak current and voltage change rates during diode turn-off at ϑ_j = 125 °C and V_{dc} = 3.5 kV. Fig. 3.14 also includes reference curves obtained by switching on the IGBT with a standard GDU and 4.1 Ω gate resistance $R_{g,on}$, as in [4]. It can be seen that *di/dt1* is a rather conservative speed for 6.5-kV devices, whereas *di/dt2* and *di/dt3* take advantage of the fast-switching properties of SiC diodes. The peak di_{rr}/dt (Fig. 3.14b) is located after the reverse recovery maximum, and it is a good indicator for the voltage ringing intensity, which is treated later in Sec. 3.6. For this semiconductor configuration, the peak di_{rr}/dt is about 50% higher than the average *di/dt*.

Common *dv/dt* values for 4.5-kV and 6.5-kV devices with conventional GDUs are under 4 kV/µs [4, 120]; in the measurement set used as a reference the *dv/dt* is even under 2 kV/µs. Although the average *dv/dt* for the SiC diode switching with the digitally controlled GDU is under 5 kV/µs for currents close to the nominal rating, the peak *dv/dt* increases considerably, comp. Fig. 3.14 (c) and (d). A higher average *dv/dt* means faster switching and lower switching losses. However, when driving a motor, high instant *dv/dt* values increase the stress applied to the windings' insulation and bearings, reducing the motor lifetime in case no filters are applied [121]. EMI generation is also not a minor issue [122]. This puts a limit to the practical application of loss reduction through high-speed switching. The impact of the higher *di/dt* at converter level is analysed in Chap. 4.

In the waveforms previously published in [4], a ringing in the voltage waveform can be observed. To avoid this problem, an *RC* snubber was connected to the diode terminals, as depicted in Fig. 3.12. The values chosen were R_s = 4.7 Ω, C_s = 9.4 nF for *di/dt1* and *di/dt2* and 14.1 nF for *di/dt3*. A thorough study of the current and voltage oscillations in the diode with this test setup as well as the selection of the *RC* snubber can be found in Sec. 3.6. The paper [4] also includes switching waveforms at a junction temperature ϑ_j = –25 °C, but since these were practically identical to the waveforms at 25 °C they were not included here.

The waveforms together with instant power and switching energy calculations for 600 A are shown in Figs. 3.15, 3.18 and 3.20, where the influence of dc-link voltage, current change rate and junction temperature are depicted. Furthermore, switching loss calculations for the three cases covering the complete current range are included in Figs. 3.16, 3.19 and 3.21.

In Fig. 3.15, different *di/dt* values were accomplished by adjusting the IGBT's GDU turn-on parameters; these correspond to a *di/dt* variation between 1.5 and 4.8 kA/µs at 3.5 kV, 600 A and 25 °C. In terms of current density, it is a variation from 0.54 to 1.68 kA/(cm^2·µs). The SiC

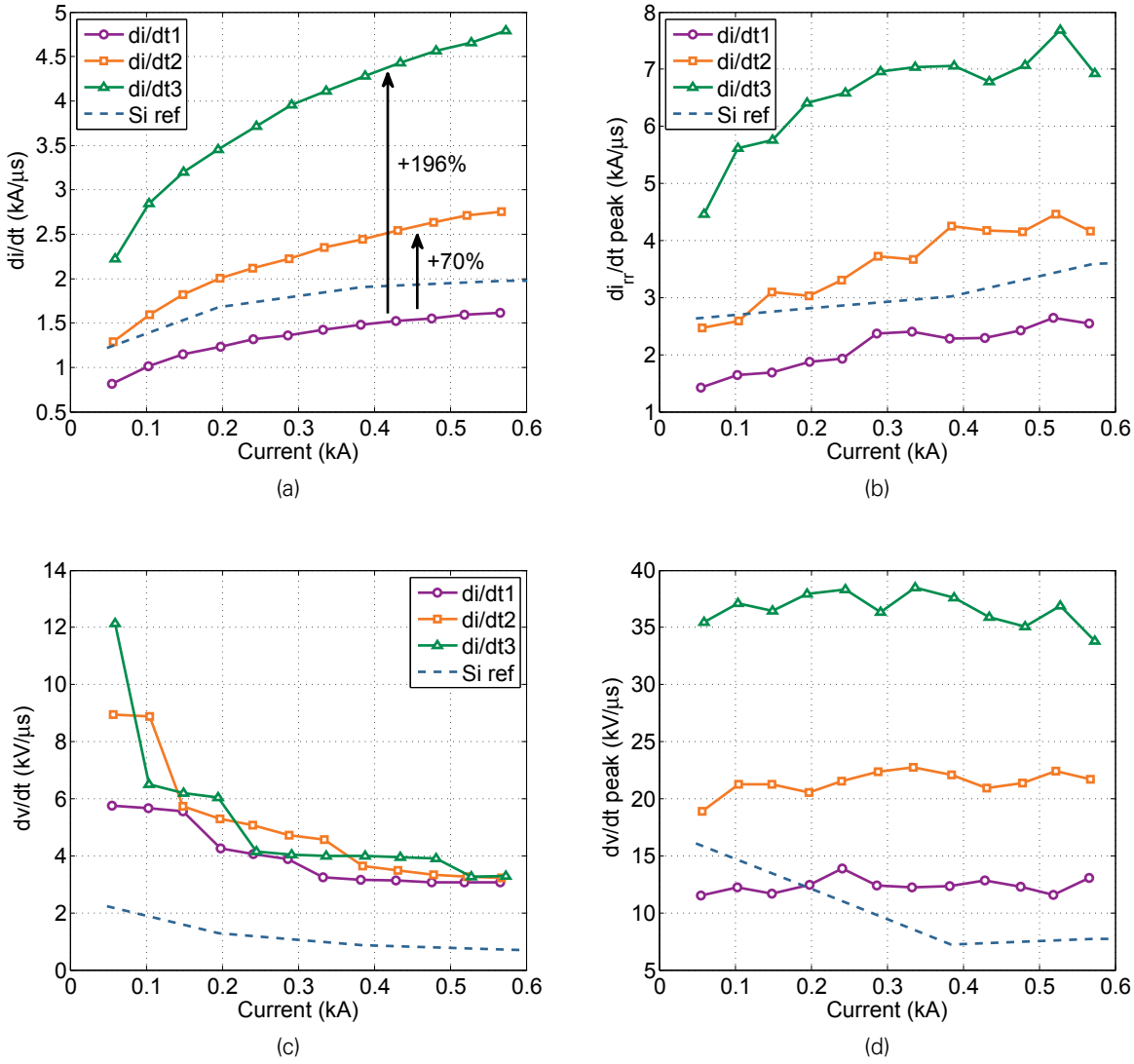
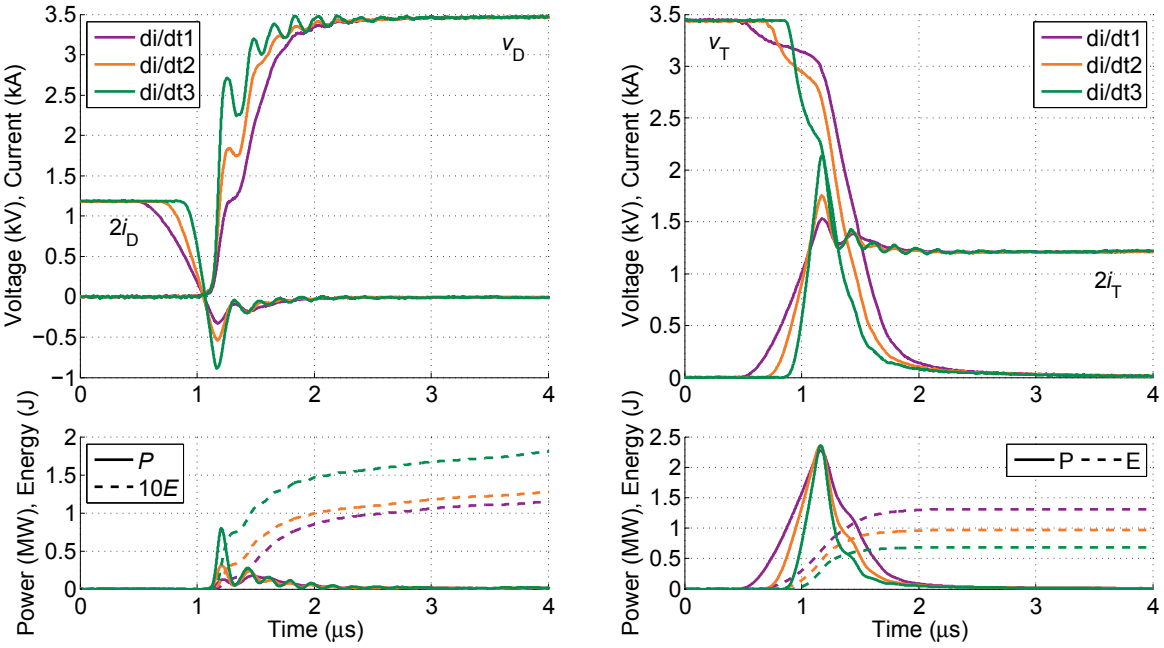


Figure 3.14: Voltage and current change rates for diode turn-off, (a) *di/dt* (50% of I_{rrm} and 50% of I_D), (b) peak reverse recovery di_{rr}/dt, (c) *dv/dt* (20% and 95%), (d) peak *dv/dt*. *Si ref*: reference *di/dt* for a 6.5-kV Si diode switched with an IGBT using a standard GDU with $R_{g,on} = 4.1\,\Omega$. ($V_{dc} = 3.5\,kV$, $\vartheta_j = 125\,°C$)



(a) Diode turn-off transient

(b) IGBT turn-on transient

Figure 3.15: Commutation waveforms for different current change rates *di/dt*: 1.5, 2.5, 4.8 kA/µs (V_{dc} = 3.5 kV, I_L = 600 A, ϑ_j = 25 °C, C_s = 9.4 nF, 14.1 nF, R_s = 4.7 Ω).

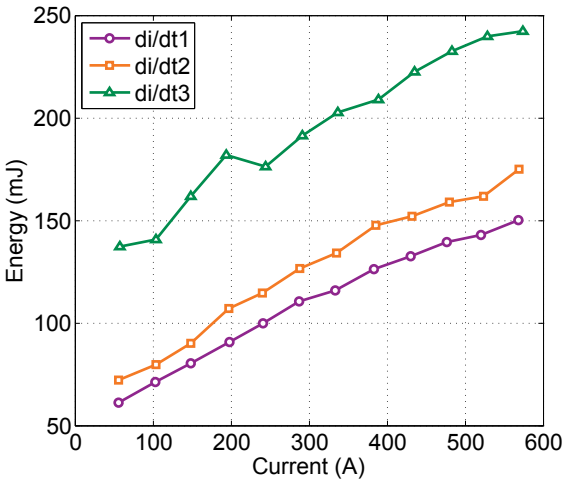
diode shows a low reverse recovery charge, with a small peak of 269 A at 2.5 kA/µs and 165 A at 1.5 kA/µs, 4 to 5 times smaller than for Si diodes [111]. At 4.8 kA/µs, the reverse recovery peak increases to 442 A. A part of the measured reverse recovery current corresponds to the capacitor C_s current, see Sec. 3.6 for details.

The small stored charge has a direct influence on the reduction of losses during diode turn-off and IGBT turn-on. This can be further appreciated in Fig. 3.16. In the case of the diode, the switching losses remain under 250 mJ, even for very high *di/dt* values and considering the additional energy in C_s. In the case of the IGBT, for a reduction of the *di/dt* from 2.5 to 1.5 kA/µs, IGBT turn-on losses increased from 1.15 J to 1.48 J (I_L = 600 A).

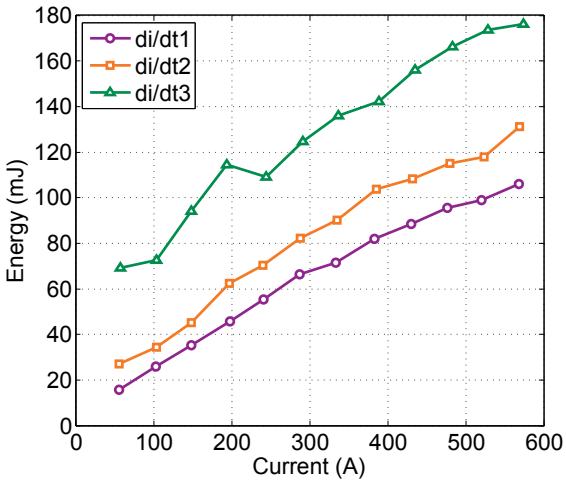
In Si devices, the maximum *di/dt* during the IGBT turn-on transient is limited by the reverse recovery behaviour of the diode that commutates. The reverse recovery safe operating area (RRSOA) of the diode is limited by the maximum power the diode module can handle. For a 6.5-kV, 600-A diode this amounts to 1800 kW [111]. Since SiC PiN diodes have a very small and short reverse recovery peak, the power stress during turn-off is minimum, see Fig. 3.15. Even for extreme *di/dt* and *dv/dt* values, the peak power does not reach 1 MW.

To get an idea on possible loss reduction in the IGBT by further increasing the *di/dt* at turn-on beyond the measured values the plot in Fig. 3.17 was elaborated. Here the losses at 600 A, 3.5 kV and 125 °C were plotted against the *di/dt* and a curve was fitted to each data set. The diode losses are directly proportional to the *di/dt*, with a low slope of 34 mJ/(kA/µs). The IGBT turn-on losses are strongly influenced by the *di/dt* for low values (e.g. < 3 kA/µs). As an example, to reduce the losses from 1.5 to 1.25 J it is necessary to increase the *di/dt* in only 0.8 kA/µs. To go from 1 to 0.75 J, however, would require an increase of 2.7 kA/µs.

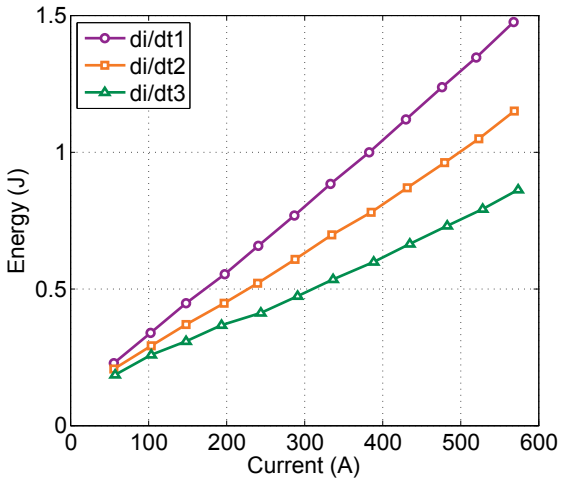
As mentioned before, an *RC* snubber was connected in parallel to the diode, in order to reduce the ringing in the voltage waveforms. The *RC* snubber can help switching the diode if high commutation speeds are desired, otherwise the overvoltage could damage the device or EMC problems could arise, depending on the external power circuit parasitics. As the *di/dt*



(a) Diode and *RC* snubber turn-off losses



(b) Diode turn-off losses



(c) IGBT turn-on losses

Figure 3.16: Switching losses for different current change rates *di/dt* (V_{dc} = 3.5 kV, ϑ_j = 125 °C, I_L = 50...600 A, C_s = 9.4 nF, 14.1 nF, R_s = 4.7 Ω).

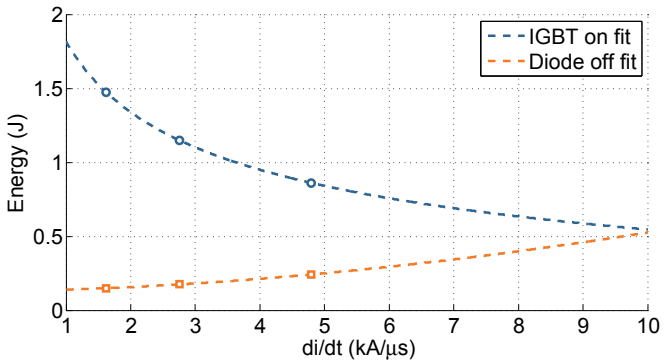


Figure 3.17: Switching losses (IGBT turn-on and diode turn-off) for different current change rates at I_L = 600 A including fitted curves (V_{dc} = 3.5 kV, ϑ_j = 125 °C, C_s = 9.4 nF, 14.1 nF, R_s = 4.7 Ω).

increases, higher capacitance values are needed to keep the oscillations under control. The losses in the diode plus *RC* snubber circuit increase due to the energy stored in the capacitor C_s [123]. The losses added by the snubber capacitor E_{Cs} during turn-off and turn-on are given by

$$E_{Cs} = C_s V_{dc}^2. \tag{3.4}$$

For V_{dc} = 3.5 kV and C_s = 15 nF, this energy amounts to 184 mJ. This is a negligible loss increase, taking into account the conduction losses of this diode. Considering a continuous current of 600 A in a full module, the conduction loss P_{cond} dissipated equals to

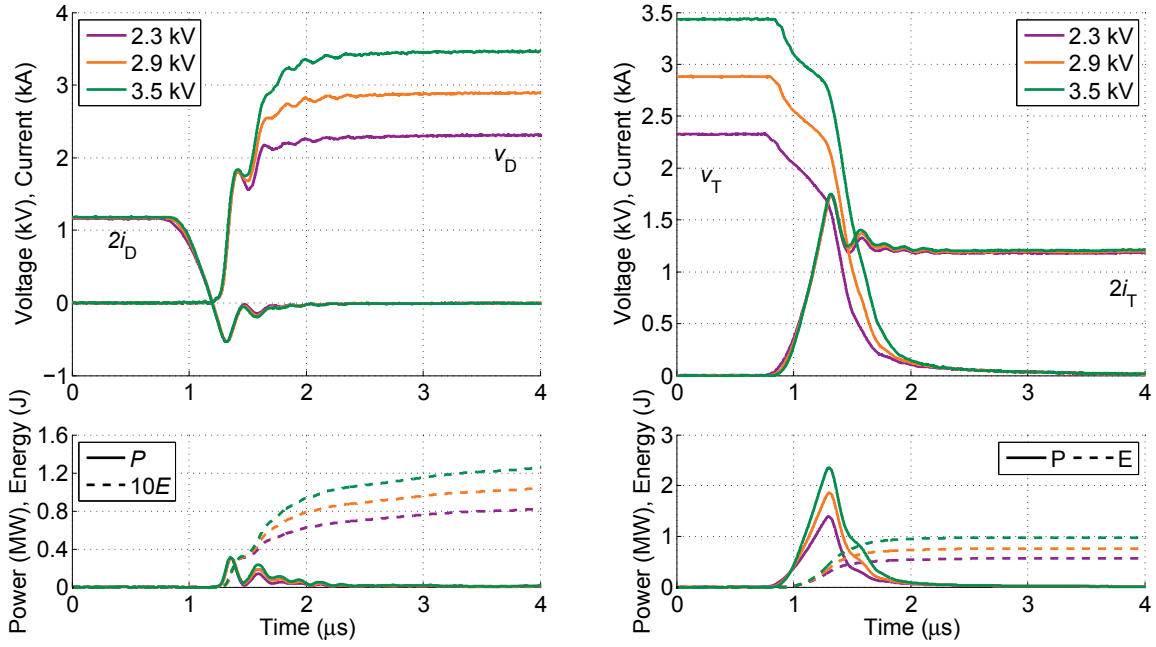
$$P_{cond} = V_F I_F = 3.8\,\text{V} \times 600\,\text{A} = 2.3\,\text{kW}. \tag{3.5}$$

With C_s = 15 nF and a switching frequency of 800 Hz, the extra losses during turn-off and turn-on due to the snubber circuit amount to only 150 W, less than 7% of P_{cond}.

The influence of the dc-link voltage V_{dc} variation in the diode turn-off and IGBT turn-on transients can be seen in Fig. 3.18. The *di/dt* increases slightly with higher commutation voltages. As expected, losses increase proportionally to the applied voltage, see Fig. 3.19. Even though the losses in the SiC diode module increase with higher voltages, they remain low in absolute terms (<200 mJ).

The last parameter studied was the junction temperature ϑ_j, see Fig. 3.20. The diode turn-off losses are slightly higher when changing from 25 to 75 °C (+17%), but increase considerably when going from 75 to 125 °C (+30%). The source of this can be appreciated in the waveforms, where the reverse recovery maximum and duration become larger at higher temperatures due to the increase in carrier density because of thermal generation in the drift zone. However, the losses in the SiC diode do not reach values higher than 250 mJ. Without the *RC* snubber, the device showed a weaker ringing at high temperature; for this issue refer to Sec. 3.6.

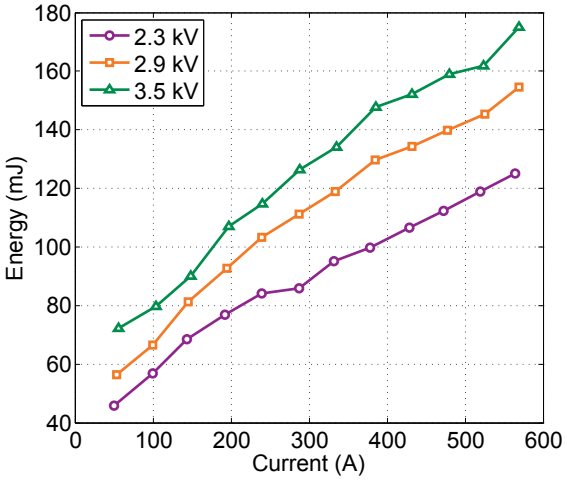
In the case of the IGBT, the changes in the reverse recovery behaviour of the diode do not considerably affect the commutation losses, these only increase by 18% from 25 to 125 °C.



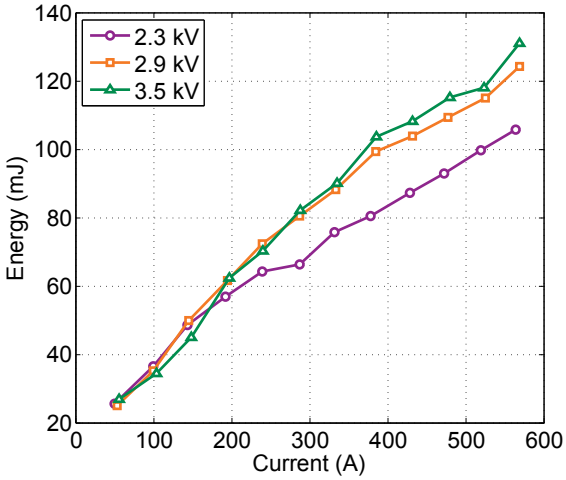
(a) Diode turn-off transient

(b) IGBT turn-on transient

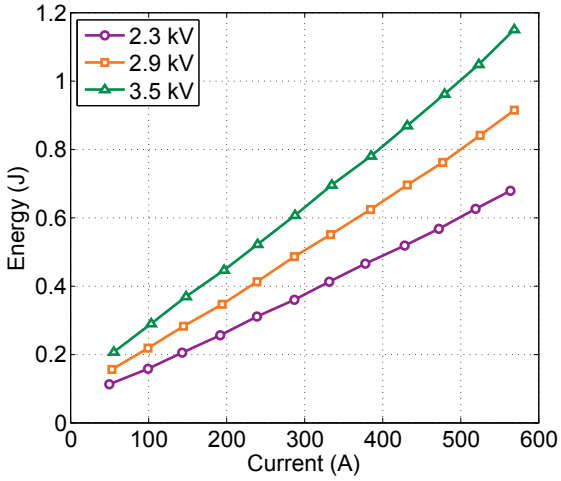
Figure 3.18: Commutation waveforms for different V_{dc} values (2.3...2.5 kA/µs, ϑ_j = 25 °C, I_L = 600 A, C_s = 9.4 nF, R_s = 4.7 Ω).



(a) Diode and *RC* snubber turn-off losses

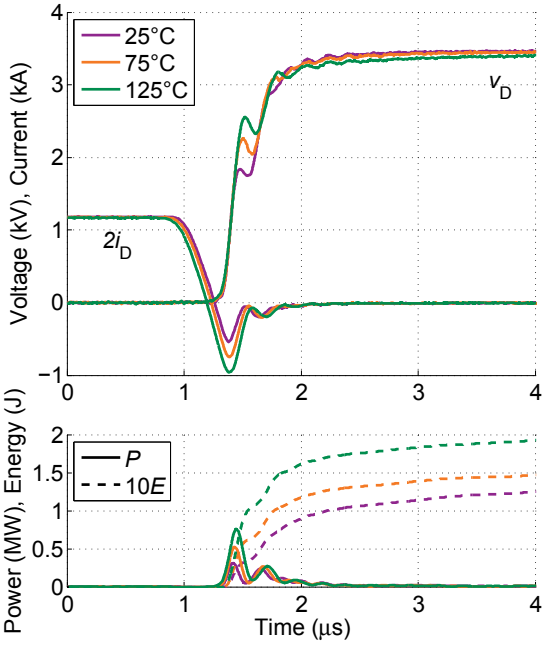


(b) Diode turn-off losses

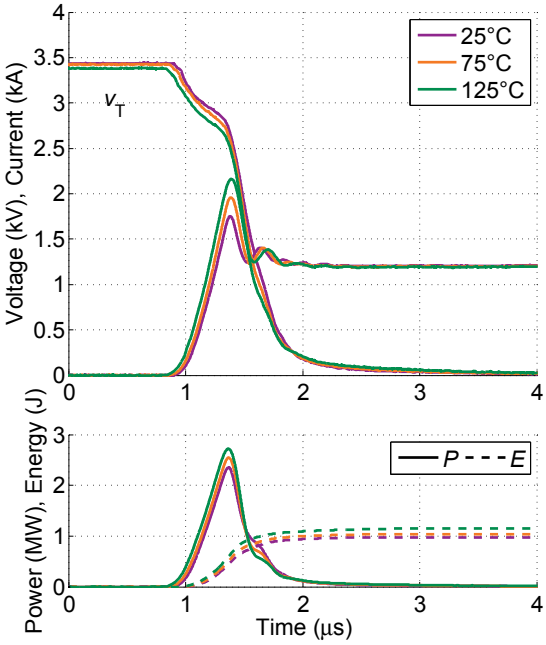


(c) IGBT turn-on losses

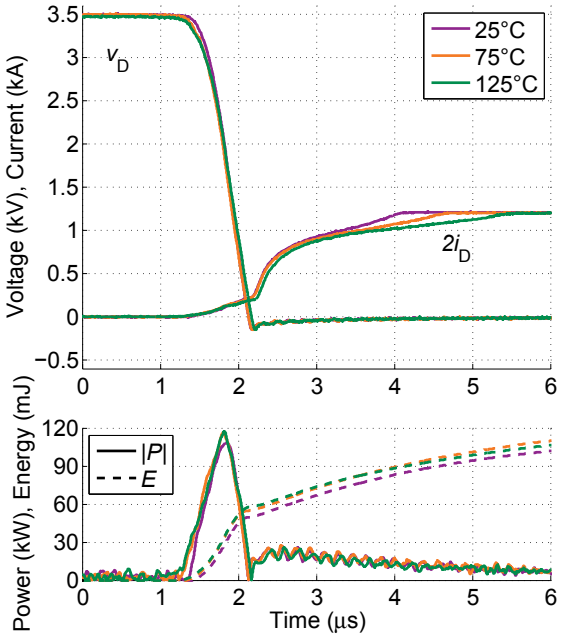
Figure 3.19: Switching losses for for different V_{dc} values (*di/dt2*, ϑ_j = 125 °C, I_L = 50...600 A, C_s = 9.4 nF, R_s = 4.7 Ω).



(a) Diode turn-off transient

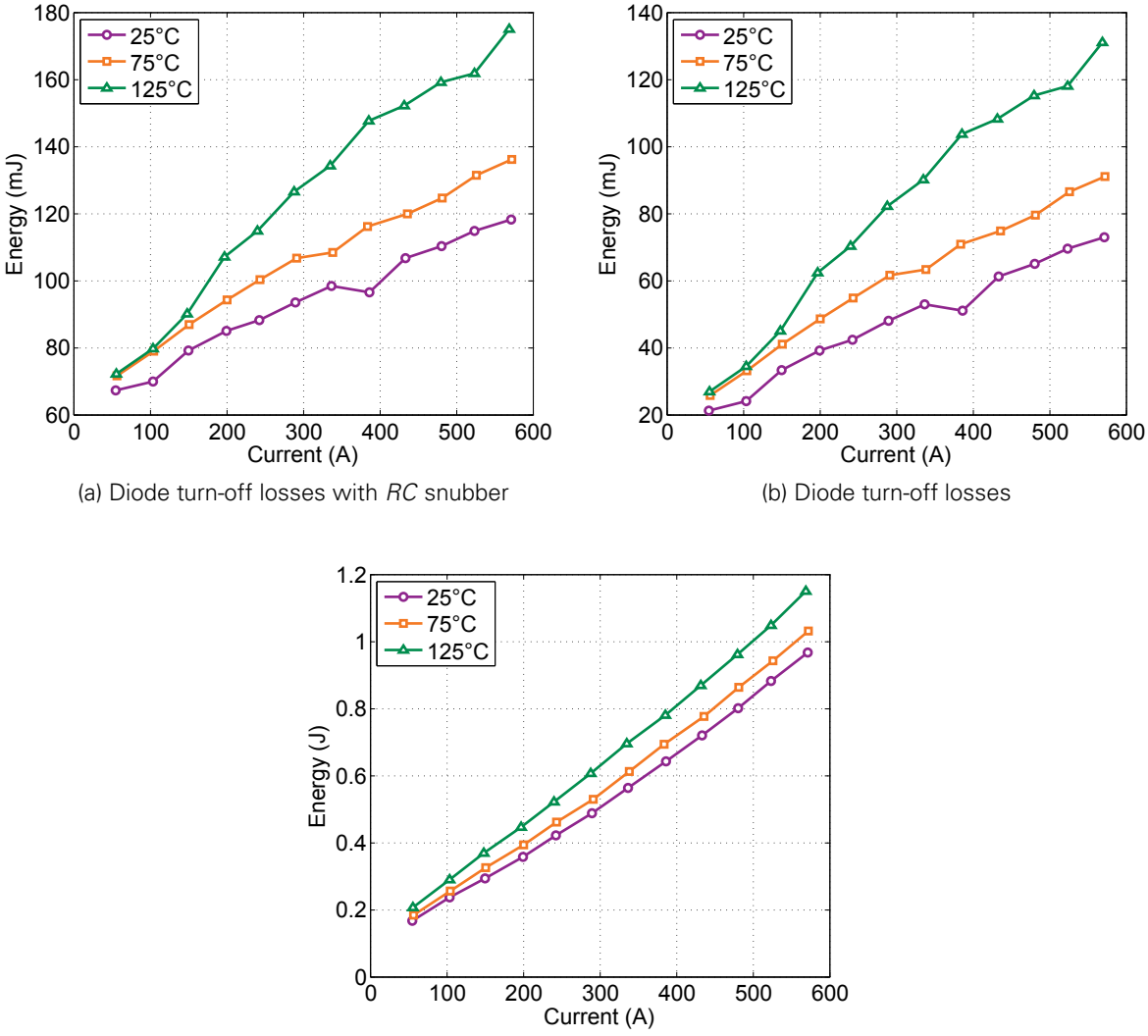


(b) IGBT turn-on transient



(c) Diode turn-on transient

Figure 3.20: Commutation waveforms for different ϑ_j values (2.5...2.7 kA/µs, V_{dc} = 3.5 kV, I_L = 600 A, C_s = 9.4 nF, R_s = 4.7 Ω).



(a) Diode turn-off losses with *RC* snubber

(b) Diode turn-off losses

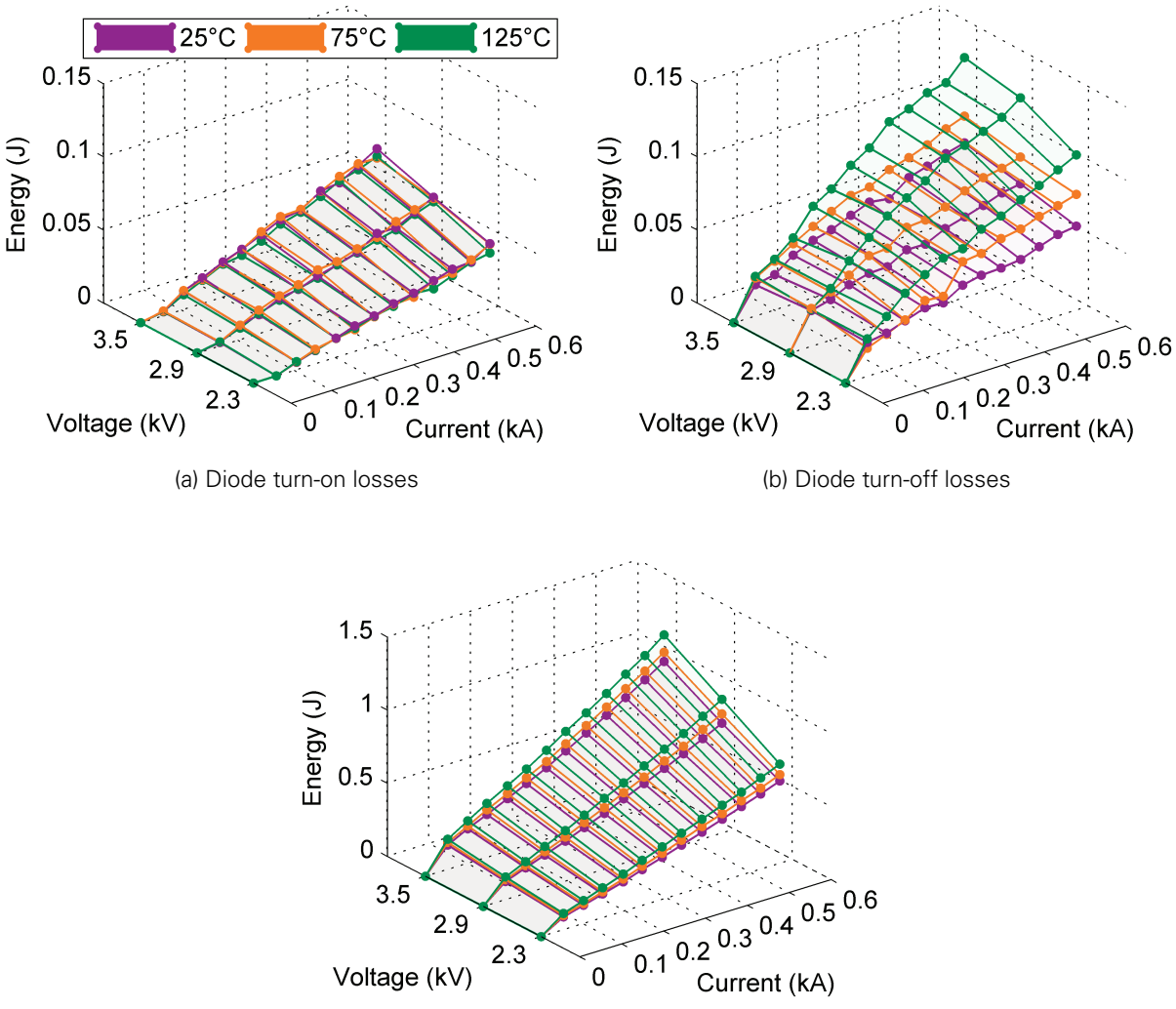
(c) IGBT turn-on losses

Figure 3.21: Switching losses for for different ϑ_j values (V_{dc} = 3.5 kV, *di/dt2*, I_L = 50...600 A, C_s = 9.4 nF, R_s = 4.7 Ω).

The slightly higher *di/dt* at higher temperatures can be noticed by the lower device voltage v_T during the current rise time for ϑ_j = 125 °C (2.5...2.7 kA/µs) , Fig. 3.20b. A summary of the switching losses for the three analysed junction temperatures can be found in Fig. 3.21.

Usually, the turn-on behaviour in Si diodes is not regarded as critical, since stress and losses in the semiconductor are considerably lower than during turn-off. For power loss calculations they are usually left out. In the case of this SiC diode, the turn-on losses are also negligible, with a forward recovery voltage under 150 V. Due to this low value, turn on losses remain under 120 mJ for nominal current, out of which 60 mJ are attributed to the energy in C_s, see Fig. 3.20c. The low value of the forward recovery has also a positive effect by diminishing the voltage stress on the IGBT during turn-off, which has to bear the overvoltage caused by the stray inductance L_σ and the forward recovery voltage simultaneously.

Fig. 3.22 presents a summary of the turn-on and turn-off switching losses in the SiC diode itself (without E_{Cs}) for *di/dt2* in the three tested ϑ_j values. It can be appreciated that the turn-on losses are temperature independent and not higher than 75 mJ. In the case of the turn-off losses, these increase with the temperature, but remain low (< 150 mJ). The losses of the IGBT during turn-on, which are also affected by the diode reverse recovery behaviour are included in Fig. 3.22c. Since the temperature dependency of the diode is low, the losses in the IGBT do not vary much over the temperature range. These losses are considerably higher than the diode switching losses, which is a critical aspect in limiting the converter output power, refer to Chap. 4 for a detailed analysis of this issue.



(a) Diode turn-on losses

(b) Diode turn-off losses

(c) IGBT turn-on losses

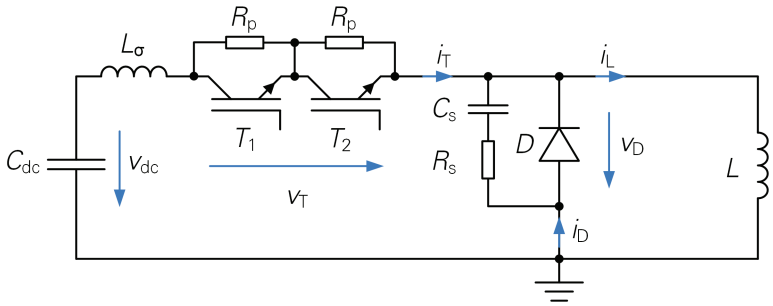
Figure 3.22: Summary of diode and IGBT switching losses, diode losses do not include the losses of the *RC* snubber (half diode module, *di/dt2*, C_s = 9.4 nF, R_s = 4.7 Ω).

3.4.3 SWITCHING BEHAVIOUR WITH TWO 3.3-KV IGBTS IN SERIES

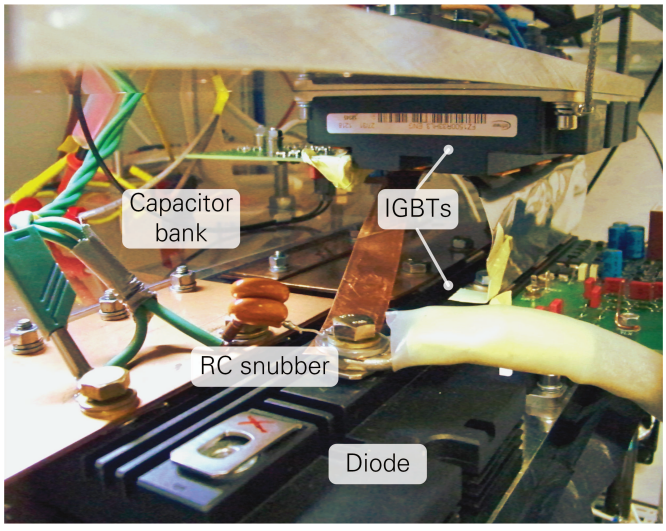
Industrial converters based on IGBT modules with an output voltage of 4.16 kV using a 3L-NPC topology can be designed with 6.5-kV devices or two series-connected 3.3-kV devices. For output currents of about 1 kA, the 3.3-kV series instead of the 6.5-kV parallel connection is preferred, due to the higher performance and lower cost of 3.3-kV devices [2]. For this reason, it is of interest to investigate the switching performance of the SiC diode within this configuration.

The test circuit used for the characterization is basically the same as in Fig. 3.12, but with two IGBTs instead of one, see Fig. 3.23. The stray inductance L_σ of the commutation circuit was kept under 255 nH, which translates into an increase of approximately 30...40 nH compared to the single 6.5-kV switch configuration. As Fig. 3.23b shows, both IGBTs were positioned facing each other. The IGBT modules correspond to the type FZ1500R33HL3, refer to Sec. 3.2.1 for details. An analogue GDU was used to switch the IGBT, instead of the digital one used for the characterization with a 6.5-kV IGBT. Equal static voltage distribution was achieved with additional resistors R_p connected to the collector-emitter terminals of each IGBT. As in the measurements performed with the 6.5-kV IGBT, only one half of the SiC diode module was connected.

An *RC* snubber connected close to the diode was included. The effect of it can be appreciated in Fig. 3.24. This figure shows the voltage and current waveforms for the diode turn-off transient with and without *RC* snubber at 25 °C. The oscillations are almost completely dampened by



(a)



(b)

Figure 3.23: Test circuit for the investigation of the switching behaviour of the SiC diode *(D)* with two 3.3-kV IGBTs *(T_1, T_2)* in series: (a) schematic drawing and (b) photo. (C_{dc} = 2 mF, C_s = 9.4 nF, R_s = 4.7 Ω, R_p = 47 kΩ)

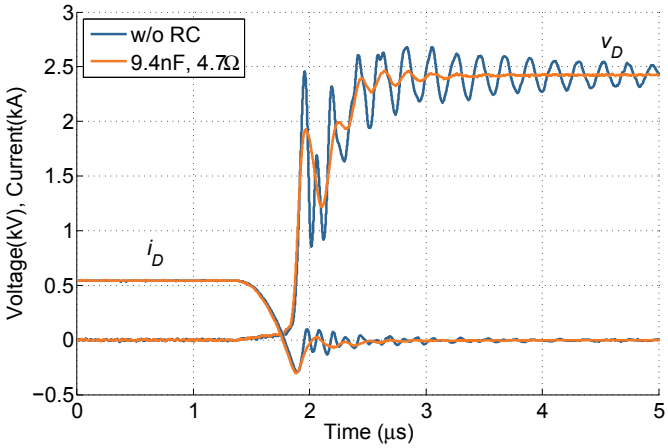


Figure 3.24: Commutation waveforms of the SiC diode module (half) with series-connected IGBTs with and without *RC* snubber (V_{dc} = 2.45 kV, ϑ_j = 25 °C, 2.5 kA/µs, I_D = 540 A, R_s = 4.7 Ω, C_s = 9.4 nF).

the snubber circuit. However, the first voltage overshoot due to the diode reverse recovery behaviour remains present, although at a lower amplitude below the dc-link voltage value. The measurements carried out in this section were done with an *RC* snubber of 9.4 nF and 4.7 Ω connected to the diode terminals, see Fig. 3.23b.

The diode switching behaviour was tested with two different current change rates. These and the corresponding *dv/dt* average and peak values are plotted for a dc-link voltage V_{dc} of 3.5 kV and 125 °C in Fig. 3.25. The current change rate *di/dt2* is only around 10% higher due to limitations in the GDU, which is not able to increase the switching speed beyond that. The current change rate *di/dt1* corresponds to $R_{g,on}$ = 0.5 Ω and is also the same *di/dt* used with Si diodes. For *di/dt2* a resistance of 0.25 Ω was used. The peak di_{rr}/dt, see Fig. 3.25, approximately doubles the average *di/dt*, more than the 50% observed in the the single 6.5-kV IGBT case. This higher value affects the intensity of the oscillations, compare to Fig. 3.14. Regarding the *dv/dt*, the average and peak values are in the range of the ones observed in the past section with the 6.5-kV IGBT.

The commutation waveforms for the diode turn-off and the IGBT turn-on transients (series-connection) and two current change rates (2.9 and 3.2 kA/µs) can be found in Fig. 3.26. Compared to the results with a single 6.5-kV IGBT, Fig. 3.15, the current and voltage waveforms are very similar. The associated switching losses are 0.21 and 0.24 J for the diode turn-off, 1.14 and 1.03 J for the IGBT turn-on. It is clear that the *di/dt* increase has little influence on the switching losses of the diode, but for the IGBT, an increase in the *di/dt* of 10% is translated into a turn-on loss reduction of roughly 10%. The price for this reduction is a higher *dv/dt* during commutation, see Fig. 3.25 (c) and (d). A summary of the switching losses can be found in Fig. 3.27. Compared to the losses of the single IGBT, Fig. 3.16, both are in a similar range.

The waveforms that show the effect of junction temperature ϑ_j variation can be found in Fig. 3.28. Contrary to effects seen with the 6.5-kV IGBT, where the temperature does not influence the intensity of the oscillations, but mainly the reverse recovery peak and duration, see Fig. 3.20, here the di_{rr}/dt increases with the temperature from 4.24 kA/µs at 25 °C to 6.10 kA/µs at 125 °C (+44%). Consequently, the amplitude of the first voltage spike in the diode also increases, but does not surpass the dc-link voltage value. The variation of the losses is marginal in the IGBT (<2%), as they are mostly affected by the higher reverse recovery current, which is relatively small in SiC diodes. In the case of the diode, the turn-off losses increase by 60 mJ if the junction temperature increases from 25 to 125 °C, but they remain under 250 mJ.

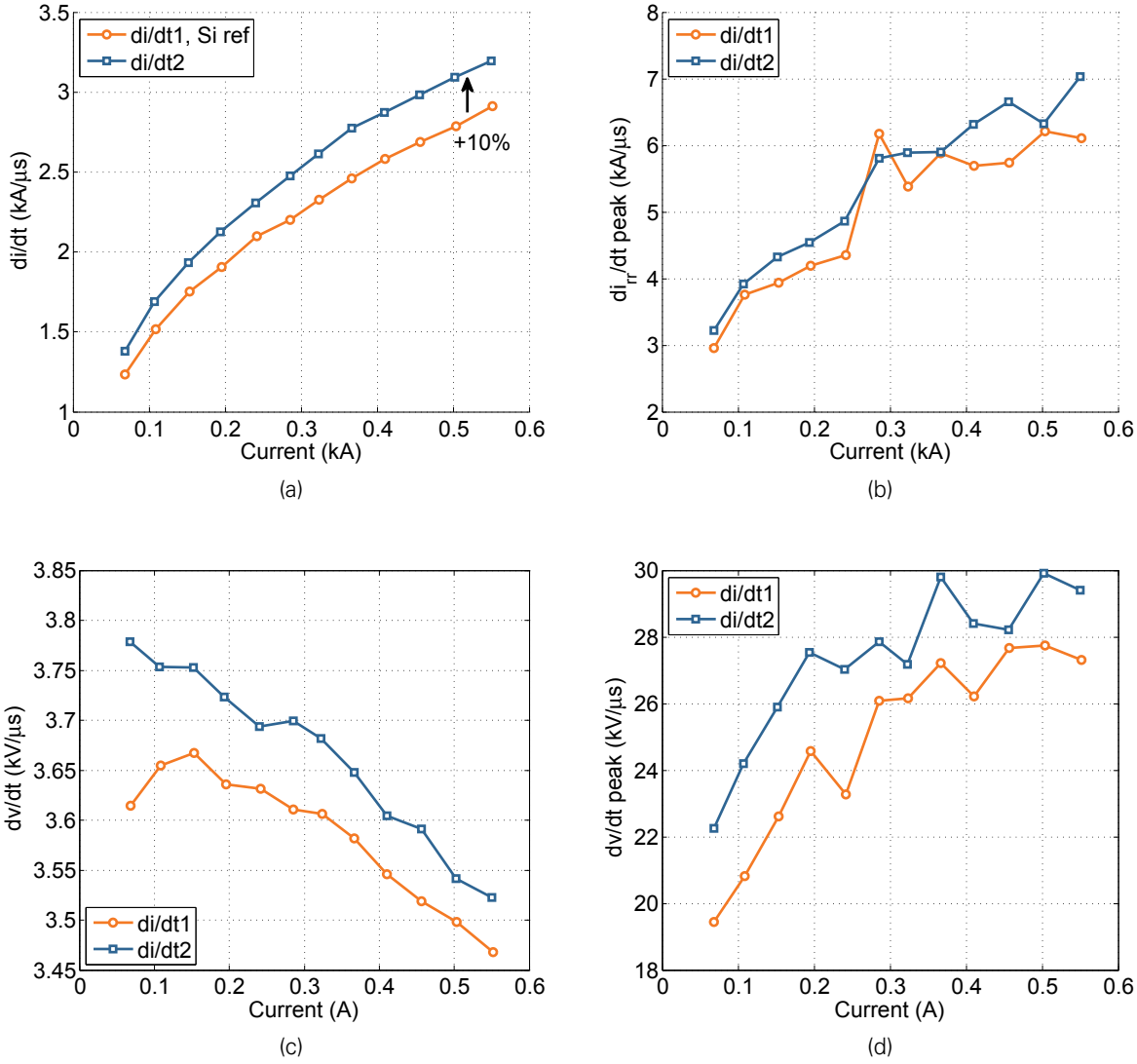
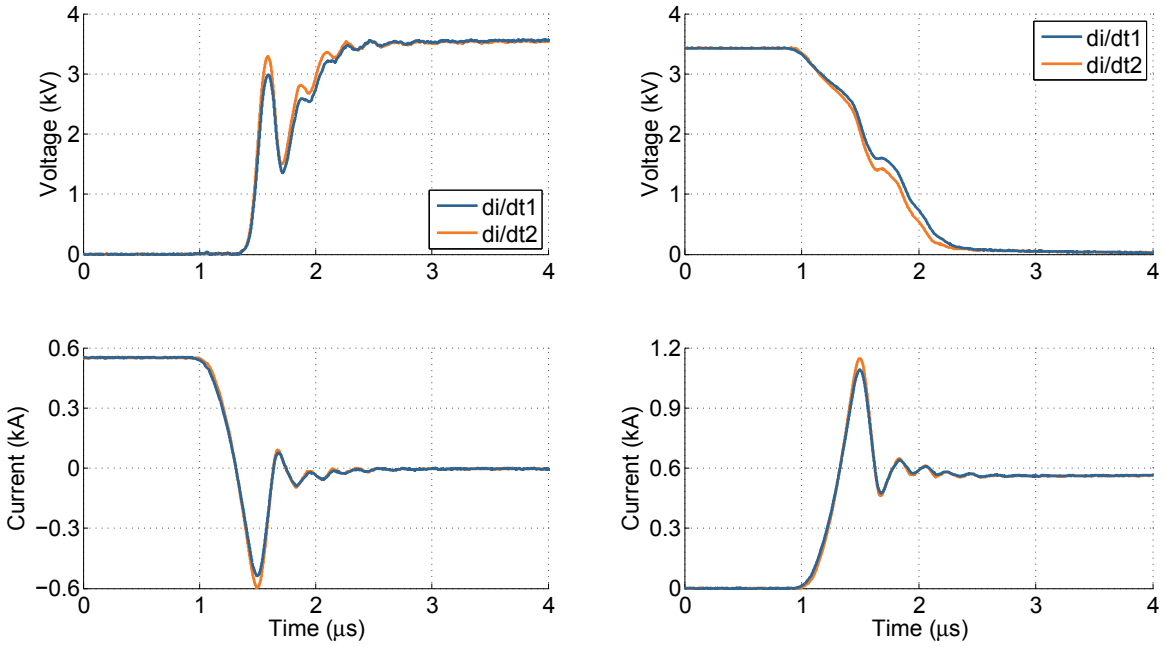
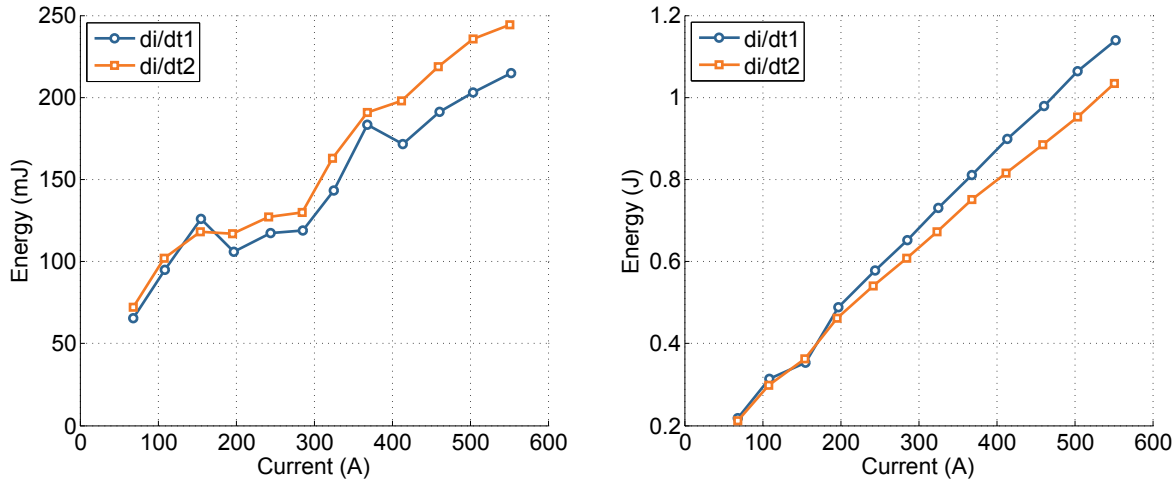


Figure 3.25: Current and voltage change rates during diode turn-off, (a) *di/dt* (50% of I_{rrm} and 50% of I_D), (b) peak reverse recovery di_{rr}/dt , (c) *dv/dt* (20% and 95%) and (d) peak *dv/dt* (V_{dc} = 3.5 kV, ϑ_j = 125 °C).



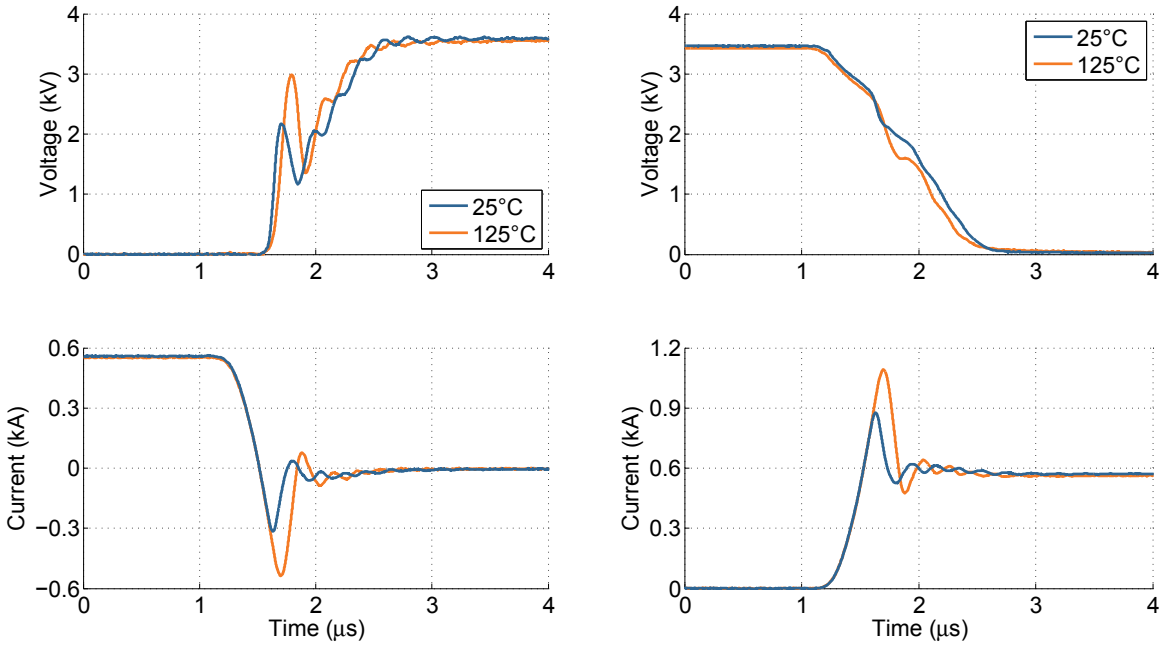
(a) Diode turn-off (b) IGBT turn-on

Figure 3.26: Commutation waveforms for different current change rates *di/dt*, diode with IGBT series connection (*di/dt* = 2.9, 3.2 kA/µs, V_{dc} = 3.5 kV, I_L = 550 A, ϑ_j = 125 °C, C_s = 9.4 nF, R_s = 4.7 Ω).



(a) Diode and *RC* snubber turn-off (b) IGBT turn-on

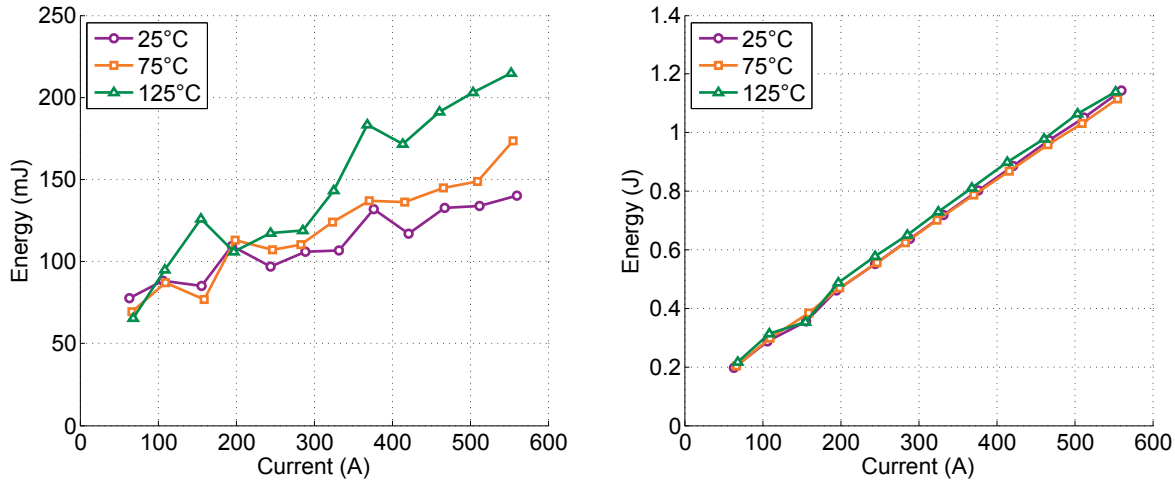
Figure 3.27: Switching losses for different *di/dt* values, diode with series-connected IGBTs (ϑ_j = 125 °C, V_{dc} = 3.5 kV, I_L = 50...550 A, C_s = 9.4 nF, R_s = 4.7 Ω).



(a) Diode and *RC* snubber turn-off losses

(b) IGBT turn-on losses

Figure 3.28: Commutation waveforms for different ϑ_j values, diode with series-connected IGBTs (ϑ_j = 25, 125 °C, *di/dt* = 2.8, 2.9 kA/µs, V_{dc} = 3.5 kV, I_L = 550 A).



(a) Diode turn-off

(b) IGBT turn-on

Figure 3.29: Switching losses for different ϑ_j values, diode with series-connected IGBTs (ϑ_j = 25, 75, 125 °C, *di/dt1*, V_{dc} = 3.5 kV, I_L = 50...550 A).

3.5 COMPARISON WITH 6.5-KV SILICON DIODE

In order to evaluate the SiC diode module a comparison with an equivalent Si counterpart is desirable. For this purpose the diode DD600S65K1 from Infineon was chosen [111]. It consists of a 6.5-kV Si diode module with dimensions of $130 \times 140 \times 48\,\mathrm{mm}^3$. The nominal values of the diode module are comparable to those of the SiC diode prototype: 6.5 kV, 2×500 A (SiC) vs. 6.5 kV, 2×600 A (Si). Both SiC and Si diode modules consist of two diode systems that can be used independently or interconnected, which means that the Si diode full module can handle currents of 1.2 kA when both diodes are connected in parallel.

The module contains 24 Si chips with an active area of $84.6\,\mathrm{mm}^2$ each, totalling an active area of $20.3\,\mathrm{cm}^2$ per module. Even though the size of both diode modules is the same, the difference in the active area has a ratio of 1:4 (SiC: $5.7\,\mathrm{cm}^2$). This affects the performance of the SiC diode negatively, especially when considering heat dissipation, but it also reflects the current development stage of SiC devices, where the die size is limited by wafer defects, see Sec. 2.1.3. Also, SiC semiconductor devices can work at higher current densities than Si devices. The information regarding the modules is summarized in Table 3.3.

3.5.1 DIODE CURRENT RATING CALCULATION

As mentioned before, the SiC diode has a current rating of 1000 A. This value was first used in the publication [108] and has been adopted for this work, as both modules are identical. By the time that paper was published, no accurate thermal characterization of the module had been carried out. This is no longer so, and as listed in Table 3.3, the thermal resistances of the module have been calculated with the help of finite element method (FEM) analysis.

The maximum permissible diode forward current I_F operating at $\vartheta_\mathrm{j,max}$ attached to a heat sink with a temperature ϑ_h can be calculated with following equation [119]:

$$I_\mathrm{F}(\vartheta_\mathrm{j,max}) = \frac{\vartheta_\mathrm{j,max} - \vartheta_\mathrm{h}}{(R_\mathrm{th,jc} + R_\mathrm{th,ch}) \cdot V_\mathrm{F}(I_\mathrm{D}, \vartheta_\mathrm{j,max})} \tag{3.6}$$

with a maximum junction temperature $\vartheta_\mathrm{j,max}$ of 125 °C. Even though the diode current $I_\mathrm{F}(\vartheta_\mathrm{j,max})$ is unknown and the on-state voltage V_F depends on its value, it is possible to find I_F by iteration. The results of (3.6) for the SiC and Si diode modules is shown in Fig. 3.30. These indicate that the heat sink temperature ϑ_h considered for the Si diode is slightly higher than 30 °C. At the same temperature, the SiC diode can only handle a current of 930 A. The initial estimation of 1 kA as the current rating for the SiC module is only possible with a heat sink temperature ϑ_h of 23 °C.

Table 3.3: SiC and Si diode module parameters

Type / model	SiC prototype	Si DD600S65K1
Voltage (V)	6500	6500
Nominal dc current (A)	1000	1200
Max. dc current ϑ_h = 30 °C (A)	944	1214
Module size (mm^3)	130×140×48	130×140×48
Number of dies	80	24
Die active area (mm^2)	7.1	84.6
Module active area (cm^2)	5.7	20.3
$R_\mathrm{th,jc}$ (K/kW)	13.9	10.5
$R_\mathrm{th,ch}$ (K/kW)	9.9	8.0

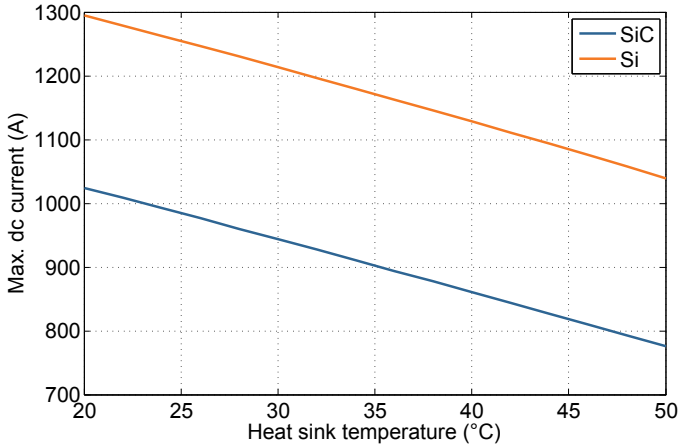


Figure 3.30: Calculation of the diode current rating (continuous) at different heat sink temperatures for the SiC and Si diode modules.

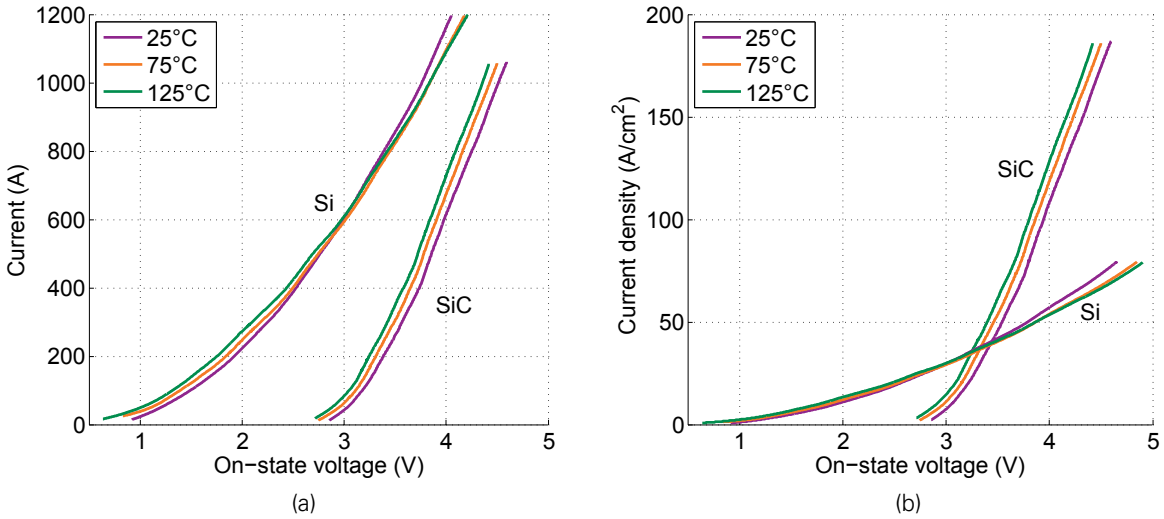


Figure 3.31: Diode on-state voltage at 25, 75 and 125 °C, Si: diode DD600S65K1 (full module), SiC: SiC diode, 80 chips in parallel. (a) Module current, (b) current density.

3.5.2 STATIC BEHAVIOUR

Figure 3.31 shows the measured forward characteristic for the SiC diode as well as for the Si diode DD600S65K1 at temperatures of 25, 75 and 125 °C. The forward voltage at 600 A and 25 °C is 2.99 V for the Si diode and 3.98 V for the SiC diode. At 125 °C the Si diode has an on-state voltage of 2.98 V and the SiC diode 3.84 V.

The Si diode shows a positive temperature coefficient for high currents, which is favourable for the thermal stability of parallel connected chips. On the other side, the SiC diode exhibits a negative temperature coefficient of approximately −1.4 mV/K, but this is not high enough to produce thermal instability, refer to Sec. 3.3 for details.

As the results indicate, the on-state voltage of SiC diodes is still high when compared with the Si counterpart, roughly 1 V more for currents over 600 A, see Fig. 3.31. This is mainly due to the higher threshold voltage in SiC diodes and the higher current density at which the SiC diode module is operated. However, when considering the current density, the advantages of SiC as material become clear. For an on-state voltage of 4 V the SiC diode can handle an about two

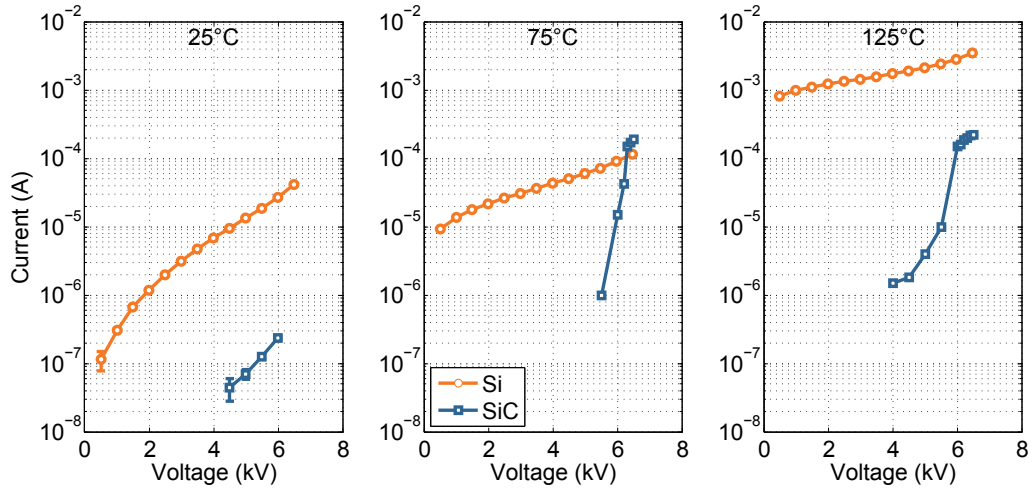


Figure 3.32: Reverse blocking characteristic at 25, 75 and 125 °C. Si: diode DD600S65K1 (full module), SiC: SiC diode (full module, 80 chips in parallel). Error bars included for the Si diode characteristics at all temperatures and for the SiC diode only at 25 °C, 99.7% confidence.

times larger current density. Instead of the typical current densities of 50 to 75 A/cm^2 at which Si diodes are usually operated, 6.5-kV SiC diodes can operate at densities close to 200 A/cm^2.

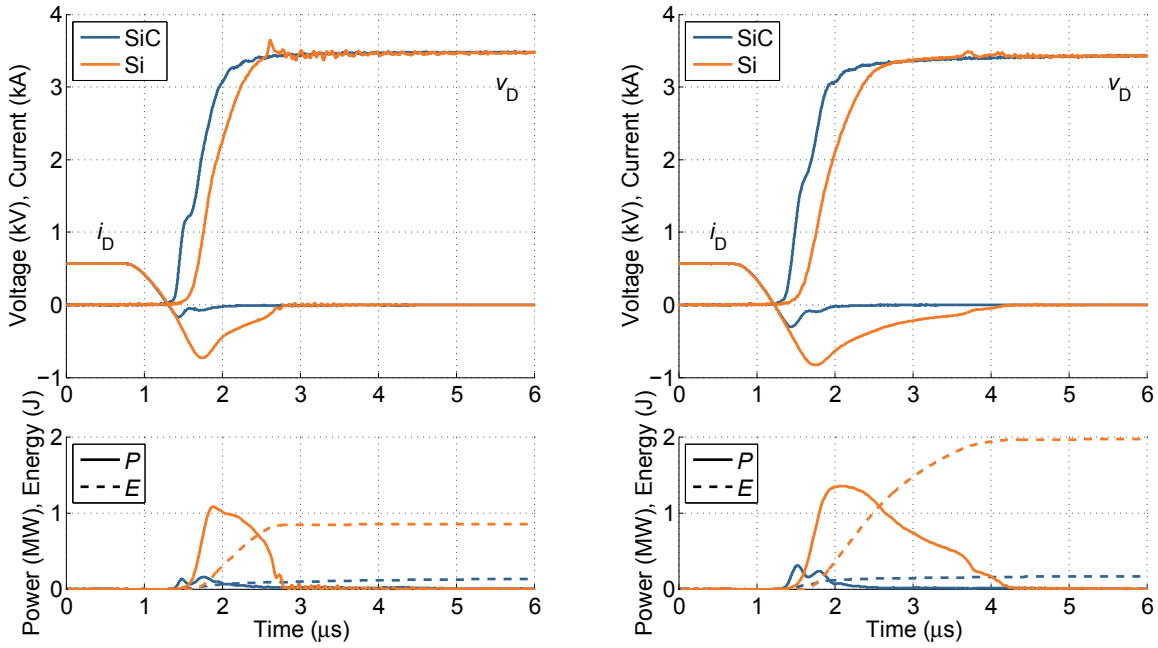
The reverse blocking characteristic at 25, 75 and 125 °C can be seen in Fig. 3.32. As expected, the leakage current of the Si diode presents a strong dependency on the junction temperature, increasing in 3 orders of magnitude for the measured temperature range, with currents close to 4 mA at 125 °C and 6.5 kV. The SiC diode has higher currents for 75 and 125 °C compared to 25 °C, but these stay under 300 µA and stay more or less at the same level.

3.5.3 SWITCHING BEHAVIOUR

The switching behaviour of the SiC and Si diodes with a 6.5-kV IGBT FZ600R65KF2 was investigated. The diode turn-on and turn-off, as well as the IGBT turn-on transients are of interest for the diode characterization. Both pairs (IGBT + SiC diode and IGBT + Si diode) were tested under identical conditions, including e.g. equal GDU, dc-link voltage, junction temperature and stray inductance, see Sec. 3.2.1 for details.

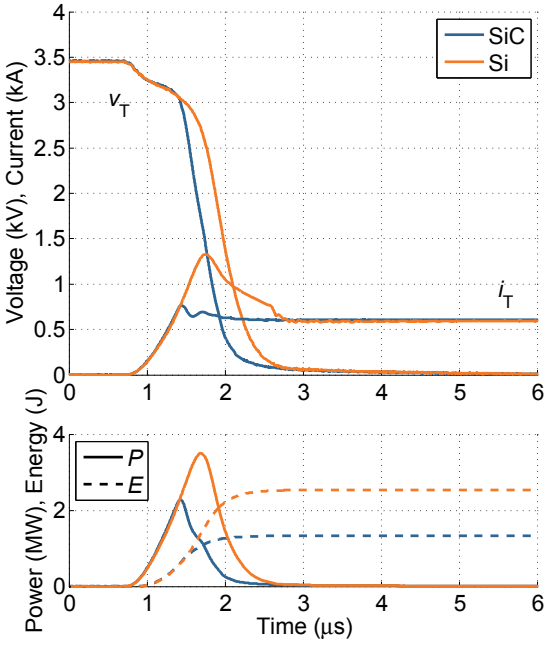
Figs. 3.33 and 3.34 show the commutation transient waveforms at 3.5 kV and 600 A for ϑ_j = 25 and 125 °C, with a *di/dt* of approximately 1.5 kA/µs. Figs. 3.33 (a) and (b) present the diode turn-off transient. As commented before, the SiC diode has a small reverse recovery current and the recovery process itself is less than 1 µs long, which drastically reduces the losses. The Si diode presents a high reverse recovery current maximum and a duration close to 3 µs at 125 °C. The losses caused by this are accordingly high (0.9 J at ϑ_j = 25 °C and 2.0 J at ϑ_j = 125 °C). A slight current snap-off can be observed in the Si diode at the end of the reverse recovery process. However, this does not cause any dangerous overvoltage. Figs. 3.33 (c) and (d) present the IGBT turn-on transient. The reduction of the reverse recovery current peak reduces also the stress and losses of the IGBT during the turn-on transient. At 125 °C the peak current was reduced from 1.4 to 0.9 kA and the IGBT turn-on losses from 3.2 J to 1.6 J, when considering a SiC instead of a Si diode.

Fig. 3.34 focuses on the diode turn-on transient. The SiC diode is not influenced by the variation of the junction temperature, whereas the Si diode presents a considerably high forward recovery peak of 435 V at ϑ_j = 125 °C. This leads to turn-on losses of about 200 mJ in the Si diode, compared to the relatively constant losses in the SiC diode under 100 mJ. It is noteworthy

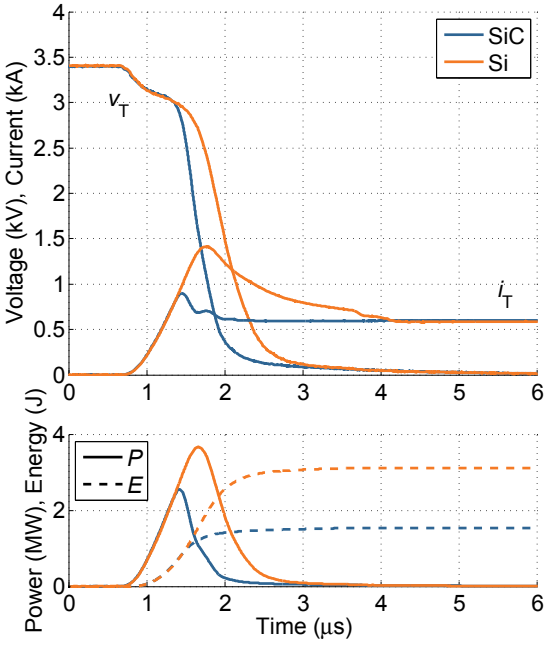


(a) Diode turn-off at ϑ_j = 25 °C

(b) Diode turn-off at ϑ_j = 125 °C



(c) IGBT turn-on at ϑ_j = 25 °C

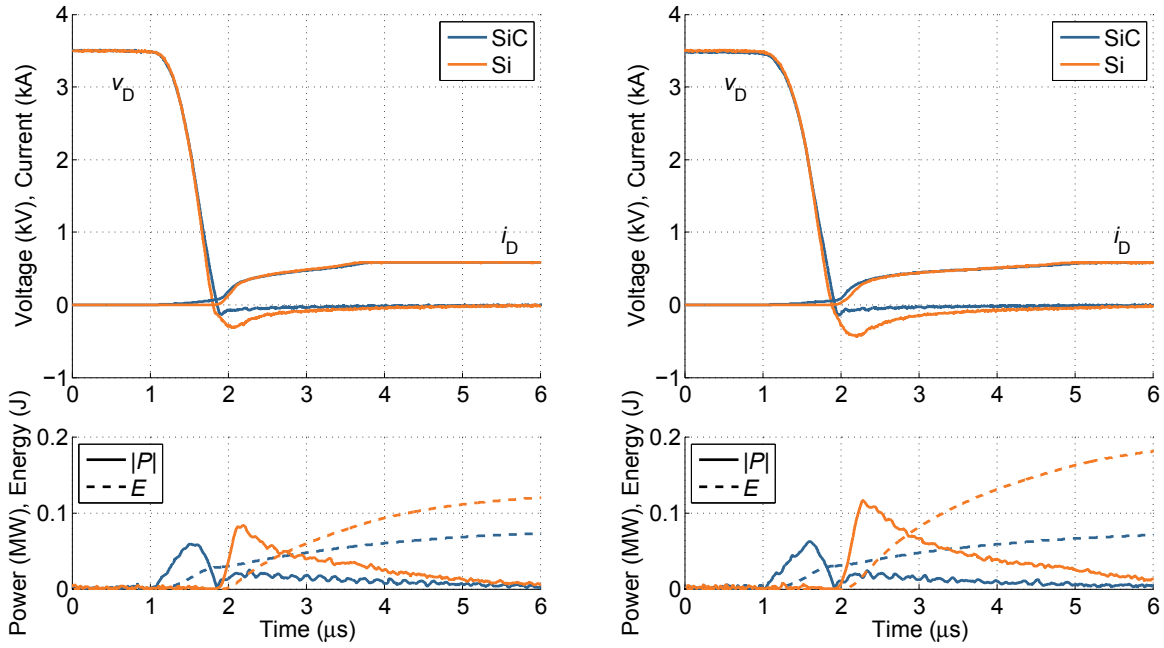


(d) IGBT turn-on at ϑ_j = 125 °C

Figure 3.33: Commutation waveforms for Si and SiC diode turn-off and IGBT turn-on (V_{dc} = 3.5 kV, I_L = 600 A, di/dt = 1.5 kA/µs at ϑ_j = 25 °C and 1.6 kA/µs at 125 °C, IGBT FZ600R65KF2 and Si diode DD600S65K1).

that the turn-on losses of SiC diodes are comparable to the turn-off losses and their contribution to the overall diode losses is marginal.

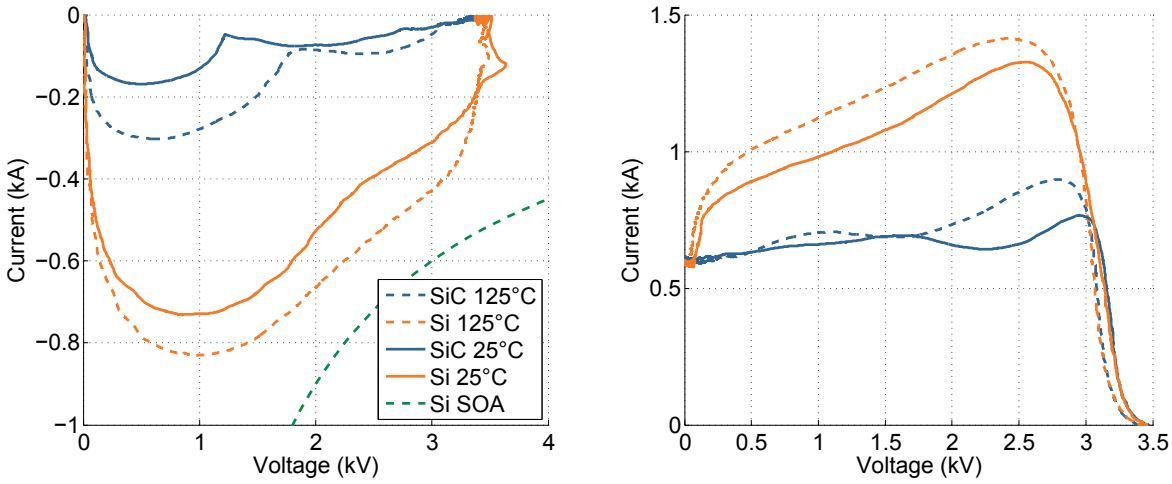
The waveforms for the diode turn-off and IGBT turn-on transients in the V-I plane are presen-



(a) Diode turn-on at ϑ_j = 25 °C

(b) Diode turn-on at ϑ_j = 125 °C

Figure 3.34: Commutation waveforms for Si and SiC diode turn-on (V_{dc} = 3.5 kV, I_L = 600 A, IGBT FZ600R65KF2 and Si diode DD600S65K1, SiC diode with *RC* snubber).

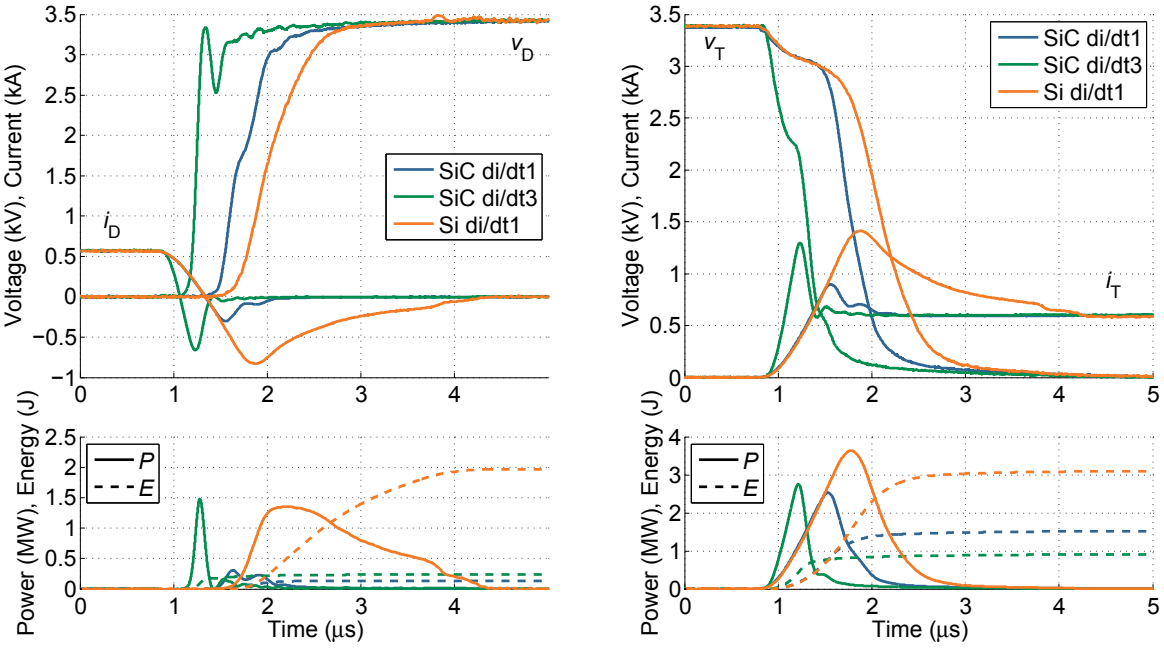


(a) Diode turn-off

(b) IGBT turn-on

Figure 3.35: V-I plane traces for Si and SiC diode turn-off and IGBT turn-on (V_{dc} = 3.5 kV, I_L = 600 A, *di/dt* = 1.5 kA/µs at ϑ_j = 25 °C and 1.6 kA/µs at 125 °C, IGBT FZ600R65KF2 and Si diode DD600S65K1, SiC diode with *RC* snubber).

ted in Fig. 3.35. With this diagram it is easier to visualize the voltage and current stress in each device configuration and also if the commutation is inside the RRSOA of the device or not. In the case of the Si diode, the limit is given by the maximum current of 1200 A, the maximum voltage of 6500 V and the power curve equal to 1.8 MW, which can be seen in the figure. Operation outside these limits can lead to failure of the device. The SiC diode commutation is far



(a) Diode turn-off

(b) IGBT turn-on

Figure 3.36: Commutation waveforms for Si and SiC diode turn-off and IGBT turn-on with increased *di/dt* (V_{dc} = 3.5 kV, I_L = 600 A, *di/dt1* = 1.6 kA/µs and, *di/dt3* = 4.8 kA/µs, ϑ_j = 125 °C, IGBT FZ600R65KF2 and Si diode DD600S65K1, SiC diode with *RC* snubber).

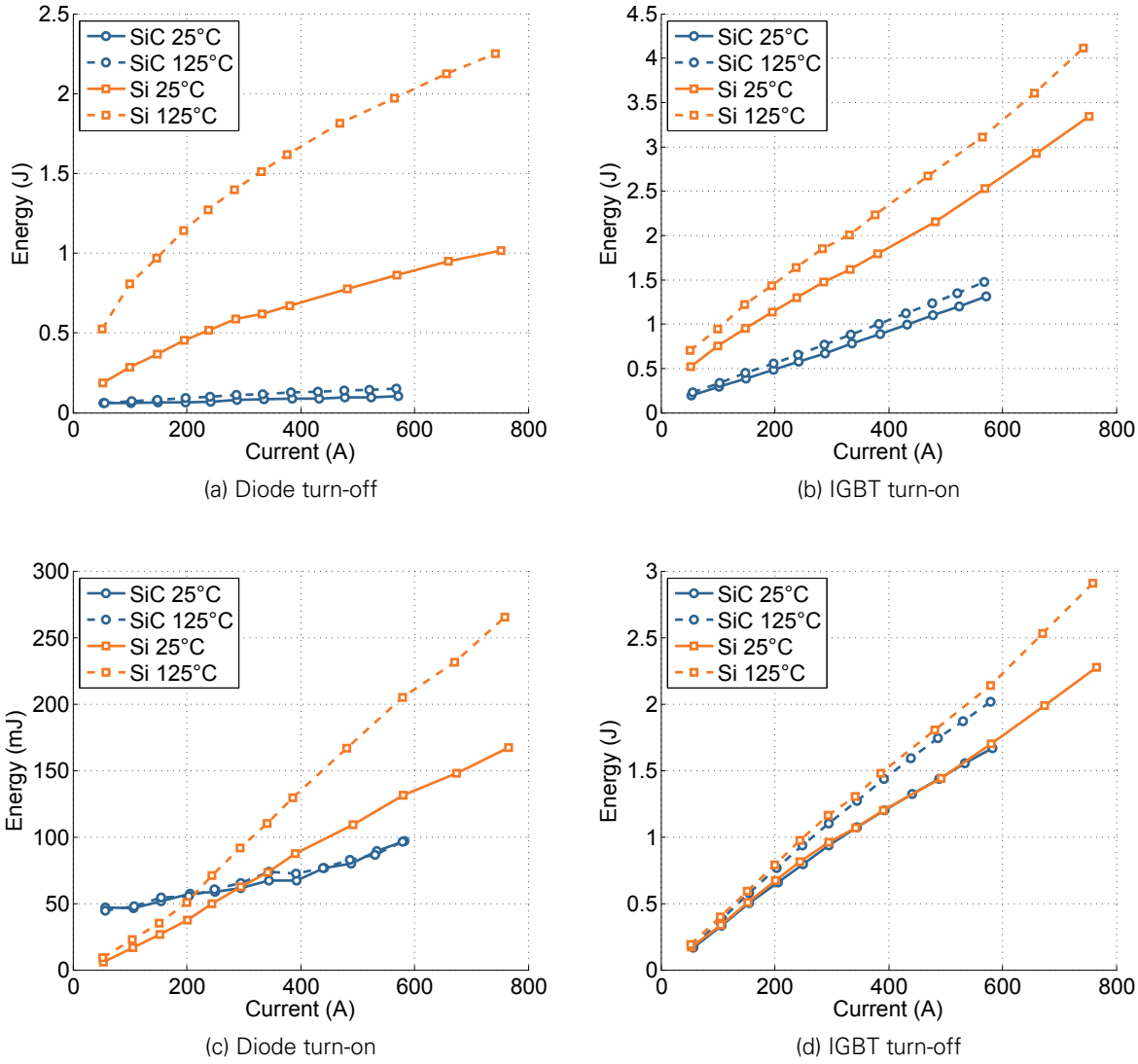
Table 3.4: Summary of switching losses for Si and SiC diodes at 3.5 kV, 600 A and equal turn-on current change rate (*di/dt1* = 1.6 kA/µs)

Diode	Silicon		Silicon carbide	
Temperature	25 °C	125 °C	25 °C	125 °C
$E_{on,diode}$ (J)	0.13	0.20	0.10	0.10
$E_{off,diode}$ (J)	0.86	1.97	0.10	0.15
$E_{on,IGBT}$ (J)	2.53	3.11	1.31	1.47
$E_{off,IGBT}$ (J)	1.70	2.14	1.71	2.06
$\sum E$ (J)	5.22	7.42	3.19	3.65

away from the 1.8-MW curve with only 0.3 MW peak power. Although the SOA limits for the SiC diode have not been specified yet, as not enough SiC module samples are available to make extensive reliability tests, it is known that the SOA in SiC devices is wider and they have a much larger overload capability, as some other research groups have already demonstrated [51, 124].

As shown in Sec. 3.4.2, it is possible to increase the *di/dt* during IGBT turn-on without endangering the devices. This way, lower losses in the IGBT can be achieved, as the measurements in Fig. 3.36 demonstrate. Here, the IGBT turn-on losses with Si diode amount to 3.1 J, which can be halved by using a SiC diode. Furthermore, if the *di/dt* is tripled, the losses are reduced to less than one third (0.9 J).

The commutation losses for both diode and IGBT were extracted from the measurements, the results can be seen in Fig. 3.37. Table 3.4 contains the comparison of Si and SiC diode switching losses operating at 3.5 kV and 600 A. The advantages of SiC technology regarding



(a) Diode turn-off

(b) IGBT turn-on

(c) Diode turn-on

(d) IGBT turn-off

Figure 3.37: Switching losses at V_{dc} = 3.5 kV and I_L = 50...800 A, IGBT FZ600R65KF2, Si diode DD600S65K1, SiC diode with *RC* snubber, *di/dt1*.

switching losses can clearly be seen. The influence of the junction temperature on the transient behaviour and losses of the SiC diode is reduced compared to the Si diode.

The turn-on losses for the SiC diode at 600 A and 125 °C (96 mJ) are only half of those of the Si diode (205 mJ). Compared to the SiC diode turn-off losses, the turn-on losses are in the same order of magnitude. The turn-off losses for the SiC diode at 600 A and 125 °C (106 mJ) are about 18 times smaller than those of the Si-diode (1.98 J). Correspondingly, the IGBT turn-on losses at 600 A and 125 °C with SiC diode are also reduced in about 50% (3.1 to 1.5 J). The IGBT turn-off losses are slightly lower (<5%) for the configuration with the SiC diode, due to the influence of the lower forward recovery of that diode.

3.5.4 SUMMARY

The SiC diode module prototype has been compared to a commercial Si diode. The forward characteristic of the SiC diode shows acceptable levels of on-state voltage, albeit higher than the Si counterpart (roughly 1 V), as expected in wide band gap devices. The reverse blocking properties of SiC, on the other hand, exhibit a very low leakage current and a satisfactory blocking

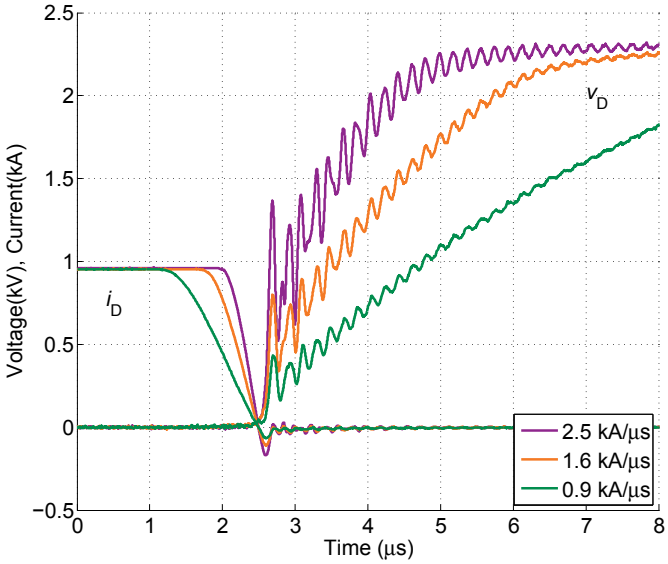


Figure 3.38: Oscillations during the diode turn-off transient for different *di/dt* values without *RC* snubber circuit (V_{dc} = 2.4 kV, I_D = 960 A, ϑ_j = 25 °C, $R_{g,on}$ = 2.3, 4.1, 8.2Ω, full SiC diode module)

capability. Leakage currents at the maximum temperature of 125 °C are in the microampere-range, compared to the milliamperes present in the Si diode. The SiC diode properties do not have such a strong temperature dependency as observed in Si diodes.

The switching behaviour of the SiC device offers marginal losses and a low device stress. Further reduction can be achieved by increasing the *di/dt* through the IGBT gate resistor, as the reverse recovery peak is not a limiting factor for the SiC diode under the studied configuration. The reduction of losses in the IGBT by the inclusion of a SiC freewheeling diode was also demonstrated, which amount to 50% for the turn-on transient at 125 °C. The reduction of semiconductor losses through the use of SiC devices will allow a higher output power for converters without increasing their size, or a reduction of the filter size for the case that a switching frequency increase is preferred; this topic is discussed in Chap. 4.

3.6 OSCILLATIONS IN THE SIC DIODE

As mentioned in the prior section, special care was taken for the dynamic characterization of the diode, as unwanted oscillations were present in the voltage and current waveforms. Since ringing is an important issue in the application of SiC devices, it is treated in detail in this section.

Parasitic oscillations during the switching transients may cause EMC problems in the gate driver, for example, or device failure due to high voltage spikes. For the machine, high *dv/dt* and common mode voltages may lead to windings' isolation and bearing failures [121, 125, 126]. With SiC devices and their faster switching rates this issue becomes critical for their application and will have an effect on the device performance. Some investigations about this subject have been recently reported, mainly related to low-voltage low-current devices [17–22, 109, 122, 127]. In these cases, the oscillations are mainly caused by high current change rates *di/dt* and the use of unipolar devices without tail current. As a consequence, circuit parasitics such as stray inductances and capacitances start to resonate.

In the case of the diode characterized here, oscillations in the range of 4.5 to 6.5 MHz are present during the diode turn-off transient, if no *RC* snubber is used, see Fig. 3.38. As stated in [126, 128], there are four possible sources to this behaviour:

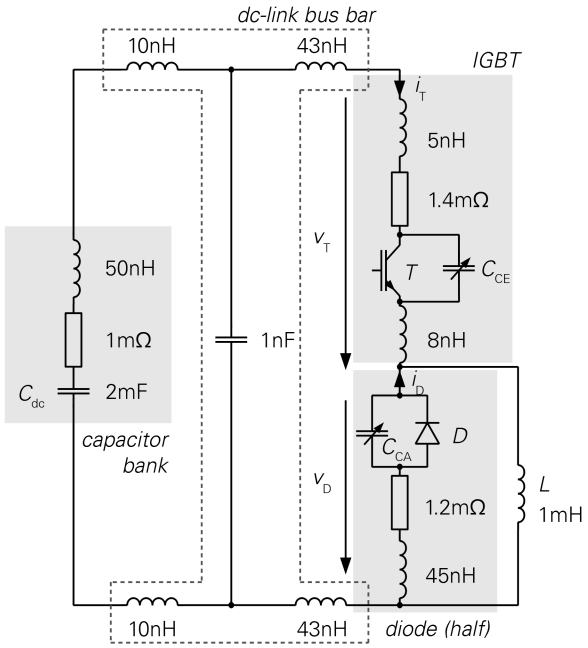


Figure 3.39: Equivalent circuit of the test bench for dynamic characterization with extracted parameters

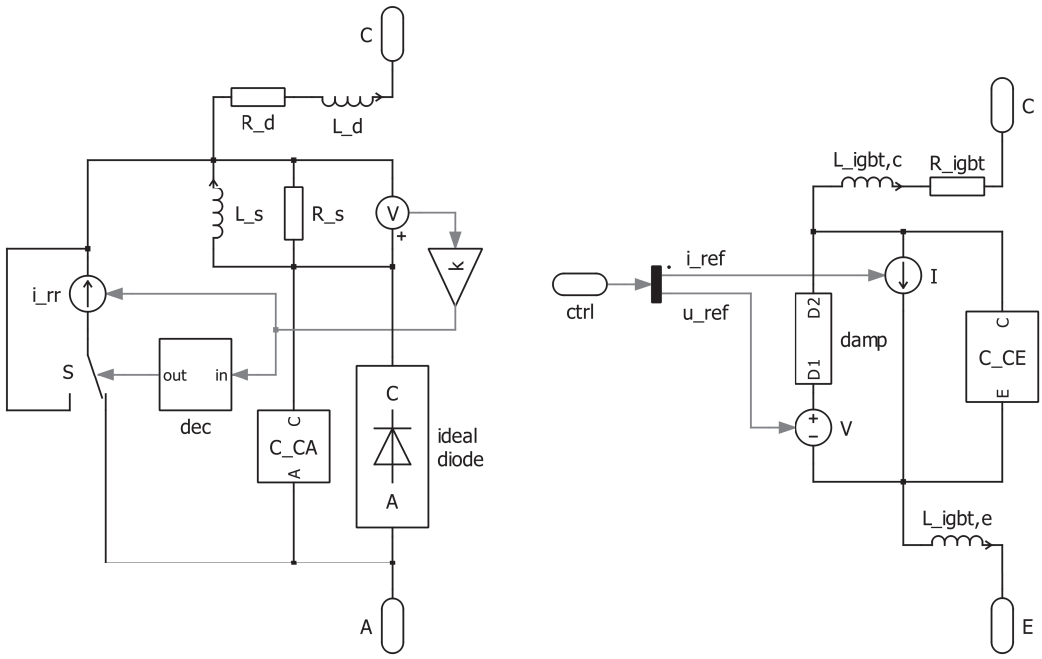
1. High *di/dt* during commutation
2. High *di/dt* after the reverse recovery current peak
3. Duration of the reverse recovery process (resonant frequency)
4. Unequal current distribution in the paralleled dies inside the module

Since these oscillations appear at common *di/dt* ratings for Si devices —i.e. 0.9...2.5 kA/µs at 1 kA, 2.4 kV, see Fig. 3.38— where usually no ringing is observed, the first source can be discarded. The fourth source can also be discarded by observing the shape of the reverse recovery current in the SiC diode, with no overlapped reverse recovery peaks. Only the second and third sources remain as possible alternatives. To investigate them, a simulation of the switching transient using behavioural models of the IGBT and the SiC diode was developed. The interactions of the circuit parasitics with the oscillations were also investigated.

The following procedure was used to determine the different factors that affect the oscillations: First, the parasitic elements in the test circuit were extracted out of measurements. As a second step, behavioural models of the IGBT and diode were elaborated and validated through measurements. With the validated models, the different parameters involved in the oscillations were analysed through simulation. Out of this analysis, possible solutions and their limitations were derived. An *RC* snubber circuit showed good results damping the oscillations. This alternative was simulated and experimentally verified in the test bench. The work contained in this section was presented in [6].

3.6.1 PARAMETER EXTRACTION

The test bench used to analyse the oscillations is the same one used in Sec. 3.4.2, see Fig. 3.4. The same circuit including the modelled parasitic elements is shown in Fig. 3.39. The diagram can be divided in four elements: dc-link capacitor —including the equivalent series resistance (ESR) and the equivalent series inductance (ESL) taken from the data sheet—, dc bus bar and the diode and IGBT (FZ600R65KF2) modules.



(a) Diode model [131] (b) IGBT model

Figure 3.40: Semiconductor device models as used in PLECS simulation software

The dc bus bar was modelled as an array of stray inductors for the positive and negative bus connected through a stray capacitance due to the laminated design. The capacitance was calculated out of the geometry assuming ideal parallel plates and the inductance was estimated through measurements and computer calculations based on the partial element equivalent circuit (PEEC) method with the software InCa3D [129, 130].

The elements of the diode and IGBT considered in the model were the module inductance, junction capacitance and on-state resistance. The IGBT and diode modules' internal stray inductance was calculated by applying the basic equation $v = L \cdot \mathrm{d}i/\mathrm{d}t$ to measured waveforms of the device during commutation.

The voltage-dependent junction capacitance C_j was determined by connecting a high-ohmic resistor R_ho (1 MΩ) to the device terminals and using the discharge curve corresponding to $C_\mathrm{j}R_\mathrm{ho}$ to extract the capacitance value for different voltage levels. This is a simple method, but due to the voltage dependency of C_j does not deliver accurate results. Nonetheless, these were good enough to be used as initial values for the simulation. The on-state resistance was approximated linearly from the on-state characteristic. The values for the extracted parameters are included in Fig. 3.39.

3.6.2 DEVICE MODELLING AND VALIDATION

The device models as implemented in the simulation software PLECS [132] are presented in Fig. 3.40. To study the oscillations, the diode model is able to produce a reverse recovery current peak and shape that can be adjusted by the user, see Fig. 3.40a.

For the realization of a reverse current peak, the model proposed in [131] was adapted: a combination of `L_s`, `R_s` and the decoupling block `dec` together with the current source `i_rr` and an ideal diode are used to generate a reverse recovery current with an adjustable shape, by choosing the reverse recovery peak I_rrm and the current change rate after the peak di_rr/dt . The current waveform obtained through the simulation is the result of the input parameters defined by the user in the diode model and the superimposed oscillations of the circuit parasitics, as shown in Fig. 3.41.

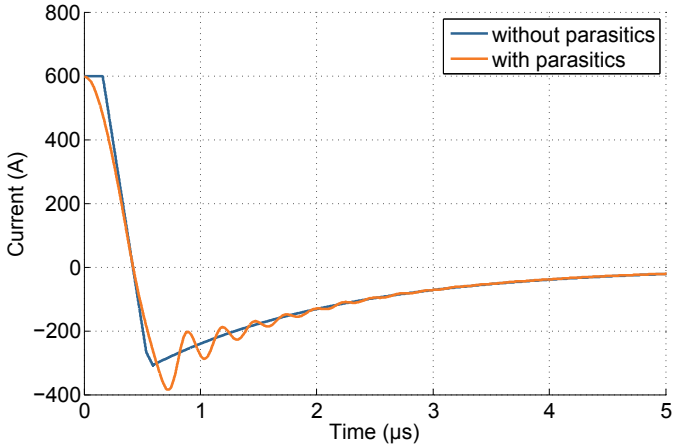
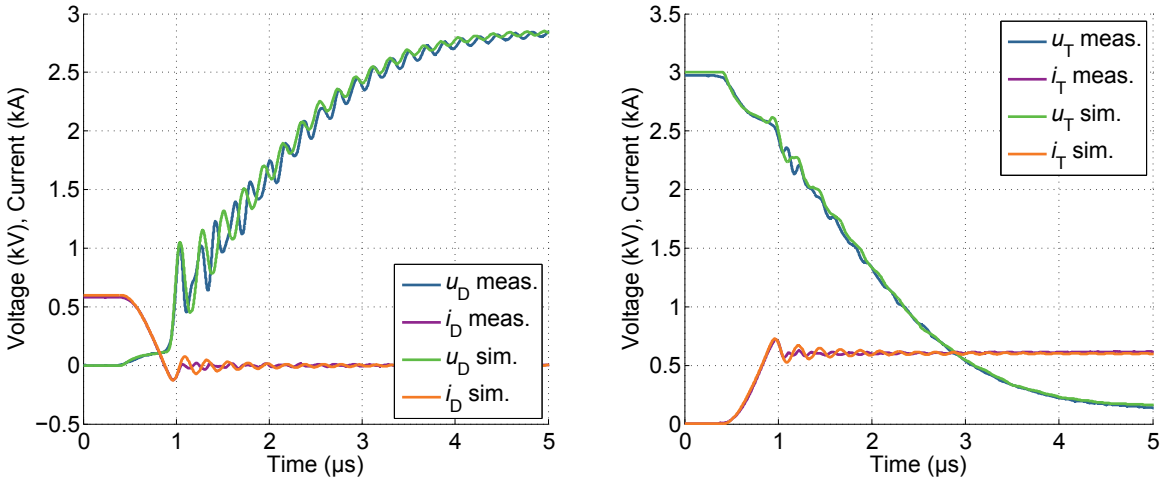


Figure 3.41: Comparison of the simulated reverse recovery current waveform with and without the effect of circuit parasitics.



(a) Diode turn-off

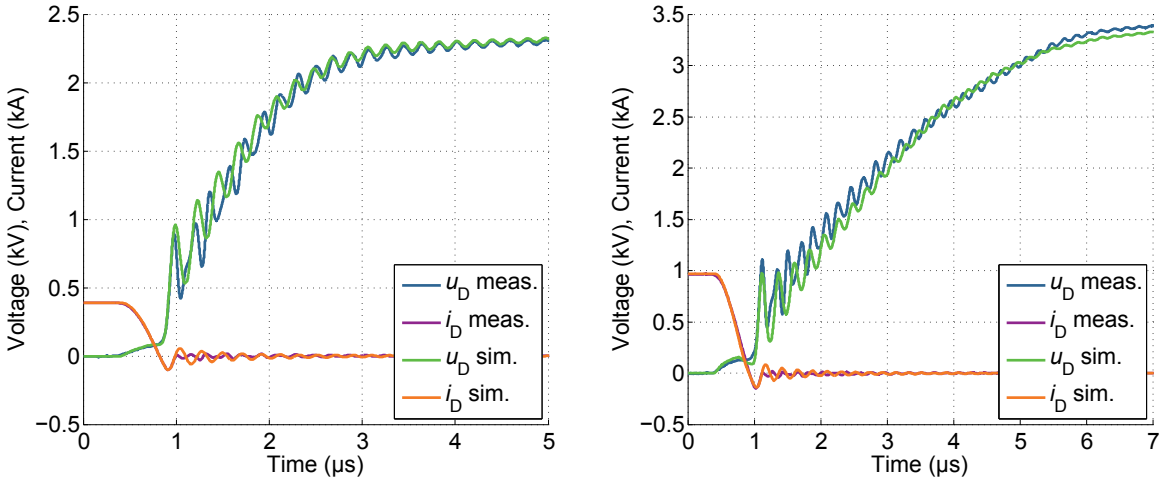
(b) IGBT turn-on

Figure 3.42: Comparison between measurement and simulation at calibration point (V_{dc} = 3 kV , I_D = 600 A, ϑ_j = 25 °C, $R_{g,on}$ = 4.1 Ω).

The IGBT model has as input the desired *dv/dt* and *di/dt* values. These input values together with a reference waveform are given to the IGBT to generate the waveforms. In the block `damp` a damping resistor was modelled. This element acts as a current-controlled resistor which is calibrated by measurement data. Additionally, values for the internal inductance, resistance and capacitance can be entered.

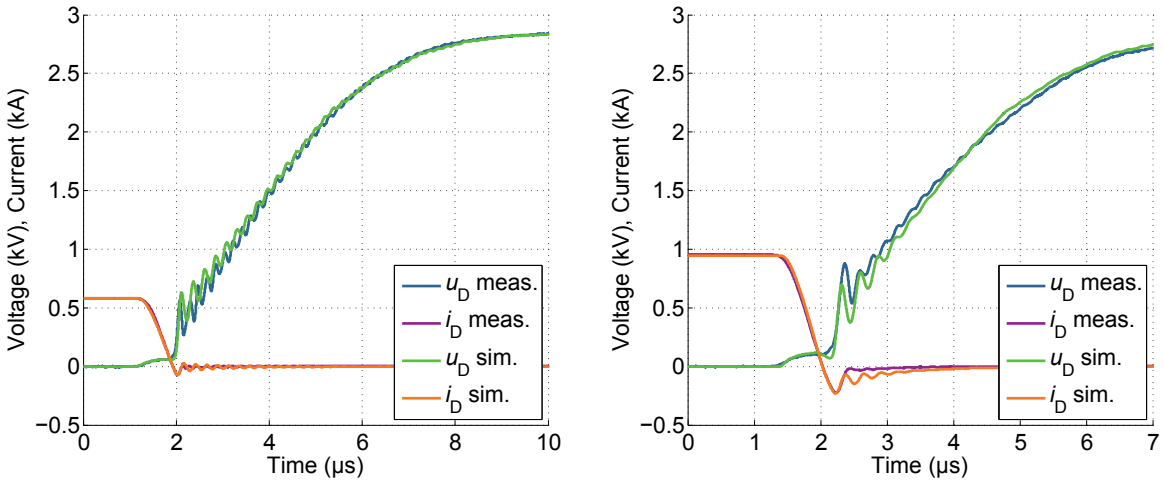
The information needed by the model —e.g. the data for the block `damp`— is taken from a reference measurement. This is shown in Fig. 3.42, with both simulated and measured waveforms. In order to validate the model, the input variables for the simulation, such as dc-link voltage V_{dc} or current change rate *di/dt* ($R_{g,on}$) were varied and the simulation results were compared to the measurements, see Figs. 3.43 and 3.44.

It can be appreciated that the frequency of the oscillations in the simulation could be matched accurately only for the last part of the turn-off transient. In the measured waveforms the oscillation frequency is not constant, but the result of the superposition of two oscillations with variable frequencies that reach a final common frequency after a few microseconds. In the simulation the modules were modelled as a concentrated element. Due to this simplification and



(a) V_{dc} = 2.3 kV, I_D = 600 A (b) V_{dc} = 3.5 kV, I_D = 1 kA

Figure 3.43: Comparison between measurement and simulation of the diode turn-off transient at different V_{dc} values (ϑ_j = 25 °C, $R_{g,on}$ = 4.1 Ω).



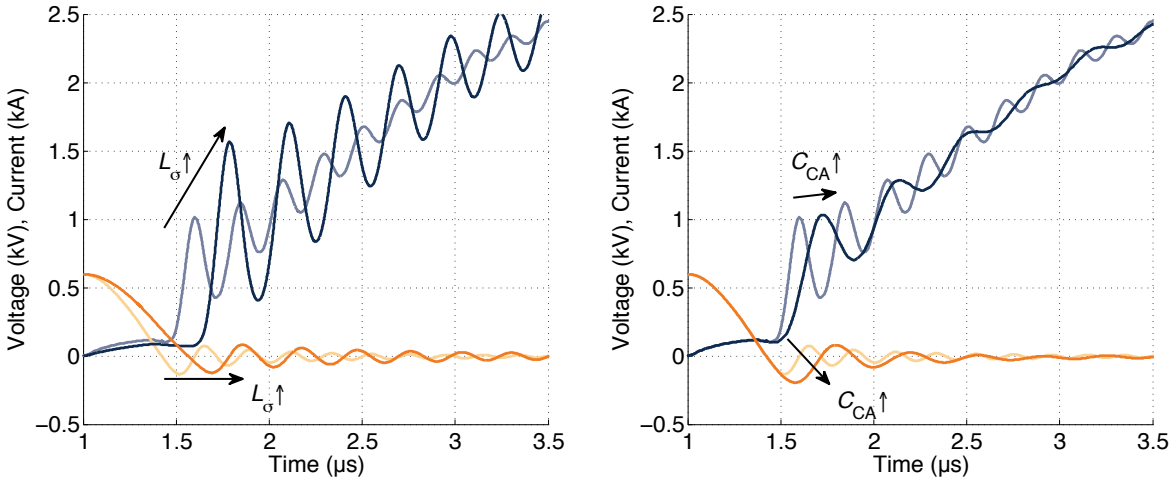
(a) $R_{g,on}$ = 8.2 Ω, I_D = 600 A, ϑ_j = 25 °C (b) ϑ_j = 125 °C, I_D = 1 kA, $R_{g,on}$ = 4.1 Ω

Figure 3.44: Comparison between measurement and simulation of the diode turn-off transient with (a) a different $R_{g,on}$ and (b) with a higher junction temperature ϑ_j (V_{dc} = 2.9 kV).

neglected parasitics, only a constant frequency was simulated in the model and was matched to the final part of the oscillation, see Figs. 3.42–3.44.

In the Fig. 3.44b an interesting behaviour can be observed. At high junction temperature (ϑ_j = 125 °C) the voltage oscillations in the SiC diode almost completely disappear. Adjusting the shape of the reverse recovery current waveform in the simulation to the shape of the measured current at ϑ_j = 125 °C delivered similar results. This indicates that the reverse recovery shape has a direct influence on the parasitic oscillations. The next section uses the simulation models to study these effects.

Despite the drawbacks mentioned above, the model is able to generate waveforms that can be used to qualitatively assess the influence of the different parameters on the voltage oscillations during the diode turn-off transient, which is the main purpose of this investigation.



(a) Stray inductance L_σ = 106, 318 nH (increase)

(b) Diode's junction capacitance C_{CA} = 1×, 3× $C_{CA,ref}$

Figure 3.45: Influence of (a) stray inductance and (b) capacitance in the oscillations, dark blue: voltage, orange: current (V_{dc} = 3 kV, I_D = 600 A, $R_{g,on}$ = 4.1 Ω, ϑ_j = 25 °C).

3.6.3 SIMULATIVE ANALYSIS

First of all, the most influential parameters were identified. As Fig. 3.39 shows, the largest parasitic inductance corresponds to the dc-link bus bar, which dominates during commutation and has a direct effect on oscillations. Variation of the IGBT's junction capacitance and bus bar capacitance did not bring, as expected, any major change and were left at their initial values. The diode's junction capacitance and the shape of the reverse recovery current, on the other side, are critical for the high-frequency oscillations and were given more attention.

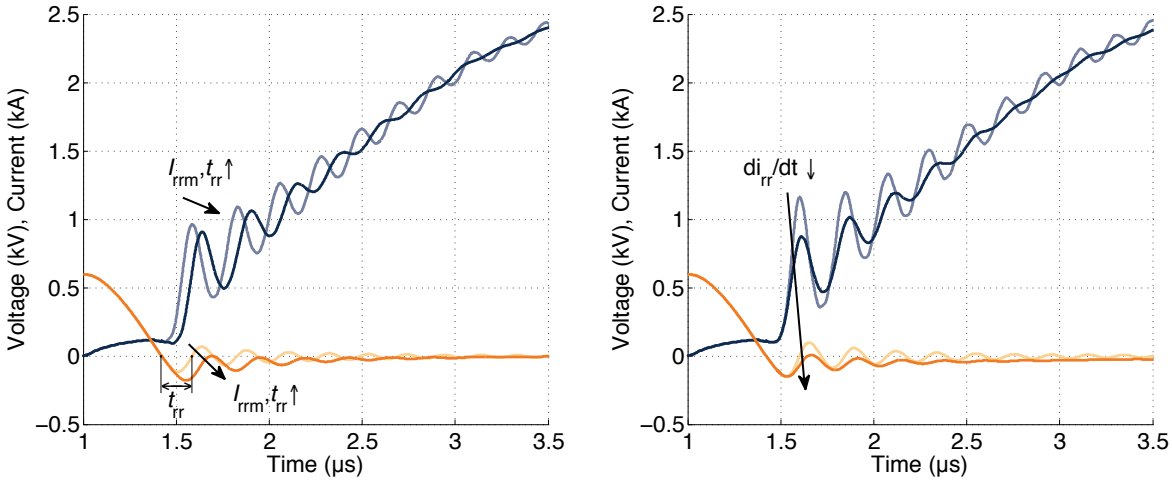
In the first part of the analysis, the influence of the stray inductance in the commutation circuit and the diode's junction capacitance is analysed. A simulation of the SiC diode turn-off transients for different stray inductance values of the dc bus bar connection was carried out, see Fig. 3.45a. It is clear that a low-inductive mechanical design is very important. However, there are certain limits given by the operating voltage of the devices and the required creepage distances and air gaps that have to be taken into account for the mechanical design. The selection of the dc-link capacitors plays also an important role; low-ESL capacitors should be preferred.

As expected, a higher junction capacitance of the diode (C_{CA}) reduces the frequency of the voltage ringing, see Fig. 3.45b. Here, the measured junction capacitance $C_{CA,ref}$ was increased threefold. A higher reverse recovery peak can be observed, which accounts for the higher capacity. Regarding the voltage oscillation amplitude, no relevant changes can be observed.

After analysing the effect of inductances and capacitances on the oscillations, the influence of the reverse recovery waveform shape was studied. The reverse recovery behaviour of a diode is related to its internal structure, as defined by the structure and design of the semiconductor device [42]. With the behavioural model of the diode, the shape of the reverse recovery current can be changed without the need of adjusting parameters in a physical model.

The first scenario, depicted in Fig. 3.46a, aims at assessing the influence of the reverse recovery current duration t_{rr}, without changing the *di/dt* before as well as after the current peak [126]. The simulations show a slight decrease in the amplitude as well as the frequency of the voltage oscillations. Changing the shape of the reverse recovery current as shown in Fig. 3.46a has a direct consequence in increasing the stored charge and, hence, the switching losses.

The current change rate after the reverse recovery current peak di_{rr}/dt is a critical parameter



(a) I_{rrm} = 116, 179 A, t_{rr} = 163, 267 ns (b) di_{rr}/dt = 3.3, 1.9 kA/µs (decrease)

Figure 3.46: Influence of (a) the simultaneous variation of reverse recovery current peak I_{rrm} and duration t_{rr} and (b) variation of the current change rate after the reverse recovery peak di_{rr}/dt in the oscillations, dark blue: voltage, orange: current (V_{dc} = 3 kV, I_D = 600 A, $R_{g,on}$ = 4.1 Ω, ϑ_j = 25 °C).

in diodes. For Si devices, diodes labelled as *soft-recovery diodes* are popular in hard-switched applications, because they ensure a low di_{rr}/dt without snappy behaviour. Oscillations caused by snappy diodes with a very high di_{rr}/dt can lead to device failure [133]. Since the di_{rr}/dt increases with faster current change rate *di/dt* during the commutation, the first voltage spike will also increase, see Fig. 3.38. This is a limiting factor for the switching speed and maximum device overvoltage.

The simulation results in Fig. 3.46b indicate that a slower di_{rr}/dt is the best way to tackle the problem of the oscillations, as both current and voltage oscillations are reduced. Since the turn-off losses of this diode are under 100 mJ at 3 kV, higher losses can be accepted with a small impact on overall performance. Considering the conditions given in (3.5), conduction losses are about two 2 kW per module. If the diode commutates at a frequency of 800 Hz, switching losses amount to only 80 W, which is a relatively low value. From an application point of view, a device redesign for a slower di_{rr}/dt would be advantageous.

3.6.4 DAMPING THE OSCILLATIONS WITH AN *RC* SNUBBER

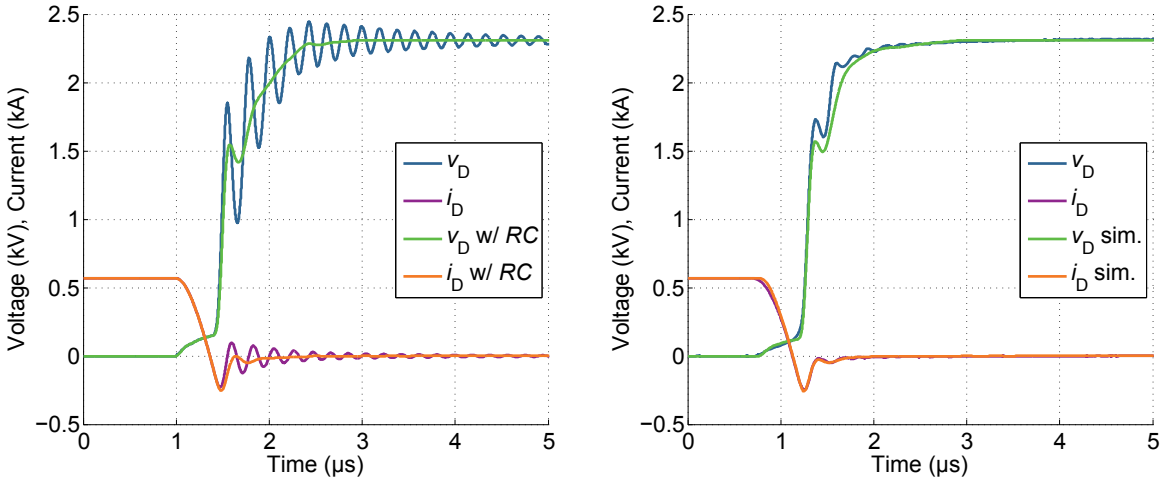
A common solution of a converter designer to reduce the parasitic oscillations in a circuit is the use of an *RC* snubber in parallel with the device that oscillates, see Fig. 3.12. To find a suitable *RC* combination the following method was used [134]:

Considering a fixed stray inductance value for the commutation circuit of L_σ = 214 nH, as in the simulation model, and a frequency range of the oscillations f_r between 4.5 and 6.5 MHz, it is possible to estimate the capacitance of the SiC diode C_{CA} as follows:

$$C_{CA} = \frac{1}{(2\pi f_r)^2 L_\sigma} \tag{3.7}$$

According to (3.7), the value of C_{CA} varies between 2.8 and 5.8 nF. The resistance R_s is determined by

$$R_s = \frac{1}{2\xi}\sqrt{\frac{L_\sigma}{C_{CA}}}. \tag{3.8}$$



(a) Simulation with and without *RC* snubber

(b) Comparison simulation and measurement

Figure 3.47: Effect of an *RC* snubber circuit connected to the diode (C_s = 9.4 nF, R_s = 4.7 Ω, V_{dc} = 2.3 kV , I_D = 600 A, *di/dt* = 2.2 kA/µs)

For critical damping ($\xi = 1$), R_s should be in the range of 3.0 to 4.4 Ω. An initial value of C_s can be found by setting the cut-off frequency of the *RC* circuit to the frequency of the oscillations f_r, that is,

$$f_c = \frac{1}{2\pi R_s C_s} = f_r. \tag{3.9}$$

The range obtained for C_s is between 5.6 and 11.7 nF. Since 4.7 nF capacitors with 6 kV blocking voltage are a standard product, the following combinations were experimentally investigated: C_s = 4.7, 9.4 nF; R_s = 3.3, 4.7 Ω. The combination 9.4 nF, 4.7 Ω showed good results, as the simulations and measurements in Fig. 3.47 demonstrate. For the case of very high *di/dt* (*di/dt3* in Fig. 3.14a) the capacitance was increased to 14.1 nF. Slight differences between the simulated and measured voltages can be seen in Fig. 3.47b, because the IGBT was switched with a different GDU than the one used for the initial modelling.

With this *RC* snubber it was possible to switch on the IGBT at a higher *di/dt* without being limited by the overvoltages caused by the oscillations, see Fig. 3.48 for measurement results. Even with a threefold increase of the switching speed the oscillations are almost completely damped by the *RC* snubber. Higher *di/dt* values than the ones tested are also possible, as long as no overvoltages endanger the device; eventual oscillations can be dampened by readjusting the snubber circuit if desired. Regarding the extra losses added by the snubber circuit, these are marginal compared to the conduction losses of the device, as already discussed in Sec. 3.4.2.

It is known that under certain circumstances, the measurement at the outer terminals of the diode module instead of directly at the diode dies could lead to the false assumption that the oscillations are gone, whereas they were only *hidden* by the snubber effect [25]. This is better exemplified by looking at the circuit in Fig. 3.49. For the analysis in this section, the diode voltage v_D represents the voltage at the module terminals, which includes the effects of the parasitic inductance inside the module and the *RC* snubber circuit connected to the outer module terminals (see Fig. 3.23b). The diode voltage inside the module $v_{D,int}$ is determined by the following equation:

$$v_{D,int} - L_{\sigma,D} \cdot \frac{di_{D,int}}{dt} = v_C - R_s i_s \tag{3.10}$$

Hence, the voltage v_D measured with the voltage probe differs from the anode-cathode voltage of the diode inside the module, $v_D \neq v_{D,int}$, see Fig. 3.50. This voltage $v_{D,int}$, in turn, differs

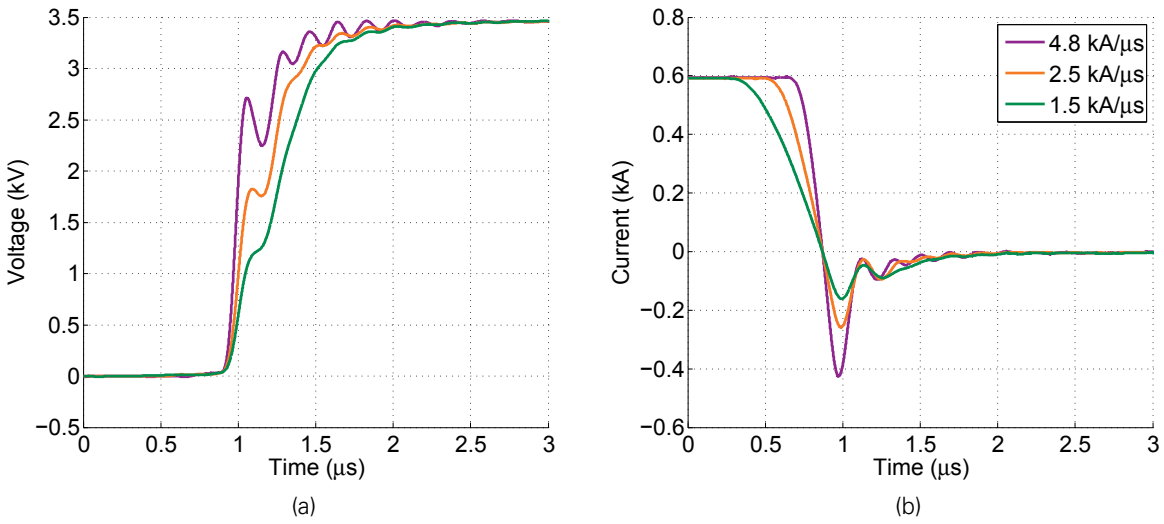


Figure 3.48: Measured voltage and current waveforms for diode turn-off at different *di/dt* with an *RC* snubber: C_s = 9.4 nF, R_s = 4.7 Ω for *di/dt* = 1.5, 2.5 kA/µs; C_s = 14.1 nF, R_s = 4.7 Ω for *di/dt* = 4.8 kA/µs (V_{dc} = 3.5 kV , I_D = 600 A, ϑ_j = 25 °C).

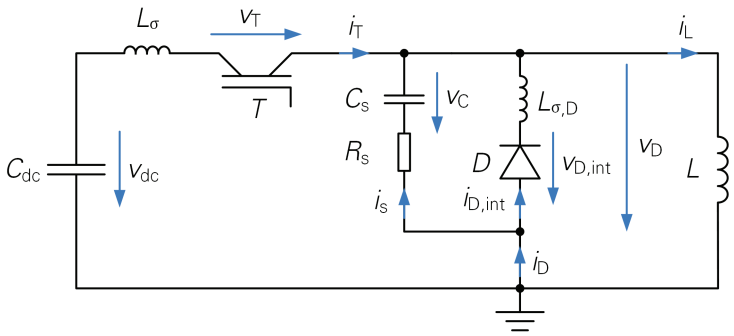


Figure 3.49: Equivalent circuit of the test bench for dynamic characterization.

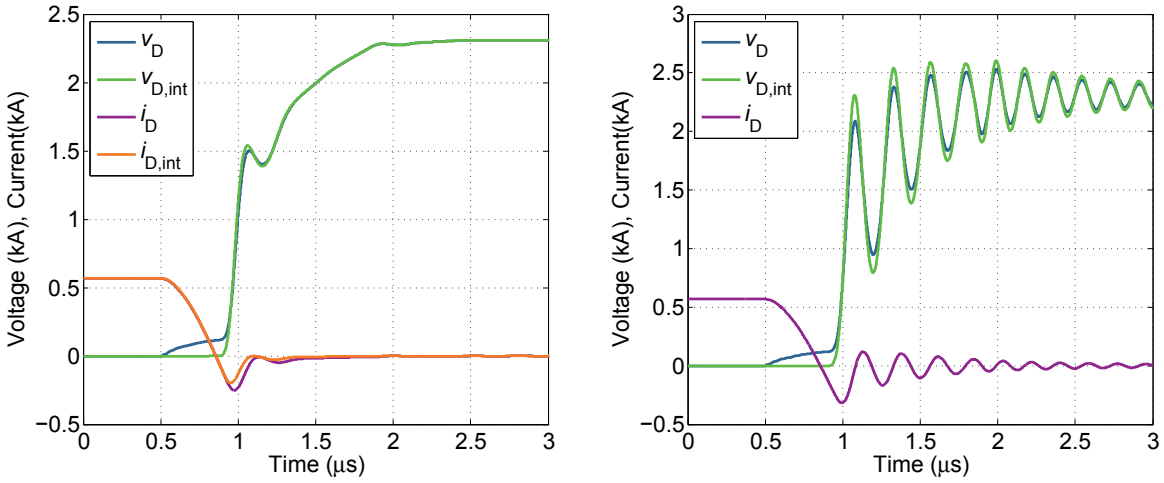
from the real diode die voltage, which due to the interconnection inductances might be slightly different for each diode when the current changes at a certain *di/dt*.

Since it is not possible to measure the voltage of the diode dies directly, the effect of the *RC* snubber should be analysed through simulation. However, a full model of the diode module including internal interconnections was not available. To verify the voltages across the dies further investigations are recommended.

3.6.5 SUMMARY

The analysis of the oscillations during the turn-off transient of a newly introduced 6.5-kV, 1-kA SiC PiN diode was presented. For this purpose, a behavioural model of the semiconductors involved was developed. A characterization of the test circuit used in the measurements was also necessary in order to model the phenomenon. The methodology used to develop the model and extract the circuit parameters was explained.

From the simulation results more insight into the sources of the oscillations was gained. The reverse recovery current change rate di_{rr}/dt was identified as the main source for the oscillations. The stray inductance of the commutation circuit plays a major role in amplifying these oscillations. Thus, a careful mechanical design of the power circuit, as well as the use of



(a) With *RC* snubber (b) Without *RC* snubber

Figure 3.50: Effect of an *RC* snubber circuit connected to the diode including internal diode waveforms (C_s = 9.4 nF, R_s = 4.7 Ω, V_{dc} = 2.3 kV , I_D = 600 A)

low-inductance components are required.

An *RC* snubber is an effective solution to the oscillation problem if the stray inductance cannot be further reduced. The measurements confirmed that a value of 9.4 nF, 4.7 Ω is a good choice for reducing the oscillations in this diode. However, the inclusion of an *RC* snubber increases the manufacturing costs and reduces the converter reliability. The application of the SiC diode would benefit from an improved device design with a softer decay of the reverse recovery current, as it would allow the possibility of obtaining oscillation-free voltage and current waveforms during turn-off without the need of an *RC* snubber.

3.7 SUMMARY

The electrical characterization of the SiC diode module is the core of this dissertation and has been presented in this chapter. The diode die and module design were briefly explained and the required experimental setup and power devices needed for the device characterization were outlined. For a better understanding of the SiC diode features, the results were compared with a commercial Si diode module with equal dimensions and similar ratings.

Through the analysis of the static behaviour it was possible to characterize the on-state voltage of the diode and its temperature dependency, the leakage current and breakdown voltage, and the forward degradation issue. The on-state voltage, compared to Si diodes of equivalent ratings, is high. For 600 A device current, roughly 100 A/cm^2, the device voltage is around 3.9 V, compared to the 3.0 V of a similar Si module. As usual in SiC devices, the diode exhibits a negative temperature coefficient. Even though this is normally an undesired property, because it can lead to problems in current sharing for paralleled devices, its low value of less than 1 mV/K at high temperatures is not high enough for a device to experience thermal runaway. The threshold voltage of the SiC diode is around 2.8...3.0 V and is a consequence of SiC PiN technology. The diode module proved that it can successfully block voltages up to 6.5 kV. The Si diode, on the other side, had currents in the milliampere-range for 125 °C junction temperature.

The switching behaviour of the SiC diode is related to one of its most notorious advantages. Contrary to the Si PiN diodes, the reverse recovery charge is substantially reduced, which translates into a very fast turn-off transient with very low losses. For the studied prototype this was

experimentally demonstrated. However, the addition of an *RC* snubber might be required if oscillations have to be damped when switching at a high *di/dt*. The extra capacitor adds losses and increases the reverse recovery current peak. Nonetheless, the added capacitance is small (<10 nF) and the diode losses can still be classified as low compared to the Si diode. For rough loss calculations, the switching losses can be neglected if the frequency is low enough (<1 kHz), as the conduction losses clearly dominate. More on this issue will be commented in the following chapter.

The IGBT turn-on losses can be halved just by changing the diode technology to SiC. Further increase of the *di/dt* during the IGBT turn-on transient will result in an even higher loss reduction. However, an increase of the *dv/dt* has to be taken into account. As it will be shown in the following chapter, switching loss reduction in the IGBT is directly related to the maximum converter output power.

The configuration with two series-connected 3.3-kV IGBTs turned out to be more sensitive to ringing than the case of the single 6.5-kV IGBT module. Obviuosly this is relatedwiss to the slightly higher stray inductance during commutation (+20 nH) and the different output capacitances of the IGBTs. This demands a careful design of the converter power circuit and the snubber circuits to avoid device failure and/or EMI problems.

Unwanted oscillations during the device commutations are a common issue in SiC devices. For the analysed 6.5-kV diode module, oscillations during the turn-off transient were observed. The phenomenon was studied and the interaction of the different parameters during switching was analysed. Through behavioural models of the devices, it was concluded that the oscillations are mainly caused by a strong current change rate after the reverse recovery peak of the diode. The stray inductance in the commutation circuit should be as low as possible to keep the amplitude of the ringing under control. An *RC* snubber connected directly to the diode terminals provides an simple way of dampening the oscillations without adding considerable switching losses. A more elegant solution relies on low-inductive module and dc bus bar design and/or an improved diode design with softer reverse recovery current change rates, which need to be further evaluated.

4 COMPARISON AT CONVERTER LEVEL

4.1 INTRODUCTION

To assess the potential of a new power semiconductor device it is necessary to evaluate its performance in a converter. In the category of medium voltage VSCs applying SiC devices, recent attention has been directed to the well-known 3L-NPC topology with 6.5- and 10-kV devices and the 2-level topology with 10-kV devices, for an output power of 1 MW [135] and 100 kVA [136]. Another approach focused on the 3L-NPC topology includes 4.5-kV, 1.2-kA hybrid power modules with Si IGBTs and SiC JBS diodes as well as 4.5-kV, 1600-A JBS diode modules in a 2.3-MW inverter [137]. All the aforementioned papers present comparisons with Si-based converters by using device models scaled from single-die measurements. The analysis is focused on converter losses, efficiency and high-frequency operation; no thermal calculations were included.

The comparison at converter level that is presented in this chapter has a different approach. The starting point is the 6.5-kV, 1-kA SiC PiN diode module that has been characterized in the previous chapter. As mentioned there, the prototype tested contains 80 dies, packaged in an industry-standard $130 \times 140\,mm^2$ module. The next version of this module prototype contains 120 dies in a $190 \times 140\,mm^2$ module with a current rating of 1.5 kA, which is the one that was considered as the basis for the converter design, see Fig. 4.1 for a photo of the module layout. The new module has also been thermally characterized, which allows the calculation of the junction temperature.

The 3L-NPC VSC topology was chosen for the evaluation of the new SiC diode. Figure 4.2, shows an NPC inverter equipped with a 12-pulse diode bridge rectifier. In this case, the energy flow is unidirectional, from the ac grid to the ac load through the dc voltage link (ac→dc→ac). Alternatively, if the diode bridge rectifier is replaced by an active front-end, it is also possible to inject energy into the grid. A series connection of two 3.3-kV IGBT modules for the switches and two 3.3-kV diodes for the neutral point (NP) positions with a current rating of 1500 A are the preferred solution in industrial IGBT-based converters with an output power of about 7 to 8 MVA [138]. For the analysis in this chapter, the different device positions in one phase leg of the NPC converter are named as indicated in Fig. 4.3.

The potential of using SiC technology in 3L-NPC converters was already experimentally investigated on a lower scale (230 V, 10 kVA) in [139], where a loss reduction of 10% compared to the Si counterpart was achieved. However, these results are not easy to scale to medium-voltage, high-power applications. This analysis contributes with a measurement-based estimation of the potential advantages of SiC PiN diodes in this field. For this purpose, several device configurations at different current change rates were investigated for the NPC converter, such as 3.3- and 6.5-kV IGBT modules, SiC diodes as NP diodes and as antiparallel diodes inside the

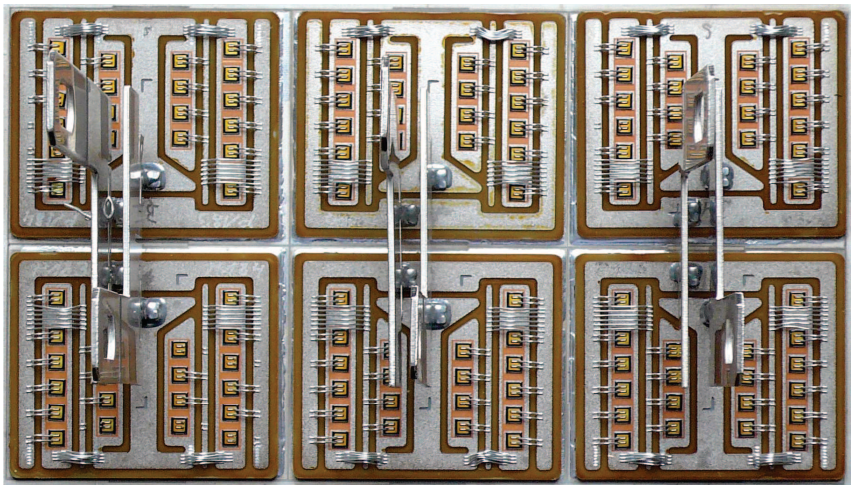


Figure 4.1: Diode module prototype layout, second version: 120 dies, $190 \times 140\,\mathrm{mm}^2$.

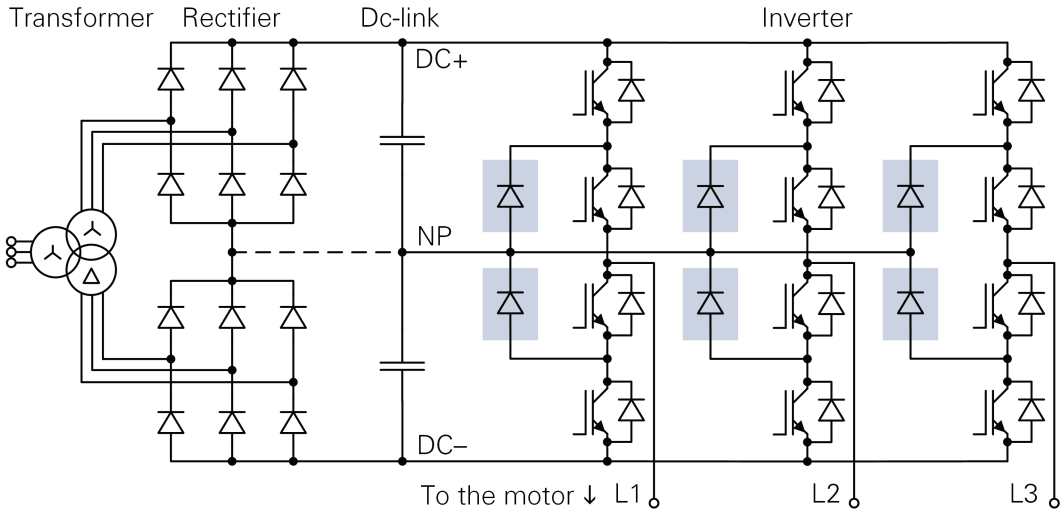


Figure 4.2: IGBT-based 3L-NPC converter with diode front-end, neutral point diodes in blue.

IGBT modules. The results contained in this chapter can also be found in [8].

Furthermore, a section of this chapter has been used to describe an MPC algorithm that takes into account the reduced switching losses of the commutations related to the SiC NP diodes in the NPC converter. With this method instead of the standard carrier-based sine-triangle modulation higher efficiency levels can be obtained without worsening the output waveform quality.

4.2 POWER DEVICE MODELLING

In order to evaluate the performance of a given power semiconductor setup in a converter it is mandatory to calculate the junction temperature for each device under worst-case conditions. The key to an accurate temperature estimation is a model of the power device that reflects the losses under conditions that resemble the ones in the final application.

Electrothermal models based on ideal devices and on accurate approximations of measured on-state voltages and switching losses, due to their simplicity, accuracy and higher simulation speed, were preferred over physical or behavioural device models for the junction temperature estimation. A look-up table containing measured on-state voltages and switching losses

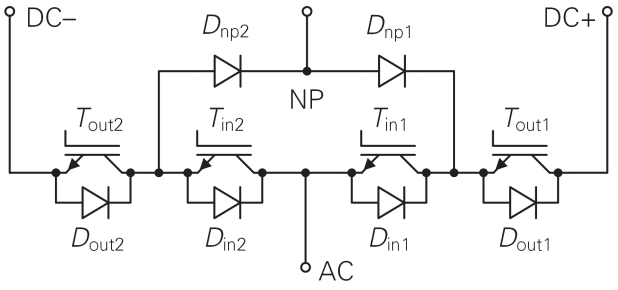


Figure 4.3: 3L-NPC topology, one phase.

assigns the losses according to the simulated voltage and current waveforms to each device. Using thermal resistance values, the device junction temperatures are calculated in a closed loop at each simulation step. This means that the temperature-dependent losses change the device junction temperature, which is used to adjust the losses in the next simulation step. The implementation is done with the simulation software PLECS, which includes all the features needed for this purpose.

The device models of this work were elaborated using the following procedure:

- For commercial devices, the on-state voltage was extracted out of the data sheet. In the case of the SiC diode, where no data sheet is available, the on-state characteristic was measured in one of the module prototypes as explained in Sec. 3.2.2.

- Switching losses are highly sensitive to external conditions, such as the stray inductance and the GDU, and also to internal conditions, such as the junction temperature and the commutation voltage. In order to obtain comparable loss characteristics, a test bench was elaborated and the different device pairs were switched under equal conditions, as presented in Sec. 3.4. The integration limits in the voltage and current waveforms for the loss calculation were set as suggested in [119], see Fig. 3.11.

- Thermal resistances of the commercial devices were taken from the data sheet. In the case of the SiC diode module, these values were estimated through an FEM simulation of the physical structure, which was carried out by the module's manufacturer. Table 4.1 lists the values for each device.

As pointed out in Sec. 3.2.1, the switching losses of the 6.5-kV IGBTs used in the models for the simulations here presented were calculated out of measurements done with a new fully digitally controlled GDU [115], which does not rely on gate resistors for adjusting the switching speed. The 3.3-kV series-connected IGBTs were driven with a traditional analogue GDU used in commercial converters. Both GDUs operate with gate–emitter voltages of −10/+15 V. In order to keep both device measurement sets and models apart, the device configurations related to the 6.5-kV IGBTs use the *R65* prefix and the ones related to the 3.3-kV devices use *R33*. The models analysed in this chapter include two different switching speeds for 3.3-kV devices and three for 6.5-kV devices. The switching speeds for the IGBT turn-on transients were labelled as *di/dt1*, *di/dt2* and *di/dt3*, Fig. 4.4 presents detailed values for each configuration. The reference speed used with Si devices is labelled as *R65 Si* or *R33 Si* depending on the voltage class and is equal or close to the corresponding *di/dt1* speed. As an example, switching waveforms of the SiC PiN diode for *R65 di/dt1*, *R65 di/dt3* and *R33 di/dt2* are shown in Fig. 4.5, which include an *RC* snubber connected to the diode.

The models of the SiC diode required some scaling in order to estimate the on-state voltage V_F and switching losses E_{sw} out of a module prototype containing n_1 dies to one containing n_2

Table 4.1: Thermal resistances

Device	$R_{th,jh}$ * (K/kW)	$R_{th,ha}$ * (K/kW)
FZ600R65KF2 IGBT	20.1	
FZ600R65KF2 diode	38.5	15.0
SiC-D-40	47.7	
FZ1500R33HL3 IGBT	18.5	15.0
FZ1500R33HL3 diode	25.5	
DD600S65K1†	18.5	21.9
DD1000S33HE33†	19.25	21.9
SiCD-120	15.9	15.0

† Thermal values correspond to the full module (two diodes in parallel).
* $R_{th,jh}$: junction to heat sink
$R_{th,ha}$: heat sink to ambient

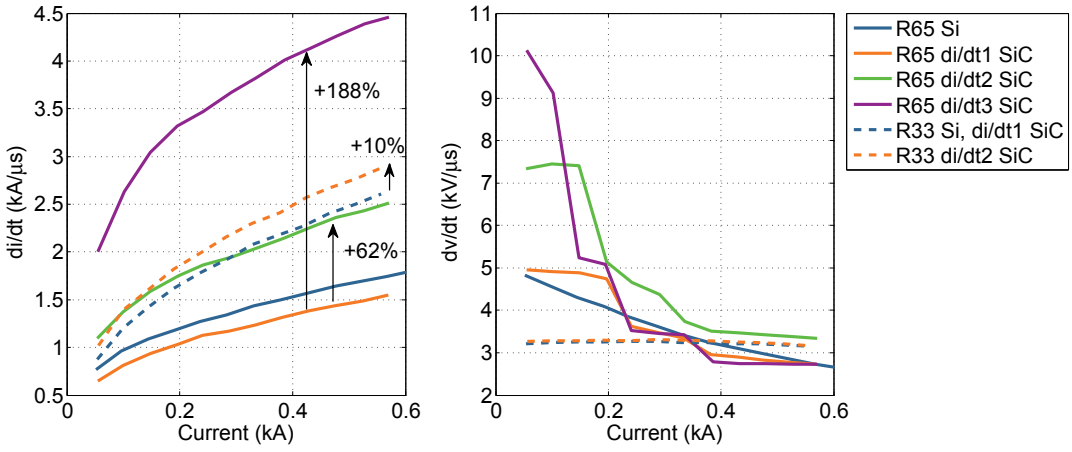


Figure 4.4: Current and voltage change rates for IGBT turn-on transients at 2.9 kV and 75 °C. R65: IGBT FZ600R65KF2 (single), R33: IGBT FZ1500R33HL3 (series connection of two devices).

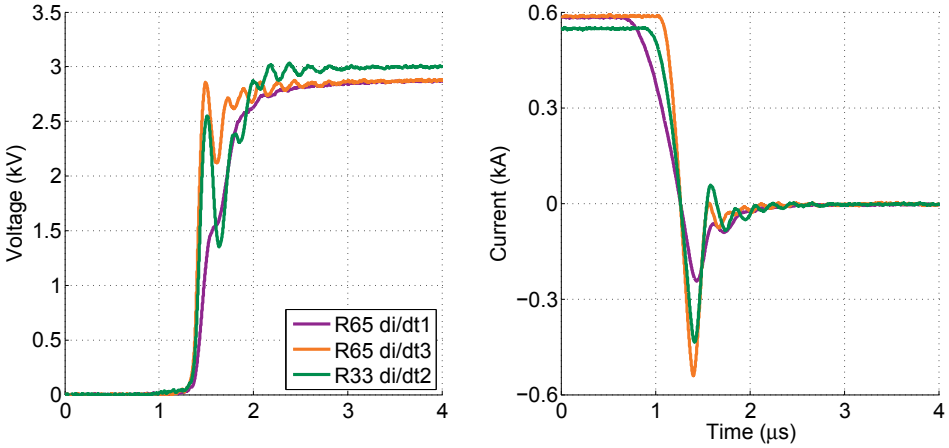


Figure 4.5: Voltage and current waveforms of the 6.5-kV, 1-kA SiC diode module turn-off transients for three different configurations. (R65: IGBT FZ600R65KF2, R33: 2× IGBT FZ1500R33HL3, $V_D = 2.9 \ldots 3.0\,\text{kV}$, $I_D = 0.6\,\text{kA}$, $\vartheta_j = 75\,°\text{C}$, *RC* snubber: 9.4 nF, 4.7 Ω for *R65 di/dt1, R33 di/dt2* and 14.1 nF, 4.7 Ω for *R65 di/dt3*)

dies. These were scaled linearly, considering equal current density values for each die:

$$V_F\left(I_F(n_2)\right) = V_F\left(\frac{n_2}{n_1} I_F(n_1)\right) \tag{4.1}$$

$$E_{sw}(n_2, I_2) = \frac{n_2}{n_1} E_{sw}\left(n_1, \frac{n_2}{n_1} I_1\right), \tag{4.2}$$

where I_1 and I_2 are the currents for the module with n_1 and n_2 dies, respectively, at which the switching loss E_{sw} occurs.

4.3 DETERMINATION OF MAXIMUM CONVERTER POWER RATING

One of the most important criteria for the evaluation of a certain device configuration is the maximum converter power. In the majority of industrial applications, the maximum converter power is limited by the maximum device junction temperature at worst-case conditions. 3L-NPC converters have an unequal junction temperature distribution among their devices. The four critical operating points (OPs) are at maximum or minimum modulation depth m_a, and at a $\cos\varphi$ of 1 or −1, as indicated in [140] and summarized in Table 4.2.

For each critical point, either the IGBTs or the diodes of one position (*in*, *out* or *np* in Fig. 4.3) per phase leg have the highest junction temperature. Not all of the points listed in that table are critical for every application. In the case of quadratic torque loads, e.g. a pump, the most critical point is OP1. If the load is regenerative, OP2 is also of interest. Considering that these loads are usually operated with a V/Hz control (output voltage increases linearly with the output frequency), at low modulation depths the current required by the load is also very low, which is why OP3 and OP4 are not critical.

In the case of loads with constant torque, as in an extruder, the points OP3 and OP4, representing nominal load current at zero speed are critical. In an NPC VSC, the inner switches T_{in} and NP diodes D_{np} are stressed with nominal current for long periods. The junction temperature over one cycle can increase over the maximum allowed, which is why a derating of the converter output current is required. Depending on the cooling conditions, this derating can amount to even 50% of the nominal power. To evaluate the converter performance in OP3 and OP4 properly, dynamic electrothermal models of the power devices are required. If the output frequency

Table 4.2: Critical operating points for 3L-NPC VSC

	OP1	OP2	OP3	OP4
m_a	max. (1.15)	max. (1.15)	min. (0.01)	min. (0.01)
$\cos\varphi$	1 (mot.)	−1 (gen.)	1 (mot.)	−1 (gen.)

Table 4.3: Device configurations

Name	T_{in} , T_{out}, D_{in}	D_{out}	D_{np}
R65 All-Si	FZ600R65KF2	FZ600R65KF2	DD600S65K1
R65 SiC-NPC	FZ600R65KF2	FZ600R65KF2	SiC-D-120
R65 SiC-D	FZ600R65KF2	SiC-D-40	SiC-D-120
R33 All-Si	FZ1500R33HL3	FZ1500R33HL3	DD1000S33
R33 SiC-NPC	FZ1500R33HL3	FZ1500R33HL3	SiC-D-120

FZ600R65KF2, DD600S65K1 and SiC-D-40: 2× parallel
FZ1500R33HL3 and DD1000S33HE3: 2× series
SiC-D-120: single

of the converter is low, e.g. <5 Hz, the instantaneous temperature in the semiconductor devices becomes more significant than the average junction temperature. Since no dynamic thermal model of the SiC PiN diode module was available, the analysis that follows is done considering output frequencies of 50 Hz and quadratic torque loads, dissipative and regenerative, where only OP1 and OP2 are of interest.

4.4 ANALYSIS

Different device configurations were considered for the converter simulations, see Table 4.3. These can be divided into three main groups: The group *All-Si* only uses commercial Si devices, the group *SiC-NPC* considers SiC diodes for the NP diodes D_{np}, and the group *SiC-D* includes SiC diodes for both the NP and the inverse diodes of the outer switches (D_{np} and D_{out}). The use of a SiC diode in D_{in} is not analysed here, as it does not provide any advantage. Contrary to the diodes D_{np} and D_{out}, the inner diodes D_{in} in an NPC phase leg do not experience reverse recovery losses, because the IGBT associated to it remains turned on when the current commutates. For these diodes only conduction losses are relevant. Since Si technology achieves currently better on-state characteristics and thermal resistance values for PiN diodes than SiC technology, e.g. Fig. 3.31 and Table 4.1, the inclusion of SiC PiN diodes would be counterproductive [139]. Preliminary results of this evaluation at converter level were presented in [7], where only 6.5-kV devices and one switching speed *di/dt* were taken into account. The GDU used in that paper was not optimized and caused higher switching losses than the one used for this analysis.

To achieve comparable device current and voltage ratings, 6.5-kV devices were connected in parallel and 3.3-kV devices in series. In other words, the switch composed of T_{out1} and D_{out1} in Fig. 4.3 represents either the series connection of two 3.3-kV, 1500-A IGBT modules FZ1500R33HL3 or the parallel connection of two 6.5-kV, 600-A IGBT modules FZ600R65KF2, depending on the voltage class analysed. The IGBT modules FZ1500R33HL3 and FZ600R65KF2 have the same footprint. For the SiC diode a special label indicates the number of chips in parallel. That is, the designation *SiC-D-120* (Table 4.3) means that 120 parallel dies are in one SiC diode module. In contrast, the inverse diode D_{out} has only 40 dies in parallel due to space limitations inside a standard 140×190 mm^2 IGBT module.

Table 4.4: Converter setup

DC-link voltage V_{dc}		6177 kV
Output voltage		4.16 kV
Output frequency		50 Hz
Switching frequency f_{sw} (carrier)		465 Hz
Output current I_{out}		1000 A
Cooling water temperature		50 °C
Max. avg. junction temp. $\vartheta_{j,max}$		120 °C
Stray inductance		245 nH
Min. turn-on time	R65	100 µs
	R33	25 µs

In an NPC VSC with series-connected 3.3-kV IGBTs, a symmetrical voltage distribution between the devices is commonly achieved by an active gate voltage control with collector-emitter voltage feedback [116]. A bulky *RC* snubber is required for the dynamic and static balancing of the NP diodes. The IGBTs are statically balanced by resistors. The parallel connection of 6.5-kV devices is not so popular at medium-voltage applications, because 3.3-kV devices enable a higher converter power than 6.5-kV devices [2]. Depending on the physical converter layout, the design for a symmetrical current distribution of parallel devices can be as complex as the methods for a symmetrical voltage distribution of series-connected devices. However, newly developed algorithms that solve dynamic and static current sharing in a simple way have been recently reported. In [141], for example, a dynamic balancing method is implemented in the GDU, without the need of either extra passive components or dedicated current measurement circuits.

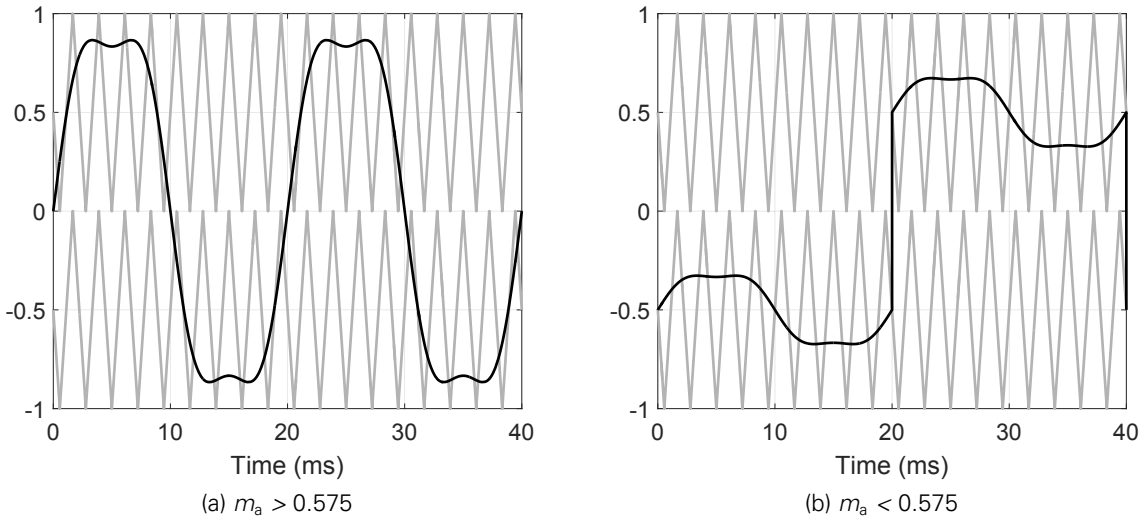
A 3L-NPC VSC with the parameters shown in Table 4.4 was considered to determine and to compare the maximum converter power and switching frequency. The modulation implemented is a conventional sine-triangle pulse width modulation (PWM) with 1/6 3rd harmonic injection, see Fig. 4.6a. For low modulation depths (< 0.575), the reference was alternated from the upper to the lower carrier band (two-level modulation), to avoid an overheating of the NP diodes [142], as in Fig. 4.6b. The thermal resistance values for the heat sink $R_{th,ha}$ correspond to a water cooling system, see the last column of Table 4.1. The dc-link voltage for an output voltage of 4.16 kV corresponds to 6.2 kV; due to the 3L-NPC topology, each device switches at 3.1 kV, which is in the range of the voltage chosen for the device switching characterization (2.3...3.5 kV). The load was modelled by an ideal 3-phase sinusoidal current source, the dc link capacitors by 2 ideal voltage sources. The simulation was carried out with the software PLECS [132].

Table 4.5 contains the simulation results for maximum output power of each device configuration under the aforementioned conditions. The following sections discuss the benefits and drawbacks of each setup.

4.4.1 SIC DIODE AS NP DIODE WITH 6.5-KV IGBTS *(R65 SIC-NPC)*

The main advantage of using a SiC diode as NP diode D_{np} is the switching loss reduction in the outer IGBTs T_{out}. As shown in Fig. 4.7a, when the current commutates from 0 to +, the current commutates from the diode D_{np1} to the IGBT T_{out1}. That is, the reverse recovery current of the diode affects the turn-on losses in the IGBT. In the case of Fig. 4.7b, when a positive phase current i_{ph} commutates between 0 and –, the diode D_{out2} turn-off affects the losses in the IGBT T_{in1}. The diode D_{in2} in Fig. 4.7b does not experience switching losses, as the IGBT T_{in2} remains turned on when the current commutates from –to 0.

Replacing the NP diodes D_{np} by SiC PiN diodes, which have a lower reverse recovery charge, leads to a switching loss reduction in the outer IGBTs T_{out}. This, in turn, leads to a lower junction



(a) $m_a > 0.575$ (b) $m_a < 0.575$

Figure 4.6: Modulation schemes for (a) high and (b) low modulation depth m_a. (f_{sw} = 450 Hz)

Table 4.5: Maximum output current for different device configurations

Configuration	OP1 (A)	OP2 (A)
R65 All-Si	1050	1202
R65 SiC-NPC di/dt1	1190	1202
R65 SiC-NPC di/dt2	1216	1202
R65 SiC-NPC di/dt3	1244	1202
R65 SiC-D di/dt1	1190	1144
R65 SiC-D di/dt2	1216	1140
R65 SiC-D di/dt3	1244	1135
R33 All-Si	1096	1379
R33 SiC-NPC di/dt1	1268	1379
R33 SiC-NPC di/dt2	1280	1379

temperature in the outer IGBTs, that allows to operate the converter at a higher output current level. Additionally, it is possible to increase the *di/dt* during the T_{out} turn-on transients to achieve an additional loss reduction. With current Si devices, the switching speed of the IGBT at turn-on is limited by the RRSOA of the diode.

It is important to note that in this configuration *(SiC-NPC)*, the diodes D_{out} are standard Si diodes, see Table 4.3. This means that the current slope *di/dt* in the T_{in} IGBTs, which commutate with the D_{out} diodes, should not be increased. Hence, the setup *R65 SiC-NPC di/dt2* stands for an NPC phase leg with 6.5-kV devices, where only the T_{out} IGBTs are turned on at a higher speed, see Fig. 4.4. The T_{in} IGBTs switch at the standard speed for Si devices.

Figure 4.8a shows the maximum converter output power for three different *di/dt* conditions using two 6.5-kV devices in parallel. As a reference, the *All-Si* configuration is included. The cases of unidirectional (only OP1) and bidirectional (OP1 & OP2) energy flow are evaluated. The use of SiC diodes as NP diodes allows an increase of at least 13% in the output power. This is a consequence of the lower switching losses in T_{out}, as shown in Fig. 4.9a, where the device loss and temperature distribution for OP1 is analysed.

Increasing the IGBT turn-on *di/dt* has only marginal influence on the output power. Considering a *di/dt* increase of 188% *(di/dt1* to *di/dt3)* and unidirectional energy flow, a 4% higher output power can be achieved (from 8.58 to 8.96 MVA). For bidirectional energy flow, the ad-

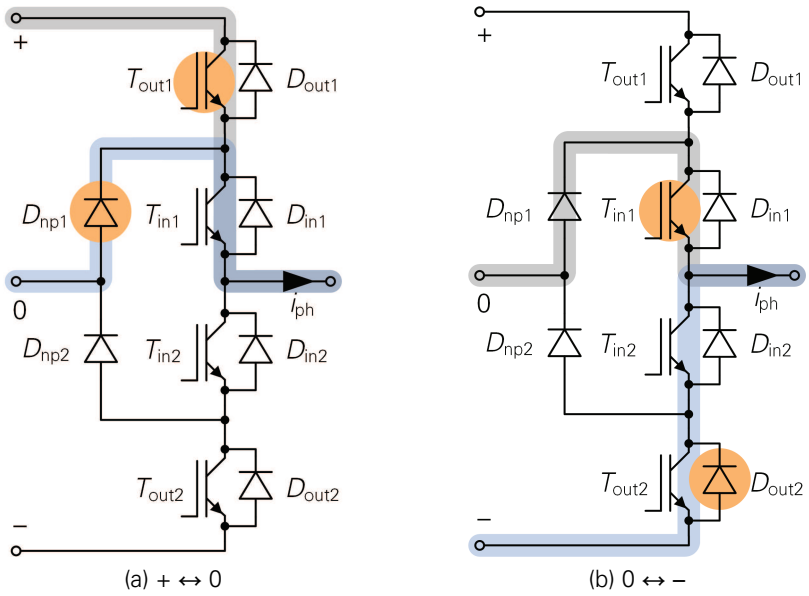


Figure 4.7: Commutation in an NPC phase leg for a positive phase current, orange circles indicate the devices that experience switching losses.

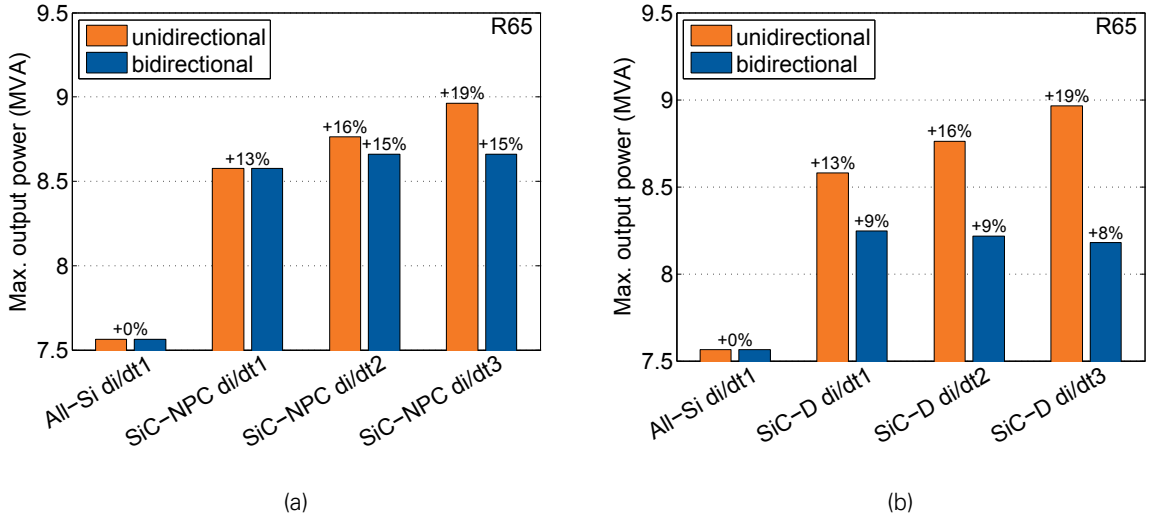
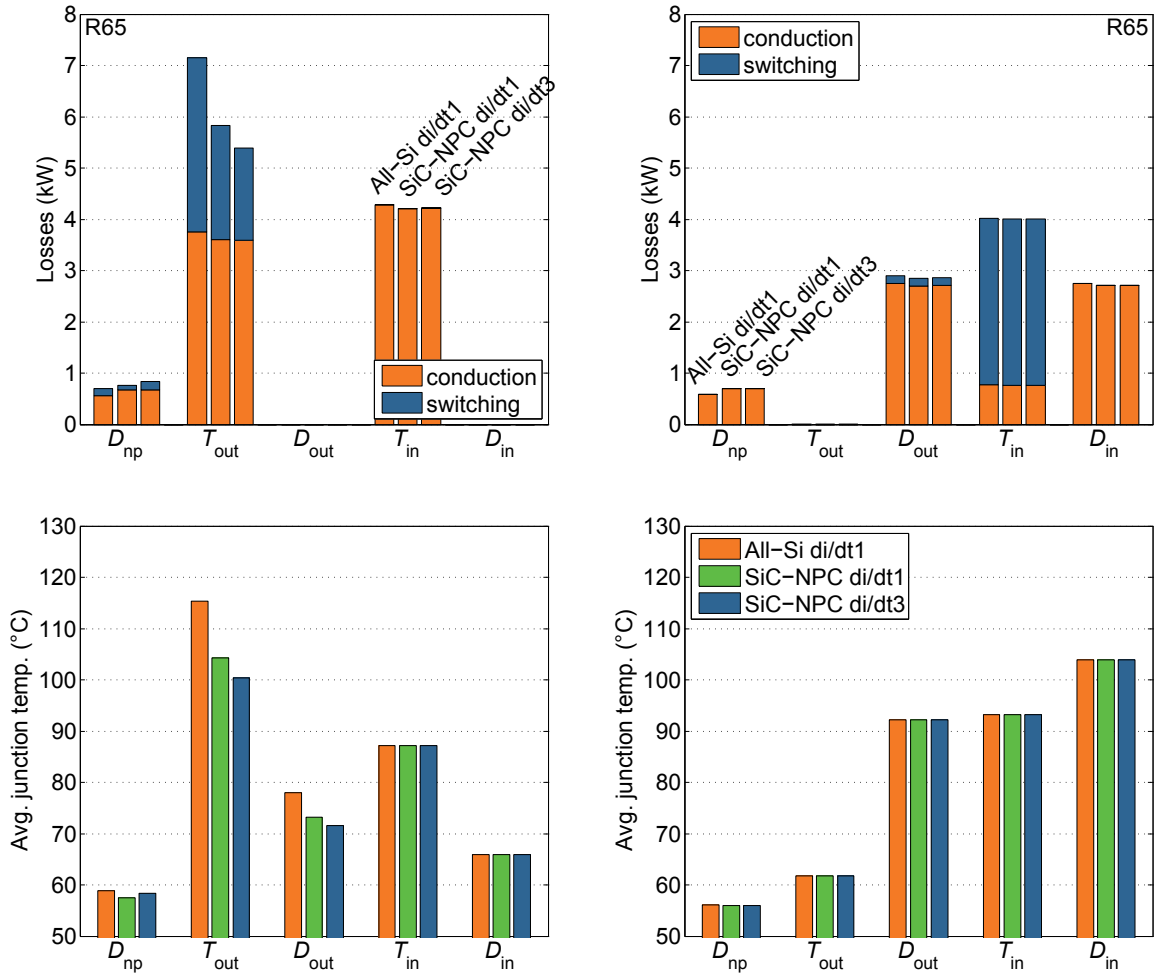


Figure 4.8: Maximum converter output power for the NPC converter with two parallel-connected 6.5-kV IGBTs as switches: (a) *R65 SiC-NPC* and (b) *R65 SiC-D* device configurations at different *di/dt* compared to *R65 All-Si*, considering unidirectional (OP1) and bidirectional (OP1 & OP2) energy flow. (f_{sw} = 465 Hz, V_{dc} = 6.2 kV)

ditional switching speed does not translate into a higher output power. This is so because for higher *di/dt* (*didt2*, *didt3*), the limiting device in the converter changes from T_{out} to D_{in}, on which the SiC NP diode does not have any influence, compare T_{out} in Fig. 4.9a and D_{in} in Fig. 4.9b.

4.4.2 SIC DIODE AS ANTIPARALLEL DIODE WITH 6.5-KV IGBTS *(R65 SIC-D)*

The next step after replacing the NP diodes by SiC diodes would be to integrate this technology in a hybrid Si-IGBT/SiC-diode module, as proposed by [46] and [137]. Using the data collected from the measurements of the FZ600R65KF2 and the SiC diode modules, a hybrid module con-



(a) OP1: $m_a = 1.15$, $\cos\varphi = 1$

(b) OP2: $m_a = 1.15$, $\cos\varphi = -1$

Figure 4.9: Total conduction and switching losses and average junction temperature distribution among each device group for *R65 SiC-NPC* compared to *R65 All-Si* device configuration. ($I_{out} = 1000\,A$, $f_{sw} = 465\,Hz$, $V_{dc} = 6.2\,kV$)

taining the 6.5-kV, 600-A IGBT and an antiparallel SiC PiN diode made of 40 dies was modelled and used in the converter simulations, see *R65 SiC-D* in Table 4.3.

The results for maximum converter output power are shown in Fig. 4.8b. For unidirectional current flow, the D_{out} diodes do not play any role in defining the maximum power, since T_{out} is the limiting device position. For bidirectional converters, the antiparallel SiC diodes have a negative effect, compare with Fig. 4.8a. The source of this behaviour can clearly be appreciated by comparing Figs. 4.9b and 4.10. The losses in D_{out} are not reduced, but increased, mostly due to the higher on-state voltage of the SiC PiN diodes. Moreover, the SiC diode has a 24% higher thermal resistance value between junction and case $R_{th,jc}$. As a consequence, the junction temperature of this diode is considerably higher, as Fig. 4.10 demonstrates, limiting the output power of the converter. One possible solution to this would be to take advantage of the high temperature operation of the SiC diode. In the prototype analysed here, the maximum junction temperature allowed is 125 °C, due to the use of standard module assembly technology. Moreover, enabling high temperature operation in a hybrid package is not simple, as the Si-based IGBT cannot be operated at a junction temperature over 125 °C. Larger thermal load cycles and their influence on the module's lifetime and reliability would also have to be

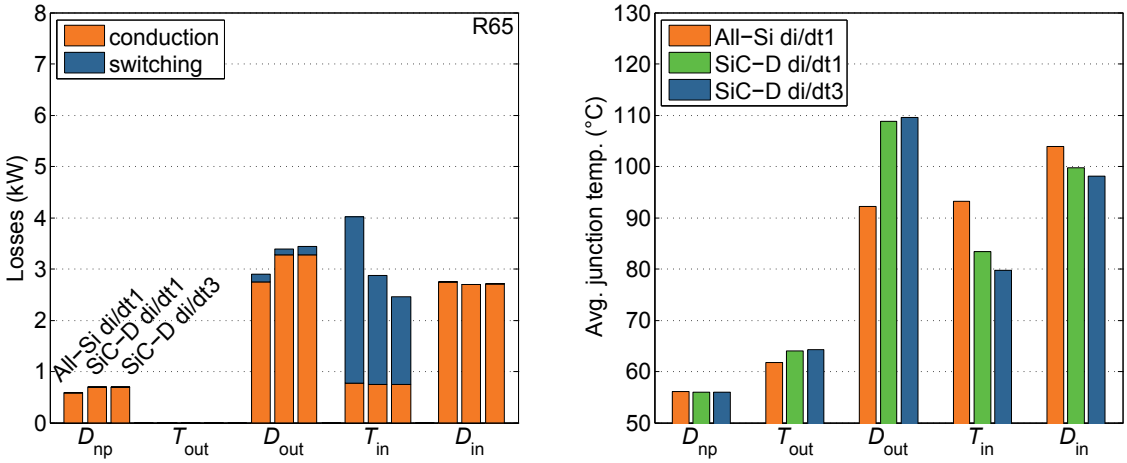


Figure 4.10: Total conduction and switching losses and average junction temperature distribution among each device group for *R65 SiC-D* compared to *R65 All-Si* device configuration at OP2: $m_a = 1.15$, $\cos\varphi = -1$. ($I_{out} = 1000\,A$, $f_{sw} = 465\,Hz$, $V_{dc} = 6.2\,kV$)

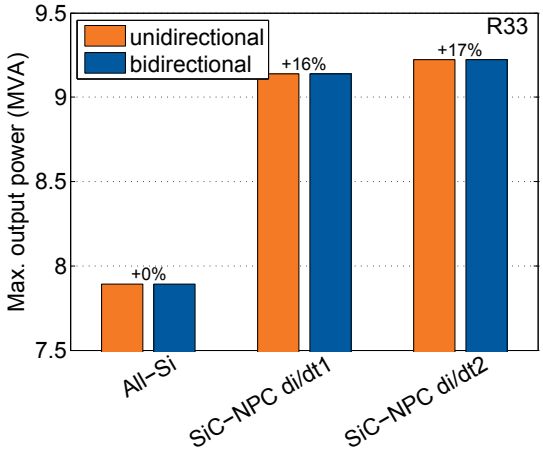


Figure 4.11: Maximum converter output power for an NPC converter with a series connection of two 3.3-kV IGBTs as switches, considering unidirectional (OP1) and bidirectional (OP1 & OP2) energy flow. ($f_{sw} = 465\,Hz$, $V_{dc} = 6.2\,kV$, $\vartheta_{j,max} = 120\,°C$)

considered.

4.4.3 SIC NP DIODE WITH 3.3-KV SI IGBTS *(R33 SIC-NPC)*

The SiC diode module was also investigated in combination with a series connection of two 3.3-kV IGBTs FZ1500R33HL3. The maximum converter output power for the configurations *R33 All-Si* and *R33 SiC-NPC* can be seen in Fig. 4.11. For this set of configurations, the power rating depends only on OP1, in both uni- and bidirectional cases. For the same *di/dt*, the SiC NP diode allowed an output power increase of 16% compared to the *All-Si* configuration. By turning on the IGBT at *di/dt2* (+10% compared to *di/dt1*), only a marginal increase of the output power can be achieved (+1%). Fig. 4.12 illustrates the loss and temperature distribution among the devices in the most critical operating point (OP1).

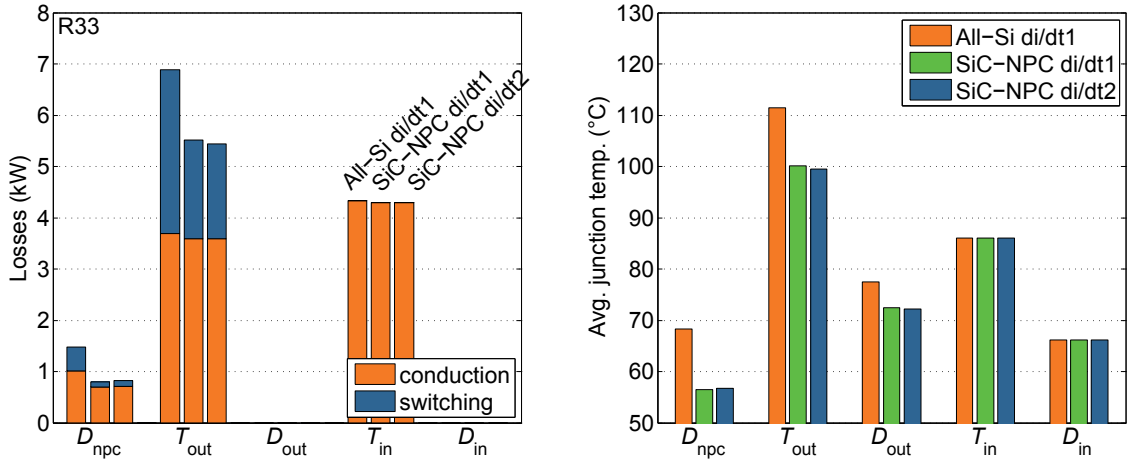


Figure 4.12: Total conduction and switching losses and average junction temperature distribution among each device group for *R33 SiC-D* compared to *R33 All-Si* device configuration at OP1: m_a = 1.15, cos φ = 1. (I_{out} = 1000 A, f_{sw} = 465 Hz, V_{dc} = 6.2 kV)

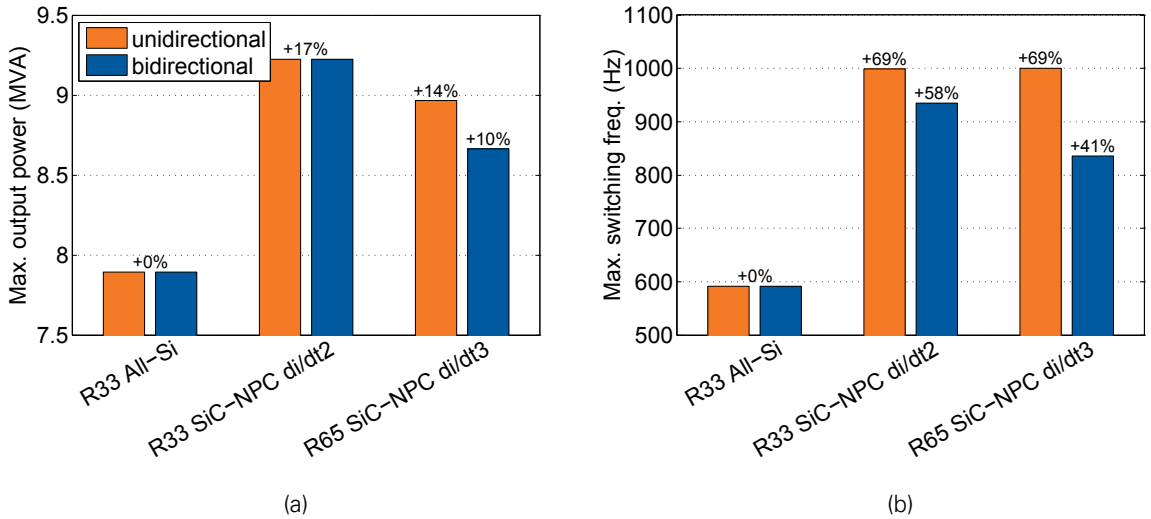


Figure 4.13: (a) Maximum converter output power and (b) switching frequency for an NPC converter with the best semiconductor configurations analysed, considering unidirectional (OP1) and bidirectional (OP1 & OP2) energy flow. ((a) f_{sw} = 465 Hz, (b) I_{out} = 1000 A, V_{dc} = 6.2 kV, $\vartheta_{j,max}$ = 120 °C)

4.4.4 BEST SEMICONDUCTOR DEVICE CONFIGURATIONS

The best device configurations analysed here are summarized in Fig. 4.13, for maximum converter output power as well as maximum switching frequency. An increase of 10% to 17% of the output power has been determined. Alternatively, the SiC diode performance can be used to increase the switching frequency by 41 to 69%. By comparing the cases *R33 SiC-NPC di/dt2* and *R65 SiC-NPC di/dt3*, the advantages of using 3.3-kV devices can be appreciated. Although the current change rate *R33 di/dt2* is considerably lower than *R65 di/dt3* (≈ –36%, see Fig. 4.4), the 3.3-kV device configuration achieves a higher output power. Better results could be achieved by increasing the *di/dt* to higher levels than the ones used here, as long as the overvoltages, oscillations and *dv/dt* values are acceptable.

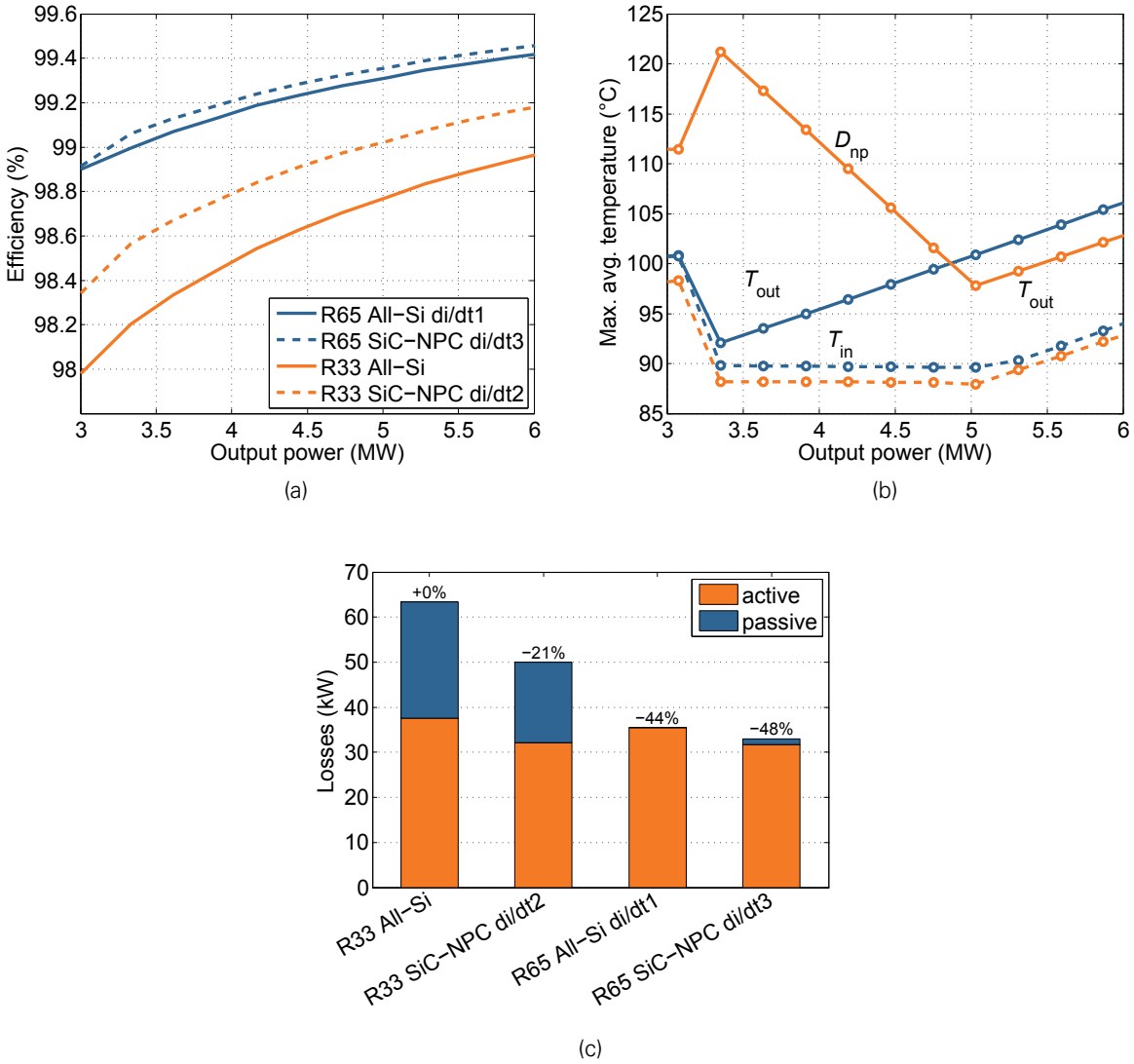


Figure 4.14: Efficiency of the 3L-NPC VSC for (a) the selected device configurations, (b) maximum average junction temperature of the hottest device and (c) total active and passive losses at max. modulation depth. (V_{dc} = 6.2 kV , I_{out} = 1000 A, $\cos\varphi$ = 0.85, f_{sw} = 465 Hz)

4.4.5 EFFICIENCY

Figure 4.14a indicates the efficiency of the 3L-NPC converter, depending on the device configuration used. For this calculation, the effect of *RC* snubbers and resistors for static balancing, in the case of the 3.3-kV IGBT configuration, was considered. For the current balancing of the parallel-connected 6.5-kV devices, non-dissipative static and dynamic balancing algorithms have been assumed [141, 143]. The maximum average junction temperature of the hottest device position in each semiconductor configuration can be found in Fig. 4.14b. The shift from one modulation scheme to the other occurs around 3.2 MW, which is why the temperature curves change abruptly in that point. In this figure the hottest device position for each configuration is indicated. It is clear that for high modulation depths (m_a > 0.9) the outer IGBTs T_{out} are the most stressed devices, no matter what kind of device configuration is selected.

Three different efficiency levels can be clearly distinguished. The lowest efficiency is achieved by the *R33 All-Si* configuration, which is mainly determined by the resistors needed for static

Table 4.6: Switching losses in a 3L-NPC VSC

i_{ph}	Comm.	T_{out1}	D_{out1}	T_{in1}	D_{in1}	T_{out2}	D_{out2}	T_{in2}	D_{in2}	D_{np1}	D_{np2}
>0	$+ \rightarrow 0$	×									
	$+ \leftarrow 0$	⊗								⊗	
	$0 \rightarrow -$			×							
	$0 \leftarrow -$			×			×				
<0	$+ \rightarrow 0$		×					×			
	$+ \leftarrow 0$							×			
	$0 \rightarrow -$					⊗					⊗
	$0 \leftarrow -$					×					

⊗: Reduced switching losses when using SiC D_{np} diodes.
×: Switching losses not affected by the SiC D_{np} diodes.
Diode turn-on losses have been neglected.

voltage sharing (in this case 11 kΩ/device). The combination *R33 SiC-NPC di/dt2* has a better performance, since the NP diodes do not require an additional circuit for static balancing. The highest efficiency is reached by 6.5-kV devices, where no extra elements are needed for balancing purposes. The small *RC* snubber required for the diode switching (9.4 or 14.1 nF, 4.7 Ω) has a negligible impact on the efficiency. The difference between *R65 All-Si di/dt1* and *R65 SiC-NPC di/dt3* is very low (≈0.05%), as it can be appreciated in the figure. The efficiency improvement by the use of SiC NP diodes is not large due to the low switching frequency used in the characteristic example for industrial applications (465 Hz) and the higher conduction losses in the SiC diode. However, even if the efficiency improvement is marginal, the main advantage of applying SiC diodes under these operating conditions lies in the possibility to increase the converter output power or frequency.

In order to better understand the influence of SiC devices and external passive snubber circuits in the converter efficiency Fig. 4.14c was elaborated. The losses for maximum modulation depth (m_a = 1.15) are plotted for each semiconductor configuration and divided into active and passive losses, where *active* stands for the losses in the device itself, and *passive* for the losses in external resistors (snubber R_s, static balance R_p). In the *R33* configurations, the resistors for voltage sharing are responsible for 36 to 41% of the total losses.

A reduction of 21% can be achieved with 3.3-kV devices, if 6.5-kV SiC NP diodes are used. In the case of *R65* configurations, the influence of the SiC NP diode in loss reduction is low, since both *R65* configurations *(All-Si, SiC-NPC)* do not need balancing resistors and the higher on-state voltage of the SiC NP compensates the switching loss reduction. The small *RC* snubber in *R65 SiC NPC* has a marginal contribution to the total losses.

4.5 INCREASED EFFICIENCY THROUGH MODEL PREDICTIVE CONTROL

As mentioned before in Sec. 4.4.1, in an NPC converter with SiC NP diodes and Si diodes and IGBTs in the inner and outer switches, the commutations that involve the turn-off of the NP diodes produce less switching losses than a commutation of an IGBT with a Si diode, as indicated in Tab. 4.6.

The idea of taking advantage of these *energy saving* commutations in such a converter by preferring them in the modulation algorithm has already been discussed in [144]. However, the modulation scheme proposed therein cannot adapt properly to the load conditions and works only in a limited range of the modulation index. As a part of this work, the use of model predictive

control (MPC) to generate the output voltage waveform considering the use SiC NP diodes to obtain higher efficiency was investigated. A comprehensive explanation of MPC in power electronics can be found in [145]. Due to space restrictions, only the essential information required to understand the algorithm will be explained here.

Preliminary simulations of an NPC converter with SiC NP diodes using MPC were presented in [146]. In the following sections, the MPC algorithm is explained and electrothermal simulation results of the converter are used to evaluate the performance at an exemplary OP. The new algorithm is compared to a converter working with a traditional sine-triangle modulation, as in Sec. 4.4. The aim of this section is to demonstrate the principle of using MPC to improve the efficiency by simulation and does not contemplate issues regarding the implementation of the algorithm in a real converter.

4.5.1 MPC ALGORITHM AND MODELS

The control method chosen corresponds to an MPC with finite control set with a predefined horizon in time $N = 1$ [145]. A converter and a load model are required in order to evaluate the cost function, which is the core of the MPC algorithm.

CONVERTER MODEL

The model of the converter is based on the space vector representation of the possible output voltages of the NPC converter. Each phase leg can generate three different voltage levels, which result in 5 levels in the line to line voltage waveform. The total number of switching states of the three-phase converter amounts to $m = 3^3 = 27$, which can be represented as 19 different space vectors that are arranged in two concentric hexagons, see [142, Fig. 2]. The outer hexagon contains no redundant states, whereas the inner hexagon has two possible switching states per vector. The null vector can be represented by three switching states.

LOAD MODEL

For the simulations a three-phase resistive-inductive load was used, which can be modelled as the following time-continuous transfer function in the Laplace domain

$$G(s) = \frac{\mathbf{i}_\mathrm{L}}{\mathbf{v}_\mathrm{conv}} = \frac{1}{sL + R}, \tag{4.3}$$

where $\mathbf{i}_\mathrm{L}$ and $\mathbf{v}_\mathrm{conv}$ are the space vectors of the load current and the converter output voltage, respectively, L the load inductance, and R the load resistance. s is the Laplace variable.

By using the Euler approximation it is possible to obtain a time-discrete model that can be implemented in the MPC algorithm:

$$\mathbf{i}_\mathrm{L}(k+1) = \left(1 - \frac{R}{f_\mathrm{s} L}\right) \mathbf{i}_\mathrm{L}(k) + \frac{\mathbf{v}_\mathrm{conv}(k)}{f_\mathrm{s} L}, \tag{4.4}$$

where $\mathbf{i}_\mathrm{L}(k+1)$ is the predicted load current at the next sampling instance, $\mathbf{i}_\mathrm{L}(k)$ and $\mathbf{v}_\mathrm{conv}(k)$ the measured load current and converter output voltage vector at the current sampling instance, respectively. f_s is the sampling frequency of the MPC algorithm.

COST FUNCTION

The cost function C used to evaluate the future switching state is

$$C = |\mathbf{i}_\mathrm{L}(k+1) - \mathbf{i}_\mathrm{ref}| + c_\mathrm{sw}, \tag{4.5}$$

where $\mathbf{i}_{\text{ref}}$ is the reference current of the MPC algorithm and c_{sw} is the cost factor that evaluates the future switching events,

$$c_{\text{sw}} = \begin{cases} 0 & \text{if no switching event occurs,} \\ k_1 & \text{if a switching event without SiC diode turn-off occurs,} \\ k_1 \cdot k_2 & \text{if a switching event involving a SiC diode turn-off occurs.} \end{cases} \tag{4.6}$$

The factors k_1 and k_2 are chosen according to the desired converter behaviour. That is,

- $k_1 \geq 0$, where higher values lead to a reduction of the switching frequency, and
- $0 \leq k_2 \leq 1$, where low values assign a lower cost to commutations involving a SiC diode turn-off, preferring them over other commutations.

MPC ALGORITHM

The MPC algorithm evaluates all the possible next switching states at each sampling instance. With the help of the cost function, the algorithm decides if a state change is necessary, and in case this is true, applied the state with the lowest cost. To achieve this, following steps are carried out consecutively every time the algorithm is called:

1. Out of all the possible switching states in the converter ($m = 27$), discard all the possible future switching states involving more than one switching action from the current state. [147]
2. Predict the future current $\mathbf{i}_{\text{L}}(k+1)$ using (4.4).
3. Calculate the cost function C with (4.5) for each of the possible switching states found in 1.
4. Apply the switching state which has the minimum cost.

4.5.2 SIMULATION RESULTS

For the simulations, an NPC inverter with the parameters listed in Tab. 4.7 was used. The power semiconductor configuration chosen was *R65 SiC-NPC di/dt3*, the switching frequency in the reference simulation with standard sine-triangle PWM was set to 750 Hz (frequency of the triangular carrier signal). The chosen sampling frequency f_{s} for the MPC algorithm of 6.5 kHz yields a comparable switching frequency between 720…840 Hz, as it will be shown later. With this power semiconductor configuration, the effect of the MPC algorithm can be observed more clearly, as the other configurations considering series-connected 3.3-kV devices showed no significant efficiency improvement.

SELECTION OF OPTIMAL WEIGHTING FACTORS

In order for the MPC algorithm to work properly, suitable weighting factors need to be found. The procedure applied to achieve this can be described as follows:

1. Simulations are carried out for the reference converter with standard sine-triangle PWM. Out of this simulations, values for the weighted total harmonic distortion (WTHD) of the output voltage, see (4.7), total semiconductor device losses $P_{\text{tot,sc}}$ (switching and conduction losses) and maximum device junction temperature $\vartheta_{\text{j,max}}$ are extracted, see Tab. 4.8.

$$\text{WTHD} = \sqrt{\sum_{h=2}^{h_{\max}} \left(\frac{V_{\text{out},h}}{h V_{\text{out},1}} \right)^2} \tag{4.7}$$

Table 4.7: Converter setup for MPC algorithm

Converter	
DC-link voltage V_{dc}	6177 V
Output voltage	4.16 kV
Output frequency	50 Hz
Output current I_{out}	1000 A
$\cos\varphi$	0.9
Heat sink temperature ϑ_h	50 °C
Semiconductor device config.	*R65 SiC-NPC di/dt3*
Sine-triangle modulation	
Switching frequency f_{sw}	750 Hz
Min. turn-on time	100 µs
3rd harmonic	1/6
Modulation index m_a	1.1
MPC algorithm	
Sampling frequency f_s	6500 Hz
Weighting factor k_1	0, 10, 20...300
Weighting factor k_2	0, 0.1, 0.2...1
Max. simulation time step	100 ns

Table 4.8: Performance of the MPC algorithm and comparison with sine-triangle modulation

	WTHD $h_{max} = 10^4$	$P_{tot,sc}$	$\vartheta_{j,max}$	f_{sw}	I_{out} (A)
MPC algorithm (60, 0.4)	0.96%	34.1 kW	98 °C	800 Hz	1002, 1009, 1005
MPC algorithm (0, 0)	1.04%	36.5 kW	107 °C	766 Hz	1002, 1009, 1005
Sine-triangle modulation	1.41%	36.1 kW	107 °C	750 Hz	1000, 1000, 1000

2. The same parameters that were calculated in step 1 are also calculated for the converter with MPC working with different k_1 and k_2 combinations.

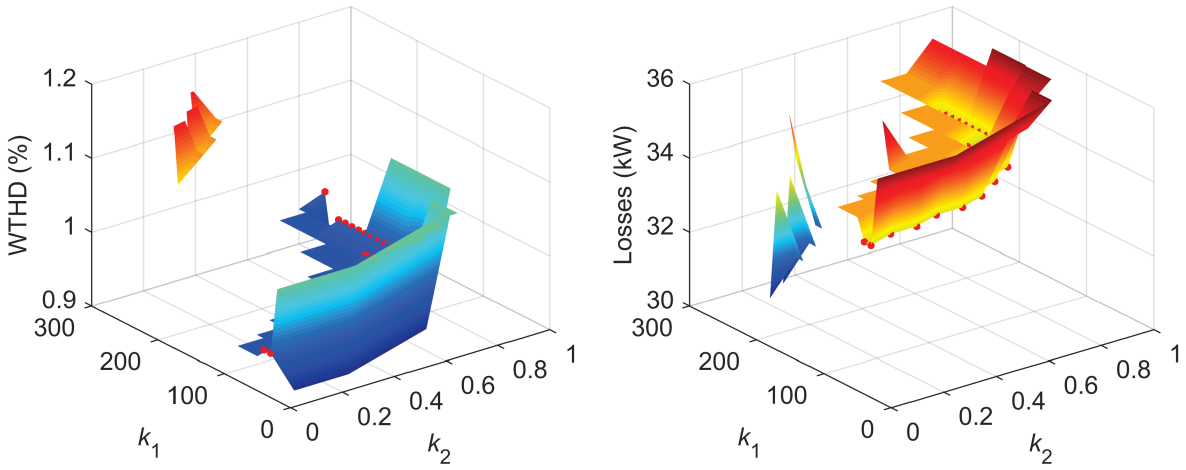
3. All the k_1, k_2 pairs that show higher WTHD and $P_{tot,sc}$ than the reference simulation of step 1 are excluded from further analysis, as they either worsen the output voltage waveform quality and/or decrease the converter efficiency. Fig. 4.15 shows the results of these calculations.

4. For the remaining weighting factor pairs, the calculated losses $P_{tot,sc}$ and WTHD are normalized, weighted and added to each other in a second cost function:

$$K = \frac{P_{tot,sc}}{P_{tot,sc,max}} + \frac{1}{2}\frac{WTHD}{WTHD_{max}} \tag{4.8}$$

   The minimum of K represents the optimum k_1, k_2 pairs, which are marked with a red dot in Fig. 4.15. The performance of the algorithm with one of the optimum pairs is summarized in Tab. 4.8.

Tab. 4.8 includes also the performance of the standard sine-triangle modulation for comparison purposes. Additionally, a simulation of the MPC algorithm with $c_{sw} = 0$ in (4.5) was performed ($k_1 = k_2 = 0$) to evaluate its performance without assigning a cost factor for the different



(a) WTHD of converter output voltage ($h_{max} = 10^4$)

(b) Semiconductor device losses

(c) Switching frequency

(d) Max. device junction temperature

Figure 4.15: Results of the weighting factor selection for the MPC algorithm, see Tab. 4.7 for simulation parameters.

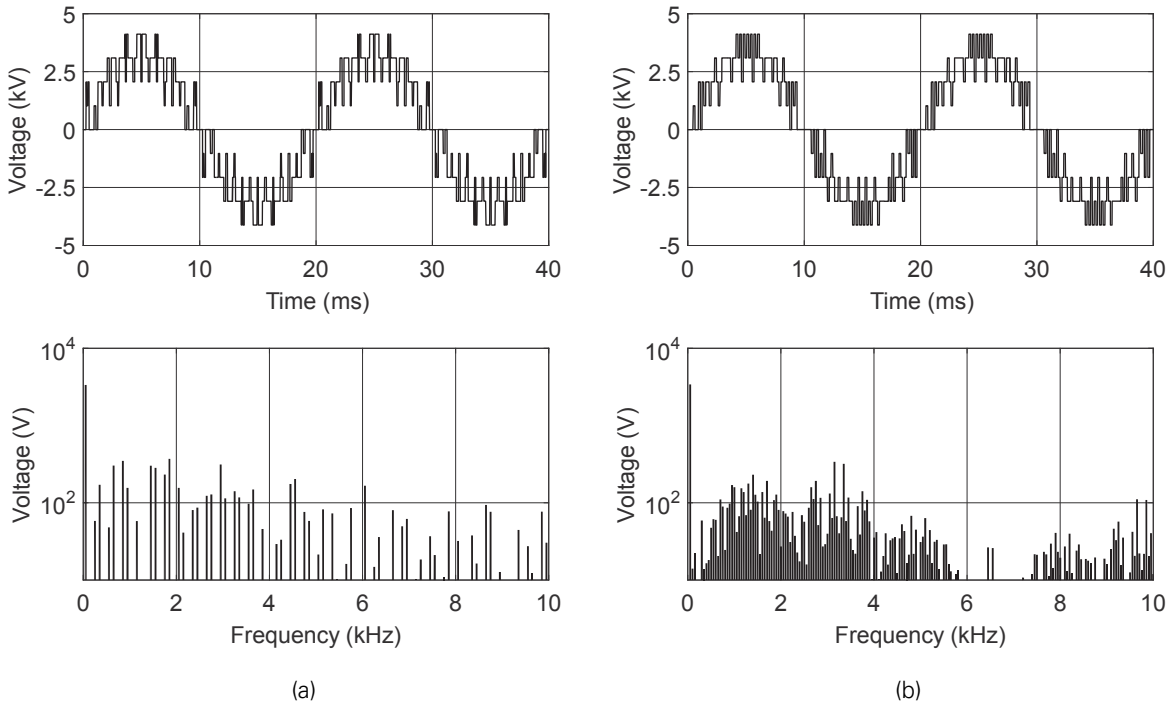


Figure 4.16: Output phase voltage waveforms of the converter with (a) standard sine-triangle modulation and (b) MPC algorithm for increased efficiency. (k_1 = 60, k_2 = 0.4, see Tab. 4.7 for simulation parameters.)

commutations. As expected, the algorithm using the pair (0, 0) achieves a better WTHD at the cost of higher losses and higher device temperature, which are comparable to the ones of the reference case with sine-triangle modulation.

OUTPUT WAVEFORM AND LOSS DISTRIBUTION

Once an optimum for the weighting factors has been found, it is possible to analyse the behaviour of the converter for that operating point and compare it to the standard sine-triangle modulation scheme. In this case, the pair (60, 0.4) was chosen for the simulations. The output phase voltage and frequency spectrum of both methods are shown in Fig. 4.16. The rms current of the fundamental component of each phase was also included in the table, as a way of showing the level of accuracy with which the algorithm can keep the reference value when operating with the studied weighting factors.

It can be seen that the waveform has a superior quality, which is reflected in the higher switching frequency f_{sw} and lower WTHD value. However, the quarter period symmetry obtained with classical sine-triangle modulation is lost when using MPC, as the $\cos\varphi$ value adds an asymmetry to the voltage waveform. This is also a reason for a more densely populated frequency spectrum, especially for $h < 40$. The sampling frequency f_s = 6500 Hz can also be clearly recognized in the frequency spectrum.

Regarding the total losses, these could be reduced by 5.5% compared to the reference simulation. By observing the loss distribution among the different device groups in one phase of the converter, as shown in Fig. 4.17, it is possible to gain some insight in the way the algorithm works. It has a clear impact on the switching losses of T_{out}, as these are reduced by 22%, with a slight increase of the conduction losses. In the case of the D_{np}, the switching losses are also reduced by 25%. The conduction losses slightly increase in the case of T_{in} and T_{out} but

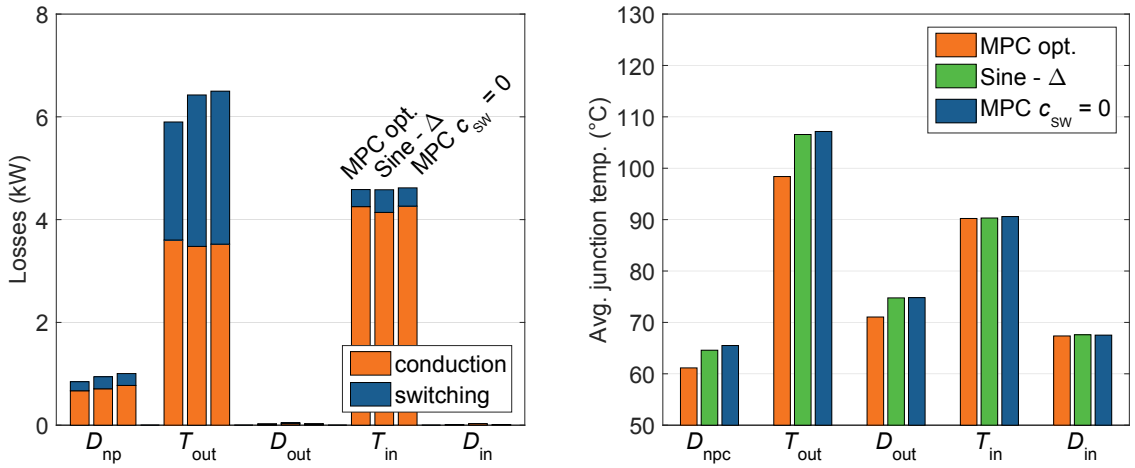


Figure 4.17: Total conduction and switching losses and average junction temperature distribution among each device group for the MPC algorithm at the optimum point (MPC) compared to the standard sine-triangle modulation method (Sine - Δ). (k_1 = 60, k_2 = 0.4, see Tab. 4.7 for simulation parameters.)

decrease for D_{np}. Hence, the algorithm forces the converter to stay longer in the positive and negative states and less in the zero state. The average junction temperatures of each device also reflect these changes. In the case of T_{out}, it is be reduced by 8 °C (–8%) and in 3 °C for D_{np}. The losses and junction temperatures of the MPC algorithm with c_{sw} = 0 are very similar to the ones obtained with the standard sine-triangle modulation.

Summarizing, it was demonstrated by electrothermal simulations that by tuning the MPC algorithm to an optimum regarding waveform quality and efficiency, a loss reduction in the semiconductors devices of 5.5% could be achieved, when compared to a standard sine-triangle modulation scheme. The waveform quality is also improved, as the WTHD is reduced from 1.41% to 0.96%. However, it is important to note that this is valid only for the chosen OP. Other operating conditions might require a readjustment of the weighting factors. For an evaluation of both modulation schemes also the frequency spectrum, the expense of an implementation as well as the requirements of the application must be considered.

4.6 SUMMARY

In this chapter, different semiconductor configurations considering 6.5-kV and 3.3-kV IGBTs in combination with SiC PiN diodes were investigated. In the application example of a 4.16-kV, 8-MVA 3L-NPC, an increase in the output power by 10 to 17% was estimated through simulations with measurement-based device loss models. Alternatively, an increase of the switching frequency by 41 to 69% could be achieved. A further increase of the output power or the switching frequency could eventually be achieved by using a higher *di/dt* during the IGBT turn-on and/or combining SiC technology with other improvements for 3L-NPC converters, such as the active NPC topology [140, 148].

The best device configuration consists of SiC diodes in the NP positions with the outer IGBTs (T_{out} in Fig. 4.3) turning on with an increased *di/dt* and the inner IGBTs T_{in} at normal speed. The switches can be either parallel-connected 6.5 kV or series-connected 3.3-kV IGBTs. The parallel connection, due to the absence of passive balancing circuits, achieves a higher efficiency. The series connection, however, achieves a higher output power and is superior for converters with bidirectional energy flow. A replacement of the inverse Si diodes inside the IGBT modules by SiC PiN diodes does not lead to a better performance regarding the maximum output power or

the switching frequency. In terms of efficiency, for the studied switching frequency (465 Hz), the influence of the SiC PiN diodes is marginal compared to that of the balancing circuits for the 3.3-kV devices.

Additionally, depending of the semiconductor device configuration, a further loss reduction without compromising waveform quality can also be possible by the use of an MPC algorithm that takes into account the reduced switching losses related to the SiC NP diodes. This was demonstrated byen electro-thermal simulations for the NPC converter using parallel connected 6.5-kV IGBT modules and SiC NP diodes, where a loss reduction of 5.5% and a WTHD reduction of 0.45% for the analysed OP were obtained.

The attractiveness of SiC PiN diodes could be increased in the future by new packaging technologies enabling higher junction temperatures, higher robustness (power and thermal cycling) and lower thermal resistances. Furthermore, improvements in the SiC bulk material and the SiC diode design process are important next steps to increase the competitiveness of medium-voltage SiC diodes [15].

5 CONCLUSION

There is a wide variety of medium-voltage converters available on the market. The requirements and constraints of the application and a cost-benefit analysis will define the type of converter to be used. There are some applications that demand high efficiency levels, high power density, or require a high waveform quality. Although the development of new topologies and devices for this field has experienced a constant development towards these goals in the last decades, the limits imposed by the Si material in the power devices put restrictions to the possible improvements. In the case of IGBTs and IGCTs, the maximum voltage class of commercial devices is 6.5 kV. In the case of IGBT modules, the performance of 6.5-kV devices is not as good as two 3.3-kV IGBTs connected in series, when considering the criteria of cost per converter output power [2]. Hence, 3.3-kV devices are preferred over 6.5-kV devices in most industrial medium-voltage converters. The additional losses caused by the use of additional passive elements to ensure voltage sharing have an impact on efficiency that is not negligible. The space needed for the cooling of the extra resistors puts also limitations on the converter design.

Another common problem in medium-voltage drives is the unequal temperature distribution among the power semiconductors. Multilevel topologies are often used to achieve high output voltages (e.g. 2.3...7.2 kV). Although the voltage requirements of each device can be reduced considerably when compared to a classical two-level topology, the stress in the devices is not equally distributed and depends on the operating point of the converter. The maximum output power is determined by the hottest device in the most critical operating point. In the case of the NPC converter topology, two devices are usually the ones that limit the converter power. One approach to improve the temperature distribution among the devices is the active NPC topology. With the addition of two active switches it is possible to change the commutation path in such a way that the losses are distributed among other devices [148].

Another way of reducing the stress in the power devices is to use new technologies such a SiC-based semiconductors. The steady evolution of SiC devices has lead to the first prototypes for medium-voltage, high-power converters, such as the device studied in this thesis. It is a PiN diode module with nominal ratings of 6.5 kV and 1 kA. Compared to Si-based 6.5-kV diodes, the new diode offers some advantages that are attractive for the application in medium-voltage converters. As the module characterization demonstrated, the SiC diode offers improved switching properties, although a higher on-state voltage due to the higher band gap has to be accepted. The switching loss reduction in the IGBT that commutates with the SiC diode is an important advantage of using these type of diodes.

When replacing the NP diodes in a 3L-NPC converter by the studied SiC diodes (only two devices out of the 6 diodes and 4 IGBTs required for one phase leg), the losses in the associated IGBT are reduced in such a way that it is possible to increase the output power of the converter. Simulations of a 3L-NPC converter based on electrothermal models of 3.3-kV and 6.5-kV devices indicated that an increase of 17% in the output power or of 69% in the switching

frequency is possible. Depending on the semiconductor configuration chosen, a further efficiency improvement can be achieved by applying an MPC algorithm that considers the reduced switching losses of the SiC NP diodes.

However, the development stage of this devices is still not mature enough for commercial applications. Several challenges in the design of reliable devices are still unsolved or the solutions remain prohibitively expensive. The attractiveness of SiC PiN diodes could be increased in the future by new packaging technologies enabling higher junction temperatures, higher robustness (power and thermal cycling) and better thermal coupling. Furthermore, improvements of the SiC bulk material quality and the SiC diode manufacturing process are important next steps to increase the competitiveness of medium-voltage SiC devices [15]. With the characterization and analysis performed for this thesis it is possible to assess the advantages of the SiC diode module considered.

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