Zuverlässigkeit 3D-integrierter Chips: Die Rolle metallischer Oberflächen und Grenzflächen

Reliability of 3D-integrated chips:
The role of metallic surfaces and interfaces

Ehrenfried Zschech,
Fraunhofer IZFP Dresden
Fraunhofer Cluster Nanoanalysis Dresden

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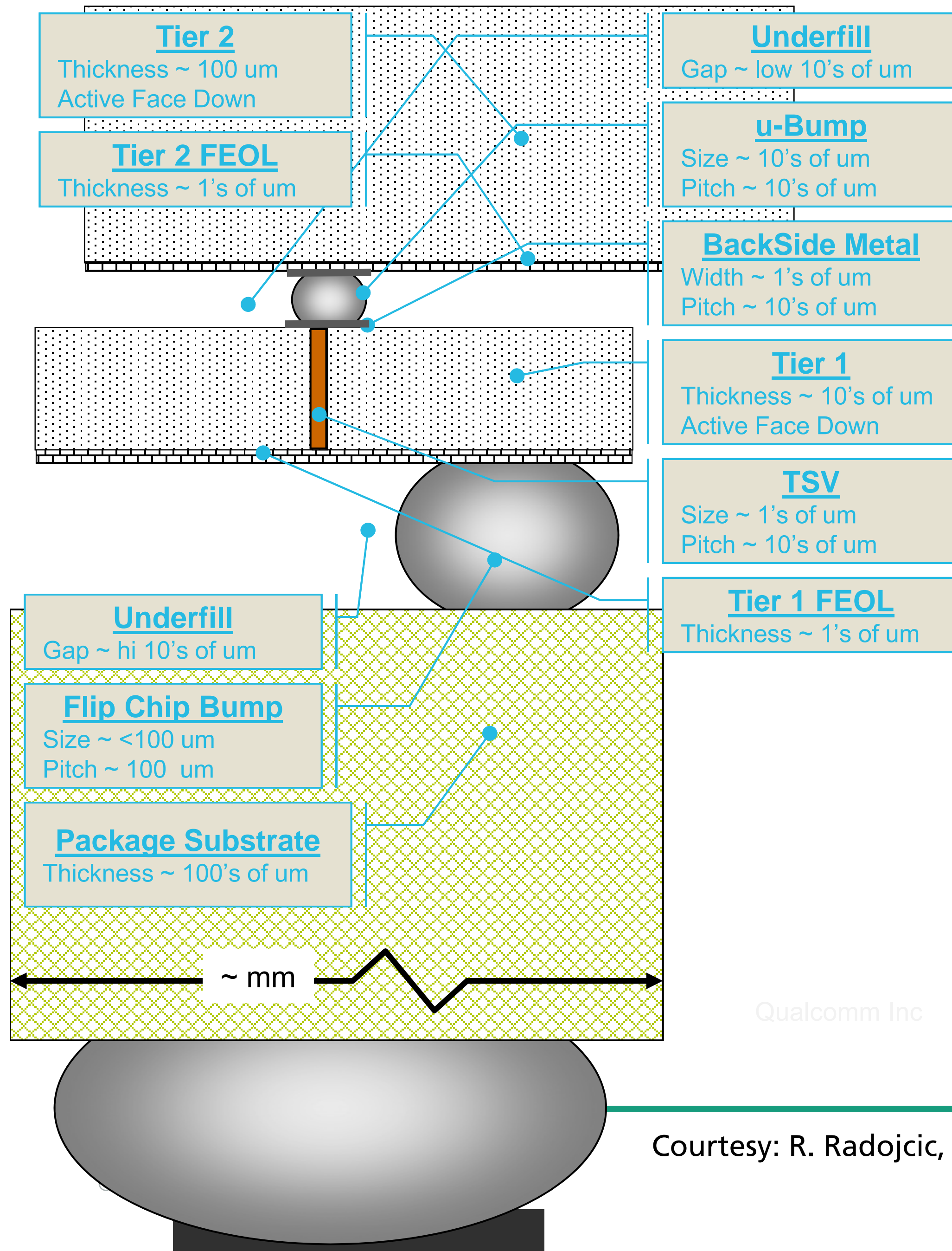
3D TSV scheme



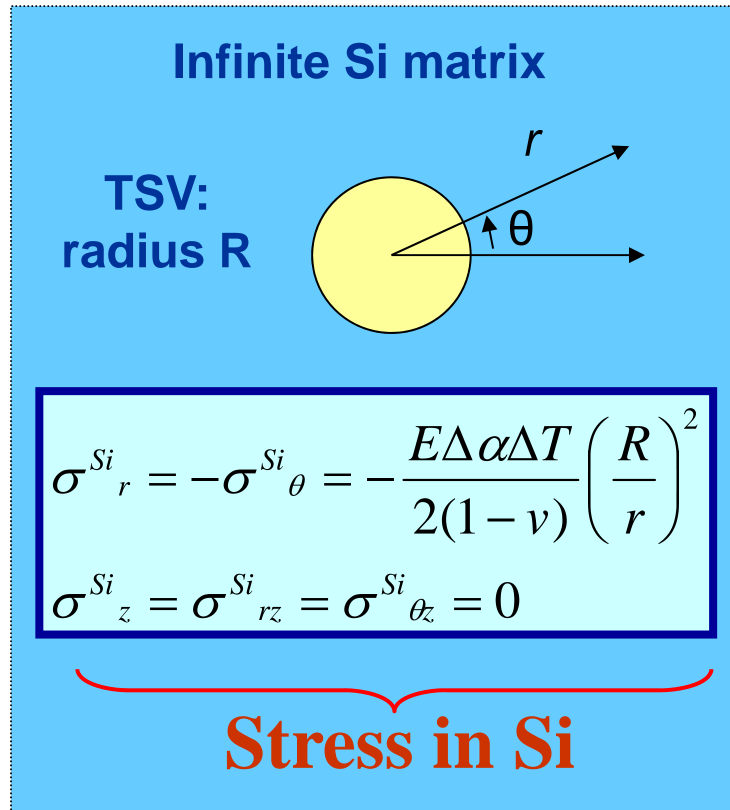
Integrated Heterogeneous 2-Die Stack

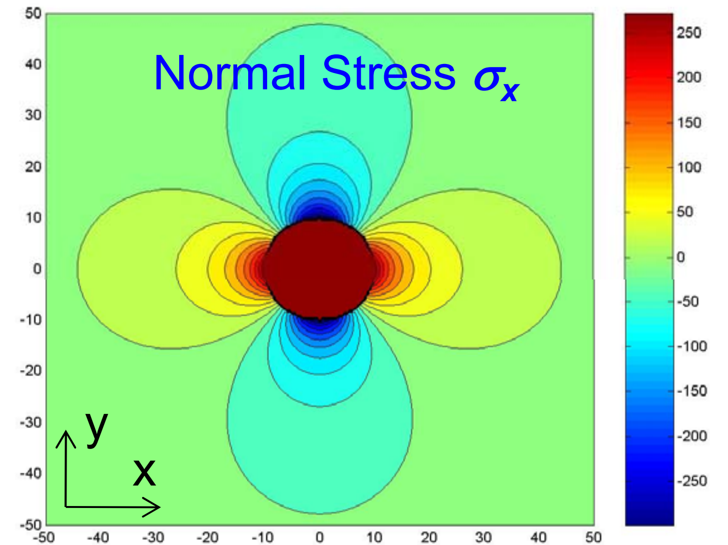
- **Tier 1 : CMOS Logic SoC**
  - TSV (connect frontside to backside)
  - Very thin Wafer (manage TSV aspect ratio)
  - Active face down
- **Interface μ-Bump**
  - Backside RDL Metal (interface to μBump and/or routing to allow offset of μBump vs TSV)
  - μ-Bump (Tier to Tier interconnect)
  - Very thin underfill
- **Tier 2 : Commercial Die**
  - Memory or Analog die, or…
  - Frontside Metal (interface to μBump)
  - Active face down & Pretty Thin
- **Flip Chip (C4) Bump**
  - Regular flip chip bump
  - Regular underfill
- **Package**
  - Regular PCB substrate
  - Regular plastic molding
  - Regular Package BGA Bump

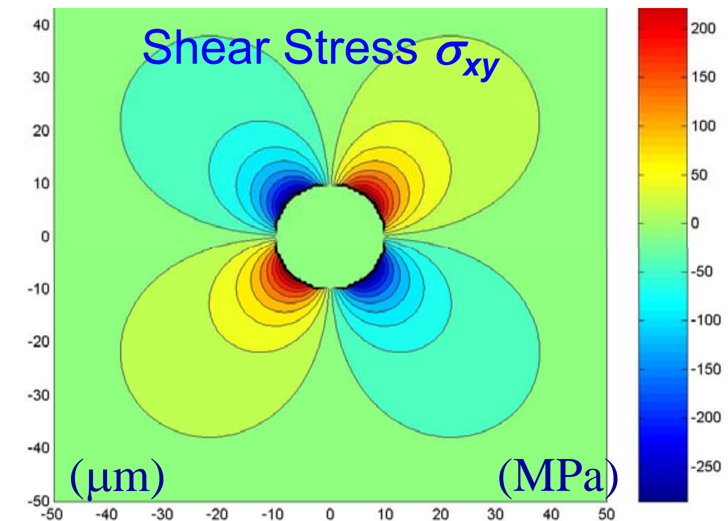
Courtesy: R. Radojcic, Qualcomm

2D stress solution of single TSV

No elastic mismatch between Si and Cu







Stresses controlled by CTE mismatch between TSV and Si; via size, material and T important.

P. S. Ho

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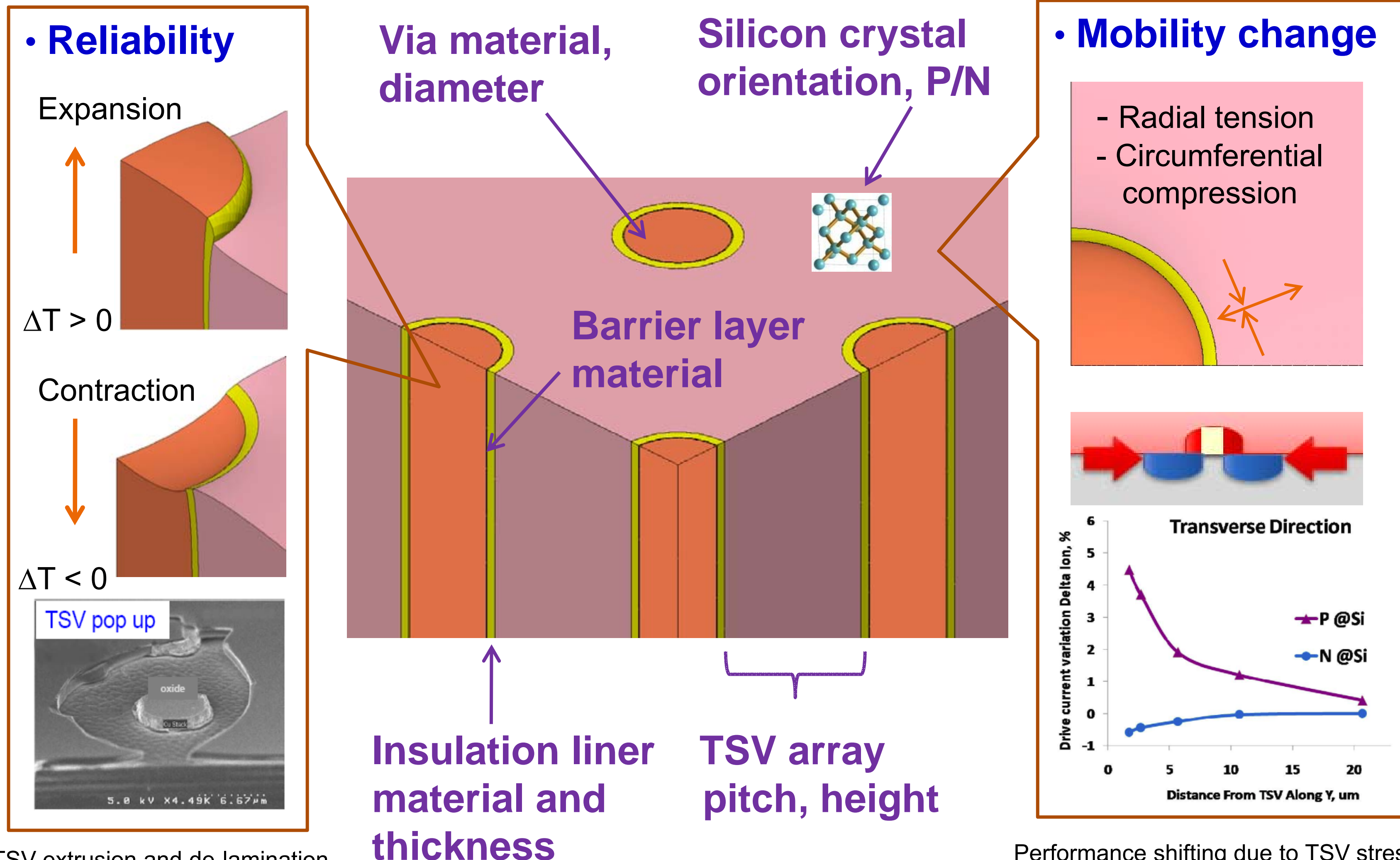
TSV performance and reliability risks



TSV extrusion and de-lamination
- P. Ho, RTI 3D Symposium 2009

Performance shifting due to TSV stress
- IMEC, VLSI 2010

Courtesy: Xiaopeng Xu, Synopsys

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Stress engineering in 3D IC structures: Need of database and input for database: Multi-scale materials data

Stress-related phenomena caused by 3D TSV integration can influence chip performance (and variability), yield and reliability.

Stress management in complex systems (packaged dies, 3D integration, etc.) requires multi-scale modeling, including accurate MULTI-SCALE MATERIALS DATA

- **Input data for simulation**
- **Model validation (and calibration)**

➔ Multi-scale materials database concept [1]

- Global and local materials data for wafer-level and package-level structures require MULTI-SCALE MATERIALS CHARACTERIZATION

- **Multi-scale (thermo-)mechanical materials data**
- **Strain in transistor channel**

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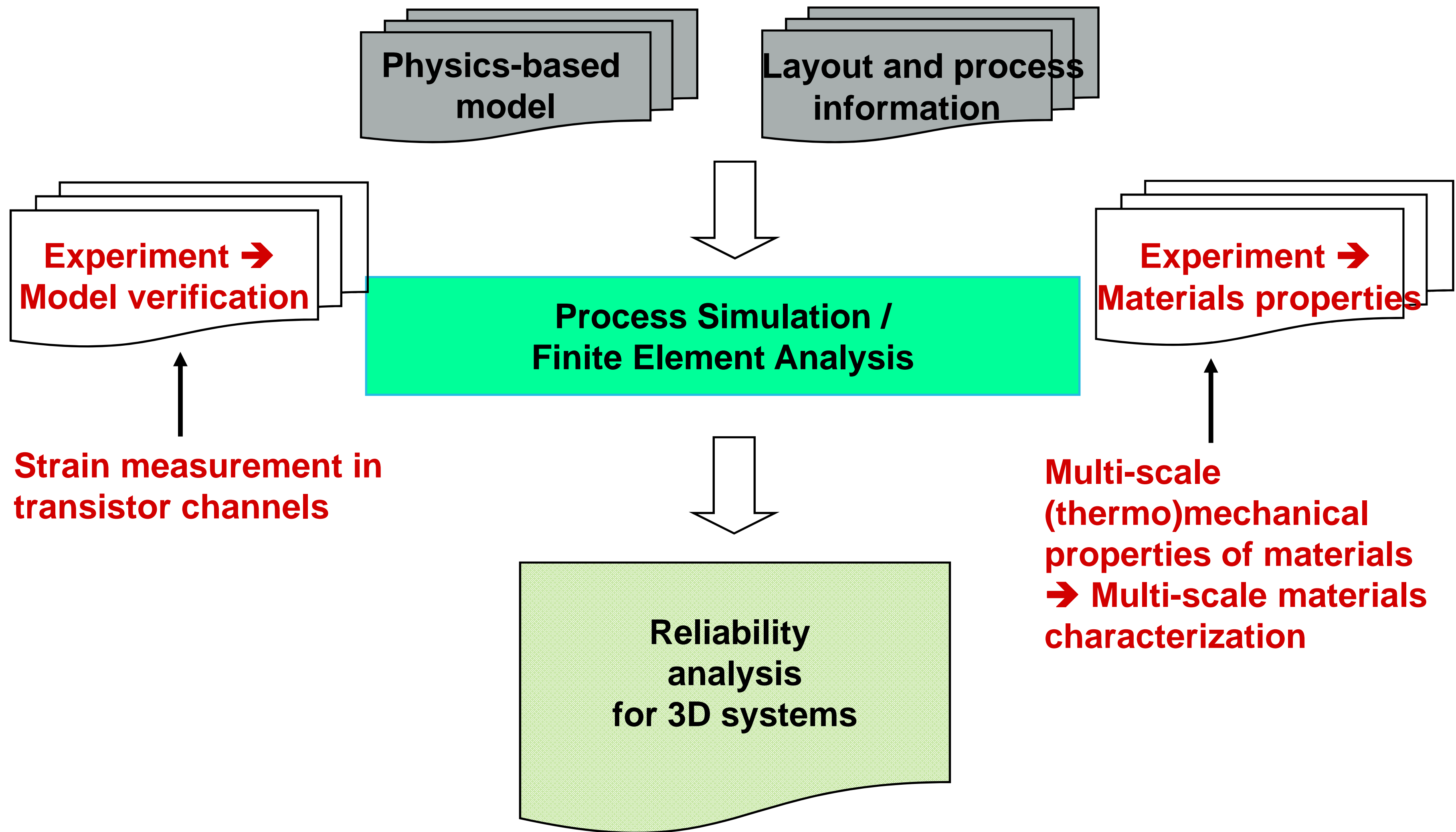
[1] V. Sukharev, E. Zschech, Int. Workshop "Stress Management for 3D ICs using Through Silicon Vias", Albany/NY 2010, AIP Proc. 1378, pp. 21 – 49 (2011)

Reliability assessment for 3D IC systems



E. Zschech et al., MRS Spring 2012

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Database information: Packaging materials

Materials	Temperature dependent	Underfill	Cu pillars	Molding compound	Flip-Chip ball (~ 100µm)	Micro ball (10s of µm)	BGA bump (>200µm)	Effective interconnect (low-k/Cu)	Effective bulk of silicon die (Si/Cu-TSV)	Effective package substrate (PCB/Cu)
CTE (ppm/K)	yes	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**
Young's modulus (GPa)	yes	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**
Poisson's ratio	no	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**
Plasticity (MPa)	yes		**x**							
Visco-plasticity (MPa)	yes				**x**	**x**	**x**			
Visco-elasticity (MPa)	yes	**x**		**x**						**x**
Glass transition Tg (°C)	no									**x**
Die attach Ta (°C)	no		x		x	x	x			

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Database information: Wafer-level materials

Materials	Cu (BEoL)	ULK	Cu (TSV)	SiO_2 Liner	Barrier	Si	BRDL
CTE (ppm/K)	x	x	x			x	x
Young's modulus (GPa)	x	x	x	x	x	x	x
Plasticity (MPa)			x				x
Poisson's ratio	x	x	x	x	x	x	x

+ adhesion

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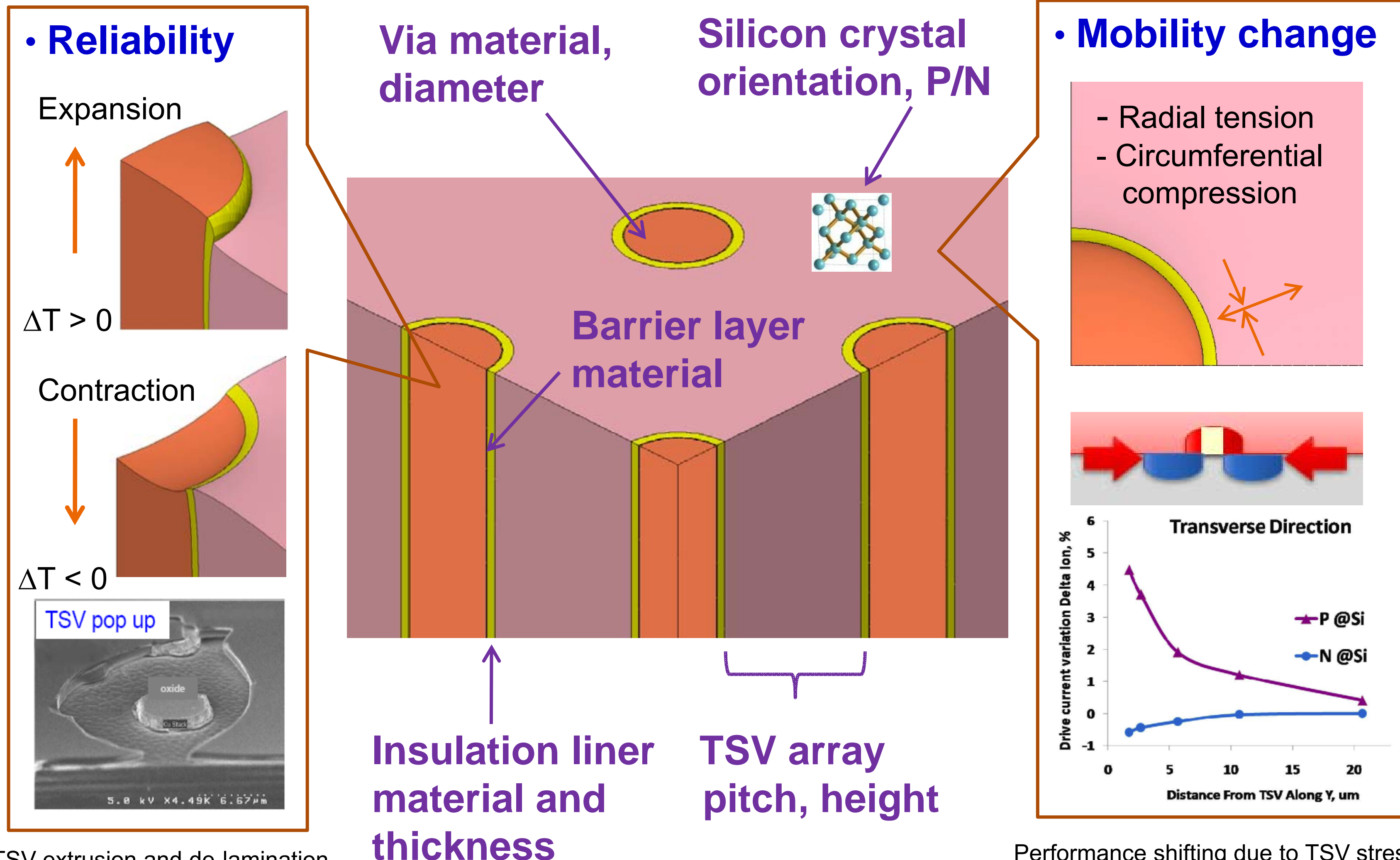
TSV performance and reliability risks



TSV extrusion and de-lamination
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Performance shifting due to TSV stress
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Courtesy: Xiaopeng Xu, Synopsys

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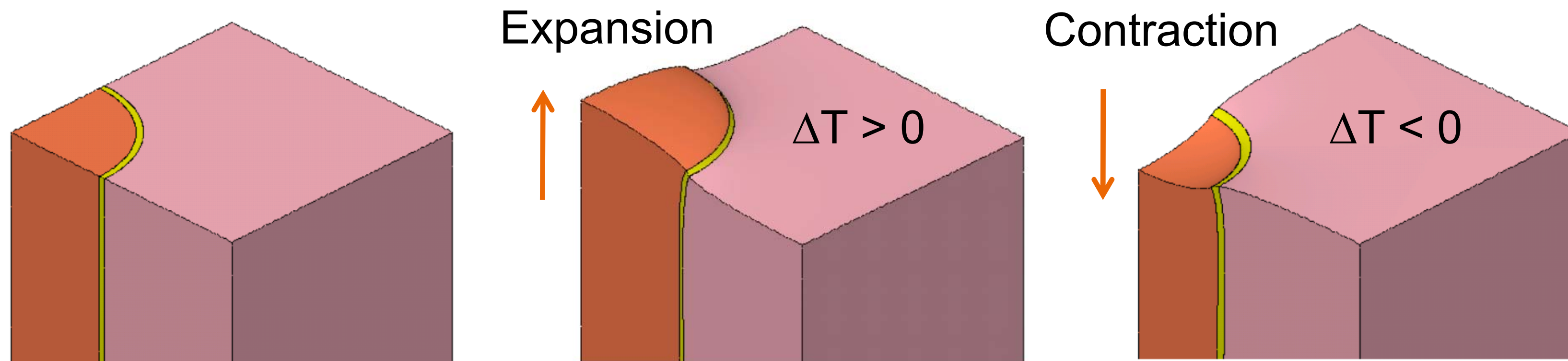
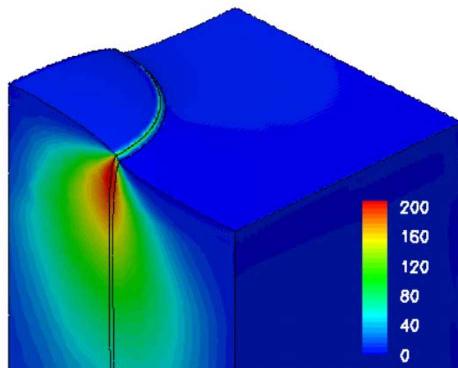
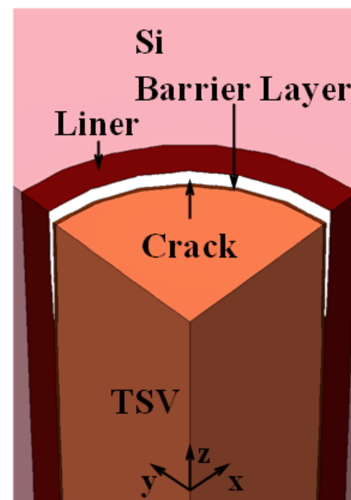
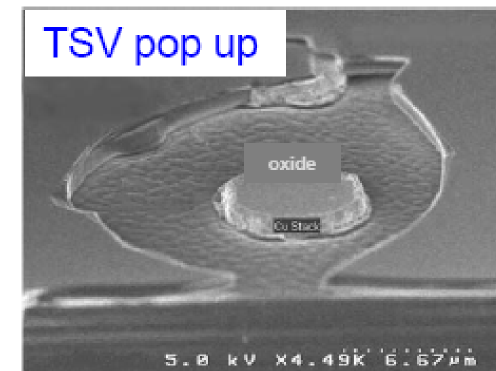
Thermal stress induced TSV pop-up





Shear Stress (MPa)





Large shear stress at Cu-TSV/Si-wafer interface and poor adhesion leads to de-bonding !

Courtesy: Xiaopeng Xu, Synopsys

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3D IC Integration: Quality engineering / failure analysis needs – Interface delamination and "pop-up"

- **Adhesive failure:**

  Interface delamination and „pop-up" only occurs if the adhesion Si/SiO_2(liner)/barrier*/copper is low !

  * TaN/Ta, TiN/Ti, (Ru), …

Which is the right analytical technique for delamination detection and quantitative „pop-up" evaluation?

- **nondestructive**
- **sub-100nm spatial resolution**

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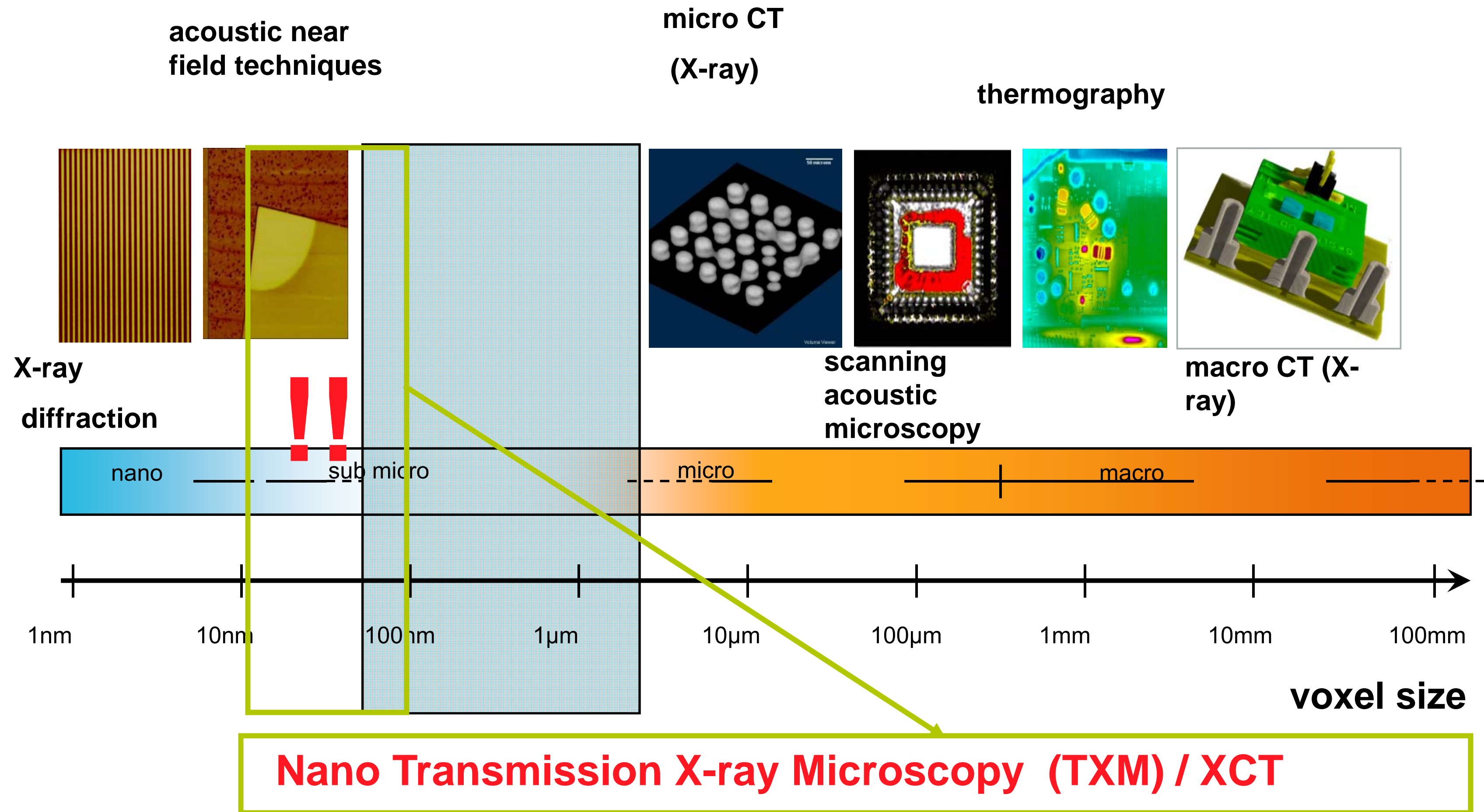
Classification of NDE techniques



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Comparison of imaging tools

Feature	X-ray	Optical	SEM	TEM
Spatial resolution	Current: 20-30 nm Ultimate: ~1 nm?	200-300 nm	1-10 nm typically >500 nm for elemental analysis	0.1 nm
Elemental sensitivity	Good (absorption edges + fluorescence)	None (labels)	Good (EDX)	Good (EDX, EELS)
Probing depth	1-50 μm for E<10 keV, 20 mm for E=100 keV	<100 nm for metal, opaque or transparent materials	< 10 nm typically < 3000 nm for element analysis	~ 100 nm
Material class	all	all	all (charging for nonconducting samples)	all (charging for nonconducting samples)
Vacuum requirement	No (multi-keV) Yes (low-E, cryo)	No	Yes	Yes
Radiation damage	modest	None (bleaching)	High	High

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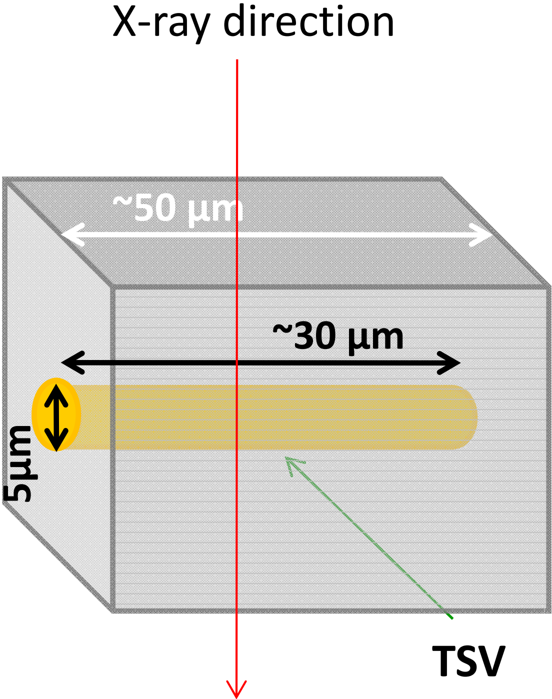
X-ray transmission in Si/Cu structures



Material	Density (g/cm³)	Absorption Length (µm)	Transmission(%)		
			50µm	30µm	5µm
Silicon	2.33	70.82	49.4	65.5	93.2
Copper	8.96	22.89	10.6	26	79.9

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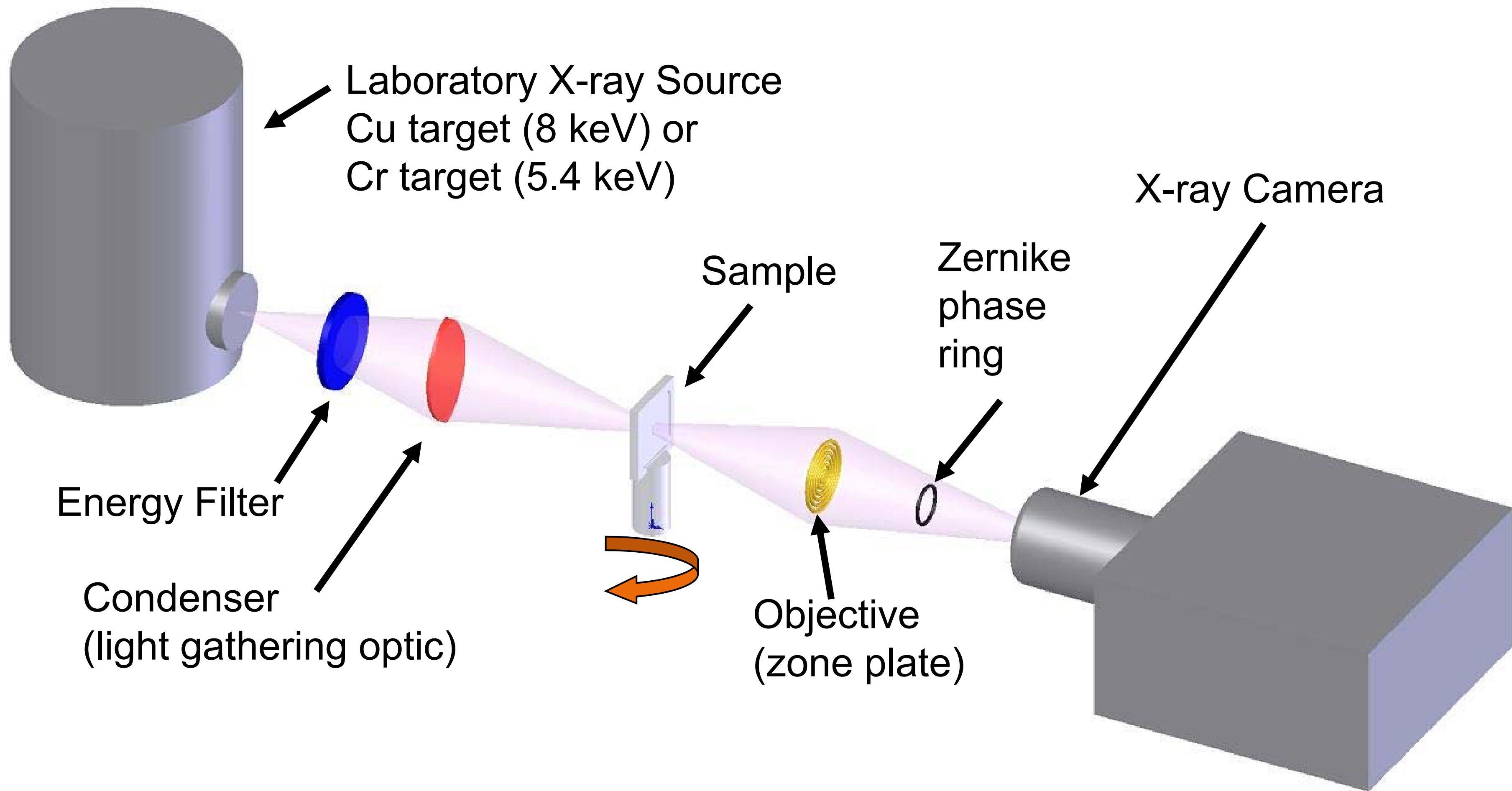
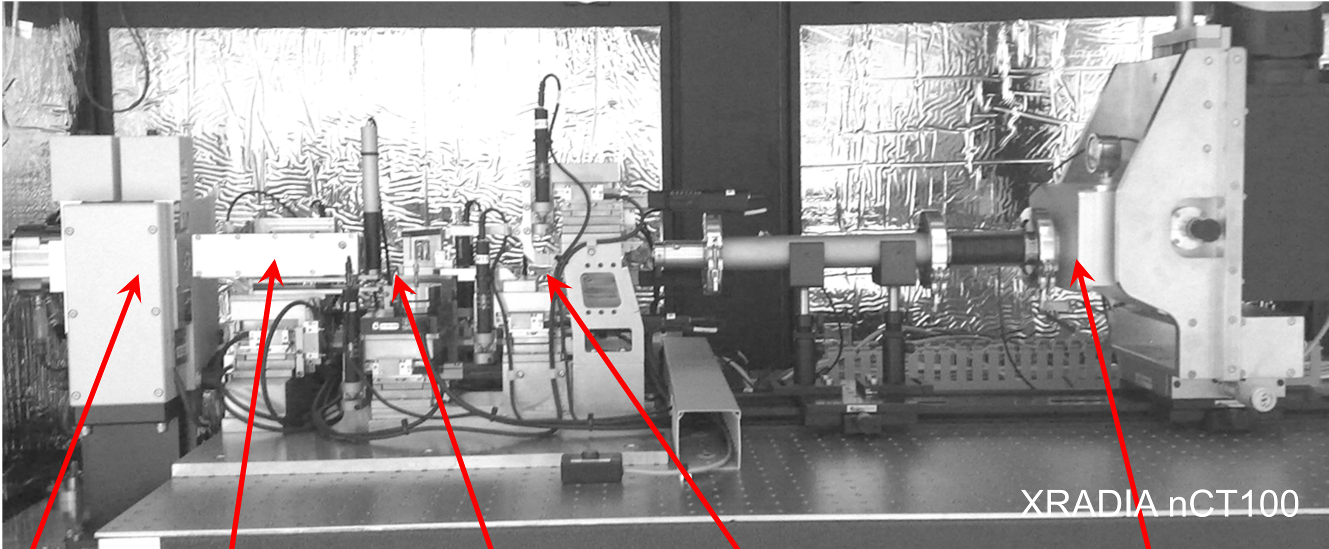
Xradia NanoXCT: Lab based X-ray microscopy



Courtesy: Xradia Inc., Concord/CA

Xradia nanoXCT @ Fraunhofer IZFP Dresden



X-ray tube

Collimator

specimen

lens

imaging system

about 30 motors

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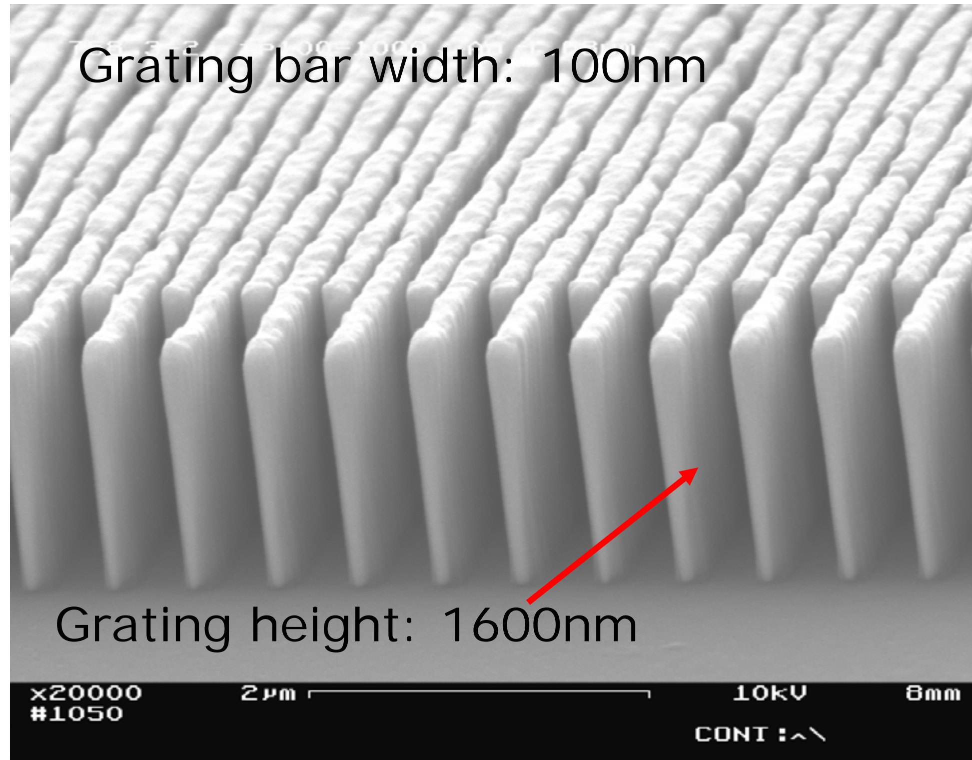
Limits of zone plates: ~ 30 nm structures



Zone plates are fabricated out of high-Z (typically gold) material using electron beam lithography, reactive ion etching and electroplating.

Focusing efficiencies 10-30% currently achievable (depends on A/R).

E. Zschech, W. Yun, G. Schneider, Appl. Phys. A 92, 423 – 429 (2008)
Courtesy: Xradia Inc., Concord/CA

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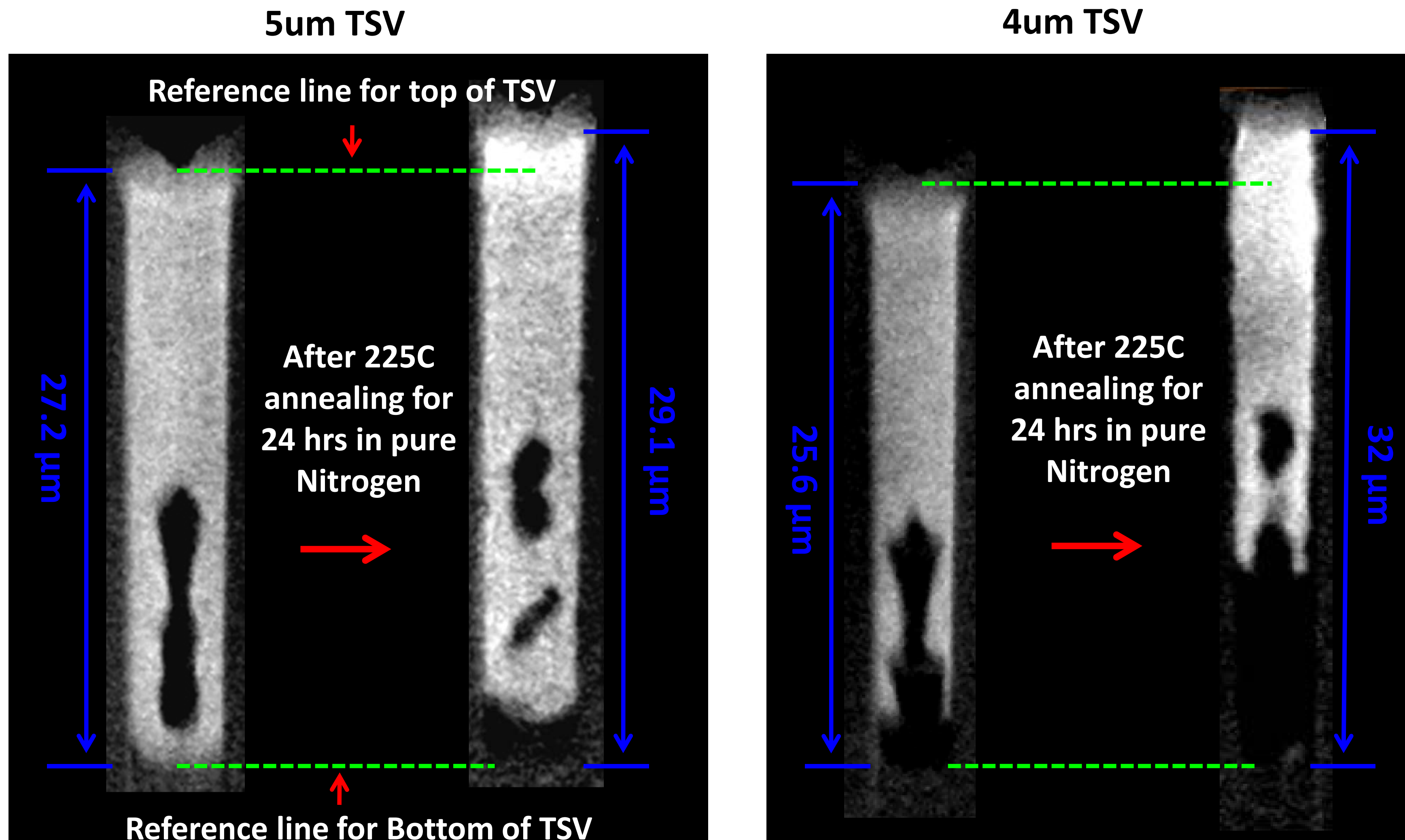
Cu TSV extrusions – Quantitative analysis (1)



Both 4 and 5um TSV show Copper is extruded and with de-lamination at the wall

Copperation with Lay Wai Kong and Alain Diebold, College of Nanoscale Science and Engineering at the University at Albany/NY, Lay Wai Kong et al., 3D IC Metrology Workshop @ Semicon West 2010

Reliability of 3D-integrated chips:
The role of metallic surfaces and interfaces

Reliability of 3D stacked ICs depends strongly on materials compatibility and stress.

Stress engineering is necessary to ensure the required product performance and reliability. Multi-scale simulations needs multi-scale materials input data.

Barrier quality, including homogeneity and surface, determine the interface energy and the adhesion of Cu-TSV/Si-wafer structures.

Failure analysis and the study of damage mechanisms like “pop-up” require nondestructive analysis techniques. Nano-XCT allows studies of Through Silicon Vias in 3D stacked Ics, including quantitative “pop-up” effect.

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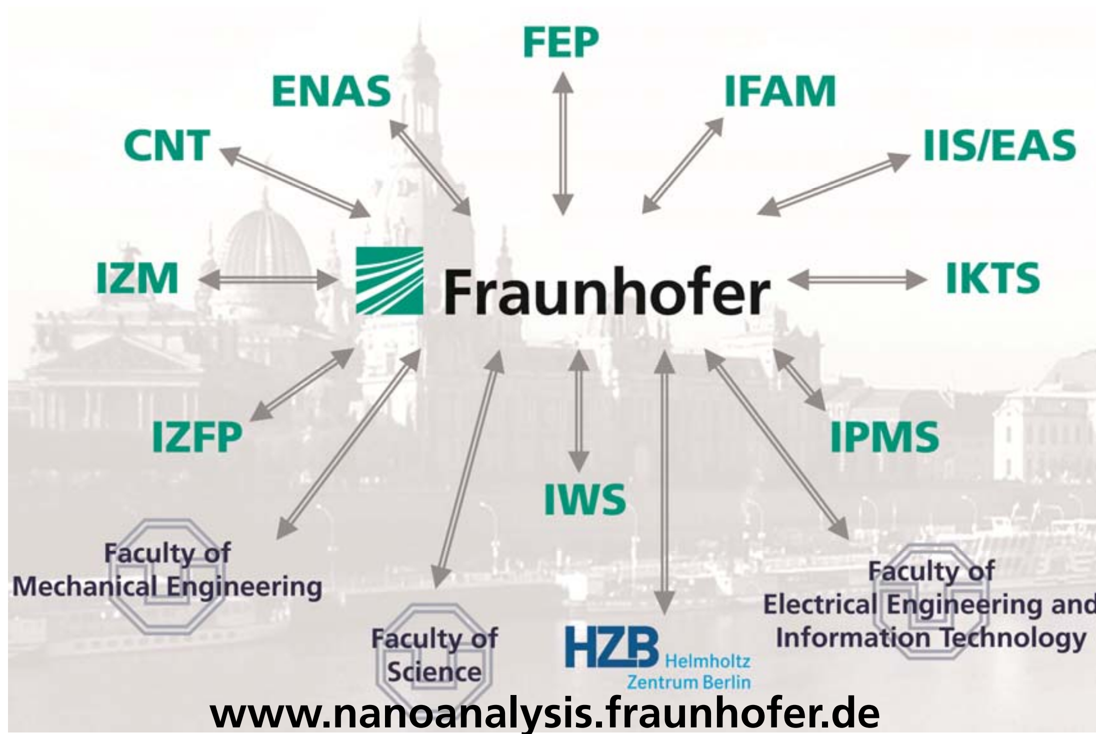
Thank you!



Sven Niese, Peter Krüger
Fraunhofer IZFP Dresden

Jeff Gelb, Kevin Fahey, *Xradia*

Contact: ehrenfried.zschech@izfp-d.fraunhofer.de

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