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Organic Electronic Devices - Fundamentals, Applications, and Novel Concepts

Dissertation

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Kurzdarstellung

Im Rahmen dieser Arbeit werden zwei grundlegende Problemstellungen elektronischer Bauelemente basierend auf organischen Halbleitern diskutiert. Zum einen wird die Kontrollierbarkeit und Einstellbarkeit der Bauelementcharakterisitiken untersucht, und zum anderen wird die Anwendung skalierbarer Integrationstechniken auf horizontale Dünnschichttransistoren und neuartige vertikale Transistoren erörtert. Die beiden genannten Aspekte sind von zentraler Bedeutung im Hinblick auf den Erfolg einer zukünftigen transparenten und flexiblen Elektronik basierend auf organischen Halbleitern.

Zunächst wird die statische Situation in molekular dotierten organischen pin-Dioden erörtert. Wichtige Bauelementparameter wie beispielsweise die Verarmungszonenkapazität, die Dichte der ionisierten Dotanden und die Durchbruchspannung für organische Zener Dioden werden bestimmt. Dieses essentielle Wissen wird in einem weiteren Schritt genutzt, um organische Dioden für Anwendungen im Ultra-Hoch-Frequenz-Bereich zu optimieren. Insbesondere wird gezeigt, dass durch eine geeignete Anpassung der Diodenfläche, der Schichtdicken, und der Dotierungsverhältnisse die Grenzfrequenz solcher pin-Dioden bis in den Bereich um $1 GHz$ geschoben werden kann.

Im zweiten Teil dieser Arbeit stehen organische Dünnschichttransistoren, hochauflösende Integrationstechniken, sowie Konzepte für neuartige vertikale Transistoren im Mittelpunkt des Interesses. Insbesondere wird eine photo-lithographische Strukturierungstechnik basierend auf hoch-fluorierten Photolacken und Lösungsmitteln vorgestellt. Diese Technik ermöglicht die Strukturierung und Integration organischer Dünnschichttransistoren unter Raumluftbedingungen. Es wird gezeigt, dass organische Dünnschichttransistoren grundlegend in ihrer Leistungsfähigkeit durch die Injektion von Ladungsträgern limitiert sind. Demzufolge stellt die Skalierung z.B. der Kanallänge keine adäquate Methode zur Verbesserung solcher Dünnschichttransistoren dar. Ein neuartiges, vertikales Transistor-Konzept, realisiert durch die vorgestellte Photolithographie-Technik, kann zur Überwindung dieser Nachteile dienen. Diese vertikalen Transistoren zeichnen sich durch eine extrem kurze Kanallänge ($\sim 50 nm$) aus. Dadurch kann in der vertikalen Elektrodenanordnung die Leistungsfähigkeit von planaren Transistor-Geometrien über- troffen werden, was die vertikalen Transistoren zu interessanten und vielversprechenden Bauelementen für eine Integration in zukünftigen flexiblen und transparenten organsichen Schaltkreisen macht.

Abstract

This work addresses two substantial problems of organic electronic devices: the controllability and adjustability of performance, and the integration using scalable, high resolution patterning techniques for planar thin-film transistors and novel vertical transistor devices. Both problems are of particular importance for the success of transparent and flexible organic electronics in the future.

To begin with, the static behavior in molecular doped organic pin-diodes is investigated. This allows to deduce important diode parameters such as the depletion capacitance, the number of active dopant states, and the breakdown field. Applying this knowledge, organic pin-diodes are designed for ultra-high-frequency applications and a cut-off frequency of up to $1GHz$ can be achieved using optimized parameters for device geometry, layer thickness, and dopant concentration.

The second part of this work is devoted to organic thin-film transistors, high resolution patterning techniques, as well as novel vertical transistor concepts. In particular, fluorine based photo-lithography, a high resolution patterning technique compatible to organic semiconductors, is introduced yielding the integration of organic thin-film transistors under ambient conditions. However, as it will be shown, horizontal organic thin-film transistors are substantially limited in their performance by charge carrier injection. Hence, down-scaling is inappropriate to enlarge the transconductance of such transistors. To overcome this drawback, a novel vertical thin-film transistor concept with a vertical channel length of $\sim 50nm$ is realized using fluorine based photo-lithography. These vertical devices can surpass the performance of planar transistors and hence are prospective candidates for future integration in complex electronic circuits.

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Contents

Introduction and Motivation

'Stay hungry! Stay foolish!'

S. Jobs, businessman, designer, and inventor.

Curiosity is deeply anchored in the spirit of mankind. It is actually the engine driving innovation and discovery and leading to a continuous evolution of the human society. However, some particular innovations and discoveries as e.g. the invention of the wheel, the movable type printing, the steam engine, the electricity, the theory of evolution, the discovery of penicillin, and development of microelectronics have substantially guided the society and are affecting our daily life essentially. Microelectronics, accompanied with the arise of modern communication techniques including the Internet, presumably represents the most remarkable development within the $20th$ and $21th$ century. It affects the way people work, the way they communicate, and i.e. led to the rise of a multi-billion euro industry - a considerable part of the global economy.

Nowadays, microelectronic devices are mainly based on inorganic materials, i.e. silicon. Owing to continuous improvements of material properties and fabrication techniques, the performance of silicon-based devices is remarkable and close to quantum mechanical limitations. Moreover, a versatile set of different devices such as transistors, diodes, light-emitting diodes, and solar cells have been developed and their performance has been optimized with regard to the targeted application. However, the fabrication of silicon-based devices is expensive and energy-intensive. Moreover, owing to its crystallinity and its optical properties, silicon is not an appropriate material for applications where flexibility of the devices and optical transparency are required.

Organic molecules, possessing a so-called conjugated electronic system, are attracting considerable attention since they are a prospective class of semiconductor materials that can be both, transparent to light and processable on flexible substrates at low temperatures.

After pioneering work done in the early $1970s$, the high potential of organic semiconductors for electronic applications has been pointed out. In particular, organic light-emitting diodes (OLEDs) and organic solar cells (OSCs) are gaining increasing scientific and commercial attention. Such devices are not only superior since they can be manufactured on flexible substrates at low temperatures (see Figure 1), they can also reach power efficiencies similar to inorganic devices and they can even surpass them concerning their
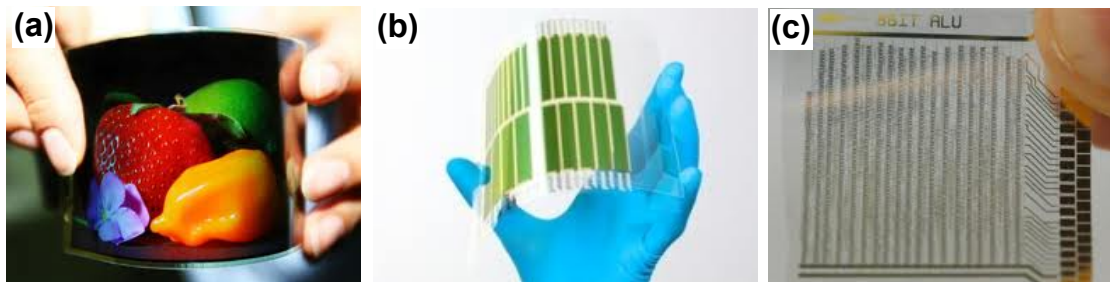
Figure 1: Photographs of **(a)** a flexible OLED display, **(b)** a flexible OSC, and **(c)** the first flexible organic microprocessor. The pictures are taken from references [1–3].

spectral properties (emission spectra of OLEDs are widely tunable, absorption profiles of OSCs are adjustable by the absorber materials). Also first flexible, complex electronic circuits comprising organic semiconductors have been successfully demonstrated. Unfortunately, glancing on the first organic microprocessor presented in 2011 (clock speed $40 Hz$, 8 bit, see Figure 1), the performance of such devices is rather poor in comparison to the benchmark material silicon. Surely, this is partially related to physical limitations of charge transport in organic semiconductors, however, there are also considerable problems concerning the controllability of device performance and appropriate integration techniques. These two aspects are essential for complex electronic circuits since a high density integration, as e.g. needed for fast devices, requires firstly a precise matching of the individual device performances and moreover a suitable high resolution integration technique, which in particular allows for fabrication of complementary electronic circuits.

Nevertheless, organic semiconductors have a huge potential to be used in flexible and transparent electronic devices with a low energy consumption. Their unique properties will give rise to the appearance of novel application concepts beyond non-flexible, opaque, and expensive silicon technology. However, in order to accomplish this, challenges concerning device controllability, performance, and integration have to be solved.

It is the intention of the present work to demonstrate that based on the understanding of the underlying physical phenomena, the performance of organic electronic devices can be adjusted and designed by using technologically accessible process parameters. Moreover, a special focus is placed on integration concepts for organic electronic devices yielding the realization of future high performance organic electronic circuits.

Starting with a general introduction to organic semiconductors, details of electronic device concepts specified to organic semiconductors are provided in Chapter II. Furthermore, the concept of molecular doping, a key technology for the adjustment of performance, and its usage for organic diodes and transistors is discussed.

Within Chapter III, the basics of the experimental techniques are described. Especially, the technique of impedance spectroscopy is explained in detail since it is a main characterization method used here. Moreover, within Chapter III, the setup used for measurements at ultra-high-frequencies (UHF) is introduced. The Chapter is finalized by on overview

on the semiconductor materials used for manufacturing of organic electronic devices.

The main results of this thesis are presented and explained within the Chapters IV,V,VI, and VII. In this sequence, the discussion starts in Chapter IV with fundamentals of diode formation and it is further extended in the Chapters V, VI, and VII to electronic devices such as UHF diodes and transistors.

The focus of Chapter IV is put on the understanding of organic pin-diodes. In particular, the junction is investigated under a static reverse voltage. This allows to study the formation of charge depletion zones and therefore the effectiveness of doping in such systems. Moreover, if large reverse voltages are applied to the diode, a reversible breakdown is observed which can be controlled by the electric field within the junction.

Based on this knowledge of the static situation within a diode, these devices are optimized and designed for ultra-high-frequency applications. As it will be shown, for such applications, charge carrier mobility is the dominant parameter limiting the device performance. Thus, before designing UHF diodes, the influence of molecular doping on charge carrier mobility is studied. A poly-crystalline to amorphous phase transition upon doping leading to a strong loss of charge carrier mobility is revealed in case of the hole transport material pentacene. This is of particular importance, since doping is essential to increase the conductivity of the organic layers. However, it is counterproductive if charge carrier mobility is reduced. Therefore, organic pin-diodes containing pentacene are optimized for highest charge carrier mobility and conductivity. In this way, such pin-diodes are applicable up to $1GHz$ at considerable low driving voltages of $2V$.

Chapters VI and VII are devoted to the organic thin-film transistor which is presumably the most important device in organic microelectronics. Although the performance of organic thin-film transistors has been improved continuously within the recent years, the integration of complex circuits suffers from the fact that no high resolution patterning technique compatible to large area fabrication is available. In Chapter VI, a novel photo-lithographic patterning technique based on highly fluorinated photo-resist and solvent compounds is presented. This technique allows for a direct patterning of organic semiconductors under ambient conditions with a special resolution $< 3\mu m$. Using this lithography method, influences of the recipe on the thin-film transistor performance, as well as general thin-film transistor scaling laws are studied. However, although it is shown that the patterning recipe has no substantial influence on the transistor performance, significant derivations from the expected scaling laws are obtained. This most notably leads to the fact that down-scaling is not an appropriate way to improve the transconductance of organic thin-film transistor. In particular, for the planar thin-film transistors investigated here, the device performance is not governed by the characteristic channel resistance, but rather by injection phenomena for a channel length $< 30\mu m$.

Owing to the strong performance limitations of planar organic thin-film transistors, a novel vertical transistor concept is presented in Chapter VII. Such vertical concepts are superior, since they firstly allow for high integration density, they secondly have an extremely short vertical channel, and thirdly, injection barriers can effectively be compensated by the high vertical electric field. Using the lithography established in Chapter

VI, n- and p-channel vertical transistors are realized and it is shown that they can surpass the performance of planar devices possessing a similar total device area.

As summarized in Chapter VIII, this work provides a deeper understanding of the physical phenomena occurring inside organic pin-diodes. Based on this insight, it is possible to design and optimize organic electronic devices with regard to the targeted electronic application. Moreover, the presented photo-lithographic patterning technique and the novel transistor concept might open the pathway for future applications of organic semiconductor devices in high performance, flexible, and transparent electric circuits.

Chapter II

Organic Semiconductors and Related Devices Concepts

'So einfach wie möglich, aber auch nicht einfacher.'

A. Einstein, physicist.

An introduction to the basic physical properties of organic semiconductors is a useful and indispensable issue since important aspects of charge transport, material interaction, and interface formation are still under scientific consideration. Focusing on small molecule organic semiconductors this chapter provides a brief overview on physical models that describe main aspects of structural and electronic properties of these materials. The transition from a single molecule to a solid state molecular film is considered in order to elucidate mechanisms of charge carrier transport in organic semiconductors. Doping, which is of major importance for every semiconductor is addressed in terms of molecular doping for small molecule organic semiconductors. Selected device concepts for organic semiconductors comprising doped layers are described, taking their specific charge transport properties into account.

2.1 Fundamentals of Organic Semiconductors

No matter where we go and no matter what we look at, our daily life is accompanied by organic materials. From the smallest virus to the tallest giant tree, from basic amino acids to the complex human brain, from the simple plastic foil to highly efficient and flexible displays, all these things are made of organic compounds. This versatility surely originates from the chemical properties of carbon, the basic element in every organic material. It is tetravalent, which facilitates the carbon atom to bind differently to other atoms depending on the hybridization of its atomic orbitals. In this way also different geometries of organic molecules can be realized, reaching e.g. from the 1-dimensional ethine, over the 2-dimensional graphene, to the 3-dimensional diamond. This impressively demonstrates the importance of chemical bonds on physical properties since the three compounds mentioned above cover the whole spectrum from a gaseous to the hardest solid-state material, from a perfect insulator to a quasi-metal. Organic semiconductors are just a "small" group of the almost innumerable set of available organic compounds. Their special semiconducting property is related to the formation of so-called π-orbitals which are spatially extended and lead to a delocalization of electrons. In this section, these so-called conjugated compounds are introduced and their structural and electronic properties are discussed.

2.1.1 Structural and Electronic Properties of Organic Semiconductors

To develop an understanding of charge carrier transport in organic semiconductors, electronics properties of a single molecule have to be discussed with regard to its structural properties. These consideration have to be extended to a bulk organic semiconductor. This distinction between properties of a single molecule and a bulk material is necessary owing to the different nature of molecular bonds and inter-molecular interaction.
Although organic semiconductors are mainly built of carbon, also other elements are involved in organic semiconductors. While hydrogen is mainly employed to avoid dangling bonds, elements such as oxygen, nitrogen, sulfur, and fluorine are used to influence the polarizability, the energy of the molecular orbitals, and the functionality of the molecules in general. Furthermore, metals such as e.g. zinc, copper, lead, and iridium are utilized to create metal-organic complexes which are favorable for optoelectronic applications due to the interaction of the extended electronic system of such atoms with the molecular orbitals. In general, molecular organic semiconductors are composed of identical molecules named monomers. If these monomers are iteratively, covalently bound to each other the material is denoted as polymer. Contrary to that, the semiconductor system is denoted as small molecule organic semiconductor if the monomers are not covalently bound to each other. The description of basic properties of organic semiconductors presented here focuses on such small molecule organic semiconductors. Nevertheless, this can also be extended to polymer organic semiconductors. Intra-molecular binding energies and atomic distances in polymers and in small molecules are rather similar and lie in the range of

$1 - 7eV$ and $\sim 0.1 - 0.3nm$ [4], respectively. Contrary to that, the total extension of a small molecule is typically less than $5nm$, while polymer chain lengths often exceed several hundreds of nanometers.

The understanding of molecular bonds is essential for the explanation of electronic properties of organic semiconductors. For sake of simplicity, the formation of a chemical bond between two atoms bearing only one electron is considered. This model system, the ionized hydrogen molecule, is suitable to understand the formation of molecular orbitals. The situation in organic semiconductors is far more complicated, but nevertheless these basic aspects can be adopted to such more complex systems. In our model system the total wave function $\Psi = \Psi(\vec{r}, \vec{R}_1, \vec{R}_2)$ obeys the one-electron Schrödinger equation

$$\hat{H}\Psi = \hat{H}_{\vec{r}}\Psi + \hat{H}_{\vec{R}_1}\Psi + \hat{H}_{\vec{R}_2}\Psi = E\Psi, \tag{1}$$

where $\vec{R}_1$ and $\vec{R}_2$ are the spatial coordinates of the atomic nuclei and $\vec{r}$ is the spatial coordinate of the electron. As indicated in Eq.1, the Hamiltonian operator $\hat{H}$ contains the kinetic and potential energy of the electron as well as energy of the atomic nuclei. Unfortunately, this already gives rise to the fact that no analytical solution for Ψ can be found. However, since an electron is 1836 times lighter than a proton, it can be assumed that the motion of a nucleus is significantly slower than the motion of an electron (Born-Oppenheimer approximation). This facilitates the separation of the wave function into a vibronic and an electronic part as $\Psi(\vec{r}, \vec{R}_1, \vec{R}_2) = \Psi(\vec{r})\Psi(\vec{R}_1, \vec{R}_2)$ and accordingly the Hamiltonian can be simplified to

$$\hat{H}\Psi = \hat{H}^{elec}\Psi(\vec{r}) + \hat{H}^{vib}\Psi(\vec{R}_1, \vec{R}_2) = E^{elec}\Psi(\vec{r}) + E^{vib}\Psi(\vec{R}_1, \vec{R}_2). \tag{2}$$

The electronic part of this Schrödinger equation can be solved analytically. However, the approach of a linear combination of atomic orbitals (LCAO) is used here since it can be generalized to more complex molecules. In this simple one-electron picture it can be assumed that the total electronic wave function is composed of atomic wave functions as

$$\Psi(\vec{r}) = c_1\Psi_1 + c_2\Psi_2, \tag{3}$$

where c_1 and c_2 are expansion coefficients and Ψ_1 and Ψ_2 are atomic wave functions (e.g. the $1s$ orbital wave functions of the hydrogen atoms). Owing to the normalization of the wave functions and its symmetry, two solutions for c_1 and c_2 are allowed which are $c_1 = \pm c_2$ ($|c_1|^2 = |c_2|^2$). This leads to a symmetric Ψ_+ and an anti-symmetric Ψ_- wave function

$$\Psi_\pm = \frac{1}{\sqrt{2 \pm 2S}}(\Psi_1 \pm \Psi_2) \tag{4}$$

with the corresponding energy eigenvalues of

$$E_\pm = \frac{H_{AA} \pm H_{AS}}{1 \pm S}. \tag{5}$$
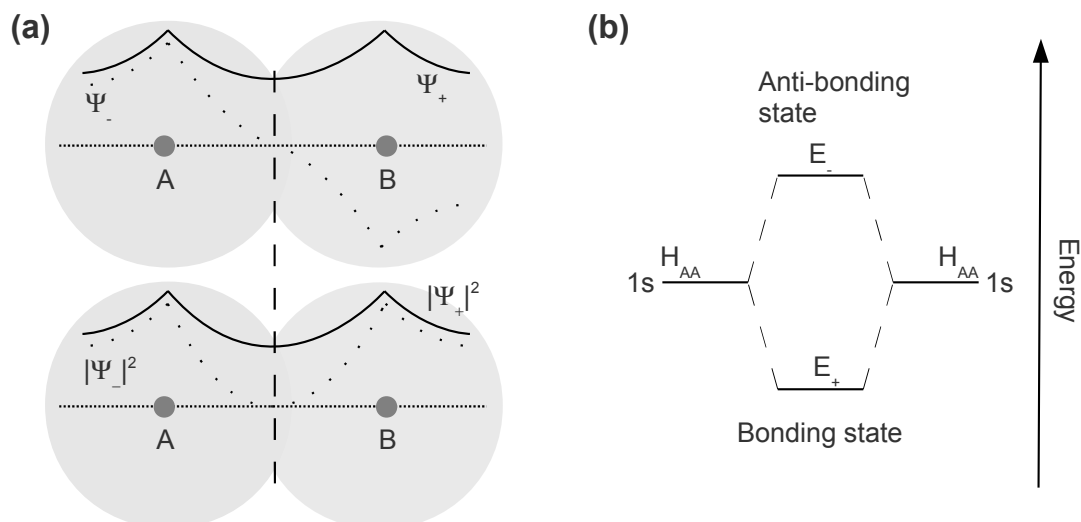
Figure 2: (a) Cross-section along the bonding axis of two nuclei (A and B). The upper graph illustrates the symmetric Ψ_+ and anti-symmetric Ψ_- wave function according to Eq.4. The lower graph shows the mean-square values of both wave functions. The spherical symmetry of the $1s$ atomic wave function is indicated by the gray background. **(b)** Schematic energy-level diagram showing the transition from atomic to molecular orbitals within the LCAO approach.

These wave functions $\Psi_\pm$ represent molecular orbitals. Their energy eigenvalues $H_{AA} = \langle \Psi_{1/2}|\hat{H}|\Psi_{1/2}\rangle$ are given by the Coulomb integral which equals the energy eigenvalue of a single electron in an atomic orbital. $H_{AS} = \langle \Psi_{1/2}|\hat{H}|\Psi_{2/1}\rangle$ is denoted as resonance integral, and $S = \frac{1}{2}(\langle \Psi_-|\Psi_+\rangle + \langle \Psi_+|\Psi_-\rangle)$ is the overlap integral. These wave functions and the corresponding energy diagram are illustrated in Figure 2.

In this picture, the mean-square value of Ψ_- and Ψ_+ exhibits a minimum exactly in the middle of both atoms. While for the anti-symmetric wave function $|\Psi_-|^2$ equals zero at this minimum point, the $|\Psi_+|^2$ of the symmetric wave function fulfills $|\Psi_+|^2 > 0$. Consequently, one can distinguish between a bonding state Ψ_+ and an anti-bonding state Ψ_- with an energy gap in between which is governed by the overlap of the atomic wave functions. Despite the simplicity of this model, it is suitable to reveal general aspects of molecular bonds that can also be generalized to more complex molecules. Methods that are commonly employed to compute such molecules are the density functional theory or the Hartree-Fock approach. Both incorporate many-electron effects and can provide solutions for molecular energy eigenstates which are in fairly good agreement to experimental observations.

Extended molecular π-systems: In the previous paragraph, the basics of molecular bindings have been established. However, charge carriers are localized within this picture and therefore electrical conduction as required for a semiconductor cannot take place. To explain electrical conduction, the model has to be extended to so-called conjugated π-systems. This will be presented here for the model system of an aromatic
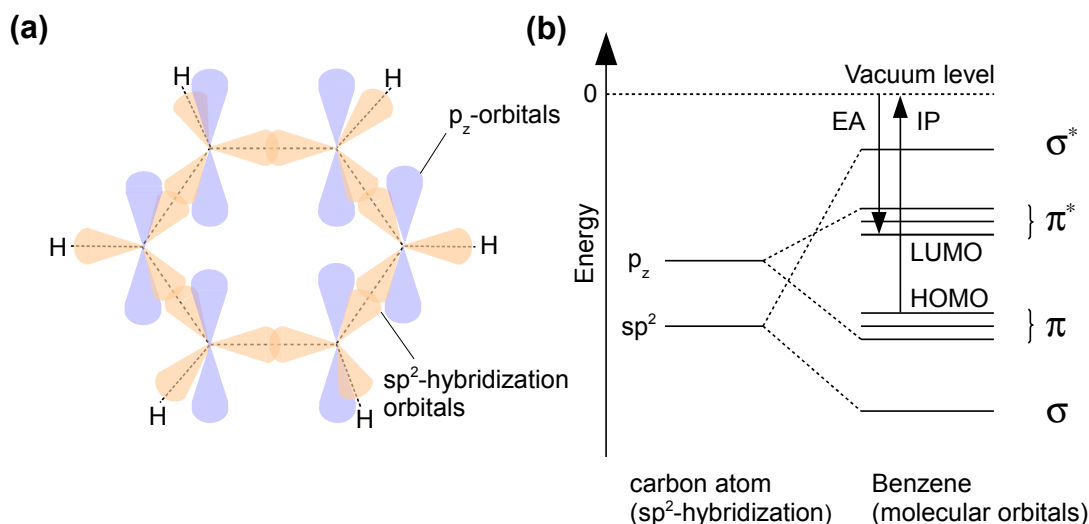
Figure 3: (a) Scheme of a benzene molecule. The sp^2- and p_z-orbitals which form σ- and π-bonds respectively are illustrated. p_z-orbitals are standing perpendicular to the molecule plane, while sp^2-orbitals are oriented in the direction of atomic connection. **(b)** Schematic energy-level diagram showing the transition from atomic to molecular orbitals for the benzene molecule. Due to the 6 carbon atoms in the benzene 6 π-orbitals are formed. The occupied molecular orbitals (π, σ) are separated from the unoccupied molecular orbitals (π^*, σ^*) by an energy gap $|IP| - |EA|$.

benzene ring as shown in Figure 3(a)

In a benzene ring all carbon atoms are covalently bound to two other carbon atoms and one hydrogen atom. The planar geometry of this molecule originates from the sp^2-hybridization of the atomic wave functions of every carbon atom[1]. Molecular orbitals with different symmetries are formed by this hybridization . Wave functions being symmetric with respect to reflection at the perpendicular center plane between two carbon atoms are denoted as σ-orbitals. Wave functions being anti-symmetric with respect to this transformation are denoted as π-orbitals. Owing to the hybridization 30 valence electrons (6 H-atoms + 6 C-atoms) are present in the benzene ring and can be used for molecular bonds. For σ-orbitals and σ-bonds respectively 24 of these electrons are employed to form six identical C-C bonds and six identical C-H bonds. The remaining 6 electrons are available to create three π-bonds which have to be delocalized within the benzene ring. This is denoted as conjugation of π-orbitals. Thus, the conjugation and subsequently the delocalization of charge carriers are the basis for electrical conduction within the benzene ring.

Conjugated molecules are the backbone of every organic semiconductor. The energy eigenvalues of such a conjugated molecule are schematically shown in Figure 3(b). For the ground state the occupied and unoccupied π-states reside within the energy gap between the σ-states. However, there is still an energy gap between the highest occu-

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[1] sp^2-hybridization of carbon: the $2s$ orbital and two $2p$ orbitals of a carbon atom are mixed to create 3 sp^2 hybrid orbitals
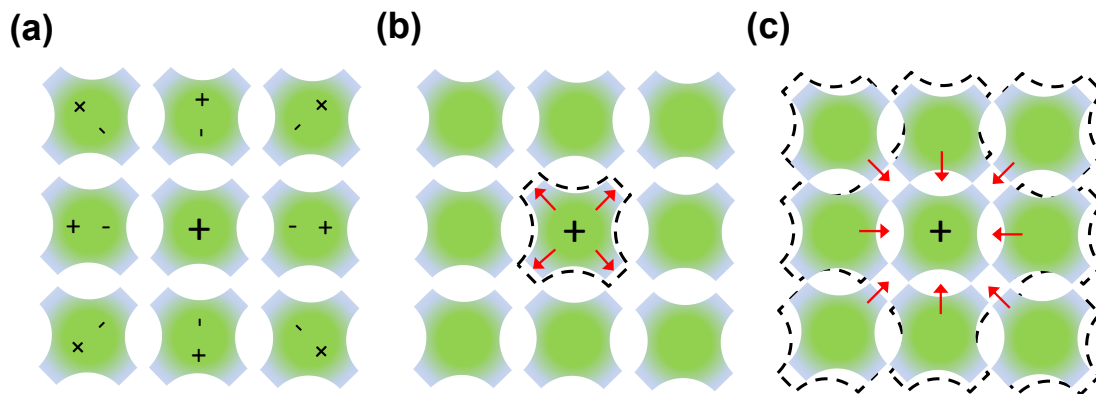
Figure 4: Series of relaxation processes which can occur subsequently if a charge carrier is brought onto a molecule (and stays localized on it): **(a)** electronic polarization, **(b)** vibronic relaxation, and **(c)** lattice relaxation.

pied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO). The importance of conjugation is demonstrated by the fact that the energy gap between HOMO and LUMO is predominantly governed by the spatial dimensions of the delocalized π-electron system. The more extended the π-system, the smaller the energy gap. The energy of HOMO and LUMO can be correlated to experimentally accessible quantities by Koopman's theorem. In particular, it states that the energy of an unoccupied molecular orbital can be approximated by the electron affinity (EA) which is the energy released by an electron which is added to the molecule coming from the vacuum energy level. Furthermore, Koopman's theorem says that the energy of an occupied molecular orbital can be approximated by its ionization potential (IP). However, one should keep the fact in mind that Koopman's theorem neglects effects of reorganization and polarization during ionization which might lead to altered energy levels. Nevertheless, it is common to associate HOMO and LUMO energy values with the ionization potential and the electron affinity.

From molecules to molecular solids: Before discussing charge carrier transport phenomena in organic semiconductors, inter-molecular interactions within a solid-state phase have to be considered owing to their influence on the electronic properties of the semiconductor material. This understanding is essential since the transition from a single molecule to a solid-state material is accompanied with significant changes in electronic, optical, and mechanical properties.

In contrast to materials like silicon, the molecule-molecule interaction in a solid-state film is dominated by van der Waals forces instead of covalent bonds. Hence, a typical molecule-molecule binding energy is in the range of $1 - 100 meV$. Nevertheless, polarization effects caused by molecule-molecule interaction can strongly influence bulk properties of organic semiconductors. Such polarization effects can originate from electronic, vibronic, or phononic couplings (compare Figure 4). The corresponding quasi-particles are entitled as polarons. Owing to these polarization effects, the ionization potential

and the electron affinity may significantly alter from the HOMO and LUMO levels of a single molecule. In effect, the ionization potential is typically lowered, while the electron affinity is typically increased in comparison to single molecule values. Thus, the energy gap between HOMO and LUMO is lowered by polaronic effects. The total difference for both energy values lies within the range of several hundreds of meV.

However, the contribution of the different polarization effects is different. The electronic polarization provides the main contribution in this context (compare Figure 4(a)). If a charge carrier is added to a neutral molecule it polarizes adjacent molecules which leads to a dipole formation - or equivalent to formation of an electronic polaron. The situation is often described with an electron shielded by its polarization cloud. Such electronic couplings take place on a short time scale (relaxations time scale $\sim 10^{-15}s$) and their interaction energy is fairly large (up to $1eV$).

The second polarization mechanism is caused by the influence of intra-molecular vibrations on the electronic wave function, and the corresponding quasi-particle is called vibronic polaron (compare Figure 4(b)). This is actually the coupling which has been so far disregarded by relying on the Born-Oppenheimer approximation. However, by inclusion of the vibronic coupling within the molecule model, the additional interaction leads to a reallocation of molecular orbitals and accordingly charge carriers. The relaxation time scale for vibronic processes is larger than for electronic processes. It is in the range of $10^{-14}s$ and subsequently typical interaction energies are lower ($0.1 - 0.3eV$).

The third prominent polarization process is due to interaction of quasi-localized charges with inter-molecular lattice deformations (phonons, compare Figure 4(c)). The corresponding quasi-particle is denoted as lattice polaron. Phononic coupling, possessing interaction energies in the range of $10 - 30meV$, is rather weak in comparison to the electronic and vibronic coupling. This is exclusively related to the typically slow lattice deformations times ($\sim 10^{-11}s$) giving rise to merely a small interaction probability with quasi-localized charge carriers. However, as it will be seen in the discussion of charge carrier transport, if charge carriers reside on a single molecule due to a small overlap of molecular wave functions, lattice polarons and vibronic polarons assist charge carriers to hop from one site to the other.

Excitons in organic semiconductors: Besides polarons, excitons represent another prominent kind of quasi-particles in semiconductors. They comprise of a negative and a positive charge carrier (electron-hole pair) which interact via their electrostatic field. Excitons can be generated in several ways: by capturing of free electrons and holes as in an OLED, by direct HOMO to LUMO transition of an electron through light excitation, or by electrical doping. In either case the important parameter characterizing the exciton is its Coulomb binding energy and its interaction radius, respectively. In that context, three types of excitons have to be distinguished: the Wannier-Mott exciton, the Charge-Transfer exciton (CT-exciton), and the Poole-Frenkel exciton (see Figure 5). The polarizability of the surrounding material is the feature that determines which of those excitons is predominantly present.

(a)   **(b)**   **(c)**
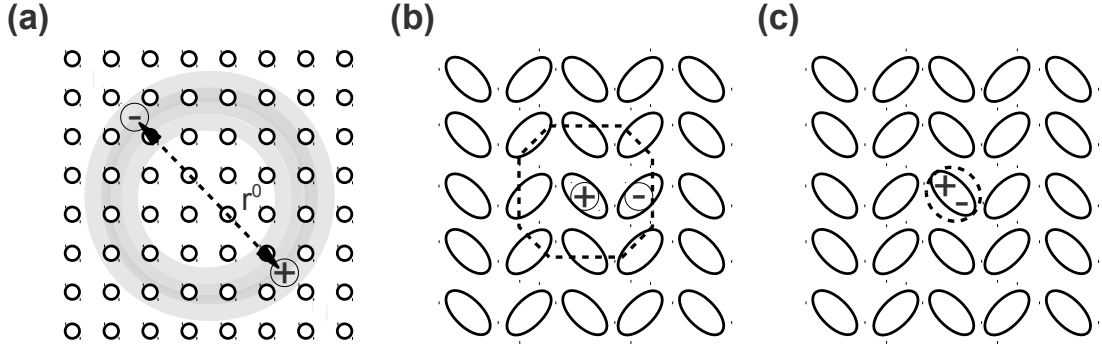
Figure 5: Visualization of the three prominent exciton species: **(a)** Wannier-Mott exciton as they typically appear in crystalline inorganic semiconductors, **(b)** Charge-Transfer exciton, and **(c)** Poole-Frenkel exciton. Latter ones are illustrated in a typical crystalline structure for organic semiconductors. Their interaction radii r^0 of the electron (-) - hole (+) pair are highlighted by dashed lines. After [4].

In case of a Wannier-Mott exciton the polarizability of the surrounding material is large corresponding to a large dielectric constant. This causes a screening of the electric field between the electron-hole pair, resulting in a small exciton binding energy and a large interaction radius. A simple and in many cases appropriate model to describe such Wannier-Mott excitons is given by the hydrogen atom model. In this picture, the ground state energy E^0 and interaction radius r^0 of the correlated electron-hole pair can be expressed as

$$E^0 = -\frac{1}{2}\frac{\pi q^4 m_r}{(\epsilon_0 \epsilon \hbar)^2} \quad \text{and} \tag{6}$$

$$r^0 = \frac{\epsilon_0 \epsilon \hbar^2}{\pi m_r q^2}, \tag{7}$$

where q is the elementary charge, $h = 2\pi\hbar$ is Planck's constant, ϵ_0 is the vacuum permittivity, ϵ is the material permittivity, and m_r is the reduced mass of the electron-hole pair. For inorganic semiconductors that have a large material permittivity, the exciton interaction radius can be up to several nanometers, while the binding energy is typically in the range of $10 - 100 meV$. Accordingly, the exciton is delocalized over several unit cells of the semiconductor.

This picture cannot generally be adopted to organic semiconductors since typically material permittivities ϵ are merely in the range of 3...6. Hence, the exciton interaction radius is small meaning that the exciton is either located on one molecule (Poole-Frenkel exciton) or distributed over two molecules (CT-exciton). In this case the exciton has to be treated as a strong correlated charge carrier pair where the local ionization potential IP_h (at the position of the hole), the local electron affinity EA_e (at the position of the electron), the electron-hole Coulomb interaction energy $C(r)$, and the polarization energy of the lattice caused by the exciton $P(r)$ have to be taken into account in order to

determine the exciton binding energy as [4, 5]

$$E^0 = IP_h - EA_e - P(r) - C(r). \qquad (8)$$

The strong polaronic coupling of such excitons leads to binding energies that can vary from hundred meV up to more than $1eV$. A typical interaction radius is given by the molecular size, which is in the range of several angstrom. The formation and dissociation of Poole-Frenkel and CT-excitons will be reconsidered for description of electro-chemical doping of organic semiconductors (see Subsection 2.1.3).

2.1.2 Charge Carrier Transport in Organic Semiconductors

Understanding charge carrier transport in organic semiconductors is a major challenge. Even for model systems such as defect-free organic semiconductor crystals, little is known and a comprehensive and conclusive theory is required that covers the whole spectrum from microscopic processes to applicable electronic devices, from an ordered crystalline material to a completely disordered molecular system. This partially unsatisfying situation is likely caused by two main aspects. On the one hand it exhibits a major challenge to formulate a theory accounting for the situation of dynamic and static disorder and on the other hand, there is still a lack in experimental realization of adequate model systems, which is a consequence of insufficient purification of organic materials. Moreover, most experimental techniques allow a characterization of charge carrier transport on either a macroscopic or a microscopic scale, but not both. In consequence, it has often been claimed from experimental studies that a charge carrier mobility proportional to temperature provides evidence for a hopping-like transport, while an anti-proportional dependence is related to a band-like transport. As discussed within this section, a delocalization of charge carriers is assumed for band-like transport. However, in most cases this is in contradiction to experimental findings.
The intention of this subsection is to present the concepts of basic models used for description of charge carrier transport in organic semiconductors. It is beyond the scope of the present work to provide a comprehensive description of all these theories in mathematical detail. Starting point will be a description of transport scenarios in ordered crystalline materials with dynamic disorder (electron-phonon coupling). The considerations on charge carrier transport are then extended to amorphous molecular systems which reflects static disorder. It will be shown that polaronic coupling effects are of particular importance to quantify important parameters of charge carrier transport such as charge carrier mobility. Furthermore, polaronic theories for charge carrier transport can explain the considerable influence of the degree of static and dynamic disorder on charge carrier mobility which typically varies in the range of $10^{-5} - 10 cm^2/(Vs)$.

2.1.2.1 Band Transport and Classical Polaron Theories

Initially, a model system of an organic semiconductor which is single-crystalline and free of defects will be considered. In case of a covalently bound inorganic semiconductor these conditions are already sufficient for the appearance of an electronic band structure. Moreover, since the overlap of atomic wave functions in such systems is rather large the energy distribution of bands is broad and charge carriers can be treated as quasi-free particles with an effective mass governed by the band dispersion.

In the naive picture of an ordered one-dimensional molecular chain where each molecular site is described by the creation and annihilation operator ($a_j{}^\dagger$ and a_j) of the frontier molecular orbital $|j\rangle$, one can formulate an electronic Hamiltonian $\hat{H}_{el}$ in tight-binding approximation as

$$\hat{H}_{el} = \sum_j \epsilon_j a_j{}^\dagger a_j + \sum_{j,k} \gamma_{jk} a_j{}^\dagger a_k, \tag{9}$$

where ϵ_j denotes the energy eigenvalues corresponding to state $|j\rangle$ and γ_{jk} is the transfer integral accounting for electronic coupling of neighboring molecules. A direct consequence of this Hamiltonian in tight-binding approximation is the appearance of electronic bands. The eigenfunctions of this system are plane waves that reflect the delocalization of charge carriers and the complete coherence of charge carrier motion. In this picture charges are moving with respect to the band dispersion with an effective mass m^*. By means of the Drude model charge carrier mobility μ is given by

$$\mu = \frac{q\tau}{m^*}, \tag{10}$$

where τ is the average time between two collision events either with ionized impurity states or phonons.

In the tight-binding approach, the width of electronic bands is proportional to the transfer integral γ_{jk}. Hence, dispersion of bands is expected to be flat in organic semiconductors due to the weak inter-molecular interaction. This statement is equivalent to a large effective mass and therefore to a low charge carrier mobility. Thus, charge carrier mobility is proportional to the electronic band width. Relying on a purely band-like transport disregarding electron-phonon coupling, a temperature (T) dependence of charge carrier mobility as $\mu \sim T^{-3/2}$ [6] and a complete delocalization of charge carriers can be expected. However, this is not in agreement to experimental findings, where charge carrier mobility for highly purified organic crystals is characterized by a power law $\mu \sim T^{-n}$, $0.5 < n < 4$ [4, 7, 8]. Moreover, Marumoto et al. [9] have shown for poly-crystalline pentacene that holes are localized within a radius of 10 molecules at room temperature. This provides strong evidence that assuming transport via electronic bands disregarding polaronic coupling is not appropriate to describe charge transport sufficiently over a wide temperature range in crystalline organic semiconductors.

Theories of more microscopic relevance are discussed in literature as polaron models. In that context, the tight-binding Hamiltonian has to be reconsidered in order to take

effects of vibronic polarons and lattice polarons into account [2]. In linear electron-phonon coupling approximation, the Hamiltonian can be expressed according to [5, 7, 8, 10] as

$$\hat{H} = \hat{H}_{el} + \hat{H}_{ph} + \hat{H}_{e-ph}^{l} + \hat{H}_{e-ph}^{nl} \tag{11}$$

$$\hat{H}_{ph} = \sum_{\mathbf{q}j} \hbar\omega_{\mathbf{q}j}\left(b_{\mathbf{q}j}{}^{\dagger}b_{\mathbf{q}j} + \frac{1}{2}\right) \tag{12}$$

$$\hat{H}_{e-ph}^{l} = N^{-1/2}\sum_{\mathbf{q}j}\sum_{m}\hbar\omega_{\mathbf{q}j}\Big(g_m(\mathbf{q},j)b_{\mathbf{q}j}{}^{\dagger} + g_m^*(\mathbf{q},j)b_{\mathbf{q}j}\Big)a_m{}^{\dagger}a_m \tag{13}$$

$$\hat{H}_{e-ph}^{nl} = N^{-1/2}\sum_{n\neq m}\sum_{\mathbf{q}j}\sum_{m}\hbar\omega_{\mathbf{q}j}\Big(g_{mn}(\mathbf{q},j)b_{\mathbf{q}j}{}^{\dagger} + g_{mn}^*(\mathbf{q},j)b_{\mathbf{q}j}\Big)a_n{}^{\dagger}a_m, \tag{14}$$

where $b_{\mathbf{q}j}{}^{\dagger}$ and $b_{\mathbf{q}j}$ in the phononic Hamiltonian $\hat{H}_{ph}$ are the creation and annihilation operator of a phonon (branch j) with the energy $\hbar\omega_{\mathbf{q}j}$ and the wave vector $\mathbf{q}$. The coupling constants for local electron-phonon (upper index l) and non-local electron-phonon (upper index nl) coupling are denoted as $g_m(\mathbf{q},j)$ and $g_{mn}(\mathbf{q},j)$, respectively. N denotes the total number of unit cells.

This system, restricted to local electron-phonon coupling, has been discussed by Holstein [11, 12] in 1959 and it has been extended later to non-local couplings by e.g. [5, 7, 8, 10, 13, 14]. The electron-phonon interaction leads to a time dependence of the transfer integrals and therefore induces a dynamic disorder. The temperature dependence of transfer integrals can be used in this model to predict the charge carrier mobility vs. temperature dependence.

In the low temperature limit ($T \to 0$) delocalized polarons form band-like states due to the assumed translation symmetry in the molecular chain. According to the theory of purely electronic bands, the width of the polaronic bands is decreased with increasing temperature which is caused by the decrease of transfer integrals. Thus, owing to the decreased band width, the effective mass is increased which in consequence gives rise to a lowering of charge carrier mobility with increasing temperature. In comparison to purely electronic bands, polaronic bands exhibit a more narrow width. As shown in Figure 6(a), this effect takes place already at $T = 0K$ and it is even more pronounced if non-local electron-phonon coupling is taken into account. The temperature dependence of charge carrier mobility in the low temperature limit can be expressed according to [13] by

$$\mu \sim \frac{const.}{k_B T}csch(\frac{E_{ph}}{k_B T})^{1/2}exp\left\{-2csch\Big(\frac{E_{ph}}{k_B T}\Big)\right\}, \tag{15}$$

where E_{ph} is the energy of the optical phonon that contributes to the polaron formation and k_B is Boltzmann's constant. For very low temperatures $T \approx 0$ this would give a $\mu \sim T^{-3/2}$ dependence. With increasing temperature the mobility drops with an exponent $n > 3/2$ in agreement to experimental findings [4, 8]. In contrast to the situation of coherent wave functions as assumed in the low temperature limit, for the

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[2]The vibronic polarons are also denoted as local electron-phonon coupling, while lattice polarons are also named non-local electron-phonon coupling.
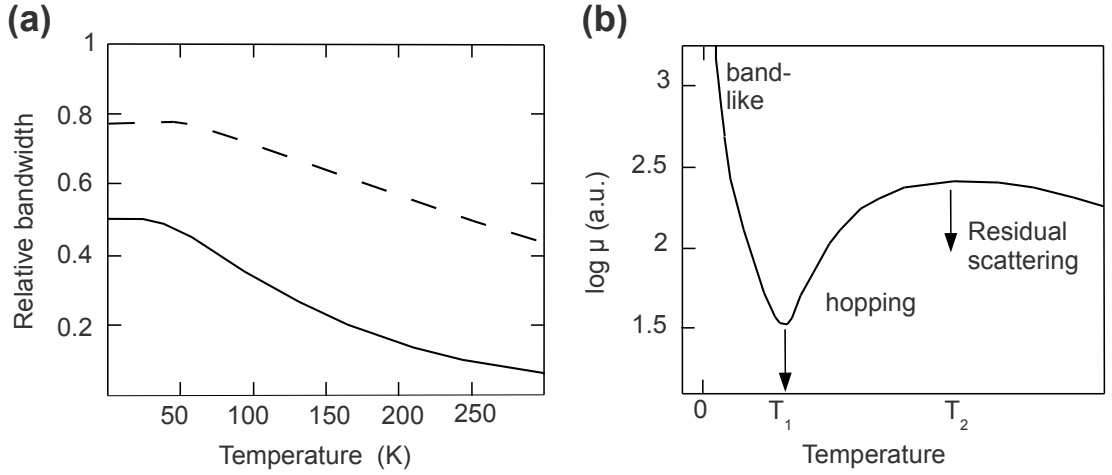
Figure 6: (a) Temperature dependence of the polaronic bandwidth including local (dashed line) and non-local (solid line) electron-phonon interaction normalized to the electronic bandwidth without electron-phonon coupling. Redrawn from [10]. **(b)** Charge carrier mobility vs. temperature for strong electron-phonon coupling $||g||^2 >> 1$ as predicted by Holstein's polaron model (see Eq. 15-16). T_1 and T_2 mark the transition from coherent band transport to incoherent hopping and to scattering at thermal phonons for temperatures above T_2. For weak electron-phonon coupling ($||g||^2 << 1$) charge carrier mobility strictly follows Eq. 15. Redrawn from [13].

high temperature limit ($k_BT >>$ phonon energy) a complete loss of coherence is expected since the polaronic bandwidth vanishes within this theory for high temperatures. Thus, at high temperatures charge carriers are not able to interact with each other. Holstein [11, 12] also described this scenario considering a hopping-like transport between localized states. In this framework charge carrier mobility μ_{hop} is expressed as

$$\mu_{hop} \sim \frac{const.}{k_BT} \frac{1}{(E_{ph}k_BT)^{1/2}} exp\Big(-\frac{E_{ph}}{2k_BT}\Big). \tag{16}$$

Charge carrier mobility vs. temperature is exemplarily shown in Figure 6(b). The Arrhenius-like temperature activation of charge carrier mobility can be seen in the medium temperature region ($T_1 < T_2 < T_2$). For $T > T_2$ mobility starts to decrease again owing to the dissociations of polarons and the scattering of electrons at thermal phonons. Polaronic theories are not applicable for $T > T_2$.

2.1.2.2 Transport under Dynamic and Static Disorder Conditions - Hopping Theories

The high temperature limit is somehow similar to the situation of static disorder that has been neglected so far. This similarity is not intuitive, but becomes more obvious if

one accounts for the fact that fluctuations of molecular HOMO/LUMO levels (diagonal disorder, e.g. a distribution of ϵ_j in Eq.9) as well as fluctuations of the inter-molecular interaction strength (off-diagonal disorder, e.g. a distribution of γ_{jk} in Eq.9) lead to the disappearance of band states and the material is rather described by molecular wave functions similar to the high temperature limit.

The effect of diagonal disorder has been discussed by Anderson [15]. He deduced that charge carriers are localized in a system of non-uniform quantum wells when the width of the quantum well depth distribution is equal to the calculated band width in tight-binding approximation. If no band states are present, charge carrier transport can be adequately expressed in a probability evolution equation (assuming linear rates)

$$\frac{\partial}{\partial t}f_i = -\sum_{i \neq j} W_{ij}f_i(1 - f_j) + \sum_{i \neq j} W_{ji}f_j(1 - f_i) - \lambda_i f_i, \qquad (17)$$

where $f_i(f_j)$ denote the occupation probability of site $i(j)$, $W_{ij}(W_{ji})$ denote the transition rates from site i to j (j to i), and λ_i reflects the decay rate if site i is excited.

Two main attempts to describe the transition rates W_{ij} have been published and they are know as Miller-Abraham's [5, 16] and Mott's approach [17]. The latter has been used to derive Eq.16[3]. It assumes a polaron assisted site-to-site hopping. However, owing to typically polaron binding energies in organic semiconductors, polarons might be dissociated at room temperature. Therefore, a description of transport supported by thermal phonons is favorable at room temperature conditions. The Miller-Abraham approach represents such a theory since it ascribes the transport to a phonon-assisted tunneling. The transition rates are given by

$$W_{ij} = \nu_0 exp(-2\alpha|R_{ij}|) \begin{cases} exp(-\frac{(\epsilon_j - \epsilon_i)}{k_B T}) & \forall \epsilon_j > \epsilon_i \\ 1 & \text{else}, \end{cases} \qquad (18)$$

where ν_0 is the phonon vibration frequency, ϵ_i and ϵ_j are the energies of sites i and j, α is the inverse localization radius of molecular wave functions (assuming an exponential decay with distance), and $|R_{ij}|$ is the spatial distance between site i and j.

The next step for description of hopping transport scenarios is to find the energy eigenvalues of the different sites.

Mott's variable range hopping and Ambegaokar's percolation approach: A hop of a charge carrier takes place according to Eq.18 if a charge carrier is able to find an unoccupied site not too distant in energy and space to have a distinct tunneling rate. Thus, a certain optimum hopping distance R_{opt} with a maximum of hopping rate requires a certain distribution of states in energy $\Delta\epsilon_{opt}$ and vice versa. For sake of simplicity a uniform density of states (DOS) given by $\rho\Delta\epsilon$ with ρ as the charge carrier density is considered. Furthermore, it is assumed that charge transport is restricted to charge car-

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[3]An equivalent expression to Eq.16 can be derived within the framework of Marcus theory[14].

riers in a certain vicinity $\Delta\epsilon$ close to the quasi-Fermi level edge E_F. To ensure that each charge carrier finds a target site within a radius R, one has to postulate

$$\frac{4}{3}\pi R^3 \rho \Delta\epsilon \approx 1. \tag{19}$$

Relying on this, Eq.18 can be modified for hops up in energy ($\Delta\epsilon = \epsilon_j - \epsilon_i$) as

$$W_{ij} = \nu_0 exp\Big(-2\alpha R - \frac{1}{\frac{4}{3}\pi R^3 \rho k_B T}\Big), \tag{20}$$

where one can find a hopping rate maximum ($\frac{dW_{ij}(R)}{dR} = 0$) at

$$R_{opt} = (\frac{1}{8\alpha k_B \pi \rho}\frac{1}{T})^{1/4} \quad or \quad \Delta\epsilon_{opt} = \frac{3}{4}\frac{(8\alpha k_B T)^{3/4}}{(\pi\rho)^{1/4}} \tag{21}$$

which leads to a hopping rate vs. temperature dependence of

$$W_{ij} \sim exp\Big[-\Big(\frac{T_0^{hop}}{T}\Big)^{1/4}\Big]. \tag{22}$$

This has been adopted by Ambegaokar et al. [18] as a starting point to associate each hopping step to a microscopic resistance. The total resistance of a film is then given by a percolation path problem where a charge carrier tends to take the path of lowest resistivity which lies within its hopping radius (see Figure 7(c)). This concept is often referred as "lazy particle principle".

Within this framework, Ambegaokar et al. assumed that the microscopic hopping current I_{ij} can be written as $I_{ij} = q[-W_{ij}f_i(1 - f_j) + W_{ji}f_j(1 - f_i)]$. The related microscopic conductivity σ_{ij} is given by Ohm's law as $I_{ij} \approx \sigma_{ij}(E_{Fj} - E_{Fi})$ where the quasi-Fermi levels E_{Fi} and E_{Fj} between the site i and j are modified by a small external voltage. Thus, according to [18] σ_{ij} can be expressed as

$$\sigma_{ij} \approx \frac{q\nu_0}{k_B T}exp(2 - \alpha|R_{ij}|)exp\Big(-\frac{|\epsilon_i - E_F| + |\epsilon_j - E_F| + |\epsilon_i - \epsilon_j|}{2k_B T}\Big). \tag{23}$$

The strategy to disclose the film conductivity is to determine a critical percolation conductance which is favorable for a hop of the "lazy particle". This has been done by Ambegaokar [18] and Mott [19] assuming an uniform DOS as mentioned above. However, it turns out that this assumption is not fulfilled for disordered organic semiconductors. Instead, non-uniform DOS functions are more adequate for disordered organic semiconductors (see Figure 7(a)). This reflects the fact that the site density close to the quasi-Fermi edge is not independent of the charge carrier density. Thus, different sites contribute to transport depending on charge carrier density.

Non-uniform DOS models: Vissenberg et al. [20] described the DOS of disordered
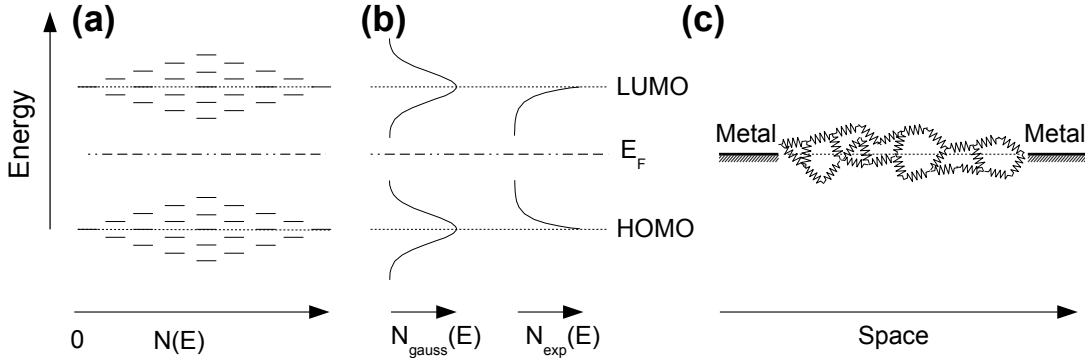
Figure 7: (a) Typical energy distribution of localized charge transport states in a disordered organic semiconductor. **(b)** Gaussian (N_{gauss}) and exponential (N_{exp}) DOS functions are suited models to describe the situation depicted in **(a)**. **(c)** Visualization of percolation paths for 1-dimensional charge carrier transport in a non-uniform DOS. The individual resistors are not equal.

organic semiconductors by an exponential function (see Figure 7(b))

$$N_{exp}(E) = \frac{N_t}{k_B T_0} exp\Big(\frac{E}{k_B T_0}\Big). \tag{24}$$

where N_t is the total density of sites and T_0 is a characteristic temperature that reflects the tailing of states. Assuming $|E_F| >> k_B T_0$, the low tail states in the DOS are occupied for $T < T_0$. For a hopping process of these charge carriers, many unoccupied states are available at higher energies while much less states with similar energy are available. Within the framework of percolation theory, Vissenberg et al. where able to express the temperature dependence of conductivity as

$$\sigma \sim exp\Big(-\frac{E_A}{k_B T}\Big). \tag{25}$$

Even if it does not reflect the microscopic situation, this Arrhenius-like equation can be interpreted as a thermal activated hopping from a discrete occupied level to a specific conductance state. Moreover, this behavior is in good agreement to most experimental findings. In particular, all temperature dependent measurements of conductivity done in this work display such an Arrhenius-like behavior.

Another approach to find a theoretical description of charge carrier mobility and conductivity based on Eq.17 has been presented by Bässler [21] and later been extended by Pasveer et al. [22]. Instead of using percolation path theories, they solved the hopping master equation (Eq.17) directly on a small lattice by Monte Carlo simulations. In particular, they assumed a Gaussian DOS

$$N_{gauss}(E) = \frac{N_t}{(2\pi\hat{\sigma})^2} exp\Big(-\frac{E^2}{2\hat{\sigma}^2}\Big). \tag{26}$$

where $\hat{\sigma}$ is the standard deviation of the DOS distribution. Similar to T_0 in the exponential DOS, $\hat{\sigma}$ accounts for the degree of static disorder. The intention of Gaussian as well as the exponential DOS models is to take tail states into account. For $|E_F| >> k_B T_0$, only these tail states are occupied and therefore the difference between a Gaussian and an exponential DOS is rather small. However, if the quasi-Fermi level is shifted by doping or by elevated temperatures a different situation is observed.

Relying on $|E_F| >> k_B T_0$ charge carrier transport between occupied and unoccupied states is described by the Miller-Abrahams hopping rate equation (Eq.18) where in the tunneling contribution (last term in Eq.18) the energy difference is lowered by the applied electric field $\mathcal{F}$.

From their simulations they are able to deduce a charge carrier density p (unipolar transport, p density of holes), a temperature, and an electric field dependence of charge carrier mobility by [22]

$$\mu = \mu(T,p)f(T,\mathcal{E}) \quad \text{with} \tag{27}$$

$$f(T,\mathcal{E}) = exp\left\{0.44(\hat{\sigma}^{3/2} - 2.2)\left\{\sqrt{1 + 0.8\frac{\mathcal{E}qa}{\sigma k_B T}} - 1\right\}\right\} \quad \text{and} \tag{28}$$

$$\mu(T,p) = \frac{\nu_0 qa^2}{\sigma k_B T}c_3 exp(-c_4\hat{\sigma}^2)exp(\frac{1}{2}(\hat{\sigma}^2 - \hat{\sigma})(2pa^3)^\delta) \quad \text{with} \tag{29}$$

$$\delta = 2\frac{ln(\hat{\sigma}^2 - \hat{\sigma}) - ln(ln(4))}{\hat{\sigma}^2}, \tag{30}$$

where c_3 and c_4 are constants from the fitting procedure and a is the lattice constant (see [22]). In this way charge carrier mobility is directly linked to a parameter that accounts for static disorder. A typical width for a Gaussian DOS for organic semiconductors is in the range $0.05 - 0.2eV$. The so-called Poole-Frenkel-like mobility vs. electric field dependence $\mu \sim exp(\sqrt{\mathcal{E}})$ has been confirmed by experiments.

Impurity dominated transport: Charge carrier transport in organic semiconductors is always associated with charge carrier traps. They can either be shallow or deep with respect to the transport states. Tail states in an exponential or Gaussian DOS as they arise from static disorder can be considered as shallow trap states. Furthermore, trap states can appear owing to chemical impurities or grain boundaries in poly-crystalline films.

Several approaches to account for trap states have been discussed in literature. In general, the kinetics of a single trap level that can be depopulated by phonons can be described according to [6] by

$$\nu_{trap} = \nu_{ATE}exp\left(-\frac{E_{act}}{k_B T}\right). \tag{31}$$

where ν_{trap} is the thermal emission rate of the trap, ν_{ATE} is the attempt-to-escape frequency due to phonon scattering. E_{act} is an activation energy that describes the thermal activated transition from the trap state to a transport state. Shallow traps states are mostly described by extended DOS functions. Also the influence of trap

(a)   **(b)**

Conductance states

Traps states

Valence states

V
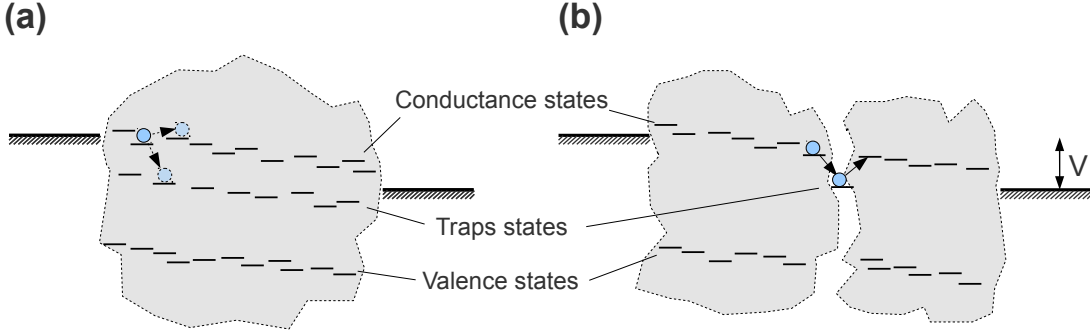
Figure 8: Scenarios of charge carrier transport in a poly-crystalline organic semi-
conductor that contains **(a)** spatial distributed deep trap states and **(b)**
localized trap states at grain boundaries.

states on device characteristics has been discussed [23–25]. However, rather often it
is important to consider one dominant deep trap level since such levels can give rise
to an enormous lowering of charge carrier mobility and device performance in general.
The influence of one dominant trap level has been reported by Horowitz et al. [26].
They discussed the influence of charge carrier mobility in organic thin-film transistors
within the framework of the so-called multiple trapping and release model (MTR) as
well as by a simple percolation theory. The MTR model accounts for one dominant
trap homogeneously distributed in space with a density of n_{trap}. In this picture, the
transport via transport states and via trap states[4] occurs in parallel (see Figure 8(a))
with an associated mobility of μ_0 and μ_{trap}. Therefore, the conductivities of the different
paths (σ_{free} and σ_{trap}) can be summed up leading to

$$\sigma = \sigma_{trap} + \sigma_{free} = q\mu_0 n_{free} + q\mu_{trap} n_{trap}$$
$$\overset{\mu_0 >> \mu_{trap}, \ n_{free} >> n_{trap}}{\Rightarrow} \quad \mu = \mu_0 \frac{n_{free}}{n_{trap} + n_{free}}. \tag{32}$$

for the trap influenced charge carrier mobility μ. In Eq.32 n_{free} denotes the density of
free charge carriers contributing to transport via transport states.
However, if the trap states are not homogeneously distributed in space, the transport via
trap and transport states is in series instead of in parallel (see Figure 8(b)). Thus, the
specific resistances of the transport via trap and transport states has to be summed up
leading to

$$\frac{1}{\sigma} = \frac{1}{\sigma_{trap}} + \frac{1}{\sigma_{free}} = \frac{1}{q\mu n} = \frac{1}{q\mu_0 n} + \frac{1}{q\mu_{trap} n}$$
$$\Rightarrow \frac{1}{\mu} = \frac{1}{\mu_0} + \frac{1}{\mu_{trap}}. \tag{33}$$

where n is the total number of charge carriers that contribute to the transport. This
relation is known as Matthiesen's rule which is often used to describe charge carrier
transport via grain boundaries in poly-crystalline materials as illustrated in Figure 8(b).

[4]transport by capture and release of charge carriers

2.1.3 Molecular Doping of Organic Semiconductors

Electrical doping of organic semiconductors has become a key technology for highly ef-
ficient organic light emitting diodes [27, 28], solar cells [29, 30] as well as for novel and
versatile organic electronic devices such as Zener diodes[31], ultra-high-frequency diodes
[32], transistors [33], triodes [34], and memory cells [35].

Similar to doping in inorganic semiconductors, the aim of adding dopants to a matrix
material is to increase electrical conductivity of a semiconductor film. Besides adjusting
conductivity, the control of the quasi-Fermi level allows to investigate effects of a modified
occupancy in a non-uniform DOS as well as to study the formation of charge depletion
zones which are important for operation of devices like diodes and transistors.

Within this subsection, the concept of molecular doping in small molecule organic semi-
conductor materials are addressed and important differences in comparison to doping
of inorganic semiconductors are pointed out. Technical details of preparation of doped
organic semiconductor films and material specifics are summarized in Subsection 3.4 and
3.5.

Electrical doping in organic semiconductors was realized at first by the pioneering work of
Yamamoto et al. [36] by using strongly oxidizing gases such as iodine for p-type doping.
Later, Haddon et al. [37] suggested alkali metals such as lithium, cesium, and strontium
for effective n-type doping. However, even if both concepts can efficiently increase electri-
cal conductivity in organic semiconductor films, they show several drawbacks such as an
insufficient control of doping rate, and low chemical and physical stability (e.g. diffusion
of dopants) within the matrix system. Nowadays, doped organic semiconductor films are
mostly prepared by co-deposition of a matrix material and a molecular dopant [38–44].

The basic mechanism of charge carrier transfer leading to electrical doping is illustrated
in Figure 9(a) and (b). Although it suggests a close analogy to doping in inorganic semi-
conductor materials, the fundamental mechanisms are rather different. In particular,
if e.g. a p-dopant (acceptor A) is added to a matrix system M, the dopant does not
interact with the matrix by a covalent bond, but rather by formation of a charge-transfer
complex (CT-complex). This formation can by considered as a chemical reaction that
can be written as [39]

$$M + \tilde{M}A \rightleftharpoons M + [\tilde{M}^+ A^-] \rightleftharpoons M^+ \tilde{M}A^- \qquad (34)$$
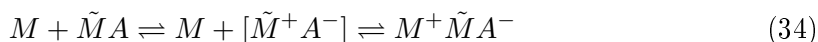
where $\tilde{M}$ represents a matrix molecule close to the acceptor molecule. In a first step of
the reaction, charge transfer takes place between the acceptor A and the molecule $\tilde{M}$.
A CT-complex ($[\tilde{M}^+ A^-]$) has been created. However, charge transfer only occurs if the
HOMO of $\tilde{M}$ and the LUMO of A allow for this transition. The energetic difference E_B
for a hole between the bound state $[\tilde{M}^+ A^-]$ and the final unbound state $M^+ \tilde{M}A^-$ is
given by [39]

$$E_B = |IP_{\tilde{M}}| - |EA_A|, \qquad (35)$$
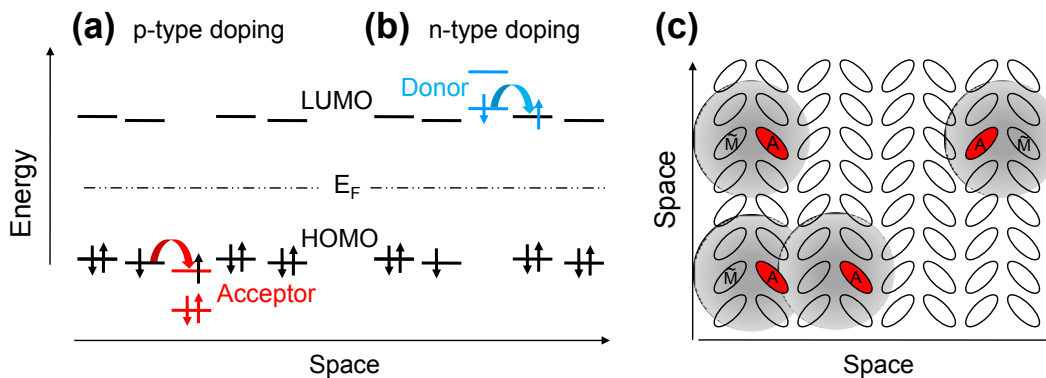
Figure 9: Illustration of the doping mechanism for **(a)** p-type doping and **(b)** n-type doping. Possible paths for charge carrier transfer from acceptor (red) or donor (blue) to the matrix (black) are indicated by arrows. **(c)** Formation of a CT-complex comprising an acceptor (A) and a matrix molecule ($\tilde{M}$). The interaction radii of the CT-complexes are highlighted by the surrounding light gray rings. A charge carrier has to escape of this area to be considered as free.

where $IP_{\tilde{M}}$ is the ionization potential of $\tilde{M}$ and EA_A the electron affinity of A. The values of EA_A and $IP_{\tilde{M}}$ can differ from solid state electron affinity and ionization potential since polarization energies [5, 39, 45] of the ionized states have to be considered (see Eq.8 in Subsection 2.1.1).

In a second step of the reaction, to provide a free charge carrier, the CT-complex has to dissociate. The dissociation probability P can be approximated by means of Boltzmann statistics as

$$P \sim exp\Big(-\frac{E_B}{k_BT}\Big). \tag{36}$$

Thus, the CT-complex binding energy is the main parameter that governs the effectiveness of doping within this model.

Two questions are subject to ongoing scientific debate [39, 42, 46–51]: (1) is dissociation of CT-complexes taking place at room temperature and (2) how do acceptor molecules behave within the matrix after dissociation and how is that affecting charge carrier transport?

To discuss the first question, Boltzmann statistics is assumed. Moreover, if the CT-complex is described by a two level system which accounts for acceptor LUMO and matrix HOMO levels, the position of the quasi-Fermi level can be derived from the neutrality equation $p = N_A$ (p density of free holes, N_A density of ionized acceptor states) as

$$E_F = \frac{E_B}{2} + \frac{k_BT}{2}ln\frac{N_V}{N_A^0} \tag{37}$$
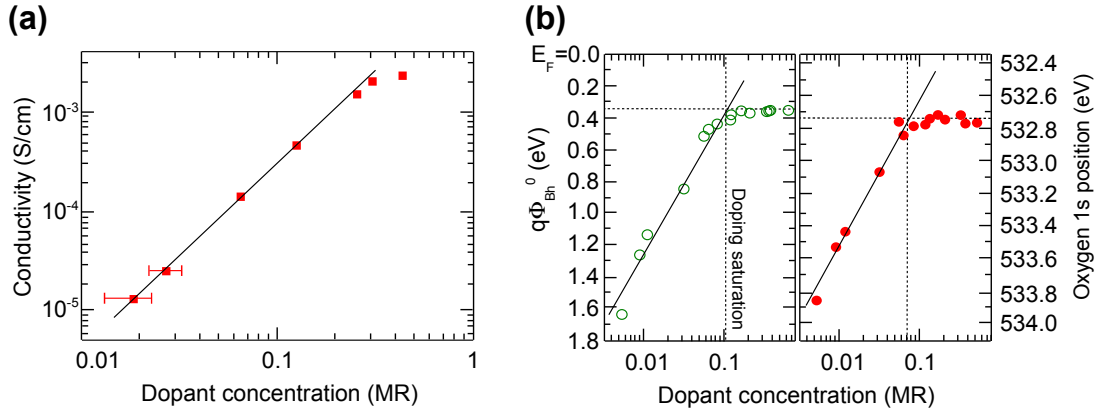
Figure 10: (a) Electrical conductivity of a molecularly doped organic semiconductor thin film. A slight super-linear increase is visible. The matrix materials is the amorphous material $MeO - TPD$. It is doped by the strong acceptor molecules $F4 - TCNQ$ (see Subsection 3.5 for clarification of material acronyms). The ionization potential of $MeO - TPD$ is $5.1eV$ and the electron affinity of $F4 - TCNQ$ is $5.24eV$ [44]. **(b)** Shift of the hole injection barrier $q\Phi_{Bh}^0$ with respect to the quasi-Fermi level (intrinsic case) and shift of the oxygen $1s$ energy position. Both quantities are directly correlated to the difference between quasi-Fermi level (doped case) and charge transport states. Redrawn from [44].

where N_V is the density of hole transport states and N_A is the density of acceptor states[5]. Relying on this result, the acceptor state can be denoted as shallow if

$$E_B << k_B T \ ln\frac{N_V}{N_A^0} \qquad (38)$$

is fulfilled. Shallow acceptor state in this context means that no thermal activation for the dissociation of the CT-complex is necessary. For technical relevant dopant concentrations ($0.1mol\% - 10mol\%$, see Subsection 3.5), E_B has to be less than $0.1eV$ to be considered as shallow. However, this is far less than one would expect for the Coulomb binding energy of two oppositely charged particles within a typical distance of two neighboring molecules. In other words, the acceptor level is supposed to be deep. However, statements can hardly be generalized since E_B can be significantly lowered by effects such as: lattice polaron coupling, electronic and vibronic polaron coupling, as well as self-polarization of molecules due to additional charges [39] (compare Koopman's theorem).

In contrast, experimental observations suggest large dissociation probabilities of CT-complexes [39, 44, 51]. This discrepancy can be explained by the fact that typically strong acceptor molecules are used as dopant. In particular, the electron affinity of the dopant is larger than the ionization potential of the matrix material ($E_B < 0$, compare Figure 9). This situation facilitates an efficient dissociation of CT-complexes and an

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[5]Further, $p << N_A^0$ is assumed.

increased number of free charge carriers.

If free charge carriers can be sufficiently generated by doping, the influence of these free charges and the ionized dopant states on charge carrier transport has to be discussed. Important parameters of charge carrier transport are electrical conductivity, charge carrier mobility, the position of quasi-Fermi level, the amount and distribution of trap states, and the DOS of the matrix material. Theoretical predictions on the influence of doping on charge carrier transport are challenging since they have to reflect all quantities and dependencies as mentioned above. Nevertheless, basic tendencies will be discussed.

The influence of doping on electrical conductivity is twofold. It firstly influences the amount of free charge carriers, but it also affects charge carrier mobility owing to its influence on the disorder in organic semiconductor material. Nevertheless, experimental investigations concordantly show a super-linear increase of electrical conductivity upon doping [38, 42, 52, 53]. This can partially be explained by the shift of the quasi-Fermi level toward the charge transport states. However, to explain the super-linear increase of conductivity upon doping, sophisticated models that assume an extended density of states have to be employed [54]. In particular, the dependency of charge carrier mobility on the density of free charges leads to the super-linear increase of conductivity. Also the density of free charge carriers exhibits a super-linear increase caused by doping. This has been confirmed by several techniques such as ultraviolet photoelectron spectroscopy (UPS) [44, 55], Seebeck coefficient measurements [38, 39, 52, 56, 57], and field-effect transistor studies [42]. In Figure 10 the increasing electrical conductivity upon doping and the shift in quasi-Fermi level are shown for a matrix-dopant system often used in organic light emitting diodes. For high mobility organic semiconductors, such as the buckyball molecule C_{60}, layer conductivities of up to $100 S/cm$ have been reported by Haddon et al. [37]. However, as mentioned above, analytical dependencies of E_F vs. dopant concentration and electrical conductivity vs. dopant concentration are specific to every material dopant-matrix system. An analytical dependency has to reflect the specific density of states, the trap distribution, as well as all details of dopant-matrix interaction.

Concerning charge carrier mobility vs. dopant concentration, both an increasing and a decreasing mobility upon doping has been reported. Arkhipov et al. [46, 47] studied the influence of the width of a Gaussian DOS of the matrix material on charge carrier mobility. Furthermore, they investigated the effect of deep Coulomb traps induced by ionized dopants in the framework of a multi-step Onsager-like process. They argued that in a low disorder material ($\hat{\sigma} = 60 meV$, compare Eq.26) charge carrier mobility is decreasing for low and moderate dopant concentrations ($< 1 mol\%$) owing to strong localization of charge carriers within Coulomb traps. For higher dopant concentrations, however, the interaction radii of Coulomb traps overlap, which leads to a reduced activation energy for trap release. Therefore, mobility is increased. For strongly disordered systems ($\hat{\sigma} \sim 0.1 eV$) Arkhipov et al. reported a continuous increase of charge carrier mobility upon doping which is caused by a filling of intrinsic deep trap and tail states of the matrix material. Both findings are in accordance to experimental investigations [38, 42, 46]. In particular, sophisticated DOS models (extended Gaussian disorder models

(EGDM)) can quantitatively describe the dependency between charge carrier mobility and the density of charges [54].

Also other effects such as impurity scattering [52, 56] and structural phase transitions in poly-crystalline materials [49] have been presented in order to explain the mobility vs. dopant concentration behavior. The loss of charge carrier mobility owing to a crystalline to amorphous phase transition will be discussed in Subsection 5.1.

An approach to explain the super-linear increase of conductivity upon doping neglecting the presence of deep trap states has been presented by Maennig et al. [42]. Within this model, charge carrier transport is described by a percolation path theory as proposed by Ambegaokar et al. [18]. The increase of conductivity is found to originate from the energetic alignment of molecular transport states with respect to the quasi-Fermi level. In this way, conductive paths for charge carrier transport appear. Furthermore, assuming a exponential DOS, this model predicts a super-linear increase of conductivity upon doping as a direct consequence arising from the percolation path theory.

2.2 Organic Diodes

Within this subsection, the basic properties of organic diodes are discussed. Despite the
commercial success of organic light emitting diodes and solar cells, basic mechanisms such
as charge carrier transport within the junction are still under scientific debate. Thus, a
deeper insight into the fundamentals of organic diodes is indispensable to continue the
rise of organic electronic devices as seen in the past.

To begin with, the metal-semiconductor interface as the simplest stack showing a diode-
like performance is considered. These so-called Schottky contacts are present in almost
every type of electronic devices. In some devices they take part in the functionality e.g.
in Schottky diodes, in other devices they are parasitic and the challenge is to overcome
these barriers. This can be done e.g. by doping.

The main part of this subsection will be on organic pin-diodes. These devices are fa-
vorable for electronic applications since they offer a certain degree of freedom in terms
of stack design. Specifically, several important diode parameters such as forward re-
sistance, reverse resistance, reverse capacitance, and charge carrier transit time can be
adjusted. It will be shown how one can evaluate these important quantities by impedance
spectroscopy and how one can make use of this knowledge to design organic diodes for
ultra-high-frequency (UHF) applications.

It is challenging to predict dynamic properties of an organic diode. This aspect can be
ascribed to the complex situation of charge carrier transport which is even more com-
plicated at high current densities, high trap densities, or high electric fields. Therefore,
first the static properties (no current flow) are discussed. As it will be shown, important
quantities that can be measured e.g. by impedance spectroscopy can be deduced from
these static properties. In a second step these considerations are extended to dynamic
properties taking current flow into account. In that context important equations that
can be used to provide a quantitative current-voltage (I-V) model are summarized. Dy-
namic properties of organic diodes are often described referring to Shockley's theory.
However, it should be strictly avoided to give complete expressions for current-voltage
behavior according to Shockley's theory without discussion of the underlying basic phys-
ical assumptions. It is worth to check these assumptions since in a majority of cases the
physical situation does not allow to adopt these models without modifications.

Furthermore, it should be mentioned that within this subsection, merely organic diodes
that contain doped organic layers are discussed. Also organic diodes comprising only
intrinsic layers have often been reported. However, organic diodes with doped layers,
especially pin-diodes, are favorable for a theoretical description since Ohmic injection
can be assumed.
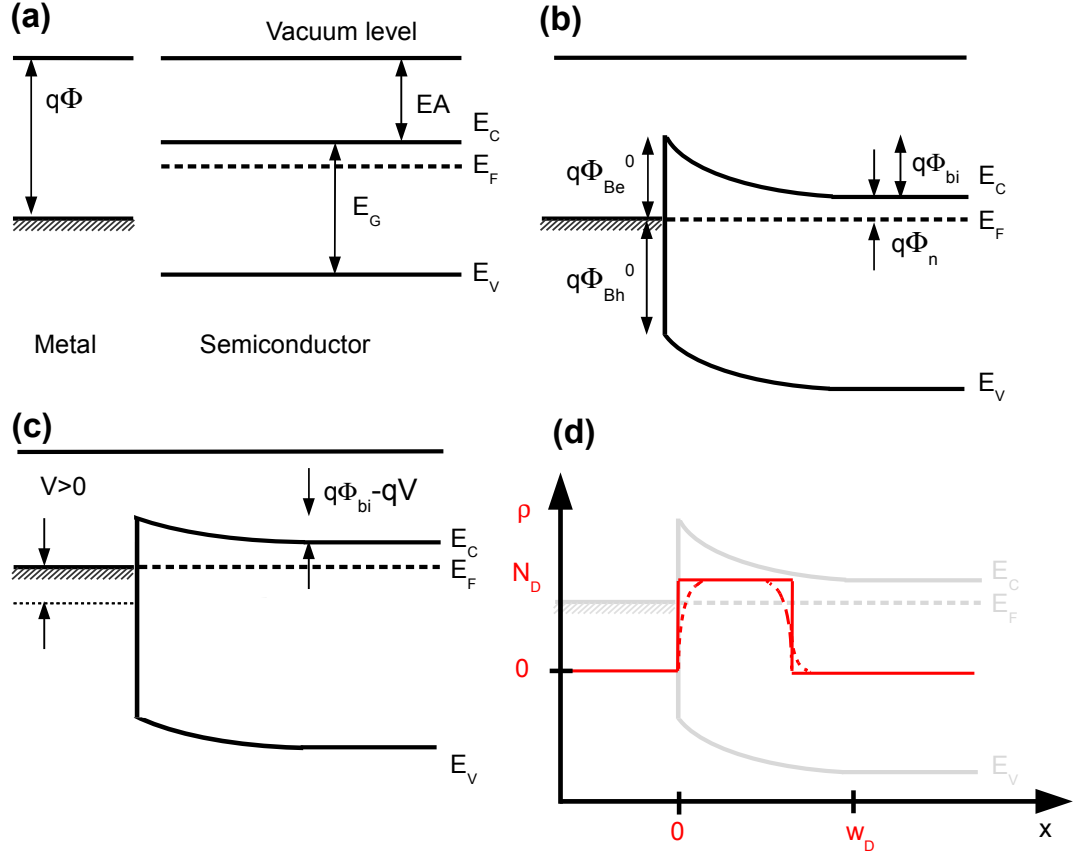
Figure 11: Energy-level diagrams for a metal-semiconductor contact (n-type doped semiconductor) for different situations: **(a)** before contact, **(b)** in contact but without external voltage, **(c)** in forward voltage direction where the barrier Φ_{Be}^0 is lowered. **(d)** Space charge density ρ distribution for a contact as shown in **(b)** (abrupt junction condition, closed line). Within $0 \leq x \leq w_D$ all donor states are ionized which leads to $\rho = N_D$. The dashed line indicates the situation if the abrupt junction condition is not fulfilled. Valence E_V and conductance E_C states of the semiconductor are represented by one dominating level with an energy gap E_G in between.

2.2.1 The Metal-Semiconductor Interface

Static conditions (zero current): When a metal and a semiconductor are brought in contact, an energy barrier appears instantaneously owing to the difference of the work functions. If effects of interface states and charge carrier injection are neglected for the moment, the barrier height for holes and electrons can be expressed as

$$q\Phi_{Be}^0 = q\Phi - EA \tag{39}$$

$$q\Phi_{Bh}^0 = E_G - q\Phi + EA, \tag{40}$$

where $q\Phi$ is the metal work function and E_G is the energy gap between hole and electron transport states in the semiconductor. In the following, a n-type doped semiconductor is

discussed. This situation is displayed in Figure 11. A consequence of the rearrangement of quasi-Fermi levels is that the conductance states within the semiconductor experience a gradient of the quasi-Fermi level in space $\partial E_F/\partial x \neq 0$. Accordingly, mobile charge carriers move away from the interface into the bulk of the semiconductors. This movement is compensated by the so-called built-in potential Φ_{bi}. Thus, within steady-state conditions a certain region close to the interface is depleted of mobile charge carriers. The remaining immobile donor states cause a space charge layer. In order to derive analytical solutions that can be used in further discussions, this space charge zone can be treated as a rectangular distribution with a width w_D (abrupt junction condition). This assumption is justified for $q\Phi_{bi} >> k_B T$ or $w_D >> L_D$ where L_D is the Debye length

$$L_D = \sqrt{\frac{\epsilon_0 \epsilon k_B T}{q^2 N_D}} \tag{41}$$

of the semiconductor material with a density of ionized donors N_D. The Debye length is a measure for a typical screening length of electric field in a dielectric material. For most Schottky contacts the upper condition is fulfilled since built-in potentials are typically $> 0.2V$.

To find the electric field, the width of the charge depletion zone, and the junction capacitance for this given charge carrier distribution, the Poisson equation under the condition $\rho = q N_D$ for $0 \leq x \leq w_D$ and $\rho = 0$ elsewhere has to be solved. Integration with regard to these boundary conditions (compare e.g. [6]) leads to the width of the charge depletion zone as

$$w_D = \sqrt{\frac{2\epsilon_0 \epsilon}{q N_D}\left(\Phi_{bi} - V\right)}. \tag{42}$$

As mentioned before, this is merely justified for $q\Phi_{bi} >> k_B T$. If this condition is not fulfilled the potential term in Eq. 42 is lowered by $k_B T/q$ [6].

Within the framework of the abrupt junction condition, the depletion capacitance of the contact can be formulated as

$$C_D = \frac{\epsilon_0 \epsilon A}{w_D} = \sqrt{\frac{q\epsilon_0 \epsilon N_D A^2}{2[\Phi_{bi} - V]}}, \tag{43}$$

which immediately leads to the so-called profiler equation

$$\frac{1}{C_D^2} = \frac{2}{q\epsilon_0 \epsilon N_D A^2}(\Phi_{bi} - V), \tag{44}$$

where A is the area of the device. This equation can be used as a standard procedure to evaluate dopant concentrations by impedance spectroscopy.

Unfortunately, the situation described above is typically not observed in experiments. This is related to interface charges and the effect of image-force lowering of the barrier, which both will be discussed. However, the formalism developed for description of image-force lowering can be employed to describe the effect of interface charges. Therefore, the

effect of image force lowering is discussed in a first step.

As depicted in Figure 12(a), an electron has to overcome a certain potential barrier for injection into a semiconductor material. If an electron has left the metal, it induces a positive charge within the metal. Thus, according to the image-force method, when the electron is at a point x, the positive counter charge appears at a position $-x$, which leads to an electrostatic force F of

$$|F| = -\frac{q^2}{16\pi\epsilon\epsilon_0 x^2}, \tag{45}$$

which modifies the energy barrier. However, the potential energy within this system is not only governed by this electrostatic force, but furthermore the electric field $\mathcal{E}(x)$ in the semiconductor has to be taken into account. Due to the built-in potential, an electric field is always present even without applied external voltage.
Considering these effects, the potential energy PE can be written as (assuming a constant field)

$$PE(x) = -\frac{q^2}{16\pi\epsilon\epsilon_0 x} - q|\mathcal{E}|x. \tag{46}$$

As illustrated in Figure 12(b), this energy has a maximum at

$$x_m = \sqrt{\frac{q}{16\pi\epsilon\epsilon_0|\mathcal{E}|}}, \tag{47}$$

and hence the effective barrier height is lowered at the point x_m by an energy of

$$q\Delta\Phi_{if} = \sqrt{\frac{q^3\mathcal{E}}{4\pi\epsilon\epsilon_0}}. \tag{48}$$

Thus, the total barrier height for electron injection is reduced to

$$q\Phi_{Be}^0 = q\Phi - EA - q\Delta\Phi_{if}, \tag{49}$$

which allows for a more efficient injection.

With slight modifications this image-force model can be utilized to describe the effect of immobile interface charges. For sake of simplicity, a uniform distribution of interface states at $q\Phi_0$ above the valence state E_V at the interface but below the quasi-Fermi level (see Figure 12(b)) is considered. Hence, they act as acceptor states. In crystalline inorganic materials such interface states arise from the breaking of translation symmetry. For organic semiconductors they can also be inherent to the material or they can be created by chemical interactions between the semiconductor material and the metal during preparation.
The density of interface states D_i (states$/cm^{-2}eV^{-1}$) gives rise to an amount of interface
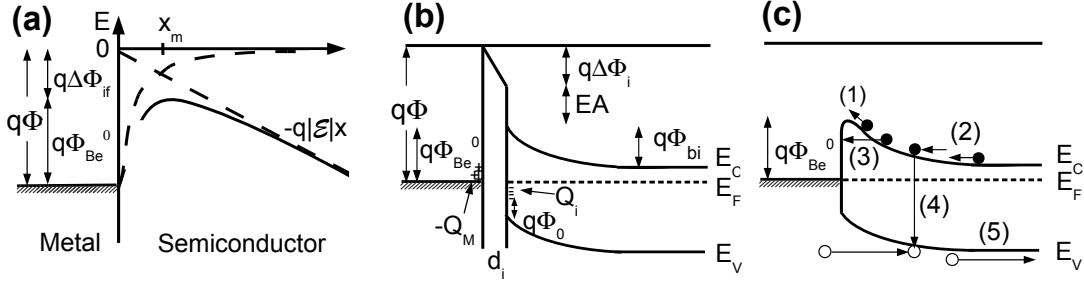
Figure 12: **(a)** Image-force lowering of the barrier by $q\Delta\Phi_{if}$. **(b)** Lowering of the energy barrier for charge carriers caused by interface charges Q_i and the image-force charges $-Q_M$. An interfacial layer with at thickness d_i is present. This layer is transparent for free charge carriers but can withstand a voltage drop across it. **(c)** Possible paths for charge carrier transport. Notation of the paths according to the main text.

charges Q_i according to Figure 12(b) as

$$Q_i = -qD_iA(E_G - q\Phi_0 - q\Phi_{bi} - q\Phi_n) = -qD_iA(E_G - q\Phi_0 - q\Phi_{Be}^0). \qquad (50)$$

The total number of charges within $0 \leq x \leq w_D$ is given by the sum of these interface charges and the ionized donor states $Q_D = qN_Dw_DA$. These charges induce counter charges in the metal. However, the simple image-force picture fails here since the electrostatic force according to Eq.45 has a singularity for the interface charges. This has been firstly pointed out by Bardeen [58]. He addressed this problem by an artificial interface layer with a thickness d_i which is transparent for charge carriers but can withstand a voltage drop across it. The thickness of this layer is in the range of the dimension of an atom. Relying on this image-force method, the potential drop across this interface layer is given by

$$\Delta\Phi_i = \frac{d_i(Q_D + Q_i)}{\epsilon_i\epsilon_0}, \qquad (51)$$

which is basically the potential drop across a charged plate capacitor (interface layer) with a relative permittivity of ϵ_i. The resulting effective injection barrier for charges is therefore reduced to

$$q\Phi_{Be}^0 = q\Phi - EA - q\Delta\Phi_i. \qquad (52)$$

In terms of junction capacitance the consequences are tremendous. The depletion capacitance C_D and the capacitance of the interface layer are coupled in a complex way and a simple expression as given by the profiler equation (see Eq.44) cannot be provided analytically. To be more specific, the two capacitors are connected in series and the parameters of the interlayer capacitance (d_i and ϵ_i) are not independent.

Dynamic conditions The current flow within a Schottky contact contains five different contributions (see Figure 12(c)): (1) thermionic-emission over the barrier, (2) drift and diffusion of majority charge carriers, (3) tunneling of majority charge carriers through

the barrier, (4) majority charge carrier recombination within the space charge region $(0 \leq x \leq w_D)$, and (5) recombination of minority charge carriers within the neutral region of the semiconductor.

The importance of the individual contributions is different and it depends on barrier height for electrons and holes, charge carrier mobility, recombination rates, temperature, and energy gap. Typically, if the semiconductor is doped, the number of minority charge carriers is low. Hence, contributions (4) and (5) are usually not dominant. Thus, the three main contributions are given by thermionic-emission, diffusion, drift, and tunneling of majority charge carriers.

In the following, it is assumed that the established thermal equilibrium remains unaffected by the net current flow (low injection condition).

Thermionic-emission theory for metal-semiconductor junctions has been formulated by Bethe [59]. For barrier heights $q\Phi_{Be}^0 >> k_B T$ and moderate electrical fields (typically $< 1 MV/cm$) thermionic currents provide the main current contribution. The total current flow $j_{S \rightarrow M}$ from the semiconductor to the metal is given by the sum over all charge carriers being able to overcome the barrier by their thermal energy. This can be expressed quantitatively according to [6] as

$$j_{S \rightarrow M} = \int_{E_F - q\Phi_{Be}^0}^{\infty} qv_x dn = \int_{E_F - q\Phi_{Be}^0}^{\infty} qv_x N(E)f(E)dE, \qquad (53)$$

where v_x is the charge carrier velocity in direction of current flow and n is the occupation density of charge carriers which is given by the density of states $N(E)$ and the thermodynamic distribution function $f(E)$.

It is complex to solve this equation for semiconductor materials that exhibit static and dynamic disorder, since the occupation density of charge carriers and the relation between velocity and energy has to be known. For quasi-free particles, as charge carriers are described in a crystalline semiconductor, Eq.53 can be solved analytically which leads to

$$j_{S \rightarrow M} = A^* T^2 exp\Big(-\frac{q\Phi_{Be}^0}{k_B T}\Big) exp\Big(\frac{qV}{k_B T}\Big), \qquad (54)$$

where A^* is the Richardson constant which mainly contains the effective mass of charge carriers as a parameter that reflects the properties of transport within the band of the semiconductor.

However, even if this expression cannot be motivated theoretically for disordered organic semiconductors, the main dependencies $j \sim T^2$ and $j \sim exp(V)$ are often observed for organic Schottky contacts [60]. This is presumably related to the following two facts: (1) $v_x \sim \sqrt{(T)}$ is a rather general dependency between velocity and temperature and (2) for one dominant transport level, $n = \int N(E)f(E)dE$ can be simplified by an effective density of states and Boltzmann statistics. Relying on these assumptions the upper integral provides the typical voltage and temperature dependencies as mentioned above [6].

The second important current contribution is tunneling of majority charge carriers. The

magnitude of tunneling current can be written as

$$j_{tunnel} \sim \int_{E_F}^{q\Phi_{Be}^0} f_S(E) T(E)(1 - f_M(E)) dE,$$ (55)

where $T(E)$ is the tunneling probability and $f_S(E)$ and $f_M(E)$ are the Fermi distributions in the semiconductor and in the metal, respectively. Again, this equation can be solved if charge carriers can be treated as quasi-free particles that move in a parabolic band structure. This either leads to the Fowler-Nordheim formula [6] for triangular barriers

$$j_{tunnel}^{FN} = \frac{c_5 V^2}{q\Phi_{Be}^0} exp\Big(-\frac{c_6 (q\Phi_{Be}^0)^{3/2}}{V}\Big),$$ (56)

or to

$$j_{tunnel}^{rect} = A^* T^2 c_7 exp\Big(-\frac{q\Phi_{Be}^0}{k_B T}\Big)\Big[exp\Big(-\frac{qV}{\eta k_B T}\Big) - 1\Big]$$ (57)

for a rectangular barrier shape. The parameters c_{5-7} are constants (compare reference [6]) and η is the ideality factor which is given by

$$\eta = 1 + \frac{d_i}{\epsilon_i \epsilon_0} \frac{\epsilon \epsilon_0 / w_D + q D_i}{1 + (d_i/(\epsilon_i \epsilon_0)) q D_i}.$$ (58)

From an experimental point of view it is challenging to distinguish between these two cases since they are typically present in parallel. Moreover, in the high field limit both functions provide similar dependencies since the shape of the barrier is less important under these conditions. Nevertheless, tunneling currents play an important role for organic Schottky contacts especially for large doping concentrations and high electric fields.

The third component of current in a metal-semiconductor diode is the drift-diffusion current of majority charge carriers. Its contribution can be calculated by the drift-diffusion equation

$$j_{DD} = qn(x)\mu_e(n, T, V)\frac{\partial V}{\partial x} + D_e \frac{\partial n(x)}{\partial x}$$ (59)

which has to be integrated. For that purpose a relation between electron mobility μ_e and diffusion constant D_e needs to be derived. Relying on the definition of mobility (see Eq.10) and diffusion constant ($D_e = \langle v_x^2 \tau \rangle$) this relation is given by

$$\frac{D_e}{\mu_e} = \frac{\langle v_x^2 \tau \rangle}{\frac{q}{m^*}\frac{\langle \mathcal{E}\tau \rangle}{\langle \mathcal{E} \rangle}} = \zeta(n, T, V) \quad \overset{\text{for quasi-free particles}}{\Rightarrow} \quad \frac{D_e}{\mu_e} = \frac{k_B T}{q}.$$ (60)

Generally, if ensemble averages are not independent ($\langle ab \rangle \neq \langle a \rangle \langle b \rangle$, a and b are observables of the ensemble) this relation is denoted as generalized Einstein equation. The mobility-diffusion constant relation is a complex function of temperature, electric field, and charge carrier density. Only for quasi-free particles, it can be reduced to the simple form as given in Eq.60. However, this assumption is presumably not justified for disordered organic semiconductors where charge carrier transport is dominated by hopping

between localized sites. Unfortunately, for this general case Eq.59 cannot be integrated analytically for an arbitrary function $\zeta(n, T, V)$. Nevertheless, an analytical solution can be found if ζ is restricted to $\zeta = \zeta(T)$. As shown e.g. by Harada et al.[61] this leads to

$$j_{DD} = j_0 \left[exp\left(\frac{-qV}{\zeta(T)}\right) - 1 \right]. \tag{61}$$

with the so-called dark current j_0 given by

$$j_0 \sim c_8 \mu_e \exp\left(\frac{-q\Phi_{Be}^0}{\zeta(T)}\right), \tag{62}$$

where the constant c_8 reflects the chosen density of states function (compare e.g. [6, 62]). The assumption of $\zeta = \zeta(T)$ is likely justified for low charge carrier densities and low voltages. For the upper derivation of j_{DD}, however, a dependency of ζ on voltage and charge carrier density has been neglected explicitly. Hence, observations on a temperature, voltage, and charge carrier density dependence of ζ directly reflect derivations from the Einstein relation. The function $\zeta(n, T, V)$ predominately contains information about the dependencies of mobility and the specific DOS function. In the next paragraph, these aspects will be reconsidered for organic pin-diodes.

2.2.2 The Organic pin-Diode

The term pin- or pn-diode[6] is often used in context of organic diodes, particularly for devices like organic light emitting diodes and solar cells. Unfortunately, rather often this term is not justified since these devices merely contain undoped materials (see e.g. [63]) that are either favorable for electron or hole transport. The following considerations are restricted to organic pin-diodes which follow the layer sequence: doped charge transport layer, intrinsic interlayer, and doped charge transport layer. Hereby, the two charge transport layers are oppositely doped so that one is restricted to electron transport and one to hole transport.

Owing to doping the depletion width in the doped layers at the interface to the metal contacts becomes extremely thin (in the range of $1nm$ [40]) which enables a highly efficient injection of charge carriers by tunneling. These so-called Ohmic contacts allow to focus on transport phenomena that occur inside the organic material. As direct consequence of the extremely thin depletion zones, an intrinsic organic layer has to be added between the doped hole and electron transport layers (HTL and ETL) to prevent a direct charge transfer by either diffusion or tunneling. Nevertheless, it should be mentioned that organic pn-diodes without intrinsic layer are possible in case of very low dopant concentrations or in case of ineffective doping. This is surely interesting for investigations on basic interface formation properties. However, low dopant concentrations are difficult to

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[6]pin - **p**-type doped layer, **i** layer, and **n**-type doped layer
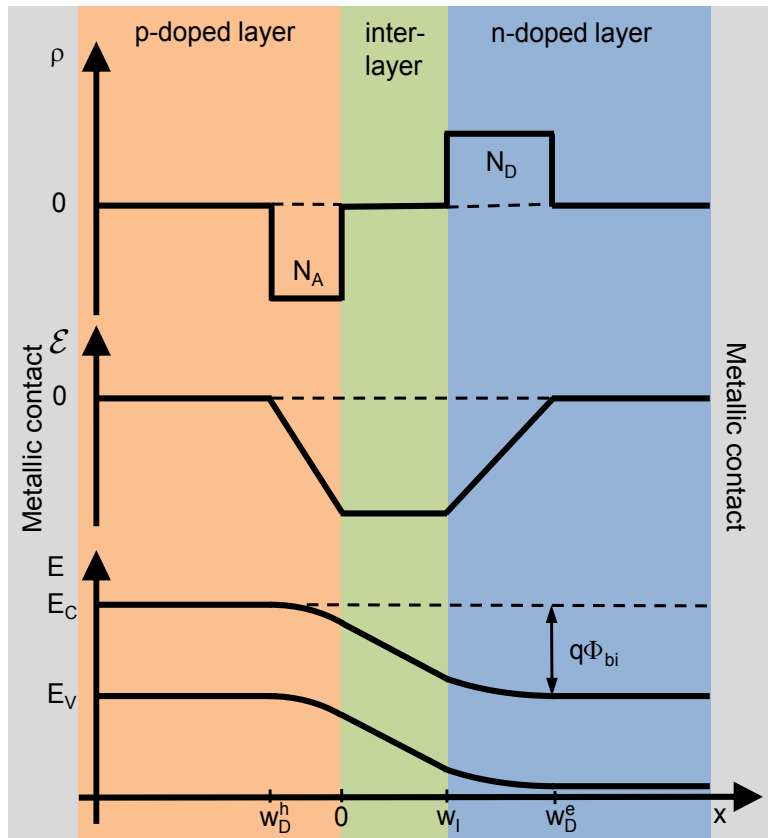
Figure 13: Charge carrier density ρ, electric field $\mathcal{E}$, and energy-level diagram for a pin-diode relying on the abrupt junction condition. The different dopant concentrations in the doped layers lead to different depletion layer widths.

control and inefficient doping is not preferable for applications.

In general, pin-diodes are favorable for electronic and optoelectronic applications since the intrinsic layer takes part in the functionality of the device and therefore the performance can be tuned by modifications of the intrinsic region.

Static conditions (zero current): The static energy-level diagram of a pin-diode and the corresponding space charge profile are displayed in Figure 13. In analogy to the metal-semiconductor contact the field distribution within the junction can be derived from Poisson's equation. The electric field, which is present in the diode to compensate the different chemical potentials in the doped layers, repels charge carriers from the interface between doped and intrinsic layer. Hence, a charge depletion zone in the doped layers at the interface to the intrinsic layer is formed. For simplicity two assumptions for further mathematical description have to be made: (1) the diode is a homo-diode which consists of only one matrix material and the relative permittivity is equal in the p-, i-, and n- layer, (2) the abrupt junction condition is fulfilled and the intrinsic layer with a thickness w_I as well as the depleted zones in the doped layers (w_D^n and w_D^p) are vacant of free charge carriers. Relying on these assumptions, the Poisson equation can be specified

to

$$\frac{\partial^2 U}{\partial x^2} = -\frac{\rho}{\epsilon\epsilon_0} = \frac{1}{\epsilon\epsilon_0} \begin{cases} -qN_A & w_D^h \le x \le 0 \\ 0 & 0 \le x \le w_i \\ qN_D & w_I \le x \le w_D^e, \end{cases} \tag{63}$$

where N_D and N_A are the numbers of ionized donor and acceptor states. With respect to boundary and transition conditions and with respect to charge neutrality ($N_D w_D^e = N_A w_D^h$), Eq.63 can be integrated. In this way the potential drop across each layer can be quantified as

$$\Phi_p = \frac{qN_A(w_D^h)^2}{2\epsilon\epsilon_0}, \qquad \Phi_i = \frac{qN_A w_D^h w_I}{\epsilon\epsilon_0}, \text{ and } \qquad \Phi_n = \frac{qN_D(w_D^e)^2}{2\epsilon\epsilon_0}. \tag{64}$$

The sum of all these three potential drops equals the built-in potential Φ_{bi} of the diode and the applied external voltage V as

$$\Phi_p + \Phi_i + \Phi_n = \Phi_{bi} - V. \tag{65}$$

Finally, the width of the charge depletion zones can be deduced from Eq.64, Eq.65, and the charge neutrality condition. This leads to (exemplarily for the depletion in the n-layer)

$$w_D^e = \frac{\sqrt{w_I^2 + \frac{2\epsilon\epsilon_0}{q}\frac{(N_A+N_D)}{N_A N_D}(\Phi_{bi} - V)} - w_I}{1 + \frac{N_D}{N_A}}. \tag{66}$$

The total depletion width w_D^{tot} can therefore be written as

$$w_D^{tot} = w_D^e + w_D^h + w_I = \sqrt{w_I^2 + \frac{2\epsilon\epsilon_0}{q}\frac{(N_A + N_D)}{N_A N_D}(\Phi_{bi} - V)} \tag{67}$$

which can be used to formulate the depletion capacitance of the pin-diode as

$$C_D = \frac{\epsilon\epsilon_0 A}{w_D^{tot}} = \frac{\epsilon\epsilon_0 A}{\sqrt{w_I^2 + \frac{2\epsilon\epsilon_0}{q}\frac{(N_A+N_D)}{N_A N_D}(\Phi_{bi} - V)}}. \tag{68}$$

It should be emphasized that the upper term for the depletion capacitance is not equivalent to the naive approach of the series connection of the depletion capacitances of the doped layers and the static capacitance of the intrinsic layer. This can be attributed to the fact that the applied external voltage drops partially across the intrinsic layer and partially across the depleted zones within the doped layers. Nevertheless, Eq.68 can be employed in the same way as the profiler equation (compare Eq.44) to evaluate dopant concentrations.

Dynamic conditions The current-voltage behavior of organic pin-diodes is discussed for low injection conditions (or better low field conditions). This is extended afterwards to the high field range and finally basic mechanisms for charge carrier transport in reverse
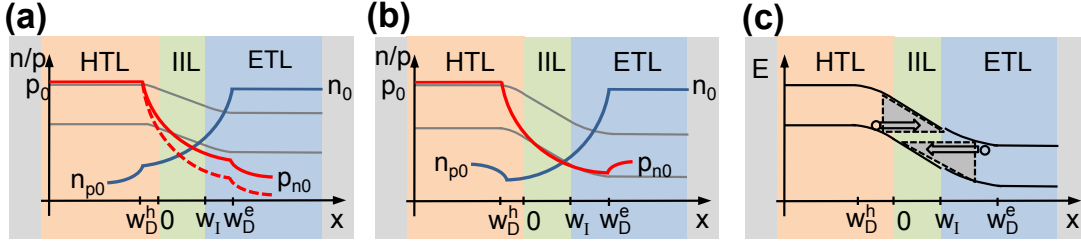
Figure 14: Charge carrier density distribution for electrons (n) and holes (p) in case of **(a)** forward voltages, and **(b)** moderate reverse voltages. The quantities p_0 (n_0) and p_{n0} (n_{p0}) denote the equilibrium charge carrier density for majority and minority charge carriers, respectively. In **(a)** the red dashed line displays the case of strong recombination in the intrinsic layer. **(c)** Energy-level diagram for the situation of high reverse fields where tunneling of charge carriers from valence to conductance states can take place (Zener tunneling).

direction are summarized.

At low fields it is worth to reconsider the assumptions that lead to the Shockley equation for inorganic pn-diodes. These assumptions can be summarized as:

- charge carriers are able to diffuse into the neutral region of the opposite site (holes reach the n-doped layer $(x > w_D^e)$ and electrons each the p-doped layer $(x < w_D^h)$),

- charge carriers recombine within this neutral region as minority charge carriers with a constant rate, and

- there is no recombination within the charge depletion zones.

All these assumptions lead to the Shockley equation

$$j = j_0(exp\Big(\frac{qV}{k_BT}\Big) - 1). \tag{69}$$

If this formula could be adopted directly to organic pin-diodes, this would imply that charge carriers can diffuse through the entire intrinsic layer without recombination. Although this might be justified for some specific materials that have a high diffusion constant, the assumptions that lead to the Shockley equation cannot be adopted for organic pin-diodes in general. The ability of a charge carrier to diffuse is given by its diffusion length $L_{diff} = \sqrt{D\tau_{min}}$ where τ_{min} is the minority charge carrier lifetime[7]. This length has to be significantly larger than the intrinsic layer thickness w_I to justify the assumption for the Shockley equation.

Nevertheless, from various experimental studies [61, 63] it has been deduced that organic

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[7]Minority charge carrier lifetime in organic materials is actually unknown. However, L_{diff} can be estimated assuming $\tau_{min} = 1ns$ (an estimated lower limit, also higher value of $> 10^{-6}s$ have been reported [64]). For $D = 10^{-5}cm^2/s$ the diffusion length would be merely $1nm$ while for $D = 10^{-2}cm^2/s$ it would be up to $30nm$.

pin-diodes follow an I-V behavior according to

$$j = \frac{V}{R_p} + j_0(exp\Big(\frac{qV}{\theta_{NI}(n,T,V)}\Big) - 1), \tag{70}$$

where R_p represents a parallel resistance and $\theta_{NI}(n,T,V)$ is an empirical function. This equation suggests a close similarity to the Shockley equation for ideal pn-diodes (identical for $\theta_{NI} = k_B T$). However, this comparison is not allowed since the Shockley equation requires the validity of the Einstein relation (compare Eq. 60). Furthermore, for the Shockley equation recombination within the charge depletion zones or the intrinsic layer of the pin-diode is neglected. However, for organic diodes with $L_{diff} \approx w_I$ or $L_{diff} < w_I$ this cannot be assumed. For such diodes the master equation for transport contains not only drift and diffusion contributions but also a strong recombination part. Therefore, the continuity equation (for electrons, analog for holes) can be written according to [6, 62] as

$$D\frac{\partial^2 n}{\partial x^2} + \mu n\frac{\partial \mathcal{E}}{\partial x} + \mu\mathcal{E}\frac{\partial n}{\partial x} + \mathcal{R}(p,n,T,V) = 0 \tag{71}$$

where $\mathcal{R}$ is a function that describes the recombination process and p is the hole density In general, this coupled system of 2nd order differential equations can merely be solved numerically for a given function $\mathcal{R}$. In the Shockley picture, the master equation for holes and electrons is decoupled since recombination solely occurs for minority charge carriers. Thus, the situation for organic diodes is rather complex since the changing recombination profile with charge carrier mobility, charge carrier density, and electric field does not allow general statements. A typical charge carrier density distribution in forward voltage direction is shown in Figure 14(a).

For low mobility materials the situation is described as follows: for low electric fields holes and electrons are not able to diffuse into the intrinsic layer for a sufficient hole-electron recombination. Therefore, the total current can be associated with a parallel resistance R_p[8]. For larger fields ($V < \Phi_{bi}$), the recombination profile is extended and charge carriers can recombine within the intrinsic layer. The value of the function θ_{NI} is then typically in a range of 2...3. For high mobility materials, however, charges are already able for low fields to recombine efficiently in the intrinsic layer. Hence, no strong parallel resistance is observed. For larger fields ($V < \Phi_{bi}$) an exponential slope of the I-V curve can be obtained and the function θ_{NI} varies between 1 and 2 (compare e.g. [61]).

Thus far it has been assumed that charge carriers are injected into the intrinsic layer in forward voltage direction, but the charge carrier density within this layer remains significantly lower than the density within the doped layers. However, this condition is surely violated at high electric fields if V excceds Φ_{bi}. This condition is denoted as high injection condition. A first consequence of this high injection scenario is that the electric field within the intrinsic layer is not constant as assumed so far (compare Eq.63). The

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[8]Since electron-hole recombination can be neglected for low electrics fields, charge carriers recombine via trap states which leads to a constant recombination rate (compare [6]).

second significant difference related to the high injection condition is provided by the fact that transport within the intrinsic layer is not governed by diffusion but rather by drift for $V > \Phi_{bi}$. These modifications have to be taken into account in order to solve Eq.71.

However, focusing on high mobility organic materials it can now be assumed that owing to the drift current, charge carriers can pass the intrinsic layer without recombination. However, if they reach the opposite side of the junction they recombine immediately as minority charges. In this picture one can solve the Poisson equation with regard to Ohm's law which leads to a current-voltage relation according to

$$j = \frac{9}{8} \mu \epsilon \epsilon_0 \frac{(V - \Phi_{bi})^2}{w_I^3}. \tag{72}$$

This relation is known as the space charge limited current (SCLC) relation, which means that the electric field, generated by the charge carriers, leads to a non-uniform charge carrier density within the layer. In particular, the charge density has a maximum directly at the electrode where charge carriers are injected. If just one kind of charge carriers is present in the intrinsic layer, Eq.72 allows for a direct evaluation of charge carrier mobility. For two species of charge carriers the general form of this formula remains unchanged. However, the value of mobility has to be treated as an effective value of mobility. This assumption is justified since recombination of holes and electrons within the intrinsic layer of the pin-diode can be neglected for high mobility materials. However, this is unlikely in case of low mobility materials. Therefore, Eq.71 has to be solved in its entire complexity[9].

For description of reverse voltage charge carrier transport, low and high field behavior has to be distinguished as well. Mechanisms of transport in reverse direction are barely discussed in the literature [65] since the electric field within the junction has to be precisely controlled. Here, some possible scenarios of charge transport for reverse voltage conditions are briefly summarized. Systematic studies on this are a main topic of investigation within this thesis and results are presented in Section 4.1.

In the low field regime transport in reverse direction is related either to direct shunt paths or to a thermally activated generation process of charge carriers. Direct shunt paths typically arise from layers that do not perfectly overlap, which leads to a current that flows at layer edges. Another possible direct shunt path may appear from direct conductive paths through the intrinsic layer (e.g. penetration of doped material in the intrinsic layer) that connect the doped layers. Both shunt paths typically display an Ohmic behavior.

The second low electric field mechanism is the generation of charge carriers within the depleted zones of the junction by thermal activation. A direct valence to conductance

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[9]Distinguishing between low and high mobility materials is also necessary owing to the different recombination mechanisms that can occur. For low mobility materials bimolecular Langevin theory can describe recombination [5]. For high mobility materials, however, bimolecular recombination can be neglected owing to the low capture cross section. Instead, direct recombination [6] is taking place.

state excitation at room temperature is unlikely since energy gaps of small molecule organic semiconductors are in the range of $2 - 3eV$. However, excitation can be supported by mid-gap trap states and tails of valence and conductance states. Hence, the specific current-voltage behavior highly depends on the properties of the used organic semiconductor material. A simple way to reduce the undesired current in reverse direction is to increase the intrinsic layer thickness. This involves two different effects. Firstly, due to the increased interlayer thickness the probability for direct shunt paths is reduced, and secondly the field within the depleted zones of the junction is lowered which causes a smaller contribution of charge carrier generation currents.

In the high field range typically a breakdown of the junction is observed which is reversible for low power dissipation. Based on the steep current-voltage characteristic within the breakdown, this regime is interesting for applications. Specifically, diodes with an adjustable reverse breakdown are utilized as voltage stabilizer in electronic circuits. Hence, the control of the breakdown conditions marks a technical challenge.

Two mechanisms are discussed in context of reverse voltage breakdown: avalanche breakdown and Zener tunneling. Avalanche breakdown is caused by impact ionization by charge carriers of high kinetic energy. Hence, it is a collective effect. Contrary, the Zener effect is related to a direct tunneling from valence to conductance states through a triangularly shaped barrier (compare Figure 14(b) and (c)). Both mechanisms can be distinguished by their temperature dependence in case of band-like transport. However, this is not possible for organic semiconductors owing to influences of structural disorder on the temperature dependence of transport processes. Nevertheless, two aspects can be employed to decide on the probability for both processes in organic semiconductors: (1) the probability of ionization is typically low due to the low minority charge carrier density (related to the large energy gap) in organic semiconductors and (2) charge carriers reside between two hopping steps in localized states and accordingly their kinetic energy is low. Hence, Zener tunneling is more likely than the avalanche breakdown.

Experimental observations and a theoretical model for Zener-like tunneling process in organic semiconductors are discussed in detail in Section 4.1.

2.2.3 Impedance Models for Organic Diodes

The I-V characteristic of an organic diode is actually a rather poor method to study charge carrier transport models, since empirical functions of the current-voltage expression (compare Eq.70) are difficult to associate to modeling parameters. Impedance spectroscopy can partially help to overcome this problem since it provides more information on the underlying transport processes.

Here, a small signal impedance model that has been developed originally for inorganic pn-diodes [66] will be introduced. Originally, this model assumes that charge carriers

have a diffusion length larger than the width of the depleted zones in the doped layers. However, recombination of charge carriers is also included within this model. Hence, the comparison of the impedance behavior of an organic pin-diode to this impedance model will indicate if diffusion is a dominant process in organic pin-diodes and if charge carriers are able to reach the opposite side of the junction before they recombine. The model which will be presented here has already been successfully adopted to organic Schottky diodes that comprise high mobility polymer materials [64].

This impedance model is again based on a charge carrier transport equation. In particular, diffusion of one charge carrier species through a thin film will be considered where charge carriers have a constant recombination rate k. The model can also be extended to ambipolar transport as it appears in pin-diodes. However, the model cannot distinguish between holes and electrons if they have a similar diffusion length. Hence, the diffusion constant that can be deduced from the impedance analysis reflects an effective value for both charge carrier species. This is similar to the SCLC currents as discussed in the previous paragraph.

In the small signal regime (small signal quantities are labeled by a tilde) the continuity equation and Fick's law can be written for electrons as

$$\frac{\partial \tilde{n}}{\partial t} = -\frac{\partial \tilde{j}}{\partial x} - k\tilde{n} \quad \text{and} \quad \tilde{j} = -D\frac{\partial \tilde{n}}{\partial x}, \tag{73}$$

which is the diffusion equation including constant recombination[10]. A drift current contribution does not appear in Eq.73 for low electric fields and low charge carrier concentrations (low injection condition). Laplace transformation of both quantities $\tilde{j}$ and $\tilde{n}$ according to $\tilde{C}(\omega) = \mathcal{L}(\tilde{n})$ and $\tilde{K}(\omega) = \mathcal{L}(\tilde{j})$ (ω is the angular frequency) leads to

$$\frac{\partial^2 \tilde{C}}{\partial x^2} = \frac{\omega + k}{D}\tilde{C}, \quad \text{and} \tag{74}$$

$$\frac{\partial \tilde{C}}{\partial x} = \frac{1}{D}\tilde{K}. \tag{75}$$

This Helmholtz equation can be solved analytically by an exponential ansatz. Thereby, absorbing boundary conditions ($\tilde{C} = 0$ for $x = w_I$) can be assumed for pin-diodes since it is likely that charges recombine almost immediately if they reach the neutral region of the doped layers at the counter side of the junction. The small signal impedance which is defined as $\tilde{Z} = \tilde{v}(\omega)/\tilde{K}(\omega)$ where $\tilde{v}(\omega)$ is the small voltage signal can be derived as (compare [67] for details)

$$\tilde{Z}(\omega) = R_{DC}\Big(\frac{D}{kw_I^2(1 + i\omega/k)}\Big)^{1/2} tanh\Big(\Big(\frac{kw_I^2}{D}\Big)^{1/2}(1 + i\omega/k)^{1/2}\Big) \tag{76}$$

where R_{DC} represents the static resistance of the device owing to the static voltage superimposed to the small signal voltage $\tilde{v}(\omega)$.

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[10]This assumption is presumably not fulfilled for low mobility materials where bimolecular recombination is the dominant recombination process.
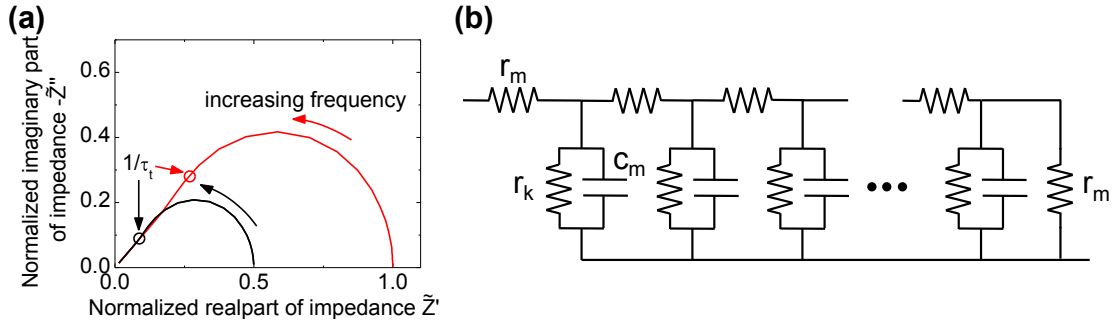
Figure 15: **(a)** Impedance function according to Eq.76 in case of no recombination
($k = 0$, red line) and moderate recombination ($\tau_t = 0.1/k$, black line).
(b) Equivalent circuit representation of the impedance function given
by Eq.76. The infinite number of repetitions is indicated by the three
dots.

To discuss the impedance behavior, recombination is initially neglected ($k = 0$) and the
only transport process that remains is diffusion. For low frequencies ($\omega < D/w_I^2$) all
charge carriers can pass the device and therefore the impedance is described by the par-
allel connection of the static resistance R_{DC} and the capacitance of the layer. Hence,
one can obtain the typical semicircle of an RC-unit in the Bode diagram (see Figure
15(a)). If ω reaches $1/\tau_t = D/w_I^2$ charge carriers are no longer able to diffuse through
the entire layer within a period of the voltage signal. Therefore, τ_t can be associated to a
transit-time for diffusion transport. For frequencies higher than the inverse of this transit
time, the layer behaves as an ideal wave resistance and it strictly follows a $\tilde{Z} \sim (i\omega)^-1/2$
relation.

If recombination is not negligible ($k \neq 0$) the shape of the impedance curve remains
unchanged. However, the point of transition from the wave resistance to the semi-circle
is influenced by the relation between τ_t and k. For $\tau_t < 1/k$ diffusion is still the dominant
process and the transition point mentioned above is determined by τ_t (compare Figure
15(a)). Merely the radius of the semi-circle is changed. For $\tau_t > 1/k$ the situation is
inverted and transport is governed by recombination instead of diffusion. Hence, charge
carriers never reach the counter electrode.

The model has two free parameters for fitting (D and k) since R_{DC} is fixed by the fre-
quency limit $\omega \to 0$. Considering the complexity of impedance spectra, this provides a
good basis for a statistically justified fitting of both parameters. Moreover, if the static
voltage is also varied further evidence an be provided. As discussed in Section 4.1, the
relation between τ_t and k strongly depends on the choice of organic material. For materi-
als with strong charge carrier recombination probability, as they are used e.g. in OLEDs,
the recombination rate is so large that the wave resistance behavior cannot be obtained.
Contrary to that, for materials, as they are used e.g. in organic solar cells, recombination
effects contribute only weakly to the impedance spectra.

To complete this paragraph on forward voltage impedance models it is worth to give an
equivalent circuit model for the impedance function discussed (Eq.76). An equivalent

circuit model represents a set of ideal electronic devices (mainly resistors and capacitors) arranged in a certain way to mimic the obtained impedance behavior. Such equivalent circuit models are often helpful to obtain an intuitive understanding of the relevant processes. It can easily be shown [67] that a circuit as illustrated in Figure 15(b), with an infinite number of repetitions, can be described mathematically by Eq.74 and 75 with the substitutions $r_m c_m = 1/D$ and $r_k c_m = 1/k$. This circuit nicely reflects the situation of charge carrier transport. Charge carriers move from one state to the next and thus diffusion constant and recombination rate obtain a microscopic meaning.

2.2.4 Organic Diodes for Ultra-High-Frequencies

A main goal of this thesis is to understand basic design rules for organic pin-diodes in order to push their performance to a level appropriate for electronic applications in the ultra-high-frequency (UHF) range. The focus of this paragraph is to deduce basic design rules for vertically stacked diodes in a coplanar contact geometry (see Figure 16(a)). In that context it turns out that one has to distinguish between scalable and not scalable diode parameters. Geometric parameters (layer thickness, active area A of the device) lead to scalable diode properties, while parameters as e.g. the recombination rate of minority charge carriers is an inherent quantity that cannot be modified by scaling. Hence, to push the scalable properties to the limit of inherent diode performance marks the main technological challenge.

Scalable diode properties: For a pin-diode, one can identify at least five scalable quantities which are

- active area of the vertically stacked device,

- thickness of the coplanar contact,

- interlayer thickness of the pin-diode,

- thickness of the doped layers,

- and the dopant concentration in the doped layers.

For further discussion the influence of one parameter is described while the others are kept constant. The main quantity in context of UHF applicability is the RC-time (τ_{RC}) of the diode. This is the product of the small signal forward resistance $\tilde{r}_{for}$ and the small signal reverse capacitance $\tilde{c}_{rev}$[11]. This quantity describes the ability of a diode to switch from a conductive to a capacitive state. If an alternating voltage signal is applied to the device with a certain frequency $f < 1/\tau_{RC}$, the device behaves as diode. If f exceeds

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[11]The reverse capacitance of a diode governs the on-switching behavior of a diode. The off-switching behavior is dominated by the minority charge carrier recombination time.
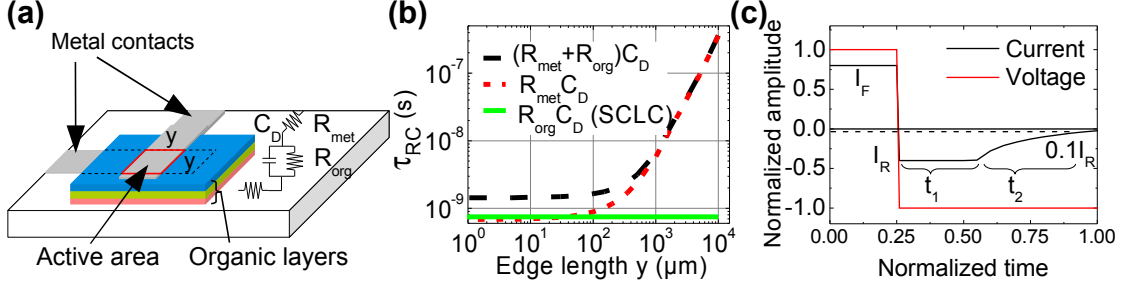
Figure 16: (a) Scheme of a vertically stacked organic pin-diode sandwiched between two metal contacts and a possible equivalent circuit model. The active area is indicated by red lines. (b) Estimation of τ_{RC} vs. edge length y considering the series resistance of the metal contacts R_{met}, the resistance of the organic layers R_{org}, and the depletion capacitance of the diode C_D. Typical values for R_{met}, R_{org}, and C_D are taken from experiments (compare Subsection 5.1). (c) Off switching behavior of a diode from a forward I_F to a reverse current I_R. The charge storage time t_1 and the current decay time t_2 ($I(t_2) = 0.1I_R$) are indicated.

$1/\tau_{RC}$ the device follows the characteristics of an ideal resistor.

For simplicity a quadratic shape (edge length y, active area $A = y^2$) of the vertically stacked diode is assumed. If the active area of the diode is modified, the resistance $\tilde{r}_{for}$ of the organic layers scales as $\sim \frac{1}{A}$ while the capacitance $\tilde{c}_{rev}$ scales as $\sim A$. Hence, τ_{RC} should be constant if the area is changed. However, the resistance of the coplanar contact R_{met} merely scales as $\sim \frac{1}{y} = \frac{1}{\sqrt{A}}$. Therefore, as shown in Figure 16(b), the RC-time is independent of the scaling parameter y if $\tilde{r}_{for} >> R_{met}$. Contrary, for $\tilde{r}_{for} << R_{met}$ the RC-time increases proportional to y. The transition point between both regimes is given by the specific resistances and it can be shifted to lower y values if the thickness of the coplanar contacts is increased (contact thickness does not influence the diode performance).

The second important scaling parameter is the interlayer thickness w_I. If the diode would behave as an Ohmic resistance in forward direction, τ_{RC} would be almost independent of w_I[12] since the forward resistance and the reverse capacitance scale as $\sim w_I$ and $\sim \frac{1}{w_I}$, respectively. However, organic pin-diodes typically follow a power-law dependence for w_I according to Eq.72. Therefore, $\tau_{RC} \sim w_I^{-2}$ can be deduced. This strong dependency gives rise to the fact that w_I is the main scaling parameter in order to push organic diodes to the UHF region. Nevertheless, as described later, there are inherent limits for reduction of w_I which are mainly the rectification properties and the importance of recombination effects.

The last two scaling parameters are the thickness of the doped layers and their dopant concentration. The role of thickness of the doped layers can be identified easily: the thickness of the doped layers has to be as small as possible to ensure a low resistance[13].

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[12] If $\tilde{c}_{rev}$ is predominantly governed by w_I which is fulfilled if w_I is larger than the thickness of the charge depletion zones in the doped layers.

[13] If the diode is operating in the SCLC regime, the doped layers contribute to the total resistance of the diode.

Typically, the resistance of the doped layers does not exceed the resistance of the inter-layer and therefore the doped layers do not contribute significantly to the RC-time.

The influence of the dopant concentration is more complex since the organic layers are typically unstructured and thus the overlap area is larger than defined by the contacts. The dopant concentration has to be chosen in a way that the resistance of the doped layers (+ injection resistance) is significantly smaller than the resistance of the interlayer. On the other hand, if the conductivity of the doped layers is too large an increase in ac-tive area A is likely due to the almost metallic behavior of the doped layers. This would cause a dramatic increase of reverse capacitance since more and more organic regions in the coplanar plane contribute to the device response.

This discussion will be continued quantitatively in Subsection 5.3.

Diode properties (not scalable): There are three diode properties that are not ac-cessible by scaling: the rectification ratio, the transit time through the interlayer [14], and the minority charge carrier recombination time in the doped layers.

The rectification ratio of the diode (defined as the ratio between forward and reverse cur-rent for a certain voltage) strongly depends on the interlayer thickness. While the forward current obeys typically the SCLC law concerning interlayer thickness, the dependency of the reverse current on the interlayer thickness is complex. The reverse current decreases strongly for thicker interlayers but the relation saturates if the electric field within the interlayer is too small for generation of charge carriers. Thus, an ideal interlayer thick-ness for the rectification ratio should be as small as possible to keep the forward current large, but on the other hand it should be close to this saturation of reverse current.

The transit time for charge carrier transport through the interlayer of the pin-diode is governed by the layer thickness w_I and the electric field distribution $\mathcal{E}(x)$. For drift transport (constant field, Ohmic behavior of the diodes), it is given by

$$\tau_{drift} = \frac{w_I}{\mu\mathcal{E}} = \frac{w_I^2}{\mu(V - V_{DC})},\tag{77}$$

and for diodes working in the SCLC regime it can be expressed according to Steudel et al. [68] as

$$\tau_{SCLC} = \frac{9\mu}{16\pi w_I^2 V_{DC}}\left((V^2 + V_{DC}^2)arcos(\frac{V_{DC} + V_F}{V}) - (3V_{DC} - V_F)\sqrt{V_A^2 - (V_{DC} + V_F)^2}\right),\tag{78}$$

where V_F marks the transition voltage at which the diode starts to show a SCLC-like behavior[15] and V_{DC} is the amplitude of the rectified voltage (compare Section 5.1). If e.g. a sinusoidal signal with a certain frequency f is applied to the device, it behaves as a diode only for voltages at which $1/\tau_{drift}$ (or $1/\tau_{SCLC}$) exceeds f. Otherwise, it

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[14]In principle, transit time and rectification ratio can be tuned by the interlayer thickness. However, here they are denoted as not scalable since these parameters are coupled in a complex way (see Section 5.3).

[15]In both cases a constant charge carrier mobility is assumed.

represents an ideal resistor in forward and reverse direction.

The transit time is the parameter that describes the ability of the diode to turn on, however, the turn-off behavior is governed by the minority charge carrier lifetime within the doped layers. If minority charge carriers reside in the doped layers they give rise to an additional capacitance that affects the switch off behavior of the diode.

During the turn off, two processes are taking place: diffusion and recombination of minority charge carriers. Both processes are required to set the minority charge carrier distribution back to its equilibrium value. To express this effect, again the continuity equation for minority charge carriers as (for holes in the n-type doped layer, recombination time τ_p)

$$\frac{\partial p_n(x,t)}{\partial t} = D_p \frac{\partial^2 p_n(x,t)}{\partial x^2} - \frac{p_n(x,t) - p_{n0}}{\tau_p} \tag{79}$$

can be used to find the characteristic time until the minority charge density reaches its equilibrium value p_{n0} at the interface between the doped layer and the interlayer. This time is denoted as charge storage time t_1 which is, according to [6] given by

$$erf\sqrt{\frac{t_1}{\tau_p}} = \frac{1}{1 + I_R/I_F}, \tag{80}$$

where I_F and I_R are the static forward and reverse current as defined in Figure 16(c). The reverse current is approximately constant at I_R during this time. After the time t_1, a rearrangement of minority charge carriers within the doped layers proceeds until the minority charge carrier distribution equals the equilibrium distribution in the whole depletion zones which is reached after a period t_2. This period is given by

$$erf\sqrt{\frac{t_2}{\tau_p}} + \frac{exp(-t_2/\tau_p)}{\sqrt{\pi t_2/\tau_p}} = 1 + 0.1\Big(\frac{I_R}{I_F}\Big). \tag{81}$$

and the reverse current is continuously decreasing during this time.

The UHF ability of a diode is predominantly governed by the higher one of both time constants $t_1 + t_2$ and τ_{drift}. In organic pin-diodes this limit is typically given by the transit time. However, one should keep in mind that both quantities are important. Furthermore, it should be mentioned that recombination within the intrinsic layer has been neglected within this model. This assumption is likely justified for high mobility materials and small forward voltage where the charge carrier concentration within the intrinsic layer is low.

2.3 Organic Field-Effect Transistors

Current analog and digital circuits rely on devices with well defined on- and off-states. In early years of electronics, vacuum tubes have been employed as first devices that can be switched between a defined on- and off-state. In such tubes, the current between two electrodes (anode and cathode) is controllable by an electric field of a grid-like patterned electrode, placed between anode and cathode. Vacuum tubes, however, are limited in their ability for integration, their switching speed, and their achievable gain (ratio of current flowing from anode to cathode and flowing via the third electrode). Furthermore, since such vacuum tube devices make use of the field emissions process of hot electrons, a substantial amount of their power consumption is going into heat generation.

The discovery of inorganic solid state electronic devices that show a conductive/resistive switching behavior such as diodes, bipolar transistors, and field-effect transistors (FET) triggered the rapid development of complex, and integrated circuits. Nowadays, the metal-oxide-semiconductor field-effect transistor (MOSFET), a special type of a FET, is dominating global semiconductor markets. MOSFETs benefit from their simplicity in architecture and their advantages in terms of scalability for planar device integration. Continuous improvements in material purification, patterning techniques, and circuit design allow a remarkable progress in device dimensions, number of FETs per wafer, and accordingly the price for an individual FET.

Due to material parameters and advantages in processing technology, organic field-effect transistors can never compete or surpass high performance inorganic FETs for high-power or ultra-high-frequency applications. However, organic semiconductors offer the possibility to build transparent and flexible electronics. Thus, the task for organic FETs is not to compete with crystalline inorganic semiconductors, but rather to employ their advantages for new fields of applications, where crystalline inorganic semiconductors are not an adequate choice.

2.3.1 Basics of Organic Thin-Film Transistor Operation

In the field of organic electronics, the most common type of field-effect transistors used nowadays is the thin film transistors architecture (TFT). Hence, physical models and the mathematical descriptions are derived for such kind of devices.

Even if different variants of TFT architectures exist, a TFT always consists of three main components: a semiconductor material, an insulating layer, and three electrodes denoted as source, drain and gate (see Figure 17). While source and drain are connected via the semiconductor, the gate electrode is separated from the other electrodes by the insulating layer. For organic thin-film transistors (OTFT) this insulating layer typically is either a metal-oxide (e.g. SiO_2, Al_2O_3, HfO_2, ZrO_2) or a polymer (e.g. $PMMA$,
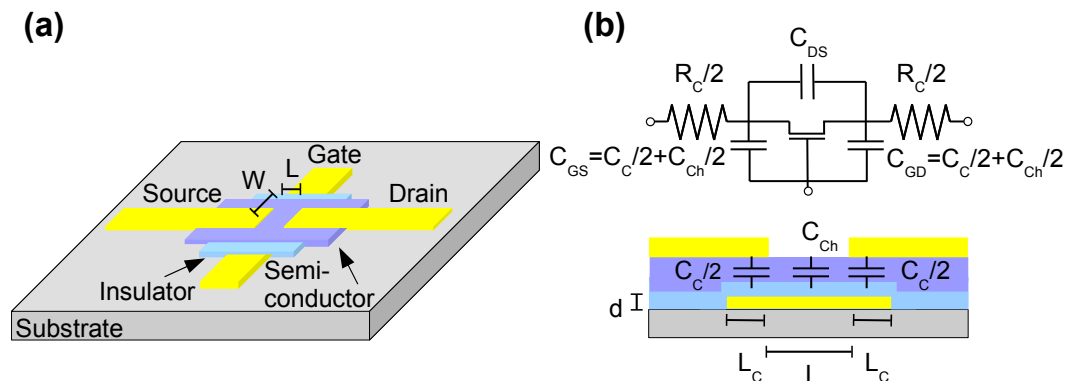
Figure 17: **(a)** Scheme of an organic thin-film transistor in bottom gate and top source-drain geometry. The channel length L and the channel width W are indicated. **(b)** Vertical profile of an OTFT and a corresponding equivalent circuit model. R_C denotes the injection/ejection resistance and C_C denotes the overlap capacitance caused by the overlap length L_C. C_{DS} represents the drain-source capacitance. The ideal OTFT in the center of the equivalent circuit is described by the set of Eq.84-85 which includes the channel capacitance C_{Ch} governed by the insulator thickness d.

PVA [16]). Also, thin charge depletion zones, as they e.g. appear at metal-semiconductor interfaces can be used as an insulating layer. This concept is successfully engaged in metal-semiconductor field effect transistors (MESFET) [69].

Important quantities that are used to adjust the OTFT performance are its spatial dimensions. The distance between source and drain electrode, denoted as channel length L, the width of this channel W, and the thickness of the insulating layer d (see Figure 17) are of particular importance. These parameters determine the capacitance as well as the resistance of an OTFT as shown in Figure 17(b).

Typically for OTFTs undoped semiconductors are used[17] which exhibits the most substantial difference between inorganic MOSFETs and OTFTs. Consequently, there are no free charge carriers within the semiconductor which gives rise to the fact that OTFTs are typically limited in their performance by the contacts [70]. This aspect has to be considered for a theoretical description of OTFT performance. Moreover, caused by the importance of charge carrier injection for OTFTs, strong variations in electrical behavior for OTFTs in different geometries have been observed. Especially in a bottom gate and bottom source-drain configuration, significant differences in OTFT performance depending on the contact preparation have been shown [70–72].

Nevertheless basic principles of OTFT operation can be understood relying on models developed for MOSFETs. In this picture, the vertical gate-insulator-semiconductor structure can be considered as a parallel plate capacitor where the insulator-semiconductor

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[16]PVA - polyvinyl alcohol, PMMA - polymethylmethacrylat

[17]Since the doping technology has been improved and developed within the last years, also doped semiconductors can be employed for OTFTs. However, in the literature undoped OTFTs are reported predominantly.
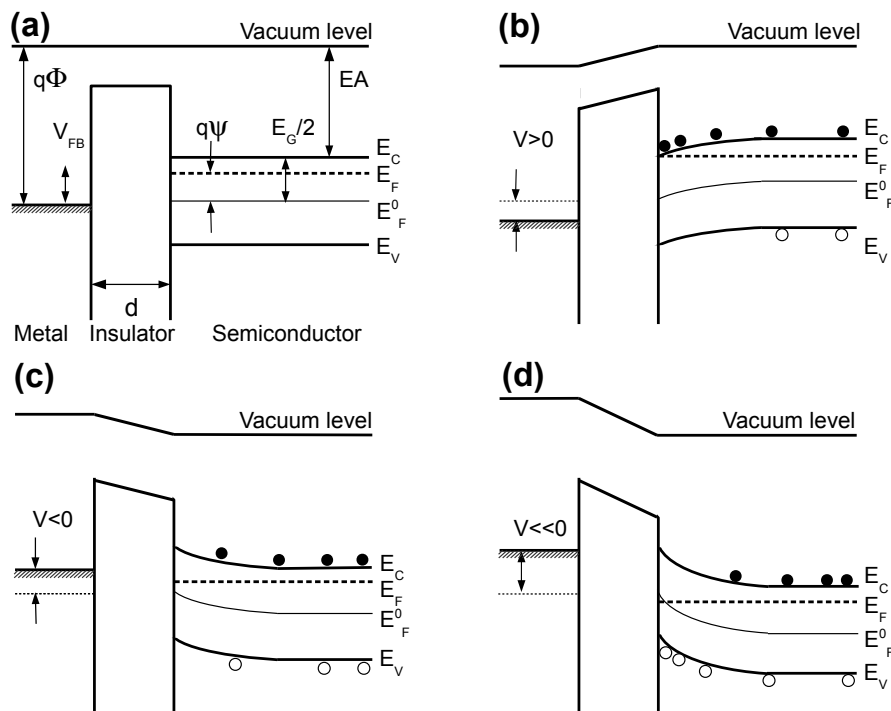
Figure 18: Energy-level diagrams across the insulator-semiconductor interface under different external bias conditions V for a n-type semiconductor. Valence E_V and conductance E_C states of the semiconductor are represented by one dominating level with an energy gap E_G in between. **(a)** Equilibrium condition ($V = 0$), **(b)** accumulation of electrons ($V > 0$, accumulation regime), **(c)** depletion of electrons ($V < 0$, depletion regime), and **(d)** accumulation of holes ($V << 0$, inversion regime). The electron affinity of the semiconductor is denoted as EA, the work function of the metal as $q\Phi$, the quasi-Fermi level as E_F, and the Fermi level as E_F^0.

interface can be populated or depopulated by different types of charge carriers which is controlled by the applied electric gate field. Three different regimes can be identified (see Figure 18, exemplary shown for an n-type doped semiconductor, p-type analog):

- the accumulation regime (Figure 18(b)) - majority charge carriers are accumulated at the insulator-semiconductor interface,

- the depletion regime (Figure 18(c)) - majority charge carriers are repelled from the interface,

- and the inversion regime (Figure 18(d)) - minority charge carriers are accumulated at the interface.

The accumulation of either majority or minority charge carriers in the so-called channel of the TFT locally changes the conductivity of the semiconductor and consequently the current flow between source and drain electrode. Thus, the operation of an OTFT is based on the control of the channel conductance by the applied electric gate field. The

spatial extension of the conductive channel depends on the applied electric gate field and on the insulator capacitance and it is typically in the range of $0.1 - 1nm$ [73].

Depending on the kind of semiconductor and the applied gate field, the charge carriers in the channel can either be electrons (n-channel) or holes (p-channel). In context of organic semiconductors, where typically undoped semiconductors are used, the choice of n- or p-channel conduction is predominantly governed by the injection/ejection behavior of charge carriers at source and drain contacts. Thus, e.g. the appearance of Schottky barriers can greatly suppress injection of one charge carrier species while the other one can sufficiently be injected. In consequence, this means that OTFT comprising undoped organic semiconductors are exclusively working in the accumulation regime. Pentacene e.g. shows hole transport if noble metals such as gold [74] and electron transport if low work function metals such as calcium [75] are used as source and drain contacts.

Operation within gradual channel approximation: In a first approximation, the operation of OTFTs can be mathematically described within the gradual channel approximation. This basically contains the following four assumptions:

- the vertical electric field between source and gate is significantly larger than the horizontal electric field present between source and drain,

- the geometrical distance between source and drain contacts is much smaller than their geometrical extensions $(L << W)$,

- the resistance of the conductive channel is much larger than the charge carrier injection/ejection resistance,

- and the charge carrier mobility μ is constant. No dependencies on charge carrier density and electric field are considered.

Moreover, the small signal validity of Ohm's law needs to be assumed which can be expressed by [76]

$$\tilde{i}_D = \tilde{g}_m V_{GS} \tag{82}$$

$$\tilde{g}_m = \frac{\tilde{i}_D}{\tilde{v}_{GS}} = \frac{\partial I_D}{\partial V_{GS}}\bigg|_{V_{DS}=const}, \tag{83}$$

where $\tilde{g}_m$ is the channel transconductance, V_{DS} the drain-source voltage, and $\tilde{i}_D$ and $\tilde{v}_{GS}$ are the small signal quantities of the drain current I_D and the gate-source voltage V_{GS}, respectively. Relying on the assumptions of the gradual channel approximation, the current flow from source to drain contact I_D for a given drain-source and gate-source
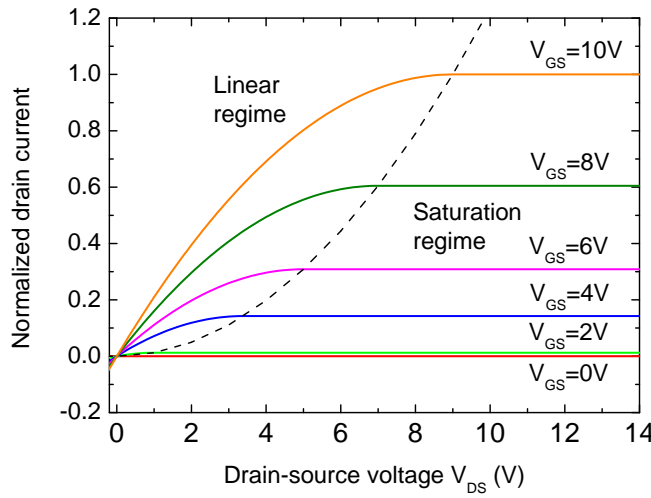
Figure 19: Current-voltages curves of an ideal TFT according to Eq.84-85 with a threshold voltage of $1V$. The dashed line separates the linear from the saturation region and it is given by $V_{DS} = V_{GS} - V_T$.

voltage can be derived as (see e.g. [6])

$$I_D = \mu C_i \frac{W}{L} \left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right) \tag{84}$$

$$\text{for } |V_{GS} - V_T| > |V_{DS}| \text{ (linear regime)}$$

$$I_D = \mu C_i \frac{W}{2L} (V_{GS} - V_T)^2 \tag{85}$$

$$\text{for } |V_{DS}| > |V_{GS} - V_T| > 0 \text{ (saturation regime)},$$

where $C_i = \frac{C_{Ch}}{LW} = \frac{\epsilon_0 \epsilon}{d}$ is the specific insulator capacitance per unit area and V_T is the threshold voltage. Current-voltage characteristics of an ideal OTFT according to Eq.84-85 are shown in Figure 19. For $|V_{GS} - V_T| > |V_{DS}|$ the OTFT is working in the linear regime and the drain current is increasing with increasing V_{DS} since the electric gate field is strong enough to create a conductive channel along the entire geometrical channel length. For $|V_{DS}| > |V_{GS} - V_T| > 0$, however, there is no accumulation of charge carriers close to the drain electrode and accordingly the channel is pinched off which leads to a saturation of current.

The threshold voltage V_T is actually defined for MOSFETs and it denotes the minimum gate-source voltage required to obtain the strong inversion within the channel [6]. OTFTs, however, are not operating in the inversion regime and thus the threshold voltage cannot be defined as for MOSFETs. Nevertheless, the threshold voltage is used for OTFTs to mark the transition between the two different conductance states of the channel [76]. Theoretical predictions of the threshold voltage are challenging since they have to take injection barriers, surface states, and charge carrier trap states into account. Thus, even if some theoretical descriptions have been reported [76, 77], no closed expression has been found up to now. Furthermore, the experimental control of the threshold voltage is

currently a big challenge which restricts the commercial applicability of OTFTs.
Organic thin-film transistors are often employed for semiconductor material characterization since the charge carrier mobility is easily accessible by rearranging Eq.84-85 as

$$\mu_{lin} = \frac{L}{C_i W V_{DS}} \frac{\partial I_D}{\partial V_{GS}} \qquad \text{for the linear regime, and} \qquad (86)$$

$$\mu_{sat} = \frac{2L}{C_i W} \Big(\frac{\partial \sqrt{I_D}}{\partial V_{GS}} \Big)^2 \qquad \text{for the saturation regime.} \qquad (87)$$

According to the assumption of the gradual channel approximation the charge carrier mobility is constant. However, for charge carrier transport in organic semiconductors a dependency of mobility on at least the applied electric field as well as on the charge carrier density is expected. Thus, the electric field dependence of charge carrier mobility as calculated by Eq.86-87 is attributed to such electric field and charge carrier density dependent transport phenomena [20, 78]. Also the influence of structural order in polycrystalline materials on the charge carrier mobility in OTFTs has been discussed [26, 79] including percolation path theories. However, owing to the strong influence of charge carrier injection mechanisms on OTFT characteristics, the charge carrier mobility analysis is partially ambiguous since it does not take influences of contact resistance, threshold voltage, and layer thickness into account. Several correction approaches have been reported [80, 81]. Unfortunately, since especially the threshold voltage is not precisely defined for OTFTs, several methods to determine threshold voltage [82] and contact resistance [83, 84] have been suggested. Accordingly, the evaluation of charge carrier mobility in OTFT is partially inconsistent and depends on the OTFT geometry and the special kind of gate insulator. Nevertheless, reliable charge carrier mobilities can be extracted from OTFT measurements if influences of threshold voltage and contact resistance are negligible. This can be achieved for long channel length devices where contact resistances are small in comparison to the channel resistance[18]. Furthermore, gate insulators possessing a low density of charged interface states are required. This leads to a reduced threshold voltage[19].
The quality of the insulator-semiconductor interface and the defect density of the gate insulator can be characterized by the subthreshold voltage behavior of the transistor. Below the threshold voltage, an exponential rise of the drain current with the gate-source voltage is typically obtained. The slope of this curve is denoted as subthreshold swing S and it is given by [86]

$$S = \frac{\partial V_{GS}}{\partial log_{10} I_D} = \frac{kT}{q} ln(10) \Big(1 + \frac{q N_{IT}}{C_i} \Big), \qquad (88)$$

where N_{IT} is the charge carrier trap density at the semiconductor-insulator interface. The smaller N_{IT}, the smaller is the subthreshold swing and typically also the threshold voltage. Typical values of S for OTFTs are varying from $> 1V/dec$ to $80mV/dec$ and

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[18]In context of OTFTs a channel length of $L > 100\mu m$ can be considered as long.
[19]The defect density of gate insulators can be reduced by special self-assembled monolayers [85].

strongly depend on the insulator as well as the surface treatment.

Contact limited behavior of OTFTs: Because of improvements in OTFT fabrication techniques leading to a shorter channel length and because of the emergence of novel organic semiconductors with higher charge carrier mobility, the specific channel resistance r_{ch} has been reduced continuously. Accordingly, the role of contacts for charge carrier injection/extraction plays an important role for modern OTFTs.

Contact resistances can actually arise from two effects: firstly from the appearance of injection barriers at source and drain contacts and secondly from charge carrier transport through the semiconductor to the channel region. The latter one is characteristic for OTFTs in top source-drain geometry while it is typically not considered for bottom source-drain OTFTs. Since top source-drain OTFTs are used within this work, contact resistance effects will be described for this device geometry.

The specific contact resistance r_C ($[r_C] = \Omega cm$) in such OTFTs can be investigated by different methods such as the transmission line method (TLM), four-point-probe measurements, and equivalent circuit models. Advantages and disadvantages of these techniques have been discussed by Richards et al. [87]. The transmission line method is most commonly used since the contact resistance can easily be evaluated by a variation of the geometrical channel length [83]. The total resistance R_{tot} of an OTFT is given by the sum of the channel resistance R_{Ch} and the contact resistance $R_C = \frac{r_C}{W}$. Thus, for small source-drain voltages (linear IV curve of the OTFT) this can be expressed according to Eq.84 by

$$R_{tot} = \frac{L}{W\mu C_i}\frac{1}{V_{GS} - V_T} + \frac{r_C}{W}. \tag{89}$$

If $R_C < R_{Ch}$ is fulfilled the contact resistance can directly be determined as shown in Figure 20(a)[20]. Typically, for an increased gate-source voltage a super-linear lowering of contact resistance is obtained. This effect can either be related to a non-ohmic injection or it can be explained within the crowded current model as it is discussed at the end of this paragraph.

However, even if the TLM provides an easy access to the contact resistance, it has considerable drawbacks. In particular, the contact resistance has to follow Ohm's law, the individual contributions of source and drain to the contact resistance cannot be separated, and for strong injection limitations TLM fails. The influences of a weak contact limitation ($R_C < R_{Ch}$) are exemplarily shown in Figure 20(b). For a weak contact limitation, the slope of the IV curve in the linear region of OTFT operation is reduced owing to the superposition of channel and contact resistance. As long as $R_{Ch} > r_C/W$ is valid a saturation current can be obtained. Its value is also reduced owing to the influence of the contact resistance. The reduced saturation current mimics a reduced charge carrier mobility (see Eq.87). This effect is more pronounced for materials with a high charge carrier mobility since their specific channel resistance $r_{Ch} = \frac{R_{Ch}}{L}$ is smaller (than in case of low charge carrier mobility materials). The reduced charge

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[20]Typical values of specific contact resistance vary from $0.3k\Omega cm$ to $100k\Omega cm$.
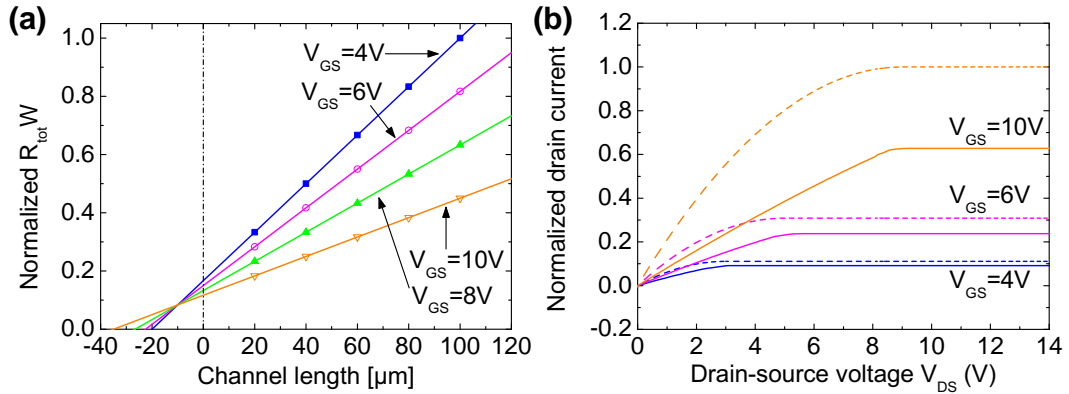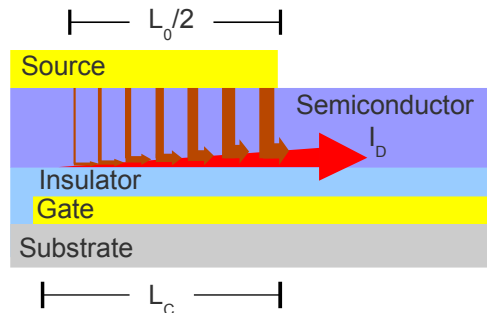
Figure 20: (a) Evaluation of contact resistance by the transmission line method for different gate-source voltages. (b) Current-voltages curves of an OTFT as shown in Figure 19 with a performance restricted by a weak contact resistance. The dashed lines visualize the behavior of the corresponding ideal OTFT.

carrier mobility, however, can be corrected since the contact resistance can be determined correctly from the linear regime of the OTFT.

In contrast, for a strong non-linear contact limitation, the IV curve of an OTFT cannot be described adequately by Eq.84-85 and accordingly the charge carrier mobility cannot be determined. The IV curve in case of strong contact limitations typically neither exhibits a distinct linear regime nor a saturation regime.

Several approaches have been reported in the literature in order to identify the mechanism of charge carrier injection, explaining contact resistance [70, 81, 87–90]. Within these models charge carrier injection has been described predominantly by an electric field assisted tunneling from a metal electrode through a Schottky barrier into a distribution of HOMO/LUMO states of the organic semiconductor [89, 91, 92]. The realization of different Schottky barrier heights as well as the typically observed low thermal activation energies of the contact resistance provides experimental evidence for these models [70, 89, 91, 92][21].

However, the strong gate-source dependence typically observed in top source/drain OTFTs cannot conclusively be explained by a contact resistance which arises only from the appearance of Schottky barriers. A second contribution to the contact resistance has to be considered. This additional contact resistance contribution, which is only present in top contact OTFT, is related to the transport of charge carriers from the electrode through

Figure 21: Illustration of the crowded current model including the transfer length L_0.

the semiconductor to the channel region. Thus, a certain area underneath the contacts is required to supply enough charge carriers for the channel (see Figure 21). This behavior

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[21]As a consequence of these models the contact resistances arising at source and drain electrode are substantially different. By TLM, however, these effects cannot be studied. Accordingly, as shown in Figure 17, in equivalent circuit models the total contact resistance is equally distributed between source and drain contact.

is considered within the crowded current model [87, 88]. In this picture, the injection
area is given by the product of channel width W and transfer length L_0[22]. If the specific
contact resistance per unit area underneath the contacts is smaller than the specific chan-
nel resistance, the injection area is small. Contrary, an area of $A = WL_0$ is required for
injection of charge carriers if the specific channel resistance is smaller than the contact
resistance. This has been described mathematically by Chiang et al. [93] for amorphous
silicon TFTs[23] and it has been adopted to organic semiconductors by Richards et al. [87].
The transfer length is given in a transcendent expression by

$$L_0 = \frac{R_C W}{r_{Ch} coth(L_C/L_0)} \approx \frac{R_C W}{r_{Ch}} \text{ for } L_C >> L_0, \tag{90}$$

where L_C is the geometrical gate-source overlap.

The transfer length has been measured experimentally and depending on semiconductor
material and OTFT geometry, values up to $40\mu m$ have been obtained [94]. Wang et al.
[94] discussed the influence of the transfer length on OTFT IV curves. Assuming a trap
free space charge limited current underneath the contacts, they obtained an additional
resistance by the transfer length that shows the same behavior, as the resistance of the
channel in the linear region. Accordingly, a transfer length limited OTFT performs as
an ideal OTFT where the active channel length is given by the sum of the geometrical
channel length and the transfer length. Relying on this picture, the TLM can be used to
determine L_0 (see Figure 20(a), L_0 can be determined for $R_{tot}W = 0\Omega cm$). If a structured
gate electrode with a source-gate overlap L_C is considered, the injection length cannot
exceed L_C and hence the current in the transistor is limited by the injection of charge
carriers.

A remarkable reduction of transfer length has been reported by Ante et al. [33]. They
used the concept of molecular doping to reduce contact resistances and subsequently also
the transfer length.

Within the crowded current model also the gate-source voltage dependence of the contact
resistance R_C can consistently be described. Thus, the lowering of the channel resistance
with increasing gate-source voltage leads to an enlarged injection area underneath and
therefore to a reduced contact resistance $R_C W$. For a certain specific contact resistance
$(r_C^A, [r_C^A] = \Omega cm^2)$ per injection area (WL_C) the gate-source voltage dependence of the
transfer length is derived as

$$L_0 = \sqrt{r_C^A C_i \mu (V_{GS} - V_T)}, \tag{91}$$

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[22]Also denoted as injection length.

[23]Transfer length related effects are not obtained for crystalline silicon based MOSFETs working in the
inversion regime. This is related to high charge carrier mobility in silicon and the utilization of doped
semiconductor layers.

and the gate-source voltage dependence on the specific contact resistance ($[R_C W] = \Omega cm$) per unit channel width as

$$R_C W = \sqrt{\frac{r_C^A}{C_i \mu (V_{GS} - V_T)}}.$$ (92)

Thus, with increasing channel conductance the transfer length is increasing, while the contact resistance per unit channel width is decreasing.

As a general remark on contact resistance, threshold voltage, and charge carrier mobility estimation from IV curves of OTFTs, it should be emphasized that from a mathematical point of view the system is under-determined. In detail, three parameters are to be determined ($\mu(V_{GS})$, V_T, $R_C(V_{GS})$), whereas only two quantities are directly accessible by measurements (V_{DS}, $I_D(V_{DS}, V_{GS})$). Hence, for a meaningful and independent analysis of charge carrier mobility and contact resistance, detailed models that account for the field dependence of these quantities have to be employed. Apart from this fact, charge carrier mobility and contact resistance can be determined in some limiting cases of OTFT operation. For instance, for long channel devices contact resistance effects can be neglected and charge carrier mobility and threshold voltage can be investigated. Contact resistance estimation by TLM is possible in case of long channel devices, however, owing to $R_{Ch} >> R_C$, the TLM is less sensitive to the contact resistance for long channel devices. Contrary, intermediate channel lengths ($30 - 100 \mu m$) are more suitable for TLM analysis, while due to contact resistance effects charge carrier mobility might be affected.

Short channel behavior of OTFTs: Scaling down of TFT dimensions is desirable since a reduction of channel length by a factor κ gives rise to an increase in channel transconductance by a factor κ and moreover it leads to an increase in cut-off frequency by a factor κ^2. However, the constraint of a one-dimensional electric field in the channel is violated if the magnitude of the electric field between source and drain becomes comparable to the applied field between source and gate. Therefore, if only the channel length is scaled down, strong deviations in TFT performance according to Eq.84-85 are observed. These deviations are denoted as short channel effects[24]. Four different short channel effects have been identified and described for OTFTs [95–98][25]:

- the channel length modulation leading to a loss of the saturation regime,

- the threshold voltage roll-off,

- the subthreshold current dependence on V_{DS}

- and the appearance of space charge limited currents between source and drain.

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[24]Elimination of short channel effects can be accomplished if all OTFT dimensions (L, W, d) are scaled by a factor κ in order to keep the electric fields constant (constant-field scaling) [6].

[25]Short channel effects in OTFTs are predominatly reported for bottom source-drain devices since the transfer length mechanism suppresses such effects for top source-drain OTFTs [99].

The channel length modulation is the most prominent short channel effect which arises from the fact that the dimension of the charge carrier depletion zone (the pinched off part of the channel) close to the drain contact becomes comparable to the channel length. For $|V_{DS}| > |V_{GS} - V_T| > 0$ (saturation regime) the size of the depletion zone increases for increasing V_{DS} which leads to a reduction of the active channel length. According to Eq.85 the lowering of active channel length gives rise to an increase of the drain current I_D. Thus the saturation behavior disappears and I_D is described by

$$I_D = I_D^{Saturation}(1 + \lambda V_{DS}), \tag{93}$$

where λ is the channel length modulation parameter which scales as $\lambda \sim L^{-1}$.
The threshold voltage roll-off and the appearance of a drain-source voltage dependent subthreshold current are caused by the electric field assisted injection of charge carriers into the semiconductor. Thus, these charge carriers govern the subthreshold current. Furthermore, they induce a threshold voltage shift since an increased electric gate field is required to deplete the channel. The device operation is changing from a normally-on to a normally-off state. The threshold voltage shifts according to $\Delta V_T \sim \frac{1}{L}$ and moreover the threshold voltage becomes drain-source voltage dependent. If the channel length is even further reduced, direct current flowing from source to drain through the semiconductor bulk dominates the OTFT performance. The on/off switching ability of the OTFT is strongly reduced and OTFT operation is typically described by space charge limited currents.
In order to avoid short channel effects the ratio between the gate-source and drain-source field can be taken as a figure of merit. This ratio should be larger than ten to guarantee long channel behavior [6, 97].

Frequency behavior of OTFTs: Thin-film transistors are favorable as fast switches due to their low power consumption required for switching. Owing to charging and discharging of the gate capacitor C_G, the only current which is flowing during a switch is given by the displacement current $\tilde{i}_G$ of the gate capacitance. Accordingly, the transistor can be used as a current switch up to a frequency f_T (cut-off frequency) where this displacement current equals the drain current $\tilde{i}_D$. For a mathematical evaluation of this cut-off frequency, small signal quantities have to be considered (small signal quantifies are labeled here by a tilde). However, according to Eq.84 OTFTs can be treated as linear devices and subsequently the equations can be generalized to large signal quantities. Thus, the cut-off frequency can be derived from

$$\frac{|\tilde{i}_D|}{|\tilde{i}_G|} = \frac{\tilde{g}_m \tilde{v}_{GS}}{2\pi f C_G \tilde{v}_{GS}} = \frac{\tilde{g}_m}{2\pi f C_G} \tag{94}$$

as

$$f_T = f\Big(\frac{|\tilde{i}_D|}{|\tilde{i}_G|} = 1\Big) = \frac{\tilde{g}_m}{2\pi C_G}. \tag{95}$$

If contact resistance effects can be completely disregarded, the OTFT cut-off frequency for the linear regime can be expressed as

$$f_T = \frac{1}{2\pi} \frac{\mu V_{DS}}{L^2} \frac{C_{Ch}}{C_G}. \tag{96}$$

If such ideal OTFT is scaled down with regard to constant electric fields, the cut-off frequency is thus strongly increasing for a reduced feature size and frequency limits of $> 10MHz$ are feasible [74] with state-of-the-art organic semiconductor materials. For non-ideal OTFTs, however, some inherent parameters such as contact resistance and transfer length are not accessible by scaling. Therefore, deviations from Eq.96 are expected. Firstly, the influence of contact resistance on f_T is discussed. Secondly, effects related to overlap capacitances are taken into account.

A resistance in series to an ideal OTFT reduces the transconductance of the series connection. Substituting Eq.89 and Eq.84 in order to derive the transconductance including contact resistances, one can obtain the cut-off frequency as

$$f_T = \frac{1}{2\pi} \frac{\mu V_{DS}}{(L + C_i r_C \mu (V_{GS} - V_T))^2} \frac{C_{Ch}}{C_G}. \tag{97}$$

Apparently, the cut-off frequency is reduced in comparison to Eq.96. Moreover, if the contact resistance is equal to the channel resistance the cut-off frequency starts to saturate if the channel length is scaled down. According to Eq.92 the contact resistance contribution can be expressed by the transfer length and therefore Eq.96 can be written as

$$f_T = \frac{1}{2\pi} \frac{\mu V_{DS}}{(L + L_0)^2} \frac{C_{Ch}}{C_G}. \tag{98}$$

Finally, effects of gate-source and gate-drain overlap capacitances have to be considered (equivalent circuit model shown in Figure 17). In this case $C_{Ch} \neq C_i W L$, but rather $C_{Ch} = C_i W L + 2 C_i W L_C$, where L_C is the overlap length as denoted in Figure 17. Thus, Eq.96 has to be rewritten as

$$f_T = \frac{1}{2\pi} \frac{\mu V_{DS}}{(L + 2L_C)^2}. \tag{99}$$

Since on the one hand the overlap effect is a capacitive contribution to the gate displacement current and on the other hand the contact resistance is a resistive contribution to the drain current, both effects are independent. Thus, Eq.96 can be factorized as [100]

$$f_T = \frac{1}{2\pi} \frac{\mu V_{DS}}{L^2} \frac{L^2}{(L + 2L_C)^2} \frac{L}{L + L_0}, \tag{100}$$

where the first factor represents the behavior of an ideal OTFT, the second factor is related to the capacitive overlap, and the third factor takes transfer length effects into account. Surprisingly, there is a certain channel length where a maximum in the cut-off frequency function appears. The value of this ideal channel length is governed by the ratio between L_O and L_C. If the channel length is reduced beyond that optimum value, the cut-off frequency starts to drop. The decay of the cut-off frequency originates from

the fact that the transconductance in Eq.95 is faster approaching a saturation than the displacement current in the denominator of Eq.95.

In summary, the cut-off frequency in OTFTs does not scale with the channel length as predicted for inorganic TFTs working in the inversion region. This is basically related to the contact resistance appearing in OTFTs leading to an enlarged active channel length. Accordingly, besides a reduction in channel length and overlap capacitances, it is of particular importance to reduce contact resistances in order to raise the cut-off frequency of OTFTs.

In the last years several new records for the cut-off frequency in OTFTs have been reported [74, 101]. Owing to a continuous reduction in contact resistance, cut-off frequencies of up to $20MHz$ have been achieved. In these devices, the channel length and the geometrical overlap of gate-source and gate-drain respectively are the limiting factors (both are in the range of $2\mu m$). Therefore, the improved injection behavior in OTFTs requires appropriate structuring techniques or new device concepts for OTFTs.

2.3.2 Thin-Film Transistor Based Inverters and Ring Oscillators

Owing to their versatility, transistors are indispensable devices in modern analog and digital circuits. In particular, transistors are predominantly used in integrated circuits which are the backbone of every microprocessor. Two basic integrated circuits in digital logic are inverters and ring oscillators. In either case one profits from the high on-state transconductance, the high off-state resistance, the high cut-off frequency, and the low static power consumption of TFTs. The realization, investigation, and optimization of inverters and ring oscillators is of particular importance for organic semiconductors because of three main reasons. Firstly, the fabrication and adjustment of complementary organic inverters[26] exhibits a technical challenge since the p-type and n-type channel TFTs must be manufactured in a small spatial vicinity to each other. Secondly, the knowledge of differences in n-channel and p-channel OTFT behavior and their influence on the inverter characteristic is required to design large array electronic circuits including thousands and millions of transistors. Thirdly, the ring oscillator provides an access to estimate the cut-off frequency of an OTFT.

In this section, the basics of inverter and ring oscillator operation are explained.

The task of an inverter is to invert voltage levels. In particular, the output voltage V_{out} of an inverter has to be "low" if the input voltage V_{in} is "high" and vice versa. To illustrate this, Figure 22 displays the circuits of an unipolar and a bipolar (complementary) inverter as well as their output vs. input voltage characteristics. For a complementary inverter the working principle can be understood as follows. If the input voltage is "low" ($0V$) the p-channel transistor is working in the linear regime since the supply voltage V_{DD} effects that a voltage of $-V_{DD}$ is applied between gate and source of the p-channel transistor. The n-channel transistor, however, is in the off-state since no gate-source

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[26]Complementary inverters contain of a p-channel and a n-channel OTFT
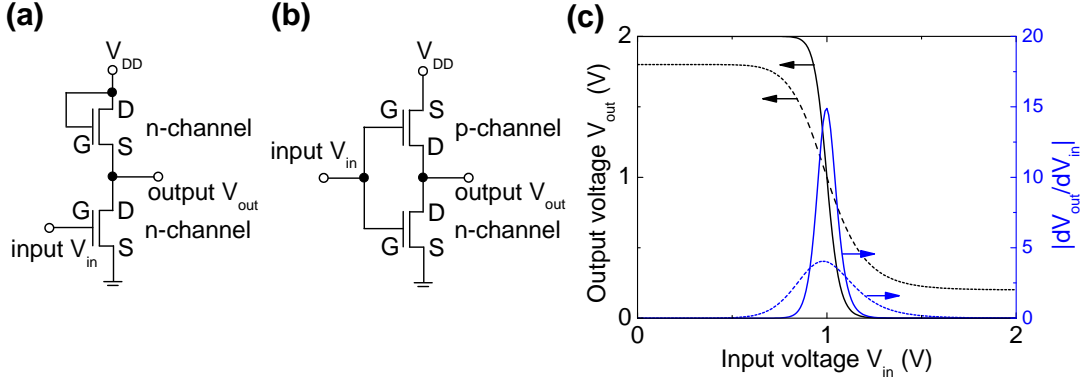
Figure 22: **(a)** Scheme of an unipolar (n-channel) inverter. **(b)** Scheme of a complementary inverter. **(c)** output vs. input voltage curve (black) and $|dV_{out}/dV_{in}|$ (blue) of a complementary inverter (closed lines) and an unipolar (n-channel) inverter (dashed lines).

voltage is applied to that transistor. Accordingly, the output is almost at the same potential as V_{DD} and thus the output is "high". The opposite behavior can be obtained if the input voltage is "high". In that case the p-channel transistor is in the off-state, while the n-channel transistor is working in the linear regime. Therefore, the output is almost at the same potential as the ground ("low"). During a switching circle only the gate displacement current and the displacement current due to the channel capacitance are flowing, which guarantees a very low dynamic power consumption. Ideally, there is no static power consumption since one transistor is always in the off-state, while the drain-source voltage of the other transistor is almost at $0V$.

The switching behavior is displayed in Figure 22(c). To characterize the quality of switching $|dV_{out}/dV_{in}|$ is used as a figure of merit and its maximum value at the point V_M is denoted as gain of the inverter. The gain is of particular importance for integrated circuits since it provides a direct measure of the number of inverters that can be connected in series without losing the logic voltage level by statistical fluctuations of transistor parameters such as threshold voltage (noise margin effect). The point V_M (both transistors have the same conductance at this point) can be derived as [102]

$$V_M = \frac{V_{th}^n + \sqrt{\frac{\mu^p}{\mu^n}\frac{C_i^p}{C_i^n}\frac{W^p}{L^p}\frac{L^n}{W^n}}(V_{DD} + V_{th}^p)}{1 + \sqrt{\frac{\mu^p}{\mu^n}\frac{C_i^p}{C_i^n}\frac{W^p}{L^p}\frac{L^n}{W^n}}}, \tag{101}$$

where the indexes p and n stand for the p-channel and n-channel transistor, respectively. As indicated by Eq.101, the point V_M can be adjusted by technical parameters of the OTFT such as channel length, channel width, and threshold voltage. In contrast to that, the gain is weakly influenced by parameters such as the threshold voltage. It is purely determined by the ideality of both transistors according to Eq.84-85.

For an unipolar inverter, as shown in Figure 22(a), the upper transistor is always working in the saturation regime where it acts as a fixed resistance. The switching is caused by the
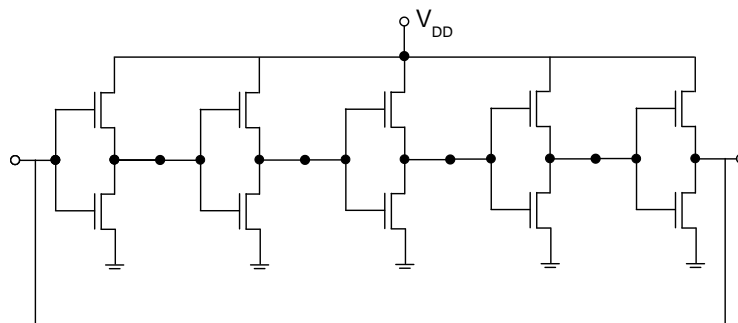
Figure 23: Scheme of a 5-stage ring oscillator with complementary inverters.

lower transistor. This configuration has two main drawbacks. Firstly, the fixed resistance of the upper transistor leads to the fact that output voltage never reaches $0V$ or V_{DD}. Secondly, caused by the first aspect, there is always a potential difference between the output and the supply node and therefore a static current can flow.

If an odd number of inverters is connected in series and the output of the last inverter is coupled back to the input of the first one, a ring oscillator as shown in Figure 23 is realized. By the odd number of inverters and the feedback, it is guaranteed that the input of the first inverter is continuously switched between "high" and "low". Thus, starting with a random input voltage, the first inverter provides the corresponding output signal within a characteristic time which is denoted as stage delay time[27] T_D. This procedure is repeated until the signal reaches the output of the last inverter which occurs after a period of $T_D N_{RO}$, where N_{RO} is the number of inverter stages in the oscillator. At this time the output of the last inverter has the opposite level in comparison to the input of the first inverter. This is equivalent to a phase shift of π. Accordingly, the signal has to pass the oscillator twice until the output of the last inverter has a phase shift of 2π to the initial input signal of the first inverter. Therefore, the ring oscillator frequency f is given by

$$f = \frac{1}{T_D \cdot 2N_{RO}}. \tag{102}$$

This frequency is an inherent parameter of the system. More complex signals can arise if the individual stage delay times are different. In this case aperiodic oscillations can appear since the resonance condition can be fulfilled for different frequency modes.

The stage delay time can be influenced in three different ways in order to adjust the oscillation frequency. The first is to change the channel length of the OTFTs. Thereby, the capacitance and the transconductance of the OTFT are changed which leads to a different cut-off frequency and subsequently to a different stage delay time. The second way to modify T_D is to add a capacitive load to every inverter. This gives rise to the fact that the stage delay time is not governed by the cut-off frequency of the OTFTs,

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[27] The stage delay time is composed by the capacitive load of the inverter and additional transit time effect. If transit time effects are negligible the stage delay time is inverse proportional to the cut-off frequency of the OTFTs employed in the inverter.

but rather by the characteristic charging and discharging time of the employed capacitor. The third method to adjust the stage delay time is given by the used supply voltage V_{DD}. As it can be concluded from Eq.96, a change in V_{DD} causes a change in cut-off frequency and therefore also in stage delay time.

2.3.3 Vertical Organic Thin-Film Transistors

State-of-the-art p-channel OTFTs have been used in certain applications such as small microcontrollers [103], small and medium size displays [104, 105], and radio-frequency identification (RFID) tags [106]. However, the utilization of OTFTs in either large scale electric circuits or applications that require a high switching frequency is still limited. Presumably, this is related to the following three aspects: (1) air-stable n-channel OTFTs still show low performance in comparison to p-channel OTFTs which is related the low charge carrier mobility in such materials [86][28], (2) down-scaling of especially n-channel OTFTs is needed, however, there is a lack of appropriate, cost-effective, high resolution structuring techniques, and (3) bias stress effects give rise to a change of OTFT performance during operation [107, 108].

The bias stress effect[29] is not unique to organic semiconductors. It has also been reported for poly-crystalline silicon [109], amorphous silicon [110], graphene [111], and transparent conductive oxides [112]. Reasons for bias stress are controversially discussed and mechanisms such as ion migration, charge carrier trapping, and breaking of molecular bonds have been suggested [107]. The bias stress induced degradation of OTFTs can be strongly reduced by the choice of the semiconductor material, the gate insulator material, and the pre-treatment of the gate insulator by self-assembled monolayers (SAMs) [107]. The first and the second aspect concerning OTFT restrictions as mentioned above, can partially be addressed by novel transistor concepts, most notably vertical organic thin-film transistors (VOTFT). The VOTFT concept is beneficial since it facilitates the realization of ultra-short vertical channels leading to a higher transconductance and moreover it allows for a higher integration density due to the overlap of source and drain. In this section, several VOTFT approaches are presented and discussed. The mechanisms causing the transistor-like operation in VOTFTs are still not fully understood. Therefore, no complete theory can be provided.

As it is the focus of Section 7.1 of this work, the review on VOTFTs done here is restricted to insulated gate VOTFTs with a vertical arrangement of the gate, source, and drain electrodes. Also other VOTFT concepts have been reported. However, in such devices the gate-source and the drain-source electric field are not completely in parallel [113–115][30] or the gate electrode is sandwiched between the source and the drain [34, 116–128][31].

---

[28]To build a high integrated circuits with a low power consumption n- and p-channel OTFTs are required.

[29]Bias stress: the current in a TFT is decreasing over time if a voltage V_{DS} and V_{GS} is applied. Possible mechanisms that may cause bias stress in OTFTs are discussed e.g. by Sirringhaus et al. [107].

[30]Such VOTFTs are typically realized employing edges of photo-resist, thus these transistors are actually quasi vertical.

[31]In this case the VOTFT is denoted as triode and the gate electrode is named as base.

Here, VOTFTs as illustrated in Figure 24 are discussed. In this geometry, gate, source, and drain electrodes are vertically arranged which means that the source-drain field and the gate-source field are in parallel.

Before the different VOTFT approaches are discussed, general similarities which are important for operation of any VOTFT reported so far are highlighted.

In analogy to horizontal OTFTs, charge carriers can be injected from the source electrode if a gate-source voltage larger than the threshold-voltage is applied. These charge carriers are accumulated at the gate-source interface. In order to push these charges from the insulator interface toward the drain electrode, the source electrode has to be perforated. This perforation of the source electrode can be achieved by either self-assembled growth on a rough gate insulator surface [129, 130], by self-assembled alignment of nanoparticles [131–136], or by a top-down structuring approach such as photo-lithography [137] or deposition through shadow masks [138]. A second characteristic feature of the source electrode, which is also of particular relevance for the functionality, is the formation of a blocking contact for charge carriers in order to prevent a parasitic current flow between source and drain which is uncontrollable by the applied gate field. This can either be accomplished by the formation of a Schottky barrier (see Figure 24(a)) between the semiconductor and the source electrode [129, 132–136, 139] or by employing an insulator material [131, 138] as shown in Figure 24(b).
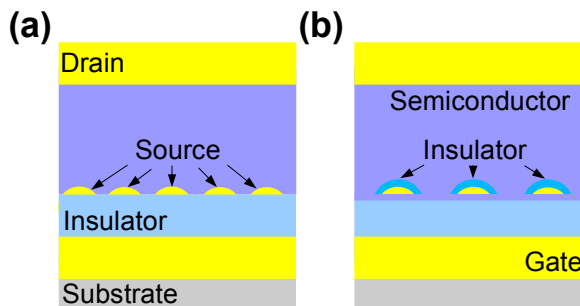
Figure 24: Scheme of two VOTFT concepts. **(a)** VOTFT without insulating layer between source and drain and **(b)** with insulating layer.

Ma's VOTFT concept: The first VOTFT, according to the previous classification, has been realized by Ma et al. [129] in 2004. As visualized in Figure 25, they employed a so-called super-capacitor comprising lithium fluoride (LiF) as insulator material with a maximum specific capacitance of $25 \mu F/cm^2$ and the buckyball molecule C_{60} as organic semiconductor. In a later publication[130] they also employed the polymer poly(3-hexylthiophene) ($P3HT$) in order to demonstrate p-channel performance of such devices. In both cases, the source electrode, which is directly deposited on the capacitor, contains microscopic pin-holes that originate from the native surface roughness of the insulator. The operation of this device is explained by the control of the charge carrier injection barrier between the source and semiconductor. They claim that this electron injection barrier is in the range of $\sim 0.8 eV$ and it is therefore sufficient to suppress charge carrier transport from source to drain. By applying the gate field and accordingly by the appearance of polarization charges at the insulator-electrode interface, this electron injection barrier can be remarkably modified. The maximum current density achieved in forward direction is $4A/cm^2$ at a drain-source and gate-source voltage of $5V$, respec-
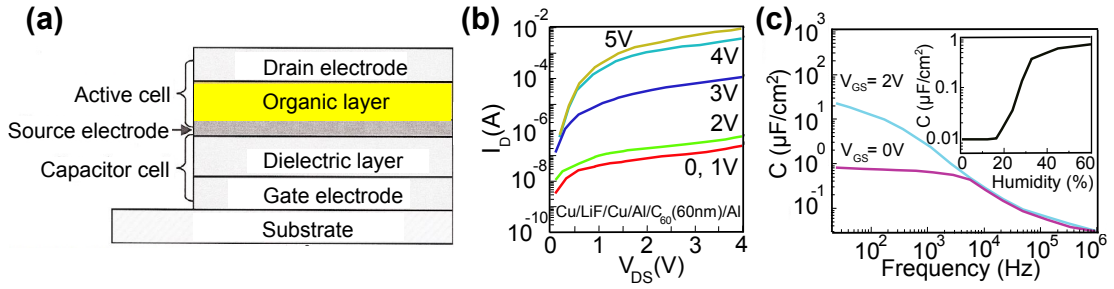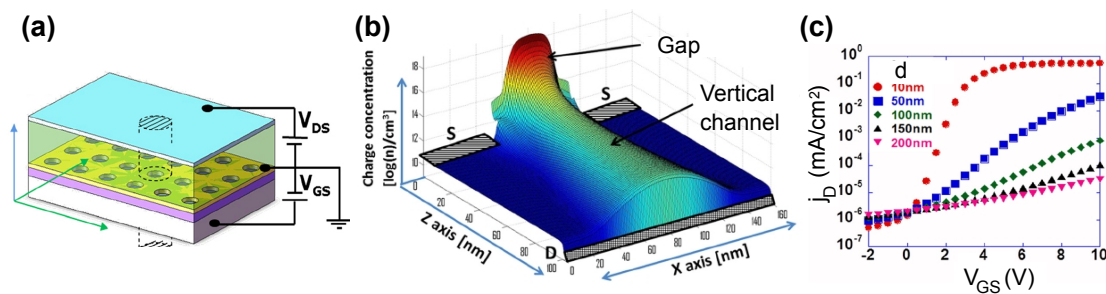
Figure 25: **(a)** Scheme of the VOTFT concept as reported by Ma et al. [129]. **(b)** Drain current vs. drain-source voltage for different gate-source voltages. **(c)** Capacitance (C) vs. frequency plot for a LiF super-capacitor for different voltages V_{GS} and different relative humidities (inset). Graphs are taken from [129].

tively. However, in forward direction no saturation-like behavior of the drain current is reached. Nevertheless, the on/off ratio[32] of such transistors exceeds 10^5. This high performance is enabled mainly by the high gate insulator capacitance which allows for large charge carrier densities at low voltages, the high electron injection barrier, and the high electron mobility of C_{60} of up to $5 cm^2/(Vs)$ [140]. Unfortunately, the reasons for this high capacitance and the high injection barrier are not sufficiently described. In particular, it has been shown by the same group [141] that the specific capacitance of the LiF super-capacitor almost does not depend on the insulator thickness, and the specific dielectric constant ϵ derived from these measurements is nearly 400 times larger than the expected value of $\epsilon = 9$. Moreover, the obtained insulator capacitance strongly depends on the environmental conditions, and changes in the total capacitance of more than two orders of magnitude have been reported if the device is characterized at different relative humidities ($20\% - 60\%$). Concerning the high injection barrier between the source electrode and the semiconductor, it has been shown by this group that also this barrier height strongly depends on sample fabrication conditions. In particular, they have used the same electrode materials and C_{60} as semiconductor to realize ultra-high-frequency diodes [142] where the absence of any kind of injection barrier is necessary.

Ben-Sasson's VOTFT concept: An alternative approach to realize VOTFTs has been demonstrated by the group of Tessler [132, 133, 136]. In order to manufacture a perforated source electrode as suggested by Ma et al. [129] they employed a block copolymer consisting of polystyrene nanocylinders as microscopic shadow mask (see Figure 26(a)) for deposition of the source electrode on a conventional gate insulator (SiO_2). This structuring procedure facilitates a controlled fabrication of conductive metal layers incorporating pin-hole openings with a dimension of several tens of nanometers. These pin-holes are filled up with C_{60} as semiconductor material. The VOTFT parameters reported [133, 136] are not exceeding values as presented by Ma et al. [129]. This

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[32]Ratio between drain current in the on-state at the maximum applied gate-source and drain-source voltage and the minimum drain current in the off-state at $|V_{GS}| < |V_T|$
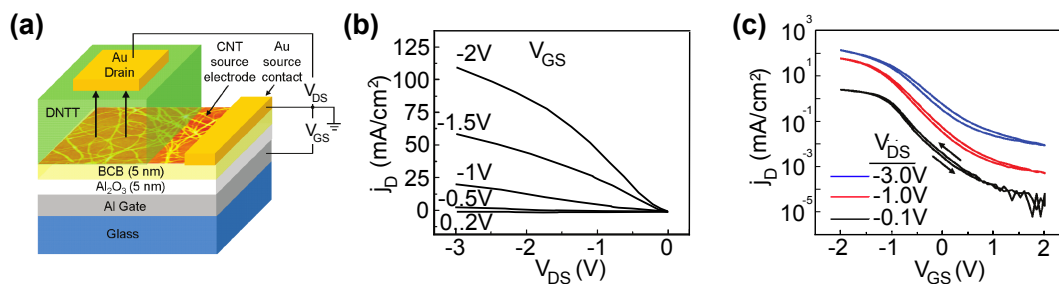
Figure 26: (a) Scheme of the VOTFT concept as presented by Ben-Sasson et al. [136]. **(b)** Numerical calculation of the charge carrier concentration in the vertical channel that appears in the gap of the source electrode (S). **(c)** Numerical calculations of the VOTFT transfer characteristics for different gate insulator thicknesses h_D. Graphs are taken from [136].

is presumably related to the lower specific capacitance of the employed gate insulator. Nevertheless, forward current densities of up to $1 A/cm^2$ have been reported at operating voltages of $V_{DS} = V_{GS} = 10V$. The on/off ratio is close to 10^5.

Most interestingly, they provided the first quantitative model for VOTFTs [136]. This theoretical description includes a 2-dimensional solution of the Poisson equation for a given electrode configuration and it assumes a field assisted injection from the source electrode into the organic semiconductor. The main parameters are the insulator thickness, the pin-hole width, the semiconductor thickness, the thickness of the source electrode, and the injection barrier between source and the organic semiconductor. The calculation of the electric field distribution provides a first step toward an understanding of the working mechanism of these devices. Within this picture, the superposition of the gate-source and the drain-source field leads to a local lowering of the injection barrier for charge carriers at the source-semiconductor interface. Thus, charge carriers can sufficiently be injected into the semiconductor which gives rise to the formation of a conductive channel within the pin-holes of the source electrode as illustrated in Figure 26(b). The pin-hole width, the insulator thickness, and the thickness of the source electrode are the geometrical parameters influencing this field distribution and accordingly the charge carrier injection behavior. Relying on these calculations, one can conclude that the amount of injected charge carriers is increased if the pin-hole width is increased or if the insulator thickness or the source thickness are reduced (see Figure 26(c)).

The role of the semiconductor thickness is twofold in this model. Since it governs the applied drain-source field, it influences the voltage that is required for charge carrier injection. Moreover, the thickness of the semiconductor determines the maximum current that can flow in such a device. This aspect is related to the fact that in this model the current has an empirical restriction when it reaches a space charge limited regime. Therefore, such devices change their operation from an injection limited to a space charge limited behavior. In a simple analogy to OTFTs, the role of the semiconductor thickness is similar to the role of the channel length. However, in VOTFTs the current exhibits a stronger dependence on the semiconductor thickness than in OTFTs, owing to the space

Figure 27: **(a)** Schema of the VOTFT concept as presented by McCarthy et al. [134]. **(b)** Drain current vs. drain-source voltage and **(c)** drain current vs. gate-source voltage of such SWCNT-DNTT VOTFTs. Graphs are taken from [134].

charge limited behavior. Furthermore, a saturation current as it appears in OTFTs is not expected in such vertical transistors.

Rinzlers's VOTFT concept: The concept of self-assembled source electrodes for VOTFTs has been adopted by the group of Rinzler [134, 135, 139]. In contrast to Tessler's approach they employed a conductive sheet of single-walled carbon nanotubes (SWCNT) as perforated source electrode. This layer is spin-coated onto a conventional gate insulator (Al_2O_3) and subsequently pentacene or dinaphthothienothiophene (DNTT) [143] is deposited. The stack is finalized by the drain electrode structured by a shadow mask (see Figure 27(a)).

For pentacene as well as DNTT one benefits from the appearance of a native Schottky barrier between the SWCNTs and the semiconductor. There are also other advantages of the SWCNT sheet. In particular, it is beneficial since the perforation of the source electrode can be changed by varying the spin-coating parameters. Moreover, the SWCNT sheet fabrication is compatible to established patterning procedures such as photo-lithography. However, the are also some specific disadvantages of the SWCNT sheet in comparison to Tessler's block copolymer approach. Especially the large series resistance of the SWCNT sheet strongly restricts the maximum current flow in the transistor. This aspect can be seen in the forward voltage behavior of the VOTFT where they exhibit a linear current-voltage performance instead of a saturation (see Figure 27(b)) which is caused by the Ohmic sheet resistance of the SWCNTs. Another disadvantage is that this VOTFT concept benefits from the high injection barrier at the SWCNT-pentacene/DNTT interface. This, however, can probably not be generalized to other organic materials. A third notable disadvantage is the roughness of such SWCNT electrodes. This feature requires a semiconductor thickness in the range of $500nm$ in order to avoid shorts in the device. Nevertheless, the performances of such VOTFTs including SWCNT electrodes are remarkable. As reported by McCarthy et al. [134], such transistors provide a current density of up to $0.1A/cm^2$ at a operating voltage of $4V$. Furthermore, the on/off ratio exceeds 10^5. The maximum current can further be increased if the thickness of the semiconductor is reduced.
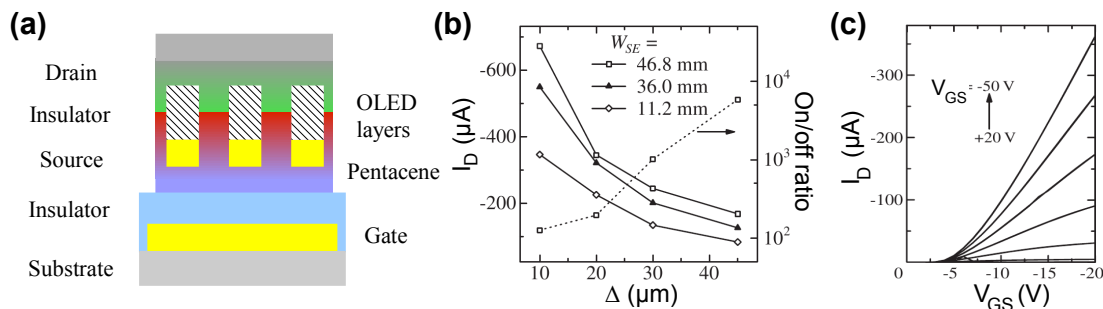
Figure 28: **(a)** Schema of Nakamura's VOTFT [144]. **(b)** Maximum drain current and on/off ratio vs. coverage width Δ of the source and the SiO_2 on top. **(c)** Drain current vs. drain-source voltage for different gate-source voltages Graphs are taken from reference [144].

Nakamura's VOTFT concept: A rather different approach to realize a vertical organic thin-film transistor has been presented by Nakamura et al. [138, 144]. As illustrated in Figure 28(a) they structured the source electrode by shadow masks. In comparison to the other approaches presented here, the size of the openings in the source ($5\mu m$) is rather large. Moreover, and also in contrast to the other approaches, they deposited a $100nm$ thick layer of SiO_2 on top of the source contact in order to provide an electric insulation between source and drain. As a special feature, they embedded a complete OLED within this stack and therefore the application of such transistors in efficient organic light emitting transistors (OLET) has been highlighted by this group. However, compared to the other approaches the performance of Nakamura's VOTFT is rather poor. The on/off ratio is clearly below 10^4 and the maximum current density merely reaches $0.01A/cm^2$ at a gate-source voltage of $50V$. The reduced performance is partially related to the poor charge carrier transport in the included OLED materials, but primarily it is caused by the low specific gate insulator capacitance of $\sim 10nF/cm^2$. Thus, an increase of its value will lead to a strong decrease of the required gate-source voltage. Nevertheless, the concept as presented by Nakamura greatly demonstrates that VOTFTs can be also realized using top-down structuring techniques which are favorable for thorough and quantitative investigations on VOTFT where a precise control of geometric parameters is essential.

In conclusion, continuous improvements and the development of new VOTFT architectures have accounted for the fact that, in terms of performance, modern VOTFTs are comparable to state-of-the-art OTFTs. All important quantities of the VOTFTs discussed in this section are summarized in Table 1. Some particular VOTFT concepts can already surpass the performance of OTFTs concerning the maximum current density, the on/off ratio and their potential to be stacked with OLEDs. Apart from that, VOTFTs have not yet reached the technological level of OTFTs. In others words, the integration of VOTFTs in complete electric circuits such as inverters, ring oscillators, or display drivers has to be demonstrated and specific integration techniques need to be developed for that purpose. Nevertheless, VOTFTs exhibit a notable alternative beyond

state-of-the-art OTFTs which is not only of scientific interest, but they will also be fascinating for certain applications since they are suited to combine novel nanocompounds, novel integration and fabrication techniques, and highly efficient organic devices such as OLEDs.

Reference	Layer sequence	Operating voltage V_{GS} / V_{DS} (V)	On/Off-ratio	Maximum current density (mA/cm^2)	Charge carrier species	Subthreshold swing S (mV/dec)	Specific gate insulator capacitance ($\mu F/cm^2$)
[129, 130]	glass/ Cu/ LiF(240nm)/ Cu(20nm)/ Al(10nm)/ C_{60}(90nm)/ Al(50nm)	5 / 5	10^5	4000	electrons - C_{60}[129] holes - P3HT[130]	~ 600	25
[133, 136]	p − doped silicon/ SiO_2(100nm)/ Au(10nm)/ C_{60}/ Al(100nm)	10 / 10	10^5	1000	electrons - C_{60}	not reported	0.03
[134]	glass/ Al/ Al_2O_3(5nm)/ DNTT(480nm)/ Au(30nm)	4 / 4	10^5	110	holes - DNTT	~ 500	1.71
[138]	glass/ indium tin oxide/ SiO_2(300nm)/ pentacene(50nm)/ Au(30nm)/ SiO_2(100nm)/ OLED (see[138])/ Al(80nm)	50 / 8	$< 10^4$	< 10	holes - pentacene	not reported	0.01

Table 1: Overview on important parameters of different VOTFT concepts reported in literature.

Chapter III

Methods and Materials

'La vérité n'est pas l'exactitude.'

———————————————————————

H. Matisse, artist.

In this section principles and technical details of impedance spectroscopy, current voltage, and field-effect transistor characterization are described with regard to their application to organic semiconductors. Hereby, these methods do not only help in disclosing characteristics of complete electronic devices, they can also reveal basic parameters of charge transport like the charge carrier mobility. Finally, materials for hole and electron transport as well as for molecular doping are introduced concerning chemical structure and electronic properties. Furthermore, technical methods for device preparation like thermal evaporation and photo-lithography are presented.

3.1 Impedance Spectroscopy

The principle of impedance spectroscopy can be treated in a general context describing the response of an arbitrary system to a given stimulus. Thus, an adopted stimulus $\mathfrak{S}(t')$ at a time t' and its effect to the system $\mathfrak{W}(t)$ at a time t are connected by the response

function $\mathfrak{h}(t, t')$ as

$$\mathfrak{S}(t') \rightarrow \mathfrak{h}(t, t') \rightarrow \mathfrak{W}(t). \tag{103}$$

In order to derive the dependencies analytically, three assumptions concerning linearity, causality, and time-invariance need to be considered which can be expressed as

$$
\begin{aligned}
\mathfrak{W}(t) =& \quad \int_{-\infty}^{\infty} \mathfrak{h}(t, t')\mathfrak{S}(t')dt' & \Rightarrow \text{linearity} \\
=& \quad \int_{-\infty}^{t} \mathfrak{h}(t, t')\mathfrak{S}(t')dt' & \Rightarrow \text{causality} \\
=& \quad \int_{-\infty}^{t} \mathfrak{h}(t - t')\mathfrak{S}(t')dt' & t' = t - t'' \\
=& \quad \int_{0}^{\infty} \mathfrak{h}(t'')\mathfrak{S}(t - t'')dt'' & \Rightarrow \text{time-invariance.}
\end{aligned}
\tag{104}
$$

Since causality and time-invariance are always fulfilled for physical systems, merely the linearity of the response needs to be ensured. However, if all these three assumptions are satisfied, it is shown [145] that the real and imaginary part of the transmission function $\mathfrak{H}(\omega)$, defined as

$$\mathfrak{H}(\omega) = \int_{-\infty}^{\infty} \mathfrak{h}(t)exp(i\omega t)dt, \tag{105}$$

are linked by a Hilbert transformation which is known as the Kramers-Kronig relation in physics. Hereby, $Re\{\mathfrak{H}(\omega)\}$ and $Im\{\mathfrak{H}(\omega)\}$ obey

$$
Re\{\mathfrak{H}(\omega)\} \quad = \frac{1}{\pi}\wp \int_{-\infty}^{\infty} \frac{Im\{\mathfrak{H}(\omega)\}}{\omega' - \omega}d\omega' \tag{106}
$$

$$
Im\{\mathfrak{H}(\omega)\} \quad = -\frac{1}{\pi}\wp \int_{-\infty}^{\infty} \frac{Re\{\mathfrak{H}(\omega)\}}{\omega' - \omega}d\omega' \tag{107}
$$

where $\wp \int$ denotes the principal value of the integral in the upper complex plane. The consequences of the Kramer-Kronig relation in the field of physics are tremendous since they separate linear systems with superposition and causality from non-linear systems that show effects like frequency multiplication.

For characterization of electronic devices, the concept of impedance spectroscopy is based on a measurement of the current response $\tilde{I}(t)$ onto a small signal voltage stimulus $\tilde{V}(t)$[33]. In the Fourier domain this can be expressed by

$$\tilde{I}(\omega) = \tilde{Z}(\omega) \cdot \tilde{V}(\omega), \tag{108}$$

where $\tilde{Z}(\omega)$ is the complex impedance and $\tilde{I}(\omega)$ and $\tilde{V}(\omega)$ are the corresponding complex Fourier functions of $\tilde{I}(t)$ and $\tilde{V}(t)$. The complex impedance $\tilde{Z}(\omega)$ (or its inverse the complex admittance $\tilde{Y}(\omega) = 1/\tilde{Z}(\omega)$) can be considered as equivalent to the transmission function of the system. This complex impedance $\tilde{Z}(\omega)$ can be expanded into to real and imaginary part as $\tilde{Z}(\omega) = \tilde{Z}'(\omega) + i \cdot \tilde{Z}''(\omega)$. These quantities are directly accessible by measurements since they represent the in-phase and out-of-phase response of the system with respect to the stimulus.

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[33]To ensure the applicability of Ohm's law, current and voltage have to be chosen in the small perturbation regime [146]. For room temperature conditions this is typically fulfilled for an amplitude of $\sim 20mV$

To obtain a physical meaning of the abstract transmission function $\tilde{Z}(\omega)$, which is an analytic function in the complex plane, $\tilde{Z}(\omega)$ has to be fitted to an equivalent electronic circuit, which will be discussed in the following section. By this approach, electronic elements like ideal capacitors, resistors, or coils are combined to model the transmission of the system under investigation. The properties and the arrangement of these electronic elements are free parameters and can be chosen in a way that one can obtain a complex impedance function that mimics the physical behavior of the device. However, since parameter descriptions of curves in the complex plane are never unambiguous, several equivalent circuits can be used to achieve the same impedance $\tilde{Z}(\omega)$. This provides the main drawback of impedance spectroscopy analysis by equivalent circuits.

A more direct approach to analyze impedance spectra is given by derivation of impedance functions from charge transport equations (e.g. drift-diffusion equation). In this way, the obtained spectra can directly be used for fitting with theoretical derived impedance functions. This approach is employed here to describe the diffusion of charge carriers in pin-diodes (compare Subsection 2.2.3).

In general, both strategies for analysis of impedance functions are powerful approaches to investigate phenomena of e.g. charge carrier transport, charge carrier trapping, and formation of charge depletion zones.

3.1.1 Capacitance-Frequency Spectroscopy

To probe the response of an electronic device, a small sinusoidal voltage stimulus of varying frequency is applied to the sample. The frequency variation typically ranges from the μHz to the MHz regime. Important physical phenomena like dielectric material relaxation, charge carrier transport, charge carrier trapping, and emission have characteristic time constants. Depending on these time constants, every process dominates a certain part of the frequency dependent impedance response. Thus, the knowledge on these time constants is indispensable for the interpretation of impedance spectra.

Dielectric material relaxation and RC equivalent circuits: A non-metallic material is characterized by a finite dielectric function $\epsilon(\omega)$[34]. Therefore a static electric field can appear in the material as well as a space charge region can emerge. However, without an external electric field, an initial space charge density $\rho(\vec{x}, t)$ will be dispersed, which is caused by the local charge carrier density gradient. The characteristic time constant for this process is denoted as dielectric material relaxation time τ_D. In a first approach adopting Ohm's law, this time constant can be derived for a single isotropic material from the continuity equation $\frac{\partial \rho}{\partial t} = -div\vec{j} = -div(\sigma\vec{E})$ and Maxwell's law $div\vec{E} = \rho/\epsilon(\omega)$. Thus, from $\frac{\partial \rho}{\partial t} = -\frac{\hat{\sigma}\rho}{\epsilon(\omega)\epsilon_0}$ the dielectric material relaxation time,

---

[34]Impedance analysis done within this thesis is restricted to frequencies $< 1GHz$. Therefore, it can be assumed that ϵ is frequency independent.

(a)

C_1=100 nF   C_2=2 nF

1 kΩ

R_s $R_{p,1}$ $R_{p,2}$

50 kΩ   5 kΩ

$f_1=(2\pi R_{p,1}C_1)^{-1}$ $f_2=(2\pi R_{p,2}C_2)^{-1}$

=31.8 Hz   =15.9 kHz

(b)

(c)

(d)
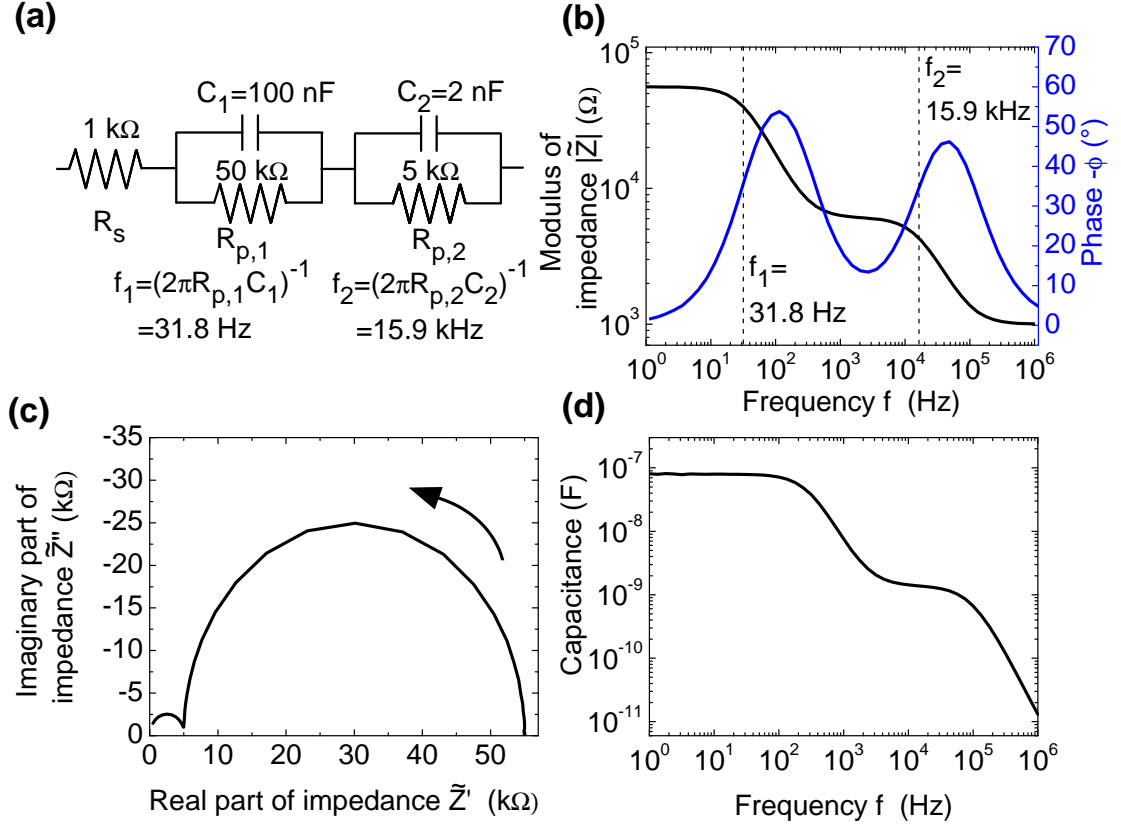
Figure 29: (a) Equivalent circuit representation for a bi-layer device including a series resistance. **(b)** Modulus of impedance and phase for the equivalent circuit depicted in (a). **(c)** Bode diagram of the impedance data shown in (b). The arrow indicates the direction of increasing frequency. **(d)** Capacitance of the impedance spectrum shown in (b) calculated according to Eq.112.

which is required for the disappearance of the local space charge gradient is given by

$$\tau_D = \frac{\epsilon\epsilon_0}{\sigma} = \frac{\epsilon\epsilon_0}{qn\mu}. \tag{109}$$

This equals the product of the specific resistance $\tilde{r} = (\sigma)^{-1} = (qn\mu)^{-1}$ and the specific capacitance $\tilde{C} = \epsilon\epsilon_0$. Accordingly, for a frequency f of a sinusoidal voltage stimulus with $f << \frac{1}{\tau_D}$, the device response can be described by the impedance of an ideal resistor with a resistance of $R = \frac{1}{\mu ne}\frac{d}{A}$, where d is the thickness of the layer and A the active area. In contrast, if the condition $f >> \frac{1}{\tau_D}$ is fulfilled, the layer behaves electrically like an ideal capacitor with the capacitance $C = \epsilon(\omega)\epsilon_0\frac{d}{A}$. Hence, an equivalent circuit representation of a single dielectric layer is given by a parallel RC-unit (compare Figure 29).

In case of a multi-layer device (layer index k), the RC-units have to be connected in series which leads to a total impedance of

$$\tilde{Z} = \sum_k \Big(\frac{1}{R^k} + i\omega C^k\Big)^{-1} = \sum_k \frac{R^k}{1 + i\omega\tau_D^k} = \sum_k \frac{R^k}{1 + (\omega\tau_D^k)^2} - i\sum_k \frac{\omega\tau_D^k R^k}{1 + (\omega\tau_D^k)^2}. \tag{110}$$

For multi-layer devices as described within this thesis, time constants τ_D^k of the individual layers are rather different. Specifically, in pin-diodes τ_D^k of the doped layers is small owing to their high electrical conductivity, while τ_D^k of the intrinsic layer is typically large (for not too large forward voltages). In this situation, having one dominant RC-unit ($\omega\tau_D^i \approx 1$, $\omega\tau_D^k << 1 \; \forall k \neq i$), Eq.110 can be simplified to

$$\tilde{Z} = \sum_{k\neq i} R^k + \frac{R^i}{1+(\omega\tau_D^i)^2} - i\frac{\omega\tau_D^i R^i}{1+(\omega\tau_D^i)^2}, \tag{111}$$

where the first term represents a series resistance and the last two terms are the dominant RC-unit. If the series resistance can be neglected and one can find the layer capacitance of the dominant RC-unit as

$$|\tilde{Z}| = \frac{(R^i)^2}{\sqrt{1+(\omega\tau_D^i)^2}} = |\tilde{Z}|^2\Big(\frac{1}{R^i} - i\omega C^i\Big) = \tilde{Z}' + i\tilde{Z}'' \Rightarrow C^i = -\frac{\tilde{Z}''}{\omega|\tilde{Z}|^2}. \tag{112}$$

However, for $\omega\tau_D^i > 1$ Eq.112 cannot be derived from Eq.111. Moreover, there is no analytic expression for determination of the layer capacitance. The specific capacitances and resistances of the individual layers have to be evaluated by fitting of the impedance spectra by Eq.110.

Figure 29 displays the impedance according to Eq.110 of a circuit that contains a series resistance and two RC-units with fairly different RC-times. The modulus of the impedance (see Figure 29(b)) shows three distinct plateaus where $|\tilde{Z}|$ is approximately given by the values of the individual resistances in the circuit (see Figure 29(a)). Accordingly, the behavior of the circuit is Ohmic in this frequency range while in between the plateaus the behavior switches to a capacitive regime. This can also be seen in the Bode diagram (see Figure 29(c)). Here, the impedance function describes two semi-circles and the starting points of these circles are given by the resistance values ($1k\Omega$, $5k\Omega$, $50k\Omega$,). Figure 29(d) displays the capacitance-frequency (C-f) spectrum of the circuit shown in (a) as calculated by Eq.112. Again, two plateaus of capacitance are visible and their values are in agreement to the circuit parameters. Hence, determination of capacitance according to Eq.112 provides an ideal capacitance (frequency independent) if the modulus of the impedance shows clear and distinct plateaus (which means that the RC-times of the individual RC-units are fairly different). In between the plateaus, the capacitance has no meaningful value. Particularly, in Figure 29(d) the transition from the plateau at $f < 100Hz$ to the plateau at $f > 10000Hz$ is related to the changing influence of the RC-units and the decay at higher frequencies $f > 100000Hz$ is caused by the series resistance.

Charge carrier trapping: Besides dielectric relaxation, another important time dependent process, especially in context of organic semiconductors, is the charge carrier trapping and release. A single trap level is characterized by its emission time τ_e. Relying on Boltzmann statistics, this time constant is proportional to the exponent of trap level depth (distance between trap level and transport level). Again, a single RC-unit can
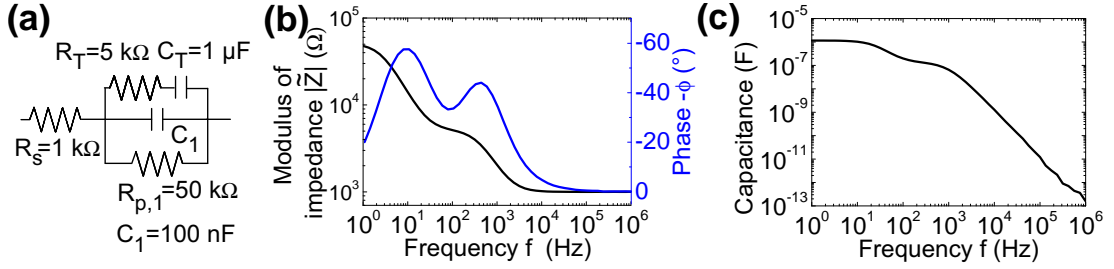
Figure 30: (a) Equivalent circuit representation for a single dielectric layer and a single trap level. **(b)** Modulus of impedance and phase for the equivalent circuit depicted in (a). **(c)** Capacitance of the impedance spectrum shown in (b) calculated according to Eq.112.

be employed to mimic the influence of a single trap level on the impedance spectrum [146, 147]. If the trap level is uniformly distributed in the layer, the trap related RC-unit has to be placed in parallel to the RC-unit of the layer (compare Figure 30(a)). As e.g. discussed by Vincent et al. [147], the circuit parameters for the trap level R_T and C_T are not independent since their product τ_e contains a temperature and trap density dependence. In consequence, the density of traps and their depth cannot be determined by fitting of a single spectrum. In order to extract these quantities, temperature dependent measurements of τ_e have to be done to determine the trap depth.

In Figure 30(b) and (c) the impedance spectrum and the calculated capacitance function according to Eq.112 are depicted. The impedance spectrum showing three plateaus has a similar shape to the spectrum shown in Figure 29(b). This is due to the fact that both circuits can be converted to each other by the right set of transformation parameters[35]. However, comparing the calculated capacitance function (Figure 30(c)), one can observe strong differences. While in Figure 29 the plateaus of the individual RC-unit can be seen in the impedance spectrum as well as in the capacitance function, this correlation is not possible for the circuit shown in Figure 30(a). In particular, the capacitance function provides a value of $1\mu F(100nF)$ if the impedance has a value of $50k\Omega(5k\Omega)$ which is in contradiction to the circuit parameters. This is related to the fact that the time constants of both RC-units in the equivalent circuit are not separable as e.g. done in Eq.110. Thus, in terms of practical impedance analysis, it is essential to test several equivalent circuit models and check if the capacitance values are reasonable and can be associated e.g. to expected layer capacitances.

For more complex trap distributions (e.g. Gaussian or exponential) special equivalent circuit models and non-ideal circuit elements (constant phase elements) have been proposed (compare e.g. [148, 149]. However, it is beyond the scope of the present work to describe these models in detail. An overview is given e.g. by Bisquert [150].

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[35]An equivalent circuit is a parameter description for a given impedance function. However, this parameter descriptions are never unambiguous.

3.1.2 Capacitance-Voltage Spectroscopy

If a dominant time constant of one RC-unit can be identified within a certain frequency range, the impedance measurement can be extended to different static large signal voltages. This situation allows for an analysis of RC time constant vs. the applied static voltage. Thus, if this time constant is e.g. associated to a depletion layer capacitance as it appears in a pin-diode, one can determine the built-in voltage of the diode as well as the density of ionized dopant states from the voltage dependent capacitance. These parameters are linked to the depletion capacitance by the profiler equation (compare Eq.44 and 68).

There are two different methods to perform capacitance-voltage (C-V) measurements. The exact one is to record impedance spectra for different voltages and extract from fitting of the frequency dependent impedance the corresponding voltage dependent capacitance function. However, very often one can simply record the impedance for a certain frequency and vary the applied static voltage. This is a rather convenient and fast approach which also reduces the measurement stress to the sample. However, this method is only feasible if the capacitance vs. frequency plot shows clear and distinct plateaus and the C-V is recorded at a frequency where the C-f spectrum exhibits such a plateau.

3.1.3 Technical Notes on Impedance Spectroscopy

For experimental investigations two different impedance spectrometers are used. Both vary in their frequency range and in the way they measure impedance. However, they are comparable concerning experimental accuracy.

The first tool is a $Precision\ LCR - Meter\ 4248A$ from $Hewlett\ Packard$ with a frequency range from $20Hz$ to $1MHz$. The automatic measurement procedure is based on a bridge comparator which allows to determine real and imaginary part of impedance. For signal frequencies $< 50Hz$ this tool is suffering from an increased noise level since the signal is not filtered e.g. by a lock-in amplifier.

The second tool is denoted as $PGSTAT302N$ from the company $AUTOLAB$. This tool records the impedance by a lock-in amplifier. This leads to a considerable increase of the accessible noisefree frequency range from $1\mu Hz$ to $1MHz$.

For investigations within this thesis both tools are used and no significant difference in measurement quality could be identified.

3.2 I-V Measurements and OTFT Characterization

Current-voltage characterization: A current-voltage measurement is presumably the most frequently used technique to characterize semiconductor devices. Within this thesis, organic diodes and thin-film transistors are characterized by quasi-static and dynamic
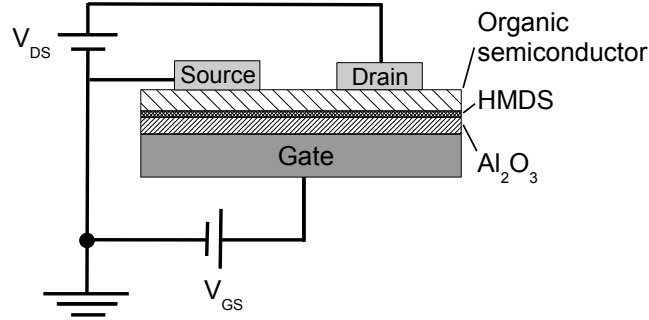
Figure 31: Scheme of an OTFT in a bottom gate, top source/drain configuration. For electrical characterization the source electrode is chosen as the reference electrode.

current-voltage measurements. Technical details of dynamic I-V measurements are explained in Subsection 3.3. All quasi-static I-V measurements performed within this thesis are recorded by source-measurement units (SMU). SMU's are convenient for I-V characterization since they can act simultaneously as a voltage (current) source while measuring the current (voltage). Several types of SMU's are used here: *Keithley SMU* 2400, *Keithley* $4200 - SCS$, and *Hewlett Packard* $4145B$. All these tools allow a characterization with a resolution of $\sim 50pA$ ($\sim 5mV$) and furthermore they cover a large current (voltage) range up to $1A$ ($200V$). The I-V characterizations done here are performed under dark conditions (or ambient light) with a typical ramp speed of $0.1V/s$ (SMU as voltage source).

OTFT characterization: Organic thin-film transistors are prepared in a bottom gate and top source/drain configuration. A highly doped silicon wafer with a specific resistance of $50m\Omega cm$ serves as gate electrode. Onto this wafer aluminum oxide (Al_2O_3) as high quality gate insulator is deposited by atomic layer deposition (ALD, $\epsilon_{Al_2O_3} = 7.8$, processing done by Namlab, Dresden). The two main layer thicknesses of Al_2O_3 are $23nm$ and $50nm$, respectively. Before deposition of the semiconductor material, these samples are routinely cleaned by acetone, ethanol, and isopropanol ($5min$ ultra-sonic bath for each solvent). Afterwards the samples are exposed to an oxygen plasma for $10min$ and dipped into pure hexamethyldisilazane (HMDS, $30min$ at room temperature) for surface passivation. Spin rinsing using isopropanol is employed to remove residuals of HMDS. Then the organic semiconductor material is deposited and the stack is finalized by deposition of source and drain electrodes (for details about the deposition technique see Subsection 3.4). Source and drain electrodes are structured either by shadow masks or by photo-lithographic patterning (see Subsection 3.4). Different source-drain geometries are realized within this thesis. The specific OTFT parameters (channel length and width) are provided in the description of the individual experiments.

OTFTs are standardly characterized in a nitrogen glovebox by a parameter analyzer (2 SMUs) *Hewlett Packard* $4145B$. The typical configuration for electrical OTFT characterization with the source electrode grounded is shown in Figure 31.
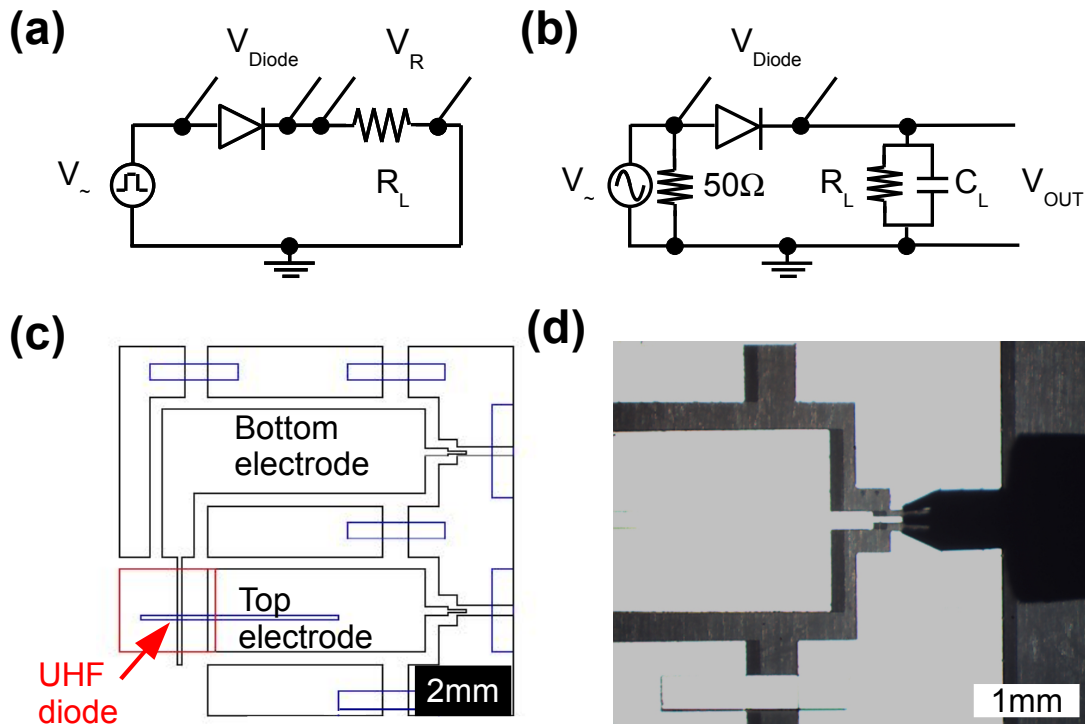
Figure 32: (a) Electric circuit for pulsed measurements on organic pin-diodes. In experiments the resistor R_L (pulse resistive) has a value of 100Ω. The diode voltage V_{Diode} and the resistor voltage V_R are measured via a scope. A $HP\ 8114A$ (bandwidth $200MHz$) is used as a pulse generator. **(b)** Electric circuit for rectification measurements. The load circuit consists of a resistor R_L and a capacitor C_L. **(c)** Layout of the UHF diodes in a special design for UHF applications. **(d)** Photograph of a UHF diode on a wafer prober with a probe attached to the sample.

Temperature dependent measurements: For temperature dependent I-V, C-f, and C-V characterization of organic diodes a cryostat, cooled by liquid nitrogen, is used. The samples are mounted on the cooling copper block in vacuum (pressure $< 10^{-1} mbar$) and the temperature can be varied between $\sim 170K$ and $\sim 390K$. The temperature control accuracy is approximately less than $1K$.

3.3 UHF Measurements and Rectification Circuits

For characterization of organic pin-diodes that are designed for UHF applications, two different measurement regimes are employed. The organic diodes are embedded in an electronic circuit to either act as a current switch or as a rectifier.

The current switch circuit basically consists of the diode and a resistor in series (see Figure 32(a)). The purpose of the resistor is to act as a reference for current determination. In this way the on- and off-switching behavior may be investigated which allows e.g. for an extraction of charge storage time (compare Subsection 2.2.4). However, it should be

noted that the resistor has a considerable influence on the switching behavior if its value is similar to the diode resistance. This particularly affects the on-switching behavior of the diode. Hence, for a quantitative analysis of transit time this additional resistance has to be taken into account. In contrast, the off-switching is almost unaffected since in reverse direction the diode resistance is significantly larger than the reference resistance. Hence, a quantitative analysis of the charge carrier storage time is possible.

The circuit used for characterization of rectification properties is displayed in Figure 32(b). Instead of a single resistor, the load circuit contains a resistor and a capacitor in parallel. If the diode is biased in forward direction the capacitor is loaded. If the diode is reverse biased, the capacitor is discharged via the load resistor which mimics an additional voltage source. The load circuit has to be chosen with respect to the diode resistance and the applied frequency. In particular, the load resistance has to be significantly larger than the forward resistance of the diode and the RC time of the load has to be larger than the period of the applied signal. If these conditions to the RC-unit are fulfilled, it acts as a smoothing circuit that can efficiently reduce ripples in the rectified signal. To supply a sinusoidal signal to the circuit either a $Agilent\ 33220A$ or a $Agilent\ E8257D$ is employed.

UHF investigations on electronic devices are challenging since the device is embedded in a geometry of metallic contacts that may act as a wave guide if the wave length of the applied signal is comparable to the dimensions of the metal geometry. A special device layout is designed to guarantee a characterization of the organic diode with a negligible influence of metal contacts and wires (see Figure 32(c)+(d)). This layout is applicable up to frequencies of $\approx 5 GHz$.

3.4 Sample Preparation

Substrates and cleaning: For fabrication of organic devices such as diodes and OTFTs different kinds of substrates are used. While organic diodes are exclusively prepared on a borosilicate glass substrate, organic thin-film transistors are fabricated on highly doped silicon wafers which are covered by a thin layer of Al_2O_3 as a gate insulator. However, all substrates are cleaned by a standard procedure using acetone, ethanol, and isopropanol in a ultra-sonic bath ($5min$ each). Afterwards samples are exposed to oxygen plasma for $10min$ and then directly transferred into either vacuum or a oxygen-free atmosphere. Substrates for OTFT are additionally dipped into pure hexamethyldisilazane (HMDS, $30min$ at room temperature) before they are stored in vacuum. HMDS leads to surface passivation of the gate insulator which strongly reduces the density of interface states and therefore hysteresis effects of OTFTs. Residuals of HMDS are removed by spin rinsing using isopropanol.

Physical vapor deposition: Organic materials and metal contacts are deposited under vacuum conditions (base pressure $10^{-7}mbar$) by thermal evaporation (physical vapor
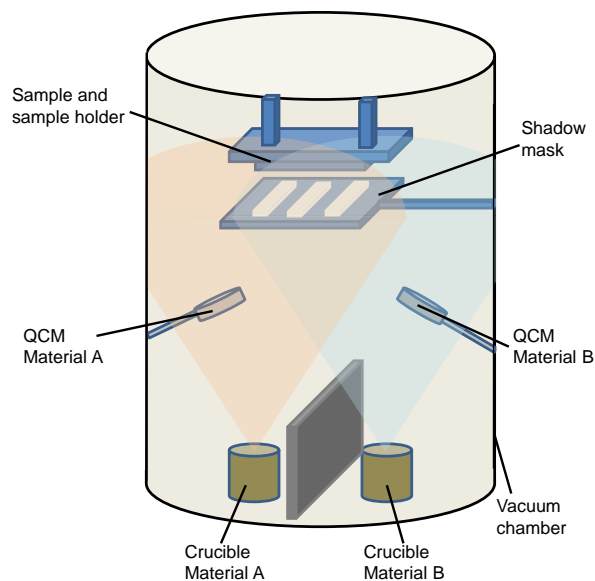
Figure 33: Sketch of a vacuum chamber as used for physical vapor deposition of organic semiconductors. The chamber contains two crucibles for co-deposition of e.g. a host and a dopant material.

deposition). Film thickness and deposition rates are controlled by quartz crystal monitors. Organic materials used in this work can be evaporated at moderate temperatures $(360 - 770K)$ out of a ceramic crucible as illustrated in Figure 33. For electrochemical doping of organic semiconductors two materials are deposited simultaneously. This co-deposition technique (compare Figure 33) with two independent rate monitors allows for a precise control of doping concentration which can be adjusted down to $0.1mol\%$ of dopant molecules.

For fabrication of organic electronic devices several vacuum systems are used. There are two multi-chamber systems (UFOI and UFOII) for manufacturing of single samples. Additionally, there are two single-chamber systems (Lesker A and Lesker B) for fabrication on a wafer scale. Within the Lesker A and B tool up to 36 samples can be prepared within one run and parameters such as materials, layer thicknesses, and doping ratios can be modified.
Organic diodes are encapsulated after deposition in a nitrogen glovebox using a glass lid and epoxy glue. Encapsulation is required to prevent moisture and oxygen induced degradation under ambient conditions.

Photo-lithography: Down-scaling and integration are major requirements to improve the performance of organic electronic circuits and therefore guarantee their commercial success. Presumably, the most reliable process for down-scaling and integration is photolithography. It combines advantages such as high spatial resolution, high controllability, high through-put, and fast and low cost processing.
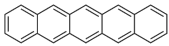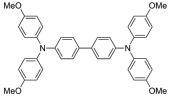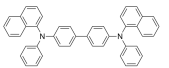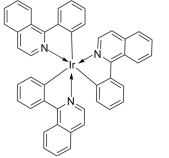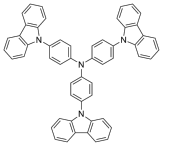
Within this work the technique of photo-lithography is used for patterning of metals, insulators, and organic semiconductors. Most small molecule organic semiconductors are not compatible with conventional photo-lithography protocols in which aggressive solvents and developer solutions that contain e.g. toluol or chemical bases (e.g. $NaOH$) are used. To allow a photo-lithographic patterning of small molecule organic semiconductors, a novel photo-lithography procedure using photo-resist and solvent compounds that are benign to organic semiconductor materials has been developed. This concept is based on highly fluorinated photo-resist and solvent compounds that are benign to most organic semiconductors and orthogonal in terms of solubility to polar and non-polar solvents. This principle has been demonstrated by DeFranco et al. [151–153] for polymers. In this work it is extended to small molecule organic semiconductors and details of manufacturing are given in Section 6.1.

To perform photo-lithography an exposure system from *Intelligent Micro Pattern, USA* is employed. Within this tool $(SF - 100)$ a mercury lamp is used that illuminates a micro-mirror array by spectral light ($313nm$, $365nm$, $405nm$). This micro-mirror array consists of $1024x768$ small micro-actuators (piezos) that can be switched electronically. The pattern generated by the micro-mirror array is transfered via a lens system and several apertures to the sample. The exposure field on the sample is $11x8mm$, hence the resolution is approximately in the range of $10\mu m$ (non-reduction mode). If an additional lens is placed in front of the sample (reduction mode) the exposure field is reduced to $3.7x2.7mm$ and the resolution is improved to $\approx 3\mu m$.
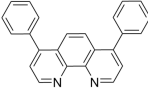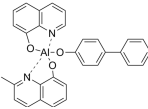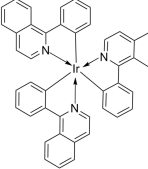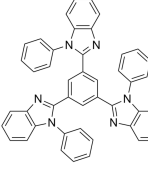
3.5 Materials

Materials used within this work can be categorized into hole transport materials, electron transport materials, and dopants. These categories actually arise from the usage of these materials in organic electronic devices, but they do not specify if a material has a higher conductivity for electrons or holes. In particular, materials are defined as hole or electron transporters by the choice of the metal of the corresponding electrode. Hence, if hole injection is energetically preferred, the material is denoted as hole transporter and if electron injection is preferred, the material is denoted as electron transporter, respectively.
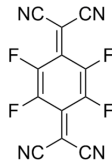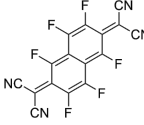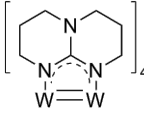
Within the following tables all small molecule organic semiconductors used within this thesis are introduced and basic physical quantities as they are important for electronic transport are summarized.

Name	Abbre-viation	Structure	HOMO/ LUMO (eV)	Charge carrier mobility $(cm^2/(Vs))$	Density (g/cm^3)
pentacene	P5		5.1/ 3.2	≈ 1	1.325
N,N,N',N'- Tetrakis (4-methoxyphenyl)-benzidine	MeO-TPD		5.1/ 1.9	$\approx 10^{-5}$	1.46
N,N'-Di(naphthalen-1-yl)- N,N'- diphenyl-benzidine	NPB		5.4/ 2.5	$\approx 10^{-3}$	1.14
Tris(1-phenylisoquinoline) iridium(III)	Ir(piq)$_3$		5/ 2.4	–	1.5
4,4',4"-tris(carbazol-9-yl)-triphenylamine	TCTA		5.7/ 2	–	1.13

Table 2: Overview on hole transport materials. Data and structures are taken from [154].

Name	Abbre- viation	Structure	HOMO/ LUMO (eV)	Charge car- rier mobil- ity $(cm^2/(Vs))$	Density (g/cm^3)
C_{60}	C_{60}		6.4/ 4	1...5	1.63
Bathophenanthroline 4,7-diphenyl-1,10-phenanthroline	BPhen		6.4/ 3	$\approx 10^{-4}$	1.244
Aluminum (III) bis(2-methyl-8-quninolinato)-4-phenylphenolate	BAlq$_2$		6.1/ 3	–	1.33
Tris(1-phenylisoquinoline) iridium(III)	Ir(piq)$_3$		5/ 2.3−2.4	–	1.5
2,2',2"-(1,3,5-Phenylen)tris(1-phenyl-1H-benzimidazol)	TPBi		6.3/ 2.8	1.8×10^{-5}	1.247

Table 3: Overview on electron transport materials. Data and structures are taken from [154].

Name	Abbre-viation	Structure	HOMO/ LUMO (eV)	n/p-type dopant
2,3,5,6-Tetrafluoro-7,7,8,8-tetracyano-quinodimethane	F_4-TCNQ		8.3/ 5.2	p-type
2,2'-(perfluoronaphthalene-2,6-diylidene) dimalononitrile	F_6-TCNNQ		−/ 5.4	p-type
Tetra-kis(1,3,4,6,7,8-hexahydro-2H-pyrimido[1,2-a]pyrimidinato) ditungsten (II)	$W_2(hpp)_4$		6.1/ 3	n-type
cesium	Cs		work function 2.14eV	n-type

Table 4: Overview on dopant materials. Data and structures are taken from [154].

Chapter IV

Properties of Organic pin-Diodes in Reverse Direction

'Never make a calculation until you know the answer.'

<div style="text-align: right">

J.A. Wheeler, physicist.

</div>

An adjustable forward and reverse performance of organic electronic devices is of essential relevance for the design of electric circuitries. In this chapter, different transport phenomena in organic pin-diodes under reverse voltage conditions are discussed and design rules for a control of reverse current are proposed. Furthermore, from the reverse capacitance of organic pin-diodes, important quantities of the junction as e.g. the distribution of electric field, the width of charge depletion zones, and the number of ionized dopant states are disclosed. The obtained field distribution serves as a starting point for a theoretical model which is used to describe the reverse breakdown behavior in organic pin-diodes by a field-assisted tunneling process from valence to conductance states of neighboring molecules.
Results presented within this chapter are reported in references [31, 51, 155]. The theoretical modelling of reverse breakdown is done by R. Gutierrez in cooperation with the group of Prof. Cuniberti from the Institute for Materials Science and Max Bergmann Center for Biomaterials in Dresden, Germany.

4.1 Reverse Current in Organic pin-Diodes for Low Electric Fields

Charge carrier transport in pin-diodes at reverse bias conditions can arise from either minority charge carrier diffusion, thermal generation of free charge carriers, direct leakage paths through the junction, or the reverse breakdown. The latter, as it is a high electric field phenomenon, is disregarded for the moment and will be discussed in Section 4.3.

The diffusion contribution is caused by diffusion of free charge carriers through the charge depletion zones of the counter side of the junction. They recombine in the neutral bulk region of the doped layers where they are minority charge carriers. Since this is a diffusion process, it is independent of the voltage and in consequence leads to a constant reverse current (reverse saturation). The magnitude of this reverse current is mainly governed by the diffusion constant of charges within the junction.

The second main contribution to reverse currents is given by thermal generation of free charge carriers within the depleted zones of the junction. This generation can either be a direct valence to conductance transition or it can be supported by inter-gap trap states, which is more likely in case of organic semiconductors that have typically an energy gap of $2-3eV$. The corresponding generation rate of free charge carriers and the associated current-voltage behavior can be found e.g. in Sze [6]. From this one can conclude that the generation process is not assisted by the applied electric field and the current depends only on the width of the charge depletion zones. According to Eq. 67 and as it will be discussed within Subsection 4.2, the depletion width scales with the square root of the voltage. Therefore, also a square root dependence is expected for the I-V behavior of generation currents.

The last component of reverse current is provided by direct leakage paths - a "short-cut" through the depleted zones of the junction. These paths can arise from e.g. metallic filaments or structural properties of the semiconductor (e.g. roughness spikes in the doped layers). Thus, these leakage paths exhibit a high specific conductivity. In particular, if the leakage paths are metallic filaments or paths of the doped semiconductors, they lead to an Ohmic I-V behavior.

In Figure 34 the three types of organic pin-diodes that are used to discuss reverse properties of pin-diodes are shown. These types are: wide gap pin-diodes, low gap pin-diodes, and low gap nip-diodes[36]. For three main reasons it is worth to distinguish between these different types. Firstly, it is expected that due to the difference in energy gap, the reverse currents can differ significantly for low and wide gap diode, and secondly, owing to the fact that low gap materials such as pentacene are poly-crystalline, influences of structural order on reverse voltage properties have to be taken into account. Therefore, for low gap diodes the pin- as well as the nip-layer sequence devices are investigated, while for amorphous wide gap materials this is not necessary. Thirdly, as summarized within the Tables 2 and 3, low gap materials typically have a significantly higher charge carrier mobility than wide gap materials.

In Figure 35 reverse current-voltage characteristics for these three types of diodes

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[36] Low gap material: the energy gap is in the range of visible light ($1.2-3eV$), e.g. pentacene and C_{60}. Wide gap material: the energy gap is larger than $3eV$
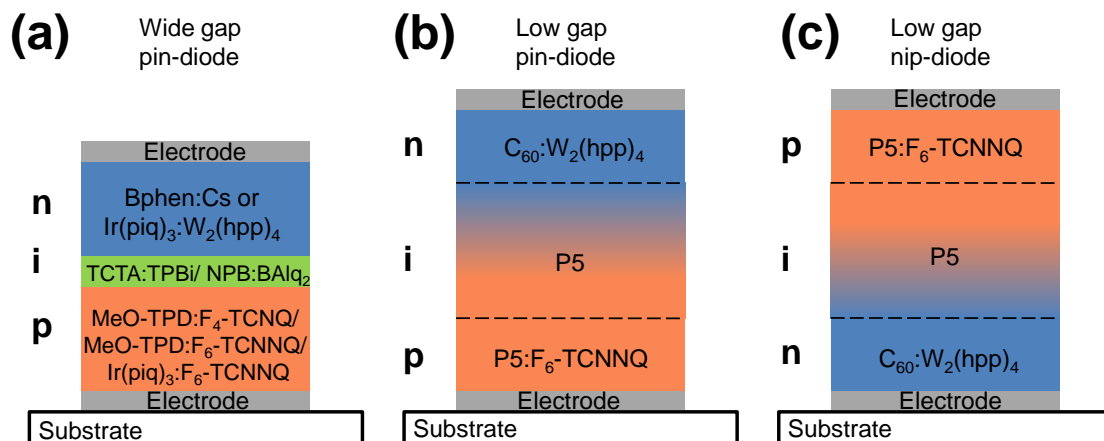
Figure 34: Overview on the three types of pin-diodes used for discussion. Typical matrix/dopant combinations for hole and electron transport layers (HTL/ETL) as well as typical materials for the intrinsic layer are shown. The device types are **(a)** wide gap pin-diodes, **(b)** low gap pin-diodes, and **(c)** low gap nip-diodes. The intrinsic layer in case of wide gap material has a thickness of typically $< 15nm$, while for low gap materials it is $> 50nm$. Moreover, owing to the poly-crystalline nature of pentacene the transition between the doped layers and the intrinsic layer is blurred.

are depicted. Apparently, all devices display an Ohmic current-voltage behavior at low voltages. To disclose whether the reverse current is dominated by leakage or by generation currents, layer conductivities, layer thicknesses, and in particular the width of the charge depletion zones have to be considered.

Since in reverse direction the applied voltage completely drops across the intrinsic layer and the charge depletion zones in doped layers, one can estimate from the leakage current level the conductivity of the intrinsic layer. For wide as well as for low gap pin-diodes, one can evaluate a conductivity of $10^{-10}...10^{-12}S/cm$. Even if this conductivity is small, it is above the expectations for an intrinsic organic semiconductor. Thus, this conductivity either arises from direct leakage paths (direct connection of the doped layers) or a thermal generation of charge carriers via inter-gap states in the intrinsic material. The latter would lead to a constant current since the generation rate is voltage independent. However, this is in contradiction to the experimental findings. Furthermore, to explain the magnitude of leakage current level one has to assume charge carrier generation rates of $> 10^8 s^{-1}$ which are physically unlikely for the energy gaps in such organic materials. Thus, the leakage current level is assumed to be caused by direct shunt paths.

The same argument can be applied when considering thermally assisted generation of charges within the charge depletion zones. The generation rates that would be required to explain the leakage current level are physically not plausible for the assumed energy gap. Additionally, also the ratio between the intrinsic layer thickness and the thickness of the charge depletion zones provides a strong argument against the importance of generation currents. The width of charge depletion zones in doped organic semiconductors is typically less than $10nm$ and more specifically they are usually thinner than $3nm$ for moderate and high dopant concentrations
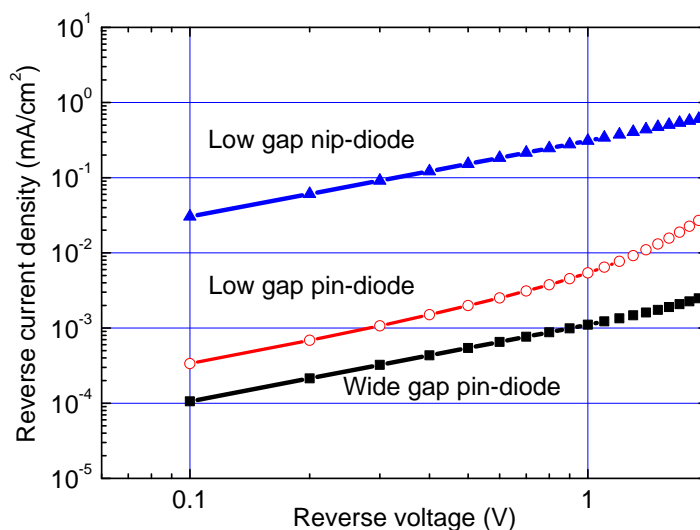
Figure 35: Current density in reverse voltage direct for a wide gap pin-diode (black rectangles), for a low gap pin-diode (red circles), and for a low gap nip-diode (blue triangles). The layer sequences are: Al(100nm)/ MeO-TPD:F$_6$-TCNNQ(50nm, 24.3$mol\%$)/ TCTA:TPBi(8nm, 1 : 1)/ BPhen:Cs(50nm)/ Al(100nm) for the wide gap pin-diode, Al(100nm)/ P5:F$_6$-TCNNQ(50nm, 0.8$mol\%$)/ P5(130nm)/ C$_{60}$:W$_2$(hpp)$_4$(50nm, 7.3$mol\%$)/ Al(100nm) for the low gap pin-diode, and Al(100nm)/ C$_{60}$:W$_2$(hpp)$_4$(50nm, 26.5$mol\%$)/ P5(110nm)/ P5:F$_6$-TCNNQ(50nm, 6.3$mol\%$)/ Al(100nm) for the low gap nip-diode.

as shown in the literature [40, 55] and discussed within the next subsection. Consequently, for a wide gap pin-diode with a 15nm thick interlayer or for a low gap junction with 100nm of intrinsic material, most of the reverse voltage drops across the intrinsic layer and not across the charge depletion zones. Hence, owing to these thin depletion zones, the weak voltage dependence, and owing to the expected low thermal generation rate of free charge carriers (caused by the large energy gap) generation current cannot be obtained for organic pin-diodes investigated within this thesis.

Another direct proof of the importance of direct leakage paths in organic pin-diodes can be found by the comparison of the low gap pin- and nip-diodes (see also Figure 35). The leakage current level is increased from pin- to nip-devices by a factor of 100. This presumably originates from the native roughness of pentacene thin-films (compare Section 5.1 or references [49, 60, 156]). If C$_{60}$ is deposited onto intrinsic pentacene, as in case of pin-diodes, C$_{60}$ smoothens the film topography which improves the interface formation and therefore reduces the probability for leakage paths. Contrarily, if a doped pentacene film is deposited onto intrinsic pentacene, as in case of nip-diodes, the layer roughness remains. This fact can e.g. cause direct shunt paths of doped semiconductor material or in the worst case metal penetration from the top contact through the intrinsic layer.

4.2 Reverse Capacitance of Organic pin-Diodes

Apparently, the analysis of reverse I-V behavior for low electric fields is not suitable to analyze charge depletion zones in organic materials. This is caused by the fact that generation currents and leakage currents are superimposed and the latter ones dominate the I-V performance in reverse direction.

However, impedance spectroscopy can help to face this problem since it allows to distinguish between Ohmic (leakage current) and capacitive (generation current) current contributions. In this context, the quantitative analysis of charge depletion zones by impedance spectroscopy is a powerful way to investigate the doping mechanism in organic semiconductor materials since the appearance of such depletion zones is a direct consequence of Poisson's equation in presence of free charge carriers.

In this subsection, the reverse voltage impedance response of organic pin-diodes is discussed. The investigation starts with organic hetero-diodes and is extended to homo-diodes for a quantitative analysis of concentration of ionized dopant states.

In a pn-diode as well as in a pin-diode, charge depletion zones are formed within the doped layers. Relying on Poisson's equation, the total width w_D^{tot} of the charge depletion zone is mainly governed by the density of dopant states, while the shape of the charge depletion zone is strongly influenced by the Debye length L_D within such system (compare Subsections 2.2.1 and 2.2.2). Within the abrupt junction approximation ($L_D << w_D^{e/h}$) with an entirely depleted intrinsic interlayer, the junction capacitance C_D is derived as (compare Eq.68 or reference [157])

$$C_D = \frac{\epsilon\epsilon_0 A}{w_D^{tot}} = \frac{\epsilon\epsilon_0 A}{\sqrt{w_I^2 + \frac{2\epsilon\epsilon_0}{q}\frac{(N_A+N_D)}{N_A N_D}(\Phi_{bi} - V)}}. \tag{68}$$

The validity of the abrupt junction condition can be confirmed by comparing the computed depletion width and the Debye length which is given by Eq. 41. This simple way of calculating the Debye length is rarely reported for organic semiconductors. This is presumably related to the fact that it does not take into account the structural disorder and the strong polaronic coupling in organic semiconductor materials. Thus, the estimation of Debye length is used for a qualitative comparison to the evaluated depletion width.

In a first step, before a quantitative impedance analysis can be done, the impedance response of organic pin-diodes has to be investigated with regard to a plausible equivalent circuit representation.

In Figure 36 the modulus and the phase of the complex impedance are displayed for a wide gap organic hetero pin-diode. For frequencies $f < 50kHz$, the phase remains at an angle of almost $-90°$ and the modulus obeys a $|\tilde{Z}| \sim 1/f$ relation. Hence, the impedance can be modeled by a single dominant RC-unit where the response is governed by the capacitor. The influence of the series resistance can be neglected. This situation warrants the validity of Eq. 112 to determine the capacitance of the diode which is shown in Figure 36(b). For frequencies $> 50kHz$ the series resistance of the device starts to dominate the impedance response. This can be seen in Figure 36(a) where the modulus of the impedance becomes fre-
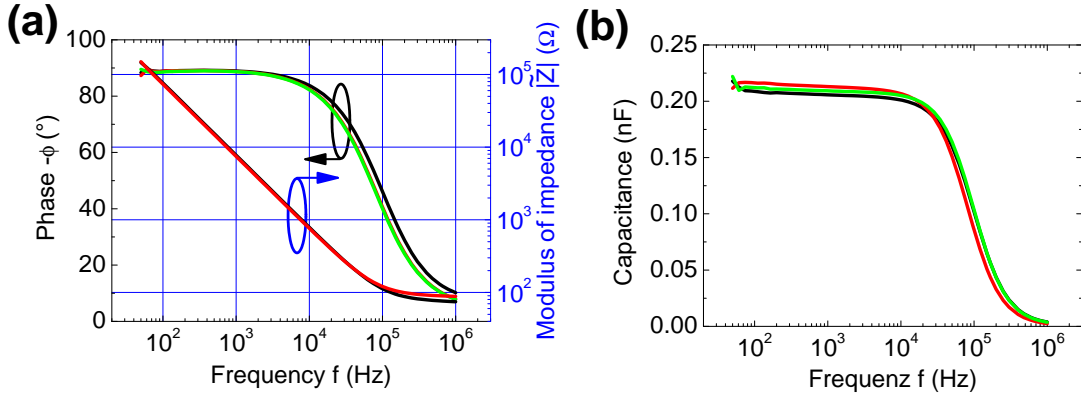
Figure 36: **(a)** Phase (left axis) and modulus of impedance (right axis) of an organic pin-diode for different reverse voltages. **(b)** Capacitance function calculated by Eq. 112 from the data shown in **(a)**. The diode contains: Al/ MeO-TPD:F_6-TCNNQ(6.5$mol\%$, 50nm)/ BAlq$_2$:NPB(1 : 1, 5nm)/ BPhen:Cs(50nm)/ Al. The colors denote the voltages as follows: $0V$ black, $-0.25V$ red, and $-0.5V$ green.

quency independent and the phase drops. Moreover, the capacitance function also becomes frequency dependent (compare Figure 36(b)) which precludes a quantitative analysis of the capacitance according to Eq. 112. However, the series resistance is not affecting the capacitance analysis performed at small frequencies ($f < 10kHz$). Another important property of the diodes that can be deduced from the impedance curves is that there are very little inter-gap trap states within the diode. This fact can be concluded from the constant capacitance function at low frequencies ($f < 1kHz$). Specifically, this means that all charges are able to follow the applied alternating voltage and therefore they can give a measurable contribution to the overall impedance. This exhibits an advantage of the pin-structure in comparison to other capacitance studies on organic diodes using MIS-capacitors, where interface states play an important role [158].

To validate the Mott-Schottky relation (Eq. 68) for organic pin-diodes, the specific interlayer thickness, dopant concentration, and voltage dependence of Eq. 68 have to be confirmed. It should be pointed out that the present study is the first systematic and quantitative study on the formation of charge depletion zones in organic pin-diodes. The appearance of such zones has been reported many times for intrinsic organic materials [158, 159]. However, these charge depletion zones in intrinsic materials can either arise from bulk trap states, interface trap states, or unintentional doping. For such a complex situation of distributed states in energy and space the capacitance response becomes frequency dependent which makes such studies often ambiguous [158] and therefore inappropriate for quantitative investigations. In case of doped organic semiconductors, MIS-capacitor structures are often used for evaluation of charge depletion zones [48, 160, 161]. Such MIS-structures are superior devices for impedance analysis since they are typically purely capacitive. However, MIS-structures have two substantial problems for analysis of charge depletion zones in organics. The capacitance of the depletion zone is in series to the capacitance of the insulator in the MIS-structure. Therefore, the capacitance value of the insulator has to be in the same range or
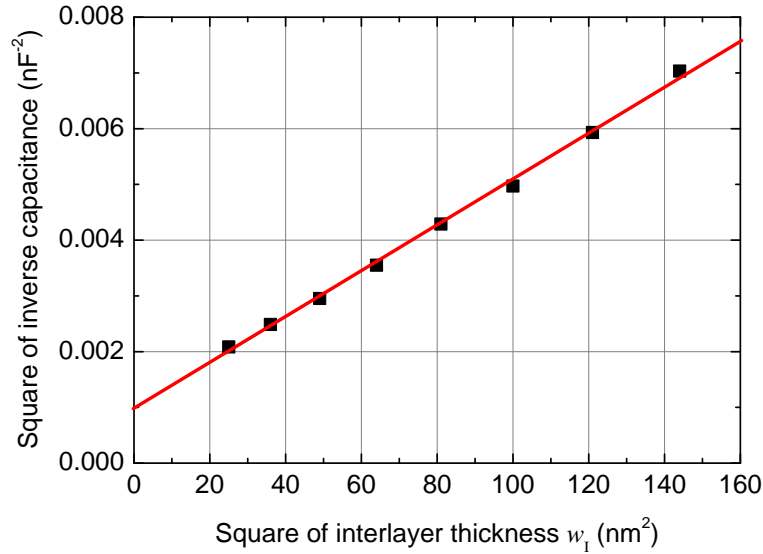
Figure 37: Square of the inverse capacitance over the square of the interlayer thickness (black dots) for thicknesses from $5nm$ to $12nm$. The layer sequence is described within the caption of Figure 36. The capacitance value is calculated from the frequency response at $0V$ and $1kHz$. Linear fit (red line) according to the prediction of the Mott-Schottky relation.

even larger than the depletion capacitance in order to be sensitive to the depletion capacitance. Since depletion zones in organic materials are typically thinner than $5nm$ [40, 44], the insulator thickness has to be in this range, or optional dielectric materials with a high dielectric constant have to be used. The second drawback of MIS-capacitors is given by the fact that states at the organic-insulator interface often give an additional complex contribution to the impedance response [158] which again precludes a quantitative analysis.

Thickness dependence of reverse capacitance: In order to demonstrate the applicability of a Mott-Schottky analysis to the capacitance of organic pin-diodes, the dependence of the capacitance on the interlayer thickness according to Eq. 68 has to be discussed. In Figure 37 the square of the inverse capacitance (assuming one dominant RC-unit, measured at $0V$, $1kHz$) is displayed against the interlayer thickness of the diode. In this graph, the interlayer thickness is systematically varied from $5nm$ to $12nm$ in the diode stack as described in the caption of Figure 36. The clear linear relation between the square of inverse capacitance and the square of interlayer thickness is a direct proof for Eq. 68. Hence, the intrinsic layer is completely depleted of free charge carriers. Moreover, the diode capacitance is smaller than the pure capacitance of the intrinsic layer. This fact suggests the presence of charge depletion zones in the doped charge transport layers. Furthermore, two other quantities can be derived from Figure 37. Firstly, the slope of this curve can be used to determine the dielectric constant of the material. The analysis provides a dielectric constant (assuming a uniform dielectric constant) of 2.8 ± 0.1. Secondly, from the intersection of the curve one can deduce the capaci-
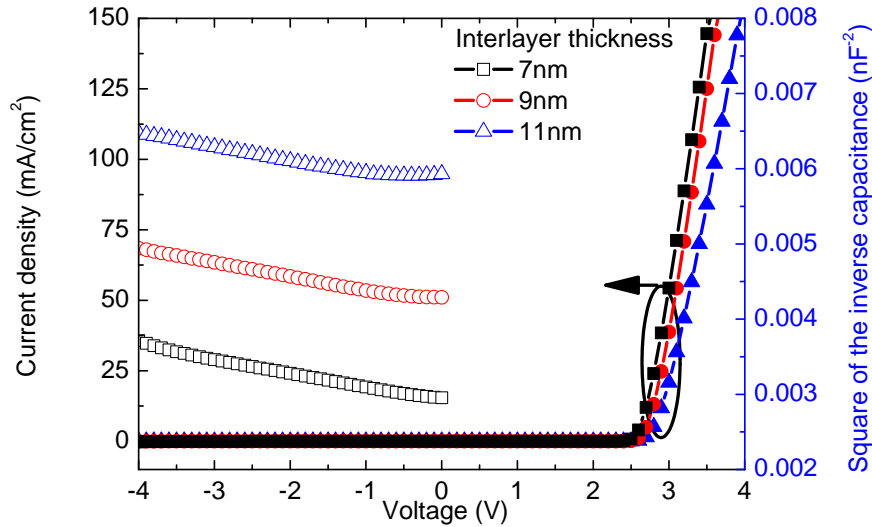
Figure 38: Current-voltage (closed symbols) and capacitance-voltage (Mott-Schottky plot, open symbols, measured at $1kHz$) curves of organic pin-diodes for different interlayer thicknesses of $7nm$ (black rectangles), $9nm$ (red circles), and $11nm$ (blue triangles). The diodes contain (compare Figure 36): Al/ MeO-TPD:F_6-TCNNQ($6.5mol\%$, $50nm$)/ BAlq$_2$:NPB($1:1$, xnm)/ BPhen:Cs($50nm$)/ Al.

tance in case of a missing interlayer. This capacitance originates from the charge depletion zones at the interface region between the transport layers and the intrinsic layer. Fitting leads to a capacitance of $(32 \pm 3)nF$. With this estimated dielectric constant, a total thickness of the charge depletion zones of $(4.8 \pm 0.5)nm$ can be derived which presents the sum of the n- and p-type charge depletion zone. Whether this depletion zone is larger on the p- or n-side cannot be decided here, but a systematic variation of the dopant concentrations on both sides can help to distinguish between them.

In Figure 38, I-V and C-V curves of these hetero diodes for different interlayer thicknesses are shown. The I-V performances of these devices are similar. In particular, in reverse direction the blocking behavior can be obtained even for very thin interlayer thicknesses of $7nm$. Also the forward direction (voltage $V > 0$) is only weakly influenced by the interlayer thickness and the current starts to raise at the same voltage independently of the interlayer thickness. Solely for large forward currents the interlayer thickness plays a role. This is caused by the fact that the intrinsic layer exhibits a series resistance in forward direction.

In contrast to the I-V curves, the C-V curves are strongly dependent on the interlayer thickness. The capacitance at $0V$ is governed by the interlayer thickness as also shown in Figure 37. The second interesting aspect is the linear increase of the capacitance function in the Mott-Schottky plot. This is in accordance to the behavior as predicted by Eq. 68, and most notably, as one can see in Figure 38, the slope of the capacitance function in reverse direction is independent of the interlayer thickness. Hence, Eq. 68 can be used to determine the built-in

potential of the diode as well as the concentration of ionized acceptor states. The built-in potential of these diodes can be obtained from the extrapolation of the Mott-Schottky curve to the intersection with the geometrical capacitance of the intrinsic layer. Its value is estimated to be $(2.9 \pm 0.3)V$. This value lies within the expectations for the energy gap of the employed material. Hence, if a pinning of the quasi-Fermi level to the conductance states is assumed, the built-in potential of these diodes is presumably close to the potential difference between valence and conductance states. The estimation of the density of ionized dopant states is more complex. In particular, the contributions of the p- and n-side are mixed up and it is not clear which side provides the dominant contribution to the overall capacitance.

Dopant concentration dependence of reverse capacitance: For a quantitative investigation of the voltage and dopant concentration dependence of the small signal impedance of organic pin-diodes, special homo-type diodes are used comprising the matrix material $Ir(piq)_3$. The homo pin-diode concept is beneficial for such quantitative studies because of the absence of interfacial energy barriers. The specific matrix material chosen here has the additional advantage of being n- and p-type dopable by the small molecule dopants $W_2(hpp)_4$ and F_6-TCNNQ, respectively. In particular, the controlled n-type doping is important, since in case of cesium doping the actual dopant concentration is hardly controllable and therefore only inaccurately known. Additionally, the special choice of material for the intrinsic layer hardly influences the formation of charge depletion zones in wide gap organic pin-diodes comprising amorphous thin-films. This arises from the fact that the interlayer is completely depleted of free charge carriers under reverse voltage conditions. Hence, the interlayer provides merely an additional capacitance contribution to the overall impedance, but it is not affecting the voltage or dopant concentration dependence of the reverse capacitance. Solely the absolute values of capacitance can differ owing to differences in dielectric constants.

In Figure 39 the C-f, I-V, and C-V curves of such an organic homo pin-diode comprising $Ir(piq)_3$ are depicted for different dopant concentrations in the hole transport layer. Again, the C-f curves show a distinct plateau of the capacitance function in the low frequency regime. The capacitance value of this plateau is decreasing if the dopant concentration is lowered. This behavior can be associated to the dependency of the width of the depletion zone on the dopant concentration. The lower the dopant concentration, the wider the depletion zone and hence, the lower the overall capacitance. For higher frequencies one can identify a drop of the capacitance function. This drop is related to the series resistance of the charge transport layers. Thus, the layer resistance of the hole transport layer is increased for lower dopant concentrations and therefore the drop of the capacitance function occurs at lower frequencies.

The current-voltage behavior of these homo pin-diodes is almost independent of the dopant concentration. Solely for large forward current densities one can observe an influence of the increased series resistance for the lowest dopant concentration. The C-V curves contain several characteristic features depending on the dopant concentration. The first point is the capacitance at $0V$. Here, the capacitance value is decreasing for decreasing dopant concentrations. This is caused by the changing extension of the charge depletion zones and their contribution to the
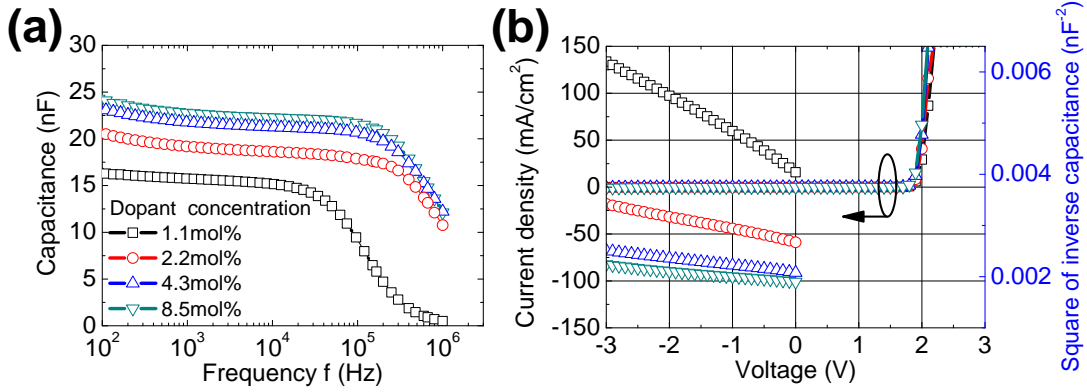
Figure 39: **(a)** Capacitance-frequency (C-f) at $0V$, **(b)** current-voltage (I-V, left axis, lines), and capacitance-voltage (C-V, Mott-Schottky plot, right axis, open symbols, measured at $500Hz$) curves of organic homo pin-diodes for different p-type dopant concentrations. The diodes contain: Al/ Ir(piq)$_3$:F$_6$-TCNNQ($x$mol%, $50nm$)/ Ir(piq)$_3$($7nm$)/ Ir(piq)$_3$:W$_2$(hpp)$_4$($14.3mol\%$, $50nm$)/ Al. The dopant concentrations in the HTL are $1.1mol\%$ (black lines and rectangles), $2.2mol\%$ (red lines circles), $4.3mol\%$ (blue lines and triangles), and $8.5mol\%$ (dark cyan lines and flipped triangles). The legend is valid for **(a)** and **(b)**.

Donor molecules ($mol\%$)	Acceptor molecules ($mol\%$)	N_A $10^{19}(cm^{-3})$	w_D^h (nm)	L_D (nm)	Doping efficiency N_A/N_A^0
14.3	8.5	14.32	1.3	0.2	0.64
14.3	4.3	9.47	2.5	0.2	0.85
14.3	2.2	5.27	4.6	0.3	0.95
14.3	1.1	1.74	7.5	0.5	0.63

Table 5: Results from fitting of data shown in Figure 40. Densities of active acceptor states N_A are calculated from the slope of the Mott-Schottky curves (assuming $\epsilon = 2.8$). N_A^0 denotes the density of deposited acceptor molecules and w_D^h is the width of the p-side depletion zone.

overall capacitance. The second aspect is that the slope of the $1/C^2$-curve can be controlled by the dopant concentration. This finding represents the final proof of Eq. 68.

The diodes shown in Figure 39 are designed as pin$^+$-junctions ($N_A << N_D$). In this way, employing a n-type dopant concentration of $14.3mol\%$, the depletion zone within the electron transport layer is assumed to be extremely thin ($< 0.5nm$). Hence, the n-side depletion has almost no contribution to the overall capacitance which is dominated by the capacitance of the intrinsic layer and the wider depletion zone within the hole transport layer. This allows to quantitatively derive the density of ionized dopant states, the width of the charge depletion zone, and the built-in potential.

The detailed Mott-Schottky plot of the organic homo pin-diodes is shown together with the extrapolation curves in Figure 40. The quantities derived from the slope of the Mott-Schottky curves and its intersection with the capacitance of the intrinsic layer are summarized in Table 5.
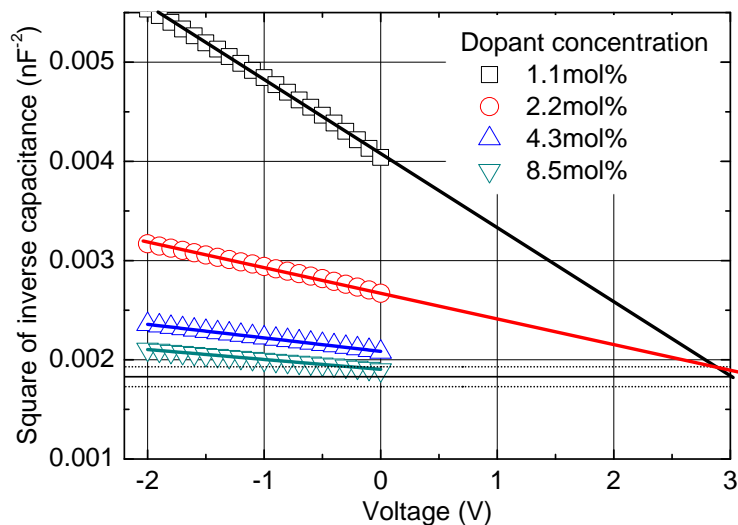
Figure 40: Capacitance-voltage curves (C-V) (Mott-Schottky plot, measured at $500Hz$) of organic pin^+-diodes for different p-type dopant concentrations. The layer sequence of the diodes is described within the caption of Figure 39. The doping concentrations in the HTL are $1.1mol\%$ (black rectangles), $2.2mol\%$ (red circles), $4.3mol\%$ (blue triangles), and $8.5mol\%$ (dark cyan flipped triangles). Colored lines show fitting results. The black line indicates the expected geometrical capacitance. The dotted lines are the standard deviations from the geometrical capacitance due to the uncertainty of the used values for relative permittivity.

The density of ionized acceptor states evaluated from the slope of the Mott-Schottky curves is in good agreement with the chosen dopant concentrations. In particular, the estimated doping efficiency is in the range of $64-95\%$ which suggests a rather efficient doping process. The error of fitting provides a negligible uncertainty for the number of ionized acceptor states. It remains unclear whether the variations in doping efficiency are related to a substantial physical mechanism or if they are caused by experimental inaccuracies of the chosen dopant concentration. One possible explanation for the lower doping efficiency at $1.1mol\%$ and $8.5mol\%$ might be given by the fact that for low dopant concentrations, a certain amount of free charges is required to fill up native trap states within the charge transport material. This would lead to a significant lowering of the density of free charges available for transport. For $8.5mol\%$ of p-type doping the assumption of a pin^+-junction is likely violated. Hence, if the condition $N_D >> N_A$ is not fulfilled, donor states contribute to the slope of the Mott-Schottky curve which leads to an underestimation of N_A.

The width of the p-side charge depletion zone w_D^h can be determined from the capacitance at $0V$. The extension of this zone varies between $7nm$ and $1.3nm$ for $1.1mol\%$ and $8.5mol\%$ of F_6-TCNNQ. With this knowledge one can compare the extension of this zone and the Debye length. As summarized in Table 5, the Debye length is significantly smaller than the depletion zone width which justifies

the assumption of an abrupt junction.

The last quantity that can be derived from the Mott-Schottky curves is the built-in potential. A value of $(2.9 \pm 0.5)V$ is determined from the intersection with the geometrical capacitance. This analysis is only possible for low dopant concentrations ($1.1mol\%$ and $2.2mol\%$) since the small slope for higher concentrations and the uncertainty of the capacitance of the intrinsic layer leads to large discrepancies. Nevertheless, relying on a high doping efficiency, the quasi-Fermi level is presumably pinned to the transport states of the matrix material. Therefore, the built-in potential is expected to be close to the potential difference between valence and conductance states of $\sim 2.6...2.7V$.

With knowledge of the built-in potential, the density of ionized dopant states, and the thickness of the intrinsic layer, the pin-diode is fully characterized in terms of its electrostatic properties. Moreover, from the extremely thin charge depletion zones it can retrospectively be justified that generation currents are typically not observed in the reverse I-V behavior of organic pin-diodes. The width of these depletion zones is too small to provide sufficient charge carriers to overcome the leakage current level which is given by direct Ohmic leakage paths.

Doping efficiency: An interesting outcome of this study on charge depletion zones is the observed extremely high doping efficiency. These high values being close to unity are in agreement to Fourier Transform Infrared Spectroscopy (FTIR) measurements on the matrix/dopant system zinc phthalocyanine (ZnPc)/F_4-TCNQ [162]. However, they are in contradiction to reports on doping of organic semiconductors by transition metal oxides (e.g. MoO_3) where doping efficiencies of typically $< 10\%$ have been reported [48, 161, 163]. These low doping efficiencies can be partially explained by a segregation and clustering of dopants. However, also for molecular dopants (F_4-TCNQ) rather low doping efficiencies of less than 10% have been reported [44, 161] using ultraviolet photoelectron spectroscopy.

There are several important differences between the technique of impedance spectroscopy used here and the photoelectron spectroscopy investigations. In particular, in case of impedance spectroscopy, the amount of ionized dopant states is determined by applying an electric field to the sample. This field and the built-in potential (typical field strength of $\sim 1MV/cm$) can support the dissociation of charge-transfer-complexes leading to a higher doping efficiency. Furthermore, there are systematic drawbacks of the photoelectron spectroscopy technique. Since the organic material is deposited layer-by-layer for the spectroscopic analysis, trap states related to adsorption of water and oxygen can strongly influence the formation of the charge depletion zones. Moreover, to mathematically derive the Mott-Schottky relation, a semi-infinite device structure is required. This means, the charge transport layer has to be significantly thicker than the charge depletion zone. This requirement, however, is not fulfilled in case of layer-by-layer deposited devices for UPS studies (compare [44]). The lower doping efficiencies determined by UPS are presumably a consequence of these two effects. Nevertheless, it is the intention of ongoing work to explain impedance spectroscopy and UPS findings in a combined picture. For the present matrix/dopant combination, the high efficiency of the doping process can likely be attributed to the strong acceptor material F_6-TCNNQ. Owing to its low LUMO level the formation of charge-transfer-complexes
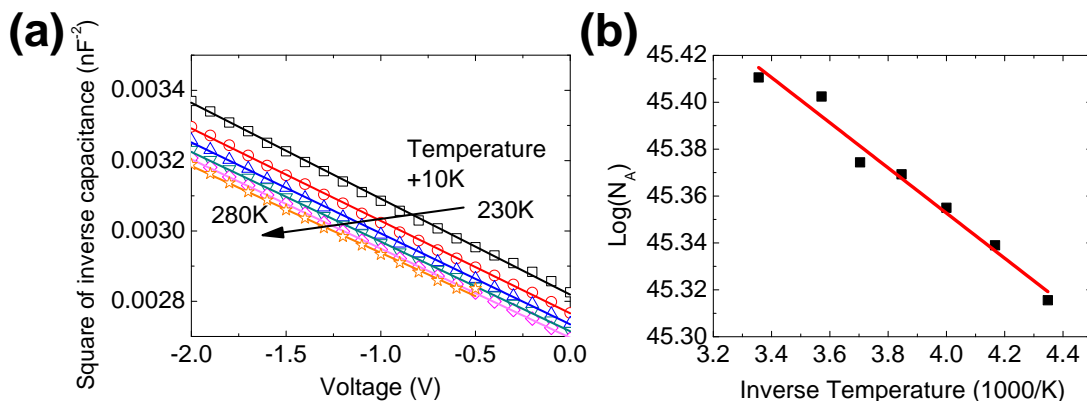
Figure 41: (a) Temperature dependent Mott-Schottky plot curves and **(b)** the density of ionized acceptor states (N_A) in an Arrhenius-plot for organic homo pin-diodes. The layer sequence of the diodes is described within the caption of Figure 39. The dopant concentrations in the HTL is $4.3 mol\%$ (blue). The lines represent fitting curves.

is enhanced. However, this is not necessarily equivalent to a high dissociation probability of CT-complexes. Hence, it is worth to study the thermal activation of the doping process.

Figure 41 shows the measured C-V data for organic homo pin-diodes at different temperatures exemplary for one dopant concentration. As it can be seen in Figure 41(a), the absolute value of capacitance and the slope of the Mott-Schottky curve varies with temperature. The change in the slope can directly be linked to the activation of the doping process. The higher the temperature, the more shallow the Mott-Schottky curves which means that more dopants are ionized and contribute to the capacitance. The changing absolute value of capacitance is also related to the activation process: the more dopants are ionized, the thinner the charge depletion zone and hence the larger the depletion capacitance that occurs. The density of ionized acceptor states determined from Figure 41(a) is displayed in 41(b). An Arrhenius-like activation process can be observed that allows to extract an activation energy of $\sim 10 meV$.

Figure 42 summarizes the temperature dependent measurements for different p-type dopant concentrations. A clear Arrhenius-like behavior can be obtained for all dopant concentrations and in all cases the evaluated activation energy is low ($< 12 meV$). The variations for different doping concentrations presumably lie within the range of experimental uncertainties. The temperature dependence of dopant activation for the present matrix/dopant system provides clear evidence for an efficient doping process with very low activation energies where all dopants are ionized at room temperature. This regime is known as the saturation regime of doping. Moreover, it can be deduced that dopant molecules act as shallow acceptor states and particularly not as deep Coulomb trap states.

To demonstrate that the concept of Mott-Schottky analysis for organic pin-diodes can also be applied to the n-side, Figure 43 shows the impedance analysis for a variation of n-type doping. Similar conclusions as for the p-type doping can be drawn from the C-f, I-V, and C-V curves. However, a quantitative analysis for
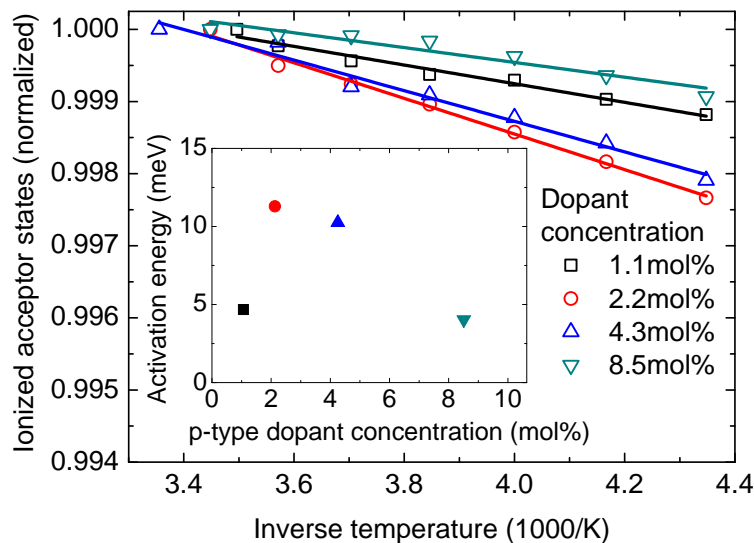
Figure 42: Number of ionized acceptor states normalized to its room temperature value (see Tab.5) for different p-type doping concentrations. The layer sequence of the diodes is described within the caption of Figure 39. The dopant concentrations in the HTL are $1.1mol\%$ (black rectangles), $2.2mol\%$ (red circles), $4.3mol\%$ (blue triangles), and $8.5mol\%$ (dark cyan flipped triangles). Colored lines show fitting results. The inset shows in the corresponding colors the activation energy of the ionized acceptor states.

the number of ionized donor states cannot be done here since the diode is not designed as a p^+in-junction ($N_A >> N_D$). Instead, another feature of the n-type doping variation should be highlighted here. A second plateau appears in the C-f curves for $0.9mol\%$ and for $3.5mol\%$ of $W_2(hpp)_4$ (see Figure 43(a)). In case of $0.9mol\%$ of dopants the second plateau cannot be reached within the frequency range. Hence, despite the low activation energy, the number of free charge carriers within the n-type doped layer is low and the layer resistance starts to play an important role for the impedance analysis. The same trend can in principle also be seen for low p-type dopant concentrations (compare Figure 39(a)). However, this does not necessarily imply that the doping efficiency for n-type doping is lower than for p-type doping, but it could rather mean that the number of electron trap states is larger than for holes and therefore more dopants have to supply free charge carriers to fill up these trap states. For $3.5mol\%$ of n-type doping the second plateau almost vanishes which means that the number of free charge carriers in the n-type doped layer is significantly higher than the density of electron trap states.

Reverse capacitance of low gap pin-diodes: To complete the studies on the reverse capacitance behavior of organic pin-diodes, finally pin-diodes comprising low gap material have to be investigated. There are two main differences between wide gap and low gap diodes that are important: (1) the intrinsic layer for low gap
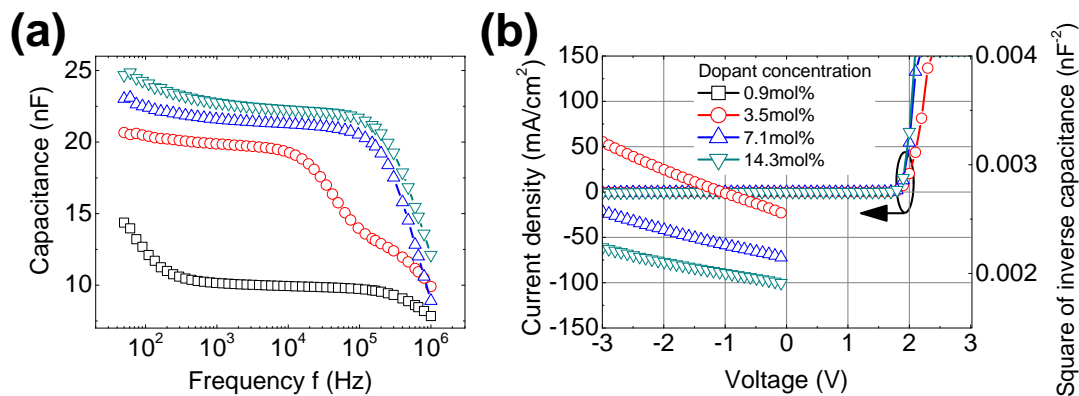
Figure 43: (a) Capacitance-frequency (C-f) at $0V$, **(b)** current-voltage (I-V, left axis, closed symbols), and capacitance-voltage (C-V, Mott-Schottky plot, right axis, open symbols, measured at $500Hz$) curves of organic homo pin-diodes for different n-type dopant concentrations. The diodes contain: Al/ Ir(piq)$_3$:F$_6$-TCNNQ($8.5mol\%$, $50nm$)/ Ir(piq)$_3$($7nm$)/ Ir(piq)$_3$:W$_2$(hpp)$_4$($xmol\%$, $50nm$)/ Al. The dopant concentrations in the ETL are $0.9mol\%$ (black lines and rectangles), $3.5mol\%$ (red lines and circles), $7.1mol\%$ (blue lines and triangles), and $14.3mol\%$ (dark cyan lines and flipped triangles). The legend is valid for **(a)** and **(b)**.

diodes comprising poly-crystalline materials such as pentacene has to be typically $> 50nm$ to guarantee a sufficient blocking of reverse currents, and (2) owing to the polycrystalline structure of e.g. pentacene, layer thicknesses have to be treated as effective values which is caused by the roughness of such films.

In Figure 44 the modulus of the impedance and the capacitance of a low gap organic pin-diode are shown for different reverse voltages. The modulus vs. frequency graph shows two slopes. For frequencies $> 10kHz$ the modulus follows $|\tilde{Z}| \sim 1/f$, while for low frequencies ($f < 10kHz$) the impedance follows a $|\tilde{Z}| \sim (1/f)^n$, $n < 1$ behavior. The low frequency behavior will be explained by a general equivalent circuit model for these diodes within Section 5.2.2. The important part of the impedance spectrum for capacitance analysis is the high frequency part. Here, a simple RC-unit can be used to compute the capacitance of the device as it is shown in Figure 44(b). This capacitance function shows a plateau and the capacitance value is given by the geometrical capacitance of the intrinsic layer [148]. As also shown in Figure 44(b), a voltage dependence of the reverse capacitance cannot be observed. However, this does not imply that no charge depletion zones are present. The "missing" voltage dependence of the reverse capacitance is related to the fact that the geometrical capacitance ($\sim 3nF$) is significantly smaller than the expected depletion capacitance ($\sim 15nF$). Hence, according to the series connection of both capacitors, a change of the total reverse capacitance caused by the voltage dependence of the depletion of less than $100pF$ is expected. However, this cannot be resolved by the impedance spectrometer. Thus, a Mott-Schottky analysis of charge depletion zones for low gap pin-diodes is not feasible.

Nevertheless, the geometrical capacitance of the intrinsic layer can be determined in order to estimate the specific dielectric constant of pentacene. Figure 45 displays the capacitance vs. interlayer thickness behavior and the fitting curve according

(a)

(b)
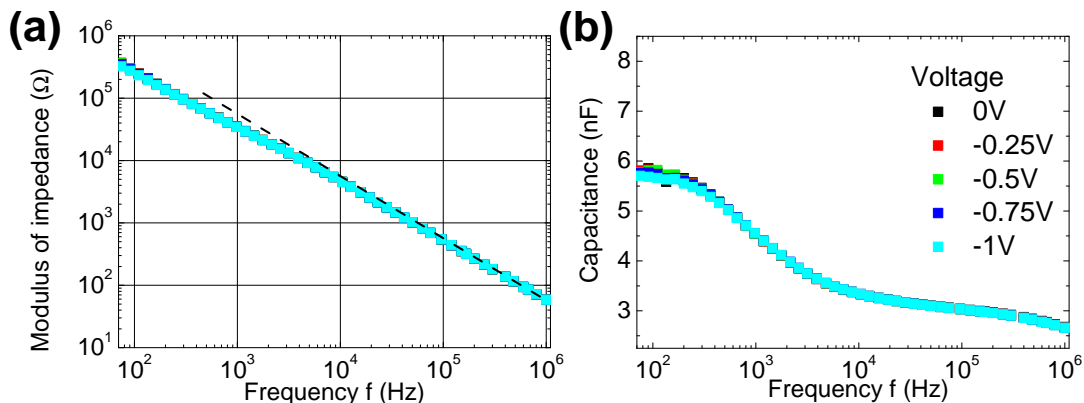
Figure 44: **(a)** Modulus of impedance of an organic low gap pin-diode for different reverse voltages. The dashed curve represents a slope of one as expected for a RC-unit. **(b)** Capacitance function calculated by Eq. 112 from the data shown in **(a)**. The diode contains: Al/ P5:F$_6$-TCNNQ(0.8$mol\%$, 50nm)/ P5(110nm)/ C$_{60}$:W$_2$(hpp)$_4$(0.8$mol\%$, 50nm)/ Al. The color code for reverse voltage value is valid for **(a)** and **(b)**.
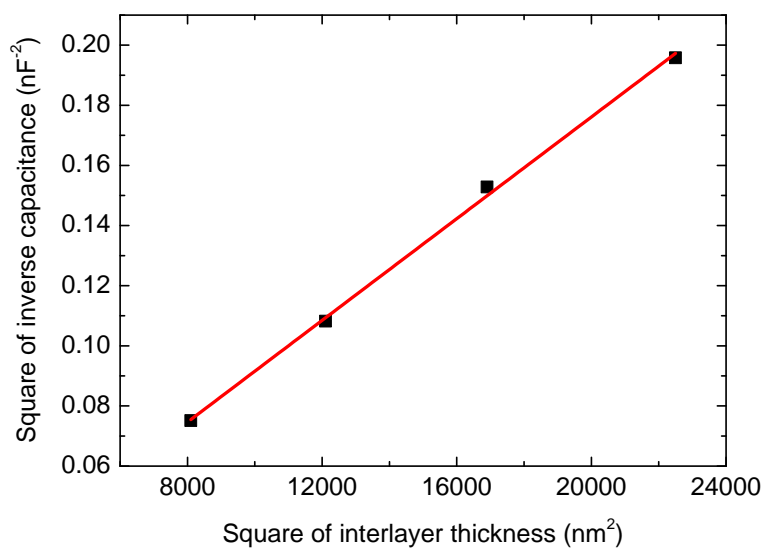
Figure 45: Square of the inverse capacitance over the square of the interlayer thickness (black dots) for thickness from 90nm to 150nm. The layer sequence is described within the caption of Figure 44. The capacitance is calculated from the frequency response at 0V. Linear fit (red line) according to the prediction of the Mott-Schottky relation.

to Eq. 68. From the slope of this curve the dielectric constant of pentacene can be extracted as $\epsilon = (6.1 \pm 0.3)$[37]. However, it should be noted that the dielectric constant of pentacene strongly depends on the layer morphology and hence on the

[37] The dielectric constant of pentacene reported in the literature [60, 164] varies between $4-6$. These large deviations are presumably related to the influence of the substrate and the deposition conditions on the growth of pentacene crystallites.

deposition conditions. Furthermore, the capacitance of the depletion zones can be determined from the intersection of the fitting curve in Figure 45. In this case, the depletion capacitance is $(13 \pm 2)nF$ which allows to calculate the depletion width as $(24 \pm 4)nm$. This width exhibits the sum of the p- and n-side depletion width and lies in the expected range since the dopant concentrations within the hole and electron transport layer is low.

4.3   Reverse Breakdown in Organic pin-Diodes

Within this section, the discussion on the reverse voltage behavior of organic pin-diodes is focused on the high electric field range. Initially, wide gap diodes are considered. In a second step, the investigations are extended to low gap junctions. The experimental findings can be quantified and generalized for both material systems which allows for a first theoretical approach to describe the obtained phenomena.
The present study exhibits the first systematic work on the breakdown behavior of organic diodes.

4.3.1   Wide-gap Organic Zener Diodes

In Figure 46, the I-V curves for wide gap organic pin-diodes for different interlayer thicknesses are depicted. The interlayer thickness neither influences the slope nor the onset of current in forward direction[38]. In reverse direction, however, a reversible breakdown of the junction can be observed and the breakdown voltage is tunable by the interlayer thickness. Such a breakdown presumably originates from a tunneling process from valence to conductance states of neighboring molecules. This mechanism is known as Zener-breakdown [165]. Another possible mechanism of reverse breakdown is the avalanche breakthrough [166]. In the following, the field and temperature dependence of the breakdown are discussed in detail.
Besides Ohmic leakage currents for low reverse voltages, the entire reverse direction of the I-V curve is dominated by an exponential current rise. This fact provides a strong hint for a tunneling-like transport mechanism. Another indicator for a field assisted tunneling process is the thickness dependency of the breakdown. As shown in Figure 46, the breakdown voltage shifts by $1V$ for each additional nanometer of interlayer. Since impedance measurements revealed that the intrinsic layer is entirely depleted of free charge carriers in reverse direction, it can be deduced that the complete interlayer acts as a tunneling barrier which is an important information for theoretical modeling of the breakdown. The flattening of reverse current for large reverse voltages should not be interpreted as a feature of the breakdown, but should rather be seen as a limitation of current that arises from the charge transport layers.
The extremely strong and sharp dependency of reverse current on the interlayer thickness within the exponential part of the I-V curve is summarized in Figure 47.

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[38]Small differences for ultra-thin $(5nm)$ interlayer samples can occur for low forward voltages. An incomplete film coverage by such thin layers might cause direct leakage paths.
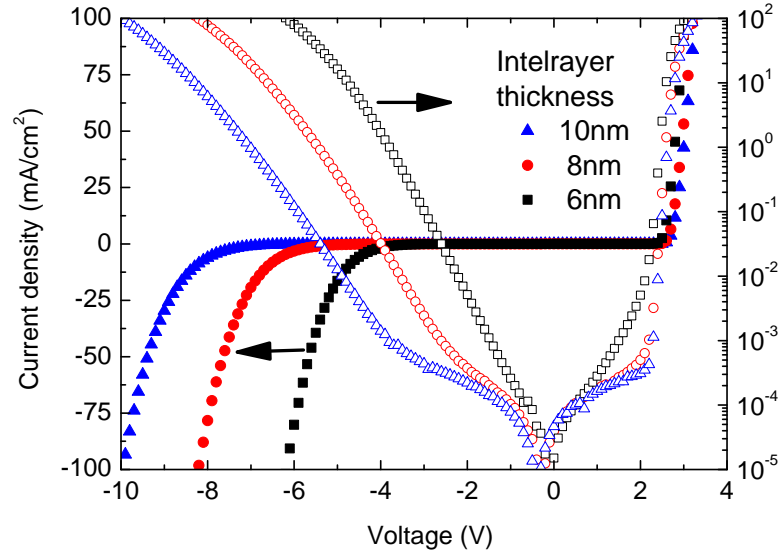
Figure 46: Current-voltage characteristics for different interlayer thicknesses in linear (closed symbols) and logarithmic (open symbols) current scale. The wide gap pin-diodes consist of: Al($100nm$)/ MeO-TPD:F$_4$-TCNQ($8.1mol\%, 50nm$)/ Balq$_2$:NPB($1 : 1$, xnm)/ BPhen:Cs($50nm$)/ Al($100nm$). The interlayer thicknesses are $6nm$ (black rectangles), $8nm$ (red circles), and $10nm$ (blue triangles).

Here, a considerable change of reverse current by almost five orders of magnitude can be observed if the interlayer thickness is varied from $5nm$ to $11nm$. As mentioned before, the reverse behavior of pin-diodes is widely independent of the special choice of intrinsic material in case of amorphous wide gap materials. This point has to be seen as a direct consequence of the extreme interlayer thickness dependence of reverse current where minute variations in layer thickness can lead to significant changes in breakdown current.

Another way to probe the breakdown behavior is its temperature dependency. For inorganic materials the Zener-mechanism is clearly distinguishable from the avalanche breakthrough by the sign of its thermal activation energy [6]. The probability for avalanche multiplication is increased for lower temperatures, while the current caused by a Zener-like mechanism increases for higher temperatures. However, in case of organic semiconductors where charges are widely localized on molecular sites, this argumentation concerning avalanche multiplication is not obvious. Nevertheless, the temperature dependence can provide an important insight to the underlying process of charge carrier transport.

In Figure 48, the current in forward and reverse direction for different temperatures and voltages is shown. Most notably, a strong difference in activation between forward and reverse currents can be obtained. While in reverse direction an activation energy of $(30 \pm 10)meV$ is observed independently of the applied voltage (compare Figure 48(b)), the forward direction exhibits a pronounced ac-
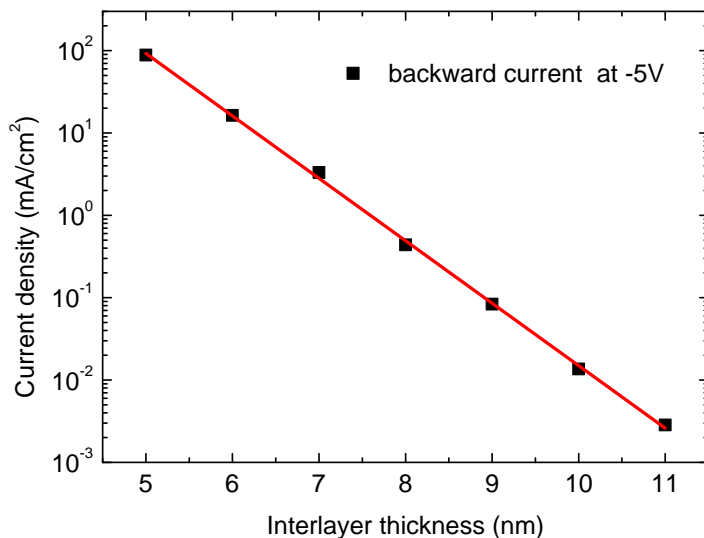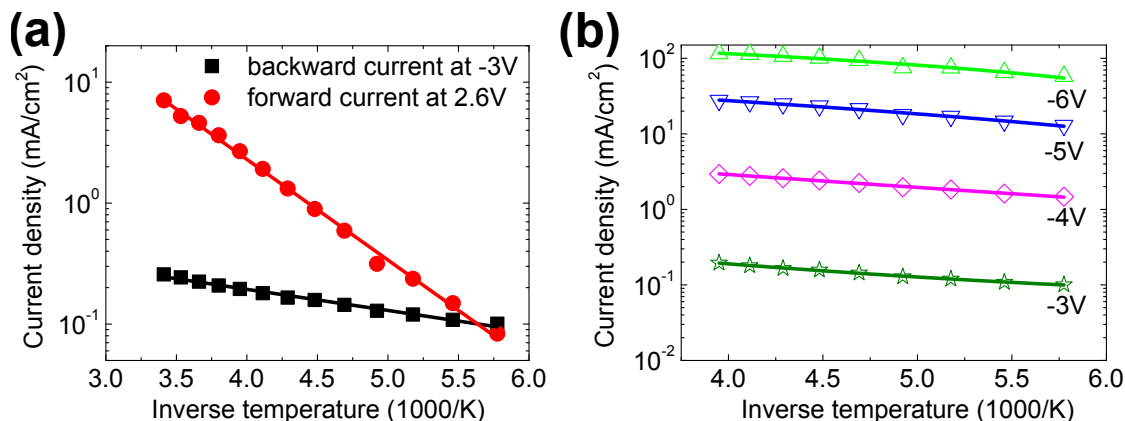
Figure 47: Current density at a reverse voltage of $-5V$ for different interlayer thick-
nesses $(5-11nm)$. The layer sequence is described within the caption
of Figure 46. The red line is a linear fit of the data points.

tivation energy of $(170 \pm 20)meV$ for comparable current densities as in reverse
direction. This result clearly indicates a substantial difference between forward
and reverse currents. The activation process in forward direction can be associ-
ated to a hopping-like transport within an extended density of states. Contrary to
this, the low activation energy within the breakdown suggests a transport mech-
anism which occurs in a small range of energies where the energetic alignment of
molecular sites plays a crucial role for charge transport.

As proposed by the impedance analysis of pin-diodes, the intrinsic layer is only
one part of the active region in a diode. The second part is given by the charge
depletion zones formed within the doped layers. Hence, the effective width of the
tunneling barrier is the sum of these two parts. In this context, it can be deduced
that a control of reverse current by modification of these depletions zones, namely
the dopant concentrations, is feasible.
The I-V behavior of homo pin-diodes including the breakdown regime are shown
in Figure 49 for different dopant concentrations. As predicted, the breakdown
voltage can be tuned by the dopant concentration for both p- and n-type doping.
In summary: the higher the dopant concentration, the thinner the depletion zone,
and the lower the breakdown voltage. To prove the dependencies of the suggested
mechanisms for the depletion zone formation and the reverse breakdown, one can
compare the breakdown and the dopant concentration as displayed in Figure 50.
As shown (compare Figure 47), the breakdown current is proportional to the ex-
ponent of the tunneling barrier width. Furthermore, the width of the depletion
zones is proportional to the square root of inverse dopant concentration. Besides
a linear relation between the logarithm of breakdown current and the square root
of inverse dopant concentration is expected within this model. The experimental

Figure 48: (a) Temperature dependence of current density in reverse direction measured at $-3V$ and in the exponential rise of the forward direction at $2.6V$. **(b)** Temperature dependence of current for different reverse voltages. The device consists of Al($100nm$)/ MeO-TPD:F$_6$-TCNNQ($6.5wt\%, 50nm$)/ Balq$_2$:NPB($1 : 1, xnm$)/ BPhen:Cs($50nm$)/ Al($100nm$). The lines indicate the Arrhenius-like behavior.

behavior, as shown in Figure 50, nicely fulfills this prediction. Moreover, the similar slope for p- and n-type doping allows to conclude that the efficiency of doping is not changing with dopant concentration for both dopant species. This finding confirms also the results on doping efficiency presented in Table 5.

4.3.2 Low-gap Organic Zener Diodes

Since the reverse breakdown is a process driven by the electric field, the energy gap of the interlayer material is a key parameter that defines the breakdown condition. In this context, a lower electric breakdown field is expected for low gap diodes. A second important parameter that affects the breakdown condition is the layer morphology. Especially in case of poly-crystalline pentacene as an intrinsic material, layer roughness and layer sequence have a considerable influence on the breakdown regime. To account for this effect, differences between pin- and nip-devices are discussed.

The control of reverse breakdown voltage for low gap organic pin-diodes is a key parameter in order to design organic diodes for ultra-high-frequency applications. Consequently, an optimized thickness of the interlayer has to be determined with regard to the trade-off between forward resistance, rectification ratio, and reverse breakdown voltage (compare Section 5.3).

In Figure 51, I-V curves for low gap nip- and pin-diodes are summarized for different interlayer thicknesses of pentacene. Moreover, the reverse current-voltage regime is highlighted in Figure 51(c) and (d). As also observed for wide gap diodes, the slope and the onset of current in forward direction are weakly affected by the choice of interlayer thickness. The current starts to rise at a rather low voltage $(0.2-0.4V)$ in comparison to the wide gap diodes (see e.g. Figure 46)). This effect is caused by the difference in charge carrier mobility for both types of materials.
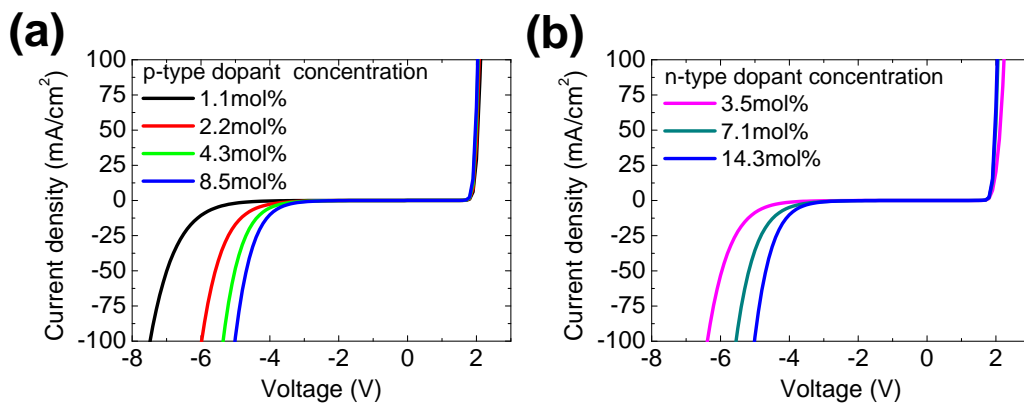
Figure 49: Current-voltage curves of homo pin-diodes for different **(a)** p- and **(b)** n-type dopant concentrations. The devices consist of Al/ Ir(piq)$_3$:F$_6$-TCNNQ(x%, $50nm$)/ Ir(piq)$_3$($7nm$)/ Ir(piq)$_3$:W$_2$(hpp)$_4$($ymol$%, $50nm$)/ Al. For **(a)** p-type dopant variation the n-type dopant concentration is $14.3mol$% and the colors denote a p-type concentration of $1.1mol$% (black), $2.2mol$% (red), $4.3mol$% (green), and $8.5mol$%(blue). For **(b)** n-type dopant variation the p-type dopant concentration is $8.5mol$% and the colors the denote a n-type concentration of $3.5mol$% (magenta), $7.1mol$% (dark cyan), and $14.3mol$% (blue).

For low reverse voltages an Ohmic leakage current, indicated in Figure 51(c) and (d)), can be observed which is slightly affected by the interlayer thickness. This feature is related to the fact that leakage currents arise from direct conductive paths through the intrinsic layer. Hence, even if in general the probability for such paths is lowered for thicker interlayers, in a certain range of layer thickness (e.g. in the range of layer roughness, or for a crucial thickness required for a closed layer coverage) the formation of leakage paths is almost independent of the interlayer thickness. For large reverse voltages a reversible breakdown is observed where the breakdown voltage is again controllable by the interlayer thickness. The general character of the breakdown mechanism seems to be the same for pin- and nip-devices. However, there are specific differences in reverse breakdown voltage and in the transition behavior from the leakage to the breakdown regime. Both features can be explained by the morphology of the intrinsic pentacene film. The transition from the leakage to the breakdown regime in case of nip-diodes is sharp which suggests a rather defined formation of interfaces between the doped layers and the intrinsic layer. For pin-diodes, this transition is continuous and smooth. This difference can be explained by the layer sequence. In nip-devices, n-type doped C$_{60}$ is deposited onto the rough intrinsic layer of pentacene which leads to a penetration of doped C$_{60}$ into the intrinsic layer. Thus, the effective intrinsic layer thickness is likely reduced and its value is blurred owing to the mixing of both films [49, 60, 156]. This hypothesis of a blurred value of layer thickness is also confirmed by the observed breakdown voltages. As shown in Figure 51, significantly higher breakdown voltages are obtained for nip-diodes than for pin-devices. Therefore, since an equivalent energy diagram can be assumed, the effective interlayer thickness has to be less for pin-diodes than in case of nip-devices.
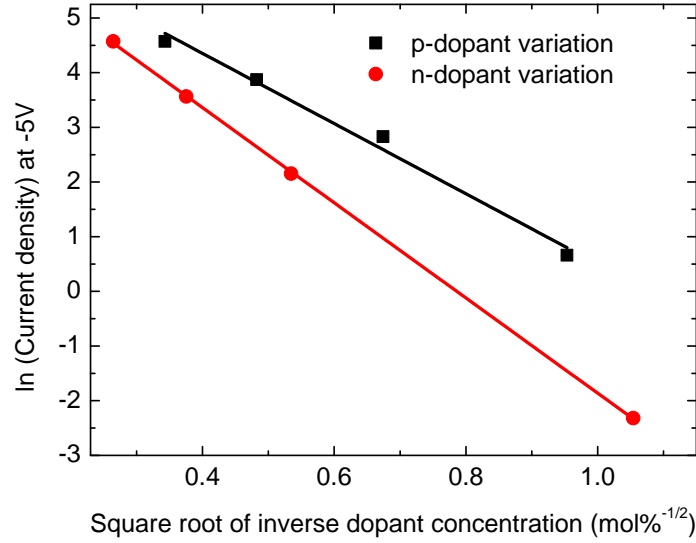
Figure 50: Reverse current at $-5V$ for different n- and p-type dopant concentra-
tions. The device structure is described in Fig.49. For n-type dopant
variation (red circles) the p-type dopant concentration is $8.5mol\%$. For
p-type dopant variation (black dots) the n-type dopant concentration
is $14.3mol\%$.

To show the general accordance of the breakdown mechanism for wide and low
gap materials, the dependency on electric field and temperature has to be investi-
gated.

The dependency of reverse current on the electric field is shown in Figure 52. If
the reverse current, taken from Figure 51(c), is plotted versus the electric field, the
transition from the leakage to the breakdown regime appears independently of the
interlayer thickness at a electric field of $\sim 1...1.5MV/cm$ (depending on whether
pin- or nip-devices are considered). Hence, the breakdown condition is defined by
the applied electric field. The exponential relation between reverse current and
interlayer thickness is depicted in Figure 52(b). As indicated in this graph, the
reverse current follows an exponential relation to the electric field. The slopes of
the exponential curves are different for pin- and nip-devices. In particular, the
curve for nip-device is steeper. This aspect results from the fact that the inter-
layer thickness for pin-devices is overestimated owing to penetration of C_{60} into
the intrinsic layer.

To compare the breakdown behavior of wide gap and low gap junctions, it is worth
to discuss the breakdown fields with respect to the energy gaps of the materials.
For wide gap diodes a breakdown field of $\sim 3MV/cm$ (compare e.g. Figure 46)
is obtained, while a value of $\sim 1...1.5MV/cm$ is concluded for low gap junctions.
Assuming a triangular barrier, as a first approximation to describe the breakdown
mechanism, a relation between electric breakdown field $\mathcal{E}_{BD}$ and energy gap E_G
according to $\mathcal{E}_{BD} \sim E_G^{3/2}$ is expected[157]. Relying upon this relation, a factor of
approximately 2 in electric breakdown field is predicted for low gap and wide gap
junctions which is in accordance to the experimental findings.
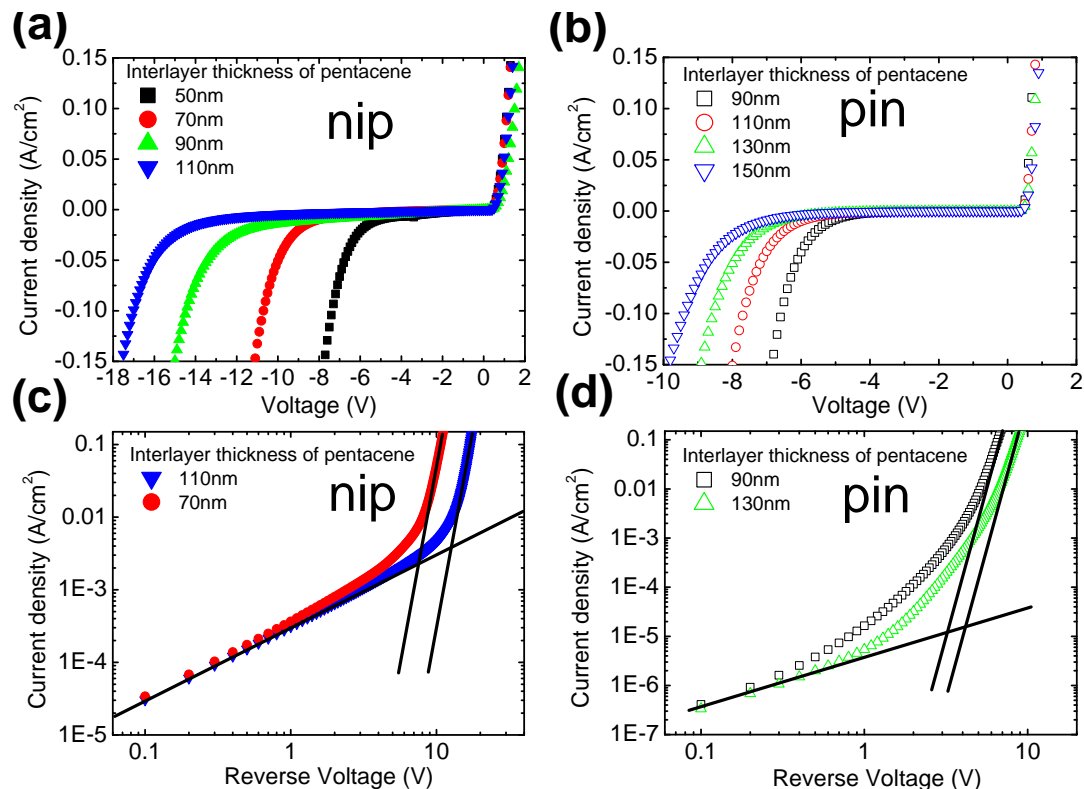
Figure 51: Current-voltage curves of organic **(a)**+**(c)** nip - and **(b)**+**(d)** pin-diodes comprising C_{60} and pentacene for different intrinsic layer thicknesses as labeled within the graphs. The individual diodes consist of: Al($50nm$)/ C_{60}:W_2(hpp)$_4$($13.0mol\%$, $50nm$)/ P5(xnm)/ P5:F_6-TCNNQ($1.5mol\%$, $50nm$)/ Al($100nm$) for nip-devices and Al($50nm$)/ P5:F_6-TCNNQ ($1.5mol\%$, $50nm$)/ P5(xnm)/ C_{60}:W_2(hpp)$_4$($3.2mol\%$, $50nm$)/ Al($100nm$) for pin-diodes.

Finally, to complete the discussion of experimental results, the temperature dependence of reverse currents for low gap diodes is shown in Figure 53. Since the I-V curves follow an Arrhenius-like behavior, an activation energy of current can be derived. As depicted in Figure 53(b), a remarkable difference in activation energy of leakage and breakdown currents can be observed. For the leakage current regime an activation of $50meV$ is determined. In contrast, if the diodes are biased in the breakdown regime, the activation energy drastically drops and reaches a value of $10meV$ which sets the experimental detection limit. The obtained activation energies for both regimes do not vary with interlayer thickness. Solely minute differences for the leakage current regime are observed for different dopant concentrations.

In summary, the experimental investigations on wide and low gap organic pin-diodes show in an unambiguous way that the reverse breakdown is in either case related to a field assisted transport mechanism, which requires a very low thermal activation energy of $10meV$. Moreover, the obtained electric breakdown field scales for low and wide gap junctions as predicted by the theory of tunneling through a triangular barrier.

(a)

(b)
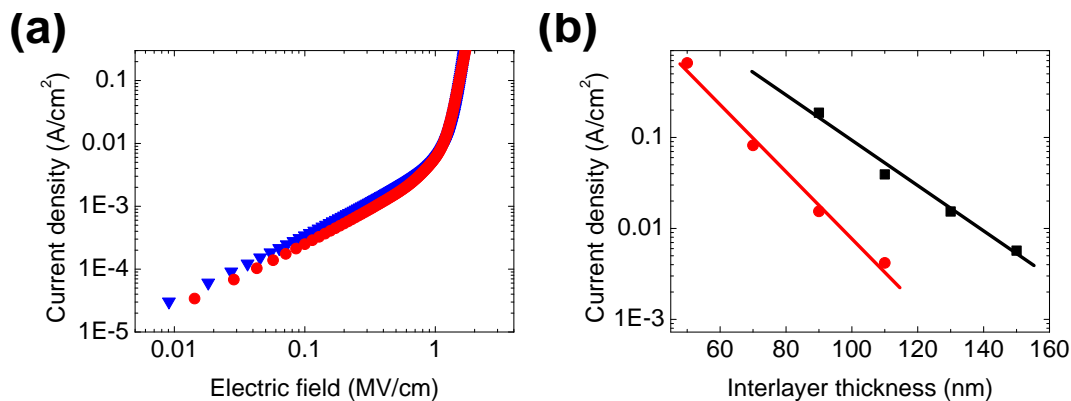
Figure 52: Current density within the reverse breakdown versus **(a)** electric field and **(b)** interlayer thicknesses of pentacene. Devices are those from Figure 51. The interlayer thicknesses in **(a)** are $70nm$ (red circles) and $110nm$ (blue triangles). The data for **(a)** is taken from Figure 51(c). To ensure that devices are operating within the breakdown regime a reverse voltage of $-7V$ for pin-diodes (black dots) and $-10V$ for nip-device (red circles) is applied in **(b)**.

4.3.3 Theoretical Description of the Reverse Breakdown

From the set of experimental investigations, the specific field and temperature dependence of the breakdown is revealed as well as a detailed energy level diagram can be drawn. Hence, a first theoretical approach to describe the breakdown mechanism is developed.

The observed experimental field dependence and the low thermal activation energy of the reverse breakdown current are rather general for a tunneling mechanism. Thus, in principle a valence to conductance state tunneling of charge carriers through a triangular barrier could provide these temperature and field dependencies. However, such a model is not reflecting the complex situation of static and dynamic disorder which typically leads to a hopping-like transport via localized states at room temperature. To account for this situation a first theoretical approach based on a minimal Hamiltonian model is formulated in cooperation with the group of Prof. Cuniberti[39]. In this subsection, the basic idea of this description is discussed in order to identify important parameters of the model. It is beyond the scope of the present work to derive the mathematical details of this model. Detailed information concerning the mathematical background are given in [31, 155, 167–169].

Initially, a representation of the active part of the pin-diode has to be found. Impedance measurements have shown that the effective tunneling barrier width is given by the sum of the intrinsic interlayer thickness and the width of the charge depletion zones. This situation allows to describe the active part of the diode by a linear ladder of states (see Figure 54). The ladder consists of N sites arranged in a linear chain with the energy eigenvalues $\epsilon_j^{s=H,L}(V)$ where $S = H, L$ denote the HOMO and LUMO strand, respectively. The energetic position of these sites can

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[39]Institute for Materials Science and Max Bergmann Center for Biomaterials Technische Universität Dresden, 01069 Dresden, Germany
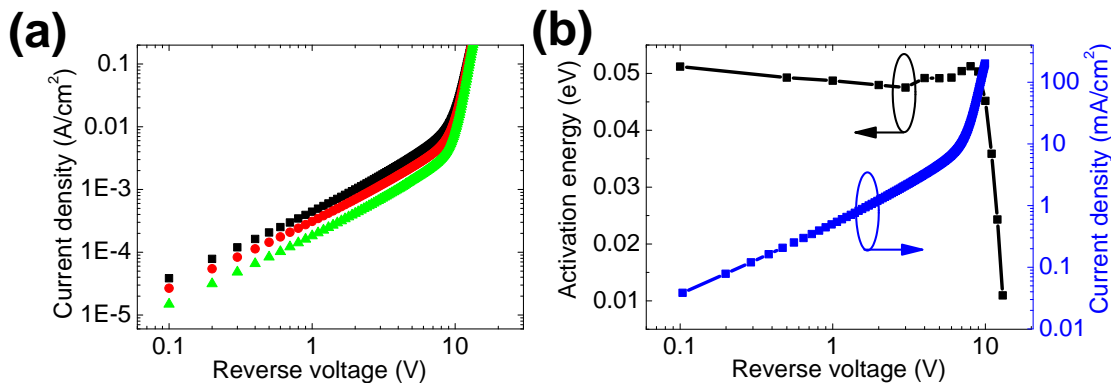
Figure 53: **(a)** Temperature dependent current-voltage curves and **(b)** activation energy of current of an organic nip-diode with an intrinsic interlayer thickness of $110nm$ (nip-diode, see caption of Figure 51 for the complete layer sequence).

be expressed with regard to the built-in potential and the applied external voltage is given by

$$\epsilon_j^s(V) = \epsilon^s - \kappa j + (j/N)qV, \tag{113}$$

where κ describes the strength of the built-in potential, and ϵ^s is the bare on-site energy of molecular orbitals (for simplicity assumed to be site-independent). According to the impedance measurements, the linear Stark-ladder perfectly describes the situation inside the intrinsic layer where the electric field is constant. However, within the charge depletion zones the electric field is not constant which leads to deviations from the linear ladder approach. Nevertheless, this approximation of a linear ladder is suitable for highly doped hole and electron transport layers or in case of a thick intrinsic interlayer.

Formulating a model for charge carrier transport along this ladder is more complex since microscopic details concerning static and dynamic disorder are unknown. Moreover, since two material systems (low and wide gap materials) are discussed, the influence of structural order has to be considered. For this reason two limiting cases of transport are discussed: incoherent, thermally assisted transport (hopping) and coherent tunneling. On a short length scale coherent transport might be sufficient. However, depending on the number of molecular sites, the static and dynamic disorder, as well as the applied voltage also incoherent transport can provide a significant contribution to the overall I-V behavior.

Incoherent transport: In case of complete loss of coherence within the ladder, transport can be described by a rate equation for the evolution of population probabilities (Markov chain). Such a coupled system of rate equations (one for each strand of the ladder) comprises the coupling to the electrode reservoirs, nearest neighbor couplings along the strands of the ladder, as well as a nearest neighbor cross-coupling between the strands. The transition rates for transport along a strand can be modeled by a phonon assisted hopping according to Eq.18. Free parameters of such a rate equation system are the coupling parameters to the elec-
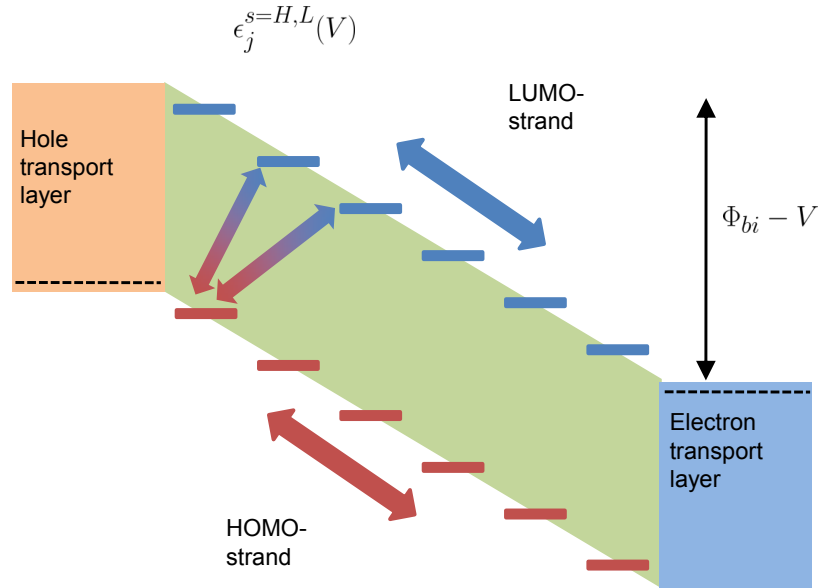
Figure 54: Schema of the electronic ladder as used within the transport model. Possible pathways for charge carrier transport are indicated by bold colored arrows. The dashed lines within the charge transport layers mark the quasi-Fermi levels within these layers.

trodes (to the charge transport layers in the present case), the number of sites, the slope of the ladder, and the intra-strand coupling terms (hopping rates). The stationary electrical current can be directly obtained from the evolution equations of population probability. Results of fitting of the experimental dataset in case of wide gap materials are shown in Figure 55(a). In forward direction, the built-in potential is counteracted by the applied voltage and the molecular energy levels along the HOMO- and LUMO-strand become increasingly aligned which leads to a steep rise of current at a voltage close to the built-in potential. More specifically, the current starts to rise when the first site of the HOMO-strand is above the quasi-Fermi level in the p-doped layer (analog for the LUMO-strand). The maximum current in this model is reached if all levels within a strand are aligned. This effect happens if the applied voltage fully compensates the built-in potential. If the diode is biased in reverse direction a sufficient blocking of current can be obtained up to a critical voltage where approximately the HOMO level of a molecule and the LUMO of its nearest neighbor become aligned. In this case, the current starts to rise exponentially as expected. Thus, the breakdown behavior is explained within this model by the cross-coupling of valence and conductance states of nearest neighboring molecules. The thickness dependence of the breakdown can be included in the model by the chosen number of sites N. If N is increased, the slope within the linear ladder is reduced and therefore a larger reverse voltage has to be applied in order to reach the exponential breakdown regime. Also the temperature dependence of reverse currents can qualitatively be explained within the incoherent transport model. For low reverse voltages, inter-strand tunneling processes are sufficiently blocked by the built-in potential barrier. If a large negative voltage lowers this barrier and the levels become aligned, a thermal activation which is required for the hopping process is effectively reduced. However,
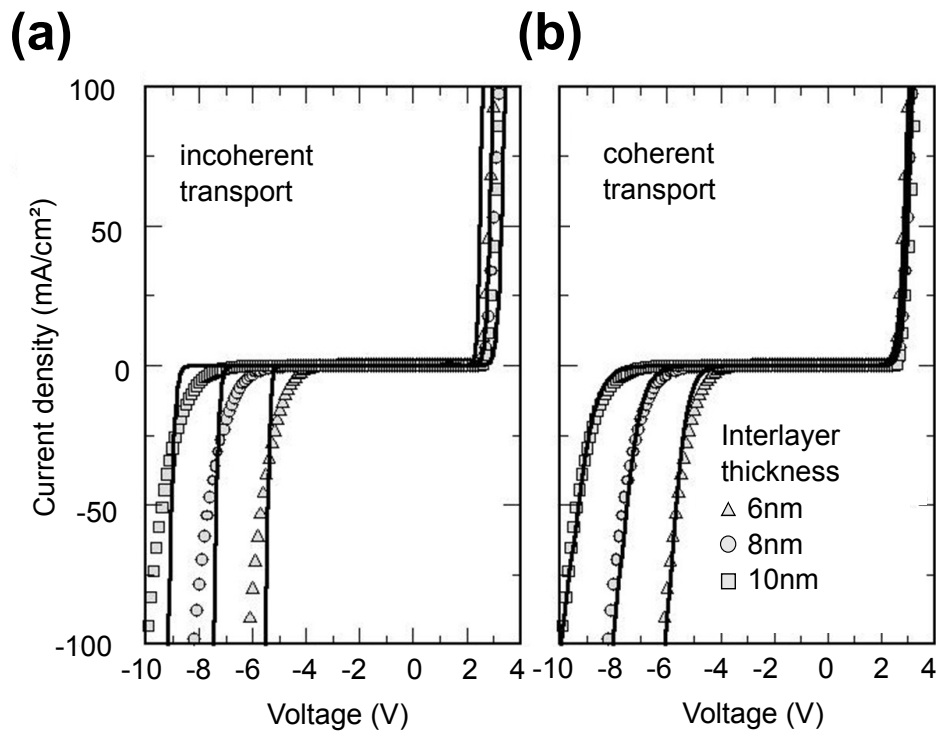
Figure 55: Calculated I-V curves (lines) in the **(a)** incoherent and **(b)** coherent transport regime compared with the measured characteristics (symbols, data taken from Figure 46). The linear ladder is modeled by: $\kappa = 0.5$, 0.37, and $0.27eV$ for $N = 3$, 4, and 5 in **(a)**; and $\kappa = 0.66$, 0.6, and $0.55eV$ for $N = 6$, 7, and 8 in **(b)**. The description of the other parameters can be found in [31].

a quantitative comparison to the experimental results is challenging since in the experimental studies the influence of the charge transport layers is included.

Coherent transport: The second limiting case for charge carrier transport is the situation of coherent transport. Even if a hopping-like mechanism is more likely for the wide gap device structures investigated here, coherent transport might sufficiently describe transport on a short length scale. Therefore, charge carrier transport presumably consists of coherent and incoherent contributions. Particularly with regard to poly-crystalline low gap materials, where a high degree of static order is expected, coherent transport might provide a contribution of considerable relevance to the overall current.

Here, coherent transport is described within the framework of Landauer-Büttiker formalism. From this theory, the current I through the system is obtained as[168]

$$I(V) = \frac{2q}{h} \int [f(E - E_F) - f(E - E_F - qV)]T(E)dE, \qquad (114)$$

where f is the Fermi function, E_F the quasi-Fermi level of the left electrode, $E_F - qV$ the quasi-Fermi level of the right electrode, and $T(E)$ the quantum mechanical transmission probability. The main challenge in order to compute the current through the system is to find the transmission probability. To derive this quantity a Hamiltonian which describes the electronic ladder is formulated in tight-binding approximation. Beside the molecular eigenstates and the nearest neighbor coupling (compare Eq.9), this Hamiltonian accounts for next-nearest neighbor coupling, for inter-strand coupling between nearest and next-nearest neighbors, as well as for coupling to the electrodes (show Figure 54 for illustration and compare references [31, 155] for the complete mathematical expressions). The transmission probability can be derived from this Hamiltonian by either evaluation of the transfer matrices (S-matrices) or it can be expressed in terms of the retarded and advanced Green functions of the system including electrodes. The latter approach is used for calculations presented here (compare [31, 155]). Similar to the incoherent transport model, the free parameters for modeling are given by the slope of the electronic ladder, the number of sites, the inter-strand and intra-strand coupling strengths, and the coupling strengths to the electrodes. The results of modeling for wide gap materials are shown in Figure 55(b). In forward direction a significant current flow appears at a voltage where the built-in potential is effectively counteracted by the applied voltage. In case of complete alignment of levels, the current reaches its maximum value. Consequently, the current flow in forward direction is widely independent of the chosen number of sites. In reverse direction, current is sufficiently blocked for low voltages, while for large reverse voltages a breakdown behavior can be obtained. The breakdown voltage is tunable by the number of sites. However, even if the results provided by the coherent and incoherent model show a good qualitative agreement, there are substantial differences particularly for reverse voltages. Most notably, the number of sites used for the coherent model is larger than for the incoherent one. These difference arises from the fact that coherent tunneling is efficient for short lengths, so that almost no zero-current gap is obtained in the modeled I-V curves. Only if the number of

sites is increased, the junction can block the current flow for low reverse voltages. Another difference between the coherent and incoherent transport model which directly affects the breakdown condition is given by the resonance condition for reverse tunneling. Specifically, in the coherent regime a sharp transition from the blocking to the breakdown regime is expected to take place if HOMO and LUMO levels of nearest neighbor sites are getting aligned. This strong resonance condition is weakened by the fact that next-nearest neighbor couplings are taken into account within the coherent model used here. Thus, the next-nearest neighbor coupling mainly gives rise to the fact that the sensitivity of reverse current on voltage and the number of sites is reduced leading to a less steep breakdown behavior for the coherent model in comparison to the incoherent scenario where only nearest neighbor couplings are considered (compare Figure 55. In general, the inclusion of next-nearest neighbor couplings within the coherent model should not be seen as a step of mandatory physical relevance, but rather as a step which leads to a better agreement between experiment and model. Nevertheless, both coherent and incoherent transport models allow the description of the experimental I-V characteristics including the reverse breakdown. This fact leads to the conclusion that both transport mechanisms might contribute to the current. However, the significance of the individual contributions might differ depending on the temperature and the applied voltage.

In case of wide gap materials, the number of sites used for modeling is almost similar to the expected number of molecular sites located within the junction. For low gap materials, however, the general conditions for charge carrier transport are rather different. In particular, charge carriers are delocalized within a radius of $\sim 10nm$ in poly-crystalline pentacene under room temperature conditions [9]. Hence, a partial coherence of electronic wave functions is expected. Consequently, there is no need to describe a poly-crystalline interlayer of pentacene by its large number of molecular sites[40], but rather it is possible to model such layer also by a number of sites $N < 20$. Furthermore, owing to the certain degree of coherence which is a consequence of the molecular order, the modeling of low gap diodes is solely done within the coherent transport model as described above.
A comparison of experimental and calculated I-V curves is shown in Figure 56. The discussion is completely analog to the case of wide gap diodes described by the coherent model. Merely the fitting parameters are modified with regard to the experimental values of built-in potential and energy gap. As shown within Figure 56(a), the model can confirm the experimental findings concerning forward and reverse I-V behavior. Especially, the reverse breakdown is described in good agreement to the experiment since the ratio of sites used within the model is equivalent to the ratio of layer thicknesses $(8/11/14/17 \sim 50/70/90/110)$. Hence, a site represents a block with an extension of $\sim 6nm$ of pentacene. Besides the dependence of breakdown voltage on interlayer thickness, also the dependency of current vs. interlayer thickness is predicted in a quantitative agreement to the experiments[41]. These modeling results for low gap diodes allow to conclude that coherent transport can play a significant role for reverse charge carrier transport

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[40] Also the numerical effort would be too large.
[41] Calculated currents curves are scaled by an arbitrary factor to match the experimental curves.

(a)   **(b)**
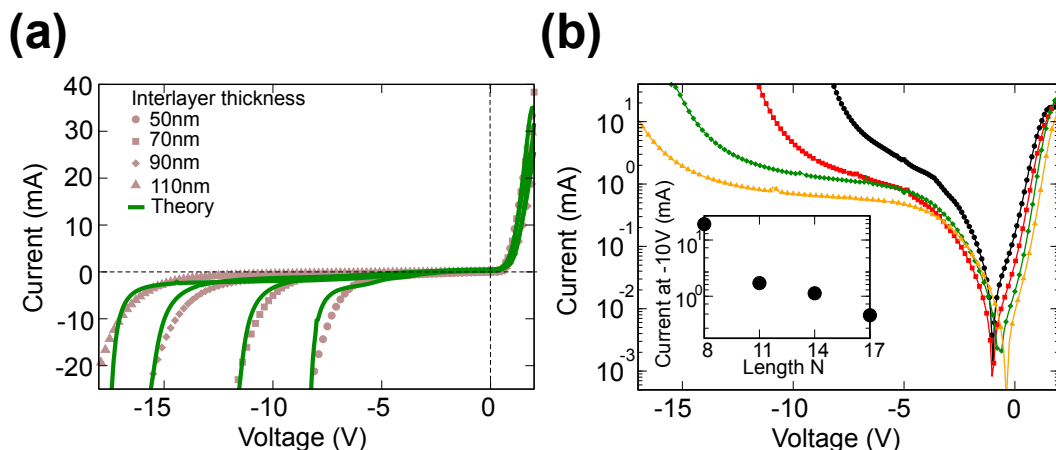
Figure 56: (a) Comparison of experimentally measured current-voltage charac-
teristics and computed curves using the model for coherent charge
carrier transport. The number of sites in the ladder is taken to be
$N = 8$, 11, 14, and 17, corresponding to the experimental effective
lengths of $L = 50$, 70, 90, and $110nm$. The corresponding values for the
slope of the ladder are $\kappa_8 = -0.32eV$, $\kappa_{11} = -0.28eV$, $\kappa_{14} = -0.20eV$,
and $\kappa_{17} = -0.18eV$. Further parameters used for modeling are given in
reference [155]. **(b)** Log-plot of the calculated I-V characteristics. The
inset shows the dependence of the current at a fixed bias $V = -10V$,
on the length of the ladder.

in poly-crystalline pentacene.

In general, this first approach to describe the reverse breakdown behavior in organic
diodes clearly shows that both coherent and incoherent charge carrier transport
scenarios are suitable to describe the experimental findings. The importance of
the individual contributions, however, might strongly depend on voltage, temper-
ature, and molecular order. A more detailed microscopic study that includes the
molecular arrangement is indispensable in order to provide a deeper understanding
of the relevant processes.

Summary

Charge carrier transport at reverse voltages is discussed within this Chapter for
wide and low gap organic pin-diodes. From current-voltage measurements and
impedance spectroscopy it can be deduced that for low reverse voltages, the I-V
performance is dominated by Ohmic leakage currents. These currents arise from
conductive paths that directly connect the doped charge transport layers through
the intrinsic interlayer. Thermally assisted generation of free charge carriers within
the charge depletion zones of the diode provides no significant contribution to the
reverse current since the extension of these charge depletion zones is typically
$< 10nm$.

Another important finding reported within this chapter is the fact that the for-
mation of charge depletion zones can be described in perfect agreement with the

Mott-Schottky relation. This result is partially surprising for pin-junctions comprising doped organic semiconductors. In particular, owing to the static and dynamic disorder, and owing to the substantial difference of the doping process in comparison to crystalline organic materials, influences of native charge carrier trap states and deep Coulomb traps induced by dopant are expected to play an important role in organic semiconductor junctions. However, as revealed by impedance spectroscopy, dopants act as shallow donor/acceptor states and the Mott-Schottky theory provides a powerful method for a quantitative analysis of the static situation in organic diodes.

Furthermore, the appearance of a reversible reverse breakdown of organic pin-diodes is shown for large reverse voltages. This breakdown is precisely controllable by the electric field within the junction. Its temperature and electric field dependence suggests a tunneling-like breakdown mechanism. Most interestingly, this breakdown mechanism is observed for wide and low gap diodes although the interlayer thicknesses differ by a factor of 10 for both types of devices.

From the experimental observations a mechanism is proposed where the breakdown is described by a valence to conductance state tunneling of neighboring molecules. Moreover, a first approach to model such breakdown behavior is developed. As limiting cases, both coherent and incoherent charge transport scenarios are investigated and they are compared to the experimental findings. Interestingly, the breakdown can be described by both models in good semi-quantitative agreement. However, whether charge carrier transport is dominated by a coherent or an incoherent mechanism cannot be clearly decided. Further investigations, particularly concerning the detailed molecular arrangement will allow to obtain a deeper insight into the fundamental processes.

Chapter V

Organic pin-Diodes for UHF Applications

'Unter allen menschlichen Entdeckungen sollte die Entdeckung der Fehler die wichtigste sein.'

St. J. Lec, poet and aphorist.

In this chapter, the properties of low gap organic pin-diodes biased in forward direction are discussed. A special focus is put on the discussion of how molecular doping affects charge carrier transport properties and specifically charge carrier mobility. This knowledge provides a suitable starting point to develop a complete small signal impedance model for low gap pin-diodes. The model is confirmed by the values of charge carrier mobility and minority charge carrier life time extracted from fitting of experimental data.

As a final step these devices are designed for ultra-high-frequencies. From the UHF characterization of these pin-diodes it is shown that design rules which are based on the small signal model allow for a targeted optimization of UHF performance.

Some parts of the work presented within this Chapter are reported in references [32, 49]. The X-ray diffraction analysis of pentacene thin-films was done in collaboration with Christoph Schünemann from the Institut für Angewandte Photophysik in Dresden, and the UHF measurements were performed at the chair of Prof. Ellinger from Lehrstuhl für Netzwerktheorie und Schaltungstechnik in Dresden.

5.1 Properties of Doped and Undoped Pentacene Thin-Films

Pentacene and C_{60} are the two materials of choice for high performance organic diodes. Owing to their fairly large charge carrier mobility in comparison to other organic semiconductors, both materials are favorable candidates that allow to push the performance of organic diodes towards the GHz regime. However, beside a large charge carrier mobility also a high electrical conductivity of these materials is needed. This aspect brings the doping technology into play since it facilitates to control the quasi-Fermi level and the injection conditions for charge carriers. Hence, before investigating pin-diodes, the structural and electronic properties of single thin-film layers of pentacene with and without dopants are discussed.

Studies on thin-film properties of C_{60} are reported e.g in references [37, 53, 56, 85, 170–172]. Depending on deposition conditions, intrinsic C_{60} grows as a nano-crystalline or amorphous film with a negligible layer roughness. The electrical conductivity of such layers is below $10^{-3}S/cm$ [171]. However, if dopants such as cesium or $W_2(hpp)_4$ are incorporated in a C_{60} layer, the conductivity increases drastically and often exceeds $10S/cm$ [37, 53]. Also charge carrier mobility as a function of dopant concentrations has been reported for C_{60} films. Harada et al. [56] have shown that charge carrier mobility in C_{60} is slightly lowered for larger dopant concentrations. This is likely attributed to a scattering at ionized impurities. However, this lowering of mobility is not accompanied with a lowering of electrical conductivity. Thus, the number of free charge carriers provided by the dopants can partially compensate for the loss in charge carrier mobility.

For pentacene the situation is far more complex since it typically grows in a poly-crystalline phase. Therefore, a particular focus of this section lies on the structural and electronic properties of undoped and doped pentacene thin-films.

5.1.1 Properties of Intrinsic Pentacene Thin-Films

Pentacene is a benchmark material in the field of organic semiconductors since rather large charge carrier mobilities in the range of $1cm^2/(Vs)$ can be obtained. However, the properties of pentacene and its specific performance in organic electronic devices strongly depend on the fabrication procedure. Hence, it is worth to investigate parameters such as film roughness, crystallite size, and charge carrier mobility in dependence of the fabrication conditions used within this work. To begin with, structural properties of pentacene thin-films deposited onto natively oxidized single crystalline (001) silicon substrates and glass substrates (borosilicate glass, substrate at room temperature for both cases) are discussed. The deposition conditions for all experiments done with pentacene are kept constant at a rate of $0.2nm/s$ and a pressure of $\sim 10^{-7}mbar$. A comprehensive study on the properties of pentacene thin-films as used within this work is given by reference [60].

Figure 57 displays scanning-force-microscopy images and surface cross-sections of two pentacene films (thickness of $40nm$ and $150nm$) deposited onto glass substrates. For both thicknesses a pronounced formation of crystalline grains can be observed. As will be discussed later (compare Figure 60), pentacene molecules are
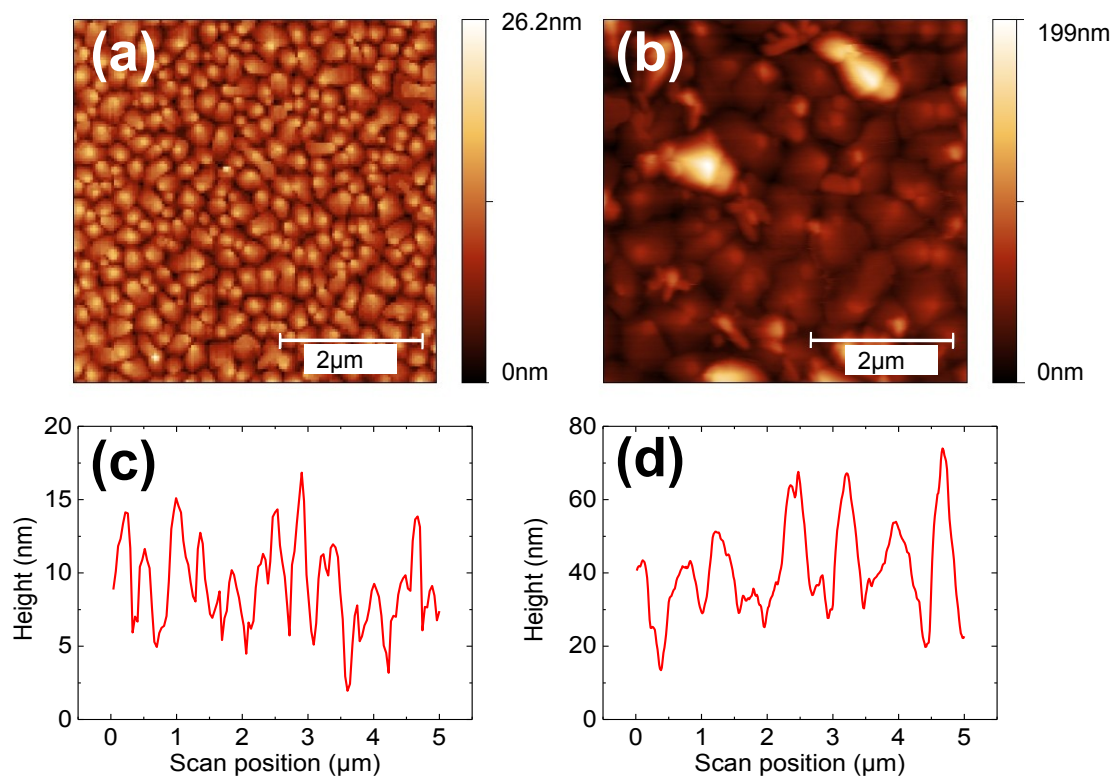
Figure 57: Scanning-force-microscopy images of a **(a)** $40nm$ and **(b)** $150nm$ thin layer of pentacene deposited onto a glass substrate. The root mean square roughness in **(a)** is $3.3nm$ and in **(b)** $24.4nm$. Cross-section graphs of the $40nm$ and $150nm$ thick layer are shown in **(c)** and **(d)**, respectively.

arranged within these grains in two triclinic crystalline phases. The size and the height of the grains is increased for thicker layers, but most notably in either case the height of the grains is in the range of the layer thickness. The layer roughness (root mean square, RMS) is $3.3nm$ for the $40nm$ thick film, and in case of the $150nm$ thick film it is $24.4nm$. Especially for the thicker film, the roughness of pentacene is an obvious problem for the fabrication of vertical devices. The influence of the substrate on layer roughness is also investigated. However, no clear dependency can be pointed out.

Charge carrier mobility is one of the most important parameters to describe charge carrier transport within a semiconductor. Here, the mobility of holes is measured within an OTFT structure. The mobility of electrons can in principle also be determined in an OTFT if the injection barrier between pentacene and the source electrode is effectively lowered. This can be realized by n-type doping of the contact region, e.g. by calcium. Applying this method, a mobility of electrons of $0.3cm^2/(Vs)$ has been reported [75]. In Figure 58, the I-V characteristics and the transfer curve of a p-channel OTFT comprising pentacene and gold source/drain electrodes are shown. In any aspect, the performance is in accordance to the behavior expected from the gradual channel approximation. Therefore, mobility of holes can be extracted by Eq.87 and the resulting mobility is shown in Figure 59. From the obtained mobility which reaches almost $0.5cm^2/(Vs)$, a rather efficient
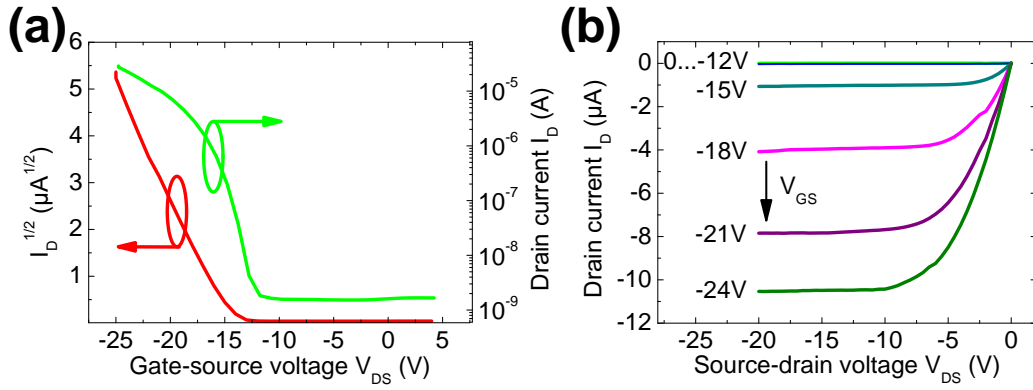
Figure 58: **(a)** Transfer characteristics $(V_{DS} = 25V)$ and **(b)** I-V curves of a pentacene top contact (bottom gate) geometry. A $50nm$ thick layer of Al_2O_3 serves as gate insulator. The $40nm$ thick layer of pentacene is covered by gold source and drain electrodes which defines the channel length of $100\mu m$ and the channel width of $1000\mu m$.
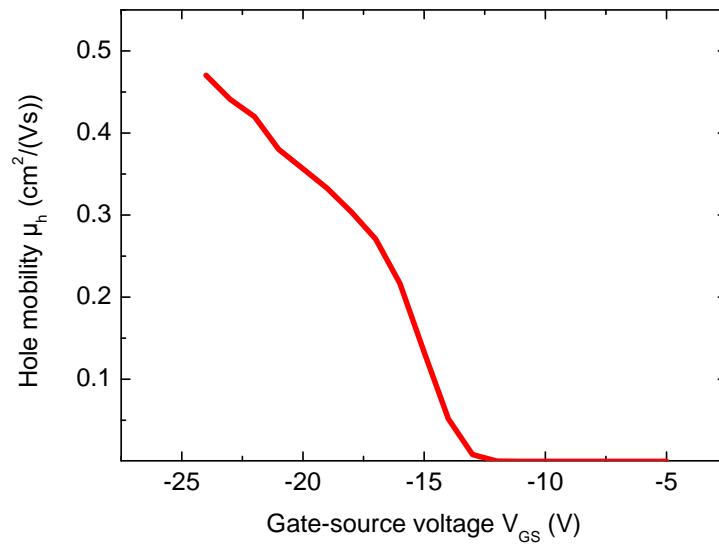
Figure 59: Mobility of holes determined in the saturation region of the OTFT according to Eq.87. The data are taken from Figure 58(a).

transport of holes in pentacene can be concluded. The gate-source voltage dependence of hole mobility can be attributed to the combined influence of contact resistance effects (compare Section 2.3.1) and the charge carrier density dependence of mobility as predicted by transport theories for organic semiconductors (compare Section 2.1.2). A detailed analysis in order to separate both influences fails because of the mathematical ambiguity of the system (compare Section 2.3.1). The large threshold voltage obtained in this OTFT of $\sim -12V$ is partially related to the low gate capacitance of the used oxide. It will be shown in Chapter 6.1 and 7.1 that this threshold voltage can be strongly reduced by using a high capacitance gate insulator.
However, the large mobility of holes of $\sim 0.5 cm^2/(Vs)$ suggests that injection (gold-pentacene) and transport of holes in pentacene is a rather efficient process.

Another important parameter which should be discussed within this context is the density of states. This quantity has been measured by Kelvin-probe spectroscopy by Yogev et al. [173]. They reported a Gaussian distribution of HOMO states with a density of $N_V = 3.1 \cdot 10^{21} eV^{-1} cm^{-3}$ and a width of $\hat{\sigma} = (0.07 \pm 0.01)eV$. Furthermore, they found an exponential distribution of tail states with a density of $8.6 \cdot 10^{14} eV^{-1} cm^{-3}$ and a characteristic energy of $k_B T_0 = 116 meV$. As will be shown in the next subsection, the influence of trap states on charge carrier transport can be lowered by molecular doping.

5.1.2 Characteristics of Charge Carrier Transport in Doped Pentacene

An efficient injection of charge carriers from gold to pentacene strongly depends on the considered device structure. For long channel devices (typically $L > 30\mu m$), the resistance of the channel dominates the OTFT performance and therefore the determined charge carrier mobility is close to the expected bulk material value. However, if the channel length is reduced, the I-V performance typically mimics a strong drop of charge carrier mobility as determined for long channel OTFTs [32, 33]. Hence, an injection barrier for charge carriers is always present, but its effect is solely visible for a short length of the channel. In this context, doping as a method to overcome these barriers is essential in order to maintain the charge carrier mobility if devices are scaled down in channel length.

Structural properties of doped pentacene films In a first step, the influence of the two molecular dopants F_4-TCNQ and F_6-TCNNQ on the structural properties of doped pentacene thin-films is analyzed. To identify crystalline order, the deposited films are investigated by X-ray diffraction (XRD) using monochromatic Cu-K$_\alpha$ radiation for a $\theta - 2\theta$-scan. These investigations and the analysis are done by Christoph Schünemann. Specific information concerning XRD characterization are given in [49].
XRD scans for undoped pentacene as well as for pentacene doped by F_4-TCNQ and F_6-TCNNQ are shown in Figure 60. All layers consist of two triclinic phases which are reported in the literature as polymorph III phase [174] and polymorph II phase [175]. For comparison, the Bragg reflections of these phases are shown
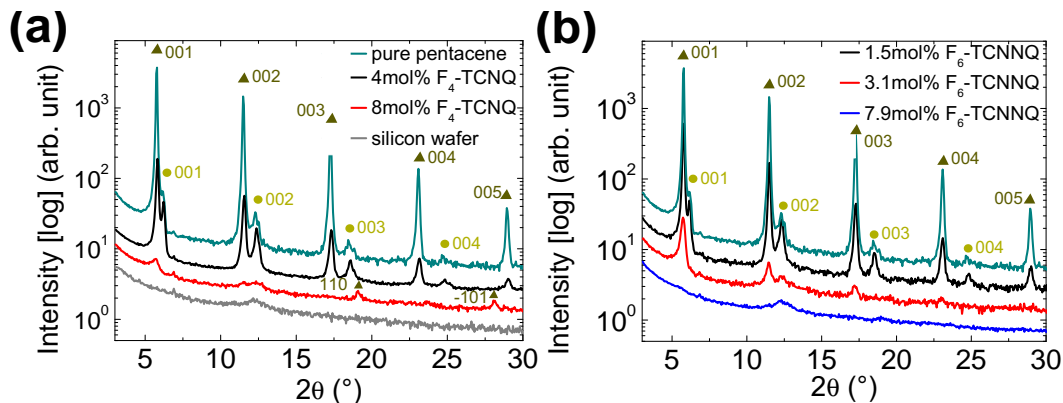
Figure 60: XRD $\theta - 2\theta$-scans of **(a)** the $150nm$ thick undoped pentacene film, the F_4-TCNQ doped pentacene film, and **(b)** the F_6-TCNNQ doped pentacene film for different dopant concentrations. The XRD pattern of the silicon substrate which is used for layer deposition is shown in **(a)**. The theoretical 2θ Bragg angle positions of the XRD reflections of the polymorph III [174] (triangles) and polymorph II [175] (circles) pentacene modifications are indicated by different symbols together with *hkl* Miller indices.

in Figure 60. The polymorph III phase is the dominant phase in all samples. For undoped pentacene merely the (001) reflections of both phases are observed. Hence, all pentacene crystallites are oriented in the same direction in the undoped film. If dopants are incorporated in the matrix material other reflections appear which indicates that structural disorder is induced. A crystallization of dopants can be excluded owing to the fact that all Bragg reflections can be associated to the two triclinic phases of pentacene. As a second aspect, the XRD measurements prove that the crystallinity of the layer is strongly decreasing upon doping. Already for the lowest dopant concentration a reduced height of the Bragg reflections is observed. Hence, the dopant molecules suppress the crystalline arrangement of pentacene molecules under co-deposition conditions. The disturbance of crystalline order is more pronounced for F_6-TCNNQ than for F_4-TCNQ. This point is likely related to the different size of these molecules since F_6-TCNNQ is larger than F_4-TCNQ. Pentacene films doped with F_6-TCNNQ are nearly amorphous for $3.1mol\%$ of dopant molecules. In case of F_4-TCNQ, a crystalline order is maintained up to a least $8mol\%$ of dopants. Also the appearance of two new orientations ((110) and (-101)) can be seen in the XRD pattern for high dopant concentrations of F_4-TCNQ.

The XRD measurements can be used to determine the size of crystallites within the layers. For this evaluation, the shapes of the Bragg reflections are analyzed using the Scherrer equation and the Cauchy-Cauchy model[42]. A full description of this method can be found in [176, 177]. The results of the calculations are summarized in Table 6. For undoped pentacene the size of the polymorph III crystallites is comparable to the overall film thickness. Thus, the crystallites reach from the bottom to the top of the film which is in accordance to the scanning-force-microscopy investigations (compare Figure 57). Crystallites present in the polymorph II phase

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[42]The crystallite size determined by this technique is the size perpendicular to the surface.
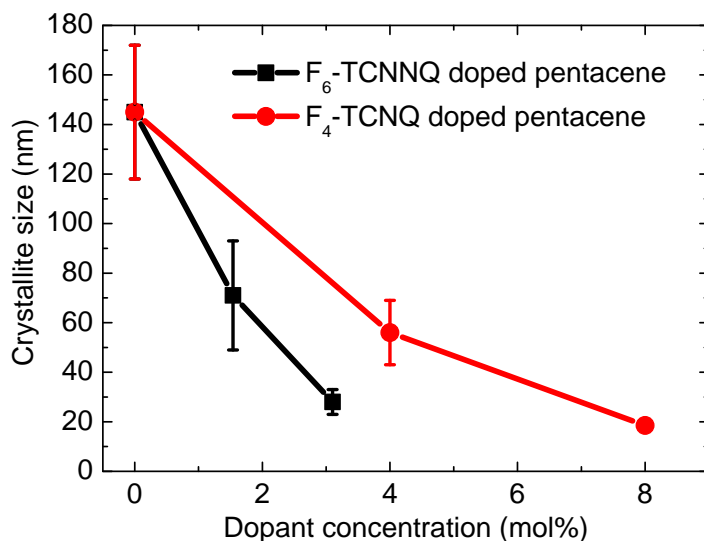
Figure 61: Crystallite size of the polymorph III phase of pentacene in dependence of the dopant concentration of F_4-TCNQ and F_6-TCNNQ. Lines are drawn as guide to the eye.

	Crystallite size (nm)	Polymorph	Bragg reflection
undoped	145 ± 27	III	001
	54 ± 37	II	001
$1.5 mol\%$ F_6-TCNNQ	71 ± 22	III	001
	42 ± 17	II	001
$3.1 mol\%$ F_6-TCNNQ	28 ± 5	III	001
		II	
$4 mol\%$ F_4-TCNQ	56 ± 13	III	001
	60 ± 33	II	001
$8 mol\%$ F_4-TCNQ	19	III	001
	23	III	110
	28	III	-101

Table 6: Crystallite sizes of the polymorph II and III phase of pentacene for different dopant concentrations of F_4-TCNQ and F_6-TCNNQ. For some crystallite size values a determination of the error is not possible because only one Bragg reflection is obtained for each molecular orientation.
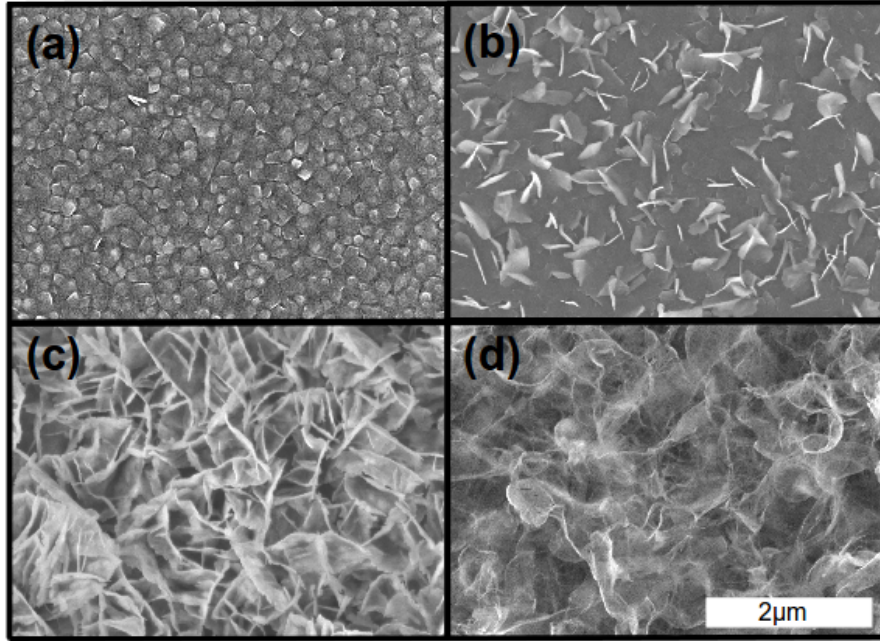
Figure 62: SEM micrographs of undoped and doped pentacene films. The images show a $150nm$ thick film of pentacene grown on a silicon wafer with $50nm$ of Al_2O_3. The dopant concentrations of F$_4$-TCNQ are: **(a)** undoped, **(b)** $2mol\%$, **(c)** $6mol\%$, and **(d)** $10mol\%$. All films are prepared in the same manner as for the XRD measurements.

are smaller ($\sim 50nm$) and the crystallite size is strongly decreasing for increasing dopant concentrations in doped pentacene layers. In Figure 61, the size of polymorph III crystallites is compared for F$_4$-TCNQ and F$_6$-TCNNQ. As expected from the XRD measurements, F$_6$-TCNNQ has a stronger influence on the structural order than F$_4$-TCNQ. In particular, for F$_4$-TCNQ the largest dopant concentration where still a crystalline phase can be observed can be more than twice as high as for F$_6$-TCNNQ.

The influence of dopant states on the surface morphology is studied by scanning-electron-microscopy (SEM). Figure 62 contains SEM micrographs of undoped pentacene and pentacene doped by F$_4$-TCNQ. SEM studies on F$_6$-TCNNQ doped pentacene result in a similar behavior. In case of undoped pentacene, a uniform distribution of grains can be seen. However, if dopants are added, the layer morphology changes. For $2mol\%$ of F$_4$-TCNQ, grains are still visible in the background. Most interestingly, flakes which seem to stick out of the surface can be detected. An agglomeration of dopant at the surface as an explanation for these flakes is unlikely since this should also be obtained in the XRD measurements. Moreover, as will be shown (compare Figure 65), a demixing of matrix and dopant is improbable since it could not explain the strong increase of electrical conductivity upon doping. However, this tendency of flake formation is even more pronounced for larger dopant concentrations. No crystalline order can be found for $6mol\%$ of dopants. In contrast, the surface morphology completely changes into a sponge-like, very rough surface. Unfortunately, the composition of this sponge-like structure cannot be disclosed from SEM micrographs and XRD measurements.

Also scanning-force-microscopy is used for surface analysis. However, it turns out
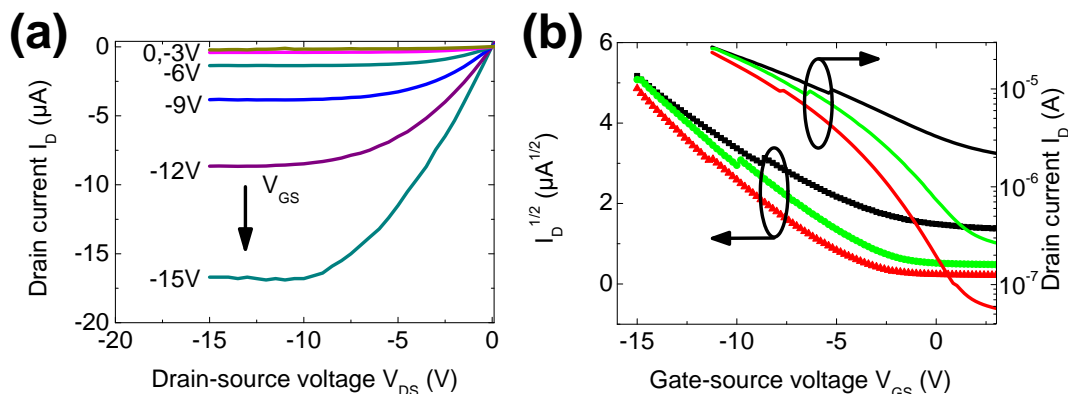
Figure 63: **(a)** I-V curves of an OTFT which comprises pentacene doped by F_4-TCNQ ($4mol\%$) for different gate-source voltages. **(b)** Transfer characteristics (saturation regime, $V_{DS} = -15V$) of molecular doped pentacene OTFTs for different dopant concentrations of F_4-TCNQ. The colors in **(b)** denote concentrations of F_4-TCNQ of $2mol\%$ (red), $4mol\%$ (green), and $6mol\%$ (black). The kink in the transfer curves is an artifact due to the switch of the measurement range of the used SMU.

that owing to the extreme surface roughness, such investigations are not possible for the sponge-like structures shown in Figure 62. In case of $2mol\%$, the highest peaks are found to have a height of $> 120nm$. For larger dopant concentrations the height of these peaks exceeds the range of the electronic controller of the scanning-force-microscope ($\sim 300nm$).

In the following, the influence of doping on the crystalline order and grain size and its effect on charge carrier transport in pentacene thin-films has to be discussed. At first, experiments on the influence of doping on charge carrier mobility are presented. Referring to these observations, the interplay between molecular doping and charge carrier mobility is discussed.

Characterization of charge transport in OTFTs comprising doped pentacene: OTFT devices are used to determine the mobility of holes in pentacene thin-films. The analysis is done in the saturation regime of the OTFT according to Eq.87. This method, however, is not straightforward for OTFTs with doped layers since in general the current in such devices is composed of two contributions: a gate-source voltage independent bulk current and the current through the channel controlled by the gate-source potential. The evaluation of charge carrier mobility is based on the gate-source voltage dependent current contribution. Therefore, for large gate-source voltages where the current through the channel is significantly larger than the bulk current, the slope of the transfer characteristics is not affected by the increased off-state current. Hence, a reliable evaluation of charge carrier mobility is feasible. The I-V and transfer characteristics of OTFTs that comprise molecular doped pentacene are shown in Figure 63. As can be seen in the I-V curve, the saturation regime of the drain current is not affected by the bulk current contribution. Merely the off-state current level of the transistors is increased. This effect has also been confirmed by Klauk and coworkers [33].

The mobility of holes in doped and undoped pentacene films determined by OTFT
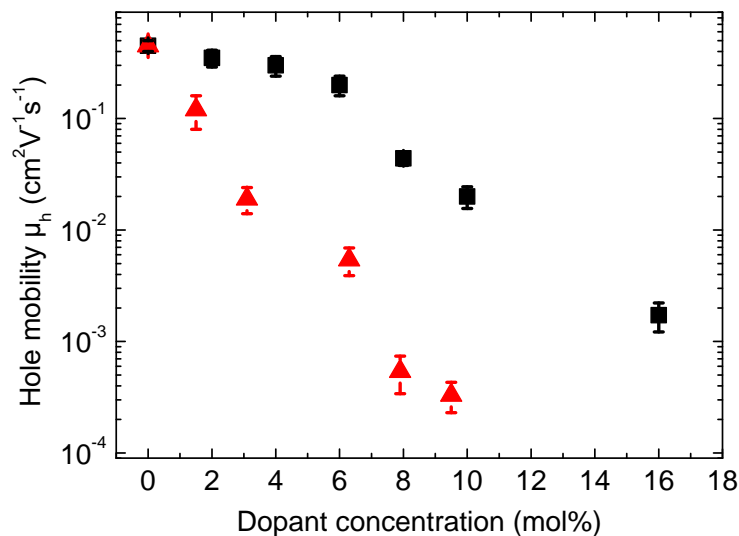
Figure 64: Mobility of holes in pentacene OTFTs doped by F_4-TCNQ (black rectangles) and F_6-TCNNQ (red triangles) for various dopant concentrations. Mobility values are calculated by the slope of the gate voltage sweep at $V_{GS} = -15V$ (saturation region). Error bars for mobility are taken from deviations of different devices built on the same sample.

measurements is depicted in Figure 64. Here, the obtained XRD pattern can clearly be correlated to the mobility of holes in doped pentacene films. Starting with a value of $\sim 0.45 cm^2/(Vs)$ for undoped pentacene, charge carrier mobility is strongly dropping if dopants are co-deposited. For amorphous films with high dopant concentrations, charge carrier mobility is reduced by almost a factor of 10^3 in comparison to the undoped material. The general tendency of charge carrier mobility vs. dopant concentration is similar for F_4-TCNQ and F_6-TCNNQ. However, there are also differences which are presumably caused by their different impact on crystallinity. In detail, with F_4-TCNQ charge carrier mobility slightly decreases for dopant concentrations up to $6 mol\%$. In accordance to the XRD measurements, it can be concluded that owing to the remaining crystallinity of the pentacene film, charge carrier mobility is only weakly affected. Contrary, if the amorphous phase dominates the film properties, the charge carrier mobility strongly drops. For F_6-TCNNQ, this behavior is less pronounced due to the fact that already a dopant concentration of $1.5 mol\%$ leads to a significant loss of crystalline order.

The main intention for doping is to increase the electrical conductivity by raising the number of free charge carriers. Figure 65 shows the conductivity of pentacene doped by F_4-TCNQ and F_6-TCNNQ as measured in the OTFT. As it is shown, the conductivity strongly increases upon doping by almost a factor of 10^4 for both dopants. The rise of conductivity upon doping is highly non-linear which is in accordance to previous findings for poly-crystalline materials [42, 57]. However, a peak in conductivity is obtained which appears at a dopant concentration of $6 mol\%$ for F_4-TCNQ and $1.5 mol\%$ of F_6-TCNNQ. For larger dopant concentrations a loss
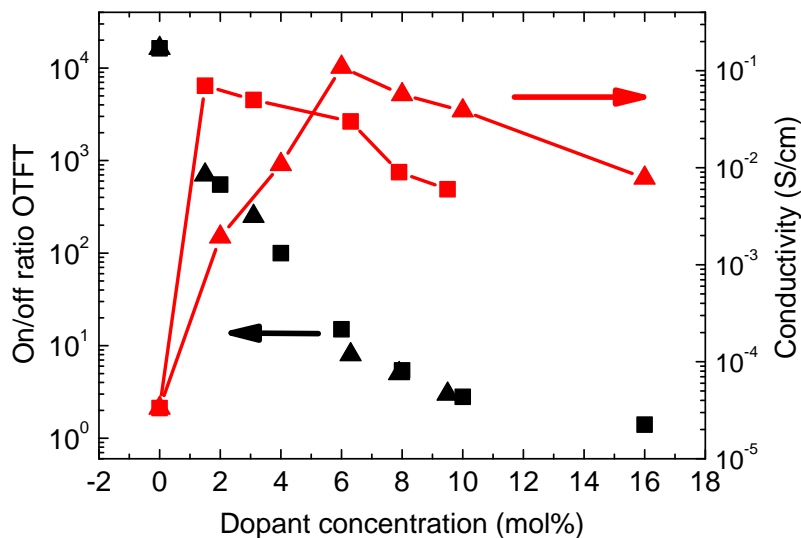
Figure 65: On/off ratio (black) and the film conductivity (red) of the OTFTs consisting of pentacene doped by F_4-TCNQ (closed triangles) and F_6-TCNNQ (open rectangles). Conductivity is measured in the OTFT geometry without applied gate-source voltage at a source-drain voltage of $-10V$. Lines are drawn as guide to the eye.

of conductivity is found. These results can be interpreted as follows. For low dopant concentrations, where the doped pentacene films still contain crystalline domains, the number of free charge carriers is effectively increased by the dopant molecules while charge carrier mobility is only weakly affected (e.g. for $< 6mol\%$ of F_4-TCNQ). On the other hand, owing to the loss of crystalline order and the related strong drop of charge carrier mobility, the electrical conductivity decreases for larger dopant concentrations. By comparing the slopes of the mobility and conductivity decay curves, one can conclude that even for large dopant concentrations free charge carriers are effectively provided by the dopant molecules. The expected increase in conductivity, however, is suppressed by the strong drop of charge carrier mobility. This behavior of charge carrier mobility and conductivity can also be seen in the on/off ratio[43] of the OTFTs. Even if the drop of on/off ratio upon doping seems to be continuous, the slope is influenced by two aspects: the on-state current (governed by the mobility) and the off-state current (governed by the bulk conductivity). For low dopant concentrations where charge carrier mobility is weakly affected, the drop of on/off ratio is dominated by the increasing off-state currents. Contrary, for larger dopant concentrations, the bulk conductivity drops and therefore the on/off ratio should increase again. However, the strong drop of charge carrier mobility leads to a reduced on-state current and hence the on/off ratio decreases continuously.

Discussion of charge carrier transport in doped organic thin-films: The influence of molecular doping on conductivity and mobility of pentacene is topic

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[43]defined here as $I_D(V_{GS} = -15V, V_{DS} = -15V)/I_D(V_{GS} = 0V, V_{DS} = -15V)$

of recent experimental and theoretical investigations [57, 178, 178, 179]. Harada et al. [57] observed a loss of charge carrier mobility upon doping by F_4-TCNQ. However, the effect on crystallinity is neglected in this work. A recent theoretical approach to understand the doping process is reported by Mityashin et al. [179]. They argue that owing to the matching size F_4-TCNQ can be incorporated within the lattice of pentacene. Relying upon this assumption they predict a super-linear increase of conductivity upon doping. However, also in this model the influence of dopants on the crystalline order is disregarded.

To understand the behavior of conductivity vs. doping in detail, it is worth to discuss possible scenarios of charge carrier transport depending on the degree of structural order. Two mechanisms presumably dominate charge transport: transport in pentacene grains for a poly-crystalline structure and a hopping-like transport in the amorphous phase. In this context two important questions have to be discussed: firstly, where are the dopant molecules located and secondly, what is the minimal crystallite size where charge transport starts to be dominated by a hopping-like process and not by transport within the poly-crystalline structure?

The first question was discussed by Maennig et al. [42]. They argued that the super-linear rise of conductivity cannot be explained by an agglomeration of dopant molecules at grain boundaries. Thus, they concluded that dopant molecules must be embedded in the grains. Moreover they need to act as shallow acceptor states in order to explain the rise of conductivity [42]. These conclusions are in accordance to the experimental findings of Ha et al. [180] and the theoretical predictions of Mityashin et al. [179]. However, even if this is also very likely in the present case, it cannot be concluded from XRD investigations whether dopant molecules are embedded in the grains or agglomerate in between them.

The second question is discussed in the literature in two different ways. On the one hand, percolation models [42] were used to describe transport by hopping between localized transport states. In this theory, the conductivity and the mobility depend on the overlap parameter. This parameter governs the tunneling rate between localized transport states. Thus, it is considered to be higher in ordered films and therefore, larger conductivity and mobility values are expected. The strong dependency of the overlap parameter on structural order can explain the loss of conductivity and mobility observed here. Therefore, dopant molecules embedded in the pentacene crystallites give rise to an increasing conductivity for low dopant concentrations owing to an increased number of free charge carriers [43, 181]. However, they can also cause a slightly decreasing mobility related to increased disorder. For larger dopant concentrations, the complete loss of crystalline order leads to a strongly reduced overlap parameter and therefore to reduced transport properties such as conductivity and mobility.

The second approach addressing the question of transport phenomena in such systems was discussed by Horowitz et al. [26]. They distinguish between transport in grains and grain boundaries. Different grains are connected by grain boundary states and thus the system can be treated as a back-to-back Schottky barrier. Conductivity and mobility are described by the Matthiessen rule taking transport via grains and grain boundaries into account (compare Eq.33). Thus, for low dopant concentrations the increasing conductivity can be explained by an increase of conductivity within the grains. The slightly decreasing mobility can be related to a

stronger contribution of grain boundary states due to the reduced crystallite size. However, the assumption of the Schottky barrier formation remains valid until the Debye length is smaller than the crystallite size. For a crystallite size smaller than the Debye length, the material can be treated as an uniform film. Thus, since doping gives rise to a strong decrease of the crystallite size, this model can explain the loss of mobility by a complete loss of the crystalline phase. Despite this fact, the model fails for disordered films (or large dopant concentrations), where the Debye length is larger than the crystallite size. Thus, this theory cannot provide mobility values under such conditions.

However, both models discussed here can qualitatively explain the obtained dependencies of mobility and the conductivity. Important parameters to describe the properties of charge transport are those describing the structural order. The structural order influences both the overlap of localized transport states and the relation between the crystallite size and the Debye length. Temperature dependent measurements on conductivity and mobility could provide a way to distinguish between the two charge migration models. For the percolation path model [42] an increased hopping probability for larger temperatures should lead to an increased conductivity and mobility. Contrary, for transport via individual grains as proposed by Horowitz et al. [26] an increased Debye length for increased temperature should not strongly affect the transport properties of the film for highly doped samples, where the crystallite size is already smaller than the Debye length.

Characterization of charge transport in vertical devices: The charge carrier mobility determined so far describes charge carrier transport in the plane of the substrate. However, also for vertical devices such as diodes, charge carrier mobility is an important parameter in order to control the device performance. Therefore, organic Schottky diodes comprising pentacene are used to evaluate the mobility of holes in the direction perpendicular to the substrate. However, one should keep in mind that the different grain sizes and crystallographic orientations in vertical and horizontal direction preclude a direct comparison of charge carrier mobility in both directions.

An illustration of the used diode stack is shown as an inset in Figure 66. In this structure, the injection of electrons is sufficiently blocked at the aluminum/pentacene interface [60]. Contrary, holes are efficiently injected from the bottom electrode and therefore the layer sequence can be treated as a p-type Schottky diode which can be used to determine charge carrier mobility by analyzing space charge limited currents [68]. At the bottom electrode the polymer PEDOT:PSS[44] acts as a buffer which firstly reduces the roughness of the gold electrode and secondly improves the injection of holes into the pentacene [68]. The PEDOT:PSS (CLEVIOS^{TM}, $PH1000$, $6vol.\%$ ethylene glycol, thickness $50nm$, conductivity $700S/cm$ [182]) is structured by photo-lithography [183] to the dimensions of the bottom electrode. In this way, it is guaranteed that the active area ($0.01mm^2$) of the devices is given by the overlap of the two metal electrodes.

Figure 66 shows the I-V curves of these pentacene Schottky diodes for different dopant concentrations of F$_4$-TCNQ. As indicated within this graph, the slope of two in the log-log plot allows to describe the I-V curves by a space charge lim-

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[44]Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate)
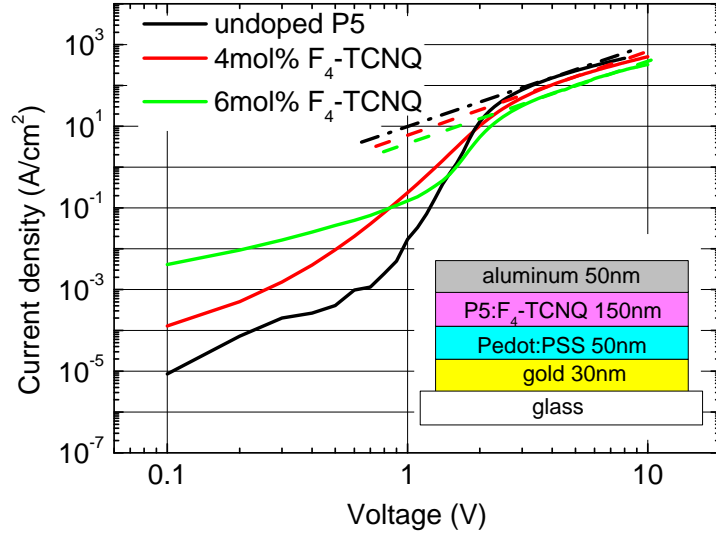
Figure 66: Current-voltage characteristics of undoped and doped pentacene Schottky diodes in forward direction. The dotted lines are drawn to illustrate the behavior expected for a trap-free SCLC according to Eq.72. The device structure is shown as inset.

	μ_{SCLC} $(cm^2/(Vs))$	μ_{OTFT} $(cm^2/(Vs))$
undoped	0.13 ± 0.03	0.45 ± 0.05
$4mol\%$ F$_4$-TCNQ	0.08 ± 0.03	0.3 ± 0.06
$6mol\%$ F$_4$-TCNQ	0.045 ± 0.001	0.2 ± 0.06

Table 7: Comparison of charge carrier mobility as determined from the SCLC analysis (μ_{SCLC}) and the OTFT characterization (μ_{OTFT}). For the SCLC analysis of hole mobility a dielectric constant of $\epsilon = 6.1$ is used (compare Subsection 4.2).

ited current (SCLC) for voltages $> 2V$. To guarantee the validity of Eq.72, the thickness dependence of the I-V curves is confirmed. As shown in Figure 67, the current-voltage behavior follows the predicted power law dependence $j \sim 1/w^3$. Hence, according to Eq.72, the mobility of holes can be extracted and the obtained values are summarized in Table 7. Even if the absolute values differ in comparison to the mobility determined by OTFTs, the general behavior of mobility versus dopant concentration is equivalent for horizontal and vertical transport. Furthermore, one should be aware of the fact that this simple SCLC model does not account for field, temperature, charge carrier density, and trap density dependence of charge carrier mobility.

Unfortunately, no clear SCLC-like behavior is obtained for dopant concentrations $> 6mol\%$ of F$_4$-TCNQ. Owing to the stronger influence of F$_6$-TCNNQ on the crystalline order, no clear SCLC is found in case of F$_6$-TCNNQ even for the lowest dopant concentration of $1.5mol\%$. This indicates that the loss of crystallinity order is associated to a change of the dominant charge transport regime. It is yet
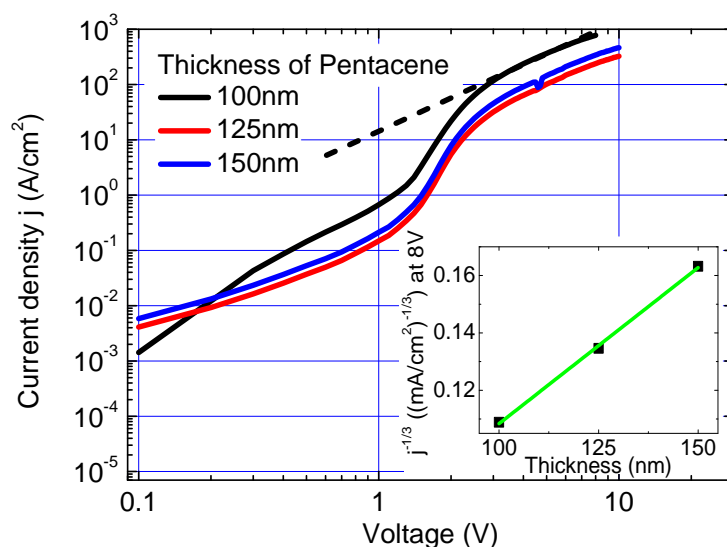
Figure 67: Current-voltage characteristics of doped pentacene Schottky diodes in forward direction ($6mol\%$ of F_4-TCNQ) for $100nm$ (black), $125nm$ (blue), and $150nm$ (red) of pentacene. The dotted line is drawn to illustrate the behavior expected for a trap-free SCLC according to Eq.72. To proof the thickness dependence predicted by Eq.72, the inset show the current density at $8V$ for different layer thicknesses.

unclear if this transition is related to a change in the density of states which is caused by the loss of crystalline, or if it is related to the appearance of deep traps states.

In contrast to the OTFT measurement, I-V curves for vertical devices allow to estimate the influence of dopant molecules on the distribution and the occupancy of charge carrier traps. The contribution of traps states to the I-V curve can be seen in the low voltage region ($< 0.7V$) in Figure 66. The pure pentacene film exhibits an intrinsic trap density which causes a trap limited current. If the number of injected charge carriers is large enough, the transition from a trap limited current to a SCLC-like behavior can be obtained.

Dopant molecules can be treated as shallow acceptor states since they provide free charges at room temperature which leads to an increase of conductivity at low voltages. An increase and a broadening of the total density of states by adding dopant molecules to pentacene has been discussed elsewhere [43, 181]. The increase of the current in the low voltage region with increasing dopant concentration up to $6mol\%$ of F_4-TCNQ can be explained by a filling of native trap states of pentacene by charge carriers provided by the dopants. Hence, for low dopant concentrations where the crystalline order is maintained, dopants can effectively provide free charge carriers at room temperature which are partially used to compensate native traps states. For larger dopant concentrations, however, deviations from the SCLC behavior suggest a transition to another type of charge carrier transport as discussed within this section.
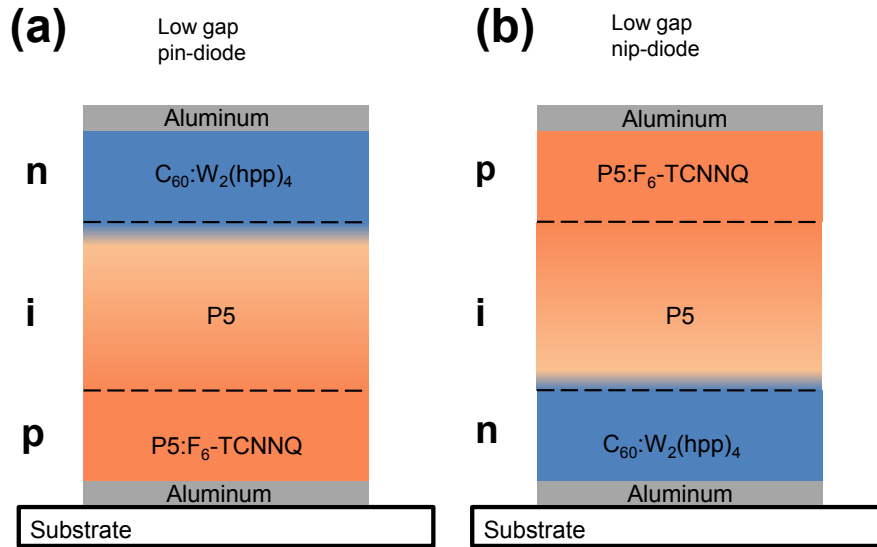
Figure 68: Overview on the two types of diodes used for discussion. Typical matrix/dopant combinations for hole and electron transport layers (HTL/ETL) as well as typical materials for the intrinsic layer are shown. The device types are **(a)** low gap pin-diodes, **(b)** low gap nip-diodes, Owing to the poly-crystalline nature of pen- tacene (P5) the transition between the doped and the intrinsic layer is blurred.

5.2 Forward Properties of pin-Diodes Comprising Pentacene and C$_{60}$

Within the following two subsections, the results of the previous study on the influence of dopants on conductivity and mobility of pentacene are used to design and optimize organic pin-diodes for UHF conditions.

As will be pointed out, the pin-diode concept facilitates an adjustment of basic diode properties such as rectification ratio, forward resistance, reverse capacitance, and charge carrier transit time. Controlling these characteristics exhibits a major requirement in order to optimize organic diodes for the targeted application. Therefore, the main intention of this subsection is to identify the crucial parameters controlling the diode performance and moreover to show how the performance of organic pin-diodes can be optimized with regard to UHF applications.

A scheme of low-gap organic pin- and nip-diodes, as they are employed in the following discussion, is shown in Figure 68.

Initially, static properties of such diodes are discussed and, based on these properties, basic design rules for organic pin-diodes are deduced. Furthermore, combining these static properties and the findings on dynamic properties, a complete small signal model for these diodes is presented.

5.2.1 Static Current-Voltage Behavior

The intrinsic interlayer thickness and the dopant concentration inside the charge transport layers are the two main parameters to adjust the static current-voltage
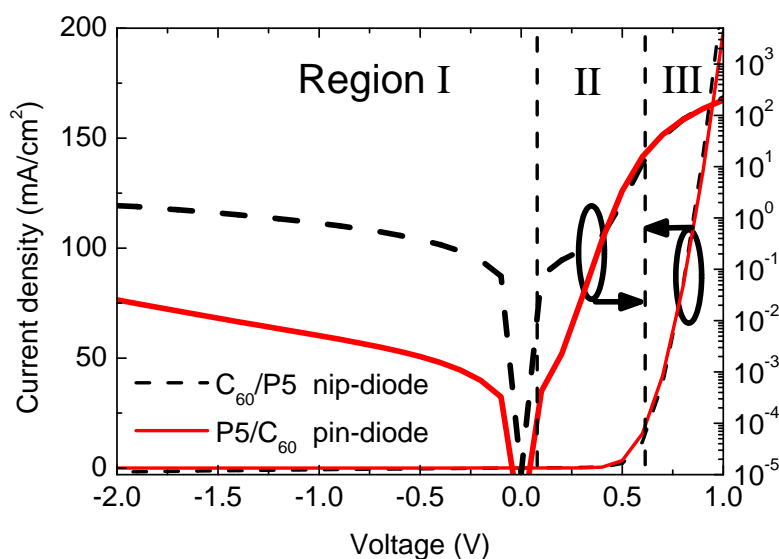
Figure 69: Current-voltage curves for pin (red line)- and nip-diodes (black dashed line). The layer sequence is Al(50nm)/ pentacene:F$_6$-TCNNQ(50nm, 0.8$mol\%$)/ pentacene(150nm)/ C$_{60}$:W$_2$(hpp)$_4$(50nm, 3.2$mol\%$)/ Al(100nm) in case of the pin-diode and Al(50nm)/ C$_{60}$:W$_2$(hpp)$_4$(50nm, 8$mol\%$)/ pentacene(110nm)/ pentacene:F$_6$-TCNNQ(50nm, 3.1$mol\%$)/ Al(100nm) in case of the nip-diode.

behavior of organic pin-diodes. In particular, the forward resistance, the reverse capacitance, and the rectification ratio can directly be tuned by the interlayer thickness. The dopant concentration is not less important since it affects charge carrier mobility and layer morphology. Therefore, both parameters are discussed here.

To begin with, the general current-voltage behavior of organic pin-diodes will be discussed. The current-voltage curves of pin- and nip-structures are presented in Figure 69. Shockley's theory for non-ideal diodes is adopted here [61] for a approximate quantitative description. Three different regions in the I-V curves can be identified. For small forward ($< 0.3V$) voltages and the entire reverse direction shown here, the I-V curves are dominated by leakage currents (Region I). As discussed in Section 4.1, such reverse currents are not caused by thermal assisted generation of free charge carriers, but rather by direct leakage paths passing through the intrinsic layer.

An exponential rise of the I-V curve (Region II) is obtained for forward voltages between $0.3V$ and approximately $0.6V$. In this region charge carriers are injected into the intrinsic layer, they diffuse to the other transport layer and recombine. This behavior is in accordance to Shockley's theory assuming a generalized Einstein equation.

Finally, for forward voltages $> 0.6V$, a space charge limited (SCLC) behavior (Region III) is observed, which is superimposed by the exponential current rise of the diode.

Using these models to describe the I-V behavior of Region I, II, and III, the experi-
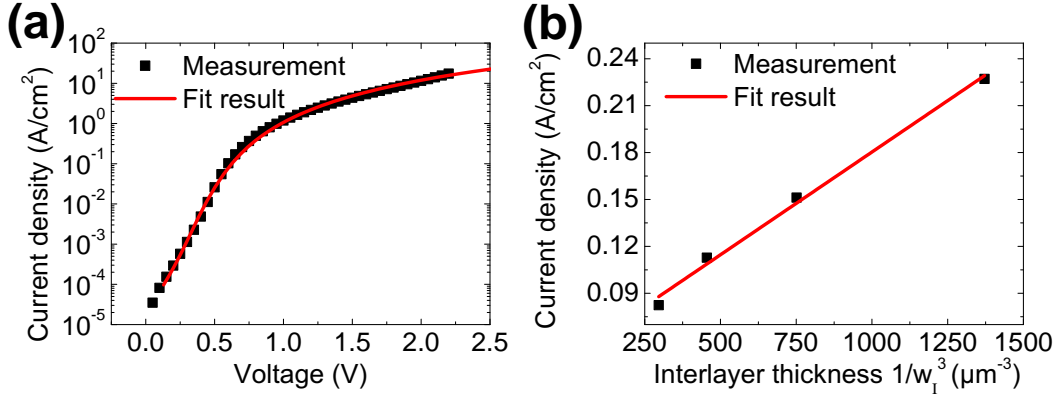
Figure 70: **(a)** Current-voltage characteristics of an organic pin-diode as described in the caption of Figure 69 with an intrinsic layer of pentacene (thickness $150nm$), and fit results using a function containing a series connection of an ideal Shockley diode, an element described by an SCLC law, and a resistor in parallel. **(b)** Current density of organic pin-diodes (Region III) as described in the caption of Figure 69 for different interlayer thicknesses, and comparison to the predicted SCLC thickness dependence.

mental current-voltage curves can be fitted as shown in Figure 70. The fit function reflects an equivalent circuit composed of an ideal Shockley diode (compare Eq.70), an element described by a SCLC behavior (compare Eq.72), and a resistor in parallel to the first two elements. Despite its simplicity, this function provides a good quantitative agreement to the experimental results. Furthermore, two important parameters for the description of the diode performance can be extracted by fitting: the ideality factor of the diode, and the charge carrier mobility according to Eq.72. The latter parameter is evaluated to be $(0.20 \pm 0.05) cm^2/(Vs)$ using a dielectric constant of $\epsilon = 6.1$ and an interlayer thickness of $150nn$. This value of charge carrier mobility is in good accordance to the value determined in pentacene Schottky diodes (compare Subsection 5.1). For sake of completeness, it should be mentioned that the layer thickness dependence of the current in Region III follows the w_I^3 dependence as predicted by the SCLC law (see Figure 70(b)). Furthermore, it should be noted that the charge carrier mobility, as estimated from the fit shown in Figure 70(a), is presumably too low owing to the fact that the applied voltage is reduced by the built-in potential of the diode which is neglected in the fitting function. Moreover, as discussed within Subsection 2.2.2, charge carrier mobility determined by SCLC in organic pin-diodes has to be treated as an effective value of mobility since both holes and electrons are present in the intrinsic layer.

The second important parameter that can be evaluated by the fitting function is the slope of the exponential current rise in Region II. This slope $1/\theta_{NI}$ (compare Eq.70) allows to extract the ideality factor of the diode η_D which is given by $\theta_{NI} = \eta_D k_B T$. In this way an ideality factor of $\eta_D = 1.7 \pm 0.1$ is determined. As discussed within Subsection 2.2.2, the interpretation of this ideality factor is difficult since it is an empirical factor. Only in case of an ideal Shockley diode (no recombination in the charge depletion zones) or in case of strong recombination (all minority charge carriers recombine in the charge depletion zones), its value is

theoretically predictable to be $\eta_D = 1$ or $\eta_D = 2$, respectively. In the present case, however, a conclusion whether recombination is a dominant process in such organic pin-diodes or not is not possible since a theoretical model for the ideality factor that includes the influence of charge carrier traps and non-uniform DOS functions (Gaussian or exponential DOS) is missing. The role of recombination and charge carrier trapping will be considered in the next subsection on the dynamic response of organic pin-diodes.

With regard to electronic circuit design and integration of organic diodes in particular for UHF applications, another property of organic pin-diodes comprising pentacene and C$_{60}$ has to be discussed here. The I-V curves of pin- and nip-diodes are nearly equal in Region II and III (compare Figure 69). This demonstrates that these diodes can be fabricated independently of the layer sequence (pin or nip) which is a remarkable advantage concerning device integration in double- or full-wave rectifier circuits.
Nevertheless, these devices show a significant difference at reverse and low forward voltages, which is caused by a difference in layer morphology and interface formation (see also Subsection 4.3). Thus, for pin-diodes, the C$_{60}$ molecules are presumably coated conformally along the peaks and valleys of the rough pentacene layer and in this way a smoother interface is created between undoped and doped regions. This leads to strongly reduced leakage currents in pin-diodes in comparison to nip-devices. This increased leakage current level represents a strong disadvantage of nip-structures especially for the targeted application in the UHF range. Therefore, the further discussion is limited to pin-diodes.

Interlayer thickness dependence of I-V behavior: In the following the influence of the intrinsic interlayer thickness on the static current-voltage behavior of low gap pin-diodes is discussed. The interlayer thickness is of major importance for the optimization of I-V curves since it is the main parameter to adjust the rectification ratio and the capacitance of the diode. This is basically due to the fact that the interlayer thickness determines the current in backward direction (compare Section 4.1), as the voltage mainly drops across this layer. Moreover, the reverse capacitance is also dominated by the intrinsic interlayer thickness, as the charge depletion zones at the interface between the doped layer and the intrinsic layer are typically thinner than the intrinsic layer itself (compare Section 4.2). Thus, thick interlayers are indispensable in order to achieve large rectification ratios and small reverse capacitances.
However, due to the low charge carrier mobility in organic materials, the transit time increases for thicker interlayers. Therefore, an optimum of intrinsic interlayer thickness has to be found in order to obtain large rectification ratios as well as a minimum of transit time.
As shown in Figure 71, the overall current density is reduced for increasing interlayer thickness. In forward direction (upper branch) this is due to the series resistance of the interlayer for small voltages and due to the characteristics of the SCLC for larger voltages. In reverse direction, almost no difference for different interlayer thicknesses at small voltages is observed, indicating a good blocking of reverse charge carrier transport. Only for larger reverse voltages a super-linear
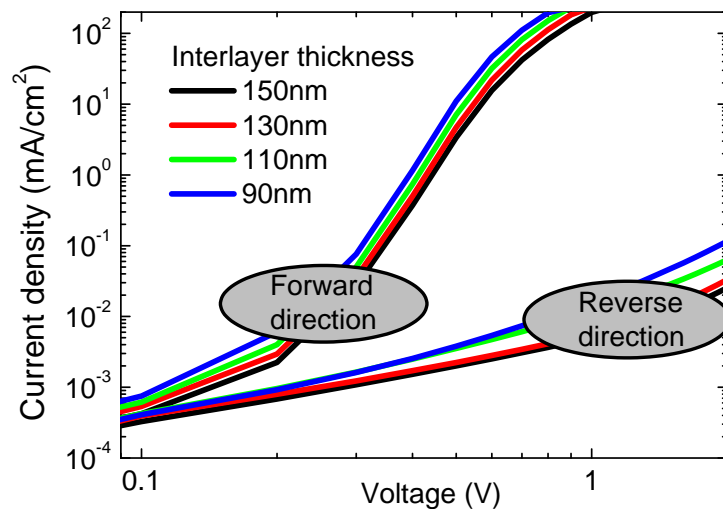
Figure 71: Current-voltage curves of pin-diodes for different interlayer thicknesses of pentacene. The layer sequence is Al($50nm$)/ pentacene:F$_6$-TCNNQ($50nm$, $0.8mol\%$)/ pentacene(ynm)/ C$_{60}$:W$_2$(hpp)$_4$($50nm$, $3.1mol\%$)/ Al($100nm$).
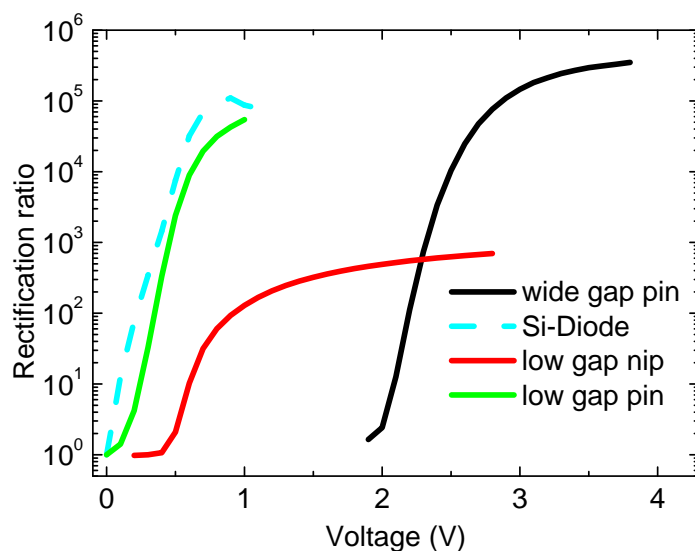
Figure 72: Rectification ratio for a low gap pin- (light green line, intrinsic layer: $130nm$ pentacene), a nip- (red line, intrinsic layer: $130nm$ pentacene), a typical silicon diode (dashed light blue line), and a wide gap organic pin-diode (black line, intrinsic layer: $10nm$ BAlq$_2$:NPB ($1:1$)) as shown in Subsection 4.2.

increase of current can be observed suggesting the transition to the reverse break-down regime. Thus, on the one hand one can effectively suppress the reverse current by increasing the interlayer thickness, while on the other hand an increased interlayer thickness leads to a reduced forward current and therefore a reduced rectification ratio[45] in total. For the targeted application of UHF diodes, it is of particular importance to design the diode in a way that it possesses a minimum of forward resistance but also a maximum of rectification ratio. As shown in Figure 72, an optimum of rectification $(9 \cdot 10^4)$ is attained for an interlayer thickness of $130nm$ of pentacene. In particular, such organic pin-diodes can almost reach the performance of state-of-the-art silicon diodes concerning rectification ratio. For comparison, also the rectification ratio of a wide gap organic pin-diode and a low gap organic nip-diode is shown. Although the forward resistances of low gap nip- and pin-diodes are equivalent concerning rectification, the nip-structure suffers from the increased leakage current level. Hence, the rectification ratio is strongly reduced for nip-devices. In contrast to this, rectification ratios even larger than for low gap pin-diodes can be obtained for wide gap diodes. However, these diodes start rectifying at considerable large voltages and hence owing to this loss, they are inappropriate for UHF application. This large onset voltage for rectification in wide gap diodes is a direct consequence of the large energy gap in these systems. In particular, charge carrier transport in wide gap diodes is not dominated by diffusion, but rather by drift. Therefore, the built-in potential needs to be compensated before the diode starts rectifying.

Dopant concentration dependence of I-V behavior: The second important parameter to adjust the I-V performance of organic diodes is the dopant concentration. It affects the width of the charge depletion zones, the conductivity of the doped layers, the built-in potential, and the layer morphology. The width of the intrinsic layer is typically larger than the width of the charge depletion zones (compare Subsection 4.2) for the devices presented here. Thus, especially the influence of doping on the layer conductivity and morphology is discussed.

Figure 73 displays the impact of the doping concentration on the forward resistance and the leakage current level. In reverse direction, a clearly reduced leakage current with decreasing dopant concentration is observed. This is presumably related to a different morphology of the p-type doped pentacene layer leading to direct shunt paths through the intrinsic interlayer. This hypothesis is confirmed by impedance measurements as shown in Figure 74. The impedance follows a $|\tilde{Z}| \sim 1/f$ law for frequencies $> 10kHz$ as expected for a RC-unit (RC parallel). For lower frequencies, however, the impedance response is dominated by the resistor which can be seen in the flat impedance curve. The magnitude of this resistor is decreasing with increasing dopant concentrations. This unambiguously shows that doping leads to an increased Ohmic leakage current and not to an increased contribution arising from trap states (such an influences should give a capacitive response). Hence, the increased leakage current can directly be attributed to the increased larger roughness induced by molecular doping (compare Subsection 5.1.2).

Apart from this increase in leakage current level, the forward direction is weakly

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[45]Rectification ratio: ratio between forward and reverse current at the same voltage but for the opposite polarity.
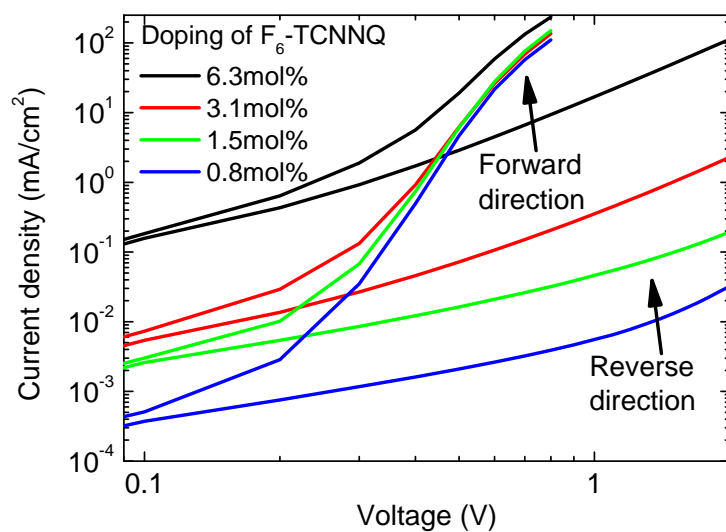
Figure 73: Current-voltage curves of pin-diodes for different p-type dopant concentrations. The layer sequence is Al(50nm)/ pentacene:F$_6$-TCNNQ(50nm, $xmol\%$)/ pentacene(130nm)/ C$_{60}$:W$_2$(hpp)$_4$(50nm, 3.1$mol\%$)/ Al(100nm).
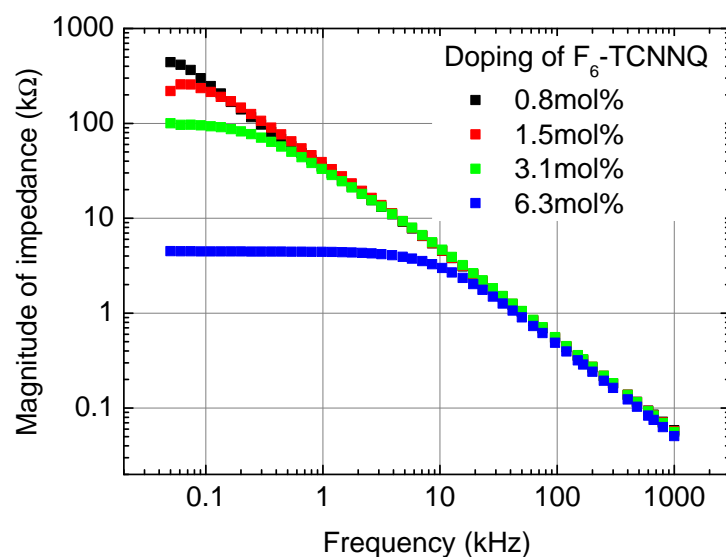
Figure 74: Impedance spectra recorded for the pin-diodes described in Figure 73. The spectra are measured without applied bias voltage (0V).

affected by the dopant concentration for voltages $> 0.8V$. However, as reported in the previous section, for higher forward voltages where the I-V curves are approaching the typical power-law for SCLCs, a reduced mobility with increasing dopant concentration is expected. This can be attributed to a reduced crystallinity of doped pentacene. For pin-diodes however, the SCLC regime is dominated by the undoped intrinsic interlayer and therefore, if the loss in mobility in the doped layers is moderate, the total space charge current is only weakly affected. Thus, for moderate dopant concentrations where the conductivity of pentacene is strongly increased (compare Section 5.1) while charge carrier mobility is almost maintained, controlled doping of pentacene is a key technology to adjust the performance of these pin-diodes. In particular, the reduced leakage level for low dopant concentrations causes an increased rectification ratio with an optimum at a doping ratio of $1mol\%$ F$_6$-TCNNQ. For dopant concentrations less than $1mol\%$, an additional voltage drop over the hole transport layer is obtained, which causes reduced forward currents.

### 5.2.2 Dynamic Properties - A Small Signal Impedance Model

Although the main parameters characterizing organic pin-diodes can be obtained from static investigations as discussed thus far, the analysis of the dynamic properties is indispensable in order to understand and predict the behavior of organic diodes at UHF conditions. More specifically, important time constants such as charge carrier transit time, minority charge carrier life time, and the characteristic dielectric relaxation time (charging and discharging of the depletion capacitance) can be estimated and allows for dynamic modeling. Furthermore, the time dependence of parasitic effects such as charge carrier trapping and release can be studied.

Impedance model for the backward direction: Before focusing on the forward voltage small signal response, the discussion on the reverse capacitance started in Subsection 4.2 is continued and completed.
In this previous discussion, the reverse capacitance of low and wide gap organic pin-diodes is calculated assuming one dominant RC-unit. In case of wide gap diodes, the capacitance-frequency plot shows one distinct plateau which justifies this equivalent circuit model. However, in case of low gap diodes, the capacitance plateau according to the geometrical capacitance is only obtained for frequencies $> 10kHz$ (compare e.g. Figure 44). Hence, this simple equivalent circuit model does not describe these diodes in their entire complexity[46].
In this paragraph, another equivalent circuit model is proposed which accounts for charge carrier trap states appearing in the diode. Figure 75 displays the capacitance of a low gap organic pin-diode as also discussed within Subsection 4.2. Apparently, two different regions can be identified within these spectra. For frequencies $> 7kHz$, the capacitance function is approaching the value of the geometrical capacitance of the intrinsic layer ($3.05nF$). Contrary to this, a second plateau of the capacitance appears for lower frequencies ($< 7kHz$). It has been

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[46]For wide gap diodes no trap states are obtained in the impedance spectra since for the devices considered here, the depletion capacitance dominates the impedance response. Nevertheless, trap states are presumably also present in such materials.
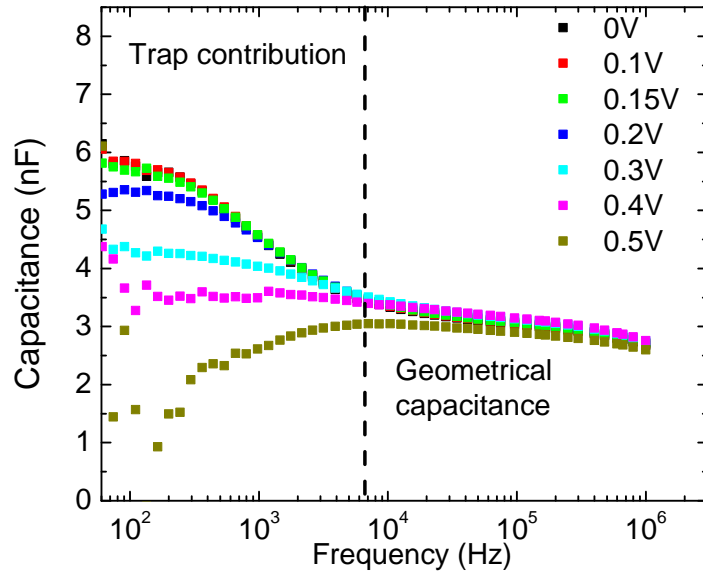
Figure 75: Capacitance-frequency curves of pin-diodes for different forward voltages. The layer sequence is Al(50nm)/ pentacene:F_6-TCNNQ(50nm, 0.8$mol\%$)/ pentacene(110nm)/ C_{60}:W_2(hpp)$_4$(50nm, 3.1$mol\%$)/ Al(100nm).

shown [148] that this slow response can be attributed to charge carrier trap states which are presumably located at the interface between the intrinsic layer and the doped layers. The presence of charge carrier trap states can also be seen in the I-V curves as discussed in the previous subsection. Comparing e.g. Figure 69 or Figure 71, one can find that the exponential current rise according to Shockley's theory starts for voltages $> 0.2...0.3V$ while an Ohmic behavior is obtained for smaller voltages. These characteristics can be consistently explained if trap states are considered in the small signal model. In particular, considering the voltage dependence of the small signal capacitance shown in Figure 75, a strong drop of the trap related capacitance contribution is revealed if a forward voltage $> 0.2V$ is applied. Contrary, the plateau of the geometrical capacitance stays unaffected. This strong drop of the trap capacitance can be interpreted by a filling of trap states by free charge carriers which are injected into the intrinsic layer. Once all trap states are filled, they stop contributing to the capacitance function.

A simple equivalent circuit approach which takes the contribution of trap states into account is shown in Figure 76(a). Within this equivalent circuit, the trap contribution on the small signal impedance response is mimicked by a series connection of a resistor R_T and a capacitor C_T which are in parallel to the depletion capacitance C_D and the parallel resistance R_P. This simple component $R_T C_T$ represents one single trap level and its characteristic capture and emission time ($R_T C_T$) which can be estimated by fitting as shown in Figure 76(b) to be $0.3ms$. Although the assumption of one dominant trap level exhibits a strong simplification, it is not necessary to employ more complex trap models (compare e.g. [148]),
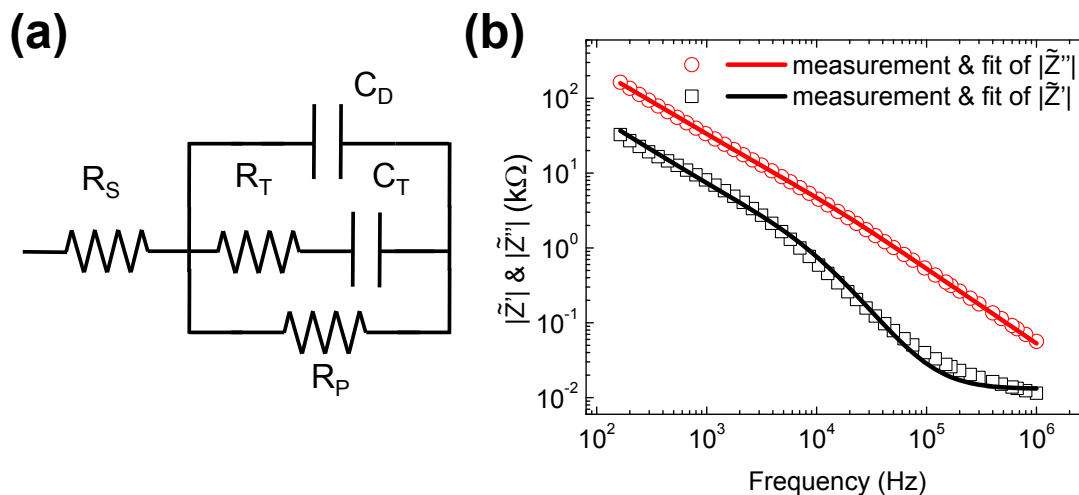
Figure 76: **(a)** Equivalent circuit model describing the impedance response of organic pin-diodes in reverse direction, and **(b)** experimental impedance curves taken from Figure 75 and the corresponding fitting curves using the equivalent circuit shown in **(a)**.

since as shown in Figure 76(b), the simple equivalent circuit approach is suitable to sufficiently describe the measured impedance of low gap organic pin-diodes. Analyzing the voltage dependence of the trap related capacitance (compare Figure 44 and Figure 76(b)), it can be concluded that all trap states are depopulated at $0V$ since the capacitance is not increasing for reverse voltages. Moreover, applying a small forward voltage, all trap states are populated easily and hence it can be concluded that there are either very little traps or they are shallow states[47].

This provides an important information concerning the dynamic response of organic pin-diodes. In this context, the trap states obtained here do not contribute to the current response on an alternating voltage signal with a frequency $> 3kHz$. The trap states are in equilibrium. Nevertheless, such states give rise to a power loss since $0.2 - 0.3V$ are lost to fill them.

Impedance model for the forward direction: As a next step to complete the small signal model of organic pin-diodes considered here, the discussion is centered on the forward voltage behavior where charge carrier transport through the junction is taking place. However, before starting the quantitative impedance analysis, the different transport scenarios that can possibly occur in organic pin-diodes are reconsidered. Moreover, corresponding equivalent circuit models and the characteristic impedance response are compared.

In forward voltage direction charge carriers occupy states in the charge depletion zones and in the intrinsic layer. They are either used to fill up trap states for voltages $< 0.3V$ or they directly give rise to the exponential rise of current for larger forward voltages. However, in either case, the driving force for charge

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[47]Since the trap emission time $R_T C_T$ contains the effective DOS as well as the trap depth both quantities cannot be determined independently without a detailed temperature dependent analysis.

carrier transport is diffusion since the voltage is smaller than the built-in voltage[48].
The basic question concerning charge carrier transport which arises is: What happens to charge carriers entering the intrinsic interlayer?
Possible scenarios can be summarized as follows:

- diffusion of charge carriers through the intrinsic layer into the neutral bulk region of the opposite side of the junction where they recombine as minority charge carriers within a characteristic minority charge carrier life time (simple diffusion model),

- recombination in, and diffusion through the intrinsic layer into the neutral bulk region of the opposite side of the junction where they recombine as minority charge carriers within a characteristic minority charge carrier life time (weak recombination model),

- and diffusion of charge carriers into the intrinsic layer where all charges recombine via trap states or by electron-hole recombination (strong recombination model).

The charge carrier density profiles for these three different cases are depicted in Figure 77. In order to distinguish between the three situations, one can either compare a typical time scale (transit time τ_t vs. recombination time τ_r) or a typical length scale (interlayer thickness w_I vs. diffusion length L_D). This allows to categorize these cases by

- $L_D >> w_I$ or $\tau_t << \tau_r$ for the simple diffusion model,

- $L_D \sim w_I$ or $\tau_t \sim \tau_r$ for the weak recombination model,

- and $L_D << w_I$ or $\tau_t << \tau_r$ for the strong recombination model.

As discussed in Subsection 2.2.3, the solution of the diffusion-recombination equation can be translated in an equivalent circuit model as shown in Figure 77.

In the following, the experimental impedance curves are described by the upper equivalent circuit models. However, to analyze the impedance spectra quantitatively it is important to know if recombination is dominant in the intrinsic region or not. This can either be decided by fitting of the impedance data or by varying the thickness of the intrinsic layer. More specific, the transition frequency where the impedance curve turns from the semicircle to the $\tilde{Z} \sim (i\omega)^{-1/2}$ behavior is not equivalent to the inverse transit time $1/\tau_t = 1/r_m c_m$ in case of strong recombination (compare Figure 77, or see [67]). In case of weak recombination, however, the obtained transition frequency has to match the fitted inverse transit time. As will be shown in the following, for the pin-diodes discussed here, the impedance spectra can be described within the weak recombination approximation or even in the simple diffusion model. For further confirmation, different interlayer thicknesses are used to study the influence of the fitted transit time. As will also be shown, the obtained transit time scales with the interlayer thickness suggesting that recombination plays a minor role in the intrinsic layer. Hence, for fitting of

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[48]The built-in voltage cannot be determined by impedance spectroscopy in a reliable way since for low gap diodes since the total reverse capacitance is not governed by the charge depletion zones (compare Subsection 4.2). Nevertheless, the built-in voltage can be estimated by the molecular HOMO/LUMO values as $0.8 - 1.0V$ assuming a pinning of the quasi-Fermi level.
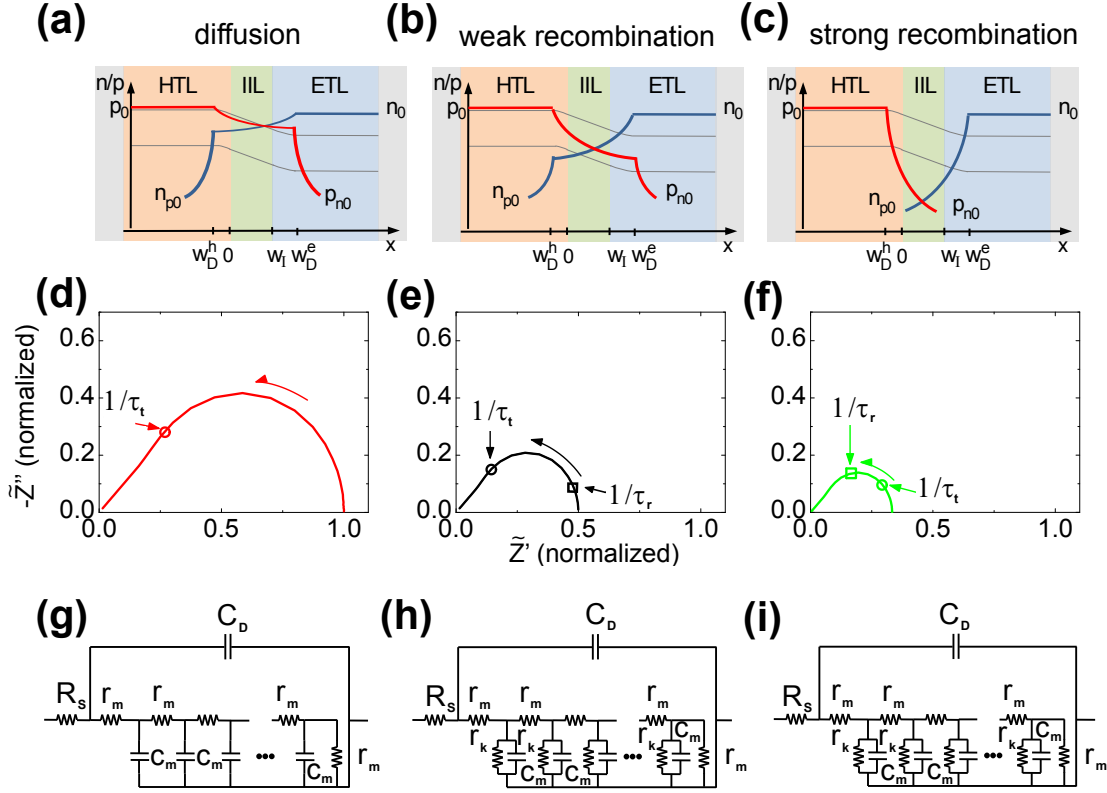
Figure 77: Charge carrier transport for different strengths of recombination, the corresponding impedance curves obtained by solving the diffusion-recombination equation (compare Eq.76), and the equivalent circuit representation of the diffusion-recombination equation. The three dots in **(g)**, **(h)**, and **(i)** indicate the infinite repetitions of the transmission line model (compare Subsection 2.2.3).

the impedance curves, the simple diffusion model is used here.

Even if this is a strong assumption, the obtained impedance spectra can clearly be distinguished from the strong recombination case. Furthermore, even in the worst case $L_D = w_I$ ($r_m = r_k$), charges still reach the opposite side of the junction. Merely their transit time is overestimated since the condition for the simple diffusion model $\tau_t << \tau_r$ is not fulfilled. This overestimation of transit time results in an underestimated diffusion constant $D = w_I^2/\tau_t$.

Impedance spectra for a forward biased organic low gap diode and fitting results according to Eq.76 (or the equivalent circuit shown in Figure 77(g)) are shown in Figure 78. Depending on the applied forward voltage, different features of the spectra can be identified. For voltages $\leq 0.5V$, the spectra contain a large semi-circle for low frequencies. This behavior is attributed to the presence of charge carrier trap states as discussed in the previous paragraph. The radius of this semi-circle is decreasing with increasing forward voltages owing to the filling of these states. In order to account for these trap states, an additional RC-unit as shown in Figure 76 is included in the equivalent circuit. If the forward voltage is increased ($> 0.5V$), this part of the equivalent circuit can be neglected since all trap states are occupied. Instead of trap states, the impedance is now dominated by
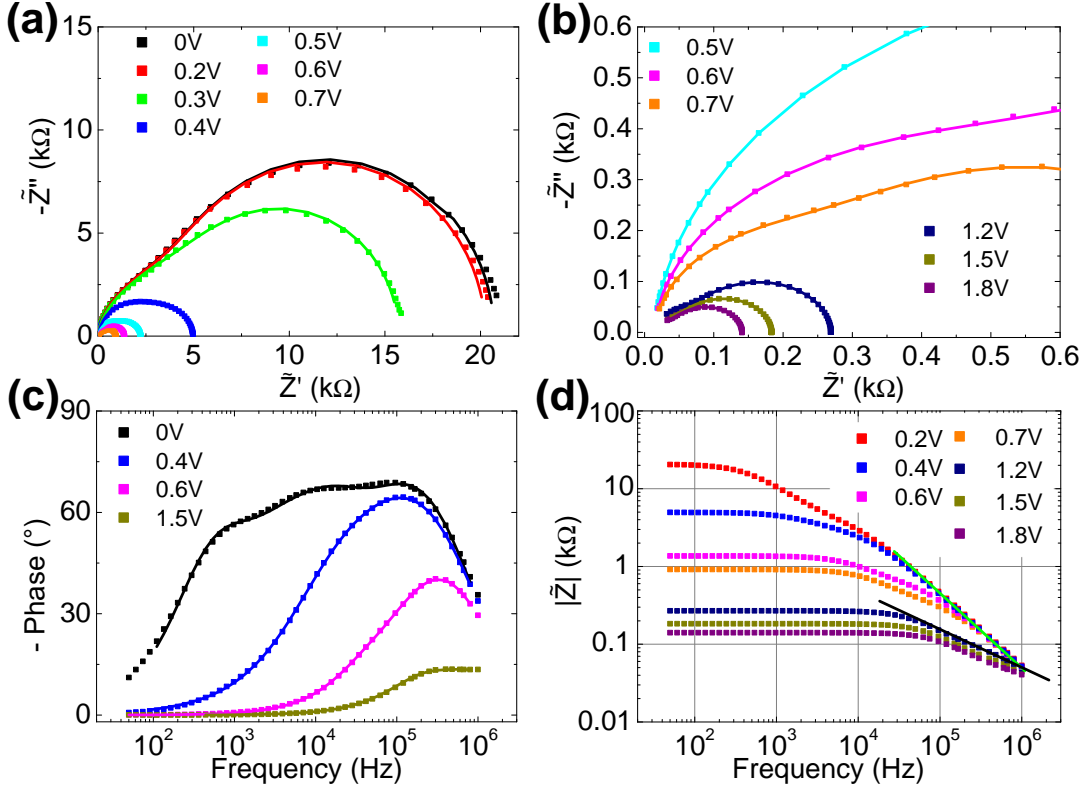
Figure 78: Measured impedance spectra (dots) for a forward biased organic pin-diode that consist of Al($50nm$)/ C$_{60}$:W$_2$(hpp)$_4$($50nm$, $3.1mol\%$)/ pentacene($70nm$)/ pentacene:F$_6$-TCNNQ($50nm$, $3.1mol\%$)/ Al($50nm$). The lines represent the fitting curves using the equivalent circuit as described in the text. The lines drawn in **(d)** indicate the slopes $\tilde{Z} \sim (i\omega)^{-1/2}$ (black line, diffusion impedance) and $\tilde{Z} \sim 1/\omega$ (light green line, series resistance limitation).

the diffusion impedance. This can be seen in the typical $\tilde{Z} \sim (i\omega)^{-1/2}$ behavior as indicated in Figure 78(d). The transition where this behavior starts is shifted to larger frequencies if the voltage is further increased. In the high frequency range $> 120kHz$ the influence of the geometrical capacitance can be seen in the typical $\tilde{Z} \sim 1/\omega$ dependence. This contribution disappears for voltages $> 1V$ since the diffusion path is increasingly conductive and dominates the impedance response. As can be seen in Figure 78, the measured impedance can be fitted in a very good quantitative agreement to the experimental data. In this context, it should be pointed out that this is done with a minimum amount of three parameters: r_m, c_m, and R_S (C_D is treated as constant). The particular effect of each parameter can be identified within the spectra. Focusing on Figure 78(d), the sum of R_S and $r_m w_I$ governs the ohmic behavior for low frequencies (constant impedance). On the other hand, the transition frequency $1/\tau_t$ from the constant impedance to the $\tilde{Z} \sim (i\omega)^{-1/2}$ region is determined by the product $r_m c_m$, and finally the transition from the $\tilde{Z} \sim (i\omega)^{-1/2}$ region to the $\tilde{Z} \sim 1/\omega$ region is described by the product of R_S and C_D[49].

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[49]Instead of using the simple diffusion model, it has also been tested to apply the more complex equivalent circuit which accounts for recombination. However, it turned out that the additional specific
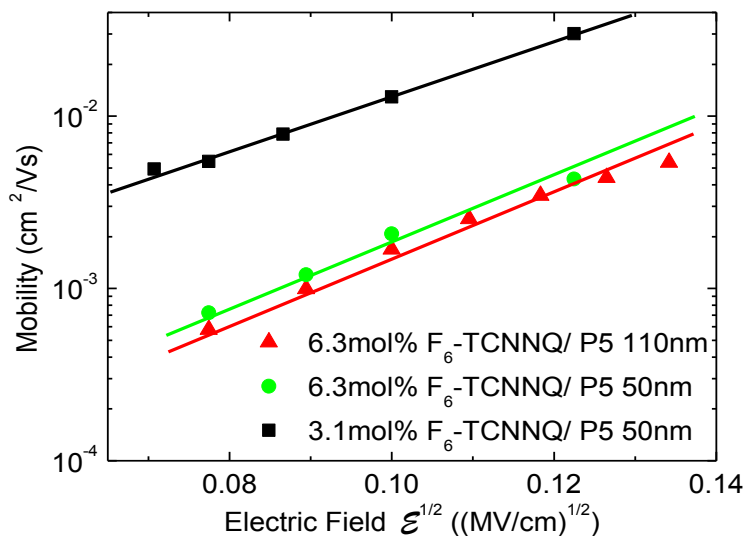
Figure 79: Charge carrier mobility within the intrinsic layer determined by impedance analysis for different interlayer thicknesses and different dopant concentrations. The layer sequence is described in the caption of Figure 78 and the colored lines indicated a Poole-Frenkel-like mobility behavior.

As result, one can take the fitting parameters c_m and r_m to compute the effective diffusion constant or charge carrier mobility of the charge carriers[50]. This estimation of diffusion constant or mobility is possible since in the simple diffusion model, recombination in the intrinsic layer is neglected. Hence, assuming that charge carriers recombine if they reach the opposite side of the junction, the diffusion constant can be determined from the transit time τ_t of charge carriers diffusing through the intrinsic layer by $D = w_I^2/\tau_t$[51]. Figure 79 shows the calculated charge carrier mobility (relying on Einstein's equation, compare Eq.60) for different dopant concentrations within the p-type doped layer and for different interlayer thicknesses. As can be seen, the charge carrier mobility shows a Poole-Frenkel-like behavior concerning the electric field which is applied across the intrinsic layer. However, two other features of the charge carrier mobility are of particular interest. Firstly, the determined mobility is independent of the chosen interlayer thickness and secondly, the mobility strongly drops for larger dopant concentrations within the hole transport layer. The first aspect basically proves the simple diffusion model since if recombination would play an important role, the determined diffusion constant (neglecting recombination) should strongly depend on the intrinsic layer thickness if the diffusion length is approaching its value. However, this contradicts the experimental findings and hence it can be justified

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resistance r_k is not required for fitting.

[50]Similar to the charge carrier mobility determined by SCLC's, the diffusion constant estimated by the impedance analysis represents an effective value for both charge carrier species.

[51]This calculation underestimates the diffusion constant since the diffusion of minority charge carriers into the doped layers is neglected. However, the minority charge carrier diffusion length within the doped layers is unknown.
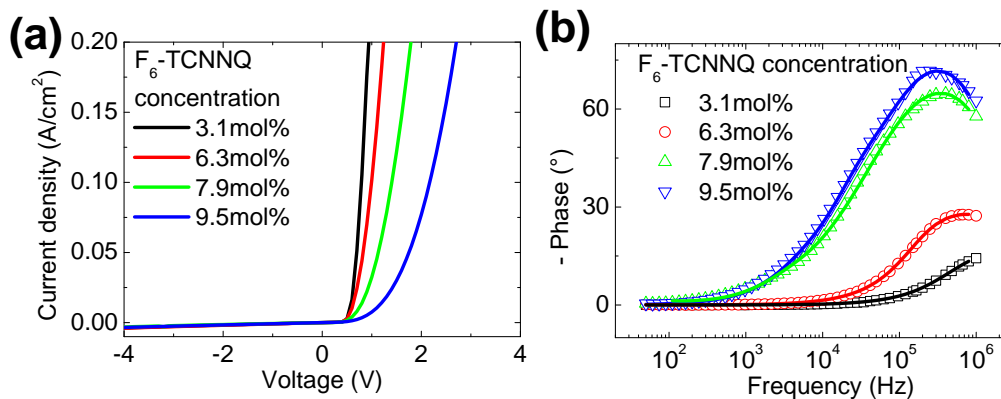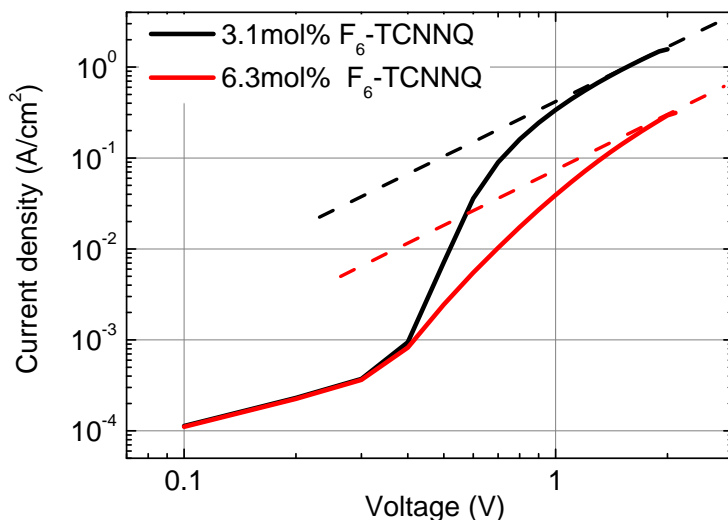
Figure 80: (a) I-V and (b) impedance curves for organic pin-diodes for different dopant concentrations of F_6-TCNNQ in the hole transport layer. The layer sequence is described within the caption of Figure 78. An interlayer thickness of $110 nm$ of pentacene is chosen. In (b) the measured impedance (open symbols) and the fitting curves (lines) are shown.

that recombination has been neglected.

At first glance, the dependence of charge carrier mobility on the p-type dopant concentration within the hole transport layer is not consistent with the small signal impedance model. A larger transit time is obtained for increased doping. However, doping of the transport layers should not directly affect the transport within the intrinsic layer and therefore the transit time. This contradiction can be clarified by reconsidering the assumptions employed for solving the diffusion-recombination equation. In particular, the doped transport layers are treated as reservoirs for charge carriers with an infinite conductivity and charge carrier mobility. Although this is warranted for doped C_{60} and slightly doped pentacene, it is violated for dopant concentrations within pentacene where the conductivity and the mobility drop owing to the structural phase transition (compare Figures 64 and 65). Hence, even if the mobility within the intrinsic layer is large, its conductivity is restricted by the hole transport layer. Therefore, the specific resistance r_m of the diffusion path is increased which finally leads to the fact that the transit time $r_m c_m$ is overestimated leading to a reduced mobility. The determined charge carrier mobility presumably reflects the hindered transport in the hole transport layer and owing to this, a good quantitative agreement of charge carrier mobility is found for OTFT measurements and the impedance analysis (compare Figure 64).

The effect of the doped hole transport layer on the I-V curves and the impedance spectra is visualized in Figure 80. In accordance to the previous discussion, strong doping of the hole transport layer gives rise to a reduced overall conductivity (compare Figure 65), which can be seen in the increased forward resistance of the diodes (see Figure 80(a)). The phase of the impedance, as displayed in Figure 80(b), confirms this effect. In particular, the phase for a given voltage is increased for larger dopant concentrations. This is due to the fact that the resistance r_m of the diffusion path is increased. In consequence, the device does not behave as a resistor but rather as a capacitor since the impedance is dominated by the contribution arising from C_D and R_S. Thus, the diffusion contribution is shifted to lower frequencies or even fully suppressed by the depletion capacitor. If C_D is

Figure 81: I-V curves of organic pin-diodes for different dopant concentrations of F_6-TCNNQ in the hole transport layer. The layer sequence is described within the caption of Figure 78. An interlayer thickness of $110nm$ of pentacene is chosen. The dashed lines indicated the SCLC behavior.

dominating the entire impedance response, an evaluation of the diffusion constant is not reliable owing to the negligible diffusion contribution. The highest dopant concentration where the diffusion constant can still be determined is $6.3mol\%$ of F_6-TCNNQ in pentacene.

In order to confirm this behavior of mobility, again a SCLC study is employed. Figure 81 displays the current-voltage curves of an organic pin-diode for two different dopant concentrations where for voltages $> 1.5V$ a SCLC-like behavior can be obtained. This behavior can be used to determine the charge carrier mobility as $9 \cdot 10^{-3} cm^2/(Vs)$ for $3.1mol\%$ and $2 \cdot 10^{-3} cm^2/(Vs)$ for $6.3mol\%$ of F_6-TCNNQ, respectively. These values are in accordance to the mobility obtained by impedance spectroscopy (compare Figure 79).

Transient analysis: The dynamic characterization of low gap organic diodes presented so far is incomplete in the sense that it covers the on-switching of the diode only. The on-switching is governed by transit time effects and thus basically by the charge carrier mobility. In order to describe the off-switching of the diode quantitatively, the recombination leading to the discharging of the diode has to be studied.

If a diode is driven by a pulsed voltage signal, charge carriers diffuse through the intrinsic layer in forward voltage direction and charge the opposite side of the junction (diffusion capacitance). If the voltage pulse switches the diode in reverse direction, charge carriers have to recombine as minority charge carriers in order to discharge the junction. As discussed within Subsection 2.2.4, this leads to an overshoot of the reverse current and its decay yields to the evaluated minority charge carrier life time.
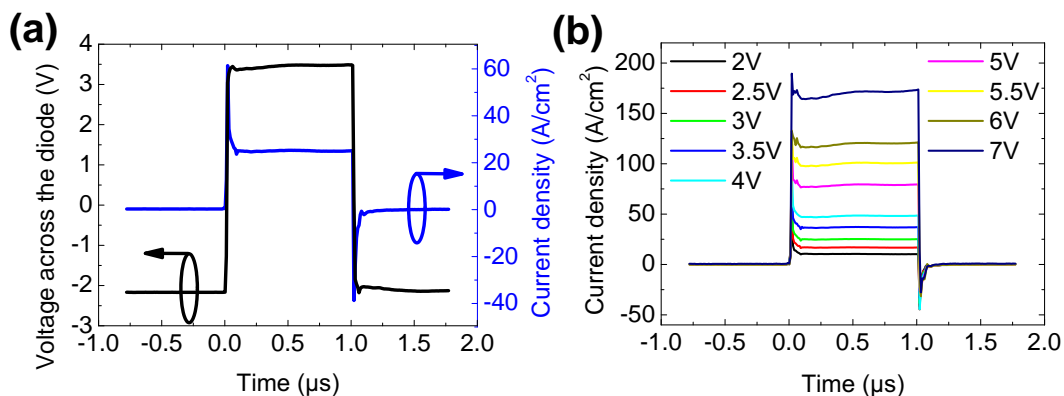
Figure 82: **(a)** Current response of an organic pin-diode on a short voltage pulse for different amplitudes **(b)**. The active area of the diode is $0.05\mu m \times 0.05\mu m$ and the device consists of: $Al(300nm)/$ pentacene:F_6-TCNNQ$(50nm,\ 0.8mol\%)/$ pentacene$(110nm)/$ C_{60}:W_2(hpp)$_4$($50nm$, $3.1mol\%$)/ $Al(300nm)$.
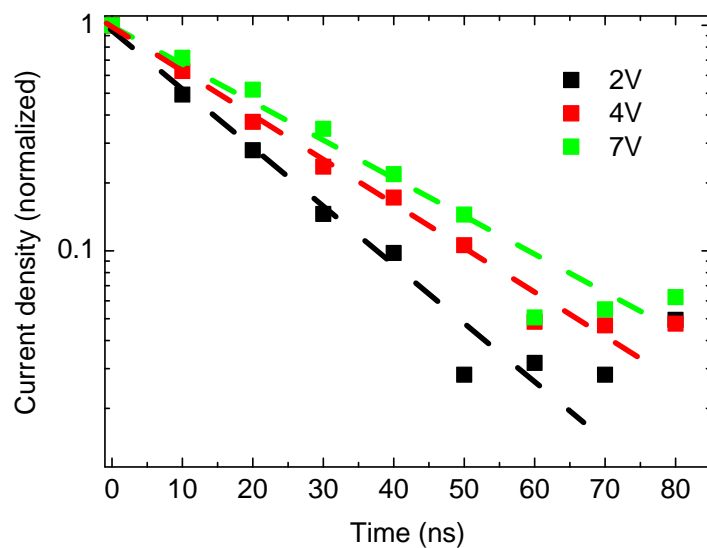
Figure 83: Extrapolation of the decay time t_2 for different voltages. The reverse current is normalized to its maximum value. The noise level of the current measurement is ~ 0.08 (normalized current).
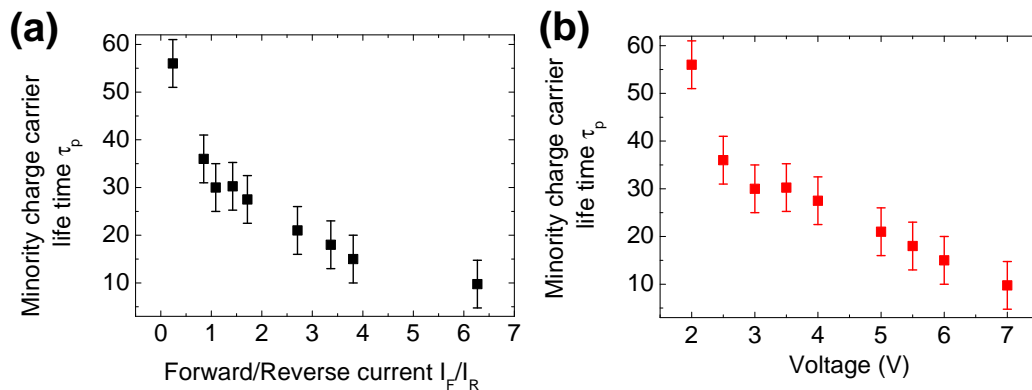
Figure 84: Minority charge carrier life time τ_p estimated according to Eq.81 for **(a)** different ratios between forward I_F and reverse current I_R and **(b)** different voltages. An error of $\pm 5ns$ for the minority charge carrier life time is deduced from the fit of t_2.

To study the fast response of organic diodes to short voltage pulses, the diode geometry has to be chosen with regard to the characteristic RC-time of the diode. This specifically means that the diode capacitance has to be so low that the RC-time of the series resistance and the depletion capacitance is smaller than the expected minority charge carrier life time. The diodes used for this study have an active area of $0.05\mu m \times 0.05\mu m$ which corresponds to a capacitance of $\sim 1.5pF$. Thus, with a series resistance of $\sim 3k\Omega$, the RC-time is estimated to be $4-5ns$. In Figure 82, the current response of a low gap organic pin-diode on a short voltage pulse is shown. Apparently, the diode can nicely follow the applied pulse and only at the flanks of the pulse, the diode shows a capacitive overshoot of current. As discussed within Subsection 2.2.4, the decay of this overshoot allows to analyze the discharging of the diode and hence to investigate the recombination mechanism. Focusing on the off-switching of the diode, an exponential decay of current can be obtained. The decay constant t_2 is correlated to the effective minority charge carrier life time of holes and electrons according to Eq.81. The evaluation of t_2 is illustrated in Figure 83 where also the exponential decay can be seen[52] [53]. In this way, the time t_2 is determined for different voltages or different ratios of forward to reverse current.

The calculated minority charge carrier life time according to Eq.81 for different voltages or different ratio between forward and reverse current is displayed in Figure 84. A large minority charge carrier life time of $\sim 55ns$ is obtained for small voltages $(2V)$. This time constant is continuously decreasing for larger forward voltages indicating a different recombination mechanism [54]. If the voltage is increased, more charges are stored in the diode and subsequently the minority charge

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[52] The noise level of the current is approximately 0.07 (normalized current). This can be improved by employing a load resistor with a larger resistance. However, this increases the RC-time of the diode and hence leads to a spurious time constant.

[53] For the measurement setup, the time resolution can be increased to $2ns$ (bandwidth of the oscilloscope $500MHz$). However, the bandwidth of the pulse generator $(200MHz)$ restricts the time resolution and first harmonics of the generator appear if the time resolution of the oscilloscope is set to $5ns$.

[54] According to Subsection 2.2.4, also a short period of a constant reverse current is expected (storage time). However, relying on the estimated minority charge carrier life time the calculated charge storage time (Eq.80) is in the range of $5ns$ and hence not detectable in a reliable way.

carrier density is enlarged. Depending on the charge carrier density, recombination can either occur via charge carrier trap states or via direct electron-hole recombination. If the density of charge carriers is increased, the dominant recombination mechanism will change from trap assisted recombination to direct electron-hole recombination. This transition presumably explains the obtained drop of the minority charge carrier life time.

The transient analysis is also performed for different dopant concentrations to study the influence of different impurity (dopant) concentrations. However, the difference for the various dopant concentrations lies within the range of the experimental errors. The diffusion length of minorities can be estimated by the evaluated minority charge carrier life time. Assuming an effective charge carrier mobility of $0.05 cm^2/(Vs)$ for holes and electrons in pentacene and furthermore relying on Einstein's equation, the diffusion length can be estimated to be $35-85nm$ depending on the applied voltage. It should be emphasized that this diffusion length characterizes the diffusion of minority charge carriers within the doped layers. The recombination within the intrinsic layer is presumably lower than in the doped regions. Hence, the diffusion length in the intrinsic layer is expected to be $>> 85nm$. This retrospectively justifies that the simple diffusion model neglecting recombination is employed to describe the transport through the intrinsic layer is valid.

5.3   Organic pin-Diodes at Ultra-High-Frequencies

In the two previous sections a complete large and small signal description of low gap organic pin-diodes is presented. Furthermore, the role of dopants acting as impurities is discussed and in this context organic diodes are optimized with the intention to design devices working at ultra-high-frequencies.

In the following section, the influence of device parameters such as interlayer thickness, dopant concentration, and device geometry on the UHF behavior is discussed. Beyond this, design rules for an optimized UHF operation are provided and moreover based on a small signal mathematical model of the diodes their frequencies cut-off behavior can be predicted. In this way, the cut-off frequency can be estimated to $1GHz$.

Although organic thin-film diodes as discussed within this work are vertical devices, their UHF behavior is not independent of the device geometry and effective area. This is basically due to the fact that the RC-time τ_{RC} of the diodes is not only governed by the resistance of the organic layers and the depletion capacitance, but also by the series resistance of the metallic contacts. However, as described in Subsection 2.2.4, the vertical quantities (depletion capacitance and resistance of the organic layers) obey another scaling law as the planar metal contacts. Figure 85 visualizes the different scaling behavior quantitatively using typical values for the depletion capacitance, the conductivity of the organic layers, and the resistance of the metal. As can be seen, the device performance is either limited by the metal contacts (feature size $> 1mm$) or by the resistance of the organic layers (feature size $< 100\mu m$). Hence, to achieve a high cut-off frequency, the feature size of the diodes has to be in the range of $100-200\mu m$. A further reduction of the feature size leads to a counterproductive behavior since firstly, τ_{RC} is not reduced
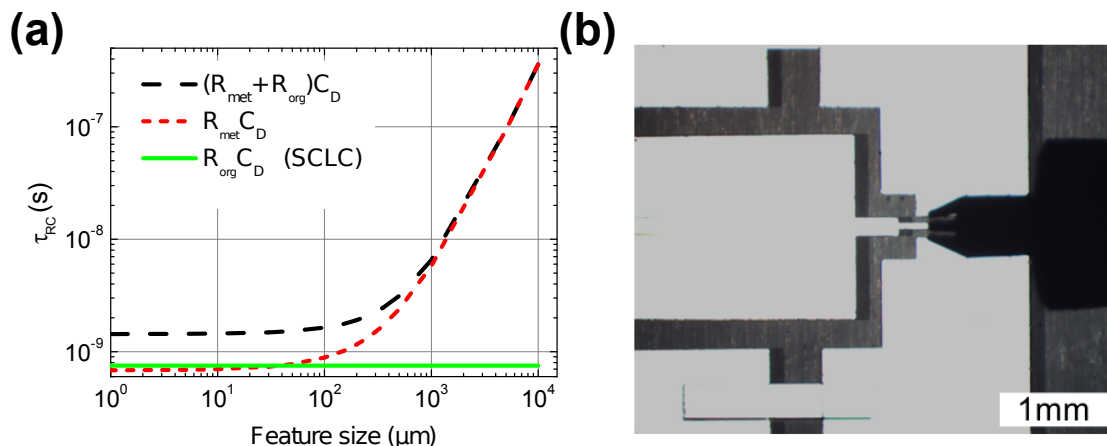
Figure 85: (a) Estimation of the characteristic RC-time of the diode (depletion capacitance times resistance) using reasonable values of mobility ($0.2 cm^2/Vs$), metal conductivity and interlayer thickness ($110 nm$). The lower limit for the RC-time is always dominated by the resistance of the organic layers. **(b)** Photograph of a UHF probe needle touching the metal electrodes of the organic UHF diode.

and secondly, the total resistance of the device, with respect to the external load, is increased which causes an increased power loss.

Owing to these considerations, organic diodes possessing different active areas of $50 \times 50 \mu m^2$, $100 \times 100 \mu m^2$, and $200 \times 200 \mu m^2$ are fabricated. Furthermore, the thickness of the metal layers is set to $300 nm$ to effectively reduce the series resistance of the contacts.

However, besides the adjustment of the RC-time of the diodes, another indispensable demand in order to measure electronic devices at UHF conditions is to design the electrode geometry with respect to the appearance of resonances in the metallic wave guides. In order to address this issue, a special electrode geometry (see Figure 85(b)) is chosen, which firstly is free of resonances in the investigated frequency range and secondly fits to a wafer prober stage with a sophisticated probe needle. The small signal impedance response of this electrode configuration containing a diode ($100 \times 100 \mu m^2$) is shown in Figures 86 and 87. A phase of almost $-90°$ and a modulus of the impedance inversely proportional to the applied frequency suggest that the circuit can be described by a RC-unit. This is confirmed by the calculated capacitance (Figure 87) which matches the expected depletion capacitance of $5.5 pF$. However, a swing of the phase, which indicates a first resonance, can be obtained for frequencies $> 1 GHz$ (higher harmonics are also visible). This resonance is caused by the inductance of the metal contacts and the capacitance of the diode. It can be shifted to higher frequencies if diodes possessing a smaller capacitance are employed. Nevertheless, this geometry of the metal contacts is suitable to characterize organic pin-diodes with an active area of $100 \times 100 \mu m^2$ without resonances up to $1 GHz$.

In the following, the influence of the active area, the dopant concentration, and the interlayer thickness on the performance of organic diodes embedded in such a UHF electrode configuration is discussed.

The doping concentration and the interlayer thickness are the key parameters that
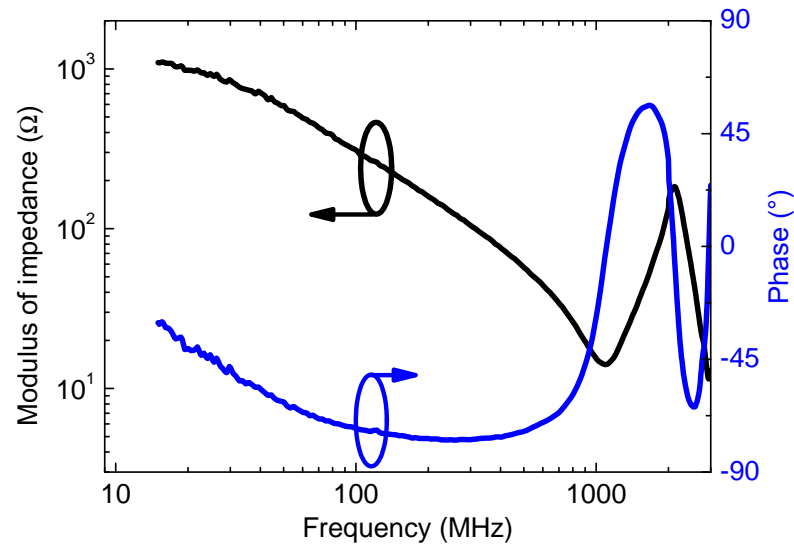
Figure 86: Modulus of impedance and phase of the metal contact configuration used for UHF measurement (compare Figure 85). An organic diode (active area $100 \times 100 \mu m^2$) is embedded in the electrode configuration. Measured without bias voltage.
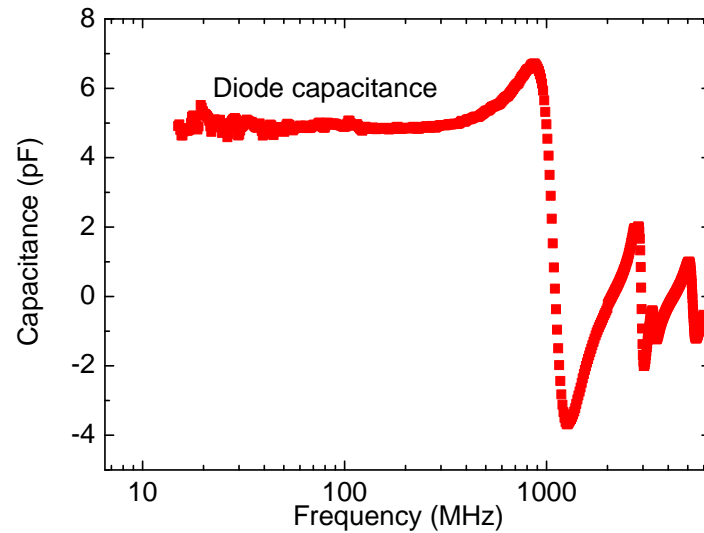
**Figure 87:** Capacitance-frequency for the metal electrode configuration shown in Figure 85. An organic diode (active area $100 \times 100 \mu m^2$) is embedded in the electrode configuration. Its depletion capacitance is approximately $6pF$. Measured without bias voltage.
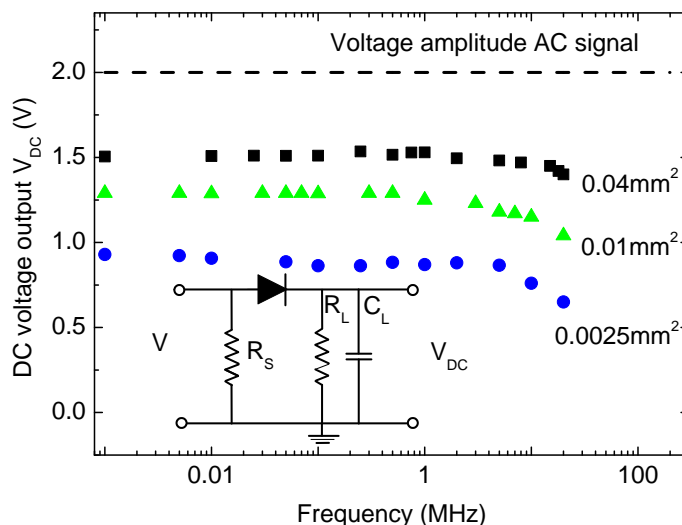
Figure 88: Frequency dependence of the DC voltage output of organic pin-
diodes for a sinusoidal input voltage (dashed line) of $2V$ ampli-
tude measured in a rectifier circuit (see inset).   Black boxes rep-
resent a pin-diode with an area of $0.04mm^2$ (pentacene interlayer
thickness $90nm$), green triangles $0.01mm^2$ (pentacene interlayer thick-
ness $120nm$), and blue circles $0.0025mm^2$ (pentacene interlayer thick-
ness $110nm$).   The inset displays the employed rectifier circuit with
$R_S = 50\Omega$, $R_L = 1M\Omega$, and $C_L = 39nF$.   The layer sequence for
the pin-diodes is Al($300nm$)/ pentacene:F_6-TCNNQ($50nm$, $0.8mol\%$)/
pentacene(xnm)/ C_{60}:W_2(hpp)$_4$($50nm$, $0.8 - 1.6mol\%$)/ Al($300nm$).

are technically adjustable in order to optimize the I-V performance of organic
diodes (compare Section 5.2). Thus, the question arises, how one can use this
knowledge to design UHF diodes with optimized output characteristics? The ac-
tive device area of the diode is reduced in order to overcome restrictions by the
geometrical capacitance. In Figure 88 the DC output voltage of a rectification
circuit (see inset) for a sinusoidal input signal (amplitude $2V$) is shown. Within
this graph the frequency is varied from $1kHz$ to $20MHz$. This DC output volt-
age is displayed for devices possessing different active areas as described above.
The rectification circuit provides a nearly constant DC voltage over a broad fre-
quency range. However, a drop in DC voltage output is observed for frequencies
$> 10MHz$ which might indicate a limitation by the internal RC-time (series resis-
tance of the organic layers times geometrical capacitance) of the diode. This time
constant, however, is independent of the area since vertical devices are considered
here. Nevertheless, low capacitance devices are favorable since the series resistance
which is related to wiring does not scale in the same manner if the device area is
reduced. Thus, if the DC output voltage is compared for different active areas,
one can observe a reduced DC output for smaller active areas. This behavior orig-
inates from a changing ratio between the external load and the series resistance of
the diode. Thus, if the active area is reduced, the series resistance of the diode is
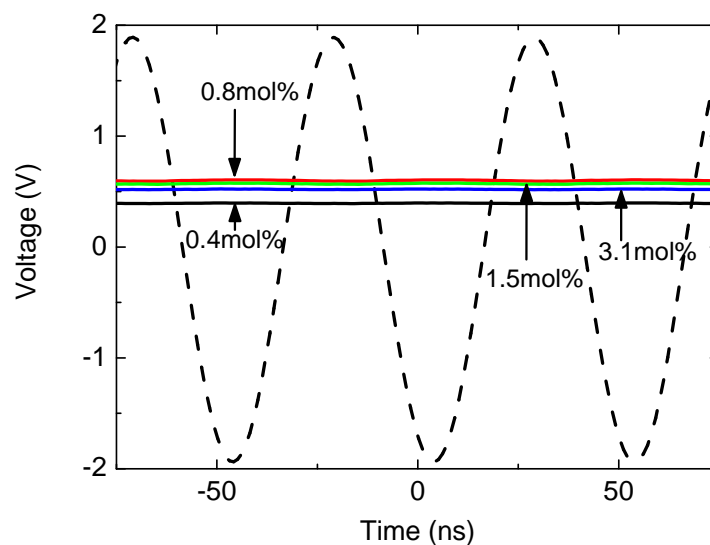
Figure 89: Time resolved response of an organic pin-diode to a sinusoidal input
voltage (dashed line) of $20MHz$ and an amplitude of $2V$. The colored
lines show the output voltage for different p-type dopant concentrations
measured over a $1M\Omega/$ $39nF$ load for 0.0025mm^2 devices. The layer se-
quence for the pin-diodes is $\text{Al}(300nm)/$ pentacene:F_6-TCNNQ($50nm$,
$xmol\%$)/ pentacene($200nm$)/ C_{60}:W_2(hpp)$_4$($50nm$, $0.8 - 1.6mol\%$)/
$\text{Al}(300nm)$ and the colored lines denote $0.4mol\%$ (black), $0.8mol\%$
(red), $1.5mol\%$ (green), and $3.1mol\%$ (blue) of F_6-TCNNQ in pen-
tacene.
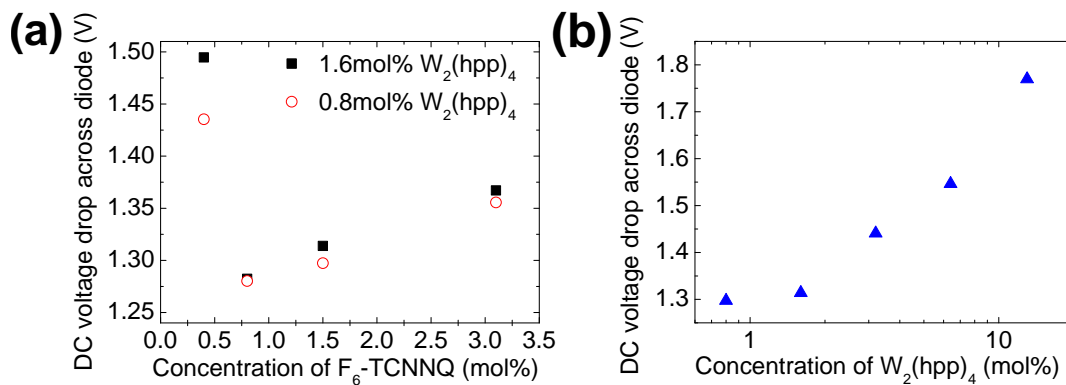
Figure 90: Voltage drop across the diode (input voltage amplitude minus the voltage measured over the load) for different p-type **(a)** and n-type **(b)** dopant concentrations (input voltage $20MHz$, $2V$ amplitude, active area $0.0025mm^2$). The layer sequence for devices shown in **(a)** and **(b)** is described in the caption of Figure 89. The last two points ($6.4mol\%$ and $13mol\%$ of $W_2(hpp)_4$ in C_{60}) in **(b)** are recorded for nip structures with a pentacene interlayer thickness of $110nm$ and a p-type dopant concentration of $3.1mol\%$ of F_6-TCNNQ in pentacene.

enlarged in comparison to the load circuit which leads to a reduced DC output. In Figure 89, time resolved measurements of the rectified sinusoidal input signal ($20MHz$, amplitude $2V$) are presented. As can be seen, a dependency of the dopant concentration on the output voltage is obtained. The highest output voltage for $0.0025mm^2$ devices is achieved for a dopant ratio of $0.8mol\%$ of F_6-TCNNQ in pentacene. Ohmic losses across the hole transport layer lead to a reduced DC voltage output for lower dopant concentrations. However, also for dopant ratios $> 0.8mol\%$ of F_6-TCNNQ a reduced voltage output is observed. This additional loss in output voltage is likely caused by the increased leakage current level and subsequently the reduced rectification ratio (compare Figure 73). Accordingly, the reduced rectification ratio gives rise to a discharging of the load capacitor via the reverse resistance of the diode in addition to the load resistance. The loss in DC voltage output for different p- as well as n-type dopant concentrations is shown in Figure 90. In particular, for p-type doping, an optimum in DC voltage output is found for $0.8mol\%$ F_6-TCNNQ in pentacene. For this dopant concentration, the leakage current is minimal, but the doping is still sufficiently high to reduce the contact and layer resistance. Such an optimum of DC voltage output is not reached in case of n-type doping. However, from the saturation behavior between $0.8mol\%$ and $1.6mol\%$ of $W_2(hpp)_4$ in C_{60} (see Figure 90(b)), it can be concluded that $0.8mol\%$ of dopants is close to this optimum. Moreover, devices with a dopant concentration of $0.4mol\%$ of $W_2(hpp)_4$ in C_{60} are not working stable, which is likely caused by the appearance of an interface barrier between the doped C_{60} layer and the metal contact. Nevertheless, Figure 90 clearly shows that more than $0.5V$ in voltage output can be gained for devices with optimized dopant ratios. It should be mentioned that the absolute value of the voltage drop across the diode depends on the device geometry as well as the external load. Therefore, it is merely used to compare the output characteristics of equivalent devices having the same geometry

and being connected to the same external circuit.

The main argument for the optimized performance at $0.8 mol\%$ F_6-TCNNQ dopant concentration is the reduced leakage current. However, from a physical point of view the dynamics of charge carrier transport in the doped layers are of particular interest. For both materials C_{60} and pentacene doping can cause a loss in mobility. While for C_{60} a continuous decrease in mobility by doping is reported [56], an abrupt transition is observed for pentacene (compare Section 5.1.2). This transition in mobility is caused by a structural phase transition in pentacene induced by the molecular dopants. In case of F_6-TCNNQ, this structural phase transition appears for a dopant concentration of approximately $3.1 mol\%$. As discussed, the pin-diodes obey in forward voltage direction a SCLC law which is governed by the intrinsic interlayer. Subsequently, a moderate loss in charge carrier mobility within the doped charge transport layers does not necessarily lead to a reduced forward current. This is related to the fact that the doped charge transport layers are significantly thinner than the intrinsic layer. Therefore, for the considered range of doping the loss of mobility is not dominating the diode performance and thus also not influencing the cut-off frequency. Such effects might appear for larger dopant concentrations ($> 1.5 mol\%$). However, they are likely superimposed by other effects induced upon doping such as the increased leakage current level.

The role of the interlayer thickness at ultra-high-frequencies is twofold. Firstly, it determines the characteristic RC-time of the device and secondly, it determines the ratio between the external load and the impedance of the diode. In Figure 91, the influence of the interlayer thickness on the DC voltage output at $20 MHz$ is presented. In accordance to the previous discussion, a reduced interlayer thickness leads to a reduced series resistance of the diode and therefore to a smaller voltage loss across the diode. Thus, the linear behavior between voltage loss and interlayer thickness can be understood by a voltage divider between the load resistance and the series resistance of the diode. In other words: the thinner the interlayer, the larger the DC voltage output. Unfortunately, in the present case a minimum of interlayer thickness is required in order to provide a sufficient blocking of reverse current. A thickness of $90 nm$ pentacene exhibits an optimum for the trade-off between lowest forward resistance and highest reverse resistance.

To highlight the potential of the presented diodes, they are characterized up to a frequency of $300 MHz$ which is the limit of the oscilloscope. As shown in Figure 92, an almost constant DC voltage output in the range from $1 kHz$ to $10 MHz$ is observed. Beyond $10 MHz$ the rectified DC voltage drops with increasing frequency. Nevertheless, at $300 MHz$ still a DC voltage of $0.5 V$ with a small ripple amplitude of $0.13 V$ is obtained. From this decay it can be concluded by extrapolation that these diodes are able to provide a DC voltage output up to frequencies close to $1 GHz$.

This estimation is in accordance to transit time predictions. As discussed in Subsection 2.2.4, two different approaches have been suggested in this context. In a first transit time model, the maximum frequency f_{max} is derived according to [68]
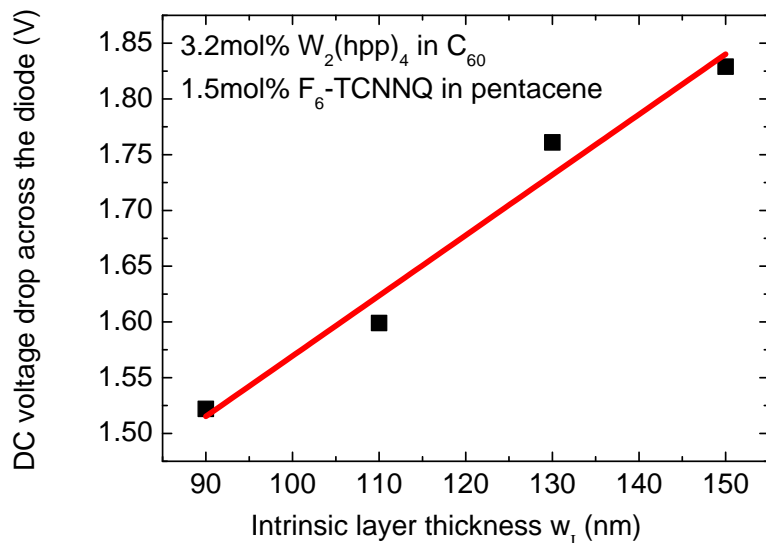
Figure 91: Voltage drop across the diode for different interlayer thicknesses (input voltage $20MHz$, $2V$ amplitude, active area $0.0025mm^2$) in case of a pin-diode. The layer sequence is described in the caption of Figure 88. The red line shows a linear fit of the data points.
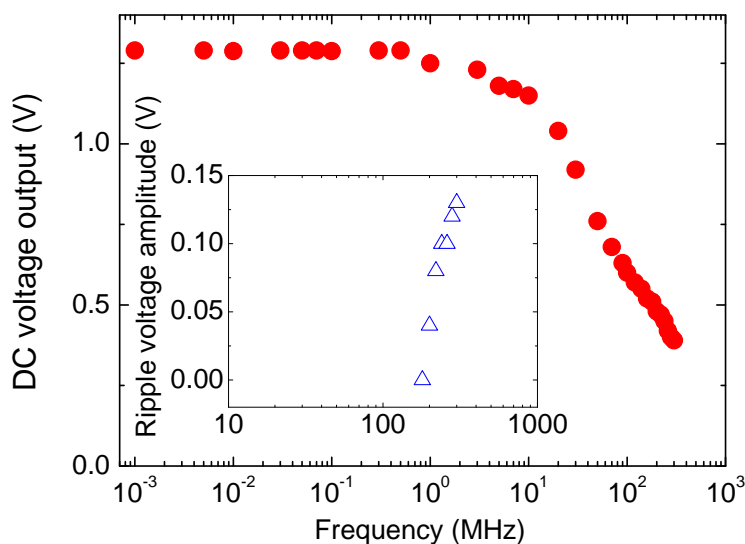
Figure 92: Frequency dependence of the DC voltage output and the ripple voltage amplitude of an organic pin-diode for a sinusoidal input voltage of $2V$ amplitude. The active area of the pin-diode is $0.01mm^2$. The layer sequence for the pin-diode is Al($300nm$)/ pentacene:F_6-TCNNQ($50nm$, $1.5mol\%$)/ pentacene($120nm$)/ C_{60}:W_2(hpp)$_4$($50nm$, $0.8mol\%$)/ Al($300nm$).

as

$$f_{\max} = \frac{1}{\tau_{drift}} = \frac{\mu}{w_I^2}(V - V_{DC}), \tag{115}$$

where V is the amplitude of the applied AC signal and V_{DC} the DC voltage measured across the load resistance. However, this simple model assumes a constant field in the diode and does not take the field dependent mobility of organic materials into account. Therefore, the maximum frequency is underestimated by this model. The second approach, reported by Steudel et al. [68, 184], derives the maximum frequency as

$$f_{\max} = \frac{9\mu}{16\pi w_I^2 V_{DC}}\Big((V^2 + V_{DC}^2)arccos(\frac{V_{DC} + V_F}{V})$$
$$+ (-3V_{DC} + V_F)\sqrt{V^2 - (V_{DC} + V_F)^2}\Big), \tag{116}$$

where V_F is the transition voltage (where the SCLC regime starts) of the diode, assuming space charge limited currents. Thus, it is mainly suited for voltages larger than V_F, where the diode shows a clear SCLC behavior. Accordingly, both approaches cannot provide exact values for the maximum frequency in case of the low voltage pin-junctions reported here. Nevertheless, Eq.115 is utilized to estimate a limit for the cut-off frequency. Assuming a charge carrier mobility of $\sim 0.2 cm^2/(Vs)$, taking an intrinsic layer thickness of $120nm$, and a DC voltage of $1.25V$, one can compute a cut-off frequency of $\sim 1.04GHz$ which is in accordance to the experimental findings. However, this is a lower limit for the cut-off frequency since Eq.115 is derived under the assumption of an Ohmic behavior. Thus, the stronger voltage dependence of the SCLC will lead to a higher cut-off frequency.

A large signal simulation of the rectification circuit using the small signal quantities determined within Subsection 5.2 is employed to confirm the experimental findings. In this simulation, the diode is described by its depletion capacitance, its forward resistance, its reverse leakage current, and the minority charge carrier life time. More specifically, the forward resistance is obtained from the experimental I-V curves fitted by the ideal Shockley equation and a SCLC in series (the data is taken from the fit shown in Figure 70). The depletion capacitance is taken from the impedance analysis shown in Figure 87 and the minority charge carrier life time is adopted from the transient analysis performed in Section 5.2. In this way, the time dependent response of the diode, the load resistor, and capacitor is mathematically described by a 2nd order differential equation which is solved numerically. The dynamic modeling of the diode is realized as described by Kuno [185] (charging and discharging of the diode (capacitor) including the minority charge carrier recombination). As shown in Figure 93, the model describes the cut-off behavior of the DC voltage output in a good quantitative agreement to the experimental results. A main conclusion which can be drawn from the simulations is that the cut-off behavior is caused by both the limited forward conductance as well as minority charge carrier life time. A reduced forward conductance (equivalent to a thick interlayer, or a low mobility, or a low transit time) leads to a shift of the whole curve shown in Figure 93 towards lower DC voltages. Accordingly, also the cut-off frequency is lowered. Contrary, the minority charge carrier life
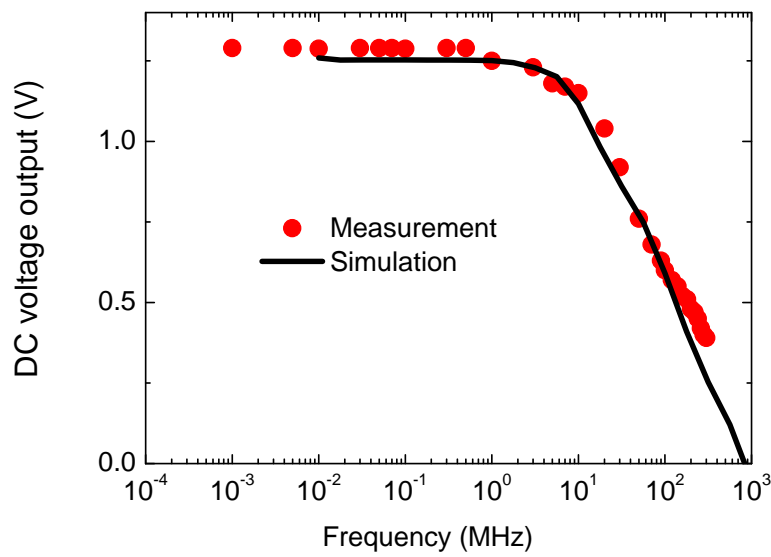
Figure 93: Experimental results (red circles) of the DC voltage output as shown in Figure 92 vs. simulation results ($2V$ amplitude of the input signal, active area $0.01mm^2$). The parameters for the simulation are: depletion capacitance $C_D = 6pF$, series resistance of the diode $R_S = 200\Omega$, ideality factor of the diode $\eta_D = 1.7$, effective charge carrier mobility (SCLC) $\mu = 0.2cm^2/(Vs)$, and a minority charge carrier life time $\tau_p = 15ns$. Latter quantity is used as parameter to match the simulated curve to the experimental results.

time does not affect the low frequency region where the DC voltage output is constant. However, it influences the onset of the voltage drop that can be found at approximately $10MHz$. Within this context, the cut-off of the DC voltage output can be interpreted as follows. According to the estimation of transit time, the cut-off frequency of $1GHz$ is presumably governed by the on-switching of the diode and therefore by the transit time and the forward conductance. Contrary, the onset and the slope of the voltage loss is dominated by the minority charge carrier life-time. However, both effects are not clearly separable since if the frequency is approaching the inverse transit time also less charges are stored in the diode during the forward voltage period of the input signal. Hence, also the discharging is faster.

In general, the influence of the minority charge carrier life time on the cut-off behavior is highly complex since according to Figure 84, τ_p is not independent of the applied voltage and hence the ratio between the forward and reverse current. This leads to the fact that τ_p is changed if the DC voltage output is reduced with increasing frequency. Moreover, the cut-off behavior depends on the external load circuit. In particular, since the cut-off behavior is caused by a discharging of the load capacitor via the diode, the ratio between the reverse resistance of the diode and the load resistor governs the voltage loss quantitatively.

Nevertheless, the large signal simulations can provide a first quantitative insight to the UHF behavior of organic diodes and furthermore they allow to study the influence of the different time constants on the UHF cut-off behavior.

Summary

In this chapter, organic pin-diodes comprising molecular doped layers of pentacene and C_{60} are chosen as prospective candidates for organic UHF devices. In order to make organic diodes applicable at UHF conditions, it is not only necessary to investigate and understand material specific properties of charge carrier transport, but it is also important to consider the fundamentals of device operation.

The first aspect concerning charge carrier transport is of particular importance since a large conductivity and charge carrier mobility are required for UHF operation. In this context, molecular doping is a key technology to control the conductivity of organic semiconductor layers. However, dopants act as impurities in the matrix materials and hence they affect charge carrier transport. In the present study, the influence of molecular doping on the structural and electronic properties of pentacene is revealed. In particular, the doping induces a structural phase transition from a poly-crystalline to an amorphous phase. Owing to this change in thin-film morphology, charge carrier mobility strongly drops upon doping. However, it is shown that for moderate dopant concentrations ($< 1.5mol\%$ of F_6-TCNNQ) where the films remain poly-crystalline, a strong increase of conductivity is obtained, while charge carrier mobility is only slightly affected.

Employing this knowledge, organic pin-diodes with an optimized performance concerning rectification ratio and forward conductance are fabricated. This adjustment of diode performance is either accomplished by the interlayer thickness or the dopant concentration. Moreover, a complete small signal model is developed

which is suitable to describe and predict the behavior of these organic devices at UHF conditions.

In order to confirm the UHF ability of these devices, an electric characterization up to $300MHz$ is presented. In particular, it is demonstrated that the design rules as deduced from the static characterization allow for an improvement of the UHF performance. Using such optimized devices, a DC voltage output of almost $1.4V$ for a sinusoidal input signal of $20MHz$ (amplitude of $2V$) is obtained. Furthermore, the UHF measurements confirm that the diodes operate up to $300MHz$ which allows to estimate a cut-off frequency in the range of $1GHz$.

Chapter VI

Fluorine Based Photo-Lithography: a Patterning Technique compatible to Organic Semiconductors

'It is fortunate that physicists suffer the genetic defect of optimism.'

L.M. Lederman, physicist.

In this chapter, the concept of fluorine based photo-lithography is presented and how it can be adopted to small molecule organic semiconductors. In particular, it will be shown that this technique is suitable for high resolution patterning of p- and n-channel OTFTs (pentacene and C_{60}) under ambient conditions. The OTFT performance is only slightly affected by the structuring procedure, which can be explained by a detailed study including OTFT characterization and X-ray photoelectron spectroscopy (XPS). Hence, fluorine based photo-lithography exhibits a powerful method for structuring of organic semiconductor materials.
However, as will be pointed out, down-scaling of OTFTs is restricted by injection of charge carriers from the source electrode. This effect leads to deviations from the gradual channel approximation and therefore from OTFT scaling laws.
The work presented in this chapter is reported in reference [172].

6.1 The Concept of Fluorine Based Photo-Lithography

The compatibility of organic materials and device concepts to high resolution, cost-effective patterning techniques exhibits a major requirement in order to warrant their commercial success. In particular, down-scaling and high density integration of OTFTs is essential to overcome current performance limitations and to make OTFTs become a prospective device for applications e.g. in active matrix displays [104] or organic microprocessors [103].

Various methods for structuring of organic semiconductors like shadow mask deposition, laser ablation, inkjet printing, or nano-imprinting have been suggested. However, they are either lacking in their throughput capacitance, accessible feature size, or their compatibility with the organic compounds themselves. Photo-lithography on the other hand is a very powerful technique which is currently adopted as a standard patterning approach for inorganic electronic industry. However, except of some limited cases [186, 187], conventional photo-resist, developer, and solvent compounds (using e.g. tuluol and alkaline solvents) are not applicable to organic materials.

A possible approach for photo-lithography on organic materials relies on using sacrificial protection layers. These layers protect the active material from the wet chemicals during the lithographic process and can be either removed or left as a functional part of the device [151, 188–190]. This concept is beneficial owing to its versatility and its potential compatibility to a wide class of organic materials. Here, this approach, which has been reported for patterning of polymers [151, 188–190], is adopted to small molecule organic semiconductors. As shown in Figure 94, photo-resists and solvents used for photo-lithographic patterning are based on highly fluorinated compounds. Therefore, such materials are highly hydrophobic and inert concerning reactions with typical organic semiconductors. These properties enable the use of fluorinated photo-resists as protection layers for organic semiconductors. Furthermore, their hydrophobic character warrants the combination with conventional photo-resist compounds using hydrophilic developer solutions.

In this subsection, the development of a photo-lithography recipe which allows to structure C_{60} and pentacene OTFTs in a top source/drain geometry under ambient conditions is described. As it will be pointed out, material properties of the organic semiconductors such as layer adhesion, surface roughness, and sensitivity to oxygen and moisture, can strongly affect the photo-lithography recipe. In the following, the influence of the patterning procedure on the performance of OTFTs is discussed.

Structuring on organic materials is performed with the intention to fabricate OTFTs. Therefore, a highly doped silicon substrate covered with Al_2O_3 ($23nm$ or $50nm$ in this study) is used as gate electrode and gate insulator, respectively. After substrate cleaning and surface preparation (compare Subsection 3.4), a layer of either C_{60} ($40nm$) or pentacene ($25nm$, $40nm$, and $80nm$) is deposited under vacuum conditions (see Figure 95(a)).

Subsequently, the samples are taken out of the vacuum chamber, and are exposed to air the first time. A first layer of lift-off resist (*Ortho* 310 - negative resist,
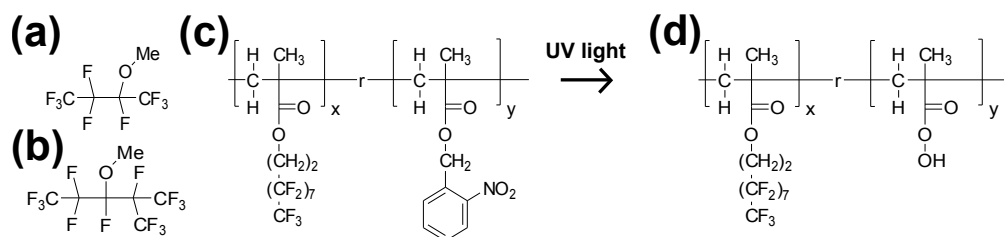
Figure 94: Chemical structures of fluorinated solvent and photo-resist compounds. The structures denote **(a)** HFE 7100, **(b)** HFE 7300, **(c)** photo-sensitive photo-resist (soluble in HFE solvents), and **(d)** photo-resist after UV light exposure (insoluble in HFE solvents).
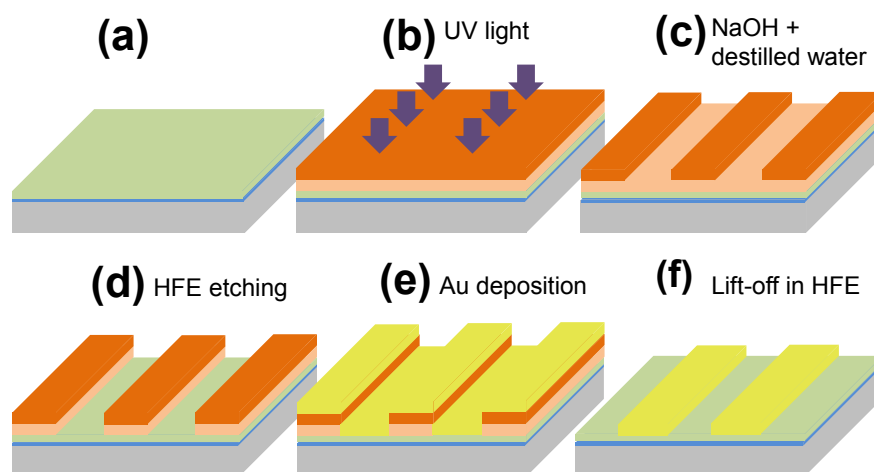
Figure 95: Scheme of the patterning procedure containing **(a)** resist coating, **(b)** exposure, **(c)** development, **(d)** etching, and lift-off **(e)**+**(f)**. The layers are: silicon substrate (light gray), Al_2O_3 (blue), organic semiconductor (green), $Ortho$ 310 (light orange), $ma-P1210$ (orange), and gold (yellow).

Orthogonal Inc.) is spin-coated ($3000rpm$, $30s$, thickness $1\mu m$) under ambient conditions directly onto the organic material (see Figure 95(b)). $Ortho$ 310 acts as a protective resist since it is based on fluorinated photosensitive polymers which are chemically benign to non-fluorinated organic compounds. It is processed (deposited, etched, and stripped off) by hydrofluoroether (HFE) solvents (compare Figure 94). However, it should be mentioned that $Ortho$ 310 only protects the organic semiconductor from the wet chemicals, but it is transparent to oxygen. The second role of $Ortho$ 310 is its use as lift-off resist. This is possible due to the mutual orthogonality of $Ortho$ 310 and non-fluorinated commercial imaging resist. Thus, processing of $Ortho$ 310 does not influence the imaging resist and vice versa. An imaging resist ($ma-P1210$, positive resist from micro resist technology GmbH, Berlin, thickness $1\mu m$) is spin-coated onto $Ortho$ 310 using the same procedure and it is exposed by the SF-100 UV broadband exposure system (Figure 95(b)). The exposed parts of $ma-P1210$ are removed by development in $NaOH$ solution[55] for $17s$ (Figure 95(c)) and rinsing in deionized water. Afterwards, $ma-P1210$ serves as an etching mask for $Ortho$ 310. This pattern of $ma-P1210$ resist is

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[55]Developer $ma-D$ 331, micro resist technology GmbH, Berlin

transferred to *Ortho* 310 by etching with HFE solvents (Figure 95(d)). The gold is deposited through the resist stencil and finally spare gold is removed via lift-off using HFE 7100 in a nitrogen atmosphere (Figure 95(e)+(f)). Apart from (f), all other steps of the structuring protocol are done under ambient conditions in air. The total exposure time to oxygen and moisture is $\sim 30min$.

Although this recipe suggests a straightforward processing, the procedure has to be modified depending on the specific organic material. Since photo-lithography is a multi-step process some conditions are kept constant in order to identify crucial parameters. In particular, for the present study, resist deposition and development time remain unchanged. Ideal processing parameters with the highest reliability, independent of layer thickness, are found for C_{60} as:

- exposure time $0.6s$ (reduction mode),

- development in $NaOH$ for $17s$,

- rinsing by deionized water,

- and spin-rinsing by HFE 7100 for $50s$ ($3000rpm$).

These conditions allow for a high resolution patterning on C_{60} without a notable influence on the organic layer (compare Figure 96).

For pentacene, however, the adaption of the patterning recipe requires more effort. In particular, the surface roughness and the weak substrate adhesion of pentacene films need major modifications of the photo-lithography recipe. In Figure 96 pentacene films of various thicknesses ($80nm$, $40nm$, and $25nm$) are shown after the lift-off process using the same procedure as established for C_{60}. Apparently, there are strong differences in layer coverage and optical contrast for the different thicknesses. In detail, for $80nm$ of pentacene, the layer is non-uniform, contains large defects, and looks perforated. This effect is reduced for $40nm$ of pentacene and even vanishes for $25nm$ where a uniform layer can be observed. As argued in Subsection 5.1, the layer roughness of pentacene films lies in the range of the layer thickness. This property can explain the different optical contrast obtained in the microscope images. Furthermore, the layer roughness leads to a different adhesion of photo-resist and organic semiconductor. In particular, since the layer roughness is increased also the effective contact area between photo-resist and pentacene is increased. Hence, if the HFE solvent creeps underneath the photo-resist in order to lift it off, the photo-resist entrains the pentacene film. This is caused by the fact that owing to the large contact area, the adhesion of pentacene to the photo-resist is larger than the adhesion to the substrate. This influence leads to the appearance of defects as obtained in Figure 96(b). If the pentacene layer is thinner, this effect is reduced which also increases the yield of the lift-off process. In general, for the chosen layer thicknesses the lift-off yield increases from $< 20\%$ for $80nm$ of pentacene to $> 80\%$ for $25nm$ thick films. Hence, for a structuring of pentacene films, the layer thickness should be preferably $< 40nm$.

However, caused by the roughness of pentacene, also other parameters such as resist treatment, exposure time, and etching procedure (compare Figure 96(d)) have to be modified. The thickness of the photo-resist is expected to be larger than for C_{60} which is related to the better resist adhesion. Therefore, also larger exposure durations are required. In detail, for $25nm$ thick pentacene films the dose
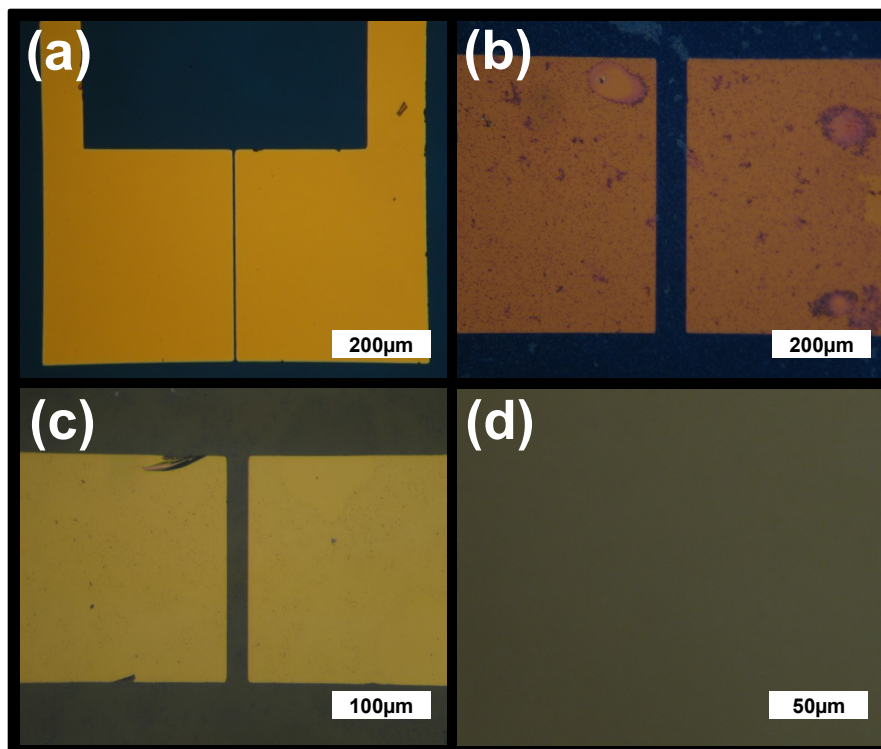
Figure 96: Optical microscope images of organic materials after a lift-off process as described in the text. The images show **(a)** C$_{60}$ ($40nm$) with gold electrodes on top, **(b)** pentacene ($80nm$) with gold electrodes, **(b)** pentacene ($40nm$) with gold electrodes, and **(d)** pentacene ($25nm$).

is increased from $0.6s$ to $0.75s - 0.8s$ to compensate for the larger resist thickness. Such differences of exposure time are undesired if C$_{60}$ and pentacene have to be structured on the same substrate as it is required for e.g. complementary circuits. Therefore, different resist treatment processes are tested. An effective reduction of exposure time is achieved in two different ways. First, the samples can be annealed after resist deposition. Heating at $70°C$ for $1min$ reduces the exposure time to $0.6s$. Unfortunately, such heating steps may not be applied to some organic materials. A second way to reduce the exposure time is to wait for at least $10min$ after resist deposition. The effect of annealing and waiting is similar. In either case, solvents can desorb of the resist which effectively reduces its thickness and therefore the exposure time.

The last step that has to be modified for structuring of pentacene is the etching process. In contrast to C$_{60}$ where a spin-rinsing process is employed, etching on pentacene requires a less aggressive procedure owing to the enhanced resist adhesion. Thus, instead of this spin-rinsing, the pentacene samples are dipped into HFE 7300 for $4min$ which is less aggressive than HFE 7100. After this dipping, the samples are again dipped in fresh HFE 7300 for $30s$ in order to avoid Langmuir-Blodgett film formation on the organic material.

With these modifications of the patterning recipe, pentacene can be structured with a high resolution and a high process yield as known for C$_{60}$.

6.2 OTFT Structuring by Photo-Lithography

In this subsection, the influence of photo-lithographic patterning on the OTFT performance is studied. The buckyball C_{60} molecule is chosen for these investigations since this material can be seen as a benchmark material for electron transporting organic semiconductors. Its high symmetry leads to highest mobility values reported for electron transporting organic semiconductors [74, 85, 140, 170, 191]. However, C_{60} has the same tendency as most other electron transporting organic materials: water and oxygen can be adsorbed easily and can act as trap states for charge carrier transport [192]. To discuss influences of the lithography on OTFT performance, changes in threshold voltage, contact resistance, mobility, and subthreshold-swing in comparison to a reference device structured by shadow mask are discussed.
Electron mobilities up to $5cm^2/(Vs)$ have been reported [85, 140, 191] for C_{60} using special surface treatments or low work function metals for source and drain electrodes. OTFTs in this study are not optimized for highest charge carrier mobility. Nevertheless, charge mobilities obtained in this work are within the state-of-the-art for C_{60} OTFTs and they can be further improved as suggested by Zhang [140, 191] and Virkar [85].

OTFT performance can be influenced by lithographic structuring in two ways. First, resist and solvent compounds will interact with the organic semiconductor. Second, there is an influence since the samples are exposed for several minutes to air and moisture before they are covered by the photo-resist. In order to distinguish between these two influences, the reference sample and the lithographically processed devices are exposed to air after the first characterization. Afterwards additional annealing steps are performed. In detail, after processing and the first measurement of fresh devices, the samples are exposed to air for one hour without protective resist and are heated afterwards for $1h$ in a nitrogen glovebox at $100°C$. It is well known that C_{60}, which has been exposed to air can be reactivated in an oxygen-free atmosphere [171, 192] (nitrogen glovebox or vacuum). Additional heating reduces the required reactivation time. As shown by Matsushima et al. [192], C_{60} contains two dominant trap levels. A deep one ($0.4eV$ below the conduction level) and a shallow one ($0.2eV$ below the conduction level), which is mainly caused by physisorption of oxygen and water. These shallow trap states can be healed by heating under vacuum conditions or inert atmosphere. Accordingly, the post-annealing step should help to remove the residuals of water and oxygen remaining in C_{60}. Thus, changes of OTFT parameters (threshold voltage, contact resistance, mobility) that can be reversed by the annealing procedure are likely caused by the accidental influence of water and oxygen and not by the lithography itself.

Comparison of threshold voltage and subthreshold-swing: In Figure 97, transfer characteristics and current-voltage curves (inset) of a lithographically structured OTFT are shown in comparison to a reference device. In general, both devices show typical OTFT performance, which means a clear off-state, a linear regime, and a saturation if V_{DS} exceeds $V_{GS} - V_{th}$. Nevertheless, there are
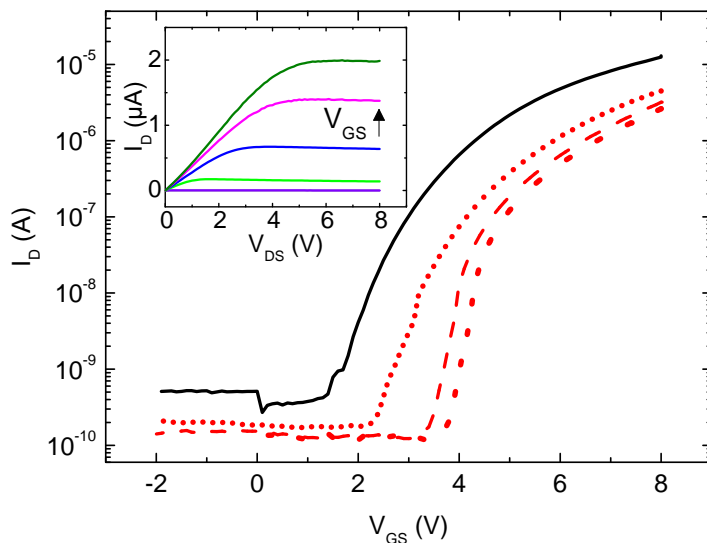
Figure 97: Transfer characteristics ($V_{DS} = 8V$) of lithographically (red) and shadow mask patterned (black) C_{60} OTFTs. The transistors have a channel length of $30\mu m$ and a channel width of $300\mu m$, respectively. The red short dotted curve denotes the performances directly after deposition. The red dotted curve shows the OTFT performance after one hour under ambient conditions (measurement in nitrogen) and the red dashed line after an annealing of one hour at $100°C$ in a nitrogen glovebox. The inset shows the current-voltage characteristics of the lithographically processed device. The gate-source voltages are: $2V$ (purple), $3V$ (light green), $4V$ (blue), $6V$ (magenta), $8V$ (dark green). The gate insulator is a $50nm$ layer of Al_2O_3 (ALD processed).

clear differences between reference OTFTs and lithographically structured OTFTs. Obviously, there is a shift in threshold voltage and a reduced on-state current.

In detail, the threshold voltage is shifted between the fresh reference sample ($V_{th} = 1.4V$) and the lithographically produced sample ($V_{th} = 2.3V$) by $0.9V$ (values are summarized in Table 8). The threshold voltage of the lithographically produced sample further increases to $V_{th} = 3.8V$ if the sample is exposed to air for one hour. If the sample is annealed, the threshold voltage decreases again to $V_{th} = 3.4V$. Thus, oxygen exposure increases threshold voltage. This effect can be partially compensated by heating. Focusing on the reference sample, a similar tendency of threshold voltage shift can be obtained. After air exposure, a threshold voltage of $3.3V$ is measured. This threshold is reduced to $2.3V$ after annealing. The threshold shift presumably arises because of water adsorbed at the dielectric interface [193]. These states, acting also as trap states, are not removable by the simple annealing procedure done here. They are caused by strongly bound hydroxyl groups at the insulator material. Utilizing highly hydrophobic gate dielectrics as e.g. polymers might help to reduce this effect. Differences in total values of threshold voltage likely arise from the fact that OTFTs produced by lithography have been exposed to air for a longer time and no annealing has

been

	V_{th} (V)	Contact Resistance			Mobility	SS-Swing
		$(k\Omega cm)$			$(cm^2/(Vs))$	(mV/dec)
		$V_{GS} = 4V$	$V_{GS} = 6V$	$V_{GS} = 8V$		
Reference						
fresh	1.4 ± 0.1	8.9 ± 0.8	6.8 ± 0.8	6.1 ± 0.5	0.17 ± 0.02	580 ± 20
$1h$ air	3.3 ± 0.1	22.3 ± 1.6	14.0 ± 1.2	11.4 ± 1.1	0.14 ± 0.02	600 ± 20
$1h$ at $100°C$	2.3 ± 0.1	14.4 ± 1.4	10.5 ± 1.2	8.3 ± 0.7	0.15 ± 0.02	610 ± 20
Lithography						
fresh	2.3 ± 0.1	43.7 ± 12.5	34.5 ± 8.5	30.1 ± 3.4	0.13 ± 0.02	510 ± 20
$1h$ air	3.8 ± 0.1	96.5 ± 11.7	46.8 ± 5.6	30.7 ± 3.6	0.10 ± 0.02	280 ± 40
$1h$ at $100°C$	3.4 ± 0.1	71.6 ± 6.1	38.2 ± 3.8	22.7 ± 4.1	0.11 ± 0.02	250 ± 40

Table 8: Threshold voltage, contact resistance, mobility, and subthreshold-swing (SS-swing) for reference C_{60} OTFTs and the lithographically processed transistors. The mobility and threshold voltage are determined for long channel devices (channel length $30\mu m$). Mobility is taken from the slope of the transfer curve at $V_{GS} = 5V$. The standard deviations are taken from variations of three OTFTs for each channel length and from fitting using the transmission line method, respectively.

employed after structuring.

Furthermore, a comparison of the transfer curves and on-state currents suggests that the transfer curve of the lithographically produced sample is merely parallel shifted for $V_{GS} > 5V$. Accordingly, mobility determined in this OTFT geometry is only slightly influenced (see Table 8). This fact indicates that the transport properties of C_{60} are only slightly affected and annealing is sufficient to remove oxygen and water related trap states in C_{60}. Apart from this, for $V_{GS} < 5V$ a steeper rise of the transfer curve is observed for lithographically produced samples. This increase in subthreshold-swing becomes more pronounced for larger threshold voltages (see Table 8). In contrast to that, the subthreshold-swing of the reference device (fresh, $1h$ air, annealing at $100°C$ for $1h$) is slightly affected ($580mV/dec$, $600mV/dec$, $610mV/dec$) in comparison to lithographically generated samples. However, assuming that the threshold shift is the only influence of lithographic structuring, changes in subthreshold-swing cannot be explained consistently. This is caused by the fact that an increased number of interface states would lead to an increased threshold voltage and an increased subthreshold-swing. The subthreshold-swing for the reference devices, however, is constant which implies according to Eq.88 that qN_{IT} is larger than C_i (this means $N_{IT} > 10^{12}cm^{-2}$). In case of lithographically prepared OTFTs, the subthreshold-swing is lowered by annealing which suggests, in contradiction to the reference devices, a reduced number of interface states. As it will be pointed out, this discrepancy can be explained
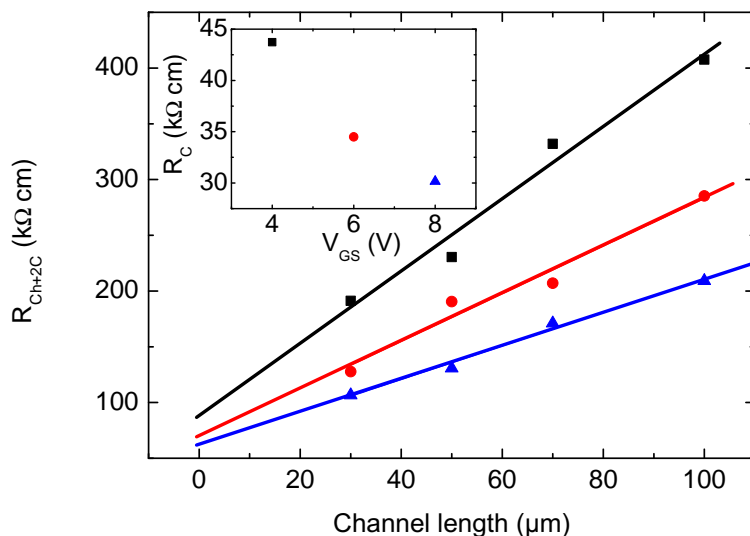
Figure 98: Transistor resistance R_{Ch+2C} (channel+contact) of lithographically produced OTFTs for different channel lengths ($V_{DS} = 2V$). The colors denote different gate-source voltages: $V_{GS} = 4V$ (black rectangles), $V_{GS} = 6V$ (red circles), and $V_{GS} = 8V$ (blue triangles). The contact resistance R_C (inset) is estimated from the intersection at zero channel length.

by the fact that lithographic structuring leads to an increase of contact resistance.

Comparison of contact resistance and mobility: The on-state current for lithographically made samples is smaller than for the reference sample. Besides mobility, an important parameter which may affect the on-state of the field-effect transistor is the contact resistance (R_C). R_C is determined using a transmission line model [83] for all tested types of devices. As shown in Figure 98, contact resistance is evaluated from a channel length variation between $30\mu m$ and $100\mu m$. The gate-source voltage dependence (inset) of contact resistance indicates a field dependent injection mechanism. Table 8 shows that lithographically prepared samples exhibit a stronger field dependence of contact resistance than the reference. Furthermore, a contact resistance four to five times larger than for the reference devices is obtained for the lithographically patterned OTFTs. The contact resistance determined for the reference device is in accordance to previously reported values [140]. Lithographically made OTFTs exhibit a contact resistance above these previously reported values.

For low gate-source voltages, significant differences in contact resistance of lithographically produced samples are obtained for different post-treatment steps. These differences presumably arise because of the threshold voltage shift for the various post-treatment steps (contact resistance depends on threshold voltage, compare Eq.92). However, for a gate-source voltage of $8V$, the contact resistance of lithographically produced OTFTs is almost independent of the post-treatment step. In consequence, since for all post-treatment steps similar values of contact resistance
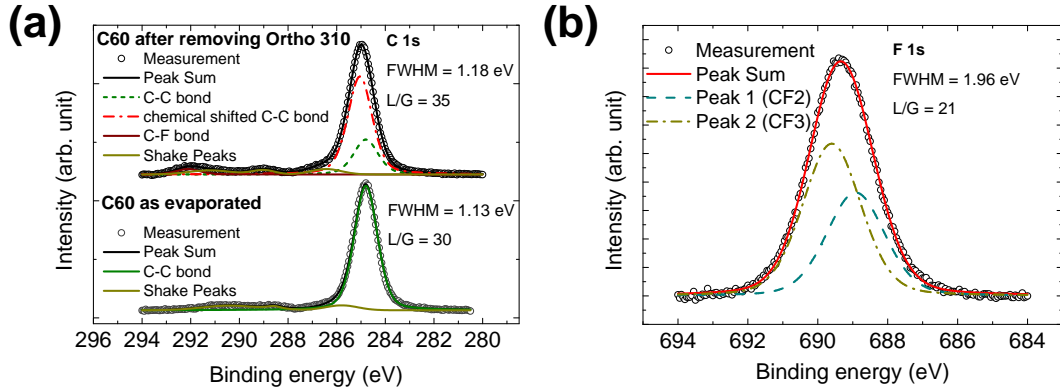
Figure 99: **(a)** XPS measurements of the C 1s signal of a C_{60} film after removing *Ortho* 310 in comparison to a C_{60} film as evaporated and **(b)** the F 1s signal of a C_{60} film after removing *Ortho* 310. The spectra are fitted with multiple peaks, assuming a full with at half maximum (FWHM) in the range of 1.0 to 2.0eV and a Lorentzian to Gaussian contribution (L/G) between 20 and 40. A Shirley background is subducted in all graphs.

are obtained for $V_{GS} = 8V$, it can be deduced that there is almost no effect of air and water related trap states in C_{60} on R_C. Accordingly, the increased R_C is a direct consequence of the lithographic patterning.

This effect presumably appears because of resist residuals between the semiconductor and the source/drain electrode. This assumption is confirmed by XPS investigations (see Figure 99 for spectra, technical details are described in [45, 172]). In particular, an XPS signal is obtained that can be attributed to fluorine, a main component of photo-resist and solvent used here. Consequently, there are partial solvent/resist residuals on the C_{60} film. For comparison, Figure 99 also contains the carbon related XPS signal for a pristine C_{60} film and a C_{60} film processed by lithography. In detail, the signal of the C 1s core level of the pristine C_{60} film can be fitted with one main peak at 284.8eV, which is generally attributed to pure carbon compounds [194]. Moreover, the spectrum contains also several shake peaks generally observed for C_{60} [195]. In comparison, the signal of the C_{60} film after removing *Ortho* 310 has slightly changed. One additional peak at 292.1eV is observed, which lies in the range of reported CF_2 and CF_3 bonds and hence it can be attributed to carbon which is directly bound to fluorine. The main peak is broadened indicating that two states are present: one again at 284.8eV and a second with a small chemical shift of 0.2eV. This shifted peak can be assigned to carbon atoms in the resist which are not directly bound with fluorine but affected by its strong electronegativity. Due to this fact and presence of fluorine signal, it can be concluded that there is still some resist left after removal. However, the presence of an unaffected C-C signal, attributed to the pristine C_{60}, indicates that the thickness of these residuals should be in the range of a few monolayers [196]. Nevertheless, XPS investigations clearly disclose the presence of resist residuals on the C_{60} film. Such residuals cause the increased contact resistance for lithographically made devices as summarized in Table 8. Beside its influence on contact resistance, the effect of resist residuals can be seen in the determined value of
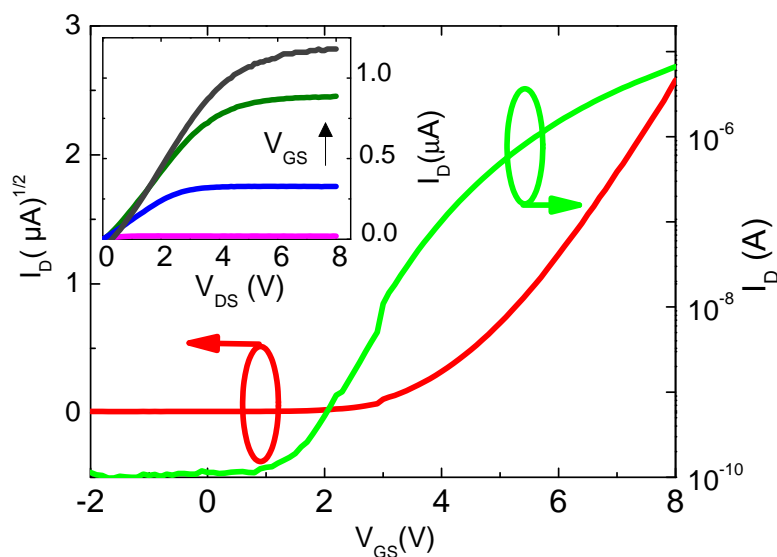
Figure 100: Transfer characteristics ($V_{DS} = 8V$) of a lithographically produced OTFT having a geometric channel length of $2.7\mu m$. The inset shows the current-voltage curve for different gate-source voltages. Colors denote the following gate-source voltages: $2V$(magenta), $4V$ (blue), $6V$ (dark green), and $8V$ (dark gray). The gate insulator is a $50nm$ layer of Al_2O_3 (ALD processed).

mobility which is slightly lower for lithographically made OTFTs than for the reference devices (see Table 8).

The problem of resist residuals is common for photo-lithography procedures. Such residuals are typically removed by a descum oxygen plasma etch process. Unfortunately, in the present case such processing cannot be directly applied to organic semiconductors, due to oxidation of C_{60}.

In summary, lithographically manufactured OTFTs show an increased threshold voltage caused by air and moisture exposure during processing. This threshold voltage shift arises because of water and oxygen related trap states at the dielectric interface. Furthermore, a sufficient healing of C_{60} by vacuum/glovebox annealing can be deduced. This can be seen in an almost unaffected mobility (parallel shifted transfer curve for $V_{GS} > 5V$). However, an increased contact resistance caused by resist residuals on C_{60} is obtained. A strong field dependence of contact resistance for lithographically prepared samples likely causes a steeper subthreshold-swing.

Short Channel devices: The ability of lithographic structuring of OTFTs in a top source-drain geometry opens the pathway for high density integration of such transistors. Thereby, a reduced channel length is required to achieve high on-state currents. However, contact resistance and transfer length effects [33, 70, 87, 94, 100] (length over which charge flow between contact and semiconductor mainly occurs, see inset Figure 101 or compare Subsection 2.3.1) strongly restrict the maximum on-state current that one can attain. Especially the transfer length L_0 governs the active channel length for short channel devices [33, 87]. For OTFTs
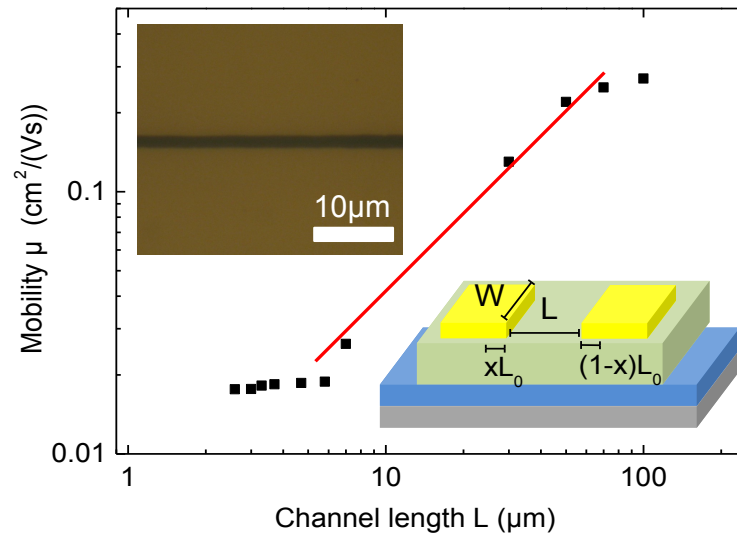
Figure 101: Mobility of electrons in lithographically produced OTFTs for different geometric channel lengths determined in the saturation regime. The width of the source and drain contacts is $500\mu m$ and thus it is significantly larger than the estimated transfer length. The upper inset displays a photograph of the $2.7\mu m$ channel. The lower inset shows a scheme of an OTFTs where measures as discussed in the main text are clarified.

in a top source-drain geometry containing a structured gate electrode, the transfer length is restricted by the geometrical overlap between source/drain and gate [33]. In case of an unstructured gate electrode, however, this transfer length can become significant and easily exceed the geometrical channel length. A main parameter influencing this transfer length is the contact resistance [70] (compare Eq.91).

The geometric channel length L of OTFTs used in this study is varied from $100\mu m$ down to $2.7\mu m$ to investigate effects of increased contact resistance and transfer length. Charge carrier mobility is determined for these devices since the dependency of mobility on channel length helps to disclose the transition from long channel to short channel devices. Figure 100 displays the transfer characteristics and the source-drain voltage sweep of a $2.7\mu m$ channel length OTFT. In accordance to the gradual channel approximation (compare Subsection 2.3.1), a linear regime for small drain-source voltages followed by a clear saturation regime is observed. Short channel devices and devices having a large contact resistance typically exhibit a non-linear behavior of drain current [97] at small drain-source voltages, which is related to the dominant contact resistance. For larger drain-source voltages, a linear behavior of drain current instead of a saturation has been reported [97]. This behavior is related to an increasing depletion at the drain electrode and therefore to a reduced active channel length. However, for the $2.7\mu m$ OTFTs discussed here, neither a strong contact limitation nor a linear regime for higher voltages is obtained.

This behavior is presumably caused by the fact that the transfer length in these

devices is larger than the geometric channel length. As Ante et al. [33] recently reported, the transfer length for OTFTs with structured gate electrode is in the range of $11\mu m$ and it is increased for larger contact resistance. Thus, owing to the enlarged contact resistance, the transfer length is significantly larger for lithographically made OTFTs. An extrapolation of transmission line analysis [197] (see Figure 97) suggests a transfer length in the range of 25 to $35\mu m$. Consequently, a strong drop of mobility is expected if the channel length is equal or less than the transfer length. Figure 101 shows the charge carrier mobility[56] measured for devices with a channel length L ranging from $2.7\mu m$ to $100\mu m$ (mobility determined by Eq.86). Three regimes can be identified: (I) mobility is almost independent of channel length (long channel device, $50 - 100\mu m$), (II) a drop of mobility by a factor of 20 (transition region, $7 - 50\mu m$), and (III) an almost channel length independent mobility for very short channels (transfer length dominated, $< 7\mu m$). This behavior of mobility is understandable if the transfer length is considered as an active part of the channel. Usually, the mobility μ as displayed in Figure 101 is determined by the slope of the transfer curve according to Eq.86. This assumes a geometrical channel length L as active channel region. However, this neglects the role of transfer length L_0 as an active part of the channel. Wang et al. [94] studied OTFT performance within the crowded current model [87] which describes transfer length effects. They have shown that the transfer length causes an additional resistance that has the same form as the channel resistance within the saturation regime of the OTFT. Thus, in this approach, the current through such an OTFT can be expressed by the formulas derived within the gradual channel approximation where merely the geometrical channel length L needs to be replaced by an effective channel length L_{eff}. Consequently, Eq.86 has to be corrected by

$$\mu_{long} = \frac{2}{WC_i} \cdot \left(\frac{\partial I_D^{1/2}}{\partial V_{GS}}\right)^2 \cdot L_{eff}, \tag{117}$$

where μ_{long} denotes the long channel device mobility for $L >> L_0$. Relying on these assumptions, a complete expression for charge carrier mobility vs. channel length has been derived by e.g. Benor et al.[198] as

$$\mu = \mu_{long}(1 - \frac{L_0^2}{(L + L_0)^2}). \tag{118}$$

For sake of simplification, this derivation implies that the transfer length can be treated as active part of the channel in the sense of the gradual channel approximation.

However, for a channel length $L > 50\mu m$, the active channel length is governed by its geometrical value and accordingly mobility is almost constant as predicted by Eq.118. For a channel length between $7\mu m$ and $50\mu m$, the contribution of transfer length as an active part of the channel is increased. In agreement to Eq.118, for such devices a reciprocal channel length dependence as indicated by a red line in Figure 101 is obtained. For a channel shorter than $7\mu m$, the channel length is pre-

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[56]The determined mobility should not be seen as a parameter characterizing transport within the channel. It is only a measure equivalent to the transconductance which quantifies the current flow.

dominantly given by the transfer length L_0 resulting in a reduced mobility of 1/20 of its original value as determined for long channel devices. Relying on the gradual channel approximation, it is expected that the mobility should continuously decrease for a reduced geometrical channel length. Since this is in contradiction to the experimental findings (mobility is almost constant for $L < 7\mu m$), it can be concluded that the transfer length cannot be treated as an active part of the channel as considered by the gradual channel approximation for $L_0 >> L$.

Nevertheless, Eq.118 can qualitatively describe the obtained behavior of mobility for short channel devices structured by the lithography technique proposed here. The transfer length can be graphically estimated from the transition between long channel mobility ($L > 50\mu m$) and the reciprocal channel length dependent mobility ($7\mu m < L < 50\mu m$). It is found to be in the range of $30-40\mu m$. Hence, strong deviation from the OTFT scaling laws as predicted by the gradual channel approximation are expected if the geometrical channel length gets close to the transfer length. However, for a more precise quantitative analysis, a more sophisticated model of transfer length as well as more experimental data points are required.

6.3 Towards Integrated Circuits

To complete this chapter on photo-lithographic patterning of organic semiconductors, two possible applications for organic TFTs are discusssed: inverter circuits and OTFTs as drivers in OLED displays.

In principle, lithographically patterned OTFTs are suitable for both applications. However, as it will be pointed out, there are strong limitations for the usage of OTFTs in such circuits. These limitations which are not specific to lithographically made devices arise from the low transconductance of organic thin-film transistors. This leads either to considerable power losses in case of display drivers or to low switching frequencies in case of organic inverters. The low transconductance can be seen as a direct consequence of the low charge carrier mobility in organic materials and the limited scalability of OTFTs as discussed in the previous subsection. These performance restrictions are not only relevant for lithographically structured OTFTs having an enlarged contact resistance; it can be shown that an equivalent performance to shadow mask patterned OTFTs can be reached if a special electrode preparation is employed.

OTFTs for OLED display drivers: To show the capability of lithographically produced OTFTs, a green OLED driven by a lithographically produced OTFT is demonstrated. The layer stack and the OLED performance is described elsewhere [199, 200].

A transistor comprising C_{60} with a channel length of $30\mu m$ and a channel width of $24mm$ is employed. The ratio between the active area of the OLED and the driving transistor is larger than 4 in this case (including OTFT contact pads). This ratio can be increased for smaller feature sizes since the photo-lithography technique enables to scale down the OTFT size. However, as discussed in the previous subsection, down-scaling will not necessarily lead to an increased transconductance for a channel length $< 30\mu m$.
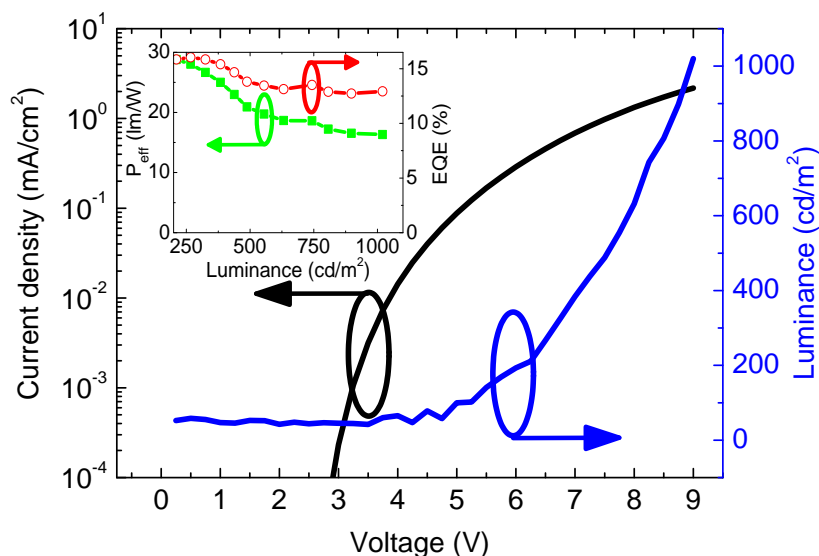
Figure 102: OLED driven by a C_{60} OTFT. The black curve shows the current through the OLED for different voltages applied across the OLED. The blue curve displays the luminance of the OLED driven by the OTFT for different gate-source voltages. The inset shows external quantum efficiency (EQE, red curve, open circles) and power efficiency (P_{eff}, green curve, closed rectangles) for different luminance values.

Figure 102 displays the luminance of the green OLED for different gate-source voltages at a fixed drain-source voltage of $12V$. The higher drain-source voltage, in contrast to Figure 95, is required to obtain the saturation regime of the OTFT with the OLED in series. Nevertheless, the highly efficient OLED used here guarantees a minimum of driving voltage: a luminance of $1000cd/m^2$ is achieved for voltages less than $4V$ (voltage drop across the OLED). As shown in Figure 102, an increase in luminance is obtained for increasing gate-source voltage and $1000cd/m^2$ are exceeded at $9V$. This clearly shows that even without aggressive scaling of driving OTFTs, sufficient luminance of OLED pixels can be achieved. Unfortunately, a comparison of the power efficiency P_{eff} of the OLED driven by the OTFT and the pure OLED ($60lm/W$, compare [200]), exhibits that $55 - 70\%$ (depending on the luminance) of the provided electrical power is consumed by the driver.

Due to the dominance of transfer length effects, photo-lithographic down-scaling of the channel length will not necessarily improve this loss ratio as described in the previous subsection. Down-scaling by shadow-masks can partially reduce power losses in display drivers since the contact resistance is smaller in comparison to lithographically produced devices. However, feature sizes accessible by shadow masks are limited and moreover alignment of shadow masks for large area displays exhibits a technological challenge. The third method for reducing the power losses is to scale the gate capacitor. Although this is a powerful technique as shown e.g. by Klauk et al. [201], aggressive scaling of the gate insulator by self-assembling processes combined with a shadow mask patterning is presumably not compatible
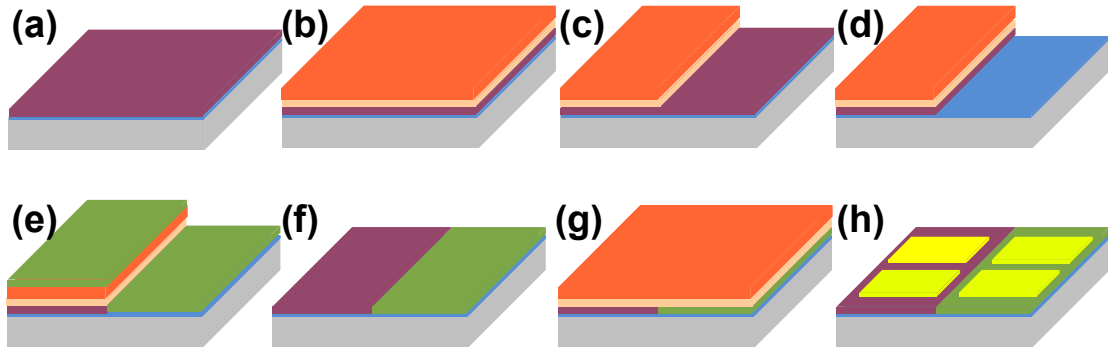
Figure 103: Recipe for photo-lithographic patterning of an organic inverter circuit. **(a)** Pentacene on substrate (n-Si and gate insulator), **(b+c)** coating, exposure, and development of $Ortho$ 310 and $ma - P1210$, **(d)** plasma etching of pentacene, **(e)** deposition of C_{60}, **(f)** lift-off in HFE 7300, **(g)** coating, exposure, and development of $Ortho$ 310 and $ma - P1210$, **(h)** gold deposition and lift-off in HFE 7300. The colors denote: silicon substrate (gray), gate insulator (blue), pentacene (violet), $Ortho$ 310 (light orange), $ma - P1210$ (orange), C_{60} (light green), gold (yellow).

to large area display production.

A prospective process for fabrication of OLED display drivers has to combine the scalability and reliability of photo-lithography and the high performance of aggressively scaled gate insulators. This combination is possible since the photo-lithography technique proposed here for patterning of organic semiconductors is compatible to the high-capacitance gate insulators as presented by e.g. Klauk et al. [201].

Complementary organic inverters: The combination of two transistors within one inverter circuit is a second important application for organic thin-film transistors. In this context, the patterning of source and drain electrodes on top of organic materials can be applied for fabrication of unipolar inverters. In particular, in order to design such inverters, photo-lithography can help matching the characteristics of the individual OTFTs which significantly improves the inverter gain. Moreover, as a consequence of the increased inverter gain for matching OTFTs, the integration density of transistors can be increased. These points exhibit a clear and strong advantage in comparison to shadow mask fabrication. However, this is not the only advantage of photo-lithographic patterning of inverters since photo-lithography can also be employed to design complementary inverters. Such complementary circuits are superior to unipolar and pseudo-complementary [202] circuits since they offer a higher gain of the inverters, a higher integration density, and less effort in terms of circuit design.

In Figure 103, a possible procedure for manufacturing a complementary inverter employing fluorine based photo-lithography is depicted. The method suggested here is a two-step procedure. In a first step (after substrate cleaning and HMDS treatment), a thin layer of pentacene serving as p-channel material is deposited. This layer is covered by photo-resist and structured by photo-lithography as explained in the previous subsections. After the development of photo-resist, the
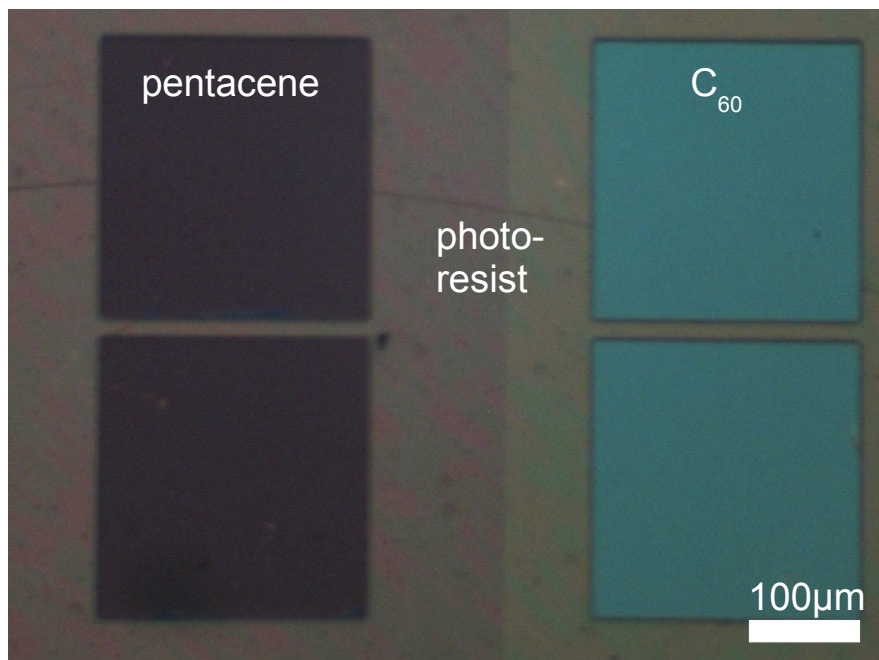
Figure 104: Microscope image of a photo-resist pattern of two OTFTs on pentacene and C_{60}. The channel length of both devices is $20\mu m$.
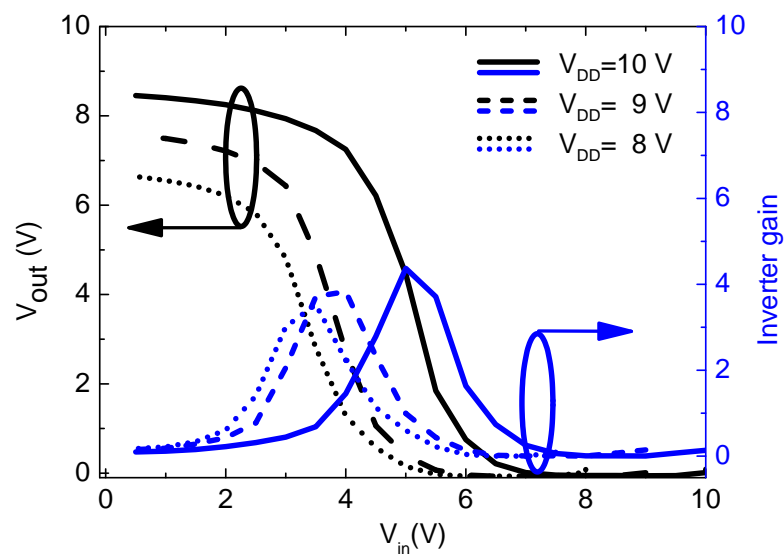
Figure 105: Input vs. output voltage of a complementary organic inverter fabricated by fluorine based photo-lithography. The channel length is $50\mu m$ for the p-channel transistor and $62\mu m$ for the n-channel OTFT respectively. The right axis shows the the gain of the inverter.

pentacene layer is removed from the uncovered areas by an oxygen plasma etch process (radio-frequency plasma). In a second deposition step, C_{60} is deposited as n-channel material. To remove spare C_{60} the sample is dipped in HFE 7300 in nitrogen atmosphere. In this way, pentacene and C_{60} can be structured on the same substrate with a high spatially resolution. The latter aspect is of particular importance for fabrication of high-frequency devices. To finalize the inverter structure, a second lithography step as described in the previous subsection is employed to pattern source and drain electrodes. A microscope image of the inverter circuit before deposition of the electrodes is shown in Figure 104.

Switching characteristics of a complementary organic inverter are shown in Figure 105. The n- and p-channel OTFT have the same channel width, however, the channel length is chosen with respect to the individual OTFT performance in order to guarantee a switching of the inverter at $V_{DD}/2$ according to Eq.101. In detail, the channel length of the pentacene p-channel transistor is $50\mu m$, while the C_{60} n-channel transistor has a channel length of $62\mu m$ for the inverter shown in Figure 105. As it can be seen, caused by this adjustment of channel length, the inverter switches at $V_{DD}/2$ showing an inverter gain above 4.

Although this inverter shows a reasonable on/off swing, apparently it does not reach V_{DD} for $V_{in} = 0$. This can be attributed to the fact that even if the inverter is balanced according to Eq.101, the pentacene transistor is not perfectly in the off-state for $V_{in} = 0$ (the threshold voltage is slightly negative). Thus, this yields a static current flow across the p-channel transistor for $V_{in} = 0$ and consequently, V_{out} does not reach V_{DD} for $V_{in} = 0$. A further consequence of the asymmetry of threshold voltage is the fact that both transistors are not working perfectly in the linear regime at $V_{in} = V_{DD}/2$ (the resistances of both OTFTs in the linear regime are not perfectly matching). This discrepancy leads also to a static current flow and consequently to a reduced inverter gain. In particular, the inverter gain is inversely proportional to the difference between the resistances of both transistors and minute variations of the inverter balance can cause significant differences in the inverter gain.

Interface doping: Photo-lithographically structured OTFTs as discussed here are clearly restricted in their performance by the increased contact resistance which is equivalent to an enlarged transfer-length. These restrictions, however, can partially be compensated by a special preparation of source and drain electrodes.

The influence of molecular interface doping on the injection of charge carriers is exemplarily discussed for lithographically patterned pentacene OTFTs. The same method can analogously be employed to n-channel OTFTs. However, this requires air-stable n-type dopants ($W_2(hpp)_4$ are not air-stable).

To improve the injection in pentacene OTFTs, a thin layer ($1nm$) of the strong acceptor compound F_6-TCNNQ is deposited on the pentacene. In order to avoid a doping effect on the channel area, the dopant is patterned by the resist mask used for deposition for source and drain electrode.

Figure 106 shows the I-V curves and the transfer characteristics of two lithographically structured OTFTs with and without interface doping. As shown there, the thin injection layer significantly improves the transistor performance. In particular, the off-state current and the threshold voltage are unaffected which means

(a)

(b)
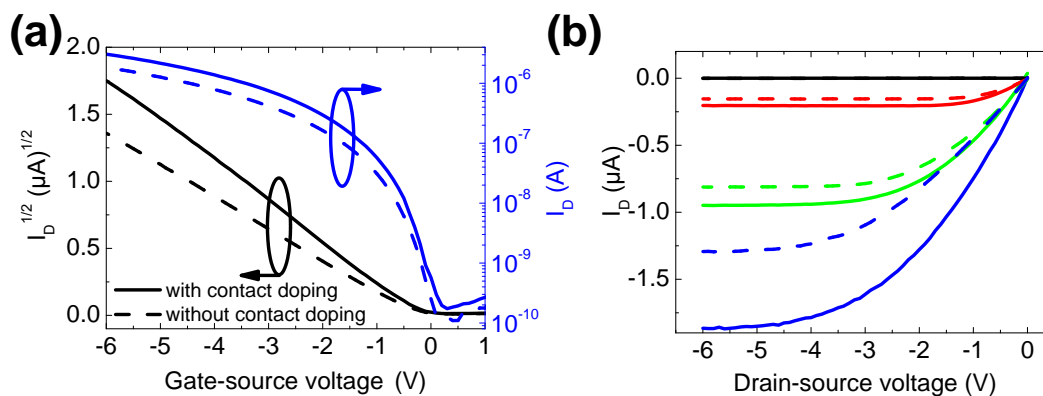
Figure 106: (a) Transfer characteristics ($V_{DS} = -6V$) and **(b)** I-V curves of two pentacene OTFTs structured by fluorine based photo-lithography (channel length $100\mu m$, channel width $1mm$, $50nm$ Al_2O_3 serves as the gate insulator). Closed lines show the performance of the transistor with interface doping and dashed lines without interface doping. The colors in **(b)** denote the gate-source voltages as follows: $0V$ (black), $4V$ (red), $5V$ (green), and $6V$ (blue).

that no free charge carriers are present in the channel. Hence, the dopant merely influences the interface at source and drain electrode. This effect of interface doping can be seen in the on-state current of the transistor. More specifically, the on-state current for $V_{GS} > V_{th}$ is strongly increased for doped devices whereas the subthreshold regime is only weakly affected. Within the subthreshold regime, the OTFT performance is not governed by injection of charge carriers, but dominated by the interface properties in the channel. In contrast, above the threshold-voltage, the OTFT behavior is restricted by the number of charge carriers injected from the source electrode. Hence, since interface doping can effectively reduce injection barriers for charge carriers, a larger on-state current is measured for doped devices. Furthermore, this experiment on interface doping shows in an unambiguous way that the performance of organic thin-film transistor is restricted by charge carrier injection even for long channel devices. For the devices shown in Figure 106 (long channel devices L=$100\mu m$), the current-voltage curves suggest an increased charge carrier mobility for doped devices ($0.1cm^2/(Vs)$ doped, $0.19cm^2/(Vs)$ doped, measured at $V_{GS} = V_{DS} = -6V$). Since the channel region is undoped, this has to be seen as an effect of the increased charge carrier density in devices with an injection layer.

To quantify the improvement of charge carrier injection, the contact resistance is measured using the transmission line method. Results of a lithographically patterned OTFT with and without interface doping and a reference OTFT structured by a shadow mask are shown in Figure 107. As can be seen, the contact resistance is effectively lowered if interface doping is employed. Moreover, doped OTFTs can even beat the reference device produced by shadow mask. The doping effect of such strong acceptor compounds deposited on pentacene has been investigated by Ha et al. [203]. They show that F_4-TCNQ can occupy vacancies on the pentacene surface which allows for an effective charge transfer.

In the present case, although there are resist residuals on the pentacene, the dopant
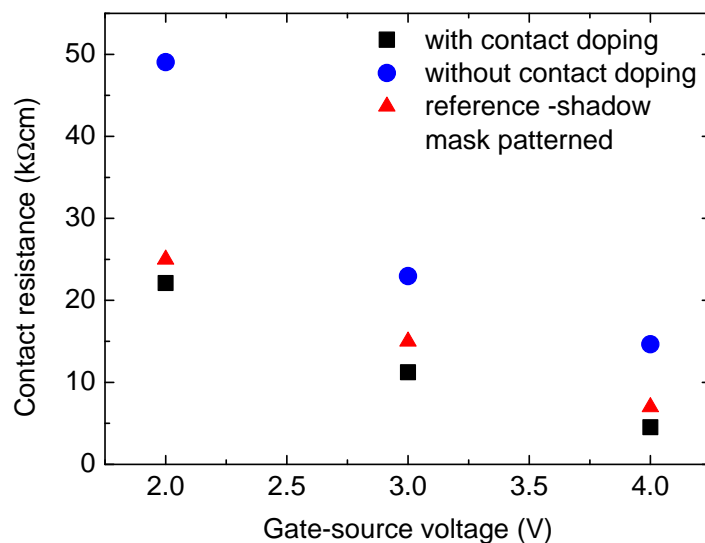
Figure 107: Contact resistance estimated by transmission line method for lithographically made OTFTs with (black rectangles) and without interface doping (blue circles). Furthermore, the contact resistance for shadow mask produced OTFT (same layer thickness, geometry, and substrate, without doping) is shown (red rectangles). The applied source-drain voltage is $-1V$.

can effectively provide charge carriers to the matrix. Since this is not possible for a closed layer of photo-resist covering the pentacene, it can be concluded that the thin photo-resist film covers the pentacene only partially and hence dopant molecules are in direct contact to the semiconductor material.

Summary

Within this chapter, it is shown that the high-mobility small molecule organic materials pentacene and C_{60} are compatible to photo-lithographic processing under ambient conditions. This is accomplished using a highly fluorinated photo-resist and solvents which are chemically benign to these materials.

A reliable lithography recipe is established for pentacene and C_{60}. This recipe also accounts for the different film properties of the organic materials, in particular for the layer roughness of pentacene films.

Organic thin-film transistors are fabricated using this lithography protocol and their performance is compared to reference devices patterned by shadow masks. In this way, influences arising from the lithography procedure and the accidental effects caused by air exposure can be distinguished. Latter ones affect the threshold voltage of the OTFTs, but not charge carrier transport in general. In this context, thermal annealing can effectively help to recover the transistor performance, and hence a similar charge carrier mobility is observed for lithographically made OTFTs and reference devices. Nevertheless, it is unambiguously shown that re-

sist residuals strongly increase the contact resistance in lithographically patterned OTFTs. In consequence, down-scaling of such OTFTs does not follow the prediction as formulated within the gradual channel approximation. Most notably, the transistor performance is predominantly governed by the transfer length if the channel length is less than $30\mu m$. This enlarged transfer length can be directly associated to the large contact resistance.

Although these mechanisms strongly restrict the transistor performance, lithographically made OTFTs are suitable for applications as e.g. driving transistors in OLED displays or as switches in inverter circuits. In particular, the good scalability of photo-lithography exhibits a considerable advantage in comparison to state-of-the-art structuring techniques as e.g. shadow mask patterning.

Interface doping as a possible method to reduce the contact resistance is demonstrated and the performances of lithographically patterned OTFTs are clearly improved. However, even these improvements will not allow to push the performances of such transistors further as it is required for e.g. radio-frequency identification (RFID) or high-definition OLED displays.

This might be achieved using novel high-mobility organic materials combined with an aggressively scaled transistor geometry, or by novel transistor concepts beyond state-of-the-art OTFTs.

Chapter VII

Vertical Organic Field-Effect Transistors

'Ce sont les terres qui savent reconnaître le blé.'

A. de Saint-Exupéry, writer, poet and pioneering aviator.

Transistors as described in Chapter 6.1 are not applicable at high- and ultra-high-frequencies. Hence, here a novel transistor geometry is proposed where the gate, source, and drain electrode are vertically arranged. Within this geometry, the distance between source and drain electrode is given by the layer thickness ($< 200nm$). The effective channel length is supposed to be within this range which is supported by a clear short channel behavior observed for these devices.

Nevertheless, it will be pointed out that such transistors exhibit an on/off ratio of up to 10^6 with excellent transfer characteristics. Furthermore, owing to their large on-state current, they can be seen as an interesting alternative to horizontal OTFTs.

7.1 VOTFT Concept and Fabrication

Generally, vertical transistors, i.e. junction field-effect transistors (JFETs), have been developed as the very first kind of transistors. Although they show an extremely high transconductance, in terms of scalability they are inferior to the planar, complementary MOSFET (CMOS) technology which has been proposed almost 40 years later. Nowadays, the usage of JFETs is mainly limited to high-power applications. However, within the last years the gate insulator thickness and the channel length in CMOS technology are approaching critical atomic dimensions which does not allow for further down-scaling. Hence, the planar design of MOSFET devices is currently revised and vertical transistor concepts are considered as prospective candidates [204].

In silicon technology it was not attractive to adopt vertical transistor concepts for a long time since structuring techniques were not suitable to reach a channel length $< 50nm$. However, owing to recent developments, the situation has changed and overlap capacitances and charge carrier injection phenomena play an important role in modern CMOS devices with a channel length $< 30nm$.

As discussed in the previous chapter, organic transistors show such injection phenomena (transfer length effects) already for channel lengths of $\sim 10\mu m$. Since these dimensions are easily accessible by modern patterning techniques, down-scaling is not an adequate way to increase the performance of organic transistors. Similar to silicon based CMOS technology, vertical concepts have to be considered.

In general, the physical parameter that determines the critical dimensions for transfer length effects is charge carrier mobility [6]. It mainly governs the electrical resistance between the source/drain electrode and the conductive channel. This resistance is inversely proportional to the charge carrier mobility. Comparing typical values of charge carrier mobility (Si: $\sim 1400cm^2/(Vs)$, pentacene $\sim 1 - 3cm^2/(Vs)$), it becomes obvious that a channel length of $5 - 10\mu m$ represents an optimum concerning performance for OTFTs without restriction by transfer length effects[57].

Several approaches for vertical organic transistors are summarized in Subsection 2.3.3. They make use of either self-assembled or shadow mask patterned source electrodes, while the drain electrode is structured through a shadow mask in either case. In principle all these device concepts have two technological relevant bottlenecks:

- reproducibility, controllability, and scalability of the self-assembling process,

- and compatibility of the shadow mask patterning to large area fabrication.

Photo-lithography on organic materials as suggested in Chapter 6.1 can be seen as an interesting and technologically applicable alternative to the VOTFT concepts presented in the literature. Here, the VOTFT concept of Nakamura [138] is adopted as a starting point to build a high-performance vertical organic thin-film transistor. This concept is chosen since it is based on a *top-down* fabrication method (shadow mask patterning). Hence, photo-lithography can be used to de-

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[57]assuming that no charge injection barrier at the electrodes is present and assuming that the gate-source/drain overlap and the gate insulator capacitance are adequately chosen with respect to the channel length.
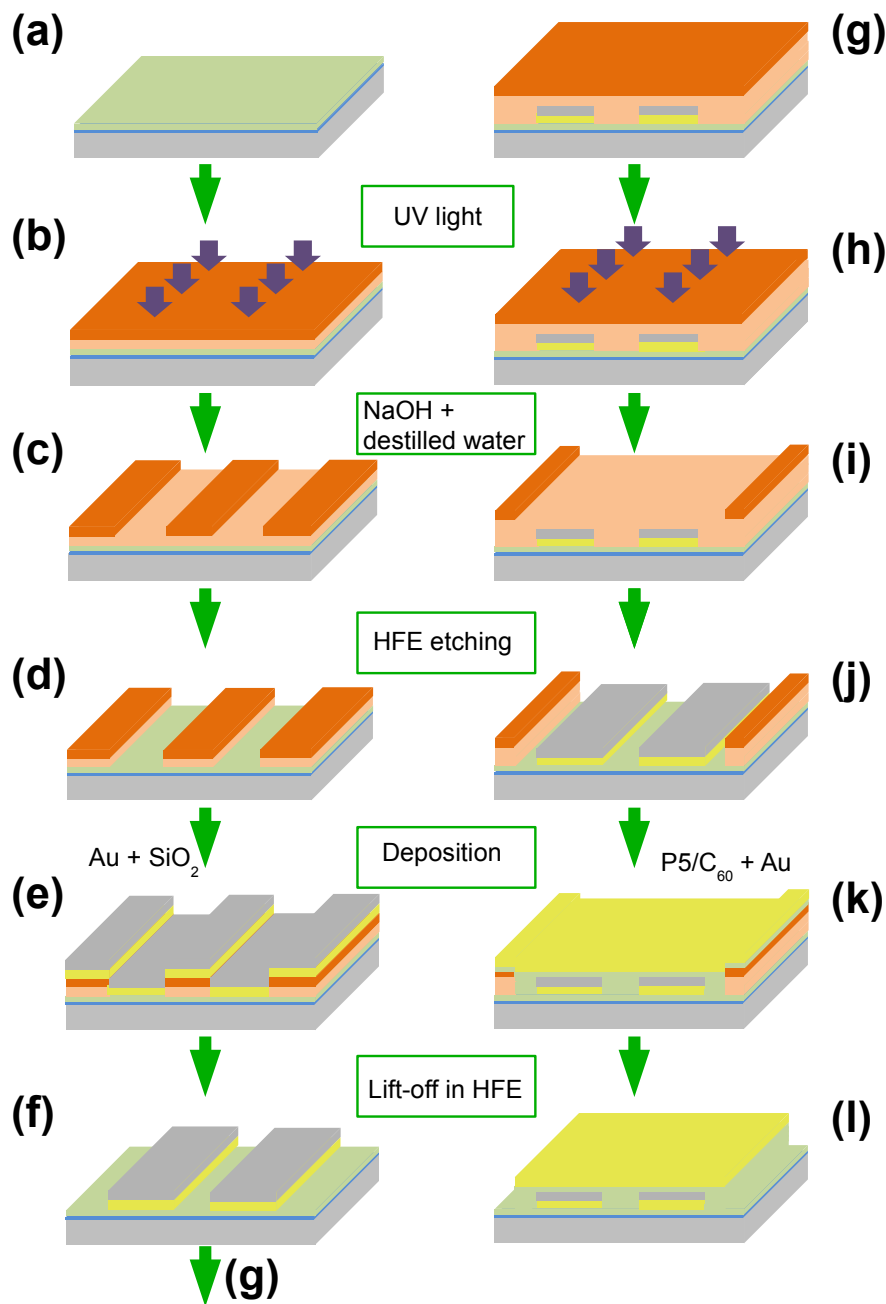
Figure 108: Fabrication protocol for a VOTFT. The individual steps **(a)-(f)** and **(g)-(l)** follow exactly the description as shown in Section 6.1. For VOTFT fabrication an additional layer of SiO_2 is deposited on the source electrode in step **(e)**. The colors denote: silicon gate electrode (gray), Al_2O_3 gate insulator (blue), organic semiconductor (light green), SiO_2 insulator (gray), and source and drain electrodes (yellow).

sign and improve the device geometry. Moreover, photo-lithography allows for a precise alignment of the vertically arranged electrodes which makes such transistors compatible to large area fabrication.
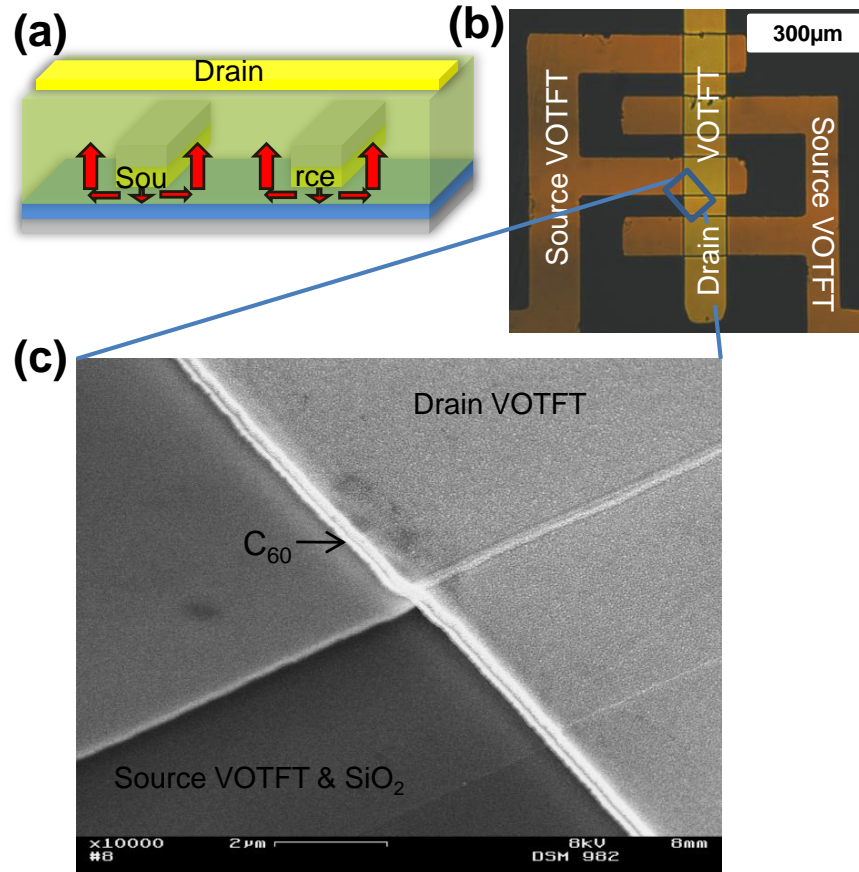
Figure 109: **(a)** Scheme, **(b)** microscopic image, and **(c)** a scanning electron microscope picture of a VOTFT fabricated as explained within the text. The colors in **(a)** denote: silicon gate electrode (gray), Al_2O_3 gate insulator (blue), organic semiconductor (light green), SiO_2 insulator (gray), and source and drain electrodes (yellow). The red arrows in **(a)** indicate a possible path for charge carrier transport. In **(b)** and **(c)** the electrode configuration is indicated. The SEM picture shows a $150nm$ SiO_2 layer covered by $50nm$ C_{60} and $30nm$ Au. The scale bar suggests wrong thicknesses since the picture is recorded under a tilted view.

In Figure 108, the fabrication protocol for a vertical organic thin-film transistor structured by fluorine based photo-lithography is displayed. The protocol contains two lithography steps. In the first one, the source electrode is patterned as described in Section 6.1 (two gold stripes in Figure 108). Additionally, an insulating layer of SiO_2 (thickness $100nm$) is sputtered onto the source electrode[58]. After lift-off, a second photo-lithography step using the same recipe is employed to form the drain electrode. During this second step, the alignment of source and drain electrode is of particular importance since it defines the active region of the device. By photo-lithography, this alignment can be controlled with an accuracy of $< 5\mu m$ which guarantees a good controllability of important geometry parameters such as channel width. To complete the layer sequence, a second layer of the organic semi-

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[58] SiO_2 deposition by planar radio-frequency (RF) magnetron sputtering, argon pressure during deposition $2 \times 10^3 mbar$, RF power $100W$, typical deposition rates are $0.1 - 0.2nm/s$

conductor and the drain electrode are deposited. Finally, spare photo-resist and metal is removed by lift-off in HFE solvents in a nitrogen glovebox. In comparison to the structuring of a planar OTFT, the exposure time of the organic materials to air is increased to approximately $2-3h$, and in general, the fabrication of these devices takes typically $2-3$ days.

VOTFTs comprising C_{60} or pentacene are realized by this method and hence, the possibility to produce n- and p-channel devices is ensured.

A schematic and a microscopic image of these VOTFTs are shown in Figure 109. The working principle of VOTFTs is discussed in Subsection 2.3.3. Applying a gate-source voltage, charge carriers are accumulated at the gate insulator interface. The larger the gate capacitance, the more charges are collected there. If a drain-source voltage is applied, the electric field pulls the free charge carriers away from the insulator interface and they move in the direction of the drain electrode. Similar to the OTFT principle, the transistor-like operation of VOTFTs is based on the control of the free charge carrier density by the gate capacitor. However, the picture of a conductive channel appearing close to the insulator interface is not appropriate to VOTFTs since the gate-source field and the drain-source field are not perpendicular to each other. Even if the lateral distance between the source and the drain electrode can serve as a first approximation for the channel length, the effective length and in particular the shape of the conductive channel are presumably governed by both, a certain area required for injection of charge carriers and the lateral electrode distance. However, this will not be studied in detail here, since a sophisticated model taking overlap capacitances and the field distribution into account would be required.

Furthermore, one considerable difference between OTFTs and this VOTFT concept has to be highlighted. The gate-source field in OTFTs is significantly larger than the drain-source field. Contrary, for VOTFTs as proposed here both electric fields are expected to be almost equal which can lead to short channel effects.

7.2 Vertical Organic Thin-Film Transistors

In the following, vertical organic thin-film transistors manufactured as described in the previous section are presented. N-channel and p-channel operation is obtained using either C_{60} or pentacene as semiconductor material. The performance of both transistor types is compared.

7.2.1 N-Channel Vertical Organic Thin-Film Transistors

Vertical organic thin-film transistors operating as n-channel transistors are realized employing C_{60} as semiconductor. In terms of processibility, one benefits from the robustness and the good substrate adhesion of C_{60}.

The current-voltage curves and the transfer characteristics of a VOTFT comprising C_{60} are shown in Figures 110 and 111. As it can be seen, the VOTFT shows a typical transistor-like behavior. For sake of comparison current-voltage curves of a VOTFT and an OTFT as illustrated in Figure 109 are shown in Figure 110.
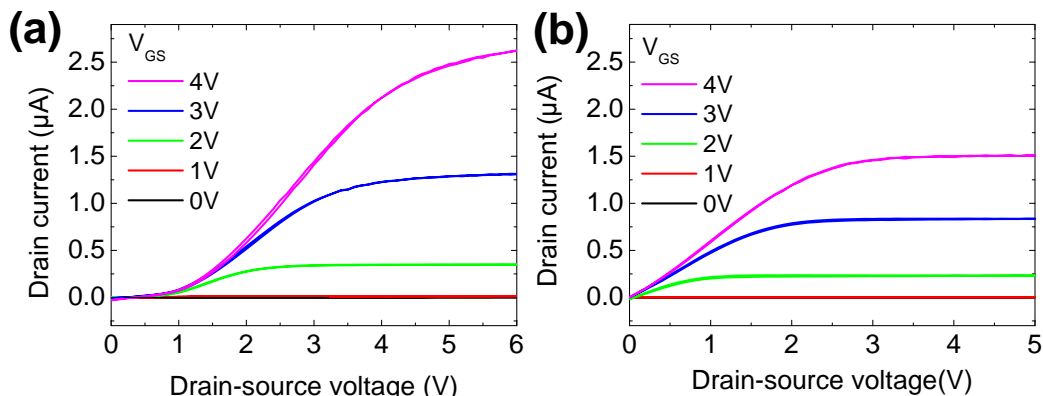
Figure 110: Current-voltage curves of **(a)** a VOTFT and **(b)** an OTFT compris-
ing C_{60} as semiconductor material. The device geometry is shown in
Figure 109 (channel length and width of the OTFT are $50\mu m$ and
$900\mu m$, respectively). The total thickness of C_{60} is $500nm$ in case of
(a) and $40nm$ in case of **(b)**. The gate insulator is a $23nm$ thick layer
of Al_2O_3 deposited by ALD.

A direct quantitative comparison of both device geometries is not feasible since
the effective channel length of the VOTFT is unknown. Accordingly, the specific
transconductance is not discussed quantitatively and merely characteristic features
of both transistors are used to argue on their operation fashion.

The OTFT performance shown in Figure 110(b) can be described in accordance
to the standard OTFT theory (Eq.84 and Eq.85, compare Section 2.3). The I-V
curve fulfills a linear current-voltage relation for small drain-source voltages, and it
displays a distinct saturation for $V_{DS} > V_{GS} - V_T$ (compare also Figure 111). Also
charge carrier mobility, as evaluated from the transfer characteristics, lies within
the expectations ($\sim 0.1cm^2/(Vs)$). This means that even after a second lithogra-
phy step and after SiO_2 sputtering C_{60} is healed by the final vacuum processing
step.

The vertical thin-film transistor (see Figure 110(a)) behaves differently from the
horizontal OTFT. It possesses neither a linear regime, nor a clear saturation of
drain current for larger V_{DS}. Nevertheless, according to the transfer characteris-
tics, the VOTFT operates as a transistor which specifically means that a clear on-
and off-state can be obtained by varying the gate-source voltage. For the specific
VOTFT shown in Figures 110 and 111, the on/off ratio reaches almost 10^5 and the
off-state current is similar to the off-state level of the horizontal OTFT. In partic-
ular, this means that the SiO_2[59] layer between the source and the drain electrode
can sufficiently block the leakage current between source and drain.

To interpret the differences in I-V characteristics for VOTFTs and OTFTs as de-
picted in Figure 110, various arguments can be employed. The non-linear behavior
($I_D \sim V_{DS}^2$) for $V_{DS} < V_{GS} - V_T$ suggests a strong injection limitation. In com-
parison to the corresponding OTFT, contact resistances can provide a significant
contribution to the overall device resistance. In particular, owing to the short
channel appearing in vertical devices, the channel transconductance is expected

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[59]A "soft" breakdown of the SiO_2 between source and drain is observed at $V_{DS} \sim 7 - 8V$ (thickness
$100nm$).
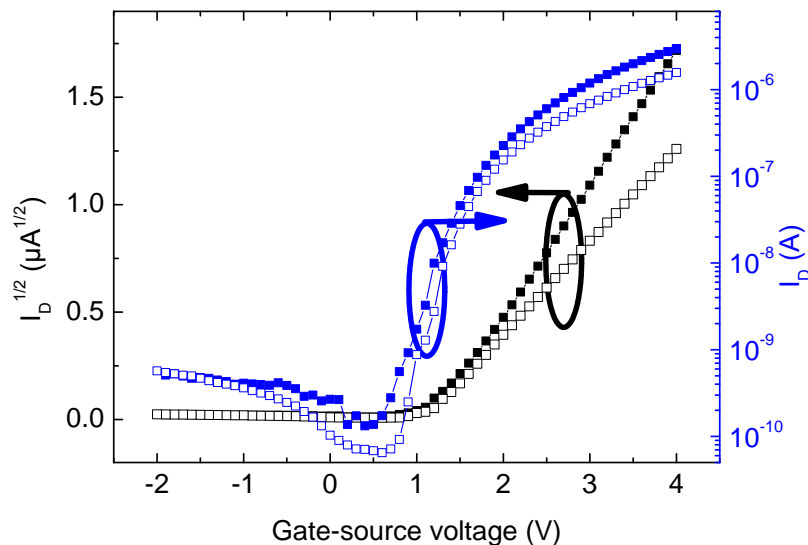
Figure 111: Transfer characteristics of the devices shown in Figure 110. Closed symbol represent the VOTFT and open symbols the OTFT. The applied drain-source voltage is $5V$.

to be higher than for horizontal OTFTs. Hence, the contact resistance dominates the device performance if the channel resistance is lower than the contact resistance. In the high voltage regime ($V_{DS} > V_{GS} - V_T$) the VOTFT fulfills a linear current-voltage relation. A similar effect, known as channel length modulation, is also observed for short channel TFTs (compare Section 2.3). It is explained by the fact that for short channel devices the channel length and the charge depletion zone appearing at the drain electrode in case of saturation ($V_{DS} > V_{GS} - V_T$) are of comparable size. Hence, if the drain-source voltage is increased, the channel length is effectively lowered and thus the drain current rises linearly. For VOTFTs possessing an extremely short channel length and devices dominated by charge carrier injection, also two other mechanisms can provide an explanation for the loss of saturation. The first mechanism is directly related to the injection limitation. Within this context, the linear I-V behavior for $V_{DS} > V_{GS} - V_T$ can be explained by a transition from a strong to a weak contact limitation. If V_{DS} is increased, more and more charge carriers are injected from the source electrode and the current through the channel is approaching its saturation current value. The second explanation for the disappearance of the saturation regime accounts for current contributions arising from the bulk of the semiconductor. Caused by the short drain-source distance and hence caused by the large electric field, charge carrier transport is not only restricted to the channel area which is controllable by the gate-source field. Additionally, direct transport paths in the bulk of the semiconductor can emerge providing a significant contribution to the drain current. These currents typically follow a power-law dependency on the voltage. Unfortunately, a more quantitative statement is not possible, since the explicit behavior strongly depends on the injection process, the electric field, and the transport properties of the semiconductor.
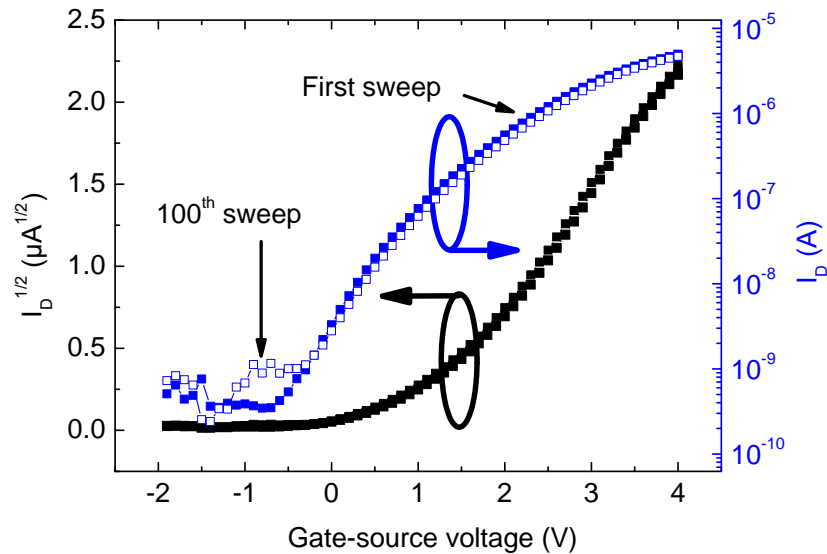
Figure 112: Transfer characteristics of a vertical organic thin-film transistor comprising C_{60} before (closed symbols) and after gate bias stress (open symbols). The gate-source voltage is continuously ramped up and down from $-2V$ to $4V$ without refresh time. A source-drain voltage of $5V$ is continuously applied to the sample. The total layer thickness of C_{60} is $50nm$ and the gate insulator is a $23nm$ thick layer of Al_2O_3 deposited by ALD.

All three mechanisms suggested here can explain the disappearance of current saturation for $V_{DS} > V_{GS} - V_T$. An experimental evaluation of the dominant effect is challenging since the channel length modulation, the injection limitation, as well as the bulk current contribution depend on the channel length and hence they cannot be distinguished easily. However, no matter which effect governs the transistor behavior, the I-V characteristics obtained for C_{60} VOTFTs provide clear evidence for an extremely short channel length since all three effects described above are pure short channel device features.

A more detailed, quantitative model of VOTFTs is beyond the scope of the present work. Such a model has to account for the 3-dimensional field distribution within the VOTFT stack and also it has to include a sophisticated model for charge carrier injection. Fortunately, the VOTFT concept proposed here is suitable for a first modeling approach since in comparison to other VOTFT concepts (compare Subsection 2.3.3), all geometrical parameters of the VOTFT (overlap capacitances) are known and can be controlled experimentally.

In order to provide a deeper insight into the principle of VOTFT operation, first scaling and stability tests are performed. While scaling experiments are indispensable for a quantitative model, stability tests can help to identify crucial device parameters which are of technological relevance.

As a first test to probe the stability of C_{60} VOTFTs, the transfer characteristics are measured continuously. In this way, the stability of off-state current, on-state current, and threshold voltage can be tested. Figure 112 displays the transfer

characteristics of a VOTFT before and after gate bias stress. The characteristic after the 100th gate-source voltage sweep is shown for comparison. Effects related to the gate-source voltage stress can be summarized as follows:

- threshold voltage: no significant effect on threshold voltage upon voltage stress

- on-state current: only a small drop of on-state current (presumably caused by degradation of C$_{60}$, stress time $> 5h$)

- off-state current: instable current measurement within the off-state, current spikes appear randomly for $V_{GS} < V_T$, the off-state current level increases continuously during the gate-source voltage stress and typically after $500 - 700$ gate-source voltage sweeps the on/off ratio is reduced to less than 100.

This means that the insulating layer of SiO_2 between source and drain is currently limiting the stability of VOTFTs. Owing to the fabrication conditions (no clean room), a considerable concentration of defects inside the insulator has to be expected leading to a lower quality of the SiO_2. In contrast, the threshold voltage and the on-state current are stable in these experiments. Hence, it can be deduced from these stability tests that the parasitic overlap between source and drain has to be minimized in order to reduce the influence of defects in the insulator. Furthermore, a reduction of parasitic overlap capacitances would certainly lead to an improved dynamic response of VOTFT devices.

In further experiments, the scaling behavior of VOTFTs is investigated. Two parameters can be modified for this study: the length of the source electrode edges (channel width) and the thickness of the semiconductor film (channel length). The latter influence is probed using two different layer thicknesses of C$_{60}$ ($50nm$ and $500nm$). Although this exhibits a considerable large thickness variation, basically no influence on the device performance is obtained. In detail, the threshold voltage, the general shape of the I-V curves, and the on-state current remains unchanged[60]. Even if this result surprises on a first glance, it is in accordance to the previous finding that C$_{60}$ VOTFTs are strongly limited by injection. In particular, for $50nm$ layer thickness of C$_{60}$ as well as for $500nm$, the channel resistance is still clearly smaller than the injection resistance. Therefore, since the device performance is in either case limited by the injection resistance, a variation of channel length does not modify the transconductance. This is in accordance to the previous findings (compare Section 6.1) where a performance restriction related to contact resistance is obtained in C$_{60}$ OTFTs for a channel length $< 30\mu m$.

The second scaling parameter for VOTFTs is the edge length of the source electrode overlapping with the drain electrode. This length is supposed to be equivalent to the channel width. In Figure 113, the influence of a variation of the edge length on the on-state current is shown. Both quantities fulfill a linear relation justifying that this edge length can be seen as the channel width of the VOTFT. In order to exclude influences of the special electrode configuration Figure 113 also contains data for different channel lengths for the OTFT beneath the VOTFT (50, 70, and $100\mu m$). In this way, it is proven that the channel length of the horizontal

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[60]Typically the on-state current differs by $\sim 5-10\%$ for equivalent devices on a substrate. The difference for various C$_{60}$ thicknesses is within this range.
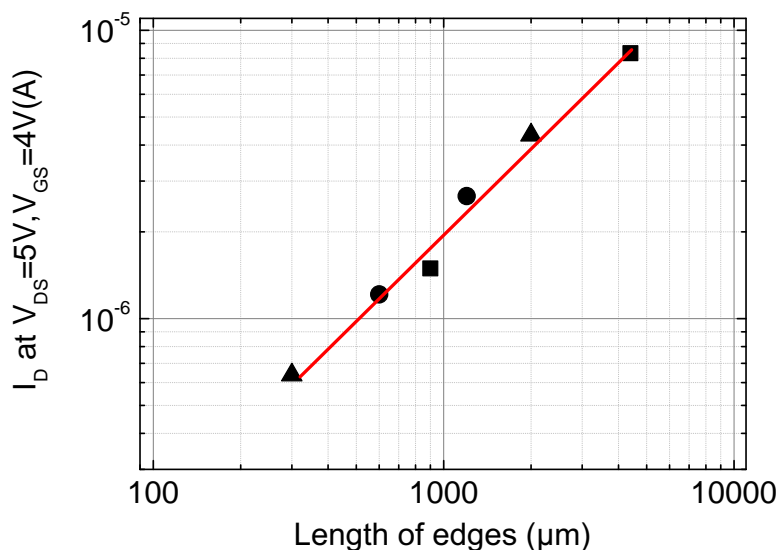
Figure 113: Scaling experiments for C_{60} VOTFTs. The drain current at $V_{GS} = 4V$ and $V_{DS} = 5V$ is determined for different VOTFT that differ in their edge length of source and drain overlap. The symbols denote the channel lengths of the OTFT beneath the VOTFT as follows: $50\mu m$ (rectangles), $70\mu m$ circles, $100\mu m$ (triangles).

transistor has no influence on the VOTFT scaling behavior.

It should be emphasized that even though it is demonstrated in Section 6.1 that C_{60} OTFTs can be manufactured under ambient conditions, n-channel OTFTs containing C_{60} cannot operate in air and hence the utilization of C_{60} as a standard material for n-channel VOTFTs is not attractive.

7.2.2 P-Channel Vertical Organic Thin-Film Transistors

In order to accomplish p-channel operation of a VOTFT, C_{60} is replaced by pentacene in the VOTFT stack. Even if lithographic processing of pentacene is challenging, it has considerable advantages in comparison to C_{60}. The most prominent advantages are that pentacene devices can operate in air and that the contact resistance appearing at the Au-pentacene interface is significantly smaller than the Au-C_{60} contact resistance (compare Sections 6.1 and 6.3). While the first aspect is beneficial for the lithographic patterning, the latter point should lead to an improvement of VOTFT performance in comparison to n-channel VOTFTs using C_{60}.

For discussion of pentacene VOTFT performance the same electrode geometry as for C_{60} transistors is used. Hence, a direct comparison of the transconductance is possible. The I-V characteristics of the pentacene VOTFT and the corresponding OTFT are shown in Figure 114. Moreover, Figure 115 displays the transfer characteristics of the transistor shown in Figure 114(a).

The behavior of the reference OTFT is as expected (Figure 114(b)). It shows
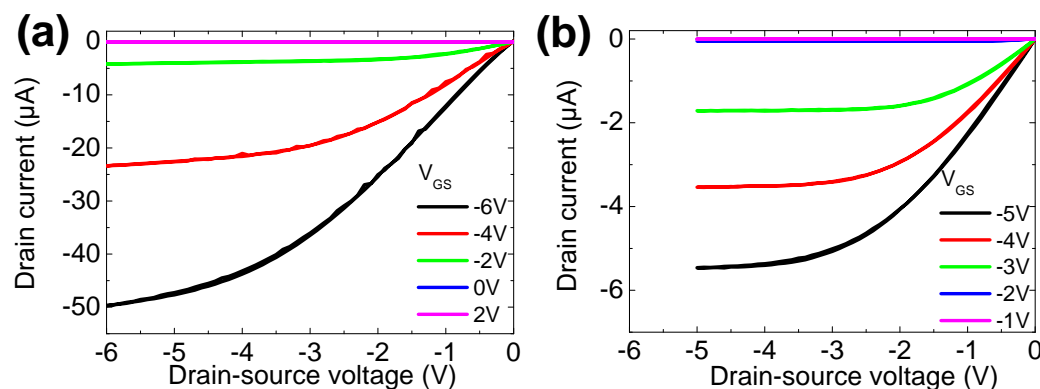
Figure 114: Current-voltage curves of (**a**) a VOTFT and (**b**) an OTFT comprising pentacene as semiconductor material. The device geometry is shown in Figure 109 (channel length and width of the OTFT are $50 \mu m$ and $900 \mu m$, respectively). The total thickness of pentacene is $50 nm$ in case of (**a**) and $25 nm$ in case of (**b**). The gate insulator is a $23 nm$ thick layer of Al_2O_3 deposited by ALD.

a clear linear regime and a distinct saturation of drain current. Furthermore, an estimation of charge carrier mobility provides reasonable values of $0.25 - 0.30 cm^2/(Vs)$.

Focusing on the VOTFT (see Figure 114(a)), several important differences can be identified in comparison to the OTFT operation and the C_{60} VOTFT discussed in the previous section. In particular, the pentacene VOTFT shows a linear regime for $V_{DS} < V_{GS} - V_T$ with only a small kink close to $V_{DS} = 0V$. This suggests that in contrast to C_{60} devices, the injection is more efficient. As a consequence of the lower contact resistance, also the overall transconductance is strongly increased. Hence, comparing the on-state current for the pentacene OTFT and VOTFT shown in Figure 114, an improved transconductance by a factor of 10 can be obtained[61]. This enhanced transconductance leads also to an improved on/off ratio which reaches almost 10^6 (compare Figure 115).

Similar to C_{60} devices, no saturation of drain current is observed for vertical organic transistors comprising pentacene. Although the same mechanisms as described for C_{60} VOTFTs can be used to explain this behavior, the strong differences of charge carrier injection behavior for both materials allow for a better interpretation. Owing to the reduced contact resistance for pentacene VOTFTs, which leads to an almost linear current-voltage behavior for $V_{DS} < V_{GS} - V_T$, a strong influence of the contact resistance on the transconductance in the saturation regime is implausible. The strong contact limitation might explain the loss of saturation for C_{60} VOTFT, however, in case of pentacene this effect should have vanished which stands in contradiction to the experimental findings.

The second possible explanation for the disappearance of the saturation region is the contribution of charge carrier transport via the bulk of the semiconductor which is not controllable by the gate-source voltage. Again, the contact resistance argument can be employed to show that bulk transport only plays a minor role in VOTFTs. In particular, if the contact resistance is reduced, also the transport via

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[61]This still neglects that the active area of the VOTFT is smaller than for the OTFT.
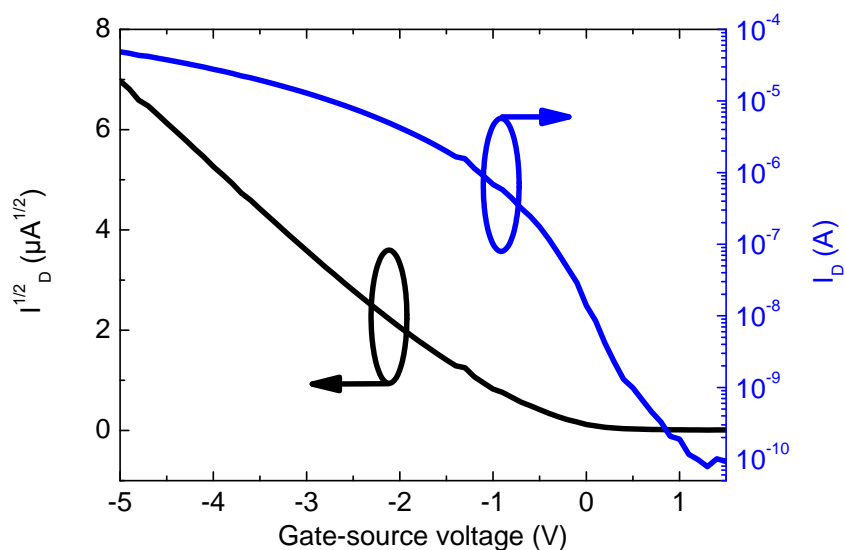
Figure 115: Transfer characteristics of the VOTFT shown in Figure 114. The applied drain-source voltage is $-5V$.

the bulk material should be more efficient. Beside an increased on-state current, this bulk current should primarily increase the off-state current. However, this is not observed in the experiments and finally it can be deduced that the channel length modulation is presumably the dominant effect leading to the disappearance of the saturation currents.

Finally, it is worth to discuss two other characteristic features of vertical organic thin-film transistors which are related partially to the short channel length and partially to the asymmetric device geometry. As shown in Figure 116, a small drain-source voltage dependence of the threshold voltage can be obtained for pentacene VOTFTs. This threshold voltage roll-off, which is discussed in Subsection 2.3.1, is attributed to an injection of charge carriers from the source electrode assisted by the drain-source field. Hence, if the drain-source voltage is increased, also a larger gate-source voltage of the opposite direction has to be applied in order to repel charge carriers out of the channel. For the device shown in Figure 116, the threshold voltage changes by $0.3 - 0.4V$ if V_{DS} is varied from $-1V$ to $-5V$. Hence, the drain-source field and the gate-source field cannot be considered independently as done for long channel devices.

The second characteristic feature of vertical organic thin-film transistors is caused by their stack asymmetry. This asymmetry is twofold since firstly, the source and drain electrode have different distances to the channel area, and secondly, the gate-source overlap capacitance and the gate-drain overlap capacitance are not equal. Both features are of technological relevance since they will lead to an asymmetric charge carrier injection and hence also to an asymmetric device operation depending on whether the upper or the lower electrode is used as source or drain, respectively. Figure 117 exemplarily displays the transfer characteristic of the pentacene VOTFT shown in Figure 115 where the role of the source and the drain electrode is flipped. Apparently, if the upper electrode is used as the
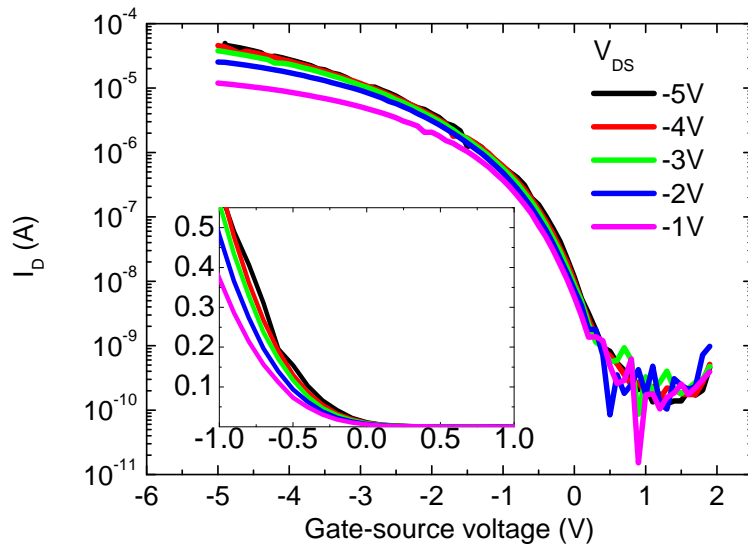
Figure 116: Transfer characteristics of the VOTFT shown in Figure 114 for different drain-source voltages varying from $-1V$ to $-5V$. The inset shows the threshold voltage region in a linear current scale. In the inset the current scale is given in μA.
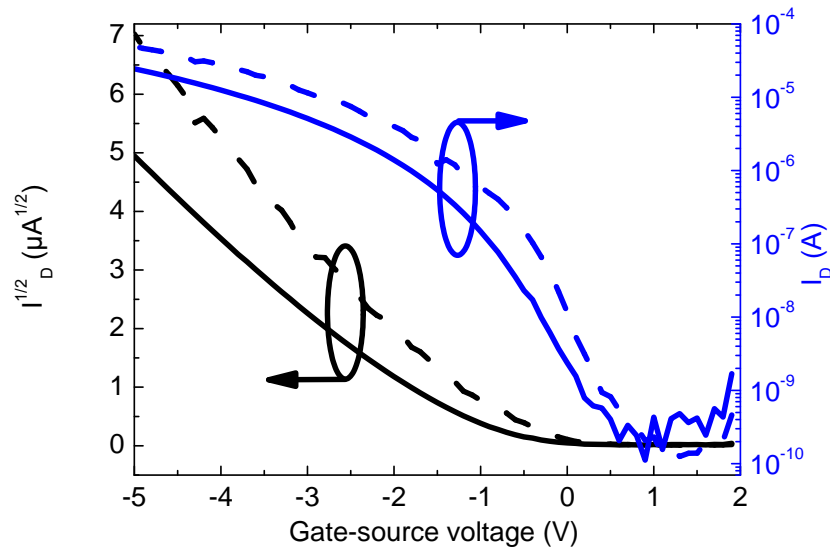
Figure 117: Transfer characteristics of the VOTFT shown in Figure 114 for a drain-source voltage of $-5V$. The role of the source and drain electrode is flipped. Upper electrode - drain, lower electrode - source (dashed line), upper electrode - source, lower electrode - drain (closed line).

source electrode, the transconductance is almost halved in comparison to its previous value (lower electrode as source). This difference is presumably caused by the fact that $50nm$ of pentacene are present between the gate insulator and the upper electrode while only $25nm$ of pentacene are in between the lower electrode and the insulator interface. Therefore, caused by the different contact resistances for both electrodes, the field distribution as well as the charge carrier density depend on the choice of source and drain electrode. This asymmetry is undesirable for integration of transistors in e.g. inverter circuits. Hence, VOTFTs have to be designed with regard to a symmetric operation. This can presumably be accomplished using interface doping at the upper electrode.

Summary

In this chapter, high performance vertical organic field effect transistors with a vertical channel length down to $50nm$ are presented. These devices are manufactured by a direct photo-lithography method, which is compatible to organic semiconductor materials. By this technique, source and drain electrodes are vertically stacked with the organic semiconductor material in between. If a source-gate voltage is applied, a conductive channel is created in the semiconductor film and its resistance is controllable by the applied gate field. This vertical conductive channel of the VOTFT, however, is a complex and 3-dimensional structure and thus OTFT theory relying on the gradual channel approximation is not adoptable to such devices. Nevertheless, VOTFTs presented in this study exhibit very high on/off ratios of 10^6 as well as high transconductance values. In particular, for VOTFTs containing pentacene, on-state current densities of almost $100mA/cm^2$ are attained.

As a consequence of the extremely short vertical channel, which is likely governed by the film thickness, short channel device characteristics as e.g. threshold voltage dependence on the source-drain field, and disappearance of the saturation region are obtained. The photo-lithography technique used for fabrication of these vertical transistors is based on fluorinated photo-resist compounds and thus it can be adopted for structuring of different organic materials under ambient conditions. Owing to this universality of the process, p-type VOTFTs comprising pentacene as well as n-type VOTFTTs comprising C_{60} are presented. Although generally both n- and p-channel devices show a transistor-like behavior with clear on and off-state levels, the maximum transconductance for n-channel devices is less. This effect presumably results from a larger contact resistance between Au and C_{60} in comparison to Au and pentacene. This underlines the importance of contact resistances in VOTFTs, whose performance is dominated by the injection process of charge carriers.

Nevertheless, in either case higher transconductances of VOTFTs compared to the underlying OTFTs are obtained and thus, the combination of high performance complementary VOTFTs on the one hand and the advantages of the photo-lithographic patterning technique on the other hand, represents a promising way for high density integration in low-power electronic devices made of organic semiconductor materials.

Chapter VIII

Conclusion & Outlook

> 'I am a firm believer, that without
> speculation there is no good & original
> observation.'

_____

C. Darwin, scientist.

Controlling and adjusting the performance of organic electronic de-
vices and demonstrating a reliable high resolution integration technique
are the two main concerns of this work. In this chapter, the achieve-
ments presented in this thesis are briefly reviewed and suggestions for
future work are provided in order to further improve the capability of
organic electronic devices.

8.1 Conclusion

The main focus of this work is devoted to organic pin-diodes and the question
how one can design and optimize such devices with regard to UHF applications.
Starting with a substantial investigation on the static reverse voltage properties,
important quantities characterizing the diode are identified which leads to a deeper
insight into the underlying phenomena. In particular, the formation of charge de-
pletion zones, a main functional part of the diode, is studied using impedance spec-
troscopy. Analyzing the voltage and frequency dependent impedance response, it
is found that the formation of charge depletion zones can be described in perfect
quantitative agreement to the Mott-Schottky theory. This especially means that
the field inside the intrinsic layer of the pin-diode is constant, while it drops lin-
early within the depletion zones. Moreover, the width of the charge depletion zones
appearing in molecular doped pin-diodes can be quantified employing the Mott-
Schottky analysis and it is found that such depletion zones are typically thinner
than $10nm$ for moderate dopant concentrations ($\sim 0.5 - 1mol\%$). These findings

suggest a high dopant efficiency which is determined to be $> 60\%$ showing a very low thermal activation energy.

A second interesting outcome of these investigations on the reverse voltage behavior is the observation of a reversible reverse breakdown. It is demonstrated that this breakdown is related to a tunneling process since it obeys an exponential voltage and layer thickness dependence and furthermore the current within the breakdown regime is almost not affected by the temperature. Owing to this exponential voltage and layer thickness dependence, the reverse breakdown voltage can be tuned independently by either the dopant concentration or the interlayer thickness. In a first approach, the reverse breakdown is modeled by a tunneling process between HOMO and LUMO states of neighboring and next neighboring molecules. Using experimentally determined values for the built-in potential and the interlayer thickness, a semi-quantitative agreement between measured and modeled I-V curves can be found.

In a second step, this knowledge of the field distribution and the depletion capacitance is employed to design and optimize organic pin-diodes for ultra-high-frequencies. However, for UHF operation, the intrinsic layer of the diode is only one active part of the device. Thus, it is also necessary to consider the influence of the electrodes, as well as of the doped charge transport layers. In this context, the role of the dopant concentration within the hole transport layer is found to be of particular importance. This is due to the fact that a structural phase transition induced by doping is revealed for molecular doped pentacene films. As a consequence of this poly-crystalline to amorphous phase transition, a strong drop of charge carrier mobility is obtained. However, the conductivity curve shows a distinct maximum for low dopant concentrations ($2mol\%$ for F_6-TCNNQ, $6mol\%$ for F_4-TCNQ). Hence, this represents a certain optimum where the density of charge carrier is effectively increased upon doping, while the mobility drop is still not leading to a loss of conductivity.

Employing these optimized dopant concentrations, the diode stack is designed for UHF conditions. In particular, it is shown that for an interlayer thickness of $90-120nm$ of pentacene, a trade-off between lowest forward resistance, highest reverse resistance, highest rectification ratio, and lowest forward current onset voltage can be achieved. These devices are characterized at ultra-high-frequencies and it is demonstrated that the design rules concerning dopant concentration and interlayer thickness give rise to an improved output performance at $20MHz$ where a DC voltage output of almost $1.4V$ is obtained for a technological relevant small AC input signal of $2V$ amplitude. Moreover, it is highlighted that such pin-diodes can serve as rectifiers up to a frequency of $1GHz$. This cut-off frequency is also confirmed by a complete small signal impedance model of the diode which allows to extract important modeling parameters such as charge carrier mobility, diffusion length, and minority charge carrier life time.

In the second part of this thesis, organic thin-film transistors, a high resolution integration technique, and a novel vertical transistor concept are discussed. In particular, a novel photo-lithographic patterning technique using highly fluorinated photo-resist and solvent compounds is established in order to manufacture highly integrated organic thin-film transistors under ambient conditions. A special feature

of this photo-lithographic technique is that it is compatible to many organic semi-conductor materials. Influences of the patterning protocol on OTFT performance are discussed. Analyzing transistor parameters such as threshold voltage, charge carrier mobility, and contact resistance, the inherent influence of the patterning technique and the effect caused by oxygen exposure can be distinguished. Most notably, the patterning procedure has no direct influence on the charge carrier mobility suggesting no substantial effect on the organic molecule itself. However, an increased contact resistance related to interfacial resist residuals is obtained. This enlarged contact resistance leads to the fact that the performance of photo-lithographically patterned OTFTs is limited by the injection of charge carriers for a channel length $< 30 \mu m$. Hence, down-scaling is not an appropriate way to improve the transconductance of OTFTs. To compensate this contact resistance limitation, it is highlighted that molecular dopants can effectively lower the injection resistance reaching the performance of shadow mask produced devices without an interfacial resist layer. Nevertheless, although interface doping can strongly reduce the contact resistance, the performance of OTFTs is limited in either case by injection of charge carriers for a channel length $< 5 \mu m$.

In order to overcome these contact resistance restrictions for planar OTFTs, a novel vertical thin-film transistor concept is proposed. This vertical transistor is realized for n- and p-channel devices employing the fluorine based photo-lithography either on C_{60} or on pentacene. The channel length in these unique VOTFTs is in the range of the vertical layer thickness ($\sim 50 nm$) which leads to a fairly large drain-source field in comparison to the gate-source field. As a consequence of this high electric field typical short channel effects, such as the loss of saturation and a threshold voltage roll-off are observed. However, even if these VOTFT are also strongly limited by charge carrier injection, they can surpass the performance of reference OTFTs. This is presumably related to the fact that the large drain-source field in comparison to the planar devices leads firstly to a lowering of the injection barrier and secondly to a higher charge carrier mobility. Secondly, owing to the vertical arrangement of source and drain electrodes, the integration density of vertical devices can be even higher than for planar devices.

8.2 Outlook

The results of this work concerning characterization and understanding of organic pin-diodes and the investigations done on integration of planar and vertical organic thin-film transistors surely represent a step towards future reliable, transparent, and flexible organic electronics. However, it is just a starting point and a lot of work has still to be done.

Future work can be devoted to very different fields such as the physical principles of device operation, material characterization, integration of devices, and circuit design. All these topics have to be addressed in order to warrant the success of organic electronics.

However, from a physicists point of view, presumably the most interesting topics are the characterization of transport in both organic diodes and vertical thin-film transistors. In particular, the findings on the reverse breakdown and on the dopant

efficiency in organic pin-diodes lead to the question if a degeneration of organic semiconductors is possible. This is a fascinating point since it directly allows to study the differences between electronic systems showing either band-like or hopping transport. Furthermore, if a degenerate organic semiconductor can be achieved by doping, this would lead to a new organic device - the tunneling or Esaki diode.

Another interesting topic for future work is the characterization of trapping and recombination in high mobility organic materials. Such investigations are essential in order to describe the transport in organic pin-diodes and to predict the cut-off frequencies. Moreover, the analysis of these time constants for recombination and trapping effects will open the way to study the effect of electric field and charge carrier density on the dominant recombination mechanism.

Such studies on organic diodes have a rather substantial character since e.g. the UHF performance of a diode represents in most cases an upper limit for transistor operation. This is due to the fact that there are no parasitic capacitances in a diode. However, for electronic applications, the transistor is an indispensable device. Hence, it is essential to further investigate the principals of OTFT and VOTFT operation. In particular, caused by its superior performance, it is worth to study the novel VOTFT concept in detail. Since such devices cannot be described within the standard OTFT theory, either a first equivalent circuit or a sophisticated mathematical model accounting for the field distribution and the charge carrier transport has to be formulated. Such a model can serve as a starting point to firstly receive a deeper physical understanding and secondly optimize such devices for highest performance.

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List of Symbols

Symbol	Description	Unit
a	Lattice constant	m
A	Active device area	m^2
$A*$	Richardson constant	AK^2/cm^2
$a_j{}^\dagger$	Creation operator of state $|j\rangle$	$-$
a_j	Annihilation operator of state $|j\rangle$	$-$
$b_{\mathbf{q}j}{}^\dagger$	Creation operator a phonon in branch j with wave vector $\mathbf{q}$	$-$
$b_{\mathbf{q}j}$	Annihilation operator of a phonon in branch j with wave vector $\mathbf{q}$	$-$
c_1	Expansion coefficient	$-$
c_2	Expansion coefficient	$-$
C_i	Specific insulator capacitance (OTFT)	F/m^2
C_{Ch}	Channel capacitance (OTFT)	F
C_D	Depletion capacitance (pin-diode)	F
C_T	Trap state capacitance (pin-diode)	F
d	Isolator thickness (OTFT)	m
d_i	Thickness of interface layer (Schottky contact)	m
D	Charge carrier diffusion constant	cm^2/s
D_e	Diffusion constant for electrons	cm^2/s
D_i	Density of interface charges	$cm^{-2}eV^{-1}$
E	Energy	eV
E^0	Ground state energy of Mott-Wannier exciton	eV
E_+	Energy eigenvalue of Ψ_+	eV
E_-	Energy eigenvalue of Ψ_-	eV
E_F	Quasi-Fermi level	eV
EA	Electron affinity	eV
E_A	Activation energy of electrical conductivity	eV
E_{act}	Activation energy for trap release	eV
E_B	CT-complex binding energy	eV
E_C	Energy of conductance states	eV
E_G	Energy gap between valence and conductance states	eV
E_{Ph}	Phonon energy	eV
E_C	Energy of valence states	eV

$f(E)$	Fermi function	—
f_i	Occupation probability of state i	—
F	Electrostatic force	N
$\hat{H}$	Hamilton operator	—
$\hat{H}$	Hamilton operator	—
$\hat{H}^{elec}$	Electronic Hamilton operator	—
$\hat{H}_{el}$	Electronic Hamilton operator (tight-binding approximation)	—
$\hat{H}_{ph}$	Phononic Hamilton operator (tight-binding approximation)	—
$\hat{H}_{e-ph}^{l}$	Hamilton operator for local electron-phonon coupling (tight-binding approximation)	—
$\hat{H}_{e-ph}^{nl}$	Hamilton operator for non-local electron-phonon coupling (tight-binding approximation)	—
$\hat{H}^{vib}$	Vibronic Hamilton operator	—
H_{AA}	Coloumb integral	eV
H_{AS}	Resonance integral	eV
I	Current	A
I_D	Drain current	A
IP	Ionization potential	eV
j	Total current density in a diode	A/cm^2
j_0	Dark current density in a diode	A/cm^2
j_{DD}	Current density related to drift and diffusion (Schottky contact)	A/cm^2
$j_{S\rightarrow M}$	Current density of thermionic-emission (Schottky contact)	A/cm^2
j_{tunnel}	Current density of tunneling current (Schottky contact)	A/cm^2
k	charge carrier recombination rate	s^{-1}
L	Channel length OTFT	m
L_0	Transfer length OTFT	m
L_C	Overlap length (OTFT)	m
L_D	Debye length	m
L_{diff}	Minority charge carrier diffusion length	m
m_r	Reduced mass of electron-hole pair	kg
$m*$	Effective mass of a quasi-free charge carrier	kg
n	Density of electrons	cm^{-3}
n_{free}	Density of free electrons	cm^{-3}
n_{trap}	Density of trapped electrons	cm^{-3}

N	Number of unit cells	cm^{-3}
N_A	Density of ionized acceptor states	cm^{-3}
N_A^0	Density of acceptor states	cm^{-3}
N_D	Density of ionized donor states	cm^{-3}
N_t	Density of sites	cm^{-3}
$N(E)$	Density of states	$eV^{-1}cm^{-3}$
N_{RO}	Number of inverters (ring oscillator)	$-$
N_V	Density of hole transport states	$eV^{-1}cm^{-3}$
p	Density of holes	cm^{-3}
P	Probability for CT-complex dissociation	$-$
PE	Potential energy within the metal-semiconductor interface	eV
$\mathbf{q}$	wave vector	cm^{-1}
Q_D	Number of ionized donor states in the depletion zone	$-$
Q_i	Number of interface charge carriers	$-$
$\vec{r}$	Coordinate of electron motion	m
r^0	Interaction radius of Mott-Wannier exciton	m
r_C^A	Specific contact resistance (OTFT)	Ωm^2
$|R_i j|$	Spatial distance between site i and j	m
$\vec{R}_1$	Coordinate of nucleus motion	m
$\vec{R}_2$	Coordinate of nucleus motion	m
R_C	Contact resistance	Ω
R_{Ch}	Channel resistance (OTFT)	Ω
r_C	Specific contact resistance (OTFT)	Ωm
r_{Ch}	Specific channel resistance (OTFT)	Ω/m
R_S	Series resistance (diode)	Ω
R_P	Parallel resistance (diode)	Ω
R_T	Trap resistance (diode)	Ω
S	Overlap integral	$-$
T	Temperature	K
T_0	Characteristic temperature for tailing of DOS	K
T_D	Oscillation period (ring oscillator)	s
V	External bias voltage (diode)	V
V_{DC}	Static voltage output of a rectifier diode	V
V_{DD}	Supply voltage (inverter)	V
V_{DS}	Drain-source voltage	V
V_F	Transition voltage	V
V_{FB}	Flatband voltage	V
V_{GS}	Gate-source voltage	V
V_{in}	Input voltage (inverter)	V
V_M	Switching voltage (inverter)	V

V_{out}	Output voltage (inverter)	V
V_T	Threshold voltage	V
v_x	Velocity of charge carriers in direction of transport	m/s
W	Channel width OTFT	m
W_{ij}	Hopping transition rate from state i to j	s^{-1}
w_D	Charge carrier depletion width (Schottky contact)	m
w_D^e	Charge carrier depletion width n-doped layer	m
w_D^h	Charge carrier depletion width p-doped layer	m
w_I	Interlayer thickness pin-diode	m
$\tilde{Z}$	Complex impedance function	Ω
$\tilde{Z}'$	Real part of impedance	Ω
$\tilde{Z}''$	Imaginary part of impedance	Ω
α	Inverse location radius of molecular wave functions	m^{-1}
γ_{jk}	Transfer integral of $|j\rangle$ and $|k\rangle$	$-$
ϵ	Relative semiconductor permittivity	$-$
ϵ_i	Relative permittivity of the interface layer (Schottky contact)	$-$
ϵ_j	Eigenstate energy of state $|j\rangle$	eV
ζ	Function for generalized Einstein equation	V
η	ideality factor, Schottky diode	$-$
η_D	ideality factor, pin-diode	$-$
Φ_{bi}	Built-in potential of a diode	V
$q\Phi$	Metal work function	eV
$q\Phi_0$	Energy of interface charges above E_V	eV
$q\Phi_0$	Distance between quasi-Fermi level and E_C	eV
$q\Phi_{Be}^0$	Barrier height for electron injection (Schottky contact)	eV
$q\Phi_{Bh}^0$	Barrier height for hole injection (Schottky contact)	eV
$q\Delta\Phi_i$	Interface charge induced barrier lowering (Schottky contact)	eV
$q\Delta\Phi_{if}$	Image-force induced barrier lowering (Schottky contact)	eV
θ	Bragg angle	$^\circ$
θ_{NI}	Empirical function in the non-ideal Shockley equation (Eq.70)	eV^{-1}
κ	Slope of the electronic ladder	eV

λ_i	Decay rate for excited site i	s^{-1}
λ	Channel length modulation (OTFT)	V
μ	Charge carrier mobility	$cm^2/(Vs)$
μ_e	Electron mobility	$cm^2/(Vs)$
μ_h	Hole mobility	$cm^2/(Vs)$
μ_{lin}	Charge carrier mobility (linear regime OTFT)	$cm^2/(Vs)$
μ_{sat}	Charge carrier mobility (saturation regime OTFT)	$cm^2/(Vs)$
μ_{free}	Charge carrier mobility (transport without trap states)	$cm^2/(Vs)$
μ_{trap}	Charge carrier mobility (transport via trap states)	$cm^2/(Vs)$
ν_0	Phonon vibration frequency	s^{-1}
ν_0	Phonon vibration frequency	s^{-1}
ν_{ATE}	Phonon scattering induced attempt-to-escape frequency	s^{-1}
ρ	Charge carrier density	$cm^{-3}eV^{-1}$
σ	Specific conductivity	$(\Omega cm)^{-1}$
σ_{free}	Specific conductivity related to free charge carriers	$(\Omega cm)^{-1}$
σ_{trap}	Specific conductivity related to trapped charge carriers	$(\Omega cm)^{-1}$
σ_{ij}	Specific microscopic conductivity	$(\Omega cm)^{-1}$
$\hat{\sigma}$	Standard deviation of the Gaussian DOS	eV^{-1}
τ	Mean collision time	s
τ_D	Dielectric relaxation time	s
τ_e	Trap emission time	s
τ_{min}	Minority charge carrier lifetime	s
τ_t	Transit time in case of charge carrier diffusion	s
τ_{RC}	RC-time	s
Ψ	Wave function	$-$
Ψ_+	Symmetric wave function	$-$
Ψ_-	Anti-symmetric wave function	$-$
$\omega_{\mathbf{q}j}$	Angular frequency of a phonon in branch j with wave vector $\mathbf{q}$	s^{-1}

Physical Constants

Quantity	Symbol	Value
Electron-volt energy	eV	$1 eV = 1.60218 \times 10^{-19} C$
Elementary charge	q	$1.60218 \times 10^{-19} C$
Boltzmann constant	k_B	$1.38066 \times 10^{-23} J/K$
Vacuum permittivity	ϵ_0	$8.85418 \times 10^{-14} F/cm$
Planck constant	h	$6.62606957 \times 10^{-34} Js$

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Erklärung

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