Integrated realizations of reconfigurable low pass and band pass filters for wide band multi-mode receivers

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Contents

Abbreviations

SDR - Software Defined Radio
ADC - Analog to Digital Converter
LNA - Low Noise Amplifier
IF - Intermediate Frequency
RF - Radio Frequency
VGA - Variable Gain Amplifier
AGC - Automatic Gain Control
SAW - Surface Acoustic Wave
BAW - Bulk Acoustic Wave
LO - Local Oscillator
.AC - Alternative Current
.DC - Direct Current
DSP - Digital Signal Processor
Q,q - Quality factor
GSM - Global System for Mobile communications
UTRA - Universal Terrestrial Radio Access
UMTS - Universal Mobile Telecommunication System
WLAN - Wireless Local Area Network
SNR - Signal to Noise Ratio
f_S - Sampling frequency
BW - Bandwidth
LSB - Least Significant Bit
OTA - Operational Transconductance Amplifier
opamp - Operational Amplifier
MOS - Metal-Oxide-Semiconductor
CDN - Current Division Network
R_S - Source resistance
R_L - Load resistance
RSSI - Received Signal Signal Strength Indicator
$H(s)$, $H(j\omega)$ - Frequency responses
H_0 - In-band gain
SF - Steepness Factor
THD - Total Harmonic Distortion
Vrms - Volts Root Mean Square
F - Frequency scaling factor
f_C - Corner frequency
CLK - Clock
GND - Ground
T - time constant
NMOS, PMOS - N/P-channel MOS transistor
BiCMOS - Bipolar-CMOS technology
CMFB - Common Mode Feedback
VBE, VDS - Base-Emitter and Drain-Source voltages

VDD - Positive supply voltage
v_{peak} - Voltage amplitude
$A(s)$, $A(j\omega)$ - Frequency dependent attenuations
G - Gain
PTAT - Proportional To Absolute Temperature
IC - integrated circuit
g_m - transconductance paremeter
CCIIp, CCIIn - positive and negative second generation current conveior
VCVS - Voltage Controlled Voltage Source
VCCS - Voltage Controlled Current Source
CCCS - Current Controlled Current Source
RSSI - Received (or RMS) Signal Strength Indicator

Chapter 1

Introduction

The recent years have shown an explosive development of wireless communication products. The evolution of the semiconductor technologies greatly facilitated the progress toward smaller, cheaper and more reliable equipments. The technology supporting the actual wireless industry is very different compared to the disciplines of classical RF and microwave electronics. The new way of thinking RF circuits implies a thorough understanding of digital communications, conventional analog electronics and the multitude of existing or emerging communication standards [56].

The introduction of digital data communication, in combination with more and more powerful digital signal processing, created an opening for many new wireless applications. Most of these applications are built upon highly sophisticated modulation techniques and data encryption, resulting in a massive improvement of the wireless link quality [67].

The evolution in wireless communications sets new standards on the hardware part of the wireless interface. These specifications have become more and more demanding due to the trend toward higher quality services, lower cost, lower consumption and better portability of the equipment. With the downscaling of the technologies and the reduction of the supply voltages all these factors have been greatly improved in the digital part of the interface. However there still is a great bottleneck in the analog front end of the transceivers. In order to optimize the costs and the performance of the analog circuitry, several careful trade-offs are required between the key performance indicators of a circuit. The key requirements can be included in a hexagon of the trade-offs as presented in [56].

According to this representation, the design procedure is always reduced to finding the compromise between individual key parameters. A typical example in this sense is the trade-off between power consumption and linearity. The consumption increases invariably with the linearity and the high dynamic range requirements due to the higher currents pumped in the transistors in order to compensate their inherently non-linear behavior [37]. Another compromise must be achieved between gain and the frequency range in which the circuit operates as expected. In most

of the cases a high gain means lower frequencies as a result of the constant gain-bandwidth product of the amplifiers [4]. The set of key parameters to be optimized for each building block in the processing chain depends on the requirements of the target communication standard and on the performances of the other circuits in the transceiver. This set usually consists of one or two critical parameters. It is obvious that the feasibility of the circuits decreases with the number of parameters to be simultaneously optimized.

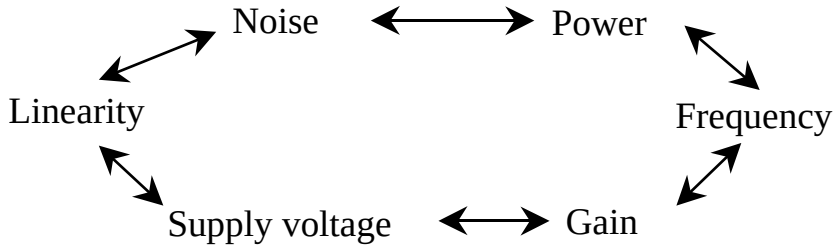


Figure 1.1: The trade-offs hexagon

As the optimization of the communication systems has been more and more successfully solved with the help of the advances in the semiconductor technology, the natural step forward in the development of modern communication devices is a result of the requirement to integrate the support for several communication standards in the transceiver. This would allow a communication with various wireless networks and implicitly a wider range of services offered by the same device. In the late '90-s the immediate goal of the wireless industry was to combine cordless and cellular phones in order to allow a communication link to be created virtually everywhere. Nowadays this ambition has been realized and the long term plan became the "omnipotent" wireless terminal that can handle voice, video, data and other services together with a sufficient amount of computing power [56]. The result would be the so called Personal Communication Services (PCS).

The first steps in the direction of offering several services supported by the same device has been made with the deployment of second generation (2G) mobile phones. The hardware architecture of 2G products was based on switched signal paths in the analog front-end of the transceivers. Each signal path was able to handle the signals specific to a single standard. The evolution of the technology allowed the removal of the redundant parts in the transceiver chain. The result was a partially switched signal processing circuit where only critical blocks have been switched. A conceptual example is given in Figure 1.2. In this scenario the filters corresponding to each standard are switched, together with the low noise amplifier, in order to achieve high selectivity and sensitivity for both the supported standards.

The next steps toward integrating multi-standard radios were the 2.5G and the third generation (3G) mobile terminals. The typical services supported by 2G, 2.5G

and 3G wireless systems are summarized in Figure 1.3. From this figure it can be seen that the evolution from 2G to 3G implies the transformation of the simple mobile telephony service into the possibility for Internet access, video conferencing and interactive application sharing, all these being parts of modern business life [39].

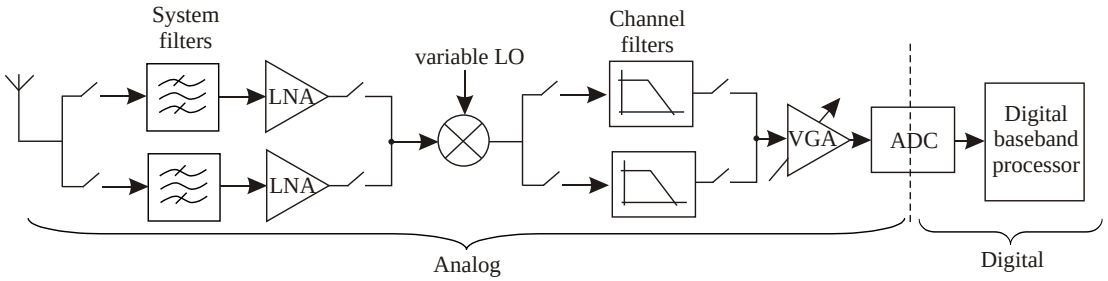


Figure 1.2: A conceptual example of switched signal paths for two different standards

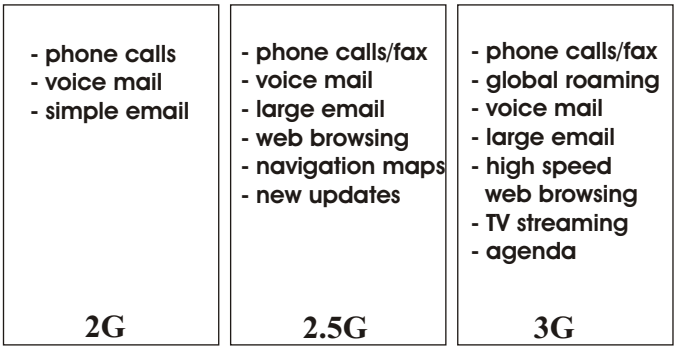


Figure 1.3: Features of the 2G, 2.5G and 3G wireless devices

According to the long term goals of the industry, a further improvement would be the support for virtually any existing or emerging standard within the given frequency range. The digital part of such a transceiver can be easily reconfigured by software in order to accommodate to any standard. The main obstacle in the way of further development is the analog front-end. Instead of having switched signal paths, a fully reconfigurable interface should be placed between the digital base-band processor and the antenna. The implications of these requirements are huge. When considering the necessity to handle a large number of standards without loosing performance the result is a wide band programmability. The main motivation for the wide band programmability can be represented hierarchically as given in Figure 1.4.

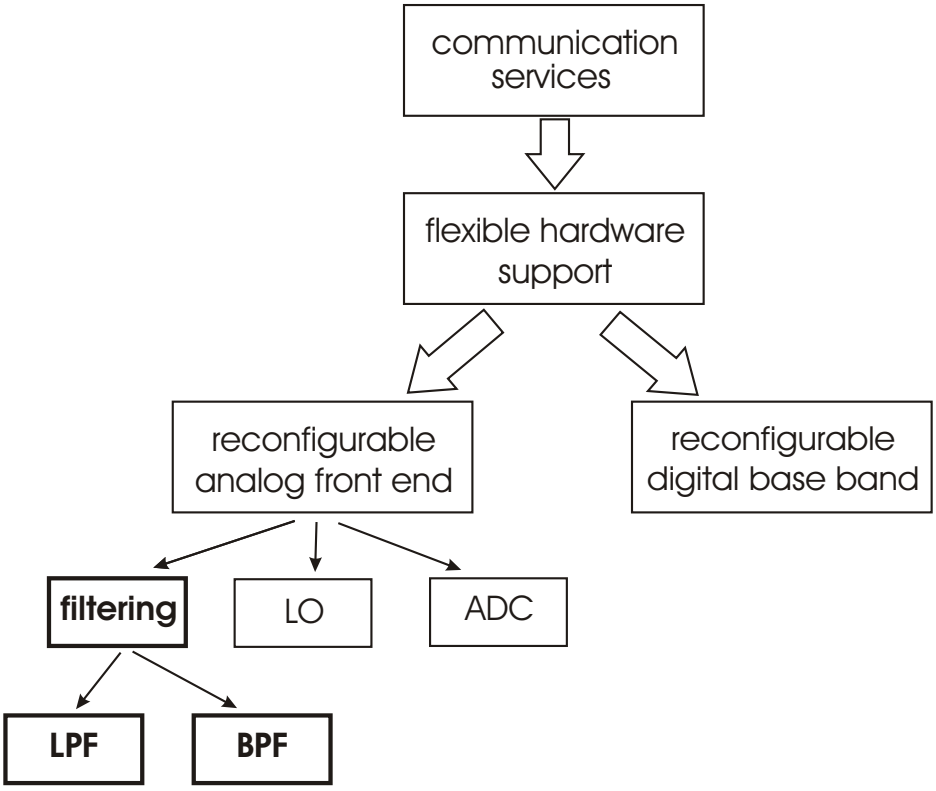


Figure 1.4: The motivation for a wide band programmability - a hierarchical approach

In order to be able to offer more and more services, multiple communication standards must be employed that help reducing interferences between the different applications. Each standard uses its own digital modulation, data encryption technique and carrier frequency. This means that the transceiver must be able to process signals with the carriers placed in a given frequency range. Therefore, a fully flexible hardware platform is required that can be reconfigured every time the user wants to employ another service. Digital equipment can be reconfigured by simply storing a more sophisticated program in a memory. The complexity of modern digital circuits supports the reconfiguration process without significant obstacles. The analog front end though, that prepares the signal for digital demodulation and interpretation, is known to be relatively rigid from the flexibility point of view, with several building blocks to be reprogrammed [44]. Among these components are the analog filters, local oscillators and data converters.

The software control of the transmitter part is relatively straight forward due to the fact that the transmitted signals are generated locally. The main problems emerge in the receiver path. There are several blocks that must be programmed for good performance. One of the most important circuits that must be fully programmable is the down conversion mixer. Since various standards have different carrier frequencies the mixers must be able to convert all these signals to some lower

frequency and eventually in the base band. This requires the local oscillator frequencies to be variable in a wide range. Other important blocks in a wide-band receiver are the channel select filter and the analog to digital converter. In most of the cases the programmability of the ADC can be simplified to the requirement for different noise shaping transfer functions for different standards. The channel select filter is causing most of the trouble in what is concerning programmability.

The main goal of the research presented in this thesis is the investigation of filter architectures suitable for wide band programmability and for different receiver architectures. The presentation follows in more or less detail the hierarchical approach presented in Figure 1.4. It includes a short study on receiver architectures suitable for multi-mode operation from the point of view of the analog filter. The final result of the investigations is a complete transistor level implementation of a fully programmable base band circuit and a feasibility study on the possible implementations of a programmable band-pass filter.

Chapter 2 deals with the main receiver architectures and their multi-mode capability. The accent will be on the specifications for the channel select filter. These specifications will be derived from different signal characteristics and the requirements emerging from the other blocks in the signal chain. Additionally some critical building blocks will be presented that make the integration of the wide-band channel select filter possible or not, depending on their performances. This chapter can be considered an identification of the main issues concerning the inclusion of the programmable filters in multi-mode receivers.

Chapter 3 gives some detailed motivations for the actuality of the research presented in this work. Here the emphasis will be on the identification of the problems that emerge due to the nature of transmission and of the channel. The problems are mainly connected to the sensitivity and the selectivity of a wireless receiver. This section also describes the necessary circuits that help maximizing these parameters. The description of the circuits is followed by a survey of the literature, intended to give the state of the art in filter and variable gain amplifier design. The circuits found in the literature are analyzed mainly from the point of view of the flexibility, possible non-idealities and the ease of programming.

Chapter 4 describes the complete design of a fully programmable base band circuit suitable for direct conversion or multi-port receivers. The chapter starts with the block specifications of the circuits derived from the constraints of the overall receiver architecture and advances toward a complete transistor level design using a $0.35\mu m$ BiCMOS process. The detailed design steps of each building block of the filter are also given. This chapter ends with some system aspects regarding the base-band circuit, such as biasing, a digital programming interface and a wide band frequency error correction system.

Chapter 5 gives some simulation and measurement results for the proposed

base band circuit. Among these the most important are the frequency response, the transient response, the gain-code correspondence of the variable gain amplifier, the gain step error and the functionality of the corner frequency error correction system.

Chapter 6 presents some investigations on possible implementations of high Q band-pass filter architectures. The starting point is once again the set of specifications. This chapter can be considered as a feasibility study on the implementation of narrow bandwidth and high center frequency band pass filters suitable for receiver architectures with sampling at the intermediate frequency. The main concern here is on feasibility, precision, flexibility and the full integration of the circuits.

Chapter 7 gives some conclusions for the achieved results and offers some perspectives for further research.

Chapter 2

Receiver Architectures Suitable for Multi-Mode Operation

After its first presentation to the design community in 1992 the concept of software defined radio (SDR) received much attention among researchers working in the field of wireless communications. The technical reason behind the popularity of the SDR is the development of reconfigurable devices for digital signal processing such as digital signal processors or FPGA-s. Recent digital signal processors can operate at high speeds and have sufficient complexity required by the full reconfigurability. Therefore, the real challenges facing SDR are the analog front-ends of the transceivers [33].

A large part of the research done in the field of SDR focuses on the software component. This is the reason why the concept of the ideal SDR has gained a great importance. The architecture of the ideal SDR is given in Figure 2.1 [44].

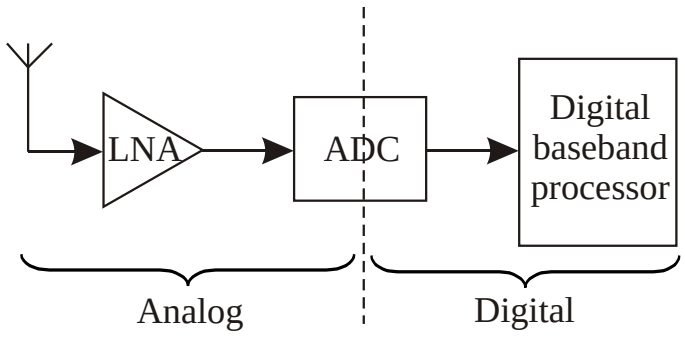


Figure 2.1: The architecture of the ideal SDR

The architecture specific to the ideal SDR is disconsidering partially or totally the analog front end of the receiver and samples the received signal directly at the carrier frequency. This requirement is imposed by the need to perform most of the necessary signal processing in the digital domain. The feasibility of this architec-

ture faces strong limitations. These limitations are mainly due to the analog to digital converter. If we consider the fact that the wanted signal power can vary between -100dBm and 0dBm and the blocking signals can have power levels around 0dBm, the feasibility of the ADC becomes a real challenge [57]. The dynamic range requirements, that result from a reasonable signal to noise and distortion ratio of the front end, can easily reach 100-120dB. This leads to an effective number of bits equal to 17 to 20. An ADC with this kind of specifications would typically consume a few hundred mA current, which is in contradiction with the idea of portability and prolonged battery life of the mobile terminal. It results that a more realistic evaluation of possible receiver architectures is required based on the realizability of each individual building block of the front-end [44]. The considered architectures could include the zero-IF, the low-IF, the classical super heterodyne and the IF-sampling receivers. These more or less classical architectures seem to offer more or less flexibility in reconfiguration for multi-mode operation. The possibility to accommodate with different standards requires a very careful evaluation of the feasibility. In the next paragraphs all the mentioned architectures will be analyzed in what concerns flexibility and programmability. A few aspects regarding the individual block specifications with an emphasis on the channel select filter will also be presented.

2.1 The classical super heterodyne architecture

The classical super heterodyne architecture has been the most popular receiver type used so far. Its popularity is due to well known operation and the possibility to precisely predict achievable performances. The main feature of the superhet architecture is that it uses at least two frequency conversions. After the first down conversion the signal is centered on the intermediate frequency (IF). The topology of a general superhet receiver is given in Figure 2.2 [56][67].

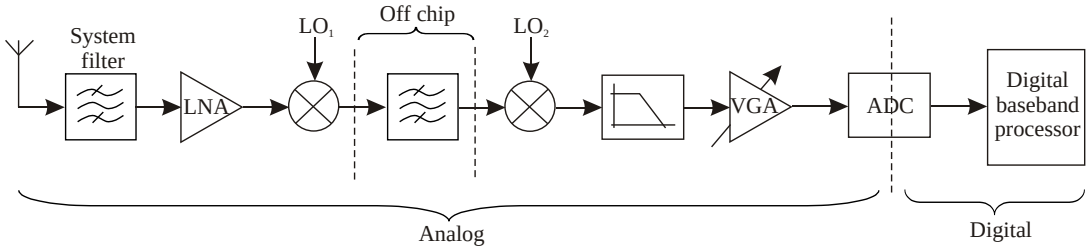


Figure 2.2: The general architecture of the classical superhet receiver

The RF signal received by the antenna is first passed through a system filter. The main purpose of this high frequency band-pass filter is to provide preliminary suppression of the out of band blocking signals and to separate the transmitter from the receiver. The necessity of the system filter is determined by the received signal spectrum specific to each standard and the directionality of the communication. Next the signal is passed through a low-noise amplifier which selectively gains up the

signal in the desired frequency range. The RF mixer performs the down conversion from RF to the intermediate frequency. At the IF the signal is filtered by a narrow bandwidth band-pass filter that usually provides channel or band selection. The second down conversion brings the signal in the base band or to some low center frequency where a low-pass filter performs anti-aliasing and the final suppression of the undesired frequency components. The purpose of the automated gain control (AGC) circuit is to adapt the signal magnitude to the full scale requirements of the ADC regardless on the received signal power [43]. This procedure must be done partly for an amplification of the wanted signal, if its level is too low, or on the other hand for an attenuation, in order to avoid the saturation of the converter if the signal level is too high.

The main problem in heterodyning is to find the trade-off between the required image rejection and the adjacent channel suppression. If the intermediate frequency is high, the RF signal is relatively far from its mirror image and the local oscillator in the frequency domain. In this case the system filter has reasonable headroom for the suppression of the image. On the other hand, the IF band pass filter must have a large center frequency together with a narrow bandwidth for channel or band selection. This idea leads to a requirement for high Q band-pass filters. These filters are not feasible in today's semiconductor technologies due to their inherently large consumption and massive component spread. The solution to this problem was so far to use off-chip passive or SAW filters [35][56][67]. If the intermediate frequency is low, the requirements for the IF filter are relaxed, but the RF signal is much closer to its mirror image. Therefore, the system filter must introduce significantly larger attenuation for the mirror signals and its realization becomes difficult. The two cases are illustrated in Figure 2.3.

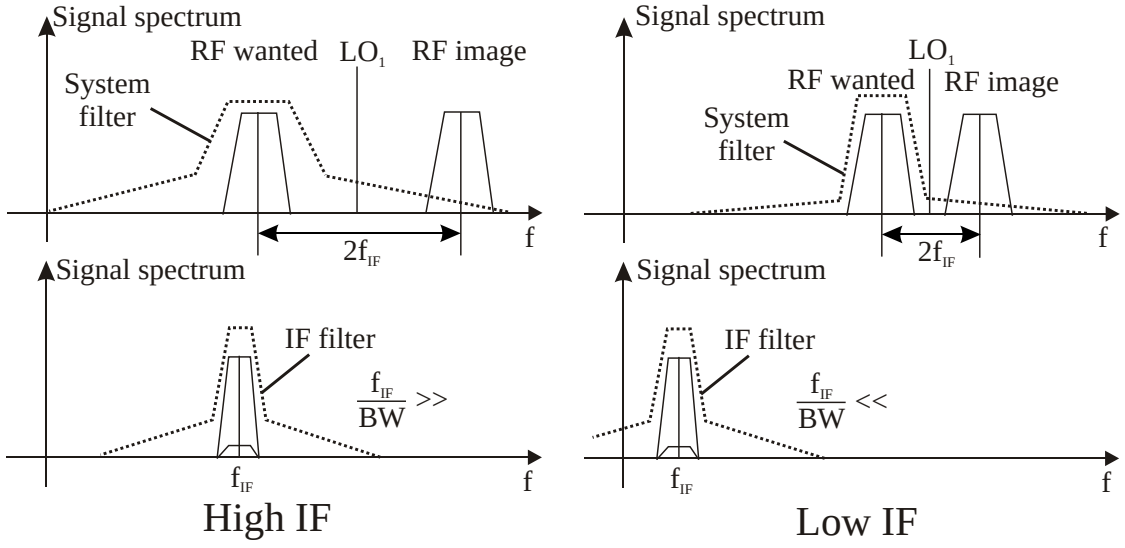


Figure 2.3: Filtering requirements for high and low intermediate frequencies

Another important drawback of superhet receivers is that, because of the external filters, the LNA and the first mixer must drive an 50Ω impedance. This requirement tends to increase the noise and the consumption [35].

The image rejection ratio of the superhet architecture can be improved when employing the so called image reject topologies, such as Hartley or Weaver. However these structures are much more susceptible to gain and phase mismatch in the quadrature signal paths. A detailed explanation of the image problem and some suitable improvements are presented in [48][56][67].

The possibilities to employ a heterodyne architecture in a multi-mode mobile receiver must be investigated from the perspective of the requirements given in the introduction of this chapter. From the point of view of the full programmability and flexibility requirements the superhet receiver is not very efficient. This structure turns out to be very rigid due to the large number of components to be programmed. In order to reconfigure the analog front-end, almost every building block of the chain must be reconfigured with a time continuous signal or by some digital code. This procedure becomes nearly impossible with the off chip band-pass filter.

In what concerns the low analog component count, low consumption, full integrability and low cost the heterodyne architecture fails again. The main bottleneck is once again the off chip band-pass filter. The sensitivity and the image rejection ratio of the receiver could also be seriously influenced by nonlinearity and component mismatch [56].

2.2 The direct conversion architecture

Direct conversion receivers have been invented some decades ago. Along the years they have been studied and several implementations have been tried. Most of these implementations failed to achieve the expected performances. There are some very important reasons for these failures among which the following can be mentioned: the inherent DC offset, the high dynamic range requirements, I/Q gain and phase imbalance, LO leakage to the antenna, second order distortion and the susceptibility to flicker noise [48].

With the advances in digital communications and signal processing the direct conversion principle became a topic of interest again. There are multiple attractive features that can be exploited by modern wireless receivers. The first major advantage of the direct conversion architecture is that it makes a monolithic implementation easier than other architectures. The next important advantage is that it suffers much less from mismatch than the classical image reject architectures. Probably the most important reason for the renewed interest is the fact that most of previous failures in achieving the desired performance arouse from the effects that were inherent and could not be removed from discrete implementations. These effects can be controlled and compensated in the fully integrated version. In other

words, direct conversion is one of the few architectures whose drawbacks can be controlled by means of a simple increase in the number of the transistors. The block diagram of a practical direct conversion receiver is given in Figure 2.4 [57][6].

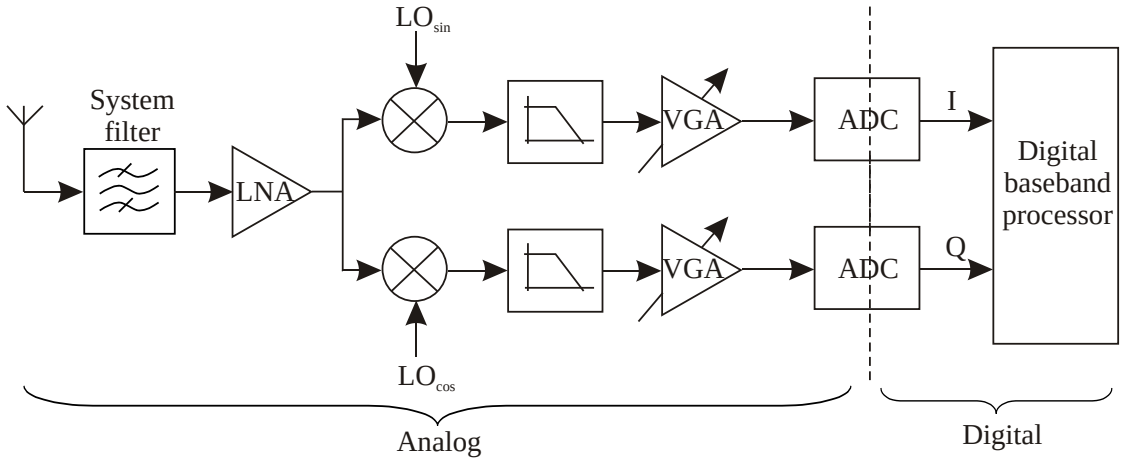


Figure 2.4: Block diagram of a practical direct conversion receiver

The high frequency part of the front-end is similar as for the superhet receiver. The down conversion to the base-band is performed by a quadrature mixer. Each of the signals on the I and the Q paths are low-pass filtered for channel selection. The signal levels are adapted for analog to digital conversion by the automated gain control circuit.

The direct conversion architecture has several advantages over the classical superhet receiver. The first advantage is concerning the image signals. Since the LO frequency is synchronized with the RF, the mirror signal is the wanted signal itself. However, this feature alone does not totally eliminate the problem of the image signals. Practically the sidebands of the signal at negative and positive frequencies are each other's mirror images. When they are down converted to the base-band they will be superposed. At this level the two become inseparable and the signal can be ultimately corrupted. This problem can be solved by employing quadrature down conversion [56][67].

Another significant advantage of the direct conversion architecture is that the need for a high frequency, narrow-bandwidth band-pass filter has been eliminated. As one of the main requirements for SDR is flexibility, the elimination of a fixed frequency, off-chip filter from the architecture has huge impact on the utility of the architecture for SDR. The various possibilities to implement a wide-band, fully programmable low-pass filter create an opening toward multi-mode operation [38].

Although the major issues regarding a monolithic integration of a multi-mode direct conversion receiver have been solved, there are several other problems inherited from the fixed frequency architecture. Moreover, these problems could be

aggravated by multi-standard specifications. These problems are the DC offset and the flicker noise. A typical case, from the point of view of the DC offset, is when the multi-mode operation includes low bandwidth standards such as GSM. In this case the elimination of the DC offset through AC coupling is not possible without significant deterioration of the signal spectrum. Digital processing helps in decreasing the offset through feedback algorithms between the DSP and the input of the ADC [47].

From the point of view of the low analog component count and low power consumption the direct conversion receiver offers good performances. This advantage is emphasized by the fact that all the signal processing, that requires high dynamic range and good linearity, is done in the baseband. This means that filtering and amplification can be implemented with a relatively small number of active components connected in closed-loop configurations. The consumption is further reduced because the mixer and LNA do not need to drive low impedance loads as in the case of the off-chip band-pass filter for the superhet receiver.

2.3 The IF-sampling architecture

In classical superheterodyne architectures, after the signal has been converted to the intermediate frequency there is a need for a second down conversion and filtering before analog to digital conversion. However these operations can be performed more efficiently in digital domain. This observation also meets the basic idea of having as few analog components as possible, comprised in the concept of the software defined radio. Performing the second down conversion in digital domain implies the shift of the analog to digital converter from low frequencies to the intermediate frequency. The resulting IF sampling architecture is presented in Figure 2.5 [6][8][31].

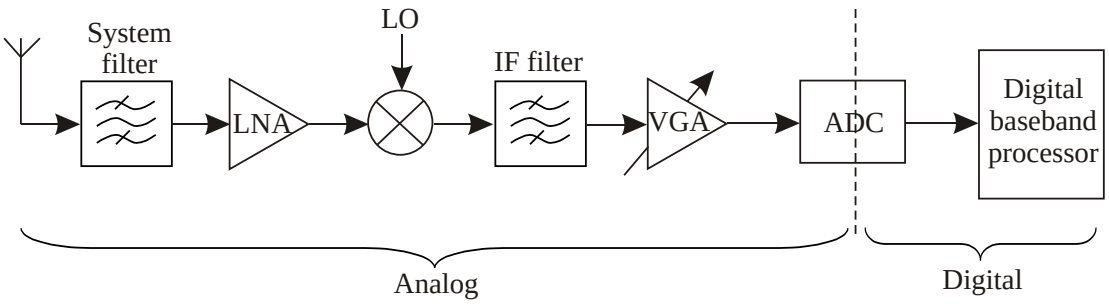


Figure 2.5: Block diagram of an IF sampling receiver

This architecture places stringent requirements on the analog to digital converter and the preceding analog band pass filter. Since the input signal of the ADC is in the mV range, the noise introduced by the converter should be sufficiently low. Additionally the ADC should exhibit a very good linearity in order to process large interferers while minimizing the corruption of the signal by intermodulation. The

main purpose of the band pass filter is the suppression of the blocking signals and to eliminate the aliasing components of the wanted signal. The performance and the specifications of the band pass filter depend on the choice of the intermediate frequency. If the intermediate frequency is chosen too low the specifications will require a nearly ideal magnitude response for the system filter in order to sufficiently attenuate the blocking signals in the adjacent channel. If the intermediate frequency is very large the specifications for the IF band pass filter are difficult or even impossible. Therefore, the choice of the intermediate frequency depends on the trade-off between the feasibility and the selectivity of the system filter and the channel- or band select filter.

2.4 Architectures summary

The basic principles discussed in the previous paragraphs are present in some form in every other receiver architecture. When analyzing their behavior in what concerns flexibility the following conclusions can be drawn:

1. the superhet receiver performs very well when a single standard operation is required. In this case the receiver can offer relatively high performance with reasonable complexity and clearly has several advantages over other architectures. When it comes to a multi-mode operation the performances are drastically decreased by the lack of flexibility. Therefore, this architecture is less suitable for software defined radio realizations.

2. the direct conversion receiver offers a lot of flexibility due to the reduced number of analog building blocks. It is also attractive due to the fact the most of the signal processing that requires high dynamic range is done in the base band. The condition for a correct functionality is the rigorous control of the DC offset, especially when the variable gain amplifier included in the AGC loop exhibits very large gain values. This condition is equally valid for the reconfigurable and the fixed frequency implementations.

3. the IF sampling receiver can potentially offer similar performances as the direct conversion receiver. Its main advantage is that the DC offset problem has been eliminated by sampling the signal at the intermediate frequency. The condition for a correct functionality is the implementation of a suitable IF band pass filter and of a high frequency variable gain amplifier, both with sufficient dynamic range and linearity.

Chapter 3

The Problematic of Filtering and Automated Gain Control in Wireless Receivers

The ultimate goal of the analog front end is to convert signals from very high frequencies to lower frequencies where they can be digitized and interpreted by the digital circuitry. The quality of the sampled signal is highly dependent on the dynamic range and the selectivity. In the previous paragraphs has been stated several times that that filtering has a great impact on the overall performance of a wireless receiver, regardless on the receiver architecture or frequency distribution. The quality of the filtering provided by the analog front end will define the dynamic range and the selectivity of the system [5].

Another important issue regarding the selectivity and dynamic range is the power of the received signal and the efficiency of the frequency conversion. One of the main requirements in any receiver is to be able to provide a high quality sampled signal even in the case when the strength of the received signal is very low [43]. On the other hand, if the received signal is very strong the front end should not saturate the analog to digital converter. The solution to this problem is the automated gain control circuit. The problem of filtering and the automated gain control are often regarded together due to the fact that both have a great impact on the selectivity.

3.1 Filtering requirements in multi-mode wireless receivers

Software defined radio is intended to accommodate to several existing and future standards. Due to the structure of the communication networks and the characteristics of the wireless link the spectrum of the received signal will always look similar, regardless on the chosen standard. As a result, the problems connected to the processing and preparation of the signal in the analog front end will also be similar. The shape of the spectrum for a general received signal include the elements

presented in Figure 3.1 [46][56][57]. It is of great importance that the magnitude of the wanted signal can be as low as -100dBm. Besides the wanted signal the received spectrum includes in-band interfering signals due to adjacent channels and out of band blockers due to standards that are using the neighboring frequencies. The worst case scenario at the definition of the specifications for a receiver usually implies very weak wanted signals and very large blockers.

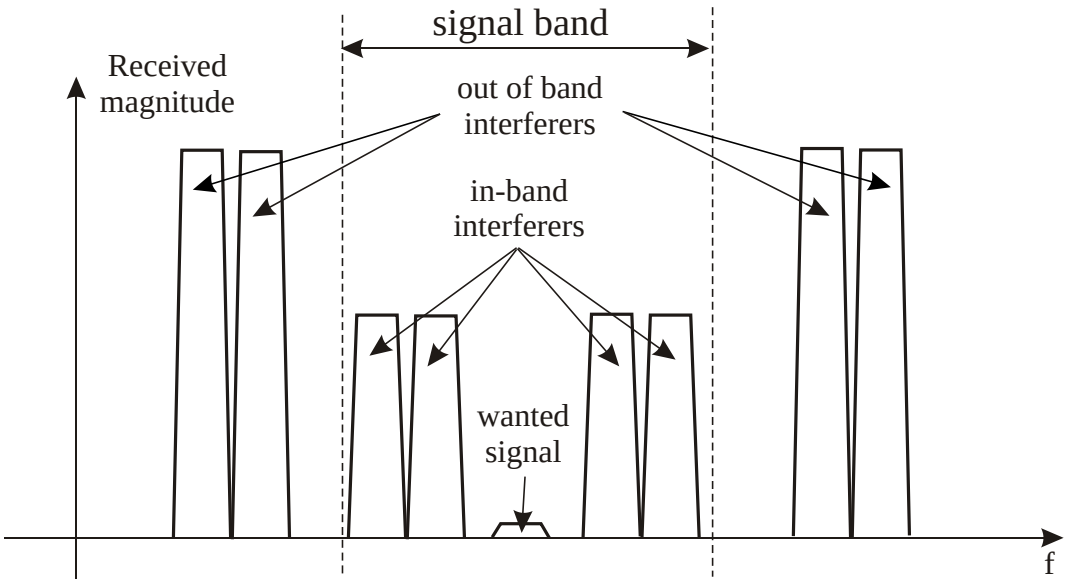


Figure 3.1: Shape of a typical received signal spectrum

In building receiver architectures it is a common practice to attenuate out of band blocking signals by means of a radio frequency system filter and the frequency dependent gain of the low noise amplifier. In spite of the attenuation provided by the high frequency part of a receiver the out of band blocking signals can still reach significant magnitudes compared to the wanted signal.

The small wanted signal power at reception is mainly due to propagation over distance and fading. It can be shown that signals propagating in a free space will experience a power loss proportional to the square of the distance from the source. However, if the signals travel through direct and reflected paths, the power loss increases with the fourth power of the distance. In crowded areas such as urban canyons the signal exhibits different phase shifts due to longer paths and multiple reflections. Statistically there is a possibility for the direct signal and a reflected signal with the same power to arrive to the receiving antenna with a 180° phase shift. These signals will effectively cancel each other and the received signal will be very weak. This phenomenon is called multi-path fading [56].

Blocking signals can exhibit significant power levels compared to the wanted signal. The most important issues concerning the large difference between wanted

and blocking signals are created by in-band interferers. The main reason for this is that the gap in frequency between the wanted signal and the in-band blocking signals is relatively small. As a consequence, the filter, used to attenuate in-band interferers, requires a very steep roll-off and high linearity.

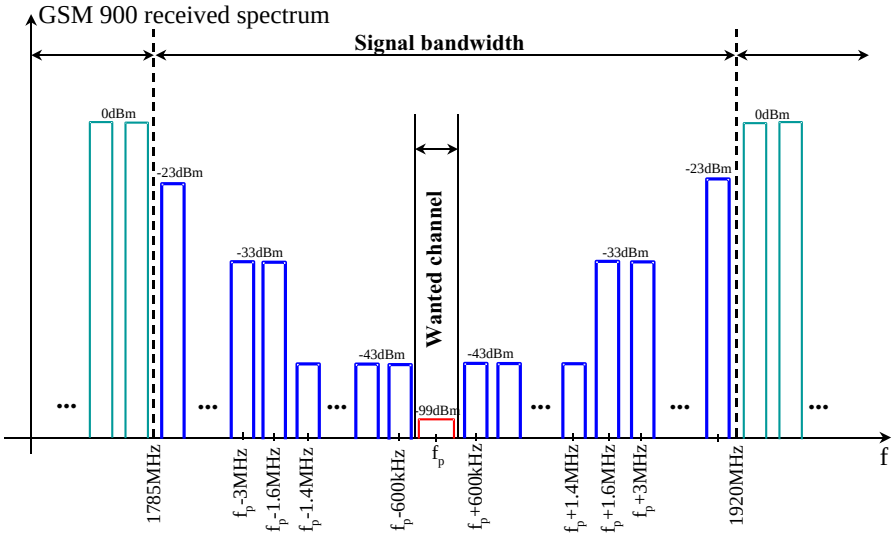


Figure 3.2: Shape of a GSM900 received signal spectrum

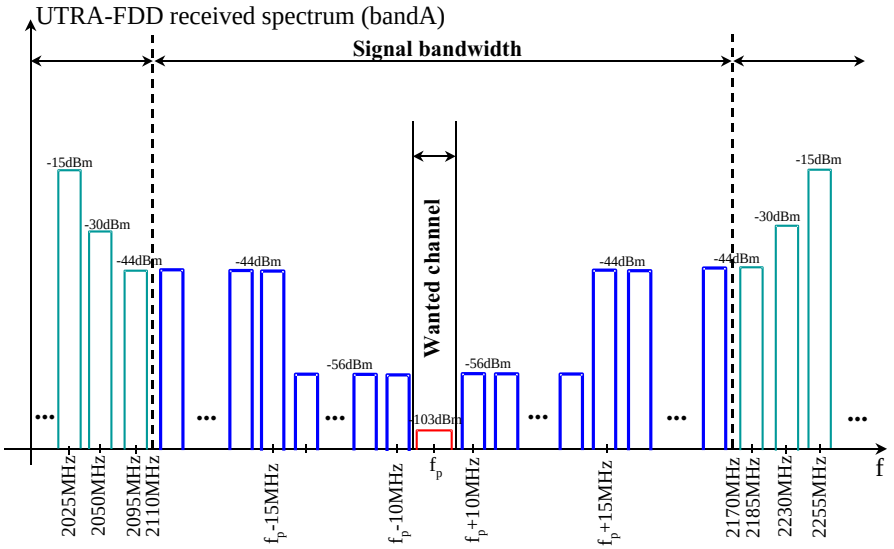


Figure 3.3: Shape of a UTRA-FDD received signal spectrum

A typical received spectrum for a GSM receiver is presented in Figure 3.2, as given in [46][67][80]. It can be seen that the wanted signal can be as low as -99dBm. The nearest in-band blocking components, placed at a 600kHz distance

in frequency, exhibit a power equal to -43dBm. At a 1.6MHz distance from f_p the blocking profile indicates -33dBm. From the spectrum of the received GSM900 signal results that the GSM standard has one of the most demanding set of specifications due to its very narrow, 200kHz channel bandwidth. Another standard example that is very often used in mobile communications is UTRA. The received spectrum corresponding to the UTRA standard is presented in Figure 3.3. It can be seen that the blocking specifications of the UTRA standard are lower compared to GSM. It is also of importance that the channel bandwidth is 3.84MHz with a distance between carriers of 5MHz [73].

One of the most important factors determining the performances of the entire receiver is the analog to digital converter (ADC). The specifications for the ADC are directly derived from the spectrum of the signal that is being sampled and digitized [75]. If the interferers are very large the ADC must be highly linear in order to be able to process the largest components in the sampled spectrum without significant distortion. This requirement is necessary for avoiding the corruption of the wanted signal by intermodulation. When the linearity of the ADC is not sufficient, the higher order harmonics of the strong blocking signals will be effectively mixed with each other. The resulting intermodulation product can fall back in the band of the wanted signal. In particular, the most damage is usually produced by the third order intermodulation products, as illustrated in Figure 3.4 [56].

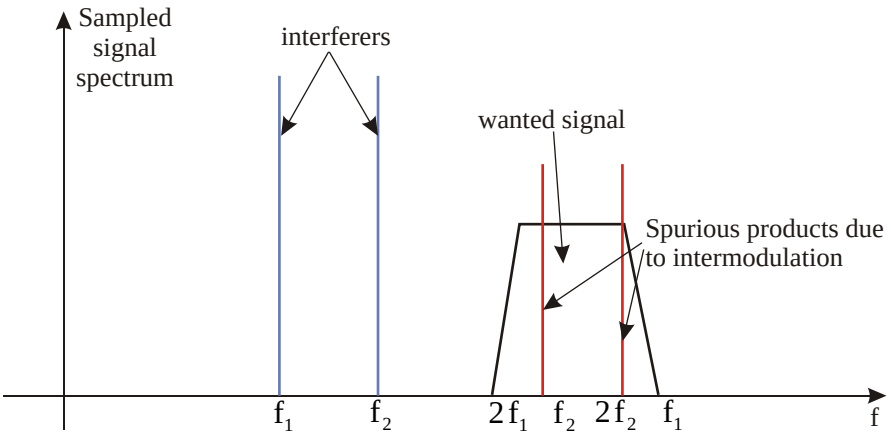


Figure 3.4: Corruption of the wanted signal by third order intermodulation products

Another important requirement for the ADC, also connected to signal levels, is dynamic range. Dynamic range can be defined as the ratio of the maximum input level, that the circuit can tolerate, to the minimum input level that provides a reasonable signal quality. In the case of the ADC this definition is changed to adapt to the specific nature of the circuit. The upper limit of the dynamic range ca be defined based on the intermodulation behavior of the converter. This limit is

considered as the maximum signal level of a two tone input signal for which third order intermodulation products do not exceed the noise floor [56]. The lower limit of the dynamic range is defined based on the sensitivity behavior of the circuit. The most often used parameter that characterizes sensitivity is the signal to noise ratio (SNR). Using this definition, the lower limit of the dynamic range is the signal level where the ADC can provide a minimum chosen signal to noise ratio. The dynamic range defined this way is called spurious free dynamic range. It results that the dynamic range of an ADC can be determined from the expression of the signal to noise ratio. The maximum achievable signal to noise ratio of an N-bit oversampled analog to digital converter can be written as in equation (3.1) [4][25].

$$SNR_{max} = 6.02 \cdot N + 1.763 + 10 \lg \left(\frac{f_S}{2BW} \right), \tag{3.1}$$

where N is the number of bits, f_S is the sampling frequency and BW is the signal bandwidth. From this definition it can be seen that a Nyquist rate converter offers approximately 6dB dynamic range for every bit. When oversampling is used, the dynamic range also increases proportionally with the ratio between the sampling frequency and the signal bandwidth, written in dB.

For an ideal ADC the dynamic range is equal to the maximum achievable signal to noise ratio. As a consequence the dynamic range of the converter is highly dependent on the number of bits. A typical example can be given in the case when the GSM signal is sampled directly at the antenna: From GSM specifications is known that the wanted signal power can vary between -102dBm and -12dBm. The minimum value for the signal to noise ratio, for which the signal can still be correctly interpreted by the digital base band processor, is taken 9dB. The resulting dynamic range of the ADC is approximately 100dB which yields 17 bits in the ideal case.

The least significant bit is regularly lost to quantization noise due to level uncertainties [4]. As a consequence, an N bit ADC can provide at its best a dynamic range corresponding to an N-1 bit ideal ADC. The loss of the least significant bit will result in a dynamic range decrease with approximately 6dB and this bit is effectively disregarded in the conversion process. In real ADC-s there is not only the LSB that is disregarded due to quantization noise. The quantization noise is considered as a white noise, whose continuous spectrum spreads across the entire frequency range of the sampled signal. All the input signal levels, that are smaller than the noise floor, will produce level uncertainty. In practice this is the case for several low order bits. Known techniques used for the control of the quantization noise, such as dithering, may use these low order bits and the ADC will effectively work as an ideal ADC with three or four bits less resolution.

The loss of the dynamic range due to quantization noise is highly important in receivers. If one attempted to sample the received GSM signal from Figure 3.2 early in the receiver chain the ADC would require approximately 100dB dynamic range which corresponds to an effective number of bits equal to 17. Due to quantization

noise the real ADC should be designed for a minimum resolution of 20 bits. Since the consumption of an ADC varies according to the exponential of the resolution a 20 bit converter would consume an enormous amount of power and it is not feasible for implementation. From this follows that the sampled signal should be preprocessed and the spectrum should be leveled for a frequency distribution of the magnitudes as equal as possible. In many cases a careful system design requires the magnitude of the wanted signal to be approximately equal to the magnitude of the filtered interferers [67].

The purpose of the analog front end is to reduce the dynamic range requirements for the ADC. This is done through consequent amplification and filtering. The preprocessing in the analog front end should be highly linear in order to avoid intermodulation, as mentioned earlier. The typical shape of the signal after filtering and amplification is given in Figure 3.5 [6]. From this figure it can be seen that the wanted signal has been amplified and the interferers have been filtered. The dynamic range requirements have been greatly reduced through preprocessing.

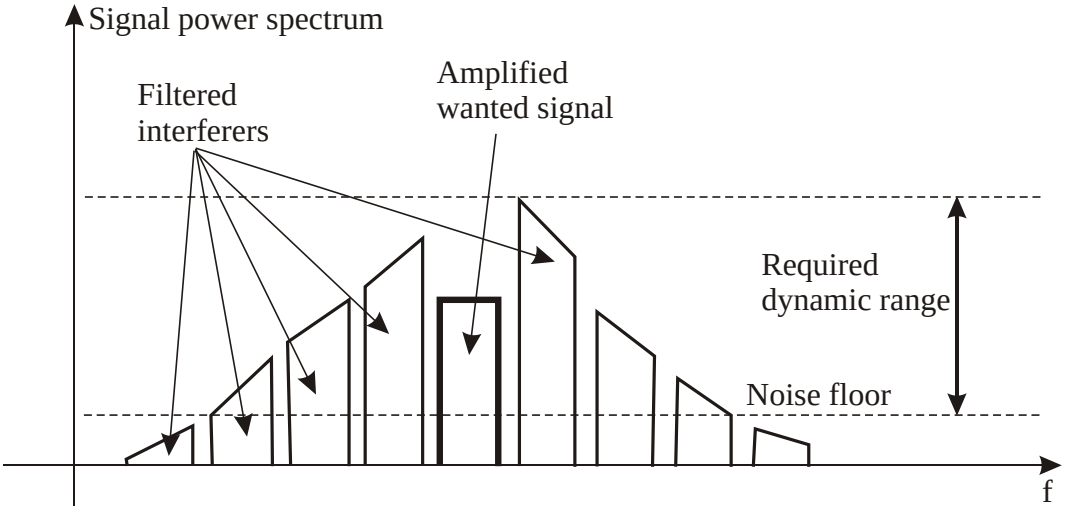


Figure 3.5: Typical spectrum of a signal before sampling

The problems concerning the dynamic range are well known by system engineers and have been dealt with in the case of single standard receivers. However an important issue in the problematic of the dynamic range in software defined radio arises from the need for high flexibility and the support for virtually any existing or emerging standard. Obviously, the signal corresponding to a wider bandwidth standard cannot be filtered with a narrow band filter due to the requirement to keep the wanted signal intact. In the case, when a narrow bandwidth signal is filtered with a wide band filter, the provided attenuation may not be sufficient [6]. Even when the filter specifications would impose a near brick wall response the dynamic range requirement for the ADC could be prohibitively large. A solution to this

problem is to use a filter with programmable bandwidth.

In most of the modern communication systems capable of multi-standard operation the signal is multiplexed through several analog filters, each designed for a given standard. Besides high overhead, the drawback of this approach is that it limits one particular architecture to only a few specified standards. Software defined radio requires the analog front end, and specifically the analog filter, to comply to all the standards in a given frequency range while maintaining the dynamic range requirements for the ADC constant. Due to these problems the idea of wide band programmability of the filter bandwidth was born. In this scenario a single, programmable bandwidth filter is used instead of several switched filters. The concept of bandwidth programmability is similar to classical auto tuning but in a much wider frequency range and far greater precision. In the ideal case the programming range should be covered continuously. Most of the real implementations found in the literature employ a digital programming strategy, with a sufficiently large number of bits in order to keep intervals between two consequent bandwidth settings as small as possible [35][38][53][65].

From the discussion above results that the main motivation for the wide band programmability of the filter is the necessity to maintain the feasibility of the ADC in a software defined radio environment by limiting its dynamic range requirements, regardless of the considered standard. The second important motivation would be an efficient anti-aliasing before sampling the signal.

The most important specifications of a programmable filter are concerning attenuation at the cutoff frequency, the in-band ripple, the variation of the group delay in the signal band, the programming range and the precision, the generated noise and the linearity.

The problems emerging in design are dependent on the filter type. When direct conversion, multi-port or low-IF receivers are considered the analog filter has a low pass response. Since the wanted signal is in the base band, a special concern must be taken on the DC offset and the flicker noise. If the signal spectrum is not prohibitive (e.g. in the case of GSM with narrow bandwidth), an AC coupling should be used in order to attenuate DC offset and to shape the dominant flicker noise.

For wide band IF sampling architectures a band pass filter is employed which realizes channel or band selection and anti-aliasing. In this case the specific problems are the choice of the intermediate frequency, the signal alias overlapping, the programming of the bandwidth independently from the center frequency, the conservation of the response shape and approximation, the programming precision and the feasibility of high Q realizations.

3.2 State of the art in programmable filtering

This paragraph is intended to give an insight into the filtering problem solved in modern wireless receivers, with emphasis on existing auto tuning methods compared to wide band programmability. The filtering methods used in today's receivers should be discussed in two main categories, depending on the receiver architectures they are intended for.

3.2.1 Band pass filters

As shown in the previous chapter, wide-band IF-sampling receivers require a band pass filter for attenuating the interfering signals and for anti-aliasing purposes. The intermediate frequency is usually chosen sufficiently high in order to avoid the overlapping of the aliasing components for wide band standards (e.g. WLAN) and to increase the feasibility of the RF system filter. Due to high intermediate frequencies the center frequency of the filter is inevitably large. In the case of narrow bandwidth standards, such as GSM, the high center frequency is always combined with very stringent selectivity requirements. This leads to large values for the quality factor. It is well known from filter theory that an increase of the quality factor produces a larger spread of the component values and reduced feasibility. Furthermore, the limited precision of the center frequency and the bandwidth often proves to be prohibitive on monolithic integration of the filters. This is the reason why conventional, single standard receivers employ a passive filter in the form of a ceramic, crystal or surface acoustic wave (SAW) structure. The main advantages of these filters are the high linearity, the low noise and the fact that they require no external power supplies [35][38].

In multi-mode filtering for software defined radio the bandwidth of the IF filter should accommodate to multiple standards and should be programmable over a wide frequency range while maintaining the shape of the attenuation characteristic. The center frequency should also be tunable in order to compensate variations with process and temperature. The lack of flexibility and the impossibility to integrate the devices makes passive filters unsuitable for software radio solutions.

One of the most well known band pass filter architectures, that allows very narrow bandwidths and high center frequencies, is the so called Q-enhanced filter [35][38][45]. The principle of realization is to implement an LC resonant circuit and to enhance the damping resistor with a negative resistance. The typical schematic of a second order band pass filter section implemented with an LC resonant circuit is given in Figure 3.6.

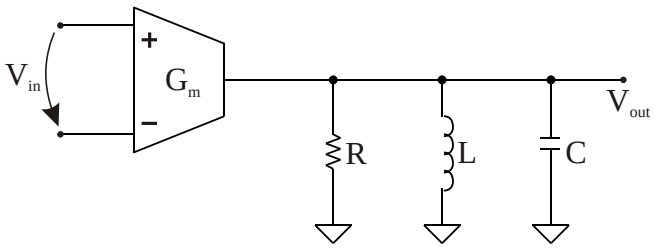


Figure 3.6: A second order band pass section with LC resonant circuit

The transfer function of the circuit can be written as follows:

$$H(s) = G_m R \cdot \frac{\frac{1}{RC}s}{s^2 + \frac{1}{RC}s + \frac{1}{LC}} \tag{3.2}$$

The resonant frequency and the quality factor are:

$$\begin{cases} \omega_0 = \sqrt{\frac{1}{LC}} \\ Q = R \cdot \sqrt{\frac{C}{L}} \end{cases} \tag{3.3}$$

From the expression of the resonant frequency and the quality factor it can be seen that, once ω_0 has been fixed, the quality factor is adjustable through the resistance R. In order to achieve narrow bandwidths the resistance must be very large. The method proposed in [35] and in [38] for Q enhancement employs a negative resistance connected in parallel with R. The expression of the quality factor becomes:

$$Q^* = \frac{R_{neg} R}{R_{neg} - R} \cdot \sqrt{\frac{C}{L}} \tag{3.4}$$

From this equation results that an infinitely high quality factor can be achieved if the condition $R = R_{neg}$ is fulfilled. R_{neg} is the absolute vaue of the negative resistance. This means that the filter bandwidth can theoretically be infinitely small. The smallest possible bandwidth is usually limited by the finite output resistance of the transconductance cell and by component mismatch.

The main drawback of Q-enhanced filters is the lack of control over the in-band gain of the circuit when the bandwidth is changed. Additionally the linearity

requirements of the transconductance amplifier could be very demanding. An important issue is concerning the precision of the center frequency and the bandwidth. In chapter 6 a detailed design methodology will be given together with a feasibility analysis of Q-enhanced filters. The accent will be put on designing for controlled magnitude responses and approximations. Additionally the precision requirements will also be described.

Another method for band pass filter design is to implement complex polyphase filters [13][67]. The preliminary condition to polyphase filter design is the existence of two quadrature signal paths in the receiver. This is usually not a problem since quadrature signal processing is required also by image rejection techniques. The functionality of active complex polyphase filters is based on the shifted response of a low pass prototype. The frequency transformation is linear instead of the classical low pass to band pass transformation. The linear frequency transformation implies adding a frequency dependent quadrature component to each voltage drop on a capacitor in the low pass prototype. A detailed explanation of the linear response shift and the design procedure has been given in [67] for passive and opamp-RC polyphase filters. The OTA-C complex filters can be implemented using the methods described in [13]. Opamp-RC filters are not discussed here since they do not have the potential to work at high center frequencies. Passive complex filters are band reject structures that are more suitable to attenuate certain frequency components. The filter architectures used for high frequency operation are based on OTA-C structures in most of the cases. This design method also has potential for fully integrated realizations. The main obstacle here is the limited precision of the frequency parameters.

There are also other, classical filter implementations in the literature, as shown in [6][12][53][62]. These are mostly suitable for lower center frequencies and larger bandwidths. Programming the bandwidth usually means the compensation of the tolerances with process and temperature. Chapter 6 gives a detailed overview on the feasibility of different band pass filter architectures. Some research results, that are meant to improve the feasibility of high Q integrated band pass filters, will also be presented.

3.2.2 Low pass filters

Other receiver architectures suitable for software defined radio implementations are low-IF, direct conversion and multi port receivers. For these structures the preparation of the signal for sampling is done in the base band. This means that these architectures employ low pass filters for anti aliasing a interferer attenuation. The main advantage of low-pass filters compared to their band pass counterparts is the much lower operating frequency requirement and the simple structure. Simple structure allows an easier programming of the bandwidth. Furthermore the tuning circuitry, used to compensate process tolerances and the effects of temperature, do not need to be very sophisticated as in the case of band pass filters. In most of the cases the

tuning is reduced to measuring a time constant and applying a correction to the circuit. Another advantage is the possibility of implementation in a fully integrated form [17][18].

One of the most important directions toward low pass filter design adopted by authors is based on opamp RC techniques [23]. The programming of the bandwidth is achieved by using more or less classical methods. Some of these implementations suggest switching capacitors when the noise is not of concern and switching resistors when noise should be minimized [5]. Most of the structures presented in the literature are implemented with programmable corner frequency over a small range and with limited precision [11][23][62]. These methods are rather suitable for classical auto tuning than for wide band programmability required by the software defined radio concept.

An interesting approach to wide band corner frequency programmability is presented in [55]. The schematic of the second order filter section proposed in this paper is based on opamp-RC structures and is given in Figure 3.7. The "-" sign of the resistance R_3 means an additional inversion of the signal. This sign can be readily eliminated in fully differential implementations.

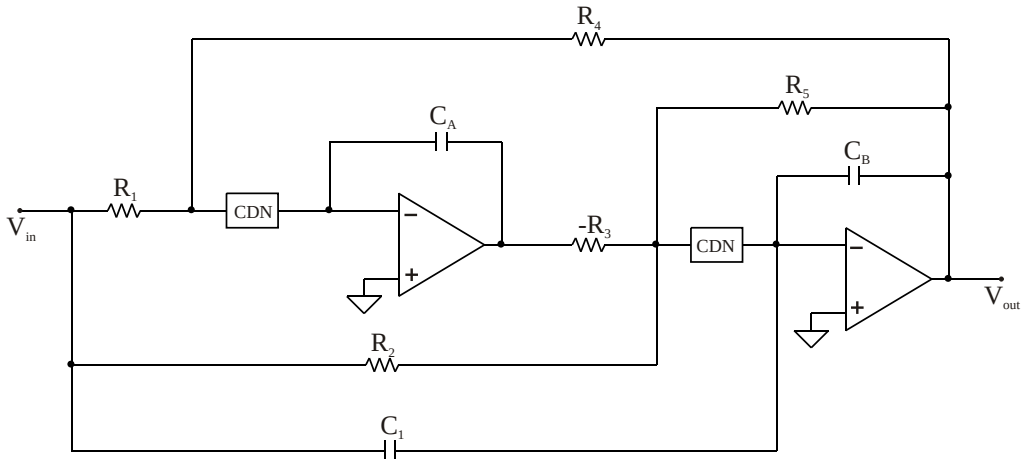


Figure 3.7: A second order low pass section programmable through a current division network

The programming principle is based on virtually scaling the capacitors. The scaling is implemented by dividing the currents that flow trough each individual capacitance with a current division network (CDN). The CDN is a switch array realized with MOS transistors biased in the triode region. The array is binary weighted, similarly as in R-2R networks used in digital to analog converters. The complete schematic of a CDN is given in Figure 3.8 [9].

The main advantage of this filter structure is its flexibility. The precision of the programming can be extended by increasing the number of switches in the CDN.

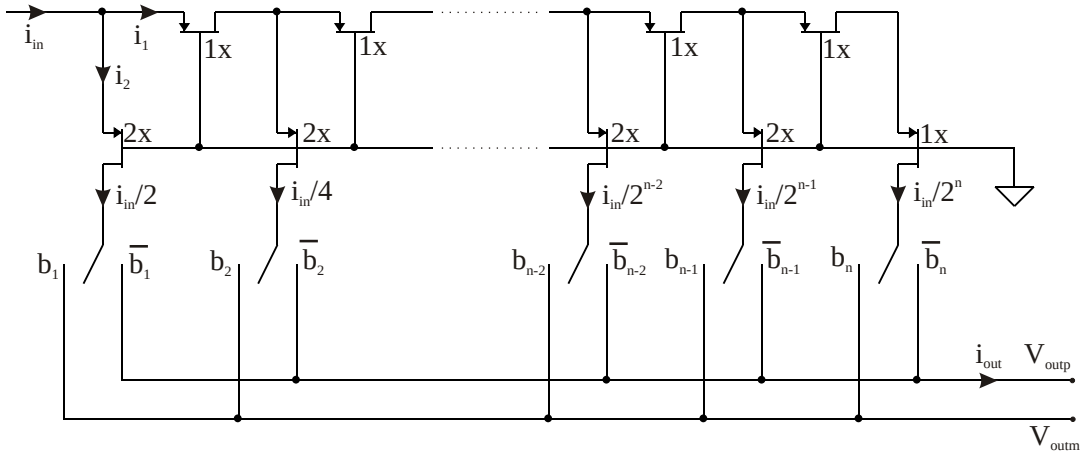


Figure 3.8: The schematic of the CDN

The main drawback of the implementation is that the correct functionality of the circuit is highly dependent on the loading effects created by the non-zero output resistance of the opamp and on the resistance of the division network. The loading effect means that the virtual ground will be shifted to the inputs of the opamps. Therefore, the voltage at the input of the division network can be determined from the balance of the currents in this node, according to Kirchhoff's theorem. This leads to the necessity of scaling the resistors in order to reduce ripples in the passband and unpredictable gain variations. A detailed explanation of the loading effect and the scaling of the resistors in the biquad have been presented in [55]. The scaling equations of the resistors connected to the first and the second CDN are given as follows:

$$\begin{cases} R_{i1} = R_{ni1}\left(1 - \dfrac{R_{CDN}}{R_{n1} \,||\, R_{n4}}\right) \\ R_{i2} = R_{ni2}\left(1 - \dfrac{R_{CDN}}{R_{n2} \,||\, R_{n3} \,||\, R_{n5}}\right) \end{cases}, \tag{3.5}$$

where R_i the scaled resistances, R_n are the unscaled values and R_{CDN} is the equivalent resistance of the division network.

Although for a fixed corner frequency the resistors can be scaled in order to reduce the loading effect, for programmable implementations the biquad quality factor varies along with the resonant frequency causing ripples in the pass band and the loss of approximation. It is of importance that the voltages at the output lines of the division network must be equal in order to insure a correct functionality and a constant equivalent resistance. Additionally, for a precise division of the currents, the geometry of the differential switches must be scaled with the current flowing through them. This procedure insures a constant voltage drop on the switches and balances the entire structure. Transistor level simulations have shown that the

division ratio of the currents and the equivalent resistance is extremely sensitive to the variations of the voltage difference between the output lines. Figure 3.9 shows the simulated equivalent resistance of the network against the voltage difference between the output lines. The simulations have been performed for a 4 bit current division network with a 1.5V common mode voltage for two different programming codes. Figure 3.10 presents the currents divided in the first node of the network.

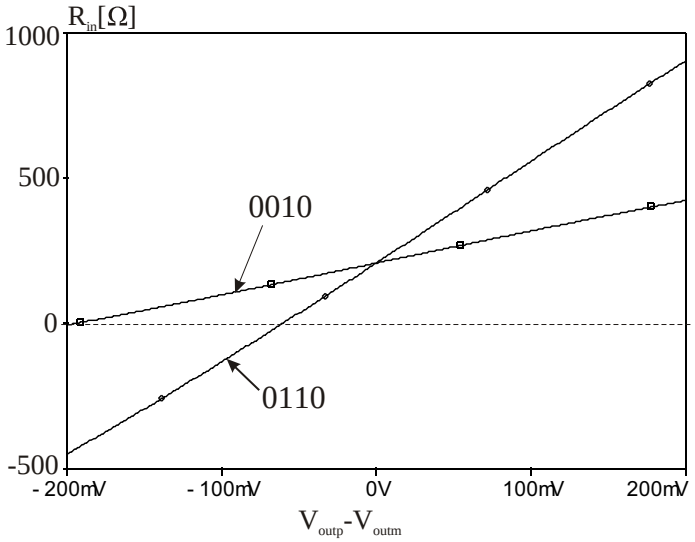


Figure 3.9: The equivalent resistance of the CDN against the voltage difference between its output lines for two different code settings

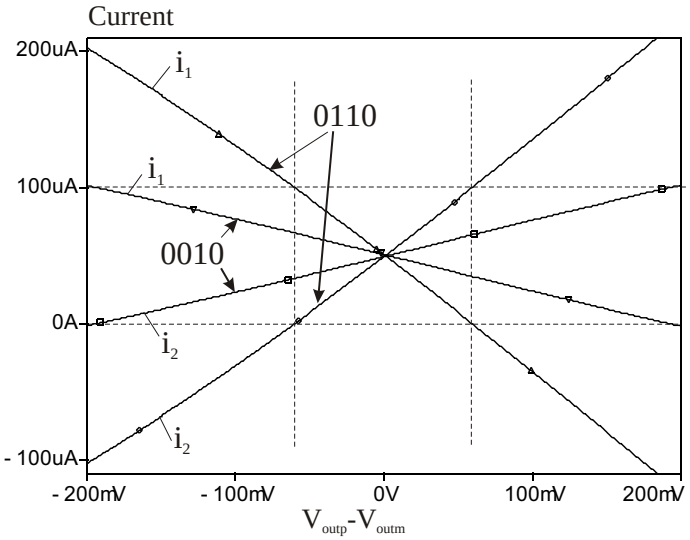


Figure 3.10: The currents divided in the input node of the network

From the Figure 3.9 it can be observed that a -60mV voltage difference causes the equivalent resistance of the network to become zero for the 0110 programming

code, while for 0010 the resistance is approximately 150Ω. The -60mV difference can easily appear between two lines in the circuit due to component mismatch and offset. For a voltage difference larger than -60mV the equivalent resistance of the network becomes negative and the currents through the transversal transistors are inverted. This can be followed on the simulation from the Figure 3.10 where the current i_2 turns negative at -60mV. From the point of view of the capacitance in the integrator this means that the current through it is rather extracted than injected. Obviously, the current inversion through the capacitance causes the circuit to behave as an inverting integrator for some codes and a non-inverting integrator for others. The consequence of this behavior is a change in the sign of the coefficients of s in the transfer function of the circuit. This introduces ripples, sometimes severe gain errors in the passband and group delay inconsistencies.

Another interesting programmable low-pass filter structure is presented in [5]. Similarly to the previously mentioned implementation, the corner frequency of the filter proposed in this paper is adjusted by means of a programmable current follower. The current follower is implemented with a current division network and a current buffer. In addition to the CDN, the filter also employs R-2R ladders in order to further increase the programming range and to allow the implementation of filters with large time constants. The unit elements of the filter are the programmable integrators. The schematics of the ideal and the lossy programmable integrator are shown in Figure 3.11.

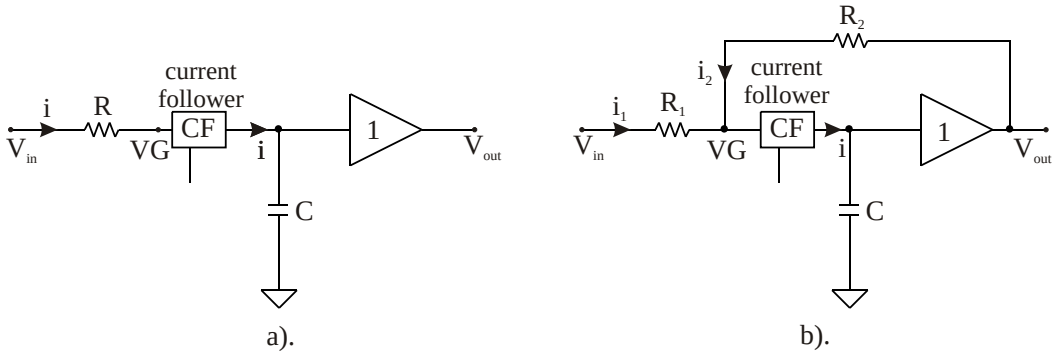


Figure 3.11: A programmable integrator a) ideal and b) lossy

When the capacitor is charged by the current αi, its charging time is α times shorter compared to the case when the charging occurs with the current i. If the scaling factor α is smaller than unity, the charging time will be eventually longer and the capacitance will seem to be larger than it is in reality. This phenomenon explains the virtual scaling of the capacitance in the integrator. The integrators operate correctly only if the current follower keeps its input at the virtual ground. If the input resistance of the unity gain buffer is infinitely large, the transfer functions corresponding to the ideal and the lossy integrators result as follows:

$$\begin{cases} H_{ideal}(s) = \dfrac{\alpha}{sRC} \\ H_{lossy}(s) = \dfrac{R_2}{R_1} \cdot \dfrac{1}{1 + sR_2\dfrac{C}{\alpha}} \end{cases} \tag{3.6}$$

The complete schematic of a second order filter section is given in Figure 3.12.

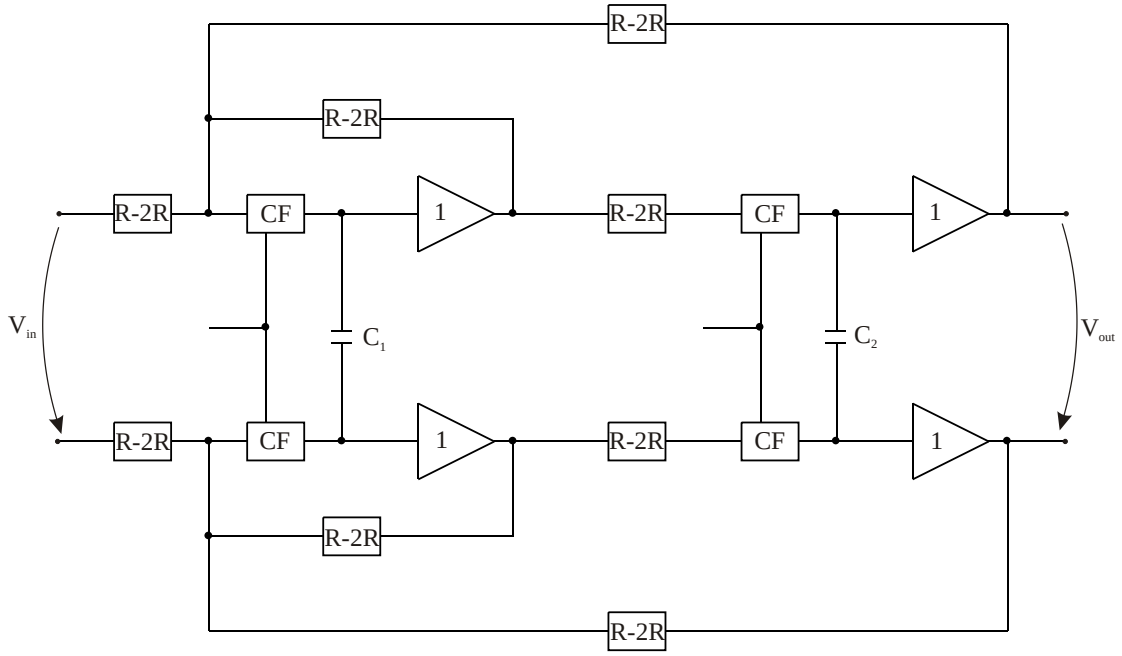


Figure 3.12: The second order filter section implemented with programmable current followers and R-2R ladders

The resistors must be chosen large or must be scaled in order to reduce the effects of the current follower internal resistance. Furthermore, the output resistance of the voltage buffers must be sufficiently small in order to avoid the aforementioned loading effect. The main drawback of the implementation is the sensitivity of the current division network with the small voltage changes across it two output lines. This voltage drop changes the division ratios of the currents and leads to a variation of the CDN equivalent resistance with the code. In spite of the drawbacks, the main and most important advantages of the circuit are the high frequency resolution, the economical way of implementing large resistors with the R-2R networks and a very good linearity.

Other programmable low pass filter implementations from the literature are based on operational transconductance amplifiers (OTA-s). Most of these use the

variable transconductance parameter for an adjustment of the corner frequency [65][76].

The approach presented in [65] uses programmable transconductance cells and additionally a binary weighted capacitor array for an extended coverage of the programming range. The range covered by the circuit from this paper is between 200kHz and 2.5MHz, intended to accommodate several standards. The programming steps are large and the resolution of the programming is relatively low. The programmable integrator used to implement the OTA-C filter is shown in Figure 3.13.

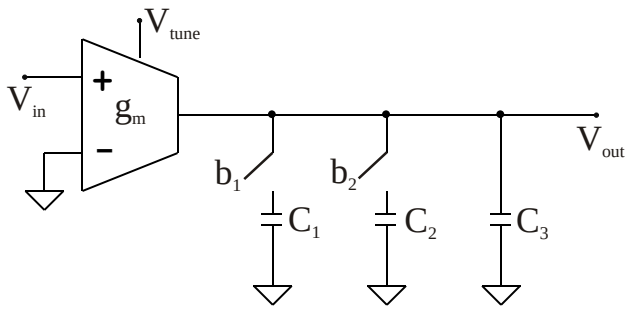


Figure 3.13: The principle of the low pass filter implementation proposed in [65]

The main drawback of OTA-C low pass filters in general is that they trade off high linearity with increased noise and consumption. Due to the increased noise floor and limited linear range these filters cannot achieve a high dynamic range [5]. Another important issue with OTA-C filters is the shift of the parameters with process corners and temperature. Transconductance amplifiers operating in open loop configurations are notoriously sensitive to process and temperature. Their transconductance parameter can vary as much as 50% compared to the ideal value. The multitude of factors [26] contributing to the variations of the transconductance parameter makes a wide band tuning difficult.

As a conclusion to this paragraph, the literature offers several approaches to filter design with wide band programmability. Some of the architectures supports only classical auto tuning, others have the potential to accommodate to the requirements of the software defined radio concept when the required trade-offs are admitted. In the most important filter examples, where the corner frequency is adjusted by virtual scaling, the designer must find the compromise between consumption, noise, precision, pass band ripples, gain variations and the change of the group delay. However the variations cannot be totally eliminated due to non-zero resistances of the building blocks and the inherent voltage offset.

3.3 The problematic of automated gain control in multi-mode receivers

Filtering in wireless receivers addresses the problems connected to large interfering signals outside the wanted channel and their effects on the performance. Automated gain control procedures address the problems regarding the variation of the wanted signal strength.

The need for sensitivity and a good control over the received signal strength is a fundamental issue in the design of any communication system. In the early days of radio circuits variable fading imposed the necessity to continuously adjust the gain of the receiver in order to maintain a relatively constant output signal. Such situations led to the idea of designing circuits whose function was to maintain a constant signal level at the output, regardless of the input signal strength variations. These circuits were generalized under the name automated gain control (AGC) [43].

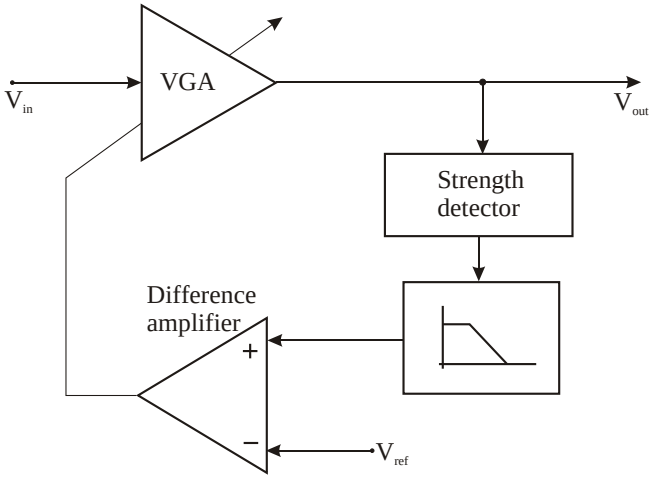


Figure 3.14: Principles of operation for an AGC loop

The principles of operation for an automated gain control loop are presented in Figure 3.14. In the diagram it is assumed that the VGA gain decreases with the detected error voltage. The received signal is amplified by means of a variable gain amplifier (VGA). The strength of the wanted signal is measured by a special circuit often called peak detector or received signal strength indicator (RSSI) at the output of the loop. The measurement result is then low pass filtered and compared with a given reference by a difference amplifier. The error is amplified and fed back as a correction signal that adjusts the gain of the VGA. If the signal strength is too large the VGA is adjusted to reduce its gain. Similarly, if the signal strength is too low the negative feedback loop will increase the gain of the VGA. Essentially the circuit works as a magnitude locked loop with the reference voltage V_{ref}.

In modern receiver architectures there can be multiple AGC loops along the signal chain. The detection of the signal strength and the comparison with a reference level can be done either by specialized analog circuitry, or by a DSP algorithm that evaluates the signal power after sampling. Regardless of the level detection and comparison method the execution element of the loop is always the VGA.

The VGA must have similar performances as the low-pass filter in what is concerning the linearity and intermodulation behavior. The dynamic range of the gain control is the extent to which the gain can be modified. Typical values for this parameter are in the range between 50dB and 100dB. The main reason for high dynamic range is the need for low noise figure and low 3^{rd} order intermodulation distortion [69].

An important factor that determines the quality of the VGA is its settling time. Settling time gains more and more importance due to the requirements imposed on the receiver to be able to receive and decode data as soon as possible, after receiving only a small number of bits [20]. The settling time of the VGA is highly dependent on its bandwidth. As a consequence, the bandwidth of the amplifier should be kept as constant as possible over the entire range of the gain. Due to constant unity gain bandwidth of voltage amplifiers the compromise between the gain and bandwidth can be difficult, especially when the dynamic range of the gain is very large. This is the reason why high dynamic range VGA-s are almost invariably constructed as a cascade of subsequent stages. The smaller gain range of each section will make the gain-bandwidth trade-off much easier [49]. The stages are usually connected in the cascade in a way that minimizes noise and non-linearity. According to this principle the higher gain stages are connected early in the signal chain.

Another important feature of practical VGA-s is that the gain should increase exponentially with the controlling signal or the digital gain selection word [43]. The exponential variation is transformed in a linear increase on a logarithmic scale. Furthermore, the increase should be monotonic in order to maintain the correct functionality of the AGC loop that the VGA is used for. This characteristic causes the specifications for the gain step error to be smaller than a fixed fraction of the gain step. Typical values for the gain step are 1dB or 2dB when a digital selection word is used, depending on the imposed precision. The monotonicity of the VGA gain variation leads to a uniform loop transient response and a good loop convergence regardless of the input signal level [69].

3.4 State of the art in VGA design

Several VGA implementations can be found in the literature. Some of these are very simple circuits, intended for radio frequency applications. These amplifiers are built mainly around single transistor gain stages or cascode configurations [43].

Another approach to VGA design employs Gilbert cells, where one of the input voltages is the predistorted wanted signal and the other is a constant voltage. The constant voltage modulates the gain of the circuit. The main advantage of the structure is its very high achievable bandwidth. A Gilbert cell VGA with 10GHz gain bandwidth product is available from Intersil corporation. It is of importance that the Gilbert cell exhibits continuous control over the gain. The typical schematic of a Gilbert cell is presented in Figure 3.15 [24].

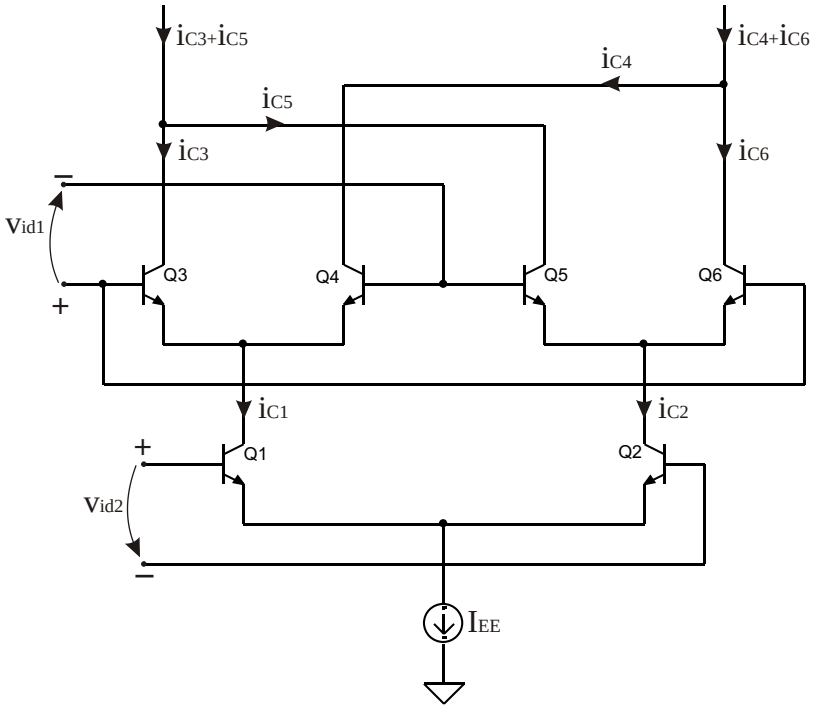


Figure 3.15: Schematic of bipolar Gilbert cell

For $v_{id1} = v_{id}$ and $v_{id2} = V_{tune}$ the operation of the circuit is described by the following equation:

$$\Delta i = i_{C3} + i_{C5} - i_{C4} - i_{C6} = I_{EE} \tanh\left(\frac{V_{tune}}{2V_T}\right) \cdot \tanh\left(\frac{v_{id}}{2V_T}\right) \tag{3.7}$$

If v_{id} is much smaller than the thermal voltage V_T, the Taylor series expansion of the current can be truncated after the first order terms and it results:

$$\Delta i = \frac{I_{EE}}{2V_T} \tanh\left(\frac{V_{tune}}{2V_T}\right) \cdot v_{id} = k(V_{tune}) \cdot v_{id} \tag{3.8}$$

It can be seen that the gain of the circuit can be easily changed by modifying the tuning voltage V_{tune}. However, the circuit is linear only for very low values of

the input voltage. Typically, even with additional linearity enhancements such as resistor degenerations or negative feedback [30][24], the circuit can only achieve a medium linearity and is not suitable for processing large signals in the base band of a receiver. An additional limitation is placed by the permitted signal swing at low supply voltages.

In modern receivers the VGA is usually placed in front of the ADC in order to maximize the dynamic range of the converter. In these systems the hardware overhead can be reduced by including the detection and comparison part of the AGC loop in the digital signal processor. In this case the baseband circuit controls the gain of the VGA in a discrete manner with a digital programming word.

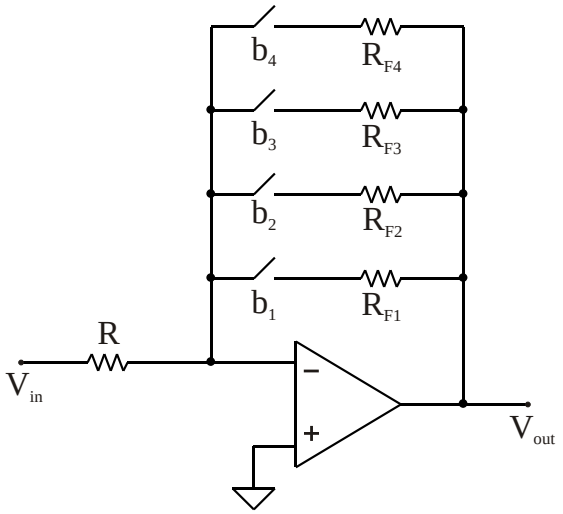


Figure 3.16: Principles of the gain variation by switching the feedback resistors in an opamp based VGA

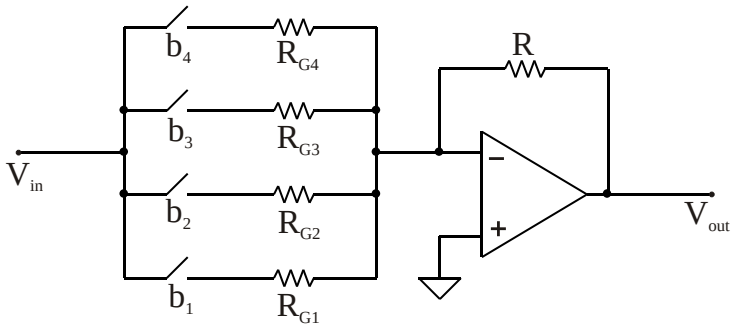


Figure 3.17: Principles of the gain variation by switching the input resistors in an opamp based VGA

For low frequencies, when the VGA must process base band signals the ampli-

fiers are built around operational amplifiers with variable resistive feedback. Such an approach has been presented in [68]. The gain of the circuit is varied by switching the feedback resistor. The principle of gain variation is presented in Figure 3.16. The gain of the amplifier is given by the following equations:

$$G = \frac{R_{Fequiv}}{R} = \frac{1}{R \cdot \sum_i \frac{b_i}{R_{Fi}}} \tag{3.9}$$

Alternatively the gain can be varied by switching the input resistors as suggested in Figure 3.17 [20]. In this case the gain becomes:

$$G = \frac{R}{R_{Gequiv}} = R \cdot \sum_i \frac{b_i}{R_{Gi}} \tag{3.10}$$

In both architectures the gain error due to mismatches and variations of the switch parameters with temperature can lead to the loss of monotonicity and significant gain errors. However the main advantages of the amplifiers are the good linearity and the capability to handle large signals.

Another approach is presented in [79]. In the circuit proposed in this paper a fixed gain amplifier is preceded by a variable attenuator as shown in Figure 3.18.

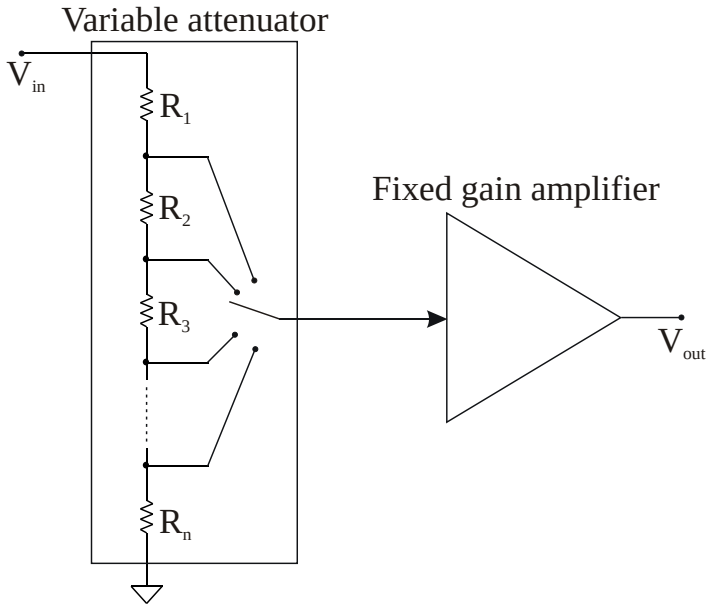


Figure 3.18: The structure of the VGA with a programmable attenuator and a fixed gain amplifier

The input signal is first attenuated and then amplified. The total gain of the

amplifier is the product between the attenuation of the input network and the fixed gain of the output amplifier. The main drawback of this approach is that the noise of the attenuation network is directly gained along with the wanted signal. Furthermore, the output resistance of the attenuator must be sufficiently small in order to maintain the gain of the amplifier constant. This issue leads to the necessity to separate the attenuation network from the amplifier through a buffer. The advantage of the circuit is that it maintains linearity by first reducing the input signal amplitude. This way the possible clipping is avoided. A direct consequence of this characteristic is the large signal handling capability.

If the magnitude of the input signal is known to be small (this is mostly the case in receivers where the VGA is placed to the input of the analog base band strip) the place of the amplifier and the attenuator can be switched in order to improve noise performance. The main drawback of the structure is then the possible saturation of the amplifier when unexpected large signals are processed. This could cause distortion by clipping. The maximum input signal level tolerated by the VGA depends on the fixed gain of the input amplifier.

3.5 Problem formulation

In the previous paragraphs it has been shown that the two main performance factors in wireless receivers are the sensitivity and the selectivity.

The selectivity of the system is the capability of the circuitry to attenuate certain components from the received signal spectrum and to pass others unaltered or amplified. The selectivity is highly dependent on the quality of the provided analog filtering and on the possibility to emphasize the wanted signal. Furthermore, in software defined radio receivers the analog front end must accommodate with several standards while maintaining its good selective behavior. This is possible only through implementing a filter transfer function with programmable frequency parameters. As a result, there is a necessity to design analog filters with variable bandwidth, either low pass or band pass, depending on the chosen architecture. The literature shows several more or less usable contributions in the area of low pass filter design, but there is a lack of band pass filters.

The sensitivity of a receiver depends on the ability to gain the wanted signal even when the reception is very weak, while adding as few noise and distortion as possible. The signal must be gained with a variable gain amplifier. This circuit is normally the execution element of an automated gain control loop.

The first part of this dissertation describes a base band circuit that is suitable for direct conversion or multi-port software defined radio. The designed circuit contains a low pass filter, that exhibits a bandwidth programmable in a wide range, and a variable gain amplifier. The detailed specifications are given in the following chapter. Additionally, the base band circuit must be considered also with some

system aspects concerning a correct biasing, the digital programming interface and a complete frequency error system. The final result of the research is a test chip fabricated in a 0.35μm BiCMOS process.

The second part of the work can be seen as a detailed feasibility study on band pass filter architectures that are intended as alternatives to passive or SAW filters nowadays used for intermediate frequency filtering in super heterodyne or IF sampling receivers. In this section different classical and new implementation techniques are investigated with emphasis on their flexibility and performance limitations. Finally there are some proposals for circuits that could improve the feasibility of high frequency and high Q band pass filters. The conclusions of this part should clearly show the problems that appear in the design process.

Chapter 4

Base Band Circuit for Multi Mode Receivers

4.1 Introduction

It has been shown in the previous paragraphs that the architectures most suitable for software defined radio implementations are the ones that are using a single down conversion and no off-chip intermediate frequency filtering. These architectures employ sampling in the base band or at the intermediate frequency. In the direct conversion architecture the channel selection and anti-aliasing is performed by low pass filters. Additionally, the wanted signal is gained in order to obtain a reasonable level before sampling and to reduce the dynamic range requirements of the ADC.

This chapter describes a fully programmable base band circuit intended for software defined radio circuits. The proposed block includes a programmable low pass filter and a variable gain amplifier that offers support for a digital AGC loop through its digital gain selection methods. The presentation of the low pass filter respects the main steps in filter design as shown in Figure 4.1.

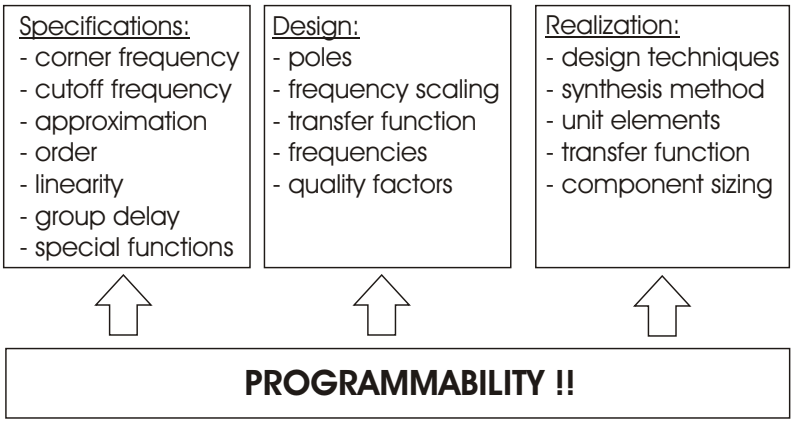


Figure 4.1: The main steps in filter design

The presentation starts with a set of specifications that are defined based upon the emerging problems, described in chapter 3. The following step will be the mathematical description of the filter according to the given specifications. At this stage a first idea will be given on the choice of the filter structure. The following and last step is the implementation of the filter at circuit level. This part contains the detailed description of the required circuitry, together with the optimization techniques used during the design procedure. All of the three distinct steps are dominated by the ultimate goal of this research, namely the implementation of a fully programmable filter, whose corner frequency can be changed in a wide range. Furthermore, the described filter allows the selection of many frequencies within a given range, offering support for actual and emerging communication standards. The main difficulty of this subject lays in the fact that only the characteristics of presently available standards are known. This is the reason why the proposed circuits have been developed based on assumptions and tendencies encountered in actual wireless communication systems.

4.2 Design specifications

The first step in the design process is the clear definition of the specifications. Some of these, such as the variation range of the corner frequency and the group delay, are derived from peculiarities of the supported and possibly emerging standards. Other requirements are based on worst case scenarios where it is assumed that, if the circuit fulfills the conditions for a very restrictive standard, then it also corresponds for processing other signals that introduce less stringent specifications. Typical parameters defined using a worst case scenario are the attenuation at the cutoff frequency and the filter order. The communication standard almost always used in worst case specifications is GSM. The reason for using the GSM standard as bases is that usually this standard has very severe requirements in what is concerning sensitivity and selectivity [56][57][80].

The specifications presented here can be divided in three categories. The first category includes the requirements concerning the selectivity of the filter. The second category is the description of the gain requirements for the other building block in the proposed base band circuit, the VGA. The third group of specifications are general and are concerning the circuit as a whole. Some examples in this sense are the current consumption, the generated noise and the supply voltage.

4.2.1 Specifications for the low pass filter

The magnitude response of the channel select filter should have a variable bandwidth and a roll-off that allows sufficient attenuation in order to achieve the selectivity required by any supported communication standard. The frequency specifications of the filter are derived based on the assumption that a filter designed for GSM usually complies with the attenuation requirements imposed by other existing standards [57]. The reason for this is that GSM requires large attenuations at frequencies

only some hundreds of kHz away from the -3dB corner frequency of the filter. As a consequence, the steepness factor, defined later, is possibly the highest for this standard.

The aim in setting the filter specifications is to attenuate the in band blockers and, if possible, equalize their magnitude with the magnitude of the wanted signal. This specification becomes of great importance as the functionality of the AGC loop usually includes verifying the magnitude of the wanted signal and not of the interfering signal [43]. The worst case attenuation of the filter should allow a maximum resolution of the ADC of around 10 bits effective, translated in approximately 60dB dynamic range for a Nyquist rate converter. The most important specifications of the low pass filter are as follows:

- **The -3dB corner frequency**

The minimum value of the -3dB corner frequency is set to 200kHz by the standard with the smallest channel bandwidth specifications, namely GSM. The upper limit of the corner frequency should allow the support for various UTRA standards whose channel bandwidth is around 4MHz and, additionally, some space for future standards [54]. Considering these requirements the -3dB corner frequency should be programmable in the range between 200kHz and 6.4MHz. The upper limit of the programming range has been chosen from tuning requirements. Since the simulated percent variation of the corner frequency with temperature and process corners can be as high as $\pm 55\%$ and the maximum achievable corner frequency is taken at around 10MHz, the upper frequency limit, that can be safely achieved in a worst case scenario, is around 6.45MHz. The 6.4MHz value of the highest frequency setting has been chosen in order to respect an octave switching template, later discussed in the filter realization. The software radio concept imposes a continuous adjustment of the corner frequency. In reality a continuous adjustment is difficult to be implemented and it is exposed to the errors and mismatch in the additional circuitry [53]. Due to this fact the compromise is to implement a quasi-continuous corner frequency selection that allows a digital programmability of the corner frequency but in very small steps. In most of the cases the code-frequency correspondence is linear on a logarithmic scale, which allows a better distribution of the achievable values over the programming range and eliminates large distances in frequency between two adjacent settings.

- **The approximation**

The choice of the approximation used in the filter design is done based on multiple criteria. The first and one of the most important decisions is concerning the flexibility of the filter. The programming should be simple, effective and should maintain the approximation for all the possible corner frequency settings. Standard approximations are much easier to control, compared to optimized frequency responses, as they have a well known, relatively simple transfer function that offers a predictable behavior and sensitivity [62][72]. The second important criterion is

concerning the group delay. The group delay variation should be kept as low as possible as to avoid the need for additional equalization circuits before demodulation. The choice of the phase variation implies a trade-off between the required attenuation, ripples in the pass band and the maximum allowed group delay variation. In spite of the flat magnitude response and low group delay the filter should exhibit a relatively steep roll-off. Since transmission zeros are not desired, the most important considered approximations are Butterworth, Bessel and Chebyshev. The compromise between these approximations is illustrated in Figure 4.2 [72]. The most balanced specifications, suitable to meet the aforementioned requirements, belong to the Butterworth response. This offers a maximally flat magnitude response in the pass band, a sufficiently steep roll-off and an average group delay variation.

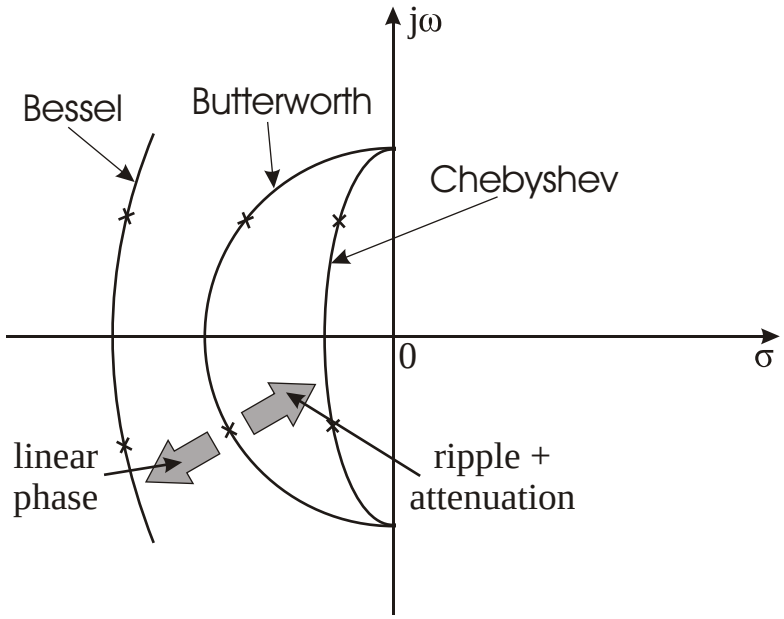


Figure 4.2: The compromise between ripple, attenuation and linear phase for the Butterworth, Chebyshev and Bessel approximations

- **Attenuation**

The attenuation requirements can be derived directly from the received GSM spectrum in Figure 3.2. As stated before, the aim is to equalize the magnitude of the wanted signal with the magnitude of the blocking signals in the adjacent frequency channels. The magnitude of the wanted signal is considered as reference. From the typical received spectrum corresponding to the GSM standard it can be observed that the magnitude of the blocking signal in the nearest interfering channel, centered at 600kHz distance from the center frequency, is 56dB larger. In order to perform the equalization of the magnitudes the filter must provide roughly 56dB attenuation at 600kHz distance from the center frequency of the wanted channel. Since the target receiver architecture is in most of the cases direct conversion, the relative distance 600kHz becomes an absolute value. This means that the required attenuation of the

filter will be at least 56dB at the 600kHz frequency. The general tolerance domain of the attenuation function $A(\Omega)$ is given in Figure 4.3 [72].

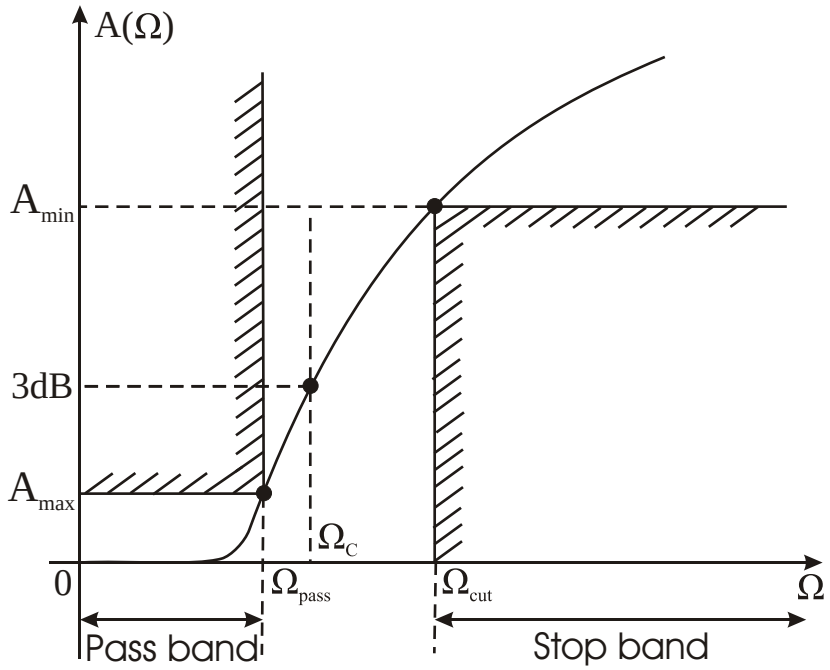


Figure 4.3: The tolerance domain of the attenuation function

In the figure Ω represents the normalized frequency with respect to the -3dB corner frequency of the filter. As a consequence, in this representation the corner frequency Ω_C, normalized to itself, is always equal to the unity. The frequencies Ω_{pass} and Ω_{cut} represent the limits of the pass band respectively the stop band. A_{max} and A_{min} are the attenuations corresponding to the frequencies Ω_{pass} and Ω_{cut}. In the following the tolerance domain will be used to compute the necessary filter order.

- **The filter order**

The order of the filter, that meets the given specifications, can be determined by starting from the expression of the attenuation and the filter transfer function. If the filter transfer function is considered to be $H(s)$, the attenuation can be written as a function of frequency. Its expression is given in the equation (4.1) [23].

$$A(\omega) = 20\lg\left(\frac{1}{|H(s)|}\right)|_{s=j\omega} = 20\lg\left(\frac{1}{|H(j\omega)|}\right) \tag{4.1}$$

The generalized magnitude response of an n^{th} order Butterworth filter is written as follows:

$$|H(s)|\,|_{s=j\omega} = |H(j\omega)| = \sqrt{\frac{1}{1+\omega^{2n}}} \tag{4.2}$$

After replacing the magnitude function in the equation (4.1) and rearranging the terms, the attenuation results:

$$A(\omega) = 10 \lg \left(1 + \omega^{2n}\right) \tag{4.3}$$

For more convenience and generality, in this expression the scaled frequency ω can be replaced by the normalized frequency Ω. The normalized attenuation is then:

$$A(\Omega) = 10 \lg \left(1 + \Omega^{2n}\right) \tag{4.4}$$

The next step in computing the required filter order is to connect the attenuation function with the critical values from the tolerance domain. The resulting system of equations is given in (4.5).

$$\begin{cases} A(\Omega_{cut}) = A_{max} = 10 \lg \left(1 + \Omega_{cut}^{2n}\right) \\ A(\Omega_{pass}) = A_{min} = 10 \lg \left(1 + \Omega_{pass}^{2n}\right) \end{cases} \tag{4.5}$$

From this system follows:

$$\begin{cases} \Omega_{cut}^{2n} = 10^{0.1 \cdot A_{max}} - 1 \\ \Omega_{pass}^{2n} = 10^{0.1 \cdot A_{min}} - 1 \end{cases} \tag{4.6}$$

By dividing the first equation with the second results:

$$\left(\frac{\Omega_{cut}}{\Omega_{pass}}\right)^{2n} = \frac{10^{0.1 \cdot A_{max}} - 1}{10^{0.1 \cdot A_{min}} - 1} \tag{4.7}$$

When computing the logarithm of the terms in the equation (4.7) we may write:

$$2n \cdot \lg \left(\frac{\Omega_{cut}}{\Omega_{pass}}\right) = \lg \left(\frac{10^{0.1 \cdot A_{max}} - 1}{10^{0.1 \cdot A_{min}} - 1}\right) \tag{4.8}$$

The final expression of the filter order can be written as follows:

$$n = \frac{\lg \left(\frac{10^{0.1 \cdot A_{max}} - 1}{10^{0.1 \cdot A_{min}} - 1}\right)}{2 \lg (SF)} \ , \tag{4.9}$$

where the steepness factor SF is defined:

$$SF = \frac{\Omega_{cut}}{\Omega_{pass}} \tag{4.10}$$

Once the filter order has been determined, the -3dB corner frequency of the filter can be calculated according to the following equation:

$$\Omega_C = \frac{\Omega_{pass}}{\sqrt[2n]{10^{0.1 \cdot A_{min}} - 1}} \tag{4.11}$$

If the attenuation A_{min} is taken exactly 3dB for simplicity, the -3dB corner frequency will be equal to Ω_{pass} and further equal to unity. In this case the expression of the filter order becomes:

$$n = \frac{\lg\left(10^{0.1 \cdot A_{max}} - 1\right)}{2 \lg\left(\Omega_{cut}\right)} \tag{4.12}$$

By replacing the numerical specifications $A_{max} = 56dB$ and $\Omega_{cut} = 3rad/s$ in this relation the filter order results equal or greater than 5.87. This value is rounded upwards to the nearest integer 6. The calculation can be verified on the family of attenuation curves corresponding to Butterworth filters of different order that are given in Figure 4.4 [72].

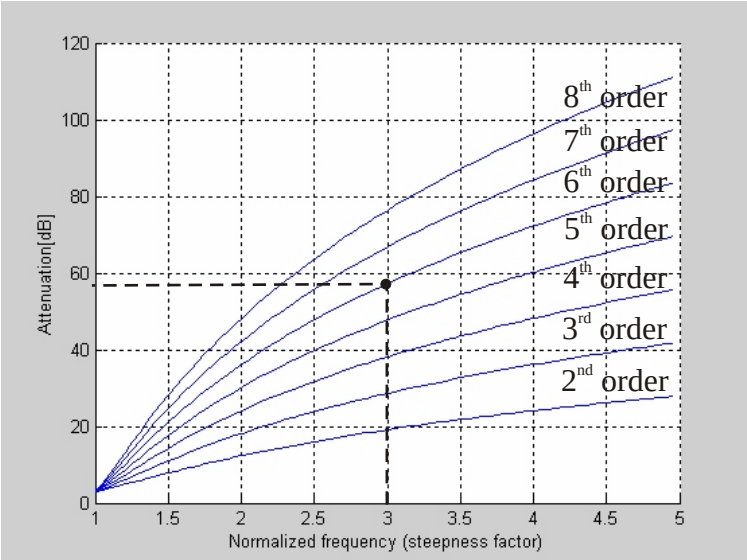


Figure 4.4: The family of attenuation characteristics for Butterworth filters with the order between 2 and 8

From the curves it can be seen that the 6^{th} order response offers approximately 58dB attenuation and satisfies the requirements.

- **Linearity**

Linearity is a very important specification due to the fact that non-linear behavior could lead to significant intermodulation distortion and implicitly to an irreversible corruption of the wanted signal. This mechanism and its effects on the wanted signal have been explained in the previous chapter. The total harmonic distortion is defined as follows [58]:

$$THD = 20 \cdot \lg \left(\frac{A_1}{\sqrt{\sum_{i=2}^{\infty} A_i^2}} \right) , \tag{4.13}$$

where A_i are the magnitudes of the i^{th} order harmonics and A_1 is the magnitude of the fundamental. It must be mentioned that the THD only characterizes the total harmonic distortion of a circuit. If the bandwidth of the circuit is limited and the higher order harmonics fall outside the pass band, the THD will be significantly improved in spite of the fact that the circuit can be highly non-linear. Therefore, a better way to describe the linearity of the circuit is through an intermodulation analysis [56]. For this the output signal is written as a function of the input signal as follows:

$$S_{out} = c_0 + c_1 S_{in} + c_2 S_{in}^2 + c_3 S_{in}^3 + \cdots , \tag{4.14}$$

where S_{out} is the output signal, S_{in} is the input signal and c_i are gain coefficients corresponding to different harmonics. For a relatively low level of distortion the components whose order is higher than 3 can be neglected. The intermodulation analysis assumes that the input signal can be written as a sum of two different sine waves, with the frequencies f_1 and f_2. For simplicity, the amplitude of both sine waves can be taken equal to A.

$$S_{in} = A \left(\cos \omega_1 t + \cos \omega_2 t \right) \tag{4.15}$$

By replacing the expression of the input signal in the equation (4.14) it can be demonstrated that the output signal is a sum of the following spectral components:

$$\begin{cases} \text{DC} : c_0 + c_2 A^2 \\ \text{Fundamental} : c_1 A + \dfrac{9}{4} c_3 A^3 \left(\cos \omega_1 t + \cos \omega_2 t\right) \\ 2^{nd} \text{ harmonic} : \dfrac{1}{2} c_2 A^2 \left(\cos 2\omega_1 t + \cos 2\omega_2 t\right) \\ 3^{rd} \text{ harmonic} : \dfrac{1}{4} c_3 A^3 \left(\cos 3\omega_1 t + \cos 3\omega_2 t\right) \\ 2^{nd} \text{ intermodulation} : c_2 A^2 \left[\cos\left(\omega_1 + \omega_2\right) t + \cos\left(\omega_1 - \omega_2\right) t\right] \\ 3^{rd} \text{ intermodulation} : \dfrac{3}{4} c_3 A^3 \left[\cos\left(2\omega_1 + \omega_2\right) t + \cos\left(2\omega_1 - \omega_2\right) t\right] + \\ \qquad\qquad + \dfrac{3}{4} c_3 A^3 \left[\cos\left(\omega_1 + 2\omega_2\right) t + \cos\left(2\omega_2 - \omega_1\right) t\right] \end{cases} \tag{4.16}$$

DC offset and second order distortion is always associated with the asymmetrical processing paths. In fully differential circuits these components should be theoretically reduced to zero. The third harmonics of the input signal are situated at high frequencies and are attenuated by the frequency response of the circuit. The most important spectral components in the list above are the third order intermodulation products. If $2f_1$ is sufficiently close to f_2, the resulting intermodulation product, whose frequency is equal to $2f_1 - f_2$, can be folded back in the band of the wanted signal although the absolute frequencies f_1 and f_2 are much larger than the circuit bandwidth. The intermodulation distortion is defined as the ratio between the amplitude of the folded third order intermodulation product and the ideal amplitude of the fundamental component or wanted signal.

$$IM_3 = \frac{3c_3}{4c_1} \cdot A^2 \tag{4.17}$$

In the case of radio receivers the blocking signals are not simple sine waves. The worst case intermodulation specification for different standards defines an adjacent channel as the most important blocking signal [57][80], whose center frequency is f_1. Note that this modulated signal occupies a bandwidth equal to the channel width of the wanted signal. In the worst case scenario this signal is modulated by a single carrier with the frequency equal to f_2. The modulation occurs due to nonlinearity and the adjacent channel is mixed down into the wanted channel. The maximum tolerated intermodulation introduced by the circuit can be defined according to the diagram in Figure 4.5.

From the diagram results that the intermodulation can be written:

$$IM_3 = A_{interf} - A_{2f1-f2} = A_{interf} - A_{wanted} + SIR \ , \tag{4.18}$$

where A_{interf} is the amplitude of the interfering signals that create the intermodulation effect, A_{wanted} is the amplitude of the wanted signal and SIR is the signal-to-interference ratio, all expressed in dB.

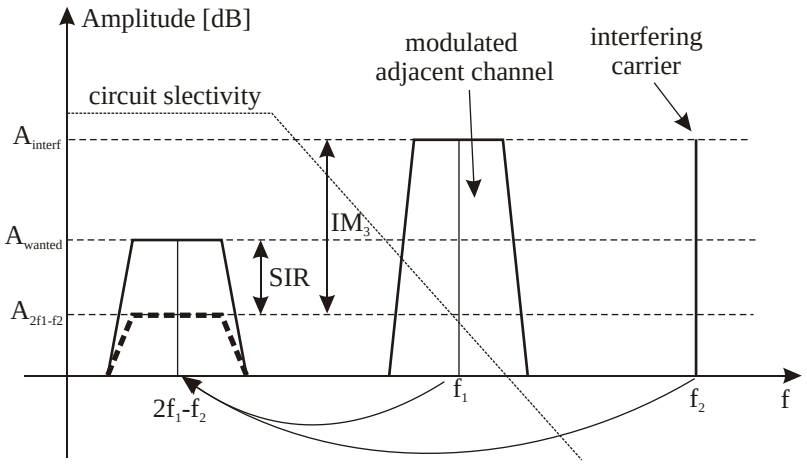


Figure 4.5: The relation between the wanted signal and the third order intermodulation product

The amplitude of the interfering signals is determined from the blocking specifications of a certain standard. The value or the SIR results from the required bit error rate (BER) of the receiver and the reference sensitivity corresponding to the considered standard. As an example, for GSM a BER equal to 10^{-3} requires a SIR equal to 12dB. The absolute values of the blocking signals and of the wanted signal are not of importance, since these are gained up together in the RF part of the receiver. What counts is the difference between these two signals. This means that the signal levels can be taken from the reference sensitivity specifications of the considered standard [57]. The intermodulation specifications for GSM specify a wanted signal at -99dBm and the interferers at -49dBm [46][80]. The maximum allowed intermodulation can be derived for the conditions when any circuit in the receiver has a reference signal level at its input and the SIR is held constant. This usually means that the third order intermodulation product is kept equal to or below the noise floor. The specified signal levels lead to the maximum allowed third order intermodulation introduced by the base-band circuit equal to -62dBm.

- **Power saving**

Consumption is an important factor that limits the applicability of circuits in wireless communications systems. In practice consumption is always traded for linearity and speed. Typically the circuits operating at lower frequencies require less current. The lower limit of the programming range for the corner frequency has a relatively low value. This allows a power saving functionality to be efficiently integrated in the filter structure. The power saving algorithm should switch the low-pass filter in a low power mode whenever the corner frequency setting is decreased

below a certain limit. Usually the limit depends on the filter architecture. The lower consumption can be achieved by reducing the current sunk by the active components of the circuit.

4.2.2 Specifications for the variable gain amplifier

Compared to the filter, the main role of the VGA is to gain the wanted signal, and usually the interfering signals as well, to a level where they can be conveniently sampled. The amplifier should work in a closed relationship with the channel select filter in order to provide the required dynamic range. The main specifications of the circuit are as follows:

- **The gain and the gain accuracy**

The variation range of the gain should bring the wanted signal in the tens of mV range even in the case of very weak received signal strength. Assuming that the gain of the RF front end is around 20dB, this requires around 80dB maximum gain. According to this the chosen variation range of the VGA is between 0dB and 79dB. The gain should be adjusted in 1dB steps with the gain error less than ±0.3dB. The low gain step error is needed in order to maintain the unconditional monotonicity of the gain function against the selection code.

- **Linearity**

The linearity requirements of the VGA are similar to the low-pass filter. Since the distortion introduced by the active elements in the circuit is decreased by the gain of the negative feedback loop, the feedback factor, and implicitly the gain of the amplifier stages in the VGA, should be limited to a reasonable value. From the feedback theory [24] it is well known that the linearity of an active amplifier connected in a feedback loop is

$$IM_3\,|_{closed-loop} = IM_3\,|_{open-loop} \cdot \frac{1}{1+Gf} \tag{4.19}$$

In this equation G is the gain of the amplifier on the direct path and f is the feedback factor. If G is sufficiently large, the gain of the closed loop circuit can be approximated with $1/f$. If the gain of the amplifier is expressed in dB, the feedback factor can be written:

$$f = 10^{-\frac{G}{20}} \tag{4.20}$$

For example, if the gain of a closed loop amplifier is 20dB, then the feedback factor is equal to 1/10. A 60dB gain of the amplifier on the direct signal paths yields an improvement of the IM_3 with approximately 40dB compared to the open loop behavior. Therefore, the gain of the individual amplifier stages in the VGA should not exceed the value of about 20 or the equivalent 26dB.

4.2.3 Additional specifications

There are some specifications that should be met by the base band circuit as a whole. These specifications are mainly referring to generated noise, consumption and supply voltages.

- **The generated noise**

The generated noise is of great importance since it influences the sensitivity of the receiver. At low frequencies the flicker noise becomes the dominant factor. The noise floor can be defined by using a similar analysis as for the linearity. When the amplitude of the wanted signal at the input of the base-band block is known, the signal to noise ratio should be above the reference value equal to 12dB [57]. If the amplitude specification is taken -82dBm from the interference specs of the GSM standard, it results that the worst case noise floor should lay at approximately -94dBm. This corresponds to $2mV_{rms}$ total integrated noise in the 0-200kHz signal band. Here GSM is considered again as it exhibits relatively severe sensitivity requirements.

- **Current consumption**

The specified current consumption for the entire base band circuit should not be larger than 10mA for the maximum corner frequency setting and the highest gain of the VGA. This specification is strictly related to prolonged battery life in modern mobile handsets.

- **The supply voltages**

The entire circuit should operate from a single 3V supply in order to comply with modern mobile receiver requirements. The common mode voltage of the circuit will be derived later from the maximum signal swing and biasing conditions.

4.3 The low pass filter

This paragraph presents the detailed design procedure of the low pass filter. The presentation starts with a complete description of the mathematical tools that are the bases of filter design. The result of this section is the transfer function of the filter that complies with the frequency requirements defined in the previous paragraphs. Additionally, the impacts of the full flexibility requirements on the filter mathematics will also be discussed in detail. The presentation continues with a short survey of design techniques and the actual realization step. A special emphasis lays on the programming strategies of the corner frequency and on the description of a wide band corner frequency error prediction circuit used to compensate the frequency errors introduced by process tolerances and temperature.

4.3.1 The second order low pass section

The main frequency specifications of the low pass filter with a significant effect on the mathematical description are summarized here for convenience:

- the corner frequency - variable between 200kHz and 6.4MHz;
- the filter approximation - Butterworth;
- the filter order - 6.

The first step in the mathematical description implies an important decision in what is concerning the synthesis method used for the design. Low pass filters can be relatively easily implemented by using classical synthesis methods such as cascading of second order sections, state variables or general impedance converters [36][23][62]. The choice is primarily influenced by the programmability requirements. For an increased flexibility the chosen filter must have a modular structure that allows the orthogonality between the corner frequency and the quality factors of the pole pairs. This requirement is introduced by the need to change the corner frequency while maintaining the quality factors and the approximation. State variable and general impedance converter methods are both based on implementing a network that emulates the functionality of a passive prototype. In these cases the entire transfer function is implemented at once, without an access to change individual pole locations or quality factors. Therefore, the most convenient way to implement low pass filters is to employ cascade of second order sections.

A second order filter section implements the transfer function corresponding to a complex conjugate pole pair. The pole pairs for different standard approximations and different filter orders can be found tabulated in design tables. The poles are of the form given in equation (4.21).

$$\begin{cases} s_{x1} = -\alpha + j\beta \\ s_{x2} = -\alpha - j\beta \end{cases} \tag{4.21}$$

The normalized second order transfer function, corresponding to the complex conjugate pole pair s_{x1} and s_{x2}, can be written as follows:

$$H_n(s) = \frac{1}{\left(1 - \frac{s}{s_{x1}}\right)\left(1 - \frac{s}{s_{x2}}\right)} = \frac{s_{x1}s_{x2}}{s^2 - (s_{x1} + s_{x2})\, s + s_{x1}s_{x2}} \tag{4.22}$$

The characterization of the frequency response with the poles is difficult to be used for design purposes. Another equivalent set of parameters includes the resonance frequency and the quality factor of the pole pair. The relation between

the poles, the resonance frequency and the quality factor is biunivocal. The transformation from one set to the other can be done according to simple geometrical calculations as presented in Figure 4.6. The position of the poles in the s plane is known to be a circle with a unity radius, as required by the Butterworth approximation. Here Ω_0 is the normalized resonant frequency equal to 1 rad/s.

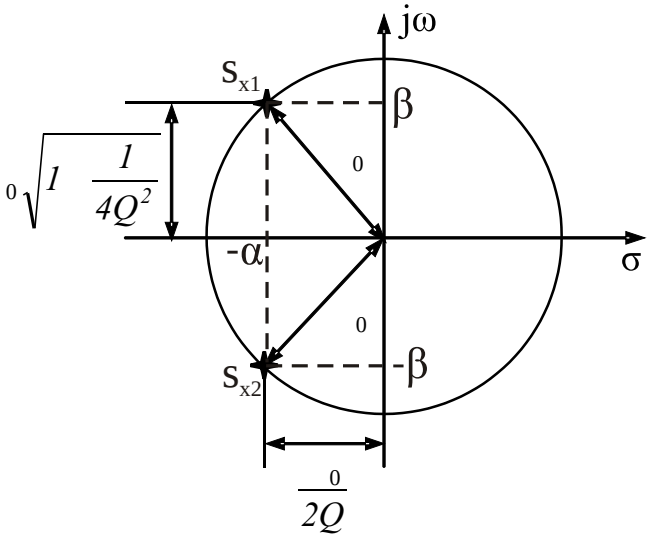


Figure 4.6: The position of the normalized poles in the s plane

The transformation from α and β to Ω_0 and Q can be performed according to the following equations:

$$\begin{cases} \Omega_0 = \sqrt{\alpha^2 + \beta^2} \\ Q = \dfrac{\sqrt{\alpha^2 + \beta^2}}{2\alpha} \end{cases} \tag{4.23}$$

The inverse transformation is given in the equations (4.24).

$$\begin{cases} \alpha = \dfrac{\Omega_0}{2Q} \\ \beta = \Omega_0 \sqrt{1 - \dfrac{1}{4Q^2}} \end{cases} \tag{4.24}$$

The normalized transfer function, written with Ω_0 and Q, is known as the standard form and is given in equation (4.25) [62]. Usually the standard form also includes a DC gain, noted here with H_0.

$$H_n(s) = H_0 \cdot \frac{\Omega_0^2}{s^2 + \frac{\Omega_0}{Q}s + \Omega_0^2} \tag{4.25}$$

It is of great importance that the poles found in design tables are normalized with respect to the desired corner frequency of the filter. Once the desired -3dB corner frequency and the reference frequency are known a frequency scaling factor F can be defined as follows [72]:

$$F = \frac{f_{Cdesired}}{f_{Creference}} = \frac{\omega_{Cdesired}}{\omega_{Creference}} \tag{4.26}$$

In many cases the reference frequency is equal to Ω_0. Since Ω_0 is equal to unity, the frequency scaled poles can be obtained by simply multiplying both the real and the imaginary parts with the frequency scaling factor.

$$\begin{cases} s_{x1}^{'} = F \cdot s_{x1} = -F\alpha + jF\beta \\ s_{x2}^{'} = F \cdot s_{x2} = -F\alpha - jF\beta \end{cases} \tag{4.27}$$

The scaled resonant frequency of the second order section and the quality factor can be written as follows:

$$\begin{cases} \omega_0 = F\sqrt{\alpha^2 + \beta^2} \\ Q = \dfrac{\sqrt{\alpha^2 + \beta^2}}{2\alpha} \end{cases} \tag{4.28}$$

It should be noticed that the quality factor does not depend on the frequency scaling factor. This means that the frequency scaled poles will exhibit the same quality factor. A general form of the squared resonant frequency can be written by using the axis variables σ and ω.

$$\omega_0^2 = \sigma^2 + \omega^2 \tag{4.29}$$

This expression can be easily recognized as the equation of a circle with the radius ω_0. As a consequence, the location of the frequency scaled poles will always be on concentric circles, whose radius is proportional with the frequency scaling factor. Furthermore, the frequency scaled poles are always collinear. This can be demonstrated by the mathematical proof method *reductio ad absurdum*. First the position of the poles in the s plane is assumed not to be collinear. This hypothesis

is illustrated in Figure 4.7 for the normalized poles and for two different frequency scaling factors F_1 and F_2.

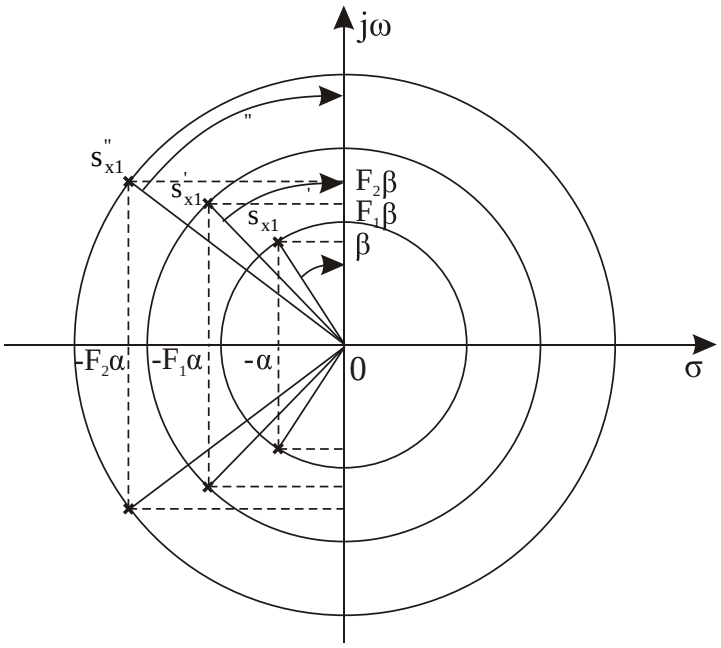


Figure 4.7: The frequency scaled poles assumed not to be collinear

The radius of each circle, connecting the poles with the origin, forms with the imaginary axis the angles φ, $\varphi^{'}$ and $\varphi^{''}$. When the poles are not collinear, then clearly φ, $\varphi^{'}$ and $\varphi^{''}$ are different. Each angle can be written as a function of the pole coordinates:

$$\begin{cases} \tan\varphi = \dfrac{\beta}{\alpha} \\ \tan\varphi^{'} = \dfrac{F_1\beta}{F_1\alpha} = \dfrac{\beta}{\alpha} \\ \tan\varphi^{''} = \dfrac{F_2\beta}{F_2\alpha} = \dfrac{\beta}{\alpha} \end{cases} \tag{4.30}$$

It results:

$$\tan\varphi = \tan\varphi^{'} = \tan\varphi^{''} \;\Rightarrow\; \varphi = \varphi^{'} = \varphi^{''} \tag{4.31}$$

This conclusion is in contradiction with the hypothesis and the collinearity is demonstrated. In this case the pole locations in the s plane for different frequency scaling factors can be redrawn as in Figure 4.8.

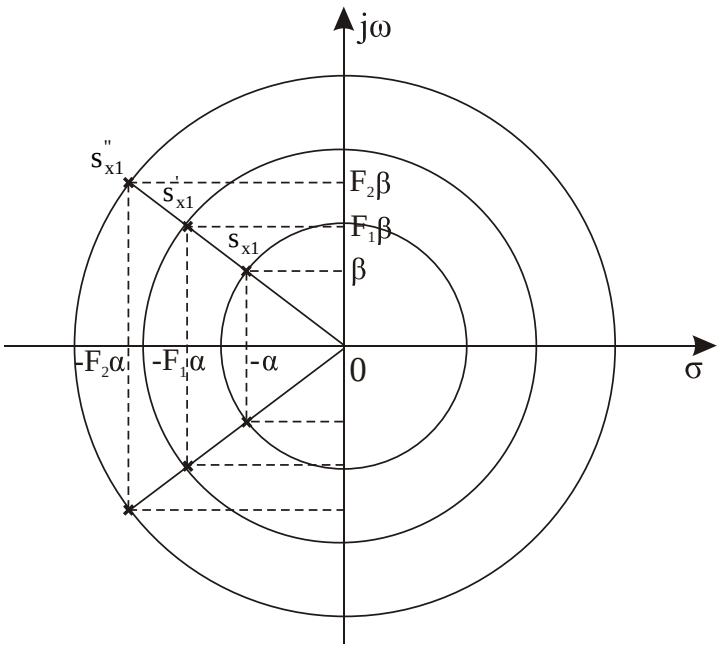


Figure 4.8: The correct representation of the pole locations after frequency scaling

The immediate consequence of the analysis is the fact that scaling the resonant frequency does not influence the pole quality factors and implicitly the filter approximation. If the corner frequency of the filter must be scaled while maintaining the approximation, this can be done simply by changing the frequency scaling factor and defining a new value for the resonant frequency. This is also the proof for the orthogonality requirement between the frequency and the quality factor of each individual second order section from a filter structure. The frequency scaled transfer function of the biquad is then written:

$$H(s) = H_0 \cdot \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{4.32}$$

The denormalized standard form is very important in filter design as it is the intermediate step in conversion of the tabulated poles in the component values of the circuit, that implements the filter with a desired approximation. The circuit transfer function almost invariably results in the standard form. The sizing equations can be directly inferred by identifying the coefficients of the terms in s in the theoretical response and the circuit transfer functions.

4.3.2 Low pass filter design techniques

Several filter design techniques have been developed for high performance low pass filter design. One of the most well known filter family is based on switched capacitor techniques. Although switched capacitor filters offer a very good precision they are

not suitable for channel selection in the analog front ends. The main reason for this is their time discrete nature. For a proper functionality in the analog domain switched capacitor filters require an anti-aliasing filter at their input and a smoothing filter at their output. Both of these additional circuits must be continuous in nature.

Another low pass filter implementation with good performance at low frequencies is based on operational amplifiers, resistors and capacitors. The main advantage of these circuits is the large signal handling capability and high dynamic range. Derivatives of opamp-RC filters can be very area and noise effective. A typical example is the opamp-MOS-C filter family, where the resistors are replaced by MOS transistors biased in the linear region. The main drawback of opamp-RC filter is their limited frequency range. With a quality operational amplifier the higher limit of the corner frequency is somewhere at 10MHz [30].

A third implementation method is based on transconductance amplifiers and capacitors. OTA-C filters are an alternative to opamp-RC structures that allow high frequency operation. The transconductance amplifiers are connected in open loop configurations; thus their natural bandwidth is not limited by feedback. The main problems arising in OTA-C filter design are concerning linearity and consumption. Since the linearity of these filters is limited by the transconductance cells, an additional effort must be put in extending the linear range. Together with the high frequency operation and the limited value of the transconductance the extended linearity often leads to a significant increase in consumption compared to other design techniques. A very important issue concerning OTA-C filters is that at low frequencies they become noisy [5]. Due to this fact the operation in the tens and hundreds of kHz frequency range should be avoided.

There are also other structures suitable for continuous time low-pass filter implementations in the literature [23][36][62][53]. These are mainly based on building blocks such as current conveyors, current feedback amplifiers or exponential-logarithmic converters. However, in practice opamp-RC, OTA-C and their derivatives are used in most of the cases. A careful analysis of the specifications imposed on the low pass filter shows that the most suitable filter architecture, with potential to meet these specifications, is the one based on opamp-RC structures.

One of the most often used second order sections is the Tow-Thomas biquad. The generalized block diagram of the second order section is presented in Figure 4.9. For this structure the following equations can be written:

$$\begin{cases} V_1 = V_{in} - V_{out} \\ V_{out} = V_1 \cdot \dfrac{1}{s\tau_2\,(1 + s\tau_1)} \end{cases} \tag{4.33}$$

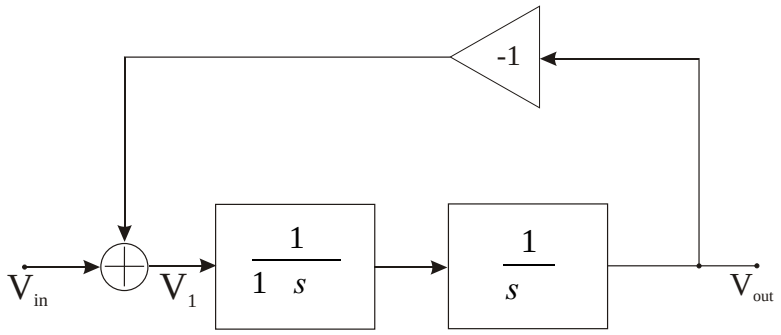


Figure 4.9: Block diagram of the Tow-Thomas biquad

The transfer function can be found by solving the system (4.33) for V_{out}. The low pass transfer function of interest is given as follows:

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{\dfrac{1}{\tau_1 \tau_2}}{s^2 + s\dfrac{1}{\tau_1} + \dfrac{1}{\tau_1 \tau_2}}, \tag{4.34}$$

where τ_1 and τ_2 are the time constants of the two integrators. The corresponding opamp-RC implementation of the Tow-Thomas second order filter section is presented in Figure 4.10.

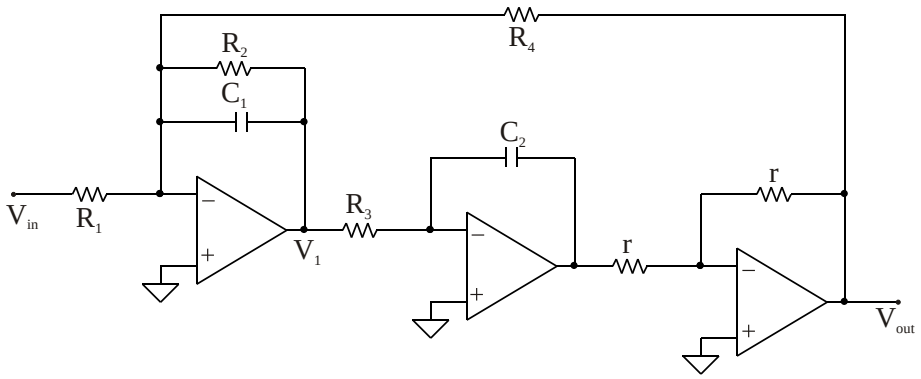


Figure 4.10: The opamp-RC Tow-Thomas biquad

The transfer function of the circuit is easily determined by using Millman's theorem. Millman's theorem is an easy way for calculating the voltage in a circuit node common to a set of impedances whose other terminals are connected to different voltages [4]. As an example let us consider the network from the following figure:

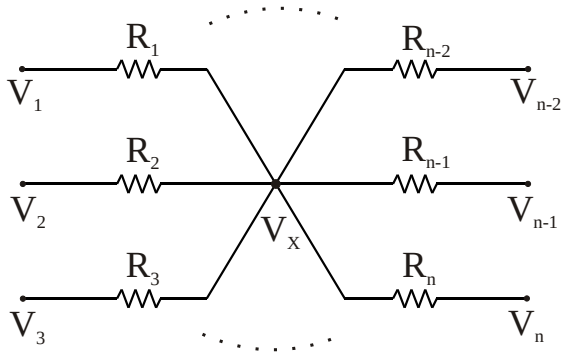


Figure 4.11: The impedance network suitable for using Millman's theorem

It can be demonstrated that the voltage V_X is given by the following equation:

$$V_X = \frac{\sum_{i=1}^{n} \frac{V_i}{R_i}}{\sum_{i=1}^{n} \frac{1}{R_i}} \tag{4.35}$$

If the opamps are considered ideal, the application of Millman's theorem at each of the inputs, that are not tied to the ground, leads to the following system of equations:

$$\begin{cases} \frac{V_{in}}{R_1} + \frac{V_{out}}{R_4} + V_1 \cdot \frac{1 + sR_2C_1}{R_2} = 0 \\ \frac{V_1}{R_3} - V_{out} sC_2 = 0 \end{cases} \tag{4.36}$$

This system is valid only if the opamps have low input bias currents and high gain. The transfer function of the circuit can be obtained by solving the system for V_{out}.

$$H(s) = \frac{V_{out}}{V_{in}} = -\frac{R_4}{R_1} \cdot \frac{\frac{1}{R_3R_4C_1C_2}}{s^2 + \frac{1}{R_2C_1}s + \frac{1}{R_3R_4C_1C_2}} \tag{4.37}$$

The expression of the resonance frequency and the quality factor is derived by comparing the transfer function of the circuit with the standard form given in the equation (4.25). It results:

$$\begin{cases} \omega_0 = \sqrt{\dfrac{1}{R_3 R_4 C_1 C_2}} \\ Q = \sqrt{\dfrac{R_2^2}{R_3 R_4}} \cdot \dfrac{C_1}{C_2} \end{cases} \tag{4.38}$$

If the band pass response offered by the circuit is not of interest, the expression of the resonant frequency and the quality factor can be simplified. This is done through equalizing as many components as possible. A careful analysis and the requirement for a unity gain results in the following identities:

$$\begin{cases} C_1 = C_2 = C \\ R_3 = R_4 = R_1 \\ R_2 = R_q \end{cases} \tag{4.39}$$

In this case the resonant frequency and the quality factor can be written:

$$\begin{cases} \omega_0 = \dfrac{1}{RC} \\ Q = \dfrac{R_q}{R} \end{cases} \tag{4.40}$$

The simplification of the transfer function is also beneficial from the point of view of the flexibility. The adjustment of the -3dB corner frequency becomes easier while the approximation is maintained. From the expression of ω_0 and Q it can be seen that the corner frequency can be varied independently of the quality factor by means of the capacitance C. Similarly, the quality factor can be adjusted independently of the corner frequency by changing the resistance R_q. An important consequence of the simplifications is that the quality factor depends only on a ratio of two resistances. This allows precise implementations of the quality factor, that are also stable with process corners and temperature variations [26]. Therefore, no Q tuning is required for precision enhancement.

In modern analog design the performances of a circuit can be drastically improved when processing differential signals. The advantages of the differential processing are the rejected common mode noise, the suppression of the even order distortion components, the doubling of the signal swing and the support for single supply operation [4]. Single supply operation is a must in modern mobile communication circuits. The opamp-RC biquad given in Figure 4.10 can be transformed to a fully differential form. The resulting circuit is presented in Figure 4.12.

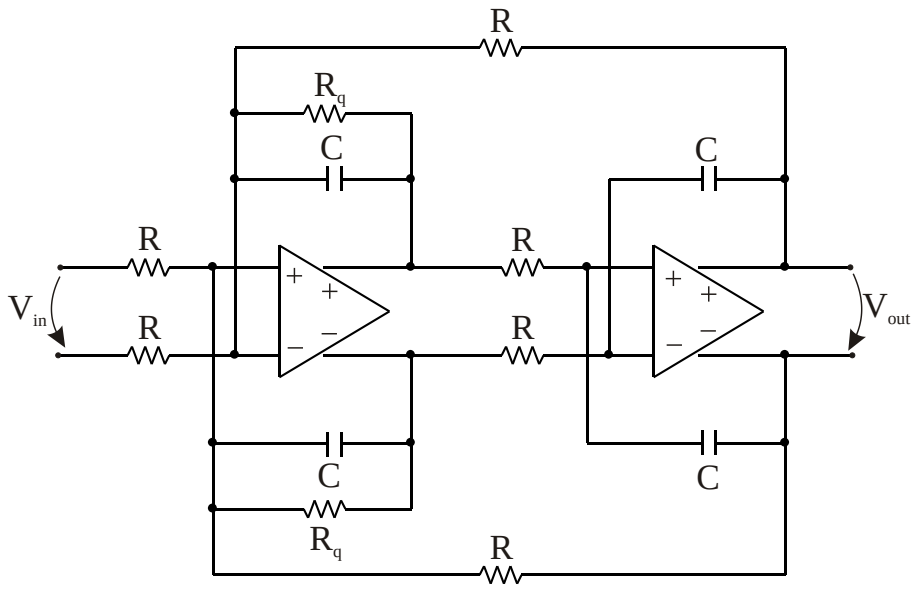


Figure 4.12: The fully differential opamp-RC Tow-Thomas biquad

Another advantage of the fully differential implementation over the single ended version is the reduced number of operational amplifiers, which implicitly lowers consumption. It can be demonstrated that the transfer function of the circuit has not been changed through the transformation from single ended to differential.

4.3.3 The effects of matching on the filter parameters

The detailed analysis of the matching effects on the filter parameters is a laborious task when considering the large number of components to be matched. Therefore, the characterization is usually done through a statistical computer simulation such as a Monte Carlo analysis. The Monte Carlo analysis randomly varies the matching parameters of the components, in this case resistors and capacitors, within a specified range of device tolerance. For example, if the statistically measured resistor matching is $\pm 1\%$ at fabrication, all the resistors in the circuit, that have a matching parameter associated, will be randomly changed within the $\pm 1\%$ range around the nominal value. The changes occur according to a defined probability density function, also measured at fabrication for a large number of resistors. The inclusion of the statistical models for the design kit is the task of the fabricant [26]. Typically, a reliable result of the Monte Carlo analysis requires a large number of runs. Figure 4.13 gives an example of Monte Carlo simulation for the transfer function of a 6^{th} order Butterworth filter model. Here all the resistors and the capacitors have been randomly varied within the range $\pm 3\%$ around their nominal value. The number of runs has been set to 10. The model has been designed using controled sources for a 1MHz ideal corner frequency.

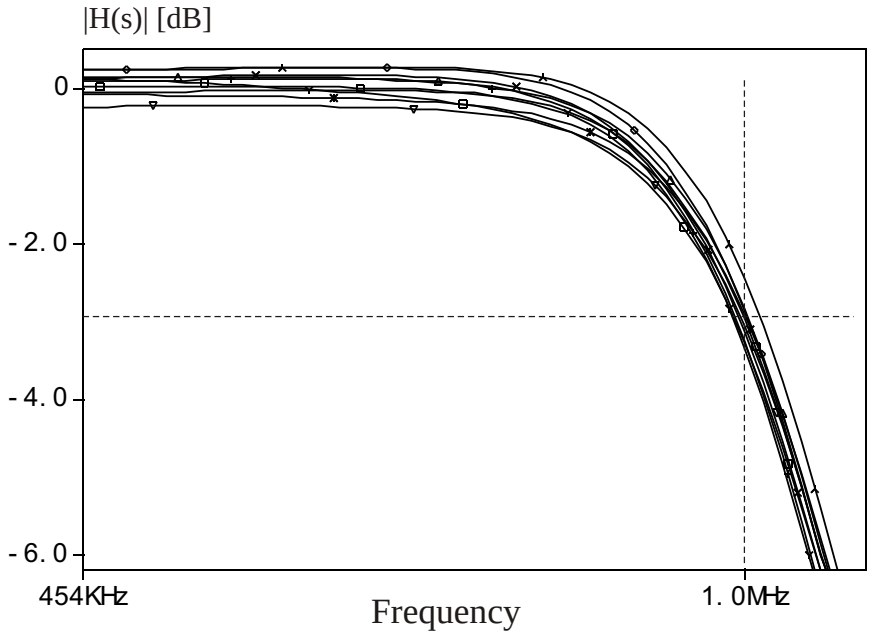


Figure 4.13: The Monte-Carlo simulation of the mismatch in the TT biquad

From the simulation it can be seen that the main effects of the component mismatch are the variation of the corner frequency and the ripples and gain variations introduced in the pass band. Typically the mismatch can be kept below $\pm 2\%$ if the minimum geometries specified by the process for 3σ matching are respected. The design of the passive components in an integrated circuit is always reduced to finding the optimal compromise between matching, silicon area, noise and parasitic components.

4.3.4 The corner frequency programming strategy

In the previous paragraphs has been demonstrated that the adjustment of the corner frequency is implemented by simply changing the RC time constant of the biquad. From the specifications results that the variation of the corner frequency should be linear on a logarithmic axes in the range between 200kHz and 6.4MHz. This requirement is connected to the distribution of the achievable frequency settings within the programming range. The programming template should be uniform as to eliminate large gaps between two consecutive frequency settings.

In chapter 3 has been shown that most of the methods based on changing the resistors and capacitors are designed for narrow band auto tuning of opamp-RC filters rather than wide bandwidth programmability. One strategy that allows the programming of the corner frequency in a wide range is to use a current division network for virtually scaling the capacitors. This method is very effective when ripples in the pass band and relatively high consumption are tolerated. However, in the case of some standards the ripples in the pass band and the gain errors

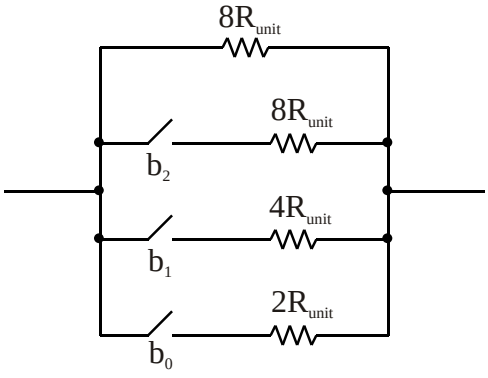
could harm the wanted signal, causing difficult digital demodulation and worse bit error rates. The consumption should also be kept as low as possible. This is the reason why switching algorithms of the resistors and the capacitors can offer better performance and predictable behavior, in spite of the larger silicon area requirement.

4.3.4.1 Switching resistors or capacitors only

One way of adjusting the corner frequency is to simply switch between resistors. In this case the achievable frequencies can be described by the general equation:

$$f_{Ci} = \frac{1}{2\pi R_i C} \ , \tag{4.41}$$

where f_{Ci} is the desired discrete corner frequency setting, R_i is the corresponding resistor and C is a fixed capacitance. In order to respect the modularity requirements of the programming template, the resistors must be switched in a way that allows the combination of a relatively small number of resistors for the implementation of a much larger number of possible settings, this is to connect the resistors in a binary weighted array. The main property of the binary weighted array is that the individual components are always doubled when jumping from one branch to the next. The schematic of a binary resistor array, controlled by 3 programming bits, is given in Figure 4.14.



$b_2\ b_1\ b_0$	R_{total}
000	8/1 R_{unit}
001	8/5 R_{unit}
010	8/3 R_{unit}
011	8/7 R_{unit}
100	8/2 R_{unit}
101	8/6 R_{unit}
110	8/4 R_{unit}
111	8/8 R_{unit}

Figure 4.14: The schematic of a binary resistor array, controlled by 3 programming bits

The corresponding programming table shows that the equivalent resistance of the array varies according to the digital control sequence between the limits R_{unit} and $8R_{unit}$. This variation means that the ratio between the largest and the smallest achievable frequencies is 8. The generalized expression for the total resistance of an N bit binary weighted array can be written as follows:

$$R_{total} = \frac{R_{unit}}{\frac{1}{2^N} + \sum_{i=0}^{N-1} \frac{b_i}{2^i}} \tag{4.42}$$

The dependence of the frequency programming ratio can be generalized for an N bit resistor array as follows:

$$\frac{f_{Cmax}}{f_{Cmin}} = 2^N \tag{4.43}$$

When the minimum and the maximum frequency settings are fixed, the number of programming bits, that offers the required variation, results:

$$N = \frac{\lg\left(\frac{f_{Cmax}}{f_{Cmin}}\right)}{\lg 2} = \log_2\left(\frac{f_{Cmax}}{f_{Cmin}}\right) \tag{4.44}$$

For the specified frequency range between 200kHz and 6.4MHz the number of bits results $N = 5$. The variation of the frequency with the equivalent resistance of the array is given in the Figure 4.15. In the simulation the capacitor has been set to 10pF.

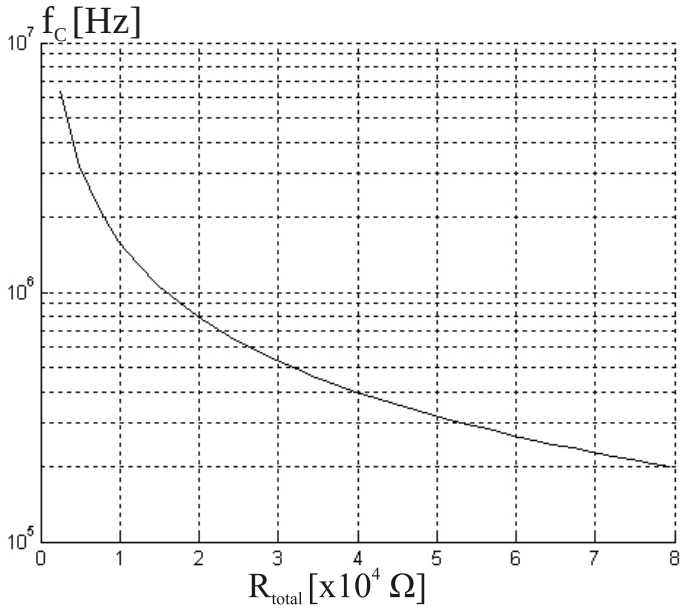


Figure 4.15: The variation of the corner frequency with the equivalent resistance of a 5 bit binary weighted array

It is of importance that, although the desired variation range has been achieved and the largest resistance is approximately $80k\Omega$, the smallest resistance results

$2.5k\Omega$, which could prove insufficient for a reasonable matching and causes a large spread in the component values. Its value can be increased when choosing a smaller capacitance, but in that case the highest resistance will introduce excessive noise due to its large value. Another important drawback of this programming approach is that the variation of the frequency introduces large gaps between consecutive values at higher frequencies. Figure 4.16 shows the simulated step between adjacent frequency settings.

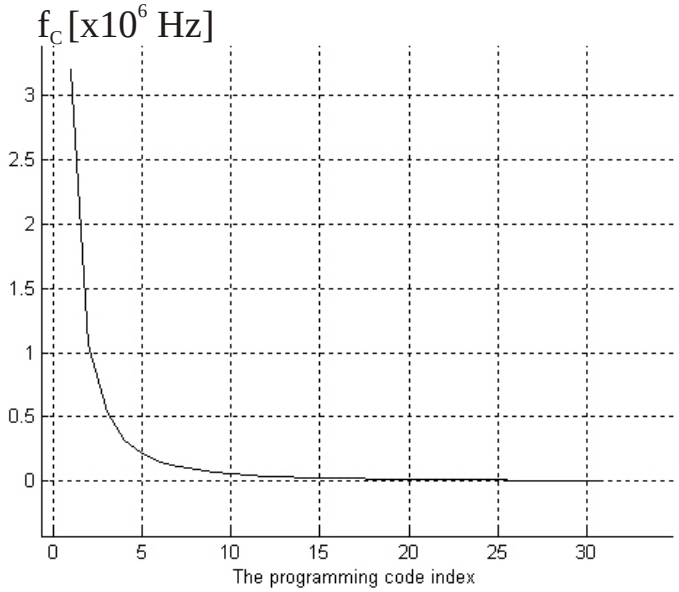


Figure 4.16: The frequency programming step

After a careful examination of the frequency step function it can be seen that for the two highest frequency settings the jump is made from 3.2MHz directly to 6.4MHz as it results also from the equation (4.41). This means that no frequency value can be selected between these two discrete steps.

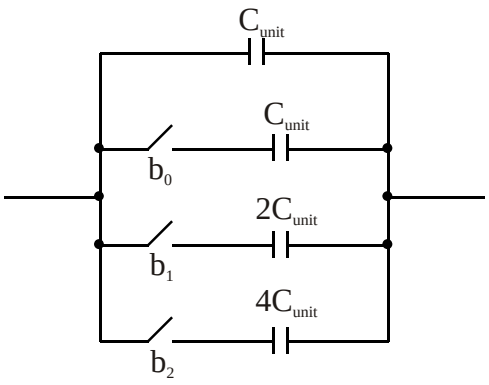
When using only a switched resistor array an additional problem arises at high corner frequency settings where the resistors are decreased. In these cases the filter response could be significantly influenced by the fixed value of the capacitance. In order to keep the resistors at reasonably large values for decent matching the capacitors need to be very small. Small capacitance values could not be sufficient to provide capacitive damping on the feedback path [27]. This pushes the unity-gain bandwidth requirements for the opamp in the high hundreds of MHz range in order to avoid peaking due to insufficient bandwidth.

A further analysis leads to similar results when switching only capacitors. Additionally, the capacitor only switching technique can be effectively implemented only at the cost of a very large silicon area. As a conclusion, switching only resistors or only capacitors in binary weighted arrays is not an optimal solution to the

investigated problems. The main drawbacks of this approach are the large spread in the component values and the very distant frequency settings at high frequencies.

4.3.4.2 Switching resistors and capacitors together

A solution, that partially overcomes the problems introduced by switching only resistors or only capacitors, is to switch both. In this scenario all the resistors and capacitors in the circuit are replaced with resistive and capacitive arrays. The arrays are controlled by a digital code that is decoded in order to ultimately define the corner frequency. Switching both the resistors and the capacitors extends the variation range of the corner frequency. The structure of the capacitor array is similar as for the resistors and it is shown in Figure 4.17 for 3 control bits.



$b_2\ b_1\ b_0$	C_{total}
000	1 C_{unit}
001	2 C_{unit}
010	3 C_{unit}
011	4 C_{unit}
100	5 C_{unit}
101	6 C_{unit}
110	7 C_{unit}
111	8 C_{unit}

Figure 4.17: The schematic of a binary capacitor array, controlled by 3 programming bits

The generalized expression of the total equivalent capacitance is:

$$C_{total} = C_{unit}\left(1 + \sum_{i=0}^{M-1} b_i 2^i\right) \tag{4.45}$$

For the switching template including both resistors and capacitors, the corner frequency can be written:

$$f_{Ci} = \frac{1}{2\pi R_i C_i} \tag{4.46}$$

If the resistor array is programmed through an N bit code and the capacitor array is controlled with M bits, the limits of the programming range are as follows:

$$\begin{cases} f_{Cmax} = \dfrac{1}{2\pi R_{unit} C_{unit}} \\ f_{Cmin} = \dfrac{1}{2\pi 2^N R_{unit} 2^M C_{unit}} \end{cases} \tag{4.47}$$

The ratio between the maximum and the minimum achievable frequencies results:

$$\frac{f_{Cmax}}{f_{Cmin}} = 2^{N+M} \tag{4.48}$$

The number of the required control bits is then:

$$N + M = \frac{\lg\left(\dfrac{f_{Cmax}}{f_{Cmin}}\right)}{\lg 2} = \log_2\left(\frac{f_{Cmax}}{f_{Cmin}}\right) \tag{4.49}$$

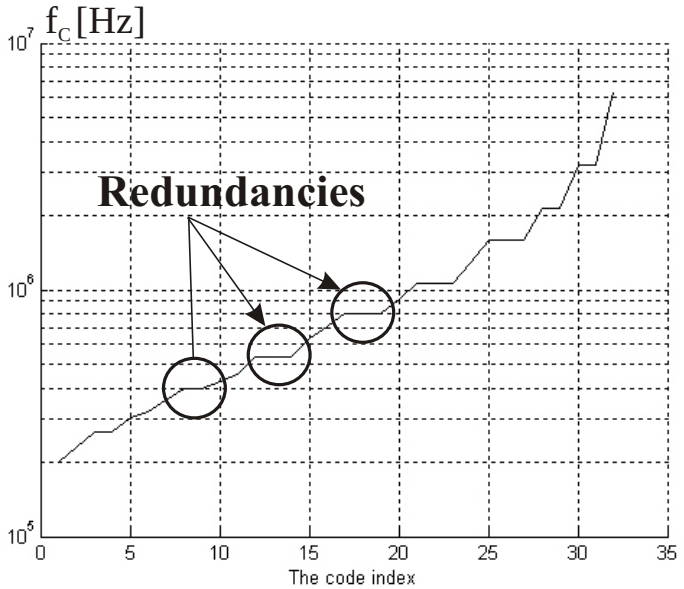


Figure 4.18: The simulated variation of the corner frequency with the code index

It is important to notice that the overall number of control bits has not been changed compared to the templates where only resistors or capacitors were switched. The most important benefit of the RC switching scheme is the possibility to distribute the available control bits between the resistor and the capacitor arrays in a way that allows the reduction of the component spread. The simulated variation of

the corner frequency with the code index is given in Figure 4.18. Here $N = 2$ and $M = 3$.

The main drawback of this programming template is that it introduces code redundancies. This means that a certain frequency value can be achieved for two or more RC combinations. The redundancies appear as short horizontal lines on the simulated frequency curve, showing that more than one code corresponds to the same frequency setting. As an example, the same frequency setting is achieved for the set of values $4R_{unit}$-C_{unit} as for R_{unit}-$4C_{unit}$.

Another drawback of the scheme is that it inherits the problems regarding the unbalanced distribution of the achievable frequencies over the programming range. At high frequencies the jump is similar as in the case of the resistor only programming template. The simulated frequency step is presented in Figure 4.19. It can be seen that between the highest two frequencies the jump is still 3.2MHz. The return to zero of the curve is a result of the code redundancies introduced by the non-biunivocal relation between the digital control word and the frequency values.

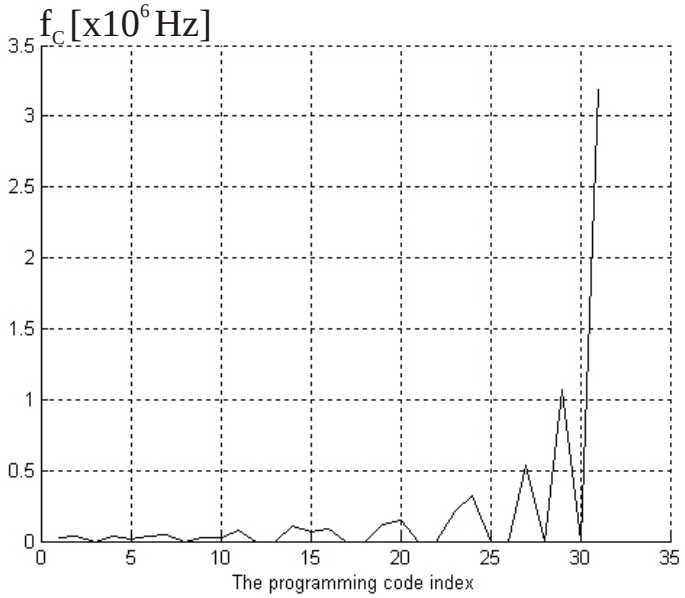


Figure 4.19: The frequency programming step for the RC switching template

4.3.4.3 An alternative RC switching template

The main goal of the proposed alternative RC switching template is the complete elimination of the code redundancies, the monotonicity of the code-frequency dependence and the introduction of a more uniform distribution of the frequency settings within the programming range. In the previous paragraphs it has been demonstrated that both, the code redundancies and the non-uniform distribution of the frequency

settings, are the consequences of using classical binary weighted resistor and capacitor arrays. These can only facilitate the doubling of the frequencies, regardless of the location in the programming template. The result is an insufficient coverage and the lack of access to any value in the upper half of the entire programming domain between 3.2MHz and 6.4MHz. The main idea, that helps overcoming these problems, is to use code segmentation and custom, yet structured arrays. These concepts are explained in detail in the following section.

The starting point of the description is presented in Figure 4.20, showing the values covered by the corner frequency settings, corresponding to a binary weighted RC switching template. The critical values representing the extremes of the achievable resistor and capacitor values have been highlighted. The programming strategy, that has been depicted here, assumes that the resistors are used for switching frequencies in a large interval. Capacitors select the possible settings within a smaller domain. Each sub-domain of the template has been marked with a separate ellipse.

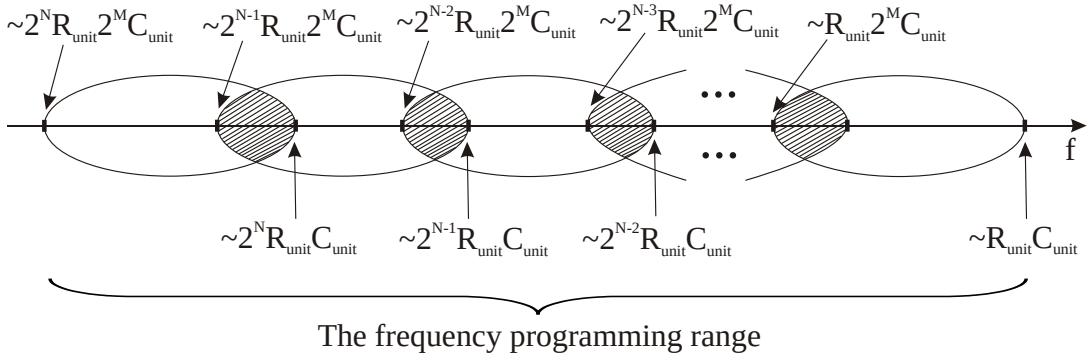


Figure 4.20: The corner frequency settings corresponding to a binary weighted RC switching template

The dashed zones, obtained by the intersection of different sub-domains, represent the settings that can be achieved by using multiple RC combinations. It is worth noticing that each sub-domain is associated with a single resistor value. From this observation results that the resistor array can be successfully used to switch the octaves in the programming template. In the following each sub-domain will be called a *segment* due to the resemblance of the code-frequency correspondence with a curve built using segments. The resistor values in the template have been chosen so far from the frequencies limiting a specific segment. An improvement can be achieved if the resistors are chosen for a nominal frequency in the middle of each segment. The nominal frequencies can still be switched in octaves. From Figure 4.20 it can be seen that the elimination of the redundancies means that the dashed zones will completely disappear. This is possible when the capacitive arrays are used to vary the frequencies within a smaller range than in the original binary case. When the resistors are setting the nominal frequencies in the middle of each segment, the capacitors must be sized for a variation with a maximum critical percent around the

nominal frequencies. This principle is shown in Figure 4.21 where multiples of f_C mark the nominal frequencies.

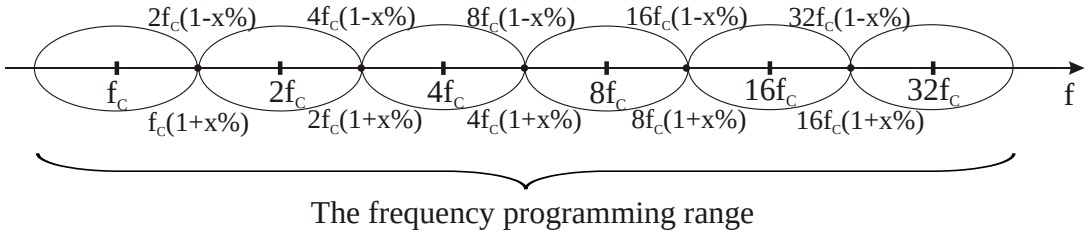


Figure 4.21: The critical percent variation around the nominal frequencies that eliminates code redundancies

The critical percent x can be determined by solving the following equation:

$$f_C\left(1+\frac{x}{100}\right) = 2f_C\left(1-\frac{x}{100}\right) \tag{4.50}$$

It results that the critical variation is $x = 33\%$. In order to cover the programming range as densly as possible, the percent variation around the nominal frequencies, introduced by the capacitive arrays, can be safely chosen 30%. The choice of the nominal frequencies is based on variations with process and temperature of the expected corner frequencies. In order to allow an eventual frequency error correction also at the margins of the programming range the nominal frequencies can be chosen 200kHz, 400kHz, 800kHz, 1.6MHz, 3.2MHz and 6.4MHz. For covering all the nominal frequencies 3 control bits are needed. For the capacitor arrays 4 bits insure a decent granularity of the achievable frequency values. The total length of the programming code is then 7 bits.

When setting the values of the capacitors and the resistors in the tuning template, one must also take into account the variations of the corner frequency with process tolerances and temperature. For the used design kit the expected maximum and minimum frequency errors are $\epsilon_{fcmax} = 55\%$ and $\epsilon_{fcmin} = -35\%$. The detailed simulation of these values will be explained later. Since the real values of the components within the specified tolerance range cannot be predicted, there is an uncertainty in setting the corner frequency of the filter. This uncertainty leads to the idea of using an error compensation system. While the distribution of the achivable frequencies within the limits of the range is dense enough for a possible compensation of the errors, the situation is different at the margins of the programming template. Here the $\pm 30\%$ variation around 200kHz and 6.4MHz might not be sufficient for a proper compensation. This is the reason why the programming range must be extended at the margins for a coverage of the simulated errors.

The proposed structure of the resistive and the capacitive arrays are given in Figure 4.22. The capacitive array is divided into binary weighted subnetworks. The choice of the subnetwork to be used for a particular frequency setting is determined by the most significant three bits of the programming code, a_1 to a_3. The final selection of the capacitive path to be used is done by correctly setting the remaining four bits, a_4 to a_7.

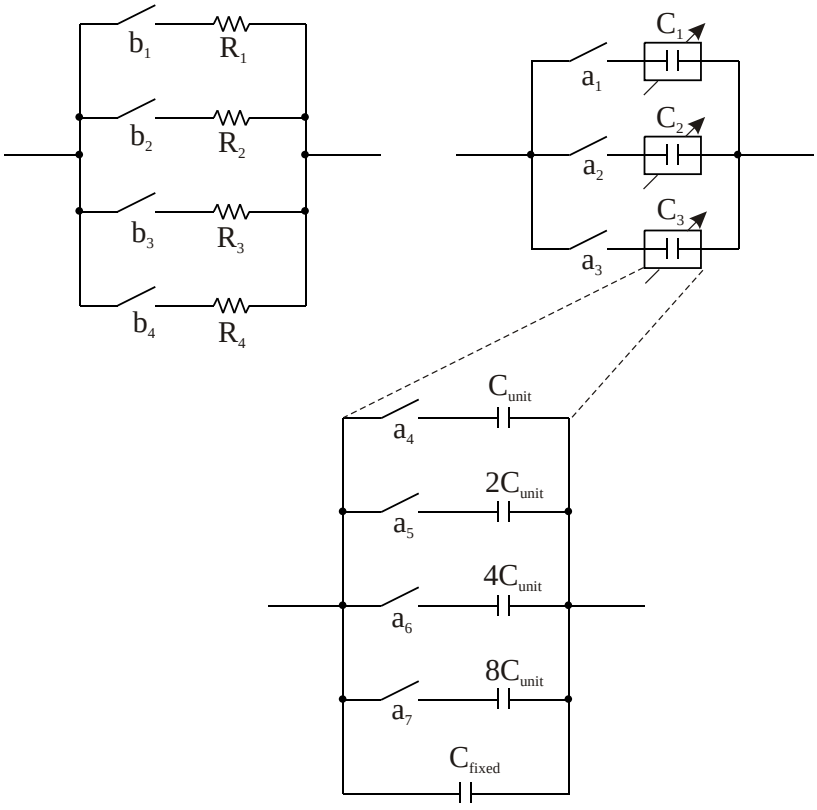


Figure 4.22: The proposed structure of the resistive and the capacitive arrays

Range	Frequency	Resistor	Capacitor array
$(200kHz - 37\%)$-$(200kHz + 30\%)$	126kHz - 260kHz	R_1	C_1
$400kHz \pm 30\%$	280kHz - 520kHz	R_1	C_2
$800kHz \pm 30\%$	560kHz - 1.04MHz	R_2	C_2
$1.6MHz \pm 30\%$	1.12MHz - 2.08MHz	R_3	C_2
$3.2MHz \pm 30\%$	2.24MHz - 4.16MHz	R_4	C_2
$(6.4MHz - 30\%)$-$(6.4MHz + 55\%)$	4.48MHz - 9.92MHz	R_4	C_3

Table 4.1: The combination of resistors and capacitors used for setting the nominal corner frequencies

The combinations of resistors and capacitors to be used for each nominal frequency and the fine variation range around it are summarized in Table 4.1. Each of these combinations define a segment of the programming range. The variation of the corner frequencies within a segment is not linear but inversely proportional to the resistance and capacitance values. However, the error compared to a linear variation is relatively small due to the narrow range covered by a segment.

The sizing of each binary weighted capacitive subnetwork is done to provide the desired variation range around the nominal frequency. The smallest achievable capacitance in the array is equal to the fixed capacitance, C_{fixed}. This value will define the maximum frequency setting within the segment i as follows:

$$f_{Cmax_i} = \frac{1}{2\pi R_i C_{fixed}} \tag{4.51}$$

R_i is the corresponding resistance which selects the nominal frequencies. The minimum frequency is then:

$$f_{Cmin_i} = \frac{1}{2\pi R_i \left(C_{fixed} + 15C_{unit}\right)} \tag{4.52}$$

In order to determine the general sizing equation of the unit capacitances the desired percent variation around the nominal frequency is noted Δf_1 in the negative sense and Δf_2 in the positive sense. In this case the following system of equations can be written:

$$\begin{cases} f_{Cnom_i}\left(1 + \dfrac{\Delta f_2}{100}\right) = \dfrac{1}{2\pi R_i C_{fixed}} \\ f_{Cnom_i}\left(1 + \dfrac{\Delta f_1}{100}\right) = \dfrac{1}{2\pi R_i \left(C_{fixed} + 15C_{unit}\right)} \end{cases} \tag{4.53}$$

By dividing the two equations it results:

$$\frac{1 + \dfrac{\Delta f_2}{100}}{1 + \dfrac{\Delta f_1}{100}} = 1 + \frac{15C_{unit}}{C_{fixed}} \tag{4.54}$$

The value of the unit capacitance can be determined by solving equation (4.54) for C_{unit}.

$$C_{unit} = \frac{C_{fixed}}{15} \cdot \frac{\Delta f_2 - \Delta f_1}{100 + \Delta f_1} \tag{4.55}$$

The value of the fixed capacitance is determined from the equation (4.51) based on the maximum frequency requirement. It is of importance that the value of the resistance must be known prior to sizing the capacitances. In the design procedure there is a trade-off between the resistance values, the noise and area specifications, matching and the feasibility of the capacitor implementations. As an example, if the resistance is equal to 40kΩ and the maximum frequency is $800kHz+30\%$=1.04MHz, the resulting fixed capacitance is 3.83pF. The unit capacitance, that offers a ±30% variation around the nominal 800kHz is 219fF. These capacitances can be safely implemented in the integrated circuit with a reasonable silicon area.

The resistance values have been chosen according to similar calculations. The minimum resistance in the resistive array, R_4, and the fixed capacitance from the C_3 capacitance network will determine the absolute maximum achievable corner frequency. It results:

$$f_{Cmax} = \frac{1}{2\pi R_4 C_{fixed3}} \tag{4.56}$$

From the Table 4.1 results that the maximum frequency is 9.92MHz. The choice of the smallest resistance must allow a reasonable matching and the feasibility of the smallest fixed capacitance. If the resistance is chosen 10kΩ the capacitance C_{fixed3} results 1.6pF. This leads to a unit capacitance in the third subnetwork equal to 175fF. From the condition of switching the octaves it results that the resistive array must be binary weighted. As a consequence, the resistances are $R_1 = 80k\Omega$, $R_2 = 40k\Omega$, $R_3 = 20k\Omega$ and $R_4 = 10k\Omega$.

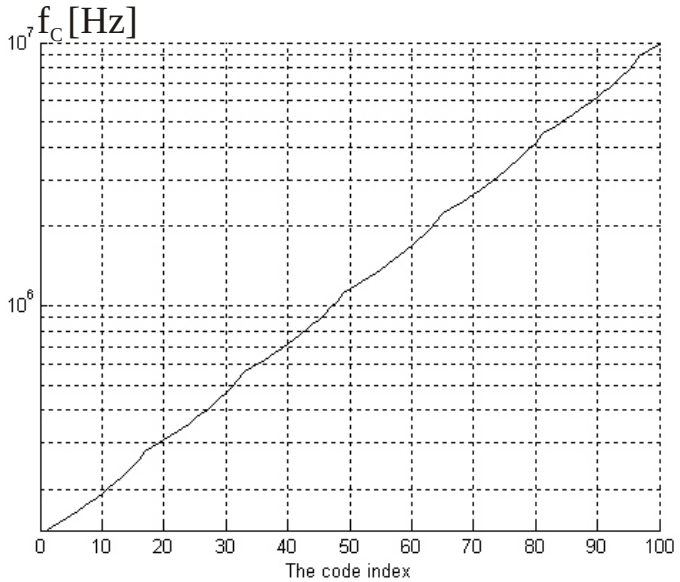


Figure 4.23: Representation of the achievable corner frequencies on a logarithmic axes against the selection code

The series resistance of the MOS switches can be compensated by weighting the transistor geometries and by correctly choosing the resistor values. The control signals of the resistive network are decoded from the most significant three bits of the selection code. According to the described programming template, the achievable corner frequencies are listed in Appendix A. These frequencies can be represented on a logarithmic scale against the filter programming code index. This representation is given in Figure 4.23. It can be seen that the distribution of the frequencies is quasi-linear on the logarithmic axes, the code redundancies have disappeared and the monotonicity of the curve has been restored.

4.3.5 The corner frequency error prediction system

The purpose of the corner frequency error prediction circuit is to give an estimate over the corner frequency percent error $\epsilon_{fc}[\%]$, that is introduced by process tolerances and temperature. The predicted percent error allows the implementation of a correction algorithm that compensates the undesired variations. This algorithm is based on a predistortion of the corner frequency setting, as specified in the following equation:

$$f_{Cset} = \frac{100 \cdot f_{Cideal}}{100 + \epsilon_{fc}[\%]}, \tag{4.57}$$

where f_{Cset} is the real corner frequency, f_{Cideal} is the ideal corner frequency and $\epsilon_{fc}[\%]$ is the percent frequency error. It is important to notice that the frequency error can be positive or negative. The equation (4.57) is equally valid in both cases. For example, if the expected frequency error is -20% and the desired frequency is 1.5MHz, the correction algorithm determines that the real frequency should be set to 1.85MHz. Similarly, if the expected frequency error is $+20\%$ and the ideal corner frequency is the same, the real setting should be approximately 1.36MHz.

4.3.5.1 Principles of the time constant measurement

An interesting approach to RC time constant measurement has been presented in [18]. The main idea is to convert the real RC time constant information to a measurable time period and then to measure this time with a counter by using a reference clock signal. The measurement result can be expressed by a digital code. The circuit described in this paper is presented in Figure 4.24.

The circuit built with the opamp and the passive components can be configured as continuous time or switched capacitor integrator. When the signal ϕ_C is asserted the output voltage of the integrator is equal to V_{AG}. When ϕ_C is turned off and ϕ_B is asserted the capacitor C_0 will be charged with a constant current through the resistor R_1. The output voltage of the inverting integrator will exhibit a linear decrease until ϕ_B is turned off. At this point ϕ_A starts to vary as a higher frequency pulse, while the comparator enables the counter. The output voltage of the switched

capacitor integrator will increase linearly in steps until it reaches the level V_{AG} and the capacitor C_0 is discharged. At this moment the content of the counter is proportional to the nominal RC time constant and the time constant error.

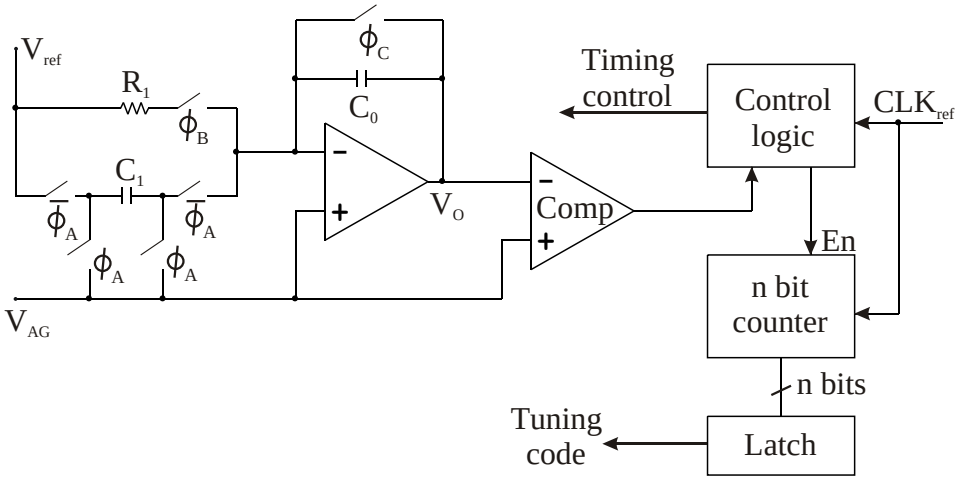


Figure 4.24: Filter automatic tuning by measurement of the RC time constant as described in [18]

The circuit is intended for tuning the corner frequency of opamp-RC filters and $\Sigma\Delta$ modulators. The accuracy of the measurement is highly dependent on the precision of the reference voltage. Another important issue is that the circuit requires several control signals with the corresponding timing. The signals ϕ_A and $\overline{\phi_A}$ must be a non-overlapping clocks for a correct operation of the switched capacitor integrator.

The error prediction system proposed in this work [14] can be considered as an improvement of the aforementioned tuning circuit. The measurement principle is still based on charging a capacitor through a resistor from a constant reference voltage. The dependence of the measurement accuracy on a reference voltage is eliminated by using a differential charging mechanism. In this case the double ramp algorithm is not necessary and the measurement can be done within a single capacitor charging cycle. The only required control signal is the reset, which simply lets the circuit perform until the measurement is finished. At the end of the cycle the circuit holds the measurement data until a read out is requested by a control logic. The digital code, proportional to the measured error, is used rather for read out and a wide band correction than for a classical auto-tuning. The block diagram of the time constant measurement circuit is presented in Figure 4.25.

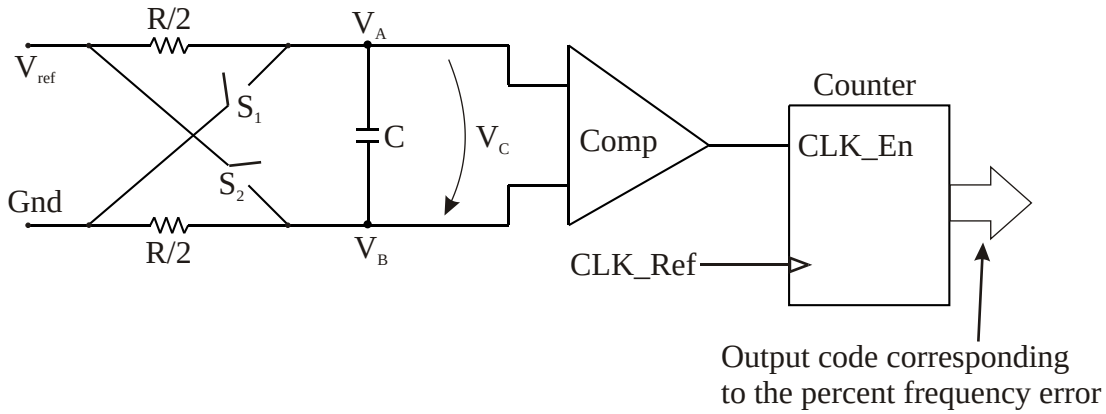


Figure 4.25: Block diagram of the time constant measurement circuit

The error prediction unit is built around an analog front end and a digital control-measurement logic. The analog front end employs resistors and a capacitor of the same type as used in the filter itself. The block diagram of the circuit is given in Figure 4.25. The logic circuit is a counter with clock enable. The functionality of the circuit is as follows: Initially the switches S_1 and S_2 are closed and the capacitor is charged with a voltage $-V_{ref}$. Accordingly, the output of the comparator is in a logic "HIGH" state. This state enables the reference clock signal to get through to the clock input of the counter. In the mean while the counter is initialized by a special logic with an all zero state. When the switches are opened and the measurement sequence starts, the capacitor begins to charge to the opposite polarity through the resistors R. The voltages V_A and V_B at the terminals of the capacitor can be expressed as functions of the reference voltage and the RC time constant.

$$\begin{cases} V_A = V_{ref} \cdot e^{-\frac{t}{RC}} \\ V_B = V_{ref} \cdot \left(1 - e^{-\frac{t}{RC}}\right) \end{cases} \tag{4.58}$$

The comparator output will switch in a logic "LOW" state when V_A equals V_B. Assuming that this happens at the moment t_1, we may write:

$$V_{ref} \cdot e^{-\frac{t_1}{RC}} = V_{ref} \cdot \left(1 - e^{-\frac{t_1}{RC}}\right) \tag{4.59}$$

It results:

$$t_1 = RC \cdot \ln 2 = T \cdot \ln 2\,|_{T=RC} \tag{4.60}$$

The variation of the moment t_1 for different time constants can be followed in Figure 4.26.

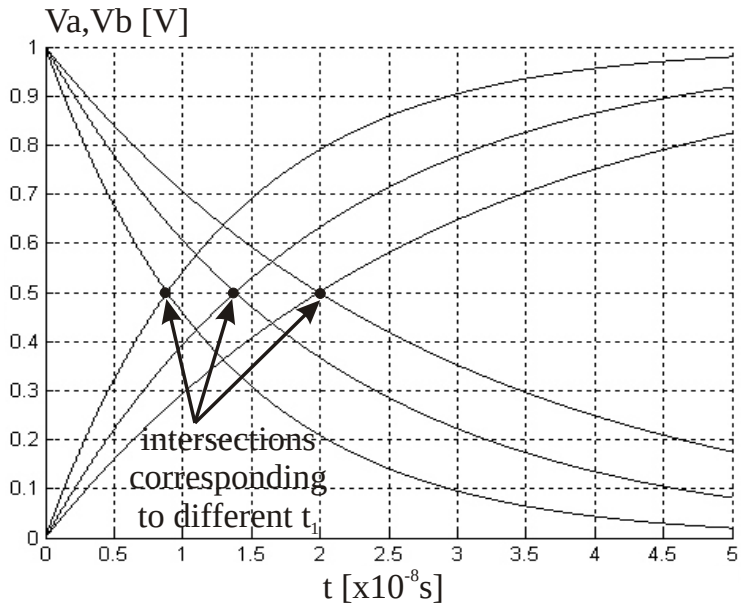


Figure 4.26: Variation of the voltages V_A and V_B and of the moment t_1 for different RC time constants

Assuming that the reference frequency of the counter clock signal is f_{CLKref}, the time t_1 can be expressed also as a function of this frequency and the number of counted cycles, N, at that moment.

$$t_1 = \frac{N}{f_{CLKref}} \tag{4.61}$$

It results:

$$N = f_{CLKref} \cdot RC \cdot \ln 2 = f_{CLKref} \cdot T \cdot \ln 2 \tag{4.62}$$

The number of cycles passed by the counter at the moment t_1 is proportional to the real on-chip time constant. The variation of the product RC includes the effects of both the process tolerances and the temperature. If the logic is a binary counter, the proportionality can be expressed by a look-up table that contains the time-code correspondence.

4.3.5.2 The time constant and the frequency error

A first overview on the expected variation of the resistors and the capacitors can be obtained from simple corner simulations. The setup for these simulations and the measured values for the used design kit are presented in the Appendix B. The specified temperature range of the circuit is between -20°C and 85°C. After running the simulations for several process corners and the extreme temperatures, the

percent variation range of a real resistor is obtained by computing the maximum and minimum relative errors ϵ_{Rmax} and ϵ_{Rmin}.

$$\begin{cases} \epsilon_{Rmax}[\%] = \dfrac{R_{max} - R_{nom}}{R_{nom}} \cdot 100 \\ \epsilon_{Rmin}[\%] = \dfrac{R_{min} - R_{nom}}{R_{nom}} \cdot 100 \end{cases}, \tag{4.63}$$

where R_{nom} is the ideal desired resistance value, simulated for nominal process corners and 27°C. Similarly, when C_{nom} is the ideal capacitance value, the maximum and minimum relative capacitance errors can be calculated as follows:

$$\begin{cases} \epsilon_{Cmax}[\%] = \dfrac{C_{max} - C_{nom}}{C_{nom}} \cdot 100 \\ \epsilon_{Cmin}[\%] = \dfrac{C_{min} - C_{nom}}{C_{nom}} \cdot 100 \end{cases} \tag{4.64}$$

The nominal, the maximum and the minimum values of the RC time constant are then:

$$\begin{cases} T_{nom} = R_{nom}C_{nom} \\ T_{max} = R_{max}C_{max} = T_{nom}\left(1 + \dfrac{\epsilon_{Rmax}}{100}\right)\left(1 + \dfrac{\epsilon_{Cmax}}{100}\right) \\ T_{min} = R_{min}C_{min} = T_{nom}\left(1 + \dfrac{\epsilon_{Rmin}}{100}\right)\left(1 + \dfrac{\epsilon_{Cmin}}{100}\right) \end{cases} \tag{4.65}$$

The expected maximum and minimum deviations of the measured time, t_1, can be determined by simply multiplying both T_{max} and T_{min} with $\ln 2$.

$$\begin{cases} t_{1max} = T_{max} \cdot \ln 2 \\ t_{1min} = T_{min} \cdot \ln 2 \end{cases} \tag{4.66}$$

The corresponding maximum and minimum corner frequency errors can be readily determined by using the following equations:

$$\begin{cases} f_{Cnom} = \dfrac{1}{2\pi R_{nom}C_{nom}} = \dfrac{1}{2\pi T_{nom}} \\ f_{Cmax} = \dfrac{1}{2\pi R_{min}C_{min}} = \dfrac{1}{2\pi T_{min}} \\ f_{Cmin} = \dfrac{1}{2\pi R_{max}C_{max}} = \dfrac{1}{2\pi T_{max}} \end{cases} \tag{4.67}$$

The maximum and the minimum relative frequency errors are:

$$\begin{cases} \epsilon_{fcmax}[\%] = \dfrac{f_{Cmax} - f_{Cnom}}{f_{Cnom}} \cdot 100 \\ \epsilon_{fcmin}[\%] = \dfrac{f_{Cmin} - f_{Cnom}}{f_{Cnom}} \cdot 100 \end{cases} \tag{4.68}$$

By combining the equations (4.65), (4.67) and (4.68) the relative corner frequency errors result as functions of the percent errors of the resistors and the capacitors.

$$\begin{cases} \epsilon_{fcmax}[\%] = \left(\dfrac{1}{\left(1 + \dfrac{\epsilon_{Rmin}}{100}\right) \cdot \left(1 + \dfrac{\epsilon_{Cmin}}{100}\right)} - 1 \right) \cdot 100 \\ \epsilon_{fcmin}[\%] = \left(\dfrac{1}{\left(1 + \dfrac{\epsilon_{Rmax}}{100}\right) \cdot \left(1 + \dfrac{\epsilon_{Cmax}}{100}\right)} - 1 \right) \cdot 100 \end{cases} \tag{4.69}$$

These expressions represent the maximum theoretical frequency error that could be expected after fabrication. When combining the contributions of the resistors and the capacitors, the maximum and the minimum errors were taken for the extremes of each individual passive component. The calculated theoretical errors could be reduced to some extent by the fact that statistically resistors and capacitors may not exhibit their extreme errors for the same process corner and the same temperature. This means that the frequency error could be somewhat lower than the theoretical maximum. The calculations yield a satisfying result only if the models provided by the process owner are sufficiently close to the real process.

4.3.5.3 Component sizing

The component sizing usually starts with the choice of the reference frequency. The reason for this is that in wireless receivers there are only some discrete frequencies available at the outputs of different PLL-s. For a standalone system it is important to relay only on the locally available resources. When the reference frequency is known the number of bits required for a correct operation, n, can be determined from the following condition:

$$2^n \geq t_{1max} \cdot f_{CLKref} \tag{4.70}$$

This condition is necessary in order to be sure that the counter will not stop counting at a moment before t_{1max} and that the result of the measurement is correct. Usually the coverage offered by the computed n bits is larger that the expected

t_{1max}. Due to the extra coverage an important issue arising in the measurement cycle is the flexibility in mapping the resulting digital code to an actual value of the frequency error. The number of cycles passed by the counter between the start of the measurement and t_{1min} is not zero. This allows a flexibility in dynamically mapping the codes to the errors in a look-up table. Therefore, the maximum and the minimum values of t_1 can be chosen with a margin with respect to the absolute minimum and the absolute maximum. The design starts by choosing an arbitrary Δt margin between t_{1max} and the the theoretical maximum measurable time supported by the counter. The time intervals used for sizing the components are represented in Figure 4.27. The valid measurement interval is fixed by the expected resistance and capacitance errors, while t_0 is the starting moment of the entire measurement cycle when the switches are opened.

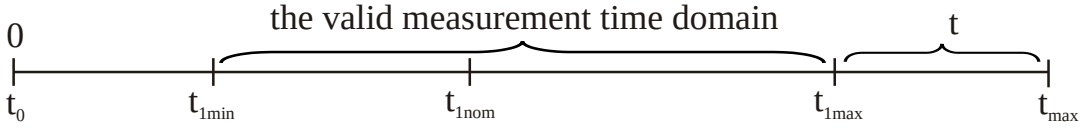


Figure 4.27: The time intervals used for sizing

The time margin Δt can be expressed as follows:

$$\Delta t = t_{max} - t_{1max} = \frac{2^n}{f_{CLKref}} - R_{nom}C_{nom}\left(1+\frac{\epsilon_{Rmax}}{100}\right)\left(1+\frac{\epsilon_{Cmax}}{100}\right)\ln 2 \quad (4.71)$$

From the distribution of the time intervals it can be seen that the choice of Δt decides the position of the measurement interval between t_0 and t_{max}. The value of the nominal time constant, T_{nom}, can be calculated from the equation (4.71). It results:

$$R_{nom}C_{nom} = \frac{\frac{2^n}{f_{CLKref}} - \Delta t}{\left(1+\frac{\epsilon_{Rmax}}{100}\right)\left(1+\frac{\epsilon_{Cmax}}{100}\right)\ln 2} \quad (4.72)$$

It is obvious that for a given Δt there is only one constraint for two variables. In this case one of the variables must be chosen and the other results from calculations. Since the noise of the circuit is not critical and the value of the capacitor has a much more important impact on the area requirements of the circuit, it usually makes sense to choose a reasonable value for the capacitor. The resistor can be computed as follows:

$$R_{nom} = \frac{\frac{2^n}{f_{CLKref}} - \Delta t}{\left(1 + \frac{\epsilon_{Rmax}}{100}\right)\left(1 + \frac{\epsilon_{Cmax}}{100}\right) C_{nom} \ln 2} \tag{4.73}$$

This resistance is implemented in two halves according to the schematic in Figure 4.25. When the nominal values of the resistor and the capacitor have been determined, the number of counter states associated with a valid frequency error can be determined from the equation (4.74).

$$\begin{aligned} Nr.states = R_{nom}C_{nom}f_{CLKref} \ln 2 \cdot \left(\frac{\epsilon_{Rmax} - \epsilon_{Rmin} + \epsilon_{Cmax} - \epsilon_{Cmin}}{100}\right) + \\ + R_{nom}C_{nom}f_{CLKref} \ln 2 \cdot \left(\frac{\epsilon_{Rmax}\epsilon_{Cmax} - \epsilon_{Rmin}\epsilon_{Cmin}}{100^2}\right) \end{aligned} \tag{4.74}$$

From the simulations and the sizing procedure presented in the Appendix B results that the nominal resistance and capacitance values are $R_{nom} = 348.7k\Omega$ and $C_{nom} = 10pF$. The reference frequency has been chosen 26MHz and the counter is built using 7 bits. The number of valid states available for measurement is 57. For the determined components and time intervals the Figure 4.28 can be redrawn with the final values of the significant time references.

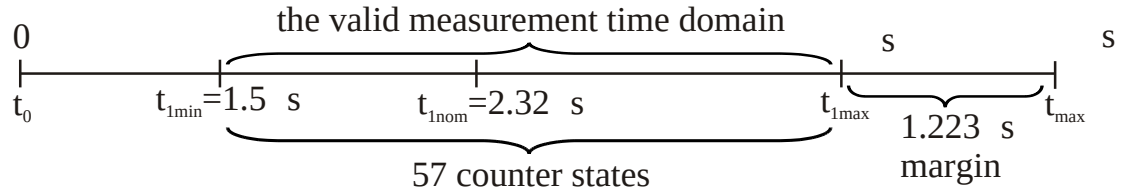


Figure 4.28: The final time intervals used for sizing

For a given set of calculated components the resolution of the circuit can be increased by increasing the reference frequency. Choosing Δt as large as possible results in the decrease of the component sizes but leads to losses in what concerns the resolution. On the other hand a lower reference frequency eases up the speed and current consumption requirements for the comparator by higher allowed switching delay times and helps sparing battery lifetime. It is of importance that the reference frequency can be changed and the values of the look-up table can be remapped accordingly without modifying the structure of the circuit and the fixed component values. This offers the required flexibility to the measurement system. Since the counter in the measurement logic is not decimal, a look-up table is needed in order to assign a corner frequency error to the measured digital code. The mapping is done

by first calculating t_{1min} and then adding a difference equal to the reference period, T_{CLKref}. The resulting t_{1i} discrete moments of time are then translated into the corresponding time constants. The real frequency and the relative frequency error associated with a given time constant can be computed according to the equations (4.67) and (4.68). The correspondence between the code and the predicted frequency error is given in Appendix C. Figure 4.29 gives the representation of the frequency error against the error code index. The code 0111110 has been assigned to a near zero corner frequency error.

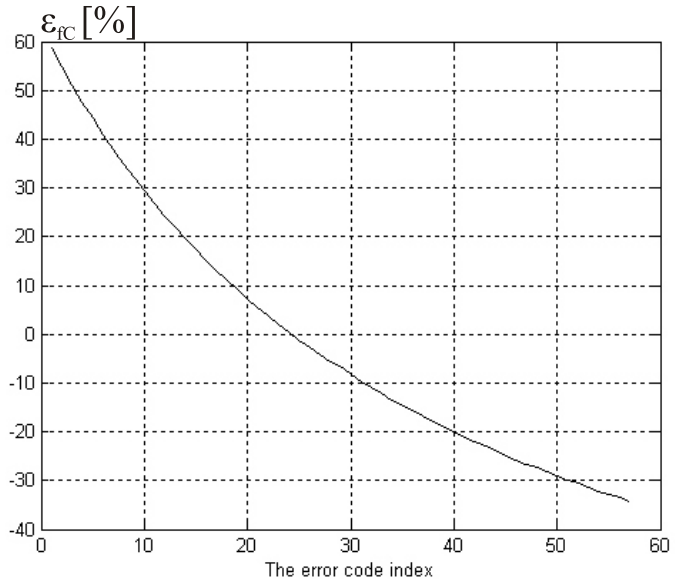


Figure 4.29: The predicted frequency errors against the code index

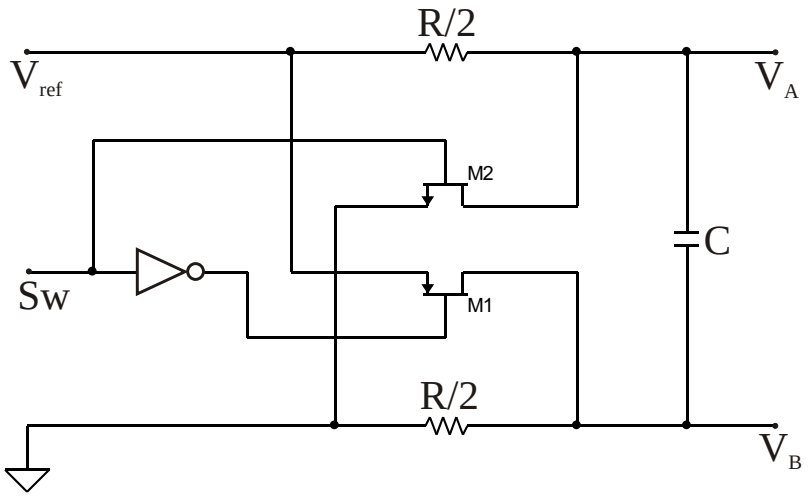


Figure 4.30: Schematic of the RC switch network

- **The analog front end of the measurement system**

As presented in Figure 4.25 the analog front end of the measurement system consists of an RC switch network and a comparator. The schematic of the RC switch network is given in Figure 4.30.

The switches are implemented as short channel complementary NMOS-PMOS transistors in order to minimize their equivalent resistance [4]. The transistors are controlled by the direct or the inverted Sw signal. When the Sw is in a $HIGH$ state the switches are opened and the capacitor charges through the resistors. When the Sw is in a LOW state the switches are closed and the capacitor is charged with the voltage $-V_{ref}$. It is of importance that each resistance is half the calculated R_{nom} due to the differential configuration of the circuit.

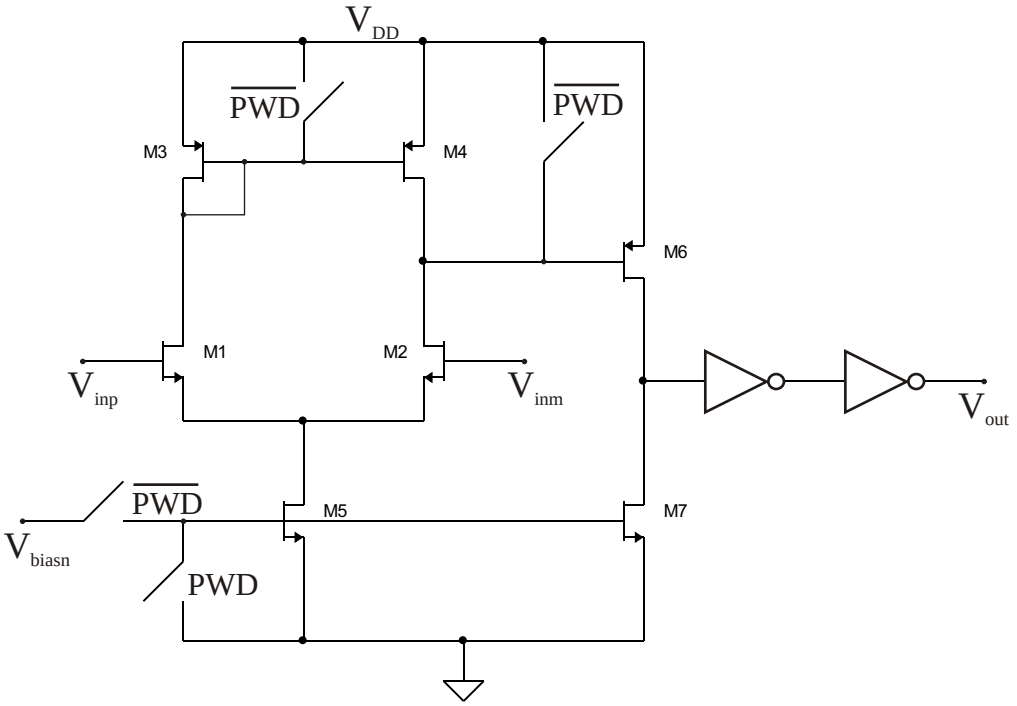


Figure 4.31: Schematic of the comparator

The schematic of the comparator is given in Figure 4.31. The circuit is built as a simple uncompensated Miller opamp. The two inverters at the output have been added in order to achieve a switching time and a delay less than quarter of the reference clock signal period. An additional power down functionality is also included in order to be able to switch off the comparator after the calibration cycle has been completed. The power down is controlled by the signal PWD. The transistors and the bias currents have been sized for a trade-off between consumption and speed. From corner simulations results that the worst case delay of the comparator is less

than one reference clock period for a 1pF load capacitance. Since the real load of the comparator is the input of an AND gate in the structure of the logic, the 1pF capacitor is sufficient for simulations.

- **The measurement logic**

The measurement logic is a 7 bit binary counter with enable, asynchronous clear and clock signals. The block diagram of the circuit is given in Figure 4.32.

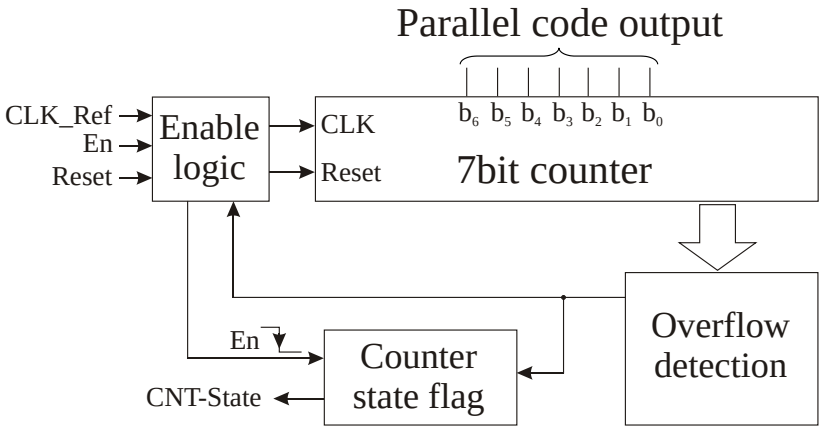


Figure 4.32: Schematic of the measurement logic

The counter is built with D type flip-flops with asynchronous clear and clock. The enable logic is a simple AND gate. When the *En* signal is asserted the reference clock signal reaches the counter. When the *En* is turned to *LOW* the clock signal will not pass through the AND gate. The *En* is directly controlled by the output of the comparator. The third input of the AND gate is driven by the overflow protection circuit. The role of the overflow protection logic is to detect the all ones state of the counter in the case of unexpected large negative corner frequency errors. If the counter reaches this state the overflow protection will act as an inhibition for the clock signal regardless of the comparator output.

The counter state circuit is used for storing a flag. The flag is asserted synchronously with the falling edge of the *En* signal or when the overflow protection is activated. The *CNT-state* signal is also used for communication with the exterior. This signal shows to an external logic that the counter has finished its cycle and the valid measurement data is available.

The *Reset* signal serves as an overall enable and is directly connected to the *Sw* signal in the analog front-end of the error prediction circuit. This signal is active *LOW*. It triggers the switches in the RC switch network and releases the counter to

increase its contents. This signal is inactive only during the measurement cycle and it can be activated once the measurement cycle is finished and the data has been read out.

4.3.6 The low pass filter opamp

The most important specifications of the low-pass filter opamp are regarding the frequency behavior, consumption and stability. The required performance in frequency is determined by the largest signal bandwidth that will be processed by the filter and the load capacitance. The largest guaranteed cutoff frequency is 6.4MHz. In order to maintain an acceptable level of peaking and distortion of the filter transfer function in practical designs, a rule of thumb sets the unity gain bandwidth of the opamp to be at least about 30 times larger than the maximum processed signal frequency [23]. From a simple calculation results that the minimum necessary unity-gain bandwidth is approximately 190MHz.

The circuit, connected in a feedback configuration, must be unconditionally stable; thus it requires a phase margin of around 60-65° for all conditions. Since the bandwidth should be maximized, this condition means that the lowest internal pole frequency should be sufficiently large to provide a good splitting with the dominant pole [4].

The maximum current consumption depends on the selected bandwidth of the filter. In order to improve the consumption of the entire filter the opamp should be switched to a lower bandwidth mode for smaller frequency settings. The power saving functionality is implemented using two identical opamps that are switched in parallel when operating at higher frequencies. The increase and decrease of the bandwidth is completely automated and the required digital control signal, *PMode*, is decoded from the programming word of the corner frequency. Simulations have shown that, in order to avoid the peaking of the magnitude response, the opamp should be switched in high frequency operation mode at the 3.2MHz nominal frequency setting. The opamp, that is switched off at lower frequencies, is separated from the signal path through transmission gates. Both the unit opamp cores share the same common mode feedback circuit.

The block diagram of the opamp is shown in Figure 4.33. The schematic of the opamp unit circuit is given in Figure 4.34. The chosen structure uses a bipolar input stage that helps maximizing gain and reducing the offset. The output stage is based on a folded cascode circuit. The folded cascode structure has been preferred to a Miller opamp due to its better potential for large bandwidths. Miller opamps have lower bandwidth due to stability requirements and compensation schemes [4][27].

The common mode voltages at the input and at the output of the circuit should be equal in order to facilitate the connection of the opamp in a cascade. The determination of the common mode voltage must be done by considering the maximum

signal swing and the biasing requirements of the transistors.

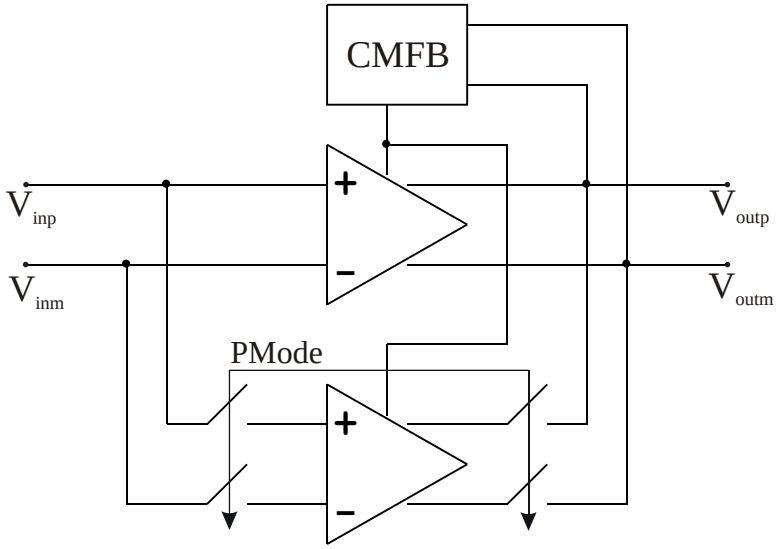


Figure 4.33: Block diagram of the opamp

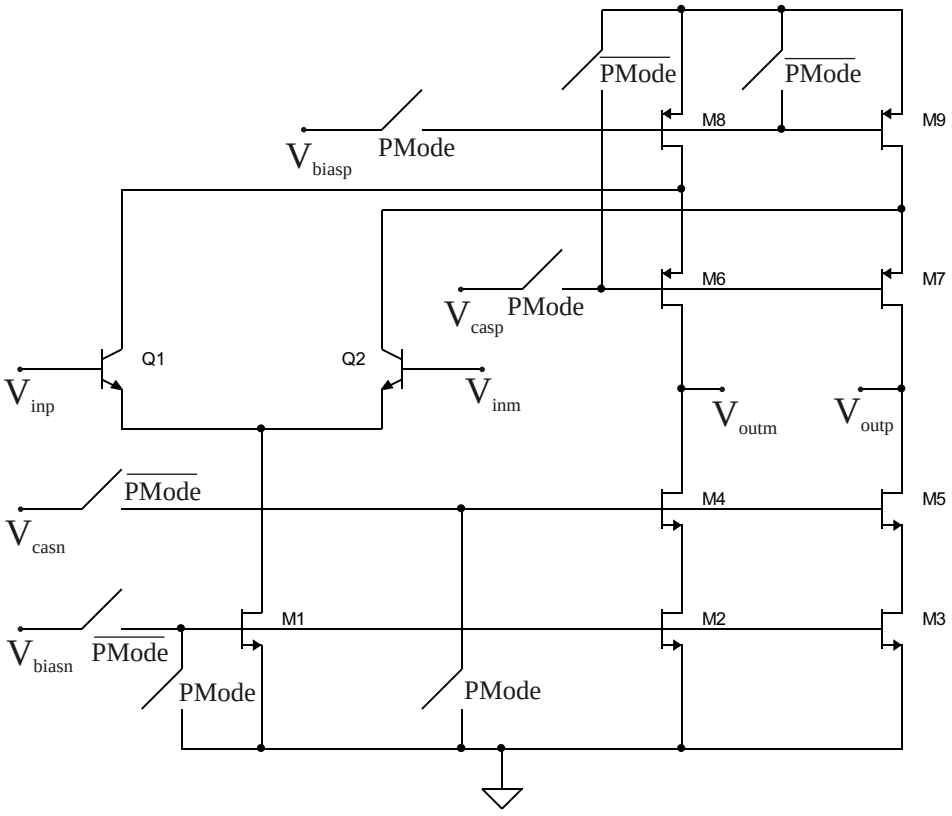


Figure 4.34: Schematic of the unit opamp

The worst case instantaneous voltage at the input should cover the peak signal value, the base-emitter voltage of the input transistors and the drain-source voltage of the n-channel current source bias of the differential pair. The drain source voltage of the current source must be determined with a margin for keeping the transistor in saturation even for large variations of the threshold voltage with temperature and process. If the overdrive voltage of this transistor is set to approximately 200mV the drain source voltage should be taken at least 300mV. The bias current of the differential stage is set to 200μA. The maximum simulated base-emitter voltage for this current is approximately 800mV. The peak input signal can be neglected here due to the high gain of the opamp. The minimum input common mode voltage can be written as follows:

$$V_{CMmin} = V_{BEmax} + V_{DSMbiasn} = 800mV + 300mV = 1.1V \tag{4.75}$$

The maximum common mode voltage is calculated at the output of the opamp. This should insure correct bias conditions for the p-channel current sources and the p-channel cascode transistors even when the output signal reaches its peak value. The maximum common mode voltage can be determined from the equation (4.76). In order to maximize the signal swing in the folded cascode output stage the common mode voltage can be set to half the supply voltage, this is 1.5V.

$$V_{CMmax} = V_{DD} - v_{peak} - V_{DSMbiasp} + V_{DSMcasp} = 2.1V \tag{4.76}$$

The common mode feedback circuit is implemented using a buffered resistive network to calculate the average value of the output signal. This average is then compared to a reference voltage by means of a difference amplifier. The resulting error voltage is gained up and used to regulate the p-channel current source in the folded cascode structure. The common mode feedback loop exhibits a gain above 100dB, its unity gain bandwidth is larger than the unity gain bandwidth of the differential opamp and it is compensated for a 65° phase margin. The schematic of the common mode feedback circuit is given in Figure 4.35.

Figure 4.36 gives the simulated frequency response of the opamp for the two different bandwidth settings. The opamp achieves a worst case unity-gain bandwidth of 160MHz for the low power mode and 290MHz for the high bandwidth mode. The DC gain is 68dB. The worst case phase margin is 63°, which insures unconditional stability. The consumption in the low power mode is approximately 500μA. This includes the common mode feedback. In high bandwidth mode the consumption is approximately doubled and reaches 950μA.

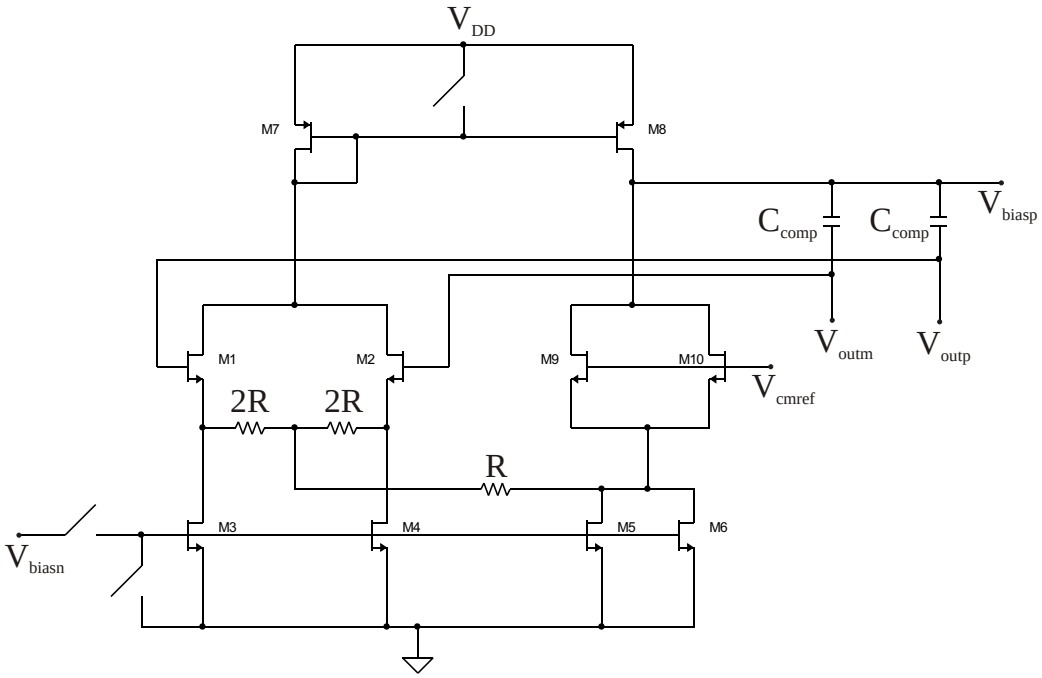


Figure 4.35: Schematic of the common mode feedback circuit

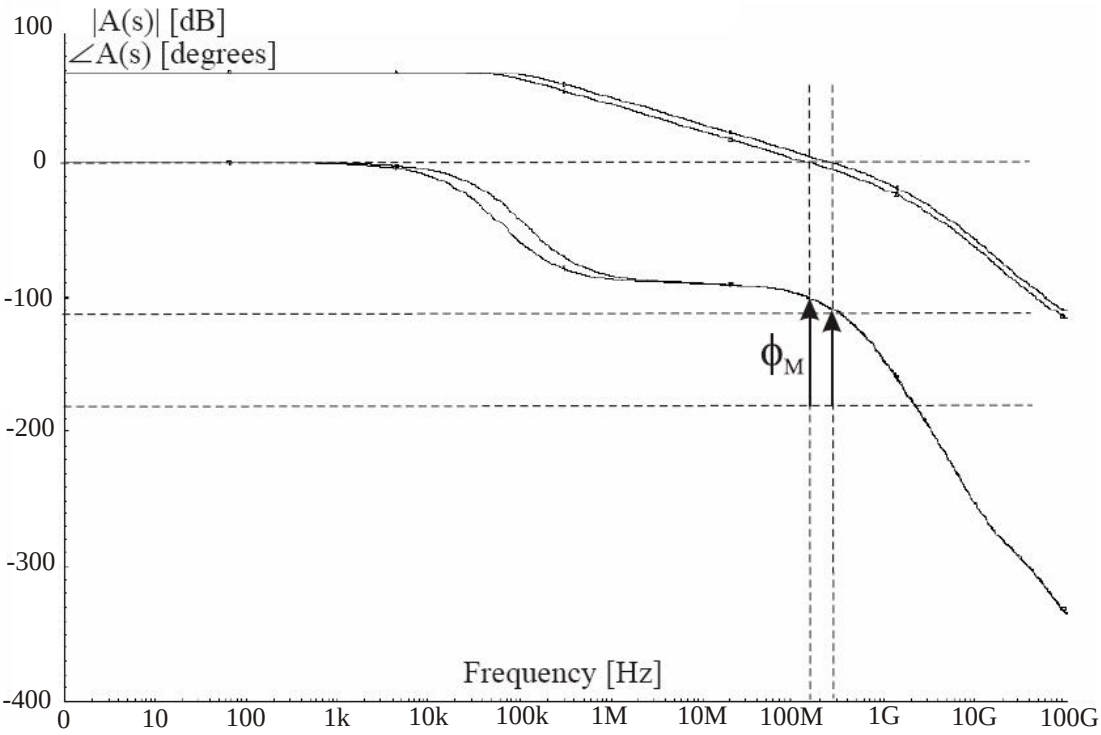


Figure 4.36: The simulated frequency response of the opamp

4.4 The variable gain amplifier

4.4.1 The VGA structure and the gain distribution

The variable gain amplifier is the second important building block of the proposed base band circuit. It is built using the same opamp as for the low-pass filter. The maximum input signal of the base-band circuit has been considered equal to 100mV peak to peak differential. In these conditions a usable VGA architecture, that minimizes the effects of the noise and the offset voltage, includes a fixed gain amplifier, followed by a programmable ladder attenuator and an output buffer. This architecture is suitable for low input signals. For larger than expected input signals clipping can occur and the signal spectrum could be distorted. Therefore the proposed VGA is only suitable for direct conversion architectures where the signal levels passing through the mixer stage are sufficiently low in order to avoid distortions. Other architectures with wider signal swing have been briefly presented in paragraph 3.4.

The specifications of the VGA have been given in paragraph 4.2.2 and are summarized here again for convenience. The most important requirements are concerning the variation range of the gain, the maximum input signal and the linearity. The variation range of the gain is 0dB to 79dB in 1dB steps. The worst case step error should not be worse than about 0.3dB. The VGA should maintain the linearity achieved by the filter having a third order intermodulation lower than -62dBm.

The first step in the design process is to determine the required number of control bits. This is defined based on the gain range, gain resolution and the number of necessary settings. A general requirement can be of the following form:

$$2^n \geq \frac{G_{max} - G_{min}}{G_{step}} \ , \tag{4.77}$$

where n is the required number of bits, G_{max} and G_{min} are the maximum and the minimum achievable gain and G_{step} is the gain step used for programming. Although theoretically the entire programming range of the gain could be covered by a single amplifier, in practice there are strong limitations in what is concerning the maximum gain achievable with an amplifier stage, others than purely technological restrictions. Since the gain is almost invariably set by some resistor or transistor ratio, a high gain means that this ratio will be very large and the components in it will exhibit an extreme spread. It has already been mentioned earlier that a large spread is not desired because it causes performance degradation in what is concerning either matching, noise and linearity. As a rule of thumb, the component ratio used in this work, that is setting the gain, should not be larger than 20, this is 26dB. In the characterization of the VGA this maximum gain of a stage will be noted $G_{max-stage}$. In this case the number of stages required to cover the programming range can be determined by dividing the length of the gain interval with the maximum allowed gain for each single stage:

$$Nr.stages = \frac{G_{max}}{G_{max-stage}} \tag{4.78}$$

It is important to notice that the minimum gain G_{min} does not appear in this equation. The reason for this is that gain values smaller than 0dB require rather attenuations than amplifications. Attenuation can be provided without additional energy from an active device; thus the smallest setting that can be regarded as proper gain is 0dB. As a consequence, G_{min} can be safely replaced by 0dB in the expression of the number of stages. For any distribution of the n control bits between the stages the following condition holds true:

$$\sum_{i=1}^{Nr.stages} n_i = n \ , \tag{4.79}$$

where n_i is the number of control bits assigned to the i^{th} amplifier stage. The condition above states that the sum of the control bits corresponding to every single gain stage must be equal to the total number of bits used for programming the VGA. A more careful analysis of the distribution problem leads to the obvious result that at least one of the stages should respect the minimum difference between consecutive gain settings equal to the required gain step of the entire amplifier, G_{step}. The general characterization of the VGA programming template assumes for simplicity that the first gain stage is associated with n_1 control bits, the second stage with n_2 bits and so on. Furthermore, it is assumed that the first stage exhibits the smallest gain difference between consecutive gain settings equal to G_{step}.

The observation regarding the replacement of G_{min} with 0dB can be extended for the entire amplifier. Since attenuation can be easily implemented, the main concern is the implementation of the gain in the range between 0dB and G_{max}. If the programming template also contains gain settings that are smaller than unity, the range in which the circuit must provide real gain decreases; thus the required number of bits, that control the gain and not the attenuations, will also decrease but the overall bit count for the entire VGA remains the same. It results that the required number of bits is associated strictly with the number of available settings, regardless of their distribution within the template.

The condition for programming the amplifier with the specified step can be derived by using a simple algorithm. The functional principle of this algorithm is presented in Figure 4.37.

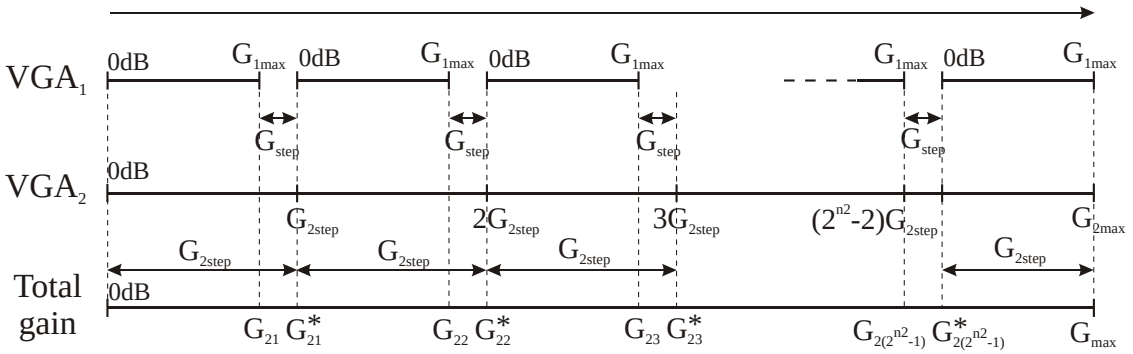


Figure 4.37: Representation of the proposed algorithm for defining the VGA programming template with a desired step

The gain of the first VGA stage is varied with the desired step, G_{step}. The maximum achievable gain corresponding to any stage is derived from the step size and the number of bits as follows:

$$G_{imax} = (2^{n_i} - 1)\, G_{istep} \tag{4.80}$$

According to this the maximum gain of the first VGA stage can be written:

$$G_{1max} = (2^{n_1} - 1)\, G_{step} \tag{4.81}$$

The total gain of the two stages is then $G_{21} = G_{1max}$. From the diagram in Figure 4.37 it can be seen that the next setting for the first stage is again 0dB. This means that the variation of the second stage gain must compensate for the necessary G_{step} difference. As a consequence, the step size of the second stage is:

$$G_{2step} = G_{1max} + G_{step} = (2^{n_1} - 1)\, G_{step} + G_{step} = 2^{n_1} \cdot G_{step} \tag{4.82}$$

The total gain of the two stages results:

$$G_{21}^{*} = 0dB + G_{2step} = 2^{n_1} \cdot G_{step} \tag{4.83}$$

Next the gain of the VGA1 is varied again with the desired step, while the gain of the second stage is held constant at G_{2step}. When the VGA1 reaches its maximum setting again, the second stage is switched to a gain equal to $2G_{2step}$. The total gain settings at the output will be:

$$\begin{cases} G_{22} = G_{1max} + G_{2step} = (2 \cdot 2^{n_1} - 1)\, G_{step} \\ G_{22}^{*} = 0dB + 2G_{2step} = 2 \cdot 2^{n_1} \cdot G_{step} \end{cases} \tag{4.84}$$

Similarly, the calculations can be repeated for the next cycle and it results:

$$\begin{cases} G_{23} = G_{1max} + 2G_{2step} = (3 \cdot 2^{n_1} - 1)\, G_{step} \\ G_{23}^{*} = 0dB + 3G_{2step} = 3 \cdot 2^{n_1} \cdot G_{step} \end{cases} \tag{4.85}$$

The algorithm is finished when both stages reach their maximum settings. The corresponding gain values are:

$$\begin{cases} G_{2(2^{n_2}-1)} = G_{1max} + (2^{n_2} - 2)\, G_{2step} = (2^{n_1+n_2} - 2^{n_1} - 1)\, G_{step} \\ G_{2(2^{n_2}-1)}^{*} = 0dB + G_{2max} = (2^{n_2} - 1)\, G_{2step} = 2^{n_1}\,(2^{n_2} - 1)\, G_{step} \end{cases} \tag{4.86}$$

Once the algorithm has been finished for the first two stages, it must be reiterated for VGA2 and VGA3. The result of a new iteration is the step size and settings of the third stage, G_{3step}. The maximum gain achievable with three stages results:

$$G_{3max-tot} = \left(2^{n_1+n_2+n_3} - 1\right) G_{step} \tag{4.87}$$

After an iteration is always necessary to also verify if the resulting maximum gain for a single stage is smaller than the imposed limit equal to A_{max}. The last iteration includes the two stages before the last in the chain. The reason for this is that the computed number of control bits usually offers some redundancies in the gain settings. Therefore, the gain of the last stage, noted with X, is always set to complement the sum of the maximum settings available in order to achieve exactly the required programming range. The results of the iterative algorithm are the numbers of the control bits associated with each amplifier stage. The gain settings can be computed by replacing the bit numbers in the algorithm equations. The general conditions that must be fulfilled by the control bits and the gain settings can be summarized as follows:

$$\begin{cases} n_1 + n_2 + n_3 + \cdots = n \quad , \quad n \in \mathbb{N}^{*} \\ [2^{n_1} - 1 + 2^{n_1}\,(2^{n_2} - 1) + 2^{n_1+n_2}\,(2^{n_3} - 1) + \cdots]\, G_{step} + X = G_{max} \\ G_{imax} \leq G_{max-stage} \quad , \quad i = \overline{1, Nr.stages} \end{cases} \tag{4.88}$$

The general algorithm for computing the gain programming template can be applied to the given specifications. The number of bits results to be $n = 7$, the minimum gain is 0dB while the maximum gain is 79dB. The amplifier should be programmed with $G_{step} = 1$dB. The maximum gain for a single stage is taken 24dB. This specification leads to a number of stages equal to 4. The system of equations (4.88) can be written in the particular case as follows:

$$\begin{cases} n_1 + n_2 + n_3 + n_4 = 7 \ , \quad n \in \mathbb{N}^* \\ \left[2^{n_1} - 1 + 2^{n_1}\left(2^{n_2} - 1\right) + 2^{n_1+n_2}\left(2^{n_3} - 1\right)\right] G_{step} + X = G_{max} \\ \left(2^{n_1} - 1\right) G_{step} \leq G_{max-stage} \\ 2^{n_1}\left(2^{n_2} - 1\right) G_{step} \leq G_{max-stage} \\ 2^{n_1+n_2}\left(2^{n_3} - 1\right) G_{step} \leq G_{max-stage} \\ X \leq G_{max-stage} \end{cases} \tag{4.89}$$

When the first equation in this system is closely analyzed from combinatorial point of view, it becomes obvious that there are only a very limited number of combinations possible for the bits allocated to different stages. These are given as follows:

$$\begin{cases} n_1 = 1 \ , \ n_2 = 2 \ , \ n_3 = 2 \ , \ n_4 = 2 \\ n_1 = 1 \ , \ n_2 = 1 \ , \ n_3 = 2 \ , \ n_4 = 3 \end{cases} \tag{4.90}$$

It is essential to notice that the number of possible combinations has been greatly reduced by the free interchange of the VGA stages. This means that the order of the stages in the amplifier chain can be freely changed, regardless of the number of bits associated with each single amplifier. Practically, it is equally feasible to associate a certain number of control bits with any stage. For example, the design is equally correct for the sets $(n_1 = 2, n_2 = 3, n_3 = 1, n_4 = 1)$ and $(n_1 = 1, n_2 = 3, n_3 = 1, n_4 = 2)$. In every setup it is only important to remember which stage has been associated with a unity gain step variation. The other bits will result accordingly from the calculations.

If the distribution of the control bits between the four stages is given by the first set in the system (4.90), it can be shown that the maximum gain of the second stage will be equal to 48dB. It is clear that this value is much higher than the imposed maximum gain of 24dB. Therefore, this distribution does not lead to good results. In the case of the second set the maximum gain of the third and the second stage will be 24dB and 32dB, respectively. The total achievable gain with the three amplifiers

would be then 63dB. As a consequence, the remaining gain X can be determined as follows:

$$X = G_{max} - G_{4max} - G_{3max} - G_{2max} = 79dB - 7dB - 24dB - 32dB = 16dB \quad (4.91)$$

Since the gain of the second stage is higher than the maximum 24dB and the maximum required gain for the first stage is only 16dB there is a possibility to transfer some of the gain requirements from the second to the first amplifier. This way both the first and the second amplifiers will have a maximum gain equal to 24dB.

One important issue arising from the high gains is the equivalent noise and distortion. A common practice to minimize the noise and distortion generated by an amplifier is to implement several gain stages interlaced with filter sections. Usually the high gain stages are connected early in the processing chain to take the benefits of the noise decrease. On the other hand, the intermodulation components generated by the high gain stages are increased by the gain of the last stages. It results that the order of the individual amplifiers must be found as a compromise between distortion and noise. In the case of the variable gain amplifier proposed in this work the wide range of the required gain settings lead to the necessity to implement four gain stages. These are interlaced with the filter biquads as shown in Figure 4.38. The proposed gain settings and the control bit distribution are also shown on the block diagram.

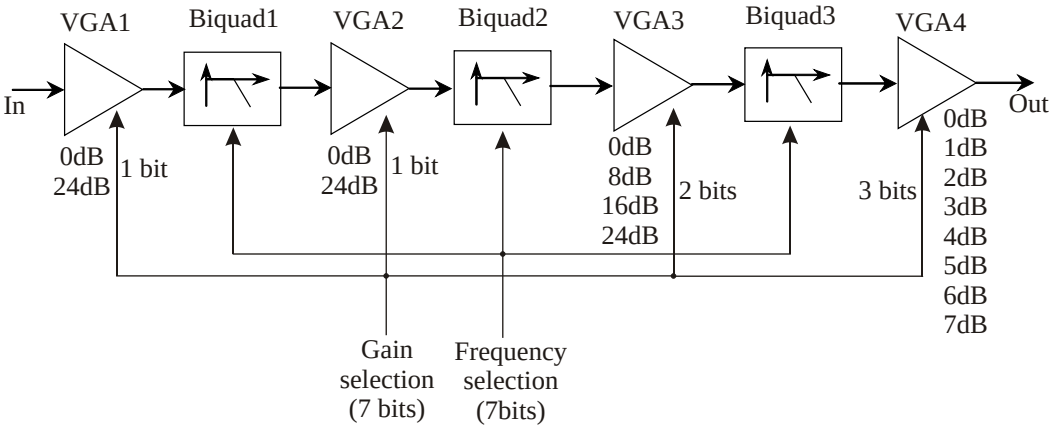


Figure 4.38: The filter-VGA interlacing and the proposed gain distribution

The general equation that defines each gain setting can be written as follows:

$$G_{total} = \overline{b_6} \cdot 24dB + \overline{b_5} \cdot 24dB + (\overline{b_4} \cdot 2^1 + \overline{b_3} \cdot 2^0) \cdot 8dB + \\ + (\overline{b_2} \cdot 2^2 + \overline{b_1} \cdot 2^1 + \overline{b_0} \cdot 2^0) \cdot 1dB \quad (4.92)$$

In this equation the line over the codes indicates that the bits should be inverted. The additional inversion is necessary as the significance of the bits is rather attenuation than a gain in this specific case. For example, if the desired gain setting is 47dB, this can be written as 0dB+24dB+16dB+7dB. In this case the corresponding digital control word that sets this gain is 1001000. A detailed correspondence between the programming code and the possible gain settings are given in Appendix D. The table also presents the composition of every gain setting. This is particularly useful in simulations because it gives an overview on the gain step error regularities caused by switching the gain of each amplifier stage. The 7 bit programming word is internally decoded in order to obtain the correct control signals for all the four stages.

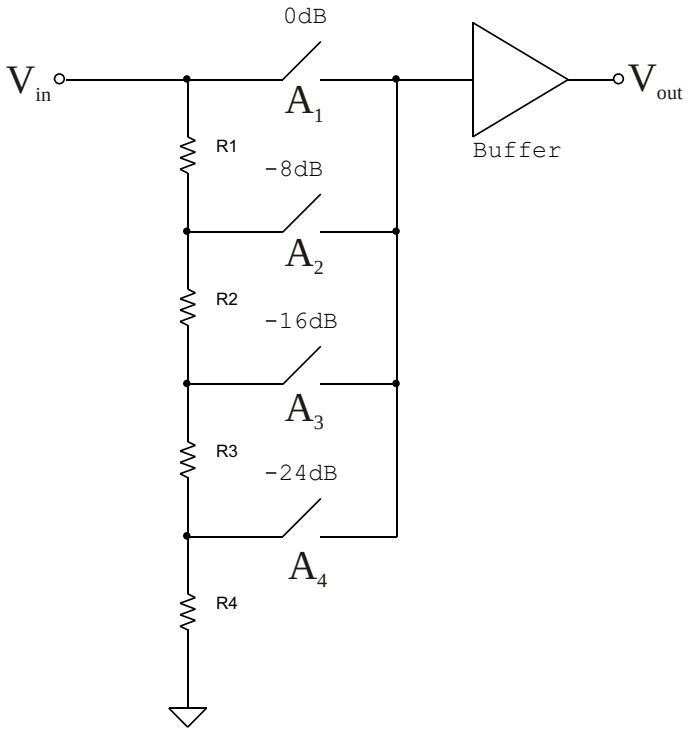


Figure 4.39: The schematic of the resistive divider

4.4.2 The voltage dividers and the sizing equation

The voltage dividers are implemented with a resistive ladder. The choice of the attenuation is controlled by switches connected to different taps of the ladder. The circuit is using the same principle as a flash ADC. As example, the divider of the third VGA stage is presented. This amplifier stage is capable of providing 0dB, 8dB, 16dB and 24dB gain. The schematic of the resistive divider is presented in Figure 4.39. The attenuations corresponding to each tap of the ladder are noted A_1, A_2, A_3 and A_4. At the A_1 setting the attenuation is 0dB and the circuit operates as

a simple voltage follower. The attenuations can be expressed as functions of the resistances in the ladder.

$$\begin{cases} A_4 = \dfrac{R_4}{R_1 + R_2 + R_3 + R_4} \\ A_3 = \dfrac{R_4 + R_3}{R_1 + R_2 + R_3 + R_4}, \\ A_2 = \dfrac{R_4 + R_3 + R_2}{R_1 + R_2 + R_3 + R_4} \end{cases} \tag{4.93}$$

where $A_4 = -24dB$, $A_3 = -16dB$ and $A_2 = -8dB$. After rearranging the terms the system becomes:

$$\begin{cases} R_1 A_4 + R_2 A_4 + R_3 A_4 + R_4 (A_4 - 1) = 0 \\ R_1 A_3 + R_2 A_3 + R_3 (A_3 - 1) + R_4 (A_3 - 1) = 0 \\ R_1 A_2 + R_2 (A_2 - 1) + R_3 (A_2 - 1) + R_4 (A_2 - 1) = 0 \end{cases} \tag{4.94}$$

These equations can be written in matrix form as follows:

$$[R_1\ R_2\ R_3] \cdot \begin{bmatrix} A_4 & A_3 & A_2 \\ A_4 & A_3 & A_2 - 1 \\ A_4 & A_3 - 1 & A_2 - 1 \end{bmatrix} = R_4 \cdot \begin{bmatrix} 1 - A_4 \\ 1 - A_3 \\ 1 - A_2 \end{bmatrix} \tag{4.95}$$

The sizing of the components is done by solving the system of linear equations with the variables R_1, R_2, R_3 and R_4. From the system in (4.93) it can be seen that there are four variables in only three equations. As a consequence, the resistance R_4 is chosen as a parameter.

$$[R_1\ R_2\ R_3] = R_4 \cdot \begin{bmatrix} 1 - A_4 \\ 1 - A_3 \\ 1 - A_2 \end{bmatrix} \cdot \begin{bmatrix} A_4 & A_3 & A_2 \\ A_4 & A_3 & A_2 - 1 \\ A_4 & A_3 - 1 & A_2 - 1 \end{bmatrix}^{-1} \tag{4.96}$$

The calculated resistance values, corresponding to the specified gain settings, are given in equation (4.97).

$$\begin{cases} R_1 = 47.7k\Omega \\ R_2 = 19k\Omega \\ R_3 = 7.56k\Omega \\ R_4 = 5k\Omega \end{cases} \tag{4.97}$$

The fixed gain amplifier is implemented using the opamp from the low pass filter design, connected in a resistive negative feedback configuration. In the layout a special consideration has been taken on the matching of the resistors. They have been laid out in a unit resistor array with diagonal symmetry in order to maximize matching and to avoid large values for the gain step error [26].

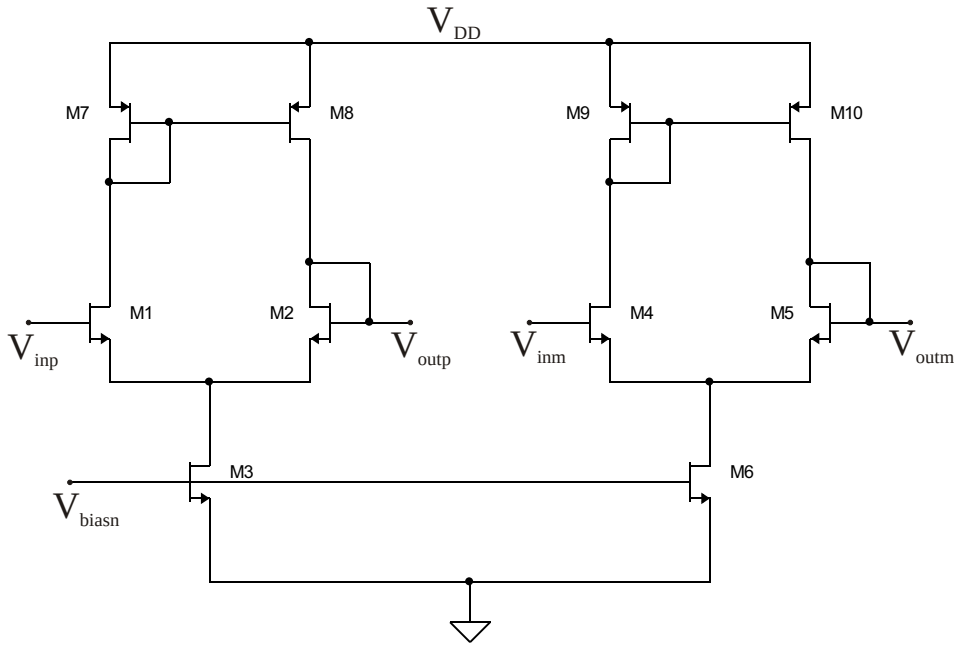


Figure 4.40: The schematic of the output buffer

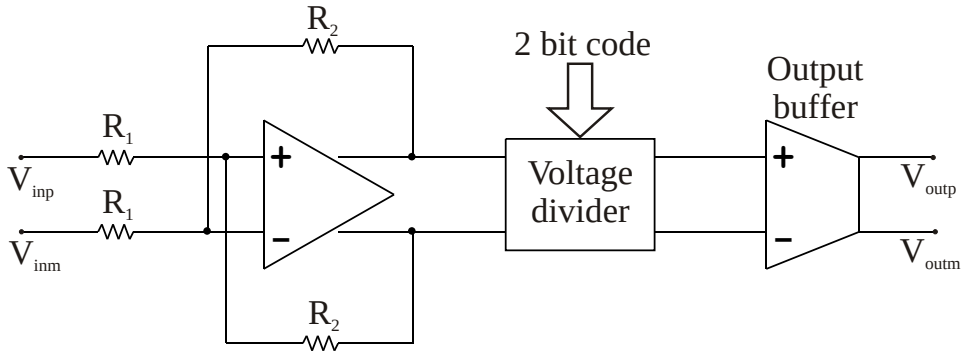


Figure 4.41: Complete schematic of the third VGA stage

The output buffer is a simple differential stage with current mirror load and a unity gain feedback [4]. A separate buffer is placed on each signal path. The main purpose of the buffer is to provide a very large input impedance and to decrease the current losses through the switches in the divider. By decreasing the leakage, the precision of the ladder is enhanced and the gain step errors are significantly reduced.

The other important role of the buffer is that it provides a low output resistance and drives the following stages without lowering the bandwidth. The schematic of the output buffer is given in Figure 4.40. Figure 4.41 gives the complete schematic of the third VGA stage.

4.5 System aspects of the low pass filter and VGA design

The proposed base band circuit has been implemented on a test chip and fabricated in a 0.35μm BiCMOS process. In order to operate properly as a standalone system, the low pass filter and the variable gain amplifier need several additional circuits. These are the reference circuit, that provides all the voltages and currents necessary for correctly biasing the transistors, the decode logic of the programming code and the digital interface circuit, which facilitates the communication between the system and the outer world. The complete block diagram of the proposed base band circuit is given in Figure 4.42. In the following paragraphs each of the additional circuits will be described in detail.

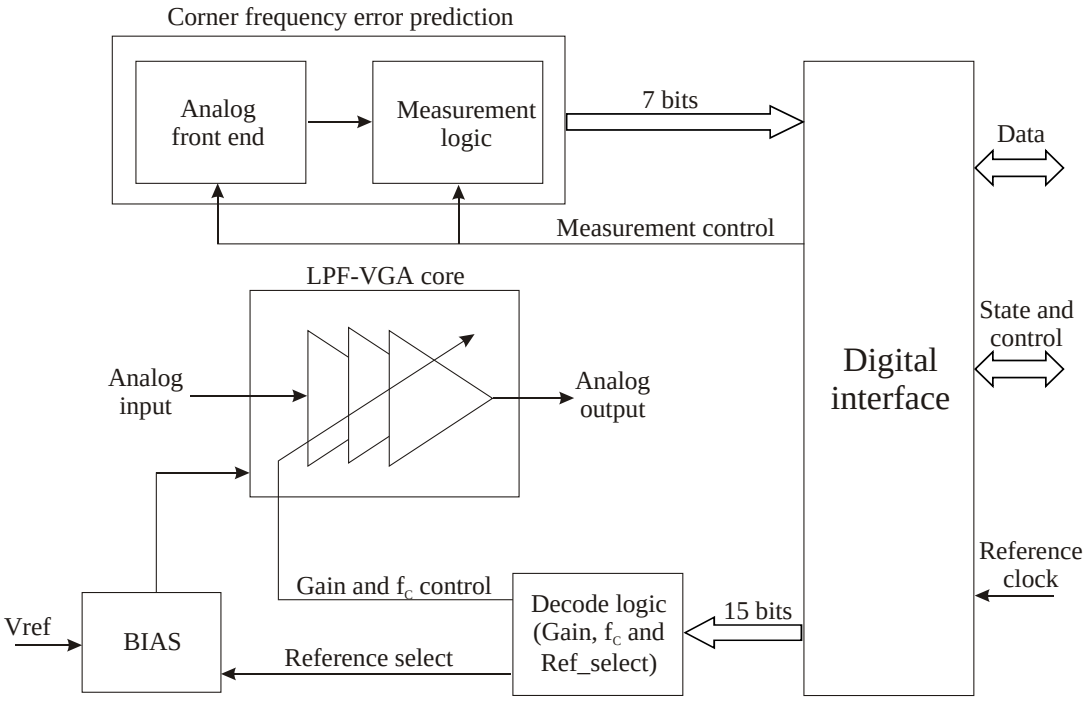


Figure 4.42: The block diagram of the proposed base band circuit

4.5.1 The bias circuit

The bias block is built around a band gap reference. This circuit provides a stable voltage that is approximately independent on temperature and supply voltage. This

voltage is stabilized using a negative feedback loop and a proportional current is fed into a low voltage cascode current mirror that generates all the required voltages. For an improved reliability in testing the bias circuit has been doubled. One part is using the stable voltage generated by the band gap reference and the other part allows an external reference voltage to be fed into the test chip. The part of the bias circuit that is not used can be switched off. The selection between the internal or the external reference voltages can be done with the *Ref-select* bit in the programming code of the circuit.

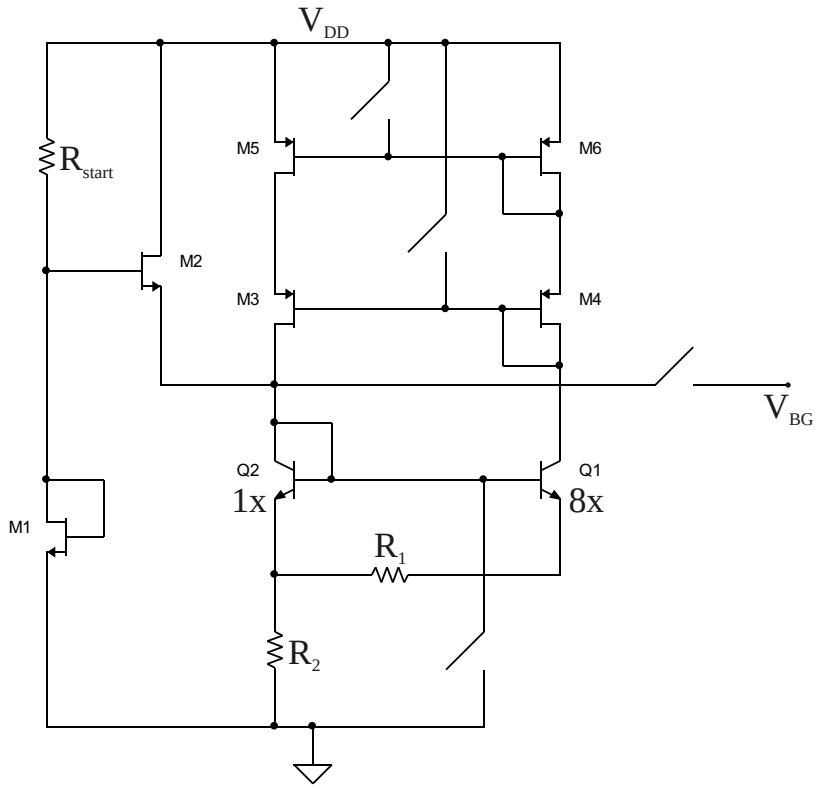


Figure 4.43: The schematic of the band gap reference with power down

The schematic of the band gap reference is given in Figure 4.43. The PTAT (Proportional To Absolute Temperature) reference is implemented with a bipolar Widlar current mirror [4]. The supply voltage independence is insured by the positive feedback and the bootstrap mechanism. For an enhanced precision of the bootstrap loop a cascode current mirror is employed. The purpose of the start-up circuit is to improve the convergence of the reference to a non-zero bias point. Once the currents and the voltages have moved away from the origin the bias circuit is deactivated and it does not influence the functionality of the circuit.

The power down functionality of the circuit is used to switch off the reference whenever the *Ref-select* bit in the programming code specifies an external reference voltage. The half circuit that is not used is switched off and separated from the

outputs with transmission gates. The current stabilization loop is compensated for a near 60° phase margin in order to avoid possible oscillations of the reference voltages. The circuit generates the V_{biasn}, V_{casn} and V_{casp} voltages required for biasing the transistors in the opamps. Additionally the 1.5V V_{cmref} voltage is provided to the inputs of each common mode feedback amplifier.

4.5.2 The digital interface

The digital interface is used for communication with the exterior. Practically all the digital information required by a correct functionality of the filter, of the variable gain amplifier and of the error prediction system are handled by this logic. The circuit consists of two distinct parts. The state logic is responsible for acquiring data from the error prediction system and for transmitting this data by request toward the exterior. The control logic is responsible reading in the programming information of the corner frequency, the gain and the bias reference voltage to be used. The following sections give a detailed overview on the state logic, the control logic and their functionality.

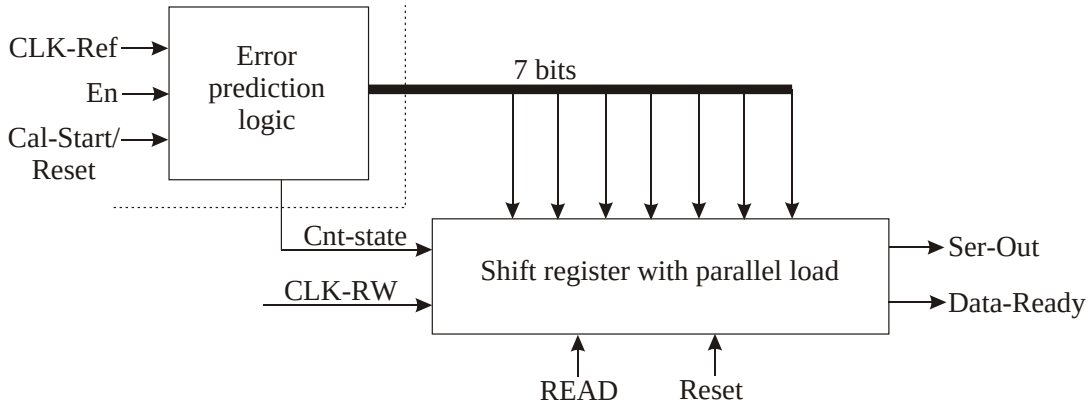


Figure 4.44: Block diagram of the state logic

- **The state logic**

The state logic is used to gather the data from the error measurement system and to provide a suitable interfacing to an external logic in order to allow a correct data transfer. The block diagram of the state logic is given in Figure 4.44. The signals from this block diagram have the following significance:

- *CLK-Ref* - it is the 26 MHz reference clock signal;
- *CLK-RW* - this is the clock signal used by all the data operation toward the exterior. Its frequency can be any value that can be generated by the external logic. Practically this signal also can be a series of clock pulses without a certain frequency and it works as a pushbutton.

- *En* - this signal enables the reference clock of the measurement logic during the measurement sequence. It is controlled by the output of the comparator in the analog measurement circuit;

- *Cal-Start* - this is the start calibration signal that toggles the switches from the analog part of the error measurement system and gives the signal that a measurement sequence has been started. Internally this signal is used as the *Reset* signal of the counter. During the period when the counter waits for a calibration startup signal its *Reset* is active and in spite of the clock signal the code is kept at all zeros. Similarly, the parallel to serial converter is initialized with an all zero state;

- *CNT-State* - this signal is the internal version of the *En* signal. While the counter increases its code the *CNT-State* signal is in a logic low state. On the falling edge of the *En* signal the output of an internal flip-flop is asserted. This means that the counting has been finished and the contents of the counter are available at its 7 bit parallel output. It can also mean that an overflow of the counter has happened.The overflow protection has been implemented as a precaution against measuring incorrect error codes in the case of unforeseen events;

- *Ser-Out* - it is the serial output of the status logic that provides the serial measurement code toward the exterior;

- *Reset* - is the equivalent of the *Cal-Start* signal and it keeps the shift register in a zero state during the wait period. It is deactivated when the measurement sequence starts;

- *DATA-Ready* - this signal warns that the serial measurement data is available in the shift register;

- *READ* - this is the signal that forces the register to send the serial data toward the exterior through the *Ser-Out* terminal.

The functionality of the circuit is as follows: the counter and the shift register are forced in a zero state by the *Cal-Start* and *Reset* signals. At this stage both circuits wait for the beginning of the measurement sequence and they are initialized with an all zero state. When the *Cal-Start* signal is deactivated the counter and the register are released. The counter will begin counting with the clock cycle corresponding to the 26MHz reference clock signal, *CLK-Ref*. When the capacitor in the analog part of the measurement circuit exhibits a zero voltage drop the comparator will deactivate the *En* signal and the counter receives no more clock. On the falling edge of *En*, the *CNT-state* signal is asserted. The assertion of *CNT-state* causes the read-write clock, *CLK-RW*, to be enabled and the contents of the counter are written in the cells of the register. In the mean time, on the same clock edge, an internal flip-flop is asserted meaning that the data is available to be read at the serial output. The assertion of the *DATA-Ready* signal warns the external logic that the data can be read by request. When the external logic considers, it initializes a

read sequence by asserting the *READ* signal. When the *READ* signal is asserted, the register starts shifting its contents, synchronized with the read-write clock. In the seven clock periods following the activation of the *READ* signal the external logic can download the serial error code from the register. The first downloaded bit is the most significant bit of the error code. After the code has been read out the external logic may activate the *Reset* signal, bringing the logic in a zero state and powering down the comparator. At this stage the measurement cycle has been finished. The logic diagram of the read sequence is given in Figure 4.45.

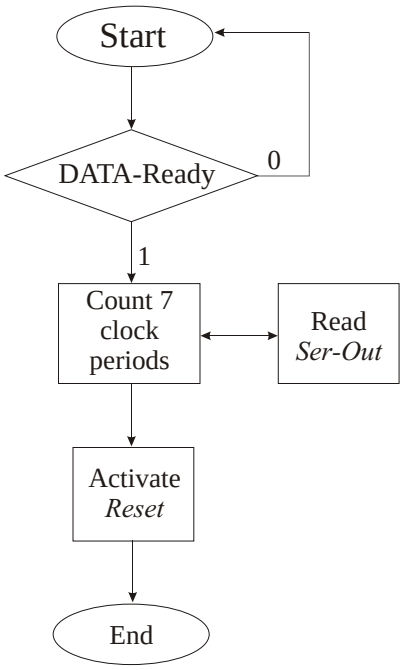


Figure 4.45: The logic diagram of the read sequence

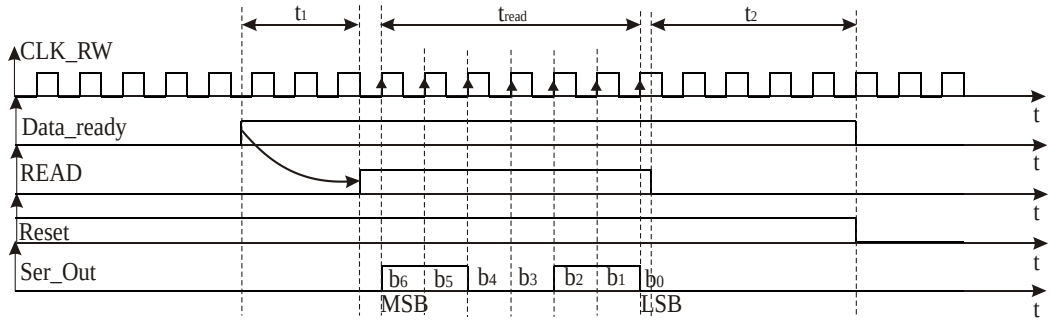


Figure 4.46: The timing and signal conditioning during the read cycle

An important aspect of the read sequence is the signal timing and the signal conditioning. The timing diagram in Figure 4.46 gives the activation order for different signals during the read-out sequence.

When the 7 bit data is available in the output shift register the status logic asserts the *DATA-Ready* signal. This signal should be scanned by the external logic. When the external logic senses an asserted *DATA-Ready* it can assert the *READ* signal which corresponds to a data request. The *READ* signal can be asserted immediately after sensing *DATA-Ready* or after an arbitrary delay. In the timing diagram this delay has been marked t_1.

The assertion of the *READ* signal changes the operation mode of the parallel to serial converter from parallel loading to serial shifting. This means that on the immediately following positive *CLK-RW* edge the register will begin shifting the data toward the exterior. From this point exactly 7 clock periods must be counted. After the seventh occurrence of a positive edge all the 7 data bits have been shifted through the serial output. After the seventh positive front the external logic can deactivate the *READ* signal. This signal can be also deactivated with some delay but the data bits read after the seventh clock have no significance. The *Reset* signal, active on *LOW*, can be activated immediately after the read cycle has been finished or with a delay marked t_2. The consequences of the active *Reset* signal are the return of the entire state logic to an all zero state and the power down of the comparator from the analog part of the measurement circuit. The timing diagram also shows the transferred data bits. In the example from Figure 4.46 the code 1100110 has been read out.

- **The control logic**

The control logic is used to store all the digital data required by the programming of the low pass filter and the variable gain amplifier. The structure of the control logic allows the new data to be written in the internal register any time when an external logic initializes an update sequence. The data transfer is serial and is controlled by a similar handshake mechanism as in the case of the state logic. The block diagram of the control logic is given in Figure 4.47.

The significance of the signals from the block diagram is:

- *CLK-RW* - has the same significance as for the state logic;

- *WRITE* - this signal is used by the external logic to initiate a programming sequence of the filter and the VGA. The assertion of the *WRITE* signal is internally memorized in a flip-flop. Practically this signal enables the clock signal to get through to the shift register. When deactivated, it causes the serial to parallel converter to perform a parallel data transfer to the control register;

- *Ser-In* - this is the serial data input of the control logic used to transfer the programming code from the external to the internal logic;

- *Gain select* - it is the 7 bit parallel control word for the variable gain amplifier;

- *Frequency select* - it is the 7 bit control word for the filter corner frequency;

- *Reference select* - this signal gives the option to select either the internal band gap reference or an external reference voltage. The reference circuit is responsible for generating all the necessary DC voltages required for a correct operation of the filter and the VGA.

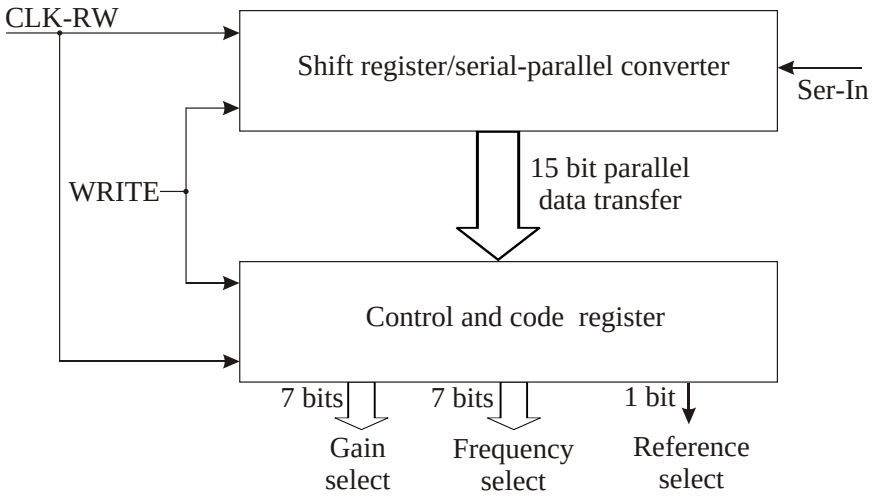


Figure 4.47: Block diagram of the control logic

The operation of the control logic is as follows: the circuit receives a *CLK-RW* clock signal which is internally disabled until a programming sequence is started. A programming sequence can be initialized any time when the external logic asserts the *WRITE* signal. At the first ascending front of the reference clock the *WRITE* signal is memorized in a flip flop. The *WRITE* signal will enable the reference clock to pass toward the shift register and will disable the clock of the control register. The external logic will send the programming code on a serial input to the shift register. When all the bits of the programming code have been transferred, the external logic may deactivate the *WRITE* signal. At this moment the internal flip-flop is cleared and the clock of the shift register is disabled. Practically the serial to parallel converter will hold its data. In the mean time the clock signal of the control register is enabled and on the first ascending edge of the clock the data will be transferred to the control register. The data will be held by the control register until a new write sequence is initiated by the external logic. The logic diagram of the read sequence is given in Figure 4.48.

The corresponding timing and signal conditioning diagram is presented in Figure 4.49. The characteristics of the *CLK-RW* signal are the same as for the read cycle. The external logic must enable the *WRITE* signal each time the write cycle is started. Practically the assertion of the *WRITE* signal causes a flip-flop to be tog-

gled and the clock signal of the serial to parallel converter to be internally enabled. This allows the data bits to be written to the circuit through the serial input.

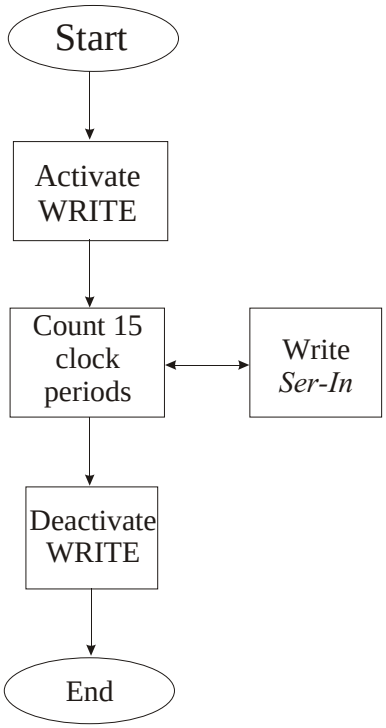


Figure 4.48: Logic diagram of the write sequence

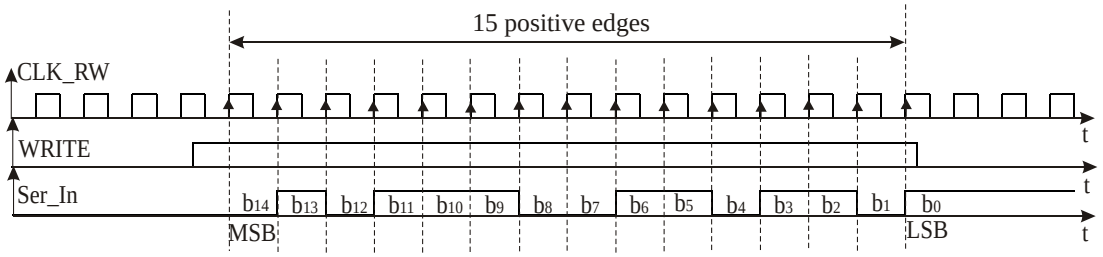


Figure 4.49: The timing and signal conditioning diagram of the write sequence

After the assertion of the *WRITE* signal exactly 15 positive clock edges must be counted, corresponding to the 15 data bits that must be written. The external logic should always write the entire 15 bits, although only some of these may need update. After 15 clock edges the *WRITE* signal can be deactivated. This will cause the clock of the serial to parallel converter to be internally disabled. Simultaneously the clock signal of the control register is enabled and the written data is transferred to the control register which drives directly the decoder circuit. The first data bit

to be written through the serial input is the MSB of the programming code. The timing diagram shows the code 010111001101101 written to the circuit.

An alternative programming scenario, that highlights the changes of the data bits at the output of the external programming logic and the corresponding changes of the *Ser-In* terminal, is given in Figure 4.50. It can be seen that the data is shifted into the serial to parallel converter synchronized with the positive clock edges. The *Ser-In* signal reflects the state of the input buffer register and not the data to be changed by the external logic. It is also of importance that the clock edges appear not necessarily with a fixed period and they can be triggered whenever required.

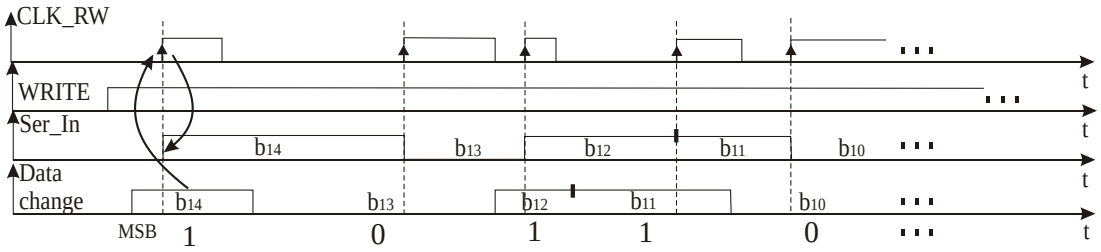


Figure 4.50: Alternative timing of the write sequence

The timing that corresponds to this diagram is as follows:

- first the write signal is activated in order to enable the programming procedure
- the data bit is set by the external logic to the wanted value (*Data-change*)
- when the data bit is considered stabilized, the value is latched into the buffer register with a positive clock edge. This bit will be held by the first flip-flop in the register until another clock edge is given. This means that the data can be safely changed without affecting the contents of the input register. The change can occur, for example, at the falling edge of the clock signal, but this is not a strict requirement
- the last two steps should be repeated until all the 15 bits have been written.

4.6 Conclusions

In this chapter a fully programmable base-band circuit has been proposed. The circuit is suitable for application in direct conversion or multi-port receivers, that employ base band or low-IF sampling. The filter section addresses the typical problems regarding the selectivity of the receiver. Its main purpose is to attenuate the blocking components and reduce the dynamic range requirements of the data converter. Additionally, it attenuates the aliasing components of the wanted signal. The most important feature of the filter, its wide band programmability, is imposed

by the software defined radio concept. The flexibility together with a power saving functionality and low consumption achieved by the design makes it suitable for channel filtering in mobile receivers where battery life is of concern.

An important issue addressed by the low pass filter design is the precision of the corner frequency. Channel select filtering usually introduces stringent requirements on the -3dB corner frequency precision. Since component tolerances and temperature variations typically cause an up to 50% corner frequency error, a performant tuning mechanism is required that reduces this error below 1-2%. In the case of multi-mode receivers the error correction functionality should be maintained over the entire programming range. The proposed error prediction circuit features a time constant measurement circuit capable of predicting the on chip RC time constant error. The provided digital code is then mapped into a look-up table and the expected corner frequency error can be identified. This procedure allows the implementation of a correction mechanism that does not depend on the programming range of the frequency parameters.

The second important building block of the base band circuit is a variable gain amplifier with wide dynamic range of the gain settings. The achieved range of variation is between 0dB and 79dB with 1dB steps. The VGA and the low pass filter stages have been interlaced in order to improve the noise figure of the circuit. The purpose of the VGA implementation is to provide support for an automated gain control algorithm whose measurement and comparison section is implemented in the digital domain.

The support for a correct operation of the filter and the VGA is offered by additional circuitry that facilitates the generation of bias voltages and implements the interface intended for communication with external circuits. These helper circuits allowed the proposed filter and VGA design to be implemented as a standalone system on a test chip.

The proposed base band circuit solves the problems typically arising from sensitivity and selectivity requirements of wireless receivers. The wide range flexibility adapts the classical filter and amplifier implementations to the need of the software defined radio concept and the requirements of modern multi-mode receivers.

Although the selectivity and sensitivity problems have been addressed, there is another very important aspect regarding a complete base band circuit. Since the signal is sampled in the baseband, a proper operation of the receiver requires the DC component to be suppressed. If this condition is not fulfilled the DC offset is gained by the VGA and could easily saturate the input stage of the ADC. Unfortunately the DC offset cannot be eliminated with simple methods such as capacitive coupling due to the low limits of the frequency range (200kHz for GSM). Due to this fact a more sophisticated offset correction circuit is required that compensates the static offset introduces by the component mismatches and the dynamic offset caused by

phenomena such as self mixing and substrate leakage.

The most important original contributions introduced by the author in this chapter are the possible developments of the classical RC switching techniques in order to obtain a wide-band programming template, the error prediction system, a generalized VGA design algorithm and the interface logic. The programming template has been developed based on classic elements of auto tuning that have been adapted to the needs of wide band programmability. The design of the frequency programming network has been done with considerations on noise, silicon area and simplicity. The error prediction system is also based on the simple principle of charging a capacitance through a resistance. This principle has been enhanced and used in order to provide the necessary support for an efficient frequency error correction algorithm that complies with the required precision for channel selection. The proposed VGA design algorithm supports a high degree of generality and can be successfully applied to any VGA with a given gain variation range and gain step. The interface logic, that facilitates the programming of the circuit and the download of the predicted error code, is based on a bidirectional transmit by request principle and a handshake mechanism that forces the circuit in the desired operation mode.

Chapter 5

The Experimental Prototype, Simulations and Measurement Results

This chapter provides some layout considerations, simulations and measurement results for the base-band circuit proposed in the previous chapter. The provided simulation and measurement results are meant to emphasize the behavior of the circuit in what is concerning the main specifications given in paragraph 4.2. This section ends with some conclusions on the measured performance in comparison to the simulated parameters.

5.1 Layout considerations

The proposed base-band circuit has been laied out and fabricated with a 0.35μm four metal layer BiCMOS process by Atmel. The silicon area required by the analog part of the circuit is approximately 1.9mm x 0.9mm from which a large part is taken by the capacitor arrays used for programming the low pass filter. The area occupied by the digital interface and the measurement logic is significantly lower. The total layout size of the test chip is a standard 2.5mm x 2.5mm set by the fabrication process. The circuit has been encapsulated in a standard PLCC44 package and operates with a single 3V supply voltage. The expected statical consumption of the circuit is around 36mW for the high frequency operation mode of the filter and 27mW for the lower corner frequencies. The pins are designed to operate with standard 3V CMOS interfaces. All the resistors and the capacitors in the circuit have been laied out as unit arrays in order to improve the symmetry of the differential sections.

In the layout a special consideration has been taken on the antenna effects. An ESD protection of the transistors, required by the employed process, implies connecting reversely biased antenna diodes to each transistor gate where also large strips of metal are present. The antenna diodes provide over voltage protection in the fabrication process, where statical charge could accumulate on the metal surface

and a punch through of the transistors could occur. The antenna diodes do not influence the functionality of the circuit.

The layout of the test chip is given in Figure 5.1.

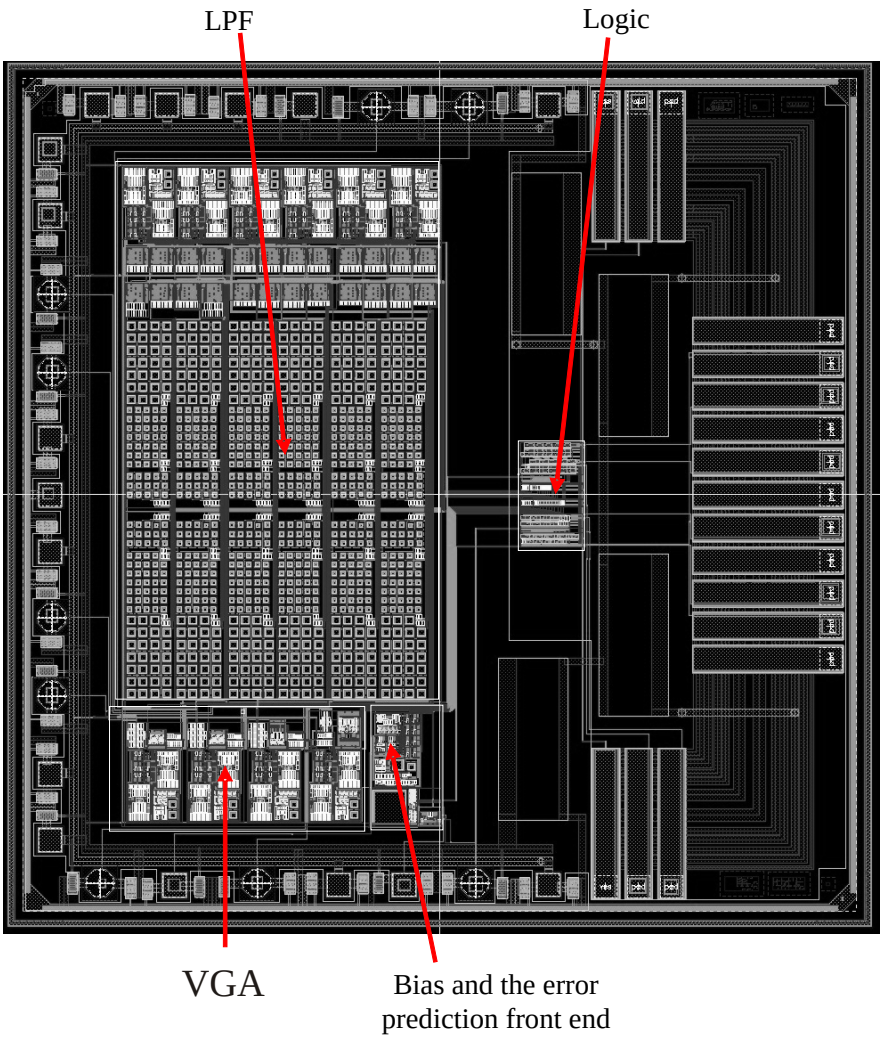


Figure 5.1: The complete layout of the fabricated testchip

5.2 Simulation results

- **The frequency response**

One of the most important simulation and measurement results is concerning the frequency behavior of the proposed circuit. Here the emphasis lays on the selectivity of the low pass filter rather than on the frequency response of the VGA. The simulated bandwidth of the VGA is sufficiently large in order to offer a flat magnitude response in the filter pass band.

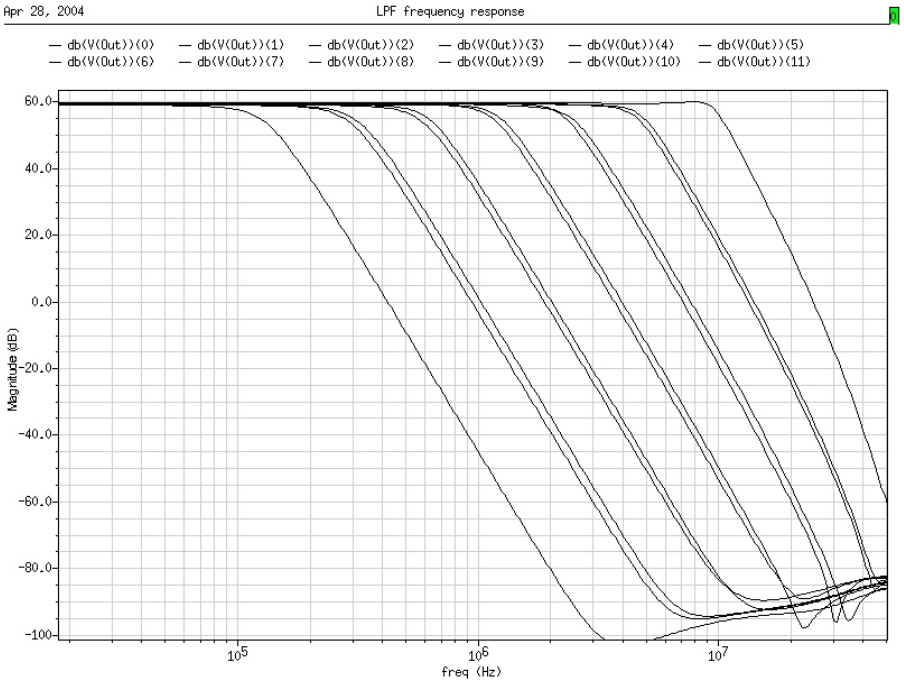


Figure 5.2: The simulated magnitude response of the circuit for the limits of the raw programming template

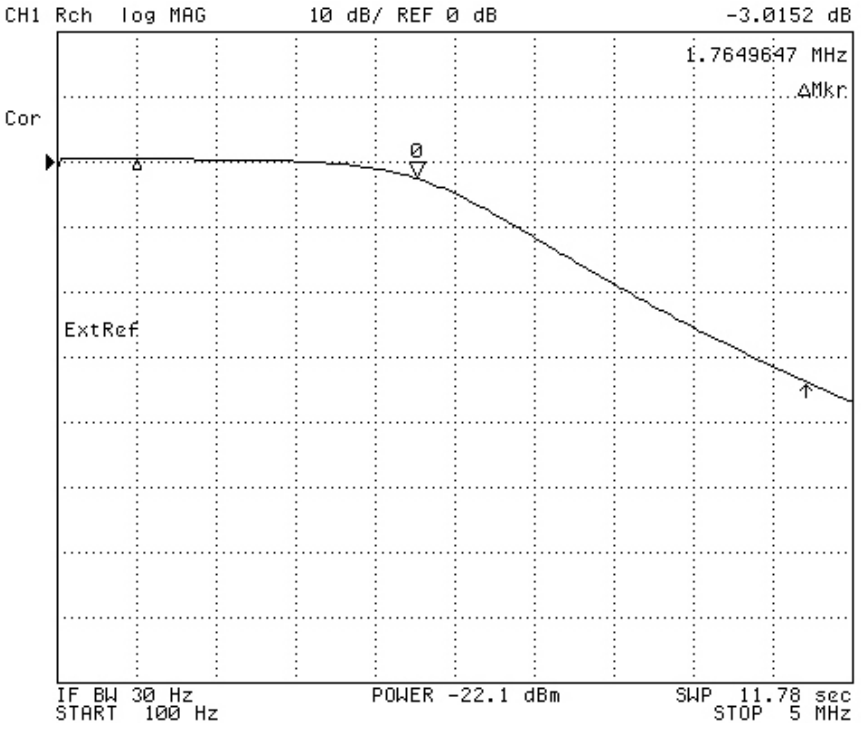


Figure 5.3: The measured magnitude response of the base band circuit

Figure 5.2 shows the simulated magnitude response of the circuit for the limits

of the raw programming template. The simulations have been performed on the parasitic extracted circuit where the gain of the variable gain amplifier has been set to 60dB. From the figure it can be seen that the simulated corner frequency programming range corresponds to the specifications in nominal conditions (27°C and nominal process corners). The functionality of the circuit has been verified by measurement.

The measured magnitude response is given in Figure 5.3. The response has been taken for a 2.285MHz corner frequency and a 0dB VGA gain setting. The reference frequency on the network analyzer was set to 500kHz which must be summed with the measured 1.765MHz measurement. The measured in-band gain is 0.22dB. In the measurements there is a systematic 2% error in the real corner frequencies compared to the simulated values. This is also confirmed by the corner frequency error prediction circuit.

The simulation in Figure 5.4 shows the magnitude response of the filter in the ideal case, for 60°C and a slow process corner and the corrected response. For the simulation the predicted percent error has been simulated and the code has been used to apply the correction. The corner frequency error has been reduced from -29% to approximately 1%. The simulations have been repeated several times for different process corner-temperature combinations. The simulated precision of the prediction system is approximately 2%.

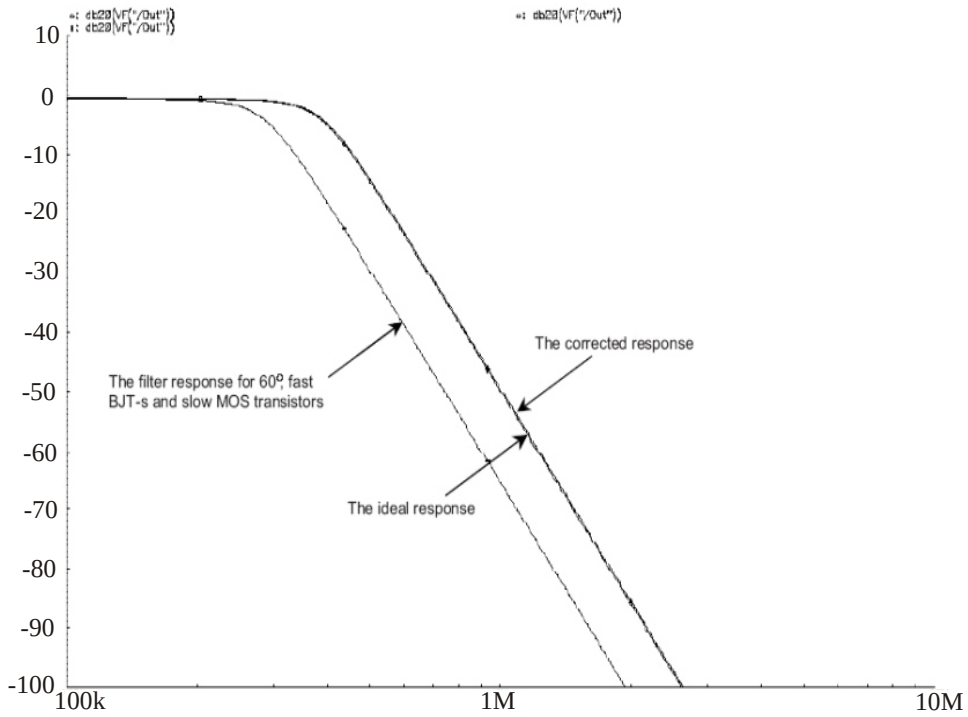


Figure 5.4: The simulated functionality of the corner frequency error prediction circuit

- **The transient response**

Another important simulation is the transient response. This should verify several aspects connected to the dynamic behavior of the circuit. The parameters considered here are the linearity and the group delay. Figure 5.5 shows the simulated input and the output signals of the circuit.

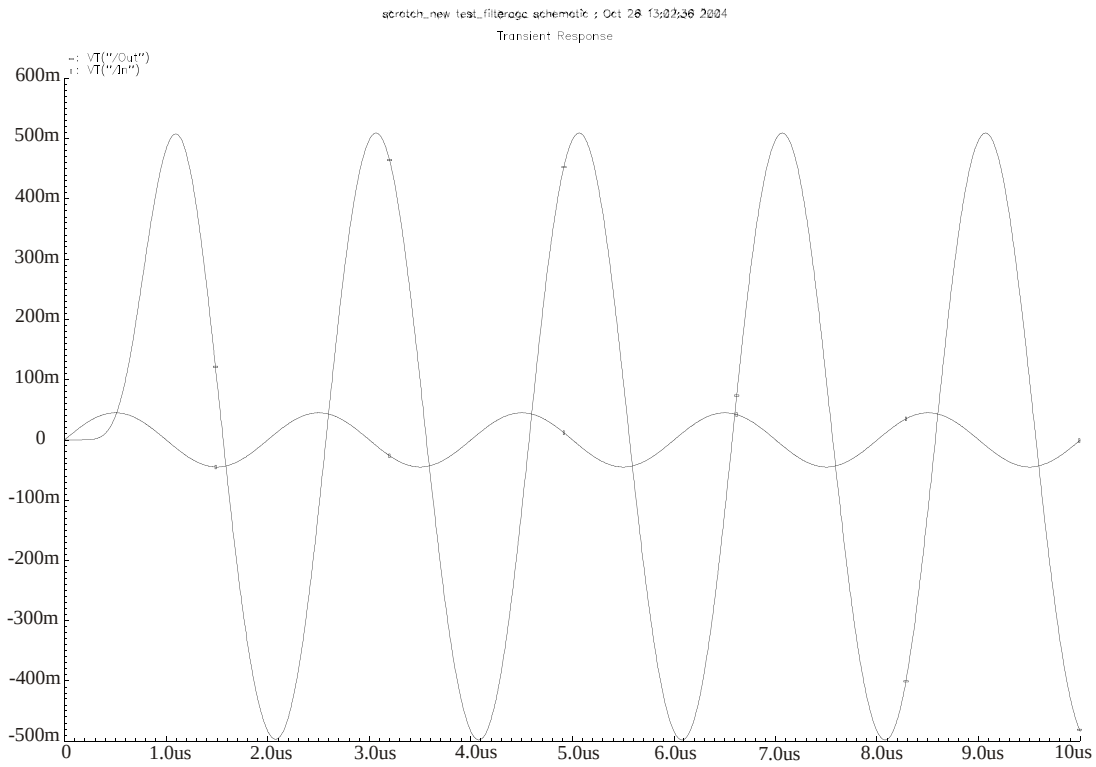


Figure 5.5: The simulated input and output signals in the time domain

The input signal is a 5MHz sine wave with the amplitude equal to 100mV peak to peak differential. The gain of the VGA has been set to 20dB. The resulting output signal has an amplitude of approximately 1V peak to peak differential. The circuit has been designed under the assumption that its output voltage should be somewhere between 800mV and 1V peak to peak since this value is usual for the full scale of the data converter. The corner frequency was set to 7.5MHz. From the figure it can be seen that the approximate time delay of the output signal is approximately 120ns, as it has been expected from the mathematical model of the filter. This simulation also proves that the phase response of the variable gain amplifier does not influence significantly the overall delay of the circuit. It also means that the bandwidth of the VGA is high compared to the corner frequency of the filter.

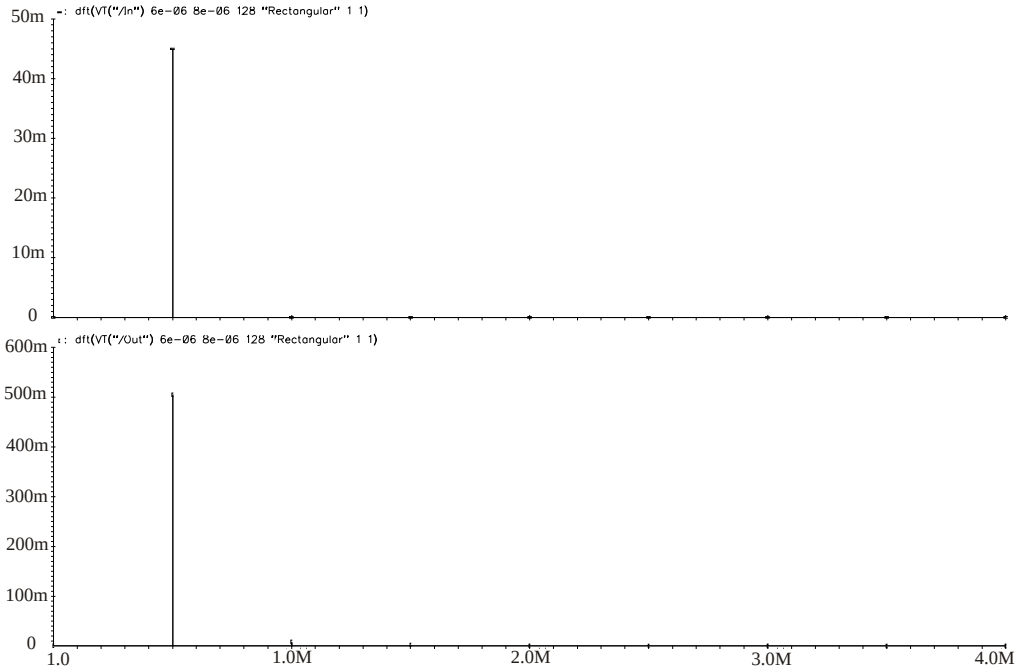


Figure 5.6: The simulated spectrum of the input and the output signals

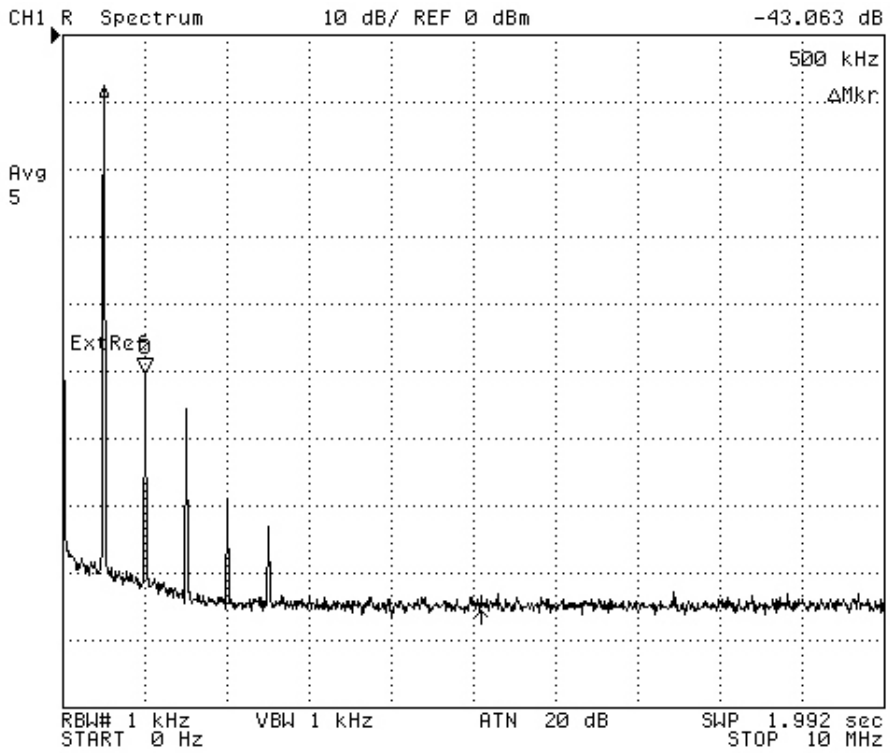


Figure 5.7: The measured spectrum of the output signal

Input signal	Gain[dB]	Harmonics	Amplitude difference[dB]
90mV	24dB	2	-45
		3	-30
		4	-58
45mV	24dB	2	-52.5
		3	-56.3
		4	-86.4
22.5mV	24dB	2	-61
		3	-
		4	-
90mV	12dB	2	-43.5
		3	-54.1
		4	-73.1
45mV	12dB	2	-51
		3	-
		4	-
22.5mV	12dB	2	-58
		3	-
		4	-
90mV	6dB	2	-40.5
		3	-55
		4	-65.5
45mV	6dB	2	-48.7
		3	-
		4	-
22.5mV	6dB	2	-54
		3	-
		4	-
90mV	0dB	2	-40.6
		3	-54.1
		4	-55
45mV	0dB	2	-49
		3	-
		4	-
22.5mV	0dB	2	-
		3	-
		4	-

Table 5.1: The measured harmonics of the output signal for different gain settings and input signal levels

Another important aspect regarding the time domain response and the large signal behavior of the circuit is the distortion introduced by nonlinearity. In the proposed circuit the main sources of nonlinearity are the switches connected in the signal path and the clipping of the opamps at high signal or offset levels. Due to

a relatively high gain and a negative feedback configuration the opamps contribute very little to the overall nonlinearity caused by the circuit. Figure 5.6 gives the simulated spectra of the input and of the output signals. The simulation has been done in identical conditions as the transient analysis presented in Figure 5.5. From the spectrum of the output signal it can be seen that all the higher order harmonics have magnitudes at least 45dB lower compared to the fundamental wanted signal. The measured spectrum of the output signal is given in Figure 5.7. This capture has been taken for an 500KHz signal with 90mV peak to peak differential amplitude. The amplitudes of the measured higher order harmonics for different input signal levels and gain settings are summarized in Table 5.1. It is of great importance that the even order harmonics have not been completely eliminated. This is due to the internal offset of the circuit that has been amplified and for large signals causes the clipping of the transient response. This is a very important aspect which leads to the idea stated before that the base band circuit must also employ an efficient offset compensation technique. Furthermore, the offset compensation should occur after each VGA stage in order to maintain the correct functionality of the circuit, even for very high gain settings.

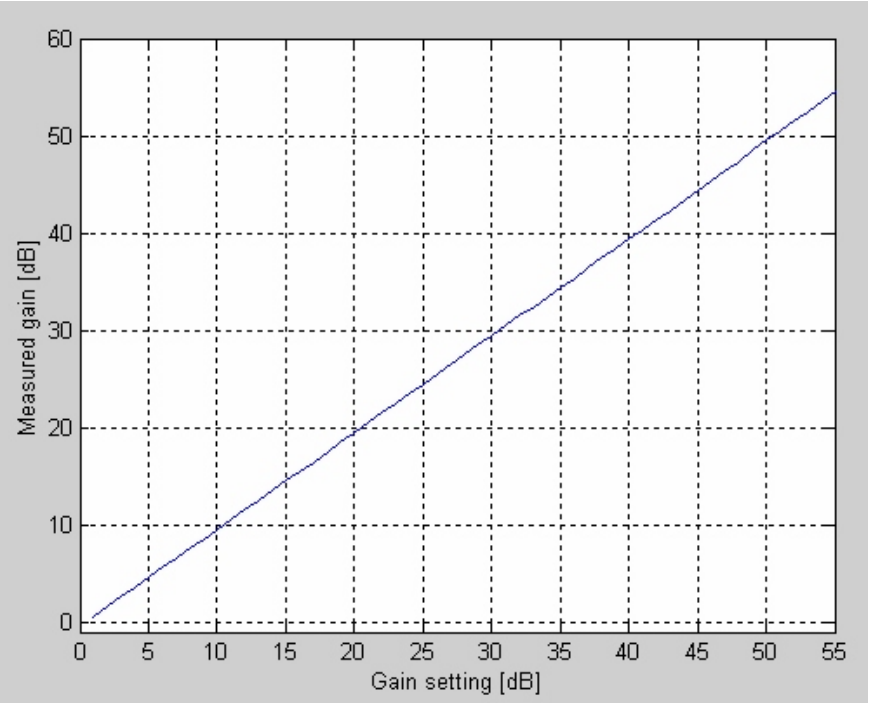


Figure 5.8: The measured gain values against the desired ideal gain settings

A similar problem occurs in gain measurements. The input offset of the circuit is approximately 7mV. This small voltage is then amplified by the VGA stages. At high gain settings, although the input signal level is very low, the offset can be made responsible of driving the output stages of the opamp in undesired operation regions; thus the gain measurements have been performed only up to a gain of 56dB

where the first VGA stage operates at a 0dB gain setting. The functionality of the first VGA stage has also been verified by programming the VGA with a special code that switches off all the gain stages except the first one. The measurements have shown that the gain difference between the two modes corresponding to the first stage are approximately 24dB away, as expected. The measured gain values against the programming code are presented in Figure 5.8. The corresponding simulated and measured gain step error functions are given in Figure 5.9.

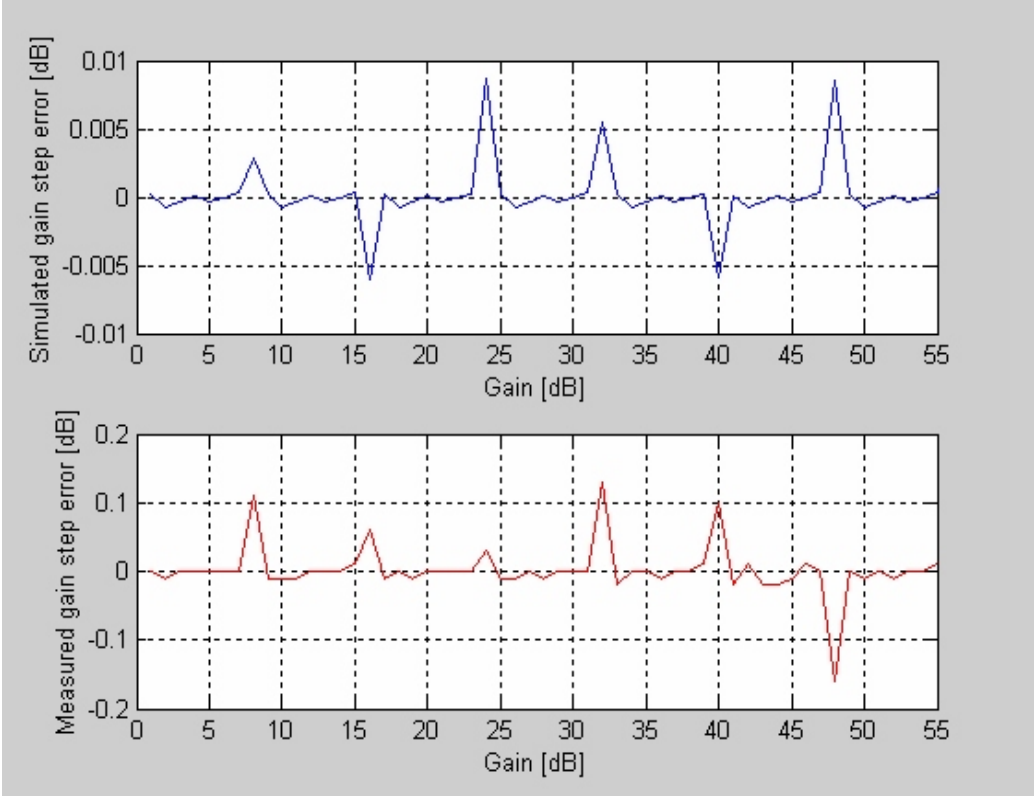


Figure 5.9: The simulated and the measured gain step error against the programming code

From this figure it can be seen that the maximum gain step error is approximately 0.15dB. This measurement complies with the 0.3dB specification given in the paragraph 4.2. It is also of importance that the gain step error function exhibits some regularities that could help finding the source of these errors. Typically a larger error peak occurs when at least two VGA stages are switched during the programming procedure.

- **Noise**

The noise of the circuit is a very important factor that determines the sensitivity of the entire receiver. Typically the difference between the noise floor of the sampled signal and the reference signal to noise ratio (e.g. approximately -100dBm for GSM)

defines the gain that must be added by the LNA and the RF mixer in the RF front end of the receiver without significant noise contribution. The noise contribution of a circuit is typically worse at lower frequencies where thermal noise is dominated by the flicker noise of the active devices. Additionally, for lower corner frequency settings high value resistors are used that generate a lot of noise. Therefore, the measurement in Figure 5.10 shows the noise spectrum of the experimental prototype for a 0dB gain setting and the lowest possible corner frequency equal to 132.7kHz. The measurement has been done by shorting both input pins to the common mode voltage.

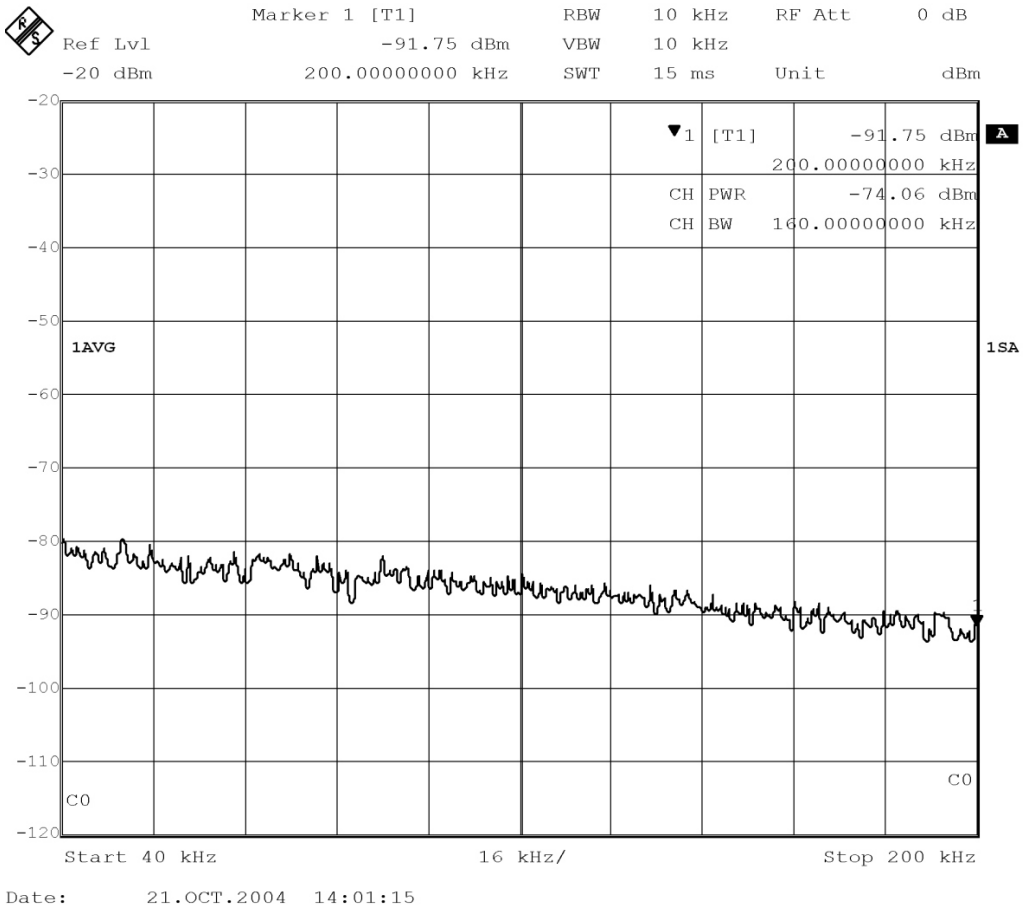


Figure 5.10: The measured noise spectrum for a 0dB VGA gain and a 132.7kHz corner frequency

From this figure it can be seen that the noise floor lays somewhere at -85dBm. The total integrated noise in the frequency range between 40kHz and 200kHz is -74dBm that corresponds to 44.7uV. For higher corner frequencies the noise power is distributed more evenly in the channel and, as a consequence, the noise floor is also lower. For a 785kHz frequency setting the measured noise floor lays at around -92dBm and the total integrated noise between 40kHz and 1.2MHz is -70dBm. The

noise measurements have lead to the conclusion that the noise behavior of the circuit is critical for lower frequency settings due to the large resistances required in order to achieve filter corner frequencies of hundreds of kHz. One possibility to alleviate the noise problem is to use R-2R networks that are capable of implementing much higher resistances than the unit resistors. This method has been suggested in [5].

- **Group delay**

The group delay of the circuit can introduce significant degradation of the modulated signal spectrum through selective time delay of individual components . In these cases the digital demodulation of the received signal in the base band can be difficult and the bit error rate of the system will be increased. If the variation of the group delay is large then additional equalization circuits are required. The Butterworth type of response has been chosen due to the fact that it offers a relatively low group delay variation in the pass band of the filter. Since the bandwidth of the VGA is large, its contribution to the group delay can be neglected. The measured group delay values for a 132.7kHz corner frequency setting are summarized in Table 5.2. The measured group delay variation in the passband approximately corresponds to the expected theoretical 3.5μs.

Frequency	**Group delay**
40kHz	1.26μs
50kHz	2.14μs
60kHz	2.74μs
70kHz	3.38μs
80kHz	3.68μs
90kHz	3.96μs
100kHz	4.2μs
110kHz	4.44μs
120kHz	4.6μs
130kHz	4.74μs
140kHz	4.9μs

Table 5.2: The measured group delay of the circuit for a 132.7kHz corner frequency setting

5.3 Performance summary

The proposed circuit complies in most of the cases with the given specifications with negligible errors. The most important parameters taken into account during the evaluation are the following:

- the programming range of the corner frequency - the measured corner frequencies are only approximately 2% away from the simulated values;

- the pass band gain - the measured pass band gain is variable between 0dB and 79dB as expected. The functionality of the higher gain settings have only been inferred by using a special programming code that is not present in the template due to offset problems;
- the pass band gain accuracy - the highest measured gain step error is approximately 0.15dB, this value being half of the worst case specifications;
- the common mode voltage - the measured common mode voltage is 1.534V corresponding to the 1.5V ideal design parameter;
- the integrated output noise for 0dB gain and 132.7kHz corner frequency - the measurements show that the total integrated output noise in the frequency range between 40kHz and 200kHz is approximately -74dBm (-44.7μV). For the given settings the average measured noise floor lays at approximately -85dBm;
- the group delay - the variation in the passband is 3.64μs and is similar as expected from theory and simulations;
- the current consumption - the total current drawn by the circuit is 11mA in low frequency mode and 13mA in high frequency mode. This consumption also includes the voltage regulators and the driver opamps on the test board.

The main issues encountered during testing are connected to the uncompensated internal offset and to a relatively high noise level at lower corner frequency settings, (typically in the 130kHz and 300kHz range). The uncompensated internal offset limits the operation of the circuit to gains of around 56dB when the input signal is very low. Additionally the presence of the large second and third order harmonics in the signal spectrum are the results of the uncompensated offset that potentially shifts the bias points of the transistors in the opamps. The noise contribution of the circuit can be lowered by avoiding the use of resistors larger than about 40kΩ and by optimally placing the gain stages in a way that decreases the noise contribution of the circuit, that is high gain stages as early as possible in the chain.

Chapter 6

Band Pass Filters for Multi-Mode IF Sampling Receivers

6.1 Introduction

One of the most important goals of the software defined radio concept is to reduce the number of the required analog building blocks as much as possible and do all the processing in the digital domain. A possible tendency, forced by the reduction of the analog component count, is to sample the signal closer to the antenna. The high frequency IF sampling receivers comply to this idea by using a single analog down conversion and a band pass analog to digital converter that samples the signal centered at some intermediate frequency. The choice of the intermediate frequency depends on the performances of the RF system filter, on the signal bandwidth and on the sampling frequency, as already discussed in the architectures section. The problems concerning the feasibility of RF and IF filtering in single conversion IF-sampling receivers are imposing a reasonable range for the intermediate frequency between 50MHz and 100MHz [31].

The high tens of MHz frequency range has been so far covered by passive or some kind of electro-mechanical (SAW or BAW) filters [35]. Modern single or multi-standard receivers employ these passive, off-chip filters in switched configurations where each filter processes the signals corresponding to a single standard. This filtering method does not exhibit the best efficiency due the lack of flexibility. The single-chip monolithic integration with the rest of the receiver is also not possible. Additionally the consumption of the receiver IC could be increased due to the 50Ω driving and matching requirements [37].

The work presented in this chapter tries to find a fully programmable, integrated alternative to passive band pass filters that have the potential to support the monolithic integration of the entire receiver. The section can be regarded as a feasibility study that is based on more or less classical band pass filter design methodologies from the literature [23][62][11][53]. These methods are adapted to the needs of the IF sampling receiver architecture with multi-mode capability. The

main specifications that will be taken into account can be derived with a similar analysis as in the case of the low pass filter and are summarized as follows:

- the center frequency at 75 MHz, according to the choice of the IF frequency - this choice is arbitrary since only the range of accepted IF frequencies is known to be between 50MHz and 100MHz, depending on the specifications of each system. The 75MHz has been chosen for this study as an average value from the variation range;
- the bandwidth variable between 200kHz (GSM) and 20MHz (possibly WLAN) - the programmability requirement originates from the necessity to support present and future standards, in compliance with the software defined radio concept;
- a Butterworth approximation for maximally flat in-band response and low group delay variation, similarly as for the low pass approach;

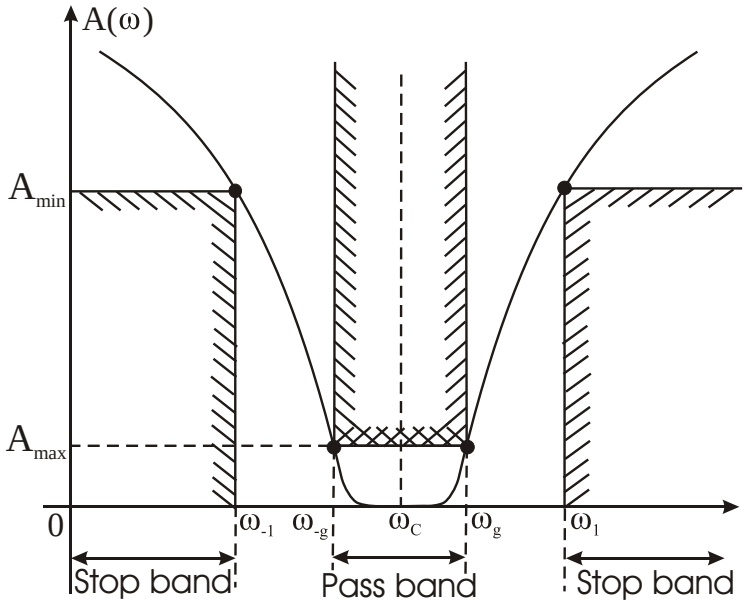


Figure 6.1: The generalized attenuation characteristic of a band pass filter and the specific parameters

- the filter order - this requirement is not very important due to the fact that the design and the programming algorithm can be easily generalized for arbitrary filter orders once they have been developed. For the feasibility study the filter order is chosen equal to 8 (the attenuation approximately corresponds to a 4^{th} order low-pass prototype). It results that the derivation of a proper attenuation characteristic is more difficult than in the case of the previously presented low pass filter, where the specifications have been clearly fixed. A general attenuation characteristic, suitable for a symbolic description, is shown

in Figure 6.1. In the diagram ω_C is the filter center frequency, while the bandwidth is defined as $BW = \omega_g - \omega_{-g}$. Note that bot frequencies are expressed in rad/s instead of Hz. The quality factor of the filter, Q_{BP}, is the ratio between the center frequency and the bandwidth. The attenuations A_{min} and A_{max} have the same significance as in the case of a low pass filter. All these parameters can be chosen according to the requirements imposed by a specific communication standard;

- linearity - this specification depends on the characteristics of the signal, sampled at IF. If the large out of band interfering signals have been previously attenuated by the system filter and the low noise amplifier, the linearity requirements could be more relaxed. The most important specification here is that the system should avoid intermodulation distortion, similarly as in the case of the base band circuit discussed earlier;

- the filter must be continuous time in nature in order to perform signal selection without smoothing and anti aliasing before sampling;

- tuning of the center frequency and a correction of the digital code that defines bandwidth in order to compensate for process tolerances and temperature;

- a current consumption as low as possible;

- full integrability in a portable device;

- single supply voltage operation;

6.2 Theoretical bases of band pass filter design

This paragraph gives the mathematical characterization of the band pass filter transfer function and offers a first impression on the possible programming possibilities. The starting point of the design is the set of normalized low pass poles or the corresponding LC ladder prototype. Although the LC ladder description is closer to a real realization instead of being purely theoretical, it is often used to develop filters suitable for implementation with a gyrator or state variable approach. The values of the components in a normalized low pass LC ladder filter can be found tabulated according to the chosen approximation. Custom transfer functions, optimized for specified performances, can be synthesized by using the continuous fraction expansion according to the Cauer-Foster method [72].

6.2.1 The frequency transformation of the transfer function

As in the case of low pass filters, the band pass frequency response can be described by the pole-zero configuration. The poles of the band pass filter must be inferred from the poles of a normalized low pass prototype. The normalized poles of the initial second order low pass filter can be found in design tables. The general expressions

of these complex conjugate pole pairs have been given for the low pass case and are repeated here for convenience.

$$\begin{cases} s_{x1LP} = \alpha_{LP} + j\beta_{LP} \\ s_{x2LP} = \alpha_{LP} - j\beta_{LP} \end{cases} \tag{6.1}$$

The corresponding second order normalized low pass transfer function is:

$$H_{nLP}(s) = \frac{1}{\left(1 - \dfrac{s}{s_{x1LP}}\right)\left(1 - \dfrac{s}{s_{x2LP}}\right)} = \frac{b}{s^2 + as + b} \ , \tag{6.2}$$

where the coefficients a and b can be expressed as follows:

$$\begin{cases} a = -\left(s_{x1LP} + s_{x2LP}\right) = 2\alpha_{LP} \\ b = s_{x1LP} \cdot s_{x2LP} = \alpha_{LP}^2 + \beta_{LP}^2 \end{cases} \tag{6.3}$$

The next step in deriving the band pass transfer function is a frequency transformation rather than a simple frequency scaling, as it was in the case of a low pass filter. The low pass to band pass frequency transformation implies the replacement of the complex variable s with s^*. It is of great importance that the transformation also includes frequency scaling [62]. The transformation is given in the following relation:

$$s \ \leftrightarrow \ s^* = Q_{BP}\left(\frac{s}{\omega_C} + \frac{\omega_C}{s}\right) \ , \tag{6.4}$$

where ω_C is the desired center frequency and Q_{BP} is the quality factor of the band pass filter. The quality factor is defined here as the ratio between the center frequency and the -3dB bandwidth. The frequency scaled band pass transfer function can be written:

$$H_{BP}(s) = \frac{b}{\left[Q_{BP}\left(\dfrac{s}{\omega_C} + \dfrac{\omega_C}{s}\right)\right]^2 + aQ_{BP}\left(\dfrac{s}{\omega_C} + \dfrac{\omega_C}{s}\right) + b} \tag{6.5}$$

The final expression of the band pass function results by rearranging the terms in the equation (6.5).

$$H_{BP}(s) = \frac{s^2 \cdot b \cdot \dfrac{\omega_C^2}{Q^2}}{s^4 + \omega_C \dfrac{a}{Q_{BP}} s^3 + \omega_C^2\left(2 + \dfrac{b}{Q_{BP}^2}\right)s^2 + \omega_C^3 \dfrac{a}{Q_{BP}} s + \omega_C^4} \tag{6.6}$$

It is of importance that the filter order has been doubled by the frequency transformation. The coefficients of s in the band pass response are functions depending on the desired center frequency, the quality factor of the band pass filter and on the normalized poles of the low pass prototype. For a convenient implementation the 4^{th} order function can be written as a product of elementary second order sections. For fixed frequency filters the factorization is usually implemented numerically by using a suitable computer algorithm. The numerical coefficients of each second order section can be directly used for solving the sizing equations of a given filter.

In order to develop a programming algorithm, the factorization of the band pass denominator should be solved symbolically. This can be done by using the special properties of the band pass poles, namely the fact that they appear in complex conjugate pairs. In this case the fourth order polynomial can be written as a product of two second order terms and equaled with zero in order to find the roots, as given below [62][23]:

$$\left(s^2 + \frac{\omega_{01}}{q_1}s + \omega_{01}^2\right) \cdot \left(s^2 + \frac{\omega_{02}}{q_2}s + \omega_{02}^2\right) = 0 \ , \tag{6.7}$$

where ω_{01} and ω_{02} are the resonant frequencies of the two second order sections while q_1 and q_2 are the corresponding quality factors of the complex conjugate pole pairs. After rearranging the terms the equation (6.7) becomes:

$$\begin{aligned} s^4 + \left(\frac{\omega_{01}}{q_1} + \frac{\omega_{02}}{q_2}\right)s^3 + \left(\omega_{01}^2 + \frac{\omega_{01}\omega_{02}}{q_1 q_2} + \omega_{02}^2\right)s^2 + \\ + \left(\frac{\omega_{01}^2\omega_{02}}{q_2} + \frac{\omega_{01}\omega_{02}^2}{q_1}\right)s + \omega_{01}^2\omega_{02}^2 = 0 \end{aligned} \tag{6.8}$$

The coefficients of the terms in s can be identified by comparing the equations (6.8) and (6.6). The following system of equations results:

$$\begin{cases} \omega_{01}^2\omega_{02}^2 = \omega_C^4 \\ \dfrac{\omega_{01}^2\omega_{02}}{q_2} + \dfrac{\omega_{01}\omega_{02}^2}{q_1} = \omega_C^3\dfrac{a}{Q_{BP}} \\ \omega_{01}^2 + \dfrac{\omega_{01}\omega_{02}}{q_1 q_2} + \omega_{02}^2 = \omega_C^2\left(2 + \dfrac{b}{Q_{BP}^2}\right) \\ \dfrac{\omega_{01}}{q_1} + \dfrac{\omega_{02}}{q_2} = \omega_C\dfrac{a}{Q_{BP}} \end{cases} \tag{6.9}$$

From the first equation it can be noticed that

$$\omega_{01}\omega_{02} = \omega_C^2 \tag{6.10}$$

From the second equation and the fourth it can be demonstrated that the pole quality factors are equal, that is $q_1 = q_2 = q$. This means that the band pass poles, whose imaginary parts have the same sign, are collinear. The collinearity has been previously demonstrated for the poles of the low pass filter. The pole locations are shown in Figure 6.2.

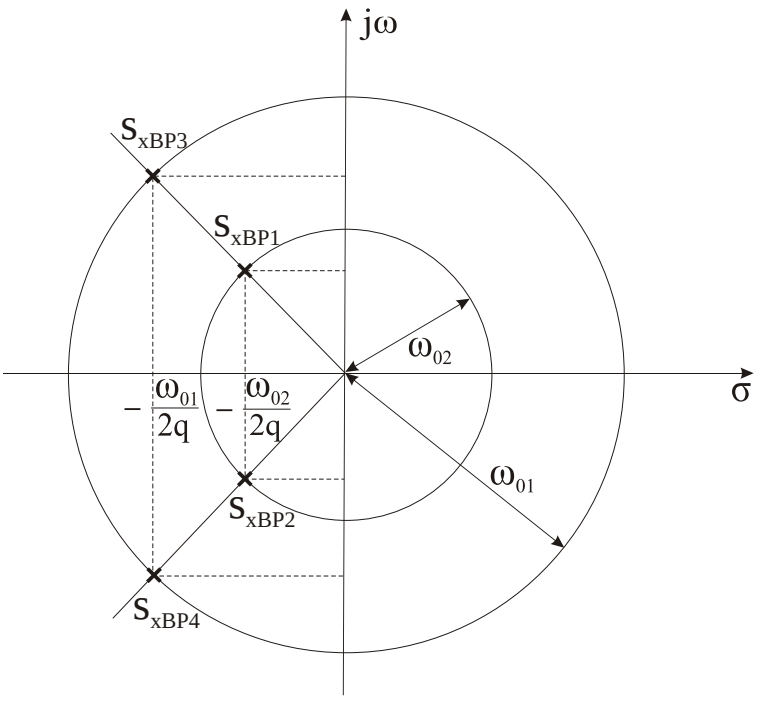


Figure 6.2: The location of the band pass poles in the s plane

In this case the following identity is valid:

$$\omega_{01} + \omega_{02} = \omega_{02} + \frac{\omega_C^2}{\omega_{02}} = \omega_{01} + \frac{\omega_C^2}{\omega_{01}} = \omega_C \cdot \frac{a \cdot q}{Q_{BP}} \tag{6.11}$$

The expressions of the resonant frequencies can be computed by combining the third equation of the system (6.9) with the equation (6.11). It results:

$$\begin{cases} \omega_{01} = \dfrac{\omega_C}{2}\left(\dfrac{a\cdot q}{Q_{BP}} + \sqrt{\dfrac{b}{Q_{BP}^2} - \dfrac{1}{q^2}}\right) \\ \omega_{02} = \dfrac{2\omega_C}{\dfrac{a\cdot q}{Q_{BP}} + \sqrt{\dfrac{b}{Q_{BP}^2} - \dfrac{1}{q^2}}} \end{cases} \tag{6.12}$$

From the expressions of the resonant frequencies it can be seen that they are fully defined only when the quality factor of the poles is known. The expression of q can be determined by using the third equation from (6.9) and the identity in (6.11). It results:

$$q^2 = \frac{b + 4Q_{BP}^2}{2a^2} + \frac{\sqrt{b^2 + 4Q_{BP}^2\,(2b-a) + Q_{BP}^4}}{2a^2} \tag{6.13}$$

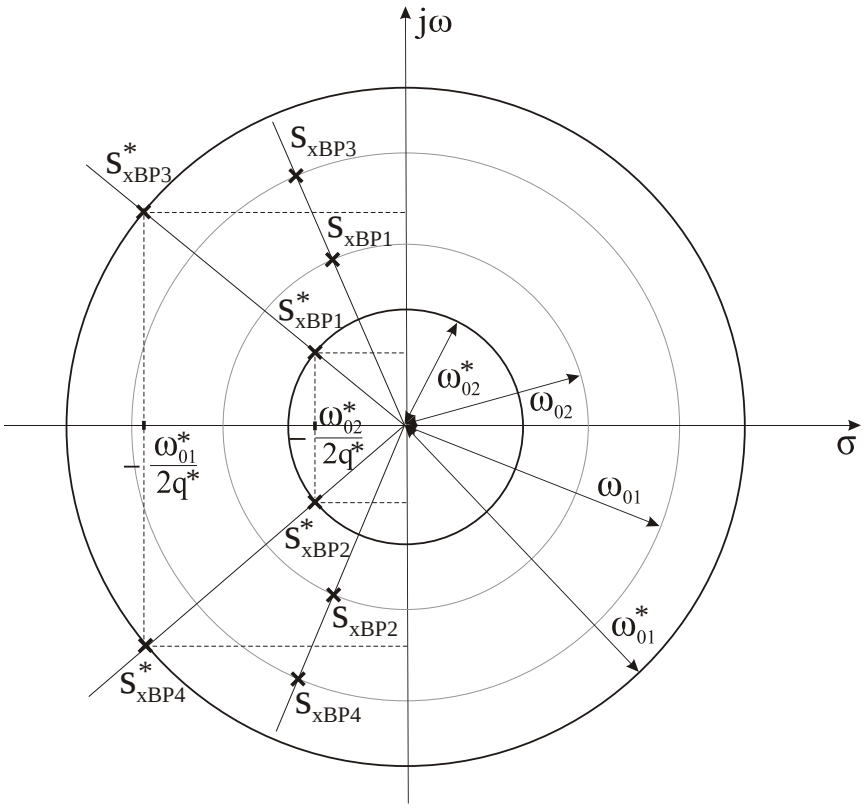


Figure 6.3: The new location of the poles in the s plane after increasing the bandwidth

The programming algorithm of the filter should vary only the bandwidth, without affecting the center frequency. This procedure varies the quality factor of the

filter, previously noted Q_{BP}. From the expressions of the resonant frequencies, given in (6.12), it can be seen that ω_{01} increases when Q_{BP} becomes smaller, while ω_{02} decreases. The scaling factor of the resonant frequencies depends on the normalized poles of the low pass prototype and on Q_{BP}. Since the quality factor q of the pole pairs also changes with Q_{BP} the angle of the line that ties the poles and the origin together will also be modified by programming.

Figure 6.3 shows the location of the poles in the s plane after increasing the filter bandwidth and implicitly lowering Q_{BP}. The poles, the resonant frequencies and the quality factor of the poles corresponding to an increased bandwidth have been marked with "*". When the bandwidth is decreased and Q_{BP} is increased, a similar analysis leads to a decreasing ω_{01} and an increasing ω_{02}.

From the analysis results that the dependence of the resonant frequencies and the pole quality factors on the filter bandwidth and quality factor is not linear. Due to this fact the band pass filter structures based on a cascade of second order section are not easily scalable. As a consequence, the programming algorithm must employ some more complicated structures that take into account square roots and sums of terms depending on the bandwidth; thus cannot be simply implemented as in the low pass case.

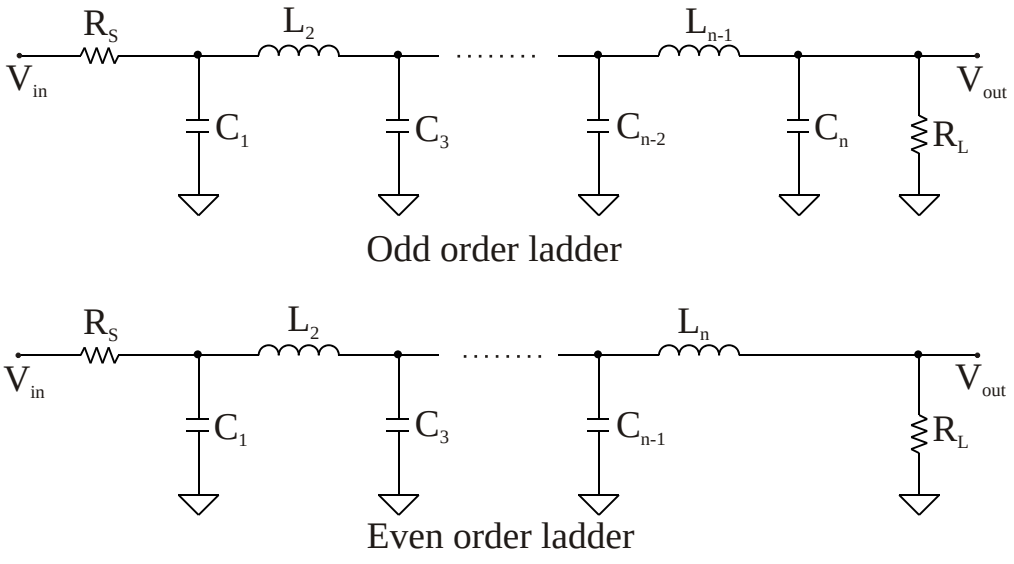


Figure 6.4: The doubly terminated low pass LC ladder prototype

6.2.2 The frequency transformation of the components

In some filter realizations the frequency transformation is performed on the components of a passive low pass prototype rather than on the transfer function [72]. This is typically the case when synthesis methods based on gyrators or state variables are

employed for designing the filter. The low pass prototype is a passive LC ladder, whose components are normalized with respect to the desired center frequency and bandwidth. The schematic of the prototype ladder is presented in Figure 6.4. For a correct functionality the ladder must be doubly terminated with the source and load resistors R_S and R_L.

The first step in the design of these filters is the frequency transformation of the passive prototype that also includes frequency and impedance scaling. The frequency transformations for the components are performed as follows [62][72][23]:

- **The frequency transformation of the inductors**

This transformation is based on replacing the complex variable s in the expression of the impedance associated with the inductor.

$$sL \;\leftrightarrow\; s^*L\;, \tag{6.14}$$

where s^* has the same significance as in equation (6.4). The inductive reactance corresponding to a band pass ladder can be written as follows:

$$s^*L = Q_{BP}\left(\frac{s}{\omega_C}+\frac{\omega_C}{s}\right)L = \frac{Q_{BP}\cdot L}{\omega_C}s + \frac{Q_{BP}\cdot L\cdot\omega_C}{s} = sL^* + \frac{1}{sC^*} \tag{6.15}$$

From this equation it can be seen that each inductance in the low pass prototype is transformed into another inductance in series with a capacitance, that correspond to a frequency scaled band pass ladder. The values of the band pass inductance and capacitance can be calculated from the following equations:

$$\begin{cases} L^* = \dfrac{Q_{BP}\cdot L}{\omega_C} \\ C^* = \dfrac{1}{Q_{BP}\cdot L\cdot\omega_C} \end{cases} \tag{6.16}$$

- **The frequency transformation of the capacitors**

Similarly as in the case of the inductors the low pass to band pass frequency transformation of the capacitive reactances is given as follows:

$$\frac{1}{sC} \;\leftrightarrow\; \frac{1}{s^*C} \tag{6.17}$$

The expression of the band pass capacitive reactance results:

$$\frac{1}{s^*C} = \frac{1}{\frac{Q_{BP}\cdot C}{\omega_C}s + \frac{Q_{BP}\cdot C\cdot\omega_C}{s}} = sL^* \,||\, \frac{1}{sC^*} \tag{6.18}$$

From the equation above results that each capacitance from the low pass prototype is transformed into an inductance, connected in parallel with a capacitance. The expressions of the band pass components are as follows:

$$\begin{cases} L^* = \dfrac{1}{Q_{BP}\cdot C\cdot\omega_C} \\ C^* = \dfrac{Q_{BP}\cdot C}{\omega_C} \end{cases} \tag{6.19}$$

The schematic of the band pass LC ladder is shown in Figure 6.5.

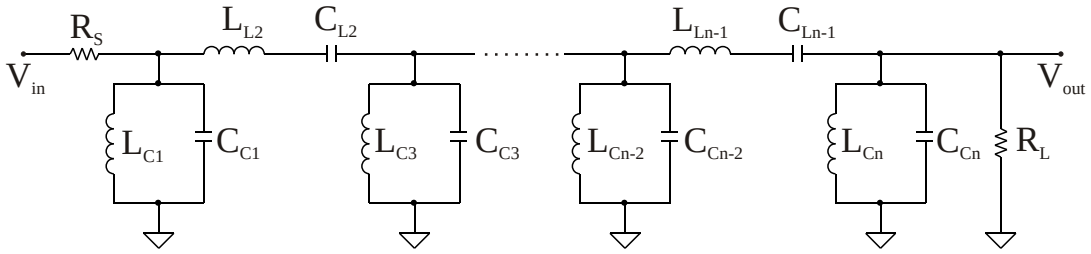


Figure 6.5: The doubly terminated band pass LC ladder

The values of the components in the resulting frequency scaled band pass ladder can be directly used for deriving the sizing equations for a real filter implementation. The final values of the band pass components are determined by impedance scaling. In the notation each index shows the original component in the prototype and Z is the characteristic input- and termination impedance of the ladder.

$$\begin{cases} L_L^* = \dfrac{Q_{BP}\cdot L\cdot Z}{\omega_C} = \dfrac{L\cdot Z}{BW} \\ C_L^* = \dfrac{1}{Q_{BP}\cdot L\cdot\omega_C\cdot Z} = \dfrac{BW}{L\cdot\omega_C^2\cdot Z} \\ L_C^* = \dfrac{Z}{Q_{BP}\cdot C\cdot\omega_C} = \dfrac{Z\cdot BW}{C\cdot\omega_C^2} \\ C_C^* = \dfrac{Q_{BP}\cdot C}{\omega_C\cdot Z} = \dfrac{C}{BW\cdot Z} \end{cases} \tag{6.20}$$

The programming of the filter bandwidth turns out to be extremely simple. By the examination of the band pass components, given in the system (6.20), it can be seen that they are either directly proportional with the bandwidth or proportional to the reciprocal of the bandwidth. In order to program the bandwidth of the filter a scaling factor can be defined as follows:

$$F = \frac{BW^*}{BW} \ , \tag{6.21}$$

where BW corresponds to a basic, fixed set of components, while BW^* is the new desired bandwidth of the filter. It results that the programming of the bandwidth is reduced to a definition of a basic set of components, scaled with F or $1/F$ according to the equations (6.20) and (6.21). The components also require a scaling with 2π due to the transformation of the frequencies from rad/s in Hz.

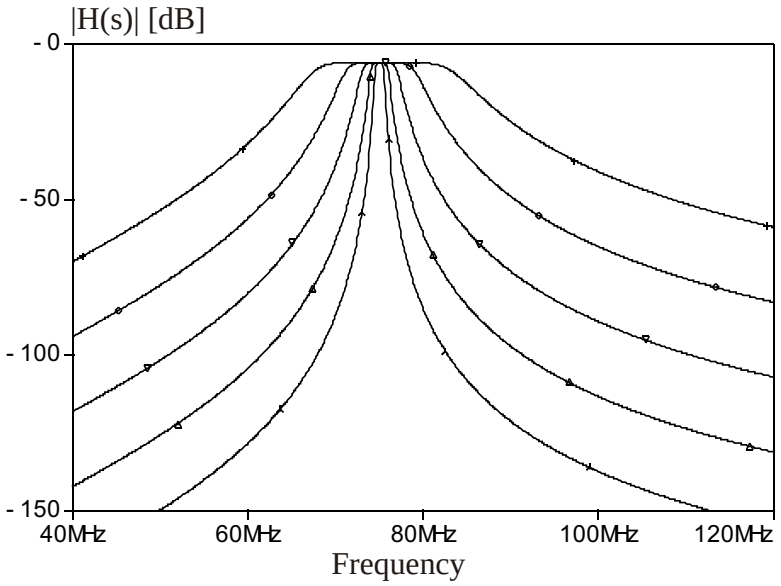


Figure 6.6: The simulated magnitude response of the band pass LC ladder with scaled bandwidth

The programming strategy can be defined with the following rules:

- scale every inductance originating from a low pass inductance with a factor $1/F$;
- scale every capacitance originating from a low pass inductance with a factor equal to F;
- scale every inductance originating from a low pass capacitance with a factor equal to F;

- scale every capacitance originating from a low pass capacitance with a factor equal to $1/F$;

The simulated magnitude response of an 8^{th} order band pass filter for different scaling factors is given in Figure 6.6.

It is of great importance that for LC filters the complicated scaling of the resonant frequencies and the quality factors, corresponding to each complex conjugated pole pair, is hardwired in the filter structure. This is the reason why the LC ladder approach leads to a highly scalable filter architecture whose bandwidth can be easily programmed regardless of the chosen center frequency. Another important advantage over biquad implementations is that the structure of the integrated band pass filters is highly modular and requires only identical active components. This feature will be demonstrated later when discussing the possible synthesis methods.

6.3 Programmable band pass filter realizations

In the previous paragraphs it has been demonstrated that band pass filters based on second order sections do not have a very scalable architecture due to the complicated dependence of the pole resonant frequencies and quality factors on the bandwidth. Band pass filters based on LC prototypes exhibit a very good scalability of the bandwidth because the complicated dependence is included in the structure of the passive ladder. The following paragraphs present some filter realizations with programmable bandwidth. In the presentation the emphasis lays on two main issues, namely programmability and feasibility. It will be demonstrated that, although LC ladder based filters are suitable for programmable realizations, they also exhibit large component spreads and reduced feasibility for high Q requirements. The filters built as a cascade of second order sections and their derivatives have the potential to trade programmability and feasibility for the filter approximation. Except some less classical implementations, the vast majority of the discussed filter architectures are based on operational transconductance amplifiers, or OTA-s.

6.3.1 Band-pass filtering with op-amp-RC structures

Op-amp RC filters have several advantages over the other types of filters. Some of the most important advantages are the high dynamic range and good linearity. The down converted and filtered signal should have a magnitude that fits the requirements forced by the conversion range of the ADC. This magnitude is usually around 1V peak to peak differential. An op-amp-RC filter can handle these signals without significant distortion. Another advantage is that the input impedance can be easily adjusted by modifying passive resistors. Due to the passive feedback network the overall consumption of the circuit is significantly reduced. The only parameter that increases consumption is the required driving power of the op-amps (when low load resistance is required together with large capacitive loads). All these advantages

make the op-amp-RC filters to be the ideal candidates for low frequency filtering [62].

At high frequencies the performances of the op-amp-RC filters are poor. The reason for this is the frequency dependent open-loop gain of the op-amps. When used with a feedback network the main role of the op-amp is to keep its inputs at a virtual ground from differential point of view. This is possible only when the instantaneous value of the open loop gain is high enough to make the transfer function of the circuit independent of the op-amp. At high frequencies the gain is decreased due to the frequency dependence. The overall transfer function of the circuit will depend on the op-amp characteristics and the performances of the filters are degraded. Usually it is not feasible to implement filters with op-amp-RC techniques at frequencies higher than about 10MHz. A general specification requires the unity-gain bandwidth of the op-amp to be much higher than the frequency of the processed signal [36].

As a conclusion, although there are several implementation methods for opamp-RC band pass filters (e.g. biquads, multiple feedback and general impedance conversion) [11], these do not comply with the high frequency and high Q requirements due to the limited unity-gain bandwidth of the opamps.

6.3.2 Band-pass filtering with switched capacitor circuits

Switched capacitor filters are used mainly in discrete time signal processing but also in continuous time domain. The reason for this is that capacitor ratios can be implemented relatively precisely on silicon and this eliminates the need for a tuning circuit. Other advantage is that the dynamic range is large. An important drawback is that a switched capacitor filter, when used for continuous time signal processing, still requires a continuous time anti-aliasing filter at the input and a smoothing filter at the output. Another problem is that switched capacitor filters are built around op-amps that still create a bottleneck with their frequency dependent open loop-gain, their offset, and their settling time. Due to these characteristics switched capacitor filters cannot be used at high frequencies and continuous time signal processing [36].

6.3.3 Band-pass filtering with transconductor-capacitor structures

The main building block of OTA-C filters are the operational transconductance amplifiers, or simply transconductors. The OTA delivers current at the output; thus it can operate in open-loop structures and the operating frequencies will be much higher than for structures based on op-amps. The higher limit of the frequency range is determined by the internal structure of the transconductors themselves and by the parasitics. The most simple OTA is a voltage controlled current source with the parameter g_m. Real OTA-s have at least one internal pole, a finite output resistance and some parasitic capacitances associated with the input and output terminals. All the simulations presented in the following paragraphs are performed

using transconductor cells modeled with controlled sources. In order to get a first idea about the influences of internal poles and parasitic capacitances on the overall filter response the model includes one internal pole with variable frequency, a model for the finite output resistance and the parasitic capacitance at the output node. The schematic of the fully differential OTA model is presented in Figure 6.7 [30]. The transconductance parameter is determined by the identical resistances $2/g_m$.

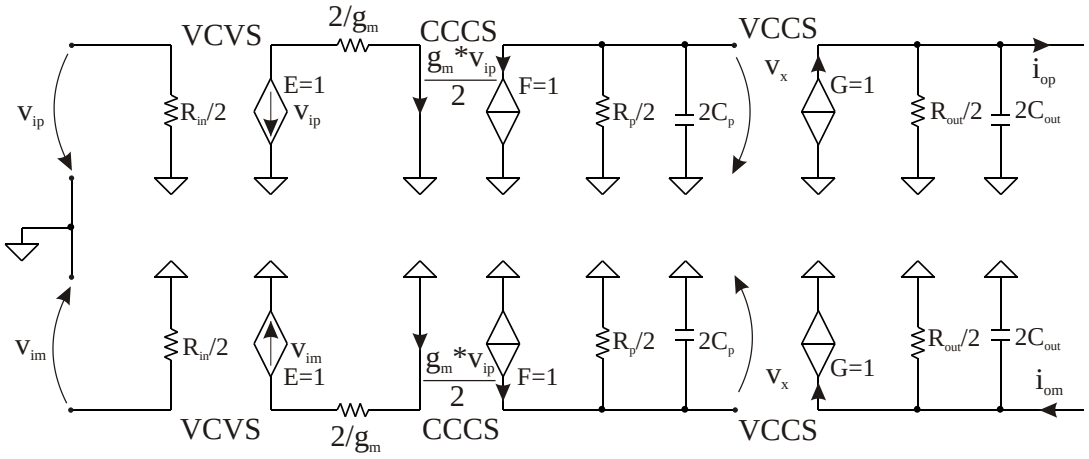


Figure 6.7: Fully differential OTA model used in simulations

6.3.3.1 OTA-C band-pass filters based on gyrators

Gyrator filters are an alternative for active implementations of the LC band pass ladder from Figure 6.5. This realization implies the replacement of all the inductors and the resistors with active structures that emulate their functionality [30]. The implementation of the resistors is based on circuit connections that realize the reciprocal of a transconductance. The practical circuit, that implements a resistor with one terminal connected to the ground, is shown in Figure 6.8 [62]. The value of the resistance is equal to the reciprocal of the transconductance g_m.

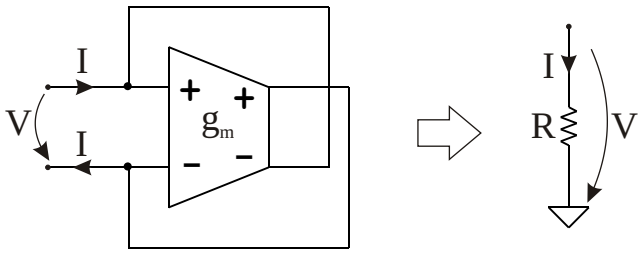


Figure 6.8: Active implementation of a resistor with one terminal connected to the ground

The implementation of a floating resistance is more complicated since two different reference voltages must be created. Therefore, a common practice is to transform the input voltage source to an input current source [4]. The transformation is shown in Figure 6.9.

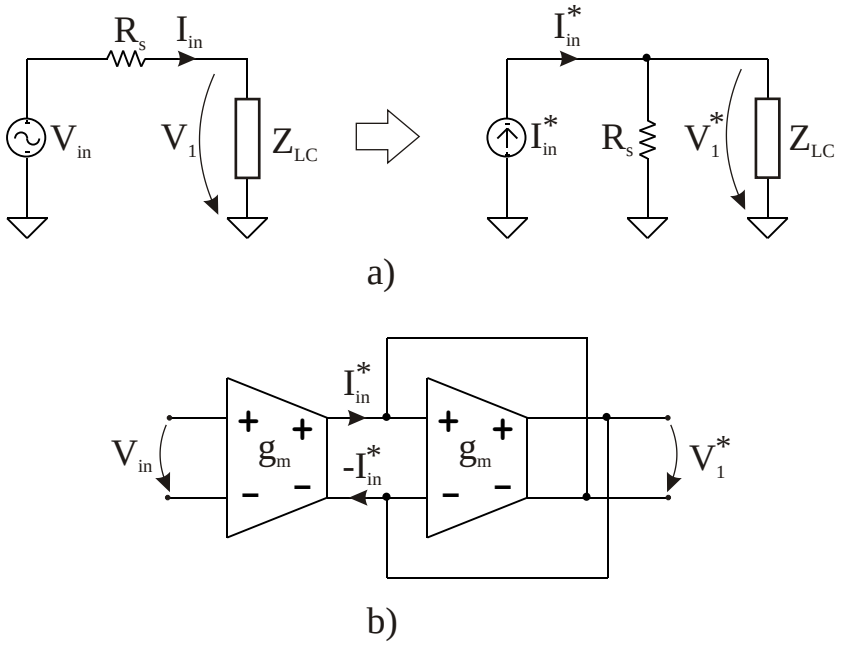


Figure 6.9: a) The transformation of the input voltage source to an input current and b) the OTA-C implementation

It can be seen that the floating source resistance has been transformed into a grounded resistance, that can be implemented with the structure from Figure 6.8. The input current I^*_{in} is determined by forcing the equivalence of the two circuits. The functionality of the sources is equal if the current and the voltage drop on the input impedance of the LC network are the same after the transformation. Then it holds true:

$$V_{in} \cdot \frac{Z_{LC}}{R_S + Z_{LC}} = I^*_{in} \cdot \frac{R_S Z_{LC}}{R_S + Z_{LC}} \tag{6.22}$$

It results that the equivalent input current source must be scaled with the reciprocal of the source resistance R_S and will be equal to V_{in}/R_S. The transformation yields the OTA-C structure from the Figure 6.9 b), where the first transconductance amplifier implements the scaled current source.

Another elements that must be replaced in the active implementation are inductances. Inductors are implemented by using an impedance conversion. The

impedance conversion is a procedure in which an impedance Z is inverted and mirrored to the input of an active structure. The inversion and the impedance mirroring is implemented with a gyrator whose input current is proportional to the output voltage and the output current is proportional to the input voltage through a conversion factor r, called the gyration resistance. The general structure of a gyrator as a two-port and the equivalent input resistance are shown in Figure 6.10 [62].

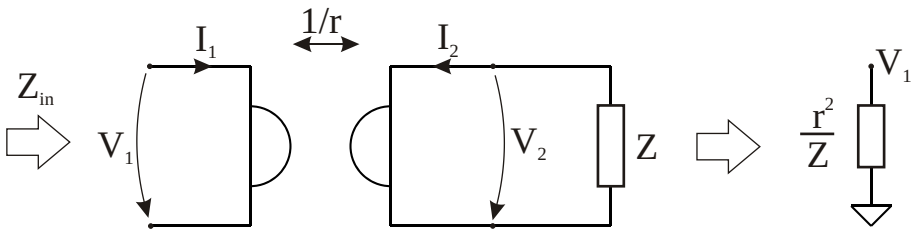


Figure 6.10: The general structure of a gyrator represented as a two-port

The equations of the circuit can be written:

$$\begin{cases} V_2 = -r \cdot I_1 \\ V_1 = r \cdot I_2 \\ V_2 = -I_2 \cdot Z \end{cases} \tag{6.23}$$

The input impedance of the structure is proportional with the reciprocal of the impedance Z and with the squared gyration resistance. It results:

$$Z_{in} = \frac{V_1}{I_1} = \frac{r^2}{Z} \tag{6.24}$$

The inversion of a floating impedance is done by creating a floating node whose voltage is referenced to the ground. This procedure can be considered as the replacement of the Z impedance ground connection from Figure 6.10 with a floating voltage. The transformation is done by using a second gyrator that creates the floating nodes at the terminals of Z, as shown in the Figure 6.11. It can be demonstrated that both the input and the output impedances of the circuit are equal to r^2/Z.

From the analysis results that an inductance can be implemented by the inversion of a capacitance. In the OTA-C design techniques the gyrators are realized as a pair of transconductance amplifiers connected in a feedback loop. The structures used to simulate the functionality of a grounded and a floating inductance are presented in Figure 6.12 and Figure 6.13.

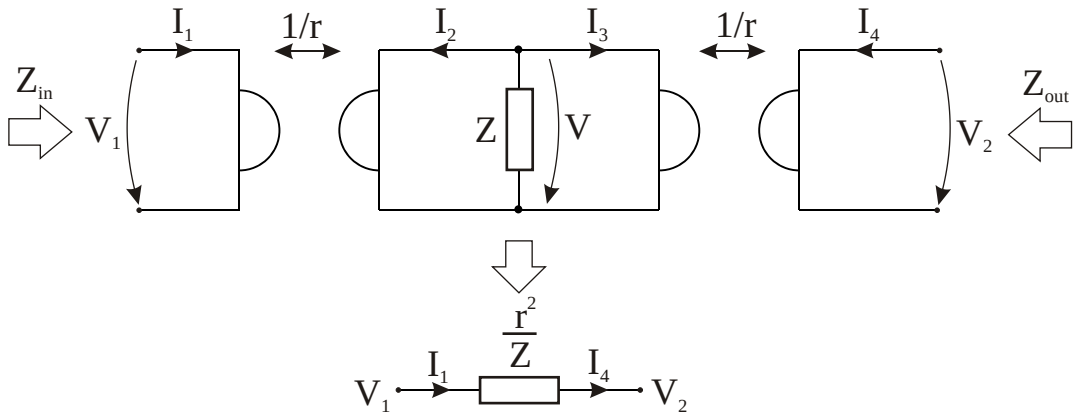


Figure 6.11: The inversion of a floating impedance with two gyrators

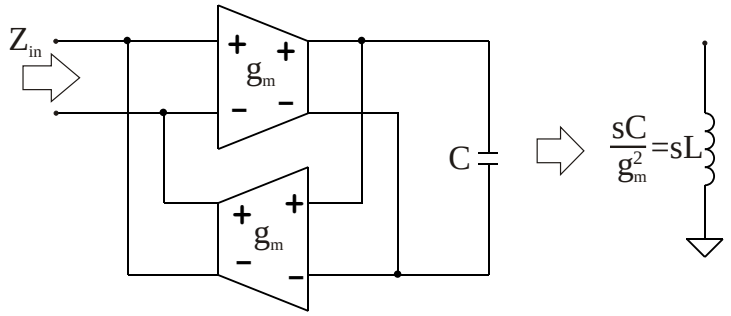


Figure 6.12: The OTA-C implementation of a grounded inductance

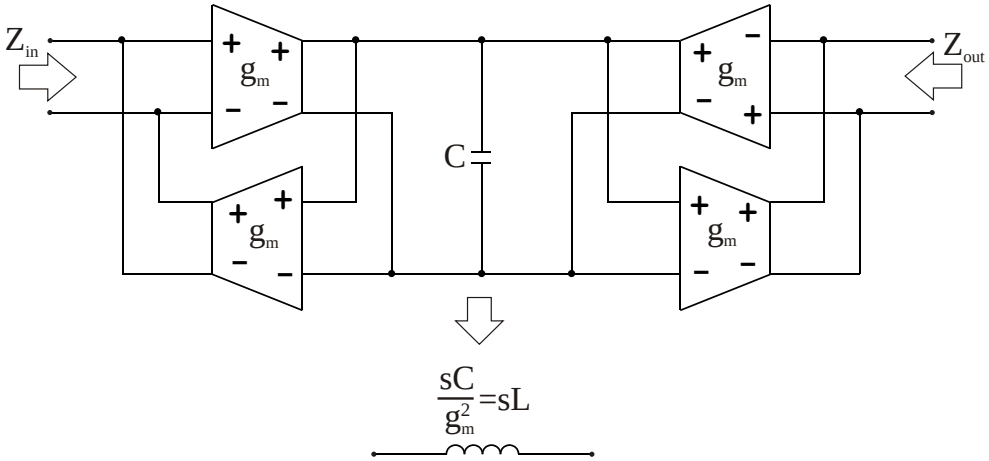


Figure 6.13: The OTA-C implementation of a floating inductance

Here the gyration resistance is equal to $1/g_m$. The value of capacitance can be calculated according to the following equation:

$$C = g_m^2 \cdot L \tag{6.25}$$

The passive LC prototype of a doubly terminated 8^{th} order band pass ladder can be derived from the general ladder structure from Figure 6.5. The corresponding active implementation is obtained by replacing the inductances and the passive termination resistors with the equivalent active structures. The final, fully differential implementation of the filter is presented in the Figure 6.14.

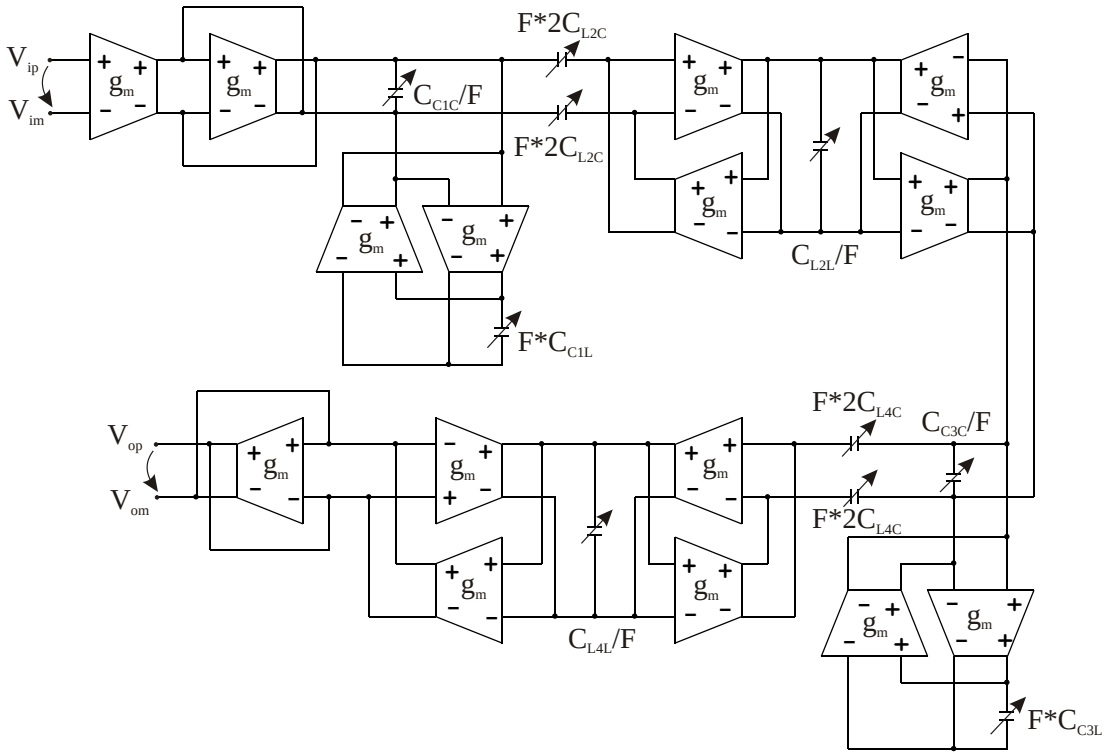


Figure 6.14: The OTA-C implementation of a complete 8^{th} order gyrator band pass filter

The schematic in this figure also emphasizes the programming of the bandwidth by changing the capacitors. The frequency scaling factor F has been previously defined. Once the filter structure is fixed and a basic set of component values has been calculated, the programming is done by selectively multiplying or dividing the capacitor values with the desired scaling factor. The variation of the capacitors can be implemented by using digitally controlled capacitor arrays as in the case of the proposed low pass filter. The basic set of component values is calculated for the narrowest bandwidth requirement as this is the setting that creates the

worst feasibility limitations. It is of importance that the transconductance of the cells must be known prior to calculating the capacitor values. The choice of the termination resistances depends on the feasible transconductance values. Typical implementable transconductance values are in the range of hundreds of μS. For an 8^{th} order Butterworth filter with 75MHz center frequency and 200kHz bandwidth the basic set of components results as given in the Table 6.1 together with the frequency scaling required for programming the bandwidth

Component	**Basic set**	**Scaled with F**
C_{C1C}	121.8pF	C_{C1C}/F
C_{C1L}	1.48fF	$F \cdot C_{C1L}$
C_{L2C}	0.61fF	$F \cdot C_{L2C}$
C_{L2L}	294.1pF	C_{L2L}/F
C_{C3C}	294.1pF	C_{C3C}/F
C_{C3L}	0.61fF	$F \cdot C_{C3L}$
C_{L4C}	1.48fF	$F \cdot C_{L4C}$
C_{L4L}	121.8pF	C_{L4L}/F

Table 6.1: The calculated set of components and the bandwidth scaling template

6.3.3.2 OTA-C band-pass filters based on state variables

Another alternative for the active implementation of the doubly terminated band pass LC ladder is to use state variables. This synthesis method first uses the state variables, namely node voltages and branch currents, to describe the functionality realized by the passive ladder [40][36][62]. The second step is to manipulate these state variables in a way that allows a simple implementation of an active circuit, that emulates the equations of the passive prototype. The starting point of the synthesis procedure is the generalized passive ladder presented in Figure 6.15 [41][42][12].

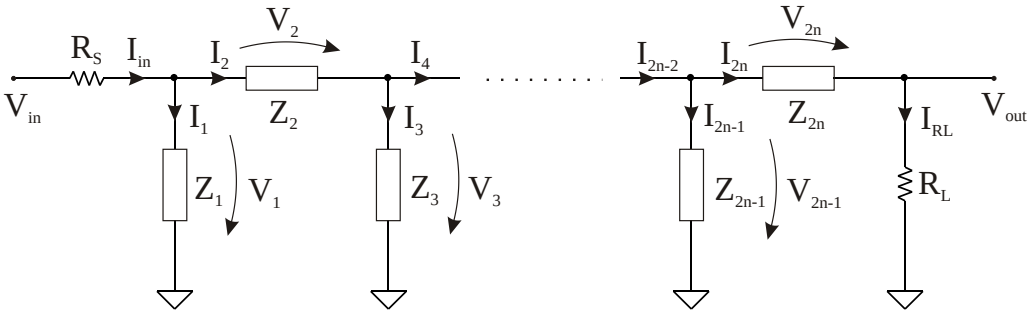


Figure 6.15: The generalized even order passive ladder used for writing the state variables

The state variables are written by applying Kirchhoff's theorems for each node and branch in the ladder. The summarized variables are given in the following system of equations:

$$\begin{cases} V_{in} - V_1 = R_S I_{in} \\ I_1 = I_{in} - I_2 \\ V_2 = V_1 - V_3 \\ I_3 = I_2 - I_4 \\ \vdots \\ I_{2n-1} = I_{2n-2} - I_{2n} \\ V_{2n} = V_{2n-1} - V_{out} \\ V_{out} = R_L I_{2n} = R_L I_{RL} \end{cases} \tag{6.26}$$

The next step in the procedure is to obtain expressions of the node voltages and the branch currents as functions of the impedances connected to every particular node. Since the equations from the system (6.26) give the branch voltages and node currents, these must be scaled with the branch impedances according to Ohm's law. It results:

$$\begin{cases} V_{in} - V_1 = R_S I_{in} \\ V_1 = Z_1 I_1 = Z_1 \left(I_{in} - I_2 \right) \\ I_2 = \dfrac{V_2}{Z_2} = \dfrac{1}{Z_2} \left(V_1 - V_3 \right) \\ V_3 = Z_3 I_3 = Z_3 \left(I_2 - I_4 \right) \\ \vdots \\ V_{2n-1} = Z_{2n-1} I_{2n-1} = Z_{2n-1} \left(I_{2n-2} - I_{2n} \right) \\ I_{2n} = \dfrac{V_{2n}}{Z_{2n}} = \dfrac{1}{Z_{2n}} \left(V_{2n-1} - V_{out} \right) \\ V_{out} = R_L I_{2n} \end{cases} \tag{6.27}$$

In order to correctly emulate the functionality of the ladder with the available active building blocks it is required to be able to sum only voltages. This necessity is imposed by the high input impedance and voltage input of the transconductance amplifiers. The equations in the system (6.27) are further scaled with a fictive

resistance R that allows the transformation of all the currents into voltages. The voltages that result from a current after scaling are marked with $\widehat{V}_i$. The scaling yields:

$$\begin{cases} \widehat{V}_{in} = \dfrac{R}{R_S}\left(V_{in} - V_1\right) \\ V_1 = \dfrac{Z_1}{R}\left(\widehat{V}_{in} - \widehat{V}_2\right) \\ \widehat{V}_2 = \dfrac{R}{Z_2}\left(V_1 - V_3\right) \\ V_3 = \dfrac{Z_3}{R}\left(\widehat{V}_2 - \widehat{V}_4\right) \\ \vdots \\ V_{2n-1} = \dfrac{Z_{2n-1}}{R}\left(\widehat{V}_{2n-2} - \widehat{V}_{2n}\right) \\ \widehat{V}_{2n} = \dfrac{R}{Z_{2n}}\left(V_{2n-1} - V_{out}\right) \\ \widehat{V}_{2n} = \dfrac{R}{R_L} V_{out} \end{cases} \tag{6.28}$$

It can be noticed that the branch impedances have been transformed into a frequency dependent transfer function between different voltages. The block diagram of the active circuit that emulates the state variables of the passive network is presented in Figure 6.16.

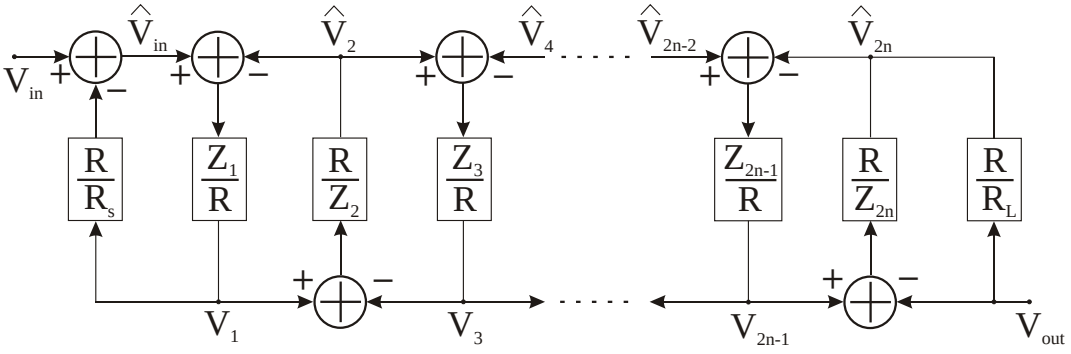


Figure 6.16: The block diagram of the active network that emulates the passive prototype

The active implementation is very straight forward if the summations are always performed at the differential input of an OTA and the scaling factor R is provided by

the reciprocal of the transconductance parameter g_m. The schematic of the circuit is shown in Figure 6.17. The single ended version has been chosen for a better overview [12].

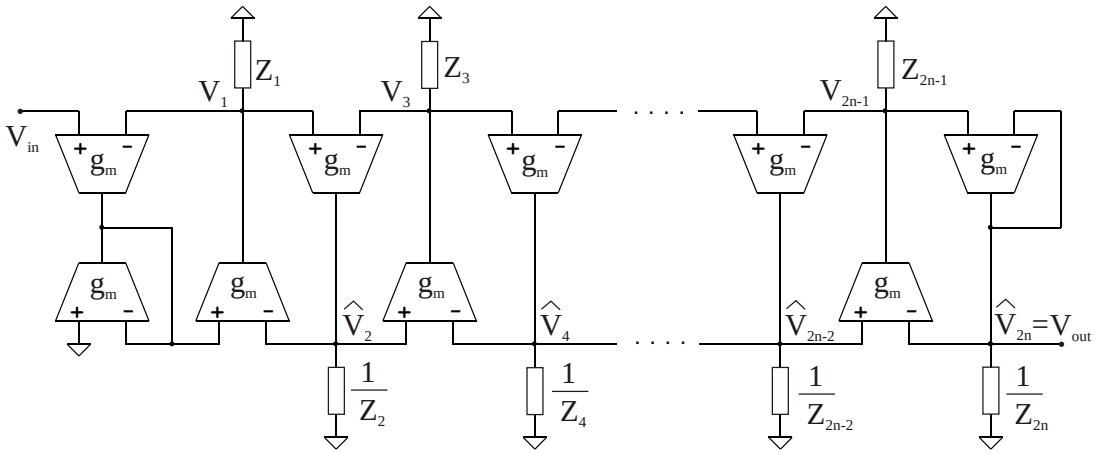


Figure 6.17: The OTA-C circuit corresponding to the block diagram in Figure 6.16

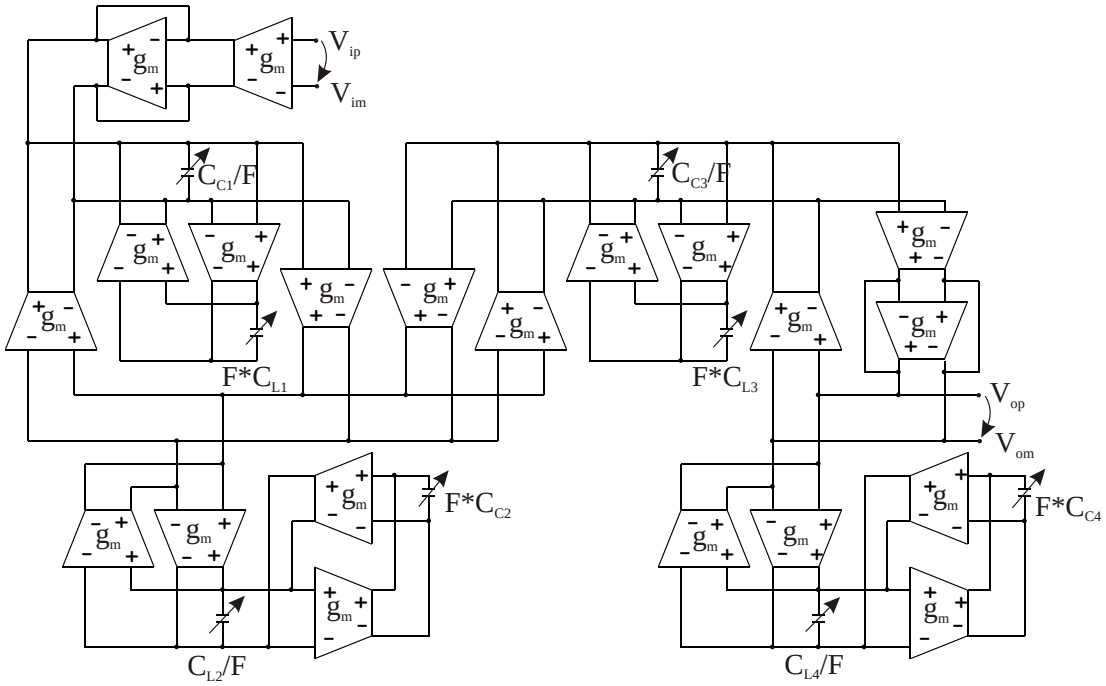


Figure 6.18: The fully differential implementation of an OTA-C band pass filters with state variables

It is of great importance that the structure above is very general and it can be applied to design low pass, high pass, band pass and band reject filters [41][42]

with and without transmission zeros. In order to change the filter type only the specific impedances must be changed according to the frequency transformations. Note that the impedances are not always simple inductors or capacitors, but they can be implemented as various series and parallel LC structures corresponding to a given LC ladder filter implementation, as already shown in Figure 6.5. The inductors from the LC groups and the termination resistances are implemented the same way as discussed for the gyrator filters. According to the presented design algorithm, the structure of an 8^{th} order band pass filter can be realized as given in Figure 6.18.

Similarly as in the case of gyrator filters, the programming of the bandwidth is simple and only implies either a multiplication or a division of the capacitors with the frequency scaling factor F. The basic set of component values and the programming template are given in Table 6.2. Although the implementation and the synthesis method are different, the component values are identical as for the gyrator filter. This is due to the fact that both structures emulate the functionality of the same passive prototype.

Component	**Basic set**	**Scaled with F**
C_{C1}	121.8pF	C_{C1}/F
C_{L1}	1.48fF	$F \cdot C_{L1}$
C_{C2}	0.61fF	$F \cdot C_{C2}$
C_{L2}	294.1pF	C_{L2}/F
C_{C3}	294.1pF	C_{C3}/F
C_{L3}	0.61fF	$F \cdot C_{L3}$
C_{C4}	1.48fF	$F \cdot C_{C4}$
C_{L4}	121.8pF	C_{L4}/F

Table 6.2: The calculated set of components and the bandwidth scaling template for the state variable OTA-C band pass filter

From an analysis of the basic set of component values for both the gyrator and the state variable band pass filters it can be seen that, despite of the very good scalability of the bandwidth, these filter implementations are not feasible for narrow bandwidths and high center frequencies. The explanation for this is the following: all the capacitors originating from transversal inductance or a longitudinal capacitance in the passive LC ladder prototype are proportional to $1/Q_{BP}\omega_C$. For large center frequencies and narrow bandwidths these capacitors will result very small. In exchange capacitors originating from transversal capacitances and longitudinal inductances are proportional only to $1/BW$ and for narrow bandwidths will result very large. This causes a massive spread in component values. Furthermore, the absolute values of the capacitances are either too large to be implemented, or too small. The very small capacitances are overdriven by the inherent parasitics of the active circuits and even of the metal connections on the circuit surface.

6.3.4 Band-pass biquad filters

In the paragraph 6.2.1 it has been shown that filters built using cascades of second order band pass sections are not suitable for scaling the bandwidth. The demonstration has been done under the assumption that the approximation of the filter should be maintained regardless of the bandwidth setting.

The discussed realization methods of gyrator and state variable band pass filters have demonstrated that these filters exhibit a very good scalability of the bandwidth, but they are not feasible for narrow bandwidth implementations.

Although band pass filters implemented with second order sections are not scalable for a constant approximation, an intuitive approach to different biquads [62] demonstrates that these filters are able to trade the approximation for feasibility and flexibility. Furthermore, there are some realization techniques in the literature that use less conventional approaches to high Q filters with variable bandwidth [35][38][45]. These techniques are almost entirely based on cascades of second order sections. The following paragraphs present some of these filter realizations, suitable for systems where a variation of the group delay, ripples in the passband and the approximation is not of concern.

6.3.4.1 OTA-C biquad filters

The transfer function of the second order band pass section is obtained after a frequency transformation and a symbolical factorization of the resulting fourth order polynomial. When the approximation is not of concern, the coefficients of the terms in s from the transfer function of the filter are defined with much less restriction. In these cases they can be calculated by simply considering the standard form of the second order band-pass transfer function, written as follows:

$$H(s) = H_0 \cdot \frac{\frac{\omega_0}{q}s}{s^2 + \frac{\omega_0}{q}s + \omega_0^2} \tag{6.29}$$

In the approach without a specific approximation the resonant frequency ω_0 of each second order section corresponds to the desired center frequency of the filter. The required pole quality factors, noted with q, can be computed as functions of the filter quality factor, Q_{BP}. The first step in this calculation implies writing the expression of the magnitude response associated with the second order section. This is:

$$|H_{bq}(s)|_{s=j\omega} = \frac{H_0\omega_0\omega}{\sqrt{\omega^2\omega_0^2 + q^2\left(\omega_0^2 - \omega^2\right)^2}} \tag{6.30}$$

If the biquadratic sections, used to build an n^{th} order band pass filter, are assumed to be identical, then the magnitude response of the filter is $\left|H_{bq}^{n/2}(s)\right|$. In order to derive the connection between the filter quality factor and the pole quality factor it is necessary to calculate the -3dB corner frequencies of the entire filter. This is done by equaling the magnitude response with -3dB and solving the equation for ω.

$$\left[\frac{H_0^2 \cdot \frac{\omega_0^2}{q^2} \cdot \omega^2}{\omega^4 + \omega_0^2\left(\frac{1}{q^2} - 2\right)\omega^2 + \omega_0^4}\right]^{\frac{n}{4}} = 10^{-3/20} \tag{6.31}$$

The two -3dB corner frequencies, ω_{-g} and ω_g, are of the form:

$$\begin{cases} \omega_{-g} = \dfrac{\omega_0}{\sqrt{2}q} \cdot \sqrt{x - \sqrt{y}} \\ \omega_g = \dfrac{\omega_0}{\sqrt{2}q} \cdot \sqrt{y + \sqrt{y}} \end{cases}, \tag{6.32}$$

where x and y are written as follows:

$$\begin{cases} x = 2q^2 + \dfrac{H_0}{0.707^{4/n}} - 1 \\ y = \left(1 - \dfrac{H_0}{0.707^{4/n}}\right)\left(1 - 4q^2 - \dfrac{H_0}{0.707^{4/n}}\right) \end{cases} \tag{6.33}$$

The calculation of the pole quality factors is done by taking into the account that $\omega_g - \omega_{-g} = BW$, expressed in rad/s. The symbolical expression of the pole quality factor is very complicated. Therefore, its detailed derivation is not discussed here. The numerical solution can be inferred for any $q - Q_{BP}$ quality factor pair. As a consequence, the filter bandwidth can be always determined with respect to a reference bandwidth, corresponding to a reference pole quality factor that has been numerically determined. The programming of the bandwidth only depends on changing the ratio between different pole quality factors and a reference value. This can be done by simply scaling some components in the circuit with the frequency scaling factor factor F. The programming template is derived from a certain biquad structure that is replicated in higher order filter realizations. It is also of importance that the all the biquads in a filter structure must be identical in order to avoid large pass band ripples and a significant attenuation of the wanted signal.

The typical schematic of an OTA-C band pass biquad is presented in Figure 6.19 [30][62][53]. This schematic has been drawn single ended for an easier overview. In practical designs the transconductors are fully differential.

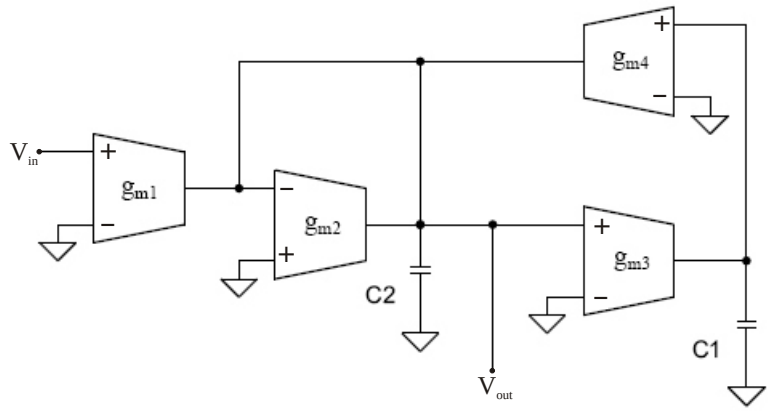


Figure 6.19: Typical schematic of an OTA-C band pass second order section

The transfer function of the circuit is given by the equation (6.34):

$$H(s) = \frac{g_{m1}}{g_{m2}} \cdot \frac{\frac{g_{m2}}{C_2}s}{s^2 + \frac{g_{m2}}{C_2}s + \frac{g_{m3}g_{m4}}{C_1C_2}} \tag{6.34}$$

The sizing equations of the circuit can be written by identifying the coefficients of the terms in s from the relations (6.29) and (6.34). It result:

$$\begin{cases} H_0 = \dfrac{g_{m1}}{g_{m2}} \\ \dfrac{g_{m2}}{C_2} = \dfrac{\omega_0}{q} \\ \dfrac{g_{m3}g_{m4}}{C_1C_2} = \omega_0^2 \end{cases} \tag{6.35}$$

The resonant frequency and the quality factor can be expressed as functions of the circuit parameters as follows:

$$\begin{cases} \omega_0 = \sqrt{\dfrac{g_{m3}g_{m4}}{C_1C_2}} \\ q = \sqrt{\dfrac{g_{m3}g_{m4}}{g_{m2}^2} \cdot \dfrac{C_2}{C_1}} \end{cases} \tag{6.36}$$

For simplicity and better matching all the transconductance parameters can be taken equal. In this case the resonant frequency and the pole quality factor becomes:

$$\begin{cases} \omega_0 = \dfrac{g_m}{\sqrt{C_1 C_2}} \\ q = \sqrt{\dfrac{C_2}{C_1}} \\ g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_m \end{cases} \tag{6.37}$$

The programming template should modify only the bandwidth while the center frequency is held constant. Since the quality factor of the band pass filter is proportional to the reciprocal of the bandwidth, it is also proportional to the reciprocal of the bandwidth scaling factor F; thus a multiplication of the quality factors by $1/F$ in each biquad yields an F times larger bandwidth. The required modifications in the capacitance values are described by the following identities:

$$\begin{cases} \omega_0^* = \omega_0 \\ q^* = \dfrac{q}{F} \end{cases} \Rightarrow \begin{cases} \dfrac{g_m}{\sqrt{C_1 C_2}} = \dfrac{g_m}{\sqrt{k_1 \cdot C_1 \cdot k_2 \cdot C_2}} \\ \sqrt{\dfrac{C_2}{C_1}} = \sqrt{\dfrac{k_2 \cdot C_2}{k_1 \cdot C_1}} \end{cases}, \tag{6.38}$$

where k_1 and k_2 are the scaling factors of the capacitors C_1 and C_2. From the calculations results that $k_1 = F$ and $k_2 = 1/F$. The sizing of the capacitors takes into account the feasibility of the transconductance amplifier implementations. For example, when $g_m = 400\mu$S and the center frequency is 75MHz, a q equal to 20 together with the capacitances $C_1 = 42.4fF$ and $C_2 = 16.96pF$ yield a bandwidth approximately equal to 1.6MHz. When comparing the component sizes with the values from the tables 6.1 and 6.2 it results that the feasibility has been significantly improved.

6.3.4.2 Band-pass filters derived from VCO-s

Oscillators have a very narrow bandwidth and the frequency response is centered on the oscillation frequency. The oscillator quality factor is determined by the phase noise generated by the circuit [56][37]. Ring oscillators are realized usually with a cascade of an odd number of open-loop inverting amplifiers (delay stages) in a ring feedback structure. These delay stages are often simple integrators with some loss introduced by non-zero output conductances of the transistors or intentionally in order to place the poles to a desired location in the s plane. The pole locations are depending on the loss in the delay stages. There is also the requirement that sets the pole locations for the complex conjugate pole pairs in the right half plane to maintain oscillations. If too much loss is added, the poles will move to the left half

plane, the circuit is stabilized and the oscillations will cease. A stable VCO will behave like a band-pass filter with inherently high quality factor. In the simulations all the delay stages have been modeled with OTA-C lossy integrators [10].

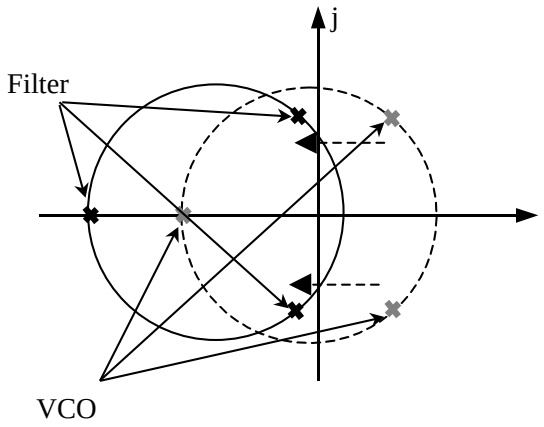


Figure 6.20: Pole locations of the VCO and the derived filter

The poles of an n-stage VCO are located on a circle defined by the unity-gain bandwidth and the pole of the lossy integrators as presented in Figure 6.20. If additional loss is added to the loop the poles can move leftwards in the left half plane to stabilize the circuit. This will result in a low-pass transfer function. In order to obtain a band-pass transfer function a zero must be added near the origin. The input of the filter is added to one of the lossy integrators in the loop. The block diagram of the filter is presented in Figure 6.21. The corresponding OTA-C implementation is shown in Figure 6.22 [10].

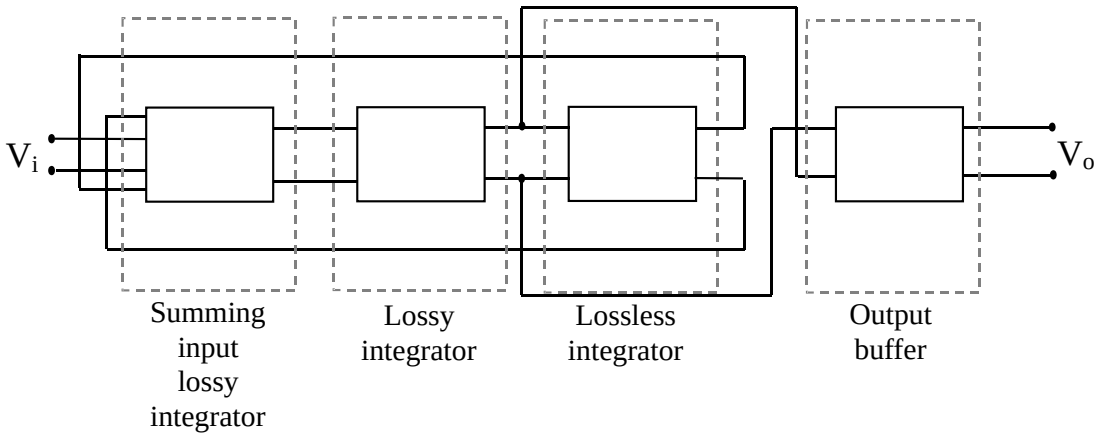


Figure 6.21: Block diagram of the VCO derived band-pass filter

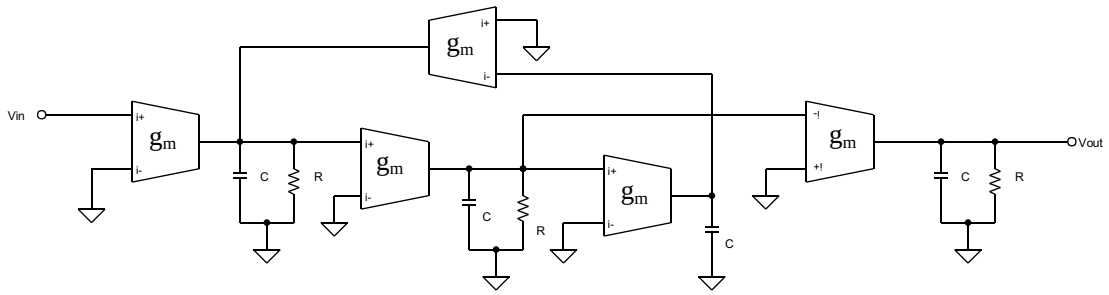


Figure 6.22: OTA-C implementation of the VCO derived band-pass filter

The transfer function of the filter is given by the equation (6.39).

$$H(s) = \frac{g_m^3 R^3 C s}{(1 + sRC)\left[sC \cdot (1 + sRC) + g_m^3 R^2\right]} \tag{6.39}$$

The simulated magnitude response for different g_m values is presented in Figure 6.23.

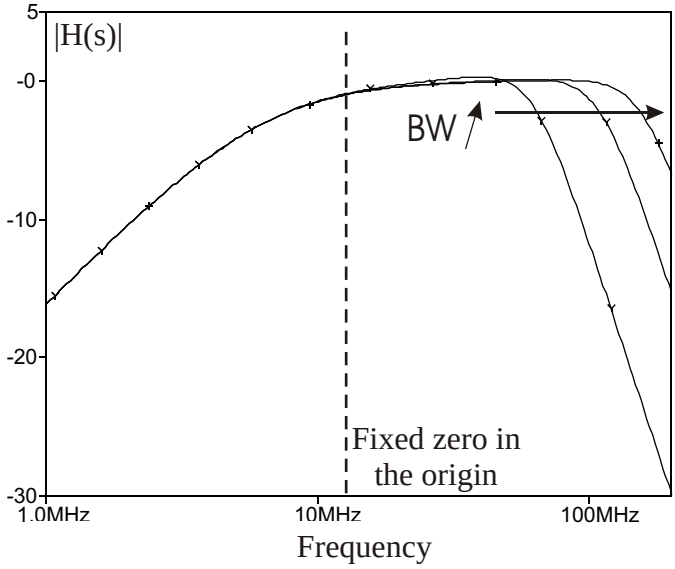


Figure 6.23: Simulated magnitude responses of the band-pass filter for different g_m values

The main drawback of this architecture is that the bandwidth cannot be modified independently from the center frequency. The lower limit of the pass-band is set by the position of the zero near the origin, determined by the unity-gain bandwidth of the delay elements. Changing the lower corner frequency would mean to change the time constants of the integrators. This task can be difficult if it is to be done

simultaneously with center frequency tuning and modifications in the transconductance values. Additionally the zero in the origin does not offer sufficient attenuation at lower frequencies. As a consequence the blocking signal around the wanted spectral components are not evenly attenuated. Furthermore the transfer function of the VCO derived band pass filter cannot be implemented for a standard approximation. In conclusion the VCO derived band-pass filters offer a sufficiently high frequency operation but they are not suitable for IF filtering in multi mode receivers.

6.3.4.3 Active LC band-pass filters with Q enhancement

The structure of active LC band-pass filters is derived from the classical OTA-C active biquads by replacing some components with an equivalent passive LC resonant tank circuit. The architecture of the filter is similar to a VCO but its parameters can be significantly better controlled by means of an input transconductance buffer and by correctly sizing the RLC elements.

The schematic of the typical OTA-C band-pass biquad can be redrawn as presented in Figure 6.24 [35]. The RLC equivalent structure can be determined if we consider that g_{m2} implements a resistor to ground and g_{m3} together with g_{m4} represent a gyrator that inverts the capacitance C_1, transforming it to an inductance. The resulting second order ideal circuit is given in Figure 6.25.

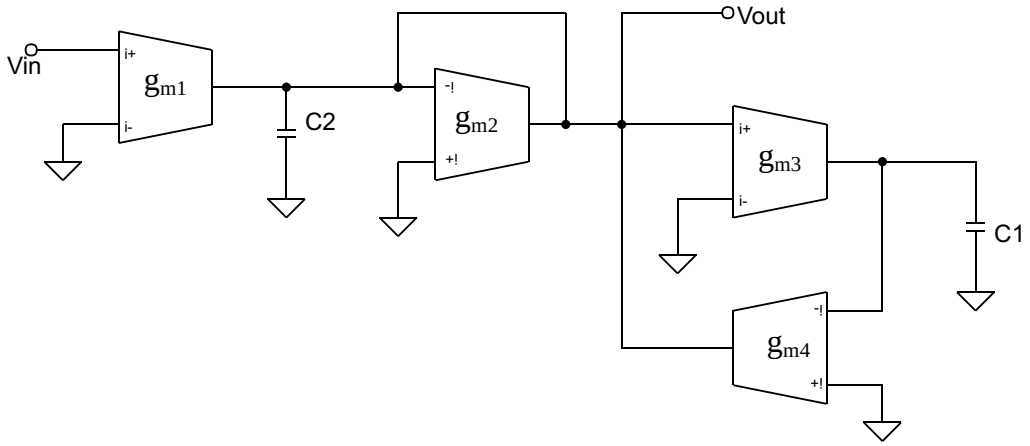


Figure 6.24: Redrawn schematic of the band-pass biquad from Figure 6.19

The transfer function of the circuit is given by the equation (6.40).

$$H(s) = \frac{\frac{g_m}{C}s}{s^2 + \frac{1}{RC}s + \frac{1}{LC}} \tag{6.40}$$

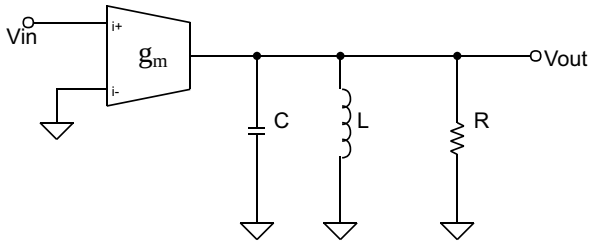


Figure 6.25: RLC equivalent of the band-pass biquad

The resistance R includes the loss resistance of the inductor. The quality factor of the second order band-pass filter is proportional to this equivalent resistance. At frequencies above a few tens of MHz and high Q requirements band-pass filters are very difficult to implement due to parasitic capacitances in circuit elements and interconnects and due to large spreads in component values. The main advantage of the RLC circuit is that the parasitics can be absorbed into the circuit and compensated. Usually passive circuits can implement band-pass structures without the need of active circuits but the achievable values of filter quality factors are limited by the component (typically inductance) Q-s. Finite inductance quality factors can be compensated by means of active circuits [35][38].

The quality factor limitation of the inductance comes from the loss resistance. This loss resistance can be compensated with a negative resistance connected in parallel with the inductance. This will result in increasing the equivalent resistance and implicitly the quality factor of the filter. The transfer function of the circuit becomes:

$$H(s) = \frac{\frac{g_m}{C}s}{s^2 + \frac{R_{neg} - R}{R_{neg}RC}s + \frac{1}{LC}} \tag{6.41}$$

From this equation can be seen that the q of the biquad can be modified by means of the negative resistance, independently of the center frequency. In literature this procedure is called Q enhancement[35][38]. The active LC structure allows an implementation with the desired filter approximation but this makes no sense due to the mathematical limitations discussed in the paragraph 6.2.1. Similarly as for the OTA-C band pass biquad filters the emphasis lays on trading the approximations for feasibility and flexibility. In fact, this circuit can be considered as an enhanced implementation of the transconductor based band pass biquad filters. The component sizing and the programming of the bandwidth are using the same principles. If the transfer function is written in the standard form given in the equation (6.29), then the in-band gain, the resonant frequency and the quality factor of the poles can be identified as follows:

$$\begin{cases} H_0 = g_m \cdot \dfrac{R \cdot R_{neg}}{R_{neg} - R} \\ \omega_0 = \dfrac{1}{\sqrt{LC}} \\ q = \dfrac{R \cdot R_{neg}}{R_{neg} - R} \cdot \sqrt{\dfrac{C}{L}} \end{cases} \tag{6.42}$$

In comparison with the classical OTA-C biquad filter discussed in the previous paragraphs, the Q enhancement improves the feasibility of the circuit while it maintains the inherent flexibility of the bandwidth programming template. The bandwidth can be modified by scaling the inductance and the capacitance in the classical way with the bandwidth scaling factor F. Additionally, the Q enhancement offers a very good tool to improve the extreme component values resulting from narrow bandwidth specifications.

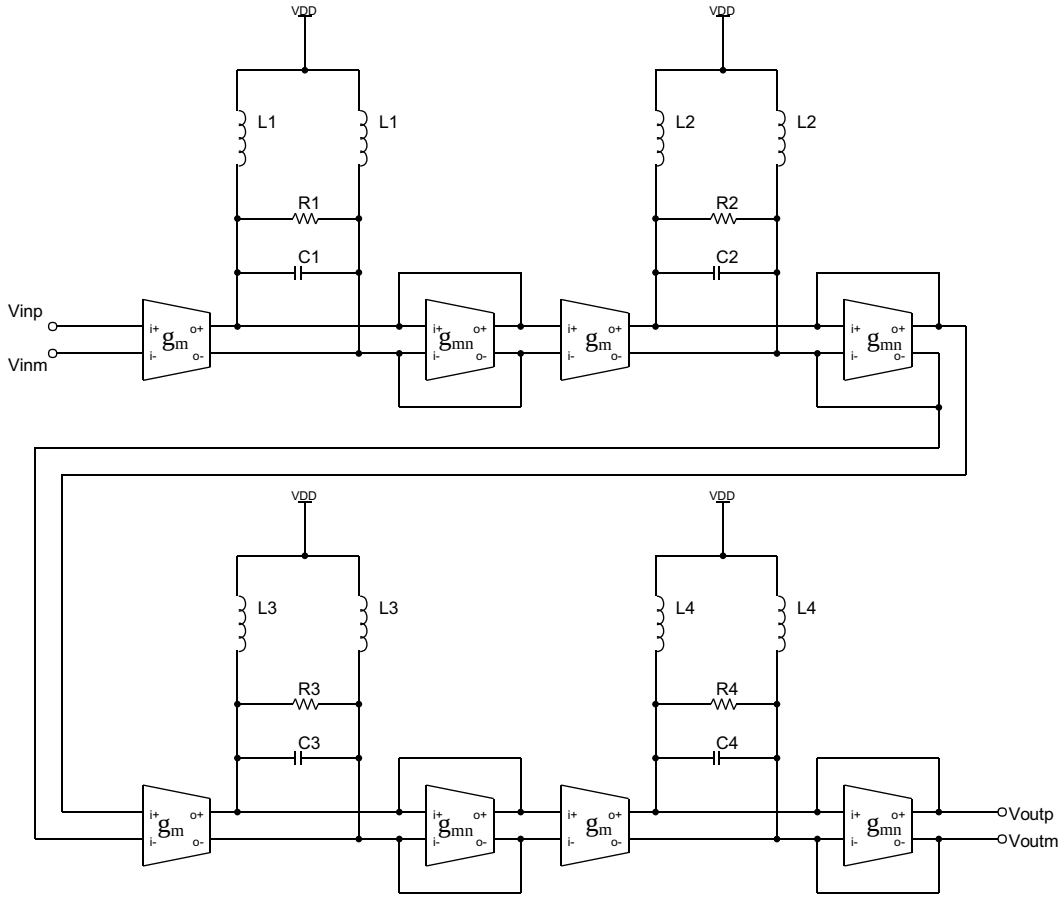


Figure 6.26: Differential implementation of the 8th order band-pass filter

In the numerical design example given at the end of the paragraph 6.3.4.1 the q has been chosen to be equal to 20, yielding a 1.6MHz bandwidth. A quality factor enhancement, that increases the q only 4 times yields a bandwidth of around 400kHz which is close to the minimum bandwidth specifications of the filter. It is of importance that the values of the critical components L and C have not been changed and are feasible in spite of the decreased bandwidth. The complete implementation of an 8^{th} order Q enhanced LC band-pass filter is presented in Figure 6.26. Common mode feedback has been omitted here for a better overview.

The main drawback of the Q enhancement method is the fact that the in-band gain is also dependent on the equivalent resistance. If the quality factor is scaled with the factor $1/F$ in order to modify the bandwidth, then also the gain of each filter section will be increased with this factor. As a consequence, the gain of the filter must be controlled with external circuits such as a programmable attenuator.

6.3.4.4 OTA-C Q-enhanced band-pass filters

The main disadvantage of the Q-enhanced LC filter presented in the previous paragraph was that its implementation required the use of a passive LC tank circuit. The integration of inductances is possible in a very limited range of values. A possibility to avoid the use of external components is to electronically implement the inductance through an impedance inversion. The procedure is the same as for OTA-C filters with gyrators. The grounded resistance is also implemented with a transconductor cell. The result is the classical Tow-Thomas biquad with Q enhancement [15]. The schematic of this circuit is given in Figure 6.27.

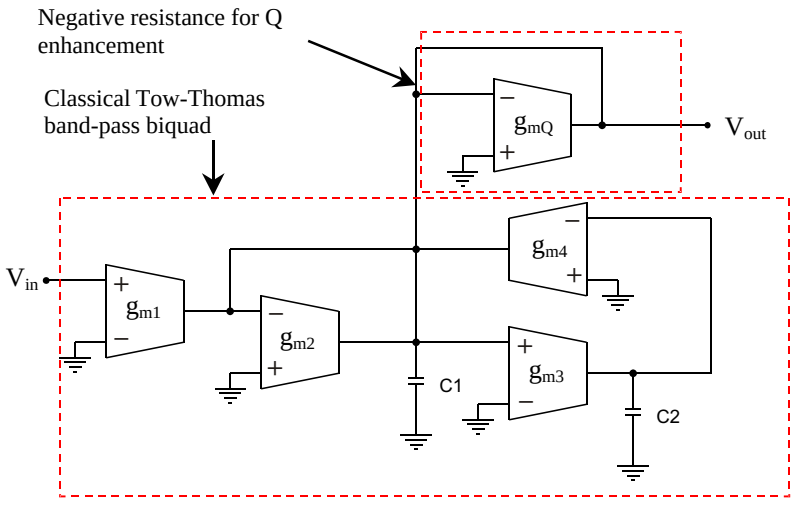


Figure 6.27: Schematic of an OTA-C band-pass biquad with Q enhancement

The transfer function of the circuit is given by equation (6.43):

$$H(s) = \frac{\frac{g_{m1}}{C_1}s}{s^2 + \frac{g_{m2} - g_{mQ}}{C_1}s + \frac{g_{m3}g_{m4}}{C_1C_2}} \tag{6.43}$$

The resulting center frequency and the quality factor are defined by the equations (6.44).

$$\begin{cases} \omega_0 = \sqrt{\frac{g_{m3}g_{m4}}{C_1C_2}} \\ q = \sqrt{\frac{C_1 g_{m3} g_{m4}}{C_2 \left(g_{m2} - g_{mQ}\right)^2}} \end{cases} \tag{6.44}$$

It can be observed that the center frequency and the quality factor can be tuned independently. The simulated magnitude response of the biquad is given in Figure 6.28.

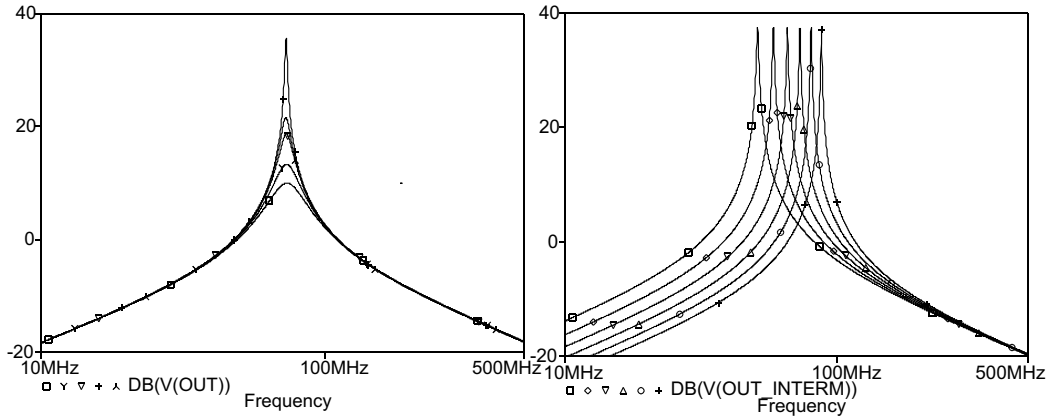


Figure 6.28: Simulated magnitude responses of the biquad for center frequency and quality factor tuning

The bandwidth programming template is the same as for the classical OTA-C band pass biquad, but the negative resistance must also be taken into account. The circuit eliminates the need of an off chip inductance and improves the feasibility of the OTA-C second order sections. The main benefit is the improved feasibility while the flexibility of the circuit remained the same.

6.3.4.5 Band-pass filters with structures based on current conveyors

An alternative implementation of transconductance amplifiers uses current conveyors as active elements. The possible improvement over the classical transconductance cells is the fact that the value of the transconductance parameter is determined by passive resistors that have a much wider range of variation than complex differential stages. This allows a better control of the filter parameters in the already discussed band pass biquads and even in scalable state variable or gyrator filters. The implementation technique with current conveyors is only meant to further improve the feasibility of the classical circuits by extending the range of variation for the active elements.

The operation of a second generation current conveyor can be described by using the following relations [34]:

$$\begin{cases} V_x = V_y \\ I_y = 0 \\ I_z = \pm I_x \end{cases} \tag{6.45}$$

The fully differential OTA-C circuit can be derived from the current conveyor by balancing the circuits and by employing the voltage inputs Y of each current conveyor. The resulting transconductance amplifier and the voltage mode biquad are given in Figure 6.29 and 6.30.

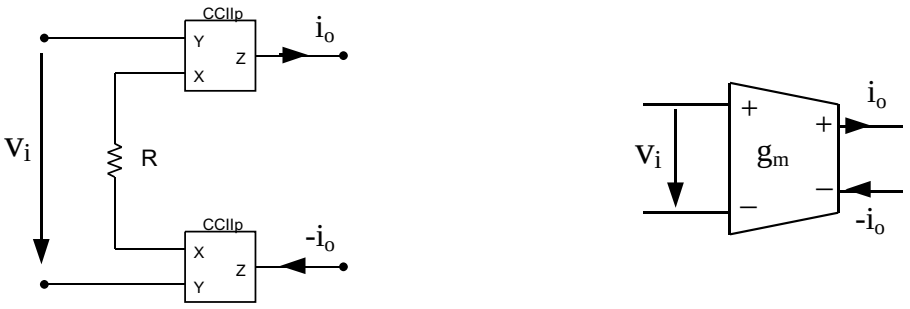


Figure 6.29: Implementation of a fully differential transconductance amplifier with current conveyors

The transfer function of the second order filter is given by equation (6.46):

$$H(s) = \frac{\frac{1}{R_1 C_1} s}{s^2 + \frac{1}{R_2 C_1} s + \frac{1}{R_3 R_4 C_1 C_2}} \tag{6.46}$$

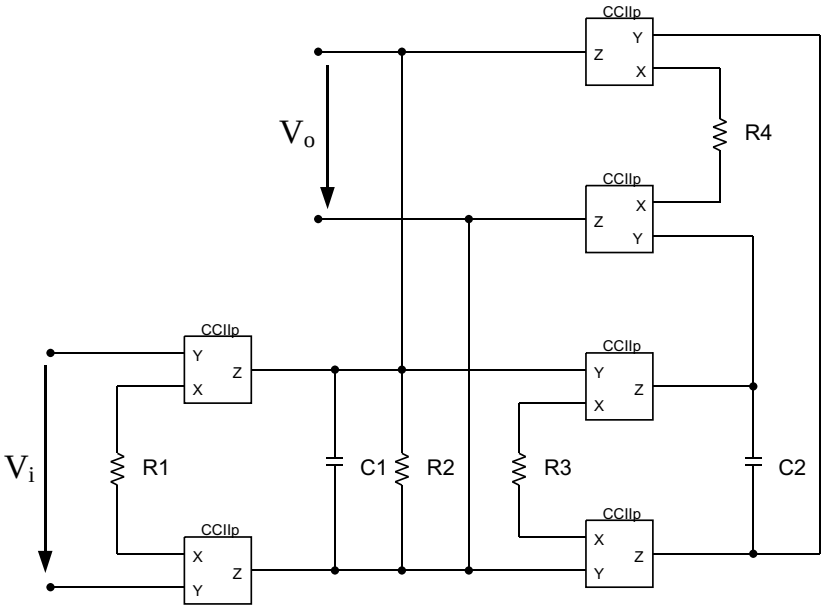


Figure 6.30: Schematic of the Tow-Thomas biquad implemented with the current conveyor transconductance amplifier

This transfer function is equivalent to the one given by equation (6.34), where all the transconductance values can be calculated as a reciprocal of the corresponding resistance. The advantage of the circuit implemented with current conveyors is that the resistances can vary in a much larger range compared to transconductance values. The higher limit is still given by the noise but the lower limit is defined by technology; thus, theoretically, very large transconductance values can be implemented. This improves feasibility of narrow band filters.

In practice there are several problems occurring when the center frequency is large and the bandwidth is small. These problems are strongly related to the parasitic effects due to non-idealities of the current conveyor cells. The most important to consider are the non-zero input resistance of the X terminals, the finite output resistance of the Z terminals and the parasitic capacitances at the Z nodes. By careful design these effects can be absorbed to some extent into the passive components. The input impedance of the X terminal can be minimized to a value of tens of Ω using negative feedback. In order to be absorbed in the passive components the Z terminal output resistance must be larger than the value of the total required resistance R_2. This condition practically limits the achievable filter quality factor.

Another drawback of this circuit is its sensitivity to component tolerances. The filter retains all the tuning problems of the classical Gm-C biquad filters. Due to the problems regarding the guaranteed bandwidth after center frequency tuning a filter implemented using this method cannot have very large quality factors and cannot be used for channel filtering.

The main advantage of the filter created with current conveyors is its improved linearity, lower consumption and better programmability. The good programmability is strongly related to the use of passive RC components and an to an increased control over the filter parameters that define the transfer function.

6.4 Limitations of the high frequency and high Q band pass filter feasibility

From the previous paragraphs it becomes obvious that there are several factors that could prove to be prohibitive regarding a high center frequency and narrow bandwidth band pass filter implementation. Among these factors the most important are the following:

- **The lack of flexibility**

This limitation is typically associated with the need to change multiple components in the filter structure in order to conserve the approximation during the bandwidth adjustment procedure. In the case of biquad filters this leads to stringent requirements for matching and sophisticated algorithms in changing each individual component. Furthermore, the tuning of the components must be somehow controlled in order to produce the expected variation of the frequency response. The errors and non-idealities could produce a significant distortion of the response. However, filters developed from a doubly terminated passive LC prototype exhibit a very good scalability of the bandwidth and the implementation of the programming template proves to be simple and efficient.

- **The precision of the frequency setting**

The precision is another bottleneck in the way of narrow bandwidth realizations. This factor determines the attenuation error to be expected when the frequency parameters are controlled within given range around their ideal value. For example, if the band pass filter is designed with consideration on the GSM standard, the bandwidth is set to 200kHz. A $\pm 1\%$ bandwidth and centre frequency error produces unacceptably high attenuation of the wanted signal while adjacent channels are passed unaltered. The simulated magnitude response of an 8^{th} order Butterworth filter with 75MHz centre frequency and 200kHz bandwidth is shown in Figure 6.31.

It results that the guaranteed minimum bandwidth of the filter is determined by the tuning precision of the center frequency. Practical precision of the center frequency tuning circuit is not better than about $\pm 5\%$ [53]. A theoretical bandwidth of 5MHz and a $\pm 5\%$ tuning precision only yields approximately 1.2MHz guaranteed bandwidth, but the approximation is completely lost. From these reasons follows that, even with scaling, in IF sampling receivers the band-pass filter is only usable as band filter. Narrow bandwidth channel filtering must be performed elsewhere in the chain.

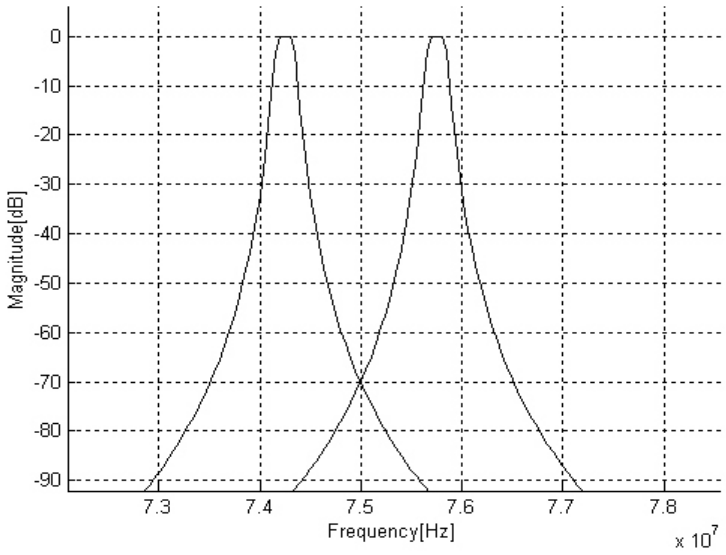


Figure 6.31: The band pass filter transfer function for ±1% centre frequency and bandwidth errors

- **The component spread**

The high spread in the component values results from the characteristics of the low pass to band pass frequency transformation. Usually the equivalent inductance and the capacitance values will be moved to opposite senses through the frequency transformation. For narrow bandwidth the shift is sufficiently large to bring the resulting inductances, the capacitances or even both to values that cannot be implemented monolithically or due to parasitics. This problem becomes less stringent when the quality factor of the filter is lowered. Although the approximation can be traded to sufficiently improve the feasibility, the lack of precision still leads to the idea of band filtering rather than channel filtering.

- **The corner frequency error compensation**

In the previous paragraphs it has been shown that the frequency response of the band pass filter is extremely sensitive to component tolerances. The programming template of the bandwidth should include some correction circuit that compensates for process tolerances and temperature variations. There are several approaches to center frequency and Q tuning in the literature [53][62][11] but none of these exhibits the flexibility required for a wide band tuning of the bandwidth. The problem of including the compensation circuit in the programming template is still an open question.

6.5 Conclusions

The aim of the material presented in this chapter was to analyze the theory and some implementations of high frequency and high Q band pass filters intended for

IF sampling software defined radio architectures. The main concern lays on the programmability of the bandwidth without changing other parameters in the band pass transfer function, on the feasibility of a physical realization and on the precision. The precision gains a special importance when signal integrity requirements are considered. The summary of the obtained results is given in Figure 6.32.

		With approximation			No approximation		
		Programmability	Feasibility	Precision	Programmability	Feasibility	Precision
LC filters	State variables	Good - simple capacitive template	Very low for high Q	Very low for high Q	Good - simple capacitive template	Average - Improved for lower Q	Very low for high Q
	Gyrators	Good - simple capacitive template	Very low for high Q	Very low for high Q	Good - simple capacitive template	Average - Improved for lower Q	Very low for high Q
Biquad filters	OTA-C	Low	Average	Very low for high Q	Good - simple capacitive and/or OTA template	Average	Very low for high Q
	Q-enhanced	Low	Average	Very low for high Q	Good - simple capacitive and/or OTA template	Average	Very low for high Q
	CCII OTA-C	Low	Improved compared to OTA-C	Low but improved by an RC template	Good - simple capacitive and/or resistive template	Improved compared to OTA-C	Low but improved by an RC template

Figure 6.32: Summary of the reconfigurable band pass filter feasibility study

The theoretical approach to band pass filter design has shown that there are two main directions in designing filters with the desired order, selectivity and approximation. The first approach is to perform the low pass to band pass frequency transformation on a doubly terminated low pass LC prototype and then to implement the resulting band pass ladder filter with equivalent active elements. Due to the nature of the passive ladder these filters proved to be highly scalable in what is concerning the bandwidth. However, their application on silicon is strongly limited by feasibility issues. The frequency transformation introduces large spreads in the component sizes and extreme values that cannot be implemented either because of area considerations or because of the inherent parasitics. The precision of the magnitude response is also low for large quality factors due to inherent process tolerances that cannot be fully compensated in real circuits. This can lead to undesired attenuations of the wanted signal. The active implementations of LC filters exhibit

similar performances also when the approximation is ignored.

The second direction is using a low pass to band pass frequency transformation and the factorization of the transfer function in elementary second order terms that can be implemented in real circuits. It has been demonstrated that, although the scalability of the bandwidth is not satisfactory, the biquad filters and their derivatives are suitable for trading the approximation for an improved feasibility and flexibility. The techniques for biquad filter design, that have been discussed in this chapter, are meant to reduce the component spread and to allow the modification of the bandwidth by electronically enhancing the circuit parameters. The conclusions to the presented research is that high frequency band pass filters are suitable for band filtering applications rather than high frequency channel filtering, due to the limited precision of real implementations. The possible application of these filters in a software defined radio architecture also depends on the decision to tolerate filter imperfections such as ripples in the pass band, gain variations and variable group delay variations for different bandwidth settings. A lowering of the center frequency together with an increase of the bandwidth improves both the feasibility and the flexibility of the physical circuit realizations.

Chapter 7

Conclusions and Research Perspectives

The research presented in this dissertation has been focused on analyzing the possibilities of implementation for fully programmable filters intended for software defined radio receivers. The work starts from the assumption that the realization of an ideal software defined radio faces many challenges that force impossible specifications on the receiver components. From this follows that the ideal flexibility can only be approximated by todays receiver architectures, whose building blocks support full reconfigurability by software. A short analysis on the receiver architectures reveals the advantages and shortcomings of the most often used receivers, namely the super heterodyne, the direct conversion and the high frequency IF sampling architectures. Among these the direct conversion and the IF sampling receiver offer the required flexibility in compliance with the software radio concept. This is the reason why the work has been concentrated on filter implementations suitable for these two receivers.

The main motivation behind fully reconfigurable receiver implementations is the necessity to support multiple services in a single device, each service having its own modulation, data encryption algorithm and carrier frequency range. It has been shown that, regardless of the considered communications standard, the frequency spectrum of the received signal always has a similar shape. Usually the wanted signal has a very low amplitude and is buried in large blocking signals from the adjacent channels and out of the signal band. In order to be correctly converted into the digital domain for further processing, the wanted signal must be selectively amplified, while the interferers should be attenuated below the acceptable limits. The main purpose of the analog signal processing before the analog-to-digital conversion is to adapt the signal properties to the full scale of the ADC and to lower the dynamic range requirements of the converter. The operations that allow this are the filtering and the amplification with a variable gain.

The approach to the filtering problem depends on the target receiver architecture. The high dynamic range filtering in direct conversion receivers is done in the

base band. Therefore, this architecture needs a low pass filter for a correct functionality. In exchange, since the signal is sampled at the intermediate frequency, IF sampling receivers require high frequency band pass filters. The band pass filter implementations described in the literature are mainly using some form of active LC filters with an electronic compensation of the inductance finite quality factors. A wide band programmability has not been discussed so far due to technological limitations

A survey of the existing literature has shown that there are several attempts to implement the required wide band reconfiguration of the -3dB corner frequency of low pass filters. The most interesting solutions are based on a current division network that virtually scales the capacitors of a fixed frequency filter, achieving this way a large programming range for the filter corner frequency. The precision of this method proves to be limited due to the shortcomings of the current division network, whose equivalent resistance depends on the programming code when a small DC offset is present at its output connections. Authors suggest that the loading effect can be neglected if the resistors in the circuit are chosen to be large compared to the equivalent resistance of the division network. However, this method generates a lot of noise and it is only effective at lower frequencies and for low offset voltages. Simulations have shown that the current through the division network can even be inverted, which means that the filter functionality is not conserved correctly. Other approaches have tried to exploit the good flexibility of resistor, capacitor and transconductance amplifier arrays. These solutions usually support the automatic tuning of the corner frequency along with eventual coverage of some well defined communications standards.

One of the main contributions in this work lays on the development of a programming algorithm and template suitable for implementing reconfigurable low pass filters based on resistor and capacitor arrays. The required resolution is achieved by switching both the resistors and the capacitors in an opamp-RC biquad filter. The switching template has been optimized to eliminate the multiple correspondence between a single corner frequency and multiple programming codes. A special care has been taken on reducing the inherently large gaps in frequency introduced by switching the components in octaves on the logarithmic axes. The proposed template uses a procedure, called here segmentation, which builds the list of achievable frequencies with a raw and a fine programming template. The result of the optimization algorithm is a quasi-linear distribution of the frequency settings on a logarithmic axes.

An important factor that must be taken into account is the accuracy of the filter corner frequency, that can vary as much as $\pm 50\%$ with process corners and temperature. Since the frequencies are changed within a wide programming range, classical autotuning is not suitable for error compensation. The solution proposed in this work is to use a corner frequency error prediction circuit that estimates the real RC time constant and gives the expected percent error of the corner frequency.

The digital code resulting after the measurement can be used for predistorting the programming code for a suitable compensation of the errors. The original idea found in the literature was to measure the time constant through using a dual ramp integrator together with a timing logic and a binary counter. The circuit presented in this work provides significant improvements over the approach described in the literature. These improvements are the fully differential operation, that eliminates the sensitivity of the measurement with a given reference voltage, the lack of non-overlapping clock signals and a simple implementation of the measurement logic.

Another problem emerging in receivers is the amplification of the signal and the conservation of the amplitude at sampling, regardless of the received signal strength. This is done through an automatic gain control algorithm, whose execution element is always a variable gain amplifier. The VGA can be placed at intermediate frequencies or in the base band. The amplifiers suitable for a base-band operation are usually based on opamps with a programmable resistive feedback factor that allows the variation of the gain. Other solutions imply a fixed gain amplification and a variable attenuation placed in front of- or after the amplifier. It is of importance that the maximum gain of the VGA stages must be kept reasonably low for a decent linearity. The VGA implemented in this work is based on a fixed gain amplifier followed by a programmable attenuator and an output buffer. The main contribution brought to this subject is the generalization of the VGA design and the implementation of a general template that can be used for designing variable gain amplifiers for any desired gain range with a given programming step. The optimization algorithm is using the relation between different gain steps and the maximum achievable gain in order to estimate the required number of bits and the distribution of the gain settings between different amplifier stages.

The proposed low pass filter and VGA together with a suitable interface logic have been implemented in a prototype integrated circuit by using a 0.35μm BiCMOS technology provided by Atmel. The programming of the circuit is done by software through connecting the test board to the parallel port of a computer. The main issues encountered during measurement are concerning the DC offset and a relatively high noise contribution for the lowest frequency settings.

Another subject addressed during the research is the implementation of a fully integrated band pass filter with programmable bandwidth. The filter is intended for high frequency IF sampling receivers. The mathematical analysis of the programming problem shows that the filters based on second order sections exhibit a low scalability due to the complicated dependence of the pole quality factors and resonant frequencies on the filter bandwidth. The most scalable architectures are implemented by using passive LC prototypes. The implementation technique used to investigate the scalability of these filters is using a gyrator approach or a state variable synthesis method together with OTA-C structures. OTA-C structures are the choice due to the high frequency operation of the filter. The results of the investigations have shown that, despite of the very good scalability and simple bandwidth

programming algorithm, the OTA-C filters developed from LC passive prototypes are not feasible for narrow bandwidth implementations. The main reason for this is the large spread of the capacitance values.

Band pass filters built with second order sections can trade the approximation for a good scalability and feasibility. Simple OTA-C biquads are able to provide an increased feasibility compared to gyrator or state variable filters. Furthermore, their operation can be enhanced with a negative resistance that allows the implementation of high frequency and high Q filters with feasible capacitor values. A suggested improvement would further increase the feasibility by creating transconductance amplifiers with higher linearity and an extended range of variation for the transconductance parameter. The proposed transconductance structures are using second generation current conveyors in fully differential configurations and a passive resistor as the transconductance element. The main contributions to this part of the work are the systematic evaluation of the directions in band pass filter design an an identification of the trade-off necessary for fully integrating a band pass filter with programmable bandwidth.

The final section of the work addresses the main limitations encountered in programmable band pass filter design. Probably the most important is concerning the precision of the bandwidth and the center frequency. The simulation results suggest that the band pass filters should only be used for band filtering and anti aliasing. Due to the limited precision they are not suitable for analog channel selection. Another important limitation is the component spread, that can only be avoided by ignoring the filter approximation.

The subjects discussed in this work are far from being completed. There is no universally good solution either for low pass or band pass filters in software defined radio receivers. The perspectives for further research include several ideas that can be tried for the optimization of the filter implementations. In the low pass problem, after some more or less successful implementation, there is still an open question: which filter architecture and programming methodology should be used for a true compliance with the software defined radio and what are the universal specifications and design tolerances that are suitable for fulfilling all the needs of the existing and future standards? The answer to this question could prove to be very important in choosing the design trade-offs and the programming templates. The methods tried so far, with current division networks and with switched RC arrays, are functioning well only in some aspects and they all need further development and intelligent implementations. In the band pass problem the immediate goal would be to improve the feasibility and the precision of the filter implementations by extending the range of the achievable transconductance parameters and by using electronic parasitic compensation techniques.

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Gabor Csipkes

Appendix A

The achievable corner frequencies and the programming code

This appendix gives the detailed correspondence between the low pass filter programming code and the achievable corner frequencies. The first three programming bits, that control the resistor arrays have been highlighted for a better overview on the code structure. The codes represented in this table are actually written into the internal latch of the test chip and they form the look-up table required for the corner frequency error compensation algorithm

Code	**Corner frequency** [kHz]
0000000	285.8
0000001	265.4
0000010	247.7
0000011	232.2
0000100	218.5
0000101	206.4
0000110	195.5
0000111	185.8
0001000	176.9
0001001	168.9
0001010	161.5
0001011	154.8
0001100	148.6
0001101	142.9
0001110	137.6
0001111	132.7
0010000	571.7
0010001	540.9
0010010	513.3
0010011	488.3

0010100	465.7
0010101	445
0010110	426.2
0010111	408.8
0011000	392.8
0011001	378.1
0011010	364.3
0011011	351.5
0011100	339.7
0011101	328.6
0011110	318.2
0011111	308.4
0100000	1143.35
0100001	1081.6
0100010	1026.18
0100011	976.2
0100100	930.9
0100101	889.7
0100110	851.6
0100111	817
0101000	784.8
0101001	755.3
0101010	727.9
0101011	702.2
0101100	678.5
0101101	656
0101110	635.4
0101111	615.9
0110000	2285.7
0110001	2162
0110010	2051
0110011	1951
0110100	1860
0110101	1777
0110110	1702
0110111	1632
0111000	1568
0111001	1509
0111010	1454
0111011	1403
0111100	1355
0111101	1311
0111110	1269

0111111	1230
1000000	4751
1000001	4474
1000010	4227
1000011	4006
1000100	3807
1000101	3627
1000110	3463
1000111	3313
1001000	3176
1001001	3049
1001010	2933
1001011	2824
1001100	2724
1001101	2630
1001110	2543
1001111	2461
1010000	10158
1010001	9486
1010010	8897
1010011	8377
1010100	7914
1010101	7500
1010110	7127
1010111	6789
1011000	6482
1011001	6201
1011010	5944
1011011	5707
1011100	5489
1011101	5286
1111110	5098
1011111	4923

Table A.1: The achievable corner frequencies and the programming code

Appendix B

Simulation of the resistance and capacitance errors

This appendix shows the methods used to estimate the expected maximum resistance, capacitance and corner frequency errors that correspond to the given 0.35μm BiCMOS design kit. The test setup for the resistance and capacitance error measurement is shown in the Figure B.1.

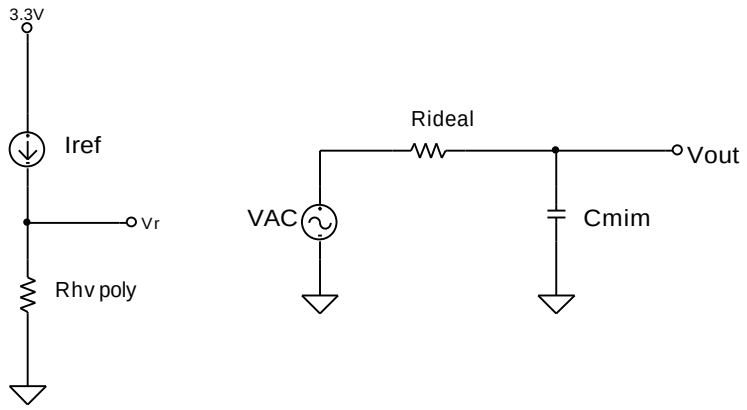

Figure B.1: Test setup for measuring resistance and capacitance variations over process and temperature

The resistance error is measured by injecting an ideal current into a real resistor from the used design kit. Practically, the real resistor value for different process corners and different temperatures can be determined by reading the voltage drop on this resistor. The measured resistor values for the extreme process corners and the limits of the specified temperature range are given in Table B.1. The resistors used for measurement are realized of high resistivity polysilicon.

From Table B.1 it can be seen that the maximum value of the resistance is

Temperature	Process corner	Resistance $[k\Omega]$
$-20°C$	Slow	**6.655**
$-20°C$	Nominal	5.407
$-20°C$	Fast	4.232
$27°C$	Slow	6.153
$27°C$	Nominal	5
$27°C$	Fast	3.913
$85°C$	Slow	5.721
$85°C$	Nominal	4.649
$85°C$	Fast	**3.638**

Table B.1: Variation of the high value polysilicon resistor characteristics for process and temperature corners

Temperature	Process corner	Capacitance [pF]
$-20°C$	Slow	1.087
$-20°C$	Nominal	0.951
$-20°C$	Fast	**0.815**
$27°C$	Slow	1.092
$27°C$	Nominal	0.955
$27°C$	Fast	0.82
$85°C$	Slow	**1.099**
$85°C$	Nominal	0.961
$85°C$	Fast	0.823

Table B.2: Variation of the metal-insulator-metal capacitor value for process and temperature corners

achieved for -20°C at the "slow" process corner and the minimum value is obtained at 85°C at the "fast" process corner. The ideal resistance value is obtained at 27°C and nominal corner. This value is equal to approximately 5kΩ. The maximum and the minimum relative resistance error can be calculated as follows:

$$\begin{cases} \epsilon_{Rmax}[\%] = \dfrac{6.655k - 5k}{5k} \cdot 100 = +33.1\% \\ \epsilon_{Rmin}[\%] = \dfrac{3.638k - 5k}{5k} \cdot 100 = -27.24\% \end{cases} \tag{B.1}$$

The capacitance variations can be measured by using a simple one pole circuit, built with the desired type of capacitance and an ideal resistor. Assuming that the ideal resistor is not process and temperature dependent, the real capacitance value can be evaluated by measuring the -3dB corner frequency of the one-pole circuit. The capacitances used for measurement and also in the filter structure are high-Q

metal-insulator-metal (MIM) capacitors. The simulated capacitance variation with process and temperature is summarized in Table B.2. It can be noticed that the minimum value is achieved for -20°C at the fast process corner. The maximum value is obtained for 85°C at the slow process corner. It can also be seen that MIM capacitors are not very temperature dependent. The maximum and minimum relative capacitance error can be calculated:

$$\begin{cases} \epsilon_{Cmax}[\%] = \dfrac{1.099 - 0.955}{0.955} \cdot 100 = 15\% \\ \epsilon_{Cmin}[\%] = \dfrac{0.815 - 0.955}{0.955} \cdot 100 = -14.7\% \end{cases} \tag{B.2}$$

The maximum and minimum values of the RC time constant are given by the following equations:

$$\begin{cases} T_{max} = R_{nom}C_{nom}\left(1 + \dfrac{\epsilon_{Rmax}}{100}\right)\left(1 + \dfrac{\epsilon_{Cmax}}{100}\right) = 1.53 \cdot T_{nom} \\ T_{min} = R_{nom}C_{nom}\left(1 + \dfrac{\epsilon_{Rmin}}{100}\right)\left(1 + \dfrac{\epsilon_{Cmin}}{100}\right) = 0.646 \cdot T_{nom} \end{cases} \tag{B.3}$$

In this system R_{nom} and C_{nom} are the resistance and the capacitance for nominal conditions. The expected maximum and minimum deviations of the measured time, t_1, can be determined by simply multiplying both T_{max} and T_{min} with $\ln 2$.

$$\begin{cases} t_{1max} = 1.53 \cdot T_{nom} \cdot \ln 2 \\ t_{1min} = 0.646 \cdot T_{nom} \cdot \ln 2 \end{cases} \tag{B.4}$$

The calculated percent variation of the corner frequency, caused by process tolerances and temperature results:

$$\begin{cases} \epsilon_{fcmax}[\%] = +55\% \\ \epsilon_{fcmin}[\%] = -35\% \end{cases} \tag{B.5}$$

The sizing of the components in the measurement circuit and in the programming template of the filter can be derived by replacing the estimated values in the equations of the paragraph 4.3.4

Appendix C

The code-frequency error correspondence

The correspondence between the digital measurement code and the measured t_1, T and the time constant and corner frequency errors is given in the following table. All the values can be calculated according to the equations given in paragraph 4.3.4.

Code	$t_1\ [\mu s]$	$T = RC\ [\mu s]$	$\epsilon_T\ [\%]$	$\epsilon_{fc}\ [\%]$
0100111	1.522	2.196	-37.03	58.8
0101000	1.56	2.25	-35.44	54.89
0101001	1.6	2.3	-33.85	54.16
0101010	1.637	2.36	-32.26	47.61
0101011	1.68	2.42	-30.66	44.226
0101100	1.71	2.47	-29.07	40.99
0101101	1.75	2.53	-27.5	37.9
0101110	1.79	2.58	-25.89	34.94
0101111	1.83	2.64	-24.3	32.1
0110000	1.87	2.7	-22.7	29.4
0110001	1.91	2.75	-21.12	26.77
0110010	1.945	2.806	-19.526	24.264
0110011	1.984	2.862	-17.935	21.85
0110100	2.022	2.917	-16.34	19.54
0110101	2.06	2.973	-14.75	17.31
0110110	2.1	3.03	-13.16	15.156
0110111	2.137	3.084	-11.57	13.083
0111000	2.176	3.193	-9.979	11.085
0111001	2.214	3.195	-8.387	9.155
0111010	2.253	3.25	-6.796	7.292
0111011	2.291	3.306	-5.205	5.491
0111100	2.33	3.361	-3.614	3.749
0111101	2.368	3.416	-2.022	2.064
0111110	2.407	3.472	-0.431	0.433

0111111	2.445	3.527	1.16	-1.146
1000000	2.483	3.583	2.751	-2.677
1000001	2.522	3.638	4.342	-4.162
1000010	2.56	3.694	5.934	-5.601
1000011	2.599	3.749	7.525	-6.998
1000100	2.638	3.805	9.116	-8.354
1000101	2.676	3.86	10.707	-9.672
1000110	2.714	3.916	12.299	-10.951
1000111	2.753	3.971	13.89	-12.196
1001000	2.791	4.027	15.481	-13.406
1001001	2.83	4.082	17.072	-14.583
1001010	2.868	4.138	18.663	-15.728
1001011	2.907	4.193	20.255	-16.843
1001100	2.945	4.249	21.846	-17.929
1001101	2.983	4.304	23.437	-18.987
1001110	3.022	4.36	25.028	-20.018
1001111	3.06	4.415	26.62	-21.023
1010000	3.099	4.471	28.211	-22.003
1010001	3.137	4.526	29.802	-22.96
1010010	3.176	4.582	31.393	-23.893
1010011	3.214	4.637	32.945	-24.803
1010100	3.235	4.693	34.576	-25.692
1010101	3.291	4.748	36.167	-26.561
1010110	3.33	4.804	37.758	-27.409
1010111	3.368	4.859	39.349	-28.238
1011000	3.407	4.915	40.941	-29.048
1011001	3.445	4.97	42.532	-29.84
1011010	3.483	5.026	44.123	-30.615
1011011	3.522	5.081	45.714	-31.372
1011100	3.56	5.137	47.305	-32.114
1011101	3.599	5.192	48.897	-32.84
1011110	3.637	5.248	50.488	-33.55
1011111	3.676	5.303	52.079	-34.245

Table C.1: The code-frequency error correspondence

Appendix D

The programming code of the VGA

This appendix gives the detailed programming code and gain distribution of the variable gain amplifier. The programming code is divided into groups according to the calculations in the VGA sizing algorithm.

Code	Gain composition	Gain value [dB]
0 0 00 000	24+24+24+7	79
0 0 00 001	24+24+24+6	78
0 0 00 010	24+24+24+5	77
0 0 00 011	24+24+24+4	76
0 0 00 100	24+24+24+3	75
0 0 00 101	24+24+24+2	74
0 0 00 110	24+24+24+1	73
0 0 00 111	24+24+24+0	72
0 0 01 000	24+24+16+7	71
0 0 01 001	24+24+16+6	70
0 0 01 010	24+24+16+5	69
0 0 01 011	24+24+16+4	68
0 0 01 100	24+24+16+3	67
0 0 01 101	24+24+16+2	66
0 0 01 110	24+24+16+1	65
0 0 01 111	24+24+16+0	64
0 0 10 000	24+24+8+7	63
0 0 10 001	24+24+8+6	62
0 0 10 010	24+24+8+5	61
0 0 10 011	24+24+8+4	60
0 0 10 100	24+24+8+3	59
0 0 10 101	24+24+8+2	58
0 0 10 110	24+24+8+1	57

0 0 10 111	24+24+8+0	56
1 0 00 000	0+24+24+7	55
1 0 00 001	0+24+24+6	54
1 0 00 010	0+24+24+5	53
1 0 00 011	0+24+24+4	52
1 0 00 100	0+24+24+3	51
1 0 00 101	0+24+24+2	50
1 0 00 110	0+24+24+1	49
1 0 00 111	0+24+24+0	48
1 0 01 000	0+24+16+7	47
1 0 01 001	0+24+16+6	46
1 0 01 010	0+24+16+5	45
1 0 01 011	0+24+16+4	44
1 0 01 100	0+24+16+3	43
1 0 01 101	0+24+16+2	42
1 0 01 110	0+24+16+1	41
1 0 01 111	0+24+16+0	40
1 0 10 000	0+24+8+7	39
1 0 10 001	0+24+8+6	38
1 0 10 010	0+24+8+5	37
1 0 10 011	0+24+8+4	36
1 0 10 100	0+24+8+3	35
1 0 10 101	0+24+8+2	34
1 0 10 110	0+24+8+1	33
1 0 10 111	0+24+8+0	32
1 1 00 000	0+0+24+7	31
1 1 00 001	0+0+24+6	30
1 1 00 010	0+0+24+5	29
1 1 00 011	0+0+24+4	28
1 1 00 100	0+0+24+3	27
1 1 00 101	0+0+24+2	26
1 1 00 110	0+0+24+1	25
1 1 00 111	0+0+24+0	24
1 1 01 000	0+0+16+7	23
1 1 01 001	0+0+16+6	22
1 1 01 010	0+0+16+5	21
1 1 01 011	0+0+16+4	20
1 1 01 100	0+0+16+3	19
1 1 01 101	0+0+16+2	18
1 1 01 110	0+0+16+1	17
1 1 01 111	0+0+16+0	16
1 1 10 000	0+0+8+7	15
1 1 10 001	0+0+8+6	14

1 1 10 010	0+0+8+5	13
1 1 10 011	0+0+8+4	12
1 1 10 100	0+0+8+3	11
1 1 10 101	0+0+8+2	10
1 1 10 110	0+0+8+1	9
1 1 10 111	0+0+8+0	8
1 1 11 000	0+0+0+7	7
1 1 11 001	0+0+0+6	6
1 1 11 010	0+0+0+5	5
1 1 11 011	0+0+0+4	4
1 1 11 100	0+0+0+3	3
1 1 11 101	0+0+0+2	2
1 1 11 110	0+0+0+1	1
1 1 11 111	0+0+0+0	0

Table D.1: The programming code of the gain and the achievable gain settings