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Kang, Narae; Sarker, Biddut K.; and Khondaker, Saiful I., "The effect of carbon nanotube/organic semiconductor interfacial area on the performance of organic transistors" (2012). *Faculty Bibliography 2010s*. 2825.

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Cite as: Appl. Phys. Lett. **101**, 233302 (2012); <https://doi.org/10.1063/1.4769439>

Submitted: 21 July 2012 . Accepted: 15 November 2012 . Published Online: 04 December 2012

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The effect of carbon nanotube/organic semiconductor interfacial area on the performance of organic transistors

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(Received 21 July 2012; accepted 15 November 2012; published online 4 December 2012)

We show that the performance of pentacene transistors can be significantly improved by maximizing the interfacial area at single walled carbon nanotube (SWCNT)/pentacene. The interfacial areas are varied by anchoring short SWCNTs of different densities (0–30/ μm) to the Pd electrodes. The average mobility is increased three, six, and nine times for low, medium, and high SWCNT densities, respectively, compared to the devices with zero SWCNT. The current on-off ratio and on-current are increased up to 40 times and 20 times with increasing the SWCNT density. We explain the improved device performance using reduced barrier height of SWCNT/pentacene interface. © 2012 American Institute of Physics. [<http://dx.doi.org/10.1063/1.4769439>]

Organic field-effect transistors (OFETs) have attracted tremendous attention due to their flexibility, transparency, easy processibility, and low cost of fabrication.^{1–4} High-performance OFETs are required for their potential applications in the organic electronic devices such as flexible display, integrated circuit, and radiofrequency identification tags.^{3,4} A significant research effort has been given in recent years to enhance the performance of the OFETs. Most of the researches were focused to improve the quality of organic semiconductors (OSCs), organic/dielectric interfaces, and other processing parameters.^{1,4} One of the major limiting factors in fabricating high-performance OFET is the large interfacial barrier between metal electrodes and OSC, which results in low charge injection from the metal electrodes to OSC.^{5,6} The interfacial barriers can be caused by several factors such as the discontinuity in morphology, dipole barriers, and Schottky barriers.^{7–9} In order to overcome the challenge of low charge injection, carbon nanotubes (CNTs) have been suggested as a promising electrode material for organic electronic devices.^{10–15}

Recently, fabrication of OFETs using the CNT electrodes has been reported by several research groups.^{10–18} In these reports, the CNT electrodes were fabricated with various techniques using either individual CNT,^{10,11} random network CNTs,^{15–17} CNT/polymer composite,¹² or aligned array CNTs.^{13,14,18} However, an important question remains unanswered: whether the density of CNT in the electrode has any role in the performance of the fabricated OFETs and how much improvement can be achieved using CNT electrode? The density of CNT in the electrodes controls the interfacial area between the CNTs and the OSC. Low density CNTs form small CNT/OSC interfacial area, while high density CNTs create large interfacial area with OSC. It has been suggested from the molecular dynamics simulation and nuclear magnetic resonance (NMR) spectroscopy that a π - π

interaction exists between CNT/OSC.^{19–21} In addition, CNT has field emission properties due their one-dimensional structure.²² These theoretical and experimental studies suggest that charge injection should depend on the CNT/OSC interfacial area and that one can improve the performance of OFETs by maximizing CNT/OSC interfacial area. However, no such investigation has been reported yet. Such a study is of great importance for achieving the overreaching goal of the CNT electrodes in organic electronics.

In this paper, we report systematic investigations of the effect of CNT/OSC interfacial area on the performance of the OFETs by varying the density of CNT in the electrode. The devices were fabricated by thermal evaporation of pentacene on the Pd/ single walled CNT (SWCNT) electrodes where SWCNTs of different densities (0–30/ μm) were aligned on Pd using dielectrophoresis (DEP) and cut via oxygen plasma etching to keep the length of nanotube short compared to the channel length. From the electronic transport measurements of 40 devices, we show that the average saturation mobility of the devices increased from 0.02 for zero SWCNT to 0.06, 0.13, and 0.19 cm^2/Vs for low (1–5/ μm), medium (10–15/ μm), and high (25–30/ μm) SWCNT density in the electrodes, respectively. The increase is three, six, and nine times for low, medium, and high density SWCNTs in the electrode compared to the devices that did not contain any SWCNT. In addition, the current on-off ratio and on-current of the devices are increased up to 40 times and 20 times with increasing SWCNT density in the electrodes. Our study shows that although a few nanotubes in the electrode can improve the OFET device performance, significant improvement can be achieved by maximizing SWCNT/OSC interfacial area. The improved OFET performance can be explained due to a reduced barrier height of SWCNT/pentacene interface compared to metal/pentacene interface which provides more efficient charge injection pathways with increased SWCNT/pentacene interfacial area.

The devices were fabricated on heavily doped silicon (Si) substrates coated with a thermally grown 250 nm thick silicon di-oxide (SiO_2) layer. Palladium (Pd) electrodes of

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$5\ \mu\text{m} \times 25\ \mu\text{m}$ were fabricated using standard electron beam lithography (EBL) process. The nanotube used in this study was a high quality SWCNT aqueous solution obtained from Brewer Science. The solution was free from surfactant, catalytic particles, and bundles and contained mostly individual SWCNTs with an average diameter and length of 1.7 nm and 1.5 μm (Figure S1), respectively, determined from atomic force microscopy (AFM) and scanning electron microscopy (SEM).^{23,24} From the electronic transport measurements of individual SWCNT assembled via DEP, we found that approximately 70% of the nanotubes are metallic and 30% are semiconducting.²⁵ The SWCNTs of different linear densities of 0–30/ μm were assembled between the Pd electrodes via DEP. The details of the SWCNT assembly can be found in our previous publications.²⁴ In short, a 3 μl SWCNT solution was dropped onto Pd pattern and an AC voltage of 5 V with a frequency of 2 MHz were applied for 30 s. Due to the DEP force, the SWCNTs are aligned in arrays between the Pd patterns (Figure S2).²³ The linear density was controlled by varying the concentration of SWCNT solution by diluting the original nanotube solution ($\sim 50\ \mu\text{g}/\text{ml}$) with deionized (DI) water. The SWCNT arrays were then cut by spin coating PMMA, defining a 4.4 μm (L) \times 25 μm (W) window in the middle of the channel using standard EBL, and subsequent oxygen plasma etching.²⁶ Finally, the chips are kept into chloroform and cleaned with isopropanol (IPA) and DI water. Figure 1(a) shows representative SEM images of the part of the electrodes containing an average of 30, 13, and 2 SWCNTs/ μm as well as a bare Pd (zero SWCNT) electrode.

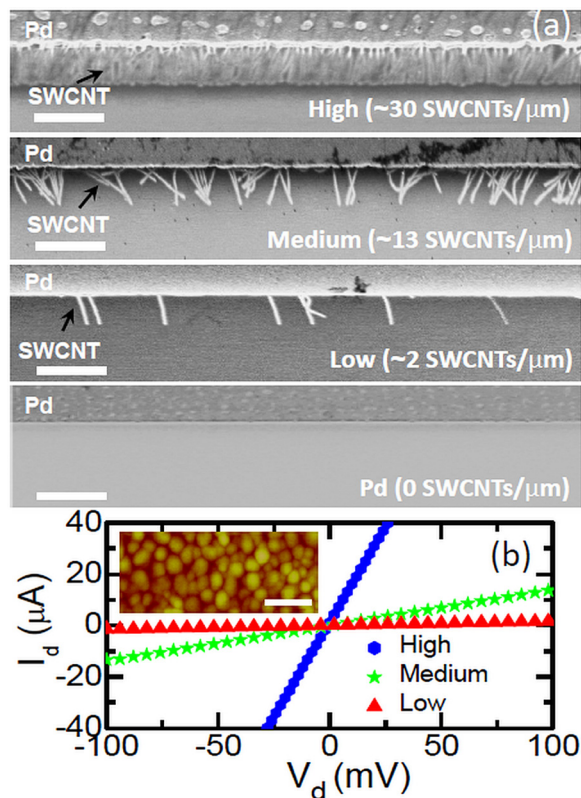


FIG. 1. (a) SEM images of parts of the source electrodes with high, medium, low density SWCNTs and Pd electrode (scale bar: 500 nm). (b) Current-voltage characteristics of the array (before cutting) with high, medium, and low density SWCNTs. Inset: Representative AFM image of a deposited pentacene film. (scale bar: 500 nm).

The average linear densities of the arrays were calculated by counting the total number of SWCNTs from the SEM images and then dividing it by the channel width. Figure 1(b) shows representative current-voltage (I - V) characteristics of the arrays before cutting. The typical resistances for the arrays with high, medium, and low nanotube density are 0.68 k Ω , 7.19 k Ω , and 63.3 k Ω . As expected, the resistance of the arrays increases with decreasing the density of the SWCNTs in the arrays.²⁴

Finally, pentacene film with thickness of 30 nm was thermally deposited in vacuum at a pressure of 2×10^{-6} mbar. In order to minimize the device to device fluctuation from the active materials morphology, all of the pentacene films were deposited under identical conditions. The morphological investigation using AFM (Figure 1(b), inset) showed that all the films have similar morphology with an average grain size of ~ 150 nm (Figure S3).²³ For a fair comparison of the device performances in terms of nanotube density in the electrodes (different interfacial areas) and to obtain statistically meaningful results, we classified the devices into four categories with a narrow range of SWCNT densities: high (25–30/ μm), medium (10–15/ μm), low (1–5/ μm), and Pd (zero SWCNT) only. The electrical transport measurement of the OFETs was performed using Hewlett-Packard (HP) 4145B semiconductor parametric analyzer connected to a probe station inside an enclosed glove box system with N_2 gas flow. A total of 40 devices were investigated with 10 of each category.

Figures 2(a)–2(d) show the drain current (I_d) vs source-drain bias voltage (V_d) curves (output characteristics) at different gate-voltages (V_g) for our best devices with zero, low, medium, and high SWCNTs in the electrodes. All the devices show a good gate modulation with linear behavior at low V_d and saturation behavior at higher V_d , typical of p-channel OFETs. For comparison of device characteristics, we plotted all the curves in the same scale. From here, we see that the output current significantly increases with increasing the SWCNT density in the electrodes. The output current (at $V_d = -50$ V and $V_g = -20$ V) of the devices with zero SWCNTs is 0.15 μA , whereas it is 0.34 μA , 0.81 μA , and 1.15 μA for the devices with low, medium, and high density SWCNTs in the electrodes. The output current is twice for low density and nine times for the high density SWCNTs compared to the device without any SWCNTs. Since the morphology of all the devices is similar, the increase of output current with increasing SWCNT density clearly shows that the interfacial area at the SWCNTs/pentacene has significant impact on the output characteristics of the devices.

To further investigate the effect of the interfacial area on the device performance, we also measured the corresponding transfer curves (I_d vs V_g) of the same devices at $V_d = -50$ V (Figures 2(e)–2(h)) and at $V_d = -10$ V (Figure S4)²³ and calculated the field effect mobility (μ), on-off ratio (I_{on}/I_{off}) and on-current (I_{on}) of the devices. The linear mobility μ_{lin} (at $V_d = -10$ V) and saturation mobility μ_{sat} (at $V_d = -50$ V) are extracted using the standard formula,¹⁸ $\mu_{lin} = (L/WC_iV_d)(dI_d/dV_g)$ and $\mu_{sat} = (2LI_{d,sat})/(WC_i(V_g - V_T)^2)$, respectively, where $I_{d,sat}$ is saturation current and C_i is the gate dielectric capacitance (13.8 nF/cm²). The maximum μ_{sat} (maximum μ_{lin}) of the devices for zero, low, medium, and high densities SWCNTs in the electrodes are 0.05 (0.03), 0.10 (0.06),

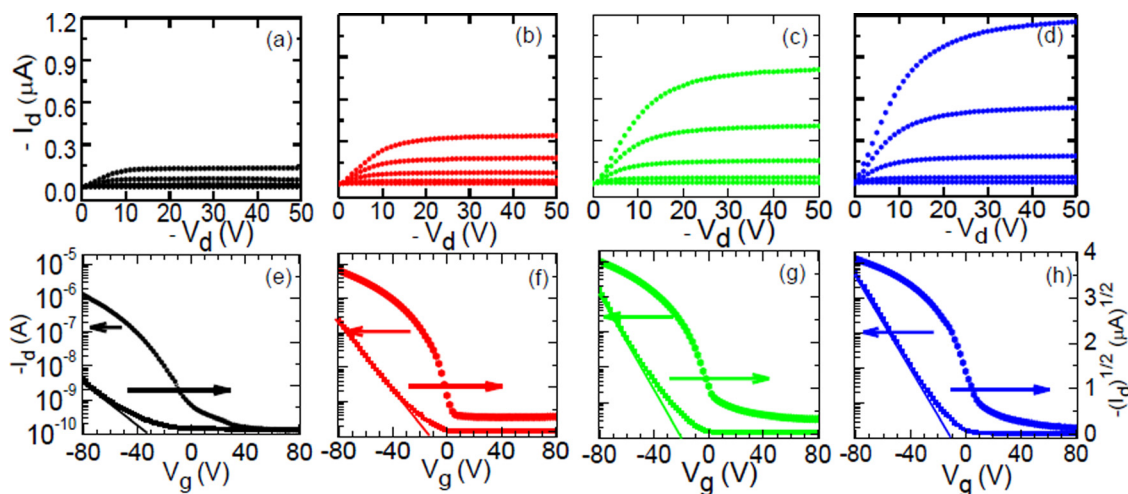


FIG. 2. (a)-(d) Output characteristics (I_d - V_d) of pentacene transistors at $V_g = 0, -5, -10, -15,$ and -20 V (bottom to top) for (a) zero, (b) low, (c) medium, and (d) high density SWCNT in the electrodes. (e)-(h) Transfer characteristics (I - V_g curve) at $V_d = -50$ V (left axis) and $(I_d)^{1/2}$ (right axis) of the devices with (e) zero, (f) low, (g) medium, and (h) high density SWCNTs in the electrodes.

0.19(0.13), and 0.29 (0.19) cm^2/Vs , respectively. This demonstrates that the mobility of the devices also increases with increasing SWCNT/pentacene interfacial area. The maximum μ_{sat} is 100%, 280%, and 480% larger for low, medium, and high density SWCNTs in the electrode compared to the devices that did not contain any SWCNT. Similar increment in the μ_{lin} with increasing the SWCNT density is also observed. In calculating the μ , we used $L = 4.4 \mu\text{m}$ and $L = 5 \mu\text{m}$ for devices with SWCNTs and no SWCNTs, respectively. However, the SEM images of Figure 1(a) for low and medium density SWCNTs in the electrode show that there may be an ambiguity in determining L for these densities as the charge injection comes from both Pd and SWCNT interfaces. In order to minimize this uncertainty, we kept lengths of anchored nanotubes to the Pd short (~ 300 nm). Nevertheless, if we were chosen $L = 5 \mu\text{m}$ for these two densities then the μ_{sat} would be 0.11 and 0.22 cm^2/Vs , for low and medium SWCNT densities. These values are even higher, and indicate that our experimental data exceed the error that may arise from the choice of L in low and medium density electrodes. In addition to μ , other important parameters to evaluate the performance of the transistors are I_{on}/I_{off} and I_{on} . The transfer curves show that the I_{on} (I_d at $V_g = -80$ V) and I_{on}/I_{off} increase with the SWCNT density in the electrodes. The maximum I_{on}/I_{off} and I_{on} for high density SWCNT electrodes devices are 1.1×10^5 and $14.2 \mu\text{A}$, respectively, whereas they are 3.1×10^4 and $12.8 \mu\text{A}$ for medium density, 1.8×10^4 and $10.8 \mu\text{A}$ for low density, and 9.6×10^3 and $3.3 \mu\text{A}$ for zero density SWCNT in the electrodes. Therefore, both the I_{on}/I_{off} and I_{on} are also increased significantly with increasing SWCNT density in the electrodes.

The device characteristics measured from 40 devices are summarized in Figure 3 (see also Table I),²³ where we plot the μ , I_{on}/I_{off} , and I_{on} as a function of SWCNT density in the electrodes. Figure 3(a) shows that, similar to our best devices, the average μ_{sat} are increased from 0.02 for zero SWCNT to 0.06, 0.13, and 0.19 cm^2/Vs (average μ_{lin} are increased from 0.01 to 0.03, 0.08, and 0.11 cm^2/Vs) for low, medium, and high SWCNT density in the electrodes, respectively. The increase in average mobility for our OFET is

three, six, and nine times higher for low, medium, and high density SWCNTs compared to the devices with zero SWCNT. Similar significant increase can also be seen in the median value of the I_{on}/I_{off} and I_{on} with increasing SWCNT density (Figures 3(b) and 3(c)). For the devices with zero SWCNT electrodes, the median value of I_{on}/I_{off} and I_{on} are 1.5×10^3 and $0.6 \mu\text{A}$, respectively. These values increased to 4.5×10^3 (3 times) and $4.1 \mu\text{A}$ (7 times) for low, 2.0×10^4 (17 times) and $8.3 \mu\text{A}$ (14 times) for medium, and 5.5×10^4 (~ 40 times) and $11.82 \mu\text{A}$ (~ 20 times) for high SWCNT densities in the electrodes. From this study, it is clear that the density of SWCNT in the electrode, which controls the SWCNT/pentacene interfacial area, has significant impact on the performance of OFETs. Our study unequivocally show that, although a small number of SWCNTs in the electrodes can enhance the devices performance, the maximum performance was obtained using the most dense SWCNTs in the electrode.

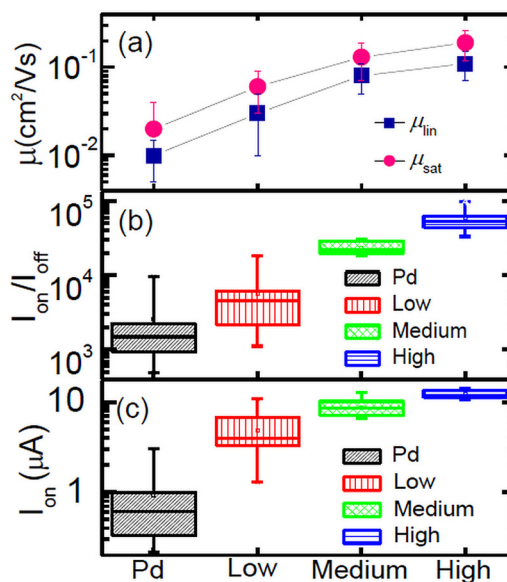


FIG. 3. Summary of OFET device performance from 40 devices. (a) Linear and saturation mobility. (b) On/off ratio and (c) on-current performance as a function of SWCNT density in the electrodes.

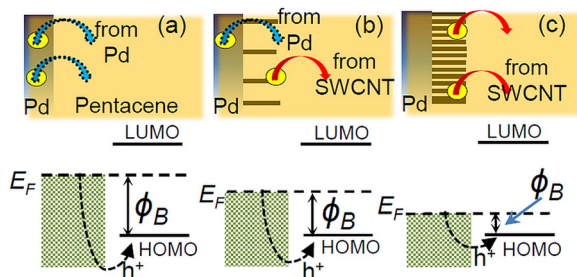


FIG. 4. Schematic of interface (top) and energy level diagrams (bottom) of (a) Pd/pentacene, (b) SWCNT (low density)/pentacene, and (c) SWCNT (high density)/pentacene interfaces. This figure shows Fermi level (E_F), HOMO level, lowest unoccupied molecular orbital (LUMO), and interfacial barrier (ϕ_B).

The remarkable improvement in the OFET device performance with increasing the SWCNT density in the electrodes is due to increased interfacial area of SWCNT/pentacene interfaces. The current at an interface at a fixed bias voltage and temperature (T) can be approximated as $I \propto \exp(-\phi_B/KT)$, where ϕ_B is the Schottky barrier between the metal/semiconductor interface and K is the Boltzmann constant.¹⁴ A decrease in ϕ_B will result in an increase of current at the interface. Although the work-functions of Pd (5.1 eV) and SWCNTs (5.0 eV) are very close and matched with the highest occupied molecular orbital (HOMO) level of the pentacene (5.2 eV),⁹ when Pd is contacted with pentacene the effective work-function of Pd is reduced due to a large diopole barrier at Pd/pentacene interface, known as push back effect.^{7,8,14} It has been recently shown that the value of ϕ_B at SWCNT/pentacene interface is ~ 0.16 eV which is much lower than the ϕ_b at metal/pentacene interface (~ 0.35 to 0.85 eV).¹⁴ Figures 4(a)–4(c) show schematic diagrams of interfacial area and energy band diagrams for the Pd/pentacene, SWCNT (low density)/pentacene, and SWCNT (high density)/pentacene interfaces, respectively. In the devices without any SWCNT, all the charge carriers are injected from the Pd and pass through only the Pd/pentacene interface. Since Pd has a larger barrier height compared to SWCNT (Figure 4(a)), charge carriers need to overcome a larger injection barriers at the Pd/pentacene interface, which may reduce the number of injected charge carriers in the pentacene film and lead to poor device performances. In contrast, when a small number of SWCNTs are anchored with Pd (low density SWCNT electrode) charge carriers are injected from both the SWCNT and Pd (Figure 4(b)). In this case, the injected charge carriers pass through a smaller barrier at SWCNT/pentacene and a larger barrier at Pd/pentacene. Since the charge carriers now have limited access of injection paths through SWCNT, the overall injection barrier is lower than that of Pd/pentacene and the injection efficiency and device properties are improved. With increasing SWCNT densities, the injection barrier is lowered further (Figure 4(c)) and the device properties continue to improve resulting in higher device performance. It is important to note that in our highest density electrodes there are

30 SWCNTs/ μm leaving an inter-nanotube separation of ~ 32 nm and we are unable to increase the density any further using DEP. If it will be possible to increase the density of SWCNT in the electrodes by any other technique, it can result in even more impressive device performance.

In conclusion, we investigated the performance of the pentacene transistors using aligned arrays SWCNT electrodes with various interfacial areas at the SWCNT/pentacene contact. From the electronic transport measurements of 40 devices, we showed that the OFET device performance such as mobility, current on-off ratio, and on-current can be significantly improved with increasing interfacial area at the SWCNT/pentacene and best performance can be achieved by maximizing SWCNT/pentacene interfacial area. We attributed the improved device performance due to a lower barrier height at the SWCNT/pentacene interface compared to metal/pentacene interface.

This work was supported by U.S. National Science Foundation (NSF) under Grant No. ECCS 1102228.

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²³See supplementary material at <http://dx.doi.org/10.1063/1.4769439> for characterization of the nanotube array, electrode fabrication, pentacene film morphology, device characteristics, and summary of all devices.

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