STARS

University of Central Florida
STARS

Faculty Bibliography 2010s | Faculty Bibliography

1-1-2010

High quality solution processed carbon nanotube transistors assembled by dielectrophoresis

Paul Stokes
University of Central Florida

Saiful I. Khondaker
University of Central Florida

Find similar works at: https://stars.library.ucf.edu/facultybib2010
University of Central Florida Libraries http://library.ucf.edu

This Article is brought to you for free and open access by the Faculty Bibliography at STARS. It has been accepted for inclusion in Faculty Bibliography 2010s by an authorized administrator of STARS. For more information, please contact STARS@ucf.edu.

Recommended Citation

Stokes, Paul and Khondaker, Saiful I., "High quality solution processed carbon nanotube transistors assembled by dielectrophoresis" (2010). *Faculty Bibliography 2010s*. 826.
https://stars.library.ucf.edu/facultybib2010/826

University of Central Florida
STARS
Showcase of Text, Archives, Research & Scholarship

Applied Physics Letters

High quality solution processed carbon nanotube transistors assembled by dielectrophoresis

Cite as: Appl. Phys. Lett. **96**, 083110 (2010); https://doi.org/10.1063/1.3327521
Submitted: 08 December 2009 . Accepted: 24 January 2010 . Published Online: 25 February 2010

Paul Stokes, and Saiful I. Khondaker

ARTICLES YOU MAY BE INTERESTED IN

Solution processed large area field effect transistors from dielectrophoreticly aligned arrays of carbon nanotubes
Applied Physics Letters **94**, 113104 (2009); https://doi.org/10.1063/1.3100197

Directed assembly of solution processed single-walled carbon nanotubes via dielectrophoresis: From aligned array to individual nanotube devices
Journal of Vacuum Science & Technology B **28**, C6B7 (2010); https://doi.org/10.1116/1.3501347

Single- and multi-wall carbon nanotube field-effect transistors
Applied Physics Letters **73**, 2447 (1998); https://doi.org/10.1063/1.122477

Applied Physics Reviews
Now accepting original research
2017 Journal Impact Factor: 12.894

AIP Publishing

© 2010 American Institute of Physics.

High quality solution processed carbon nanotube transistors assembled by dielectrophoresis

Paul Stokes and Saiful I. Khondaker[a)]
Department of Physics and Nanoscience Technology Center, University of Central Florida, 12424 Research Parkway, Orlando, Florida 32826, USA

(Received 8 December 2009; accepted 24 January 2010; published online 25 February 2010)

We report on high quality individual solution processed single-walled carbon nanotube (SWNT) field effect transistors assembled from a commercial surfactant free solution via dielectrophoresis. The devices show field effect mobilities up to 1380 $cm^2/V\ s$ and on-state conductance up to 6 μS. The mobility values are an order of magnitude improvement over previous solution processed SWNT devices and close to the theoretical limit. These results demonstrate that high quality SWNT devices can be obtained from solution processing and will have significant impact in high yield fabrication of SWNT nanoelectronic devices. © *2010 American Institute of Physics.*
[doi:10.1063/1.3327521]

The exceptional electronic properties of single-walled carbon nanotubes (SWNTs) make them promising building blocks for future nanoelectronic devices.[1] For the fabrication of high quality devices, clean and defect-free SWNTs are desired. High temperature growth of SWNTs directly on the substrate via chemical vapor deposition (CVD) has been the most widely used technique to achieve high quality SWNT devices. Assembly of SWNT devices by CVD are typically done by randomly dispersed catalyst or patterning catalytic islands for which the later allows for parallel assembly of SWNT devices at selected position of the circuit (direct growth method).[2] Following growth at ~900 C, electrical contact to the SWNT are made without further possessing. Such devices have shown excellent field effect transistor (FET) properties with typical mobility values ranging from 1000 to 10 000 $cm^2/V\ s$ depending upon the diameter[3] and conductance approaching the ballistic limit ($G=4e^2/h \sim 155\ \mu S$, or $R \sim 6.5\ k\Omega$).[4,5] Although high quality devices have been obtained using direct growth CVD method, however high growth temperatures (900 °C) is a major bottleneck to make them compatible with current complementary metal-oxide-semiconductor (CMOS) fabrication technologies.

Post synthesis fabrication techniques from solution processed SWNTs offers an attractive alternative to high temperature growth for the parallel assembly of electronic devices due to the ease of processing at room temperature as well as compatibility with CMOS technology and various substrates including plastics.[6] It is however, generally believed that solution processing techniques such as purification with acids and intense ultrasonication to create stable suspension can introduce defects and degrade the intrinsic electrical properties of SWNTs which in turn could limit their application in nanoelectronic devices. As a result there has been tremendous effort and continuous progress in producing high quality SWNT stable solutions and effort to minimize degradation.[7–9] This has led to the sorting of metallic and semiconducting SWNTs,[10] and the commercialization of electronic grade SWNT solutions.[11] Despite these efforts, the reported device characteristics of solution processed SWNTs are still far from their performance limit. Previous studies of Vijayaraghavan *et al.*[12] found an average on-state conductance ($G_{on} \sim 0.2\ \mu S$) for semiconducting SWNTs and Burg *et al.*[13] reported average on-off ratios of 80 but did not report mobility values. Kim *et al.*[14] has found a mobility of 19.4 $cm^2/V\ s$ on average for individual semiconducting SWNTs by density gradient techniques. Wang *et al.*[15] used dip-pen lithography to fabricate individual SWNT devices from solution and found a mobility of 67 $cm^2/V\ s$. In comparison to devices fabricated by direct growth method using CVD, these reported device properties of solution processed SWNTs are much inferior and calls for further improvement.

Here, we report on considerably improved device quality of individual solution processed SWNT FETs from a commercially available surfactant-free solution. Individual SWNTs were assembled between 1 μm spaced Pd source and drain electrodes (DEs) using ac dielectrophoresis (DEP). The semiconducting devices show on-state conductance values up to 6 μS and field effect mobilities as high as 1380 $cm^2/V\ s$. The maximum mobility value approaches the theoretical performance limit for clean SWNTs and both the on-state conductance and mobility are more than an order of magnitude improvement from previous solution processed SWNT devices. Raman spectroscopy done on individual SWNT devices show the absence of defect related *D*-band. The electrical properties in combination with Raman spectroscopy are indication of high quality SWNT devices. This study shows promise for the use of solution processed SWNTs for high performance nanoelectronics devices.

The devices are fabricated on highly doped Si substrates with a 250 nm thick SiO_2 caped layer. An array of tapered shape, source and DE patterns with 1 μm spacing were defined with electron beam lithography and electron beam deposition of 2 nm Cr for a sticking layer and 25 nm thick Pd followed by lift-off. Pd is used because it is known to make the best contact to SWNTs.[5] The assembly is done in a probe station under ambient conditions and is carried out as follows. A stable, surfactant-free solution of SWNT was obtained from Brewer Science (shelf life six months)[11] that had a concentration of SWNTs ~50 $\mu g/ml$. The solution con-

[a)]Author to whom correspondence should be addressed. Electronic mail: saiful@mail.ucf.edu.

 © 2010 American Institute of Physics

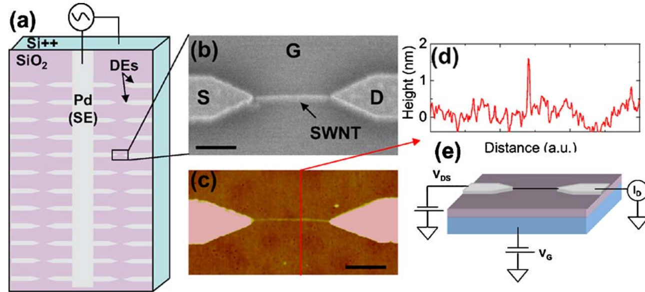

FIG. 1. (Color online) (a) Schematic of the electrode array and DEP assembly setup. (b) Representative SEM image of an individual SWNT between source (s) and drain (d) electrodes. Scale bar: 500 nm. (c) AFM image of the same SWNT in (b). Scale bar: 500 nm. (d) Height profile of the SWNT showing a diameter of ~1.7 nm. (e) Schematic diagram of device geometry and electronic transport measurement setup.

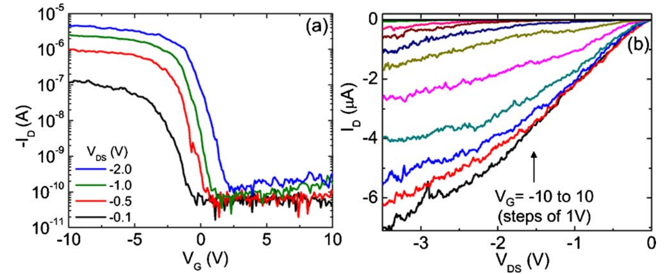

FIG. 2. (Color online) (a) Transfer characteristics of a representative SWNT FET device ($d \sim 1.7$ nm) at $V_{DS}=-0.1$, -0.5, -1.0, and -2.0 V. (b) Output characteristics showing currents up to 7 μA in the saturation regime.

sists of mostly individual SWNTs and is free of catalytic particles. The average length of the SWNTs was ~1–2 μm determined by scanning electron microscopy (SEM). After dilution of the solution to ~10 ng/ml in de-ionized water, a 3 μL drop is cast onto the electrode array. Figure 1(a) shows a three-dimensional cartoon of the assembly setup where we apply the ac voltage (1 MHz, 5 Vp-p) between the common source electrode (SE) and gate (G) electrode for 3 min. This allows for each DE to become capacitivly coupled to the gate electrode and obtain a similar potential as the gate. Therefore at each source and DE pair there is a potential difference allowing for the alignment of many SWNTs simultaneously.[12] Figure 1(b) shows a SEM image of an individual SWNT assembled between the source and DEs following the assembly. The total yield of individual SWNTs is ~20% on average and as high as 35% for a single chip, which is consistent with other similar DEP studies.[13,16] Figure 1(c) shows a representative atomic force microscopy (AFM) image of the same device in Fig. 1(b). Figure 1(d) shows the corresponding height profile for which we measure a diameter (d) of ~1.7 nm. The average diameter of the SWNTs for all of our devices was ~1.5±0.2 nm. After the assembly the devices were annealed in forming gas (Ar/H_2) at 200 C for 1 h to reduce the contact resistance.

Electrical measurements were performed using a DL Instruments 1211 current preamplifier combined with a high resolution DAC card interfaced with LABVIEW. Figure 1(e) shows a cartoon of the measurement setup where we use the highly doped Si as a back gate. We measured a total of 120 individual SWNT devices. Approximately 70% of the devices show metallic or semimetallic behavior (i.e., less than one order of magnitude change in current (I_D) as a function of gate voltage (V_G) and 30% of the devices show semiconducting behavior (one or more orders of magnitude change in I_D as a function of V_G). See supplementary information regarding the DEP assembly of metallic and semiconducting SWNTs.[17] Here, we present FET device properties of the semiconducting SWNTs.

Figure 2(a) shows transfer characteristics, I_D-V_G, for a representative FET device at $V_{DS}=-0.1$, -0.5, -1.0, and -2.0 V ($d \sim 1.7$ nm) showing p-type transport characteristics. The drain current changes by several orders of magnitude with gate voltage and maintains approximately the same on-off ratio (I_{on}/I_{off}) for each V_{DS}. For example, at $V_{DS}=-1.0$ V, the on-off ratio is $\sim 3.6\times 10^4$ ($I_{off}\sim -70$ pA and $I_{on}\sim -2.5$ μA). The linear conductance in the on-state ($G_{on}=I_{on}/V_{DS}$) is ~2.5 μS at $V_{DS}=-1.0$ V. In Fig. 2(b) we plot I_{DS} versus V_{DS} up to the saturation regime at different gate voltages (from −10 to 10 V, bottom to top). Output currents are as high as 7 μA, comparable to Pd contacted CVD SWNTs of similar diameter, directly grown on the substrate.[18] We note that the I_D-V_{DS} characteristics show slightly nonlinear behavior at low V_{DS}, which is an indication of a small Schottky barrier.[5] Work is in progress for the further optimization of the contact. The field effect mobility was calculated from the linear regime in Fig. 2(a) from $\mu=(L^2/C_G\times V_{DS})(dI_D/dV_G)$, where the gate capacitance is $C_G=(2\pi\varepsilon L/\ln(2h/r))$, L is the length of the channel, $\varepsilon=3.9\varepsilon_0$ is the dielectric constant for SiO_2, h is the thickness of the oxide, and r is the radius of the CNT,[18] and $dI_D/dV_G=g_m$ is the transconductance. We find $g_m\sim 0.06$, 0.30, 0.57, and 1.15 μS at $V_{DS}=-0.1$, -0.5, -1.0, and -2.0 V, respectively. Setting $r=0.85$ nm gives a mobility of $\mu \sim 157$, 172, 163, and 164 cm^2/V s, respectively, indicating the mobility values are relatively constant at each value of V_{DS} (see supporting information for additional mobility calculations for a few other devices[17]).

Figure 3(a) shows a scatter plot of the mobility versus the on-state conductance for all 35 devices that we measured

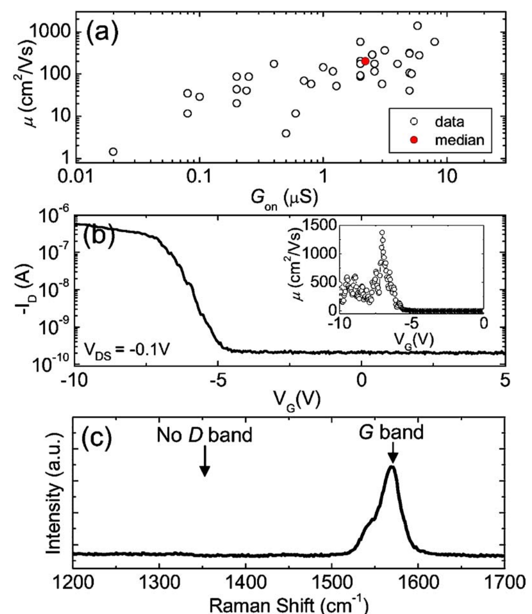

FIG. 3. (Color online) (a) Scatter plot of mobility vs on-conductance for 35 FET devices. The median values of mobility and on-conductance are ~200 cm^2/V s and 2.2 μS, respectively. (b) I_D vs V_G at $V_{DS}=-0.1$ V for our highest performance FET device ($d \sim 1.3$ nm). Inset: Mobility vs gate voltage showing a peak mobility value of ~1380 cm^2/V s. (c) Representative Raman spectroscopy of an individual SWNT device.

TABLE I. Comparison of some recent SWNT solution processed device parameters, this work, and one CVD SWNT made by direct growth methods (N/R: Not reported).

Fabrication method	On-state conductance (μS)	Mobility (cm^2/V s)	Ref.
DEP	Median: 2.2 Max: 6.0	Median: 200 Max: 1380	This work[a]
DEP	Median: 0.2 Max: 1.0	N/R	12[a]
Drop cast	N/R	Median: 19.4 Max: 60	14
Drop cast/dip pen	N/R	67[b]	15
CVD	1.5[c]	~2500 [c]	3

[a]1 μm long devices.
[b]Not indicated whether this is maximum or a typical value.
[c]1.5 nm diameter SWNT (10 μm long).

for this study taken at $V_{DS}=-0.1$ V. We obtain a median on-state conductance and mobility of ~ 2.2 μS and ~ 200 cm^2/V s, respectively. These parameters are a large improvement from previous studies. This is more clearly seen in Table I where we list several recent reported values for on-state conductance and mobility for solution processed devices, and one direct growth CVD devices. Note that all quoted solution processed devices are from *stable* SWNT suspensions. It can be clearly seen that the median on-state conductance is an order of magnitude higher than previous median values reported by Vijayaraghavan *et al.*[12] Our average mobility values are also an order of magnitude higher than previous studies by Kim *et al.*[14] and ~3 times higher than previous report of Wang *et al.*[15]

In Fig. 3(b) we show a plot of I_D versus V_G at $V_{DS}=-0.1$ V for our highest mobility SWNT-FET device ($d \sim 1.3$ nm). The on-state conductance for this device is ~ 6 μS. Inset of Fig. 3(b) shows a plot of the calculated mobility versus gate voltage with $r \sim 0.65$ nm and $g_m \sim 0.45$ μS. We find that the peak mobility for this device is ~ 1380 cm^2/V s. Comparing with the theoretical limit at room temperature for clean SWNTs,[3,19] $\mu_{peak} \sim 1000$ $cm^2/V\,s \times [d(nm)]^2$ where d is the diameter of the tube, we find $\mu_{peak} \sim 1700$ cm^2/V s, which is reasonably close to the experimental value indicating that this device is being pushed close to its performance limit. This device shows significantly better properties than the best reported samples from Table I. Our highest value of G_{on} is six times higher than the highest value found in Ref. 12. The maximum mobility is ~20 times higher than the highest previous reported values and close to what is expected in high quality direct growth CVD devices of similar diameter.

We speculate that the improved device performance stems from the nonexistence of residual surfactant and the cleanliness of the as-assembled devices with the absence of bundles. We verified the cleanliness of the SWNT devices by Raman spectroscopy. We used a Renishaw *inVia* micro-Raman spectrometer with 514 nm excitation, ~1 μm spot size and ~1 mW power. Figure 3(c) shows representative Raman spectra near the *G*-band mode which is clearly observed at ~ 1570 cm^{-1}. Note the absence of the defect induced *D*-band typically observed at ~ 1350 cm^{-1}. The missing *D*-band observation indicates low density of defect sites[20,21] and is consistent with high quality devices reported here.

In conclusion, we have shown improved device performance of individual SWNT FETs assembled by DEP from a surfactant free commercial solution. The devices show a median on-state conductance of 2.2 μS with a maximum of 6 μS while the median field effect mobility is 200 cm^2/V s with a maximum of 1380 cm^2/V s, approaching the performance limit. The absence of the *D*-band in the Raman spectroscopy measurements demonstrates that the SWNTs have a low density of defects further verifying high quality device. This study show promise for solution processed SWNTs to be viable for the parallel fabrication of high quality CMOS compatible nanoelectronic devices.

This work was supported by U.S. National Science Foundation under Grant No. ECCS-0748091 (CAREER).

[1]P. Avouris, Z. H. Chen, and V. Perebeinos, Nat. Nanotechnol. **2**, 605 (2007).
[2]A. Javey, Q. Wang, A. Ural, Y. Li, and H. Dai, Nano Lett. **2**, 929 (2002).
[3]X. Zhou, J.-Y. Park, S. Huang, J. Liu, and P. L. McEuen, Phys. Rev. Lett. **95**, 146805 (2005).
[4]D. Mann, A. Javey, J. Kong, Q. Wang, and H. Dai, Nano Lett. **3**, 1541 (2003).
[5]A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, Nature (London) **424**, 654 (2003).
[6]L. Huang, Z. Jia, and S. O'Brien, J. Mater. Chem. **17**, 3863 (2007).
[7]M. J. O'Connell, S. M. Bachilo, C. B. Huffman, V. C. Moore, M. S. Strano, E. H. Haroz, K. L. Rialon, P. J. Boul, W. H. Noon, C. Kittrell, J. Ma, R. H. Hauge, R. B. Weisman, and R. E. Smalley, Science **297**, 593 (2002).
[8]M. C. Hersam, Nat. Nanotechnol. **3**, 387 (2008).
[9]M. C. LeMieux, M. Roberts, S. Barman, Y. W. Jin, J. M. Kim, and Z. Bao, Science **321**, 101 (2008).
[10]M. S. Arnold, A. A. Green, J. F. Hulvat, S. I. Stupp, and M. C. Hersam, Nat. Nanotechnol. **1**, 60 (2006).
[11]See http://www.brewerscience.com for more information about the commercially available SWNT solution.
[12]A. Vijayaraghavan, S. Blatt, D. Weissenberger, M. Oron-Carl, F. Hennrich, D. Gerthsen, H. Hahn, and R. Krupke, Nano Lett. **7**, 1556 (2007).
[13]B. R. Burg, J. Schneider, M. Muoth, L. Durrer, T. Helbling, N. C. Schirmer, T. Schwamb, C. Hierold, and D. Poulikakos, Langmuir **25**, 7778 (2009).
[14]W. J. Kim, C. Y. Lee, K. P. O'Brien, J. J. Plombon, J. M. Blackwell, and M. S. Strano, J. Am. Chem. Soc. **131**, 3128 (2009).
[15]W. M. Wang, M. C. LeMieux, S. Selvarasah, M. R. Dokmeci, and Z. Bao, ACS Nano **3**, 3543 (2009).
[16]L. F. Dong, V. Chirayos, J. Bush, J. Jiao, V. M. Dubin, R. V. Chebian, Y. Ono, J. F. Conley, Jr., and B. D. Ulrich, J. Phys. Chem. B **109**, 13148 (2005).
[17]See supplementary material at http://dx.doi.org/10.1063/1.3327521 for mobility calculations of a few other devices and discussion regarding the assembly of metallic and semiconducting SWNTs.
[18]W. Kim, A. Javey, R. Tu, J. Cao, Q. Wang, and H. Dai, Appl. Phys. Lett. **87**, 173101 (2005).
[19]M. J. Biercuk, S. Ilani, C. M. Marcus, and P. L. McEuen, Top. Appl. Phys. **111**, 455 (2008).
[20]S. K. Doorn, L. Zheng, M. J. O'Connell, Y. Zhu, S. Huang, and J. Liu, J. Phys. Chem. B **109**, 3751 (2005).
[21]A. W. Bushmaker, V. V. Deshpande, S. Hsieh, M. W. Bockrath, and S. B. Cronin, Phys. Rev. Lett. **103**, 067401 (2009).