

---

Retrospective Theses and Dissertations

---

1976

## A Simulator for the Motorola M6800 Microprocessor

Carolyn Elizabeth Jordan  
*University of Central Florida*

 Part of the [Engineering Commons](#)

Find similar works at: <https://stars.library.ucf.edu/rtd>

University of Central Florida Libraries <http://library.ucf.edu>

This Masters Thesis (Open Access) is brought to you for free and open access by STARS. It has been accepted for inclusion in Retrospective Theses and Dissertations by an authorized administrator of STARS. For more information, please contact [STARS@ucf.edu](mailto:STARS@ucf.edu).

---

### STARS Citation

Jordan, Carolyn Elizabeth, "A Simulator for the Motorola M6800 Microprocessor" (1976). *Retrospective Theses and Dissertations*. 224.

<https://stars.library.ucf.edu/rtd/224>

A SIMULATOR FOR THE MOTOROLA M6800 MICROPROCESSOR

BY

CAROLYN ELIZABETH JORDAN  
B.S., Florida Technological University, 1974

RESEARCH REPORT

Submitted in partial fulfillment of the requirements  
for the degree of Master of Science  
in the Graduate Studies Program of  
the College of Engineering of  
Florida Technological University

Orlando, Florida  
1976



A SIMULATOR FOR THE MOTOROLA M6800 MICROPROCESSOR

by

Carolyn E. Jordan

ABSTRACT

The Motorola Company has developed a microprocessor called the M6800 Microprocessor. While the microprocessor is being configured, it is general practice to develop the software at the same time. This is where simulation of the proposed hardware operation can become very important to the success of the design effort. The simulator duplicates the microprocessor execution of machine language instructions on another computer.

The simulator discussed in this paper is denoted the SIM6800. The purpose of this paper is to describe the structure, coding, and execution of the SIM6800 simulator. A User's Guide and sample program have been included.

Christian S. Baum, PE  
Director of Research Report



## TABLE OF CONTENTS

I.	INTRODUCTION . . . . .	1
II.	CHAPTER 1 . . . . .	6
	SIM6800 Structure	
III.	CHAPTER 2 . . . . .	.15
	SIM6800 Coding	
IV.	CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK. . .	.19
V.	APPENDIX A . . . . .	.22
	SIM6800 User's Guide for the Motorola M6800 Microprocessor	
VI.	APPENDIX B . . . . .	.34
	Sample Output from the SIM6800 Simulator Program	
VII.	APPENDIX C . . . . .	.40
	Computer Listing of the SIM6800 Simulator Program	
VIII.	BIBLIOGRAPHY . . . . .	.53



## INTRODUCTION

A microprocessor is fundamentally no different from any other computer in that the five major subsystems are present, including: the ALU (arithmetic logic unit), the CPU (control function), input, output, and memory. A microprocessor is constructed by putting the ALU and the CPU into one or a small number of integrated circuit chips. The Motorola Company has developed a processor of this type called the M6800 Microprocessor.

While the microprocessor hardware is being configured, it is general practice to develop the software at the same time. This is where simulation of the proposed hardware operation can become very important to the success of a design effort. A simulator program facilitates overall checkout and error elimination from programs written for the microprocessor. The simulator duplicates the microprocessor execution of machine language instructions on another computer. Although the simulator program does not match the microprocessor's real time operating speeds, a count is kept of elapsed time cycles in simulated execution which can be used to estimate program execution times. The simulator program discussed in this paper was designed and written to operate in a time-sharing mode. Choosing the time-sharing mode over the batch mode allows the user to



have complete interactive control over the program being tested. The user gives appropriate commands to the simulator, resulting in execution of all or any part of the program being tested. This flexibility of user control would be difficult to obtain using only the microprocessor hardware.

The simulator is only part of the overall software support aids for the Motorola M6800 (Figures 1 and 2). The microprocessor users begin by writing a program in the assembler language for the computer. The assembler language program serves as input to a Cross-assembler, an assembler resident on a computer other than the computer for which it generates the machine code. The machine code from the Cross-assembler is then used as input to the simulator program. The simulator duplicates the execution of the machine language. The output from the simulator is a computer activity listing which the user can review to determine if the assembler language program has executed correctly with the intended results.

The original purpose of the simulator was to allow parallel work on the microprocessor software and hardware. The configuration of the microprocessor hardware allows only one user at a time. However, the host computer containing the simulator is usually large enough to support several terminals allowing several users of the simulator software at once. With this increased access to the



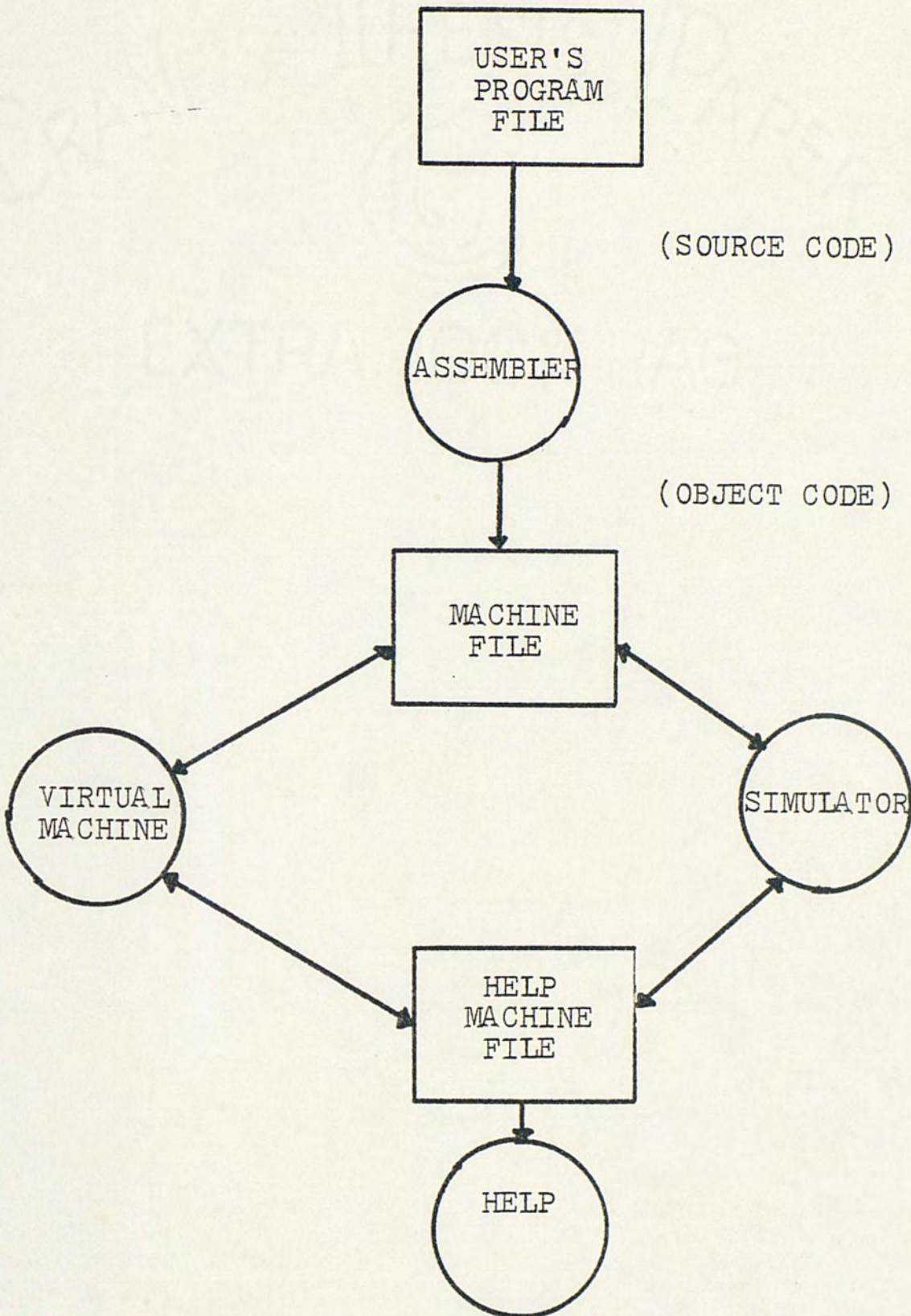


Fig. 1.--FILE INTERCONNECT SCHEME FOR SOFTWARE SUPPORT



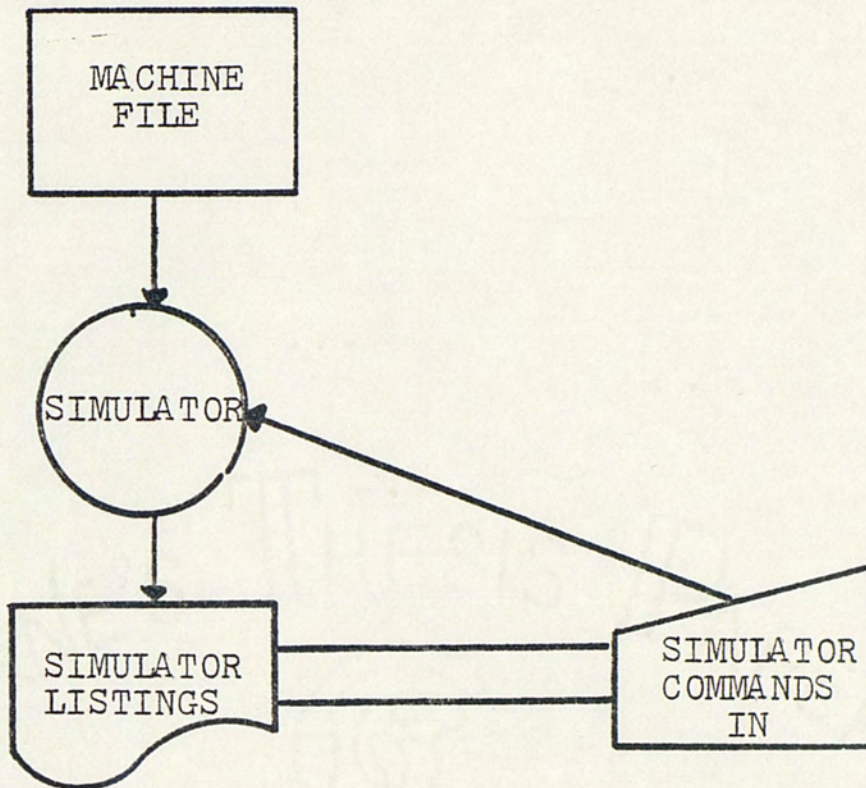


Fig. 2.--SIMULATOR, A BLOCK DIAGRAM



simulator, the use of the simulator can later be expanded to general debugging of all microprocessor software.

The simulator discussed in this paper, denoted the SIM6800, was written in IBM PL/1-F for the IBM 360-75 computer. PL/1 lends itself to this type of programming application due to the structural format of the language, the character string and bit string manipulation abilities, and the access methods to the machine's bits and addresses. The simulator program can be executed in a minimum core partition of 120K-bytes under time-sharing.

The purpose of this report is to describe the structure, coding, and execution of the SIM6800 simulator. A User's Guide and sample program have been included to allow any individual to use the SIM6800 simulator with ease.



## CHAPTER 1

### SIM6800 STRUCTURE

The input to the simulator is the result of several previous steps in the software support scheme. The user written assembler language program (Figure 3), the assembled program (Figure 4), and the object code file, named EXAMPLE 1 (Figure 5) have all been generated prior to the execution of the simulator.

SIM6800 itself is a single program written in PL/1. All subprocedures are contained internally to the main program, but the simulator does require three files for it to execute. These three files are:

1. Object code file (OBJ)
2. Machine operation table (MOT)
3. Simulator commands

The name of the OBJ file is supplied by the user when dialog to SIM6800 is initiated through an interactive terminal. The procedure call for establishing communication is as follows:

```
exec sim6800(example1)
```

This statement moves the object file EXAMPLE 1 into simulated memory. Each line of the object code symbolically represents each line of the assembler program and is divided into two components:



```

100  NAM ITEM1
110  OPT MEM DIRECTS THE ASSEMBLER TO SAVE
120  *      AN OBJECT PROGRAM.
130  *
140  *  ADDITION OF TWO EIGHT-BYTE
150  *  BINARY-CODED-DECIMAL NUMBERS.
160  *
190  ORG $1000
200  LDA B #8
210  LDA #P   LOADS INDEX REGISTER
220  *      WITH THE ADDRESS OF THE
230  *      MOST SIGNIFICANT BYTE
240  *      OF P
250  CLC
260  NEXT LDA A 7,X
270  ADC A 15,X
280  DAA
290  STA A 23,X
300  DEX
310  DEC B
320  BNE NEXT  LOOPS BACK FOR NEXT
330  *      BYTE IF ADDITION NOT COMPLETED.
400  NOP
410  BRA *-1
500  *  ALLOCATE A DATA AREA IN READ-WRITE
510  *  MEMORY FOR THE NUMBERS TO BE ADDED
520  *  (P AND Q) AND FOR THE SUM (RES)
530  ORG $0100
540  P RMB 8
550  Q RMB 8
560  RES RMB 8
600  END
610  MON

```

Fig. 3.--ASSEMBLER LANGUAGE PROGRAM



```

00010          NAM      ITEM2
00020          * REVISION 1.0
00030          OPT      MEM
00040          OPT      SYMBOLS

00060          * ADDITION OF TWO-MULTIPLE-PRECISION
00070          * BINARY-CODED-DECIMAL NUMBERS.
00080          *
00090          0008    NB      EQU      8          SPECIFIES 8-BYTE
          *                                     OPERANDS

0110          * BEGIN SUBROUTINE
00120 1000          ORG      $1000
00130 1000 C6 08    BCD      LDA B      #NB
00140 1002 FE 0100  LDX      ADDR      LOADS DATA ADDR
00150 1005 0C          CLC
00160 1006 A6 07    NEXT     LDA A      NB-1,X    START LOOP
00170 1008 A9 0F          ADC A      2*NB-1,X
00180 100A 19          DAA
00190 100B A7 17          STA A      3*NB-1,X
00200 100D 09          DEX
00210 100E 5A          DEC B
00220 100F 26 F5          BNE      NEXT
00230 1011 39          RTS          END OF BCD SUBROU
          *                                     TIME

00250          * BEGIN MAIN PROGRAM
00260          * TEST OF SUBROUTINE 'BCD'
00270          ORG      $1100
00280          LDS      # $13F    INITIALIZE STACK
          *                                     POINTER
00290          LDX      #P      LOADS ADDRESS
          *                                     OF P
00300          STX      ADDR
00310          JSR      BCD      DO BCD ADDITION
00320          NOP
00330          BRA      *      END OF MAIN PROG

00350          * ALLOCATE A DATA AREA IN READ-WRITE MEM
00360          ORG      $0100
00370          * (1) FOR THE SUBROUTINE
00380 ADDR RMB 2
00390          * (2) FOR THE MAIN PROGRAM
00400 P RMB NB
00410 Q RMB NB
00420 RES RMB NB
00430          END

```

Fig. 4.--ASSEMBLED PROGRAM



4364	001	0
4365	032	254
4361	189	4096
4358	255	256
4355	206	258
4352	142	319
4096	198	8
4098	254	256
4101	012	0
4102	166	7
4104	169	15
4106	025	0
4107	167	23
4109	009	0
4110	090	0
4111	038	245
4113	057	0

Fig. 5.--OBJECT CODE FILE EXAMPLE1



<u>Component</u>	<u>PL/1 Variable Names</u>
1. Instructional address	BYTE1
2. Operands	BYTE2

The second file, MOT, is automatically moved into a storage structure called MOT. The MOT file remains the same for all programs being tested. This file contains information needed to decode and execute the object code. There are 197 entries in the MOT file and each entry contains the following categories:

<u>MOT Entry</u>	<u>PL/1 Variable Names</u>
1. Operator number	OP
2. Mnemonic code	MNEMONIC
3. Address mode	ADDR_MODE
4. Time	TIME
5. Bytes	BYTES
6. MOT number	MOT_NO
7. Address accumulator	ADDR_ACC

Once these first two files are set up, SIM6800 will print the following header:

```
SIMULATOR FOR THE MOTOROLA M6800 MICROPROCESSOR
      WRITTEN FOR THE IBM360
      VERSION 1           1976
```

The simulator acknowledges a request for a command by printing a "?". At this time the user creates the third file by entering a simulator command after every prompt. The simulator commands now available are:



<u>MNEMONIC</u>	<u>MEANING</u>
DM	Display memory
DR	Display register
EX	Exit simulator
HR	Set header count
RN	Run
SM	Set memory
SR	Set register

A complete explanation of these commands may be found in Appendix A.

The SIM6800 has 72 executable instructions. These instructions assemble into 1 to 3 bytes of object code. The length of the instruction depends on the particular instruction and on the type of addressing used. The length of the instruction is the value of BYTES in the MOT file.

SIM6800 has two 8-bit data registers where arithmetic calculations are performed. These are equivalent to Accumulator A and Accumulator B in the M6800 processor chip. The corresponding PL/1 variable names are ACCA and ACCB, respectively.

SIM6800 has seven types of addressing, as follows:

1. Inherent addressing
2. Relative addressing
3. Immediate addressing
4. Accumulator addressing
5. Indexed addressing



## 6. Extended addressing

## 7. Direct addressing

The addressing mode used is coded 1 through 7 and this code is entered in the MOT variable ADDR\_MODE. If either Accumulator A or Accumulator B is needed in the addressing, an "A" or a "B" is placed in MOT entry ADDR\_ACC.

SIM6800 uses a 16-bit register called the Index Register (IX), again, corresponding to a hardware register on the M6800 chip. This register is needed for instructions that use the indexed addressing mode. The use of IX allows the current instruction or data address to be computed during execution of the program and allows additional flexibility over the strict use of fixed addresses predetermined by the assembler.

The SIM6800 simulated memory is a two dimensional array, denoted  $M(5000,2)$ . The size of memory is 10,000 8-bit memory locations. The design of M as a 2-dimensional array is based on the format of the object code for the M6800 hardware. The maximum length of a coded instruction is 3 bytes. The first byte is the memory address which will be the array M subscript. Therefore, only two dimensions of array M are needed to store the last two bytes of the instructions.

The memory location of the current instruction about to be executed is assigned to the program counter variable,



PC. That memory location is also assigned to the instruction address, IA. Once the length of the instruction has been determined, PC is incremented by that length. This new value of PC is the memory location of the next instruction to be executed.

Like most microprocessors, the Motorola M6800 is not designed to handle the conventional subroutine return-address storage scheme. Rather, the M6800 uses a hardware "push-down stack." The stack consists of any number of locations in memory providing for temporary storage and retrieval of successive bytes of information. Usually, the stacks will be one single block of successive memory locations but there could conceivably be several stacks, each consisting of a block of successive memory locations. Associated with the stack is a 16-bit stack pointer called SP. When a subroutine is called, the current contents of PC (return address) are stored on the stack at location SP. The stack pointer SP is then decremented by 2. When a return from subroutine occurs, the current contents at stack location SP (entry address) is assigned to PC. The stack pointer SP is incremented by 2.

The Condition Code Register, CC, is a 6-bit register containing information on the status of the program being run. The 6 bits in CC are:



<u>Bit No.</u>	<u>Condition Code</u>
0	C (Carry-borrow)
1	V (Overflow)
2	Z (Zero)
3	N (Negative)
4	I (Interrupt Mask)
5	H (Half-carry)

The CC can be set by any of a number of instructions. The value to which CC is set depends on the result of the last instruction executed. If, for example, the subtraction of two numbers results in a negative number, the N bit would be turned on (set to "1"). The value of the CC register can be used to control branching within a program, and is useful in implementing data comparison operations and similar program functions.



## CHAPTER 2

### SIM6800 CODING

The simulator program is divided into 10 subprocedures contained within a main procedure. Each subprocedure performs one step in the decoding of the object code. This modular approach aids in debugging and future modification to the simulator. Figure 6 is an overall flowchart of the SIM6800.

When the simulator is executed, the first two subprocedures CREATE1 and CREATE2 are called. Their function is to load the OBJ and MOT files already discussed. Before executing any further, the simulator prompts the user for a command. The user-supplied commands EX, SM, SR, DM, DR, and HR either set variable values or end execution of the simulator. The RN command causes all of the subprocedures to be executed.

A brief, functional description of each of these subprocedures follows.

#### LKUP

BYTE1 of the object code identifying the instruction should match with an entry in the MOT file if the instruction is valid. If the match is found, all entries in the MOT file structure are filled in. At this point, the simulator should have information available to it



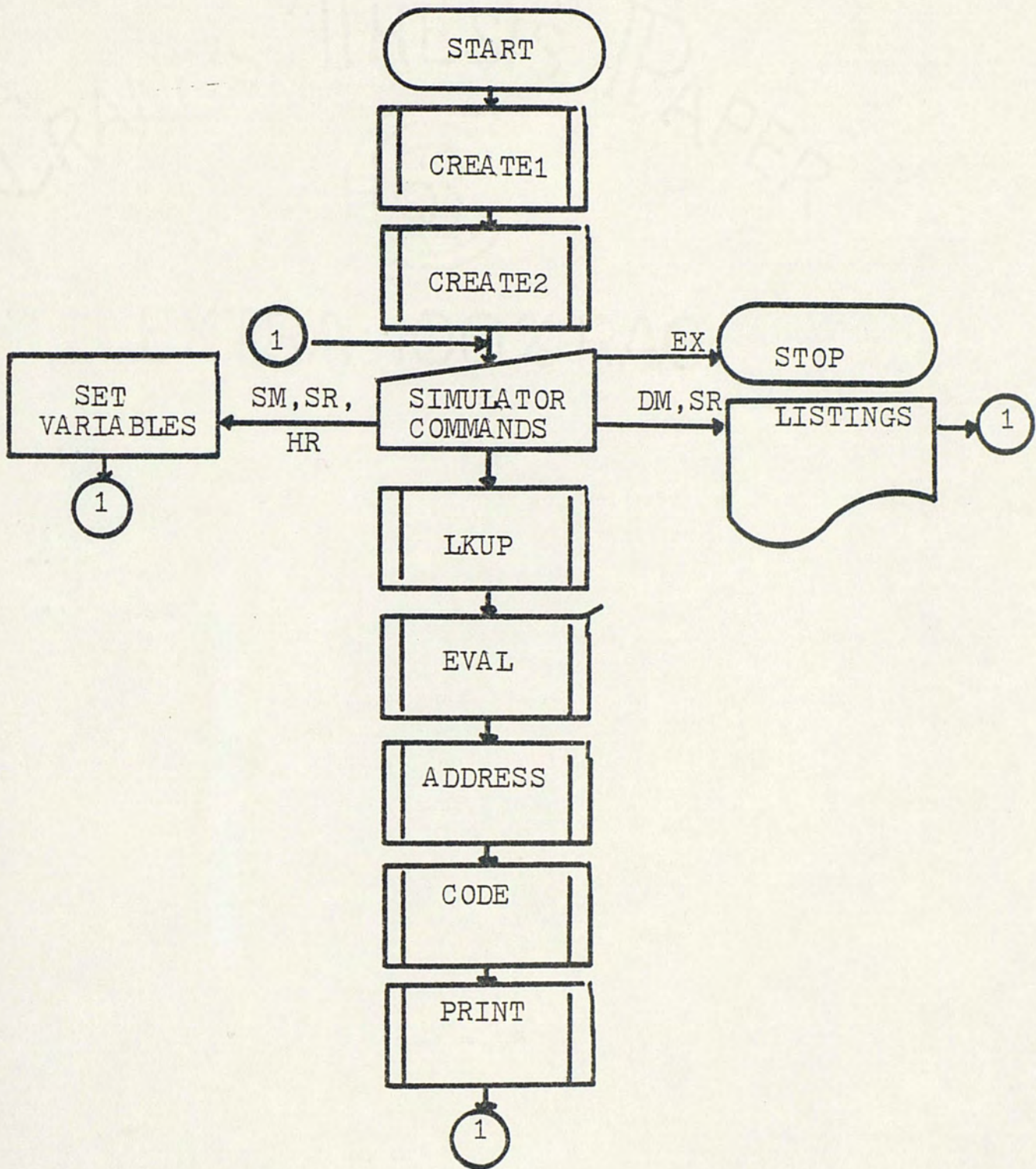


Fig. 6.--SIM6800 FLOWCHART



concerning the instruction abbreviation (MNEMONIC), the type of address used (ADDR\_MODE), and number of execution cycles needed (TIME), length of the instruction (BYTES), the instruction number from 1 to 72 (MOT\_NO), and whether or not an accumulator is needed in the addressing (ADDR\_MODE). If a match is not found, Error #301 will be printed on the terminal to flag the problem (see Appendix A for a list of error codes and corrective actions).

### ADDRESS

The variable ADDR\_MODE in the MOT file determines which of the seven types of addressing is required. The address of the instruction operands is calculated in this subprocedure to be used in another procedure. If the calculated address exceeds the bounds of simulated memory, Error #313 will be printed (see Appendix A).

### EVAL

The operation number OP from the OBJ file determines what type of operation the instruction is to perform (e.g. ADD). Using the address generated by ADDRESS, the operands needed in the operation are obtained and the instruction can then be completely evaluated.

### CODE

The results of the operation identified in EVAL are now tested. The CC bits are set to a specific value based on the particular instruction. The Boolean formulae used to test the results are the same as those used by Motorola



in the hardware operation.

PRINT

After each instruction is evaluated, the values of the simulated machine registers are printed along with the register abbreviation as a header.



## CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

The SIM6800 shows how a simulator can be used to verify a microprocessor program without the use of the microprocessor hardware. The PL/1 simulator program was written with "ease of use" in mind and was written for a wide range of users, from the less experienced to the experienced. The SIM6800 also shows execution of the programs in various amounts of detail as required by the user. Two additional concepts, MACRO commands and HELP files are suggested as future work to the SIM6800. The following is an overall description of these concepts.

### MACRO COMMANDS

A user defined simulator command(s) is called a MACRO. MACRO commands allow the user to create a string of commands or redefine existing commands. Suppose the user repeatedly enters:

```
RN 7
DM 0102 8
DM 010A 8
DM 0112 8
```

To avoid repetition, the user could define a MACRO command named XY by typing

```
? XY(RN 7.DM 0102 8.DM 010A 8.DM 0112 8)
```



A MACRO command is executed in the same way as an existing command.

?XY

Once the MACRO concept has been implemented, it can be expanded to include MACROs with variable parameters and MACROs with multiple variable parameters.

Commands would then be needed to give the user control over MACRO commands. These would be:

<u>MACRO Command</u>	<u>Meaning</u>
MD	Delete MACRO
ML	List MACRO
MR	Read MACRO from machine file
MS	Save MACRO in machine file

#### HELP FILES

Once the entire M6800 software and hardware have been assembled, a HELP system should be created. The HELP system provides up-to-date information on improvements and new developments of the M6800 microprocessor system. The users enter a request for assistance and a search is made through the HELP file for the desired information. The HELP file is a set of messages, each divided into three sections:

1. the message number
2. the message description
3. the message text

The amount of detail to be printed with the HELP message is specified by format control commands. With the added



feature of format control, the user could print all messages added within the last month, all simulator messages, all HELP messages, or any combination of messages desired.

The inclusion of MACROs and HELP files will round out user control and interface with SIM6800.



APPENDIX A

SIM6800 USER'S GUIDE

FOR THE MOTOROLA M6800 MICROPROCESSOR



## EXECUTING THE SIM6800 SIMULATOR

The SIM6800 simulator is designed to be used in a time-sharing mode. Since every computer installation has its own form of time-sharing, procedures may vary. The sample problem included in this appendix and Appendix B was executed on an IBM2741 terminal to an IBM360/75 computer operating under OS/360. To execute the SIM6800 simulator, the user logs on the computer and types in:

```
exec sim6800(example1)
```

(EXAMPLE1 is the file containing the object code of the program being simulated.)



## SIMULATOR COMMANDS

The following is a list of the currently available M6800 simulator commands:

<u>MNEMONIC</u>	<u>MEANING</u>
DM	Display memory
DR	Display registers
EX	Exit simulator
HR	Set header count
RN	Run
SM	Set memory
SR	Set registers

The exact format and explanation of each of these commands are found on the following pages. There are several basic directives which must be observed when executing SIM6800.

1. Insert at least one blank between operands in the command.
2. Hexidecimal values must contain four positions. Leading zeros must be added if needed.
3. Real number values must not contain a decimal point.
4. All operands listed in the command format must be included.



5. All memory locations (addresses) must be hexadecimal and other operands must be integers (unless otherwise stated).



## DM--DISPLAY MEMORY

## Format

DM a n

Display n memory positions starting at memory address  
a.

The DM command can be used to display n memory  
locations containing data values or n memory locations  
containing the object code of the program being simulated.



## DR--DISPLAY REGISTERS

## Format

DR

The DR command causes the value of the registers to be printed.

The codes for the registers to be displayed are:

IA -- Instruction address  
OC -- Operation code  
EA -- Effective address  
P -- Program counter  
X -- Index register  
A -- Accumulator A  
B -- Accumulator B  
C -- Condition codes  
S -- Stack pointer  
T -- Time

Note: This simulator command has no operands.



## EX--EXIT FROM SIMULATOR

Format

EX

The EX command causes all simulation to stop. The only file saved is the machine program file.

After entering the EX command, the user will return to an idle state under TSO.

Note: This simulator has no operands.



## HR--SET HEADER COUNT

Format

HR        n

The HR command controls the number of times the header line will be printed. The header will print every n lines of output.



## RN--RUN n INSTRUCTIONS

## Format

RN        n

The RN command causes the simulator to execute the next n instructions of the machine program file.

Simulation (execution) continues until:

1. n instructions have been executed
2. an error occurs.



## SM--SET MEMORY (CHANGE MEMORY)

## Format

SM      a      n      v<sub>1</sub>      v<sub>2</sub> . . . . v<sub>n</sub>

Starting at memory address a, set n memory positions with the values v<sub>1</sub>, v<sub>2</sub>, . . . . v<sub>n</sub>.

The SM command can be used to enter data before execution or can be used to modify the actual machine program file.



## SR--SET REGISTERS

## Format

SR        r        v

The SR command sets register r to the value v.

The codes for the r operand with corresponding v input bases are:

<u>r</u>	<u>v</u>
P -- Program counter	Hexidecimal
X -- Index register	Hexidecimal
A -- Accumulator A	Integer
B -- Accumulator B	Integer
C -- Condition codes	Bit-string*
S -- Stack pointer	Hexidecimal
T -- Time	Integer

\* To turn all condition codes "on" enter '111111'B.

To turn all condition codes "off" enter '000000'B.



## ERROR MESSAGES

<u>Error Number</u>	<u>Description</u>
301	**** ERROR 301 AAAA Undefined simulator command.
302	**** ERROR 302 AAAA Possible syntax error in simulator command.
306	**** ERROR 306 AAAA The operand in the simulator command caused a register overflow.
313	**** ERROR 313 NNNN The calculated address beyond bounds of memory.

AAAA -- The simulator address which caused the error.

NNNN -- A numeric field.



APPENDIX B

SAMPLE OUTPUT FROM THE  
SIM6800 SIMULATOR PROGRAM



The M6800 program being tested is one designed to add the following two 8-byte binary coded decimal numbers:

```
1357902468097531
+9258147036741852
0616049504839383 (result)
```

The object code exists in a file named "EXAMPLE1". The simulator was started by the statement:

```
exec sim6800(example1)
```

The SR command was used to initialize the program counter with the hexadecimal value 1100. This is the address in memory of the first instruction.

The SM command was used to enter the data values to be added.

A repetition of the RN and DM commands were used to execute the instructions and to display the results.



SIMULATOR FOR THE MOTO DLA M6800 MICROPROCESSOR  
 WRITTEN FOR THE IBM 360  
 VERSION 1 1976

?  
 sm 0102 8 13 57 90 24 68 99 75 31

?  
 sm 010a 8 92 58 14 70 36 74 18 52

?  
 sm 0112 8 0 0 0 0 0 0 0 0

?  
 sr p 1100

?  
 hr 7

?  
 rn 7

IA	OC		EA	P	X	A	B	C	S	T
1100	LDS		1102	1103	0000	0	0	00N000	013F	3
1103	LDX		1105	1106	0102	0	0	00N000	013F	6
1106	STX		0101	1109	0102	0	0	00N000	013F	12
1109	JSR		013E	1000	0102	0	0	00N000	013D	21
1000	LDA	B	1001	1002	0102	0	8	000000	013D	23
1002	LDX		0101	1005	0102	0	8	00N000	013D	28
1005	CLC		1005	1006	0102	0	8	00N000	013D	30

?  
 rn 7

IA	OC		EA	P	X	A	B	C	S	T
1006	LDA	A	0109	1008	0102	31	8	000000	013D	35
1008	ADC	A	0111	100A	0102	83	8	00N0V0	013D	40
100A	DAA		100A	100B	0102	83	8	00N000	013D	42
100B	STA	A	0119	100D	0102	83	8	00N000	013D	48
100D	DEX		100D	100E	0101	83	8	00N000	013D	52
100E	DEC	B	100E	100F	0101	83	7	000000	013D	54
100F	BNE		1010	1008	0101	83	7	000000	013D	58

?



dm 0102 8  
 13 57 90 24 68 37 9 75 31  
 ?  
 dm 010a 8  
 92 58 14 70 36 74 18 52  
 ?  
 dm 0112 8  
 0 0 0 0 0 0 0 83  
 ?  
 rn 7

IA	CC		EA	P	X	A	B	C	S	T
1006	LDA	A	0108	1008	0101	75	7	000000	013D	63
1008	ADC	A	0110	100A	0101	93	7	00N0V0	013D	68
100A	DAA		100A	100B	0101	93	7	00N000	013D	70
100B	STA	A	0118	100D	0101	93	7	00N000	013D	76
100D	DEX		100D	100E	0100	93	7	00H000	013D	80
100E	DEC	B	100E	100F	0100	93	6	000000	013D	82
100F	BNE		1010	1006	0100	93	6	000000	013D	86

?  
 dm 0102 8  
 13 57 90 24 68 9 75 31  
 ?  
 dm 010a 8  
 92 58 14 70 36 74 18 52  
 ?  
 dm 0112 8  
 0 0 0 0 0 0 93 83  
 ?  
 rn 7

IA	CC		EA	P	X	A	B	C	S	T
1006	LDA	A	0107	1008	0100	9	6	000000	013D	91
1008	ADC	A	010F	100A	0100	83	6	000000	013D	96
100A	DAA		100A	100R	0100	83	6	00N000	013D	98
100R	STA	A	0117	100D	0100	83	6	00N000	013D	104
100D	DEX		100D	100E	00FF	83	6	00N000	013D	108
100E	DEC	B	100F	100F	00FF	83	5	000000	013D	110
100F	BNE		1010	1006	00FF	83	5	000000	013D	114

?  
 dm 0102 8  
 13 57 90 24 68 9 75 31  
 ?  
 dm 010a 8  
 92 58 14 70 36 74 18 52  
 ?  
 dm 0112 8  
 0 0 0 0 0 83 93 83  
 ?



rn 7

38

IA	OC		EA	P	X	A	B	C	S	T
1006	LDA	A	0106	1008	00FF	68	5	000000	013D	119
1008	ADC	A	010E	100A	00FF	104	5	00N0V0	013D	124
100A	DAA		100A	100B	00FF	4	5	000000	013D	126
100B	STA	A	0116	100D	00FF	4	5	000000	013D	132
100D	DEX		100D	100E	00FE	4	5	000000	013D	136
100E	DEC	B	100E	100F	00FE	4	4	000000	013D	138
100F	BNE		1010	1006	00FE	4	4	000000	013D	142

?  
dm 0102 8  
13 57 90 24 68 9 75 31

?  
dm 010a 3  
92 58 14 70 36 74 18 52

?  
dm 0112 8  
0 0 0 0 4 83 93 85

?  
rn 7

IA	OC		EA	P	X	A	B	C	S	T
1006	LDA	A	0105	1008	00FE	24	4	000000	013D	147
1008	ADC	A	010D	100A	00FE	95	4	00N0V0	013D	152
100A	DAA		100A	100B	00FE	95	4	00N000	013D	154
100B	STA	A	0115	100D	00FE	95	4	00N000	013D	160
100D	DEX		100D	100E	00FD	95	4	00N000	013D	164
100E	DEC	B	100E	100F	00FD	95	3	000000	013D	166
100F	BNE		1010	1006	00FD	95	3	000000	013D	170

?  
dm 0102 8  
13 57 90 24 68 9 75 31

?  
dm 010a 3  
92 58 14 70 36 74 18 52

?  
dm 0112 8  
0 0 0 95 4 83 93 85

?  
rn 7

IA	OC		EA	P	X	A	B	C	S	T
1006	LDA	A	0104	1008	00FD	90	3	00N000	013D	175
1008	ADC	A	010C	100A	00FD	104	3	00N000	013D	180
100A	DAA		100A	100B	00FD	4	3	000000	013D	182
100B	STA	A	0114	100D	00FD	4	3	000000	013D	188
100D	DEX		100D	100E	00FC	4	3	000000	013D	192
100E	DEC	B	100E	100F	00FC	4	2	000000	013D	194
100F	BNE		1010	1006	00FC	4	2	000000	013D	198

?



```

dm 0102 8          39
  13  57  90  24  68  9  75  31
?
dm 010a 8
  92  58  14  70  36  74  18  52
?
dm 0112 8
  0   0   4  95  4  83  93  83
?
rn 7

```

IA	OC		EA	P	X	A	B	C	S	T
1006	LDA	A	0103	1008	00FC	57		2 00000C	013D	203
1008	ADC	A	0108	100A	00FC	116		2 H0N0V0	013D	208
100A	DAA		100A	100B	00FC	16		2 H0000C	013D	210
100B	STA	A	0113	100D	00FC	16		2 H0000C	013D	216
100D	DEX		100D	100E	00FB	16		2 H0000C	013D	220
100E	DEC	B	100E	100F	00FB	16		1 H0000C	013D	222
100F	BNE		1010	1006	00FB	16		1 H0000C	013D	226

```

?
dm 0102 8
  13  57  90  24  68  9  75  31
?
dm 010a 8
  92  58  14  70  36  74  18  52
?
dm 0112 8
  0  16  4  95  4  83  93  83
?
rn 7

```

IA	OC		EA	P	X	A	B	C	S	T
1006	LDA	A	0102	1008	00FB	13		1 H0000C	013D	231
1008	ADC	A	010A	100A	00FB	106		1 00N000	013D	236
100A	DAA		100A	100B	00FB	6		1 00000C	013D	238
100B	STA	A	0112	100D	00FB	6		1 00000C	013D	244
100D	DEX		100D	100E	00FA	6		1 00000C	013D	248
100F	DEC	B	100E	100F	00FA	6		0 000Z0C	013D	250
100F	BNE		1010	1011	00FA	6		0 000Z0C	013D	254

```

?
dm 0102 8
  13  57  90  24  68  9  75  31
?
dm 010a 8
  92  58  14  70  36  74  18  52
?
dm 0112 8
  6  16  4  95  4  83  93  83
?
ex

```

READY



APPENDIX C

COMPUTER LISTING OF THE SIM6800  
SIMULATOR PROGRAM



MAIN: PROC OPTIONS(MAIN);

```

1      MAIN: PROC OPTIONS(MAIN);
2      OCL 1 MOT(200);
3          OP FIXED BIN,
4          MNEMONIC CHAR(3),
5          ADDR_MODE FIXED BIN,
6          TIME FIXED BIN,
7          BYTES FIXED BIN,
8          MOT_NO FIXED BIN,
9          ADDR_ACC CHAR(1) INIT(' ');
10     DCL M(1:500,2) FIXED BIN;
11     OCL (C,V,Z,N,I,H,ERR) BIT(1) INIT('0'B);
12     OCL BS BIT(15),CC BIT(6);
13     OCL (C1,C2,C3,C4,C5) FIXED BIN;
14     OCL (X,Y,XY) FIXED BIN;
15     OCL HC FIXED BIN INIT(5);
16     OCL $HC FIXED BIN INIT(0);
17     OCL (RYTE2,IA,ADDR) FIXED BIN INIT(0);
18     OCL (ACC_CODE,$ACC_CODE) BIT(1) INIT('0'B);
19     OCL CHAR_P CHAR(4) T;
20     OCL HEXSTR CHAR(26);
21     OCL HEXREP CHAR(16) VAR;
22     OCL CONVERT RETURNS (CHAR(16)VAR);
23     OCL CON RETURNS(FIXED BIN(15));
24     OCL CODE ENTRY(FIXED BIN,FIXED BIN,FIXED BIN,
25     FIXED BIN,FIXED BIN,FIXED BIN,FIXED BIN,FIXED BIN,
26     BIT(1),BIT(1),BIT(1),BIT(1),BIT(1),FIXED BIN);
27     OCL (T,EA,PC,IX,ACCA,ACCB,SP,ACCX) FIXED BIN INIT(0);
28     OCL CC_CHAR CHAR(6);
29     OCL OC_CHAR(3) INIT('000');
30     OCL BUFFER CHAR(120);
31     OCL LBL3(10) LABEL;
32     OCL (Z0,Z1,Z2,Z3) FIXED BIN;
33     OCL Y0 CHAR(2);
34     OCL (Y1,Y2,Y3) CHAR(1);
35     OCL REGISTER CHAR(7) INIT('PXSCART');
36     OCL COMMAND CHAR(14) INIT('SMOMSRRNHRDREX');
37     OCL OSO FILE INPUT;
38     OCL OSM FILE INPUT;
39     OPEN FILE(SYSPRINT) LINESIZE(132);

40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92

PRINT: PROC;
IF $HC=1 THEN DO;
PUT SKIP;
PUT EDIT('IA','OC','EA','P','IX','A','R','C','S','T')
(COL(1),A(2),COL(7),A(2),COL(15),A(2),COL(21),A(1),
COL(27),A(1),COL(35),A(1),COL(41),A(1),COL(47),A(1),
COL(53),A(1),COL(60),A(1));
PUT SKIP;
END;
CC_CHAR='000000';
IF I THEN SUBSTR(CC_CHAR,1,1)='H';
IF J THEN SUBSTR(CC_CHAR,2,1)='I';
IF N THEN SUBSTR(CC_CHAR,3,1)='N';
IF Z THEN SUBSTR(CC_CHAR,4,1)='Z';
IF V THEN SUBSTR(CC_CHAR,5,1)='V';
IF C THEN SUBSTR(CC_CHAR,6,1)='C';
PUT EDIT(CONVERT(UNSPEC(IA)),OC,MOT(MM),ADDR_ACC,
CONVERT(UNSPEC(EA)),
CONVERT(UNSPEC(PC)),CONVERT(UNSPEC(IX)),ACCA,ACCB,CC_CHAR,
CONVERT(UNSPEC(SP)),T)
(COL(1),A(4),COL(7),A(4),COL(12),A(1),COL(15),A(4),
COL(20),A(4),COL(27),A(4),COL(33),F(5),COL(39),F(5),
COL(45),A(6),COL(52),A(4),COL(58),F(5));
PUT SKIP;
END PRINT;

EVAL: PROC;
DCL LBL2(72) LABEL;
LBL2(1)='E1'; LBL2(19)='E19'; LBL2(37)='E37'; LBL2(55)='E55';
LBL2(2)='E2'; LBL2(20)='E20'; LBL2(38)='E38'; LBL2(56)='E56';
LBL2(3)='E3'; LBL2(21)='E21'; LBL2(39)='E39'; LBL2(57)='E57';
LBL2(4)='E4'; LBL2(22)='E22'; LBL2(40)='E40'; LBL2(58)='E58';
LBL2(5)='E5'; LBL2(23)='E23'; LBL2(41)='E41'; LBL2(59)='E59';
LBL2(6)='E6'; LBL2(24)='E24'; LBL2(42)='E42'; LBL2(60)='E60';
LBL2(7)='E7'; LBL2(25)='E25'; LBL2(43)='E43'; LBL2(61)='E61';
LBL2(8)='E8'; LBL2(26)='E26'; LBL2(44)='E44'; LBL2(62)='E62';
LBL2(9)='E9'; LBL2(27)='E27'; LBL2(45)='E45'; LBL2(63)='E63';
LBL2(10)='E10'; LBL2(28)='E28'; LBL2(46)='E46'; LBL2(64)='E64';

```



MAIN: PROC OPTIONS(MAIN);

```

100          LBL2(11)=F11; LBL2(29)=F29; LBL2(47)=F47; LBL2(65)=F65;
101          LBL2(12)=F12; LBL2(30)=F30; LBL2(48)=F48; LBL2(66)=F66;
102          LBL2(13)=F13; LBL2(31)=F31; LBL2(49)=F49; LBL2(67)=F67;
103          LBL2(14)=F14; LBL2(32)=F32; LBL2(50)=F50; LBL2(68)=F68;
104          LBL2(15)=F15; LBL2(33)=F33; LBL2(51)=F51; LBL2(69)=F69;
105          LBL2(16)=F16; LBL2(34)=F34; LBL2(52)=F52; LBL2(70)=F70;
106          LBL2(17)=F17; LBL2(35)=F35; LBL2(53)=F53; LBL2(71)=F71;
107          LBL2(18)=F18; LBL2(36)=F36; LBL2(54)=F54; LBL2(72)=F72;
108          BYTE2=M(PC,2);
109          PC=PC;
110          PC=PC+MOT(MM).BYTES;
111          T=T+MOT(MM).TIME;
112          OC=MOT(MM).MNEMONIC;
113          CALL ADDRESS;
114          IF ADDR>5000 THEN DO;
115          ERR='1'B;
116          PUT SKIP;
117          PUT EDIT('*** ERROR 313 ',CONVERT(UNSPEC(ADDR)),
118          'THE CALCULATED ADDRESS BEYOND BOUNDS OF MEMORY',
119          (COL(1),A(14),COL(16),A(4),SKIP,A));
120          PUT SKIP;
121          RETURN;
122          END;
123          GO TO LBL2(MOT(MM).MOT_NO);
124
125 E1: /* ABA */
126      X=ACCA; Y=ACCB;
127      ACCA=ACCA+ACCB;
128      XY=ACCA;
129      CALL CODE(X,Y,XY,4,4,4,4,6,H,N,Z,V,C,ACCX);
130      RETURN;
131
132 E2: /* ADC */
133      IF MOT(MM).ADDR_MODE >4 THEN ADDR=M(ADDR,2);
134      IF ACC_CODE THEN DO; X=ACCA+BIN(C);
135                          Y=(ADDR);
136                          ACCA=ACCA+ADDR+BIN(C);
137                          XY=(ACCA);
138      END;
139      ELSE DO; X=(ACCB); Y=(ADDR);
140              ACCB=ACCB+ADDR+BIN(C);
141              XY=(ACCB);
142      END;
143      $ACC_CODE=ACC_CODE;
144      CALL CODE(X,Y,XY,4,4,4,4,6,H,N,Z,V,C,ACCX);
145      RETURN;
146
147 E3: /* ADD */
148      IF MOT(MM).ADDR_MODE >4 THEN ADDR=M(ADDR,2);
149      IF ACC_CODE THEN DO; X=ACCA; Y=ADDR;
150                          ACCA=ACCA+ADDR; XY=ACCA;
151                          END;
152      ELSE DO; X=ACCB; Y=ADDR;
153              ACCB=ACCB+ADDR; XY=ACCB;
154      END;
155      CALL CODE(X,Y,XY,4,4,4,4,6,H,N,Z,V,C,ACCX);
156      RETURN;
157
158 E4: /* AND */
159      IF ACC_CODE THEN DO; ACCA=DEC( BIT(ACCA) & BIT(M(ADDR,2)));
160                          XY=ACCA; END;
161      ELSE DO; ACCB=DEC( BIT(ACCB) & BIT(M(ADDR,2)));
162              XY=ACCB; END;
163      CALL CODE(X,Y,XY,1,4,4,2,1,H,N,Z,V,C,ACCX);
164      RETURN;
165
166 E5: /* ASL */
167      IF ADDR=0 THEN DO; IF ACC_CODE THEN REL=ACCA;
168                          ELSE REL=ACCB;
169      END;
170      ELSE REL=M(ADDR,2);
171      BS=BIT(REL);
172      C=SUBSTR(BS,8,1);
173      SUBSTR(BS,8,7)=SUBSTR(BS,9,7);
174      SUBSTR(BS,15,1)='0'B;
175      REL=DEC(BS);
176      XY=REL; CALL CODE(X,Y,XY,1,4,4,1,1,H,N,Z,V,C,ACCX);
177      V=(N&C) | (-N&C);
178      IF ADDR=0 THEN DO; IF ACC_CODE THEN ACCA=REL;
179                          ELSE ACCB=REL;
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212

```



MAIN: PROC OPTIONS(MAIN);

```

215          END;
216          ELSE M(ADDR,2)=REL;
217          RETURN;

218      E6: /* ASR */
219          IF ADDR=0 THEN DO; IF ACC_CODE THEN REL=ACCA;
220                                ELSE REL=ACCB;
221          END;
222          ELSE REL=M(ADDR,2);
223          BS=BIT(REL);
224          I=SUBSTR(BS,8,1); C=SUBSTR(BS,15,1);
225          SURSTR(BS,8,7)=SURSTR(BS,9,7);
226          SURSTR(BS,8,1)=I;
227          I='0'B;
228          REL=DEC(BS);
229          XY=REL; CALL CODE(X,Y,XY,1,4,4,1,1,H,N,Z,V,C,ACCX);
230          V=(N&C) | (-N&C);
231          IF ADDR=0 THEN DO; IF ACC_CODE THEN ACCA=REL;
232                                ELSE ACCB=REL;
233          END;
234          ELSE M(ADDR,2)=REL;
235          RETURN;

236      E7: /* BCC */
237          IF -C THEN PC=PC+2+ADDR;
238          RETURN;

239      E8: /* BCS */
240          IF C THEN PC=PC+2+ADDR;
241          RETURN;

242      E9: /* BEQ */
243          IF Z THEN PC=PC+2+ADDR;
244          RETURN;

245      E10: /* BGE */
246          IF (N&V) | (-N&-V) THEN PC=PC+2+ADDR;
247          RETURN;

248      E11: /* BGT */
249          IF (-Z) & (N&V) | (-N&-V) THEN PC=PC+2+ADDR;
250          RETURN;

251      E12: /* BHI */
252          IF (-C) & (-Z) THEN PC=PC+2+ADDR;
253          RETURN;

254      E13: /* BIT */
255          IF ACC_CODE THEN XY=RIN( BIT(ACCA) & BIT(M(ADDR,2)) );
256                                ELSE XY=RIN( BIT(ACCB) & BIT(M(ADDR,2)) );
257          CALL CODE(X,Y,XY,1,4,4,2,1,H,N,Z,V,C,ACCX);
258          RETURN;

259      E14: /* BLE */
260          IF (Z) | (N&-V) | (-N&V) THEN PC=PC+2+ADDR;
261          RETURN;

262      E15: /* BLS */
263          IF (C) | (Z) THEN PC=PC+2+ADDR;
264          RETURN;

265      E16: /* BLT */
266          IF (N&-V) | (-N&V) THEN PC=PC+2+ADDR;
267          RETURN;

268      E17: /* BMI */
269          IF N THEN PC=PC+2+ADDR;
270          RETURN;

271      E18: /* BNE */
272          IF -Z THEN PC=PC+2+ADDR;
273          RETURN;

274      E19: /* BPL */
275          IF -N THEN PC=PC+2+ADDR;
276          RETURN;

277      E20: /* BRA */
278          PC=PC+2+ADDR;
279          RETURN;

```



MAIN: PROC OPTIONS(MAIN);

```

286      E21: /* RSP */
287          PC=PC+2;
288          SP=SP-2;
289          PC=PC+ADDR;
          RETURN;

290      E22: /* BVC */
291          IF ~V THEN PC=PC+2+ADDR;
292          RETURN;

293      E23: /* BVS */
294          IF V THEN PC=PC+2+ADDR;
295          RETURN;

296      E24: /* CRA */
297          REL=ACCA-ACCB;
298          X=ACCA; Y=ACCB; XY=REL;
299          CALL CODE(X,Y,XY,1,4,4,5,5,H,N,Z,V,C,ACCX);
300          RETURN;
301

302      E25: /* CLC */
303          C='0'B;
          RETURN;

304      E27: /* CLR */
305          IF ADDR=0 THEN DO; IF ACC_CODE THEN DO; ACCA=0;
306                          XY=ACCA; END;
307                          ELSE DO; ACCB=0;
308                          XY=ACCB; END;
309          END;
310          ELSE DO; M(ADDR,2)=0; XY=M(ADDR,2); END;
311          CALL CODE(X,Y,XY,1,2,3,2,2,H,N,Z,V,C,ACCX);
312          RETURN;

322      E28: /* CLV */
323          V='0';
          RETURN;

324      E29: /* CMP */
325          IF ACC_CODE THEN REL=ACCA;
326          ELSE REL=ACCB;
327          X=REL; Y=ADDR;
328          REL=REL-ADDR;
329          XY=REL; CALL CODE(X,Y,XY,1,4,4,5,5,H,N,Z,V,C,ACCX);
330          IF REL<0 THEN N='1';
331          IF REL=0 THEN Z='1';
332          RETURN;

333      E30: /* COM */
334          IF ADDR=0 THEN DO; IF ACC_CODE THEN DO; ACCA=DEC(~BIT(ACCA));
335                          XY=ACCA; END;
336                          ELSE DO; ACCB=DEC(~BIT(ACCB));
337                          XY=ACCB; END;
338          END;
339          ELSE DO; M(ADDR,2)=DEC(~BIT(M(ADDR,2))); END;
340          CALL CODE(X,Y,XY,1,4,4,2,3,H,N,Z,V,C,ACCX);
341          RETURN;

354      E31: /* CPX */
355          X=IX; Y=ADDR;
356          REL=IX-ADDR;
357          XY=REL; CALL CODE(X,Y,XY,1,4,4,4,1,H,N,Z,V,C,ACCX);
358          RETURN;

360      E32: /* DAA */
361          CALL CODE(X,Y,XY,1,4,4,2,7,H,N,Z,V,C,ACCX);
362          IF $ACC_CODE THEN ACCA=ACCX;
363          ELSE ACCB=ACCX;
364          RETURN;

365      E34: /* DES */
366          SP=SP-1;
          RETURN;

367      E36: /* EOR */
368          IF ACC_CODE THEN DO;
369          ACCA=DEC((BIT(ACCA)&~BIT(M(ADDR,2))) | (~BIT(ACCA)&BIT(M(ADDR,2))));
370          XY=ACCA; END;
371          ELSE DO;
372          ACCB=DEC((BIT(ACCB)&~BIT(M(ADDR,2))) | (~BIT(ACCB)&BIT(M(ADDR,2))));
373          XY=ACCB; END;
374

```



MAIN: PROC OPTIONS(MAIN);

```

376          CALL CODE(X,Y,XY,1,4,4,2,1,H,N,Z,V,C,ACCX);
377          RETURN;

378      E37: /* INC */
379          IF ADDR = 0 THEN DO; X=M(ADDR,2); M(ADDR,2)=M(ADDR,2)+1;
382              XY=M(ADDR,2); END;
384          ELSE DO; IF ACC_CODE THEN DO; X=ACCA; ACCA=ACCA-1;
389              XY=ACCA; END;
391              ELSE DO; X=ACCB; ACCB=ACCB+1;
394              XY=ACCB; END;
396          END;
397          CALL CODE(X,Y,XY,1,4,4,1,1,H,N,Z,V,C,ACCX);
398          IF X=127 THEN V='1'B; ELSE V='0'B;
401          RETURN;

402      E38: /* INS */
403          SP=SP+1;
404          RETURN;

405      E39: /* INX */
406          IX=IX+1;
407          XY=IX; CALL CODE(X,Y,XY,1,1,4,1,1,H,N,Z,V,C,ACCX);
408          RETURN;

409      E40: /* JUMP */
410          PC=ADDR;
411          RETURN;

412      E33: /* DEC */
413          IF ADDR = 0 THEN DO;
414              X=BIT(M(ADDR,2));
415              M(ADDR,2)=M(ADDR,2)-1;
416              XY=BIT(M(ADDR,2));
417              GO TO E333;
418          END;
419          IF ACC_CODE THEN DO; X=(ACCA);
420              ACCA=ACCA-1;
421              XY=(ACCA);
422          END;
423          ELSE DO; X=(ACCB); ACCB=ACCB-1;
424              XY=(ACCB);
425          END;
426      E333: CALL CODE(X,Y,XY,1,4,4,1,1,H,N,Z,V,C,ACCX);
427          IF BIN(X)>80 THEN V='1'B; ELSE V='0'B;
428          RETURN;

429      E35: /* DEX */
430          IX=IX-1;
431          XY=(IX);
432          CALL CODE(X,Y,XY,1,1,4,1,1,H,N,Z,V,C,ACCX);
433          RETURN;

434      E41: /* JSR */
435          EA=SP-1;
436          M(SP,2)=PC;
437          SP=SP-2;
438          PC=ADDR;
439          RETURN;

440      E42: /* LDA */
441          IF MOT(MM).ADDR_MODE > 4 THEN ADDR=M(ADDR,2);
442          IF ACC_CODE THEN DO; ACCA=ADDR; XY=(ACCA); END;
443          ELSE DO; ACCB=ADDR; XY=(ACCB); END;
444          CALL CODE(X,Y,XY,1,4,4,2,1,H,N,Z,V,C,ACCX);
445          RETURN;

446      E43: /* LDS */
447          IF MOT(MM).ADDR_MODE > 4 THEN ADDR=M(ADDR,2);
448          SP=ADDR;
449          XY=(SP);
450          CALL CODE(X,Y,XY,1,4,4,2,1,H,N,Z,V,C,ACCX);
451          RETURN;

452      E44: /* LDX */
453          IF MOT(MM).ADDR_MODE > 4 THEN DO;
454              ADDR=M(ADDR,2);
455          END;
456          IX=ADDR;
457          XY=(IX);
458          CALL CODE(X,Y,XY,1,4,4,2,1,H,N,Z,V,C,ACCX);
459          RETURN;

```



MAIN: PROC OPTIONS(MAIN);

```

469      E45: /* LSR */
470          IF ADDR=0 THEN DO; IF ACC_CODE THEN REL=ACCA;
471                                ELSE REL=ACCB;
472          END;
473          ELSE REL=M(ADDR,2);
474          BS=BIT(REL);
475          C=SUBSTR(BS,15,1);
476          SUBSTR(BS,8,7)=SUBSTR(BS,9,7);
477          SUBSTR(BS,8,1)='0'B;
478          REL=DEC(BS);
479          XY=REL; CALL CODE(X,Y,XY,1,2,4,1,1,H,N,Z,V,C,ACCX);
480          V=(N&-C) | (~N&C);
481          IF ADDR=0 THEN DO; IF ACC_CODE THEN ACCA=REL;
482                                ELSE ACCB=REL;
483          END;
484          ELSE M(ADDR,2)=REL;
485          RETURN;
486
492      E46: /* NEG */
493          IF ADDR=0 THEN DO;
494              IF ACC_CODE THEN DO; X=ACCA; ACCA=0-ACCA;
495                                  XY=ACCA; END;
496              ELSE DO; X=ACCB; ACCB=0-ACCB;
497                          XY=ACCB; END;
498          END;
499          ELSE DO; X=M(ADDR,2); M(ADDR,2)=0-M(ADDR,2);
500                  XY=M(ADDR,2); END;
501          CALL CODE(X,Y,XY,1,4,4,1,1,H,N,Z,V,C,ACCX);
502          IF X=80 THEN V='1'B; ELSE V='0'B;
503          IF X=0 THEN C='1'B; ELSE C='0'B;
504          RETURN;
505
519      E47: /* NOP */
520          RETURN;
521
522      E48: /* ORA */
523          IF ACC_CODE THEN DO; ACCA=DEC( BIT(ACCA) | BIT(M(ADDR,2)) );
524                                  XY=ACCA; END;
525          ELSE DO; ACCB=DEC( BIT(ACCB) | BIT(M(ADDR,2)) );
526                                  XY=ACCB; END;
527          CALL CODE(X,Y,XY,1,4,4,2,1,H,N,Z,V,C,ACCX);
528          RETURN;
529
531      E49: /* PSH */
532          IF ACC_CODE THEN M(SP,2)=ACCB;
533          ELSE M(SP,2)=ACCB;
534          SP=SP-1;
535          RETURN;
536
537      E50: /* PUL */
538          SP=SP+1;
539          IF ACC_CODE THEN ACCA=M(SP,2);
540          ELSE ACCB=M(SP,2);
541          RETURN;
542
543      E51: /* ROL */
544          IF ADDR=0 THEN DO; IF ACC_CODE THEN REL=ACCA;
545                                ELSE REL=ACCB;
546          END;
547          ELSE REL=M(ADDR,2);
548          BS=BIT(REL);
549          I=C;
550          C=SUBSTR(BS,8,1);
551          SUBSTR(BS,8,7)=SUBSTR(BS,9,7);
552          SUBSTR(BS,15,1)=I;
553          I='0'B;
554          REL=DEC(BS);
555          XY=REL; CALL CODE(X,Y,XY,1,4,4,1,1,H,N,Z,V,C,ACCX);
556          V=(N&-C) | (~N&C);
557          IF ADDR=0 THEN DO; IF ACC_CODE THEN ACCA=REL;
558                                ELSE ACCB=REL;
559          END;
560          ELSE M(ADDR,2)=REL;
561          RETURN;
562
566      E52: /* ROR */
567          IF ADDR=0 THEN DO; IF ACC_CODE THEN REL=ACCA;
568                                ELSE REL=ACCB;
569          END;
570          ELSE REL=M(ADDR,2);
571          RETURN;
572

```



MAIN: PROC OPTIONS(MAIN);

```

573          BS=BIT(REL);
574          I=SUBSTR(BS,15,1);
575          SUBSTR(BS,8,7)=SUBSTR(BS,8,7);
576          SUBSTR(BS,8,1)=C;
577          C=I;
578          I='0'B;
579          REL=DEC(BS);
580          XY=REL; CALL CODE(X,Y,XY,1,4,4,1,1,H,N,Z,V,C,ACCX);
582          V=(N&C) | (~N&C);
583          IF ADDR=0 THEN DO; IF ACC_CODE THEN ACCA=REL;
587                                     ELSE ACCB=REL;
588          END;
589          ELSE M(ADDR,2)=REL;
590          RETURN;

591      E54: /* RTS */
592          SP=SP+2;
593          PC=M(SP,2);
594          EA=SP;
595          RETURN;

596      E55: /* SBA */
597          ACCA=ACCA-ACCB;
598          RETURN;

599      E56: /* SBC */
600          IF MOT(MM),ADDR MODE > 4 THEN ADDR=M(ADDR,2);
601          IF ACC_CODE THEN ACCA=ACCA-ADDR-C;
602                                     ELSE ACCB=ACCB-ADDR-C;
603          RETURN;

604      E57: /* SEC */
605          C='1'B;
606          RETURN;

607      E59: /* SEV */
608          V='1'B;
609          RETURN;

610      E60: /* STA */
611          IF ACC_CODE THEN DO; M(ADDR,2)=ACCA;
612                                     XY=(ACCA);
613          END;
614          ELSE DO; M(ADDR,2)=ACCB;
615                                     XY=(ACCB);
616          END;
617          CALL CODE(X,Y,XY,1,4,4,2,1,H,N,Z,V,C,ACCX);
618          RETURN;

619      E61: /* STS */
620          M(ADDR,2)=SP;
621          XY=SP; CALL CODE(X,Y,XY,1,4,4,2,1,H,N,Z,V,C,ACCX);
622          RETURN;

623      E62: /* STX */
624          M(ADDR,2)=IX;
625          XY=IX; CALL CODE(X,Y,XY,1,4,4,2,1,H,N,Z,V,C,ACCX);
626          RETURN;

627      E63: /* SJR */
628          IF MOT(MM),ADDR MODE > 4 THEN ADDR=M(ADDR,2);
629          IF ACC_CODE THEN ACCA=ACCA-ADDR;
630                                     ELSE ACCB=ACCB-ADDR;
631          RETURN;

632      E65: /* TAB */
633          ACCR=ACCA;
634          XY=ACCR; CALL CODE(X,Y,XY,1,4,4,2,1,H,N,Z,V,C,ACCX);
635          RETURN;

636      E66: /* TAP */
637          BS=BIT(ACCA);
638          CC=SUBSTR(BS,10,6);
639          N=SUBSTR(CC,1,1); I=SUBSTR(CC,2,1); N=SUBSTR(CC,3,1);
640          Z=SUBSTR(CC,4,1); V=SUBSTR(CC,5,1); C=SUBSTR(CC,6,1);
641          RETURN;

642      E67: /* TBA */
643          ACCA=ACCB;
644          XY=ACCA; CALL CODE(X,Y,XY,1,4,4,2,1,H,N,Z,V,C,ACCX);
645          RETURN;

```



MAIN: PROC OPTIONS(MAIN);

```

649      E68: /* TPA */
650          CC=H || I || N || Z || V || C;
651          SUBSTR(BS,8,2)='11';
652          SUBSTR(BS,10,6)=CC;
653          ACCA=DEC(BS);
654          RETURN;
655
656      E69: /* TST */
657          IF ADDR=0 THEN DO: IF ACC_CODE THEN XY=ACCA;
658                          ELSE XY=ACCB;
659          END;
660          ELSE XY=M(ADDR,2);
661          CALL CODE(X,Y,XY,1,4,4,2,2,H,N,Z,V,C,ACCX);
662          RETURN;
663
664      E70: /* TSX */
665          IX=SP+1;
666          RETURN;
667
668      E71: /* TXS */
669          SP=IX-1;
670          RETURN;
671
672      E99: RETURN;
673          END EVAL;
674
675  ADDRESS: PROC;
676      OCL ONE FIXED RIN: XX BIT(15);
677      OCL LBL1(7) LABEL;
678      LBL1(1)=A1;
679      LBL1(2)=A2;
680      LBL1(3)=A3;
681      LBL1(4)=A4;
682      LBL1(5)=A5;
683      LBL1(6)=A6;
684      LBL1(7)=A7;
685      IF (MOT(MM).ADDR_ACC='A') THEN ACC_CODE='1'R;
686      ELSE IF (MOT(MM).ADDR_ACC='B') THEN ACC_CODE='0'B;
687      GO TO LBL1(MOT(MM).ADDR_MODE);
688
689  A1: /* INHERENT */
690      EA=SP;
691      RETURN;
692
693  A2: /* RELATIVE */
694      EA=SP+1;
695      IF BYTE2 >= 240 THEN BYTE2=(255-BYTE2+1) * (-1);
696      ADDR=BYTE2;
697      RETURN;
698
699  A3: /* IMMEDIATE */
700      IF MOT(MM).MOT_NO = 31 |
701          MOT(MM).MOT_NO = 43 |
702          MOT(MM).MOT_NO = 44 THEN EA=SP+2;
703      ELSE EA=SP+1;
704      ADDR=BYTE2;
705      RETURN;
706
707  A4: /* ACCUMULATOR */
708      EA=SP;
709      ADDR=0;
710      RETURN;
711
712  A5: /* INDEXED */
713      EA=BYTE2+IX;
714      ADDR=BYTE2+IX;
715      RETURN;
716
717  A6: /* EXTENDED */
718      ADDR=BYTE2;
719      EA=ADDR+1;
720      RETURN;
721
722  A7: /* DIRECT */
723      ADDR=BYTE2;
724      EA=ADDR+1;
725      RETURN;
726
727  END ADDRESS;

```



MAIN: PROC OPTIONS(MAIN);

```

709      LKUP: PROC;
710          DO MM=1 BY 1 TO 197;
711          IF M(PC,1)=MOT(MM).OP THEN GO TO LK1;
713          END;
714      LK1:  END LKUP;

715      CODE: PROC (XX,YY,XYXY,C1,C2,C3,C4,C5,H,N,Z,V,C,&ACCX);
716          DCL (H,N,Z,V,C) BIT(1);
717          DCL (C1,C2,C3,C4,C5) FIXED BIN;
718          DCL (X,Y,XY) BIT(15) INIT( (15) '0'B);
719          DCL (XX,YY,XYXY,ACCX,LO,UP) FIXED BIN;
720          DCL (BITUP,BITLO) BIT(15);
721          DCL (LBL3(4),LBL4(4),LBL5(4),LBL6(5),LBL7(5)) LABEL;

722          LBL3(1)=CC2; LBL4(1)=CC3; LBL5(1)=CC4; LBL6(1)=CC5; LBL7(1)=CC6;
727          LBL3(2)=HCL; LBL4(2)=NCL; LBL5(2)=ZCL; LBL6(2)=VCL; LBL7(2)=CCL;
732          LBL3(3)=HS;  LBL4(3)=NS;  LBL5(3)=ZS;  LBL6(3)=VS;  LBL7(3)=CS;
737          LBL3(4)=HP;  LBL4(4)=NP;  LBL5(4)=ZP;  LBL6(4)=VP;  LBL7(4)=CP;
742          LBL6(5)=VP2; LBL7(5)=CP2;

744          UP=XX/10; BITUP=BIT(UP);
746          LO=XX-FLOOR(XX/10)*10; BITLO=BIT(LO);
748          SUBSTR(X,8,8)=SUBSTR(BITUP,12,4) || SUBSTR(BITLO,12,4);
749          UP=YY/10; BITUP=BIT(UP);
751          LO=YY-FLOOR(YY/10)*10; BITLO=BIT(LO);
753          SUBSTR(Y,8,8)=SUBSTR(BITUP,12,4) || SUBSTR(BITLO,12,4);
754          IF C5<=5 THEN DO;
756              UP=XYXY/10; BITUP=BIT(UP);
758              LO=XYXY-FLOOR(XYXY/10)*10; BITLO=BIT(LO);
760              SUBSTR(XY,8,8)=SUBSTR(BITUP,12,4) || SUBSTR(BITLO,12,4);
761          END;
762          ELSE DO;
763              UP=BIN(SUBSTR(X,8,4)) + BIN(SUBSTR(Y,8,4));
764              LO=BIN(SUBSTR(X,12,4)) + BIN(SUBSTR(Y,12,4));
765              IF LO>=16 THEN DO; LO=LO-16; UP=UP+1; END;
770              BITUP=BIT(UP); BITLO=BIT(LO);
772              SUBSTR(XY,8,8)=SUBSTR(BITUP,12,4) || SUBSTR(BITLO,12,4);
773          END;
774          IF C5=6 THEN C5=4;
776          IF C5<7 THEN GO TO CC1;
778              LO=BIN(SUBSTR(XY,12,4));
779              IF LO>9 | H='1'B THEN LO=LO+6;
781              UP=BIN(SUBSTR(XY,8,4));
782              IF LO>=16 THEN DO; LO=LO-16; UP=UP+1; END;
787              IF UP>9 | C='1'B THEN DO; UP=UP+6; C='1'B; END;
792              ELSE C='0'B;
793              BITUP=BIT(UP); BITLO=BIT(LO);
795              XY='0000000'B || SUBSTR(BITUP,12,4) || SUBSTR(BITLO,12,4);
796              ACCX=BIN(SUBSTR(BITUP,12,4))*10 + BIN(SUBSTR(BITLO,12,4));
797              C5=1;

798      CC1:  GO TO LBL3(C1);
799      HCL:  H='0'B; GO TO CC2;
801      HS:   H='1'B; GO TO CC2;
803      ID:   H=( SUBSTR(X,12,1) & SUBSTR(Y,12,1) ) |
              ( SUBSTR(Y,12,1) & -SUBSTR(XY,12,1) ) |
              (-SUBSTR(XY,12,1) & SUBSTR(X,12,1));

804      CC2:  GO TO LBL4(C2);
805      NCL:  N='0'B; GO TO CC3;
807      NS:   N='1'B; GO TO CC3;
809      NP:   N=SUBSTR(XY,8,1);
810      CC3:  GO TO LBL5(C3);
811      ZCL:  Z='0'B; GO TO CC4;
813      ZS:   Z='1'B; GO TO CC4;
815      ZP:   Z=-SUBSTR(XY,9,1) & -SUBSTR(XY,9,1) &
              -SUBSTR(XY,10,1) & -SUBSTR(XY,11,1) &
              -SUBSTR(XY,12,1) & -SUBSTR(XY,13,1) &
              -SUBSTR(XY,14,1) & -SUBSTR(XY,15,1);

816      CC4:  GO TO LBL6(C4);
817      VCL:  V='0'B; GO TO CC5;
819      VS:   V='1'B; GO TO CC5;
821      VP:   V=( SUBSTR(X,8,1) & SUBSTR(Y,8,1) & -SUBSTR(XY,8,1) ) |
              (-SUBSTR(X,8,1) & -SUBSTR(Y,8,1) & SUBSTR(XY,8,1));

```



```
MAIN: PROC OPTIONS(MAIN);
```

```

822      GO TO CCS;
823      VP2: V=( SUBSTR(X,8,1) & -SUBSTR(Y,8,1) & -SUBSTR(XY,8,1) ) |
          (-SUBSTR(X,8,1) & SUBSTR(Y,8,1) & SUBSTR(XY,8,1));
824      CCS: GO TO LRL7(CC5);
825      CCL: C='0'B; GO TO CC5;
826      CS: C='1'B; GO TO CC6;
827      CP: C=( SUBSTR(X,8,1) & SUBSTR(Y,8,1) ) |
          ( SUBSTR(Y,8,1) & -SUBSTR(XY,8,1) ) |
          (-SUBSTR(XY,8,1) & SUBSTR(X,8,1) );
830      GO TO CC6;
831      CP2: C=( -SUBSTR(X,8,1) & SUBSTR(Y,8,1) ) |
          ( SUBSTR(Y,8,1) & SUBSTR(XY,8,1) ) |
          ( SUBSTR(XY,8,1) & -SUBSTR(X,8,1) );
832      CC6: RETURN;
833      END CODE;

834      CONVERT: PROC(A) RETURNS(CHAR(16)VAR);
835      DCL A BIT(*),HEXREP CHAR(16)VAR INIT(''),
          HEX_DIGITS CHAR(16) INIT('0123456789ABCDEF') STATIC,
          TABLE(0:15) CHAR(1) DEF HEX_DIGITS.DIGIT FIXED BIN(4);
836      LP: DO K=1 BY 1 TO LENGTH(A)/4;
837          DIGIT=SUBSTR(A,4*K-3,4);
838          HEXREP=HEXREP||TABLE(DIGIT);
839          END LP;
840      RETURN(HEXREP);
841      END CONVERT;

842      CON: PROC(CHAREP) RETURNS(FIXED BIN(15));
843      DCL CHAREP CHAR(4);
844      DCL BITS FIXED BIN;
845      DCL DIGIT CHAR(15) INIT('123456789ABCDEF');
846      BITS=0;
847      DO II=1 BY 1 TO 4;
848          K=INDEX(DIGIT,SUBSTR(CHAREP,II,1));
849          BITS=BITS+(K)*(16**(4-II));
850      END;
851      RETURN(BITS);
852      END CON;

853      SIM: PROC;
854      IA=PC;
855      CALL L&UP;
856      CALL EVAL;
857      IF ERD THEN RETURN;
858      ADDR=0;
859      SHC=SHC+1;
860      IF SHC>HC THEN SHC=1;
861      CALL PRINT;
862      RETURN;
863      END SIM;

864      CREATE1: PROC;
865      DO MM=1 BY 1 TO 197;
866          GET FILE(DSM) EDIT(MOT(MM))
            (COL(1),F(3),COL(5),A(3),COL(9),F(1),COL(11),F(1),COL(13),F(1),
            COL(15),F(2),COL(18),A(1));
867      END;
868      RETURN;
869      END CREATE1;

870      CREATE2: PROC;
871      ON ENDFILE(DSO) GO TO INEND;
872      DO WHILE('1'B);
873          GET FILE(DSO) LIST(NN,N1,N2);
874          M(NN,1)=N1;
875          M(NN,2)=N2;
876      END;
877      INEND: RETURN;
878      END CREATE2;

879      ON ERROR BEGIN;
880      PUT SKIP;
881      PUT EDIT('*** ERROR 302 ',Y0,
            'POSSIBLE SYNTAX ERROR IN SIMULATOR COMMAND')
            (COL(1),A(15),COL(17),A(2),SKIP,COL(1),A);
882      PUT SKIP;
883      GO TO M&STRT;
884      END;
885      STRT: PUT SKIP;

```



```
MAIN: PROC OPTIONS(MAIN);
```

```

890          PUT EDIT('SIMULATOR FOR THE MOTOROLA M6800 MICROPROCESSOR',
                   'WRITTEN FOR THE IBM 360',
                   'VERSION 1          1976')
                   (COL(5),A,SKIP,COL(15),A,SKIP,COL(15),A);
891          PUT SKIP;
892          MINT: CALL CREATE1;
893          CALL CREATE2;
894          M5TRT:
895          PUT SKIP;
896          PUT EDIT('?')(COL(1),A(1));
897          PUT SKIP;
898          READ FILE(SYSIN) INTO(RUFFER);
899          Z0=VERIFY(RUFFER,' ');
900          BUFFER=SUBSTR(BUFFER,Z0);
901          GET STRING(RUFFER) EDIT(Y0)(A(2));
902          Z0=INDEX(BUFFER,' ');
903          BUFFER=SUBSTR(BUFFER,Z0);
904          Z0=INDEX(COMMAND,Y0);
905          IF Z0=0 THEN DO;
906          PUT SKIP;
907          PUT EDIT('*** ERROR 301 ',Y0,
                   'UNDEFINED SIMULATOR COMMAND')
                   (COL(1),A(15),COL(17),A(2),SKIP,COL(1),A);
908          PUT SKIP;
909          GO TO M5TRT;
910          END;
911          Z0=(Z0+1)/2;
912          LBL3(1)=M1;
913          LBL3(2)=M2;
914          LBL3(3)=M3;
915          LBL3(4)=M4;
916          LBL3(5)=M5;
917          LBL3(6)=M6;
918          LBL3(7)=M7;
919          GO TO LBL3(Z0);
920          M1: /* SET MEMORY */
921          Z0=VERIFY(RUFFER,' ');
922          BUFFER=SUBSTR(BUFFER,Z0);
923          GET STRING(RUFFER) EDIT(CHAREP)(A(4));
924          Z0=INDEX(BUFFER,' ');
925          BUFFER=SUBSTR(BUFFER,Z0);
926          GET STRING(RUFFER) LIST(          Z2);
927          Z1=CON(CHAREP);
928          Z0=Z1+Z2-1;
929          GET STRING(BUFFER) LIST(          Z2,(M(Z3+2) DO Z3=71 TO Z0));
930          GO TO M5TRT;
931          M2: /* DISPLAY MEMORY */
932          Z0=VERIFY(RUFFER,' ');
933          BUFFER=SUBSTR(BUFFER,Z0);
934          GET STRING(RUFFER) EDIT(CHAREP)(A(4));
935          Z0=INDEX(BUFFER,' ');
936          BUFFER=SUBSTR(BUFFER,Z0);
937          GET STRING(RUFFER) LIST(Z2);
938          Z1=CON(CHAREP);
939          Z2=Z2+Z1-1;
940          Z0=MOD(Z2,12);
941          IF Z0=0 THEN Z0=Z2/12;
942          ELSE Z0=Z2/12+1;
943          PUT EDIT((M(Z3+2) DO Z3=Z1 TO Z2))((Z0)(12 F(5),SKIP));
944          GO TO M5TRT;
945          M3: /* SET REGISTERS */
946          Z0=VERIFY(RUFFER,' ');
947          BUFFER=SUBSTR(BUFFER,Z0);
948          GET STRING(RUFFER) EDIT(Y1)(A(1));
949          Z0=INDEX(BUFFER,' ');
950          BUFFER=SUBSTR(BUFFER,Z0);
951          Z0=VERIFY(RUFFER,' ');
952          BUFFER=SUBSTR(BUFFER,Z0);
953          Z0=INDEX(REGISTER,Y1);
954          IF Z0>4 THEN GO TO M3_2;
955          IF Z0=4 THEN GO TO M3_3;
956          M3_1: GET STRING(RUFFER) EDIT(CHAREP)(A(4));
957          IF Z0=1 THEN PC=CON(CHAREP);
958          IF Z0=2 THEN IX=CON(CHAREP);
959          IF Z0=3 THEN SP=CON(CHAREP);
960          IF PC>5000 | SP>5000 | IX>5000 THEN DO;
961          PUT SKIP;
962          PUT SKIP;

```



MAIN: PROC OPTIONS(MAIN);

```

966          PUT EDIT('*** ERROR 306 ',Y1,
          'THE OPERAND IN THE SIMULATOR COMMAND ',
          'CAUSED A REGISTER OVERFLOW')
          (COL(1),A(15),COL(17),A(1),SKIP,COL(1),A,SKIP,COL(1),A);
967          PUT SKIP;
968          GO TO MSTRT;
969          END;
970          GO TO MSTRT;
971          M3_2: GET STRING(BUFFER) LIST(Z1);
972          IF Z0=5 THEN ACCA=Z1;
974          IF Z0=6 THEN ACCB=Z1;
976          IF Z0=7 THEN T=Z1;
978          GO TO MSTRT;

979          M3_3: GET STRING(BUFFER) EDIT(CC)(R(6));
980          H=SUBSTR(CC,1,1); I=SUBSTR(CC,2,1); N=SUBSTR(CC,3,1);
983          Z=SUBSTR(CC,4,1); V=SUBSTR(CC,5,1); C=SUBSTR(CC,6,1);
986          GO TO MSTRT;

987          M4: /* RUN */
          GET STRING(BUFFER) LIST(Z1);
988          DO Z2=1 BY 1 TO Z1;
989          CALL SIM;
990          IF ERR THEN GO TO MSTRT;
992          END;
993          GO TO MSTRT;

994          M5: /* SET HEADER COUNT */
          GET STRING(BUFFER) LIST(Z1);
995          HC=Z1;
996          SHC=0;
997          GO TO MSTRT;

999          M6: /* DISPLAY REGISTERS */
          CALL PRINT;
999          GO TO MSTRT;

1000         M7: /* EXIT */
          END MAIN;

```



## BIBLIOGRAPHY

- Cohen, Leo J. Operating System Analysis and Design.  
Rochelle Park, N.J.: Hayden Book Company, Inc., 1970.
- M6800 Microprocessor Programming Manual. Motorola Semi-  
conductor Products, Inc., 1975.
- Ogdin, Jerry L. "Microprocessors: The Inevitable Tech-  
nology." Modern Data 8 (January 1975): 42-47.
- O'Malley, John. The Digital Computer. New York: Holt,  
Rinehart, and Winston, Inc., 1972.
- Struble, George. Assembler Language Programming: The IBM  
System/360. Reading, Massachusetts: Addison-Wesley  
Publishing Company, 1971.