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The General Purpose Interface Bus

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BY

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ABSTRACT

The General Purpose Interface Bus, as defined by the IEEE Standard, deals with systems that require digital data to be transferred between a group of instruments. An overview of this standard is presented which summarizes the interface's capabilities, functions and versatility by explaining the basic interface concepts. In addition, a GPIB testing application and a GPIB related design example are presented and investigated.

Herbert C. Towle

Herbert C. Towle, Chairman

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GLOSSARY OF TERMS

ASCII - The American standard code for intercommunication interfaces

BIT - A single amount of digital information with the capability of off (equal to zero) or on (equal to one)

BYTE - A group of eight bits, usually with the most significant bit being bit eight and least significant bit being bit one

CONTROLLER - A device on the GPIB that has the capability to control and configure the interface at all times

GPIB - The General Purpose Interface Bus

HANDSHAKE - The asynchronous process used by the GPIB to transfer a message byte across the interface

IEEE-488, 1978 - The Institute of Electrical and Electronics Engineers published standard titled "IEEE Standard Digital Interface for Programmable Instrumentation", copyrighted in 1978

INSTRUMENTS - Any device used to perform tests, store test results or provide displays of tests or results

INTERFACE - The actual hardware and format conventions used for the interconnection of two items

I/O DEVICE - Input/Output device

LISTEN ADDRESS - A seven bit ASCII address used to configure a GPIB device to receive data

LISTENER - A device on the GPIB with the capability of receiving information from the interface

LSB - Least significant bit

MESSAGE - A seven bit ASCII code, sent over the GPIB interface, that represents addresses, commands, or data

MSB - Most significant bit

NETWORK - Any configuration or test setup of devices that are configured to a GPIB interface

TALK ADDRESS - A seven bit ASCII address used to configure a GPIB device to transmit data

TALKER - A device on the GPIB with the capability of transmitting information on the interface

INTRODUCTION

Generally, systems interfacing between dissimilar devices requires customized hardware and software which involves expensive designs with extensive code and format manipulations. One solution to the interfacing problem is an innerconnection standard that utilizes a compact but versatile interface. Throughout the instrumentation industry, this standard is the IEEE-488, 1978, "The IEEE Standard Interface For Programmable Instrumentation". This standard interface, also known as the General Purpose Interface Bus (GPIB) or the Hewlett Packard Interface Bus, deals with systems that require digital data to be transferred between a group of instruments, computer peripherals or system components (Hewlett-Packard 1975).

The IEEE-488, 1978, is a rigid standard, being comprised of complex state diagrams and extensive acronyms that often provides an overabundance of information which the system designer or casual GPIB user does not require. The objective of this paper is to provide a working overview of the IEEE-488 by: (1) providing a summary of the General Purpose Interface Bus, it's capabilities and functions, and (2) demonstrating the versatility of the interface by investigating an actual GPIB testing application.

GENERAL PURPOSE INTERFACE BUS FUNCTIONAL OVERVIEW

The IEEE-488, 1978, Standard provides the designer and system user with explicit guidelines and requirements for the General Purpose Interface Bus. The Standard supplies complete function explanations of every interface operation and provides state diagrams for every known device related mode of operation. The General Purpose Interface Bus provides an interconnection standard that uses a byte-serial, bit parallel approach to the transfer of digital data and specifies hardware and software requirements which ultimately ease the interconnection of any device network or custom instrumentation system. As an overview of the General Purpose Interface Bus (GPIB) the interface will be investigated in four areas:

1. GPIB Interface Capabilities
2. GPIB Interface Functions
3. GPIB Interface Signals
4. GPIB Example Testing Network

INTERFACE FUNCTIONAL CAPABILITIES

The IEEE-488, 1978, provides a standard for interface systems used to interconnect programmable and nonprogrammable devices and has the following general capabilities:

1. Data exchange on the interface is in digital format

2. The number of devices in any GPIB configuration is 15

3. Total cable length of any GPIB network is 20 meters

4. Data exchange is limited to 1 megabyte/second maximum

The General Purpose Interface Bus uses a simplistic architecture as a basis for all communication or information transfer on the interface. This basic methodology specifies all devices on the interface as 'talkers', 'listeners', 'controllers', or a combination of each. A 'controller' is a device, calculator, or minicomputer capable of governing the GPIB interface. A controller has the power to seize control of the bus at any time and to dictate which devices are active, which devices are 'talkers', and which devices are 'listeners'. A 'talker' is a device configured by the controller to transmit information. A 'listener' is a device configured by the controller to receive information from a talker. Due to the bidirectional nature of the data lines, there may be only one talker at any one time, but multiple listeners may be receiving data simultaneously. As an added insight, the controller may configure himself as a talker or listener to send or receive data respectively.

The General Purpose Interface Bus uses the seven bit ASCII standard for all device addresses, commands and messages. The IEEE-488 standard has renamed and redefined certain ASCII codes to perform specific tasks on the interface and called it the "Multiline Interface Message: ISO-7 bit code representation". This code format convention separates the ASCII seven bit codes into two major command groups: primary command group and secondary command group.

The secondary command group is the binary range '1100000' (Hex 60) through '1111110' (Hex 7E), and is provided to allow device designers the ability to customize their device to respond with a desired operation upon receipt of a specific secondary command. These codes are totally device dependent and carry no system oriented designations.

The primary command group is the binary range '0000000' (Hex 00) through '1011111' (Hex 5F) and is composed of four major subsets: the addressed command group, the universal command group, the listen address group, and the talk address group. The primary command group provides ASCII seven bit codes which are reserved for explicit bus operations or device addressing and cannot be used for customized operations as was the secondary command group.

The first subset of the primary command group is the addressed command group. This group of commands, binary range '0000000' (Hex 00) through '0001111' (Hex 0F), are commands to which previously addressed devices must respond. Some examples of the addressed command group are:

Go To Local (GTL) - X'01' - The GTL command places a previously addressed device in the local mode, i.e., the device should now respond to his front panel controls instead of responding to the GPIB interface.

Selected Device Clear (SDC) - X'04' - The SDC command forces the previously addressed device to perform an internal reset. This command is very useful when a device is in a hung state.

Group Execute Trigger (GET) - X'08' - The GET command provides a syncronization command to the addressed devices to execute the instructions previously issued to the device. This command is very useful when test networks require multiple devices to take readings simultaneously.

The second subset of the primary command group is the universal command group. Unlike the addressed command group, all devices, addressed or not must respond to these commands. This command group, binary range '0010000' (Hex 10) through '0011111' (Hex 1F), represent specific operations on the GPIB interface, of which the following are examples:

Local Lock out (LLO) - X'11' - The LLO command forces all devices on the interface to ignor their front panel controls and to disable the return to local button found on most instruments.

Device Clear (DCL) - X'14' - The DCL command forces all devices to perform an internal reset. This command is useful when operations need to be retried due to errors or "hung" systems.

The third and fourth subsets of the primary command group are the listen address group and the talk address group respectively. The listen address group is the binary range '0100000' (Hex 20) through '0111111' (Hex 3F) and is the set of allowable listen addresses. Included in this subset is the GPIB Universal Unlisten Command (UNL) which forces devices previously configured as listeners to remove themselves from that state. Similarly , the talk address group is the binary range '1000000' (Hex 40) through '1011111' (Hex 5F) and is the set of allowable talk addresses. Included in this subset is the GPIB Universal Untalk Command (UNT) which forces a previously configured talker to remove himself from that state.

Actually, the listen address group and the talk address group have a point of commonality that is felt at the device hardware level. Since a device may have the capability of both talking and listening, two distinct addresses, one each for talker and listener, would prove repetitive. What the standard utilizes in this area is a five bit subaddress which is common to both a talk address and a listen address, therefore designating a unique talk-listen address for each subaddress. This subaddress is usually prewired at the factory or jumperable on the device. The two Most Significant Bits (MSB) of the GPIB address specify whether the address is a talk address or a listen address. A talk address has the MSB equal to '10' where the listen address has the MSB equal to '01'. For example:

> A voltmeter has a subaddress of '10101'. When the Most Significant Bits are for a talker ('10') the complete address is '1010101' (Hex 55) which is an ASCII 'U'. If the Most Significant Bits are for a listener ('01') the complete address is '0110101' (Hex 35) which is an ASCII '5'.

The Most Significant Bits of the device address are not jumpered or preset, as the controller of the interface issues talk and listen addresses determined upon the operation of the GPIB device network.

GPIB INTERFACE FUNCTIONS

The IEEE-48, 1978, describes all the capabilities of the GPIB as a set of ten major interface functions. Table 1 shows the allowable interface functions, the IEEE-488, 1978 function

TABLE 1

IEEE-488 ALLOWABLE INTERFACE FUNCTIONS

SOURCE HANDSHAKE (SH) -	The SH function provides a device with the capability to guarantee the proper transfer of multiline messages
ACCEPTOR HANDSHAKE (AH) -	The AH function provides a device with the capability to guarantee the proper reception of remote multiline messages
TALKER OR EXTENDED TALKER (T OR TE) -	The T function provides a device with the capability to send device dependent data over the interface to other devices. The T function which uses a two byte talk address is the TE function
LISTENER OR EXTENDED LISTENER (L OR LE) -	The L function provides a device with the capability to receive device dependent data over the interface from other devices. The L function which uses a two byte listen address is the LE function
SERVICE REQUEST (SR) -	The SR function provides a device with the capability to request service synchronously from the controller of the interface
REMOTE LOCAL (RL) -	The RL function provides a device with the capability to select between two sources of input information. This function indicates to the device that either input information from the front panel controls (Local) or input from the GPIB interface (Remote) is to be used
PARALLEL POLL (PP) -	The PP function provides a device with the capability to send a PPR message (Parallel Poll Status) to the controller without being addressed to talk

TABLE 1 - Continued

DEVICE CLEAR (DC) -	The DC function provides a device with the capability to be cleared (Initialized) either individually or as part of a group of devices
DEVICE TRIGGER (DT) -	The DT function provides a device with the capability to have its basic operation started either individually or as part of a group of devices
CONTROLLER (C) -	The C function provides a device with the capability to send device addresses, universal commands, and addressed commands to other devices over the interface. It also provides the capability to conduct parallel polls to determine which devices require service

symbol and the definition of that function. Devices that adhere to the standard do not have to incorporate all of the interface functions but may utilize only a subset of the capabilities. All devices, however, must use basic functions such as Source Handshake (SH) and Acceptor Handshake (AH) to transmit or receive information respectively. This assortment of selectable interface functions allows device designers to customize a device for a certain application and provides a wide range of device capabilities. Devices currently available range from listener only type display stations to complex interface controllers such as found in the Hewlett Packard Calculator product line. A partial list of the available GPIB device manufacturers and devices appears in Appendix A. Minicomputer manufacturers have recognized the market place value of the IEEE-488, 1978, interface and are providing GPIB input/output (I/O) attachments. The DEC PDP-11, Hewlett Packard's 6100 line and IBM's Series/1 are just a few of the minicomputors presently available with GPIB.

GPIB INTERFACE SIGNALS

The General Purpose Interface Bus signal interface is composed of sixteen active signals, six associated grounds, and a logic ground. The sixteen active signals can be divided into three subsets: management lines, handshake lines, and data lines (see figure 1).

The management subset of the sixteen active signals consists of five lines which provide the interface with the required control

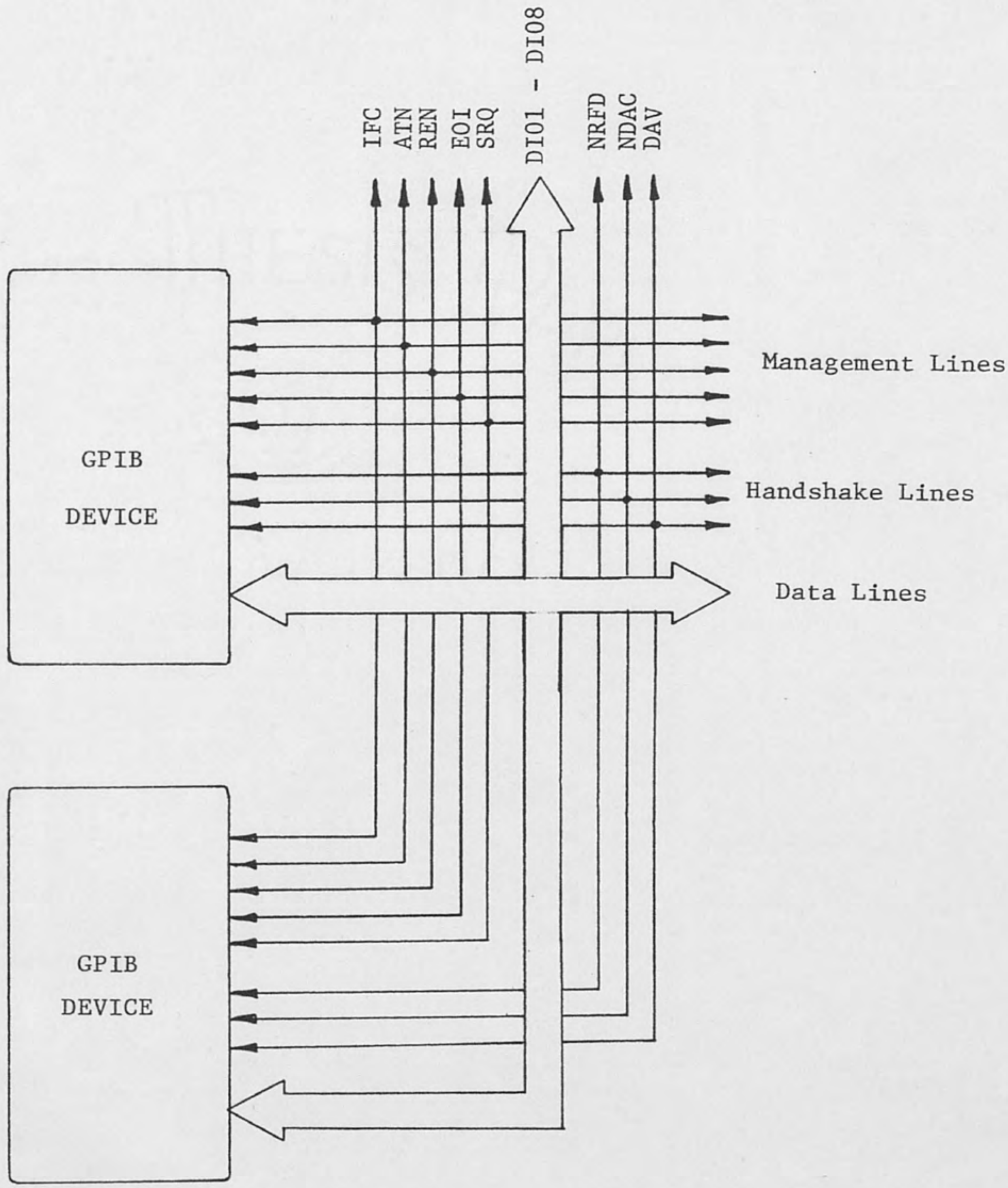


Fig. 1. General Purpose Interface Bus signals

for the orderly transfer of data and information. The five signals that compose the management subset are: interface clear, attention, remote enable, service request and end or identify. Interface clear, attention, and remote enable are always controlled by the specific device who governs the interface, herein known as the controller. End or identify (EOI) is activated only by a transmitting device whereas service request (SRQ) is activated only by the non-controller devices. Table 2 provides definitions for all management signals.

The second subset of the GPIB active signals is the handshake lines. These three lines form an asynchronous method of information transfer which is utilized for all transfers on the GPIB. Since the capability exists for multiple devices to cohabit the same interface, a 'Wire-Oring' of handshakes occurs which allows different speed devices to communicate, without data rate consequences, with the slowest device controlling the data transfer rate. Table 3 provides definitions of the three handshake lines. Figure 2 explains the handshake procedure and the timing relationship to the data lines.

The final subset of the sixteen active signal lines is the data lines. These eight bidirectional lines provide a byte wide path for data, address and information exchange and are always controlled by the device configured to transmit data on the interface. The data lines (DIO1-DIO8) are organized with DIO1 being the Most Significant Bit (MSB) and DIO8 being the Least Significant Bit (LSB).

TABLE 2

MANAGEMENT LINE DEFINITIONS

INTERFACE CLEAR (IFC) -	The IFC signal is a unidirectional line which provides the capability to asychronously put all devices on the bus in a known quiescent state. Devices must remove all signals from the interface and are no longer under the direct control of the GPIB.
ATTENTION (ATN) -	The ATN signal provides two main functions. The first priority is to attain the "Attention" of all devices on the interface. Upon receipt of an active attention line, all devices are forced into a receiving mode for universal commands and system addresses. The second function the ATN line performs is to designate whether the information on the data lines is commands, configuration messages or whether it is device dependent data. An active ATN line specifies configuration information, and an inactive ATN line specifies device oriented information.
REMOTE ENABLE (REM) -	The REM signal specifies that the GPIB interface is active and interaction on the bus is valid. A device upon receipt of an active REM line goes into a mode of operation in which he can receive GPIB commands and messages.
SERVICE REQUEST (SRQ) -	The SRQ signal is a device oriented signal that allows a device or instrument to request service on the interface.
END OR IDENTIFY (EOI) -	The EOI signal is used by any device that can transmit data on the GPIB to indicate the end of a data transfer. During the transmission of the last byte of data, the device activates the EOI line which specifies to the receiving devices that the transfer is being completed

TABLE 3

HANDSHAKE LINE DEFINITIONS

NOT READY FOR DATA (NRFD) -	THE NRFD line specifies a receiving device is not ready for the next byte of information. This signal is always controlled by the receiving device and is 'Wire-Ored' on the interface as multiple receiving devices may specify ready or not ready.
NOT DATA ACCEPTED (NDAC) -	The NDAC signal specifies that a receiving device has not accepted the byte on information currently on the interface. This line is always controlled by the device or devices receiving information on the interface as the signal is 'Wire-Ored' with NDAC signals from other receiving devices.
DATA VALID (DAV) -	The DAV signal is always controlled by the device transmitting data on the GPIB. When the DAV line is active, the information on the data lines must remain valid and unchanging.

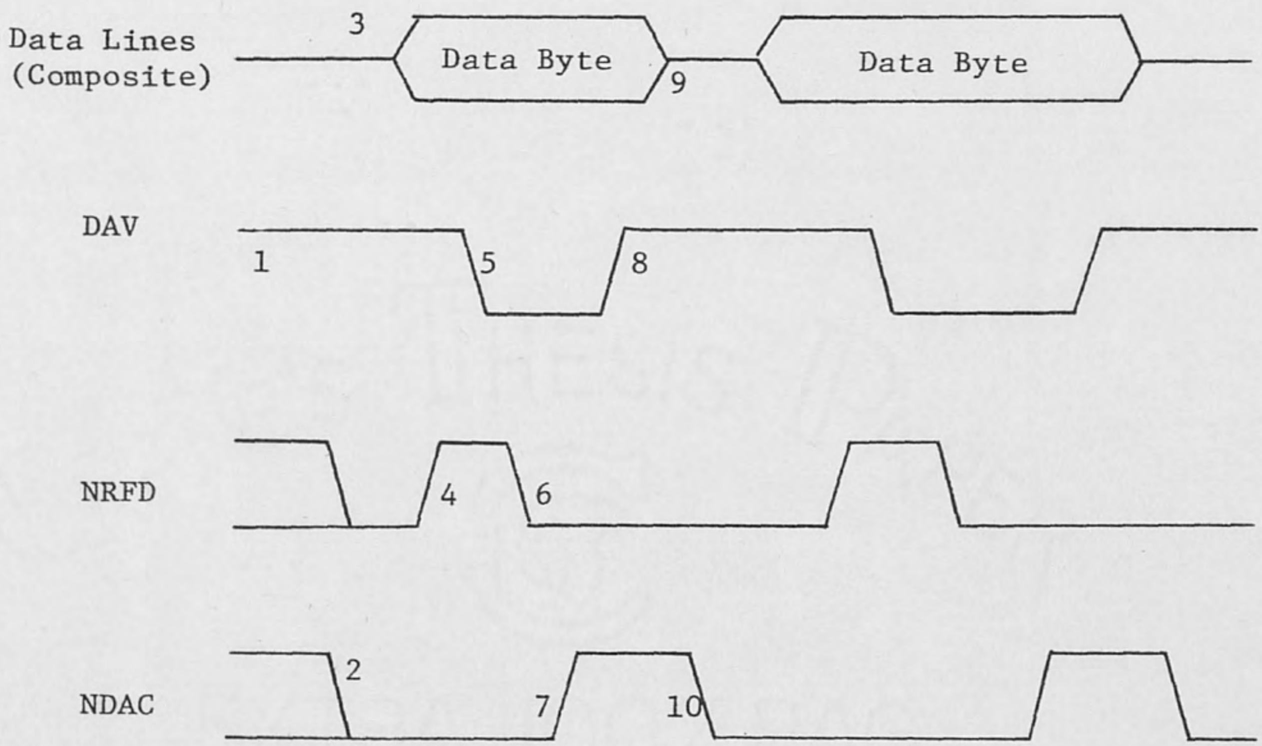


Fig. 2. GPIB handshake timings

Cabling for the General Purpose Interface Bus signals as specified by the IEEE-488, 1978, is provided in a 23 wire shielded cable that utilizes male and female twenty four pin trapezoidal connectors at each cable end. Figure 3 shows a typical male/female connector end and the connector contact assignments. This male/female connection scheme provides multiple device network configurations as the cables are stackable and provide star or linear device configurations (figure 4). GPIB cables are restricted to a maximum of four meters in length with the maximum cable distance in any configuration calculated by the following formula:

Maximum cable distance = 2 x the number of devices in the network

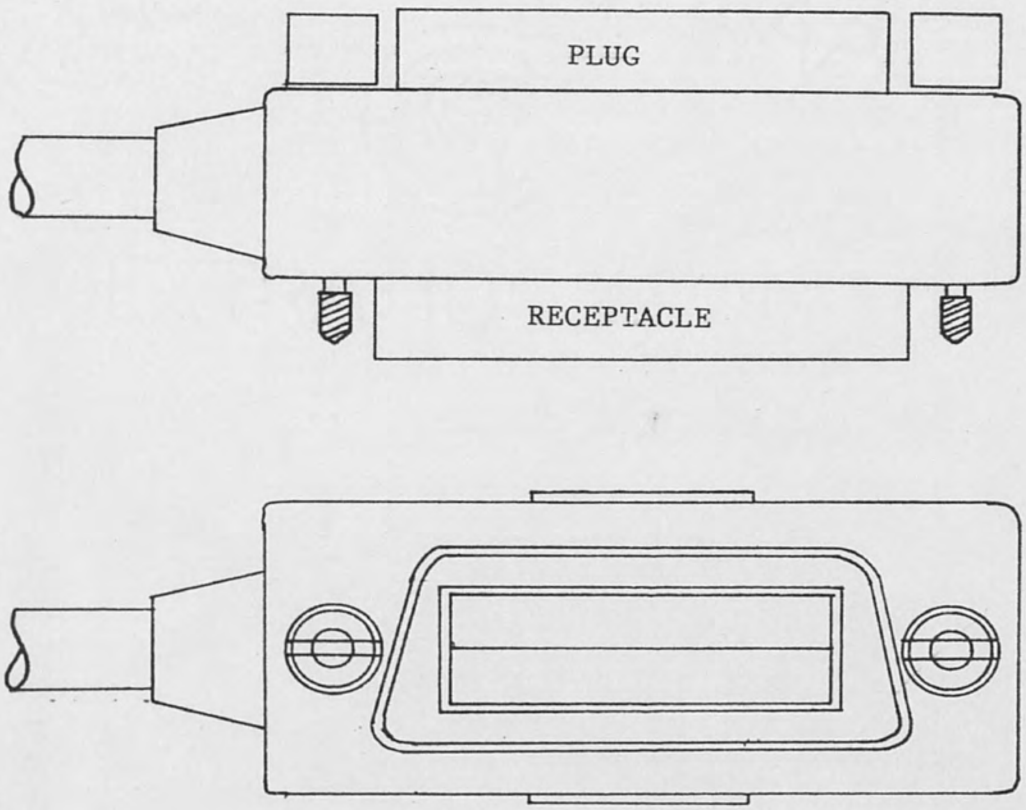
Thus, for example, if a voltmeter, a signal generator and a calculator were interconnected in a system, the maximum cable length in the network would be:

Maximum cable distance = 2 meters/device x 3 devices
= 6 meters

Therefore, the devices would be interconnected with a four meter and a two meter cable maximum.

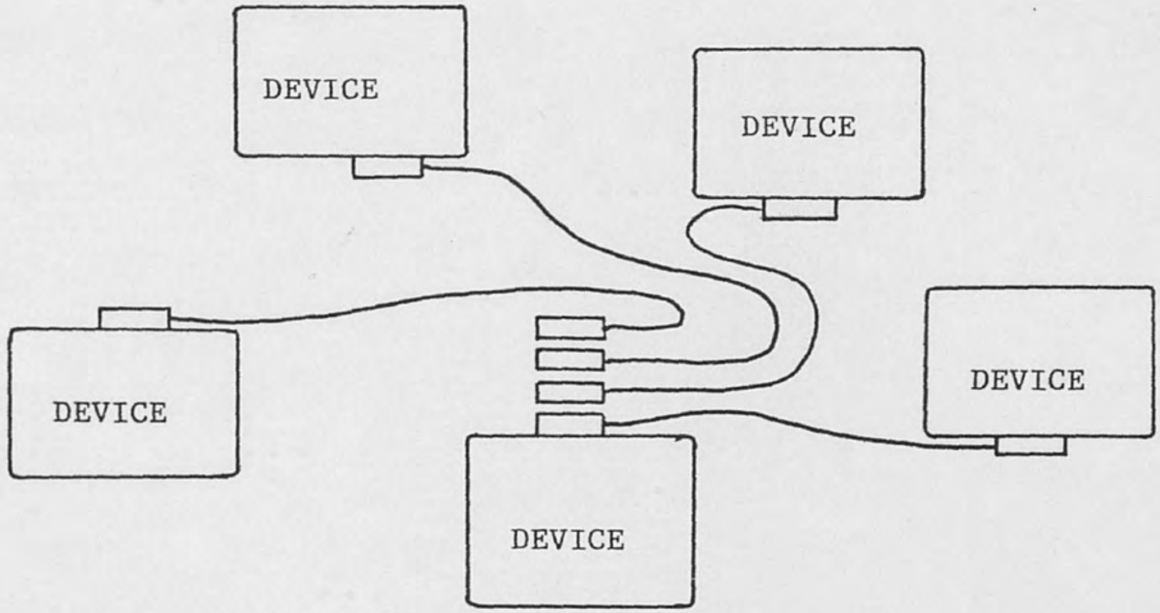
EXAMPLE GPIB TEST NETWORK

To provide a working overview of the GPIB interface, an example device network will be examined. This network is being implemented for an IBM marketing demonstration to be presented at the Instrumentation Society of American Convention in 1980. The demonstration network is a computer controlled low pass filter card test station which will automatically perform the required testing operations. The example station will be composed of a

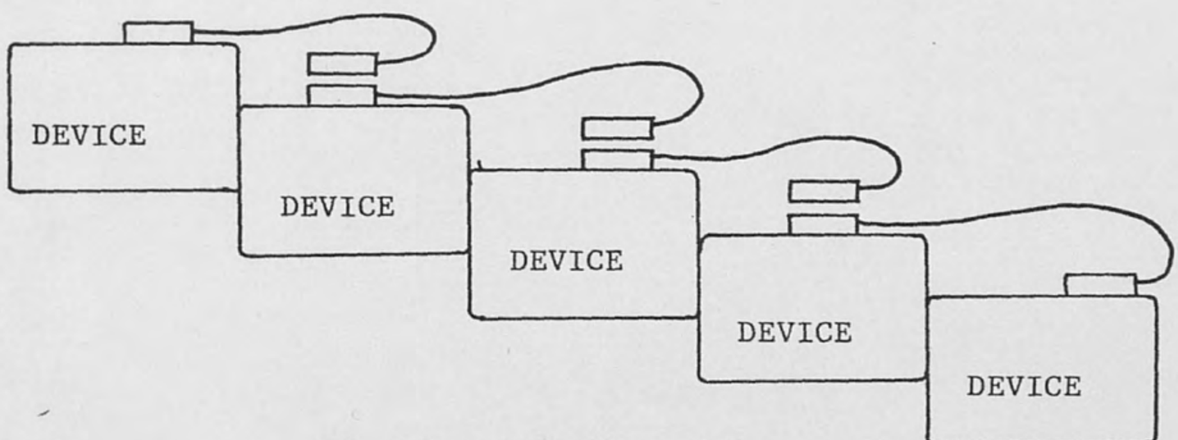


CONTACT	SIGNAL	CONTACT	SIGNAL
1	DIO1	13	DIO5
2	DIO2	14	DIO6
3	DIO3	15	DIO7
4	DIO4	16	DIO8
5	EOI	17	REN
6	DAV	18	GND(6)
7	NRFD	19	GND(7)
8	NDAC	20	GND(8)
9	IFC	21	GND(9)
10	SRQ	22	GND(10)
11	ATN	23	GND(11)
12	SHIELD	24	LOGIC GND

Fig. 3. GPIB cable connector



a) Star Configuration



b) Linear Configuration

Fig. 4. Example GPIB network configurations

minicomputer controller, such as the IBM Series/1 equipped with the General Purpose Interface Bus adapter, a system voltmeter, such as the Hewlett Packard HP905A, a frequency generator, such as the Fluke 6011A, a graphics plotter, such as the Tektronics 4662, and a custom low pass filter text fixture. Figure 5 shows the demonstration network configuration.

The overall filter test requirements are: (1) to incrementally stimulate the filter throughout it's frequency range, (2) to accurately monitor and record the filter response at each increment, (3) to compile and evaluate the test results and (4) to provide a graphic display of those results with an overall pass fail indication for that specific test. The operator then changes the filter card, replaces the plotter paper and repeats the test on the next filter.

Once the test system has been physically interconnected the next step is to provide the GPIB interface sequences that perform the testing operation:

1. The controller seizes authority of the interface (The controller performs an IFC operation)
2. The controller remotely enables all devices to respond to the GPIB interface commands (The controller performs a remote enable operation for addresses 1,2,3)
3. The controller waits for an indication from the operator that a filter card is installed on the custom test fixture
4. The controller assigns himself as a talker, and the frequency generator as a listener (Controller sends '?U1' as configuration data) Programming information for amplitude and frequency are then sent to the generator
5. The controller assigns himself as a talker, and the system voltmeter as a listener (Controller sends '?U2' as configuration information) Programming information on range, scale and triggering are sent to the voltmeter

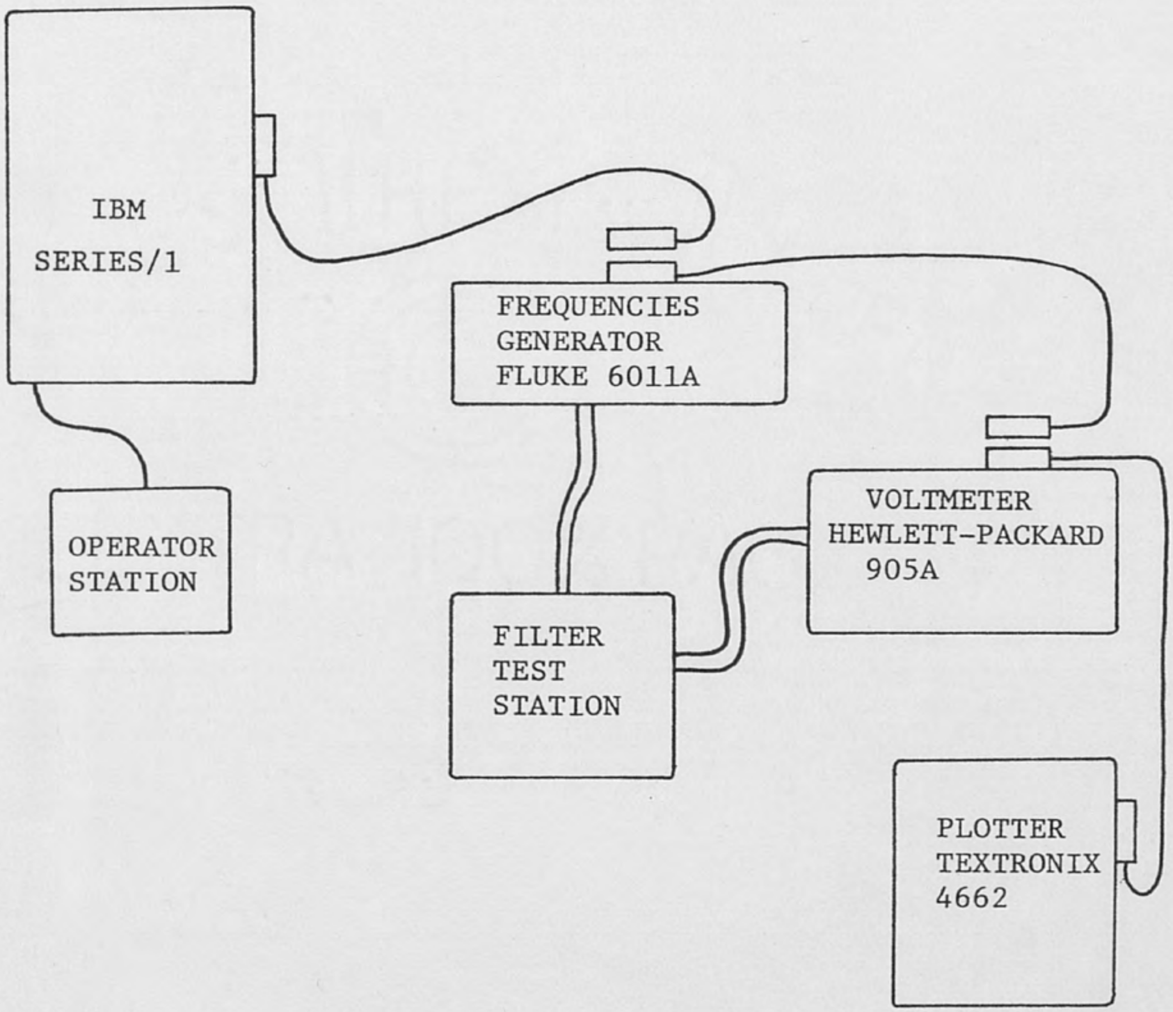


Fig. 5. GPIB demonstration network

6. The controller sends a trigger message to the voltmeter This message forces the voltmeter to take multiple readings to determine an RMS reading of the filter output

7. The controller assigns the voltmeter as a talker and himself as a listener and receives the RMS reading (Controller sends '?R5' as configuration information)

8. The controller stores the result, increments the frequency (If less than the max value for the test) and repeats steps #4 through #8 until all the test results have been taken and stored

9. The controller compiles the data for the plotter graph, compares the results to an acceptable group of results and prepares a pass/fail message to be printed on the plotter

10. The controller assigns himself to be a talker and the plotter to be a listener (Controller sends '?U3' as configuration information) Once assigned, information for the test results graph are sent to the plotter for display

11. The operator interprets the results, replaces the plotter paper, inserts a new card to test and starts the automatic test again (Return to step #3)

This example shows the ease and versatility of implementing a GPIB testing network. This ease of implementation can be extended to the custom device hardware design phase by incorporating one of the LSI GPIB modules that are currently available. Appendix B provides an LSI GPIB design example.

CONCLUSION

The increasing industry acceptance of the GPIB is shown with the growing number of manufactures that offer IEEE-488, 1978, options on their equipment. In addition, the technology industry is supporting the GPIB with specialized LSI modules that eliminate all custom GPIB interface hardware. This industry support, coupled with the growing need for instrument communication and functional versatility of the GPIB, provide solid evidence that the General Purpose Interface Bus is "the" interface for equipment interconnection.

APPENDIX A

CURRENT GENERAL PURPOSE INTERFACE BUS (GPIB)
USERS THAT HAVE APPEARED IN TRADE JOURNALS

CORPORATION	MODEL	DESCRIPTION
A.D. Data Systems	-----	Interface for Reed Relay Multiplexer
A.D. Data Systems	-----	Automatic Teet Equip. Switch. Matrix
Aiken Industries	DSM 44	Digital Multimeter ($1590)
Aiken Industries	DSM 52	Digital Multimeter ($1595)
Ailtech	7370	System Noise Monitor ($875)
AMS Inc.	703	Analog-Digital Interface
AMS Inc.	704	Analog-Digital Interface
AMS Inc.	810	GPIB/HPIB Interface*
AMS Inc.	801	Controller Mainframe
AMS Inc.	811	Serial ASCII Interface
AMS Inc.	812	Direct Connect Modem
AMS Inc.	820	High Speed digital Voltmeter
AMS Inc.	821	Inteprating Digital Voltmeter
AMS Inc.	830	8-Channel Voltage Multiplexer
AMS Inc.	840	24-Bit Digital Inputface
Analogic	AN5400	Minicomputer
Ballentine	5500B	118 MHz Universal Autoranging Timer
Ballentine	5600B	Universal Counter Timer
Booton Elecs.	76A	Automatic Capacitance Bridge
Booton Elecs.	82AD	AM/FM Modulation Meter
Calif. Instr. Co	DSM44	Digital Multimeter
Calif. Instr. Co	DSM52	Digital Multimeter
Calif. Instr. Co	830T-Ser.	Programmable Oscillators
Computer Automation	14676-01	IEEE Intelligent Cable
Comstron/Adret	7100	Programmable Signal Generator
Daltec Systems, Inc.	D1488	Digital Equipment Interface
Dana Labs Inc.	55GPIB	Interface/Translator For:
Dana Labs Inc.	5000	Digital Voltmeter
Dana Labs Inc.	5900	Digital Voltmeter
Dana Labs Inc.	6900	Digital Voltmeter
Dana Exact Elect.	605	Microprocessing Timer Counter
Data Precision	3400	4.5 Digit Multimeter
Data Precision	7500	5.5 Digit Systems Multimeter
Data Works	4880	Interface Bus Coupler
Decca Comm. Ltd.	3000	HF Communications Receiver
Digital Equipment	1EC11-A	PDP-11 Controller Interface
Digital Equipment	IBV-11	LSI-11 Computer Spstem Interface
Dranetz Engr. Labs.	305C/110	Phase Angle Meter

APPENDIX A - Continued

CORPORATION	MODEL	DESCRIPTION
Dylon Corp.	1015A-S	Magnetic Tape Recording System
EH Research Labs.	1501A	Programmable Pulse Generator
EH Research Labs.	1503A	Programmable Pulse Generator
Eldorado Instr. Co.	797	100 Picosecond Time Interval Meter
Eldorado Instr. Co.	989G	18-GHz Pulsed Microwave Counter
Eldorado Instr. Co.	988G	12.4-GHz Pulser Microwave Counter
Electro Scientific	296	Automatic LCR Meter
Electronic Devel.	501J	Programmable DC Voltage Standard
Electronic Devel.	Kit 488	IEEE Interface for all Programmable EDC Units
Elgar Corp.	-----	Programmable Oscillator
Exact	340	Material Testing Generator
Exact	600 Ser.	Programmable Function Generator
Exact	801	Frequency Synthesizer
Exact	802	Frequency Synthesizer
Fairchild Instr.	4880	Instrument Interface Coupler
Fairchild Instr.	1700	Dual Instr. Interface Coupler
Fluke Mfg. Co.	2204A	Scanner-100 Channels @ 125 Per Sec
Fluke Mfg. Co.	5100	Calibration Unit
Fluke Mfg. Co.	5101A	Calibration Unit
Fluke Mfg. Co.	6010A	Synthesized Signal Generator
Fluke Mfg. Co.	6011A	Signal Generator
Fluke Mfg. Co.	1953A	Counter
Fluke Mfg. Co.	8500A	Digital Voltmeter
Fluke Mfg. Co.	8502A	Digital Voltmeter
Fluke Mfg. Co.	8920A	True Digital RMS Voltmeter
Gen Rad	1658	RLC Digibridge
Gen Rad	1687	Megahertz LC Digibridge
Gen Rad	1688	Precision LC Digibridge
Gould	054100	Digital Storage Scopes
Grumman	AT160	Colorgraphics Terminal
Guideline	9575	Precision Digital Voltmeter
Guideline	9576	Precision Digital Voltmeter
Guideline	9577	Precision Digital Voltmeter
Hewlett-Packard Co.	(See Separate List Of Products)	
ILC Data Device	DBA-488	IEEE-488 Data Bus Adapter
Interface Technology	RST-432	Data and Timing Generator
Interface Technology	RST-648	Timing Simulator/Word Generator
Interface Technology	488	Bus Analyzer/Monitor for Debugging
Interstate Elect.	820	14 MHz Function Generator
Interstate Elect.	845	14 MHz Pulse/Function Generator
Interstate Elect.	860	20 MHz Pulse/Function Generator
Ithaco	4001	Programmable Filter
Keithley Instr. Inc.	7033	IEEE Scanner Mainframe Interface
Keithley Instr. Inc.	7802-ISB	System 1 (I/O Port)

APPENDIX A - Continued

CORPORATION	MODEL	DESCRIPTION
Keithley Instr. Inc.	160B	Digital Multimeter
Keithley Instr. Inc.	164	Digital Multimeter
Keithley Instr. Inc.	172	Digital Multimeter
Keithley Instr. Inc.	173	Digital Multimeter
Keithley Instr. Inc.	174	Digital Multimeter
Keithley Instr. Inc.	180	Digital Nanovoltmeter
Keithley Instr. Inc.	190	Digital Multimeter
Keithley Instr. Inc.	445	Digital Picoammeter
Keithley Instr. Inc.	616	Digital Electrometer
Kepco Inc.	SN-488	GPIB Power Supply Prog. Interface
Kinetic Systems	3388	Camac to GPIB Interface
Kinetic Systems	3388	GPIB to Camac Interface
Matrix Systems Corp.	-----	Audio/Coaxial Switching Systems
National Instr.	GPIB11-1	PDP-11 GPIB Interface
National Instr.	GPIB11V-1	LSI-11 GPIB Interface
National Instr.	GPIB-100	Bus Extender to 300 Meters
Nicolet Instr. Corp.	1180	Data Acquistion System
North Atlantic Ind.	8800	Angle Position Indicators
N.V. Philips	PM2467	Printer
N.V. Philips	PM2460	Scanner
N.V. Philips	PM2441	Digital Voltmeter
N.V. Philips	PM2527	Digital Voltmeter
N.V. Philips	PM6620	Timer/Counter
N.V. Philips	PM6650	Counter
Pacific Measurement	1018B	Peak Power Meter (100MHz-12.4GHz)
Paratronics Inc.	532	Intelligent Analyzer Tool
Polarad Electronics	632	Spectrum Analyzers 100KC to 2GHz
Polarad Electronics	630	Spectrum Analyzers 10MHz to 40GHz
Polarad Electronics	640	Spectrum Analyzers 10MHz to 40GHz
Polarad Electronics	631	Spectrum Analyzers 10MHz to 40GHz
Polarad Electronics	641	Spectrum Analyzers 10MHz to 40GHz
Process Dynamics	488	Flexible Disc System
Rockland Systems	FFT512/S15	Spectrum Analyzer
Rohde & Schwarz	PCL	Card Reader
Rohde & Schwarz	PCW	Code Converter
Rohde & Schwarz	SMPU	Radio Set Test Assembly
Schlumberger	2017	Universal Counter
Schlumberger	-----	R.F. Test Set
Schlumberger	2711	Universal Counter
Spectral Dynamics	SD345	Spectrum Analyzer
Systems Consultants	111	EIA RS-232C to GPIB Adapter
Systron-Donner	154-4	Pulse Generator
Systron-Donner	1600A	Series Microwave Synthesizer
Systron-Donner	1702	Signal Generator
Systron-Donner	3530	Instrument Controller (Programmable)

APPENDIX A - Continued

CORPORATION	MODEL	DESCRIPTION
Systron-Donner	DPSD-50	Programmable Power Supply (Dual)
Systron-Donner	6054B	Microwave Counter
Systron-Donner	7115	Digital Multimeter
Systron-Donner	7244	Digital Multimeter 4.5 Digits
Systron-Donner	7344	Thin Digital Multimeter 4.5 Digits
Tektronix	4051	Graphic Computing System
Tektronix	4924	Magnetic Tape Unit
Tektronix	4662	Digital Plotter
Tektronix	DF2	Scope Plug in for Bus Debugging
TRW	System IV	ATE System
Wang	2254	Computor (2200) Based Controller
Wavetek	152	Function Generator
Wavetek	158	Waveform Generator
Wavetek	159	Waveform Generator
Wavetek	172	Programmable Signal Source
Wavetek	175	Prog. Arbitrary Waveform Generator
Wavetek	3002	520 MHz Waveform Generator
Vector Assoc. Inc.	1625	Logic Analyzer
Ziatech Corp.	ZT 80	INTEL SBC 80 Computer Interface
Ziatech Corp.	ZT 488	Bus Analyzer for Debuggingface

Hewlett-Packard Products

3320B	13 MHz Frequency Synthesizer	Option 007
3325A	1UHz to 21 MHz sunction synthesizer/Function Generator	
3330B	13 MHz Automatic Synthesizer/Sweeper	
3335A	200Hz to 80 MHz Synthesizer/Level Generator	
6002A	DC Power Supply; 200w	Option 001
8016A	9 x 32 Bit Word Generator	Option 001
8160A	Pulse Generator--50MHz range	
8165A	High Speed Waveform Generator	
8170A	Programmable Data Generator	
8507A	Network Analyzer System	
8580B	Automated Spectrum Analyzer (Port)	
8620C	Sweep Oscillator	Option 011
8660A	Synthesized Signal Generator	Option 005
8660C	Synthesized Signal Generator	Option 005
8662A	Synthesized Signal Generator	Option 005
8671A	Microwave Frequency Synthesizer	
8672A	Synthesized Signal Generator	
9500D	Autoratic Test System (Port)	
59308A	Timing Generator	
59501A	Power Supply Programmer: Isolated D4A Converter	
436A	Power Meter	
1600A	Logic Analyzer	

CORPORATION	MODEL	DESCRIPTION
	3050B	Data Acquisition System
	3042A	Network Analyzer System
	3044A	Spectrum Analyzer System
	3045A	Spectrum Analyzer System
	3437A	High Speed System Digital Voltmeter
	3455A	Digital Voltmeter, Auto Calibration
	3490A	Digital Voltmeter, Self Test
	3495A	40 Channel Scanner
	3571A	Tracking Spectrum Analyzer
	3582A	Low Cost Spectrum Analyzer
	3745A	Selective Level Measuring Set: CCITT FDM Systems
	3745B	Selective Level Measuring set: Bell FDM Systems
	4261A	Digital LCR Meter
	4262A	Digital LCR Meter (New)
	4270A	Automatic Capacitance Bridge
	4271A	1 MHz Digital LCR Meter
	4272A	1 MHz Preset C Meter
	4282A	Digital High Capacitance Meter
	4942A	Transmission Impaired Measurement System (TIMS)
	5312A	HP-IB Interface (Talker) for 5300B Systems
	5328A	Universal Counter
	5340A	Automatic Microwave Counter
	5341A	High Speed Automatic Microwave Counter
	5345A	General Purpose Plug-In Counter
	5353A	Frequency Counters, Channel Plug-In
	5354A	Converter Plug-In
	5363A	Time Interval Probes
	5381A	80 MHz Counter
	5390A	Frequency-Stability Analyzer
	5501A	Laser Transducer; for Accurate Positioning
	8503A	S-Parameter Test Set
	8505A	RF Network Analyzer
	8901A	Modulation Analyzer
	59303A	Digital to Analog Converter
	59306A	Relay Actuator; for Programmable Switches
	59307A	VHF Switch
	59309A	Digital Clock
	59313A	Analog to Digital Converter
	59500A	Multiprogrammer Interface Kit: For 6940B/6941B
	2631	High Performance Printer
	2635	High Performance Printer/Keyboard
	5150A	Alphanumeric Thermal Printer; 20 Columns
	59304A	Numeric Display, 12 LED Displays
	7225A	Graphics Plotter
	9871A	Character-Impact Printer, 132 Columns

APPENDIX A - Continued

CORPORATION	MODEL	DESCRIPTION
9872A		Plotter
3964A		Instrumentation Tape Recorder: 4 Channel
8968A		Instrumentation Tape Recorder: 8 Channel
3070A		Data Intry Terminal
59301A		ASCII-to-Parallel Converter
59403A		HP-IB/Common Carrier Interface: RS232C or CCITT V24
DTS70		Digital Test System (Port)
59301A		Interface for 21Mx & 2100 Computers
59405A		Interface for 9820A Calculator
59405A		Interface for 9821A Calculator
59405A		Interface for 9830A/B Calculator
9803A		Interface for 9825A Calculator
98135A		Interface for 9815A Calculator
10631A		HP-IB Interconnection Cable: 1M (3.3 Ft)
10631B		HP-IB Interconnection Cable: 2M (6.6 Ft)
10631C		HP-IB Interconnection Cable: 4M (13.2 Ft)
59401A		Bus System Analyzer
Miscellaneous Products with GPIB Compatability		
AMP Connectors		Connector Kit for IEEE-488 Connector
Motorola		MC68488 IEEE Interface to 6800 Chip
INTEL		8291 IEEE Talker/Listener Chip
INTEL		8292 IEEE Controller Chip

APPENDIX B

IEEE-488 DESIGN EXAMPLE

The IEEE-488 standard for system interconnection has been widely accepted by the instrumentation industry. In addition, the companies that design and manufacture Large Scale Integration (LSI) modules have incorporated the IEEE-488, 1978, interface requirements into specialized designs which all but eliminate hardware requirements for custom projects. These LSI modules provide off-the-shelf GPIB interfaces that only require minimal software programming support for IEEE-488, 1978, compatibility. The following section provides a design example that demonstrates the ease of interconnection for a custom design to the General Purpose Interface Bus.

In many testing environments the need arises for automated testing methods. These requirements range from complicated system test networks that require multiple test stations to simplistic bench type test applications that require only hardcopy output for measurements. This design example will deal with a minor application which requires measurements taken by a digital voltmeter with a GPIB interface option to be automatically transferred to an output station for display. Therefore, the design is to implement an IEEE-488 interface for the output station.

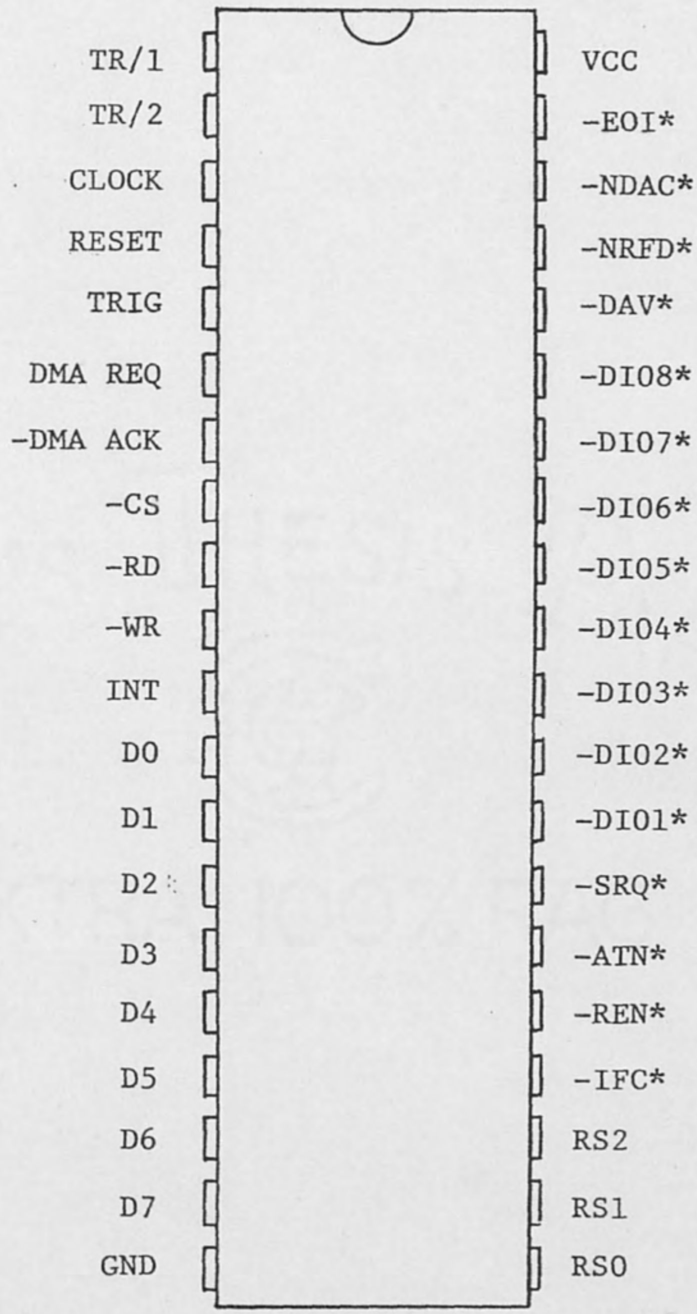
The output station selected was a keyboard display unit which operates on the CRT serial interface, a common efficient interface used throughout the industry. The design approach was then to specify a vendor microprocessor which could easily control both the IEEE-488 interface and the CRT interface. A state of the art microprocessor which could satisfy these requirements is the INTEL 8085. Furthermore the INTEL 8085 microprocessor is available in an engineering design kit, which provides both monitor interfaces and monitor software for the CRT interface. This monitor function allows reading from memory, writing to memory and microprocessor interrogation. Selection of the INTEL 8085 design kit provided both a working microprocessor system and the interface and software support for the CRT monitor. This selection provided a basic system on which to install the IEEE-488, 1978, interface hardware, and write the software (microcode) support for the LSI GPIB module to complete the design.

The design example will be investigated in three sections: (1) a basic overview of the 8085 design kit, (2) a brief overview of the INTEL 8291 GPIB module and (3) a review of the microcode used to initialize and control the 8291. Additional specifications and information on the INTEL design kit or the INTEL 8291 module is available from the manufacturer.

The INTEL MCS-85 design kit (SDK-85) is a complete, single board microprocessor system in kit form. The kit contains all required hardware, light emitting diode (LED) displays, input keyboard, required discrete components, random access memory (RAM), a display (CRT) interface, and a system software monitor, to construct a functioning 8085 microprocessor system. The kit provides room for expansion memory and I/O modules and is an exceptional kit for investigative designs.

The INTEL 8291 GPIB talker/listener chip is a 40 pin Large Scale Integration (LSI) module that provides the conversion between the INTEL 8085 microprocessor bus and the IEEE-488, 1978, interface. Figure 6 shows the pin configuration for the 8291 module. The microprocessor controls the 8291 with normal I/O commands which governs the initialization and capabilities of the module. All GPIB related protocol functions and interface requirements are automatically handled by the 8291, providing those capabilities have been enabled by the 8085 microprocessor. The 8291 provides all device addressing, device clearing, GPIB status polling sequences, handshaking and device oriented commands automatically. Interrupt posting capability, 8085 status reporting and Direct Memory Access (DMA) are also provided to the microprocessor system.

The microcode for the design example will be approached in two parts: CRT interface and GPIB interface. The CRT interface microcode required very little modification as extensive capabilities are in the SDK-85 system monitor. The system monitor provides microcode that handled all timings and constraints for the CRT interface and could be referenced from the GPIB microcode routines. The GPIB Microcode is sectioned into initialization code and interrupt handling code. The source listing for these sections can be found in appendix C. The initialization code prepares the 8291 for interrupting, handshake delay times, device addresses, primary and secondary addresses, and listener or talker only capability. In reference to the source listing in appendix C, the initialization code:



*GPIB Interface Lines

Fig. 6. INTEL 8291 GPIB module

1. Resets the chip (lines 11,12)
2. Sets the interrupt mask to interrupt when a byte is received (lines 13,14)
3. Zeros out all secondary mask interrupts (lines 15,16)
4. Sets up the primary address as ASCII 4 (lines 17,18)
5. Disables the secondary address (lines 19,20)
6. Assigns the 8291 RO respond to GPIB addressing (lines 21,22)
7. Clears out auxiliary masks A and B (lines 23,24,25,26)
8. Sets the handshake value for open collector drivers (lines 27,28)
9. And issues a power on command to enable the 8291 module (lines 29,30)

The remainder of the initialization microcode prints a message to the output device to indicate the 8291 has been properly initialized (lines 31-50).

The interrupt routine is accessed automatically whenever the 8291 posts an interrupt to the 8085 microprocessor. The interrupt handler accesses the byte just received from the GPIB interface by the 8291, checks for a character terminator (Hex 0A) and calls the monitor teletype routines to print the character on the output device. Upon successful display of the character, the interrupt routine enables the 8291 module to interrupt the 8085 processor when the next byte is received and goes to a halt condition to wait for that interrupt. When a terminator (Hex 0A) is received, a subroutine to force a carriage return/line feed command to be sent to the displays output station. This vertical spacing occurs between each message received and provides the operator with a cleaner display. After the carriage return/line feed command has been successfully completed, the interrupt routine enables the

8291 to interrupt and waits for the next byte received.

This GPIB design, simplistic in nature, demonstrates the ease of design and interconnection of the General Purpose Interface Bus. The LSI modules such as the INTEL 8291 provide a superior range of capabilities for the GPIB interface which the designer or system integrater can utilize.

APPENDIX C

INTEL 8085 6PIB MICROCODE EXAMPLE

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ISIS-II 8080/8085 MACRO ASSEMBLER, V3.0        MODULE   PAGE    1

  LOC  OBJ        LINE        SOURCE STATEMENT

                    ; THE FOLLOWING ROUTINE IS WRITTEN TO INITIALIZE AND CONTROL THE FLOW OF
                    ; DATA FROM THE INTEL 8291 GPIB CHIP.  THIS PRELIMINARY ROUTINE WILL NOT
                    ; USE A DMA AND THE ADDRESS OF THE GPIB CHIP IS X'A0'.  THE ROUTINE IS
                    ; DESIGNED TO RECIEVE BYTES OF INFORMATION FROM THE GPIB INTERFACE AND OUTPUT
                    ; THEM TO THE MONITOR DEVICE ON THE SYSTEM (IN THIS CASE A 4800 BAUD TTY).
05C4                CO      EQU    05C4H       ;DEFINE CO TTY OUTPUT ROUTINE
05EB                CROUT   EQU    05EBH       ;DEFINE CROUT TTY OUTPUT ROUTINE
8800                GPORG0  SET    8800H       ;DEFINE GPIB ORG ORIGIN
8800                        ORG    GPORG0      ;DEFINE GPIB ORIGIN
8800 31C220         GPIB:   LXI    SP,20C2H    ;INITIALIZATION POINTER FOR STACK
8803 3E02                   MVI    A,02H       ;RESET FOR GPIB CHIP
8805 D3AD                   OUT    0ADH        ;OUT INSTRUCTION FOR CHIP RESET
8807 3E11                   MVI    A,11H       ;SET UP INTERRUPT MASK 1 FOR GPIB
8809 D3A9                   OUT    0A9H        ;OUT INSTR. FOR MASK1
880B 3E00                   MVI    A,0CH       ;SET UP INTERRUPT MASK 2 FOR GPIB
880D D3AA                   OUT    0AAH        ;OUT INSTR. FOR MASK
880F 3E00                   MVI    A,C0H       ;SET UP PRIMARY GPIB ADDRESS AS ASCII 4
8811 D3AE                   OUT    0AEH        ;OUT INSTR. FOR PRIMARY ADDRESS
8813 3E80                   MVI    A,80H       ;DISABLE SECONDARY ADDRESS IN CHIP
8815 D3AE                   OUT    0AEH        ;OUT INSTR. FOR SECONDARY ADDRESS
8817 3E40                   MVI    A,40H       ;SET UP ADDRESSING MODE FOR GPIB CHIP
8819 D3AC                   OUT    0ACH        ;OUT INSTR. FOR ADDRESSING MODE
881B 3E80                   MVI    A,80H       ;CLEAR OUT AUXILLARY MASK A
881D D3AD                   OUT    0ADH        ;OUT INSTR. FOR AUX. MASK A
881F 3EA0                   MVI    A,0A0H      ;CLEAR OUT AUXILLARY MASK B
8821 D3AD                   OUT    0ADH        ;OUT INSTR. FOR AUX. MASK B
8823 3E23                   MVI    A,23H       ;SET UP TIMER SYNC FOR OPEN COLLECTOR DRIVERS
8825 D3AD                   OUT    0ADH        ;OUT INSTR. FOR TIMER SYNC
8827 3E00                   MVI    A,00H       ;SET UP POWER ON COMMAND(PON)
8829 D3AD                   OUT    0ADH        ;SEND POWER ON COMMAND (PON) TO GPIB CHIP
882B 3EC3                   MVI    A,0C3H      ;SET UP JUMP INSTRUCTION IN ACCUMULATOR
882D 32CE20                 STA    20CEH       ;STORE AT LOCATION FOR GPIB INTERRUPT
8830 3E00                   MVI    A,00H       ;SET UP LSB OF INTERRUPT ROUTINE
8832 32CF20                 STA    20CFH       ;STORE AT LOCATION IN INTERRUPT TABLE
8835 3E89                   MVI    A,89H       ;SET UP MSB OF INTERRUPT ROUTINE
8837 32D020                 STA    20D0H       ;STORE AT LOCATION IN INTERRUPT TABLE
883A 0600                   MVI    B,00H       ;CLEAR OUT B REGISTER
883C CDEB05                 CALL   CROUT       ;CALL ROUTINE FOR CR-LF
883F CDEB05                 CALL   CROUT       ;CALL ROUTINE FOR CR-LF
8842 0E47                   MVI    C,47H       ;MOVE ASCII G INTO C REGISTER
8844 CDC405                 CALL   CO          ;CALL OUTPUT ROUTINE FOR TTY
8847 0E50                   MVI    C,50H       ;MOVE ASCII P INTO C REGISTER
8849 CDC405                 CALL   CO          ;CALL OUTPUT ROUTINE FOR TTY
884C 0E49                   MVI    C,49H       ;MOVE ASCII I INTO C REGISTER
884E CDC405                 CALL   CO          ;CALL OUTPUT ROUTINE FOR TTY
8851 0E42                   MVI    C,42H       ;MOVE ASCII B INTO C REGISTER
8853 CDC405                 CALL   CO          ;CALL OUTPUT ROUTINE FOR TTY
8856 3E18           GPSIM1: MVI    A,18H       ;SET INTERRUPT MASK FOR INT6.5
8858 30                     SIM                ;SET INTERRUPT MASK
8859 C31289                 JMP    GPEND       ;GO TO END OF OUTPUT ROUTINE
8900                GPORG1  SET    8900H       ;SET NEXT GPIB ORG STATEMENT
8900                        ORG    GPORG1      ;DEFINE GPIB ORG STATEMENTY
8900 31C220         GPINTR: LXI    SP,20C2H    ;SET STACK POINTER FOR INTERRUPT
8903 DBA8                   IN     0A8H        ;INPUT BYTE FROM GPIB CHIP
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APPENDIX C - Continued

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ISIS-II 8080/8085 MACRO ASSEMBLER, V3.0        MODULE   PAGE    2

  LOC  OBJ        LINE        SOURCE STATEMENT

  8905 FE0A          55 GPTERM: CPI    0AH            ;CHECK FOR MESSAGE TERMINATOR
  8907 CA1289        56         JZ     GPEND          ;IF TERMINATOR, GO TO END OF ROUTINE
  890A 4F            57         MOV    C,A            ;MOVE NEW BYTE FROM A TO C REGS
  890B CDC405        58         CALL   CO             ;CALL ROUTINE FOR TTY OUTPUT
  890E DBA9          59 GPCOMP: IN     0A9H           ;ENABLE CHIP FOR NEXT BYTE OF DATA
  8910 FB            60         EI                    ;ENABLE NEXT INTERRUPT
  8911 76            61         HLT                   ;WAIT FOR NEXT INTERRUPT
  8912 CDEB05        62 GPEND:  CALL   CROUT          ;CALL ROUTINE FOR CR-LF
  8915 CDEB05        63         CALL   CROUT          ;CALL ROUTINE FOR CR-LF
  8918 C30E89        64         JMP    GPCOMP         ;GO TO ROUTINE ENDING
                     65         END                   ;END STATEMENT

PUBLIC SYMBOLS

EXTERNAL SYMBOLS

USER SYMBOLS
CO     A 05C4   CROUT  A 05EB   GPCOMP A 890E   GPEND  A 8912   GPIB   A 8800   GPINTR A 8900   GPORG0 A 8800
GPORG1 A 8900   GPSIM1 A 8856   GPTERM A 8905

ASSEMBLY COMPLETE,   NO ERRORS
```

ASM80 :F1:GPIB.1 MOD85

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