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Development of a DME Simulator

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DEVELOPMENT OF A DME SIMULATOR

BY

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ABSTRACT

This report summarizes the design of a DME (Distance Measuring Equipment) simulator to be used in the testing of an Area Navigation System.

The purpose of the simulator is to generate a signal representing an aircraft's distance from a ground station. This information is in the form of two pulses whose separation represents the elapsed transmission time for an aircraft to receive a reply from the ground station to an interrogation by the aircraft.

The pulse spacing must be selectable as fixed distances for static tests and as distance changing at a constant rate to simulate flying to or from the station for dynamic testing.

Thumbwheel switches are used to input fixed distances and up/down counters provide inbound and outbound range rates. The rate clock is derived from a crystal oscillator whose output is divided down by a programmable, modulo-n, divider to the desired rate/frequency.

This input distance information, available in parallel binary coded decimal format, is then converted to the required pulse pair spacing. This is accomplished with presettable down counters clocked by another crystal oscillator whose frequency represents two-way propagation time for radio waves.

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1.0 PROBLEM DEFINITION

This report describes the development of a bench test set to be used in the design and testing of a new Area Navigation system for general aviation aircraft. An Area Navigation (RNAV) system is a station-oriented navigation system whose primary position determining data sources are VOR bearing and DME distance relative to a selected ground facility.

VOR is an abbreviated term for Very high frequency Omnidirectional Range. A ground station transmits reference (magnetic north) and variable (bearing) phase information as a VHF composite NAV signal. An airborne receiver then interprets this data to determine the aircraft's magnetic bearing from the station providing conventional, along-radial, navigation capability.

A DME (distance measuring equipment) is an airborne pulsed interrogator-transponder system operating in the 960-1215 MHz band. Interrogations from an aircraft are answered by a bround transponder, and the elapsed time between interrogation and reply is converted, in the aircraft, to a reading of distance between aircraft and the ground transponder.

An auxillary output of the DME, analog distance, is a pulse pair representing the calculated distance

for use in RNAV equipment. It is the purpose of this test set to simulate this DME input to an Area Navigation system.

1.1 AREA NAVIGATION

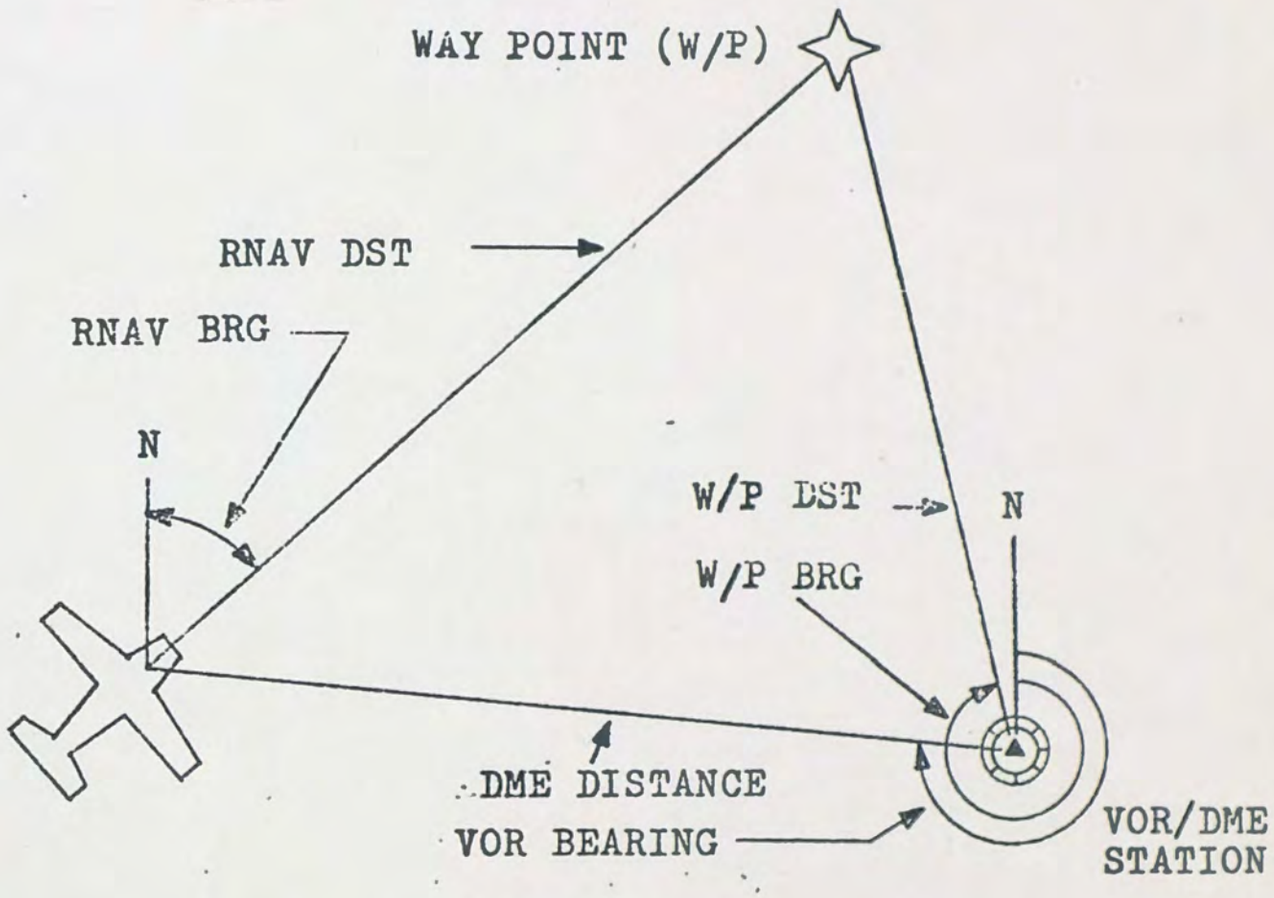
Conventional, VOR/DME, NAV systems provide guidance along routes or airways that lead directly to or from the VOR/DME ground station. This creates a convergence or funneling effect of air traffic over each VOR/DME station that limits the traffic volume, as well as the number of airways available between departure and arrival points.

An Area Navigation system is defined as one that permits navigation along a predefined course to a specified destination, but does not necessitate flying directly toward, or away from, a ground-based VOR/DME navigational aid. When operated within the service volume of a co-located VOR/DME ground station, this system provides position information relative to any specified location defined as a way point. This way point, sometimes refered to as a phantom station, is arbitrary and is defined in terms of bearing and distance from the reference ground facility. Area Navigation is accomplished by continuously solving the horizontal navigation triangle as shown in Figure 1.

The triangle is solved by vector addition to give the bearing (BRG) and distance (DST) from the aircraft to the

waypoint (W/P).

RNAV DST $\angle$RNAV BRG = W/P DST $\angle$W/P BRG - DME $\angle$VOR



Area Navigation Triangle

Figure 1

1.2 RANGE, RATE AND ACCURACY REQUIREMENTS

The distance measuring equipment which will be interfaced with the RNAV varies from relatively simple, low power, units with limited range and accuracy to the more sophisticated, longer range boxes used by commercial aviation. The former are normally refered to as GA (General Aviation) units. The latter are called ARINC units and are designed to meet the requirements

of ARINC characteristics. The latest being No. 568 for MARK III Airborne Distance Measuring Equipment.

Aeronautical Radio, Inc. (ARINC) is a corporation in which the United States scheduled airlines are the principal stockholders. A major activity of the corporation is the formulation of standards for electronic equipment and systems for the airlines and establishment of equipment characteristics. These ARINC Characteristics serve the two-fold purpose of channeling new equipment designs in a direction resulting in maximum standardization and interchangeability and specifying technical requirements the equipment must meet. ARINC Characteristic No. 568 will be used as a guide in the design of the DME Simulator.

The range requirement is that the equipment should provide at least 300 nautical mile range. As the readout on the RNAV system is resolved down to 0.1 nm, the static distance input was chosen to be four decades of thumbwheel switches with the least significant digit representing 0.1 nm increments.

Maximum airspeeds of the type aircraft expected to carry the RNAV are in the 600 KT category. Including consideration of possible tail winds, this dictates a range rate capability on the order of 800 KTS. As the RNAV also calculates ground speed and time-to-station,

a further consideration is that incremental speeds should be easily handled in distance/time computations. Since time-to-station is read out in minutes, the logical choice is increments of 60 KTS so that the simulator flies at rates of 1, 2, 3, etc. nautical miles per minute and conversions between distance, time and speed are simplified. The selectable rates were therefore chosen to be 0 KTS to 840 KTS inbound or outbound in increments of 60 KTS. In order to provide a smoothly transitioning appearance of the distance data to the RNAV, the distance output is to be updated in .01 nm increments for all rates.

ARINC Characteristic No. 568 specifies an accuracy of $\pm$0.2 nm for distance computation with an additional error of $\pm$0.1 nm permitted in conversion to analog pulse pair output. However, in the interest of keeping input errors to the RNAV system to a minimum during testing, an arbitrary limit of $\pm$0.1 nm maximum error is chosen as a design goal for fixed distances. Ground speed is calculated and displayed by the RNAV system in one knot increments. It is therefore desirable that the rate error be less than one knot at all speeds. With a maximum rate of 840 KTS, this leads to an accuracy goal of less than 0.1% error in range rate.

2.0 PRELIMINARY CONSIDERATIONS

Prior to the actual design several factors must be considered which will, to a large extent, determine the method of system implementation. These include control and display requirements, component availability and cost and component/system compatibility. This section discusses the basis for selecting the various components used and describes the output pulse pair in detail, setting the requirements for system timing and circuit device speed.

2.1 CONTROL AND DISPLAY REQUIREMENTS

As described in section 1.2, fixed distances are to be selectable in increments of 0.1 nm from 0.0 to at least 300.0 nm, preferably in normal decimal format. The desired inbound and outbound rates are from 0 to 840 KTS in increments of 60 KTS with the output distance updated every .01 nm. The actual output DME distance, whether from the fixed distance selector or the rate controlled range circuitry, is to be displayed with some type of readout device. Since the distance is updated in .01 nm steps when "flying" inbound or outbound, the readout should indicate distance with .01 nm resolution. The system should have the capability to begin inbound or outbound travel at any designated fixed distance, switch from inbound to outbound, or vice-versa, as desired and automatically switch from inbound to outbound at 0.0 nm

distance.

2.2 COMPONENT SELECTION

Thumbwheel switches were chosen as the means of inputing fixed distances for several reasons. They provide an easy means of selecting discrete distances in the standard 100's, 10's, 1's and 0,1's decimal format, are inexpensive and are readily available. Also, having BCD outputs, they are easily interfaced with digital systems.

A rotary selector switch was used for rate inputs because of the relatively small number of discrete steps required. With one position for fixed inputs from the thumbwheels and 60 KT increments from 0 to 840 KTS, 16 positions would be required. Since a 10 position switch was available and the 60 KT resolution is not necessary at high speeds, it was decided that the rotary switch select speeds up to 420 KTS, requiring only 9 positions, and be used in conjunction with a X1-X2 multiplier, selected by a 2 position toggle switch, to achieve speeds to 840 KTS.

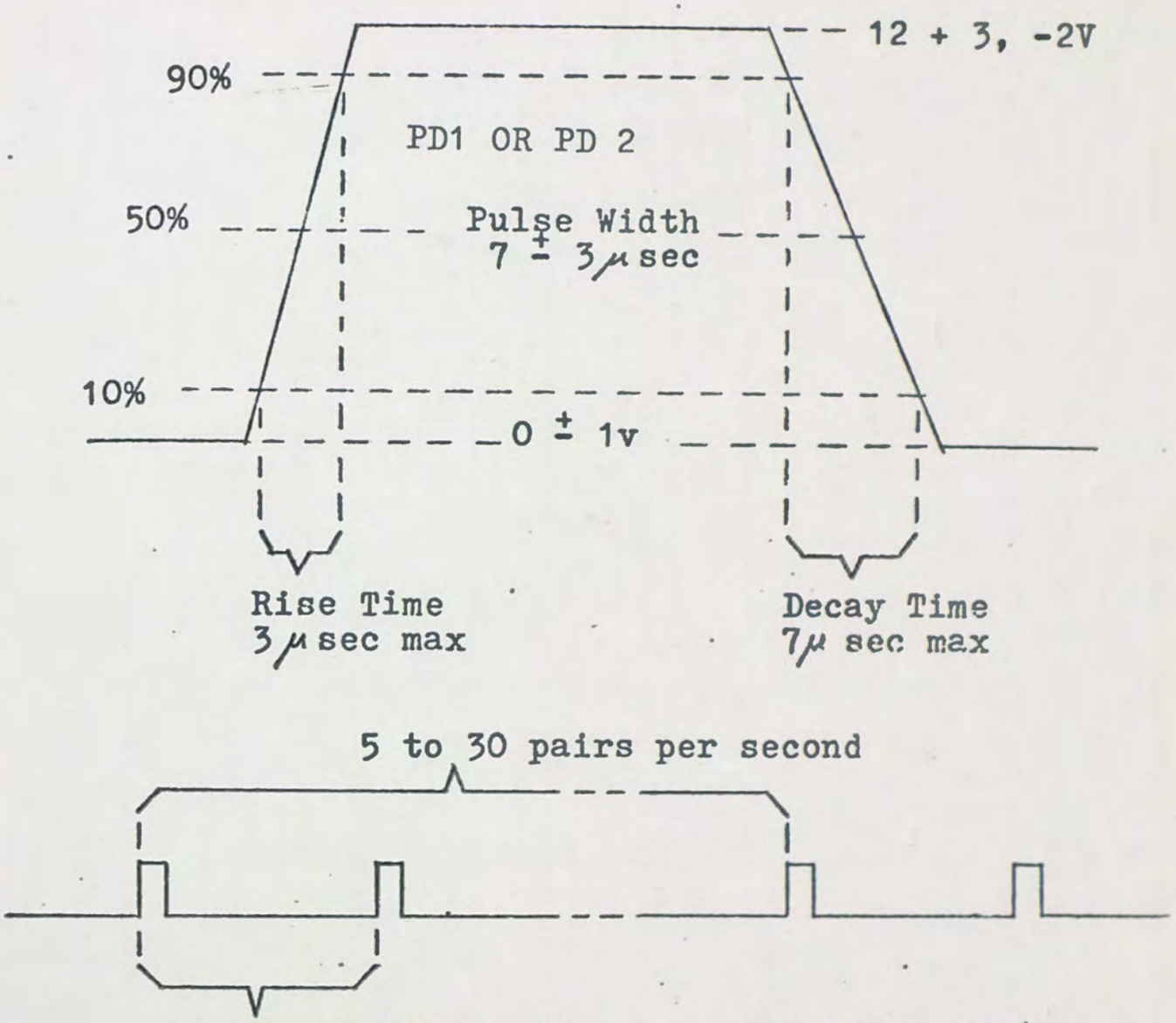
Seven-segment light-bar displays were selected for the distance readout. They provide the required .01 nm resolution, present a pleasing, easy to read, display and are simple to control with digital data. There are many types of seven segment displays to choose from, including vacuum fluorescent, electroluminescent, liquid

crystal, light emitting diode and incandescent. Incandescent displays with direct viewing segments were selected because they are inexpensive, reliable and bright enough to be read easily even in relatively high ambient lighting conditions. The type chosen can be driven directly from logic circuitry, requiring less than 10 ma per segment at 5 vdc, a standard logic supply voltage. The 7400 series TTL, being compatible with the system requirements, was selected as the logic family to be used. All the anticipated functions, such as presettable, up-down, BCD counters and 7-segment decoder drivers, can be obtained from several sources. The family is easy to work with, familiar to the prople involved and has adequate noise immunity for the expected environment. Switching speeds are also compatible with the 8 MHz maximum clock rates as described in the next section.

2.3 DME PULSE PAIR DESCRIPTION

As stated in section 1.2, ARINC Characteristic No. 568 will be used to define the DME pulse pair. The analog distance shall be represented by the time delay between pulses of the analog distance pulse-pair, PD1 and PD2. This output shall be transmitted at a rate between 5 and 30 pulse pairs per second. The nominal spacing, in micro-seconds, when measured between any two equal amplitude points on the leading edges of PD1 and PD2 from 3.5 to 6.5 volts amplitude, shall be equal to 50 plus (12.359

times the distance in nautical miles).[1]



Analog Pulse Pair

Figure 2

Pulse Characteristics

Pulse Width----------7 ± 3 μ sec

Rise Time----------3 μ sec max

Decay Time----------7 μ sec max

[1]Airlines Electronic Engineering Committee, ARINC Characteristic No. 568, MARK III Airborne Distance Measuring Equipment (Annapolis, Md.: Airlines Electronic Engineering Committee, 1968), pp. 7-13.

Pulse Characteristics (contd)

Pulse Amplitude----------12 + 3, - 2 volts

Base Line Noise----------0 ± 1v PK to PK MAX

PD1 and PD2 must be identical in risetime and amplitude, insofar as is practical, in order to meet accuracy requirements. Each utilization equipment shall present a load of not less than 12k ohms in parallel with not more than 100 picofarads.

For distance measurement the two way propagation time of the r-f signal shall be standardized at 12.359 microseconds per nautical mile. System delay from the first interrogation pulse to the first reply pulse shall be 50 microseconds.

Using 3×10^8 m/sec as the approximate velocity of radio waves, the 12.359 μ sec delay time may be calculated as follows:

$(3 \times 10^8 \text{ m/sec})\ (3.281 \text{ ft/m}) = 9.839 \times 10^8 \text{ ft/sec}$

$$\frac{6080 \text{ ft/nm}}{9.839 \times 10^8 \text{ ft/sec}} = 6.1795 \ \mu \text{ sec/nm}$$

for two-way propagation

$(2)\ (6.1795 \ \mu \text{ sec/nm}) = 12359 \ \mu \text{ sec/nm}$

There will be some additional pulse separation due to ground station receiver and transmitter delays. A fixed 50 μ sec system delay was chosen as adequate to include receiver delay, transmitter delay and a pad to

standardize the total delay at all ground stations.

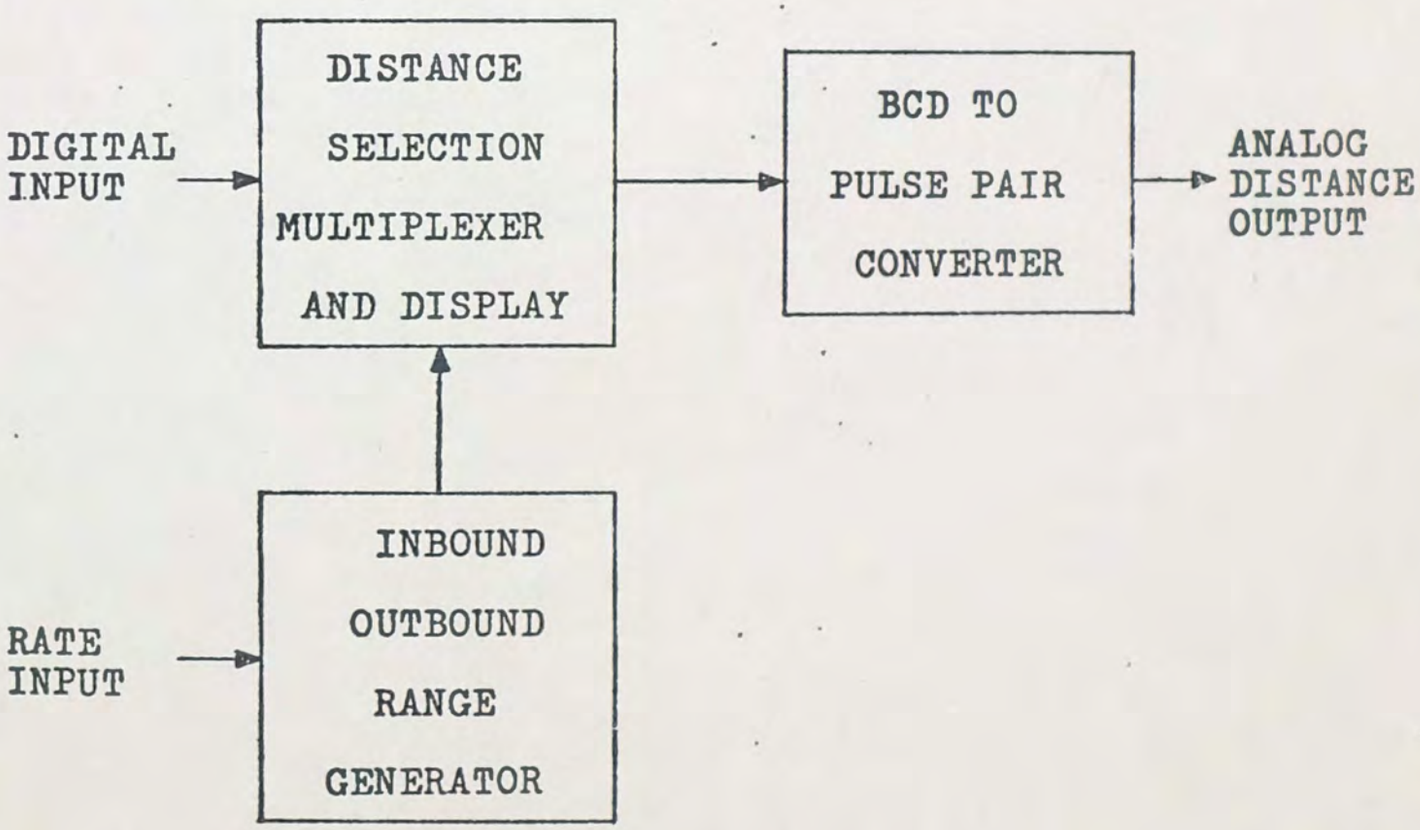
As stated in section 1.2, the desired resolution of distance is .01 nm. This implies a basic clock frequency for distance computation of:

$$\frac{1}{12.359\ \mu\text{ sec/nm} \times .01\text{ nm}} = 8.09127\text{ MHz}$$

Which is a standard DME crystal frequency.

3.0 SYSTEM DESIGN

As the initial step in the actual design, the system is partitioned into three main parts; the DISTANCE SELECTION MULTIPLEXER AND DISPLAY, the INBOUND-OUTBOUND RANGE GENERATOR and the BCD TO PULSE PAIR CONVERTER as shown in Figure 3, the Basic Block Diagram.



Basic Block Diagram

Figure 3

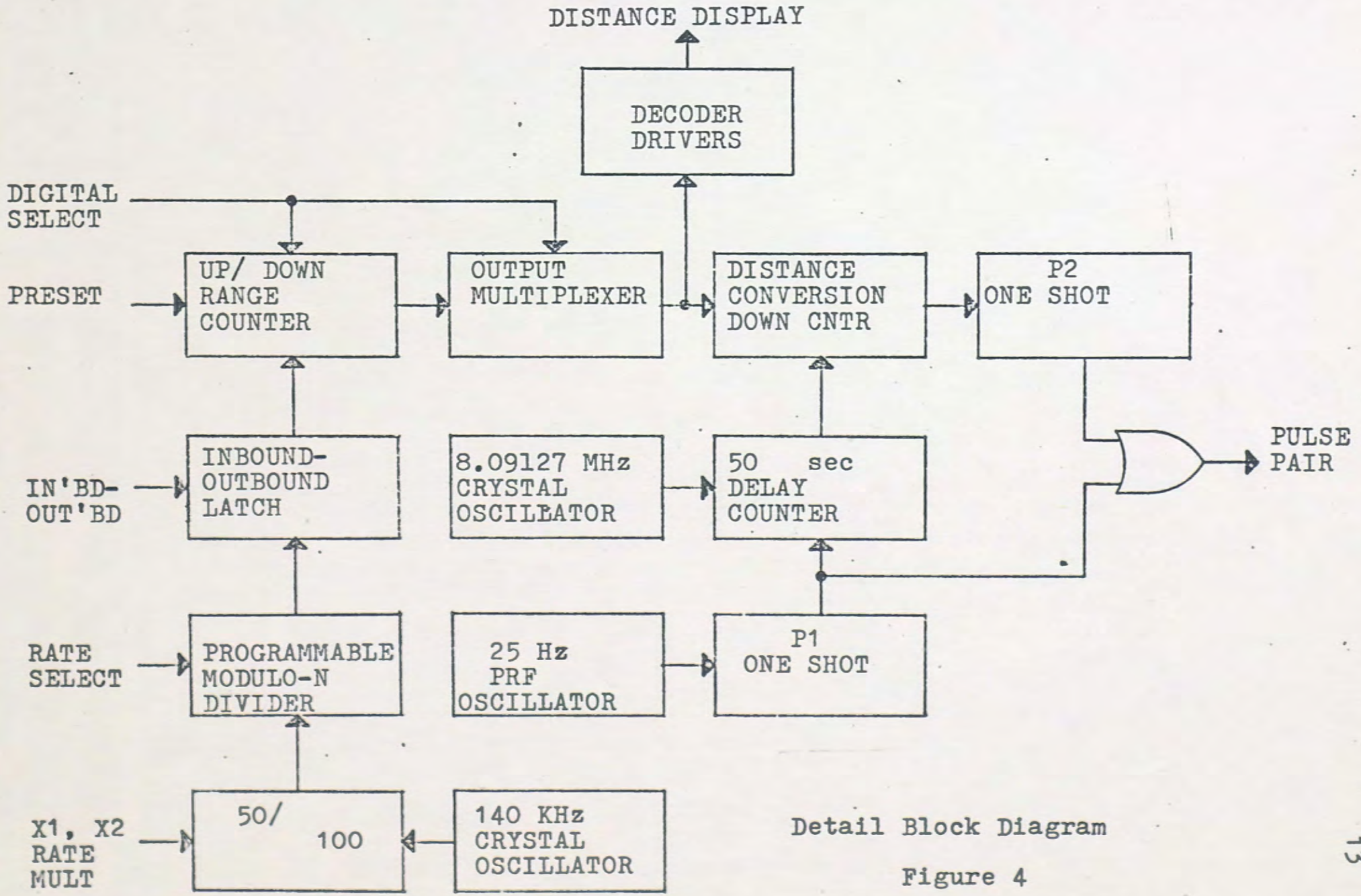
Each of these sections is then further broken down to form the Detail Block Disgram of Figure 4 from which the circuit design follows.

3.1 DISTANCE SELECTION MULTIPLEXER AND DISPLAY

The DISTANCE SELECTION MULTIPLEXER AND DISPLAY consists of the OUTPUT MULTIPLEXER and the DECODER DRIVERS. The main function of this group is to select either digitally input distance from the thumbwheels or rate-varying distance from the inbound/outbound range generation circuitry and to display the actual pulse pair distance output of the simulator.

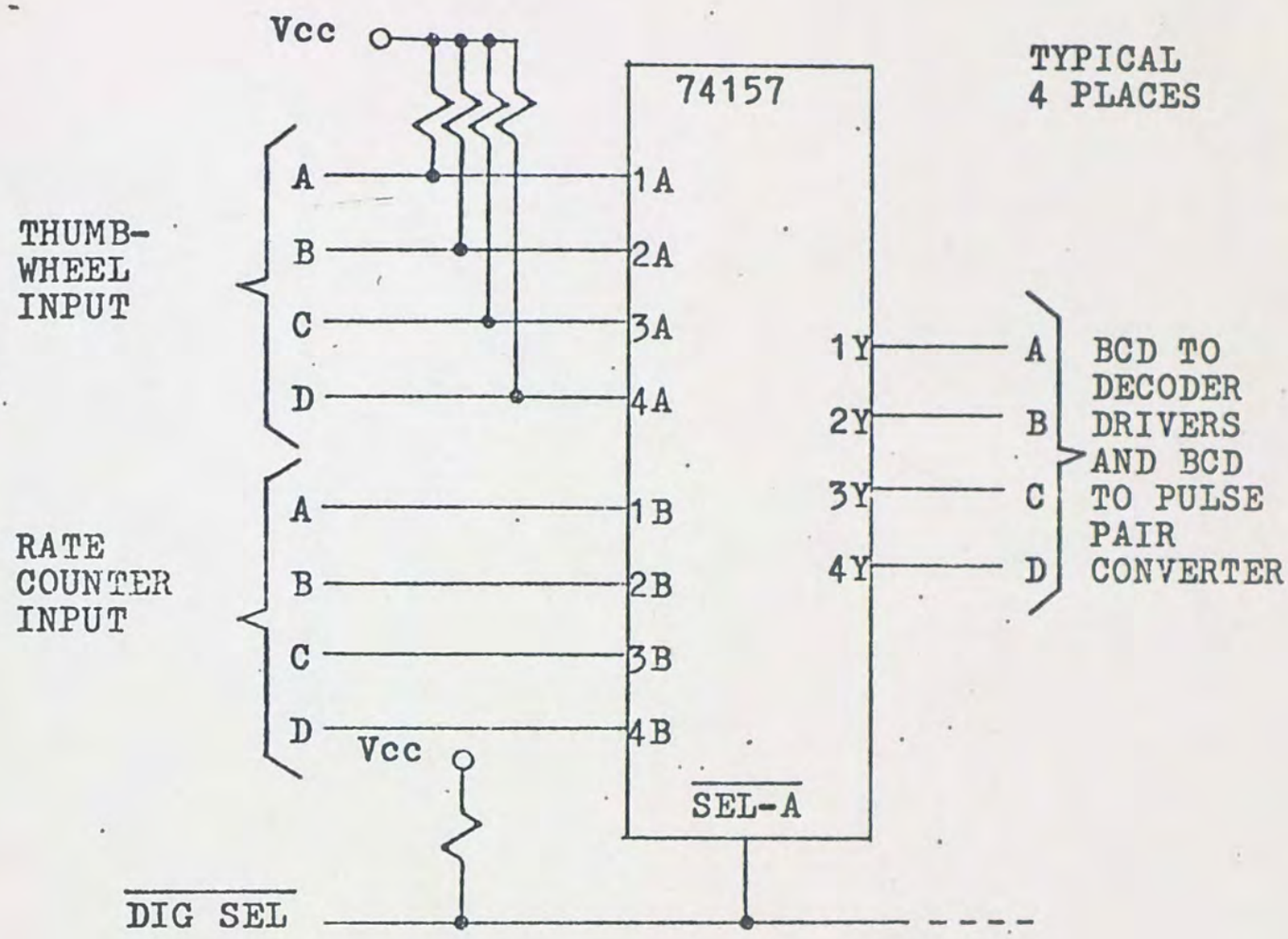
3.1.1 OUTPUT MULTIPLEXER

The OUTPUT MULTIPLEXER consists of four quad 2:1 multiplexers connected as shown in Figure 5. The device selects either the A or B group of inputs, as directed by the $\overline{\text{SEL-A}}$ input, to be the y output set. The A group comes directly from the thumbwheel selector switches. Using BCD compliment switches, grounding the switch commons and placing pull-up resistors on the data lines privides true BCD information to the multiplexer. The B group is the BCD output from the rate counters. Grounding the $\overline{\text{SEL-A}}$ line, by placing the rate rotary switch in the digital distance position, connects the thumbwheel inputs to the output y lines.



Detail Block Diagram

Figure 4



Output Multiplexer

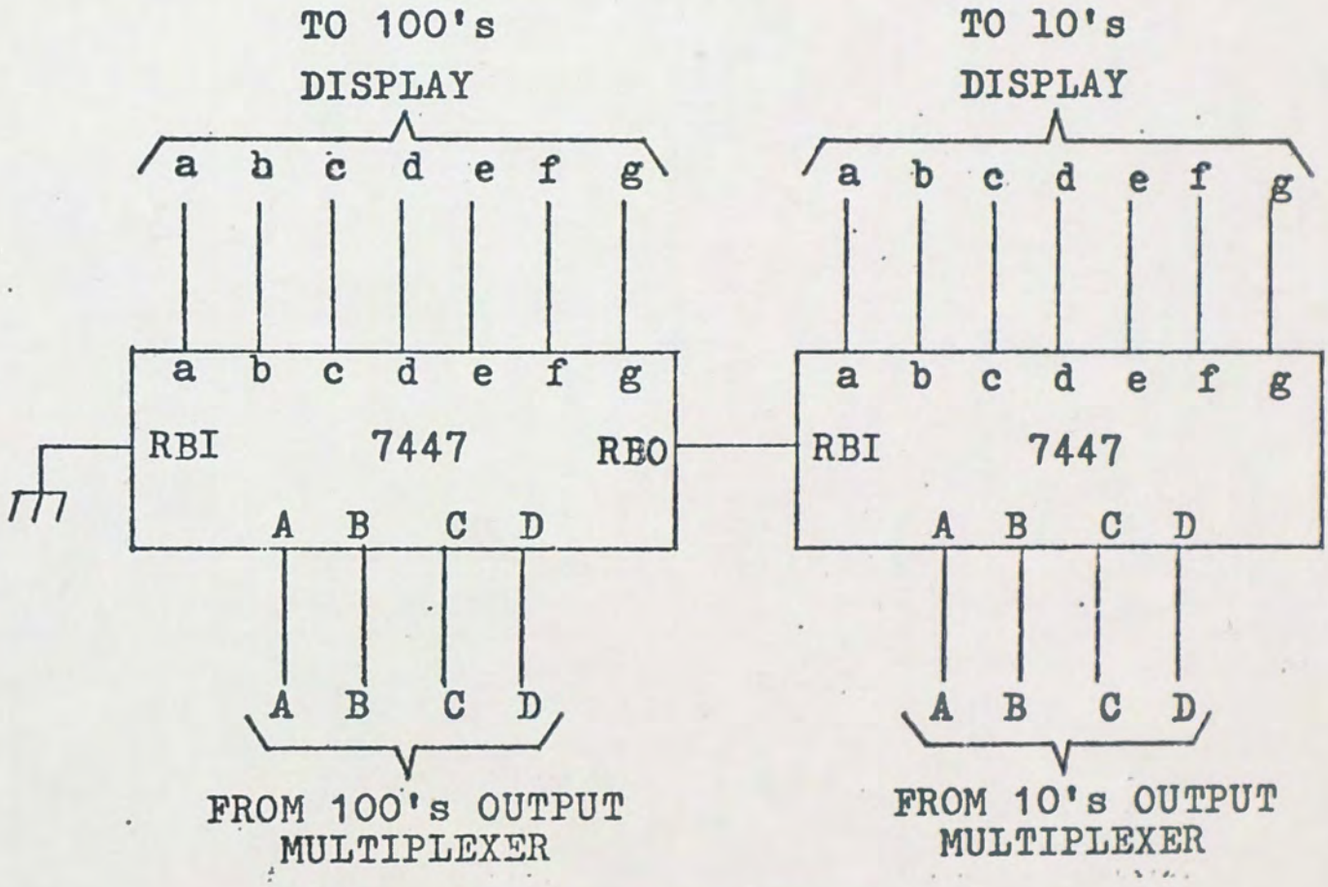
Figure 5

3.1.2 DECODER DRIVERS

The decoder drivers consist of five BCD to 7-segment decoder driver packages connected to ripple blank leading zeros in the first two digits. Eliminating extra zeros to the left presents the data in the normally accepted fashion. The two most significant decades are shown interconnected in Figure 6. The other three drivers are similar but without the ripple blanking (RBI and RBO) connections.

The displays consist of seven lamp filaments, one

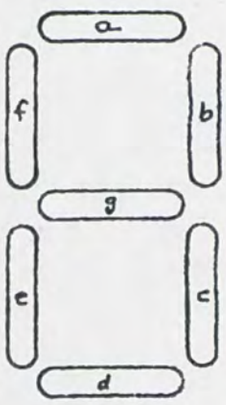
for each segment, connected to a common. The common is wired to the 5 vdc logic supply voltage and the decoder drivers turn on the appropriate filaments by supplying a ground through an open collector output transistor.



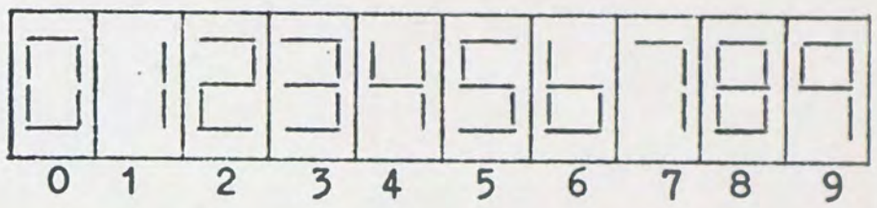
Decoder Drivers

Figure 6

Figure 7 shows the truth table for the decoder drivers and the resulting displays for BCD inputs.



Segment Identification



Numerical Designations and Resultant Displays

DECIMAL OR FUNCTION	INPUTS					OUTPUTS							
	RBI	D	C	B	A	RBO	a	b	c	d	e	f	g
0	0	0	0	0	0	0	1	1	1	1	1	1	1
0	1	0	0	0	0	1	0	0	0	0	0	0	1
1	x	0	0	0	1	1	1	0	0	1	1	1	1
2	x	0	0	1	0	1	0	0	1	0	0	1	0
3	x	0	0	1	1	1	0	0	0	0	1	1	0
4	x	0	1	0	0	1	1	0	0	1	1	0	0
5	x	0	1	0	1	1	0	1	0	0	1	0	0
6	x	0	1	1	0	1	1	1	0	0	0	0	0
7	x	0	1	1	1	1	0	0	0	1	1	1	1
8	x	1	0	0	0	1	0	0	0	0	0	0	0
9	x	1	0	0	1	1	0	0	0	1	1	0	0

Truth Table

Note: A "0" in the truth table implies the lamp segment is "on", an "x" represents a "don't care" condition.

Display Chart

Figure 7

3.2 INBOUND/OUTBOUND RANGE GENERATOR

The inbound/outbound range generation circuitry consists of a 140 KHz crystal oscillator, the X1, X2 rate multiplier control and clock divider, a programmable modulus divider for rate selection, an inbound/outbound latch and the up/down range counter. This circuitry must supply the distance output when the rate selector switch is in any position other than digital select. It provides the control and updates the distance at the selected rate to allow "flying" inbound or outbound with respect to the simulated ground station.

3.2.1 140 KHz CRYSTAL OSCILLATOR

A crystal oscillator was used as the basic rate clock because of its inherent accuracy and stability. The 140 KHz oscillator frequency was chosen by selecting the lowest frequency compatible crystal available from stock. The actual clocking rates to the up/down counters are on the order of a few Hertz, hence the use of a low frequency oscillator minimizes the amount of division (and thereby the number of integrated circuits) required. A further restriction on the frequency is that it be a whole integer multiple of all the desired clock rates so that digital dividers may be used. The desired rates are from 0 to 420 KTS in 60 KT increments with a rate doubling switch to provide rates to 840 KTS. The frequencies required to provide .01 nm updates at each of these rates

are calculated as follows:

$$60 \text{ nm/hr} = 1 \text{ nm/min} = \frac{1}{60} \text{ nm/sec} = \frac{100}{60} .01 \text{ nm/sec}$$

Therefore an update rate of 60 KTS in .01 nm increments requires a clock frequency of $\frac{100}{60} = 5/3$ Hz. Similarly the remaining frequencies are calculated to be:

Rate	Frequency
120 KTS	10/3 Hz
180 KTS	5 Hz
240 KTS	20/3 Hz
300 KTS	25/3 Hz
360 KTS	10 Hz
420 KTS	35/3 Hz

The selected oscillator frequency must be a whole number multiple of the least common denominator of these frequencies and the X2 multiplier. The least common denominator was determined to be 700/3. Dividing the available low frequency crystals by this number led to the selection of the 140 KHz crystal since its division yielded the first whole integer.

$$\frac{140,000}{700/3} = 600$$

The actual divisor for each frequency may be determined by the following equation:

$$\text{DIVISOR} = \frac{140,000}{\text{FREQUENCY}}$$

For example at 60 KTS the desired frequency is 5/3 Hz and the divisor is found to be:

$$\text{DIVISOR} = \frac{140{,}000 \text{ Hz}}{5/3 \text{ Hz}} = 84{,}000$$

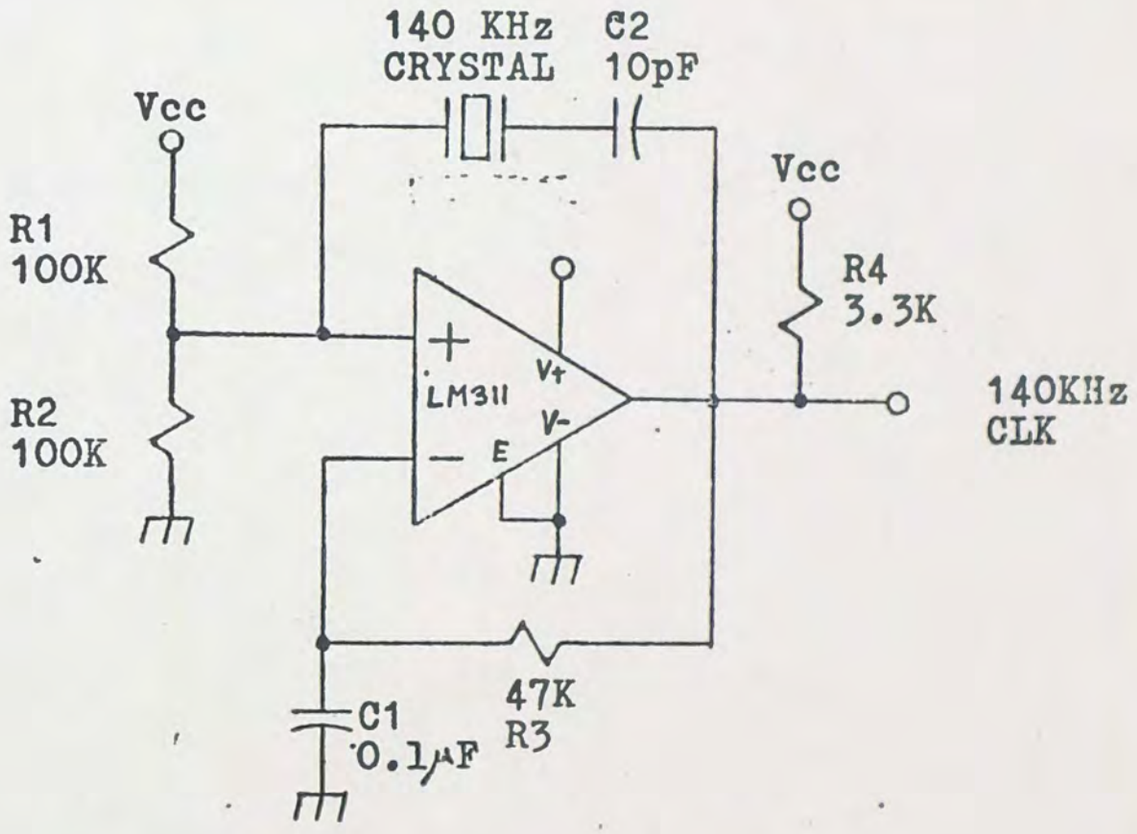
Similary the remaining divisors are found to be:

Rate	Divisor
120 KTS	42,000
180 KTS	28,000
240 KTS	21,000
300 KTS	16,800
360 KTS	14,000
420 KTS	12,000

Noting that each of these divisors may be broken up into two divisors, one of which is always $\div 100$, provides an easy method of achieving the X1/X2 rate multiplication by changing this divisor to $\div 50$ when X2 is selected. This doubles the rate clock frequency and hence the rate in each case. The programmable modulus counter will then supply the remaining divisor as required.

The oscillator, which uses a voltage comparator as the active device, is shown in Figure 8. It is similar to a free running multivibrator, except that the positive feedback is obtained through a quartz crystal. The inputs are biased within the common mode range by R1 and R2. DC stability, which insures starting, is provided by

negative feedback through R3. The circuit oscillates when transmission through the crystal is at a maximum, so the crystal operates in its shunt-resonant mode. The high input impedance (approximately 25M ohms for this circuit) of the comparator and the isolating capacitor, C2, minimize the loading of the crystal and contribute to frequency stability.[2]



140 KHz Crystal Oscillator

Figure 8.

As shown, the oscillator provides a 140 KHz square-wave output. The comparator has an output transistor with uncommitted collector and emitter (E) and will operate

[2]R. J. Widlar, National Semiconductor Corp. Applications Note AN-41, Precision IC Comparator Runs from 5v Logic Supply (Santa Clara, Calif.: National Semiconductor Corp., 1970), p.3.

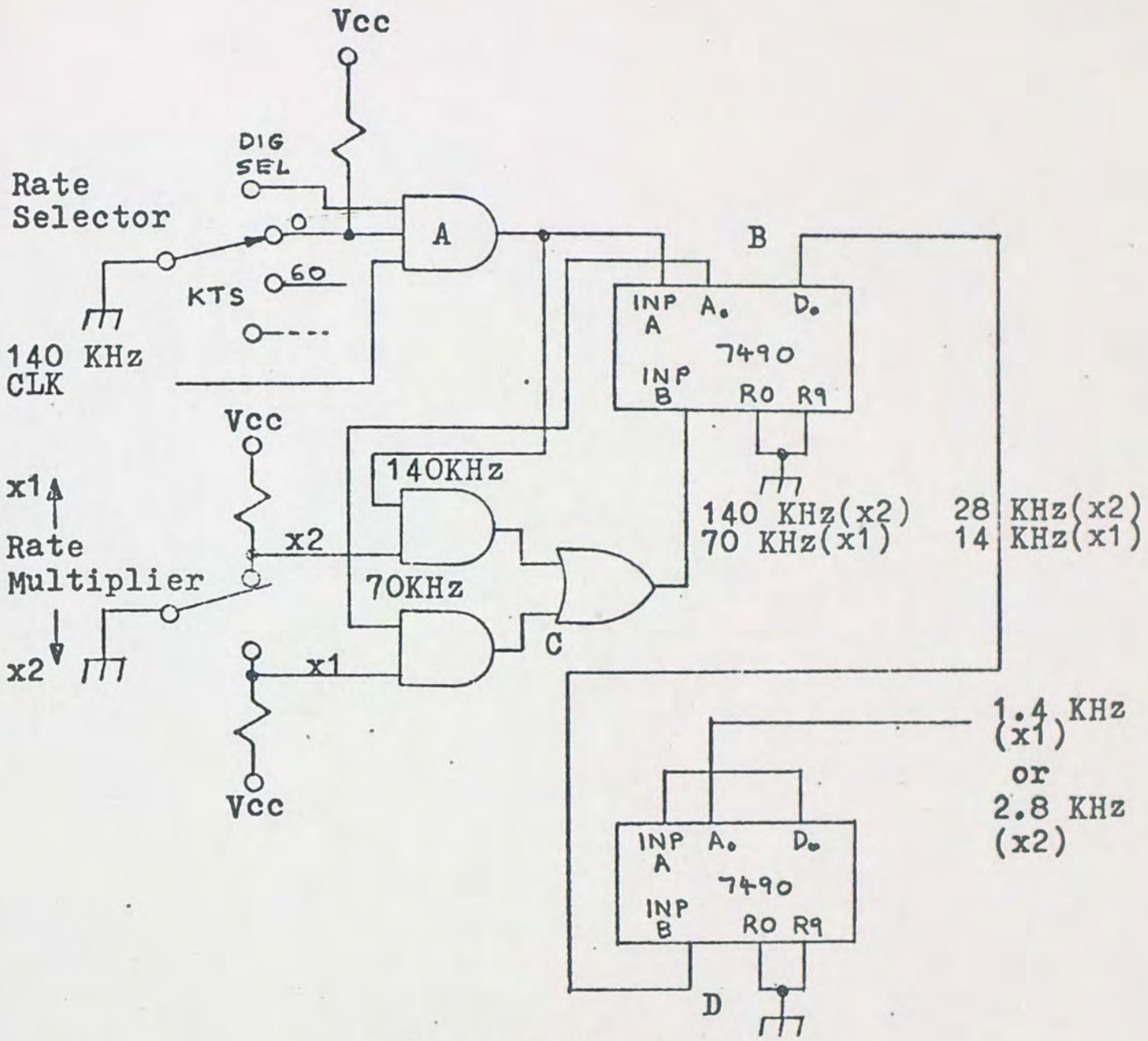
from a single +5v (Vcc) supply. It is therefore easily interfaced with TTL by grounding the emitter and using a pull-up resistor (R4) from the collector to the Vcc, logic supply voltage.

Since the loading of the crystal is minimal, the accuracy of the oscillator is determined mainly by the frequency tolerance of the crystal. The device used has a specified tolerance of .02% which can be translated directly to a rate tolerance of .02% (0.168 KTS at 840 KTS) which is well within the accuracy goal of 0.1% as stated in Section 1.2.

3.2.2 X1, X2 RATE CONTROL

The X1, X2, rate control circuit divides the 140 KHz clock from the crystal oscillator by 100 or 50 to 1.4 KHz (X1) or 2.8 KHz (X2) respectively as selected with the rate multiplier switch. The circuit is shown in Figure 9.

AND gate A enables the 140 KHz clock signal whenever the rate selector switch is in any position other than digital select from the thumbwheels or the zero knots position. Integrated circuit B is a standard decade counter arranged as a divide by two and a divide by five counter. The clock at INP A is divided by two at Ao to give 70 KHz. The AND-OR circuit C selects either 70 KHz (X1) or 140 KHz (X2) as dictated by the position of the rate multiplier switch. The switch is shown in the X1



Rate Multiplier Control

Figure 9

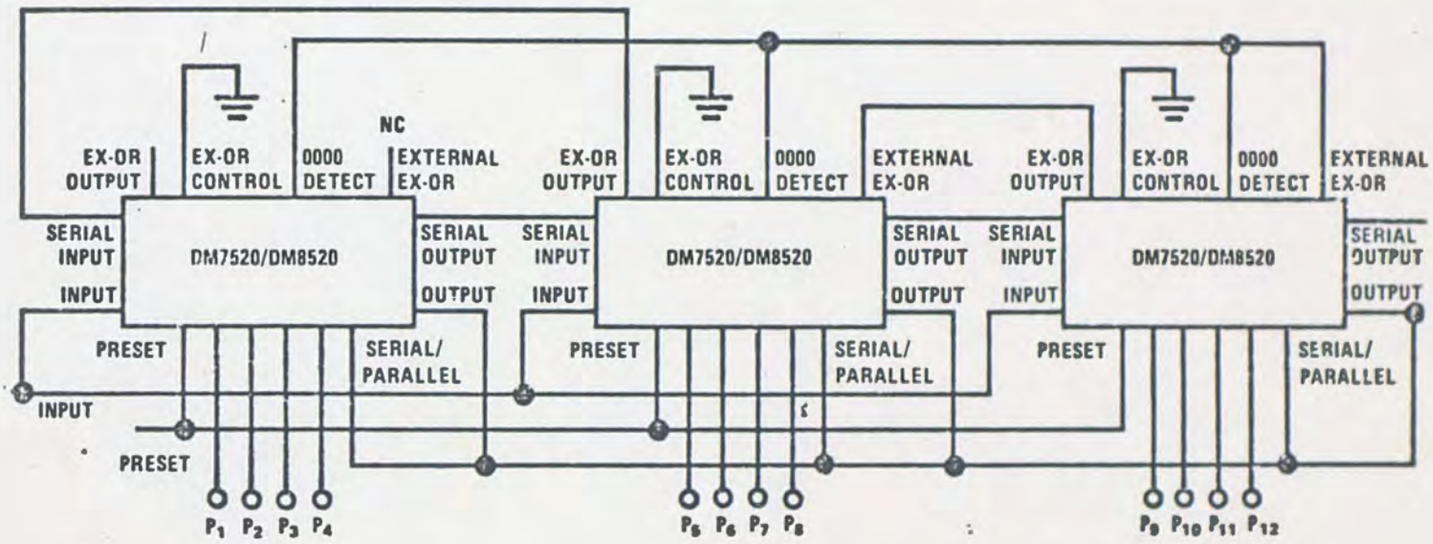
position, thereby supplying 70 KHz as the clock input at the BD INPUT of the decade counter. This frequency is then divided down to 14 KHz (28KHz in X2 position) at the Do output. Decade counter D is wired to provide a symmetrical divide by ten at the Ao output. The output is then the desired 1.4 KHz or 2.8 KHz for a rate multiplier of X1 or X2 respectively.

3.2.3 PROGRAMMABLE DIVIDER

The device selected for use as the programmable divider is the DM8520, a four bit shift register counter. The DM8520 is a shift register with internal gating to perform the exclusive OR required for operation as a maximal sequence shift register generator. The divider function is performed by the addition of a known-state detector to provide a once-per-cycle output. Programming capability is provided by parallel data input lines which are gated by the output signal to allow short-cycling of the generator to any desired period, The all-zero state is precluded; and, therefore, the maximum number of states is always one less then the theoretical maximum number. Since the DM8520 contains four flip-flops, its maximum number of states is 15. Because the 1111 state occurs only once during a 15-state sequence, this state is detected; and its output becomes the output of the divider. To divide by numbers greater than 15, it is necessary to cascade the dividers with two packages providing division by 2 through 255 and three packages extending the range to 4095.[3] As stated in Section 3.2.1, the required divisions are from120 to 840 so that three devices must be used.

[3]J. Kalb, National Semiconductor Corp. Applications Note AN-17, Programmable Divider Applications (Santa Clara, Calif.: National Semiconductor Corp., 1968), p.2

The manufacturer's recommended circuit was used for a three stage divider and is shown in Figure 10. Program inputs for the various divisions available for a three-package configuration are given in the published Data Sheet and partially reproduced in the appendix.

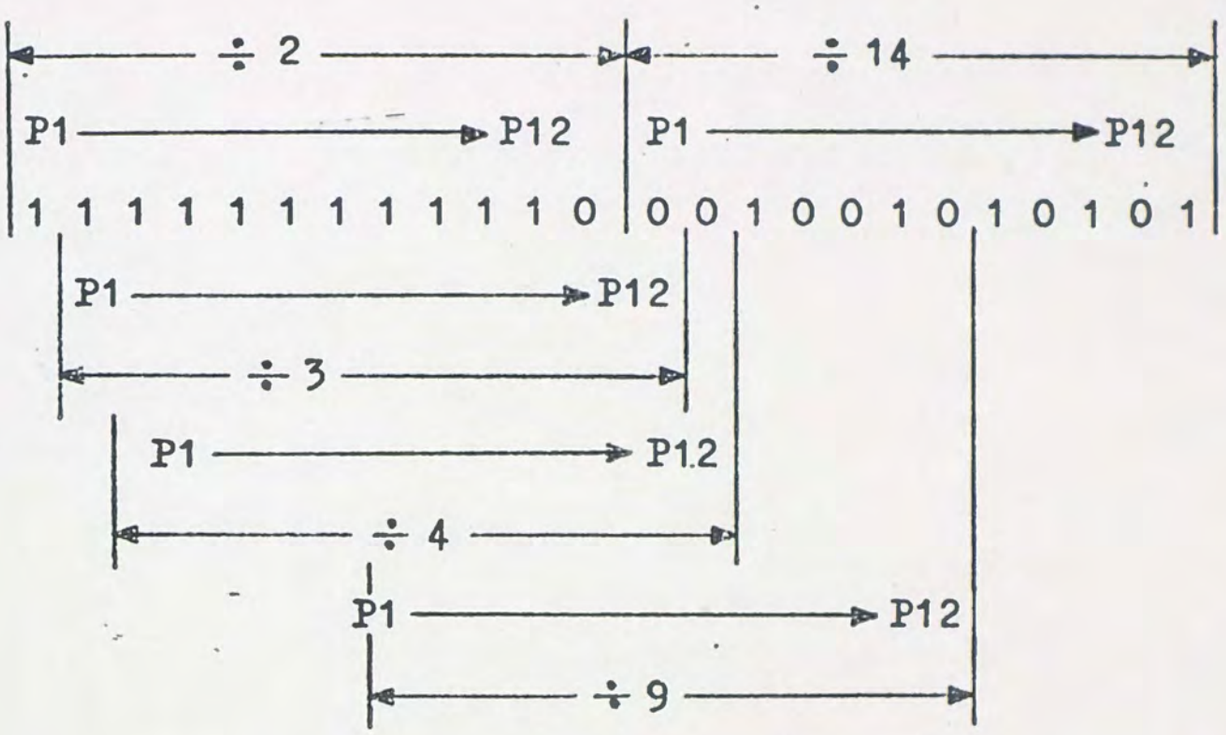


Since there are twelve stages in such a configuration, the entire bit pattern is accounted for by printing every twelth shift, i.e., the program input for every twelfth divisor. Program inputs for division between those shown in the chart may be determined by combining two adjacent lines of the chart[5] and shifting right

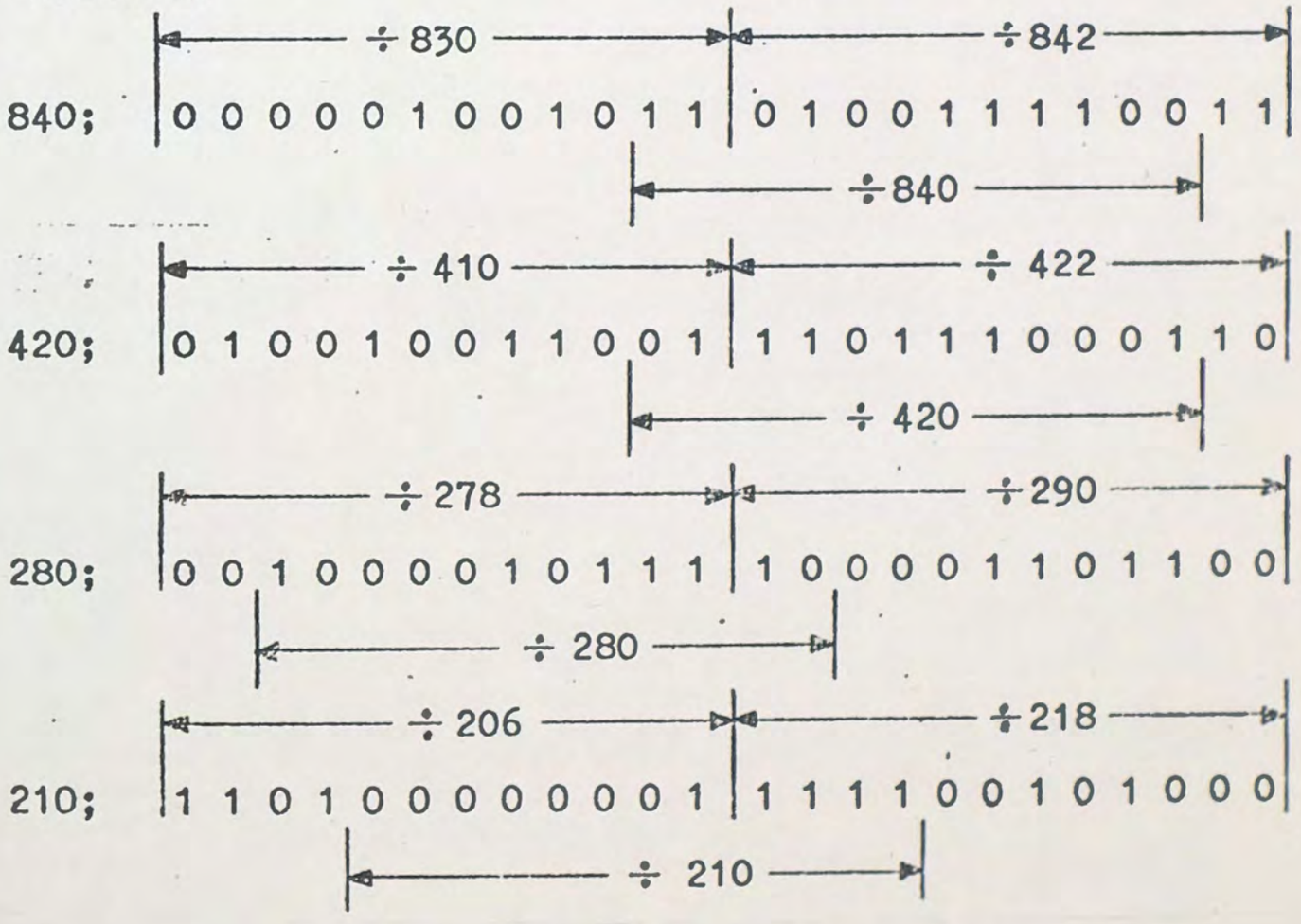
[4] J. Kalb, National Semiconductor Corp. Applications Note AN-17, Programmable Divider Applications (Santa Clara, Calif.: National Semiconductor Corp., 1968), p.4.

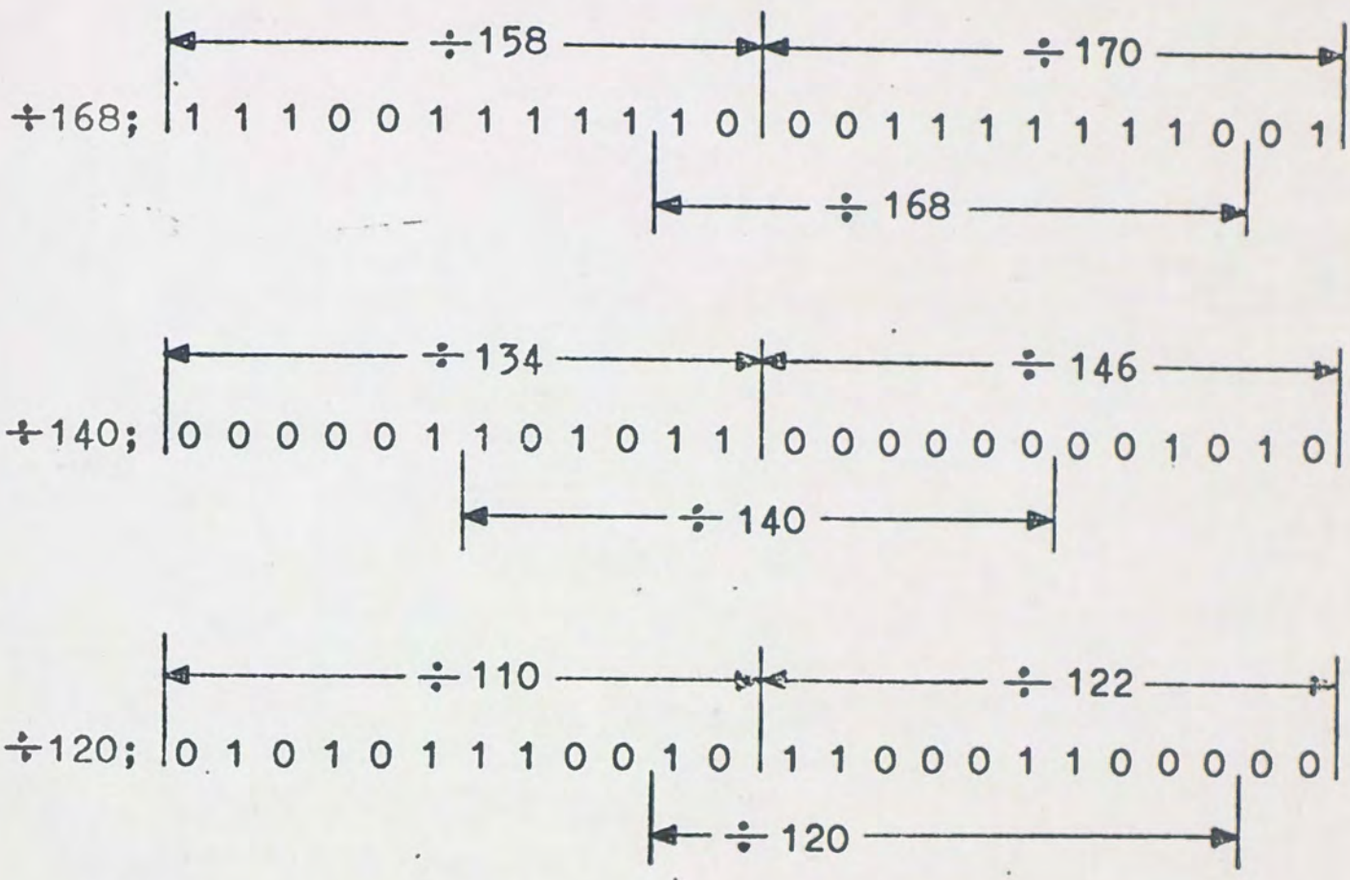
[5] J.Kalb, National Semiconductor Corp. Applications Note AN-17, Programmable Divider Applications (Santa Clara, Calif.: National Semiconductor Corp., 1968), p.5.

to the required divisor as shown below:



Using this method, the programming inputs (P1 through P12) for the required divisions were found as follows:





The results were then tabulated to form the programming truth table of Figure 11.

KTS	÷BY	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12
60	840	1	1	0	1	0	0	1	1	1	1	0	0
120	420	0	1	1	1	0	1	1	1	0	0	0	1
180	280	1	0	0	0	0	1	0	1	1	1	1	0
240	210	0	0	0	0	0	0	0	1	1	1	1	1
300	168	1	0	0	0	1	1	1	1	1	1	1	0
360	140	1	0	1	0	1	1	0	0	0	0	0	0
420	120	1	0	1	1	0	0	0	1	1	0	0	0

Programming Truth Table

Figure 11

The equations for the programming inputs can now be written directly from the truth table. Each equation is written for 1's or 0's, whichever is least, to minimize gate inputs. The bars over the KT inputs indicate their normally high state (until selected by the rate switch).

$$\overline{P1} = \overline{120} + \overline{240}$$

$$\overline{P2} = \overline{60} + \overline{120}$$

$$\overline{P3} = \overline{120} + \overline{360} + \overline{420}$$

$$\overline{P4} = \overline{60} + \overline{120} + \overline{420}$$

$$\overline{P5} = \overline{300} + \overline{360}$$

$$\overline{P6} = \overline{60} + \overline{240} + \overline{420}$$

$$\overline{P7} = \overline{60} + \overline{120} + \overline{300}$$

$$\overline{P8} = \overline{360}$$

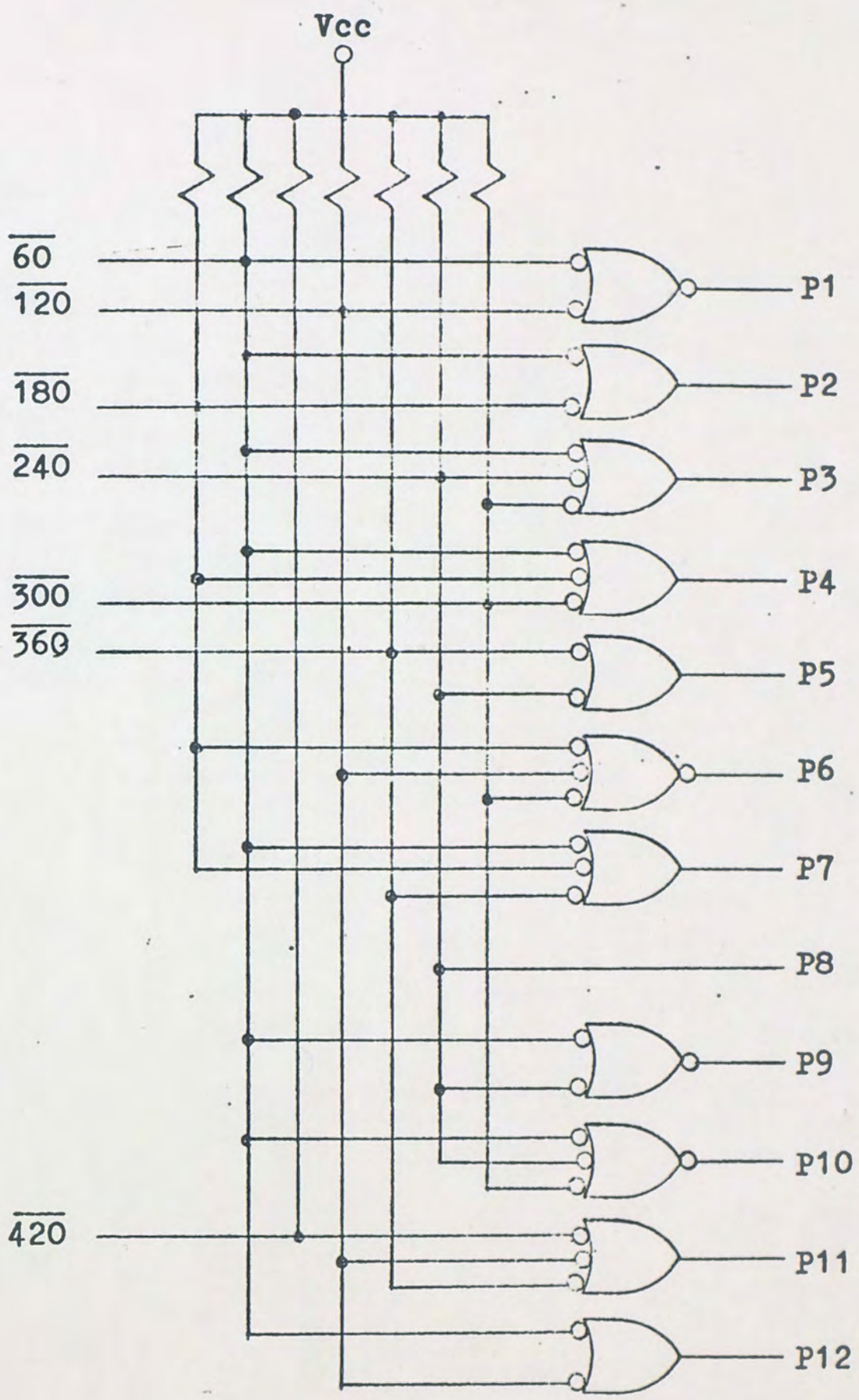
$$\overline{P9} = \overline{120} + \overline{360}$$

$$\overline{P10} = \overline{120} + \overline{360} + \overline{420}$$

$$\overline{P11} = \overline{180} + \overline{240} + \overline{300}$$

$$\overline{P12} = \overline{120} + \overline{240}$$

The gating logic to develop these inputs is shown in figure 12. This is a representative schematic only in that the actual gating was changed slightly later to minimize the number of gate-type integrated circuits, using spare gates where advantageous, in the overall system.

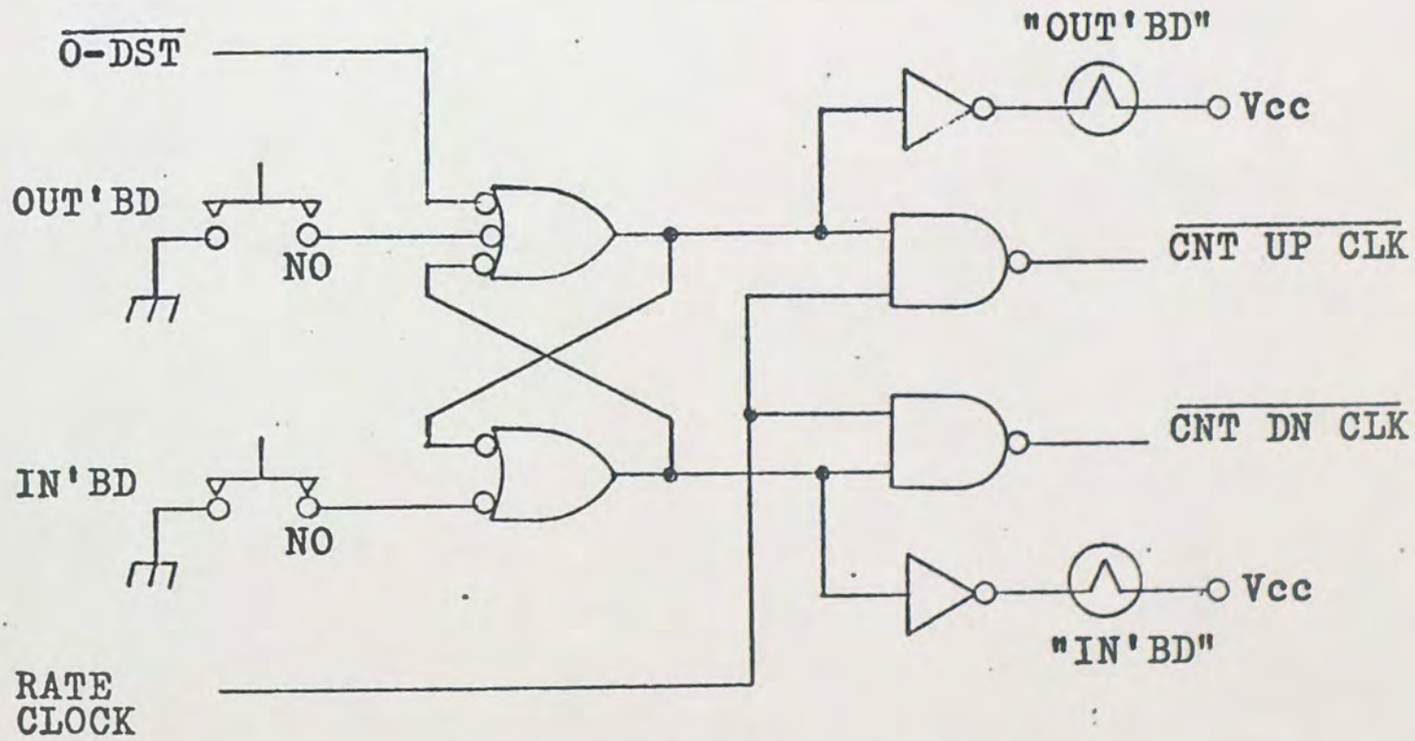


Programming Input Logic

Figure 12

3.2.4 INBOUND/OUTBOUND LATCH

The Inbound/Outbound Latch is a simple bistable latch which gates the rate clock from the programmable rate divider to either count up (outbound) or count down (inbound) the range counter. The latch is set to the outbound state manually by depressing the outbound push-button or automatically upon reaching zero distance($\overline{\text{O-DST}}$) when flying inbound. Depressing the inbound push-button sets the latch to the inbound state. In addition, the outputs control open collector lamp drivers to indicate the state of the latch. The circuit is shown in Figure 13.



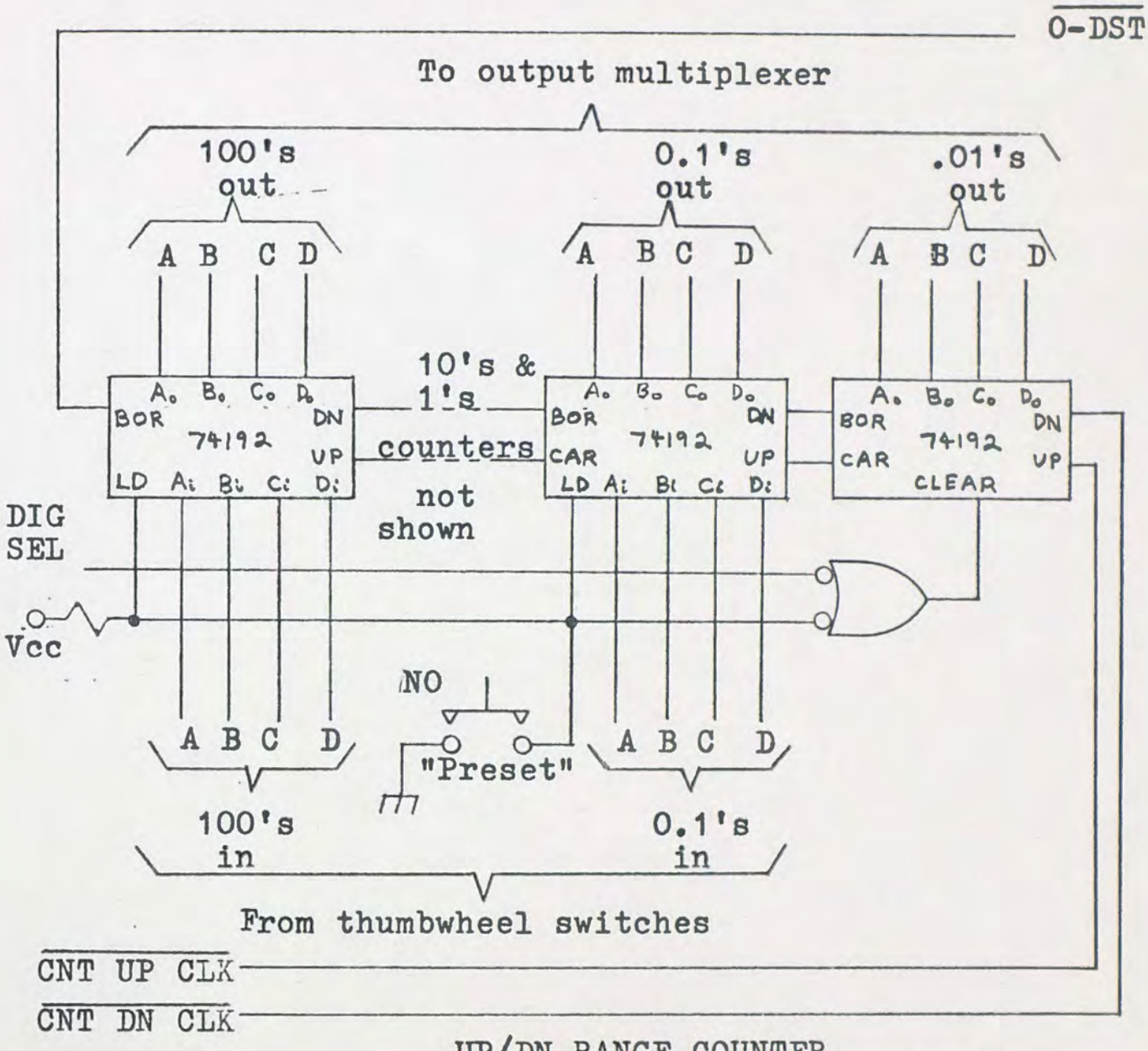
Inbound-Outbound Latch

Figure 13

3.2.5 UP/DOWN RANGE COUNTER

The up/down range counter consists of five preset-table, up/down, decade counters cascaded, ripple borrow/carry, to provide a maximum count of 999.99. When clocked up or down by the .01 nm increment rate clock, these counters provide the desired BCD output to the output multiplexer for inbound or outbound flight. The circuit is shown in Figure 14. The rightmost counter is the least significant digit and corresponds to hundredths of a nautical mile. The leftmost counter represents hundreds of nautical miles.

The count up clock ($\overline{\text{CNT UP CLK}}$) and count down clock ($\overline{\text{CNT DN CLK}}$) from the inbound/outbound latch drive the count up and count down inputs of the hundredths counter. If the count is zero and a count down is specified, a borrow (BOR) pulse is output to the next significant counter. Similary, if the count is nine and a count up clock is received, a carry (CAR) pulse is generated. These carry and borrow outputs supply the input up and down clocks respectively to the tenths decade counter and so on through each digit to the hundreds counter, providing standard BCD format data from .01's to 100's. When all five counters reach zero, the next count down pulse will propagate through all five counters' CNT DN and BOR lines. The borrow output of the 100's counter, indicating zero distance ($\overline{\text{O-DST}}$), is used to set



UP/DN RANGE COUNTER
Figure 14

the inbound/outbound latch to the outbound state. This prevents the counters from going to 999.99 nm on this count pulse and, by simultaneously shifting the VOR bearing to the RNAV system by 180°, allows simulation of station "fly-over".

The BCD inputs to the counters (Ai, Bi, Ci and Di) are connected directly to the outputs of the corresponding thumbwheel switches, 100's counter inputs to 100's thumbwheel outputs etc.. When the preset push-

button is actuated, the thumbwheel distance is loaded into the counters allowing them to begin counting up or down from any preset input distance.

The hundredths counter, having no corresponding thumbwheel switch (0,1 nm resolution for digital input), is momentarily cleared to zero when the preset pushbutton is depressed. When the rate switch is in the digital select position, the hundredths counter is held at a constant zero. Hence selecting a distance of 100.0 nm with the thumbwheels for example, applies an input of 100.00 nm to the output distance converter and display. A multiplexer is therefore not required for this digit as in the other four to select between the thumbwheels and the rate counter.

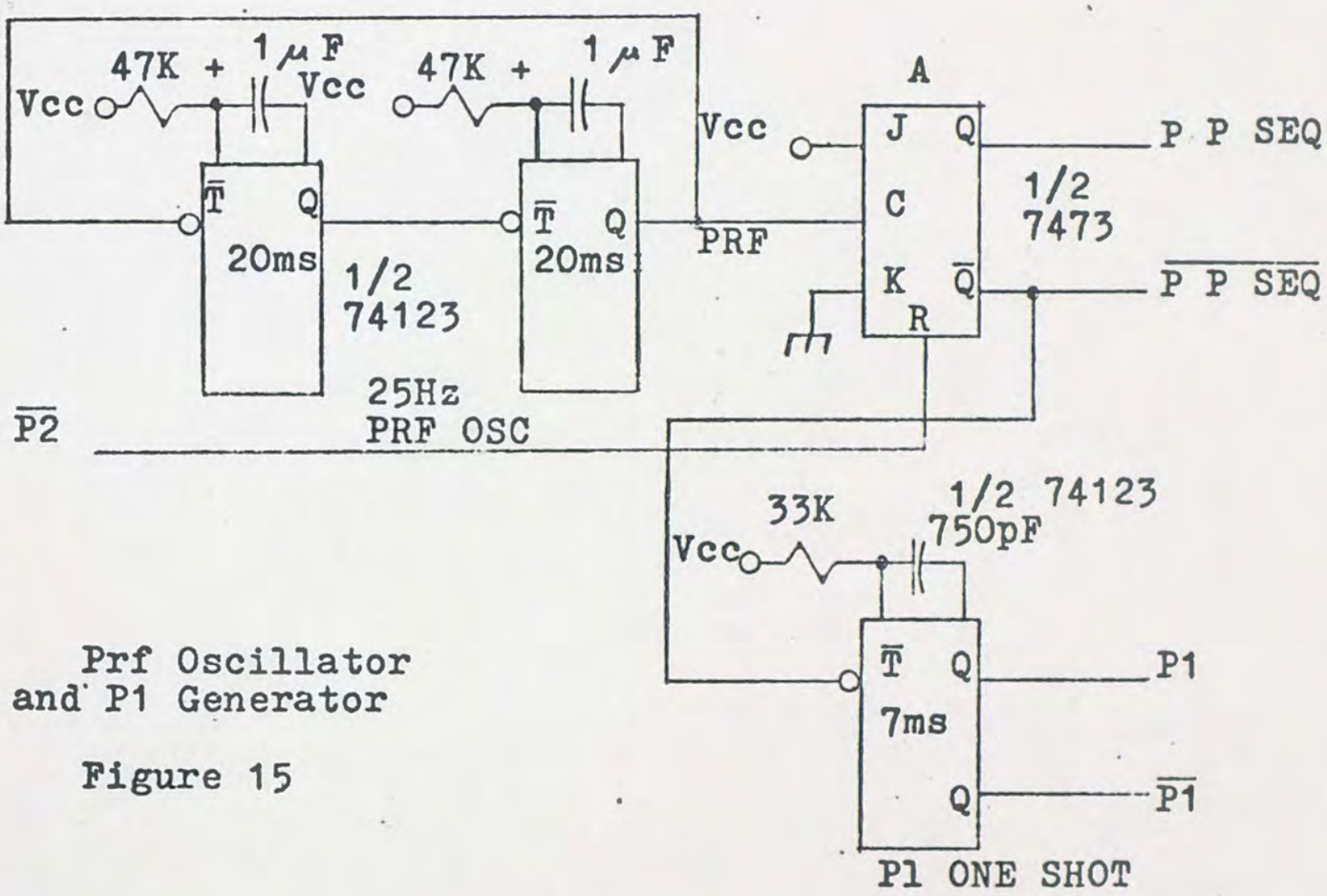
3.3 BCD TO PULSE PAIR CONVERTER

The function of this circuitry is to convert the BCD information from the distance output multiplexer into the analog pulse pair as described in Section 2.3 within the accuracy restraints of Section 1.2. The circuitry is partitioned into four groups for the actual design; the PRF Oscillator and P1 Generator, the 8 MHz Oscillator and 50 μ sec Delay, the Distance Counter and P2 Generator and the P1/P2 Output Interface.

3.3.1 PRF OSCILLATOR AND P1 GENERATOR

Section 2.3 states that the PRF (Pulse Repition Frequency) will be from 5 to 30 pulse pairs per second.

An astable multivibrator consisting of two one shots was used as the oscillator with the frequency arbitrarily set at 25 Hz. The circuit is shown below and the timing is illustrated in Figure 16.



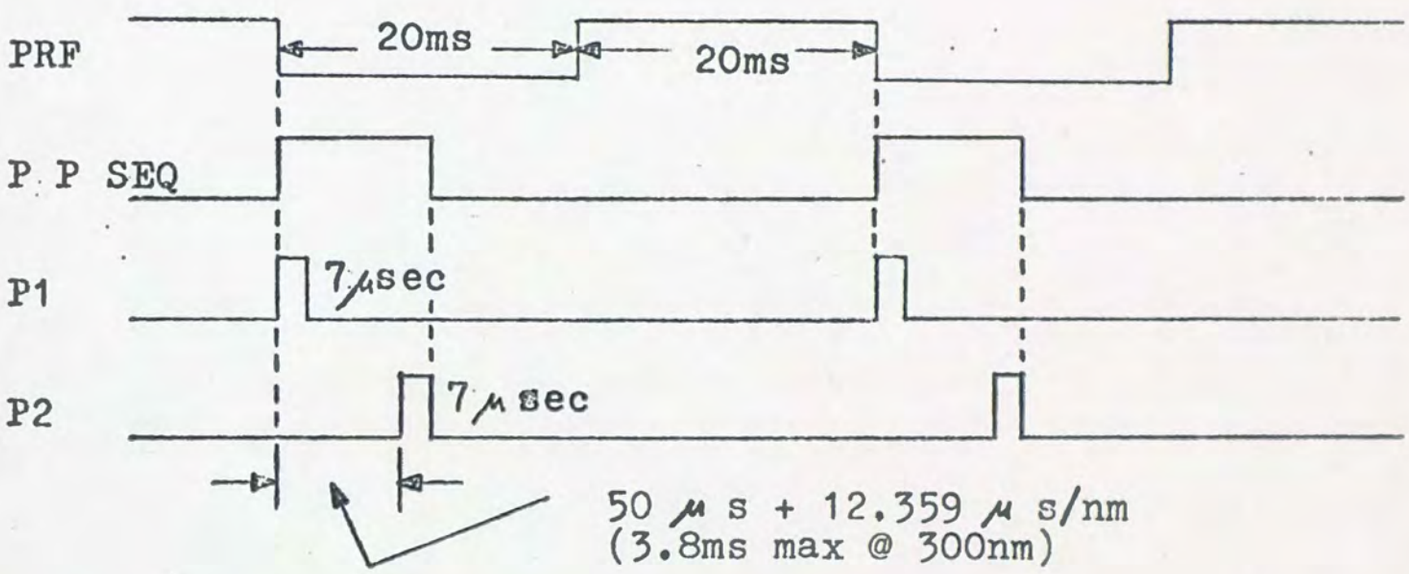
Prf Oscillator and P1 Generator

Figure 15

The timing components were selected by using the manufacturer's charts to pick ball-park standard values for the resistor and capacitor and adjusting the selections as indicated by the tested results.

The fall of the PRF oscillator output toggles Flip-Flop A, beginning a PP SEQ (Pulse Pair Sequence). This signal will be used to control the 50 μ sec delay circuit and will be terminated by the $\overline{P2}$ pulse as indicated in Figure 16. The beginning of the sequence

also triggers the P1 one shot, generating the 7 μ sec P1 pulse. The P1 pulse is used to load the distance counter of Section 3.3.3 and is combined with P2 in Section 3.3.4 to form the output analog DME distance.

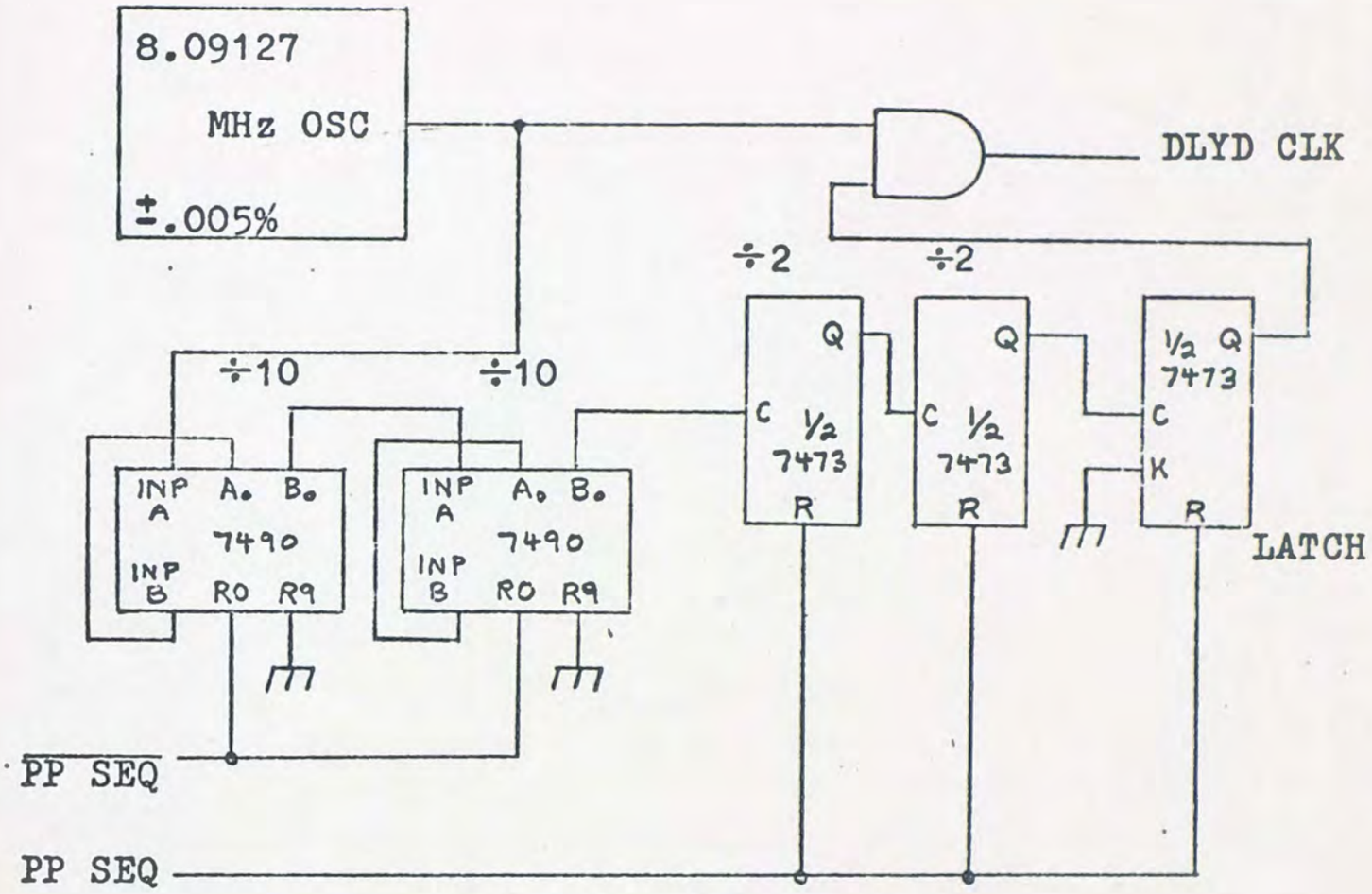


PRF And Pulse Pair Timing

Figure 16

3.3.2 8 MHz OSCILLATOR AND 50 μ SEC DELAY

The 8.09127 MHz oscillator is a purchased item with TTL compatible output. It is a standard device used in DME's to make the two-way propagation time to distance output conversion. The particular oscillator used was specified to a tolerance of $\pm$ .005% which translates directly to distance accuracy. At the stated 300 nm maximum range this would correspond to a clocking accuracy of $\pm$ .015 nm.

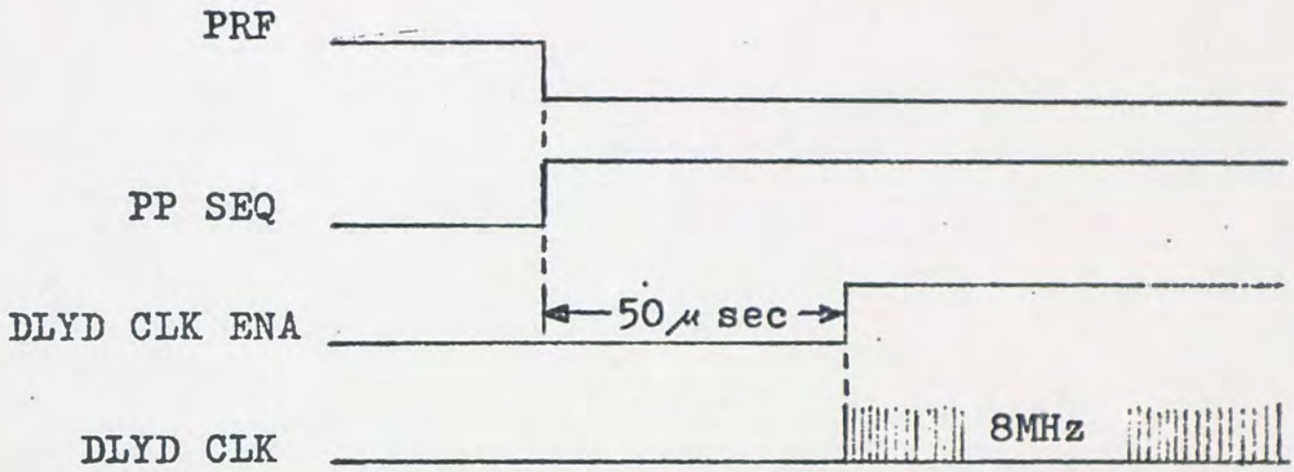


50 μ sec Delay Circuit

Figure 17

The 50 μ sec delay circuit, shown in Figure 17, consists of a divide by 400 counter and a latch. This does not provide an exact 50 μ sec delay but is repeatable, is not subject to increasing error caused by component changes or ageing and is well within target accuracies. Four hundred counts at 8.09127 MHz provides a delay of 49.436 μ sec or 0.564 μ sec $\cong$ .045 nm short of the desired delay. An additional average of one half clock period error (corresponding to -.005 nm) is encountered due to the non-synchronization of the

8 MHz oscillator with the PRF oscillator.



Delayed Clock Timing

Figure 18

The PP SEQ signal holds the counter and latch cleared (RO and R) to zero count until the fall of the PRF oscillator output which begins the sequence. At this time the counters are free to count the 8 MHz clock pulses. Ignoring gate delays, the fall of the 400th clock will toggle the delayed clock enable (DLYD CLK ENA) latch, enabeling the .01 nm increment clock (DLYD CLK) to the distance counter.

The typical gate delay from count input (INP A) to D output (Do) for a 7490 decade counter is given in the manufacturer's data sheets as 65 n sec. The delay from Clock input (CLK) to Q output for a 7473 flip flop is listed as 25 n sec typical. This gives a total delay through the five integrated circuit de-

vices of about 205 n sec which corresponds to adding a delay of approximately +.016 nm. Tabulating the expected errors we have:

SOURCE	ERROR
Oscillator tolerance	± .005%
400 Counts ≠ 50 μ sec	- .045 nm
Asynchronous oscillators	- .005 nm
Gate delays	+ .016 nm

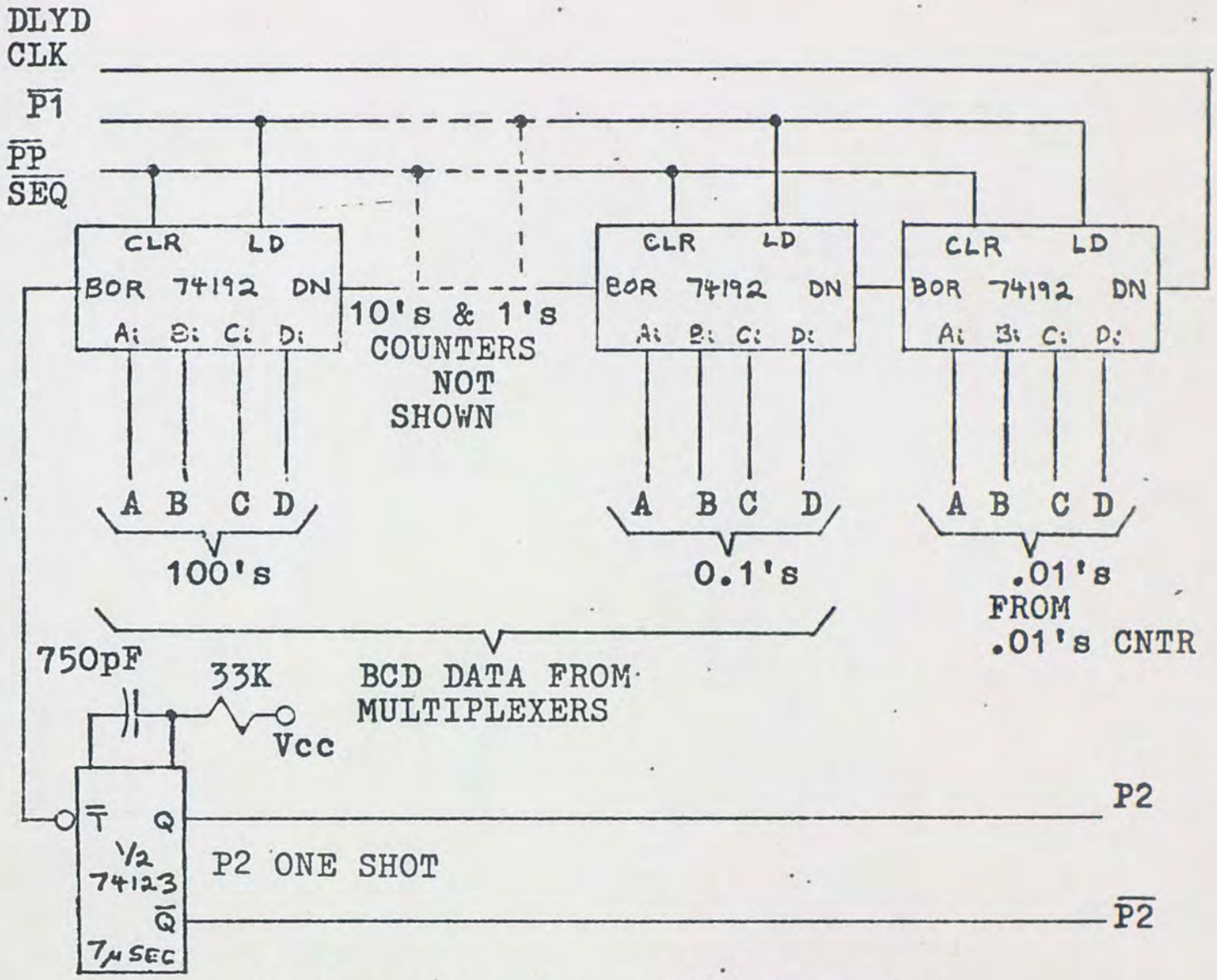
TOTAL ERRORS = - .036 nm ± .005% OF DISTANCE

With the possible error contribution from the 8 MHz oscillator being ± .015 nm at the maximum desired range of 300 nm, the total error from these sources should not exceed - .05 nm which is half the target error of Section 1.2.

3.3.3 DISTANCE COUNTER AND P2 GENERATOR

The distance counter consists of five presettable, up/down, BCD counters wired in cascade to count down with ripple borrows (BOR). The counters are held at zero by the PP SEQ signal on the clear (CLR) inputs until the start of P1. With the removal of the clear input at the start of a pulse pair sequence (PP SEQ), which enables the counters for loading (LD) or counting, P1 loads them with the distance information from the output multiplexers and the hundredths rate counter.

After the 50 μ sec delay the delayed clock (DLYD CLK) increments the counters downward at an 8 MHz (.01

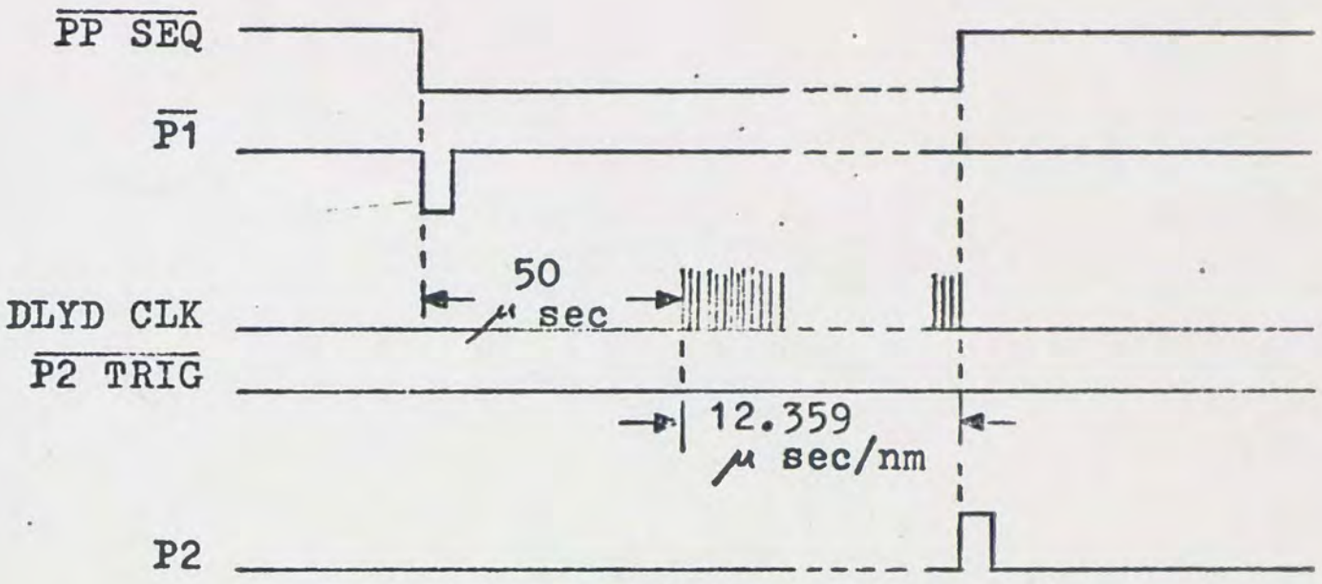


Distance Counter and P2 Generator

Figure 19

nm per period) rate. When the count reaches zero distance, a borror pulse (P2 TRIG) is propagated through all five counters and triggers the P2 one shot. The width of the P2 pulse is set as with the P1 pulse and the timing is shown in Figure 20.

The $\overline{P2}$ pulse is used to reset the PP SEQ flip flop in preparation for the next PRF cycle and the positive going P2 is routed to the output interface circuit.



P2 Timing

Figure 20

The error contributed by this circuitry consists mainly in the delays through the five counters. This delay is specified by the manufacturer to be typically 18 n sec per counter for a total of 90 n sec or about + .007 nm error.

3.3.4 P1/P2 OUTPUT INTERFACE

The function of this circuit is to convert the logic level P1 and P2 pulses into the required shape as specified in Section 2.3. The circuitry and resulting waveshapes are shown in Figure 21. NOR gate A and inverter B OR the pulses together to get the desired pulse pair. The inverter is a high voltage, open collector type (part of the same 7406 package used to drive the inbound and outbound indicator lights) and is pulled up by RL to +14v (a standard voltage in AVIONICS shops).

The value of RL was calculated to provide the nominal 12 volt required amplitude into a 12 K OHM load as a simple voltage divider:

$$\frac{RL + 12K}{14v} = \frac{12K}{12v}$$

$$RL + 12K = 14K$$

$$RL = 2K$$

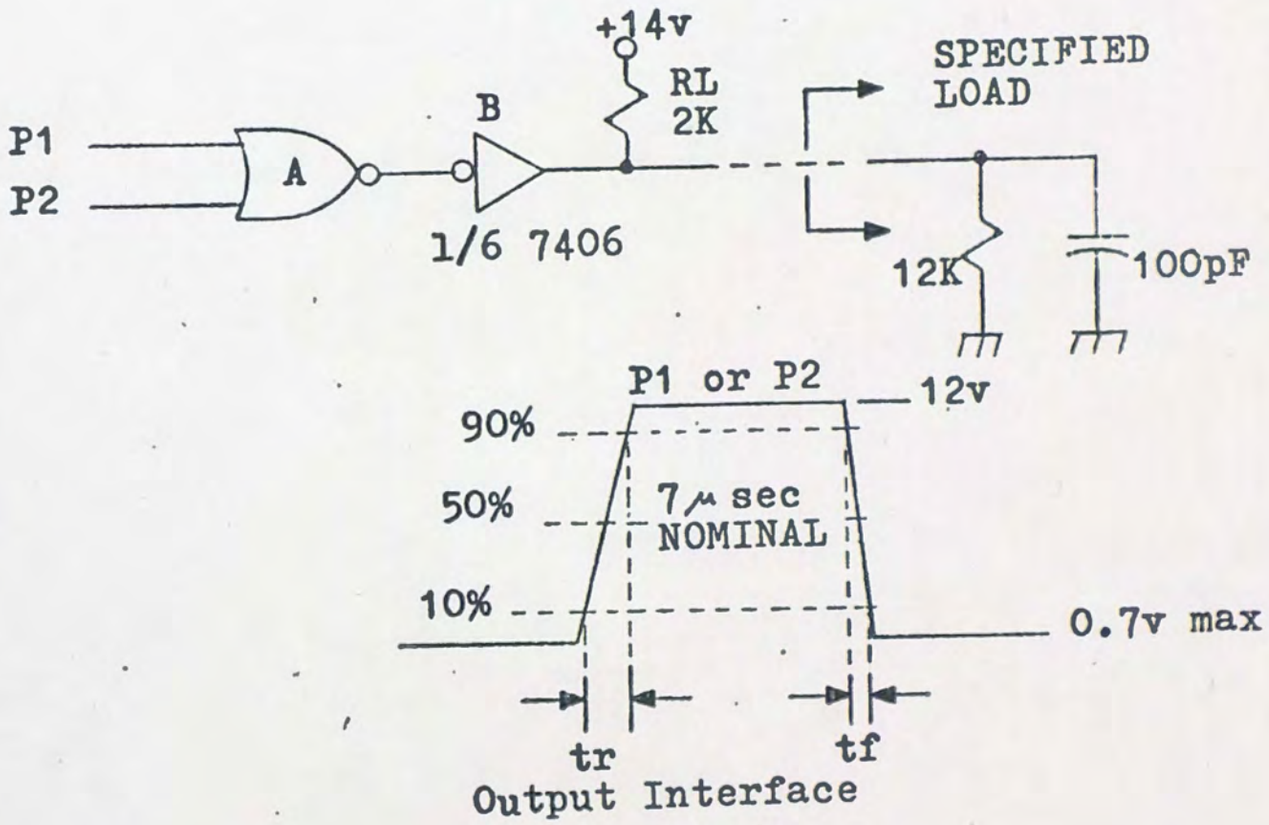


Figure 21

The low voltage output is specified by the manufacturer as 0.7 volts maximum which is within the specified ± 1 v.

The rise time can be predicted by considering the charge time of the 100 pico farad capacitor through the

equivalent charging resistance, Rc.

$$Rc = \frac{(2k)\ (12k)}{2k + 12k} = 1.7k$$

$$t_r = Rc\ C = (1.7 \times 10^3)\ (10^{-10}) = 0.17\ \mu \text{ sec}$$

In 3 time constants the capacitor will be charged to approximately 95% of the final voltage. Therefore, with the rise time being measured between the 10% and 90% amplitude points, the rise time will be less than 3 time constants or about 0.5 μ sec. Which is within the 3 μ sec maximum.

The normal TTL fall time is delayed by the output impedance of the transistor which must discharge the capacitor in a similar fashion. The output impedance of the 7406 gate may be approximated using typical drive current and output voltage specifications from the manufacturer's data sheets.

$$Ro = \frac{0.7v}{40\ ma} = 17.5 \text{ OHMS}$$

$$tf = Ro\ C = (17.5)\ (10^{-10}) = 1.75 \text{ n sec}$$

This becomes insignificant however when compared to the normal 10 to 20 n sec TTL fall time which is likewise insignificant to the allowed 7 μ sec delay time.

The output pulse width will decrease only about 0.5 μ sec from the nominal 7 μ sec one shots when interfaced (the specified width was 7 $\pm$ 3 μ sec) and the pulse

will be identical except for minor pulse width variations related to timing component tolerances.

As the interface is the same for both pulses, this circuit adds no appreciable error to the BCD to pulse pair conversion. Adding the contributions from the 8 MHz oscillator, 50 μ sec delay and the distance counter:

8 MHz OSC and 50 μ sec delay = -.036 nm $\pm$ .005%

Distance Counter = +.007 nm

$$\overline{-.029 \text{ nm} \pm .005\%}$$

We have an accumulated error of -.029 nm $\pm$ .005% of the output distance which is well within our fixed distance accuracy goal of $\pm$ 0.1 nm.

4.0 SYSTEM DESCRIPTION AND OPERATION

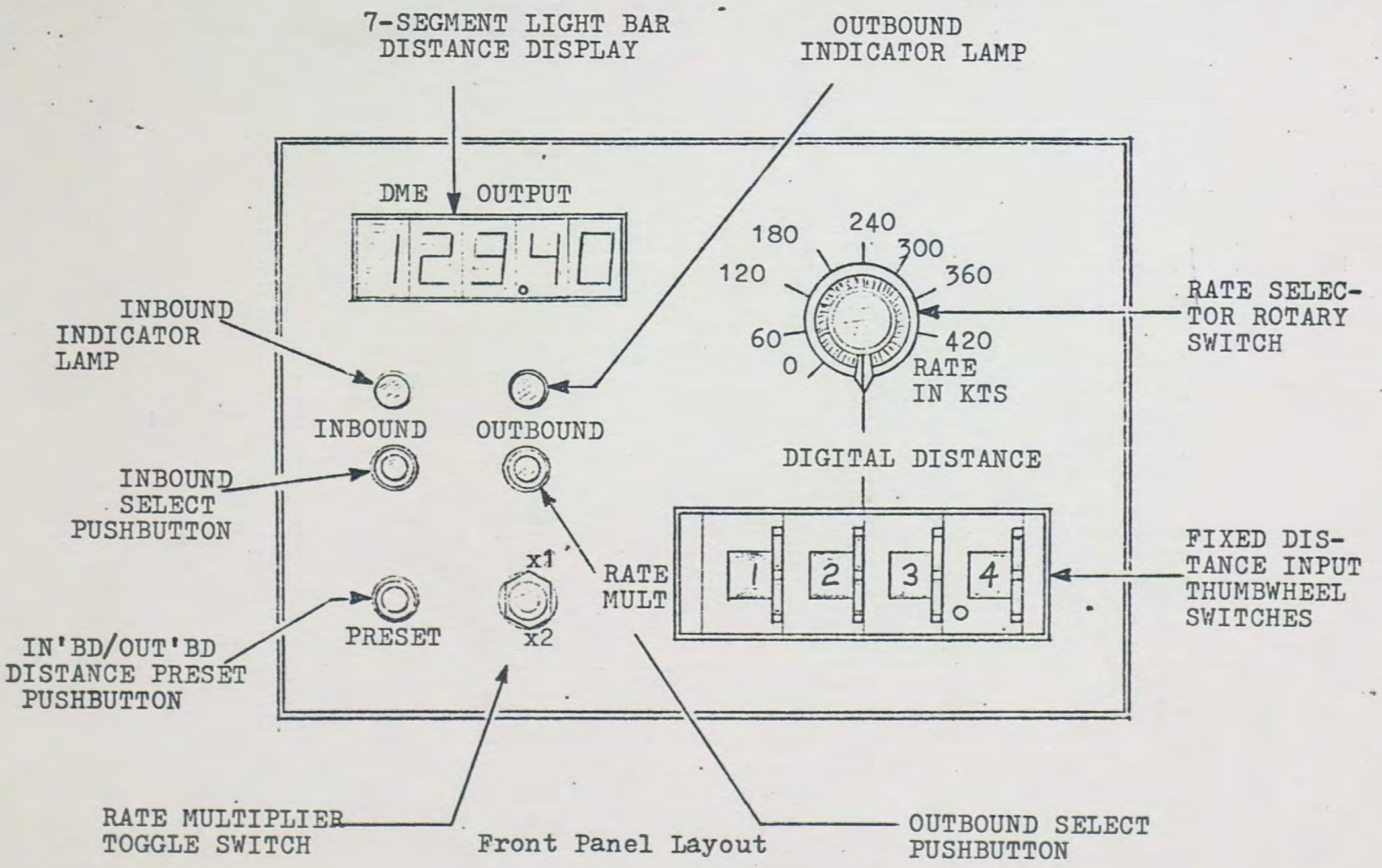
This section describes the functions of the various controls and displays and the operating procedure for the system.

4.1 CONTROL AND DISPLAY FUNCTIONS

Figure 22 shows a typical panel layout for the DME simulator. The functions of the individual controls and displays are described below.

4.1.1 7-SEGMENT DISPLAYS

These are incandescent light-bar displays used to indicate the DME output distance. With the rate selector switch in the digital distance position, the displayed information is the same as the distance selected by the thumbwheel switches. When flying inbound or outbound at



Front Panel Layout

Figure 22

some rate, the display tracks the up/down distance counters to constantly monitor the output DME distance.

4.1.2 INBOUND LAMP

Indicates flying toward the station; will automatically switch to outbound when the distance reaches 0.0 nm.

4.1.3 OUTBOUND LAMP

Indicates flying away from the station.

4.1.4 INBOUND PUSHBUTTON

Selects inbound flight at the closing rate indicated by the rate selector switch.

4.1.5 OUTBOUND PUSHBUTTON

Selects outbound flight.

4.1.6 PRESET PUSHBUTTON

Selects the range at which the aircraft will begin inbound or outbound flight by presetting the up/down distance counters to the distance selected with the thumbwheel switches.

4.1.7 RATE MULTIPLIER SWITCH

Allows selection of twice the rate indicated by the rate selector switch by changing the 140 KHz oscillator divider from ÷100 to ÷50, extending the rate capability to 840 KTS for high speed dynamic testing.

4.1.8 DISTANCE THUMBWHEELS

Select fixed DME distance in 0.1 nm increments.

4.1.9 RATE SELECTOR

Selects either the fixed distance (digital distance position) indicated by the thumbwheel switches as the DME output or the variable distance output from the up/down counters (any position except digital distance) and the rate at which the counters are clocked and therefore the aircraft's inbound or outbound speed. A zero rate position is provided to allow stopping at any distance without having to go to digital distance and reselecting.

4.2 OPERATING PROCEDURE

The system has two basic modes of operation, static and dynamic, for simulating the output of a DME. This section describes the operation of the controls as shown in Figure 22 and described in 4.1 for each of these modes.

4.2.1 STATIC OPERATION

In this mode the simulator puts out a fixed distance pulse pair in 0.1 nm increments. The Rate Selector rotary switch is placed in the Digital Distance position and the thumbwheel switches are set to the desired distance. The 7-segment readout will display the selected distance with the .01's digit indicating a constant zero.

4.2.2 DYNAMIC OPERATION

Aircraft flight inbound or outbound from a selected distance at a selected rate may be simulated by the following procedure. The distance at which the flight is to begin is selected with the thumbwheel switches and

loaded into the rate counters by momentarily depressing the Preset pushbutton. The inbound or outbound direction is chosen by depressing the appropriate switch and will be indicated by the associated indicator lamp. The desired rate is then programmed in with the Rate Selector rotary in conjunction with the Rate Multiplier toggle switch. The output distance will now be updated in .01 nm increments at the selected rate and will be continuously read out on the DME Output display.

5.0 SUMMARY AND CONCLUSIONS

The circuitry was constructed and tested as described and has subsequently been incorporated into general RNAV test sets used in production testing and in the design of new Area Navigation systems. Although the DME simulator has reliably performed its designated tasks, advances in the "state of the art" suggest possible improvements. As of this writing, the author would recommend changes in two areas; the programmable divider and the crystal oscillators.

The three DM8520 programmable dividers could be replaced by two SN7497N 6-bit binary rate multipliers. This would save one chip plus providing simpler programming logic. The device output frequency is equal to the input frequency multiplied by the rate input M and divided by 64, ie.:

$$f_{out} = \frac{M f_{in}}{64}$$

where: $M = F \cdot 2^5 + E \cdot 2^4 + D \cdot 2^3 + C \cdot 2^2 + B \cdot 2^1 + A \cdot 2^0$

Cascading two stages would give a 12-bit divider (10-bits are sufficient for the simulator) with the division encoded in straight binary.

The 140 KHz crystal oscillator could also be simplified by using an oscillator chip such as the MC12060. The only external components required are the crystal and two capacitors. The device works off the 5 volt logic supply and is TTL compatible. Similarly, the 8 MHz oscillator could be constructed using the high frequency version, the MC12061.

Whereas these changes would not affect the functional capabilities of the system they would result in a cost reduction and would simplify the circuitry, making it easier to maintain.

Programmable Counter Encoding

÷By	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12
2	1	1	1	1	1	1	1	1	1	1	1	0
14	0	0	1	0	0	1	0	1	0	1	0	1
26	0	1	1	1	0	1	1	0	0	0	0	1
38	1	0	0	1	1	1	1	1	0	0	1	1
50	0	0	1	0	1	1	1	0	0	1	0	0
62	0	0	1	0	0	0	0	0	0	0	0	0
74	0	0	1	0	0	1	1	0	1	1	1	1
86	1	1	1	1	1	0	0	1	1	0	1	0
98	0	0	1	0	1	0	1	0	0	0	0	1
110	0	1	0	1	0	1	1	1	0	0	1	0
122	1	1	0	0	0	1	1	0	0	0	0	0
134	0	0	0	0	0	1	1	0	1	0	1	1
146	0	0	0	0	0	0	0	0	1	0	1	0
158	1	1	1	0	0	1	1	1	1	1	1	0
170	0	0	1	1	1	1	1	1	1	0	0	1
182	0	1	1	1	0	1	0	0	1	0	1	0
194	0	0	0	0	0	0	0	0	1	0	1	1
206	1	1	0	1	0	0	0	0	0	0	0	1
218	1	1	1	1	0	0	1	0	1	0	0	0
230	0	0	1	0	0	1	0	0	0	0	0	0
242	1	0	1	1	1	0	0	1	1	1	0	1
254	1	1	1	0	0	0	0	0	0	0	0	1
266	1	1	0	0	0	1	1	1	0	0	0	0
278	0	0	1	0	0	0	0	1	0	1	1	1
290	1	0	0	0	0	1	1	0	1	1	0	0
302	0	0	0	1	1	1	0	0	1	0	1	0
314	0	1	1	0	0	0	1	0	0	0	0	0
326	0	0	1	0	0	1	0	0	1	0	0	1
338	0	0	0	0	0	1	1	0	0	0	1	1
350	1	0	0	0	1	0	0	0	1	0	1	1
362	0	1	0	0	0	0	1	0	0	1	0	1
374	1	1	1	0	1	0	1	0	0	1	1	0
386	0	0	0	0	0	1	1	0	1	1	0	1
398	1	0	1	1	0	0	0	0	1	0	1	0
410	0	1	0	0	1	0	0	1	1	0	0	1
422	1	1	0	1	1	1	0	0	0	1	1	0
434	1	1	1	0	0	0	1	1	1	1	1	0
446	1	0	1	0	0	0	0	0	1	0	1	1
458	0	1	1	0	1	1	0	1	0	0	0	1
470	1	1	1	0	1	1	0	1	1	0	1	0

÷By	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12
482	1	0	1	0	0	1	1	0	0	1	0	0
494	1	0	1	1	0	0	1	0	0	1	0	0
506	0	0	1	1	1	1	1	0	0	0	0	1
518	1	1	0	1	1	0	1	1	0	1	1	1
530	0	0	1	0	0	0	1	1	0	1	1	0
542	1	1	1	1	1	1	1	0	1	0	1	0
554	1	1	0	1	1	1	0	1	0	1	1	0
566	1	1	0	0	0	1	0	0	0	0	1	0
578	0	0	1	0	0	1	1	0	1	1	0	1
590	1	0	0	1	0	1	1	0	0	1	0	1
602	1	0	1	1	0	0	0	0	0	0	1	1
614	1	1	1	1	0	1	1	0	0	1	1	1
626	1	0	1	1	0	1	0	0	1	1	0	0
638	0	1	1	0	0	1	1	0	1	0	1	1
650	0	1	1	0	1	0	1	1	1	0	1	0
662	1	1	1	0	1	1	0	1	0	0	0	0
674	0	1	0	0	0	0	0	1	1	0	1	0
686	1	0	0	0	1	1	0	1	1	1	0	1
698	0	1	0	0	1	0	1	0	1	0	1	1
710	1	1	0	1	1	0	1	1	1	1	0	0
722	1	1	1	1	0	0	1	1	0	1	1	1
734	0	0	0	0	1	1	0	0	0	0	1	0
746	1	1	1	1	1	0	0	1	0	1	1	0
758	0	1	1	1	1	1	0	1	1	1	1	1
770	1	1	0	0	0	1	1	0	1	1	0	0
782	0	1	0	1	0	0	0	1	0	1	0	1
794	1	0	0	1	0	0	0	1	0	1	0	0
806	0	1	1	1	0	0	0	0	1	0	1	1
818	1	0	1	0	1	0	0	0	0	1	1	0
830	0	0	0	0	0	1	0	0	1	0	1	1
842	0	1	0	0	1	1	1	1	0	0	1	1
854	1	1	1	0	1	0	1	1	0	0	1	1
866	1	1	0	0	1	0	0	1	0	0	0	1
878	1	1	0	0	1	1	1	1	1	0	0	0
890	1	0	1	0	0	0	0	0	1	1	0	1
902	1	1	0	1	1	1	0	1	0	0	0	1
914	0	1	0	0	0	0	1	1	1	1	0	1
926	0	1	0	0	0	1	0	1	1	0	1	1
938	0	0	1	0	0	1	0	1	0	0	0	0
950	1	0	0	1	1	1	1	0	0	0	0	1
4094	0	0	1	1	1	1	1	1	1	1	1	1

[6]

[6] J. Kalb, National Semiconductor Corp. Applications Note AN-17, Programmable Divider Applications (Santa Clara, Calif.: National Semiconductor Corp., 1968), p.7.

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