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Accumulative Errors in Low-Level MOS-FET Multiplexers

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ACCUMULATIVE ERRORS IN LOW-LEVEL MOS-FET MULTIPLEXERS

BY

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ABSTRACT

ACCUMULATIVE ERRORS IN

LOW-LEVEL MOS-FET MULTIPLEXERS

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This paper provides a brief historical discussion of the development of time division low level multiplexing techniques and especially emphasizes MOS-FET multiplexers currently being implemented. Error sources which may affect system accuracy and therefore must be considered in the design of the multiplexer are described. Some of the more significant of these errors: aliasing, interchannel crosstalk, static offset, transient coupled errors, and common-mode injected errors are analyzed and covered in detail.

Equations expressing the overall interchannel DC crosstalk and static offset for a generalized multiplexer are derived and presented. Settling errors arising from transient events in time division multiplexers are derived for a two channel multiplexer and plotted to illustrate their dependency on the multiplexer input and output capacitances. A multi-tier channel path is also examined for common-mode to differential-mode signal conversion. As a conclusion, the author discusses how these error sources accumulate and gives a means for predicting the overall cumulative average error to be expected from the time division multiplexing equipment.

Approved: Richard C. Harden
Director of Research Report

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INTRODUCTION

The accuracy to which information can be sampled and time-division multiplexed depends on the information rate of the sampled signals, the multiplexer configuration, and the multiplexer switch characteristics. The maximum rate at which a time-division multiplexer can be operated within a given percentage of accuracy is limited by the parameter characteristics of the devices used as the switching elements and how these switches are interconnected to form the multiplexer.

Metal-Oxide semiconductor field-effect transistors (MOS-FET) are predominately used today as the switching element in time-division multiplexing due to their attributes of high OFF impedance and very low leakage currents. Unfortunately, the devices exhibit several parameters which limit the accuracy and speed with which information can be multiplexed. These parameters include ON resistance, input capacitance, output capacitance and the signal levels necessary to switch the device ON or OFF. The errors produced in MOS-FET multiplexer equipment are a result of these parameters and are a function of the data source impedance and output load impedance.

This paper delineates some of the most significant of these error sources, illustrates their data source dependence, indicates how the errors accumulate, and enlightens the reader to the pitfalls which may occur in low-level signal processing.

1. HISTORY OF TIME-DIVISION MULTIPLEXING

In early telemetry systems only a few measurements were performed and each of the transducers were usually hardwired through long cables to a single frequency modulated transmitter. As the art of telemetry instrumentation expanded, a larger number of measurements were required and the type of measurements became more complex.

The instrumentation engineer became faced with the problem of simultaneously monitoring a wide range of static, quasi-static, and dynamic signals representing varying physical parameters of experiments with which he was concerned. To alleviate this increased demand of high volume data gathering, time-division multiplexing (TDM) was developed.

A TDM multiplexer acquires a number of variables from unrelated sources and permits these variables to share common processing and transmission equipment. Variables are sensed by transducers, whose outputs are continuous voltages representing the state of the variables. The most common types of variables are physical phenomena: temperature, stress, strain, acceleration, vibration, etc. The transducer output voltage range of these signals tends to be quite low, typically less than a few hundred millivolts.

Normally signal processing equipment requires high level signal ranges, typically zero to five volts; therefore, signal conditioning amplifiers are required to adapt the transducer outputs for processing. A substantial savings in size and cost can be achieved if the transducer outputs are multiplexed and then signal conditioned by a single amplifier as compared to signal conditioning prior to multiplexing, which requires an amplifier for each signal input. Hence, the need arises for accurate

low-level multiplexing. Low level multiplexing equipment may be single-ended, but usually consists of two or more parallel signal paths. The single-ended type is the simplest and requires the least hardware; however, it can not differentiate between coupled noise and the sampled signal. Therefore, differential sampling (the difference between two parallel signal paths) is required to preserve the high common-mode rejection necessary in high noise environment.

Various types of devices have been utilized as the switch element in TDM multiplexer equipment to date. Earlier multiplexers employed mechanical switches, such as crossbar scanners and relays; however, they had the disadvantages of limited sampling speed, bulky size and they were not particularly suited for airborne environments. Solid state devices marketed in the late 1950's and early 1960's such as the diode bridge, Bright switch and PINCH transistor were used and proven quite successful. In 1960, junction-field effect transistor (J-FET) semiconductors were introduced for multiplexer switch applications. In particular they were well suited for signal multiplexing because they did not have an inherent voltage offset as their counterpart, the bipolar transistor. The J-FET did not require transformers to achieve high isolation between the input and the switch drive circuitry, and therefore was not duty cycle limited. J-FET's, on the other hand, did have a disadvantage of turning-off due to transients being coupled from the source to the gate.

Later in the 1960 s, metal-oxide semiconductor field effect transistors (MOS-FET) became available. The MOS-FET switch had the same basic advantages as the J-FET switch and furthermore exhibited a much higher isolation from the input (source or drain) terminal to the gate terminal and required simpler drive circuitry. MOS-FET's were also

adaptable to monolithic integrated circuits with relative ease, which resulted in still greater reduction in cost, size, and weight of TDM multiplexers.

Today, MOS-FET's can be purchased as single devices, as monolithic dual devices or as monolithic multi-channel devices having from four to sixteen channels available. A few MOS-FET multiplexers presently available have the associated gate drive circuitry and decode logic designed into the same integrated circuit package.

2. ERROR SOURCES

No measurement is without error. In the design or selection of any instrumentation system, there are many interrelated parameters affecting the system accuracy, all of which must be taken into consideration. Too often the signal source or transducer loading effects on the data multiplexer being employed are not well understood by the instrumentation engineer, and therefore inadequately specified. This is also true of the interconnect cabling between the transducer and multiplexer.

Figure 1 illustrates a simple diagram of a data channel which enumerates the pertinent error sources that must be considered in the design of a TDM multiplexer. The transducer transforms the measurement parameter into a continuous voltage which, prior to being sampled and time-division multiplexed, may be signal conditioned with a band-limited filter network. (Amplifiers also may be included as part of the signal conditioning.) In the process of data multiplexing multi-signal sources, sampling errors occur because of insufficient sampling rates or multiplexer transfer inaccuracies. Multiplexer transfer inaccuracies often limit the sampling rates which can be achieved.

Transfer inaccuracy of a multiplexer channel arises from non-idealistic switch parameters: finite ON resistance, finite OFF isolation, leakage currents, and shunt capacitance, etc. Errors resulting from these non-idealistic parameters include static offset, dynamic settling, transient coupled charge, crosstalk, scatter, common-mode noise, etc. Many of these sources of error are input data source impedance dependent. For example, leakage currents flow out of the channel input of the multiplexer and through the source resistance (transducer or signal conditioner) producing an undesirable biasing potential drop called back-current

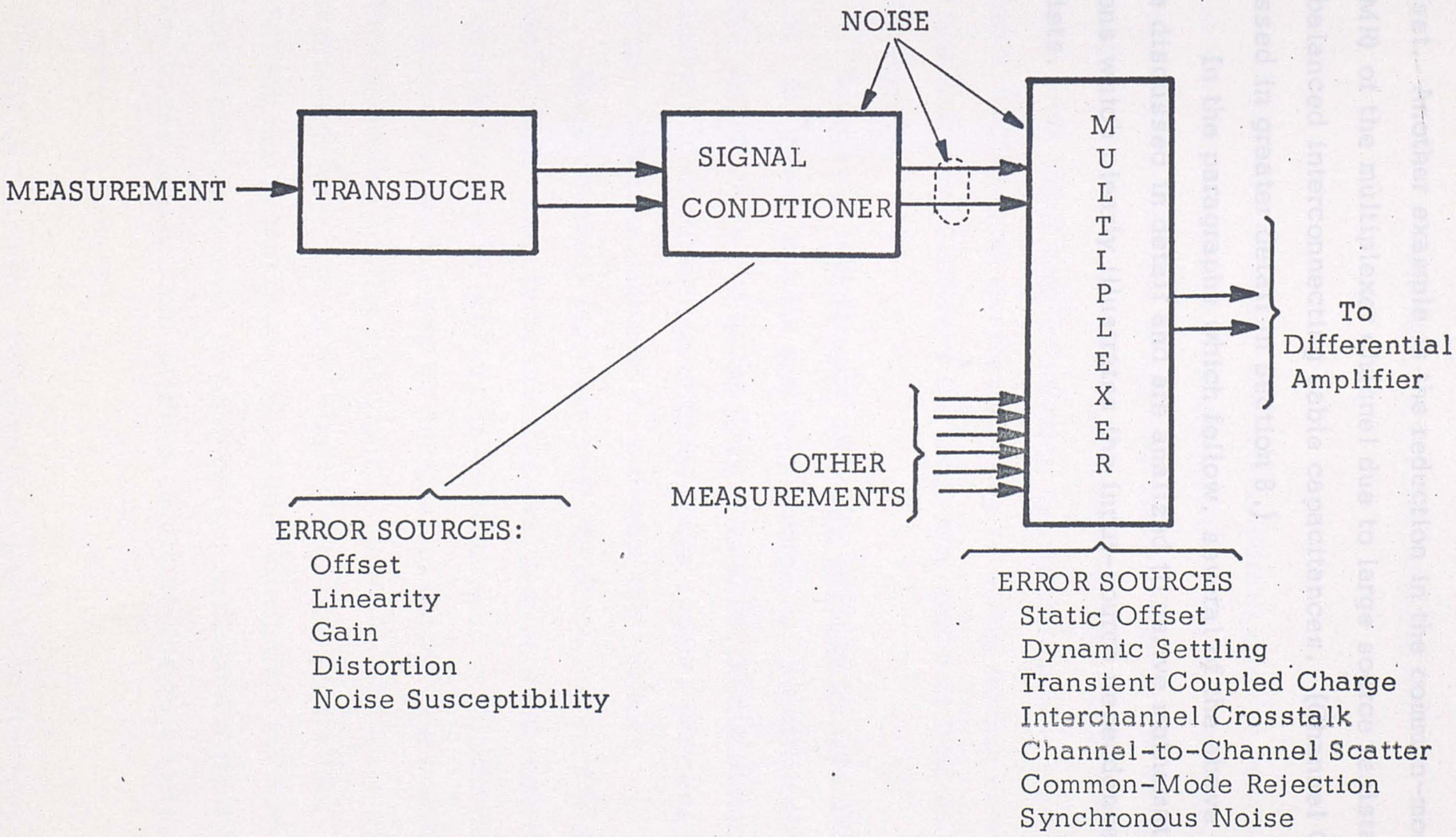

Figure 1. -- Typical differential-ended data channel and associated error sources.

offset. Another example is the reduction in the common-mode rejection (CMR) of the multiplexer channel due to large source resistances and unbalanced interconnecting cable capacitances. (Channel CMR is discussed in greater detail in Section 8.)

In the paragraphs which follow, several of the above error sources are discussed in detail and are analized to derive mathematical expressions which clearly illustrates the input-source dependence, if it exists.

3. SPURIOUS INTERFERENCE

A problem requiring major consideration in the design of any instrumentation system is electrical interference. By definition, electrical interference is any electrical energy in the system which is unrelated to the desired signal information and which degrades the precision with which that information can be detected at the system output.[1] Electrical interference may be either random or periodic in nature and may encompass the frequency spectrum from audio to radio frequencies.

Sources of interference are many and may include DC power circuits, AC power circuits and their harmonics, thermoelectric generators, switching devices and in the case of aircraft, static surface potential discharge. Identification of these noise sources provides the basis for design techniques employed to minimize their effects.

There are three principle methods which are used to reduce interference: first, the source of noise can be minimized; second, the mode of energy transfer or pickup can be attenuated or eliminated; and third, the measuring device may be designed to incorporate maximum noise rejection to the interference signal. Normally, all three of these methods are required when low-level signals are being processed. Adequate shielding and proper grounding usually eliminate a majority of these interferences; however, in some cases, additional attention must be given to the channel and amplifier rejection characteristics.

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[1]Frank J. Oliver, Practical Instrumentation Transducers, (New York: Hayden Book Company, Inc., 1971), p. 290.

The type of cabling used to connect the transducer or signal conditioner to the multiplexer and how the cable is shielded and grounded are particularly critical in low-level signal processing. For example, single wire channels provide no rejection to the interference once the undesired interference is coupled to the line. On the other hand, a differential channel (one having two signal paths) can provide a high degree of rejection to the coupled noise if the noise is equally common to both sides of the channel (common-mode signal).

Low-level signal processing systems are particularly susceptible to interference signals; therefore, differential signal techniques are almost exclusively employed. Balancing of the channel signal paths, isolation of the channel from signal ground, or both, then become significant as to how much rejection of the undesirable interference is achievable.

A balanced differential channel is one in which both signal paths are electrically identical and are symmetrical with respect to the common reference point. In the balanced configuration, each of the two signal paths provides identical signal processing and therefore no net difference (common-mode to differential-mode conversion) occurs for common-mode type noise. However, if the channel is not balanced, common-mode to differential-mode conversion does occur and is dependent on both the degree of channel unbalance and the magnitude of channel impedances. (This subject is treated in some detail in a later section.) To achieve any further increase in noise rejection, the effects of the shunt impedances of the channel must be minimized by making them sufficiently large so that the unbalance becomes insignificant. This minimization is accomplished by isolating the channel transmission paths from the

common interference signal by shielding the channel. The shield, which surrounds both signal transmission paths, provides an auxiliary shunt or short-circuit path for the interference currents to return to the ground terminal of the interference source without entering the signal transmission paths.

In multiplexer applications this approach requires switching the channel shield or guard as well as the channel, thus increasing the physical size of the multiplexer. Hence, guarding is not normally employed except where common-mode rejection of greater than 120db is required.

4. ALIASING

In the process of reconstruction of sampled data, there is the possibility of introducing errors known as aliasing errors. Aliasing is a measurement error which is introduced when a continuous function is sampled periodically and then reconstructed by interpolation filtering or mathematical analysis of the samples. The value of the data sampled represents the data during the time of sampling, except for the measurement error; however, the difficulty arises in predicting the value of the data in between samples.

The Sampling Theorem[2] developed by Shannon states that the data between sampling periods can be reconstructed in an ideal system if the data does not contain spectral components greater than one-half the sampling rate. The minimum sampling rate (twice the highest frequency component in the band limited signal) is often referred to as the Nyquist rate. This theorem is often interpreted in terms of bandwidth--the sampling frequency (f_s) being twice the bandwidth. This interpretation is true of course, for a data source having frequency components no greater than one-half the sampling frequency or a data source filtered with an ideal filter having a cutoff frequency equal to or less than one-half the sampling frequency. However, in a practical system, true ideal bandwidth limited data signals cannot be achieved. Therefore, some data signal frequencies exist higher than one-half the sampling frequency. The energy associated with these higher

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[2]Leonard S. Schwartz, Principles of Coding, Filtering, and Information Theory, (Baltimore: Spartan Books, Inc., 1963), p. 81.

frequencies causes an error to appear in the recovered data. This error phenomenon is known as aliasing.

Aliasing errors are primarily dependent upon the sampling rate and the input data spectrum, but are independent of the amplitude probability distribution of the data.[3] A significant reduction in aliasing errors (less than one percent) can be achieved, as demonstrated by Stiltz,[4] if the sampling frequency is choosen to be ten times the data frequency half-power point and the data is attenuated by at least eighteen db per octave above the data's cutoff frequency.

Caution should be taken by the engineer when assigning high sampling rates in order to minimize aliasing errors. This conservative approach often carries with it performance penalties of higher imposed error throughout the measurement system due to an increase in the spectrum bandwidth of the sampler.

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[3]D. G. Childers, "Study and Experimental Investigation on Sampling Rate and Aliasing in Time-Division Telemetry Systems," IRE Transactions on Space Electronics and Telemetry, XII (December, 1962), pp. 267-283.

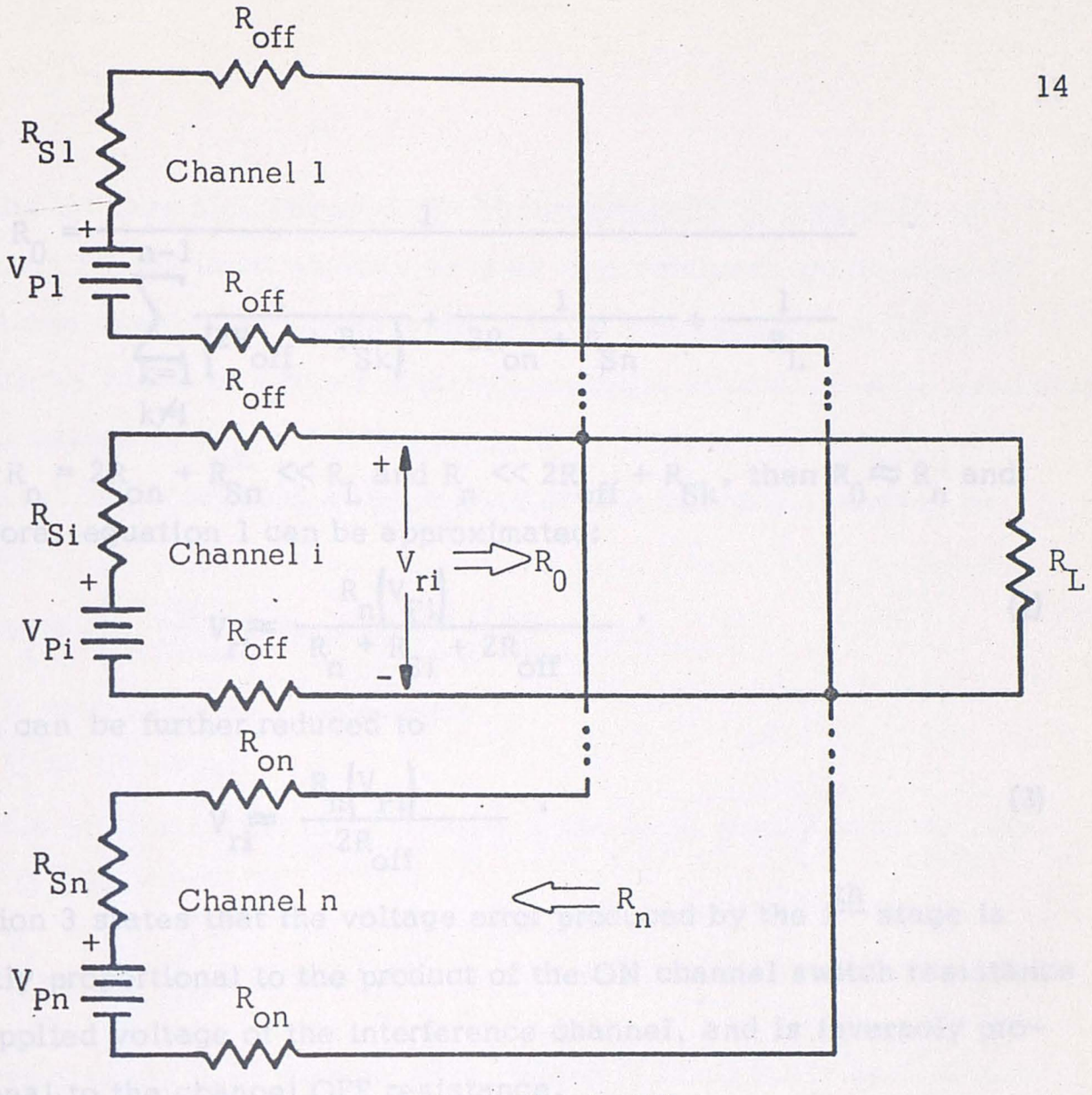
[4]Harry L. Stiltz, Aerospace Telemetry, (Englewood Cliffs, N. J.: Prentice-Hall, Inc., 1961), p. 90.

5. INTERCHANNEL CROSSTALK

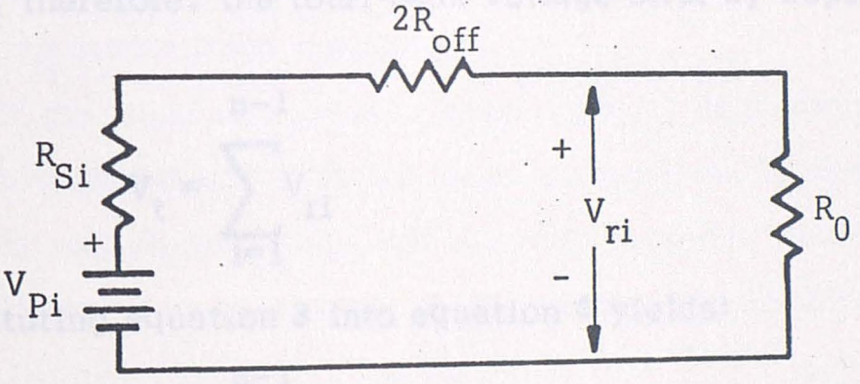
Crosstalk is defined as the interference of one channel caused by interaction with another channel. Crosstalk is referred to often as signal feed-through. Signal feed-through is a signal that is transferred through an OFF channel impedance causing an error in another ON channel. There are other types of crosstalk errors other than signal feed-through errors. As will become apparent later, crosstalk is also the result of residual stored charge on a multiplexer's output capacitance. Another form of crosstalk arises from charge transfer of gate signal through the gate-to-drain capacitance. (See Transient Coupled Errors, Section 7.) The remainder of this section is concerned with the first type--direct crosstalk or signal feed-through.

Figure 2 is a simplified multiple switch circuit where all the channel switches are OFF (open) except channel "n". V_{Pi} represents the peak voltage of the input voltage source of the $i^{\underline{th}}$ stage and R_{Si} represents the input source resistance of the $i^{\underline{th}}$ stage. The voltage error V_{ri} due only to the $i^{\underline{th}}$ stage is determined by replacing all the voltage sources other than V_{Pi} with a short circuit and calculating the voltage produced across the output:

$$V_{ri} = \frac{R_0 V_{Pi}}{R_0 + R_{Si} + 2R_{off}}, \qquad (1)$$



(a) Multiple switch circuit -- channel n is ON.



(b) Simplified circuit with all voltage sources replaced with short-circuit except V_{Pi}.

Figure 2 -- Equivalent circuit of multiple switch network for calculation of direct crosstalk.

where $R_0 = \dfrac{1}{\sum_{\substack{k=1 \\ k\neq i}}^{n-1} \dfrac{1}{(2R_{off} + R_{Sk})} + \dfrac{1}{2R_{on} + R_{Sn}} + \dfrac{1}{R_L}}$.

Since $R_n = 2R_{on} + R_{Sn} \ll R_L$ and $R_n \ll 2R_{off} + R_{Sk}$, then $R_0 \approx R_n$ and therefore, equation 1 can be approximated:

$$V_{ri} \approx \frac{R_n(V_{Pi})}{R_n + R_{Si} + 2R_{off}} , \tag{2}$$

which can be further reduced to

$$V_{ri} \approx \frac{R_n(V_{Pi})}{2R_{off}} . \tag{3}$$

Equation 3 states that the voltage error produced by the $i^{\underline{th}}$ stage is directly proportional to the product of the ON channel switch resistance and applied voltage of the interference channel, and is inversely proportional to the channel OFF resistance.

There are (n-1) unselected switches and all are approximately equal; therefore, the total peak voltage error by superposition is the sum:

$$V_t = \sum_{i=1}^{n-1} V_{ri} \tag{4}$$

Substituting equation 3 into equation 4 yields:

$$V_t \approx \frac{1}{2} \sum_{i=1}^{n-1} \frac{R_n}{R_{off}} (V_{Pi}) \tag{5}$$

the total peak voltage error.

As an example, suppose the circuit consists of a bank of 16 gates and all the input sources have 40 millivolt peak static signals except one unselected source which has an overvoltage condition of 28 volts -- which in aircraft is a very realistic situation. Also assuming typical values of R_{off} = 1,000Mohms, R_{Si} = 1000 ohms, and R_{on} = 200 ohms, the total peak voltage error of this example computes as follows:

$$V_t \approx 7\left(\frac{1.4K\Omega}{1000M\Omega}\right)40mV + \frac{1}{2}\left(\frac{1.4K\Omega}{1000M\Omega}\right)28V,$$

or $V_t \approx 0.39\mu volts + 19.5\mu volts,$

or $V_t \approx 20\mu volts.$

The ratio of this output error voltage to the input peak signal voltage, which is also 40mV, is

$$\frac{V_t}{V_{Pn}} = \frac{20\mu V}{40mV} = 0.5 \times 10^{-3}$$

or approximately 0.05 percent error, which is due almost exclusively to the overvoltage channel. Normally, as illustrated by this example, direct crosstalk in a small array MOS-FET multiplexer is not significant except in overvoltage conditions.

If the input data source types consist of dynamic signals, then the above model and analysis must be modified to account for the multiplexer's switch reactance and the multiplexer's internal stray reactance. The technique presented above, however, is still valid.

6. STATIC OFFSET

Static offset errors in MOS-FET multiplexers occur because of leakage currents of the MOS-FET devices and amplifier bias currents. These currents flow through the ON resistance of the switches producing a voltage drop across the source-drain terminals of the device, thus producing an offset voltage.

If the offset voltages of all channels throughout the multiplexer are identical, then the offset can be treated as an insertion loss which can be compensated for by increasing the gain of the post-amplification stage. Unfortunately in real systems it is impossible to compensate for all of the offset because of variations in ON resistance and leakage currents from one device to the next. Achieving perfect compensation is complicated by the fact that both ON resistance and leakage currents are functions of bias voltages and temperature.

Toney[5] has previously computed the static offset error for a four tier J-FET multiplexer. Here the static offset error will be computed for a more generalized MOS-FET multiplexer model having "n" tiers. The single-ended multiplexer illustrated in Figure 3 will be used in the analysis, and the differential multiplexer configuration obtained by taking the difference between two of these singled-ended multiplexers. The model employs the technique of tiering which is also referred to as pyramiding, treeing and subcommutating. Tiering minimizes the offset due to

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[5]Phillip A. Toney, "Design Considerations for Differential Low Level Junction Field Effect Transistor Commutators," IEEE Transactions on Aerospace and Electronic Systems, Vol. AES-3, No. 6, November, 1967, pp. 871-898.

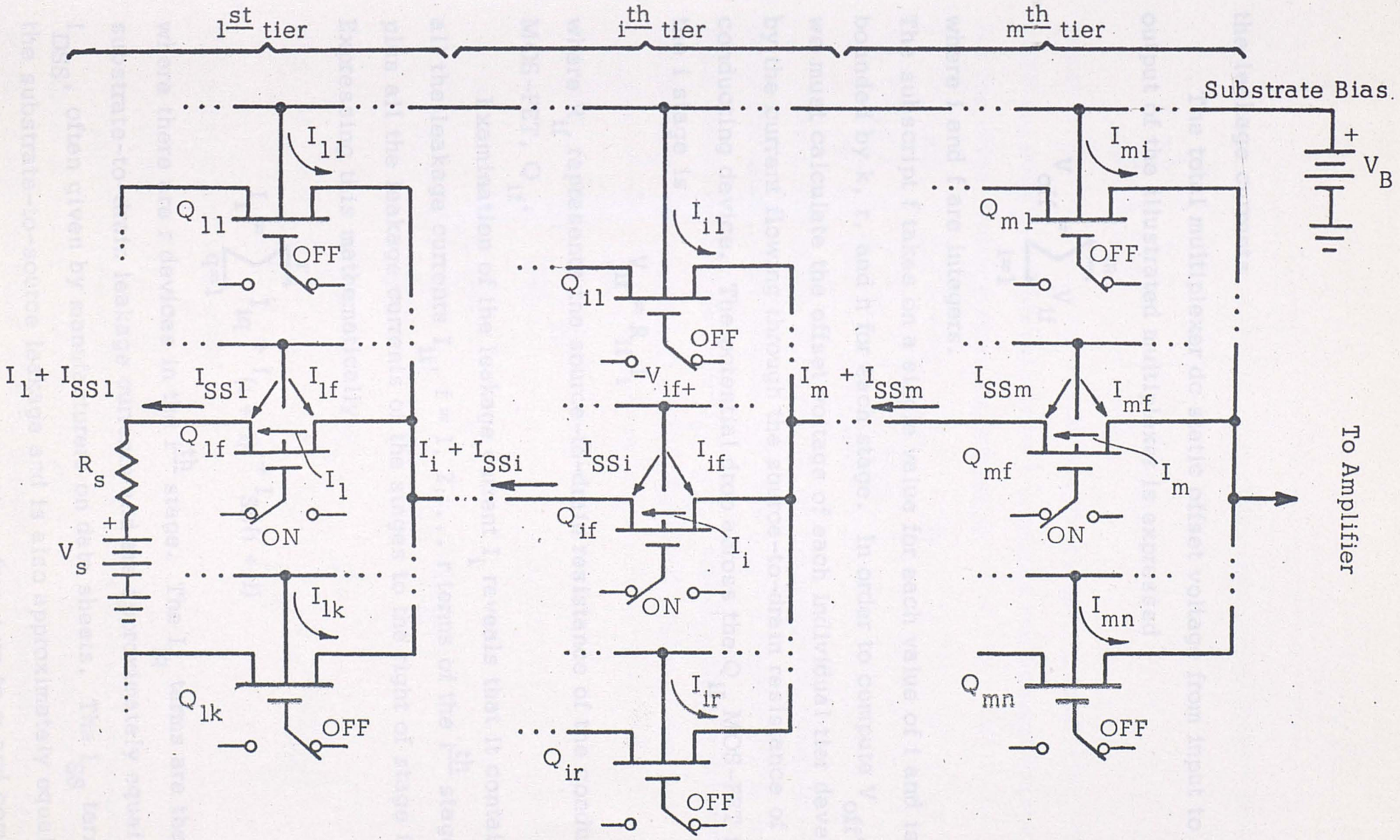


Figure 3. -- Generalized MOS-FET multiplexer for calculation of static offset.

the leakage currents.

The total multiplexer dc static offset voltage from input to output of the illustrated multiplexer is expressed

$$V_{off} = \sum_{i=1}^{m} V_{if} \tag{6}$$

where i and f are integers.

The subscript f takes on a single value for each value of i and is bounded by k, r, and n for each stage. In order to compute V_{off}, we must calculate the offset voltage of each individual tier developed by the current flowing through the source-to-drain resistance of the conducting device. The potential drop across the Q_{if} MOS-FET in the i stage is

$$V_{if} = R_{if} I_i \tag{7}$$

where R_{if} represents the source-to-drain resistance of the conducting MOS-FET, Q_{if}.

Examination of the leakage current I_i reveals that it contains all the leakage currents I_{if}, f = 1, 2, ... r terms of the $i^{\underline{th}}$ stage plus all the leakage currents of the stages to the right of stage i. Expressing this mathematically,

$$I_i = \sum_{q=1}^{r} I_{iq} + I_{(i+1)} + I_{SS(i+1)} \tag{8}$$

where there are r devices in the $i^{\underline{th}}$ stage. The I_{iq} terms are the substrate-to-drain leakage currents and are approximately equal to I_{DSS}, often given by manufacturers on data sheets. The I_{SS} term is the substrate-to-source leakage and is also approximately equal to I_{DSS}. Summing all the current equations from i up to m and combining

them yields:

$$I_i = \sum_{p=i}^{m} \left[\sum_{q=1}^{k,r,\ldots n} I_{pq} \right] + \sum_{p=i+1}^{m} I_{DSS\,p} \qquad (9)$$

where k, r, ..., n is the respective range of q for each tier. Substituting equation 9 into equation 7 produces the general expression for the offset voltage across each stage:

$$V_{if} = R_{if} \left[\sum_{p=i}^{m} \left(\sum_{q=1}^{k,r,\ldots n} I_{pq} \right) + \sum_{p=i+1}^{m} I_{DSS\,p} \right] \qquad (10)$$

For clarification of this equation the following example of a three tier multiplexer where m = 3, k = 8, r = 6, and n = 4 is presented. Also, assuming that devices Q_{15}, Q_{23}, and Q_{31} are the conducting MOS-FET's, the tier offset voltages are:

$$V_{31} = R_{31} \sum_{q=1}^{4} I_{3q};$$

$$V_{23} = R_{23} \left[\sum_{q=1}^{6} I_{2q} + \sum_{q=1}^{4} I_{3q} + I_{DSS} \right];$$

and $$V_{15} = R_{15} \left[\sum_{q=1}^{8} I_{1q} + \sum_{q=1}^{6} I_{2q} + \sum_{q=1}^{4} I_{3q} + 2I_{DSS} \right].$$

The total offset from equation 6 is:

$$V_{offset} = V_{31} + V_{23} + V_{15}$$

Typical values of leakage currents for MOS-FET devices are in the order of 0.1 to 1 nanoampere and their ON resistance 150 to 250 ohms. Using the upper limit on current and resistance and assuming that all the leakage currents are equal and all ON resistances are equal,

the voltage offsets for the above example is computed as

$$V_{31} = (250\Omega)(4)(1\text{nA}),$$

$$V_{23} = (250\Omega)(11)(1\text{nA}),$$

$$V_{15} = (250\Omega)(20)(1\text{nA}),$$

and the total maximum voltage offset is the sum:

$$V_{off(A)} = (250\Omega)(35)(1.0\text{nA}) = 8.75\ \mu\text{volts}.$$

Similarly the total minimum offset expected is computed for the minimum values of current and resistance listed above to be

$$V_{off(B)} = (150\Omega)(35)(0.1\text{nA}) = 0.53\ \mu\text{volts}.$$

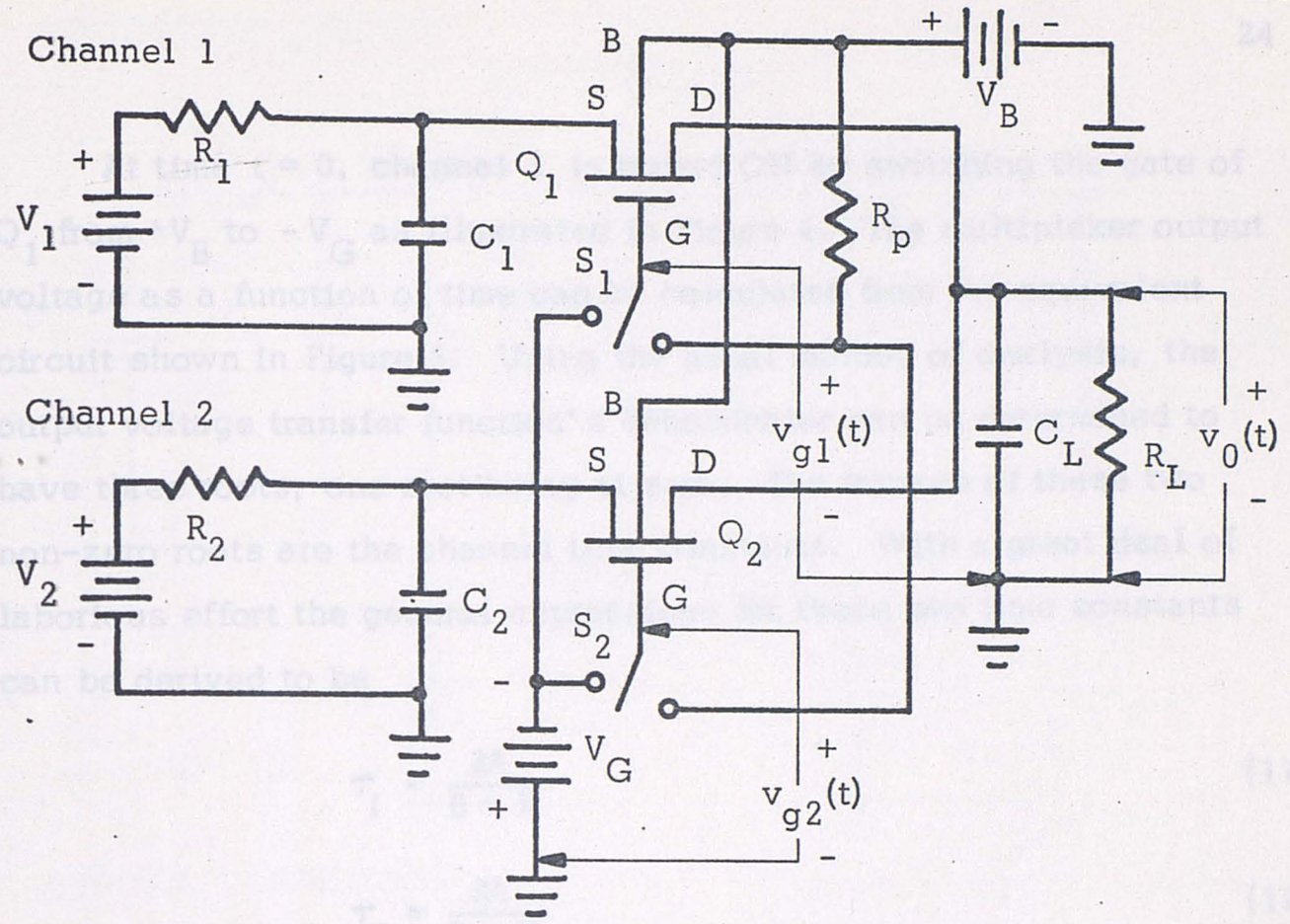
Hence taking the difference, $V_{off(A)} - V_{off(B)}$, the worst-case offset for the differential channel is approximately eight microvolts.

For a forty millivolt full-scale input signal source, the eight microvolts offset error would produce 0.02% error. Normally, the average of the sum of the individual channel voltage offsets is labeled the "multiplexer voltage offset error". The deviation of each channel offset from the average is termed the multiplexer scatter error (channel-to-channel scatter).

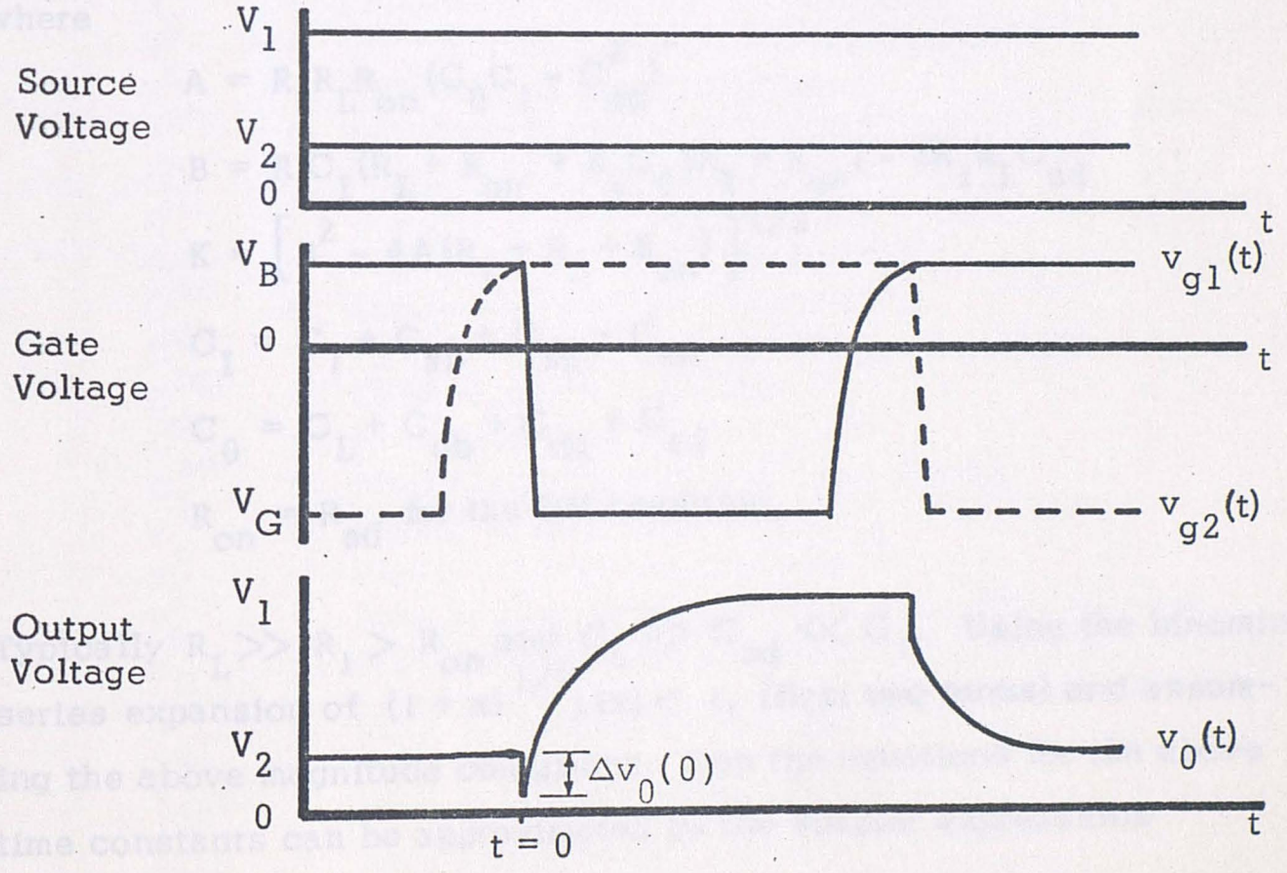
7. TRANSIENT COUPLED ERRORS

Whenever one channel of a multiplexer is switched OFF and another channel is switched ON, transient errors occur. These transient errors are a result of two events. One is due to voltage signals being coupled from the gate control circuit through the drain-to-gate and the source-to-gate capacitances to the switch's drain and source terminals. The other is due to the transfer of energy between the multiplexer input capacitance and the multiplexer output capacitance. The magnitude of the transient voltages fedthrough are a function of the channel input and output capacitances and the gate capacitances. These transient voltages coupled to the channel signal path will cause errors in the sampled data, if sufficient settling time is not available. The settling time is a function of the switch's time constants and it is usually defined to be the time required for the output voltage to settle to within a specified percent of the input signal voltage each time a new channel is switched ON.

To illustrate more clearly the effects of these transient events the two channel multiplexer shown in Figure 4 will be considered. Prior to the multiplexer being switched, channel 2 is assumed to be ON and the multiplexer output voltage, $v_0(t)$ equals the channel 2 input voltage, V_2. Channel 2 is then switched OFF allowing for break-before-make switching to prevent shorting channel 2's input data source to channel 1's input data source during the transition state. The rise time at the gate of MOS-FET Q_2 is assumed to be sufficiently slow, so that the multiplexer output voltage remains at the potential V_2.



(a) Two channel single-ended MOS-FET multiplexer



(b) Time relation of signal waveforms

Figure 4. -- Two channel multiplexer and control timing signal waveforms

At time t = 0, channel 1 is turned ON by switching the gate of Q_1 from $+V_B$ to $-V_G$ as illustrated in Figure 4. The multiplexer output voltage as a function of time can be calculated from the equivalent circuit shown in Figure 5. Using the nodal method of analysis, the output voltage transfer function's denominator can be determined to have three roots, one root being at zero. The inverse of these two non-zero roots are the channel time constants. With a great deal of laborious effort the general expressions for these two time constants can be derived to be

$$\tau_1 = \frac{2A}{B + K} \tag{11}$$

$$\tau_2 = \frac{2A}{B - K} \tag{12}$$

where

$$A = R_1 R_L R_{on} (C_0 C_I - C_{sd}^2)$$

$$B = R_1 C_I (R_L + R_{on}) + R_L C_0 (R_1 + R_{on}) - 2R_1 R_L C_{sd}$$

$$K = \left[B^2 - 4A(R_1 + R_L + R_{on}) \right]^{1/2}$$

$$C_I = C_1 + C_{sb} + C_{sg} + C_{sd}$$

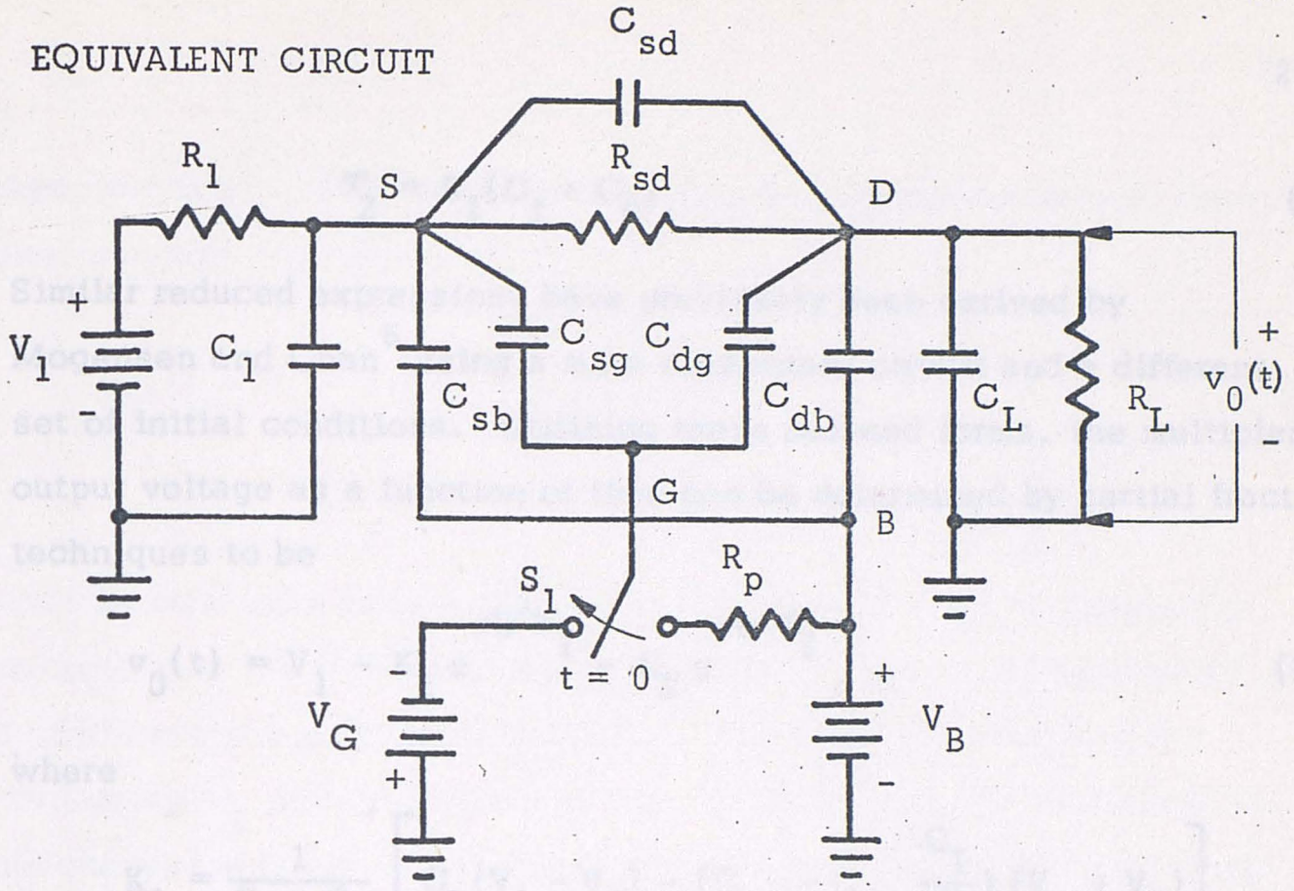
$$C_0 = C_L + C_{db} + C_{dg} + C_{sd}$$

$R_{on} = R_{sd}$ for the ON condition.

Typically $R_L >> R_1 > R_{on}$ and $C_L >> C_{sd} << C_1$. Using the binominal series expansion of $(1 + x)^{1/2}$; $|x| < 1$, (first two terms) and assuming the above magnitude conditions, then the equations for the above time constants can be approximated by the simpler expressions

$$\tau_1 = R_{on} C_I C_0 / (C_I + C_0) \tag{13}$$

EQUIVALENT CIRCUIT



SYMBOL DEFINITIONS

R_1	=	Channel 1 input source resistance
R_2	=	Channel 2 input source resistance
R^p	=	Gate-to-substrate pullup resistance
R_{sd}	=	MOS-FET channel resistance
R_L	=	Multiplexer output load resistance
C_1	=	Channel 1 input capacitance
C_2	=	Channel 2 input capacitance
C^{sb}	=	Source-to-substrate capacitance
C^{db}	=	Drain-to-substrate capacitance
C^{sg}	=	Source-to-gate capacitance
C^{dg}	=	Drain-to-gate capacitance
C^{sd}	=	Source-to-drain capacitance
C_L	=	Multiplexer output load capacitance
V_1	=	Signal voltage into channel 1
V_2	=	Signal voltage into channel 2
V_B	=	Bias voltage to substrate of MOS-FET switches
V_G	=	Bias voltage switched to gate of MOS-FET switches
$v_{g1}(t)$	=	Gate 1 control voltage signal
$v_{g2}(t)$	=	Gate 2 control voltage signal
$v_0(t)$	=	Multiplexer output voltage

Figure 5. -- Circuit model and symbol definitions.

$$\tau_2 = R_1(C_I + C_0) \tag{14}$$

Similar reduced expressions have previously been derived by Mogensen and Chan[6] using a more elementary circuit and a different set of initial conditions. Utilizing these reduced forms, the multiplexer output voltage as a function of time can be determined by partial fraction techniques to be

$$v_0(t) = V_1 - K_1 e^{-t/\tau_1} - K_2 e^{-t/\tau_2} \tag{15}$$

where

$$K_1 = \frac{1}{C_I + C_0}\left[C_I(V_1 - V_2) - (C_{sg} - C_{dg}\frac{C_I}{C_0})(V_G + V_B)\right]$$

$$K_2 = \frac{1}{C_I + C_0}\left[C_0(V_1 - V_2) + (C_{sg} + C_{dg})(V_G + V_B)\right]$$

From equation 15 we can draw the following conclusions. Upon initial closure of the multiplexer switch device Q_1, at $t = 0$, the output voltage $v_0(t)$ initially decreases by the amount

$$\Delta v_0(0) = \frac{C_{dg}}{C_0}(V_G + V_B) \tag{16}$$

For time $t > 0$ the output voltage $v_0(t)$ charges exponentially towards the input source potential V_1, as a function of the two time constants, τ_1 and τ_2. Immediately after the channel turns ON a portion of the energy stored on the input capacitance, C_I, is transferred to the output

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[6]Per Mogensen and Wallace Chan, "MOS multiplexer switches can do well at high frequencies," Electronics, November 11, 1968, pp. 152-156.

capacitance C_0. This charge transfer occurs exponentially with the time constant τ_1. For $t \gg \tau_1$

$$v_0(t) = V_1 - \frac{1}{C_I + C_0}\left[C_0(V_1 - V_2) + (C_{sg} + C_{dg})(V_G + V_B)\right] e^{-t/\tau_2} \quad (17)$$

At this point in time the output voltage $v_0(t)$ is predominately controlled by the time constant τ_2 and will charge to the final value V_1 if sufficient sample time is available. The difference between the final value V_1 and the output voltage $v_0(t)$ at time "t" is defined as the channel settling error. For a single-ended channel this difference is

$$E_S(t) = \frac{1}{C_I + C_0}\left[C_0(V_1 - V_2) + (C_{sg} + C_{dg})(V_G + V_B)\right] e^{-t/\tau_2} \quad (18)$$

In the case of a differential-ended channel, the settling error is the difference between the errors achieved for each of the two signal paths. If the signal paths are considered to be equally balanced; then the settling error can be calculated to be

$$E_D(t) = \frac{2C_0}{C_I + C_0}(V_1 - V_2)\, e^{-t/\tau_2} \quad (19)$$

For the case of equally balance signal paths, the settling error portion attributed to the gate coupling capacitance is observed to cancel out. Typical settling errors that can result from the phenomena of transient events described above are illustrated graphically in Figure 6. The curves are plotted for various sample rates, source resistance and multiplexer capacitances. Time "t" is the period of time occurring after

the channel is turned ON. The settling error as a percentage of $(V_1 - V_2)$ is plotted in Figure 6. The family of curves are a plot of

$$\% \; E_D(t) = \frac{200 \; C_0}{C_I + C_0} \; e^{-t/\tau_2} \tag{20}$$

From the graph we can see that, for the case where V_1 and V_2 are DC sources, which represents the peak amplitude of the input data, the higher the sample rate, the smaller the source resistance, or the smaller the output capacitance; then the less the settling error will be. To minimize settling errors, the input capacitance should be either very small or very large in value.

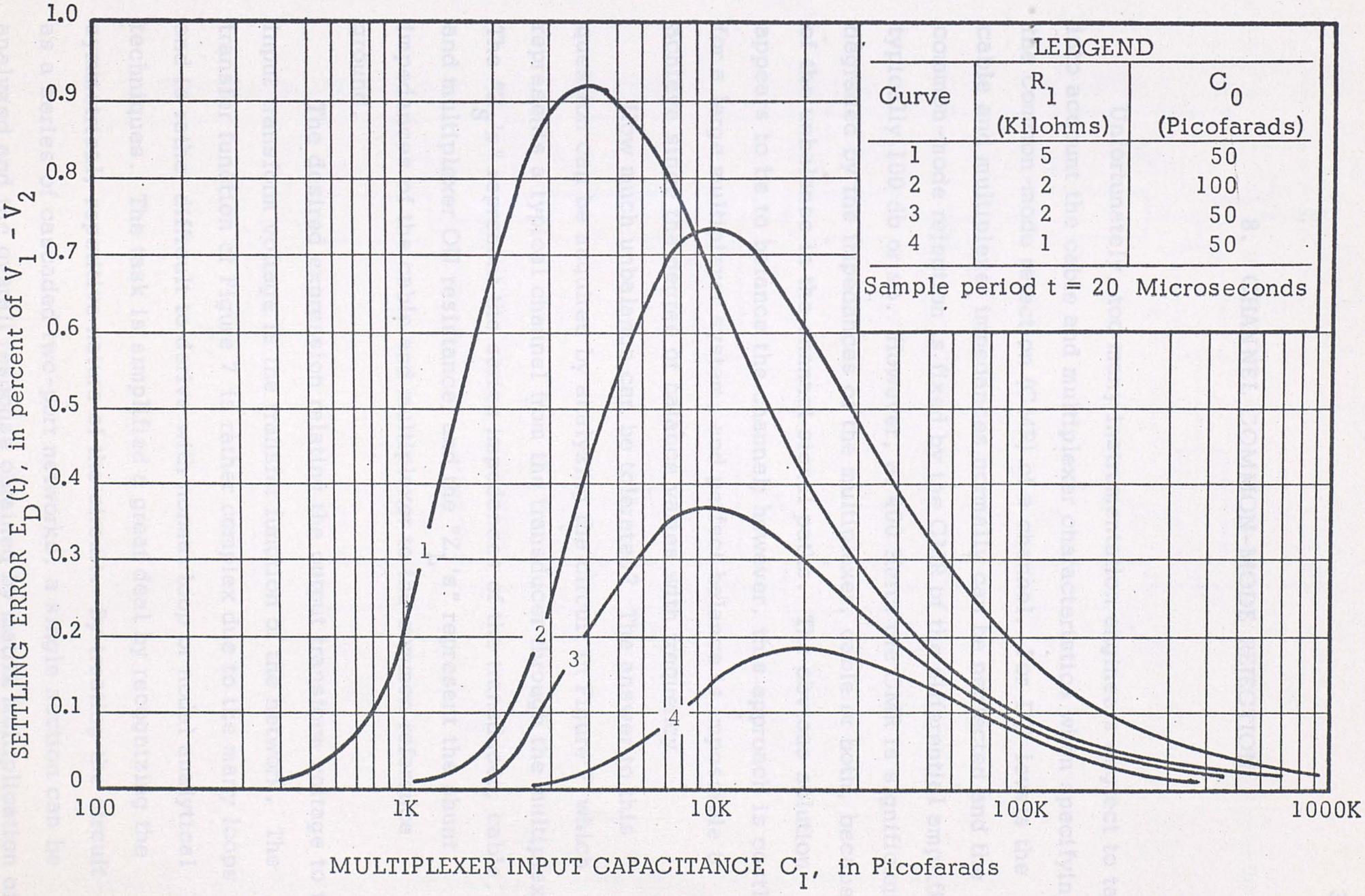

Figure 6. -- Differential channel settling errors.

8. CHANNEL COMMON-MODE REJECTION

Unfortunately, too many instrumentation engineers neglect to take into account the cable and multiplexer characteristics when specifying the common-mode rejection (CMR) of a channel. For DC levels the cable and multiplexer impedances normally can be neglected and the common-mode rejection is fixed by the CMR of the differential amplifier, typically 100 db or so. However, at 400 Hertz the CMR is significantly degraded by the impedances of the multiplexer, cable or both, because of the unbalance in the channel signal paths. The obvious solution appears to be to balance the channel; however, this approach is costly for a large multiplexer system, and perfect balance is impossible to achieve since the degree of balance varies with frequency.

How much unbalance can be tolerated? The answer to this question can be acquired by analyzing the circuit in Figure 7 which represents a typical channel from the transducer through the multiplexer. The "Z_S's" represent the series impedances of the transducer, cable, and multiplexer ON resistance; and the "Z_L's" represent the shunt impedances of the cable and multiplexer to the common reference ground.

The desired expression relating the output transform voltage to the input transform voltage is the transfer function of the network. The transfer function of Figure 7 is rather complex due to the many loops and is rather difficult to derive with normal loop or nodal analytical techniques. The task is simplified a great deal by recognizing the symmetrical, repetitive nature of the circuit. By treating the circuit as a series of cascaded two-port networks, a single section can be analyzed and the overall response obtained by matrix multiplication of

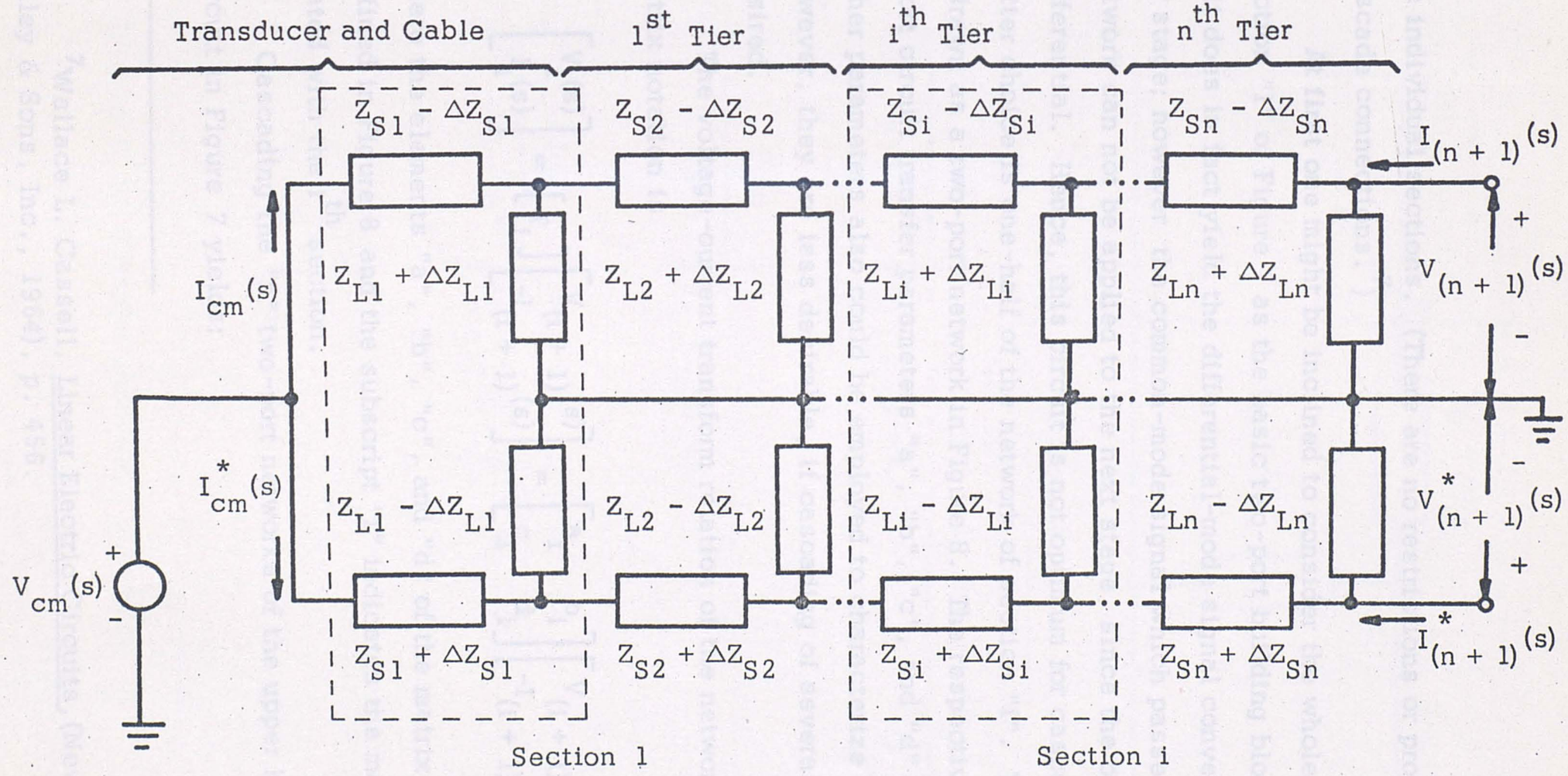

Figure 7. -- Differential channel impedance model for calculation of CMR.

the individual sections. (There are no restrictions or problems in the cascade connections.[7])

At first one might be inclined to consider the whole circuit in section "i" of Figure 7 as the basic two-port building block. This circuit does in fact yield the differential-mode signal conversion of the i^{th} stage; however the common-mode signal which passes through the network can not be applied to the next stage, since the output is purely differential. Hence, this circuit is not optimum for cascading. A better choice is one-half of the network of section "i". This network is redrawn as a two-port network in Figure 8. The respective open and short circuit transfer parameters "a", "b", "c", and "d" are also listed. Other parameters also could be employed to characterize this network; however, they are less desirable, if cascading of several networks is desired.

The voltage-current transform relation of the network in Figure 8 in matrix notation is

$$\begin{bmatrix} V_i(s) \\ I_i(s) \end{bmatrix} = \begin{bmatrix} T_i \end{bmatrix} \begin{bmatrix} V_{(i+1)}(s) \\ -I_{(i+1)}(s) \end{bmatrix} = \begin{bmatrix} a_i & b_i \\ c_i & d_i \end{bmatrix} \begin{bmatrix} V_{(i+1)}(s) \\ -I_{(i+1)}(s) \end{bmatrix} \tag{21}$$

where the elements "a", "b", "c", and "d" of the matrix array are those defined in Figure 8 and the subscript "i" indicates the matrix is associated with the i^{th} section.

Cascading the "n" two-port networks of the upper half of the circuit in Figure 7 yields:

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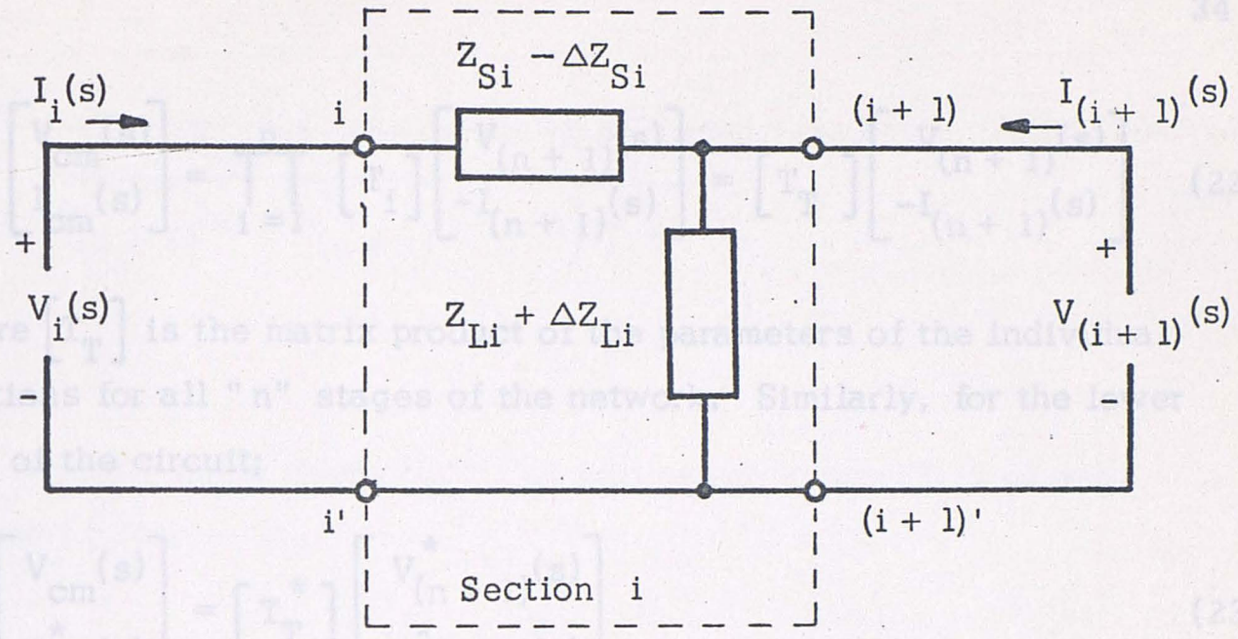
[7]Wallace L. Cassell, Linear Electric Circuits, (New York: Wiley & Sons, Inc., 1964), p. 456.



$$a_i = \left.\frac{V_i(s)}{V_{(i+1)}(s)}\right|_{I_{(i+1)}(s) = 0} = \frac{Z_{Si} + Z_{Li} + \Delta Z_{Li} - \Delta Z_{Si}}{Z_{Li} + \Delta Z_{Li}}$$

$$b_i = \left.\frac{V_i(s)}{-I_{(i+1)}(s)}\right|_{V_{(i+1)}(s) = 0} = Z_{Si} - \Delta Z_{Si}$$

$$c_i = \left.\frac{I_i(s)}{V_{(i+1)}(s)}\right|_{I_{(i+1)}(s) = 0} = \frac{1}{Z_{Li} + \Delta Z_{Li}}$$

$$d_i = \left.\frac{I_i(s)}{-I_{(i+1)}(s)}\right|_{V_{(i+1)}(s) = 0} = 1$$

Figure 8. -- Transfer parameters of Section i.

$$\begin{bmatrix} V_{cm}(s) \\ I_{cm}(s) \end{bmatrix} = \prod_{i=1}^{n} \begin{bmatrix} T_i \end{bmatrix} \begin{bmatrix} V_{(n+1)}(s) \\ -I_{(n+1)}(s) \end{bmatrix} = \begin{bmatrix} T_T \end{bmatrix} \begin{bmatrix} V_{(n+1)}(s) \\ -I_{(n+1)}(s) \end{bmatrix} \quad (22)$$

where $\begin{bmatrix} T_T \end{bmatrix}$ is the matrix product of the parameters of the individual sections for all "n" stages of the network. Similarly, for the lower half of the circuit;

$$\begin{bmatrix} V_{cm}(s) \\ I^*_{cm}(s) \end{bmatrix} = \begin{bmatrix} T^*_T \end{bmatrix} \begin{bmatrix} V^*_{(n+1)}(s) \\ -I^*_{(n+1)}(s) \end{bmatrix} \quad (23)$$

where the asterisk symbol denotes the lower sections. Hence the voltage transfer functions of the composite "n" sections are

for the upper half:
$$\left. \frac{V_{cm}(s)}{V_{(n+1)}(s)} \right|_{I_{(n+1)}(s) = 0} = A_T \quad (24)$$

for the lower half:
$$\left. \frac{V_{cm}(s)}{V^*_{(n+1)}(s)} \right|_{I^*_{(n+1)}(s) = 0} = A^*_T \quad (25)$$

where A_T, A^*_T represents the composite "a" parameter in the $\begin{bmatrix} T_T \end{bmatrix}, \begin{bmatrix} T^*_T \end{bmatrix}$ matrix

$$\begin{bmatrix} T_T \end{bmatrix} = \begin{bmatrix} A_T & B_T \\ C_T & D_T \end{bmatrix} = \begin{bmatrix} a_1 & b_1 \\ c_1 & d_1 \end{bmatrix} \begin{bmatrix} a_2 & b_2 \\ c_2 & d_2 \end{bmatrix} \cdots \begin{bmatrix} a_n & b_n \\ c_n & d_n \end{bmatrix} \quad (26)$$

The ratio of the input voltage to the difference of the output voltages of the composite circuit is calculated as:

$$\frac{V_{cm}(s)}{V_{(n+1)}(s) - V^{*}_{(n+1)}(s)} = \frac{A_T A^{*}_T}{A^{*}_T - A_T} \tag{27}$$

The common-mode rejection of the network in Figure 7 is clearly defined to be

$$\text{CMR} \triangleq 20 \text{ Log} \left| \frac{A^{*}_T - A_T}{A_T A^{*}_T} \right| \tag{28}$$

As an example, consider the effects of the cable and source impedances (represented in the first section) on the CMR performance of the channel. Normally, the multiplexer input impedance is much greater than the cable shunt impedance to ground. Hence, the second section's loading on the first section can be neglected without introducing substantial error. With this assumption, the ratio of the difference of the output voltages to the input voltage is:

$$\frac{V_2(s) - V^{*}_2(s)}{V_{cm}(s)} = \frac{1}{a_1} - \frac{1}{a^{*}_1} = \frac{Z_{L1} + \Delta Z_{L1}}{(Z_{L1} + Z_{S1}) + (\Delta Z_{L1} - \Delta Z_{S1})} - \frac{Z_{L1} - \Delta Z_{L1}}{(Z_{L1} + Z_{S1}) - (\Delta Z_{L1} - \Delta Z_{S1})} \tag{29}$$

or combining,

$$\frac{V_2(s) - V^{*}_2(s)}{V_{cm}(s)} = \frac{2Z_{S1}Z_{L1}\left(\frac{\Delta Z_{S1}}{Z_{S1}} + \frac{\Delta Z_{L1}}{Z_{L1}}\right)}{(Z_{L1} + Z_{S1})^2 - (\Delta Z_{L1} - \Delta Z_{S1})^2} \tag{30}$$

which is approximately equal to:

$$\frac{V_2(s) - V_2^*(s)}{V_{cm}(s)} \approx \frac{2Z_{S1}Z_{L1}\left(\frac{\Delta Z_{S1}}{Z_{S1}} + \frac{\Delta Z_{L1}}{Z_{L1}}\right)}{(Z_{S1} + Z_{L1})^2} \tag{31}$$

since $(Z_{L1} + Z_{S1})^2 >> (\Delta Z_{L1} - \Delta Z_{S1})^2$. Letting $Z_{S1} = R_{S1} + j0$ and $Z_{L1} = C_{L1}/j\omega(C_{L1}^2 - \Delta C_{L1}^2)$, then equation 31 can be written as

$$\frac{V_2(j\omega) - V_2^*(j\omega)}{V_{cm}(j\omega)} \approx \frac{2R_{S1}\left(\frac{C_{L1}}{j\omega(C_{L1}^2 - \Delta C_{L1}^2)}\right)\left(\frac{\Delta R_{S1}}{R_{S1}} + \frac{\Delta C_{L1}}{C_{L1}}\right)}{\left[R_{S1} + \frac{C_{L1}}{j\omega(C_{L1}^2 - \Delta C_{L1}^2)}\right]^2} \tag{32}$$

From which the CMR is found by taking the product of 20 and the logarithm of the magnitude of the above expression. Typically $C_{L1}^2 >> \Delta C_{L1}^2$, therefore the CMR can be simplified to

$$CMR \approx 20 \text{ Log } \frac{2R_{S1}}{\omega C_{L1}}\left[\frac{\frac{\Delta R_{S1}}{R_{S1}} + \frac{\Delta C_{L1}}{C_{L1}}}{R_{S1}^2 + \left(\frac{1}{\omega C_{L1}}\right)^2}\right] \tag{33}$$

The CMR (Equation 33) is plotted as a set of curves in Figure 9. Note from equation 33 that the CMR is reduced by approximately six db each time either the shunt capacitance unbalance doubles or the source resistance unbalance doubles. From Figure 9 we see that the common-mode rejection of the channel is degraded quite severly for a five percent unbalance in the source resistance and the shunt cable capacitance.

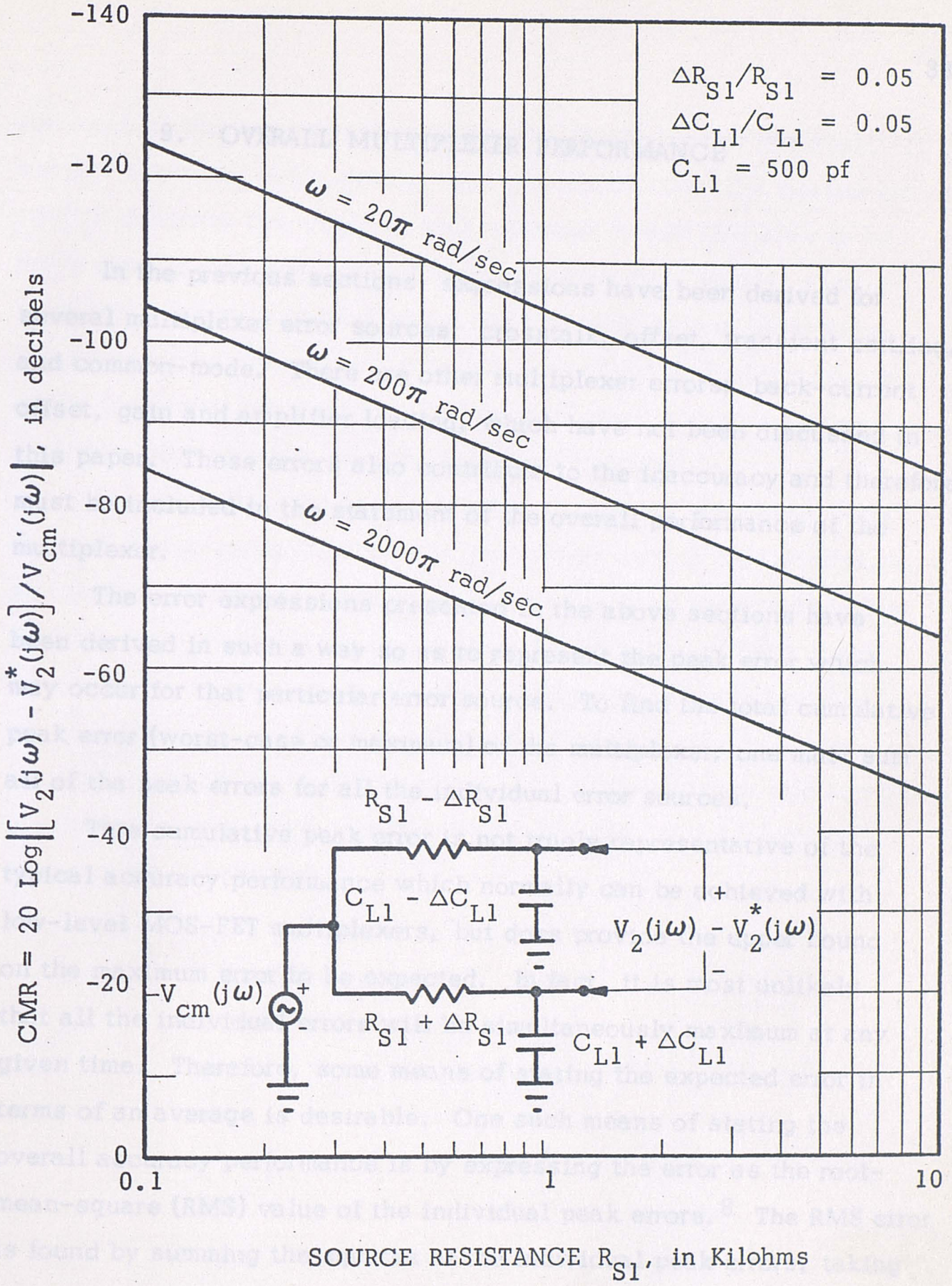


Figure 9. -- Common-mode rejection due only to Section 1.

9. OVERALL MULTIPLEXER PERFORMANCE

In the previous sections, expressions have been derived for several multiplexer error sources: crosstalk, offset, transient settling, and common-mode. There are other multiplexer errors: back-current offset, gain and amplifier loading, which have not been discussed in this paper. These errors also contribute to the inaccuracy and therefore must be included in the statement of the overall performance of the multiplexer.

The error expressions presented in the above sections have been derived in such a way so as to represent the peak error which may occur for that particular error source. To find the total cumulative peak error (worst-case or maximum) of the multiplexer, one must sum all of the peak errors for all the individual error sources.

This cumulative peak error is not truely representative of the typical accuracy performance which normally can be achieved with low-level MOS-FET multiplexers, but does provide the upper bound on the maximum error to be expected. In fact, it is most unlikely that all the individual errors will be simultaneously maximum at any given time. Therefore, some means of stating the expected error in terms of an average is desirable. One such means of stating the overall accuracy performance is by expressing the error as the root-mean-square (RMS) value of the individual peak errors.[8] The RMS error is found by summing the squares of the individual peak errors, taking

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[8]Petr Beckman, Probability in Communication Engineering, (New York: Harcourt, Brace and World Inc., 1967), p. 82.

the mean of the sum, and then taking the square root of the mean. If several errors are much smaller than the others, then the smaller errors tend to dominate the resulting RMS error and forces this error to be much smaller than may normally occur in practice. Hence, another expression for error is often used; the root-sum-square (RSS) value. The RSS error is defined as the square root of the sum of the squares of the individual peak errors. RSS error calculations give a more realistic error estimate than the RMS error calculation.

In conclusion, we have seen from the above paragraphs, that the multiplexer configuration, the multiplexer switch characteristics, and the sample rate all effect the total accuracy of the system. Two of the largest sources of errors are attributed to the settling error, which shows up as channel crosstalk, and common-mode injected errors. Therefore, these two major error factors should be given special attention in the design phase. On the otherhand, one shouldn't overlook the other error sources, which may also cause significate errors if not considered.

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