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Uniformity correction for a scanned long wavelength infrared focal plane array

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UNIFORMITY CORRECTION FOR A SCANNED LONG WAVELENGTH INFRARED FOCAL PLANE ARRAY

BY

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THESIS

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ABSTRACT

This paper presents an alternative approach in providing uniformity correction for an infrared focal plane array by utilizing analog MOSFET circuitry. This technology is compatible with modern VLSI production and is capable of enhanced operation at cryogenic temperatures. The method presented here is a potential contribution to the growing list of special analog circuit configurations which may be incorporated for on-chip signal processing, inside the cryogenic dewar assembly. Electronic packaging of current thermal systems could be significantly reduced in size and weight by trading some of the cumbersome digital algorithms and complex post-processing circuitry for implementation in VLSI form.

The proposed method employs capacitor storage of the thermal reference voltages to correct for the Responsivity and Bias of each detector channel. This compensation for gain and level can be achieved in real operating time using a background subtraction technique and feedback which features pulse-width modulation of the detector's elemental integration period.

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Finally, I wish to remember my grandfather, Charles A. Nelson, who recognized the importance of modern technology development, and taught me many of the principles I live by today.

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INTRODUCTION

Infrared focal plane arrays (IR FPA) have become a very important technology development with respect to military and space applications. These include requirements of missile seeker, threat warning, search and track, and surveilance systems [1,2]. Unique technical obstacles introduced by focal plane arrays include saturation, nonuniformity, charge transfer efficiency, noise and crosstalk [1]. This paper will present a solution to maintaining uniform performance between detector channels. The method for correction utilizes sampling of the thermal references on each line scan and subsequent modulation of the detector's elemental integration period.

The analog circuitry considered for this application is that of Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) technology. Complementary MOS (CMOS) is compatible with the present techniques of Very Large Scale Integrated (VLSI) circuit production. Furthermore, it is anticipated that other research will seek to employ CMOS rather than traditional technologies in the pursuit of FPA development [3].

By implementation of CMOS multiplexing and signal processing circuitry with an array of detectors, an improved

version of today's hybrid focal plane array may be produced. However, one of the long term goals of large FPA design is the incorporation of both the detector and processing circuitry into one material, preferably Mercury Cadmium Telluride (HgCdTe). This accomplishment would yield a true monolithic FPA, eliminating the thermal mismatches between the detector and signal processing material which force limitations on existing hybrid arrays [1].

It is the author's desire that the information presented in this paper contributes to the development of cryogenic analog circuits which are compatible with Long Wavelength Infrared (LWIR) focal plane arrays. The potential contribution of this uniformity correction method would be production of a self-calibrating LWIR camera, thereby simplifying the post-processing circuitry presently required external to the cryogenic dewar assembly.

Detector Materials

The earth's atmosphere is not transparent at all wavelengths. Specifically, there are three well-known spectral intervals or atmospheric windows in which the transmission is high. These include the 2 to 2.5 micron window and the 3 to 5 micron window, located in the near infrared and middle infrared regions respectively [4]. However, the far infrared region which contains the 8 to 12 micron window is of importance to this paper. At the extended

wavelengths above 10 micron, the LWIR FPA multiplexer exhibits some notable problems. One of these is the increase in nonuniformity between array channels near the 12 micron end of the spectrum [3].

A number of semiconductors and other materials have been used in the development of focal plane arrays. While no single material is considered sufficient for all applications, detectors manufactured from Mercury Cadmium Telluride have evolved into the most "universal" in the fabrication of monolithic and hybrid focal plane arrays. This is due to its multispectral (middle and far infrared) and high performance properties [2]. Accordingly, the United States Department of Defense has made it the material of choice for IR FPA development [1]. This paper assumes the use of HgCdTe as the detector material.

Focal Plane Arrays

Focal plane arrays are the product of years of development beginning with the electromechanical scanning of the scene of interest by a single elemental detector. The linear array, comprised of n X 1 detectors, was introduced next and was employed by sweeping the target area in a pushbroom fashion. Alternatively, image detection was achieved via optical movement of the scene across the stationary array [5].

The numerous tactical requirements of the military emphasized the need for increased resolution and sensitivity, requiring from hundreds to thousands of detector elements (dependent on the system application). Thus, two-dimensional matrices of detector elements have been produced which are capable of multiplexing all the detector outputs on the focal plane [1]. However, most of the current arrays are still significantly smaller than desired and special techniques such as bidirectional scanning and time delay integration must be used to obtain the entire thermal scene content.

The primary advantages of focal plane arrays are that they provide an economical method for high-density packaging of detectors and they allow signal processing to take place on the focal plane. In comparison with the prior generation linear array which required one preamplifier and signal line per detector, the FPA preprocessing is accomplished within the cryogenic dewar assembly and multiplexing is utilized to drastically reduce the number of signal leads protruding through the dewar walls [1]. This allows a reduction of size, weight, power requirements, and cost, all of which are important improvements over former thermal systems. Similarly, these enhancements continue to be driving factors in the ongoing development of focal plane arrays.

CHAPTER 1: DOUBLE SAMPLE CORRELATION

Scene Dissection

A LWIR FPA consists of n X m detector elements where n constitutes the number of detection channels and m the number of time delay integration (TDI) channels [2]. There are many types and sizes of focal plane arrays which are used for various purposes. The application itself generally dictates the FPA design [1].

A military requirement might be for a vehicle-borne infrared search and track (IRST) thermal system, necessary to extract target information from background clutter. The system must provide high resolution and wide field of view (FOV). Typical FPA parameters for such a device are n = 480 and m = 12 [1]. This array is normally used to obtain the thermal scene content of a larger FOV by employing a mixture of serial and parallel scanning techniques [6].

Parallel scanning is a mode of imaging in which the scene of interest is scanned across a linear (n X 1) array of sensor elements. The array is oriented perpendicular to the primary scan axis as depicted in Figure 1.1 [6]. All of the detector/preamplifier outputs may be sampled simultaneously, yielding true parallel scene dissection.

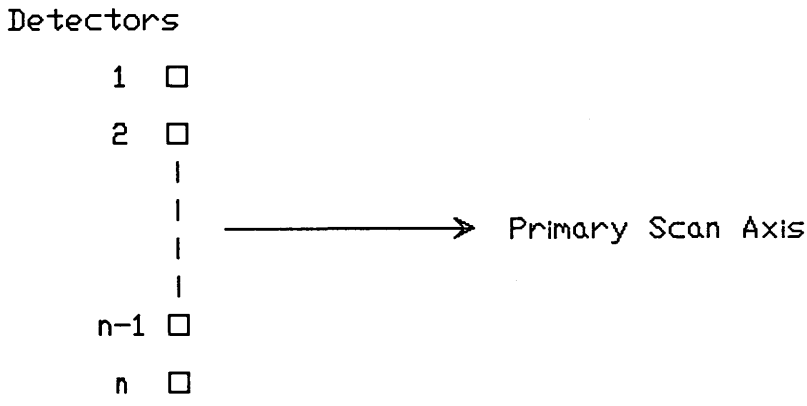

Figure 1.1. Parallel Scan.

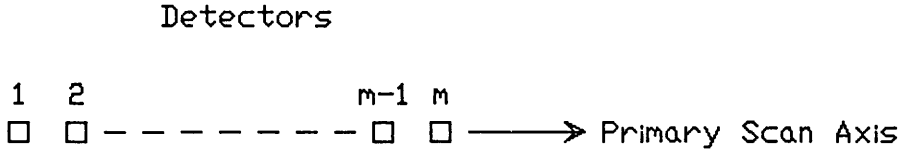

Figure 1.2. Serial Scan.

In the serial scan mode, m detectors are oriented in a single line, within the plane of the primary scan axis, and each point of the image is scanned by all m detectors, shown in Figure 1.2 [6]. If m > 1, the method is termed time delay integration because the detector outputs are delayed and summed by an integrating delay line which superimposes the outputs. This simulates a single scanning detector but yields an increased signal to noise ratio (SNR) [6].

Employing the two-dimensional n X m array in a scene dissection requires parallel optical scanning and serial TDI. The number of detector elements, n, perpendicular to the scan direction determines the resolution of the device [7]. While there are many scanning algorithms and processing techniques which are used, future FPA design consideration should be given to some form of time division multiplexing (TDM). This has already been successfully interlaced with TDI and helps to minimize VLSI circuit size and complexity [8].

Thermal System Parameters

A typical thermal imaging system might require a n X m FPA to dissect a scene whose optical field of view size, as measured by picture elements (pixels), is n X p, where p >> m. A pixel is defined to be a FOV resolution element that corresponds to a single exposure of the detector during one dwell time [9]. For the purpose of this paper, it is assumed that: n = 480 m = 1 p = 620.

Thus, true parallel scene dissection via linear array will be considered although the techniques for detector uniformity correction developed here may be extended to parallel scanned, TDI arrays and eventually perhaps to large, two-dimensional mosaic staring arrays.

Thermal imaging is achieved by scanning each point of the scene across the FPA as depicted in Figure 1.3. There is a finite dwell time associated with each image point and its incident photon flux on the detector element. For analysis purposes it will be assumed that the scanning velocity is constant over the total FOV, there is no dead time in retrace or at the line scan edges, and there is no overlapping of scan lines. This implies an ideal scan efficiency of 100% [9]. The entire scene or "field" is thus obtained after 620 equal but discrete time periods. During each time period, the detector output should be sampled and the result stored for subsequent processing. Additionally, the acquired charge should be dispersed in order to allow imaging of the next point in the scene.

In similar fashion to televison rasters, FPA scanning rates may be calculated. Typical frame and field periods are defined below in terms of our assumed thermal system:

620 Columns	per	Field
1 Field	per	Frame
30 Frames	per	Second
18,600 Columns	per	Second

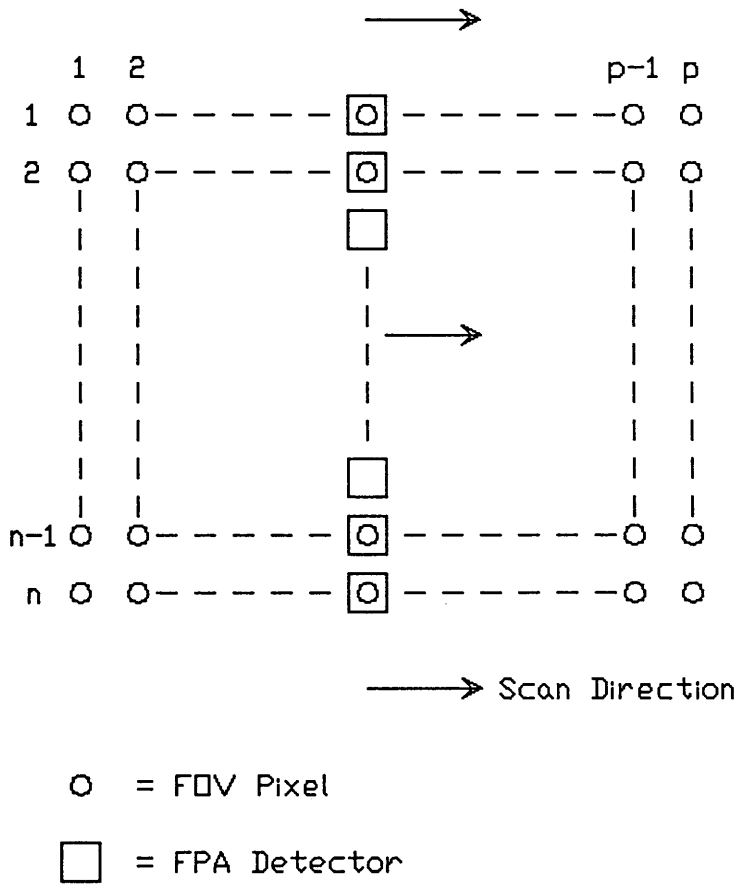

Figure 1.3. Parallel Scene Dissection.

The FPA scanning rate is seen to be only 30 Hz, which is sufficient in acquiring most scene changes. However, the dwell time associated with each column of detectors is:

$$T = (18{,}600 \text{ Columns per Sec})^{-1} = 53.76 \text{ usec/column}$$

This equates to only 112 nsec in which to sample each image point if TDM were not utilized. That is,

$$(53.76 \text{ usec/column}) \div (480 \text{ detectors/column}) = 112 \text{ nsec/detector}$$

However, it should be noted that each detector's dwell time is still 53.76 usec.

By employing a total of eight, 60-to-1 multiplexers (MUX) as shown in Figure 1.4, each detector may be accessed up to 896 nsec (53.76 usec ÷ 60 detectors). Using this scheme, a multiplexer must sample only 60 detectors in 53.76 usec, a much more manageable task. This paper supposes the use of TDM as briefly described here.

Additionally, it is assumed that each unique detector or any part of that detector can image one and only one FOV pixel at any particular instant of time. This precludes the possibility of incident photon flux from two distinct image points contributing to the same IR detector at the same time.

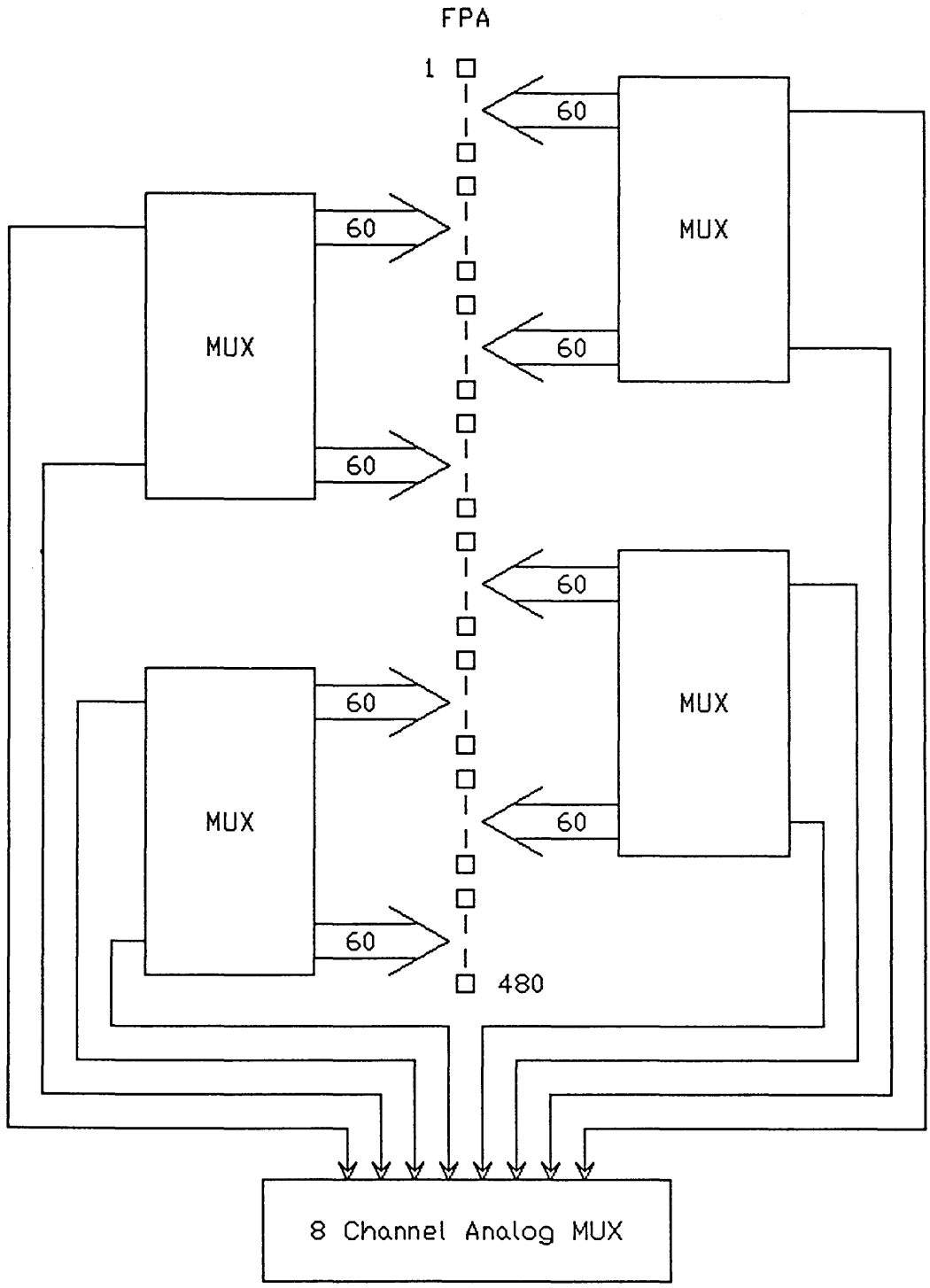

Figure 1.4. FPA Time Division Multiplexing.

Detector Preamplification

The product RoA is the Figure of Merit for infrared detectors, where Ro is the output resistance in ohms and A is the active area in square centimeters. The output resistance is very sensitive to temperature changes in the cryogenic region, doubling for every 3° to 10° Kelvin decrease. For that reason, RoA is generally specified at the reference temperature of 77° K, which is likewise the commonly used operating ambient of focal plane arrays [10].

At elevated temperatures (above cryogenic region) and/or wavelengths exceeding 10 micron, Ro decreases rapidly [3]. Charge transfer efficiency is thereby substantially reduced, necessitating the requirement of preamplification.

Detector preamplification is normally achieved with a transresistance Buffered Direct Injection (BDI) circuit as represented in Figure 1.5. For this configuration it has been shown that the optimum reverse bias is not 0 volts but rather lies between 1 and 5 thermal equivalent voltages or about 6 to 30 millivolts for most thermal systems [10]. In this manner 1/f noise is minimized by considering the contributions of the amplifier. However, for the analysis of this paper we will assume a diode voltage of 0 volts, further discussed in Chapter 2.

Photocurrents induced in the detector element are determined by the speed of the system optics, the incident photon flux, and the element's quantum efficiency. These

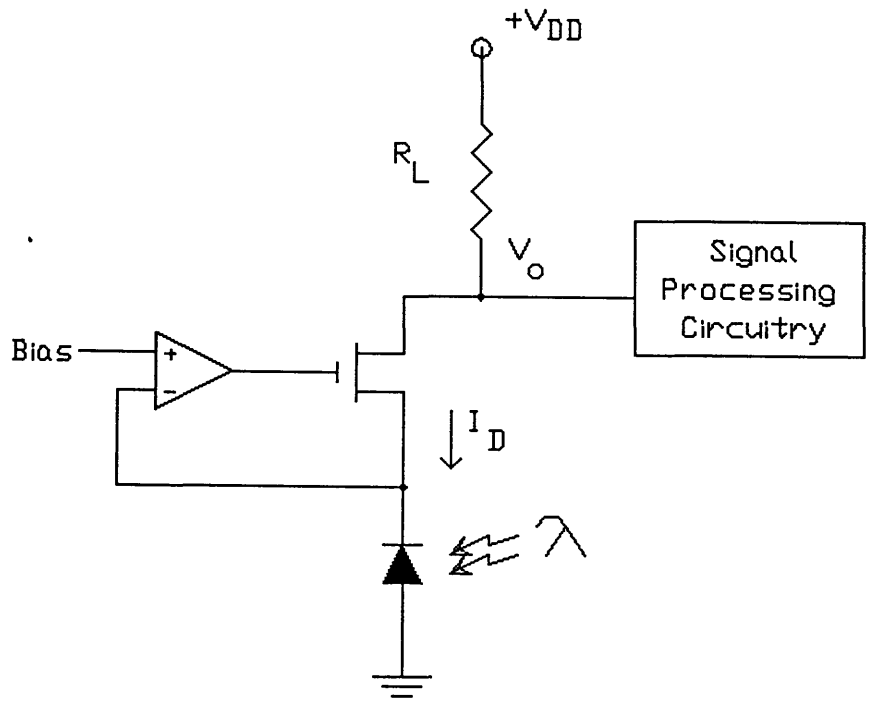

Figure 1.5. Transresistance BDI Preamplification.

photocurrents are generally in the range of 10 to 200 nanoamperes [10]. The amplifier will produce an output voltage Vo in response to an input current I_D. Assuming a charge-transfer efficiency of 100%, the transfer resistance R_T is equal to the circuit's load resistance R_L and is defined by the following equation [10]:

$$R_T = \frac{Vo}{I_D}$$

This quantity R_T is normally in the range of 10 Megohms. The actual load resistor is configured between the amplifier's open drain output and the positive power supply rail, $+V_{DD}$ as shown in Figure 1.5.

This paper assumes operation of detector and preamplifier at the fixed reference temperature of 77° K with direct current coupling to subsequent processing circuitry as described here.

Signal Processing

Integration will be used to process the output voltage of the BDI circuit by substitution of a switched capacitor for R_L. The nominal integration time will be one-half of the detector's dwell time on one pixel or 26.88 usec and thus a double integration is achieved for each pixel. A FET switch is implemented across the capacitor, shown in Figure 1.6, to allow periodic discharging and subsequent resetting of the integration process. During integration the switch will be

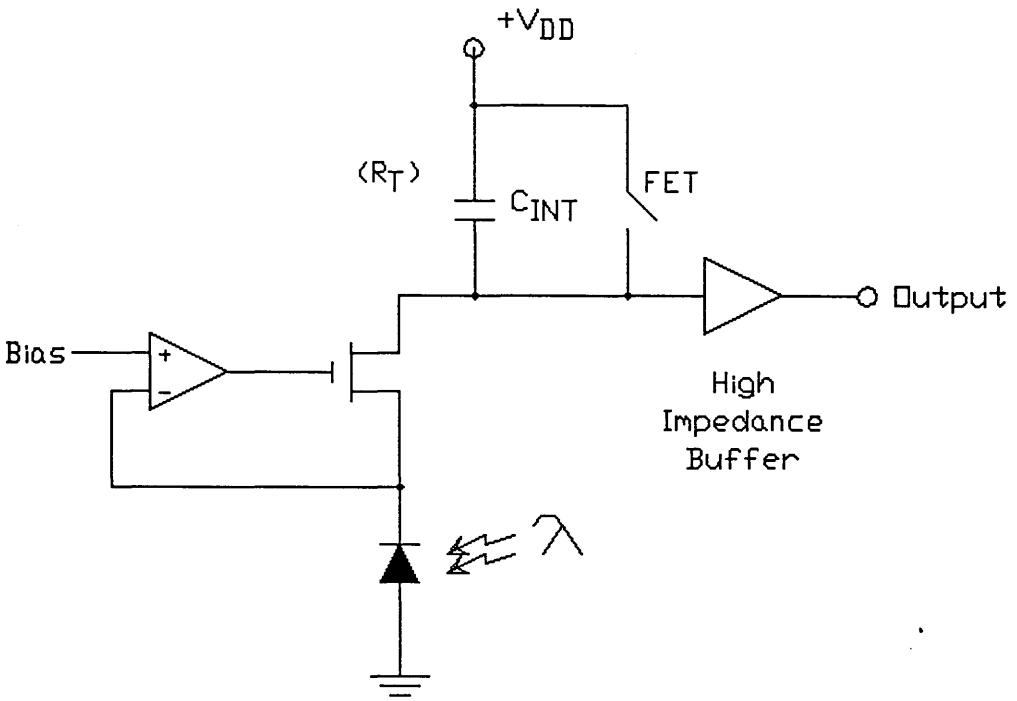

Figure 1.6. BDI Integration Technique.

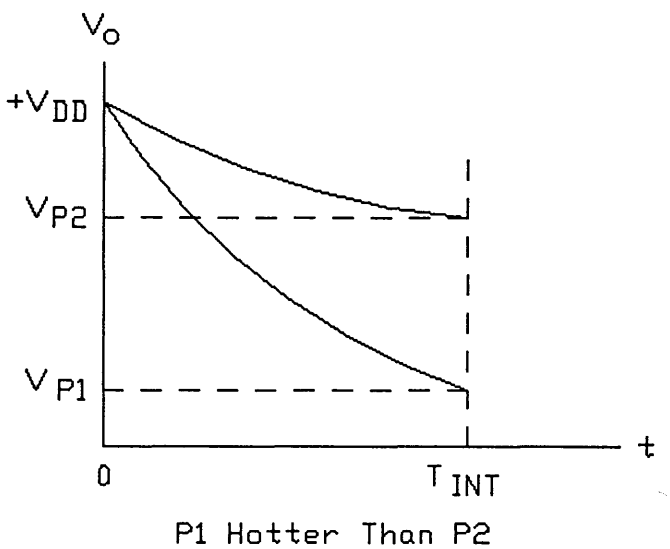

Figure 1.7. Integrator Output for Thermally Dissimilar Pixels.

"off" and will only be turned on briefly to allow sufficient discharging of the capacitor. Note that this integrator reset pulse will occur at a 37.2 KHz rate or exactly double that of the column scan rate due to the double integration technique.

From this circuit configuration the following relationship is evident:

$$R_T = \frac{T_{INT}}{C_{INT}}$$

Assuming an input current of 100 nanoamperes and an output voltage of 1 volt will yield a value of 10 Megohms for R_T. Since T_{INT} = 26.88 usec, C_{INT} is calculated to be approximately 2.7 picofarads. While this can be easily implemented in VLSI design, impedance scaling was necessary for the design example constructed and will be discussed in Chapter 3.

Given two FOV pixels, P1 and P2, where P1 > P2 in thermal content (P1 hotter), the output voltage of the BDI circuit will be less for P1 than for P2. That is, more detector photocurrent is induced for hotter target pixels, thus dropping more voltage across R_L and yielding a lower V_o. This in turn will produce the various integrator outputs as shown in Figure 1.7.

Correlation

As the pixel of interest is scanned across the detector, there is a point of maximum incident photon flux. The first half of the pixel scan provides increasing IR incidence until

this peak is reached. Symmetrically, the second half of the pixel scan provides decreasing flux intensity until the scan is terminated. This pixel scan characteristic is depicted in Figure 1.8.

By providing double integration, the area under the function is obtained for each half of the pixel scan. Assuming a constant scan velocity, the end result of both integration processes should yield similar values. A sampling process should take place just prior to the resetting of the integrator, at the maximum incidence peak and again at the end of the pixel scan. These two sampling points and their relationship to the integrator reset pulses are shown in Figure 1.9.

By providing a double sample for each pixel dwell time the Nyquist sampling criterion is achieved. Briefly recalled, this states that the sampled waveform can be reconstructed without loss of useful information as long as the sampling frequency is at least twice that of the continuous signal's highest frequency component. Assuming that this signal is bandwidth limited implies that

$$f_s > 2\ B$$

where f_s is the sampling frequency and B is the bandwidth of the signal to be sampled. Were f_s less than twice the bandwidth, i.e., an inadequate sampling rate, aliasing in the frequency spectrum could occur. This would yield an erroneous waveform during reconstruction and would manifest itself in

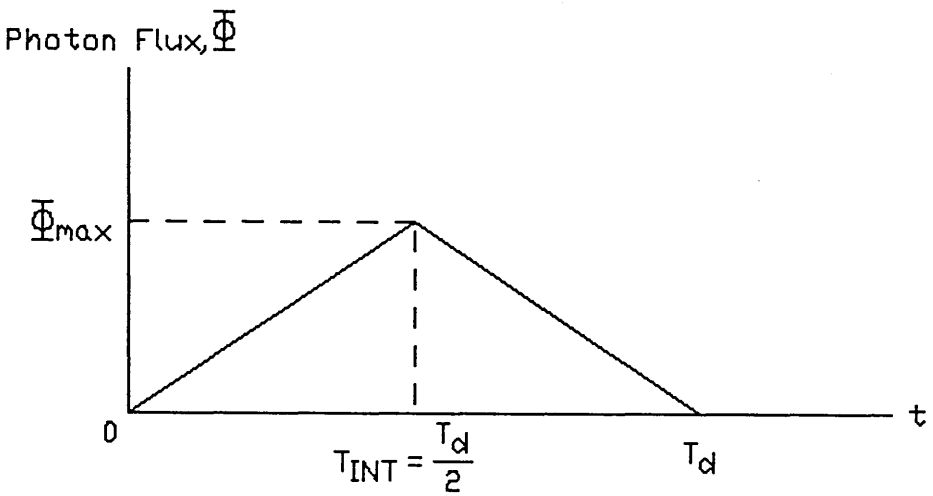

Figure 1.8. Photon Flux Incidence vs. Detector Dwell Time.

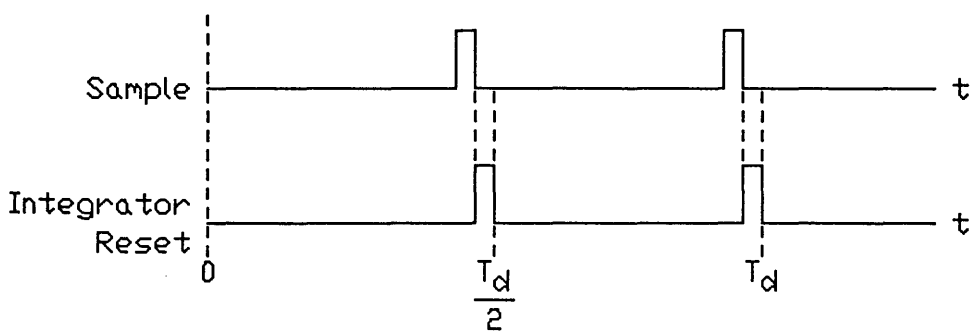

Figure 1.9. Control Pulses vs. Detector Dwell Time.

the form of image distortion. From Figure 1.9 note that the sampling occurs at equally spaced intervals of 26.88 usec ($T_D/2$) or equivalently at a rate of 37.2 KHz.

The bandwidth B for a scanned IR FPA is defined by the following equation [9]:

$$B = \frac{1}{2 T_d}$$

where T_d is the detector dwell time for one pixel.

Using our dwell time of 53.76 usec, it can be determined that B = 9.3 KHz, or approximately one-fourth the sampling frequency of 37.2 KHz. While this meets the minimum Nyquist criterion, there will always be some aliasing present due to high frequency signals originating from noise and nonideal components. These can be minimized by performing cross-correlation between the two samples for each pixel, also known as Double Sample Correlation.

This method of cross-correlation is actually a special case of autocorrelation because the same informational content is obtained at two distinct points in time. That is, autocorrelation gives a measure of the similarity or coherence between a signal and a time delayed version of that signal [11]. Mathematically it is equivalent to the convolution of the two functions.

It has been noted earlier in this chapter that for a parallel processed scanner, the scene is dissected by convolution in the x-direction and TDM sampling in the

y-direction. Since this paper only considers one channel and thus one detector scan in the x-direction, the two samples per dwell are essentially convolved. In this manner noise components are reduced since their contributions should add incoherently while the two fundamental signals should be similar if not identical.

Sampling

The sampling itself should be accomplished with a sample and hold circuit which is a special mode of the "boxcar" integrator, shown in Figure 1.10. This circuit employs a FET switch as its sampling gate and will be considered in Chapter 2.

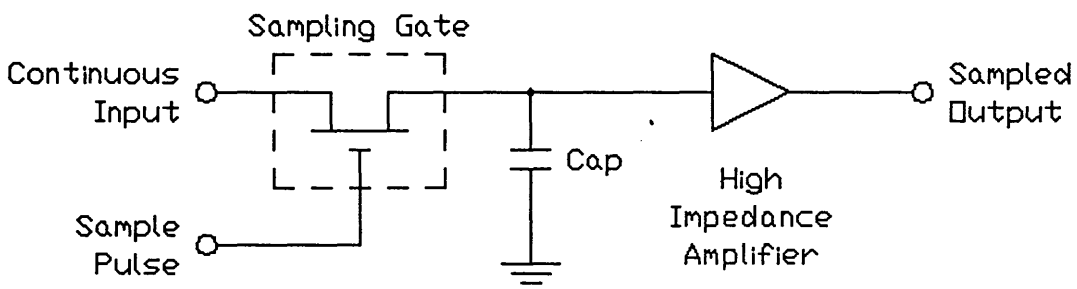

Figure 1.10. Boxcar Integrator.

CHAPTER 2: GAIN AND LEVEL REQUIREMENTS

Whenever more than one infrared detector is utilized in scene dissection, there are several technical obstacles which are introduced. One of these is nonuniformity between detector channels. With our assumption of a linear FPA, each channel equates to a single line scan with one detector element. In proposing a method of uniformity correction, this paper realizes that other special analog circuit techniques are yet to be developed in order to overcome existing deficiencies and optimize FPA performance. However, it is believed that all of these methods together can be developed into practical cryogenic configurations which are compatible with very large scale processing techniques.

In thermal imaging systems each detector scan normally includes a view of a thermal reference source during an inactive portion of the scan cycle. This source might be an active source such as a heated strip or a passive source such as an optical stop [6]. For the purposes of this paper it will be assumed that a single detector will view both a cold reference and a hot reference in addition to the scene of interest for each line scan.

The thermal references will be at the beginning or end of each line scan and each one will be viewed 10% of the line scan period, covering 62 pixels. The remaining 496 pixels or 80% of the line scan period is reserved for the desired target. These are rough approximations to time constants of actual thermal imaging systems currently in use.

The proposed method of uniformity correction utilizes sampling of each thermal reference per line scan and subsequent capacitor storage for real-time processing. The two distinct variables which need addressing are the Responsivity and the Bias for each detector diode. A switched capacitor technique is presented for Bias correction. Pulse-width modulation is considered for Responsivity variations. Taken in its entirety, the circuit should make adjustments for m and b in the well-known straight line equation:

$$y = mx + b$$

where y represents the photo-induced diode current, slope m the gain or Responsivity of the detector, and b the Bias level attributed to background photon flux.

Infrared Detectors

Infrared detection can be achieved in a number of ways. This paper assumes operation of the IR transducer (photodiode) in a photovoltaic process. That is, a change in the number of photons incident on the semiconductor p-n junction will cause a change in the voltage generated by that junction [9].

The current-voltage relationship of a typical IR photodiode is shown in Figure 2.1 where the top curve represents the unilluminated case and the lower curve the illuminated case [9]. Note that even for the unilluminated case, a short-circuit current and open-circuit voltage will be observed. This is due to incidence of background photon flux with sufficient energy to produce free electron-hole pairing [9]. The current through the p-n junction is described by the following equation [9,10]:

$$I_D = I_S[\exp(-\frac{V_D}{\beta V_T}) - 1] - I_P + G_S V_D \qquad \{2.1\}$$

where I_D is the diode current in amperes

I_S is the reverse saturation current in amperes

V_D is the diode voltage in volts

V_T is the thermal equivalent voltage (kT/q) in volts

β is an efficiency factor for photodiodes

I_P is the photo-induced diode current in amperes

G_S is the effective shunt conductance in mhos, thereby making $G_S V_D$ the leakage current

The above equation includes the contributions due to diffusion and drift currents as evidenced by the first term. However, it neglects second-order effects attributed to diode breakdown, generation-recombination currents, and modulation of the reverse saturation current by short base effects [10].

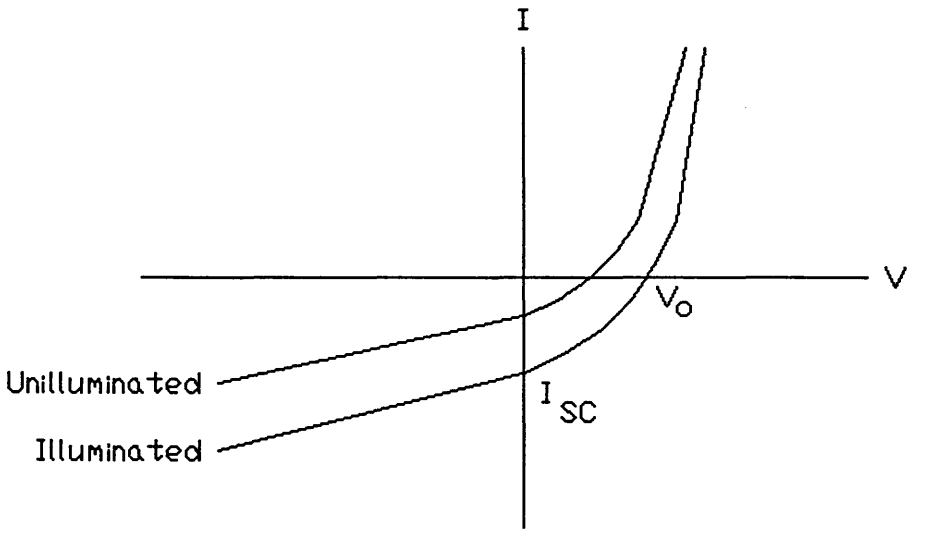

Figure 2.1. Current -- Voltage Relationship of an Infrared Diode.

These will not be considered within this paper and are assumed to be negligible owing to our assumption of a noise-optimized BDI preamplification input circuit [12].

Recall from Chapter 1 that the optimum reverse bias of the detector diode is not 0 V when considering the noise contributions of the BDI preamplifier. However, for our analysis this slight deviation in diode voltage is not significant so we will set V_D at 0 volts. By making this condition, equation {2.1} is reduced to the following:

$$I_D = - I_P \qquad \{2.2\}$$

Additionally, I_P is comprised of photon flux contributions from both the background and target images. Mathematically this is represented in equation {2.3} below [9]:

$$I_P = q \epsilon A (\phi_B + \phi_I) \qquad \{2.3\}$$

where
- q is the electronic charge in Coulombs
- ϵ is the quantum efficiency per photon incidence
- A is the active area of the photodiode in cm^2
- ϕ_B is the photon flux contribution from the background in photons/($cm^2 \cdot sec$)
- ϕ_I is the photon flux contribution from the target image in photons/($cm^2 \cdot sec$)

Typically the background flux contributions are at least an order of magnitude greater than those emanating from the image. Rewriting equation {2.3} it can be seen that it is in

the line equation form of $y = mx + b$ as shown in equation {2.4} below. That is,

$$I_P = q \epsilon A \phi_B + q \epsilon A \phi_I \qquad \{2.4\}$$

Note that since $\phi_B > 10 \cdot \phi I$, the first term of equation {2.4} is essentially a very large DC offset and thus corresponds to the Bias level b in the line equation. The second term equates to the mx term of the line equation where the slope m is represented by the product $\epsilon \cdot A \cdot \phi_I$. This term corresponds to the detector's gain or Responsivity, normally expressed in terms of current or voltage output per incident power in watts.

It is the second term which is necessary to reproduce the image, so a method is required which provides elimination of the first term and thus background subtraction. Other techniques should then be used to compensate for the three variables which are part of the image term, ϵ, A, and ϕ_I.

Employing current technology in the volume production of infrared detector diodes can yield differences as much as ± 50% between two given diodes. This is due to possible stack-up tolerance errors of the aforementioned three variables.

The quantum efficiency ϵ can vary as much as ± 20% dependent on the doping ratio of Mercury to Cadmium. Likewise, the photon flux density can vary as much as ± 20%.

Finally, the active area of the photodiode can differ by at least ± 10%, knowing that a typical sensor is 30 um square, with a side length tolerance of ± 3 um. It is these variables which must be taken into account in producing thermal images with multiple detector elements.

As discussed in Chapter 1, preamplification of each detector will be accomplished with BDI and the subsequent signal processing will be initiated with integration. The next consideration is the sampling process itself.

Sample and Hold

Recall that the integrator output should be sampled at the end of the integration period, just prior to resetting of that circuit as shown in the timing diagram of Figure 1.9. This sample must then be retained until the next sampling instant. The most efficient circuit for accomplishing this task is the Sample and Hold, previously depicted in Figure 1.10. Combining Figures 1.6 and 1.10 results in the arrangement of Figure 2.2.

The FET switch acts as the sampling gate by providing a very high "off" resistance in the absence of a control pulse, typically greater than 10^9 ohms from drain to source. Alternatively, a low "on" resistance is activated upon application of a signal to the transistor gate. Then the FET channel resistance r_{ds} can be as low as 10 ohms, particularly at cryogenic temperatures where transconductance improves as

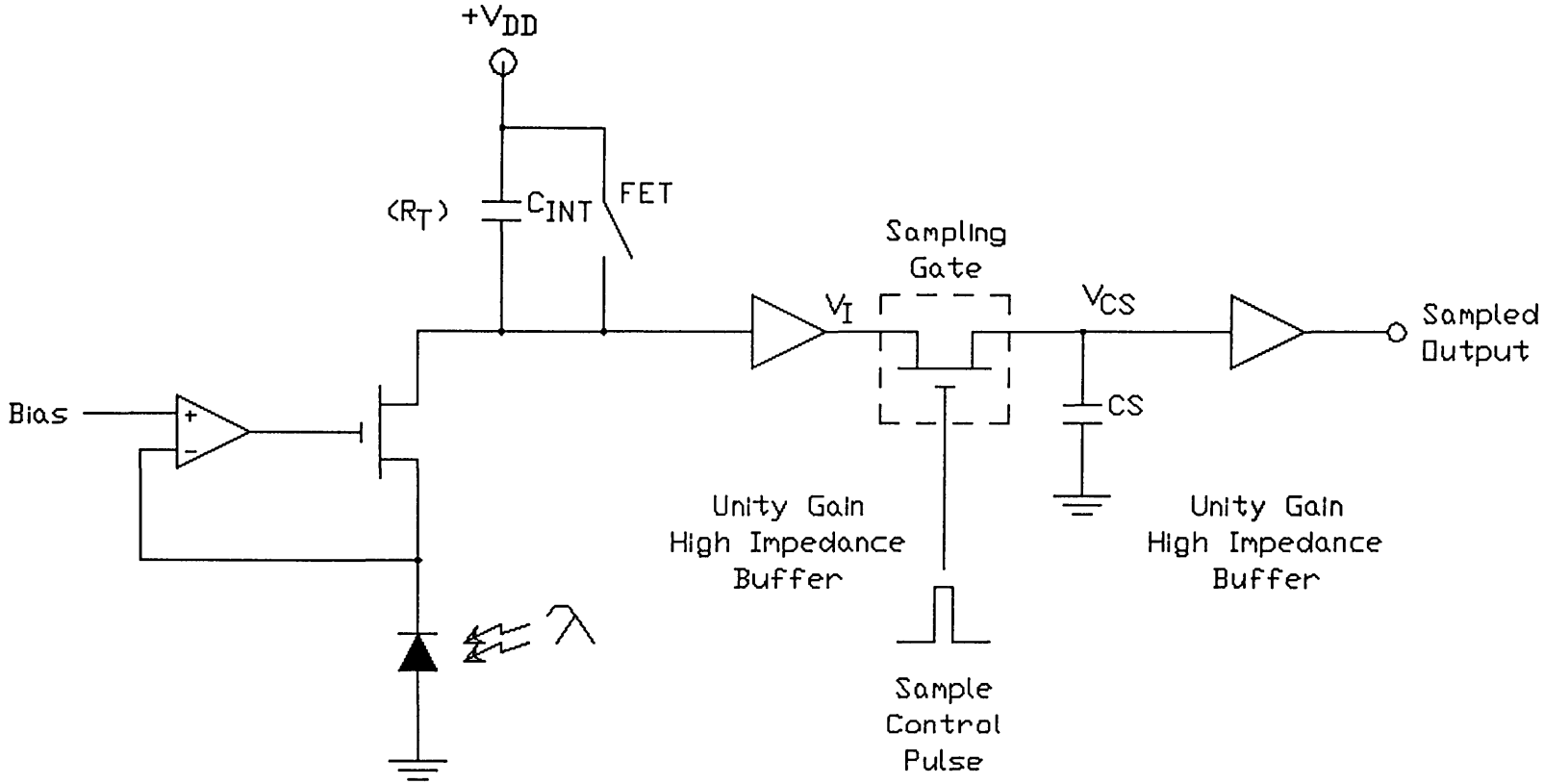

Figure 2.2. Sample and Hold Processing.

much as 8 times that at normal ambient. This is due to the increased mobility of its carriers [10].

The sample mode implies that $r \cdot CS << T_s$, where r is the resistance of the "on" FET channel and signal source. T_s is defined to be the sampling period, specified previously as $T_d/2$ or 26.88 usec. While in this mode the capacitor CS charges up to the input voltage almost immediately, with the time constant $r \cdot CS$ in accordance with the following equation:

$$V_{CS} = V_I \left[1-\exp^{\left(\frac{-t}{r \cdot CS}\right)}\right] + V_i \exp^{\left(\frac{-t}{r \cdot CS}\right)} \qquad \{2.5\}$$

where V_{CS} is the instantaneous voltage across the capacitor in volts

V_I is the voltage input to the sampling gate in volts

V_i is the initial voltage residing on CS, maintained since the prior sampling instant

From this equation it is evident that each control pulse width should be as small as possible yet sufficient (at least $5 \cdot r \cdot CS$) to obtain an accurate sample of the continuous voltage input V_I. This will produce a sampled voltage $V_{CS}(t)$ within 1 percent of $V_I(t)$, assuming ideal components (no capacitor self-leakage and infinite FET "off" resistance).

A high impedance unity gain buffer is required as the Sample and Hold output stage to obviate discharging of the capacitor. Typical input impedance, Z, for such a device is again 10^9 ohms. In the Hold mode the capacitor is susceptible

to discharging through Z in accordance with the following equation:

$$V_{CS} = V_i \left[\exp^{\left(-\frac{-t}{Z \cdot CS}\right)}\right] \qquad \{2.6\}$$

where V_{cs} is the instantaneous voltage across the capacitor in volts

V_i is the initial capacitor voltage immediately after removal of the sample pulse

The hold state should accurately maintain the stored charge on the capacitor until the next sample is obtained. This infers that the time constant Z·CS in equation {2.6} should be at least 100 times greater than the sampling period T_s, in order to maintain $V_{CS}(t)$ within 1 percent of the initial capacitor voltage V_i.

At some period of time during each line scan the hot and cold thermal reference sources will be sampled instead of the scene of interest. This can be used to great advantage in developing real-time uniformity correction circuitry.

Background Subtraction

While the light incident on the IR detector is in the form of individual photon events as shown in Figure 2.3, the measured input to the integrator appears as a DC signal with variations superimposed on it, depicted in Figure 2.4. This

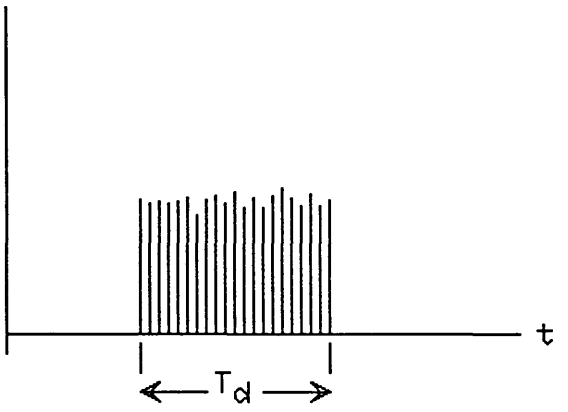

Figure 2.3. Actual Photon Incidence for One Pixel Dwell.

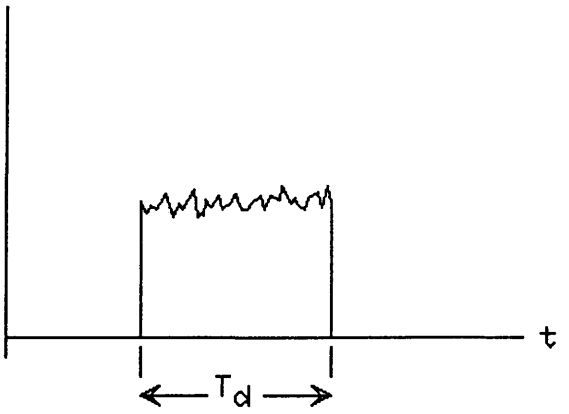

Figure 2.4. Measured Photon Incidence for One Pixel Dwell.

is due to the much faster rate of photon arrival with respect to the resolution and response time of the electronics [3].

Shown in Figure 1.7, a colder pixel will yield higher voltages at the integrator output. The assumption will be made that no scene pixel can be colder than the cold thermal reference. In typical thermal systems this is most always true. Thus, the reference may be calibrated to the FOV background and this background can then be discarded without loss of image content. By utilizing a sample of the cold reference for each line scan, the signal due to background photon flux can be subtracted from the total signal thereby leaving the image information intact.

This can be achieved with a switched capacitor circuit as presented in Figure 2.5. The FET switch should only be enabled once per channel, obtaining a voltage across CB of a previously sampled cold thermal reference. This is essentially a charge transfer mechanism. Recall that approximately 20% of a line scan is reserved for scanning of both thermal references. The reference sampling pulse should preferably occur after several cold pixel scans to allow settling time of the Sample and Hold capacitor. This is most easily accomplished by simply performing the operation in the exact middle of the reference scan, after one-half (31) of the total number of cold pixels have been observed.

The timing relationship of the cold reference sample pulse is depicted in Figure 2.6. We will delay discussion of

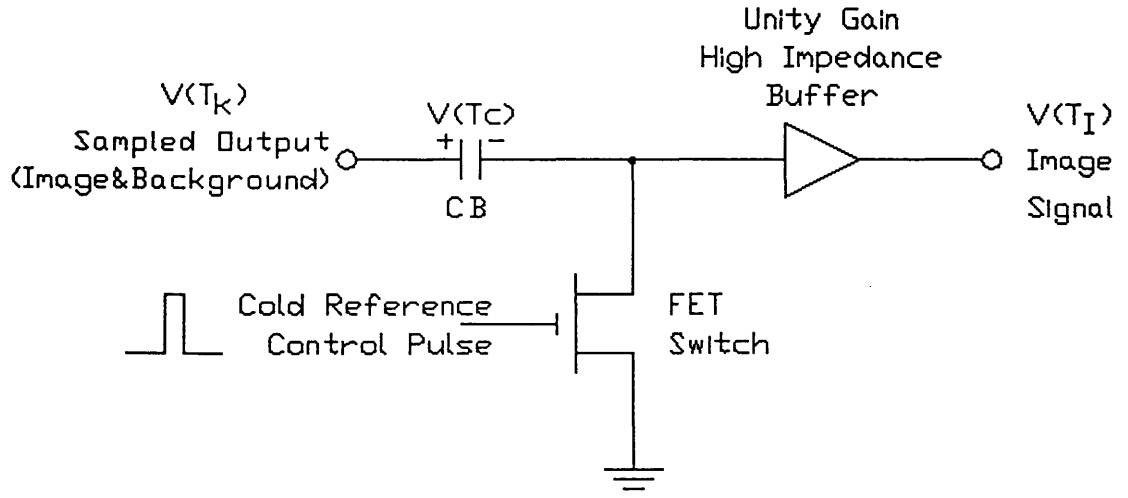

Figure 2.5. Background Subtraction Technique.

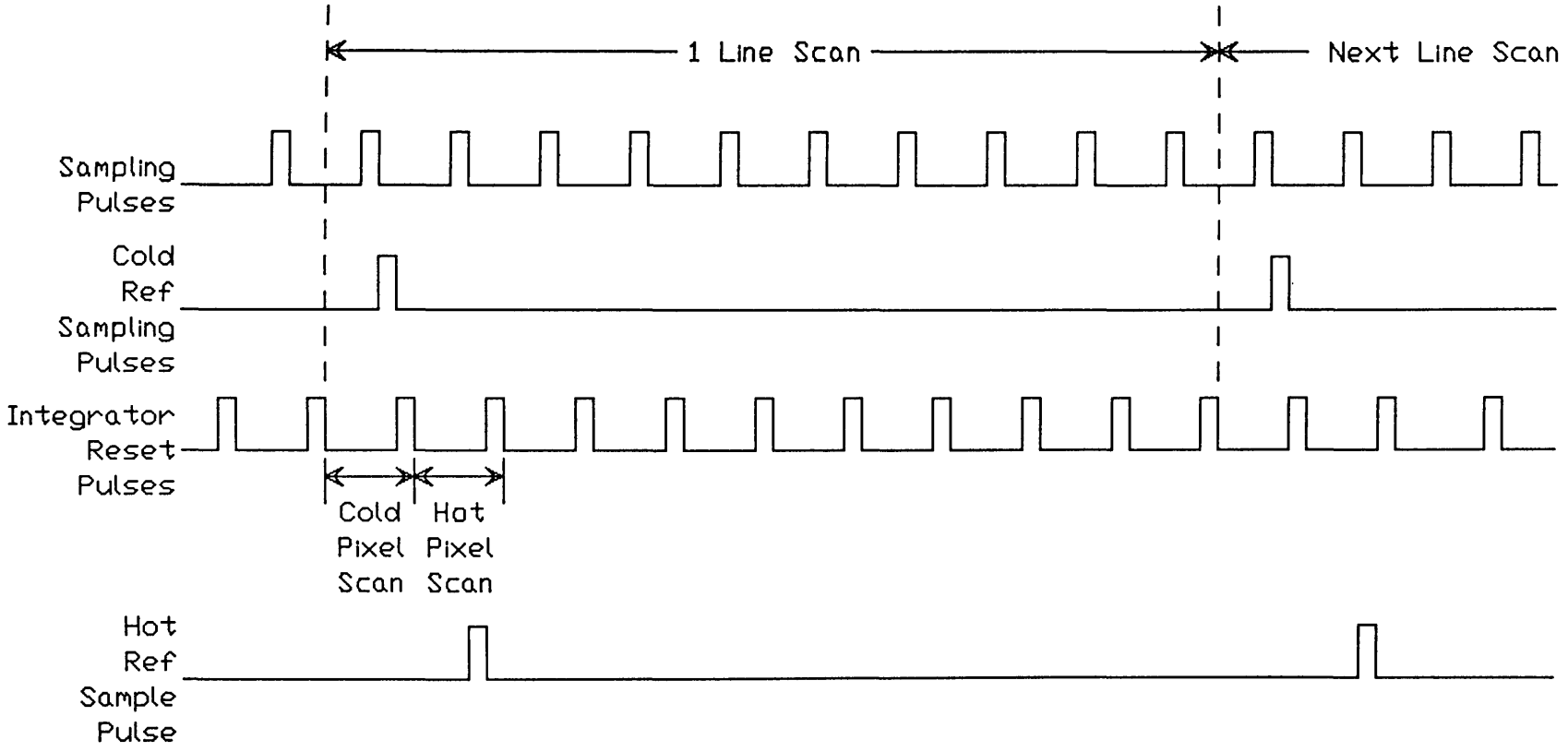

Figure 2.6. Timing of Thermal Reference Sampling Pulses.

the hot reference sampling until later in this chapter, but it is also shown here. For clarity, only 10 sampling pulses have been used to represent one line scan, rather than the actual number of 620. Upon comparison with Figure 1.9 it is seen that the cold reference sample pulse has been inserted between the high speed sampling pulse and its integrator reset pulse for one particular cold pixel. This is to allow sufficient time for the transfer of charge to "ripple down" through the processing circuitry before resetting of the integrator. Note that the reference sampling only occurs once per line scan and its frequency is thus equivalent to the FPA scanning rate of 30 Hz.

The premise of the background subtractor circuit follows. Referring again to Figure 2.5 it is seen that the Sample and Hold output voltage can be represented by $V(T_k)$ where k denotes the current pixel and T the thermal content of that pixel. Likewise, the sampled voltage occurring by dwell of a cold reference pixel is denoted by $V(T_c)$. As briefly discussed above, the FET switch is activated to obtain a sample of $V(T_c)$ across capacitor CB, at the beginning of each channel. This reference voltage should then be maintained for the length of the existing line scan period, or approximately 33 msec.

During the remainder of the scan the FET switch is inactive, providing a very high impedance to ground. Additionally, CB does not have an efficient discharge path

owing to the use of high impedance buffering. Thus, the incoming DC contributions are effectively blocked and only the desired image variations are allowed passage by CB, a form of AC coupling. The output can be mathematically described as:

$$V(T_k) - V(T_c) = V(T_I) \qquad \{2.7\}$$

where $V(T_I)$ represents the signal attributed to the desired image point in volts.

This implies that the charge on CB must be maintained for a significantly longer time than was required for the high speed sample and hold capacitor CS.

Equation {2.5} may again be used to describe this reference sampling process. However, now realize that V_{CB} replaces V_{CS}, $V(T_c)$ correlates to V_I, and the initial voltage on CB is that of the cold reference maintained from the previous line scan or $V(T_{c-1})$. The describing equation is presented below:

$$V_{CB} = V(T_C)\ [1-\exp^{(\frac{-t}{r \cdot CB})}] + V(T_{C-1})\ \exp^{(\frac{-t}{r \cdot CB})} \qquad \{2.8\}$$

where V_{CB} is the instantaneous voltage across capacitor CB in volts

$V(T_c)$ is the voltage output from the preceding Sample and Hold circuit during dwell on a cold reference pixel in volts

$V(T_{c-1})$ is the initial voltage residing on CB, maintained since the previous line scan

Again note that the cold reference control pulse width should be at least 5 time constants in order to ensure that V_{CB} is an accurate measurement of $V(T_c)$.

Returning to equation {2.6} in like fashion will yield the following equation which describes the voltage across CB during the line scan:

$$V_{CB} = V(T_C)[\exp^{(-\frac{-t}{Z \cdot CB})}] \qquad \{2.9\}$$

where V_{CB} is the instantaneous voltage across the capacitor in volts

$V(T_c)$ is the initial capacitor voltage immediately after deactivation of the FET control pulse

As before, note that if the time constant Z·CB is at least 100 times greater than the 33 msec line scan period, $V_{CB}(t)$ will remain within 1 percent of $V(T_c)$. Assuming this requirement is met, the voltage across CB cannot vary significantly (will not change instantaneously or otherwise) and the output will be as described in equation {2.9} above.

It is assumed that an inverting buffer can be achieved if so desired to produce an output of $V(T_c) - V(T_k)$, but this is not considered within this paper. The complete background subtraction circuit is therefore represented by Figure 2.7, which is merely a compilation of Figures 2.2 and 2.5. Note the addition of another unity gain buffer, necessary for implementation of multiplexing n channels in VLSI form.

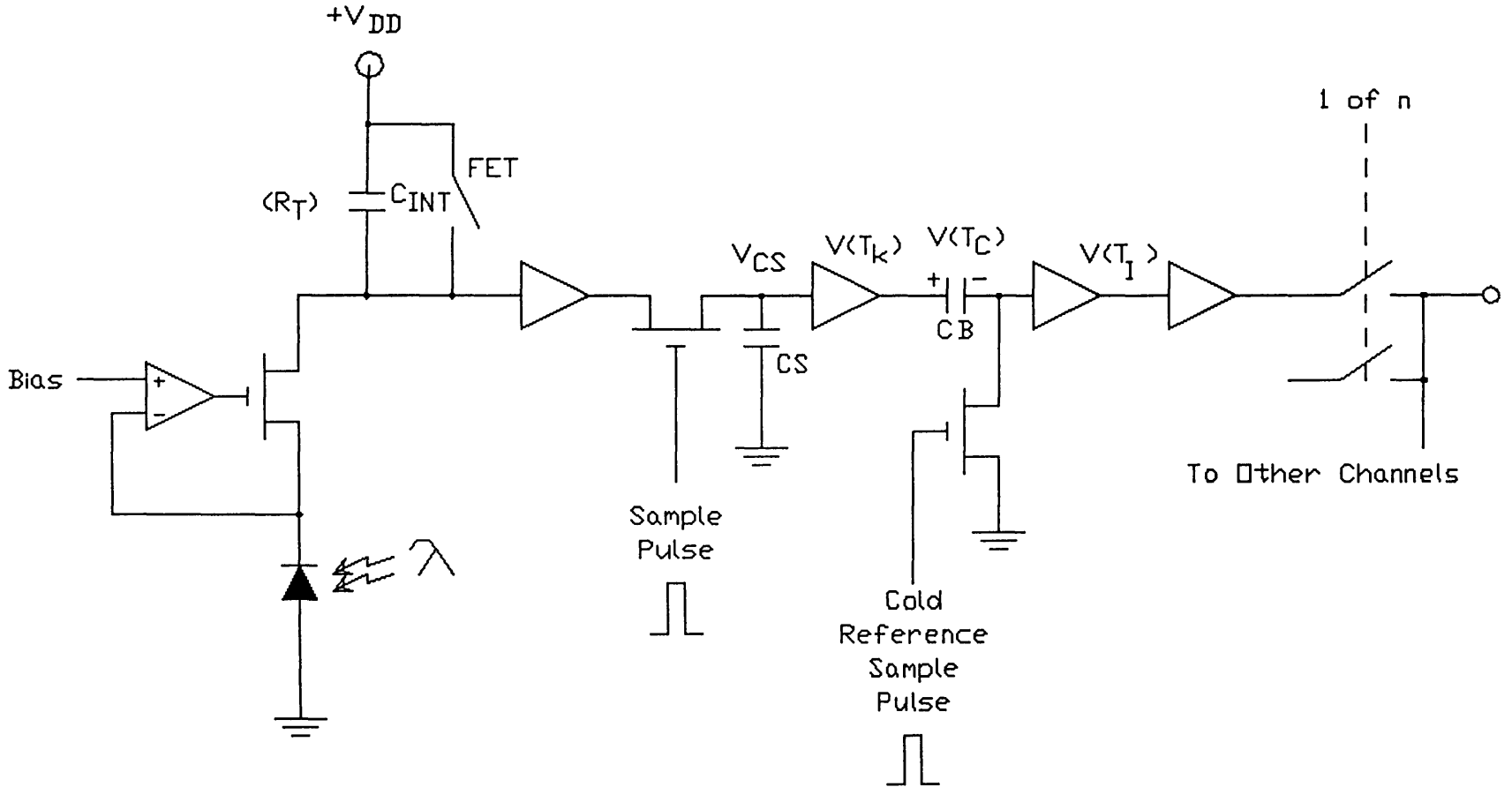

Figure 2.7. Complete Background Subtraction Circuit.

Pulse Width Modulation

Having removed the background contribution and produced $V(T_I)$, another correction is required for the Responsivity of each channel. This is necessary to ensure that two unique detectors with different gains can reproduce the same thermal image content. Consider the circuit presented in Figure 2.8. One more sample will be obtained but this time it will correspond to the detector's dwell on a hot reference pixel. The assumption here is that no scene pixel can be hotter than the hot thermal reference, a good approximation for most thermal systems. This characteristic can be used to provide a means of real-time gain correction.

The first processing mechanism is another Sample and Hold, where CH is now the storage capacitor. The FET shall be turned on by the hot reference sample pulse, in accordance with the timing diagram of Figure 2.6. This should again occur only once per channel after several hot pixel scans, to allow settling of the system capacitors. Note that this sample pulse has the exact relationship with respect to the high speed sampling and integrator reset pulses that the cold reference sample pulse utilized, and for the same reason.

The sampling gate is activated when $V(T_k) = V(T_h)$ where $V(T_h)$ is the sampled voltage occurring by dwell of a hot reference pixel. Therefore the sample obtained by CH will be $V(T_h) - V(T_c)$, denoted as $V(T_r)$ or the difference between samples of the hot and cold thermal references for each line

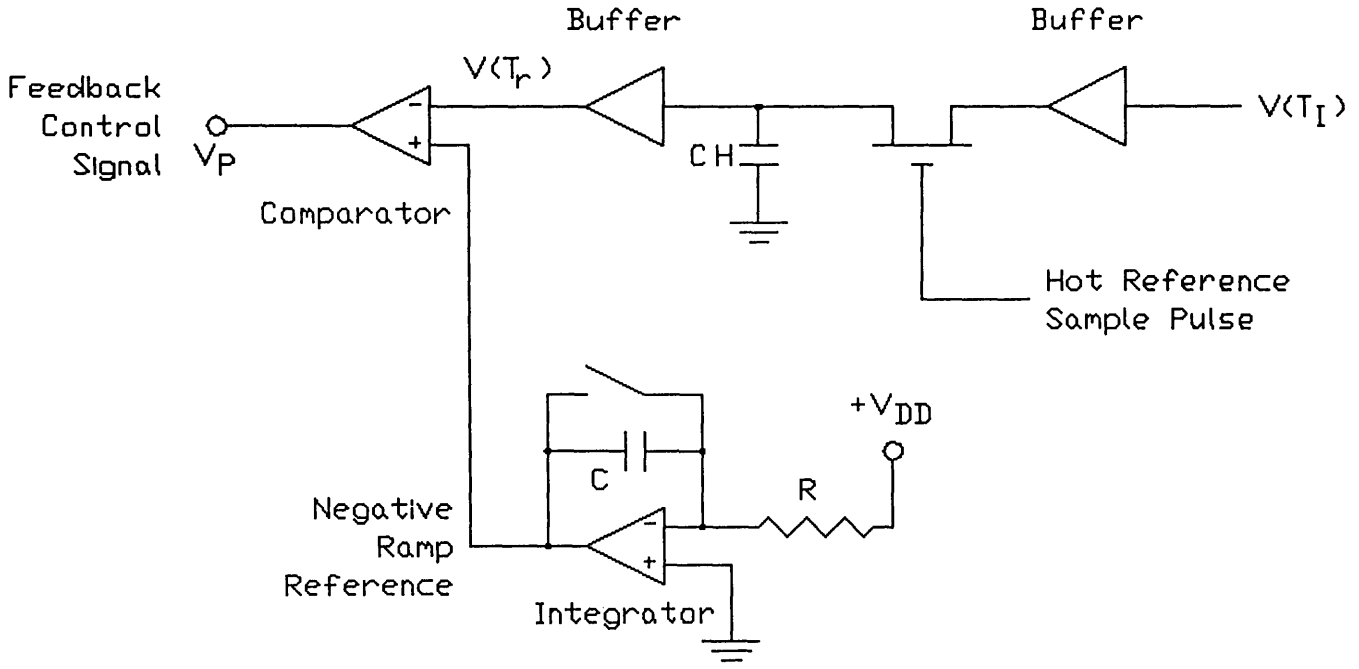

Figure 2.8. Generation of Feedback Control Signal.

scan. This voltage difference is dependent on the gain or Responsivity of the individual detector since all channels will view exactly the same reference sources. By implementing this information in some form of feedback control loop, real-time correction can be obtained for each channel.

The output of this sample and hold stage can be described by the following equation during the sample state:

$$V_{CH} = V(T_r)\ [1-\exp^{(-\frac{-t}{r \cdot CH})}] + V(T_{r-1})\ \exp^{(-\frac{-t}{r \cdot CH})} \qquad \{2.10\}$$

where V_{CH} is the instantaneous voltage across capacitor CH in volts

$V(T_r)$ is the voltage input to the sampling gate in volts, the difference between hot and cold reference pixels

$V(T_{r-1})$ is the initial voltage residing on CH, maintained since the previous line scan

The hot reference control pulse width should be at least $5 \cdot r \cdot CH$ to produce a sampled voltage $V_{CH}(t)$ within 1 percent of $V(T_r)$.

The reference difference $V(T_r)$ should also be maintained for the length of the existing line scan period or approximately 33 msec. In order to achieve this, the time constant $Z \cdot CH$ in the following equation should be at least 3.3 seconds (100 times greater):

$$V_{CH} = V(T_r)\ [\exp^{(-\frac{-t}{r \cdot CH})}] \qquad \{2.11\}$$

where V_{CH} is the instantaneous voltage across the capacitor in volts

$V(T_r)$ is the initial capacitor voltage immediately after deactivation of the sampling gate

Upon acquisition of $V(T_r)$, a comparison will be performed with a fixed ramp reference. Recalling Figure 1.7 it is seen that $V(T_c)$ will always be greater than $V(T_h)$, thus making $V(T_r)$ a negative quantity. The absolute magnitude of $V(T_r)$ will increase with larger disparities between hot and cold reference samples. Thus a means should be provided which can produce compensation.

Shown in Figure 2.9 is a negative ramp reference and two typical values of $V(T_r)$, attributed to two unique detectors 1 and 2. Note that the reference ramp is generated by the integrator of Figure 2.8 and that this circuit is reset exactly in accordance with the BDI integrator timing, shown in Figure 1.9. By using a comparison between each value of $V(T_r)$ and the fixed ramp reference, a pulse output is achieved whose width is dependent on the magnitude of $V(T_r)$. The pulse widths are denoted by $V(P_n)$ where n is the detector channel of interest, shown for the two $V(T_r)$ samples in Figure 2.9.

By implementing the outputs $V(P_n)$ as a feedback control signal, modulation of the initial BDI integration period can be achieved. The complete circuit is presented in Figure 2.10 by merging Figures 2.7 and 2.8. Note the addition of an extra FET switch for resetting of the initial integration process.

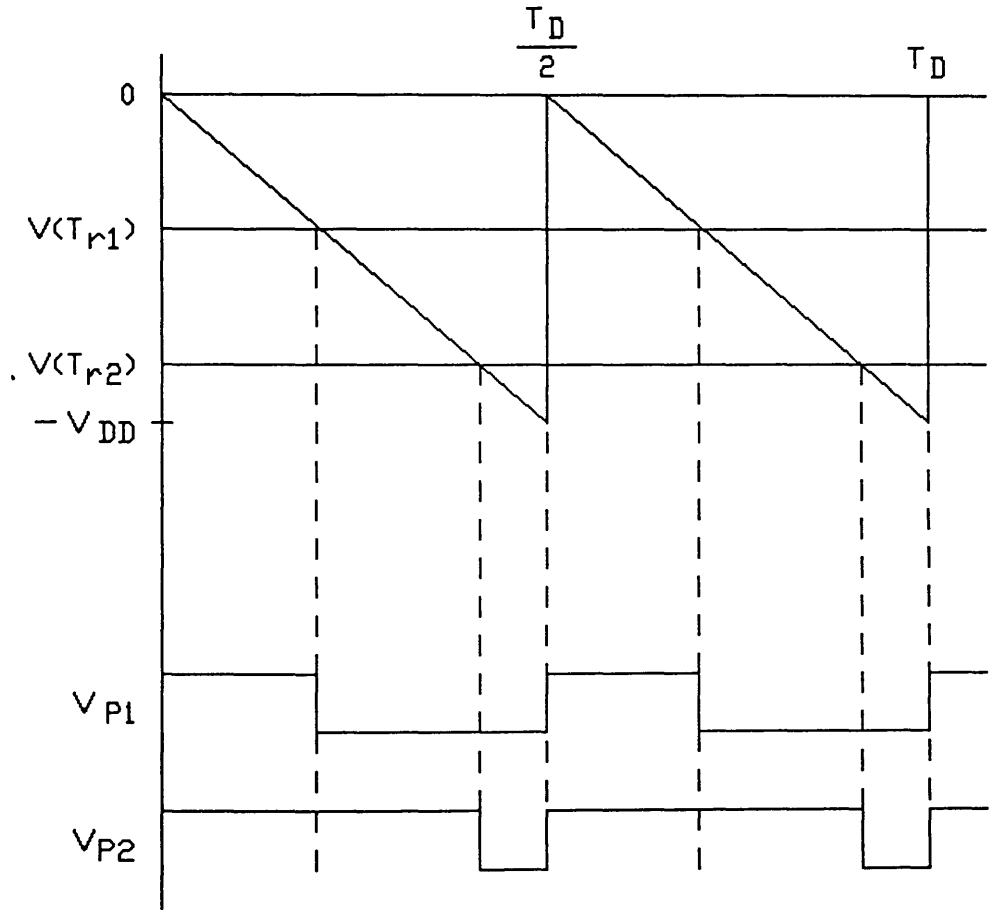

Figure 2.9. Comparator Inputs and Outputs for 2 Unique Detector Channels.

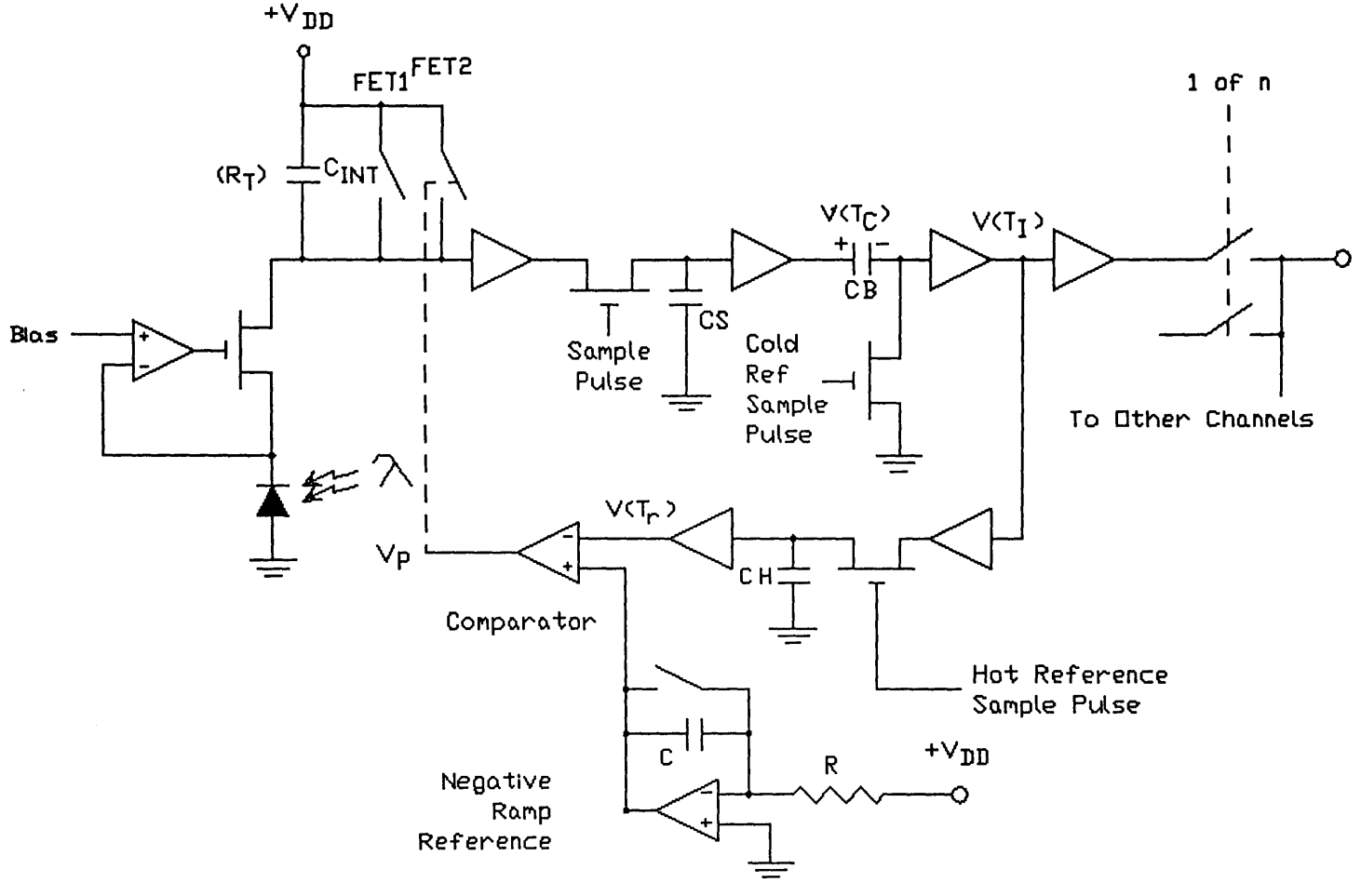

Figure 2.10. Complete Uniformity Correction Technique.

That is, if either FET1 or FET2 is activated, the initial processing circuit is held in reset. FET1 is controlled by the normal reset pulse as detailed in Figure 1.9. FET2 is controlled by $V(P_n)$, thus allowing longer integration times for less responsive detectors and shorter integration times for detectors having more gain.

As discussed earlier, the image term can vary as much as ± 50% due to the three variables ϵ, A, and ϕ_I. Therefore, the pulse width modulation scheme presented here should provide an approximate transfer characteristic in accordance with Figure 2.11. Slope m is basically used to multiply the BDI integration period, dependent on the value of $V(T_r)$. Recall that $V(T_r)$ is a negative quantity so that its minimum value is actually the largest difference magnitude, representative of a detector with highest Responsivity. In this case, it is desired to implement the shortest integration time (duty cycle of .32) so the integrator reset FET2 is activated for 68% of the period, holding the circuit in an initial state. Alternatively, if a detector possessed the least amount of Responsivity, corresponding to a minimum difference magnitude and therefore maximum value of $V(T_r)$, the BDI integration should be allowed to occur with a very large duty cycle of .98. FET2 would then be activated for only 2% of the integration period.

Returning to Figure 2.9 it is observed that detector channel 1 has lower gain than that of channel 2 as evidenced

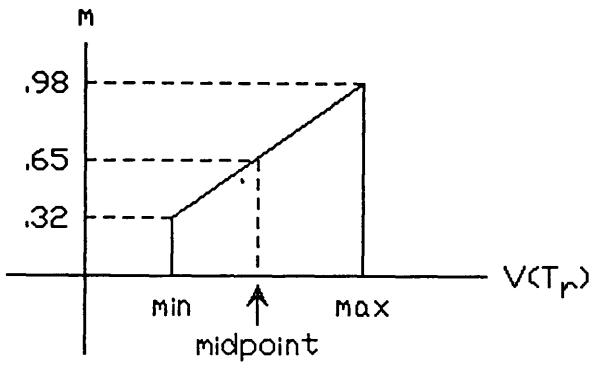

Figure 2.11. Modulation Transfer Characteristic.

by the fact that $V(T_{r1})$ is greater than $V(T_{r2})$. By implementing the comparison process the waveforms V_{Pn} are produced with which to activate FET2. Note that V_{P1} allows approximately 60% duty cycle for the BDI integration period and that V_{P2} only allows 20%. In this manner, the lower gain of channel 1 may be compensated to yield the same results as channel 2. In Chapter 3 a design example is constructed which demonstrates the entire technique of background subtraction and pulse-width modulation for uniformity correction.

CHAPTER 3: DESIGN EXAMPLE

During the composition of this paper several prototype circuits were constructed to demonstrate feasibility of this method of uniformity correction. These are presented here. Additionally, it was necessary to establish conditions which closely approximated their description in prior chapters. Deviations from actual system parameters are so noted.

In selecting active components for the design example, CMOS circuitry was a first consideration, owing to its direct compatibility with VLSI production techniques. There are many digital and linear CMOS devices currently in industry and thus a wide selection exists. Texas Instruments was the primary vendor considered for linear devices such as operational amplifiers and comparators, part of its LinCMOS product line. Part number TLC271 was the single op-amp used for implementing all integrators and unity gain buffers. The voltage comparator utilized was part number TLC372. National Semiconductor and Motorola devices were used interchangeably for digital control purposes, employing 4000 series CMOS circuitry.

The entire circuit was operated from ±5 VDC power rails, with sufficient bypass capacitors (.1 uF) adjacent to each

integrated circuit. All programmable operational amplifiers were used in their high bias mode in order to provide the maximum slew rate of 4.5 volts per microsecond. For clarity these connections are not shown on the following schematics. Reference designations have also been assigned to each discrete part.

Military grade components were used where possible. These include ceramic capacitors (MIL-C-39014) and metal film resistors (MIL-R-39017) for integration, sampling and timing circuitry.

The purpose of the design example is to provide an implementation of uniformity correction for one detector channel. Provision was made to vary the cold and hot thermal reference voltages and thus simulate detectors having different Responsivities. Figure 2.10 depicts the actual circuit we wish to implement using practical devices.

Line Scan Simulation

Consider the simulation of detector and BDI preamplifier during a single line scan. As the detector is passed across the FOV, it first observes cold and hot reference pixels and then the scene of interest. The scene normally contains many pixels with various thermal contents but with magnitudes between that of the cold and hot reference pixels. Each reference was achieved by injecting a DC voltage for 10% of the line scan period. During the remaining 80% of the line

scan the variations in scene pixels were simulated by driving the circuit with a sinusoidal voltage. The maximum and minimum values (peaks and valleys) of the sine wave were limited to ensure that they did not exceed the reference voltages.

Operation from dual power supplies allowed generation of the cold reference from -5 VDC and the hot reference from +5 VDC. These reference voltages were made adjustable via trimpots as shown in Figure 3.1. The cold reference produced settings between approximately -1 and -2 VDC, and the hot reference between +1 and +2 VDC. Finally, the sinusoidal input had a maximum value of +1 VDC and a minimum of -1 VDC. Each of the three signals were input to an integrator circuit at different points in time, via CMOS analog switches (base part number 4066). This nearly duplicates the BDI integration process described in Chapter 1. The provided control logic and timing signals satisfy the requirements of Figure 2.6 and will be presented later in this chapter.

Applying a voltage at the integrator input equates to current injection since the negative op-amp terminal is a virtual ground. The current is set by the ratio of input voltage to resistance R4. For the voltages used here, the input currents vary between approximately -3.5 microamperes and +3.5 microamperes. The current attributed to the sinusoidal voltage input fluctuates between -1.8 and +1.8

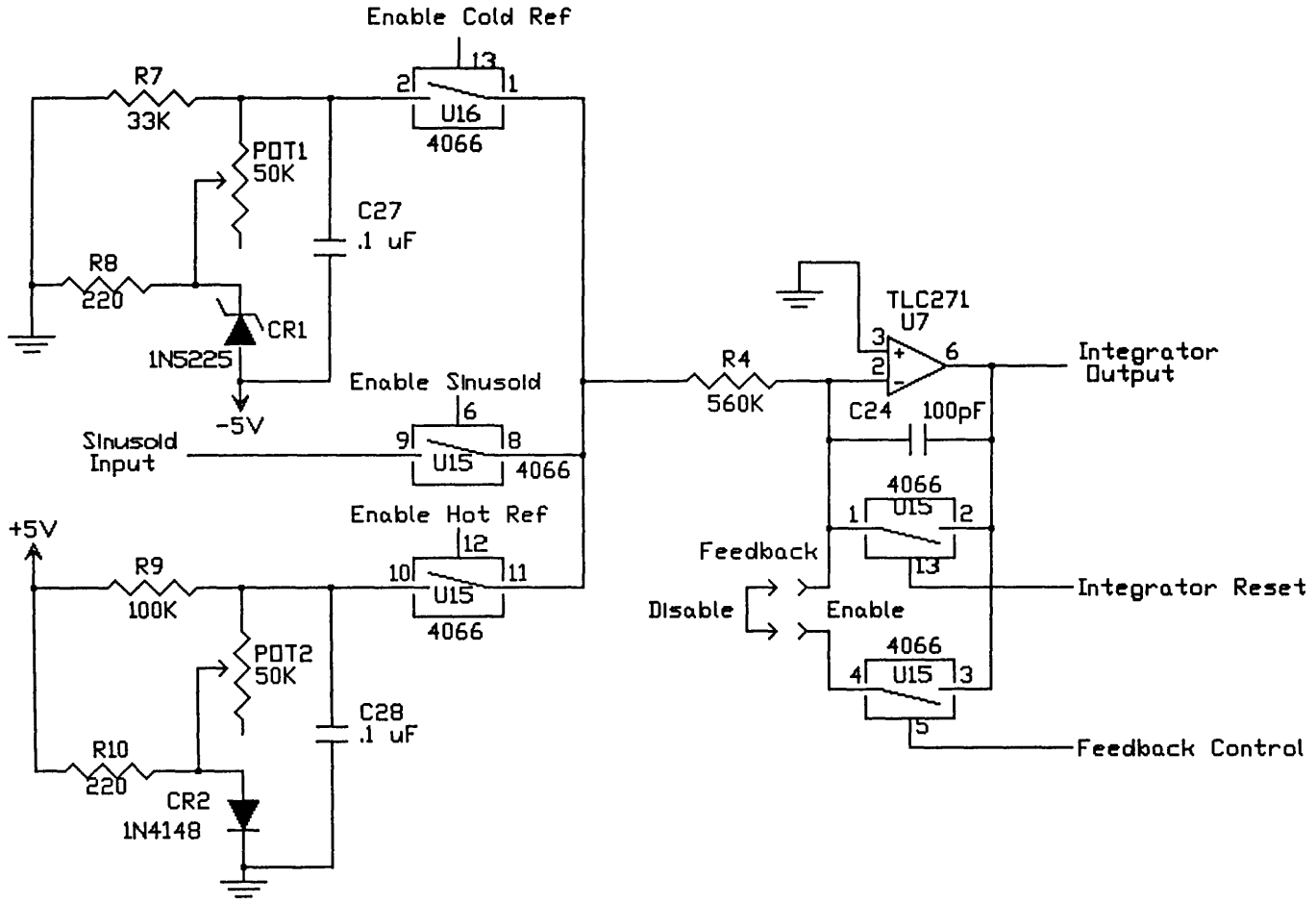

Figure 3.1. Line Scan Simulation.

microamperes. These currents are about 20 times greater than actual photocurrents detected by real thermal systems.

The integration period chosen for the design example is equivalent to one pixel dwell. Thus, increasing SNR by double integration and double sample correlation is not considered. Each integration period is nominally 59 usec, close to the actual dwell time of 53.76 usec presented in Chapter 1. The high speed sampling then occurs at an approximate rate of 17 KHz. The Nyquist sampling criterion is observed by limiting the sinusoidal input frequency to less than 8.5 KHz.

The integrator output is essentially the voltage across its capacitor. This voltage will change with respect to time as the circuit's input current will charge the capacitor. This rate of change in volts per second is determined by the ratio of input current to C_{INT}. In the design example, the capacitor value chosen was 100 picofarads to avoid saturation of the operational amplifier. With a 100 pF capacitor and a maximum input current of ±3.5 uA, the voltage output cannot exceed -/+2 volts in the dwell time of 59 usec. The integrator is then reset to 0 volts, allowing a maximum output of ±2 volts at the end of the integration period, dependent on the thermal content of the pixel.

Note that the cold reference injects a negative voltage into the integrator, producing a positive ramp. Likewise, the hot reference input is positive, yielding a negative ramp output. This satisfies the condition of Figure 1.7 in that

the hotter pixels will produce smaller output voltages at the end of the integration process. The sinusoidal input will yield ramps whose slopes fall between those of the hot and cold references, dependent on the sign and magnitude of the time-varying voltage.

The sinusoid input was generated by a function generator, Circuitmate model number FG2. The frequency was varied between 50 Hz and 8 KHz and the peak amplitude was limited to ±1 V. Within this paper only 2 frequency inputs will be presented on the scope photographs, 200 Hz and 2 KHz. This is considered sufficient for demonstration.

The output of the design example integrator is shown in Figure 3.2 for a cold thermal reference of -2 volts and a hot thermal reference of +2 volts. The sinusoidal input is set at 200 Hz and is asynchronous with respect to the system timing. Figure 3.3 presents the integrator output for a sine wave input of 2 KHz and reference voltages of -1 V cold and +1 V hot. The top waveform is the integrator input and the output is then shown as the lower waveform. Note that for both cases the sine wave yields slopes which do not exceed the thermal reference outputs, as stated earlier.

The circuit of Figure 3.1 will be used as the foundation for subsequent processing circuitry. Therefore, the designated input and output signals will be located on other schematics presented later in this chapter. The 2 analog switches for resetting of the integrator correspond to those

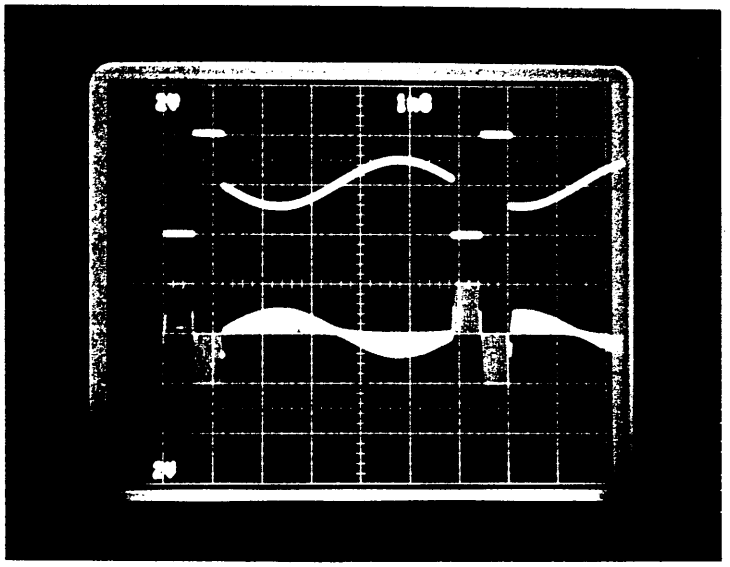

Figure 3.2. Integrator Output for ±2 V Reference and 200 Hertz Sinusoid Inputs.

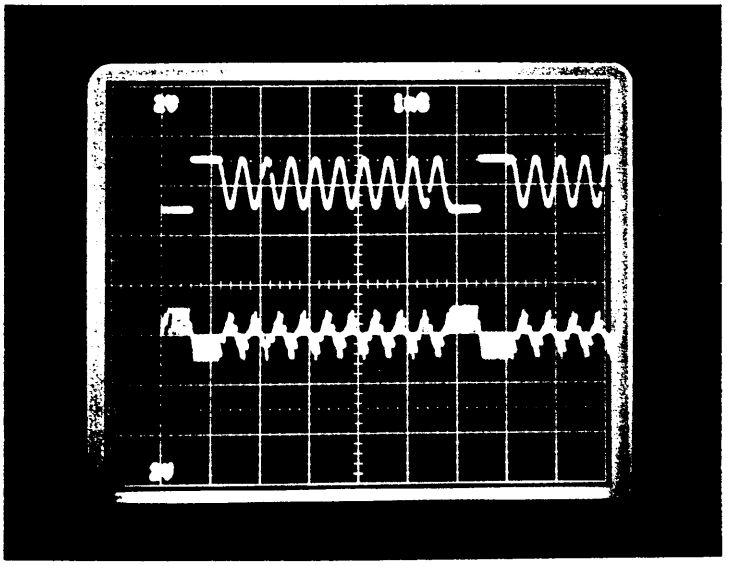

Figure 3.3. Integrator Output for ±1 V Reference and 2 KHz Sinusoid Inputs.

of Figure 2.10. A single jumper was also incorporated to allow manual enabling and disabling of the pulse-width modulation feedback loop.

Signal Path

The remainder of the forward path implements the high speed sample and hold and background subtraction technique previously depicted in Figure 2.7. The actual circuit schematic is presented in Figure 3.4.

The high speed sampling occurs at approximately 17 KHz. Typical "on" resistance of the 4066 analog switch can be 100 ohms at an ambient temperature of 25° C. By selecting a capacitor of 1000 pF, one charging time constant is calculated to be 100 nsec. Thus in 5 time constants or .5 usec, the capacitor can accurately sample the integrator output. The sample pulse width utilized was indeed .5 usec, significantly smaller than the dwell time of 59 usec. Since the maximum slope change of the integrator can be 2 volts in 59 usec, the output will change by only 17 millivolts during the .5 usec sampling, worst case. This sampling pulse occurs just prior to the integrator reset signal, allowing thermal reference sampling when required in accordance with Figure 2.6.

The capacitor discharge was negligible due to the high impedance buffering of the TLC271 device. This part has a typical input impedance in excess of 10^9 ohms, making one discharge time constant approximately 1 second. Using

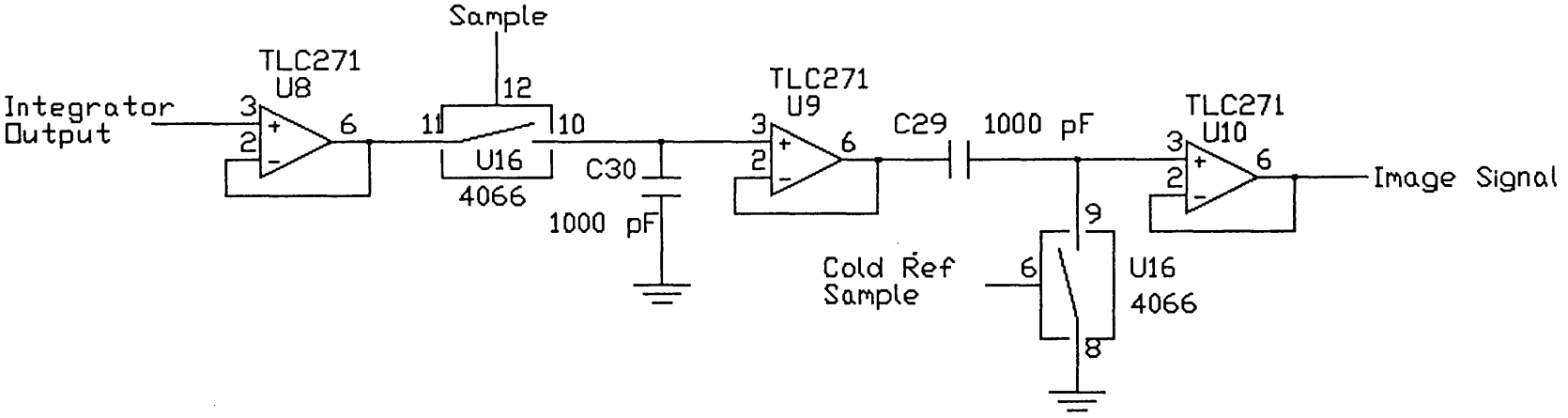

Figure 3.4. Forward Path Implementation.

equation {2.6} it is seen that the capacitor will retain voltage within 1 percent, even after a dwell of 59 usec. Figure 3.5 displays the sample and hold output for the input of Figure 3.2. Likewise, Figure 3.6 presents the sampled output of Figure 3.3. On these scope photographs, the integrator output is the top waveform and the lower waveform is the sampled output.

The background subtraction mechanism also used a 1000 pF capacitor, 4066 analog switch, and TLC271 op-amp buffer. Due to the ease in implementation, the design example simulated 100 pixels per line scan rather than the specified number of 620. Therefore capacitor C29 did not have to maintain the cold reference voltage for as long as would normally be required. However, for this prototype the line scan period is 5.9 msec, equating to a frame scan frequency of about 170 Hz. As before, the discharge time constant is calculated to be 1 second, which substantially exceeds the line scan period by more than 100 times. Thus equation {2.9} is satisfied and the cold reference sample will be maintained within 1 percent until the next line scan. The cold sample pulse width was also .5 usec, sufficient for accurate charge transfer as detailed above. The timing of this signal is in accordance with Figure 2.6 and will be presented later.

The subtractor output for the input of Figure 3.5 is shown in Figure 3.7 and for the input of Figure 3.6 is shown in Figure 3.8. Again, the top waveforms represent the inputs.

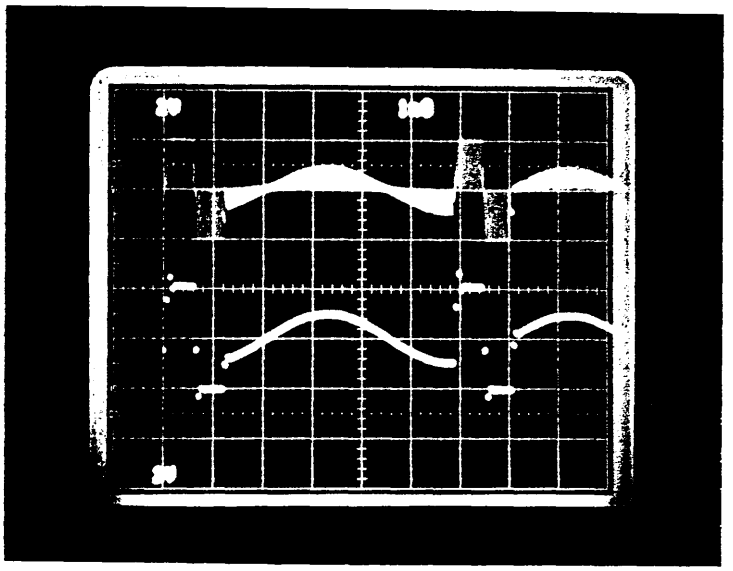

Figure 3.5. Sampled Output for the Input of Figure 3.2.

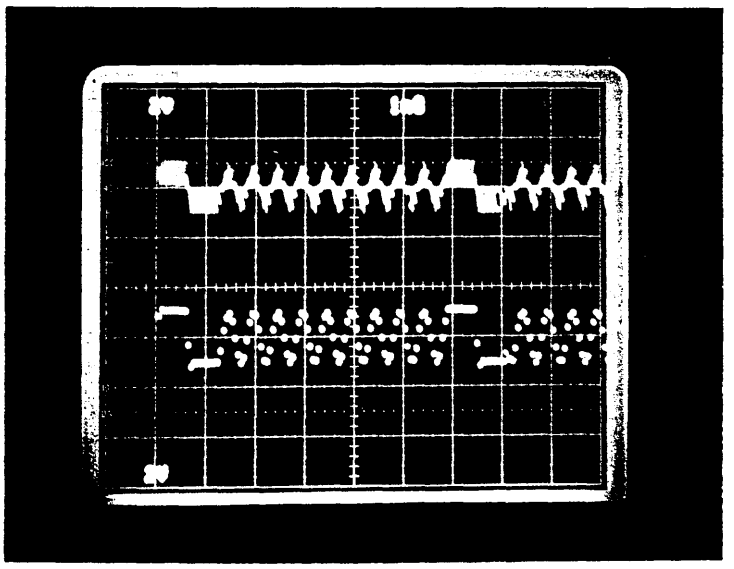

Figure 3.6. Sampled Output for the Input of Figure 3.3.

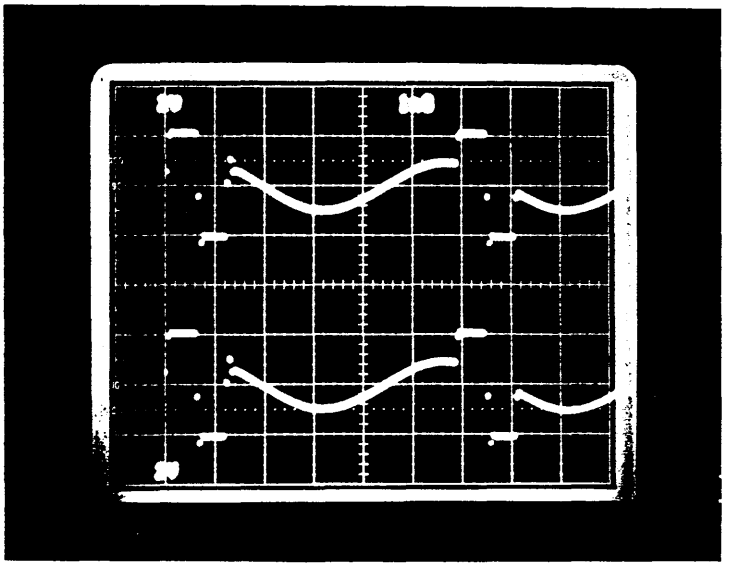

Figure 3.7. Subtractor Output for the Input of Figure 3.5.

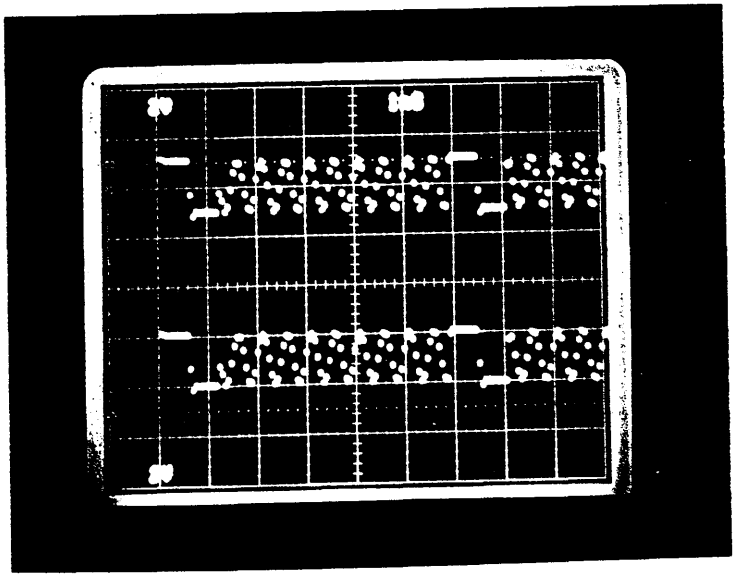

Figure 3.8. Subtractor Output for the Input of Figure 3.6.

Upon observation of the lower waveforms it is seen that the output of the subtraction circuit has been displaced by the value of the cold reference sample. Recall that this sample corresponds to the background flux for most thermal systems. Therefore true background subtraction was obtained. The upper waveform displays the preceding sample and hold output with background signal.

Feedback

The feedback portion of the design example was constructed to generate a control signal for pulse-width modulation of the BDI integration process. This circuit is shown in Figure 3.9 and closely approximates the concept of Figure 2.8. Although multiplexing of n channels was not implemented, an additional buffer was added to the circuit in anticipation of future prototype use.

The sample and hold (which corresponds to dwell on a hot reference pixel) is an exact duplicate of the high speed sample and hold except that it is strobed at the frame rate of 170 Hz. This sample is sufficient for the length of the line scan period for the same reasons as the cold reference sampling mechanism presented above. As stated in Chapter 2, the sample obtained will represent the difference between cold and hot thermal references. This reference difference will then be compared to a fixed ramp reference.

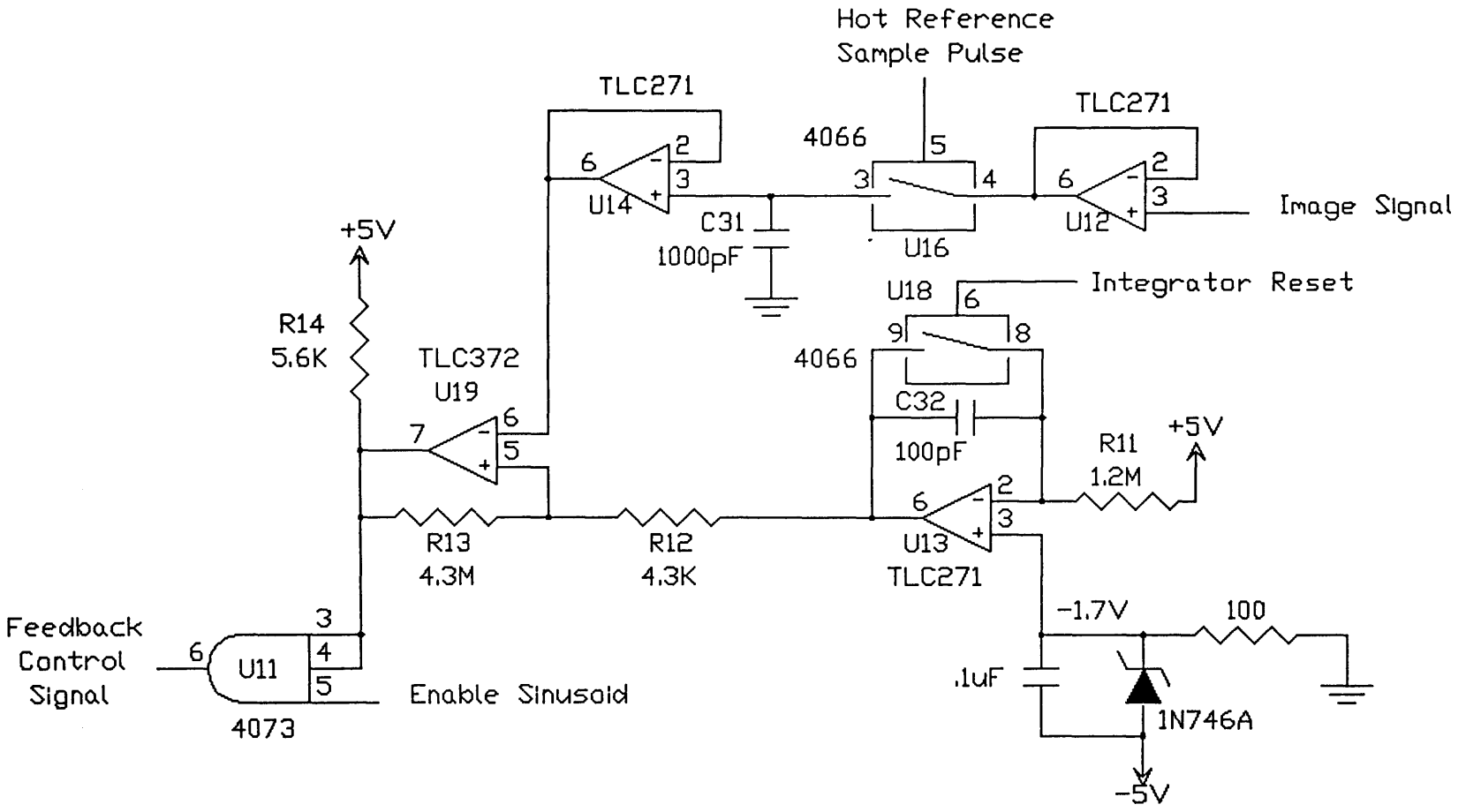

Figure 3.9. Feedback Implementation.

The negative reference ramp was generated by integrating a positive DC voltage as shown in Figure 3.9. This circuit is initialized with the same reset pulse as the BDI integrator, at the frequency of 17 KHz. However, the reference slope is reset to -1.7 V rather than 0 V. For the input voltage of +5 VDC, the ramp can attain -5 VDC at the end of the 59 usec period with an input resistance of 1.2 Megohms. This is necessary when considering the difference between hot and cold reference samples and the transfer characteristic of Figure 2.11.

Recall Figure 2.9 and the subsequent comparison process to be performed. With the maximum reference samples (cold/hot) of ±2 VDC, the measured value for $V(T_{rn})$ can be negative 4 VDC since it is simply the hot sample minus the cold sample. Even for this worst case disparity, a pulse should be produced such that the BDI integration can occur with a 32% duty cycle, in accordance with Figure 2.11. With the minimum reference samples of ±1 VDC, the value for $V(T_{rn})$ is -2 VDC. In this case a control pulse should be provided which will provide BDI integration with a 98 percent duty cycle. The constructed circuit closely approximates this transfer characteristic.

Shown in Figure 3.10 is the negative reference ramp (top waveform) and the comparator pulse output for the maximum thermal difference, ±2 V. This corresponds to a detector with highest Responsivity. Note that this signal will provide the

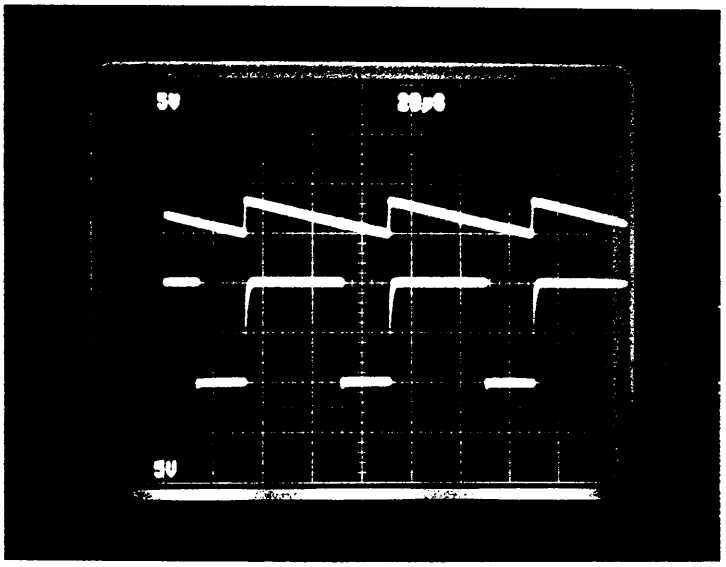

Figure 3.10. Pulse Width Output for Highest Gain Detector.

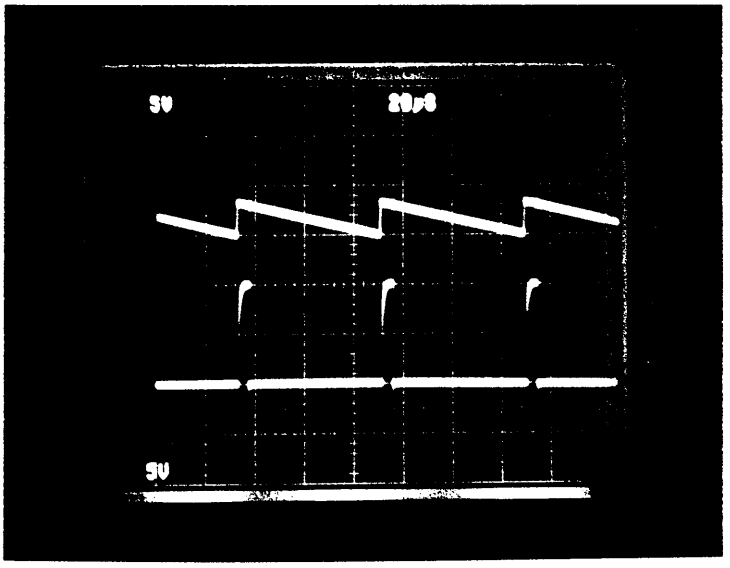

Figure 3.11. Pulse Width Output for Lowest Gain Detector.

least amount of integration when used to control the reset FET of Figure 3.1.

Figure 3.11 shows the pulse width output for a detector with the lowest amount of Responsivity. In this case the minimum thermal difference of ±1 V has been introduced. This control signal will provide the maximum BDI integration time.

The comparator used is TLC372, also from Texas Instruments LinCMOS family. It has a response time of 200 nsec which is sufficient for this application. Hysteresis was added, in order to switch cleanly through the transition points. A pullup resistor was incorporated on its open drain output for driving the input of the subsequent CMOS gate.

The CMOS AND gate was necessary to provide the feedback control signal only during the scanning of the scene and not the thermal references. That is, for each thermal reference full BDI integration is utilized. This is necessary since it is exactly this information which is sampled to provide modulation of the scene pixel integration.

Control Logic

Figure 3.12 presents the digital control circuitry built for the design example. At the heart of the system timing is Texas Instruments' TLC555 (designated as U1), another CMOS device. This timer circuit is operated with a 50% duty cycle at approximately 17 KHz. Each clock period is then 59 usec and corresponds to the dwell time of one pixel. The clock

output at U1-7 is asynchronous with respect to the sinusoid input.

This clock is input to three different circuits as shown in Figure 3.12. One circuit is comprised of 4528 monostable multivibrators (U4 and U5) which are daisy-chained to generate the pulses required for high speed sampling, reference sampling, and integrator resetting. Each one-shot is configured as non-retriggerable and is activated by the falling edge of the preceding pulse. In this manner, overlapping of pulses is precluded and the relationship presented in Figure 2.6 is maintained. The timing relationships are presented as part of Figure 3.13.

U2 and U3 are also daisy-chained and represent another circuit which accepts the 17 KHz clock. These two devices are decade counters with decoded outputs (base part number 4017) and are used to divide the 17 KHz clock into usable time frames with which to simulate the cold, hot, and scene pixel scanning periods. A simple divide by 10 is the function of U2. This circuit thus provides a single clock output at U2-12 for every 10 clock inputs from U1-7. This signal is used by yet another 4017 decade counter, U17, in the generation of thermal reference sampling pulses.

By providing U17 with the same 17 KHz clock and using the inverted U2-12 output as its reset signal, the two counters are synchronized with respect to each other and the timing is as presented in Figure 3.13. Note that the output

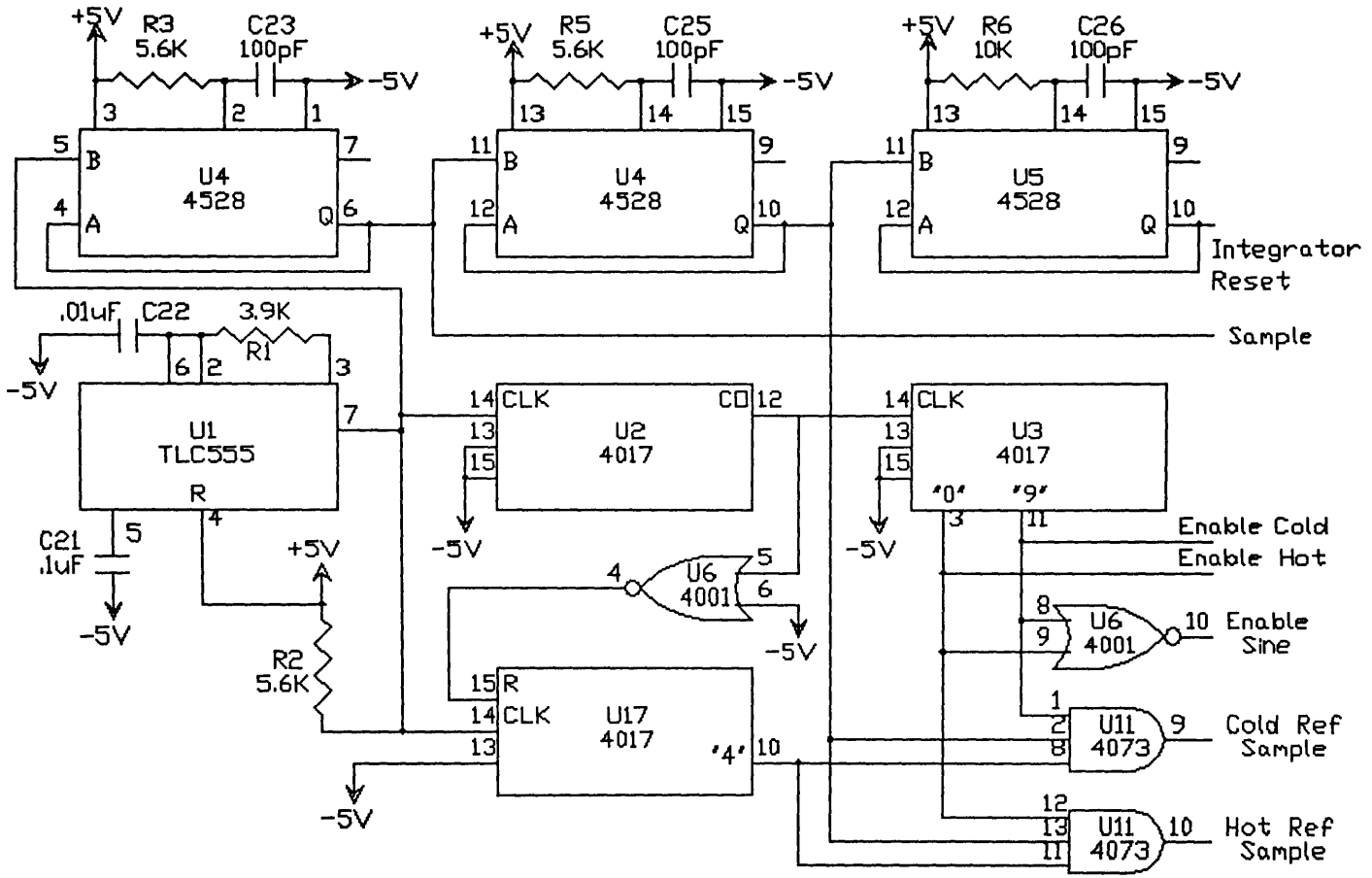

Figure 3.12. Digital Control Circuitry.

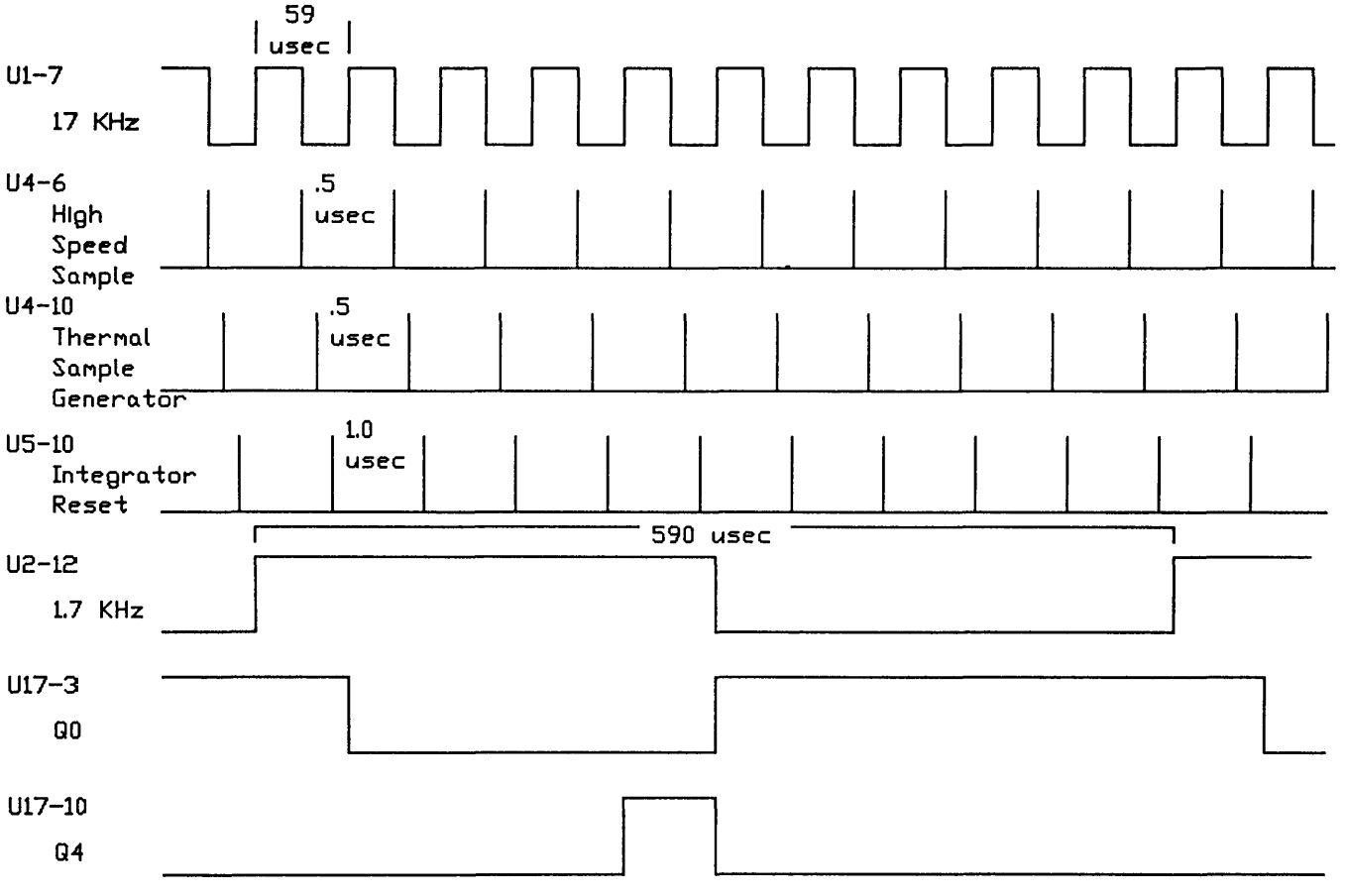

Figure 3.13. Timing Diagram -- Pulse Generation.

at U17-10 only occurs once during each cycle of U2-12, just prior to the center, falling edge of the U2 output. This is very useful in the generation of the thermal reference sampling pulses.

First, the output of U3 should be considered. This device is employed to further divide the output of U2-12. Therefore, each decoded output of U3 represents one clock input of 1.7 KHz (or 10 clock cycles of the 17 KHz waveform) as shown in Figure 3.14. Note that the frequency remains 1.7 KHz, but with a .10 duty cycle. By using these decoded outputs in controlling 4066 analog switches, scanning of the thermal reference and scene pixels may be simulated.

The design example used the output of U3-11 to control the switching of the cold reference voltage to the integrator of Figure 3.1. Likewise, the output of U3-3 was used to enable the hot reference voltage. Each signal therefore represented 10% of a single line scan or the simulation of 10 pixel dwells for each reference. Finally, the scene pixels were considered by gating the two U3 outputs with the NOR circuit U6 (part number 4001). This output at U6-10 is also presented in Figure 3.14 and was used to enable the sinusoidal input for 80% of each line scan period.

The output of U17-10, U4-10, and the two outputs of U3 were then employed to produce one sampling pulse per thermal reference every line scan. The cold reference sample pulse is necessary for the background subtraction technique in the

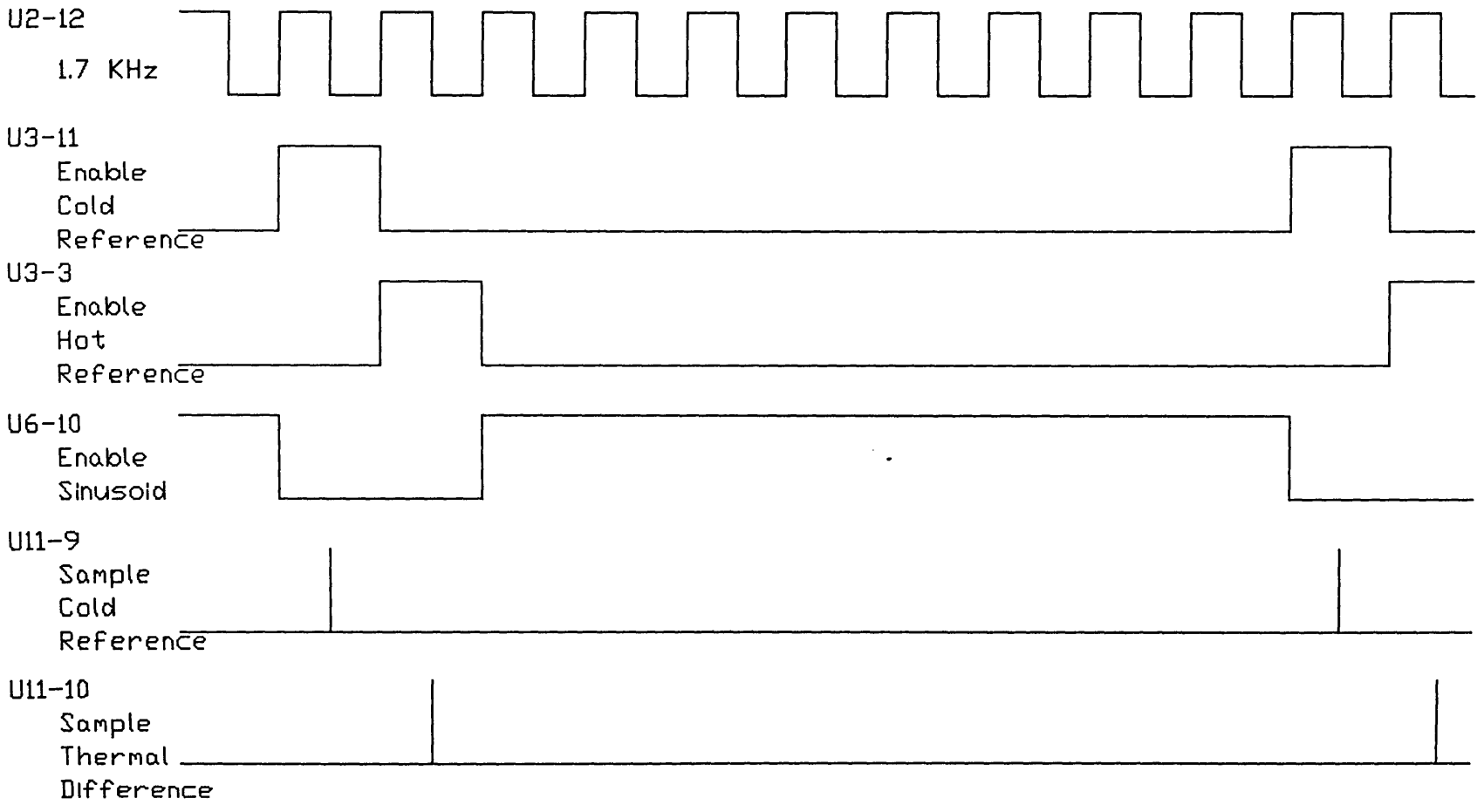

Figure 3.14. Timing Diagram -- Thermal References and Scene.

forward path. The feedback path uses the hot reference sample pulse.

Triple 3-input AND gates, U11 (part number 4073) were necessary for gating of the proper signals. The circuitry is included in Figure 3.12. It is easily seen that the outputs from U3 are necessary because these signals correspond to the scanning of each thermal reference. The output from U4-10 is required to maintain the timing relationship between the high speed sampling and integrator reset as presented in Figure 2.6. Finally, the output from U17-10 ensures that only one pulse is used in obtaining each sample. More importantly, this one pulse occurs very near the center of each reference, only after scanning of several pixels with the same thermal content. This allows sufficient settling time for the sampling capacitors by not subjecting them to abrupt voltage changes. The complete timing diagram is then presented in Figure 3.14.

CHAPTER 4: EVALUATION OF DESIGN EXAMPLE

Chapter 3 detailed the design example and demonstrated background subtraction and generation of a feedback control signal. In this chapter the control signal will be fully implemented, thus closing the feedback loop. The circuit's performance in providing correction for Responsivity and Bias will then be evaluated.

The design example was constructed with a jumper to manually enable and disable the feedback loop as shown in Figure 3.1. By installing this jumper, the BDI integration process will be modulated by the pulse width of the feedback control signal.

First consider the case where the reference voltages are ±1 V. This corresponds to a detector with the minimum Responsivity and the control signal shown in Figure 3.11. Note that BDI integration will be performed for 54 usec of the 59 usec dwell time, or approximately 91%. Figure 4.1 displays the circuit's output for an input sinusoid of 200 Hz. It is seen that background subtraction has been maintained and, upon comparison with Figure 3.7, that the sinusoidal amplitude has not been significantly diminished. Likewise,

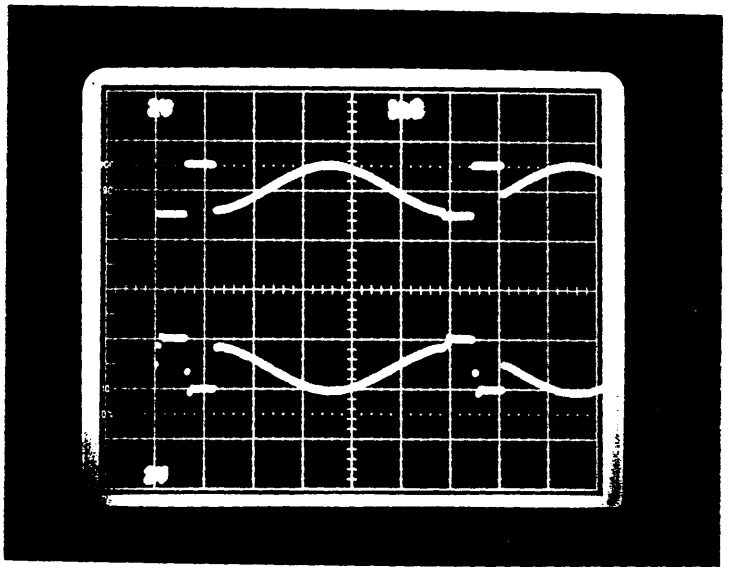

Figure 4.1. Circuit Output for 200 Hz Input and ±1 V Thermal References.

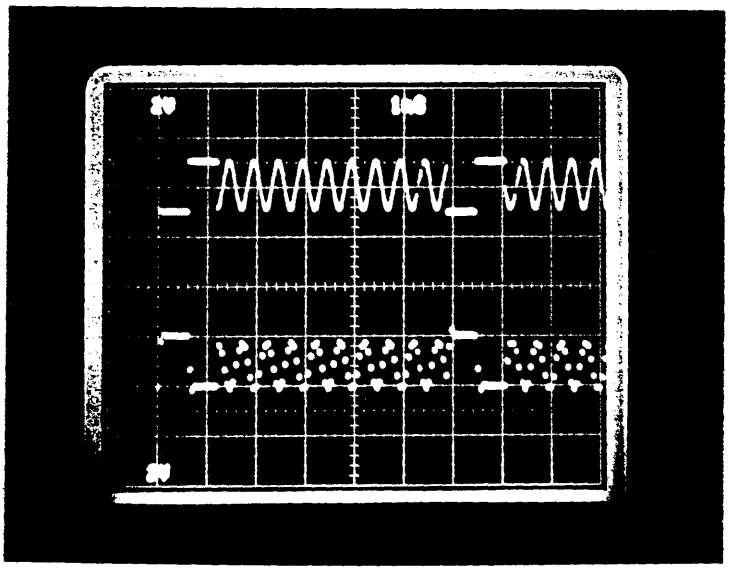

Figure 4.2. Circuit Output for 2 KHz Input and ±1 V Thermal References.

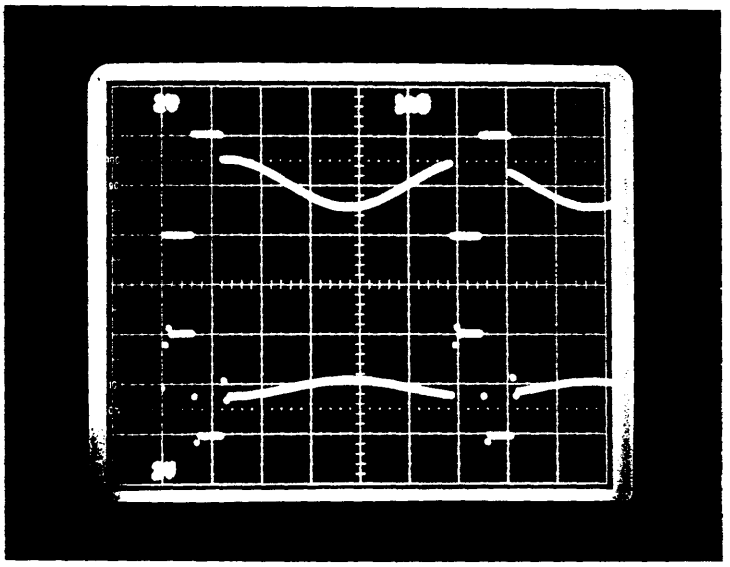

Figure 4.3. Circuit Output for 200 Hz Input and ±2 V Thermal References.

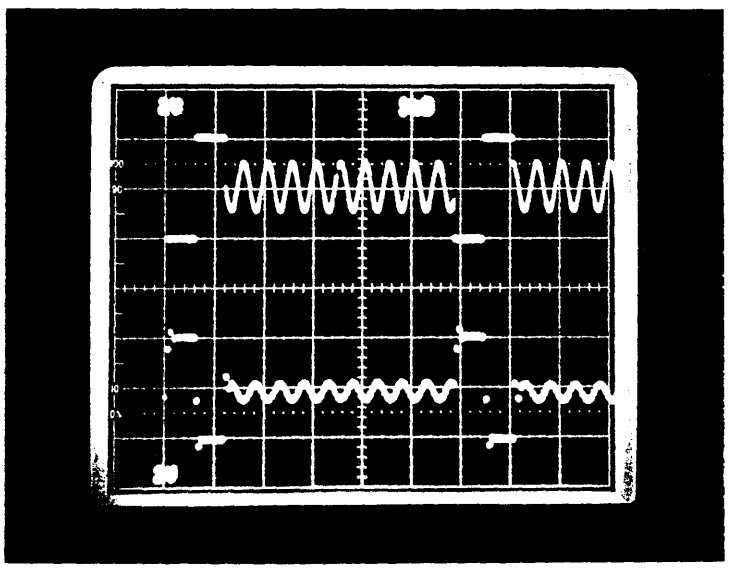

Figure 4.4. Circuit Output for 2 KHz Input and ±2 V Thermal References.

Figure 4.2 presents the circuit output for an input sinusoid of 2 KHz and should be compared to Figure 3.8.

A detector with maximum gain will be simulated by adjusting the reference voltages to yield ±2 V. The feedback signal of Figure 3.10 will then be produced, enabling BDI integration for 18 usec of the 59 usec dwell time or about 30%. With an input sinusoid of 200 Hz, the circuit output is as shown in Figure 4.3. The output amplitude has been decreased from that of Figure 4.1; however, the background subtraction is still produced in the same manner.

Figure 4.4 presents the circuit output for an input sinusoid of 2 KHz and reference voltages of ±2 V. This output is also less than its earlier yield of Figure 4.2. Therefore, the circuit has produced compensation which is dependent on the gain of the detector.

In future implementation, this circuit should provide a means of adjustment (trimpot, select at test resistor, or switched capacitor) in order to change the slope of the reference ramp and thus alter the pulse-width modulation period. This adjustment would be made once only, at time of FPA system integration. Both compensation techniques performed sufficiently to consider their future implementation in scannned LWIR focal plane arrays.

SUMMARY

This paper has presented an alternative approach to providing uniformity correction between detector channels of a LWIR FPA using analog MOSFET circuitry. The compensation for gain and level was achieved in real operating time by employing the detector's response to cold and hot reference pixels. Background subtraction was utilized in order to correct for DC Bias contributions. Responsivity was addressed via pulse-width modulation of the BDI integration process.

A VLSI implementation of this circuit may be produced for cryogenic compatibility with focal plane arrays. This could potentially reduce the size, weight, and packaging constraints of current thermal systems.

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