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Pulse Width Modulated Adaptive Delta Modern Design and Analysis

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PULSE WIDTH MODULATED ADAPTIVE DELTA MODEM DESIGN AND ANALYSIS

BY

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ABSTRACT

A unique design of a voiceband adaptive delta modem will be presented. The modulator utilizes a constant amplitude variable width pulse combined with the principles of delta modulation. This results in a modem that has lower amplitude distortion, requires less transmission channel bandwidth, and is less prone to slope overload than conventional adaptive delta modems. The design also allows the use of a simple single integration demodulator while maintaining fidelity.

The modem design and analysis is presented assuming a transmission channel which is bandwidth limited and amplitude limited.

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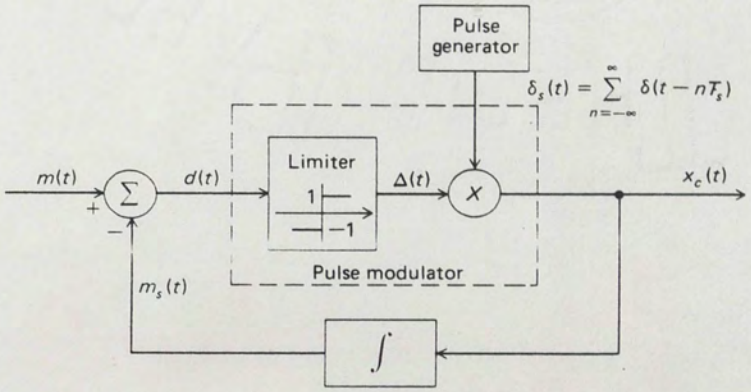
CHAPTER I

INTRODUCTION

Background of Previous Work

Delta modulation was invented in ITT French Laboratories and patented in 1946. Various forms of delta modulation have been in use for several years, primarily due to the simplicity of the circuits required to implement the modulator and demodulator. The output of the delta modulator is a series of narrow positive and negative pulses whose polarity is determined by the difference between two adjacent sample points of the analog input signal. These pulses convey information about the derivative or slope of the input, thus the name delta modulation. The analog signal is recovered by the demodulator by integrating the pulses and low pass filtering. A typical block diagram of a delta modulator along with corresponding waveforms is shown in Figure 1.

Since the modulator output is a stream of narrow pulses, a large transmission channel bandwidth is required to accurately transmit these pulses. Slope overload is another problem inherent to delta modulators. Each pulse results in a constant magnitude change in the demodulator output which should closely match the analog input signal. If the analog input changes rapidly, the demodulator output



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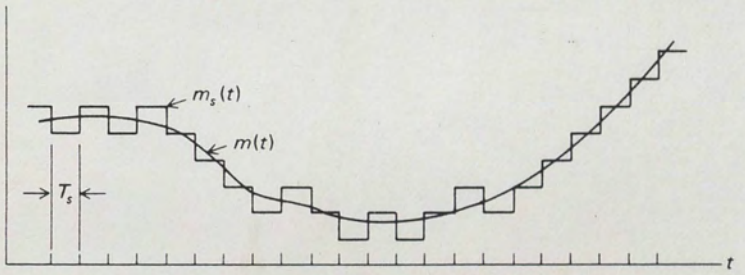

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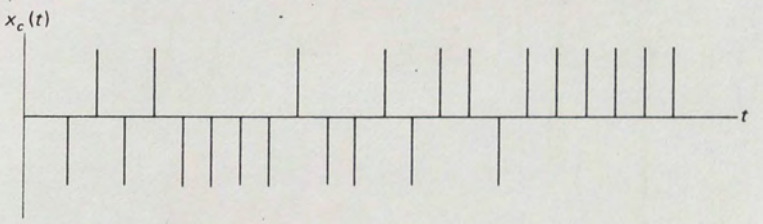


(c)

Figure 1. Delta Modulator. (a) Block Diagram. (b) Analog Input and Integrator Output. (c) Pulse Output. (Ziemer and Tranter 1985).

will ramp at its maximum slope determined by the pulse frequency and weighting in an attempt to mirror the analog input. If the input signal slope is greater than this maximum slope the modem is capable of, significant error and distortion can result. The demodulator output (m'(t)) and analog input (m(t)) are shown in Figure 2 operating under various conditions.

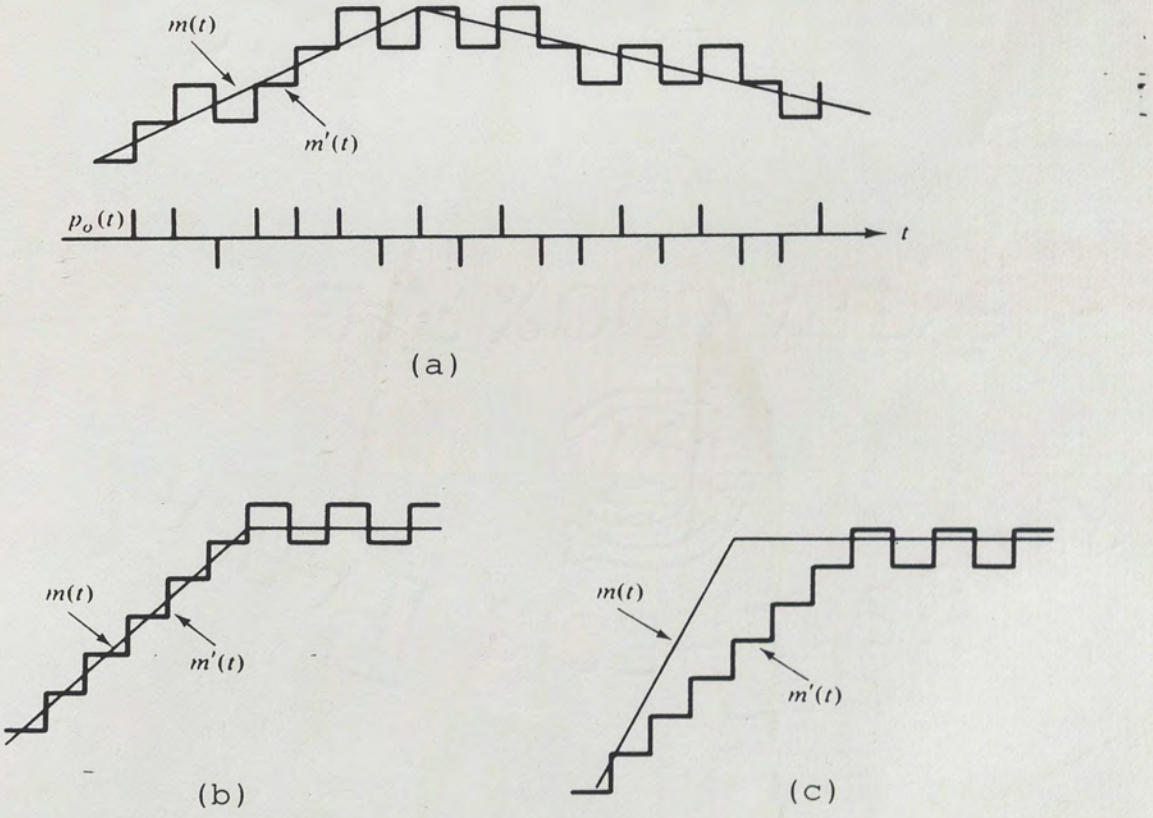


Figure 2. Delta Modulator Waveforms with Analog Input m(t) and Reconstructed Signal m'(t) under conditions of (a) Input Slope Less Than Maximum, (b) Maximum Slope, and (c) Slope Overload. (Roddy and Coolen 1981).

The problem with slope overload can be compensated by adding circuitry which allows the maximum slope of the modem to change or adapt to the changing slope of the input signal. One form of this adaptive delta modulation (ADM) is continuously variable slope delta modulation (CVSD). This is illustrated in Figure 3 with a typical demodulator output waveform.

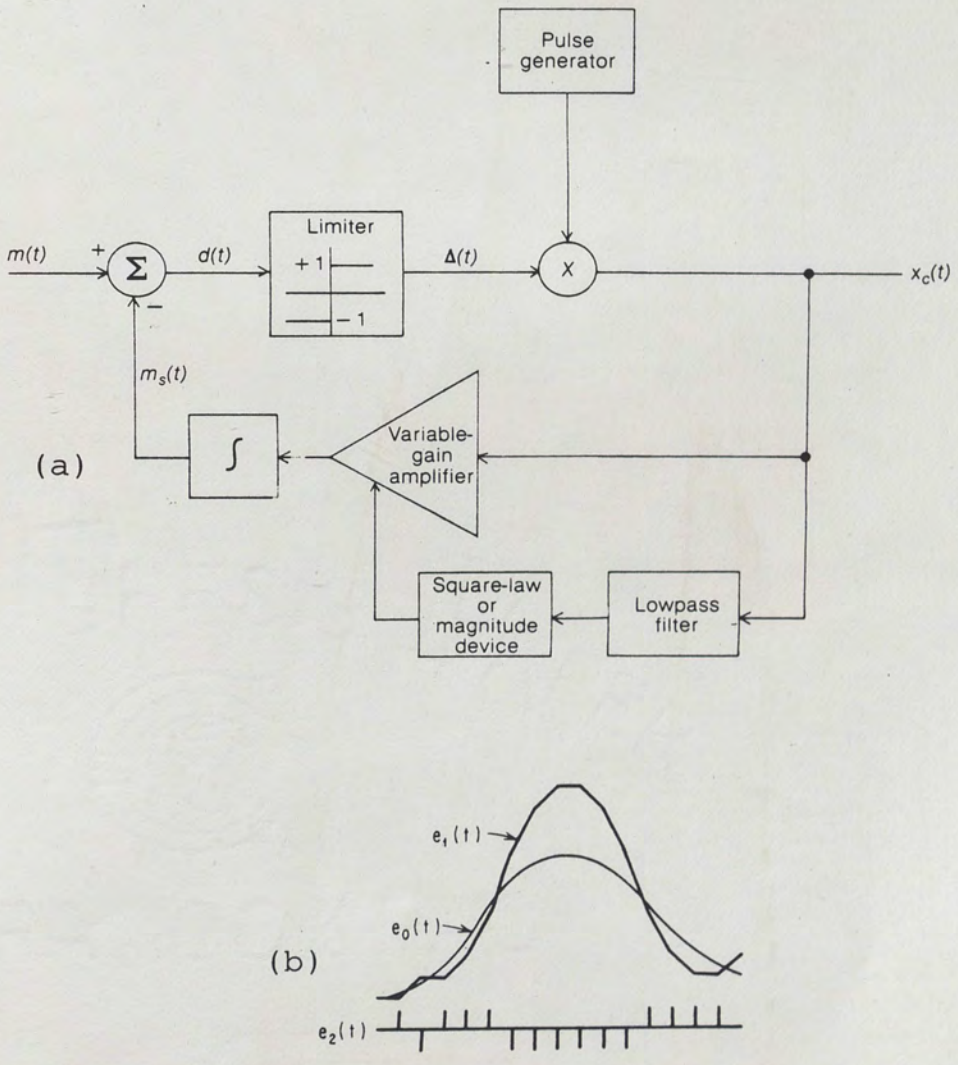


Figure 3. (a) CVSD Modulator (Ziemer and Tranter 1985). (b) Analog Input and Demodulator Output, $e_0(t)$ and $e_1(t)$ (Panter 1965).

Operation of the CVSD modulator is similar to conventional delta modulators with the exception of the feedback circuit. If several pulses of the same polarity are generated by the modulator, this indicates an attempt to track with the input by ramping in one direction. This series of pulses, applied to a low pass filter, causes an increase in filter output which increases the gain of a variable gain amplifier in the feedback network. Therefore, each pulse is given a greater weighting causing the integrator slope to increase to match the demand of the input. The result is less error as compared to non-adaptive delta modulation. The demodulator for this circuit is identical to the feedback network of the modulator (in dotted lines) coupled with a low pass filter.

One problem with this system can be seen from Figure 3 where $e_0(t)$ is the analog input and $e_1(t)$ is the demodulator output, ignoring channel conditions. When the input signal changes rapidly, the modulator responds with several pulses before the error is corrected, and then may overshoot the analog input. Significant distortion can result since this adaptive process is relatively slow due to the time delays inherent to this design. Other variations of adaptive delta modulation such as High Information Delta Modulation (Panter, 1965) and variable clock frequency delta modulation (Prezas, 1979) also require several clock cycles to recover from a slope overload condition.

Problem Statement

A modem will be designed based on the principles of delta modulation which will allow better tracking of the input signal than that displayed by typical adaptive delta modems, such as the CVSD. Any generated error will be corrected within one pulse. This will lower distortion and allow a lower sampling frequency.

The input will be a variable frequency and amplitude voiceband analog signal and the modulator output will be matched to the available transmission channel. This channel is bandwidth limited to a frequency range of 100 to 3000 hertz, and amplitude limited to a maximum of one volt, above which amplitude distortion becomes significant.

The design will be implemented with operational amplifiers and digital logic.

CHAPTER II

DESIGN APPROACH

For error correction with a single pulse, additional information must be modulated onto the pulse such that not only the polarity of error is transmitted, but also its magnitude. This can be conveyed with the pulse amplitude or the pulse duration.

If amplitude modulation of the delta pulse were employed, the amplitude would correspond to the amount of error that is to be corrected such that the corrected demodulator output would equal the sampled input. The pulse amplitude must be constrained below a maximum value to prevent distortion by the transmission channel. For a given pulse width, the transmission bandwidth required to accurately transmit the pulse is relatively independent of pulse amplitude.

In pulse width modulation of the delta pulse, the width or duration of the pulse is made proportional to the error between the sampled analog input and the integrator output (which corresponds to the unfiltered demodulator output). One advantage over amplitude modulation is a reduction in required bandwidth when correcting a greater error. A large error results in a wide delta pulse which

requires a lower transmission channel bandwidth for a given pulse distortion. A wider pulse has a higher power spectral density at lower frequencies which are passed by the channel. Thus, error correction is performed best when it is most needed: when the error is large. For this reason, pulse width modulation was chosen as the adaptive medium for the delta modulator. The functional block diagram for the modulator is shown in Figure 4.

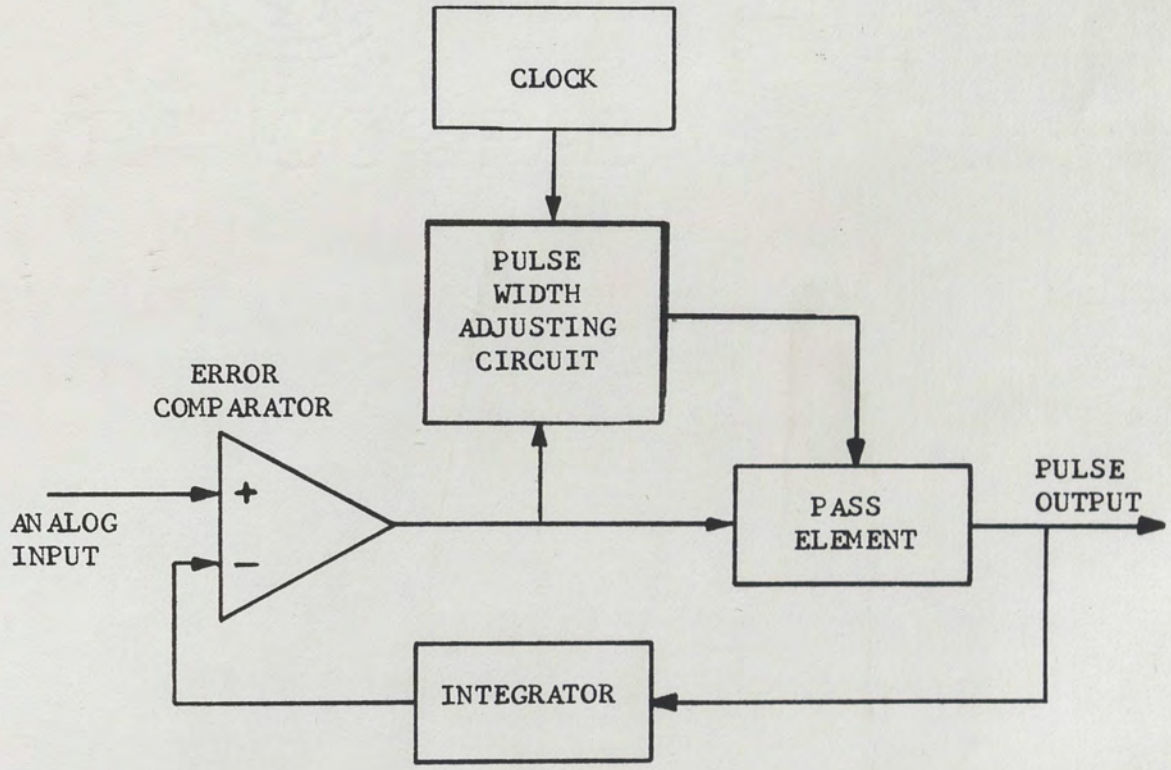


Figure 4. Functional Block Diagram of Pulse Width Modulated Delta Modulator.

Pulses will be transmitted at a constant frequency determined by the clock. Between pulses the integrator output will be constant and a change in input will generate an error which will cause the error comparator to switch to the correct polarity to allow error correction. At the clocks leading edge, the pulse width adjusting circuit will enable the pass element forcing the output to equal the error comparator voltage. The integrator output then ramps at a predetermined slope until the integrator output equals the input signal. At this time the error comparator switches to its opposite state which is sensed by the pulse width adjusting circuit which terminates the pulse. Thus, a single pulse will zero the integrator error with the pulse width being a measure of the initial error.

The integrator gain can be calculated based on the maximum possible error and the maximum allowable pulse width. With the error corrected to zero with each pulse, the clock frequency may be set to the Nyquist rate. The maximum clock frequency is limited by the constraints of the assumed transmission channel.

Several potential problems exist for this design. Since the pulse is terminated at the point when the error is corrected to zero, the time of zero error occurs at different points in the clock cycle due to the variance in pulse widths. This leads to a phase lag with higher

frequency signals and some phase distortion. These effects should be insignificant for voice transmissions.

The transmission channel will distort and spread out the pulse due to its limited bandwidth and variance of phase velocities of the pulses frequency components. This requires that the pulse frequency be low enough to prevent interference or overlapping between two adjacent pulses, termed intersymbol interference. The spreading due to the difference in phase velocities should be negligible at the frequencies to be transmitted.

The maximum clock frequency determines the maximum analog input frequency which may be reconstructed at the demodulator output, based on the Nyquist criterion. An input above this frequency may result in distortion at the output of the demodulator reconstruction filter. This problem, called aliasing, will be precluded by band limiting the input signal.

CHAPTER III

CIRCUIT DESCRIPTION AND OPERATION

The pulses generated by the modulator will be of the correct polarity to correct any accumulated error and the pulse duration will be mathematically proportional to the error. Once the error is zeroed, the pulse is terminated and no further pulses should be generated until the clock enters its active cycle. The mathematical model of the pulse width adjusting circuit will be implemented using digital logic while the error comparison and pulse integration will be performed by operational amplifiers. High speed components will be chosen to minimize error caused by loop time delays. The schematic diagram of the modulator is shown in Figure 5.

Circuit Operation

The analog input signal is bandwidth limited by an anti-aliasing filter composed of a unity gain fourth order Butterworth low pass filter with a -3 dB cutoff frequency of 1600 HZ. The filtered input is fed to the error comparator which monitors the integrator output and the input signal. The error comparator output is applied to an exclusive or gate, which controls the pulse termination, and also through a CMOS switch to a sample and hold comparator circuit. The

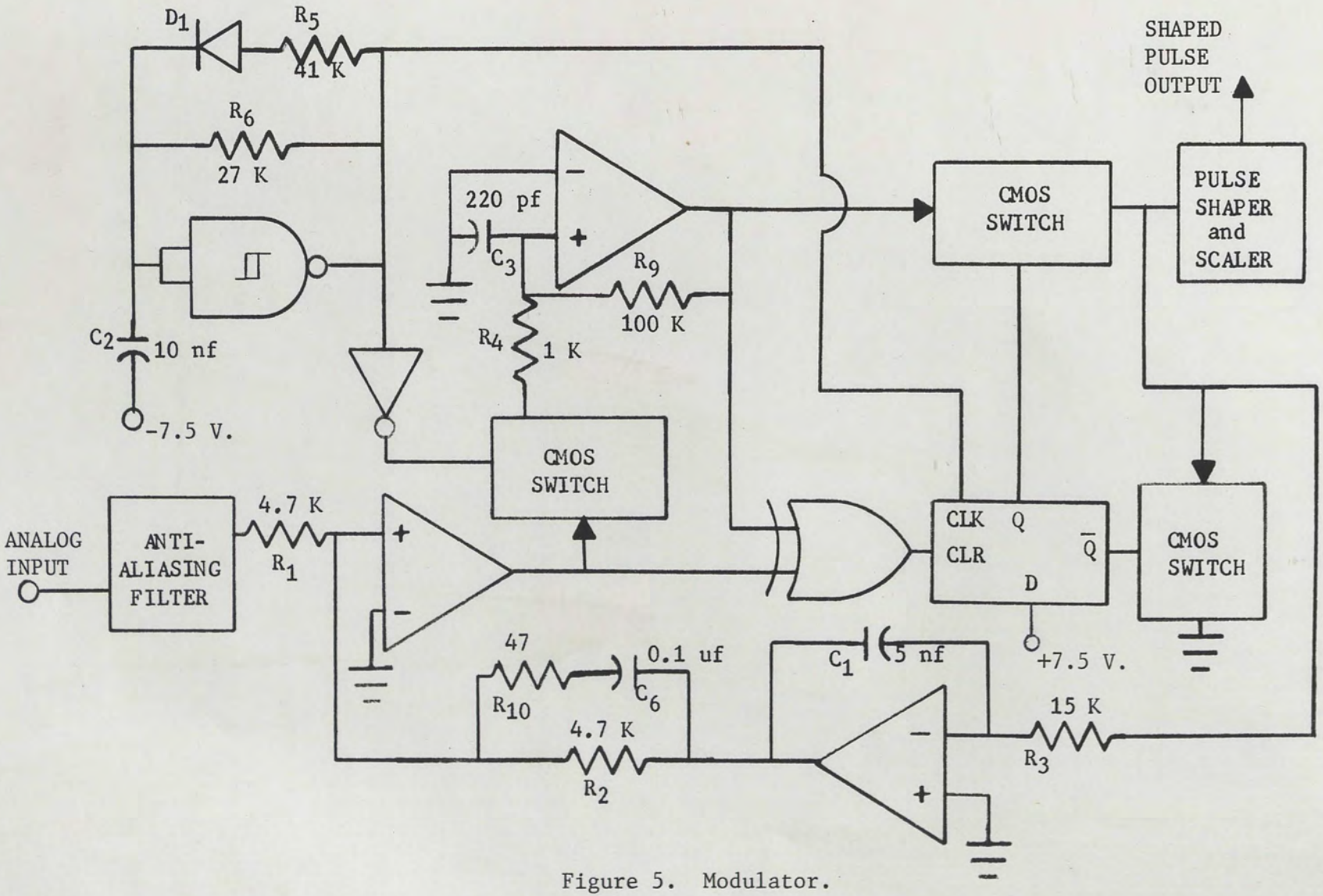


Figure 5. Modulator.

output of the sample and hold circuit is applied to another CMOS switch which serves as the pass element and controls the pulse width. The pulse output is sent to an inverting op amp integrator in the feed back circuit whose output will be compared to the input signal. The clock for the modulator is made from a Schmitt nand gate configured as an inverter with a feed back network designed for a 33 percent duty cycle. The edge triggered D flip flop is configured to set on the clocks leading edge and clear when the exclusive or output goes high.

On the leading edge of the clock, the D flip flop sets, enabling the CMOS switch to pass the sample and hold comparator output. This output is fed to the inverting integrator which ramps in a direction opposite to the pulse polarity. When the integrator output equals the input signal, the error comparator switches to its opposite state. Since the CMOS switch to the sample and hold comparator is disabled when the clock is high, the sample and hold comparator maintains its previous output. Now the exclusive or gate has one input high and one input low forcing the output high. This clears the D flip flop disabling the CMOS switch and terminating the pulse. Since the D flip flop is leading edge triggered, another pulse will not be generated until the clock again makes its transition from low to high. A CMOS switch connecting the pulse output to ground is enabled by the D flip flop inverted output to more quickly terminate the pulse.

The pulse output is passed through a scaler and conditioner before it is applied to the channel. This reduces the maximum pulse amplitude to one volt to conform to the channel constraints and removes high frequency components of the pulse which may be capacitively coupled to adjacent lines of the transmission channel causing crosstalk and interference.

The demodulator is shown in Figure 6. The integrator is similar to to that in the modulator with the exception of a soft limiter in the feedback circuit to keep the integrator output from saturating at the supply rails. Also, the integrator gain is increased to account for the pulse scaling at the modulator output. The low pass reconstruction filter used is an eighth order Butterworth with a -3 dB cutoff frequency of 1600 HZ.

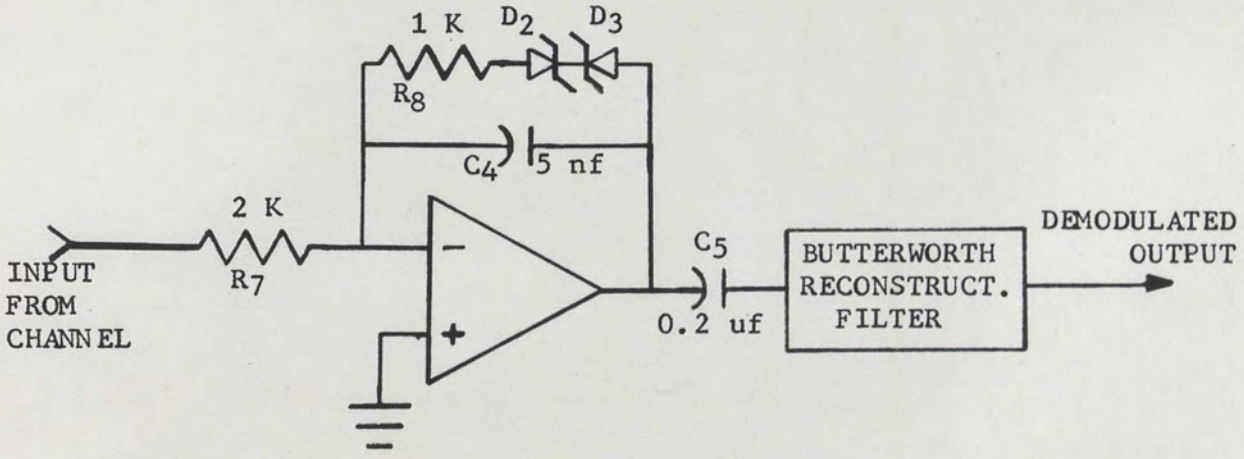


Figure 6. Pulse Width Modulated Delta Demodulator.

Design Equations

A split 7.5 volt power supply will be used for all active components of the modulator and demodulator.

Clock Frequency and Maximum Pulse Width

A 3 KHZ band limited channel exhibits a time constant of approximately 53 microseconds (1/2*PI*freq). A voltage step applied to this channel will exponentially build to a steady state value in approximately 250 microseconds (ignoring the 100 HZ lower band pass cutoff frequency). Two time constants or 106 microseconds will allow the voltage to build to 86 percent of its final value (1-EXP[-2]). This time will be chosen as the maximum pulse width, i.e., the pulse width required to correct the maximum possible error.

Upon termination of the pulse, the voltage transmitted should decay to near zero to prevent intersymbol interference with the next transmitted pulse. If four time constants (212 microseconds) are allowed for decay, the channel voltage will drop to less than 2 percent of its peak value. The chosen clock waveform is illustrated in Figure 7.

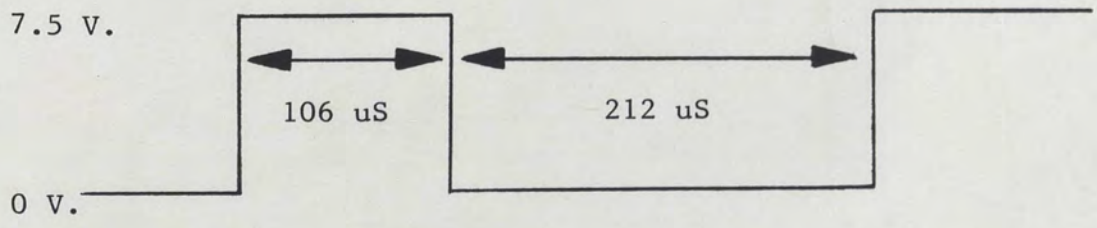


Figure 7. Modulator Clock Waveform.

This results in a clock frequency of 3.14 KHZ. Based on the Nyquist theorem (and ignoring the 100 HZ lower channel cutoff frequency), the maximum analog signal frequency that may be reconstructed is 1.57 KHZ.

With the nand Schmitt trigger configured as an inverter, the upper and lower trigger voltages were measured to be the following:

V_{utl}= 1.9 V. V_{ltl}= -3.2 V.

The clock timing capacitor was chosen to be 10 nf. Capacitor discharge time from V_{utl} to V_{ltl} is determined by C_2 and R_6. This determines the time period the clock is low in each cycle (212 microseconds):

$$-7.5 + (V_{utl} + 7.5)EXP(-212E-6/R_6C_2) = V_{ltl}$$

Substituting and solving yields R_6 = 27.1 Kohms.

Charging time from V_{ltl} to V_{utl} is determined by R_6 in parallel with R_5 (R_{eq}). Ignoring the diode forward voltage drop:

$$7.5 + (V_{ltl} - 7.5)EXP(-106E-6/R_{eq}C_2) = V_{utl}$$

Substituting and solving yields R_{eq} = 16.4 Kohms and R_5 = 41.4 Kohms. Diode D_1 is a low current switching diode.

Integrator

The integrator must ramp fast enough to correct the maximum expected error with the maximum pulse width, 106 microseconds. The input signal is constrained within +5 to

-5 volts, resulting in a maximum possible error of 10 volts between input samples. A 7.5 volt pulse 106 microseconds in duration must correct this error. The integrator gain is equal to $1/R_3C_1$. C_1 should be large enough to minimize voltage drift while the integrator is in the hold state. If the minimum discharge resistance is 5 megohms (primarily the op amp input impedance) and the maximum allowed drift voltage is 0.1 volts at maximum voltage (5 volts):

$$5EXP(-t/RC_1)=4.9$$

$t=1/f_{clock}$ = 318E-6 sec; R = 5 megohms

C_1 should be greater than 3.15 nf. 5 nf will be used.

$(1/R_3C_1)(7.5\ V.)(106E\text{-}6\ sec)$ = 10 volts

R_3 = 15.9 Kohms; 15 Kohms will be used.

Sample and Hold Comparator

Capacitor C_3 is chosen to be large enough to prevent significant discharge during hold operations but small enough to charge rapidly through R_4 during sampling. Assuming a maximum discharge resistance of 5 megohms, a discharge time of 318 microseconds, and a maximum drift voltage of 2 volts:

$$7.5EXP(-318E\text{-}6/RC_3) = 5.5 \text{ volts}$$

C_3 = 205 pf; 220 pf will be used.

R_4 is chosen to allow rapid charging of C_3 while limiting the maximum current drawn from the error comparator and the CMOS switch. Assuming an error comparator slew rate of 50

volts/microsecond, the comparator will slew 7.5 volts in approximately 0.2 microseconds. Charging time of C_3 should be roughly comparable to this:

R_4C_3 = 0.2E-6; R_4 = 909 ohms; R_4 = 1 Kohm will be used This will limit the peak chargingcurrent to:

(15 V/1000 ohms) = 15 mA.

Output Pulse Shaper and Scaler

The op amp pulse shaper is a second order low pass filter with a low frequency gain of 0.133 (1/7.5). The filter is designed with a damping factor of 0.5 (Q of 1.0) and a cutoff frequency of 3000 HZ. A second order filter was chosen to give a parabolic output in response to a square wave input which is more complementary to the transmission channel.

Active Components

The integrators, sample and hold comparator, and filters are constructed from LF 351 op amps which have extremely high input impedance (10E+12 ohms) and high slew rate (13 V/microsecond). The error comparator is a LM 311 high speed voltage comparator. A relatively low resistance of 4.7 Kohms was chosen to couple the input signal and integrator output to the error comparator through R_1 and R_2 to enhance speed. Digital logic used is high speed CMOS.

Demodulator

The demodulator integrator has a gain 7.5 times greater than the modulator integrator to account for the pulse scaling at the modulator output. This is accomplished by making $R_7 = R_3/7.5 = 2$ Kohms. A soft limiter is also used to keep the integrator output from saturating at the +7.5 or -7.5 volt supply rails. The limiter consists of back to back 6.1 volt zener diodes D_2 and D_3 in series with resistor R_8. Limiting begins at an integrator output of about 6.6 volts (6.1 volts plus 0.5 volt forward diode voltage). To limit the maximum integrator output voltage to a magnitude of 7 volts, R_8 must be chosen to shunt all pulse input current when the integrator is at the limits of +7 or -7 volts. Maximum pulse current to the integrator =

$1\ V/R_7 = 0.5$ mA. $\quad R_8 = (7-6.6)/0.5$ mA $= 800$ ohms

$R_8 = 1000$ ohms will be used.

The demodulator integrator is AC coupled to the reconstruction filter by capacitor C_5 to remove any DC bias present at the integrator output.

CHAPTER IV

MODEM CONSTRUCTION

Bread-board construction was chosen for this low frequency design prototype for simplicity. A photograph of the modulator, demodulator, and power supply is shown in Figure 8. All resistors used are 1/4 watt 5 percent tolerance except where noted.

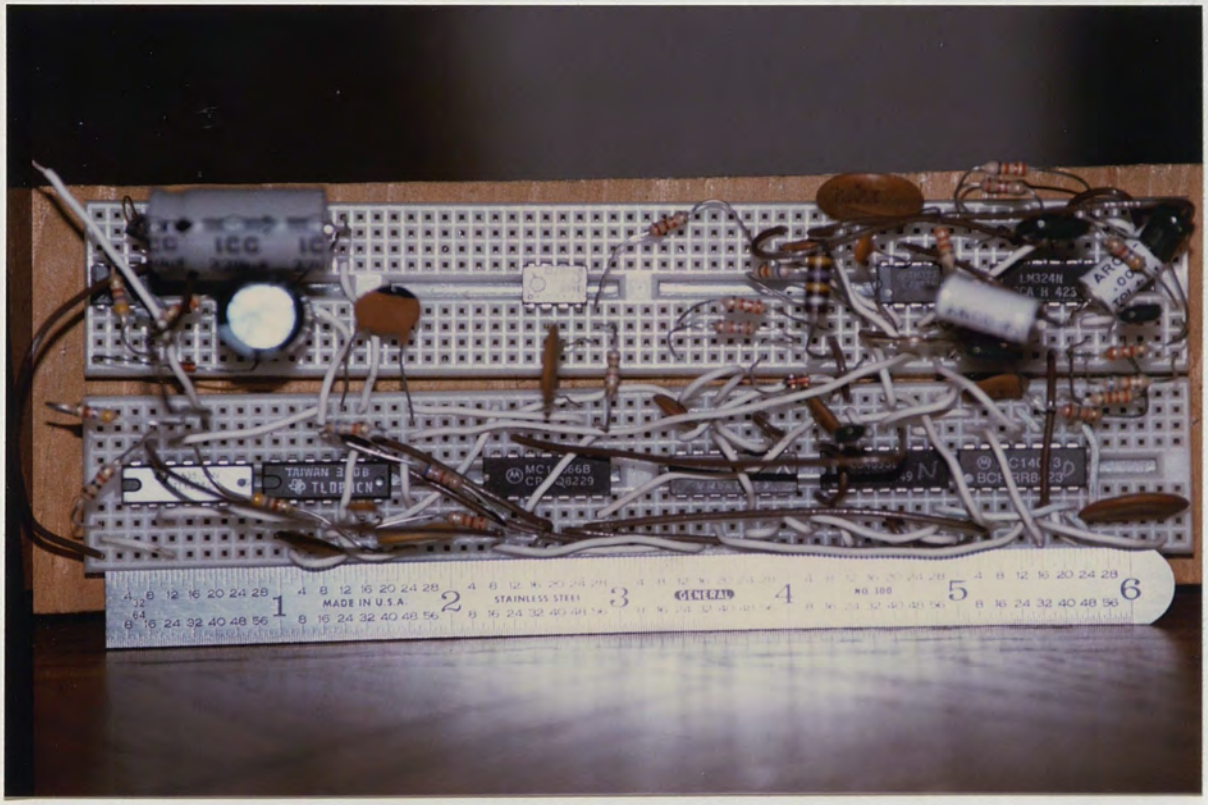


Figure 8. Photograph of Completed Modem.

The power supply includes a split 7.5 volt tracking regulator with high output current op amps to supply the 25 milliamps required by the modulator, and is shown in Figure 9. The regulator is powered by a split 12 volt unregulated supply. Decoupling capacitors of 0.1 microfarads are used at the power supply connections at the IC chips.

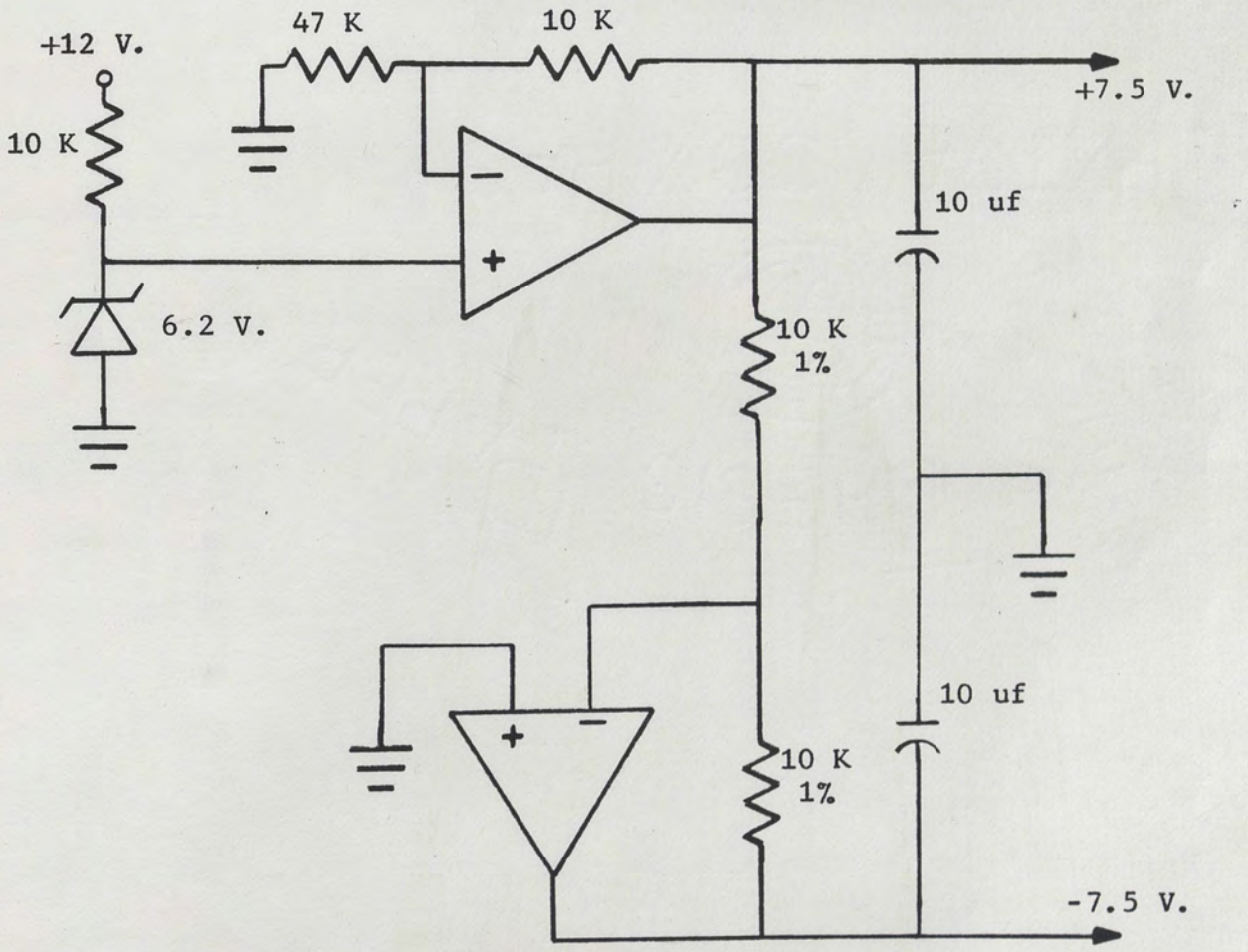


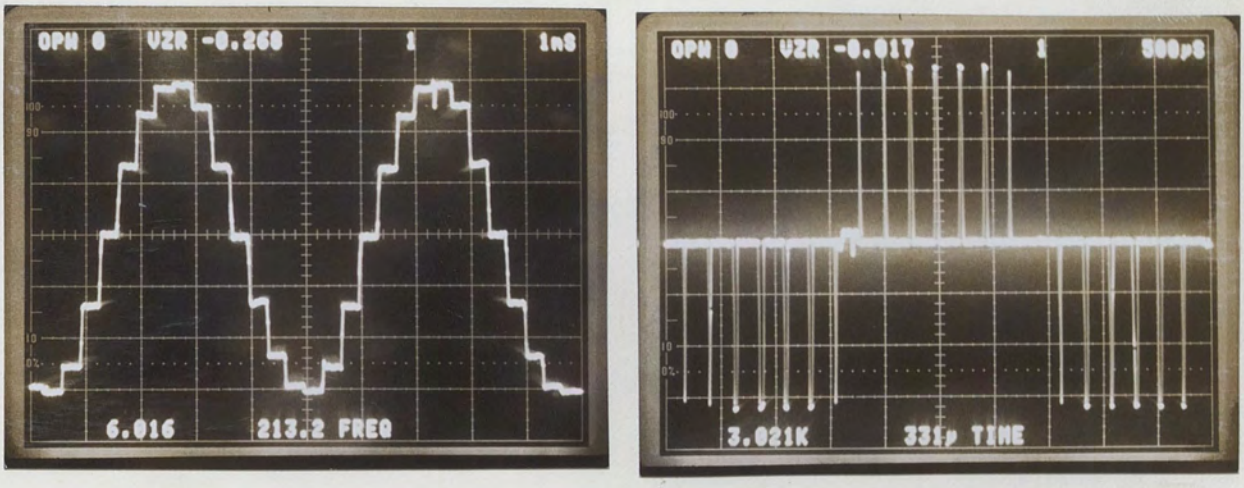
Figure 9. Schematic Diagram of Tracking Regulator.

CHAPTER V

RESULTS AND PERFORMANCE

Initial operation of the modulator resulted in oscillation of the sample and hold comparator at the clock frequency. Since the inputs to the sample and hold comparator are very close to the power supply voltages, there was not enough difference in voltage between the input voltage and power supply voltage to maintain correct operation of the LF 351 op amps internal current sources. Therefore the op amp performance deviated significantly from the ideal characteristics resulting in undesired switching. This problem was cured by adding positive feedback to the sample and hold comparator with resistor R_9. This results in approximately 150 millivolts of hysteresis which will not hamper the comparator performance since its input is always near the power supply rails.

The clock frequency and duty cycle were fine tuned by adjusting R_5 and R_6. The resulting operation showed good fidelity between the analog input and integrator output. The modulator integrator output and unshaped pulse output are shown in Figure 10 for two different sinusoidal inputs of approximately 3.1 volts peak at 215 hertz. The modulators immunity to slope overload is illustrated by



(a) (b)

Figure 10. Modulator Waveforms for Sinusoidal Input. (a) Integrator Output. (b) Unshaped Pulse Output.

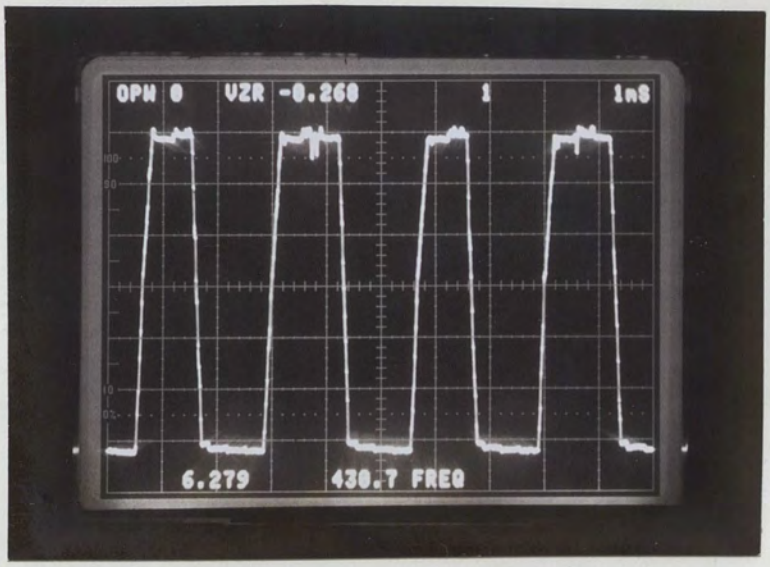


Figure 11. Modulator Integrator Output In Response to a Square Wave Input.

Figure 11 where the input is a square wave of 3.3 volts peak at 431 HZ. Here the integrator closely tracks with the analog input with maximum error corrected by one pulse. A photograph of error versus time is shown in Figure 12 for a 3.1 volt peak 170 HZ sinusoidal input. This is the waveform appearing at the input to the error comparator and illustrates how error is accumulated during periods of no pulse output then zeroed by each pulse.

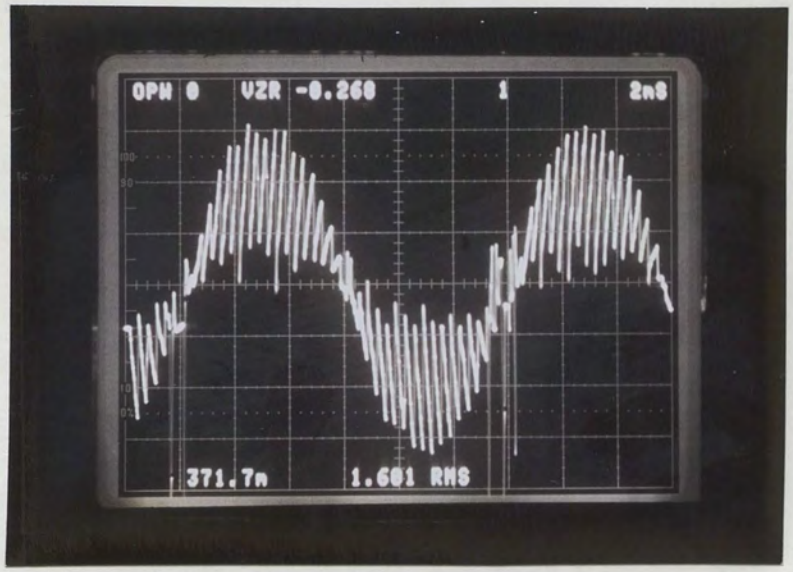


Figure 12. Modulator Integrator versus Input Error.

With zero input, the modulator integrator was observed to "hunt" or oscillate about zero volts. The non-zero output is due to the integrator overshooting the output corresponding to zero error. This is due to time delays in the system which prevent the pulse from being terminated exactly at the point of zero error. The majority of this error was traced to the error comparator circuit. Due to significant propagation delays, the error comparator output was not immediately switching when the input crossed the switching threshold of zero volts (corresponding to zero error). This time delay was reduced by using a very high slew rate LF 357 op amp, which also has a lower propagation delay, and then finally installing an LM 311 high speed voltage comparator. Speed was further enhanced by placing a lead network consisting of R_{10} and C_6 in parallel with resistor R_2 at the integrator output. This allows a change in integrator output to have a larger effect on the error comparator, indicated by a substantial decrease in response time. This is most noticeable with small or zero input signals. This change substantially reduced hunting error.

The effect of the transmission channel can be determined by observing the demodulator integrator output and comparing it to that of the modulator. Figure 13 shows the demodulator integrator output in response to a 3.5 volt peak 218 HZ sinusoidal input. The channel is simulated by a 3 KHZ first order low pass filter AC coupled to the

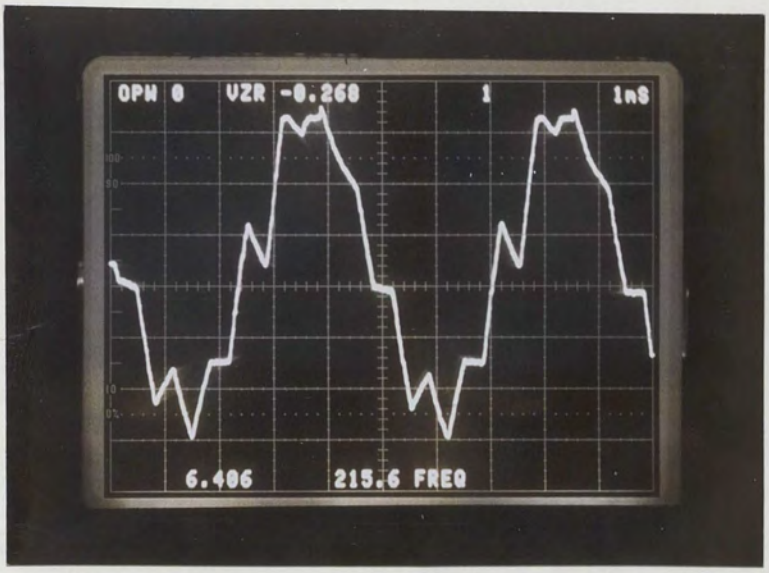


Figure 13. Demodulator Integrator Output Showing Channel Distortion.

demodulator with a lower cutoff frequency of 100 HZ. The waveform shows decay due to the band limited channel, but still maintains good correlation with the analog input after filtering. A DC bias of about 2.5 volts was noted at the integrator output but the soft limiter is shown to be keeping the integrator out of saturation. The output of the reconstruction filter shows a low distortion reproduction of the original analog input.

At analog input frequencies near the maximum determined by the Nyquist theorem, the demodulator output

was a low distortion sinusoid but showed signs of insufficient input sampling. Figure 14 shows the output envelope where too low a sampling frequency is evident. The input signal is 3.5 volts peak at 1.4 KHZ. This "breathing" effect was negligible at input frequencies below 1 KHZ.

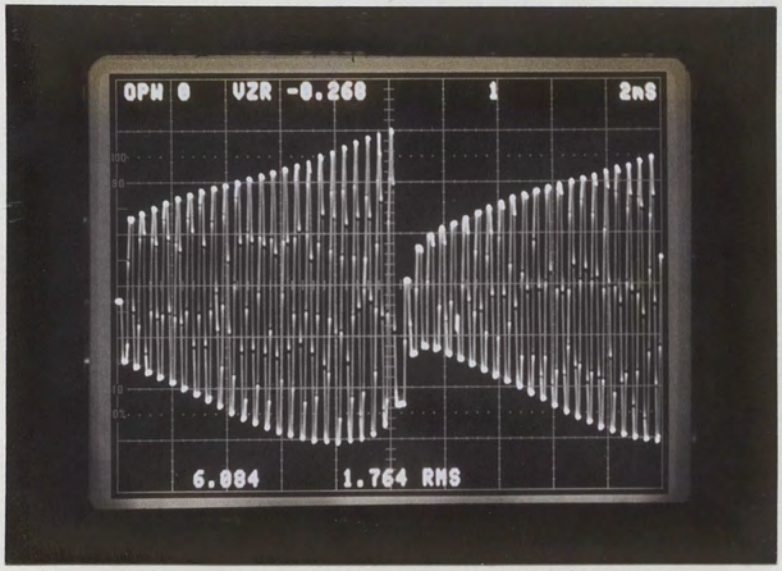


Figure 14. Modulator Integrator Output "Breathing" Due to Insufficient Sampling.

A small sinusoidal output at one-half the clock frequency was noted at the demodulator output when the signal input is zero. This is due to hunting of the modulator. Since the integrator output of the modulator makes a transition at the leading edge of each clock cycle, a small amplitude square wave is generated with a frequency of one-half the clock frequency. The demodulator reconstruction filter has a cutoff frequency close to one-half the clock frequency based on the Nyquist sampling criterion. This allows the fundamental frequency component of the square wave to leak to the demodulator output. This component can be removed by reducing the cutoff frequency of the reconstruction filter or minimized by reducing the hunting error, thereby reducing the amplitude of this square wave.

CHAPTER VI

CONCLUSION

Modem Performance

The method used in determining a maximum clock frequency based on the channel constraints is shown to be a valid approach. Although the input sampling rate can theoretically be set to the Nyquist rate, there are advantages to sampling at a higher rate. The effect of "breathing" at the demodulator output, in response to inputs near the maximum frequency as determined by the Nyquist criterion, can be reduced or eliminated by more frequent sampling. Since the maximum clock frequency is fixed (due to the channel), this reduces the maximum input frequency which may be recovered. If the demodulator output reconstruction filter cutoff frequency is lowered to correspond to this maximum input frequency, then the hunting seen during conditions of zero input will be eliminated by the filter.

This form of adaptive delta modulation using pulse width modulation results in more rapid error correction while requiring less bandwidth than typical adaptive delta modems. This is especially important when dealing with restrictive transmission channels. In general, pulse

modulation of any form is not the best choice for transmission on a low bandwidth channel due to the resulting pulse distortion and attenuation. In the present case, the full capabilities of the modulator design were only partially utilized due to channel limitations. If the channel is ignored, the modulator's response is limited by the time delays and slew rates of its components. With high speed voltage comparators and digital logic, the total delay is on the order of one microsecond. This allows the maximum clock frequency and sampling rate to be increased to a few hundred kilohertz. It was experimentally shown that the pulse width delta modulator will perform satisfactorily at a clock rate of 100 kilohertz when the integrator gain is appropriately adjusted. At frequencies above this, hunting error became significant due to system time delays and high integrator gain.

Comparison of Delta Modulation to Pulse Code Modulation

Shanmugam (1979) shows that for a fixed bandwidth transmission channel, the signal to noise ratio (SNR) of standard delta modulation is inferior to pulse code modulation (PCM), due primarily to a larger quantization noise. However, when an adaptive technique such as CVSD is employed, it was found that there is little difference in performance between CVSD and PCM, and for most analog signal applications CVSD and PCM require approximately the same transmission channel bandwidth.

Panter (1965) shows that for an analog signal which is to be represented by samples that can have one of more than ten discrete values, delta modulation is approximately equal to pulse code modulation in terms of channel capacity. Channel capacity is a measure of the rate of information transmission for a given pulse or bit rate. Panter also shows that for more than ten discrete signal sample levels, delta modulation requires about 60 percent less signal power than pulse code modulation. This is an important consideration for low power applications.

Berger (1979) states that for the same information transmission rate, delta modulation is always better than standard pulse code modulation, yet most of the United States and NATO investments are in pulse code modulation equipment, which makes the transition to a delta modulation system difficult.

Another major advantage of delta modulation over PCM is the simplicity of circuitry required to implement a delta modulator and demodulator. This is illustrated by the presence of single chip delta modems (Nishitani et al. 1982), making use of the uncomplicated circuitry and low parts count. The pulse width modulated delta modem uses a demodulator consisting of an integrator and filter. This is simpler than most adaptive modems and similar to that used by standard delta demodulators.

It should be emphasized that the preceding comparisons have been made based on standard delta modulation or typical adaptive modulation, such as CVSD. When the pulse width modulated delta modem is compared to these delta modems, advantages are realized in bandwidth, channel capacity, and simplicity. This results in a modulation scheme which compares very favorably to pulse code modulation or any other form of delta modulation.

Applications

Delta modulation has been used primarily for voice modulation and transmission and some video applications (Barba, 1983). The high efficiency (channel capacity) and low signal power of adaptive delta modems make them desirable in satellite telecommunications and related uses. The space shuttle currently uses a form of adaptive delta modulation for encoding and transmitting voice transmissions (Schilling 1978) since it can operate at a relatively low sampling frequency and can tolerate a high bit error rate.

As pointed out earlier, pulse modulation is practical only if the transmission channel bandwidth is not seriously limited. In the case of a three kilohertz band limited channel, the maximum reconstructed analog frequency was approximately 1.6 kilohertz or about one half the channel bandwidth. Extending the results of this design to a general case, the required channel bandwidth is

approximately twice the maximum analog frequency when using this form of delta modulation. In a practical case, the clock rate should be above the Nyquist rate, reducing the maximum analog frequency.

Specific uses of the pulse width modulated adaptive delta modem can be extrapolated from the current uses of delta modulation, pulse code modulation, and other forms of adaptive delta modulation. The superiority of this adaptive form has been shown in terms of bandwidth and efficiency and makes it an attractive alternative to other forms of pulse modulation.

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