1985

# Analysis and Modification of an Electro-Oculometer

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# ANALYSIS AND MODIFICATION OF AN ELECTRO-OCULOMETER

BY

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B.S.E., University of Central Florida, 1982

THESIS

Submitted in partial fulfillment of the requirements
for the degree of Master of Science in Engineering
in the Graduate Studies Program of the College of Engineering
University of Central Florida
Orlando, Florida

Spring Term
1985

ABSTRACT

This paper describes an electro-oculometer and analyzes the electronic circuits required to process the signal. This electro-oculometer is a passive, two-channel device which detects the eye orientation using commercially available electrodes attached near the eyes. The electro-oculometer is composed of a special amplifier followed by a parabolic filter. The amplifier has high common mode rejection ratio, low drift, and low input bias current. Both DC and AC analyses of the electro-oculometer have been performed. The common mode rejection ratio (CMRR) of the input stage of the device is computed both at low and high frequencies. The experimental data were then compared with theoretical results.

A parabolic low pass filter was designed and implemented as part of the electro-oculometer. A parabolic filter was chosen because it gives a minimum overshoot step response. The input stage (preamplifier) of the electro-oculometer is modified so as to prevent a latch up problem. This latch up is a saturated state of the system. When the output of the system reaches saturation, the system cannot reset itself. The new configuration of the preamplifier does not require any extra active elements.

ACKNOWLEDGEMENTS

I would like to gratefully acknowledge the generous support and invaluable advice of the advisor of this thesis, Dr. Robert J. Martin. Thanks is given to my thesis committee members, Dr. Michael G. Harris and Dr. Robert L. Walker, for the time they spent evaluating this paper. Last, but no means least, I am greatly indebted to my parents, Mr. A.K. Azad and Mrs. Olimon Nessa, and my brother, Dr. Kabir Ahmed, for their encouragement and financial support in pursuing my education in the past several years.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF FIGURES (Continued)

# INTRODUCTION

The purpose of this paper is to present an electro-oculometer and a detailed analysis of its electronic circuit. The electro-oculometer is composed of three functional sections. The first section is a differential preamplifier that amplifies eye position voltages while attenuating common mode voltages. The second section is a trim amplifier which adjusts the offset voltages inherent in the preamplifier. This stage also contains the first pole of the low pass parabolic filter. The final section consists of two cascaded second order Sallen and Key configurations making up the remaining portion of the fifth order low pass filter.

Chapter I describes the corneo-retinal potential, electro-oculography, and the electrical eye model. The detailed analyses of each amplifier section are described in Chapters II and III. In Chapter II, the common mode rejection ratio (CMRR) of the preamplifier was also determined both at low and high frequencies. Furthermore, in Chapter II, a high frequency model of the FET was inserted into the preamplifier to verify the response and the CMRR was determined at various frequencies using this high frequency model.

In Chapter III, the parabolic low pass filter design is also explained. The intent of designing this parabolic filter is to obtain a minimum overshoot in response to a step input.

In Chapter IV, the existing preamplifier is modified so as to prevent latch up. This latch up is a disallowed state of the system, because when the output of the system reaches saturation, the system cannot reset itself.

# CHAPTER I

## BASIC CONCEPT OF THE EYE AS A SOURCE

This chapter describes corneo-retinal potential (CRP), electro-oculography, and the electrical eye model.

### Corneo-Retinal Potential (CRP)

The electrical dipole existing between the cornea and the retina of the eye is known as corneo-retinal potential (CRP) (Mowrer et al. 1936). This potential is on the order of one millivolt. It arises because of the higher metabolic rate at the retina (Young and Sheena 1975). The static electric field caused by the dipole creates a small voltage on the skin surface. This voltage changes with eye position. As shown in Figure 1, the transfer characteristic of the coupling from the CRP of the eye to the skin's surface is a sinusoidal function of the eye's angle Q.

### Electro-Oculography

Electro-oculography (EOG) is the measurement of the existing voltage of the skin surface near the eye. As shown in Figure 2, this skin voltage is measured by placing electrodes on the skin surface, in close proximity to the eye. The kind of electrodes used are normally silver silver-chloride (Ag Ag-Cl). Ag Ag-Cl is

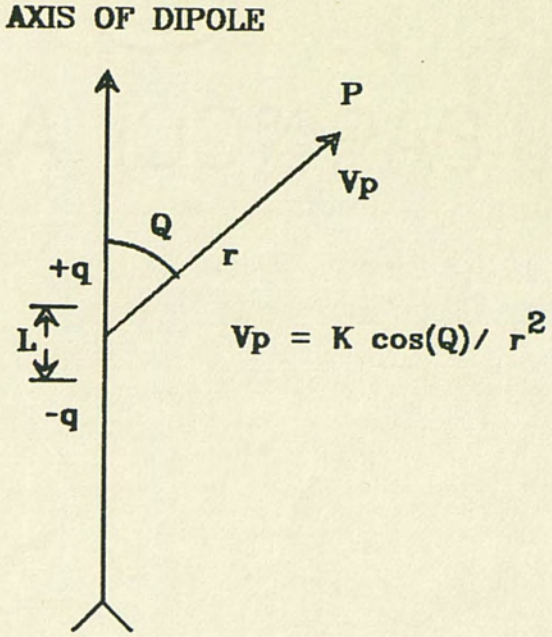



Fig. 1. Potential at a point P, at a distance r from a dipole.

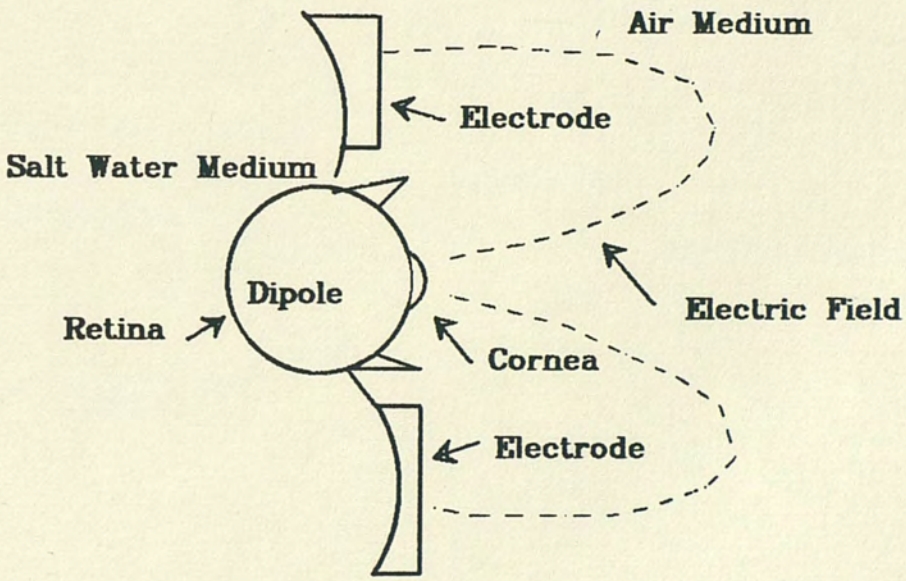



Fig. 2. Detection of skin voltage.

compatible with the body chemistry and can be used without abrading the skin to ensure electrical contact (Geddes 1972). Commercially-available electrodes (NTRON 140E) were used in this research. They are silver silver-chloride electrodes. As shown in Figure 3, a pair of electrodes placed above and below the eye are used to detect vertical eye position. Another set of electrodes are placed on the left and right temples in order to measure horizontal eye position.

A new set of electrodes are specified in Appendix A for use in a helmet-mounted electro-oculometer. The electrode is specified on the basis of shape rather than chemical properties.

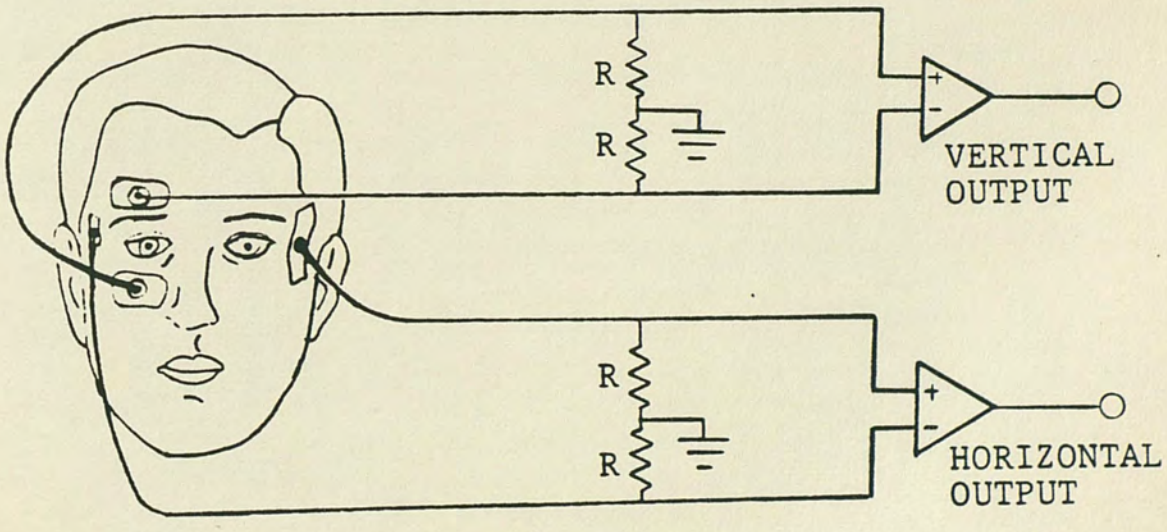



Fig. 3. Electrode placement.

## Electrical Eye Model

It is important to develop an electrical eye model before designing an electro-oculometer. The electrical eye model allows one to determine how the skin voltage changes in response to eye movements. As shown in Figure 4, the model is believed to consist of an RC network that is primarily a bandpass filter (Harris and Martin 1984). The body's blood and the layer of the skin is represented by a resistance of 20,000 ohms (Grings 1974). A capacitance of 10 nanofarads exists at the output of the model. This capacitance is a function of the large dielectric constant of the body's blood. The resistance $R_{skin}$ at the output is a function of the skin's surface resistance.

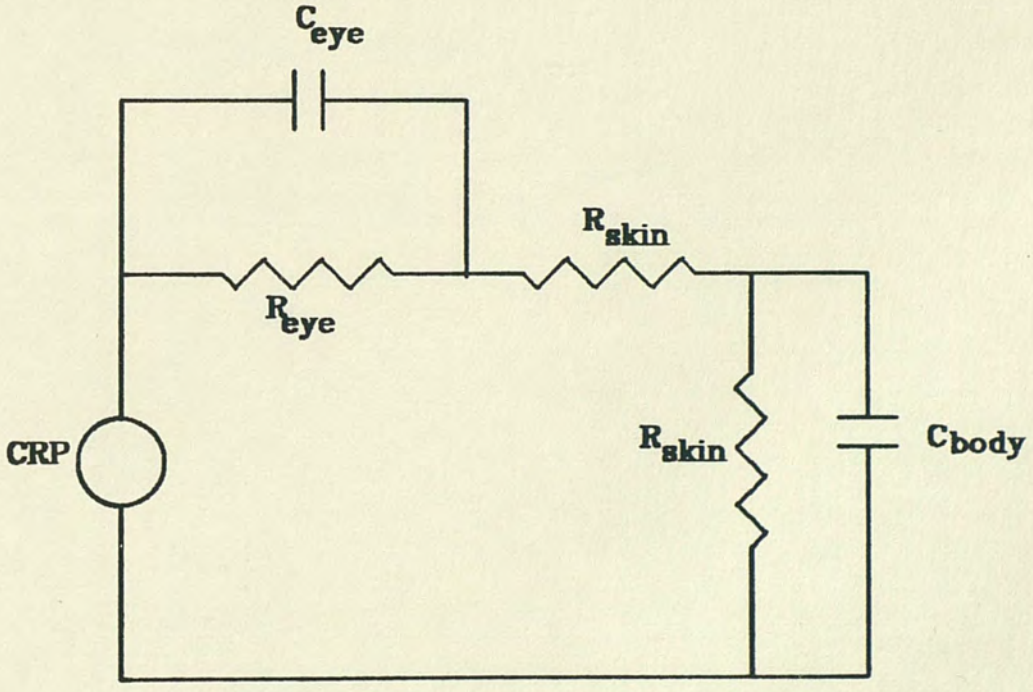



Fig. 4. Electrical eye model.

## CHAPTER II

## ANALYSIS OF THE OCULOMETER

The electro-oculometer contains three functional sections as shown in Figure 5. The first section is a differential preamplifier to amplify all eye position voltages while attenuating common mode voltages. The second is a trim amplifier. This stage also contains the first pole of the fifth order parabolic low pass filter. The final stage consists of two second order Sallen and Key low pass parabolic filters to attenuate all the frequencies above 15 hertz.

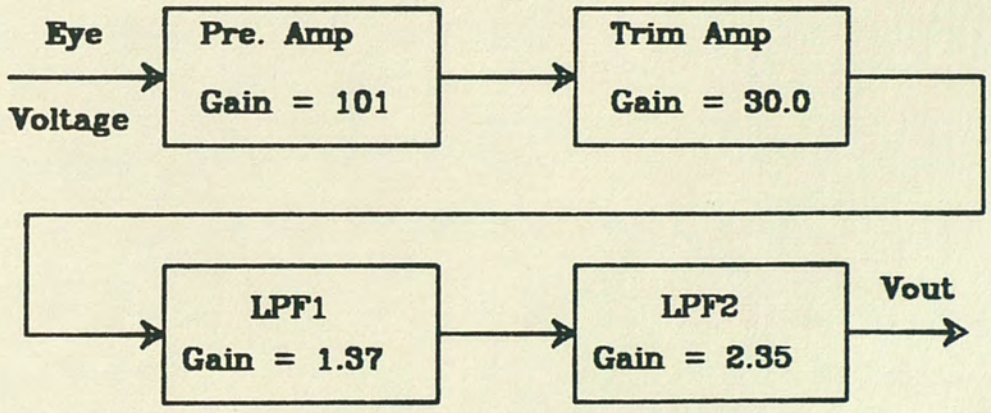



Fig. 5. Oculometer's functional block diagram (single channel).

## Preamplifier

The preamplifier shown in Figure 6 consists of an NJFET (U404) differential pair driving a BIFET (LF347) operational amplifier arranged in a negative feedback configuration. A FET differential pair was selected to provide ultra low input bias currents and high input impedance. The particular NJFET pair selected had input bias current of 10 picoamperes. The low input bias currents are needed in order to avoid charging the capacitance associated with the eye voltage source, thereby creating baseline drift. The NJFET can be biased at zero degrees temperature change to avoid warm-up drifts and ambient temperature variations. In addition, the close physical location and shared substrate of the FET's assure a uniform temperature. The uniform thickness of the substrate is also a function of the uniform temperature. The thickness of the substrate varies with the fabrication process (Mead and Conway 1980).

It becomes obvious, upon examining the databook graphs, that a very slight change in a drain current results in a substantial change in the gate to source voltage temperature coefficient. It is possible to set the voltage temperature coefficient to 0 microvolts/°C by properly setting the drain current. The drain current is set by FET 2N3823 and a resistor $R_{19}$. The FET 2N3823 exhibits a 0 TC (zero tempco) at the drain current of 750 micro ampere. At this operating point, $\frac{\partial I_{DSS}}{\partial T}$ and $\frac{\partial V_P}{\partial T}$ are zero. The

transfer characteristic of the $I_D$ and $V_{GS}$ temperature curve is given in Appendix B.

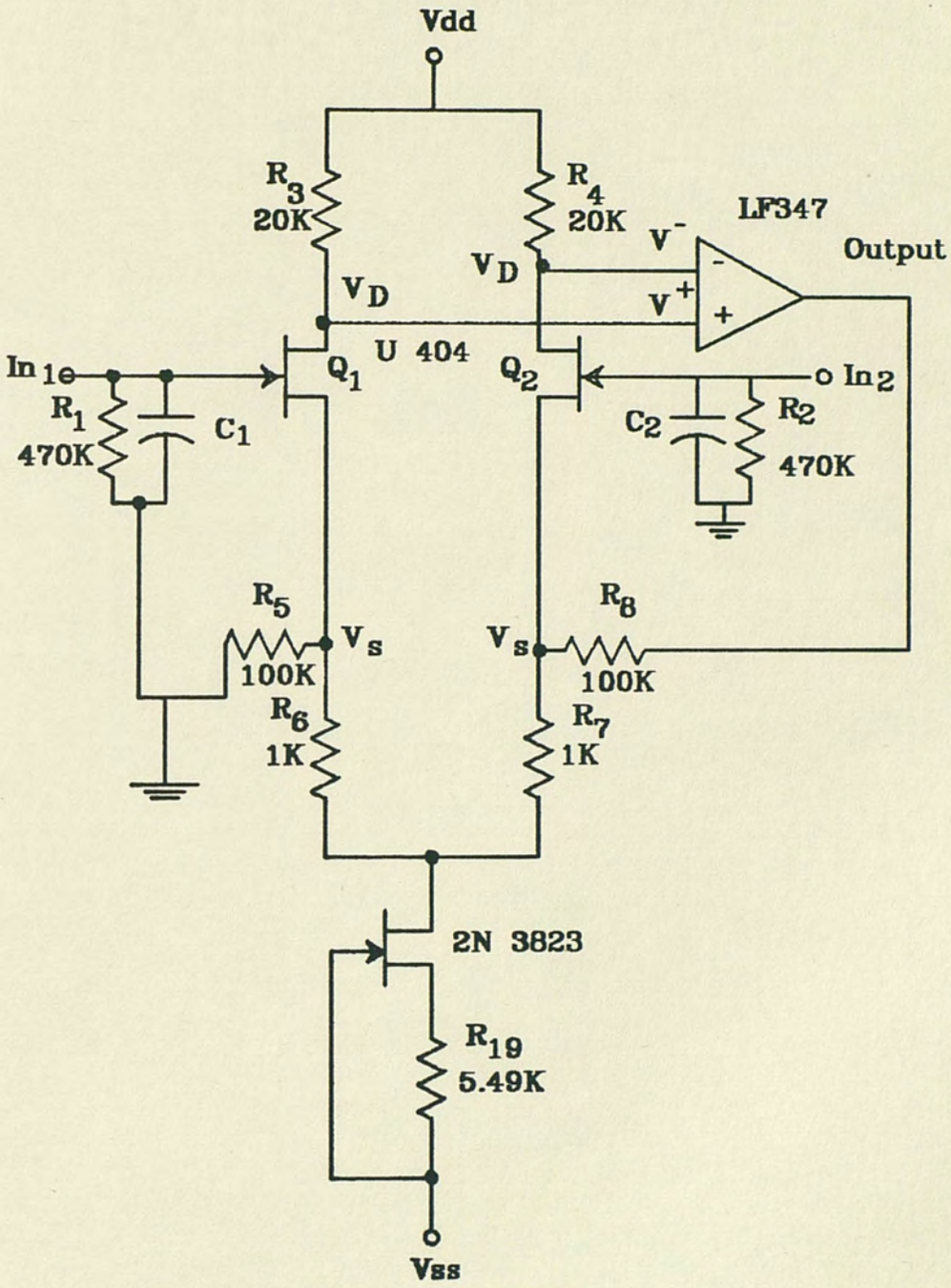



Fig. 6. Preamplifier.

In order to achieve zero tempco, the FET's of the preamplifier are biased at $I_D$ = 0.375 mAmp. The drain voltage, $V_D$ at this $I_D$ is set as shown below.

$$V_D = 7.5 \text{ v} \pm 1 \text{ v}$$

Constant current source, $I_C$ = 0.75 mAmp.

The preamplifier was designed accordingly. The description of the components is given below.

* $R_1$, $C_1$, $R_2$, and $C_2$ are selected to match the impedance of the eye voltage source
* $R_3$ and $R_4$ are selected to give

$$\frac{V_{dd} - V_s}{2} + V_s = V+, V-$$

* $R_5$, $R_6$, $R_7$ and $R_8$ = > are selected to provide the gain given by

$$A_v = \frac{R_5 + R_6 + R_7 + R_8}{R_6 + R_8}$$

* $R_{19}$ = > is chosen to adjust the current source.

The purpose of the operational amplifier (LF347) is to amplify the difference of the two drain voltages and also acts as a current feedback.

## Current Source

Whenever the FET is operated in the saturation region, its output conductance is very low. This occurs whenever the drain-source voltage $V_{DS}$ is significantly greater than the cut-off voltage $V_{GS(off)}$. The FET may be biased to operate as a constant current source at any current below its saturation current $I_{DSS}$.

For a given device where $I_{DSS}$ and $V_{GS(off)}$ are known, the approximate $V_{GS}$ required for a given $I_D$ can be set by the following equation.

$$V_{GS} = V_{GS(off)} \left[1 - \left\{\frac{I_D}{I_{DSS}}\right\}^{1/k}\right]$$

$$1.7 \leq k \leq 2$$

The resistance required between source and gate is

$$R_s = \frac{V_{GS}}{I_D}$$

The equivalent circuit of the current source is shown in Figure 8.

$$V_{gs} = - V_R$$

$$I_o = V_{ds} g_{oss} + V_{gs} g_{fs}$$

$$I_o = V_{ds} g_{oss} - I_o R_s g_{fs}$$

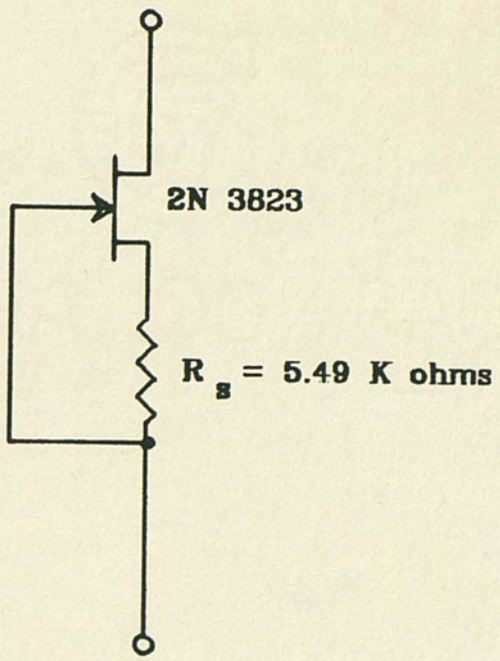



Fig. 7. Current source.

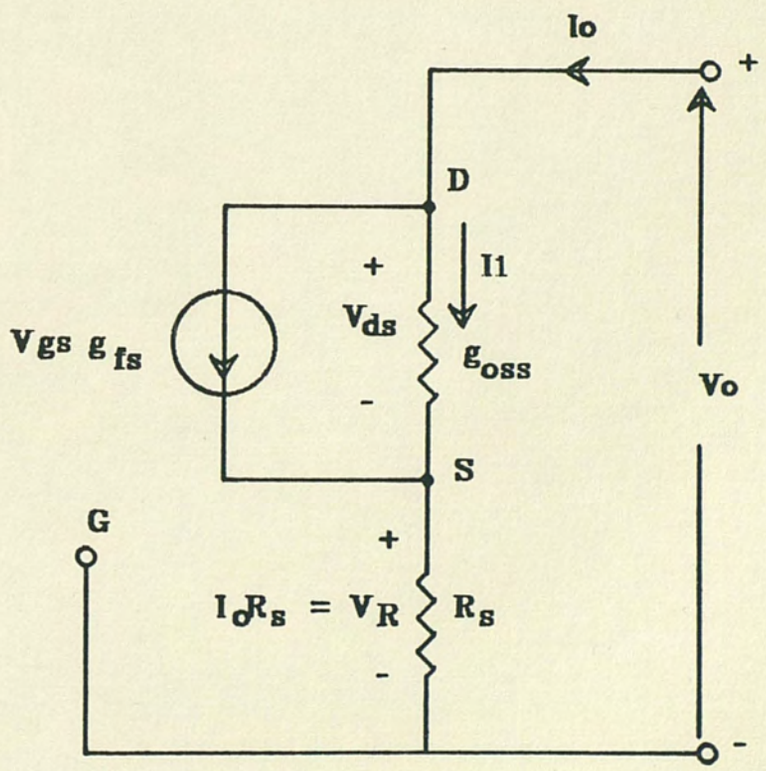



Fig. 8. Equivalent circuit of the current source.

$$I_o(1 + R_s g_{fs}) = V_{ds} g_{oss}$$

$$I_o = \frac{V_{ds} g_{oss}}{1 + R_s g_{fs}}$$

$$V_o = V_{ds} + V_R$$

$$V_o = V_{ds} + I_o R_s$$

$$V_o = V_{ds} + \frac{V_{ds} R_s g_{oss}}{1 + R_s g_{fs}}$$

$$V_o = V_{ds} \left[ \frac{1 + R_s g_{fs} + R_s g_{oss}}{1 + R_s g_{fs}} \right]$$

$$g_o = \frac{I_o}{V_o} = \frac{g_{oss}}{1 + R_s g_{fs} + R_s g_{oss}}$$

$$R_o = \frac{1}{g_o} = \frac{1 + R_s g_{fs} + R_s g_{oss}}{g_{oss}}$$

For FET 2N3823

$$g_{fs} = 3.2 \text{ E} - 3 \text{ mohs}$$

$$g_{oss} = 200 \text{ E} - 6 \text{ mohs}$$

Substituting these values, $R_o$ becomes 98.33 kilo ohms ($R_o$ = 98.33 K ohms). The current source can be replaced by $I_o$ and $R_o$.

## DC Analysis of the Preamplifier

The purpose of the following analysis is to compare the calculated values with the measured values of each node. Figure 6 can be redrawn by replacing the current source with an equivalent resistance $R_o$ and $I_o$. From Figure 9,

$$I_1 + I_2 = I_o$$

Since the circuit is symmetrical, $I_1 = I_2$

$$I_1 = I_2 = \frac{I_o}{2}$$

$$I_1 = I_2 = \frac{0.75}{2} \text{ mA} = 3.75 \text{ E} - 4 \text{ amp}$$

$$I_{s1} = I_{s2} = I_s$$

$$I_s = I_1 \frac{R_5 + R_6}{R_5} = 3.7875 \text{ E} - 4 \text{ amp}$$

$$I_s = 3.7875 \text{ E} - 4 \text{ amp}$$

$$I_{s1} = I_{D1} = I_s$$

$$I_{s2} = I_{D2} = I_s$$

$$I_{D1} = I_{D2} = I_D = 3.7875 \text{ E} - 4 \text{ amp}$$

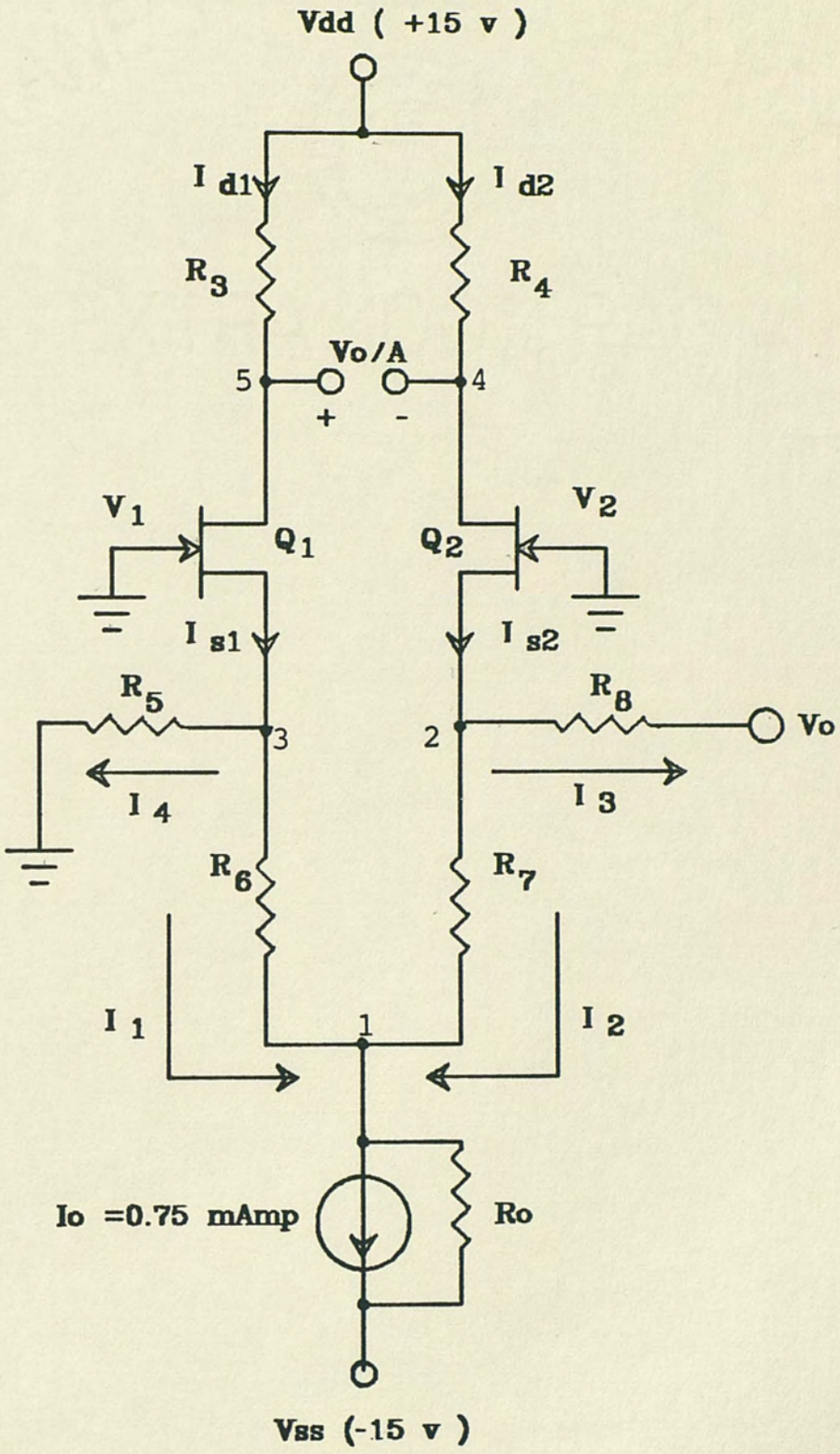



Fig. 9. Input stage (DC analysis).

Note,

$$V_{D1} = V_{dd} - I_{D1}R_3 = 15 - 7.575$$

$$V_{D1} = 7.425 \text{ volt}$$

$V_D$ is within the specification.

Now, all the node voltages are written in terms of the components. Some assumptions were made to simplify the analysis. They are stated below.

1. The output resistance of the dual NJFET is neglected.
2. $R_3 = R_4$

   $R_5 = R_8$

   $R_6 = R_7$
3. $R_o \to \infty$

From Figure 9 at node 1

$$I_1 + I_2 - I_o = 0$$

$$\frac{V_3 - V_1}{R_6} + \frac{V_2 - V_1}{R_7} - I_o = 0$$

$$- V_1 \left[\frac{1}{R_6} + \frac{1}{R_7}\right] + \frac{V_2}{R_7} + \frac{V_3}{R_6} - I_o = 0 \qquad (1)$$

at node 2

$$I_{s2} - I_2 - I_3 = 0$$

$$I_{s2} - \left[\frac{V_2 - V_1}{R_7}\right] - \left[\frac{V_2 - V_o}{R_8}\right] = 0$$

$$I_{s2} + \frac{V_1}{R_7} - V_2\left[\frac{1}{R_7} + \frac{1}{R_8}\right] + \frac{V_o}{R_8} = 0 \qquad (2)$$

at node 3

$$I_{s1} - I_1 - I_4 = 0$$

$$I_{s1} - \left[\frac{V_3 - V_1}{R_6}\right] - \left[\frac{V_3}{R_5}\right] = 0$$

$$I_{s1} + \frac{V_1}{R_6} - V_3\left[\frac{1}{R_6} + \frac{1}{R_5}\right] = 0 \qquad (3)$$

at node 4

$$I_{d2} = \frac{V_{dd} - V_4}{R_4} \qquad (4)$$

at node 5

$$I_{d1} = \frac{V_{dd} - V_5}{R_3} \qquad (5)$$

Substituting all the components value

$R_3 = R_4 = 20$ K

$R_5 = R_8 = 100$ K

$R_6 = R_7 = 1$ K

From equation (5)

$$V_5 = V_{dd} - I_{d1}R_3 \qquad (5a)$$

$$V_5 = 15 - 7.575 = 7.425 \text{ volts}$$

Ideally, $V_4 = V_5$

$$V_4 = 15 - 7.575 = 7.425 \text{ volts}$$

subtracting equation (3) from equation (2)

$$V_1 \left[\frac{1}{R_7} - \frac{1}{R_6}\right] + \left[\frac{1}{R_6} + \frac{1}{R_5}\right] (V_3 - V_2) + \frac{V_o}{R_8} = 0$$

$$V_o = R_8 \left[\frac{1}{R_5} + \frac{1}{R_6}\right] (V_2 - V_3)$$

$$V_o = 101 \ (V_2 - V_3)$$

$$V_o = A \ (V_5 - V_4)$$

where A is the open loop gain of the operational amplifier (LF347).

$$101 \ (V_2 - V_3) = A \ (V_5 - V_4)$$

$$V_2 - V_3 = \frac{A}{101} \ (V_5 + V_4)$$

Ideally, $V_2 = V_3 = V_s = I_4R_5$

$I_4 = I_s - I_1 = 3.75 \text{ E} - 6$

$V_s = 0.375$ volt

From equation (1)

$$V_1 \left[\frac{1}{R_6} + \frac{1}{R_7}\right] = (V_2 + V_3) \left(\frac{1}{R_6}\right) - I_o$$

$$V_1 \left[\frac{2}{R_6}\right] = 2\, V_2 \left(\frac{1}{R_6}\right) - I_o$$

$$V_1 = V_2 - \frac{I_o R_6}{2}$$

$V_1 = 0$ for ideal current source.

A comparison between the calculated and measured values is shown in Table 1.

TABLE 1

COMPARISON BETWEEN CALCULATED AND MEASURED VALUES

| | Calculated (Volts) | Measured (Volts) |
|---|---|---|
| $V_1$ | 0 | 0.08 |
| $V_2$ | 0.375 | 0.401 |
| $V_3$ | 0.375 | 0.390 |
| $V_4$ | 7.425 | 7.865 |
| $V_5$ | 7.425 | 7.768 |

NOTE: The difference in value is due to the mismatch of the resistor values.

## AC Analysis of the Preamplifier

The AC analysis is presented by using the small signal equivalent model of the FET. The DC power supply is connected to ground. The purpose of this analysis is to determine the common mode rejection ratio (CMRR) by finding the transfer function of the preamplifier. See Figure 10.

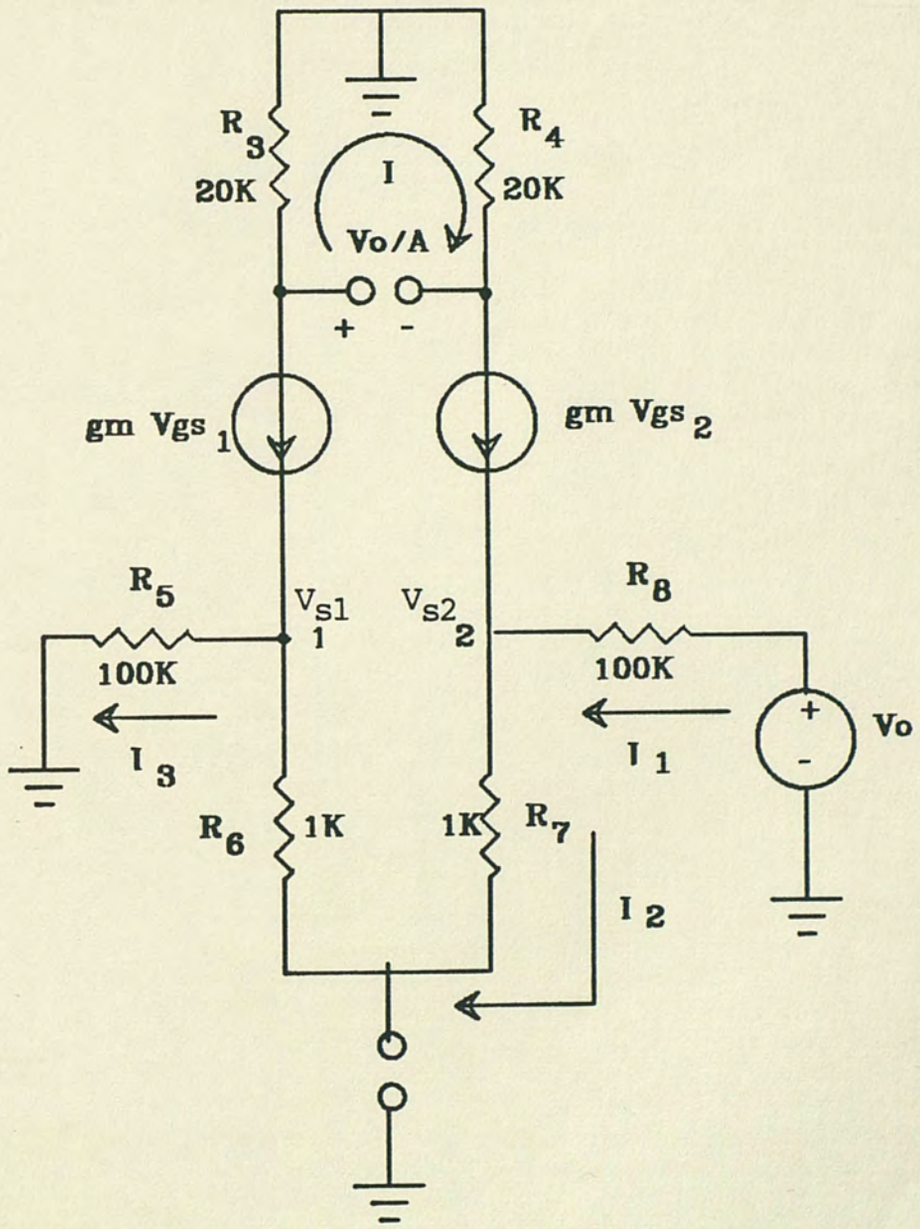



Fig. 10. Incremental analysis with FET equivalent model.

Note that for the U404 dual channel NJFET

$$V_P = - V_{GS(off)} = + 1.5 \text{ volt}$$

$$V_{gs} = + 0.9 \text{ volt}, \; I_{DSS} = 1.5 \text{ m Amp}$$

At 0.9 volt, $V_{gs}$ does not vary with the temperature.

$$g_m = \frac{2}{(|V_P|)} \sqrt{I_D I_{DSS}}$$

$$g_m = \frac{2}{(|1.5|)} \sqrt{(3.7875 \text{ E} - 4)\ 1.5 \text{ E} - 3}$$

$$g_m = 1.0049 \text{ E} - 3 \text{ mohs}$$

From Figure 10, at node 2

$$I_1 + g_m V_{gs2} - I_2 = 0$$

$$\frac{V_o - V_{s2}}{R_8} + g_m V_{gs2} - \frac{V_{s2} - V_{s1}}{R_6 + R_7} = 0 \qquad (6)$$

at node 1

$$I_2 + g_m V_{gs1} - I_3 = 0$$

$$\frac{V_{s2} - V_{s1}}{R_6 + R_7} + g_m V_{gs1} - \frac{V_{s1}}{R_5} = 0 \qquad (7)$$

Writing a KVL for loop I:

$$-\frac{V_o}{A} g_m V_{gs1} R_3 + g_m V_{gs2} R_4 = 0 \qquad (8)$$

Assuming that

$$g_m = g_{m1} = g_{m2}$$

$$R_3 = R_4$$

$$R_5 = R_8$$

$$R_6 = R_7$$

Note that $V_{gs} = V_g - V_s$; $V_{gs1} = V_{g1} - V_{s1}$; $V_{gs2} = V_{g2} - V_{s2}$

From equation (6)

$$\frac{V_o}{R_8} + g_m V_{g2} = \frac{V_{s2}}{R_8} + \frac{V_{s2}}{R_6 + R_7} - \frac{V_{s1}}{R_6 + R_7} + g_m V_{s2}$$

$$V_o + g_m R_5 V_{g2} = V_{s2} \left[1 + \frac{R_5}{2R_6} + g_m R_5\right] - V_{s1} \frac{R_5}{2R_6} \qquad (6a)$$

From equation (7)

$$\frac{V_{s2}}{2R_6} - \frac{V_{s1}}{2R_6} = \frac{V_{s1}}{R_5} - g_{m1} (V_{g1} - V_{s1})$$

$$g_m R_5 V_{g1} = V_{s1} \left[1 + \frac{R_5}{2R_6} + g_m R_5\right] - V_{s2} \frac{R_5}{2R_6} \qquad (7a)$$

From equation (8)

$$\frac{V_o}{A} + g_m R_3 \, (V_{g1} - V_{s1}) = g_m R_3 \, (V_{g2} - V_{s2})$$

$$\frac{V_o}{A} + g_m R_3 \, (V_{g1} - V_{g2}) = g_m R_3 \, (V_{s1} - V_{s2}) \qquad (8a)$$

subtracting equation (6a) from equation (7a)

$$- V_o + g_m R_5 \, (V_{g1} - V_{g2}) = V_{s1} \left[1 + \frac{R_5}{R_6} + g_m R_5\right] - V_{s2} \left[1 + \frac{R_5}{R_6} + g_m R_5\right]$$

$$(V_{s1} - V_{s2}) = \frac{g_m R_5 \, (V_{g1} - V_{g2}) - V_o}{\left[1 + \frac{R_5}{R_6} + g_m R_5\right]} \qquad (9)$$

From equation (8a)

$$\frac{V_o}{A g_m R_3} = (V_{s1} - V_{s2}) - (V_{g1} - V_{g2})$$

Substituting the equation (9)

$$\frac{V_o}{A g_m R_3} = \left[\frac{g_m R_5 \, (V_{g1} - V_{g2}) - V_o}{1 + \frac{R_5}{R_6} + g_m R_5}\right] - (V_{g1} - V_{g2})$$

$$\frac{V_o}{Ag_mR_3} = \frac{g_mR_5\ (V_{g1} - V_{g2}) - V_o - (V_{g1} + V_{g2})\ (1 + \frac{R_5}{R_6} + g_mR_5)}{1 + \frac{R_5}{R_6} + g_mR_5}$$

$$\frac{V_o}{Ag_mR_3} = \frac{-V_o - (V_{g1} + V_{g2})\ (1 + \frac{R_5}{R_6})}{1 + \frac{R_5}{R_6} + g_mR_5}$$

$$\frac{V_o}{V_{g2} - V_{g1}} = \frac{1 + \frac{R_5}{R_6}}{1 + \frac{1 + \frac{R_5}{R_6} + g_mR_5}{Ag_mR_3}}$$

$$V_o = (Vg_2 - V_{g1}) \frac{1 + \frac{R_5}{R_6}}{1 + \frac{1 + \frac{R_5}{R_6} + g_mR_5}{Ag_mR_3}}$$

For $V_{g1} = 0$

$$V_o = V_{g2} \frac{1 + \frac{R_5}{R_6}}{1 + \frac{1 + \frac{R_5}{R_6} + g_mR_5}{Ag_mR_3}}$$

For $V_{g2} = 0$

$$V_o = V_{g1} \frac{1 + \frac{R_5}{R_6}}{1 + \frac{\frac{R_5}{R_6} + g_m R_5}{A g_m R_3}}$$

At a frequency of 15 Hz, A (open-loop operational amplifier gain) is 108 dB, which is equivalent to 25.11E4.

For $V_{g2} = 0$

$$A_1 = \frac{V_o}{V_{g1}} = - \frac{1 + \frac{R_5}{R_6}}{1 + \frac{\frac{R_5}{R_6} + g_m R_5}{A g_m R_3}}$$

$$A_1 = - 100.9959$$

For $V_{g1} = 0$

$$A_2 = \frac{V_o}{V_{g2}} = \frac{1 + \frac{R_5}{R_6}}{1 + \frac{\frac{R_5}{R_6} + g_m R_5}{A g_m R_3}}$$

$$A_2 = 100.9959$$

Difference mode gain,

$$A_d = \frac{A_1 - A_2}{2}$$

$$A_d = 100.9959 \frac{\text{volt}}{\text{volt}}$$

Common mode gain,

$$A_c = A_1 + A_2 = 0$$

Assuming one percent difference in all resistors values, $A_d$ decreases to 99.989 volt/volt and $A_c$ increases to 0.02 volt/volt.

$$\text{CMRR} = \frac{A_d}{A_c} = 73.978 \text{ dB}$$

The comparison between the calculated and the measured values is given in Table 2. The measured common mode gain is much higher than the calculated common mode gain. The wide variation is due to the mismatch of the resistors values. For example,

$$A_c = A_1 + A_2 = \frac{1 + \frac{R_5}{R_6}}{1 + \frac{1 + \frac{R_5}{R_6} + g_m R_5}{A g_m R_3}} - \frac{1 + \frac{R_5}{R_6}}{1 + \frac{1 + \frac{R_5}{R_6} + g_m R_5}{A g_m R_3}}$$

Assuming one to two percent error in resistor values.

$$A_c = \frac{1 + \frac{R_5}{R_6}}{1 + \frac{1 + \frac{R_5}{R_6} + g_m R_5}{A g_m R_3}} - \frac{1 + \frac{1.0015\ R_5}{R_6}}{1 + \frac{1 + \frac{R_5}{0.99\ R_6} + g_m\ 1.01\ R_5}{A g_m\ 0.99\ R_3}}$$

$$A_c = 0.15$$

TABLE 2

CALCULATED AND MEASURED VALUES

| | Calculated | Measured |
|---|---|---|
| $A_d$ | 100.999 | 100 |
| $A_c$ | 0.02 | 0.15 |
| CMRR | 73.98 dB | 56.5 dB |

It is clear that the higher common mode gain results from the mismatch of the resistor values.

## AC High Frequency Model

The capacitance between the channel and the gate of a FET is a function of $V_{GS}$ and $V_{DS}$. This capacitance is distributed not in one particular area. Because of the complexity of dealing with

such a distributed capacitance, a simplification is made so that the two lumped capacitances, $C_{gs}$ and $C_{gd}$, exist between the gate and the source and drain, respectively. A much smaller capacitance, $C_{ds}$, also exists between the drain and the source. This capacitance is small enough that it can be ignored for most purposes. The equivalent capacitance from the gate to the source, $C_{gs}$, is shunted by a very large input resistance, $r_{gs}$. Similarly, the equivalent capacitance from the gate to drain is shunted by a large resistance, $r_{gd}$. For most purposes, $r_{gs}$ and $r_{gd}$ are neglected and the gate impedance of the FET treated as pure capacitance. The resulting equivalent circuit is shown in Figure 11. From the databook,

$$C_{dss},\ C_{oss} \approx C_{gd}$$

$$C_{gd} = C_{rss}$$

$$C_{gs} = C_{iss} - C_{gd} = C_{iss} - C_{rss}$$

For U 404 FET,

$$g_{os} = 20\ \mu\text{mohs}$$

$$r_{ds} = \frac{1}{g_{os}} = 50\ \text{Kohms}$$

$$C_{iss} = 8\text{pF} = 8\text{E} - 12\text{F}$$

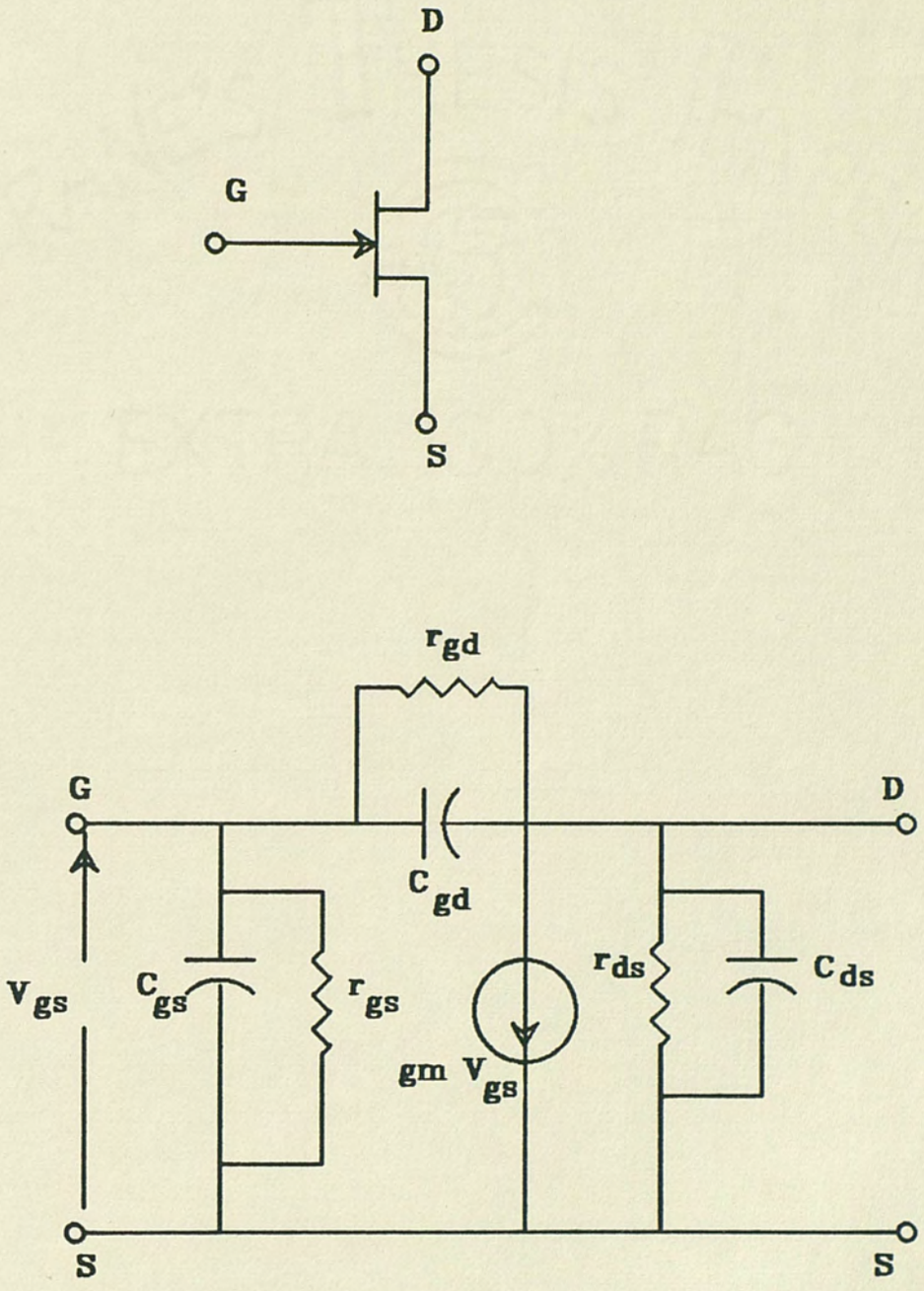



Fig. 11. FET high frequency model.

$$C_{pss} = 3pF = 3E - 12F$$

$$C_{gd} = C_{rss} = 3pF$$

$$C_{gs} = C_{iss} - C_{rss} = 8pF - 3pF = 5pF$$

$$C_{gd} = 3pF$$

$$C_{gs} = 5pF$$

$$r_{ds} = 50 \text{ Kohms}$$

Figure 11 is further simplified as shown in Figures 12 and 13. From Figure 13, we obtain

$$I(s) = \frac{g_m V_{gs} r_{ds}}{r_{ds} + \frac{1}{sC_{gd}} + \frac{1}{sC_{gs}}}$$

The preamplifier is drawn by replacing the FET's by the high frequency model, as shown in Figure 14. The following node equations are written by referring to Figure 14. At node 2

$$I_1 + \frac{g_m V_{gs2} r_{ds2}}{r_{ds2} + \frac{1}{sC_{gd2}} + \frac{1}{sC_{gs2}}} - I_2 = 0$$

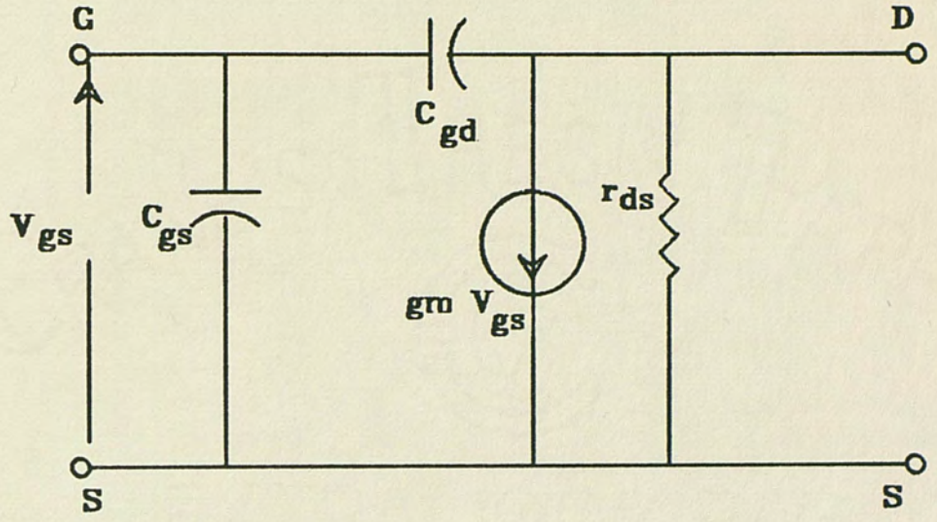



Fig. 12. Simplified form of FET high frequency model.

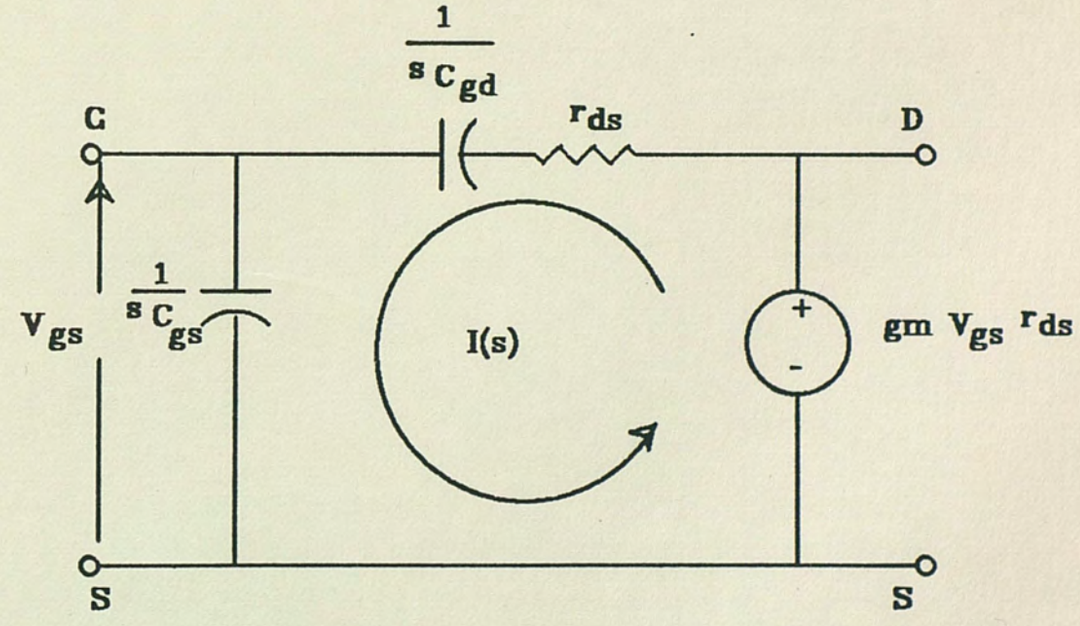



Fig. 13. Equivalent circuit.

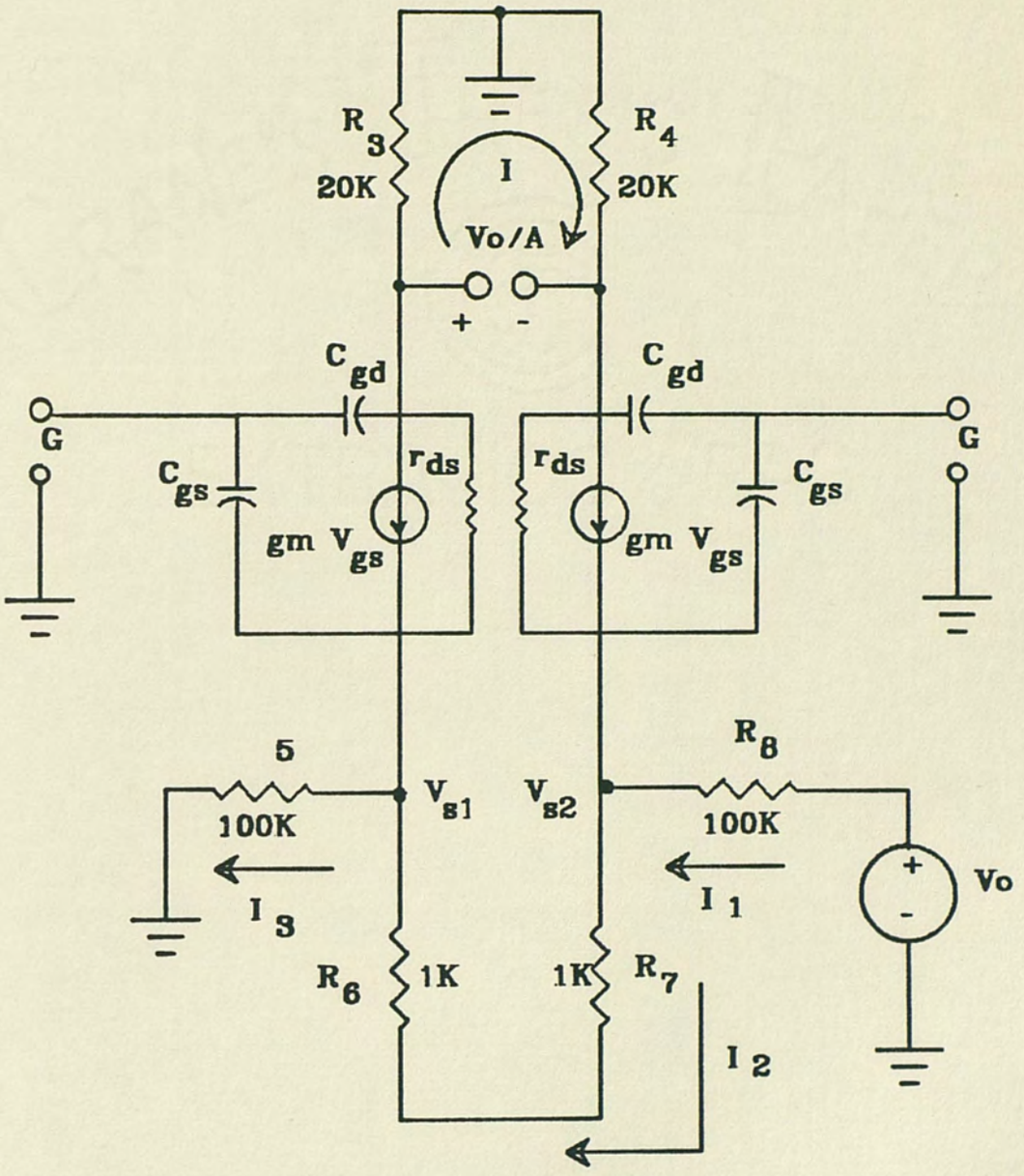



Fig. 14. AC high frequency input stage.

$$\frac{V_o - V_{s2}}{R_8} + \frac{g_m V_{gs2} r_{ds2}}{r_{ds2} + \frac{1}{sC_{gd2}} + \frac{1}{sC_{gs2}}} - \frac{V_{s2} - V_{s1}}{R_6 + R_7} = 0 \qquad (10)$$

$$I_2 + \frac{g_m V_{gs1} r_{ds1}}{r_{ds1} + \frac{1}{sC_{gd1}} + \frac{1}{sC_{gs1}}} - I_3 = 0$$

$$- \frac{V_{s1}}{R_5} + \frac{g_m V_{gs1} r_{ds1}}{r_{ds1} + \frac{1}{sC_{gd1}} + \frac{1}{sC_{gs1}}} - \frac{V_{s2} - V_{s1}}{R_6 + R_7} = 0 \qquad (11)$$

Writing KVL for loop 1

$$- \frac{V_o}{A} - \frac{g_m V_{gs1} r_{ds1}}{r_{ds1} + \frac{1}{sC_{gd1}} + \frac{1}{sC_{gs1}}} R_3 + \frac{g_m V_{gs2} r_{ds2}}{r_{ds2} + \frac{1}{sC_{gd2}} + \frac{1}{sC_{gs2}}} R_4 = 0 \qquad (12)$$

Making the assumptions that

$$r_{ds1} = r_{ds2} = r_{ds}$$

$$C_{gd1} = C_{gd2} = C_{gd}$$

$$C_{gs1} = C_{gs2} = C_{gs}$$

From equation (10)

$$\frac{V_o - V_{s2}}{R_5} + \frac{g_m r_{ds}}{r_{ds} + \frac{1}{sC_{gd}} + \frac{1}{sC_{gs}}} (V_{g2} - V_{s2}) - \frac{V_{s2} - V_{s1}}{2R_6} = 0 \quad (10a)$$

From equation (11)

$$- \frac{V_{s1}}{R_5} + \frac{g_m r_{ds}}{r_{ds} + \frac{1}{sC_{gd}} + \frac{1}{sC_{gs}}} (V_{g1} - V_{s1}) - \frac{V_{s2} - V_{s1}}{2R_6} = 0 \quad (11a)$$

From equations (10a) and (11a)

$$(V_{s1} - V_{s2}) = \frac{- V_o + \frac{g_m R_5 r_{ds}}{r_{ds} + \frac{1}{sC_{gd}} + \frac{1}{sC_{gs}}} (V_{g1} - V_{g2})}{[1 + \frac{g_m R_5 r_{ds}}{r_{ds} + \frac{1}{sC_{gd}} + \frac{1}{sC_{gs}}} + \frac{R_5}{R_6}]} \quad (13)$$

From equation (12)

$$\frac{V_o}{A} + \frac{g_m R_3 r_{ds}}{r_{ds} + \frac{1}{sC_{gd}} + \frac{1}{sC_{gs}}} (V_{g1} - V_{s1}) = \frac{g_m R_3 r_{ds}}{r_{ds} + \frac{1}{sC_{gd}} + \frac{1}{sC_{gs}}} (V_{g2} - V_{s2})$$

$$\frac{V_o}{A} + \frac{g_m R_3 r_{ds}}{r_{ds} + \frac{1}{sC_{gd}} + \frac{1}{sC_{gs}}} (V_{g1} - V_{g2}) = \frac{g_m R_3 r_{ds}}{r_{ds} + \frac{1}{sC_{gd}} + \frac{1}{sC_{gs}}} (V_{s1} - V_{s2}) \quad (12a)$$

Substituting equation (13)

$$\frac{V_o}{V_{g2} - V_{g1}} = \frac{(1 + \frac{R_5}{R_6})\, Ag_m R_3 r_{ds}}{(1 + \frac{R_5}{R_6})\,(r_{ds} + \frac{1}{sC_{gd}} + \frac{1}{sC_{gs}}) + g_m r_{ds}\,(R_5 + AR_3)}$$

Let

$$r_{ds} + \frac{1}{sC_{gd}} + \frac{1}{sC_{gs}} = Z_1(s)$$

$$Z_1(\omega) = 50K + j\,(-\frac{1}{1.875E - 12})$$

$$V_o(\omega) = [V_{g2}(\omega) - V_{g1}(\omega)]\, \frac{(1 + \frac{R_5}{R_6})\, Ag_m R_3 r_{ds}}{(1 + \frac{R_5}{R_6})\, Z_1(\omega) + g_m r_{ds}\,(R_5 + AR_3)}$$

For $V_{g1}(\omega) = 0$,

$$A_1(\omega) = \frac{V_o(\omega)}{V_{g1}(\omega)} = -\frac{(1 + \frac{R_5}{R_6})\, Ag_m R_3 r_{ds}}{(1 + \frac{R_5}{R_6})\, Z_1(\omega) + g_m r_{ds}\,(R_5 + AR_3)}$$

For $V_{g2}(\omega) = 0$,

$$A_2(\omega) = -A_1(\omega)$$

Difference mode gain,

$$A_d(\omega) = \frac{A_1(\omega) - A_2(\omega)}{2}$$

Common mode gain,

$$A_c(\omega) = A_1(\omega) + A_2(\omega)$$

$$A_c(\omega) = 0 \text{ (ideally)}$$

$$CMRR(\omega) = \frac{A_d(\omega)}{A_c(\omega)}$$

at frequency, f = 15 Hz

$$\omega = 2\pi f = 94.247 \text{ rad/s}$$

$$A = 108 \text{ dB} = 25.11 \text{ E } 4$$

$$g_m = 1.0049\text{E} - 3 \text{ mohs}$$

$$A_1(\omega) = - 30.83$$

$$A_d(\omega) = \left|\frac{- 30.83 - 30.83}{2}\right| = 30.83$$

Assuming one percent variation in all resistive components.

$$A_c(\omega) = 0.02$$

$$A_d(\omega) = 30.52$$

$$CMRR(\omega) = 63.67 \text{ dB}$$

at frequency, f = 100 Hz

$$\omega = 2\pi f = 628.318 \text{ rad/s}$$

$$A = 90 \text{ dB} = 31.662 \text{ E } 3$$

$$g_m = 1.0049\text{E} - 3 \text{ mohs}$$

$$A_1(\omega) = - 27.31$$

$$A_d(\omega) = \left|\frac{- 27.03 - 27.03}{2}\right| = 27.03$$

$$A_c(\omega) = 0.02$$

$$A_d(\omega) = 27.03$$

$$\text{CMRR}(\omega) = 62.62 \text{ dB}$$

at frequency, f = 1000 Hz

$$\omega = 2\pi f = 6283.18 \text{ rad/s}$$

$$A = 70 \text{ dB} = 31.662 \text{ E } 2$$

$$g_m = 1.0049\text{E} - 3 \text{ mohs}$$

$$A_1(\omega) = - 27.3$$

$$A_d(\omega) = \left|\frac{- 27.3 - 27.3}{2}\right| = 27.03$$

$$A_c(\omega) = 0.02$$

$$A_d(\omega) = 27.0$$

$$CMRR(\omega) = 62.6 \text{ dB}$$

The CMRR varies depending on the FET model being used. The CMRR of the preamplifier degraded by 10 dB while using the high frequency model of the FET. Some variation of CMRR with respect to frequency are shown in Table 3.

TABLE 3

CMRR AND FREQUENCY

| f (Hz) | CMRR (dB) |
|---|---|
| 15 | 63.67 |
| 100 | 62.62 |
| 1000 | 62.6 |

CHAPTER III

TRIM AMPLIFIER AND FILTER DESIGN

This chapter describes the analysis of the trim amplifier and the low pass filter.

## Trim Amplifier

The function of the trim amplifier is to adjust the offset voltage inherent in the preamplifier. It is a summing inverting integrator as shown in Figure 15. The circuit can be expressed in block diagram form as shown in Figure 16.

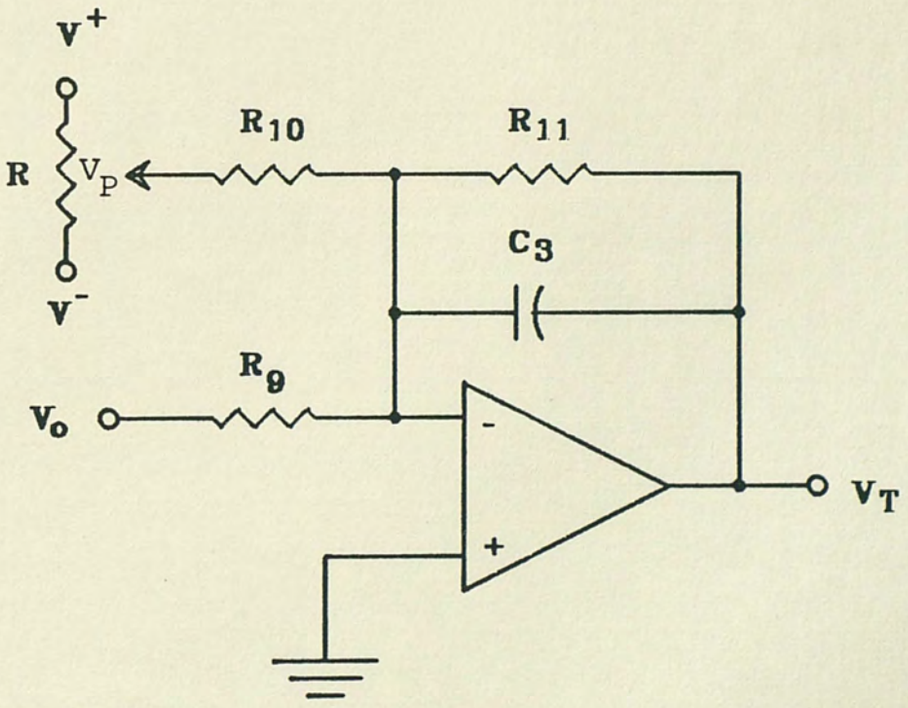



Fig. 15. Trim amplifier.

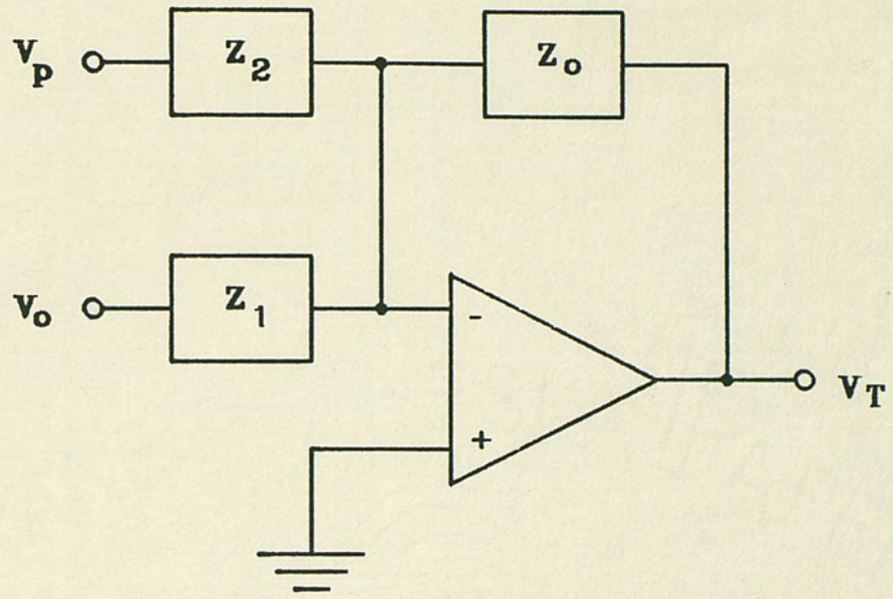



Fig. 16. Block diagram of the trim amplifier.

From Figure 15,

$$V_P = \frac{V^- + (V^+ - V^-)\ (1 - \Delta)\ R}{\Delta R + R - \Delta R}$$

$$V_P = V^+ + \Delta(V^- - V^+)$$

where $\Delta$ is less than 1.

$$R_T = \frac{\Delta R(1 - \Delta)R}{\Delta R + (1 - \Delta)R}$$

$$Z_2 = R_{10}$$

$$Z_1 = R_9$$

$$Z_o = \frac{R_{11}}{R_{11}\, C_3 s + 1}$$

$$V_T = Z_o \left(\frac{V_P}{Z_2} + \frac{V_o}{Z_1}\right)$$

$$V_T = \left[- \frac{R_{11}}{R_{11}\, C_3 s + 1}\right] \left[\frac{V^+ + \Delta(V^- - V^+)}{R_{10}} + \frac{V_o}{R_9}\right]$$

$R_{11}$ and $C_3$ are selected to provide the first order pole of the low pass filter with a cutoff frequency of 15 hertz. The ratio of $R_{11}$ and $R_9$ provides a gain of 30.3 volt/volt for the trim amplifier signal path.

## Low Pass Filter

The low pass filter is needed to remove any 60 hertz power line signals that were not rejected by the preamplifier. There are two possible filter approximations that can be used in this application. These are the Butterworth and Parabolic filters. A Butterworth filter has the flattest possible response within the passband of all possible filters. The roots of the Butterworth polynomial approximation are found by solving

$$1 + (-s^2)^n = 0$$

The roots are located on a unit circle in the complex s-plane, spaced 180/n degrees apart, where n is the order of the filter. The root locations in polar form are specified as follows:

M = 1 rad/sec, where M is the magnitude

$\alpha = 90 + (k + \frac{1}{2})\ 180/n$ degrees, where k = 0, 1, 2, ..., (n - 1)/2 and $\alpha$ is the angle measured with respect to the positive real axis. The normalized function for a fifth order Butterworth filter is given by (Daryanni 1976)

$$H(s) = \frac{1}{(s + 1)(s^2 + 1.618s + 1)(s^2 + 0.618s + 1)}$$

The filter has a 12.8 percent overshoot in response to a step input.

On the other hand, the roots of the parabolic polynomial approximation lie on a parabola in the complex s-plane. The normalized transfer function for the filter is given by

$$H(s) = \frac{5.33}{(s + 1)(s^2 + 1.895s + 1.371)(s^2 + 1.219s + 3.888)}$$

This filter was designed and measured to have less than one percent overshoot in response to a step input. Theoretically, the overshoot is zero. The parabolic approximation was chosen instead of the Butterworth approximation because of the minimum value of the step response overshoot.

## Parabolic Filter Design

The transfer function of the parabolic filter is given by (Martin and Harris 1984)

$$\frac{V_o(s)}{V_i(s)} = \frac{H_o}{\left(\frac{s}{(\omega_o)} + 1\right)\left(\frac{s^2}{(\omega_1)^2} + \frac{s\ 2\cos\ \theta_1}{(\omega_1)} + 1\right)\left(\frac{s^2}{(\omega_2)^2} + \frac{s\ 2\cos\ \theta_2}{(\omega_2)} + 1\right)}$$

180/5 = 36 degree

$$\theta = 0°$$

$$\theta_1 = 36°$$

$$\theta_2 = 72°$$

$$\left(\frac{s}{\omega_o} + 1\right)\left(\frac{s^2}{1.371} + \frac{1.895s}{1.368} + 1\right)\left(\frac{s^2}{3.888} + \frac{1.219s}{3.888} + 1\right)$$

$$= \left(\frac{s}{\omega_o} + 1\right)\left(\frac{s^2}{1.371} + 1.3852s + 1\right)\left(\frac{s^2}{3.888} + 0.31352s + 1\right)$$

Now, equating the coefficient of s and $s^2$ for each root,

$$\frac{2\ \cos\ \theta_1}{\omega_1} = 1.3852$$

$$\omega_1^2 = 1.371$$

$$\omega_1 = 1.170897\,\omega_o \text{ rad/sec}$$

$$\frac{2 \cos \theta_2}{\omega_2} = 0.31352$$

$$\omega_2^2 = 3.888$$

$$\omega_2 = 1.9718\omega_o \text{ rad/sec}$$

$$\omega_o = \frac{1}{R_o C}$$

Let C = 0.1 μF (constant capacitance design)

$f_o$ = 15 Hz

$$\omega_o = 2\pi f_o = 94.24 \text{ rad/s}$$

$$R_o = \frac{1}{\omega_o C} = 106.1 \text{ Kohms}$$

$$R_1 = \frac{1}{1.170897\omega_o C} = 90.624 \text{ Kohms}$$

$$R_2 = \frac{1}{1.9718\omega_o C} = 53.814 \text{ Kohms}$$

Let

$$R_3 = R_5 = 10 \text{ Kohms}$$

$$R_3 (2 - 2 \cos \theta_1) = 3.819 \text{ Kohms} = R_4$$

$$R_5 (2 - 2 \cos \theta_2) = 13.819 \text{ Kohms} = R_6$$

The first order of the fifth order low pass filter was constructed in the trim amplifier with $R_o$ and C. The two second order Sallen and Key low pass filters were cascaded to produce a fourth order low pass filter. The complete diagram is shown in Figure 17. Frequency response and step response of the filter were conducted. In order to measure rise time, overshoot and frequency response easily on the oscilloscope, all the capacitors value was changed from 0.1 μF to 1500 pF.

The step response of the filter is shown in Figure 18. From Figure 18, the overshoot is 2 percent. The frequency response of the filter is shown in Table 4 and Figure 19. The gain of the parabolic filter is expressed by the following equation.

$$A_{v(\text{parabolic})} = \left(\frac{R_{11}}{R_9}\right)\left(1 + \frac{R_3 (2 - 2 \cos \theta_1)}{R_3}\right)\left(1 + \frac{R_5 (2 - 2 \cos \theta_1)}{R_5}\right)$$

$R_{11}$ and $R_9$ are in the trim amplifier

$$A_{v(\text{parabolic})} = 97.55$$

A computer program (Appendix B) is written for finding the pole locations of any order filter up to the one-hundredth order.

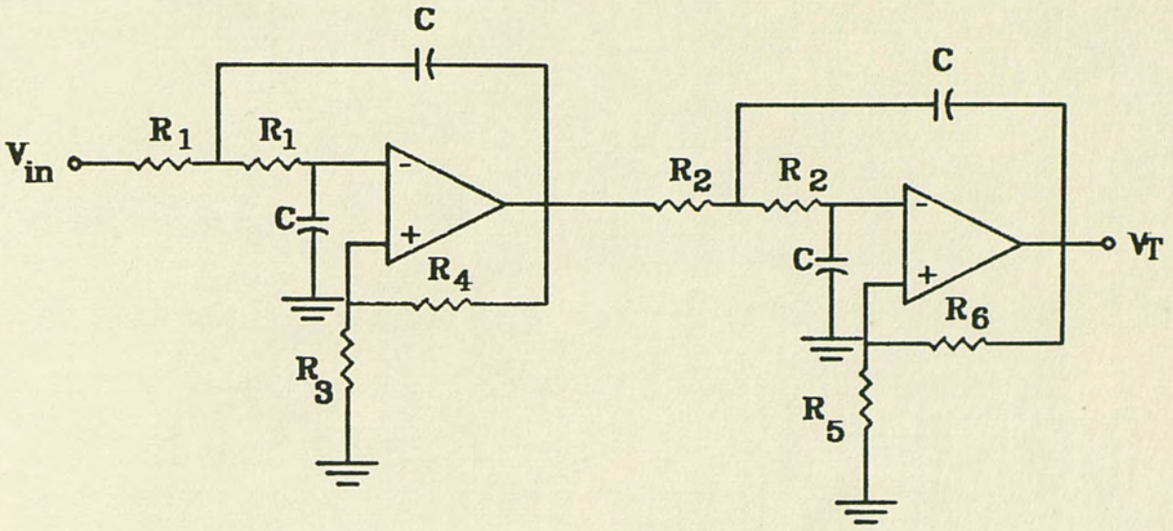



Fig. 17. Fourth order low pass filter.

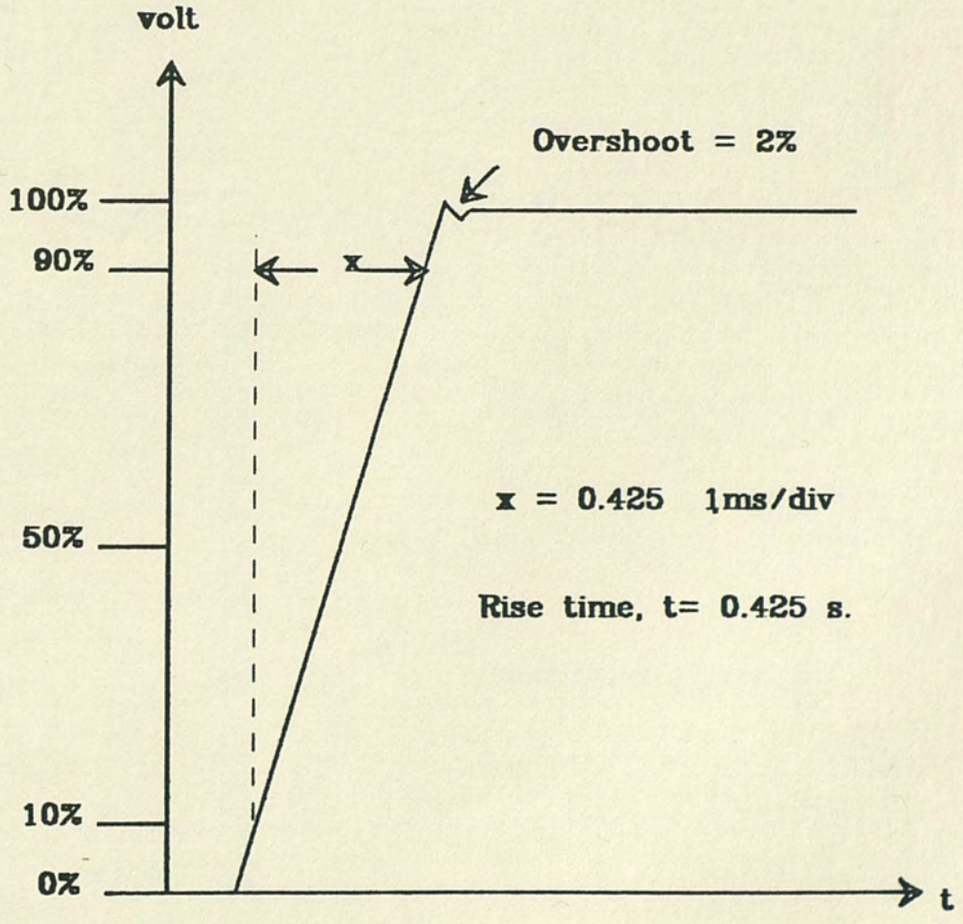



Fig. 18. Step response of the filter.

TABLE 4

PARABOLIC FILTER FREQUENCY RESPONSE DATA

| f (Hz) | $V_{out}$ (volts) |
|---|---|
| 20 | 1.2 |
| 40 | 1.2 |
| 60 | 1.2 |
| 80 | 1.2 |
| 100 | 1.2 |
| 120 | 1.2 |
| 140 | 1.2 |
| 160 | 1.18 |
| 180 | 1.18 |
| 200 | 1.18 |
| 400 | 0.92 |
| 600 | 0.84 |
| 800 | 0.74 |
| 1000 | 0.64 |
| 2000 | 0.17 |

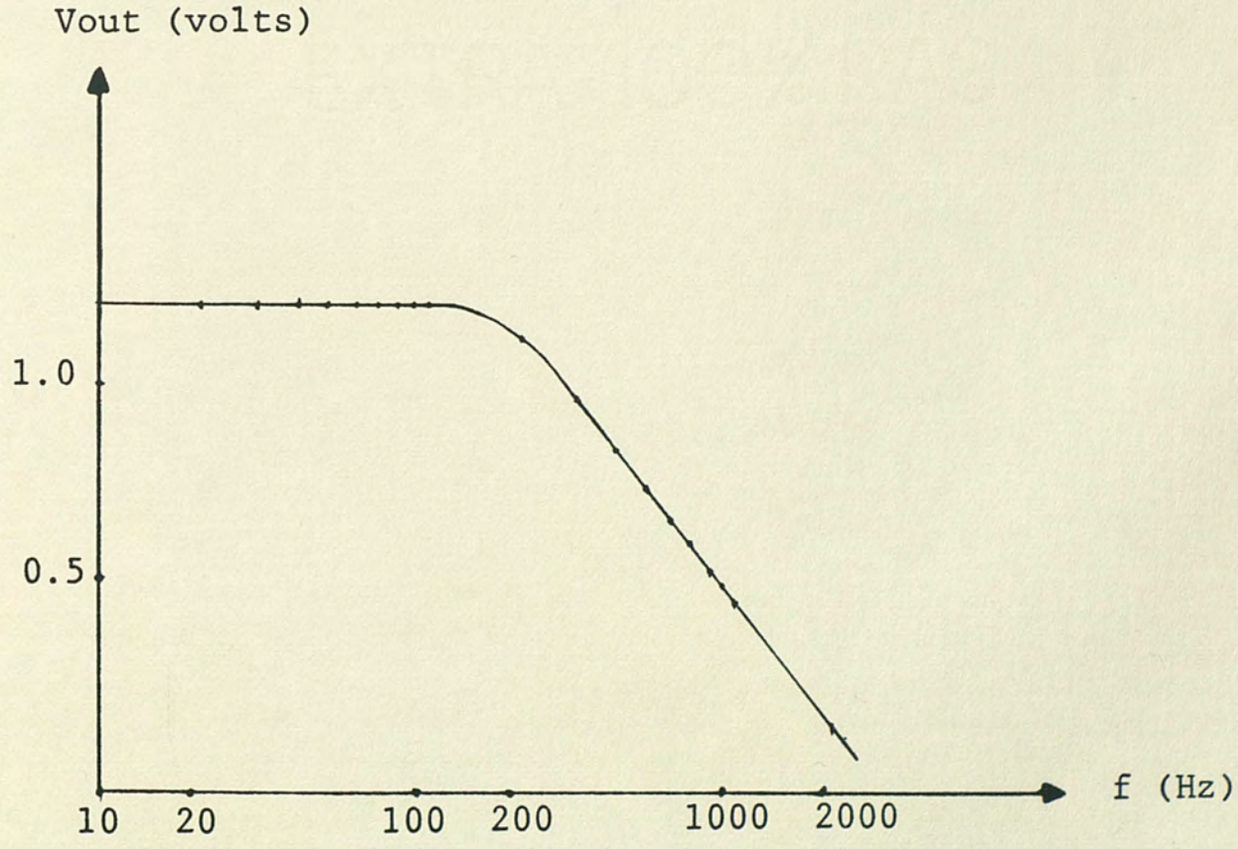



Fig. 19. Parabolic filter frequency response.

# CHAPTER IV

## SUGGESTED DESIGN OF PREAMPLIFIER

This chapter describes the modified design of the preamplifier and also describes the latch-up problem of the preamplifier.

### Preamplifier

When both the FET's are conducting, the preamplifier works in the linear mode. But in any situation, if one of the FET's is turned off, as shown in Figure 20, the preamplifier latches up to saturation (15 volt).

$A_o$ is the ratio of the output to the input signal of the preamplifier and A is the open loop gain of the op-amp. When $|A_o| < |A|$, the feedback is termed negative, or degenerative. When $|A_o| > |A|$, the feedback is termed positive, or generative (Millman 1979).

The regenerative feedback can be easily verified. Let us redraw Figure 20 as shown in Figure 21. The drain voltage, $V_{D1}$, can be written in terms of $V_o$.

$$V_{D1} = V_o \left[\frac{R_5}{R_o + R_o}\right]$$

The feedback factor can be expressed as

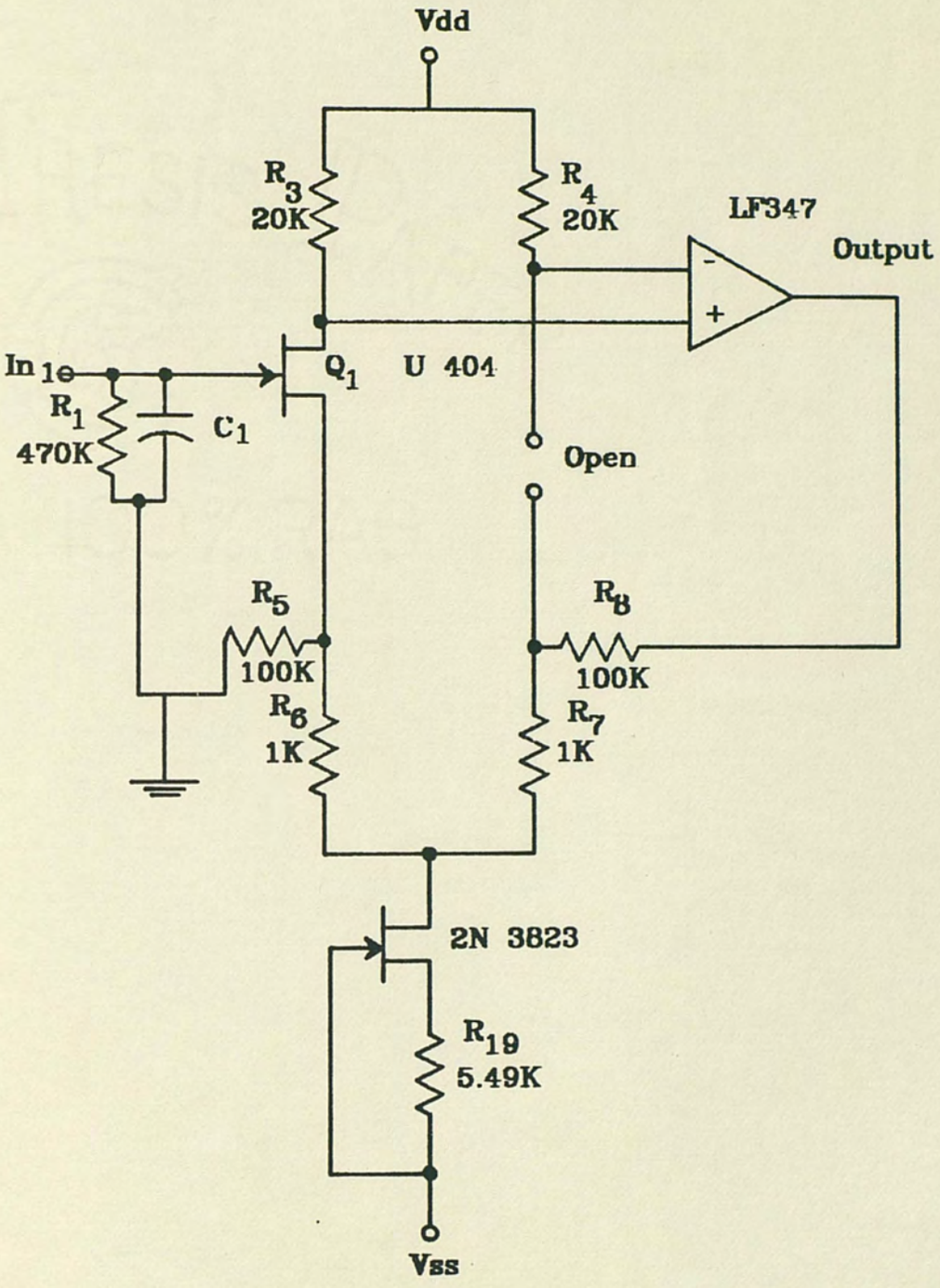



Fig. 20. Preamplifier with one FET off.

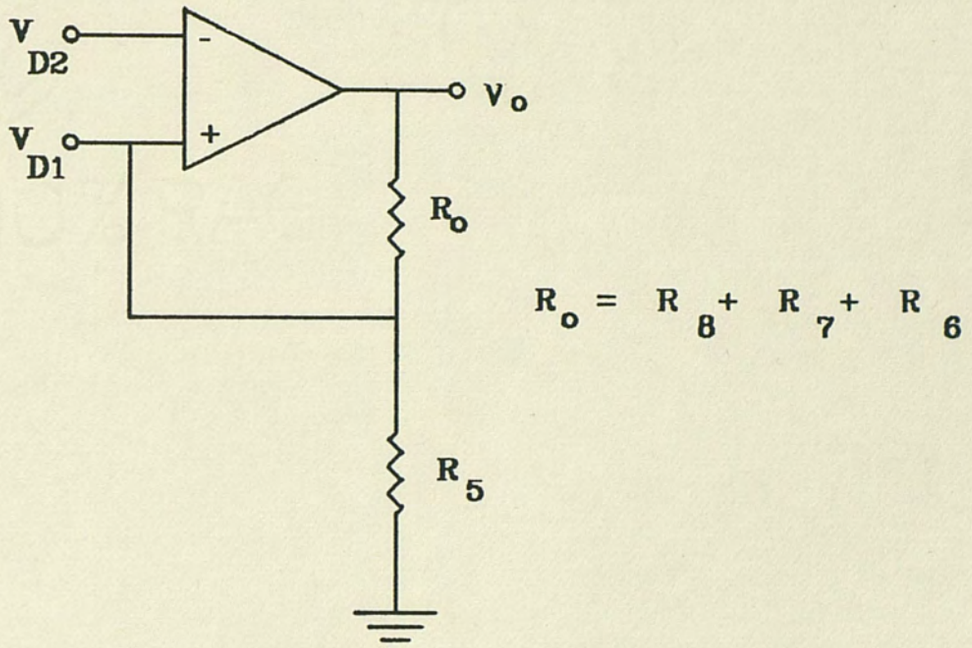



Fig. 21. Inverting Schmitt trigger.

$$\beta = \frac{R_5}{R_o + R_5}$$

The loop gain = - $\beta A$.

If the output increases by $\Delta V_o$, the $\beta \Delta V_o$ is fed back to $V_{D1}$, the non-inverting input terminal. Hence, $V_o$ will increase further by $\beta A \Delta V_o$, indicating positive feedback. Once the output reaches saturation, a problem occurs as the system cannot reset itself to normal operating conditions. It behaves like a Schmitt trigger. As soon as $V_{D1}$ is equal or less than $V_{D2}$, no regeneration will occur.

The preamplifier was redesigned as shown in Figure 22. The positive path was completely isolated and a constant voltage, 7.5 volt, was provided to the non-inverting terminal using a voltage divider. Now, the non-inverting terminal will never exceed more than 7.5 volts. If $Q_2$ is turned off, the circuit will appear as shown in Figure 23. The open loop gain has dropped by 6 dB.

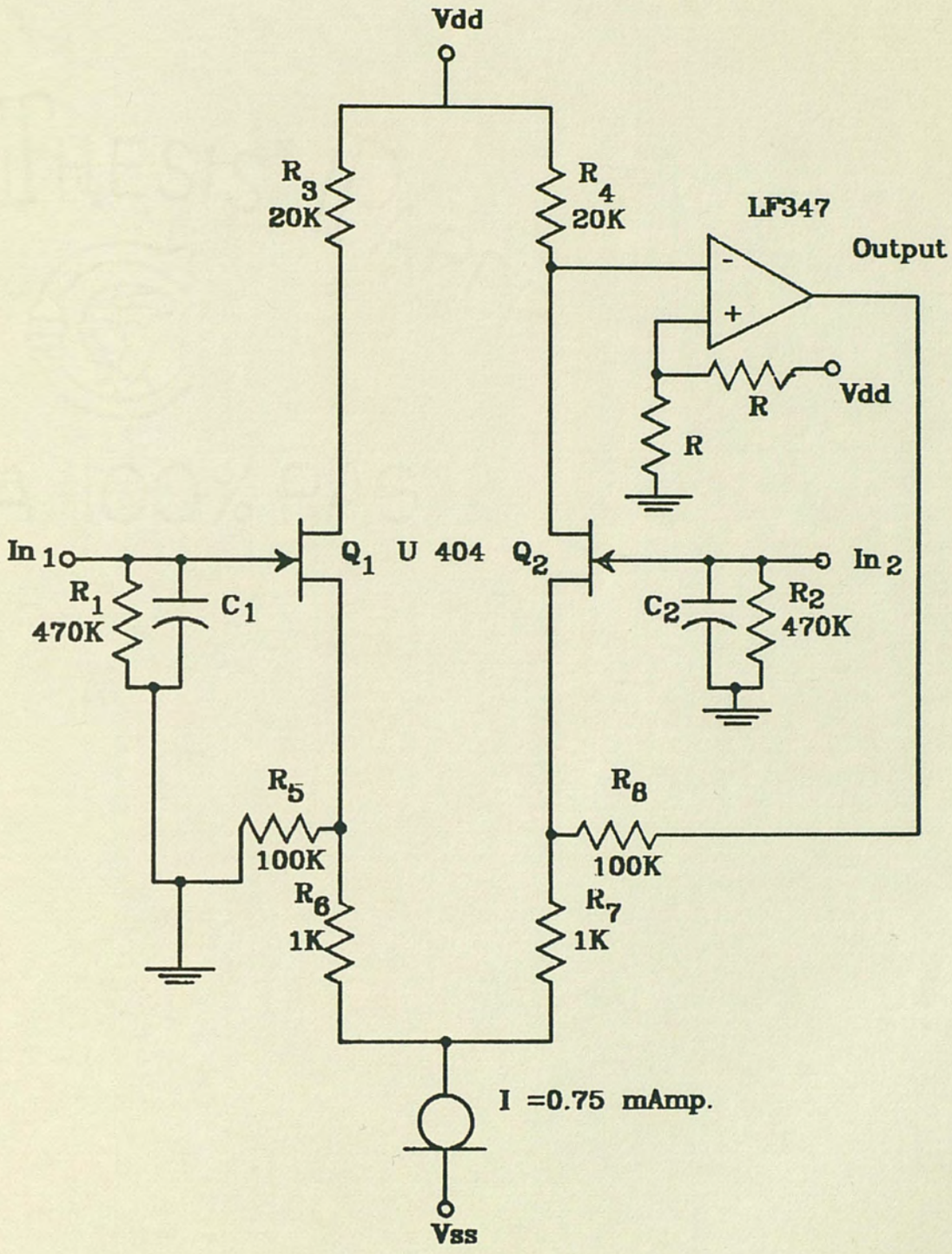



Fig. 22. Modified Preamplifier

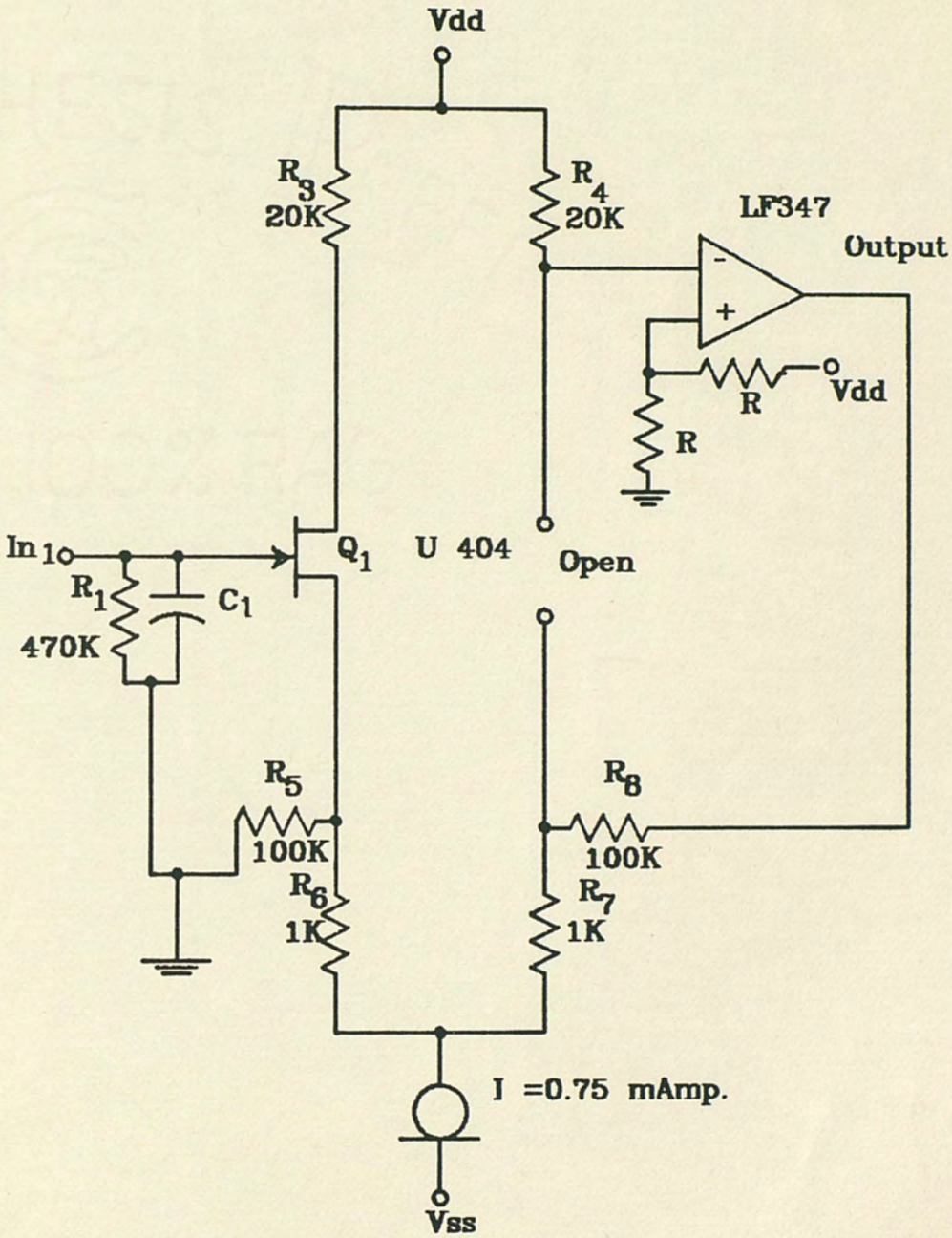



Fig. 23. Modified preamplifier with FET off.

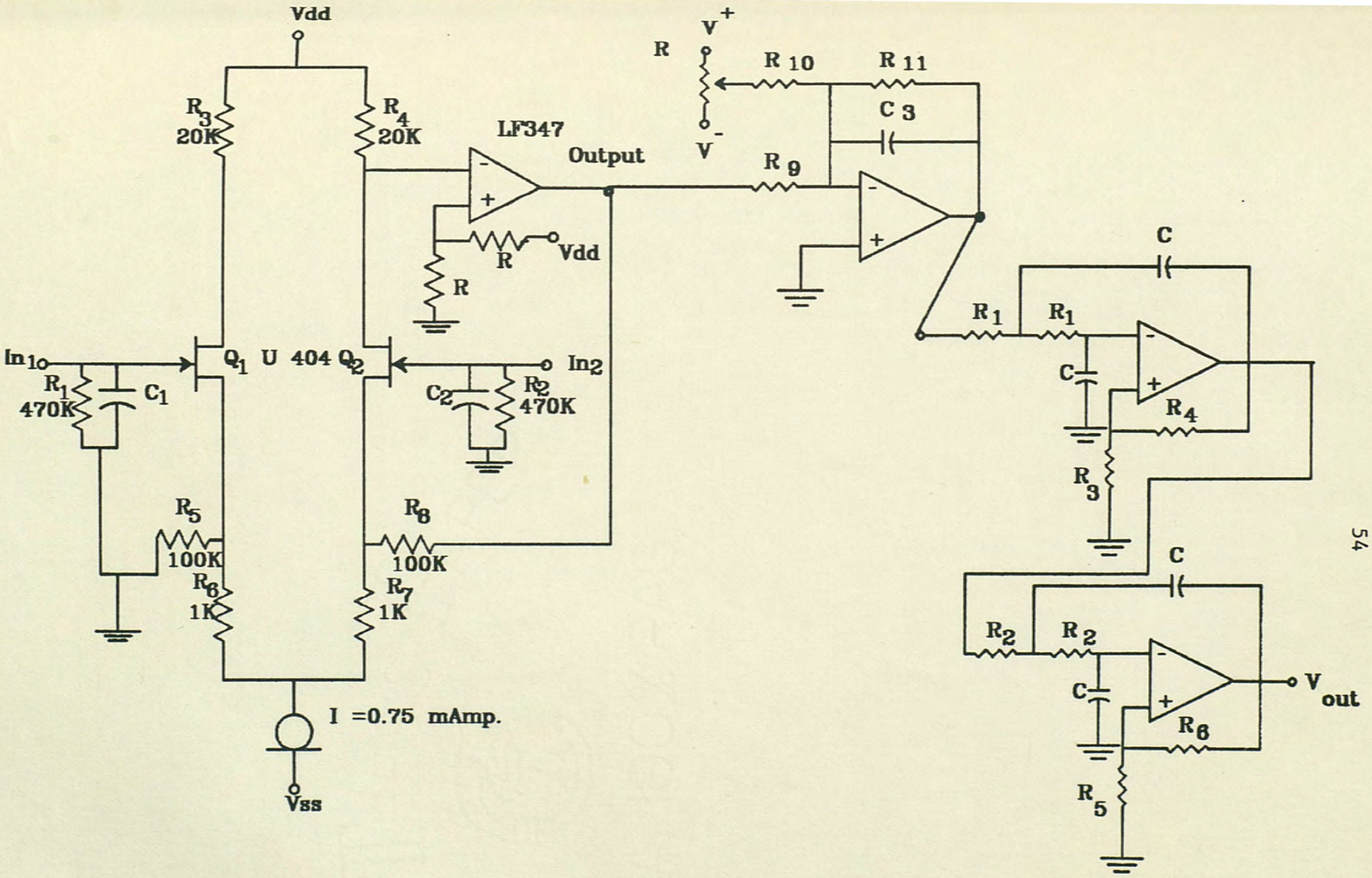



Fig. 24. Complete schematic.

# CHAPTER V

# CONCLUSION

The electro-oculometer was analyzed. The theoretical values were compared with the experimental values. Both AC and DC analyses were conducted. The calculated CMRR of the preamplifier is 73.978 dB, whereas the measured CMRR is 56.5 dB. The measured CMRR is almost 17 dB lower than the calculated CMRR because of its higher measured common mode gain, which is 0.15. This higher common mode gain results from the mismatch of the resistor values. A high frequency model of the FET was inserted in the preamplifier to verify the response. The CMRR of the preamplifier degraded by 10.308 dB while using the high frequency model of the FET. The fifth order Parabolic filter was designed and implemented into the electro-oculometer. The overshoot of the filter was 2 percent, which is much better than the 12 percent overshoot of the Butterworth filter. The rise time of the filter was 0.425 millisec. This rise time is quite reasonable for this kind of application because the maximum frequency of the eye movement is only 15 hertz. The new preamplifier was designed to prevent latch-up. The open loop gain of the new preamplifier dropped down to one-half of that of the previous amplifier.

# APPENDICES

# APPENDIX A

# ELECTRODE SPECIFICATION

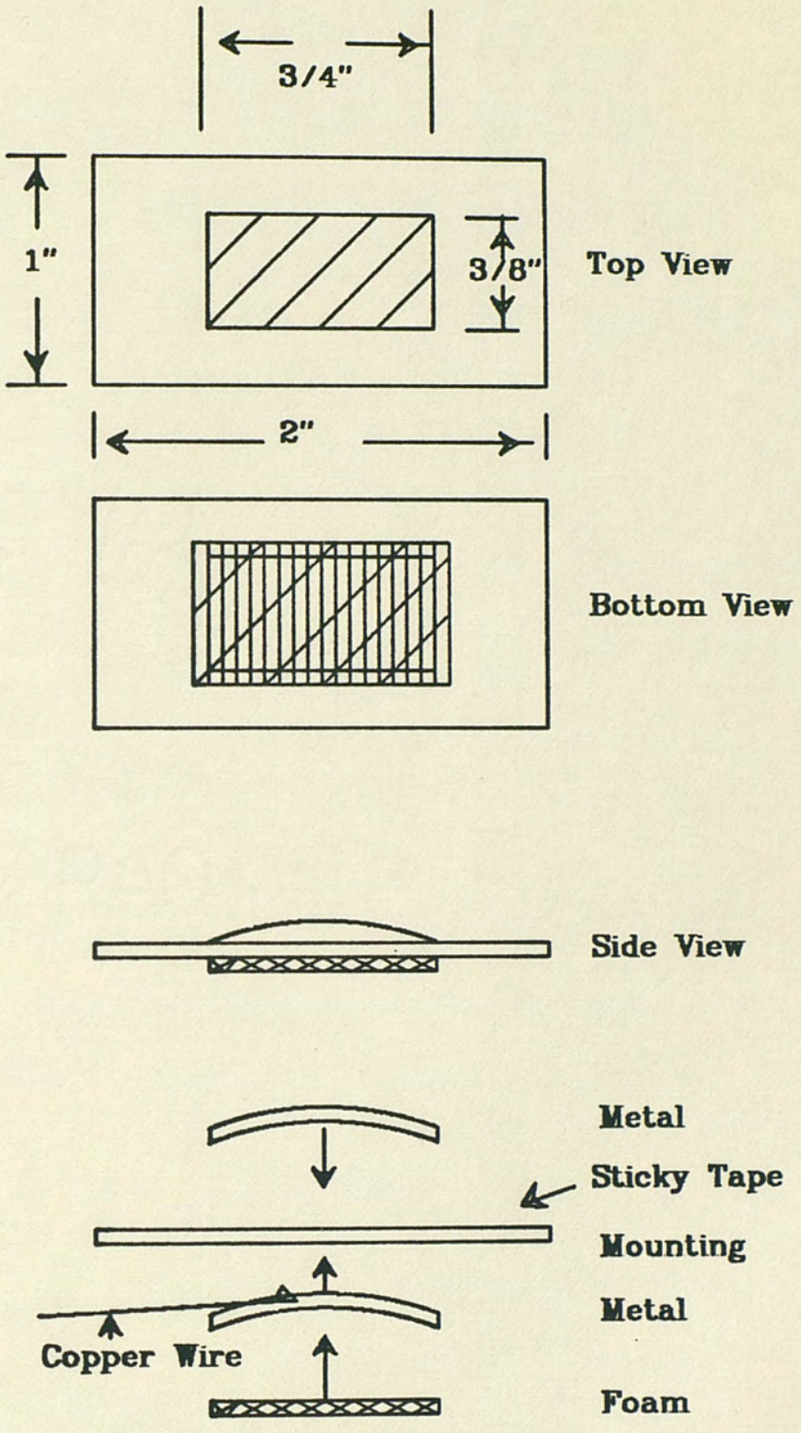



Fig. 25. Electrode specification.

## Electrodes

Several types of electrodes were tested for the best performance. Some of them have better sensitivity than others. For example, NTRON 140 E is more sensitive than NTRON 144 E. Most electrodes have snaps which frequently cause discomfort to the user. Finding the right kind and shape of electrode is important. The electrode shown in Figure 25 is specified on the basis of shape rather than on its chemical properties.

This shape was chosen on the basis of the comfort and ease of wearing for the user. It is a two inch long and one inch wide electrode. The electrode is attached with a six inch long, 26-gauge standard copper wire with PVC insulation. The metal piece is expected to possess the same chemical properties as NTRON 140 E. The detailed material information was not available.

# APPENDIX B

## DATA SHEETS AND COMPUTER PROGRAM

The information for FET 2N 3823 is given below.

# n-channel JFET
## *designed for . . .*

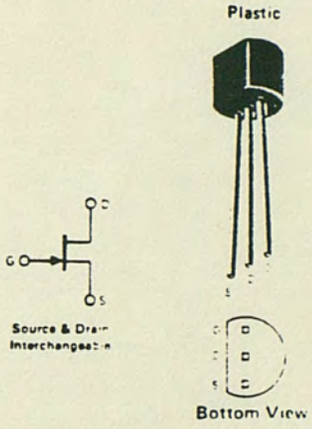
Siliconix

**Performance Curves NH**
**See Section 4**

- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

BENEFITS
- Low Cost
- Automatic Insertion Package

TO-92
See Section 6




### ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 25 V
Source-Gate Voltage . . . . . 25 V
Drain-Source Voltage . . . . . 25 V
Forward Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . −55 to 135°C
Storage Temperature Range . . . . . −55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

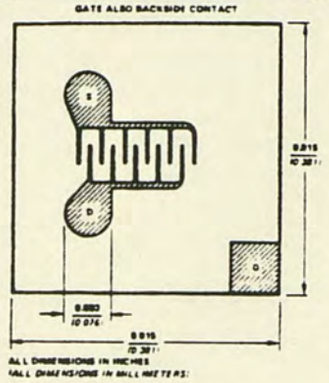
### ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

| | | Characteristic | | Min | Max | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|---|
| 1 | STATIC | $I_{GSS}$ | Gate Reverse Current | | −2.0 | nA | $V_{GS}$ = −15 V, $V_{DS}$ = 0 | |
| 2 | | | | | −2.0 | μA | | $T_A$ = +100°C |
| 3 | | $BV_{GSS}$ | Gate-Source Breakdown Voltage | −25 | | V | $I_G$ = −10 μA, $V_{DS}$ = 0 | |
| 4 | | $V_{GS(off)}$ | Gate-Source Cutoff Voltage | | −8.0 | | $V_{DS}$ = 15 V, $I_D$ = 2 nA | |
| 5 | | $I_{DSS}$ | Saturation Drain Current | 2.0 | 20 | mA | $V_{DS}$ = 15 V, $V_{GS}$ = 0 (Note 1) | |
| 6 | | $V_{GS}$ | Gate-Source Voltage | −0.5 | −7.5 | V | $V_{DS}$ = 15 V, $I_D$ = 200 μA | |
| 7 | DYNAMIC | $g_{fs}$ | Common-Source Forward Transconductance | 2000 | 7500 | μmhos | $V_{DS}$ = 15 V, $V_{GS}$ = 0 | f = 1 kHz |
| 8 | | $Re(y_{fs})$ | Common-Source Forward Transconductance | 1600 | | | | f = 100 MHz |
| 9 | | $Re(y_{os})$ | Common-Source Output Conductance | | 200 | | | |
| 10 | | $Re(y_{is})$ | Common-Source Input Conductance | | 800 | | | |
| 11 | | $C_{iss}$ | Common-Source Input Capacitance | | 7.0 | pF | | f = 1 MHz |
| 12 | | $C_{rss}$ | Common-Source Reverse Transfer Capacitance | | 3.0 | | | |

**NOTE:**
1. Pulse test PW = 300 μs; duty cycle ≤ 3%.

NH

# FET 2N 3823




## n-channel JFET
***designed for . . .***

- VHF/UHF Amplifiers
- Oscillators
- Mixers
- Low Input Capacitance High Speed Switch

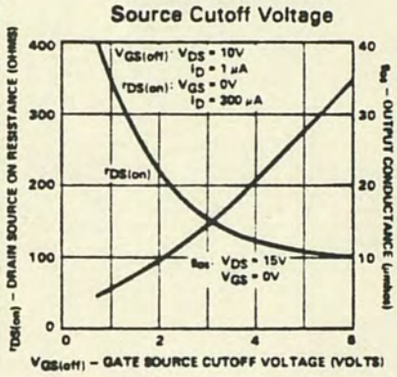
**BENEFITS:**

- Low Noise
  NF = 3 dB Typical @ 400 MHz
- Wideband
  High $g_{fs}/C_{iss}$ Ratio

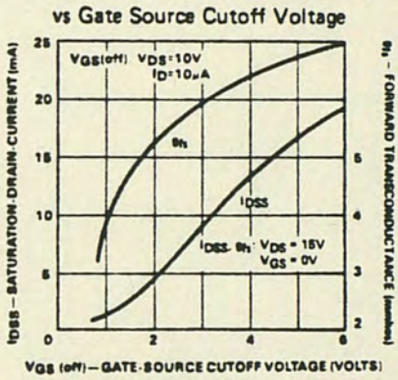
| TYPE | PACKAGE | PRINCIPAL DEVICES |
|---|---|---|
| Single | TO-72 | 2N3966, 2N4416-16A 2N3819 |
| Single | TO-92 | 2N5484-6, 2N5555, 2N5668-70, MPF102, MPF108, MPF112, PN4416, J304-5, |
| Single | Chip | All of the above devices |

## PERFORMANCE CURVES (25°C unless otherwise noted)

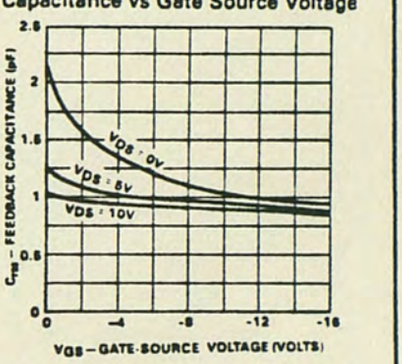
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



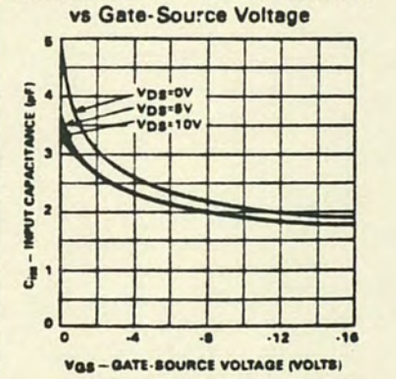

Drain Current & Transconductance vs Gate Source Cutoff Voltage



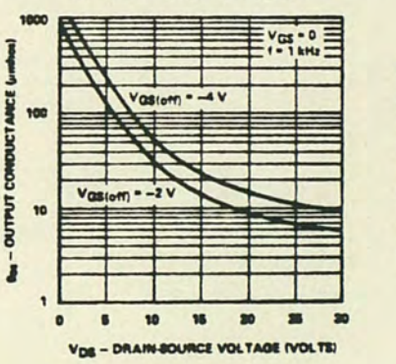

Common Source Reverse Feedback Capacitance vs Gate Source Voltage



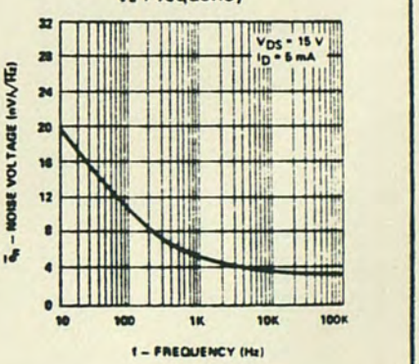

Common Source Input Capacitance vs Gate-Source Voltage



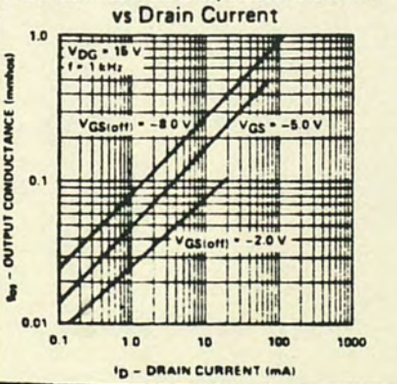

Common-Source Output Conductance vs Drain-Source Voltage



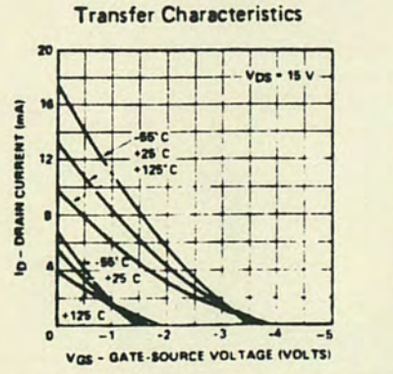

Equivalent Input Noise Voltage vs Frequency



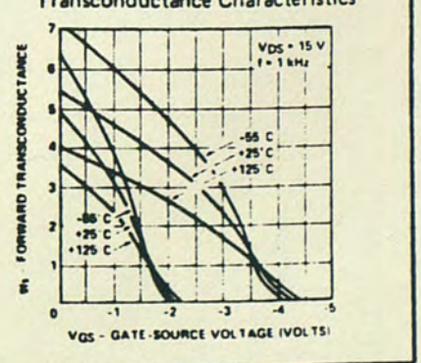

Common-Source Output Conductance vs Drain Current




Transfer Characteristics



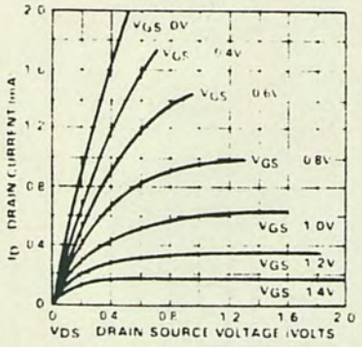

Transconductance Characteristics



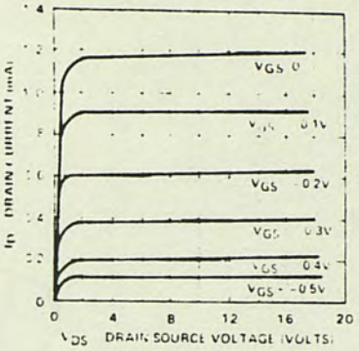
# FET 2N 3823

## PERFORMANCE CURVES (Cont'd) (25° C unless otherwise noted)

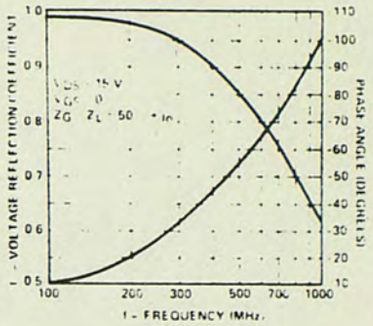
Output Characteristic
($V_{GS(off)}$ = -2V)



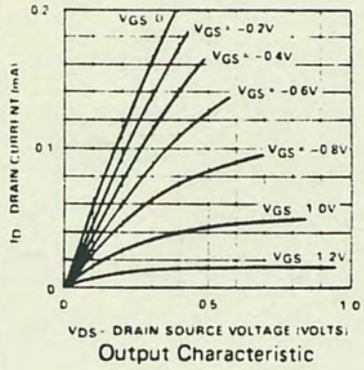

Output Characteristic
($V_{GS(off)}$ = -1.0V)



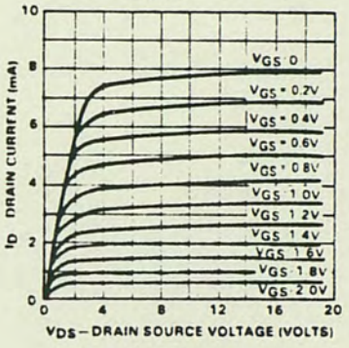

S Parameters $S_{11}$ Common-Source
vs Frequency



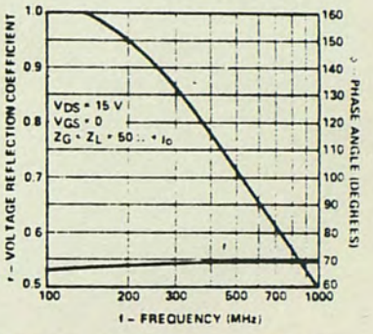

Output Characteristic
($V_{GS(off)}$ = -1.5V)



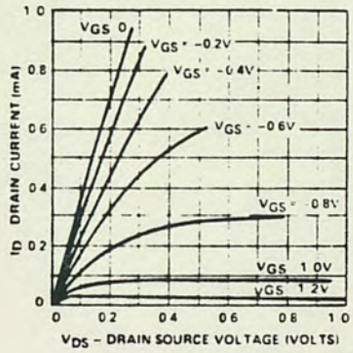

Output Characteristic
($V_{GS(off)}$ = -3.0V)



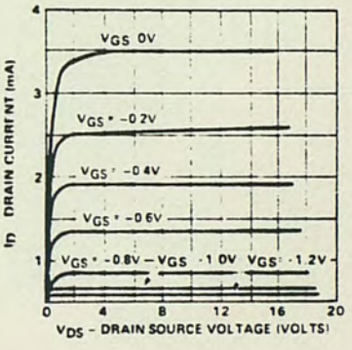

S Parameters $S_{21}$ Common-Source
vs Frequency



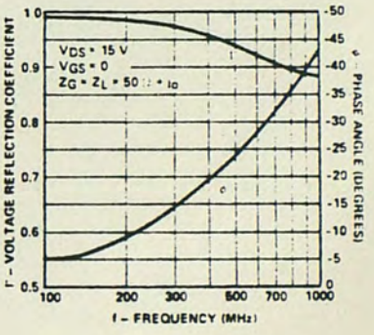

Output Characteristic
($V_{GS(off)}$ = -1.5V)



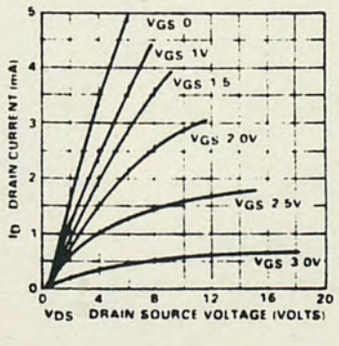

Output Characteristic
($V_{GS(off)}$ = -1.5V)



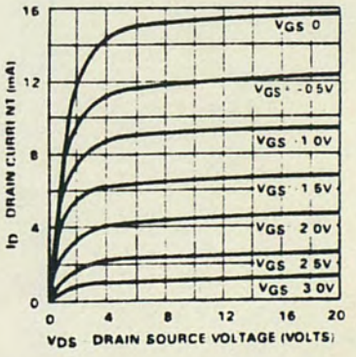

S Parameters $S_{22}$ Common-Source
vs Frequency




Output Characteristic
($V_{GS(off)}$ = -4.0V)

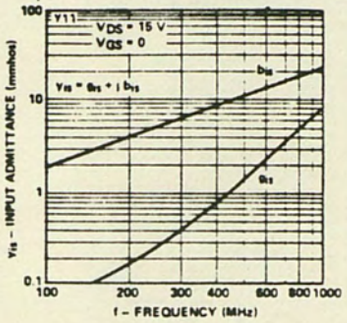



Output Characteristic
($V_{GS(off)}$ = -4.0V)

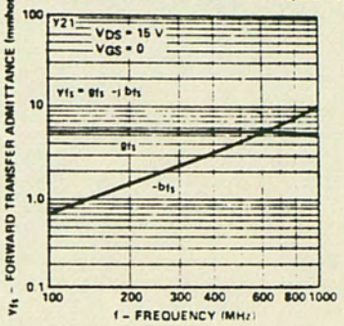


## PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

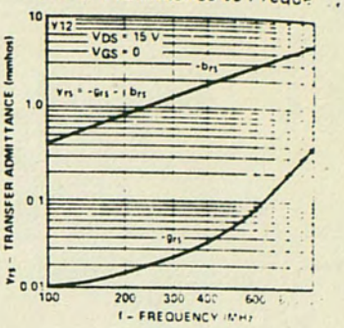
Common-Source Input Admittance vs Frequency



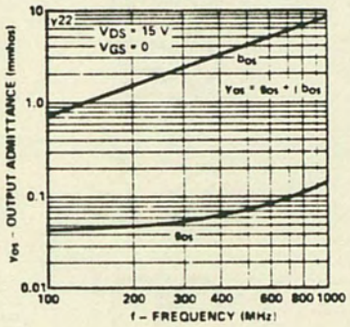

Common-Source Forward Transfer Admittance vs Frequency




Common-Source Reverse Transfer Admittance vs Frequency




Common-Source Output Admittance vs Frequency



The information for NJFET U 404 is given below.

# monolithic dual n-channel JFETs *designed for . . .*

- **Low Noise FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

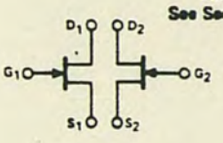
Siliconix

**Performance Curves NNR**
**See Section 4**

BENEFITS

- Minimum System Error and Calibration
  5 mV Offset Maximum (U401)
  95 dB Minimum CMRR (U401-04)
- Low Drift with Temperature
  10 μV/°C Maximum (U401, 02)
- Operates from Low Power Supply Voltages
  $V_{GS(off)} < 2.5$ V
- Simplifies Amplifier Design
  Output Conductance < 2 μmho
- Low Noise
  $\overline{e}_n = 6\ nV/\sqrt{Hz}$ at 10 Hz Typical

TO-71
See Section 6





Bottom View


ABSOLUTE MAXIMUM RATINGS (25°C)

| | |
|---|---|
| Gate-Drain or Gate-Source Voltage | 50 V |
| Forward Gate Current | 10 mA |
| Device Dissipation (each side) @ $T_A$ = 85°C derate 2.6 mW/°C | 300 mW |
| Total Device Dissipation @ $T_A$ = 85°C (derate 5 mW/°C) | 500 mW |
| Storage Temperature Range | −65 to 200°C |

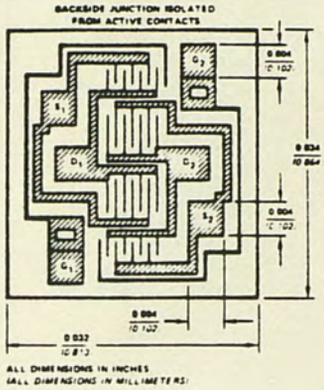
ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

| | | Characteristic | U401 Min | U401 Max | U402 Min | U402 Max | U403 Min | U403 Max | U404 Min | U404 Max | U405 Min | U405 Max | U406 Min | U406 Max | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | STATIC | $BV_{GSS}$ Gate-Source Breakdown Voltage | -50 | | -50 | | -50 | | -50 | | -50 | | -50 | | V | $V_{DS}$ = 0, $I_G$ = -1 μA | |
| 2 | | $I_{GSS}$ Gate Reverse Current (Note 1) | | -25 | | -25 | | -25 | | -25 | | -25 | | -25 | pA | $V_{DS}$ = 0, $V_{GS}$ = -30 V | |
| 3 | | $V_{GS(off)}$ Gate-Source Cutoff Voltage | -.5 | -2.5 | -.5 | -2.5 | -.5 | -2.5 | -.5 | -2.5 | -.5 | -2.5 | -.5 | -2.5 | V | $V_{DS}$ = 15 V, $I_D$ = 1 nA | |
| 4 | | $V_{GS(on)}$ Gate-Source Voltage (on) | | -2.3 | | -2.3 | | -2.3 | | -2.3 | | -2.3 | | -2.3 | | $V_{DG}$ = 15 V, $I_D$ = 200 μA | |
| 5 | | $I_{DSS}$ Saturation Drain Current (Note 2) | 0.5 | 10.0 | 0.5 | 10.0 | 0.5 | 10.0 | 0.5 | 10.0 | 0.5 | 10.0 | 0.5 | 10.0 | mA | $V_{DS}$ = 10 V, $V_{GS}$ = 0 | |
| 6 | | $I_G$ Gate Current (Note 1) | | -15 | | -15 | | -15 | | -15 | | -15 | | -15 | pA | $V_{DG}$ = 15 V, | |
| 7 | | | | -10 | | -10 | | -10 | | -10 | | -10 | | -10 | nA | $I_D$ = 200 μA | $T_A$ = 125°C |
| 8 | | $BV_{G1-G2}$ Gate-Gate Breakdown Voltage | ±50 | | ±50 | | ±50 | | ±50 | | ±50 | | ±50 | | V | $V_{DS}$ = 0, $V_{GS}$ = 0, $I_G$ = ±1 μA | |
| 9 | DYNAMIC | $g_{fs}$ Common-Source Forward Transconductance (Note 2) | 2000 | 7000 | 2000 | 7000 | 2000 | 7000 | 2000 | 7000 | 2000 | 7000 | 2000 | 7000 | μmho | $V_{DS}$ = 10 V, $V_{GS}$ = 0 | f = 1 kHz |
| 10 | | $g_{os}$ Common-Source Output Conductance | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | | | |
| 11 | | $g_{fs}$ Common-Source Forward Transconductance | 1000 | 2000 | 1000 | 2000 | 1000 | 2000 | 1000 | 2000 | 1000 | 2000 | 1000 | 2000 | | $V_{DG}$ = 15 V, $I_D$ = 200 μA | f = 1 kHz |
| 12 | | $g_{os}$ Common-Source Output Conductance | | 2.0 | | 2.0 | | 2.0 | | 2.0 | | 2.0 | | 2.0 | | | |
| 13 | | $C_{iss}$ Common-Source Input Capacitance | | 8.0 | | 8.0 | | 8.0 | | 8.0 | | 8.0 | | 8.0 | pF | | f = 1 MHz |
| 14 | | $C_{rss}$ Common-Source Reverse Transfer Capacitance | | 3.0 | | 3.0 | | 3.0 | | 3.0 | | 3.0 | | 3.0 | | | |
| 15 | | $\overline{e}_N$ Equivalent Short Circuit Input Noise Voltage | | 20 | | 20 | | 20 | | 20 | | 20 | | 20 | $\frac{nV}{\sqrt{Hz}}$ | $V_{DS}$ = 15 V, $V_{GS}$ = 0 | f = 10 Hz |
| 16 | MATCHING | CMRR Common Mode Rejection Ratio (Note 3) | 95 | | 95 | | 95 | | 95 | | 90 | | | | dB | $V_{DG}$ = 10 to 20 V, $I_D$ = 200 μA | |
| 17 | | $\lvert V_{GS1} - V_{GS2} \rvert$ Differential Gate Source Voltage | | 5 | | 10 | | 10 | | 15 | | 20 | | 40 | mV | $V_{DG}$ = 10 V, $I_D$ = 200 μA | |
| 18 | | $\frac{\Delta\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$ Gate Source Voltage Differential Drift (Note 4) | | 10 | | 10 | | 25 | | 25 | | 40 | | 80 | μV/°C | $V_{DG}$ = 10 V, $I_D$ = 200 μA | $T_A$ = -55°C, $T_B$ = +25°C, $T_C$ = +125°C |

NOTES
1. Approximately doubles for every 10°C increase in $T_A$. 2. Pulse test duration = 300 μs, duty cycle ≤ 3%. 3. CMRR = $20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta V_{GS1} - V_{GS2}}\right]$, $\Delta V_{DD}$ = 10 V. 4. Measured at end points $T_A$, $T_B$ and $T_C$.

NNR

NJFET U 404




# monolithic dual n-channel JFET *designed for . . .*

Siliconix

- FET Input Amplifiers
- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Comparators

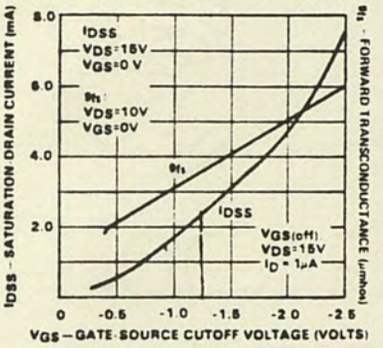
**BENEFITS:**

- Minimum System Error and Calibration
  5 mV Offset Maximum (J401)
  95 dB Minimum CMRR
- Low Drift With Temperature
  10 μV/°C (J401)
- Simplifies Amplifier Design
  Output Conductance < 2 μmho
- Low Noise
  $\bar{e}_n$ = 6 nV/√Hz at 10 Hz Typical

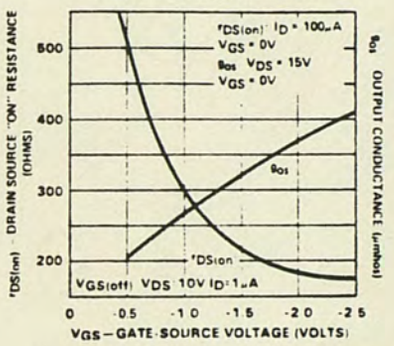
| TYPE | PACKAGE |
|---|---|
| Dual | TO-71 |
| Dual | Chip |

**PRINCIPAL DEVICES**
2N3921-2, 2N4084-5, 2N5045-7, 2N5516-24 U401-6 2N4085CHP, 2N5046CHP-47CHP, U403CHP-06CHP

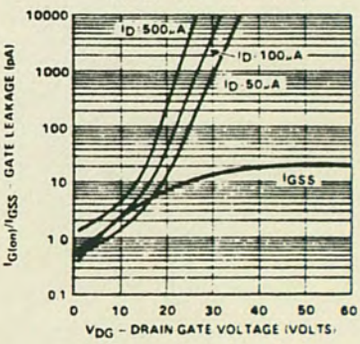
Drain Current & Transconductance vs Gate Source Voltage



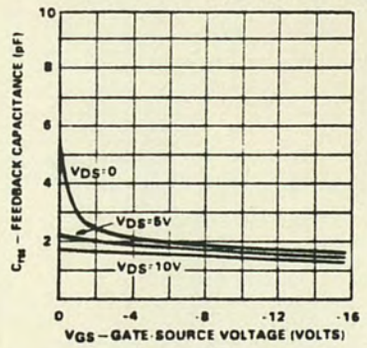

On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



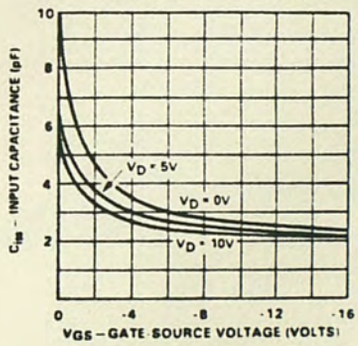

Gate Operating Current vs Drain Gate Voltage



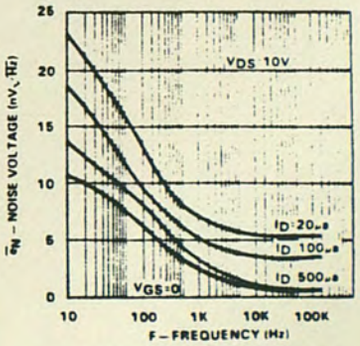

Common Source Reverse Feedback Capacitance vs Gate Source Voltage



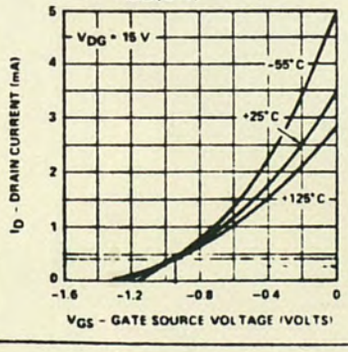

Common-Source Input Capacitance vs Gate-Source Voltage



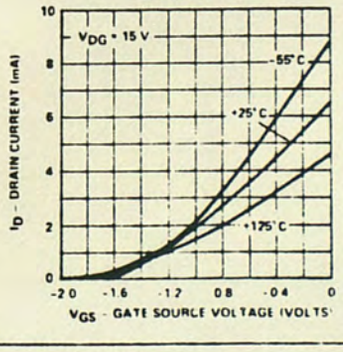

Noise Voltage vs Frequency



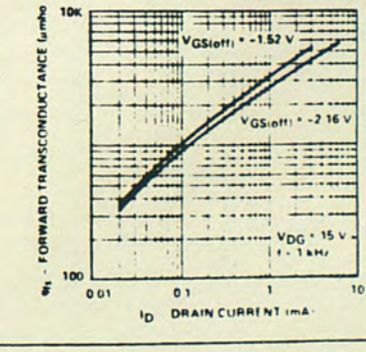

Transfer Characteristics Low $V_{GS(off)}$ Unit (−1.5 V)




Transfer Characteristics Medium $V_{GS(off)}$ Unit (−2.2 V)



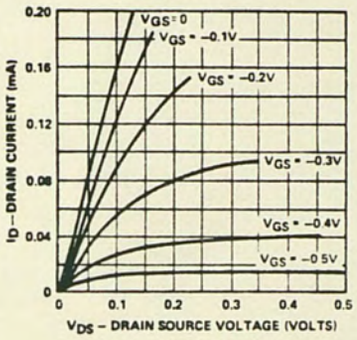

Forward Transconductance vs Drain Current



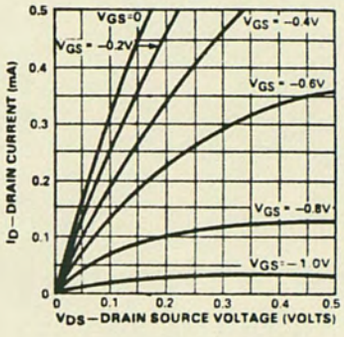
# NJFET U 404

## PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

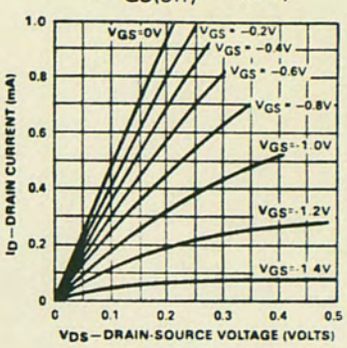
Output Characteristic
($V_{GS(off)}$ = −0.6V)



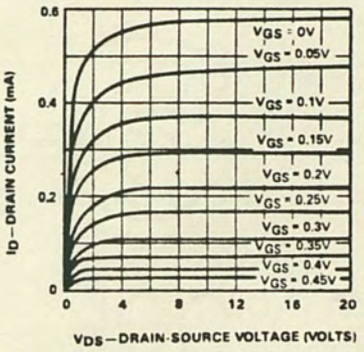

Output Characteristic
($V_{GS(off)}$ = −1.2V)



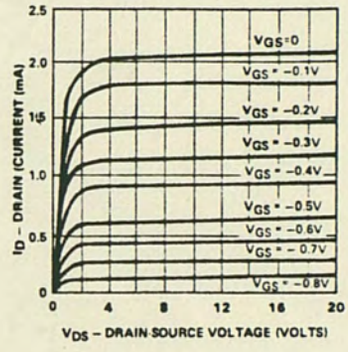

Output Characteristic
($V_{GS(off)}$ = −1.7V)



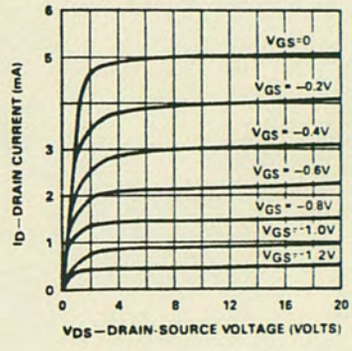

Output Characteristic
($V_{GS(off)}$ = −0.6V)



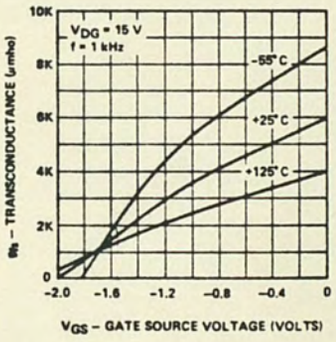

Output Characteristic
($V_{GS(off)}$ = −1.2V)



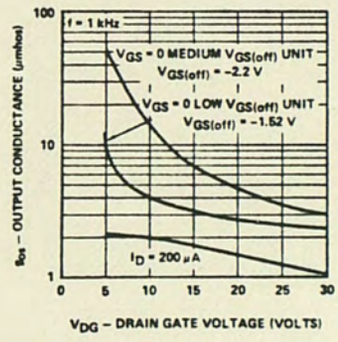

Output Characteristic
($V_{GS(off)}$ = −1.7V)




Transconductance vs Gate Source Voltage
Medium $V_{GS(off)}$ Unit (−2.0V)




Output Conductance
vs Drain Gate Voltage

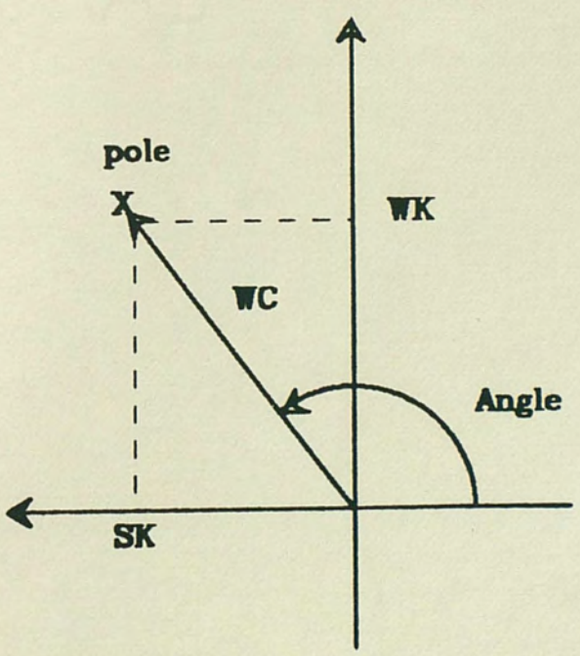


The computer program for the pole location of the parabolic filter is given below.

```
]LIST

 5  PRINT  CHR$ (4);"BRUN PRINT USING"
 10 PI = 4 *  ATN (1):DR = PI / 180:RD = 180 / PI
 15  DIM S(99),W(99)
 20  HOME : PRINT "PARABOLIC FILTER POLE FINDER": PRINT : INPUT "DEGREE O
     F FILTER: ";N: IF N < 1 THEN  GOTO 20
 25  PRINT : PRINT " POLE  ANGLE    WC         SK         WK"
 30  FOR K = 0 TO N - 1
 40 AN = 90 + (K + 1 / 2) * 180 / N
 50  &  PRINT " ## ",K + 1;: &  PRINT "   ### ",AN;
 60 AN = AN * DR
 70 SK = (9 -  SQR (81 + 36 *  TAN (AN) *  TAN (AN))) / (2 *  TAN (AN) *
      TAN (AN))
 90 WK = SK *  TAN (AN)
 95 S(K) = SK:W(K) = WK
 100 WC =  SQR (SK * SK + WK * WK)
 110  IF K = (N - 1) / 2 THEN WC = 1
 120  &  PRINT "    #.###",WC;: &  PRINT "    #.###",SK;: &  PRINT "    #
     .###",WK
 122  NEXT K: PRINT
 123  PRINT "   QUADRATIC TERMS"
 124  FOR K = 0 TO (N - 1) / 2
 125  IF K = (N - 1) / 2 THEN  PRINT "           S + 1": GOTO 160
 130  PRINT "S©2 + ";
 140  &  PRINT "#.###", - 2 * S(K);: PRINT "S + ";
 150  &  PRINT "#.###",S(K) * S(K) + W(K) * W(K)
 160  NEXT K
 170  PRINT : INPUT "ANOTHER FILTER? (Y,N) ";A$: IF  LEFT$ (A$,1) <  > "N
     " THEN  GOTO 20
 180  END
```

The output of the program and the variables are shown below.

```
]RUN
PARABOLIC FILTER POLE FINDER

DEGREE OF FILTER: 5

 POLE   ANGLE     WC          SK          WK
   1      108      1.972     %-0.609      1.875
   2      144      1.171     %-0.947      0.688
   3      180      1.000      0.000     0.000
   4      216      1.171     %-0.947     %-0.688
   5      252      1.972     %-0.609     %-1.875

    QUADRATIC TERMS
S©2 + 1.219S + 3.888
S©2 + 1.895S + 1.371
           S + 1

ANOTHER FILTER? (Y,N) N

]
```



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