STARS

Retrospective Theses and Dissertations

1986

Switched-Capacitor Programmable Sallen and Key Low Pass Filters

Karl P. Eriksson
University of Central Florida

STARS Citation

Showcase of Text, Archives, Research & Scholarship

SWITCHED-CAPACITOR PROGRAMMABLE
SALLEN AND KEY LOWPASS FILTERS

BY

KARL PAUL ERIKSSON
B.S.E., University of Central Florida, 1973
M.S.M., Rollins College, 1981

THESIS

Submitted in partial fulfillment of the requirements
for the degree of Master of Science
in the Graduate Studies Program of the College of Engineering
University of Central Florida
Orlando, Florida

Fall Term
1986

ABSTRACT

This thesis deals with a different approach to
switched-capacitor filters than previously seen by the use of a
Sallen and Key topology. It is shown that a Sallen and Key
second-order topology approach to a switched-capacitor filter gives
reasonable filter performance results, contrary to what the
literature leads one to expect. It is also shown that the Sallen
and Key second-order topology with modification to a third-order
section with buffers results in a high performance switched-
capacitor filter with fewer components than previous
switched-capacitor filters. This results in fewer monolithic chip
size requirements, reduced power requirements, and less cost.
Higher order filters could be obtained by cascading either one of
the second- or third-order switched-capacitor sections together.
Desired filter Q values and cutoff frequencies are shown to be
obtained by changing the capacitor ratios and clock frequencies,
respectively.

TABLE OF CONTENTS

LIST OF FIGURES

CHAPTER 1

DEVELOPMENT OF SWITCHED-CAPACITOR FILTERS

Digital filters have often been the choice for adaptive or higher order filters, but they require a digital input signal and thus call for analog-to-digital converters on the front end. In addition, for analog output, a companion d-a converter must join the design. Furthermore, a digital filter often requires extensive software development. These requirements combine with the cost of the necessary digital signal processor to make a digital filter much too costly for many jobs.

On the other hand, analog filters offer a designer a vast array of filter implementations. Unfortunately, each type and, consequently, each new design, present an engineer with another design challenge. Since analog filters lack the flexibility of digital designs, they remain the domain of a specialist who, after considerable time, produces a filter that does the job.

The desire is to have a monolithic chip that would be frequency programmable in that the cutoff frequency of a lowpass filter could be clock tunable. This chip could then be used in many applications where a cutoff frequency selection is desired. Such applications as voice communications require a series of filters with different cutoff frequencies for frequency discrimination and selection. One

switched-capacitor monolithic chip could provide the same function as a series of filters now provides. This would significantly reduce the number of components and design time in such applications. The switched-capacitor monolithic chip is such a device, with programmability.

Analog filters that are frequency selective which can be completely integrated on a silicon chip have escaped the efforts of designers. Frequency selective filters on a monolithic chip are now possible due to several key developments.

Periodically operated switches were first put into use for linear periodically-switched circuits, in particular for the realization of precision modulators for carrier telephone systems. With the discovery of the resonant-transfer principle in the early 50s, it was shown that capacitances interchange charges periodically by being interconnected appropriately by means of resonant circuits (Caruthers 1939).

It was pointed out in 1968 in a publication by A. Fettweis that resonant frequencies depend only on capacitance ratios, not on individual capacitance values for resonant-transfer circuits (Fettweis 1968). Low cost high-performance monolithic op amps led to the use of active-RC filtering techniques to replace passive RLC filters in the late 1960s. RC-active filters have proven difficult to realize in completely monolithic form because precise RC products were difficult to achieve in standard monolithic processes.

Metal-oxide-semiconductor (MOS) integrated circuits offer the unique capability to store charge on a node over a period of many milliseconds and to sense the value of the charge continuously and non-destructively. The high impedance of the MOS transistor in the off state combined with essentially infinite impedance in the active mode of operation gives it this unique charge-storing ability. This feature of MOS circuits was first used in dynamic random-access memory devices. This allowed the elimination of active or pullup transistors which were required to refresh the information charge. The MOS storage feature has also been used for the bucket brigade shift register. A time-varying analog signal is converted to a series of charge packets, proportional to the value of the input signal at the sample instants. The charge packets are passed serially through MOS capacitors, the motion of the charge being brought about by the action of appropriately clocked MOS devices. The charge at each capacitor is sensed non-destructively by MOS transistors.

Further advances made the charge-coupled device (CCD) possible by which the storage capacitance was integrated with the MOS switch structure and MOS sensing device in such a way that transversal filters and other analog signal processing devices could be fabricated in a smaller silicon area and achieve higher performance.

Using CCD and bucket-brigade filters required peripheral circuitry that had to be realized off chip to convert the input signal into charge packets and to recover a low-impedance voltage signal at the output. Since the sampling rate in CCDs must be low, a complex

anti-aliasing filter is required to bandlimit the input signal to a frequency below the sampling rate. As a result, the filter size is great and requires a large silicon area, making it impractical for monolithic chips.

All these developments led to switched-capacitor filters which are characterized by the fact that they use a capacitor and MOS switches to simulate the circuit behavior of a resistor. One of the key features is that the switched-capacitor simulated resistor requires considerably less area on a silicon chip than an analog resistor. In addition, the silicon area decreases when the required resistance increases. As an example, a 10-Meg ohm equivalent resistance might be typically matched to a monolithic capacitor which is normally small, a 10-pF capacitor being typical. Simulating the 10-Meg ohm resistance can be accomplished with a 1-pF capacitor that is switched at a 100-KHz rate. The area required for the switched-capacitor is only 0.01 mm^2, on a chip that would typically be 10 to 20 mm^2. To do a 10 Meg ohm analog resistor using a polysilicon line or diffusion would require an area 100 times greater than the switched-capacitor resistor.

Many conventional RC-active filters can be made using switched-capacitor resistors to replace the conventional resistors. In that switched-capacitor filters are a sample-and-hold type system, the input signal must be bandlimited with an anti-aliasing filter. A key feature of switched-capacitor filters is that as the sampling rate is increased the sensitivities of the filter generally decrease,

approaching that of a continuous analog filter. Also, since the clock frequency can be much greater than the input signal frequencies, the anti-aliasing filter can be simplified considerably.

Another key feature of switched-capacitor filters is that the clock frequency can be used to determine the time constants of the filter. It was pointed out in 1968 that resonant frequencies depend only on capacitive ratios, not on individual capacitive values, for resonant-transfer circuits (Fettweis 1968). This applies to switched-capacitor circuits so that instead of attempting to synthesize close RC products for time constants, capacitor ratios which are easier to synthesize monolithically are used instead. These properties make the switched-capacitor filter much more practical for monolithic realizations than other filter technologies. MOS switched-capacitor filters with good filter properties have been built as early as 1977 (Hosticka et al. 1977).

CHAPTER 2

CHARACTERISTICS OF SWITCHED-CAPACITOR FILTERS

The switched-capacitor is approximately equal to a series resistor, as shown in Figure 2.1a. A switched-capacitor version of this resistor is shown in Figure 2.1b and a MOS switch version is shown in Figure 2.1c. Two MOS switches are connected in series and driven by two waveforms, ϕ_1, and ϕ_2. It is required that ϕ_1 and ϕ_2 have the same frequency and also that they be non-overlapping so that when ϕ_1 is on, ϕ_2 is off and vice versa, as shown in Figure 2.2. There is never a direct connection from the input port to the output port.

With a time varying input voltage, $v_1(t)$ on the input port, and when switch 1 (S_1) is closed and switch 2 (S_2) is open, the circuit of Figure 2.3a is in effect. When v_1 is constant, the voltage of the capacitor increases by the time constant $R_{on} C_R$, R_{on} being the ON resistance of the MOS switch and C_R being the value of the capacitor used in the simulation of the resistor. The voltage of the capacitor reaches 63 percent of its final value in $R_{on} C_R$ seconds.

When S_1 opens and S_2 closes, the circuit of Figure 2.3b is in effect and the capacitor discharges to the output port which then has a voltage v_2. The charge transferred in time T_c is
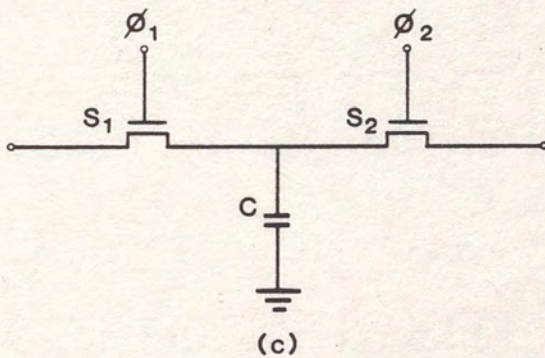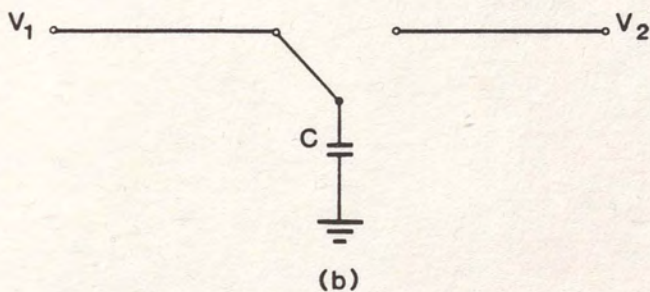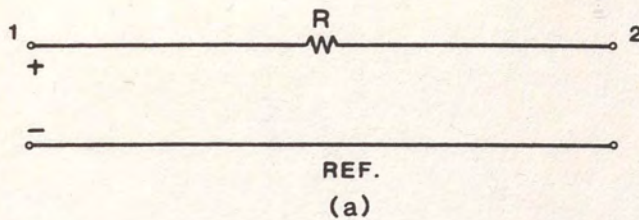
Figure 2.1.   Switched-capacitor resistor.
(a) Resistor to be simulated
(b) Switched-capacitor model of resistor
(c) MOS switch implementation of
switched-capacitor
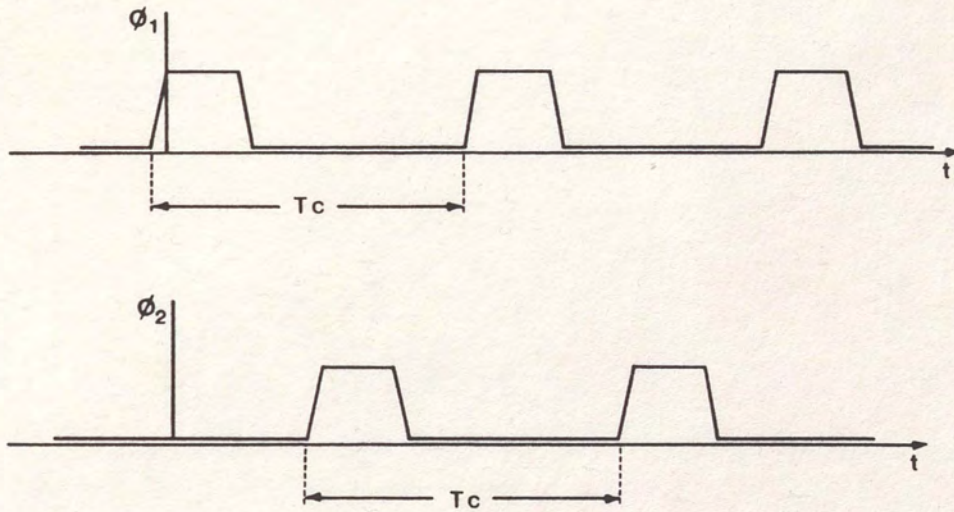
Figure 2.2. Clock waveforms ϕ_1 and ϕ_2 that drive MOS switches.
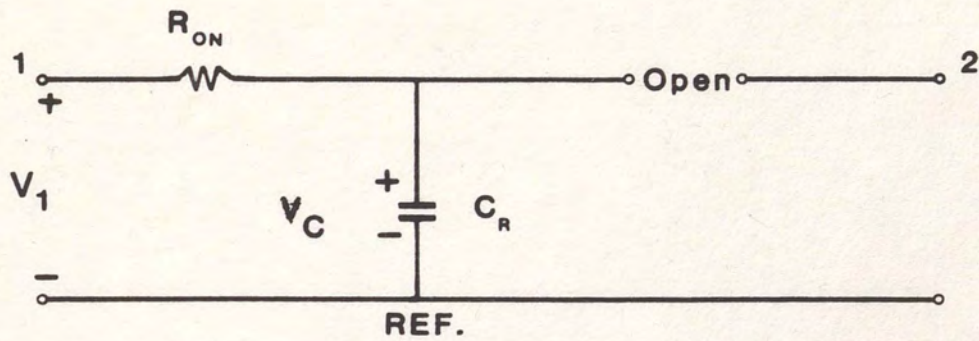
(a)
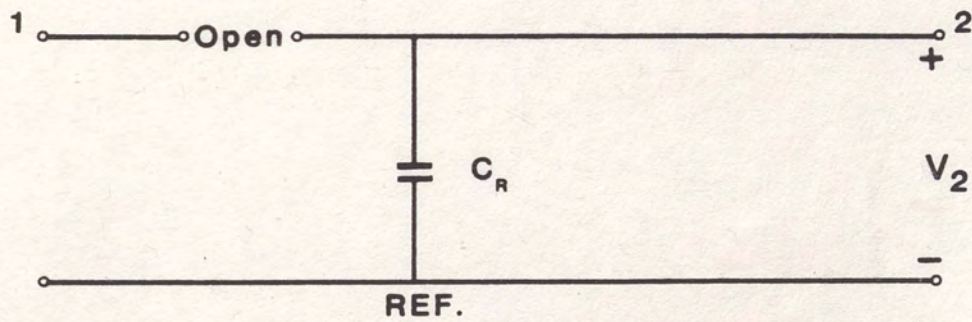
(b)

Figure 2.3. Switched-capacitor circuit operation.
(a) S_1 closed and S_2 open
(b) S_1 open and S_2 closed

$$q = C_R(v_1 - v_2) \tag{1}$$

The current on the average is

$$i(t) = \frac{\Delta q}{\Delta t} \approx \frac{C_R(v_1 - v_2)}{T_c} \tag{2}$$

This approximation holds when the clock frequency (f_c) is greater than the input signal frequency. The equivalent resistor value for this same current is

$$R = \frac{v_1 - v_2}{i} = \frac{T_c}{C_R} = \frac{1}{f_c C_R} \tag{3}$$

Next, consider comparing a conventional first-order RC-low pass filter, shown in Figure 2.4a with its switch-capacitor filter version, shown in Figure 2.4b. The 3-dB bandwidth of the conventional first-order RC filter is

$$\omega_{-3 \text{ dB}} = \frac{1}{R_1 C_2} \tag{4}$$

The 3-dB bandwidth of the switched-capacitor filter is found by substituting the effective resistance of the switched-capacitor C_R from equation (3) into equation (4) which gives

$$\omega_{-3 \text{ dB}} \approx f_c \frac{C_1}{C_2}, \text{ for } f_c > f_{input} \tag{5}$$
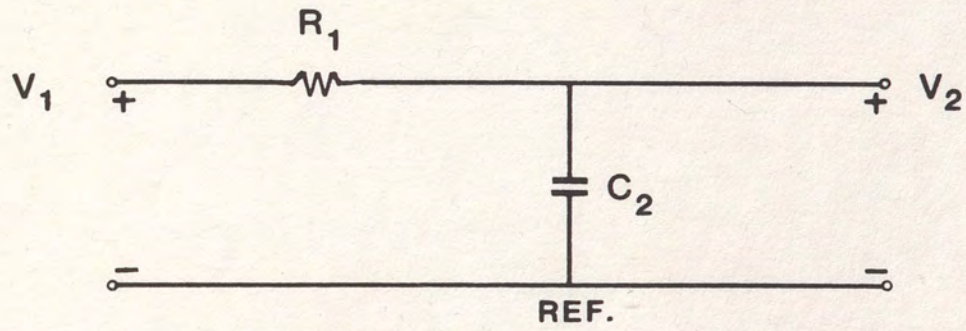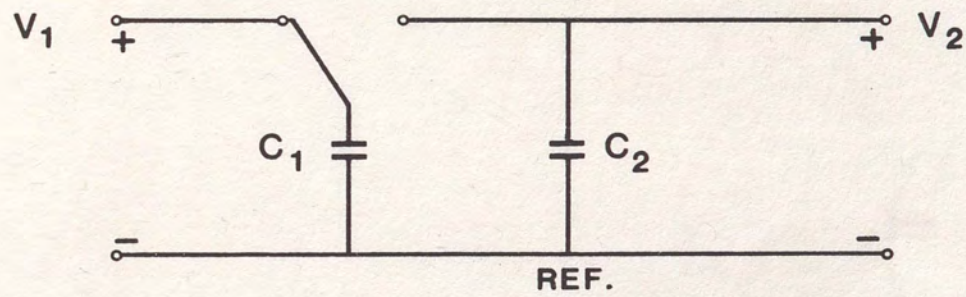
Figure 2.4. Switched-capacitor first-order lowpass filter.
(a) a single-pole RC continuous lowpass filter
(b) switched-capacitor version

This relation holds when the clock frequency is greater than the input frequency.

From equation (5), it can be seen that the bandwidth of the switched-capacitor filter is dependent upon the ratio of the capacitor values instead of an RC product. With monolithic chips, the ratio of capacitor values can be tightly controlled, whereas RC products cannot. Also from equation (5), it can be seen that the cutoff frequency of the switched-capacitor filter is dependent upon the clock frequency. This leads to being able to change the cutoff frequency of a filter by just changing the clock rate.

The ability of a switched-capacitor to accurately reproduce the desired frequency response is highly dependent upon the accuracy of the capacitor ratios. MOS capacitor ratios are primarily determined by the geometrical shape of the capacitors which is defined by the photolithographic mask used to make the integrated circuit. Errors occur because the definition of the capacitor area is done optically whereby the wavelength of light results in errors. Also, precisely controlling the chemical or plasma etching of the metallization is difficult. The percentage of error generally gets smaller as the capacitor dimensions are made larger. The achievable area accuracies range from 1 to 2 percent for small capacitor areas ($\sim$400 μm^2) to on the order of 0.1 percent for larger areas ($\sim$40,000 μm^2) (McCreary and Gray 1979). The closer the capacitor ratio value approaches one, usually the greater the capacitor dimension accuracy, as there is less

of a tendency towards using a very small capacitor value to get a high ratio.

An adverse feature of switched-capacitors is that parasitic capacitance exists between the bottom plate of the switched-capacitor to the substrate and between the top plate of the switched-capacitor to the substrate. These parasitic capacitances are unavoidable, but the degrading of the filter output performance can be reduced or eliminated by careful design techniques.

The MOS switches also produce parasitic capacitances that feed through the circuit, referred to as switch feedthrough. A typical MOS switch with a channel length and width of 5 μms and an on-resistance of 5k ohms with a gate drive voltage of 5 volts would display a parasitic capacitance from source and drain to substrate of about 0.02 pF each and an overlap capacitance from drain to gate and source to gate of about 0.005 pF each. The device would display a leakage current from the source and drain to the substrate of on the order of 10^{-14} amps (Broderson et al. 1979).

The switched-capacitor integrator causes a phase shift at input frequencies approaching the clock frequency. The frequency response is given by

$$H(\omega) = -\left[\frac{C_1(f_c/C_2)}{j\omega} \right] \frac{\omega T_c}{2 \sin(\omega T_c/2)} \exp(-j\omega T_0/2) \qquad (6)$$

where:

T_0 = input signal period

T_c = clock period

f_c = clock frequency

C_1 = switched-capacitor value

C_2 = integrating capacitor value

The term in brackets of equation (6) represents the response of an ideal continuous integrator. The rest of the expression is the deviation from the response caused by the sampling process. The phase shift will distort the frequency response of the filter, typically in the form of a Q-enhancement. The Q-enhancement results in some undesired peaking in the filter response.

The phase shift can be corrected in different ways. By introducing additional phase shift, the total phase will then be the correct one. To do this requires adding circuitry that increases the component sensitivities and adds zeros to the response. Another approach is to decrease the delay time through the integrator by one-half clock cycle, by using a more complex integrator (Bruton 1975). For ladder filters, by reversing the phase of alternate clocks, one can alternately remove a full unit of delay from every other integrator.

There are several limitations to be considered in the design of a switched-capacitor filter when precise, high performance filters are desired.

The first of these is a switched-capacitor resistor cannot be in an op amp feedback path by itself. Continuous time feedback is needed to stabilize an op amp. A switched capacitor resistor can be used in parallel with capacitors to shape the frequency dependence of the feedback, as the parallel capacitor would still provide the continuous time feedback path.

Secondly, floating nodes should be avoided when possible. This is because the capacitive plates of the switched-capacitor resistors accumulate charges from parasitic sources, as addressed earlier. By providing a path from every node to a voltage source, the effects of the parasitic capacitance can be reduced.

Thirdly, at least one plate of every capacitor should be connected to a voltage source or switched between voltage sources. The plate will then be charged and discharged without affecting the filter response. Capacitive voltage dividers which sequentially switch both ends of a capacitor into an op amp should be avoided.

Fourth, the non-inverting input side of the op amp should be connected to a constant voltage. Otherwise, the filter response is sensitive to all the parasitic capacitances due to switches, bus lines and substrate that are connected to the inverting input. Increased common-mode performance would then be needed from the op amp to compensate.

Noise is another adversary of switched-capacitor filters. Noise in switched-capacitor filters is due to both thermal noise in the MOS switches and noise in the operational amplifiers. The thermal noise

source in the switch is the resistive channel of the switch when turned on, given as 4kTR. Here, k is Boltzman's constant and T is the absolute temperature. Since the MOS switch is in series with a sampling capacitor, an RC circuit is formed between the switch resistance (R) and the sampling capacitor (C). This RC circuit then bandlimits the noise power to

$$V_{RMS}^2 = (4kTR) \ [\frac{1}{4RC}] = \frac{kT}{C} \tag{7}$$

When the switch turns off, the noise is sampled and passed to the sampling capacitor.

CHAPTER 3

SWITCHED-CAPACITOR SALLEN AND KEY FILTER

In that the Sallen and Key analog filter has many benefits over other types of analog filters, it was highly desirable to examine its use as a switched-capacitor filter. No previous literature has been found that attempted to implement a switched-capacitor Sallen and Key filter. Previous literature states that the Sallen and Key structure has been avoided because it results in floating nodes (Van Valkenburg 1982). Floating node circuits are generally considered to be more susceptible to parasitic capacitance than some other types of switched-capacitor circuits. The parasitic capacitance susceptibility of the switched-capacitor Sallen and Key filter is to be examined in this chapter.

Selection of Sallen and Key Topology

The unity gain Sallen and Key lowpass analog second-order section shown in Figure 3.1 was chosen for switched-capacitor implementation because it has several benefits over other filter topologies. It has the lowest sensitivity values of all the other Sallen and Key topologies and is the only topology independent of the Q value. Also, it consists of a voltage follower op amp topology which reduces the number of components by at least two resistors over
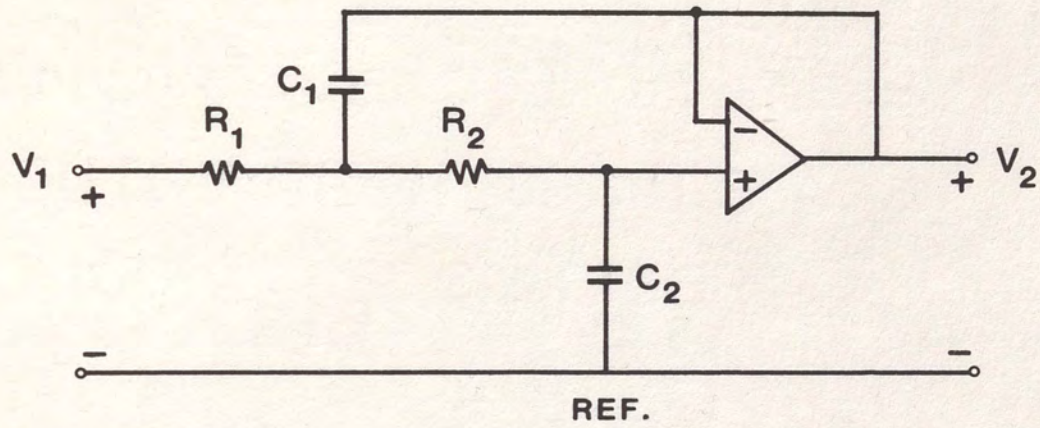
Figure 3.1. Sallen and Key lowpass analog second-order filter
section.

the other Sallen and Key topologies. This results in this circuit being the easiest to design because the gain of the amplifier would not need to be precisely designed and built. This topology would be minimum cost to implement as there would be fewer components and trimming of resistor values would not be needed. Other Sallen and Key filters would require trimming of resistor components to get precise gain values needed.

Transfer Function of Sallen and Key Second-Order Section

The transfer function for the circuit of Figure 3.1 is

$$\frac{V_2}{V_1} = \frac{1}{R_1 R_2 C_1 C_2 S^2 + (R_1 + R_2) C_2 S + 1} \tag{7a}$$

Recognizing the transfer function to be of the general form of a second-order lowpass filter of

$$T(s) = \frac{K}{\frac{s^2}{\omega_o^2} + \frac{1}{\omega_o Q} s + 1} \tag{7b}$$

and setting equal the coefficients of the S midterms gives

$$\frac{1}{\omega_o Q} = (R_1 + R_2) C_2$$

Rearranging gives

$$Q = \frac{1}{\omega_o C_2 (R_1 + R_2)}$$

Considering the case where $R_1 = R_2 = 1$ and $\omega_0 = 1$ gives

$$Q = \frac{1}{2C_2} \tag{8}$$

and

$$C_1 C_2 = 1 \tag{9}$$

Then

$$C_2 = \frac{1}{C_1} \quad \text{(from equation 9)}$$

and

$$C_2 = \frac{1}{2Q} \quad \text{(from equation 8)}$$

$$\frac{1}{C_1} = \frac{1}{2Q}$$

$$C_1 = 2Q$$

$$\frac{C_1}{C_2} = \frac{2Q}{\frac{1}{2Q}} = 4Q^2$$

The C_1/C_2 ratio being equal to $4Q^2$ indicates that there could be a large spread of values for C_1 and C_2. The larger the desired Q, the wider the spread of C_1 and C_2. The values of R_1, R_2 and ω_0 can be changed to practical values from unity by magnitude and frequency

scaling. The values of R_1 and R_2 should be as close to equal as practical.

The switched-capacitor version of the transfer function can be found by substituting $R_1 = 1/f_c C_{R1}$ and $R_2 = 1/f_c C_{R2}$ into equation (7a).

$$\frac{V_2}{V_1} = \frac{1}{[\frac{1}{f_c C_{R1}} \frac{1}{f_c C_{R2}}] C_1 C_2 s^2 + [\frac{1}{f_c C_{R1}} + \frac{1}{f_c C_{R2}}] C_2 s + 1}$$

$$\frac{V_2}{V_1} = \frac{1}{\frac{C_1 C_2}{f_c^2 C_{R1} C_{R2}} s^2 + [\frac{1}{C_{R1}} + \frac{1}{C_{R2}}] \frac{C_2}{f_c} s + 1} \tag{10}$$

Switched-Capacitor Implementation of Sallen and Key Circuit

The switched-capacitor implementation of the Sallen and Key circuit in Figure 3.1 is shown in Figure 3.2. The clock frequency signals ϕ_1 and ϕ_2 results from an RC circuit signal that passes through four Schmitt triggered NAND gates. The resulting one shot clock frequency from the RC product of the capacitor of 361 pF with a 4700 ohm resistor was 589,379 Hz. A capacitor was added on each of the plus and minus 5 volt inputs to remove noise from the voltage source signals and add stability to the signals. The MOS switch pairs S_1 and S_2 are used to switch capacitor C_{R1} of 47.5 pF, to simulate resistor R_1. Similarly, the MOS switch pairs S_3 and S_4 are used to switch capacitor C_{R2} of 49 pF, to simulate resistor R_2.

Capacitors C_1 and C_2 are approximately 2.2 nF each. This gives a C_1/C_2 ratio of approximately one and a Q of one-half.

MOS switches of the type HC 4066 were chosen because of their low ON resistance and low "off" leakages.

The integrating op amp chosen was an LF 351 op amp because of its high slew rate of 13 volts per microsecond, large gain bandwidth product of 4 MHz, fast settling time of 2 microseconds to within 0.01%, and its high common mode rejection ratio of 100 dB. This gives greater stability and higher performance capability to the circuit.

Operational Results of Switched-Capacitor
Sallen and Key Circuit

The operational results of the circuit of Figure 3.2 showed that a switched-capacitor Sallen and Key filter was feasible but the rolloff of the filter leveled off early and there was considerable noise in the output signal, as shown in Figure 3.3. Figure 3.3 is a photograph of the frequency response of the switched-capacitor filter with a cutoff frequency of about 2600 Hz. The photograph was taken on a Hewlett-Packard 3528A spectrum analyzer. The vertical scale is 10 dB per division and the horizontal scale is 2500 Hz per division. The rolloff can be seen in Figure 3.3 to descend about 45 dB over a 25 kHz bandwidth and then level out. This was believed to be caused by a problem familiar to sample and hold systems called aliasing. The maximum clock frequency determines the maximum analog input frequency
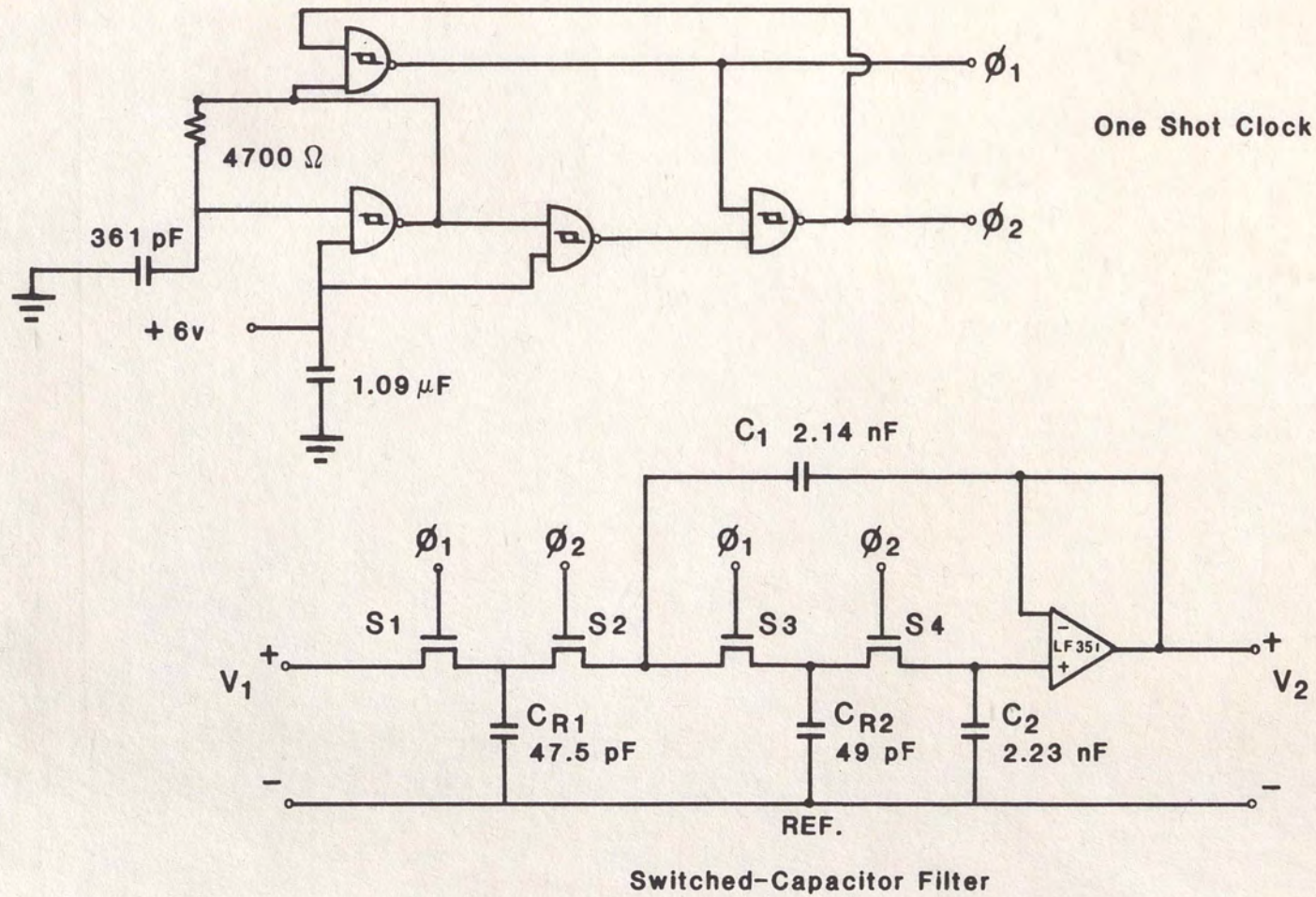
One Shot Clock

Switched-Capacitor Filter

Figure 3.2. Switched-capacitor Sallen and Key lowpass second-order filter section with one shot clock.
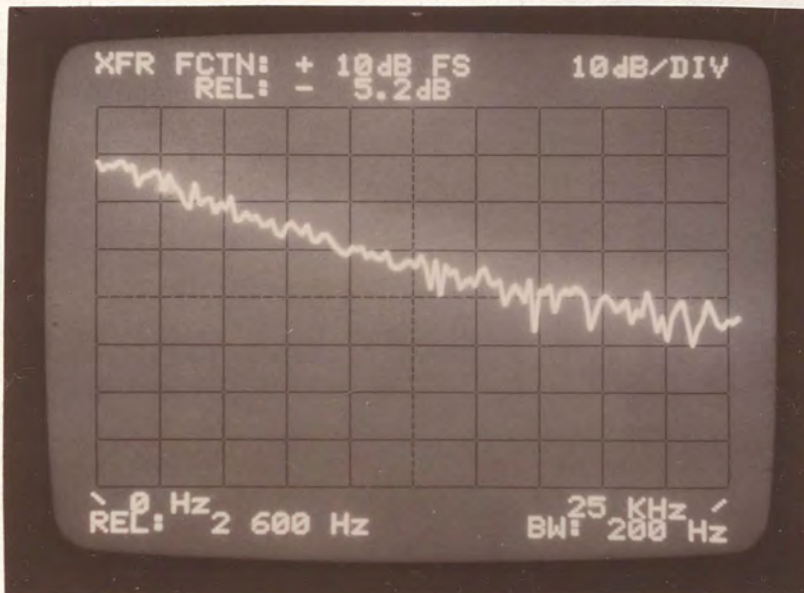
Figure 3.3.   Spectrum analyzer photograph of Figure 3.2
             switched-capacitor filter frequency response.
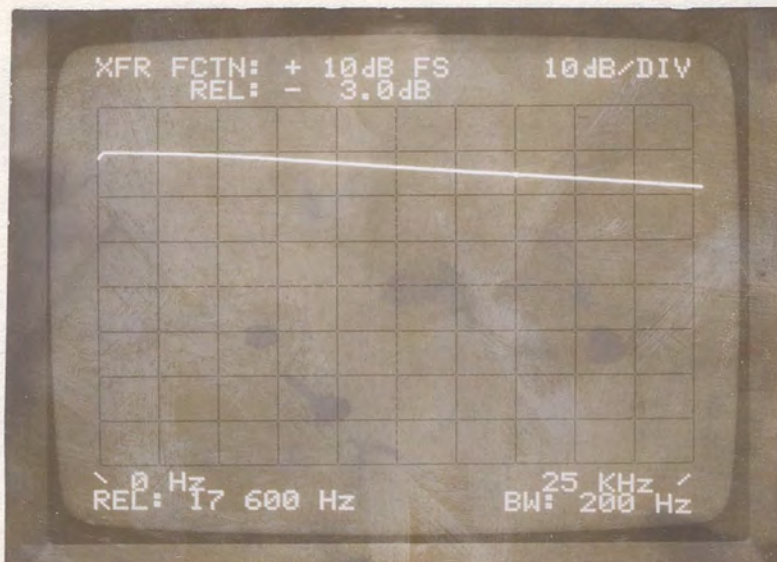
Figure 3.4.   Spectrum analyzer photograph of Figure 3.5
             anti-aliasing filter frequency response, displaying
             cutoff frequency of 17,600 Hz.

which may be reconstructed at the integrator output. The clock frequency must be at least twice the input signal frequency, according to the Nyquist criteria, to avoid aliasing. The aliasing distortion is caused by foldover of the higher frequencies. This aliasing problem will be precluded by bandlimiting the input signal.

The analog input signal is bandwidth limited by an anti-aliasing filter composed of a unity gain second-order Sallen and Key lowpass filter with a cutoff frequency of 17,600 Hz. Figure 3.4 displays the frequency response of the anti-aliasing filter over a 25 kHz bandwidth. The cutoff frequency of the anti-aliasing filter is seen in the photograph to be at 17,600 Hz. The anti-aliasing filter with the switched-capacitor filter circuit is shown in Figure 3.5.

There was a considerable performance improvement in the filter with the addition of the anti-aliasing filter. The performance of the rolloff improved by approximately 10 dB over a 25 kHz bandwidth. Figure 3.6 displays the performance of the switched-capacitor Sallen and Key lowpass circuit with the anti-aliasing filter. The rolloff descends about 55 dB over a 25 kHz bandwidth, but there is still noise distortion in the output of the filter, as seen by the rippling.

Much of the noise was thought to be caused by the switch feedthrough of the MOS switches. Although the clock pulses were non-overlapping, there was too close a transition from ϕ_1 to ϕ_2. This did not give enough time for the MOS switches to open and close properly, allowing switch feedthrough noise to show up in the filter
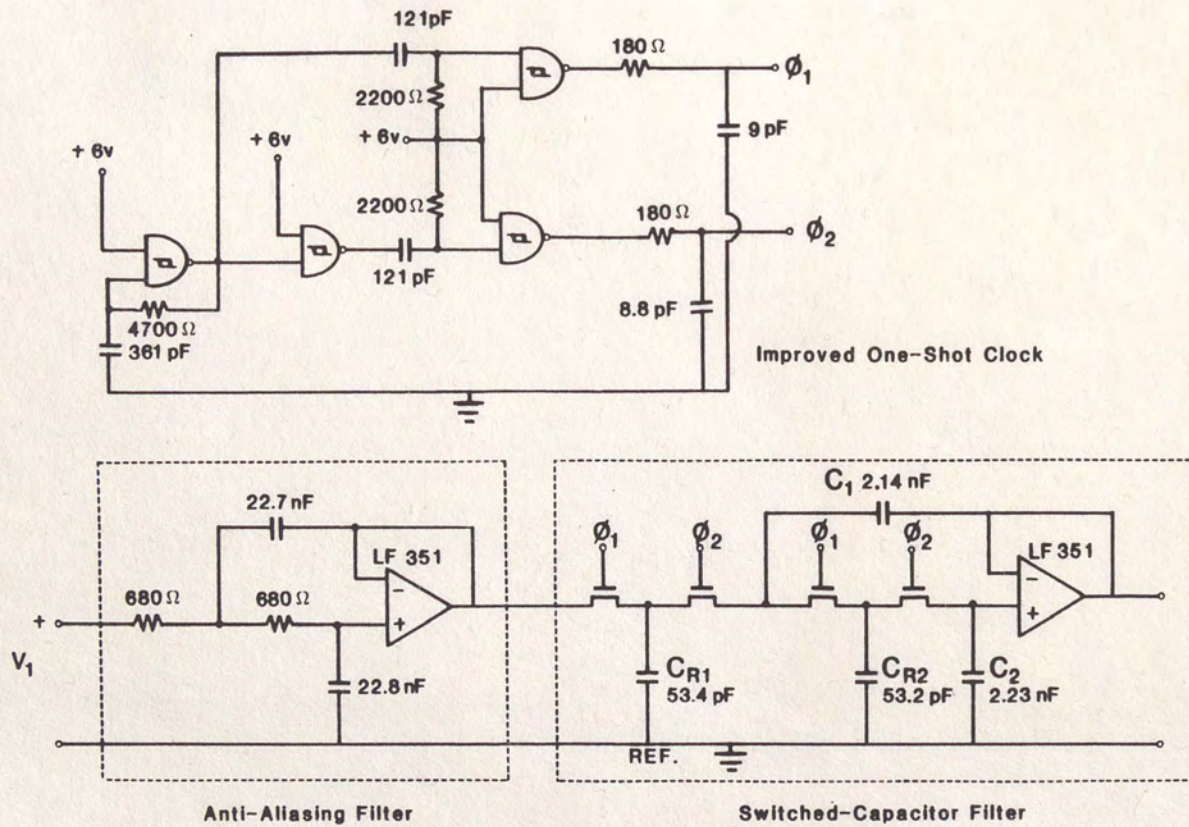
Figure 3.5. Switched-capacitor Sallen and Key lowpass second-order filter with anti-aliasing filter and improved one shot clock.

output. By increasing the delay between ϕ_1 and ϕ_2, the MOS switches could properly close and open, reducing the switch feedthrough noise. The delay on the transition from ϕ_1 to ϕ_2 and ϕ_2 to ϕ_1 was accomplished by adding an RC circuit in front of each of the last NAND gates for both ϕ_1 and ϕ_2. The two RC circuits consisted of a 121 pF capacitor and a 2200 ohm resistor for each.

The switched-capacitors did not have enough time to fully charge and discharge. To remedy this, an RC circuit was added on the front of each of the ϕ_1 and ϕ_2 outputs. The RC circuit consisted of a 9 pF capacitor and a 180 ohm resistor. The RC circuits caused the clock pulses to ramp up and ramp down, allowing time for the switched-capacitors to fully charge and discharge. The resulting switched-capacitor one shot clock circuit is shown in Figure 3.5.

The actual results of the RC circuits on the clock outputs ϕ_1 and ϕ_2 are shown in Figure 3.7. The photograph was taken on a Leader LBO-514A Dual Trace Oscilloscope with the vertical scale on 5 v/division and the horizontal scale on 0.5 μs/division. The top trace is the clock ϕ_1 and the bottom trace is the clock ϕ_2. The clock frequency is 589,379 Hz, as before. The pulses can be seen to ramp up and down with considerable spacing between the pulses to allow for different clock frequencies. The actual results of the operation of the filter with the improved one shot clock and anti-aliasing filter over a 10 kHz bandwidth is shown in the photograph of Figure 3.8a. The noise distortion is significantly reduced, resulting in a quality switched-capacitor filter.
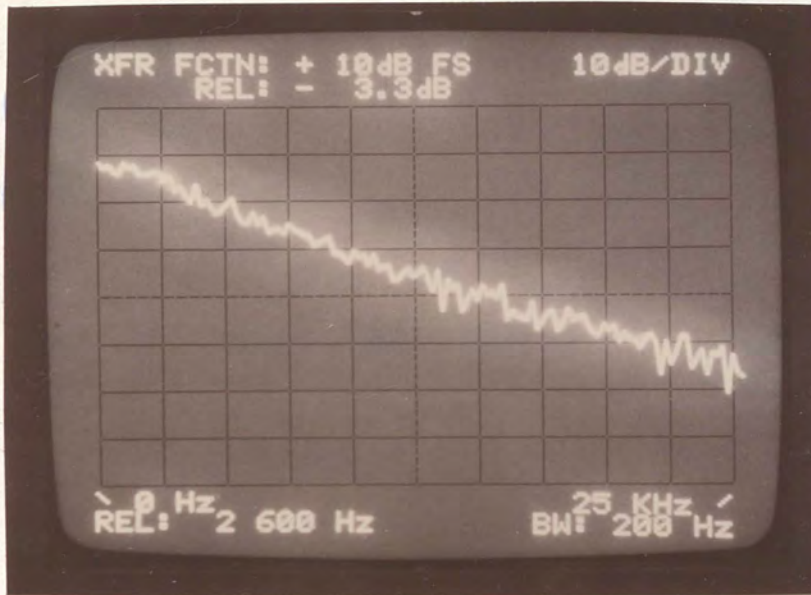
Figure 3.6.   Spectrum analyzer photograph of Figure 3.2
switched-capacitor filter frequency response,
with the anti-aliasing filter.

VER = 10 dB/cm

HOR = 2500 Hz/cm
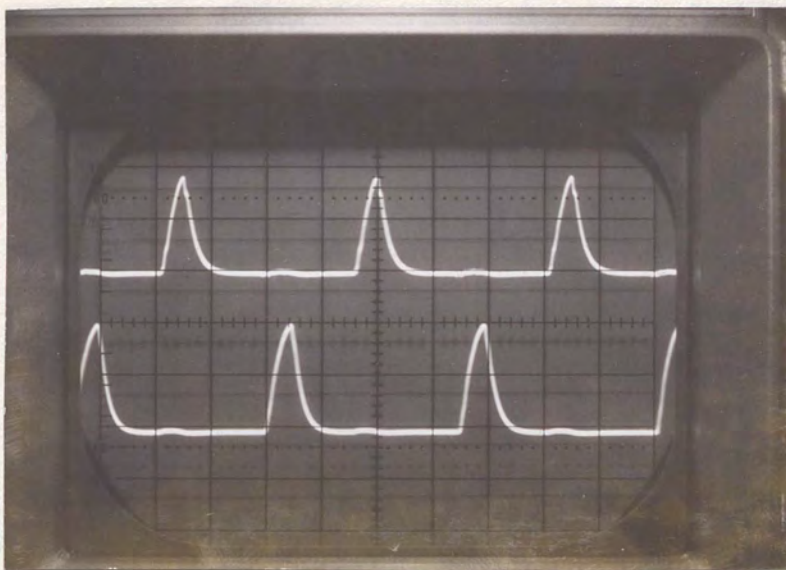
VER = 5 v/cm

HOR = 0.5 μs/cm

Figure 3.7.   Oscilloscope photograph of clock signal ϕ_1 (upper
trace) and clock signal ϕ_2 (lower trace).
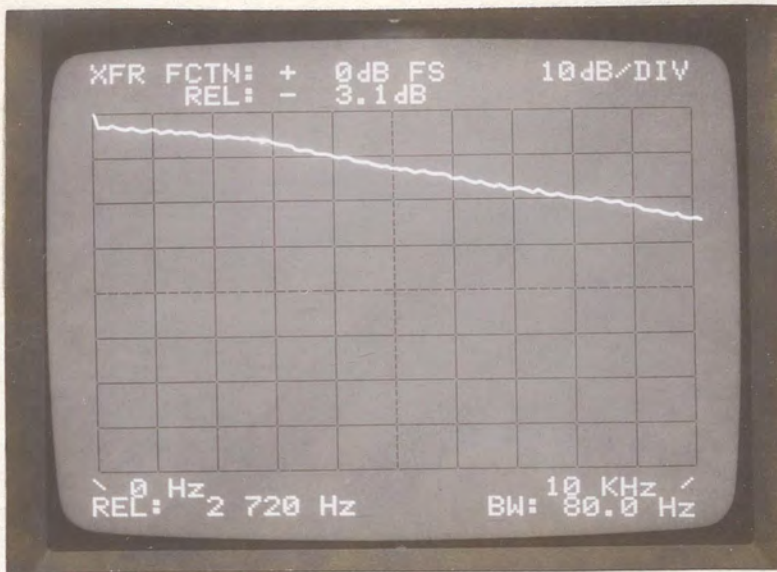
VER = 10 dB/cm

HOR = 1000 Hz/cm

(a)
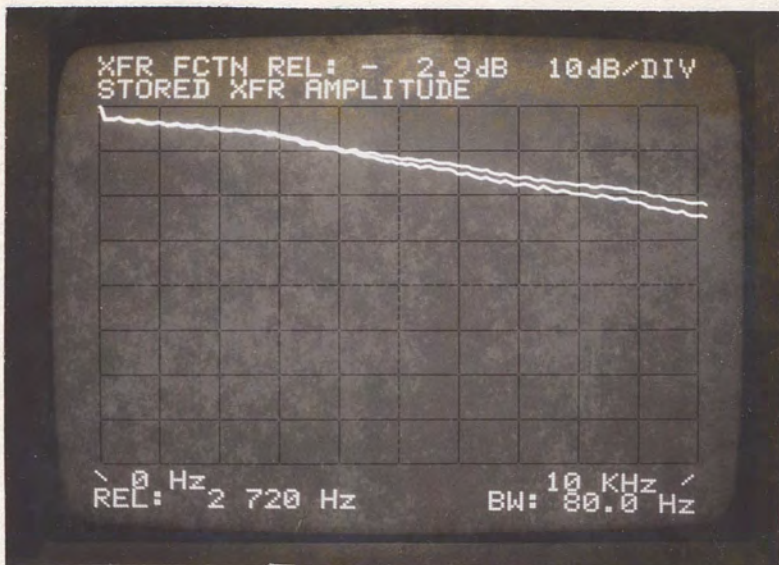
VER = 10 dB/cm

HOR = 1000 Hz/cm

(·b)

Figure 3.8.   Spectrum analyzer photographs of the Figure 3.5
switched-capacitor filter frequency response.
(a) with anti-aliasing filter
(b) comparison of without anti-aliasing filter
(upper trace) and with anti-aliasing filter
(lower trace)

Figure 3.8b demonstrates the need for the anti-aliasing filter, even with the one shot clock changes. The Hewlett-Packard 4528A Spectrum Analyzer has a storage feature that allows storing a trace and later displaying the trace simultaneously with another trace. The top trace of the photograph of Figure 3.8b is the switched-capacitor filter output without the anti-aliasing filter and the lower trace is the switched-capacitor filter output with the anti-aliasing filter, both over a 10 kHz bandwidth. The dynamic range performance is seen to increase by 4 dB over the 10 kHz bandwidth by the addition of the anti-aliasing filter.

To demonstrate that the switched-capacitor Sallen and Key second-order lowpass filter of Figure 3.5 cutoff frequency is clock frequency variable, the clock frequency was changed from 589,379 Hz to 247,978 Hz by changing the clock frequency capacitor from 361 pF to 858 pF. The result is shown in Figure 3.9a. The upper trace represents the filter frequency response for the 589,379 Hz clock frequency. The lower trace represents the filter frequency response for the 247,978 Hz clock frequency. The cutoff frequency of the filter changed from 2720 Hz to 960 Hz, as expected for the switched-capacitor filter.

Figure 3.9b shows the results of varying the clock frequency as before, but this time over a 25 kHz bandwidth. The cutoff frequency changes from 2400 Hz to 800 Hz with a dynamic range of about 50 dB. This dynamic range is excellent for a second-order filter.

(a)

VER = 10 dB/cm

HOR = 1000 Hz/cm

(b)
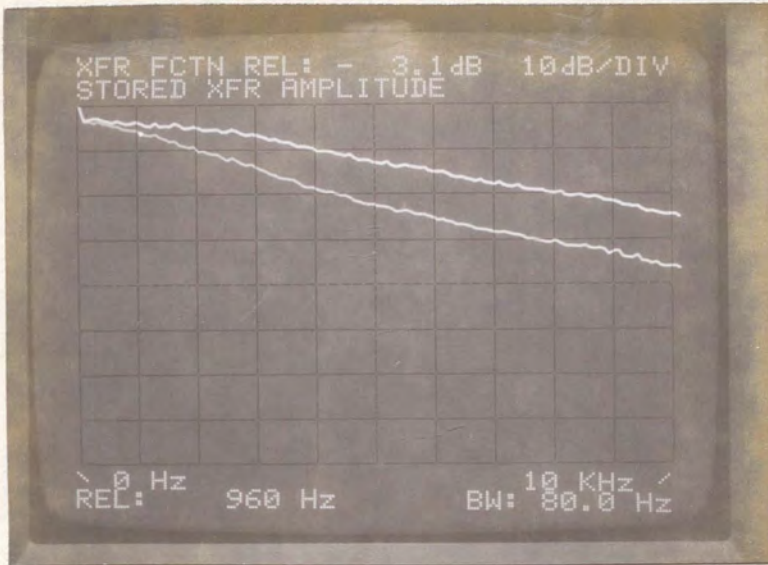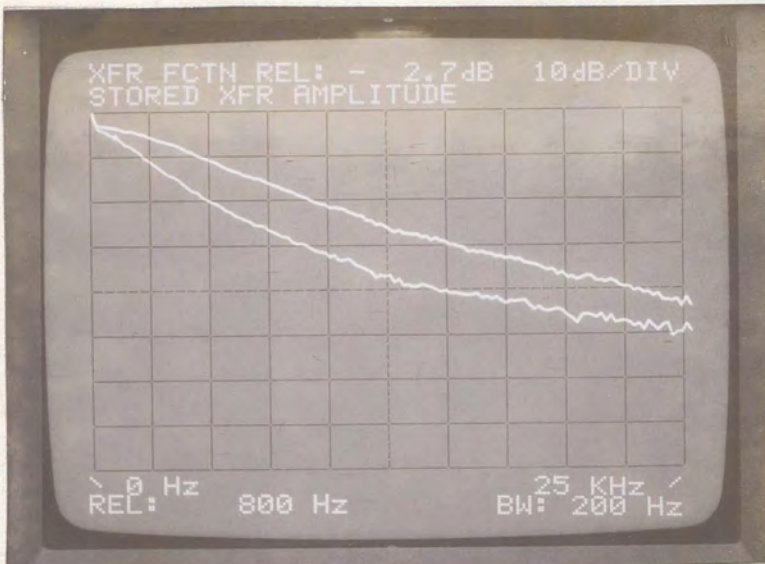
VER = 10 dB/cm

HOR = 2500 Hz/cm

Figure 3.9. Spectrum analyzer photographs of the Figure 3.5
switched-capacitor filter frequency response for
different clock frequencies and bandwidths.
(a) 589,379 Hz clock frequency (upper trace) and
    247,978 Hz clock frequency (lower trace), over
    a 10 kHz bandwidth
(b) 589,379 Hz clock frequency (upper trace) and
    247,978 Hz clock frequency (lower trace), over
    a 25 kHz bandwidth

Figure 3.10 shows the random noise input of the spectrum analyzer on the top trace of the oscilloscope photograph and the resulting output of the switched-capacitor Sallen and Key filter on the bottom trace of the same photograph. The filter does an excellent job of attenuating the incoming signals. The cutoff frequency of the filter was set at 800 Hz.

Figure 3.11 shows a photograph of the actual breadboard of the switched-capacitor Sallen and Key lowpass second-order filter section. Figure 3.12 is the board layout used for the switched-capacitor Sallen and Key second-order lowpass filter section with the one shot clock and the anti-aliasing filter. The component values selected for the actual circuits were made to give the switched-capacitor filters cutoff frequencies in the range of 2000 Hz for ease of viewing and analysis. The components were 1/4 watt, $\pm$ 5% resistors and 20 to 50 volts, $\pm$ 10% to $\pm$ 20% capacitors. The actual circuits were operated with a supply voltage of $\pm$ 6 volts.

A MICROCAP simulation of the switched-capacitor Sallen and Key second-order lowpass circuit was run using the equivalent resistor values for the switched-capacitors at a clock frequency of 589,379 Hz. The cutoff frequency of the filter came out considerably less than the actual circuit. With the breadboard layouts, there is a 5 pF per board connection capacitance and a 3 pF per IC pin connection capacitance. Since there were four board connections and two IC pin connections in each switching action, this added 26 pF to the switched-capacitors. With this accounted for in the equivalent
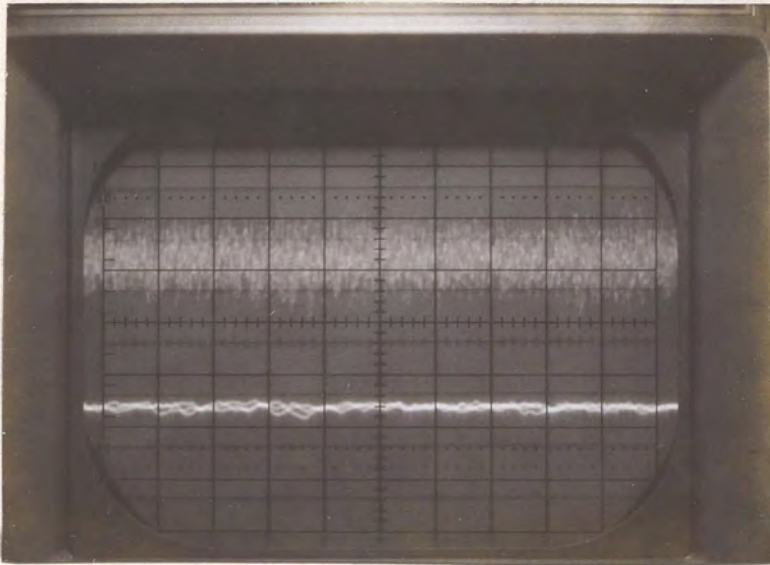
VER = 2 v/cm

HOR = 1 ms/cm

Figure 3.10.   Oscilloscope photograph of random noise input (upper
trace) and Figure 3.5 switched-capacitor filter
response (lower trace). The filter cutoff frequency
was 800 Hz.
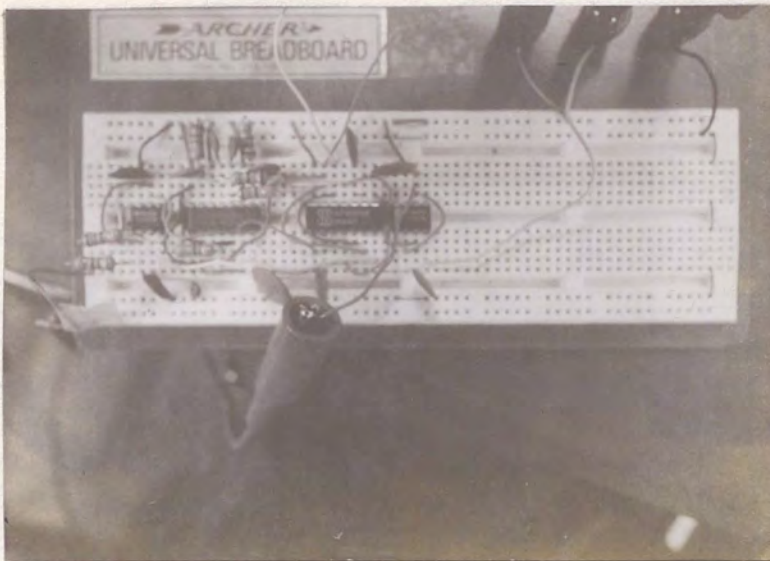
Figure 3.11.   Photograph of switched-capacitor Sallen and Key
lowpass second-order filter section breadboard.
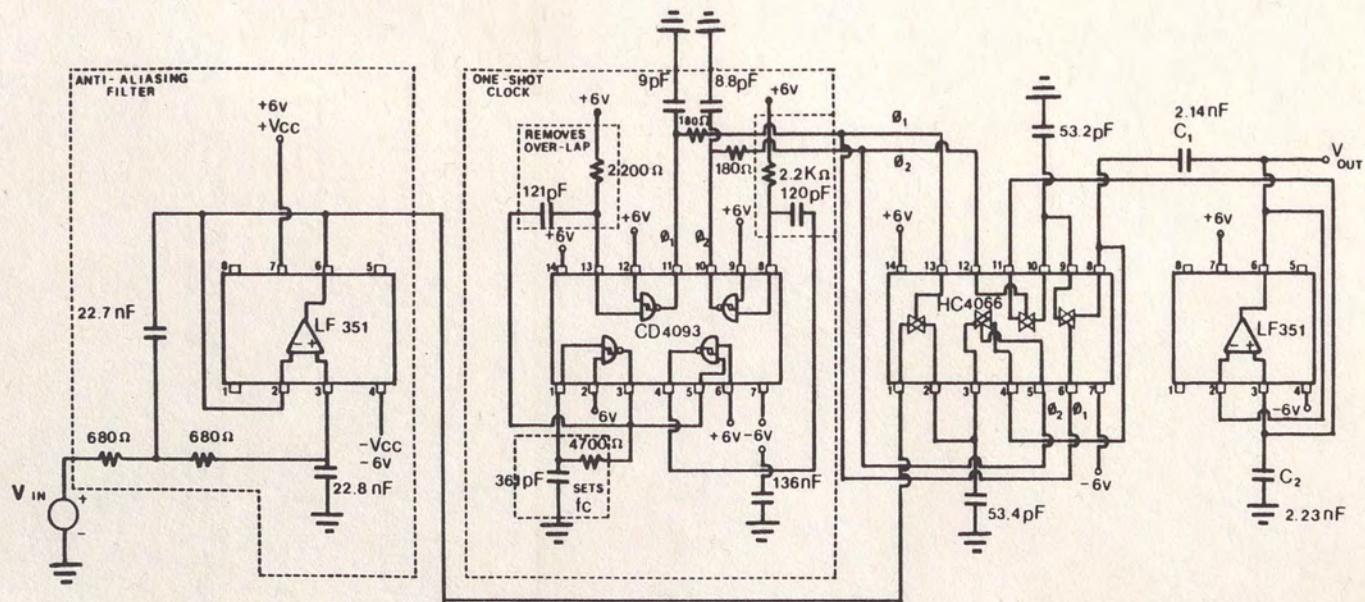
Figure 3.12. Board layout of the switched-capacitor Sallen and Key lowpass second-order filter section with one shot clock and anti-aliasing filter.

resistors, the cutoff frequency matched closely with the actual board cutoff frequency. The MICROCAP simulation circuit is shown in Figure 3.13. The MICROCAP gain (dB) versus frequency (Hz) plot is shown in Figure 3.14. The MICROCAP frequency anlysis is shown in Figure 3.15, with the filter cutoff frequency bracketed. The frequency response and the cutoff frequency of the MICROCAP simulation match closely with the actual filter frequency response photograph of Figure 3.8a, which was at the same clock frequency of 589,379 Hz. Although the Sallen and Key second-order lowpass filter section could be considered quite acceptable for many applications, there is some distortion in the output that could cause problems.

If the distortion is a problem in an application, the order of the filter could be made higher by cascading the switched-capacitor sections together. This would move the distortion out at the rate of the order times 6 dB per octave to a point where the noise would be insignificant. Another approach would be to add MOS switches for each capacitor plate of the switched-capacitors so that the plate is switched to ground when in the off state, thereby fully discharging the capacitor plate. The distortion could also be reduced by adding an RC buffer in front of each op amp to cutoff the noise. This approach was used to develop a modified topology which is covered in the next chapter.

Figure 3.13. MICROCAP simulation circuit of the switched-capacitor
Sallen and Key second-order filter section.

Figure 3.14. MICROCAP gain (dB) versus frequency (Hz) plot of the switched-capacitor Sallen and Key second-order filter section.

```
                        SPECTRUM SOFTWARE
                          MICRO-CAP II
                       FREQUENCY ANALYSIS
                              FOR
                         THESIS CIRCUIT
                   TEMPERATURE= 27 CASE= 1
```

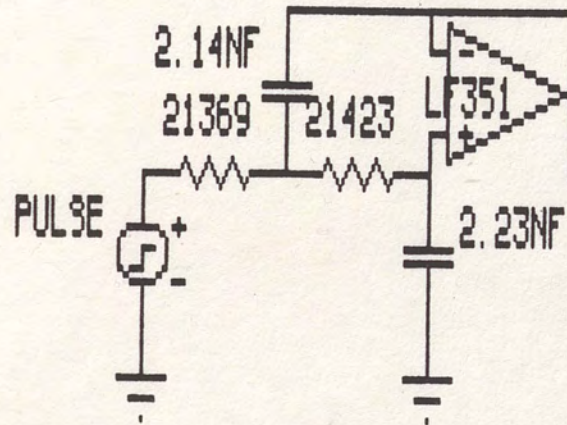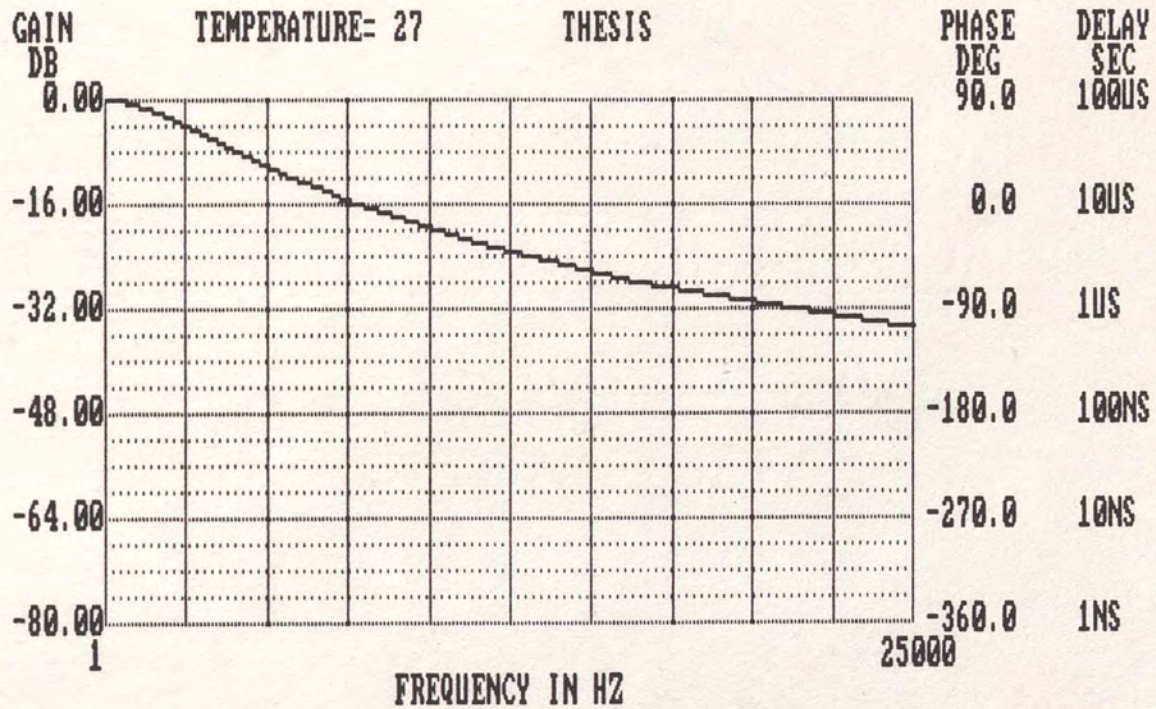| FREQUENCY	GAIN(DB)	ANGLE(DEGREES)	DELAY(SEC)	SLOPE(DB/OCTAVE)
100.00000D-02	-875.47432D-05	-343.85381D-04	185.40783D-08	-118.02339E-01
105.00000D-02	-875.48263D-05	-361.04651D-04	955.15013D-07	-118.06329E-08
115.00000D-02	-875.50047D-05	-395.43190D-04	955.14951D-07	-135.90604E-08
135.00000D-02	-875.54101D-05	-464.20265D-04	955.14948D-07	-175.24422E-08
175.00000D-02	-875.64154D-05	-601.74416D-04	955.14939D-07	-268.52726E-08
255.00000D-02	-875.92045D-05	-876.82711D-04	955.14918D-07	-513.50180E-08
415.00000D-02	-876.78959D-05	-142.69925D-03	955.14838D-07	-123.70142E-07
735.00000D-02	-879.77321D-05	-252.73211D-03	955.14638D-07	-361.81191E-07
137.50000D-01	-890.72170D-05	-472.79604D-03	955.13865D-07	-121.16315E-06
265.50000D-01	-932.54244D-05	-912.91043D-03	955.10939D-07	-440.55204E-06
521.50000D-01	-109.58600D-04	-179.30349D-02	954.99626D-07	-167.68479E-05
103.35000D+00	-174.09010D-04	-355.24625D-02	954.55057D-07	-653.66989E-05
205.75000D+00	-429.99020D-04	-706.48188D-02	952.78768D-07	-257.61217E-04
410.55000D+00	-144.19718D-03	-140.38345D-01	945.84510D-07	-101.53673E-03
820.15000D+00	-535.50888D-03	-275.94816D-01	919.35704D-07	-391.96631E-03
163.93500D+01	-192.78399D-02	-520.57993D-01	829.50775D-07	-139.34956E-02
327.77500D+01	-588.30337D-02	-880.15556D-01	609.63210D-07	-395.68479E-02
409.69500D+01	-795.85224D-02	-100.51893D+00	609.63210D-07	-644.87314E-02
491.61500D+01	-995.32681D-02	-110.42162D+00	335.78453D-07	-758.51998E-02
573.53500D+01	-118.32767D-01	-118.36206D+00	269.24773D-07	-845.27845E-02
655.45500D+01	-135.88313D-01	-124.81970D+00	218.96826D-07	-911.42635E-02
737.37500D+01	-152.23158D-01	-130.14616D+00	180.61195D-07	-962.22982E-02
819.29500D+01	-167.45564D-01	-134.59863D+00	150.97637D-07	-100.16848E-01
983.13500D+01	-194.92688D-01	-141.59079D+00	118.54656D-07	-104.45079E-01
114.69750D+02	-219.05817D-01	-146.80882B+00	884.67502D-08	-108.51741E-01
131.08150D+02	-240.48684D-01	-150.84071D+00	683.57595D-08	-111.24253E-01
147.46550D+02	-259.71175D-01	-154.04575D+00	543.38928D-08	-113.14539E-01
163.84950D+02	-277.11825D-01	-156.65379D+00	442.17165D-08	-114.52109E-01
180.23350D+02	-293.00525D-01	-158.81786D+00	366.90092D-08	-115.54524E-01
213.00150D+02	-321.11004D-01	-162.20537D+00	287.16326D-08	-116.61913E-01
245.76950D+02	-345.38952D-01	-164.74252D+00	215.07634D-08	-117.60903E-01
250.00000D+02	-348.29552D-01	-165.02489D+00	185.40783D-08	-118.02339E-01

Figure 3.15.   MICROCAP frequency analysis of the switched-capacitor
               Sallen and Key second-order filter section.

CHAPTER 4

IMPROVEMENT OF SWITCHED-CAPACITOR SALLEN AND KEY FILTER

Improved Switched-Capacitor Sallen and Key Topology

A third-order section with built-in buffers between each of the stages was used in modification of the Sallen and Key second-order lowpass filter of the previous chapter. The analog and switched-capacitor versions of this improved Sallen and Key filter are shown in figures 4.1 and 4.2, respectively. The unity gain voltage follower concept that was used for the Sallen and Key second-order filter was retained in the third-order section to keep the benefits of minimum components and less gain sensitivity requirements. RC circuits were added between each of the op amps to act as buffers and, thereby, shield out parasitic feedthrough. Feedback paths were added on the first and second op amp paths to increase the settling rate of the filter and, thereby, improve the filter response time.

Transfer Function of Improved Sallen and Key Circuit

The transfer function for the circuit of Figure 4.1 is derived using Mason's rule (Franklin and Powell 1980). Mason's rule gives the transfer function as

$$T(s) = \frac{FFG}{1 - \Sigma FBG}$$

Figure 4.1. Improved Sallen and Key analog filter to be implemented as a switched-capacitor filter.
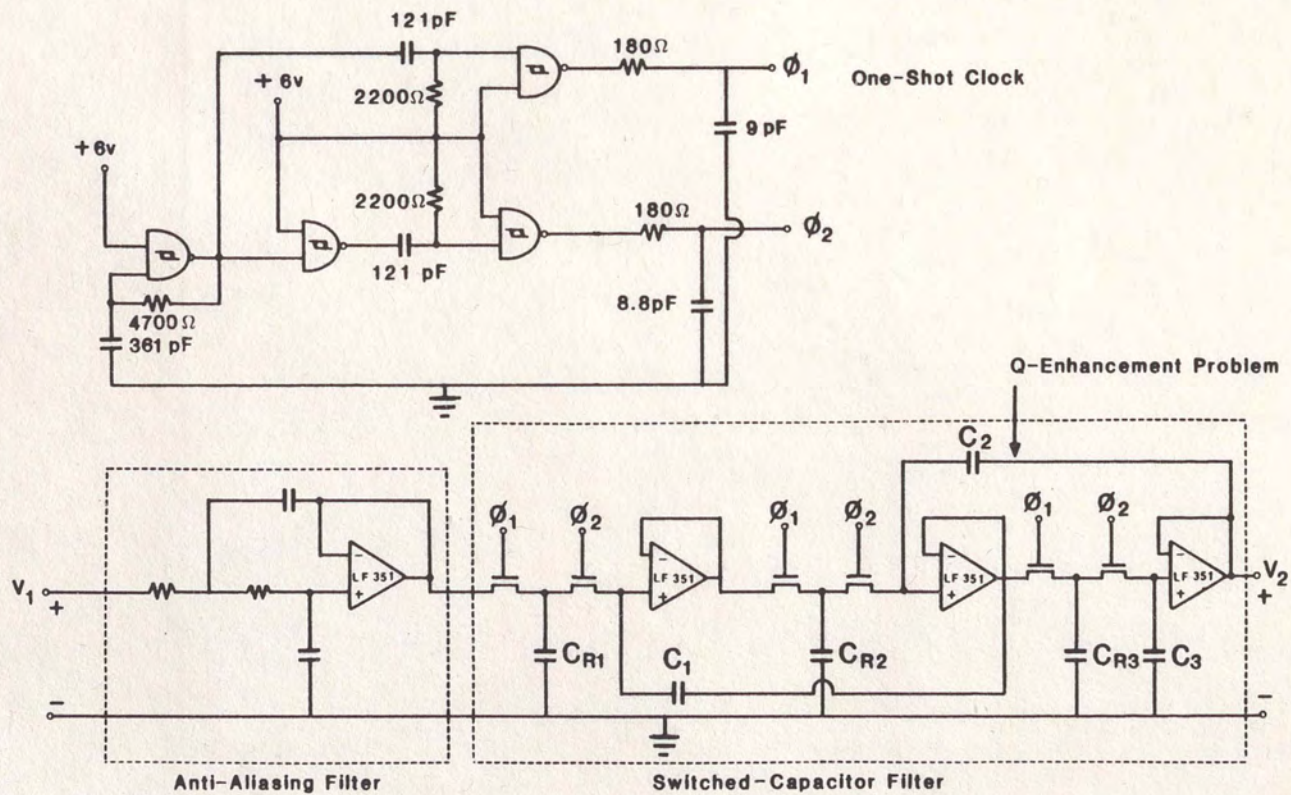
Figure 4.2. Improved switched-capacitor Sallen and Key third-order lowpass filter section.

$$\frac{V_2}{V_1} = \frac{\dfrac{1}{(1+R_1C_1s)(1+R_2C_2s)(1+R_3C_3s)}}{1 - [\dfrac{R_1C_1s}{1+R_1C_1s} \times \dfrac{1}{1+R_2C_2s} + \dfrac{R_2C_2s}{1+R_2C_2s} \times \dfrac{1}{1+R_3C_3s}]}$$

$$= \frac{1}{(1+R_1C_1s)(1+R_2C_2s)(1+R_3C_3s)-[R_1C_1s(1+R_3C_3s)+R_2C_2s(1+R_1C_1s)]}$$

$$= \frac{1}{(1+R_2C_2s+R_1C_1s+R_1R_2C_1C_2s^2)(1+R_3C_3s)-(R_1C_1s+R_1R_3C_1C_3s^2+R_2C_2s+R_1R_2C_1C_2s^2)}$$

$$= \frac{1}{1+R_2C_2s+R_1C_1s+R_1R_2C_1C_2s^2+R_3C_3s+R_2R_3C_2C_3s^2+R_1R_3C_1C_3s^2+\ldots}$$

$$\frac{1}{\ldots R_1R_2R_3C_1C_2C_3s^3-R_1C_1s-R_1R_3C_1C_3s^2-R_2C_2s-R_1R_2C_1C_2s^2}$$

$$\frac{V_2}{V_1} = \frac{1}{R_1R_2R_3C_1C_2C_3s^3+R_2R_3C_2C_3s^2+R_3C_3s+1}$$

The transfer function for the switched-capacitor filter is

$$\frac{V_2}{V_1} = \frac{1}{\dfrac{C_1C_2C_3}{f_c^3C_{R1}C_{R2}C_{R3}}s^3 + \dfrac{C_2C_3}{f_c^2C_{R2}C_{R3}}s^2 + \dfrac{C_3}{f_cC_{R3}}s + 1}$$

Results of the Improved Switched-Capacitor Sallen and Key Filter

The results of the modified Sallen and Key lowpass filter was

an undesired Q-enhancement and distortion of the response. This can

(a)

VER = 10 dB/cm

HOR = 1000 Hz/cm

(b)
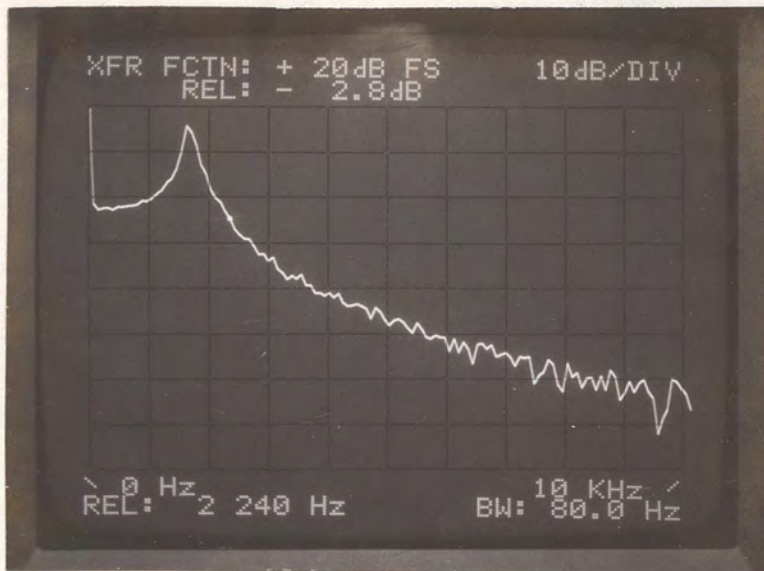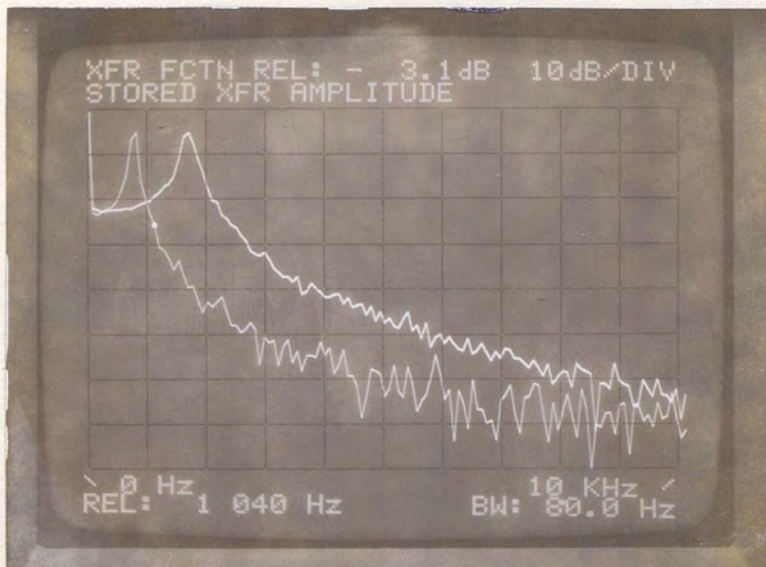
VER = 10 dB/cm

HOR = 1000 Hz/cm

Figure 4.3. Spectrum analyzer photograph of Figure 4.2 improved switched-capacitor Sallen and Key filter frequency response.
(a) displays Q-enhancement at 1500 Hz
(b) comparison of filter frequency response and cutoff frequency for 589,379 Hz clock frequency (upper trace) and 247,979 Hz clock frequency (lower trace)
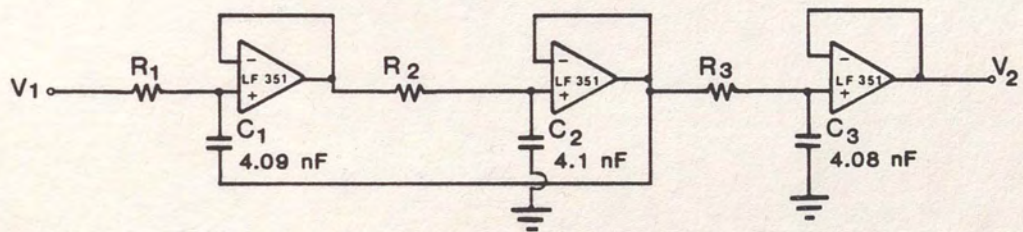
Figure 4.4. Improved Sallen and Key analog filter with changed feedback path.
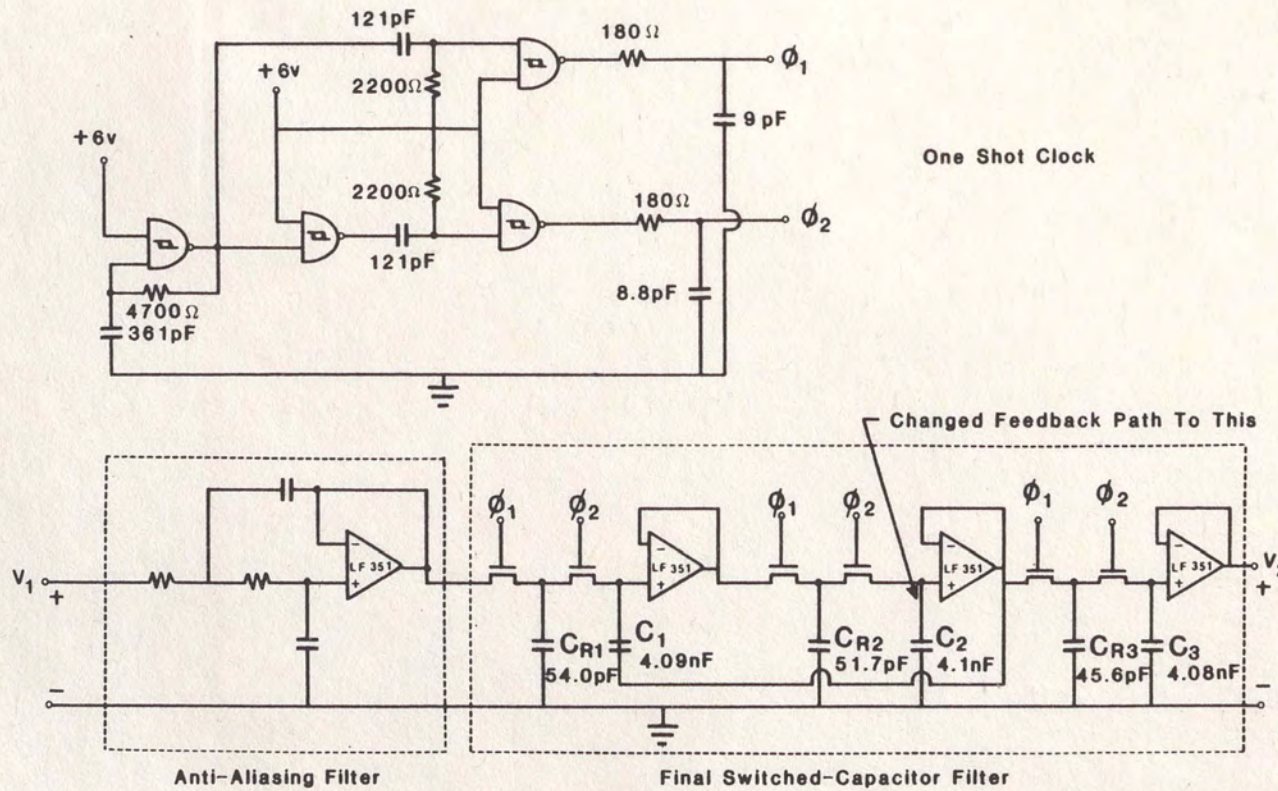
Figure 4.5. Improved switched-capacitor Sallen and Key third-order lowpass filter section with changed feedback path.

be seen in Figure 4.3a. The Q-enhancement was most likely caused by a phase shift of the frequency response between the second and third stages. Even still, the filter acted properly as a switched-capacitor filter. When the clock frequency was changed, the filter cutoff frequency changed appropriately, as seen in Figure 4.3b.

Improved Switched-Capacitor Sallen and Key Filter with Changed Feedback Path

When the feedback path from the second to third stage was removed from the third stage and terminated to ground, the operation of the filter showed a much improved, high-performance response. The result of this change to the circuit is shown as Figure 4.4. Figure 4.5 is the corresponding switched-capacitor implementation of the circuit.

Transfer Function of Improved Switched-Capacitor Sallen and Key Filter with Changed Feedback Path

The transfer function for Figure 4.4 is derived using Mason's rule. Mason's rule gives the transfer function as
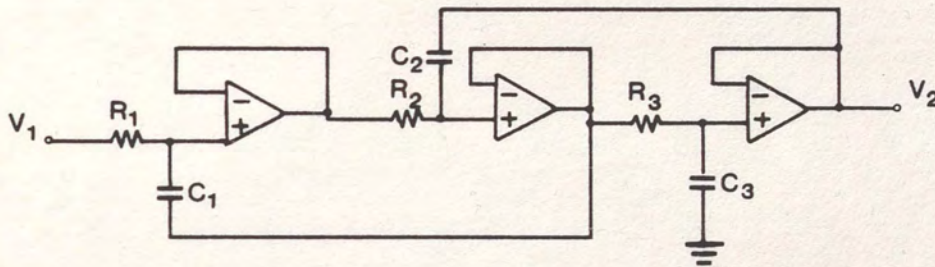
$$T(s) = \frac{FFG}{1 - \Sigma FBG}$$

$$\frac{V_2}{V_1} = \frac{\dfrac{1}{(1+R_1C_1s)(1+R_2C_2s)(1+R_3C_3s)}}{1 - [\dfrac{R_1C_1s}{1+R_1C_1s} \times \dfrac{1}{1+R_2C_2s}]}$$

$$= \frac{1}{(1+R_1C_1s)(1+R_2C_2s)(1+R_3C_3s)-(R_1C_1s)(1+R_3C_3s)}$$

$$= \frac{1}{(1+R_2C_2s+R_1C_1s+R_1R_2C_1C_2s^2)(1+R_3C_3s)-(R_1C_1s+R_1R_3C_1C_3s^2)}$$

$$= \frac{1}{1+R_2C_2s+R_1C_1s+R_1R_2C_1C_2s^2+R_3C_3s+R_2R_3C_2C_3s^2+R_1R_3C_1C_3s^2\ldots}$$

$$\frac{1}{\ldots+R_1R_2R_3C_1C_2C_3s^3-R_1C_1s-R_1R_2C_1C_2s^2}$$

$$= \frac{1}{R_1R_2R_3C_1C_2C_3s^3+R_1R_2C_1C_2s^2+R_2R_3C_2C_3s^2+R_2C_2s+R_3C_3s+1}$$

$$\frac{V_2}{V_1} = \frac{1}{R_1R_2R_3C_1C_2C_3s^3+(R_1R_2C_1C_2+R_2R_3C_2C_3)s^2+(R_2C_2+R_3C_3)s+1}$$

The transfer function for the switched-capacitor filter is

$$\frac{V_2}{V_1} = \frac{1}{\dfrac{C_1C_2C_3}{f_c^3C_{R1}C_{R2}C_{R3}}s^3 + \left[\dfrac{C_1C_2}{f_c^2C_{R1}C_{R2}} + \dfrac{C_2C_3}{f_c^2C_{R2}C_{R3}}\right]s^2\ldots}$$

$$\frac{1}{\ldots+ \left[\dfrac{C_2}{f_cC_{R2}} + \dfrac{C_3}{f_cC_{R3}}\right]s + 1}$$

Results of the Improved Switched-Capacitor Sallen and Key Topology with Changed Feedback Path

By changing the feedback path, the circuit showed considerable performance improvement. The Q-enhancement went away and the filter rolloff performance was excellent. With the clock frequency at 589,379 Hz, the filter exhibited a cutoff frequency of 1520 Hz, as seen in Figure 4.6a. When the clock frequency was changed to 438,693 Hz, the filter cutoff frequency changed to 1280 Hz, as seen in Figure 4.6b. Also, when the clock frequency was changed to 247,979 Hz, the filter cutoff frequency changed to 640 Hz, as seen in Figure 4.6c. This demonstrates that varying the clock frequency directly changes the filter cutoff frequency. The clock frequency was changed by changing the RC time constant capacitor in the clock trigger from 361 pF to 485 pF and then to 858 pF, respectively. Figure 4.6d simultaneously shows both the filter cutoff frequency of 1520 Hz due to the clock frequency 589,379 Hz and the filter cutoff frequency of 640 Hz due to the clock frequency of 247,979 Hz. It can be seen that the DC portion of the output of the filter remains constant with only the filter cutoff frequency changing as a result of the clock frequency change.

Figures 4.7a, 4.7b and 4.8 demonstrate the filtering capability of the improved switched-capacitor Sallen and Key third-order lowpass filter section. Figure 4.7a shows in the top trace of the Leader oscilloscope the random noise source of the Hewlett-Packard spectrum analyzer as an input to the switched-capacitor filter set

(a)

VER = 10 dB/cm

HOR = 1000 Hz/cm

(b)
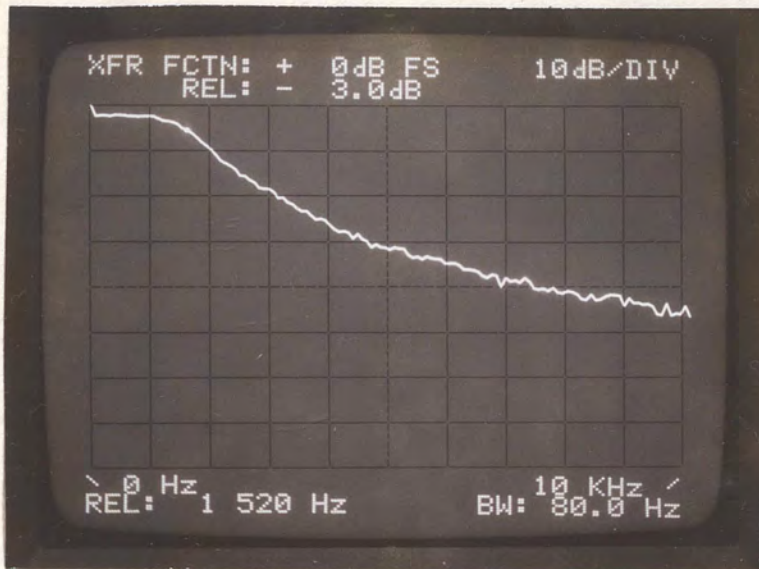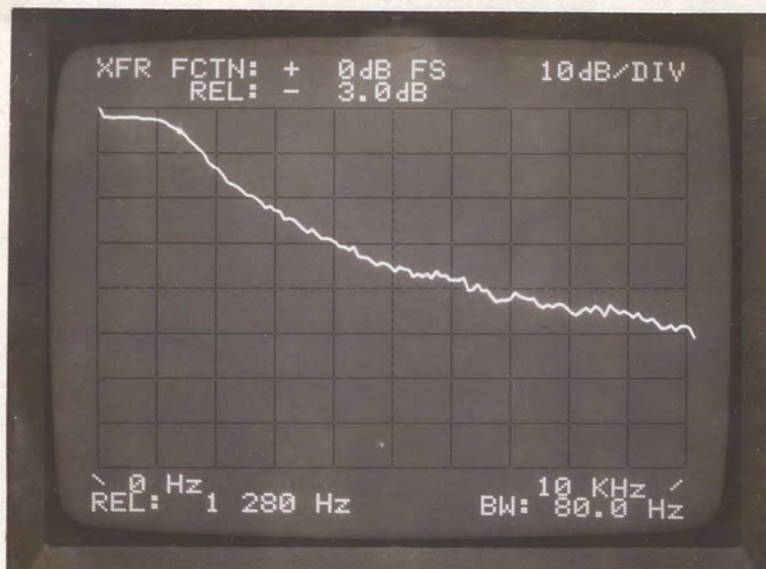
VER = 10 dB/cm

HOR = 1000 Hz/cm

Figure 4.6. Spectrum analyzer photographs of Figure 4.5 improved
switched-capacitor Sallen and Key filter with changed
feedback path frequency response variation with changing
clock frequency.
(a) with clock frequency of 589,379 Hz
(b) with clock frequency of 438,693 Hz
(c) with clock frequency of 247,979 Hz
(d) comparison of filter frequency response and
    cutoff frequency for 589,379 Hz clock frequency
    (upper trace) and 247,979 Hz clock frequency
    (lower trace)
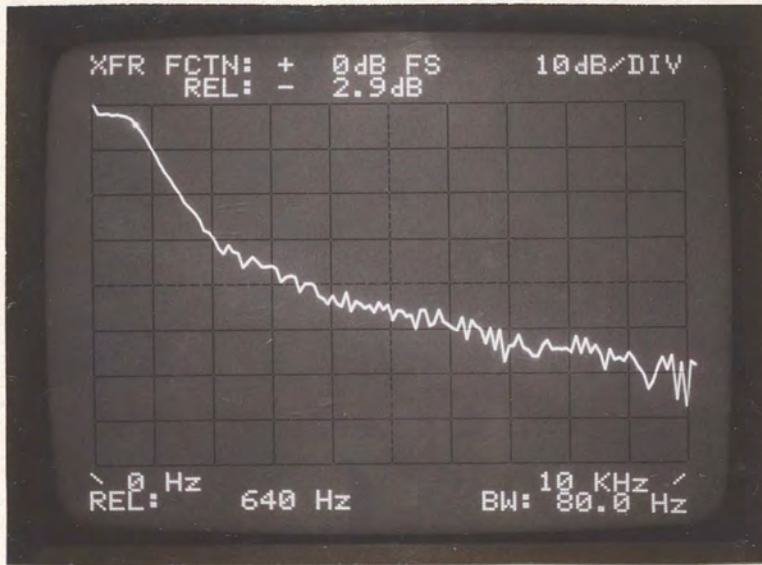
VER = 10 dB/cm

HOR = 1000 Hz/cm

(c)
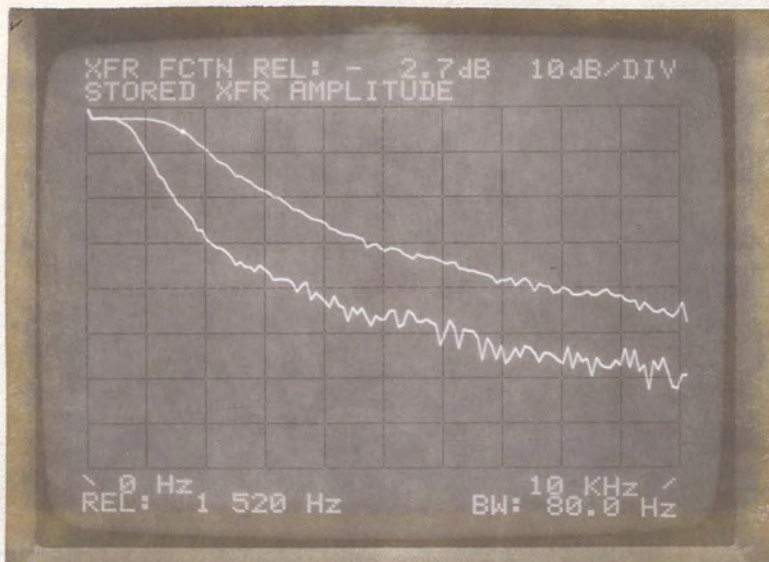
VER = 10 dB/cm

HOR = 1000 Hz/cm

(d)

Figure 4.6.--CONTINUED
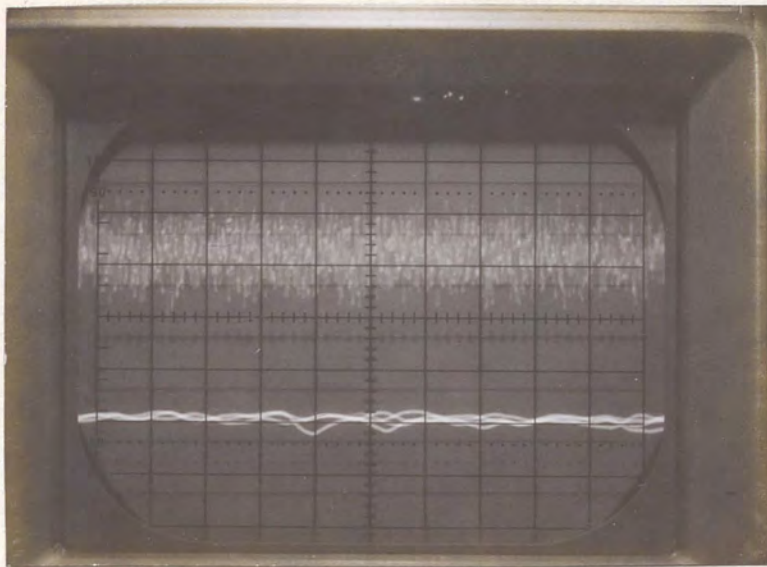
VER = 2 v/cm

HOR = 1 ms/cm

(a)
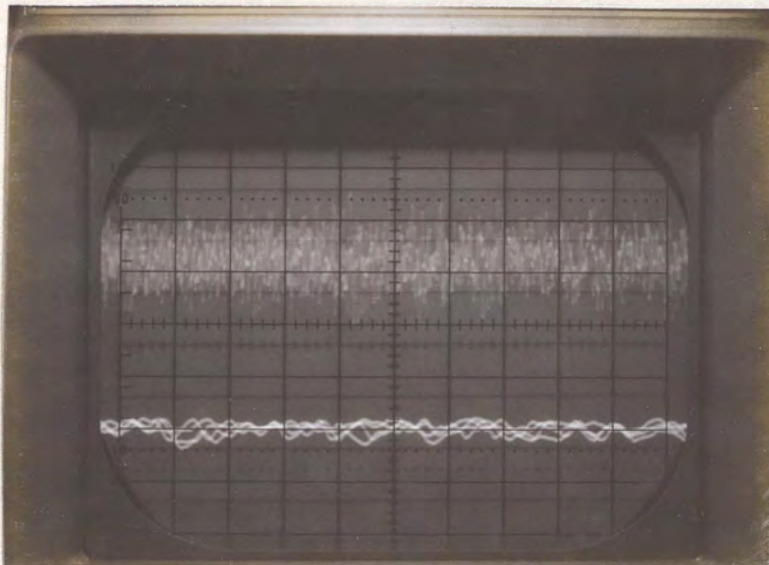
VER = 2 v/cm

HOR = 1 ms/cm

(b)

Figure 4.7.   Oscilloscope photographs of a random noise input
              (upper trace) to the switched-capacitor filter of
              Figure 4.5 and the filter output response (lower trace)
              for different cutoff frequencies.
              (a) with a cutoff frequency of 640 Hz
              (b) with a cutoff frequency of 1520 Hz

up with a cutoff frequency of 640 Hz. The lower trace of the oscilloscope displays the resulting output from the filter. The vertical scale of the oscilloscope is on 2 volts/division and the horizontal scale is on 1 ms/division. Figure 4.7b shows the same random noise source in the top trace as the input to the filter but the lower trace is the filter output with the filter cutoff frequency set at 1520 Hz. Figure 4.7a is seen to give substantial attenuation of the signal due to the low filter cutoff frequency, whereas Figure 4.7b gives less attenuation with the higher filter cutoff frequency. Figure 4.8 shows in the upper trace of the oscilloscope photograph a square wave input from a Model 119 function generator set on 250 Hz. The lower trace represents the reconstructed output of the filter with a cutoff frequency of 1520 Hz. There is seen to be slight overshoot and undershoot on the reconstruction, but little attenuation as desired.

Figure 4.9 is a photograph of the actual breadboard used for the improved switched-capacitor Sallen and Key third-order lowpass filter section with the changed feedback path. Figure 4.10 is the board layout used for the improved switched-capacitor Sallen and Key third-order lowpass filter section with the changed feedback path. The one shot clock and the anti-aliasing filter are not shown but they were the same as shown in Figure 3.12. The MICROCAP simulation circuit of the switched-capacitor Sallen and Key third-order lowpass filter is shown in Figure 4.11. The equivalent resistors for a clock frequency of 589,379 Hz were used in the simulation circuit.
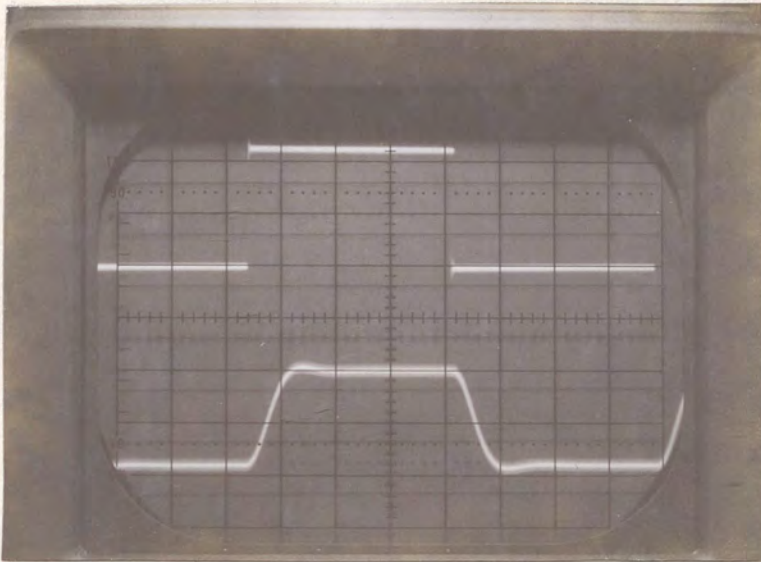
VER = 0.2 v/cm

HOR = 0.5 ms/cm

Figure 4.8.   Oscilloscope photograph of a square wave input at 250 Hz (upper trace) to the switched-capacitor filter of Figure 4.5 at a cutoff frequency of 1520 Hz and the filter output response (lower trace).
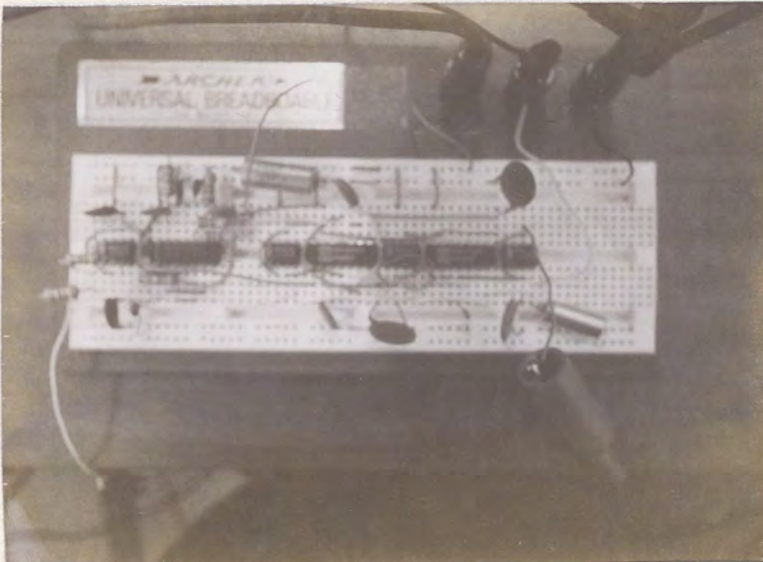
Figure 4.9.   Photograph of the Figure 4.5 switched-capacitor filter breadboard.
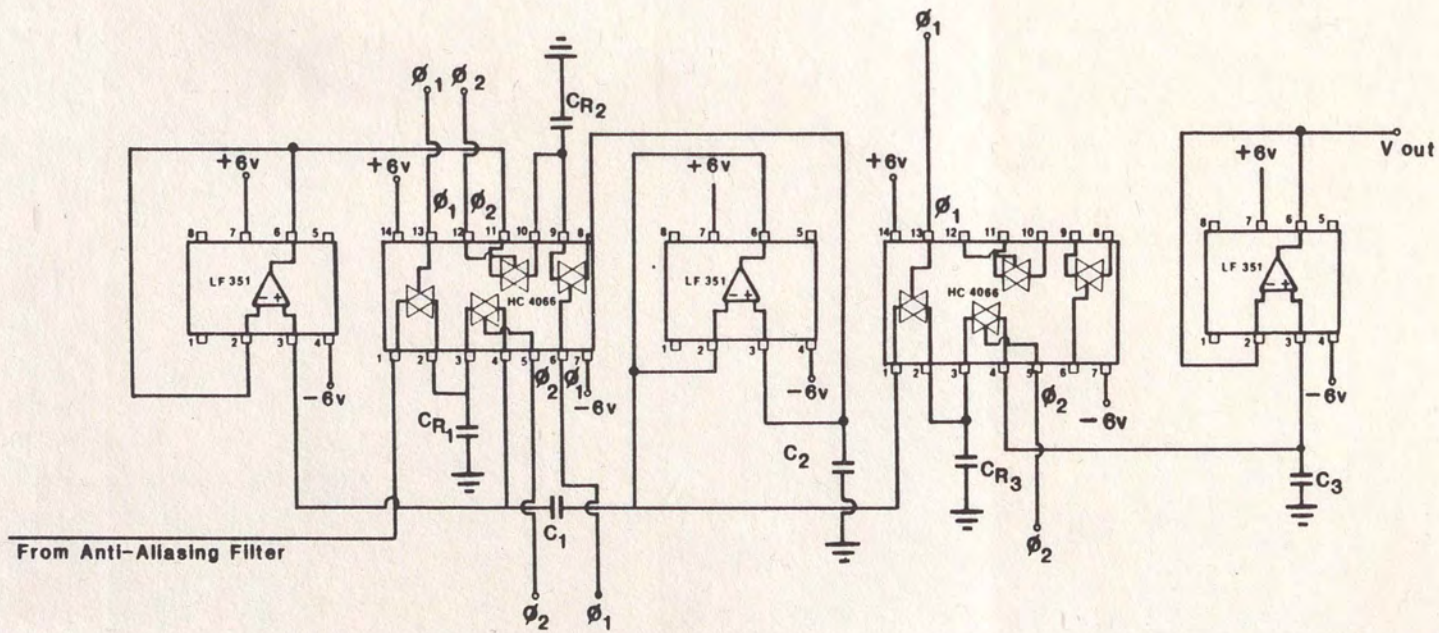
Figure 4.10. Board layout of improved switched-capacitor Sallen and Key third-order lowpass filter section with changed feedback path. One shot clock and anti-aliasing filter (not shown) were the same as shown in Figure 3.12.
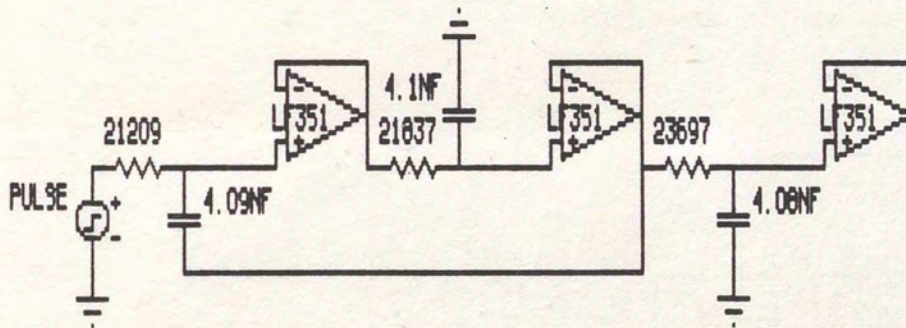
Figure 4.11. MICROCAP simulation circuit of the improved
switched-capacitor Sallen and Key third-order
lowpass filter section.

GAIN   TEMPERATURE= 27   THESIS3   PHASE   DELAY
 DB   DEG   SEC
 0.00   90.0   100US

-16.00   0.0   10US

-32.00   -90.0   1US

-48.00   -180.0   100NS

-64.00   -270.0   10NS

-80.00   -360.0   1NS
  1   25000
                          FREQUENCY IN HZ

FREQUENCY = 250.00000D+02 HZ   GAIN   = -69.302 DB
PHASE ANGLE=-264.480   DEGREES   GROUP DELAY= 120.76087D-08 SEC
GAIN SLOPE =-180.66973E-01 DB/OCT   PEAK GAIN = -0.009DB/F= 100.00000D-02
1:ANOTHER RUN 2:ANALYSIS LIMITS 3:RETURN 4:TITLE

Figure 4.12.   MICROCAP gain (dB) versus frequency (Hz) plot of the
               improved switched-capacitor Sallen and Key third-order
               lowpass filter section.

The MICROCAP gain (dB) versus frequency (Hz) plot is shown in Figure 4.12. The MICROCAP frequency analysis is shown in Figure 4.13, with the cutoff frequency bracketed. The frequency response and cutoff frequency of the MICROCAP simulation match closely with the actual filter frequency response photograph of Figure 4.6a, which was at the same clock frequency as the simulation.

The control of the switched-capacitor Sallen and Key filter could be extended to a programmable selector by which a variety of combinations of capacitor values could be selected to give any clock frequency needed and subsequently any desired cutoff frequency up to the maximum capability of the filter. The need for this capability has been realized in that, while the research for this thesis was going on, two companies have developed frequency programmable switched-capacitor chips and are now marketing them. One chip offers a fourth-order Butterworth lowpass filter, another chip gives a sixth-order Butterworth lowpass filter, and two other chips give choices of performing lowpass, highpass, allpass, bandpass or notch functions and the configurations of Butterworth, Bessel, Cauer, Elliptic and Chebyshev, on a single chip. One chip operates at a 50:1 ratio of the clock frequency to the cutoff frequency. A 50 kHz clock frequency would give a filter cutoff frequency of 1 kHz. The other chip operates at a 100:1 ratio of the clock frequency to the cutoff frequency. Since the maximum recommended clock frequency is 1 MHz, for either chip, the maximum cutoff frequency is 20 kHz for the 50:1 chip and 10 kHz for the 100:1 chip. The clock-to-center

```
                SPECTRUM SOFTWARE
                  MICRO-CAP II
                FREQUENCY ANALYSIS
                      FOR
                 THESIS3 CIRCUIT
             TEMPERATURE= 27 CASE= 1
```

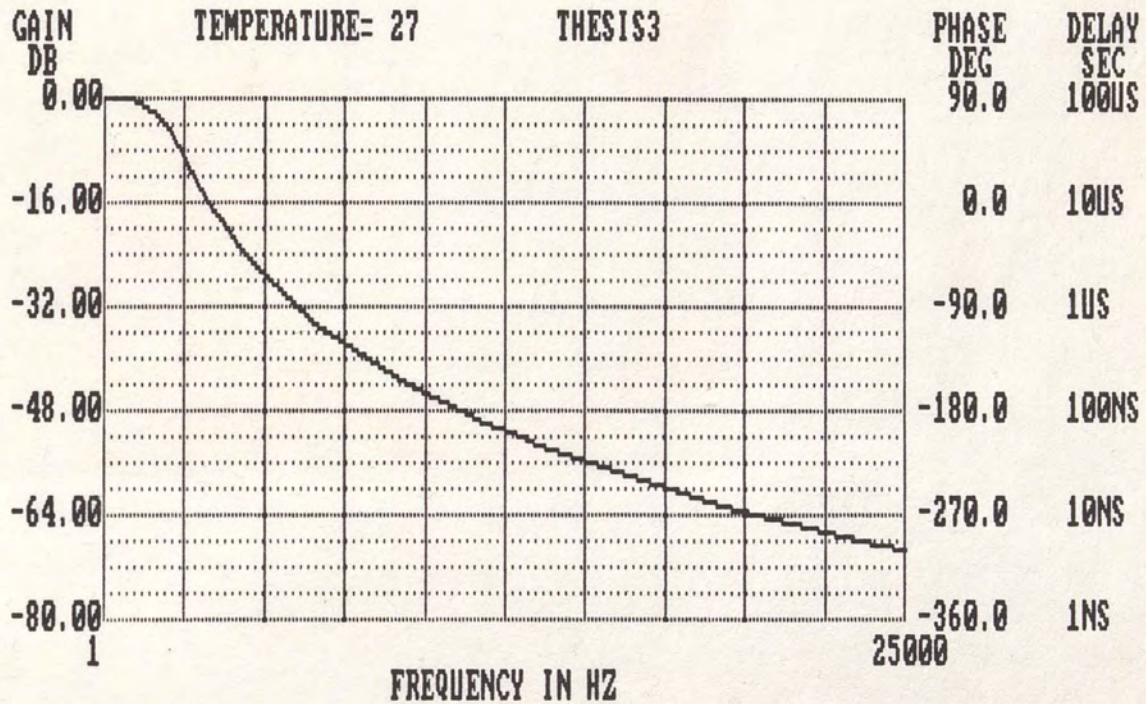| FREQUENCY	GAIN(DB)	ANGLE(DEGREES)	DELAY(SEC)	SLOPE(DB/OCTAVE)
100.00000D-02	-889.90053D-05	-671.33576D-04	120.76087D-08	-180.66973E-01
105.00000D-02	-889.90370D-05	-704.90256D-04	186.48224D-06	-449.50445E-09
115.00000D-02	-889.91049D-05	-772.03614D-04	186.48218D-06	-517.44144E-09
135.00000D-02	-889.92592D-05	-906.30333D-04	186.48222D-06	-667.21338E-09
175.00000D-02	-889.96420D-05	-117.48376D-03	186.48217D-06	-102.23705E-08
255.00000D-02	-890.07039D-05	-171.19066D-03	186.48228D-06	-195.50705E-08
415.00000D-02	-890.40130D-05	-278.60449D-03	186.48235D-06	-470.97024E-08
735.00000D-02	-891.53725D-05	-493.43265D-03	186.48279D-06	-137.75198E-07
137.50000D-01	-895.70550D-05	-923.09240D-03	186.48427D-06	-461.28604E-07
265.50000D-01	-911.62519D-05	-178.24380D-02	186.48994D-06	-167.70278E-06
521.50000D-01	-973.76306D-05	-350.13314D-02	186.51188D-06	-637.99490E-06
103.35000D+00	-121.87074D-04	-694.07236D-02	186.59898D-06	-248.22103E-05
205.75000D+00	-218.37303D-04	-138.32620D-01	186.95466D-06	-971.47925E-05
410.55000D+00	-594.35478D-04	-277.32079D-01	188.52348D-06	-377.23962E-04
820.15000D+00	-226.42229D-03	-567.42283D-01	196.73805D-06	-167.26616E-03
163.93500D+01	-245.05662D-02	-124.33079D+00	381.16964D-06	-222.60041E-02
204.89500D+01	-557.30727D-02	-155.52690D+00	211.56218D-06	-970.44315E-02
245.85500D+01	-932.96381D-02	-178.21209D+00	153.84379D-06	-142.87705E-01
286.81500D+01	-130.01695D-01	-193.84724D+00	106.03263D-06	-165.17521E-01
327.77500D+01	-163.59433D-01	-204.93436D+00	751.89382D-07	-174.35066E-01
368.73500D+01	-193.85664D-01	-213.15367D+00	557.40773D-07	-178.14085E-01
409.69500D+01	-221.17708D-01	-219.49355D+00	429.95067D-07	-179.78006E-01
450.65500D+01	-245.99336D-01	-224.54271D+00	342.41780D-07	-180.51725E-01
491.61500D+01	-268.69143D-01	-228.66752D+00	279.73162D-07	-180.85314E-01
532.57500D+01	-289.58906D-01	-232.10680D+00	233.24121D-07	-181.00117E-01
573.53500D+01	-308.94360D-01	-235.02280D+00	197.75387D-07	-181.05816E-01
614.49500D+01	-326.96369D-01	-237.52972D+00	170.01154D-07	-181.07048E-01
655.45500D+01	-343.81958D-01	-239.71038D+00	147.88576D-07	-181.06028E-01
696.41500D+01	-359.65161D-01	-241.62641D+00	129.93875D-07	-181.03979E-01
778.33500D+01	-388.69234D-01	-244.84137D+00	109.01421D-07	-181.00231E-01
860.25500D+01	-414.81689D-01	-247.43886D+00	880.76769D-08	-180.95163E-01
942.17500D+01	-438.55737D-01	-249.58639D+00	728.19242D-08	-180.90643E-01
102.40950D+02	-460.31266D-01	-251.39553D+00	613.45305D-08	-180.86815E-01
110.60150D+02	-480.38937D-01	-252.94362D+00	524.93172D-08	-180.83641E-01
118.79350D+02	-499.02816D-01	-254.28598D+00	455.17326D-08	-180.80996E-01
126.98550D+02	-516.42137D-01	-255.46329D+00	399.20768D-08	-180.78783E-01
135.17750D+02	-532.72519D-01	-256.50615D+00	353.61585D-08	-180.76939E-01
143.36950D+02	-548.06814D-01	-257.43801D+00	315.98016D-08	-180.75386E-01
159.75350D+02	-576.28263D-01	-259.03816D+00	271.29215D-08	-180.73532E-01
176.13750D+02	-601.73726D-01	-260.36982D+00	225.77324D-08	-180.71575E-01
192.52150D+02	-624.92440D-01	-261.50259D+00	192.05240D-08	-180.70128E-01
208.90550D+02	-646.21527D-01	-262.48405D+00	166.39808D-08	-180.69008E-01
225.28950D+02	-665.89683D-01	-263.34784D+00	146.45014D-08	-180.68140E-01
241.67350D+02	-684.19538D-01	-264.11848D+00	130.65570D-08	-180.67429E-01
250.00000D+02	-693.02449D-01	-264.48047D+00	120.76087D-08	-180.66973E-01

Figure 4.13.   MICROCAP frequency analysis of the improved switched-capacitor Sallen and Key third-order lowpass filter section.

frequency is very accurately controlled, with a typical error of only 0.3%. Temperature stability is very good with a typical clock-to-center frequency ratio temperature coefficient of 15 ppm/^{o}C. The only external components that are needed are the R and C components to set the clock frequency. The power supply voltage can range from 5 volts ($\pm$ 2.5 v) to 14 volts ($\pm$ 7 v).

The switched-capacitor topology used on these chips is modeled after a third-order passive RLC ladder filter. A differential switched-capacitor integrator with an output voltage that is the time integral of the difference of two input voltages is used as a building block for replacement of the capacitor and inductor components of the passive ladder filter.

The various functions are performed by MOS switch selection of the appropriate feedback paths and differential switched-capacitor sections to give the topology needed for a lowpass, highpass, allpass, bandpass or notch functions. The different configurations of Butterworth, Bessel, Cauer, Elliptic and Chebyshev are determined by using the appropriate mathematical approximation to get the order and Q values from the tables to meet the filter requirements. A programmable switched-capacitor chip that gives all the filter types mentioned above and up to eighth-order has just been offered. The way this chip works is the requirements for the filter desired are selected from a software menu by the designer, and then they are stored in an EPROM. The software calculates the filter order and Q values to determine the filter parameters. The parameters are then

used to determine appropriate MOS switch connections for circuit
topology and capacitor values to give the required switched-
capacitor filter. The switched-capacitor building blocks are
modeled after inverting RC op amp biquads. Up to four second-order
building blocks on a chip can be cascaded to give the eighth order
filter.

None of the chips offered use the switched-capacitor Sallen and
Key topology developed by this thesis.

CHAPTER 5

DESIGN PROCEDURE

The design procedure and design equations are shown below.
Using the transfer function of equation (10) and the general form of
the second-order lowpass filter (equation 7b) and setting the
coefficients of the s terms equal gives

$$\frac{1}{Q\omega_o} = \frac{C_2}{f_c} [\frac{1}{C_{R1}} + \frac{1}{C_{R2}}]$$

from which

$$Q = \frac{f_c}{\omega_o C_2} [\frac{C_{R1} C_{R2}}{C_{R1} + C_{R2}}] \tag{12}$$

Setting equal the coefficients of the s^2 terms of equations (10) and
(7b) gives

$$\frac{1}{\omega_o^2} = \frac{C_1 C_2}{f_c^2 C_{R1} C_{R2}}$$

resulting in

$$f_c = [\frac{C_1 C_2}{C_{R1} C_{R2}}]^{\frac{1}{2}} \ 2\pi f_o \quad (f_o \text{ being the desired} \atop \text{filter cutoff frequency}) \tag{13}$$

Substituting $\omega_0 = f_c [\frac{C_{R1} C_{R2}}{C_1 C_2}]^{\frac{1}{2}}$ into equation (12) gives

$$Q = \frac{[\frac{C_{R1} C_{R2}}{C_1 C_2}]^{-\frac{1}{2}} \frac{C_{R1} C_{R2}}{C_{R1} + C_{R2}}}{C_2} \tag{14}$$

From equation (13), the cutoff frequency of the switched-capacitor filter can be designed by setting the clock frequency to a fixed value. From equation (14), the desired Q value of the switched-capacitor filter can be determined by changing the capacitor values. To determine the order of a filter and the Q values for a Butterworth response, use the same procedure as that for a conventional analog filter. The order is given by

$$n \geq \frac{1}{2} \frac{\log_{10} [\frac{10^{.1\alpha} - 1}{10^{.1\beta} - 1}]}{\log_{10} \frac{\omega_s}{\omega_p}}$$

where:

α = stopband attenuation (dB)

β = passband attenuation (dB)

ω_s = cutoff frequency

ω_p = pass frequency

From the order, use the Butterworth tables given in most filter books to get the necessary Q values. Equation (14) can then be used to get the capacitor values. Equation (13) is then used to select the cutoff frequency. If some noise is tolerable in the output of the filter and second-order sections can be used, then the switched-capacitor Sallen and Key second-order lowpass section should be used. If low noise is needed at the filter output or third-order sections are called for, use the improved switched-capacitor Sallen and Key third-order lowpass section with changed feedback path.

CHAPTER 6

CONCLUSION

The Sallen and Key lowpass conventional analog filter has been shown to be not only feasible but highly desirable as a switched-capacitor filter. The improved switched-capacitor Sallen and Key lowpass filter with changed feedback path is an optimum section to use for a switched-capacitor lowpass filter. The low Q means reduced sensitivity to component value variations over other switched-capacitor topologies which allows ease in monolithic design. The Sallen and Key approach minimizes the components required. This results in allowing a monolithic design of smaller size and lower cost. Also, the sections could be cascaded together to form higher order lowpass filters as needed. Although not attempted, it can be expected that this topology could also be used with some variation to give all other filter types, as bandpass, band reject, allpass and highpass, as well as Butterworth, Chebychev and Elliptic filters.

By the use of a bank of capacitors that would be microprocessor selectable, the switched-capacitor Sallen and Key sections could be varied to produce a frequency response from DC to 20 kHz or more on the output, depending in part on the anti-aliasing filter used.

Butterworth, Chebychev, or Elliptic filters could be formed by using a series of CMOS switches that are microprocessor selectable. This would also allow selection of lowpass, highpass, bandpass, bandstop and allpass filters. Higher order responses could also be selected with additional switched-capacitor sections. A monolithic chip could be developed with switched-capacitor Sallen and Key sections that would have the above-mentioned qualities. For monolithic chip layouts, the capacitors could be scaled down to the 0.1 to 50 pF capacitors normally used for monolithic components. The op amps could also be replaced by FETs which require less area on the monolithic chips. Also, with the monolithic chips, the capacitive feedthrough would be negligible.

With a programmable, switched-capacitor filter, anyone who can define a filter's characteristics could design a filter, with a software menu. In addition, the filter's specification can be continuously or completely changed by a host microprocessor or a simple thumbwheel switch.

The programmable switched-capacitor filter gives an engineer both the flexibility of a digital filter and the cost-effectiveness of an analog filter. The filter's capability for reprogramming opens up a variety of new filter tasks. The choices range from realizing filters for spot noise measurement in op amp test systems to controlling the cutoff frequency and the Q of a lowpass filter in a phase-locked loop. In a feedback loop, an external program could

direct the chip to hunt for fixed signals or a family of signals

(Dille et al. 1986).

REFERENCES

Broderson, R.W.; Gray, P.R.; and Hodges, D.A. "MOS
    Switched-Capacitor Filters." Proceedings of the IEEE 67
    (January 1979): 61-75.

Bruton, L.T. "Low Sensitivity Digital Ladder Filters." IEEE
    Transactions on Circuits and Systems CAS-22 (March 1975):
    168-179.

Caruthers, R.S. "Copper Oxide Modulators in Carrier Telephone
    Systems." Bell Systems Technical Journal 18 (April 1939):
    315-317.

Dille, T.; Holberg, D.; and Taylor, R. "Programmable Filter Chip
    and its PC-Based Tools Offer New Analog Solutions." Electronic
    Design (May 29, 1986).

Fettweis, A. "Theory of Resonant-Transfer Circuits and Their
    Applications to the Realization of Frequency Selective
    Networks." Proceedings Summer School on Circuit Theory, 68
    pages, Czechoslovak Academy of Sciences, Prague, June 28-July
    12, 1968.

Fettweis, A. "Theory of Resonant-Transfer Circuits Lecture Notes."
    Nato Advanced Study Institution on Network and Switching
    Theory, Grignano, Italy, August 28, 1968.

Franklin, G.F., and Powell, J.D. Digital Control of Dynamic
    Systems. New York: Addison-Wesley Publishing Company, 1980.

Hostika, B.J.; Brodersen, R.W.; and Gray, P.R. "MOS Sampled Data
    Recursive Filters Using Switched-Capacitor Integrators." IEEE
    Journal of Solid-State Circuits SC-12 (December 1977):
    600-608.

McCreary, J.L., and Gray, P.R. "All-MOS Charge Redistribution
    Analog-to-Digital Conversion Techniques - Part I." IEEE
    Journal of Solid-State Circuits SC-10 (December 1975):
    371-379.

Van Valkenburg, M.E. Analog Filter Design. New York: Holt,
    Rinehart and Winston Publishing Company, 1972.