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Integration of Computer Generated Images with NTSC Video

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INTEGRATION OF COMPUTER GENERATED IMAGES WITH NTSC VIDEO

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ABSTRACT

From the growing field of computer graphics comes the need to combine the computer graphics with video from other sources. Combining video from separate sources creates a problem since both sources are asynchronous to each other. The objective of this research report is to present a hardware design approach that will combine two asynchronous video sources to produce one video picture. The combining of two video sources is called "overlaying." The hardware design described in this report will overlay video from a Digital Equipment Computer PRO-350 with the video from an RS-170 video source. The design approach presented includes system block diagrams and circuit descriptions for a video frame buffer.

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I would like to thank my wife, Sherry, for the many sacrifices that she has made for me while I was away working on this paper and my masters degree. Also, thanks to Elizabeth and Eddie for putting up with me for not being home all the time.

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INTRODUCTION

Integration of Computer Generated Images, CGI, with the National Television Standards Committee, NTSC, style video refers to overlaying video from one source onto the video from another source to produce one image. CGI video refers to graphic images produced by a computer. Video from different sources can be easily overlaid when the sources are in synchronization, SYNC, with each other. Usually the sources are not in SYNC and this is where the problem occurs.

There are two main methods of synchronizing the sources Ciarcia [1]. The first method is called "Frame Buffering." This method works by storing a frame of video in memory and then reading the memory at a time that would make the memory data be in SYNC with the second source. The second method, called "Genlocking," works by using the SYNC signals from one source as the SYNC signals for the second source and therefore, both sources are in SYNC. The "Genlocking" approach can only be used when the source that is to be overlayed has a provision for an external SYNC input built in. Therefore, this method cannot be used on all equipment.

The "Frame Buffering" method can be used any time, but requires hardware for storing the video information and can be expensive. The Genlock approach is used by Commodore [2] to overlay color graphics, produced by their Amiga computer, onto RS-170 video. This system locks the internal video memory of the Amiga to the external RS-170 video. When the internal memory of a computer cannot be controlled another type of system can be used called the Graph0ver 9500 [3]. This system contains a video memory that is written to, via an RS-232 port, by a host computer. The video memory is then locked to an outside video source by the Genlock method. This research paper will focus on a frame buffer method in which the video coming out of the PRO 350 video outputs will be caught in a memory and then locked to a RS-170 video source.

CHAPTER I

SYSTEM OVERVIEW

System Operation

The total system, as shown in Figure 1, consists of two video sources, Special Purpose Hardware (SPH) and a video monitor.

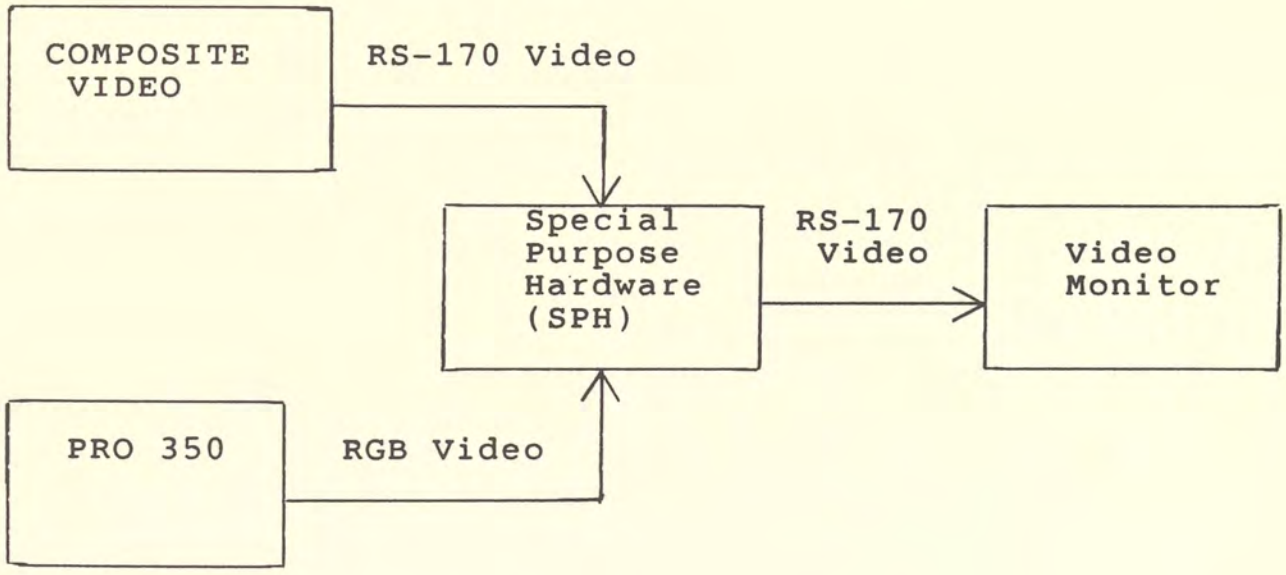


Figure 1. Top level system diagram.

The SPH receives video from two asynchronous sources, overlays them, and then outputs one video picture.

The first video input is composite video in the format specified by the RS-170 video standard for color television Gilbert [4]. The second video input is from a PRO-350 computer and is in an Red-Green-Blue, RGB, video format. The output of the Special Purpose Hardware will be RS-170 video and will be capable of driving a color monitor.

Input/Output Specifications

RS-170 video produces a 525 line picture that is interlaced with one odd field and one even field. Each field has 262.5 lines each and a field rate of 30 Hz. The line frequency is 15,720 KHz. The video signal has a 1 volt peak to peak level with a negative SYNC and drives a 75 OHM load. Black is 0.07 volts and white is 0.7 volts. The blanking level is 0.0 volts and the horizontal SYNC is -0.3 volts. The RGB video has a horizontal line frequency of 15,720 KHz and a field frequency of 60 Hz. The active horizontal time is 51.9 microseconds and contains a maximum of 800 pixels. The active vertical time is 15.5 milliseconds for 240 lines out of a possible 262 lines Meadows [5]. The video is non-interlaced. The SYNC information is on the "green" line and has the same format as the RS-170 video.

The video data is 1 volt peak to peak where black is 0.3 volts and white is 0.7 volts. The design of the SPH will be limited to allowing the RS-170 video to occupy the upper half of the monitor while the RGB video will occupy the lower half of the monitor. This will give the monitor a split screen look. The video memory data will be updated at an 7.5 Hz rate. Also, the color data for the RGB video will be limited to eight colors. The output of the SPH will be in the RS-170 video format.

CHAPTER II

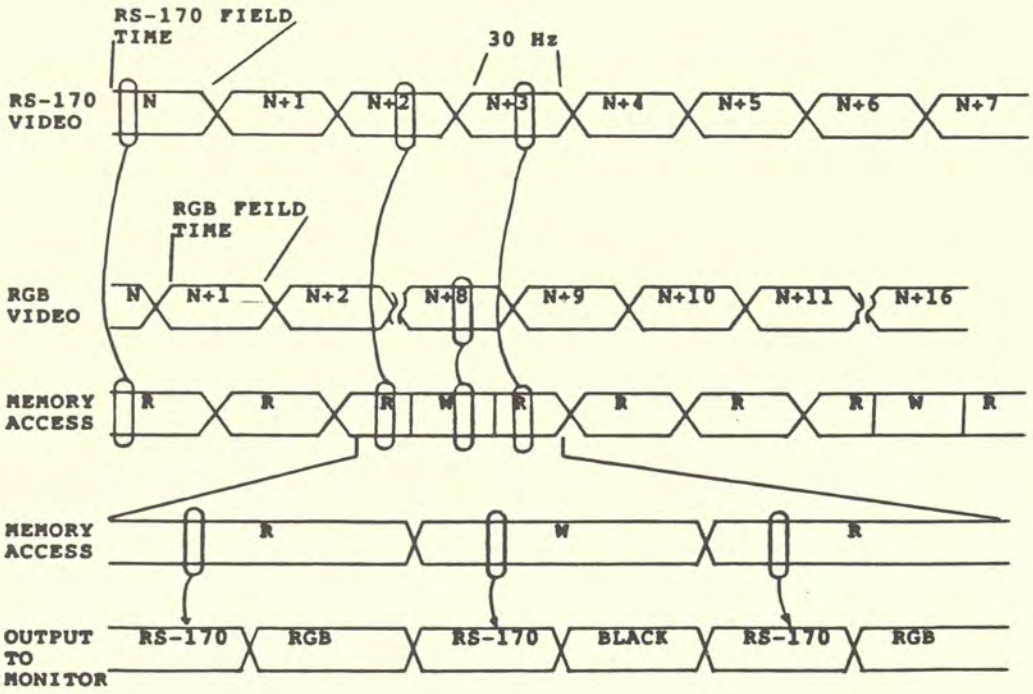
Frame Buffer Theory

Overview

The RS-170 video and RGB video are asynchronous to each other. This means that at a given time the RS-170 video could be on line 130 while the RGB video is on a completely different line or it could be doing a horizontal or vertical retrace. If video from two asynchronous sources were overlaid the resulting picture would roll, jitter, and tear because the vertical retrace and the horizontal retrace would be happening at random times. Therefore, the video sources must be put in SYNC with each other if the video is to be displayed on the same monitor. The purpose of the Frame Buffer is to provide a time delay for the RGB video so that it will line up with the RS-170 video.

The video signals for the RS-170 video and RGB video are made up of fields. The RS-170 field contains 262.5 horizontal scan lines and the RGB video contains 525 lines. The field rate for the RS-170 video is 30 Hz while the RGB video field rate is 60 Hz. It is these

fields that must be synchronized in order to overlay the RS-170 and RGB video signals. At the beginning of every eigth RGB video field time, the video that is output is stored in a memory and held there until the RS-170 video starts outputting a new field. At this point the video memory is read at a 30 Hz rate and the RS-170 and RGB video are lined up and synchronized. Figure 2 shows the timing for this synchronizing process.



NOTE: W = WRITE CYCLE, R = READ CYCLE

Figure 2. System level timing.

Figure 2 shows that the RS-170 video and RGB video signals are not synchronized. This is because the field

times do not line up. The MEMORY ACCESS signal shows that the video memory is read during every RS-170 video field. Therefore, the RGB field data that is read out of the memory is synchronized with the RS-170 video. Figure 2 also shows that the video memory is updated every eigth RGB field time. During this update the color black is output to the monitor.

Once the video is synchronized, all that is needed to overlay the video is to select what horizontal lines of video, from each source, should be output to the monitor. This is done by using an analog switch to select the RS-170 video or the RGB video data that was stored in the video memory. For this design, the first 121 lines of a field that is output will be the RS-170 video and the other 121 lines will be the RGB video from the video memory. Figure 2 shows these outputs to the monitor.

Functional Block

The SPH is made up of six functional blocks which are shown in Figure 3.

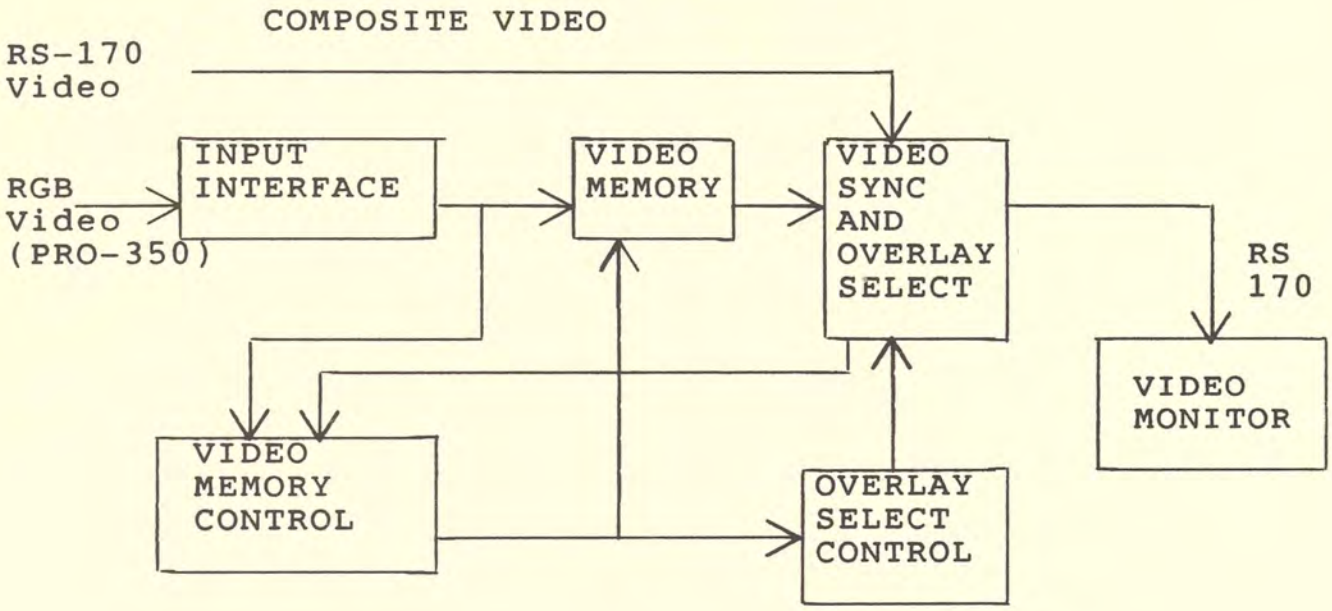


Figure 3. SPH functional block diagram.

The RGB video comes from the PRO-350 and is input to the SPH via the Input Interface block. The RS-170 is input to the Video SYNC And Overlay Select block where the overlay select is done. The combined video is then output to the Video Monitor. The theory of operation for each block is discussed in the following sections.

Input Interface

The Input Interface is used to convert the input RGB video to Transistor-Transistor-Logic, TTL, levels. The PRO-350 RGB levels are 0.3 - 0.7 volts and therefore, cannot be directly interfaced to TTL logic. The amplitude of the voltage level is the intensity of the color. For a voltage level of 0.3 volts the color will have a very low intensity and would display dim. If the voltage level is 0.7 volt then the color will be bright. Since there are many possible colors many voltage levels are possible. For simplicity, the SPH will only deal with eight possible colors. This means eight combinations of red, green, and blue will be used. The interface will convert any RGB input greater than 0.4 volts to a logic 1. This makes the color have either an on or off state. This testing is done by using voltage comparators. When the input voltage is greater than 0.4 volts then the comparator output will go to a TTL level of 1 otherwise the output is a logic 0.

The color states will then be sent to the video memory block for storage. By using only eight colors, three analog to digital converters are saved and a memory reduction of four times is achieved. The memory reduction is due to having to store 1 bit per color

instead of four bits. Four bits per color is used on most computers that have graphic capabilities.

The SYNC information is on the green line and must be stripped off so it can be used as timing information during video memory writes. The SYNC is composite SYNC as specified by RS-170 specifications. The voltage level for blanking is 0.0 volts and the horizontal SYNC is -0.3 volts. The interface logic will convert any voltage that is less than or equal to 0.0 volts to a logic 1. This stripping is also done by voltage comparators. The timing information is then sent to the Video Memory Control block which is used to control the write cycle of the video memory. The interface also provides 75 ohm impedance matching terminations for the RGB lines.

Video Memory

The function of the Video Memory block is to provide the time delay needed to synchronize the RS-170 video and the RGB video signals. The Video Memory contains three separate memories. One for red, green, and blue data. The Video Memory block also contains address counters for storing data and reading data out. The time when the data is written is controlled by the Video Memory Control

block. The data is written into the memory during every eighth RGB field time and read out every RS-170 field time except when for when data is being written into the memory. The timing signals for the read come from the Video Synchronizer And Overlay Control block. The active horizontal line time for the PRO-350 is 51.9 microseconds in which time a maximum of 800 pixels are displayed. This means that the pixel output frequency is 15.4 MHz or 64 nanoseconds per pixel. Each of the pixels must be stored in the video memory, but 64 nanoseconds is a very fast rate for memory write cycles. In order to write the data into the video memory, each pixel that is received is stored in a shift register until a block of 4 pixels are stored. Each pixel block will be stored in one memory address location. This will slow down the video memory write cycle by 4 clocks. Therefore, the data is written into the memory at a rate of 3.85 MHz or 259 nanoseconds per write. The shift register is clocked at a 15.4 MHz rate, which is the same as the pixel rate, in order to catch all the pixel data. Figure 4 shows the input data and the 15.4 MHz clock that catches the data. The pixel data is caught on the rising edge of the 15.4 MHz clock.

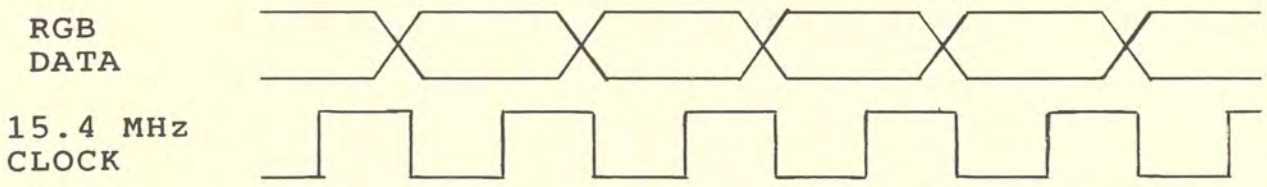


Figure 4. Input data sampling.

The number of active horizontal lines output by the PRO 350 are 240 and since 800 pixels will be stored, the amount of memory required is

memory size/color = 240 lines * 800 pixels/line

= 192,000 bits/color.

Therefore, each color would require 192,000 bits of memory for a total memory of 567,000 bits. In order to save memory, only half of the 240 lines will be stored in memory. This can be done since only half of the video data output by the PRO 350 is needed to be displayed on the monitor. This means that the memory will begin storing data when the PRO-350 is outputting line 121. Also, in order to save memory, the video memory will be updated every eighth field. During the update time no data can be read out of the video memory. This update rate was chosen because the video data that is output by the PRO 350 is assumed to be not changing at a fast rate.

Therefore, the update rate is

video update rate = 60/8 Hz = 7.5 Hz.

The memory requirements for each color are now 96,000 bits or a total of 288,000 bits for three colors.

The video memory for each color is implemented as six 4K X 4 blocks. Address counters are used to generate each pixel block address. The data that is stored in this memory is read out under control of the Video SYNC And Overlay Select block. During the read out time, the same address counters are used to generate the memory addresses. Also, during the read cycle the data is read out based on the RS-170 video timing. The memory data is read out and sent to the Video SYNC And Overlay Select block.

Video Memory Control

The Video Memory Control block is used to control the write cycle of the video memory. The write timing is derived from the SYNC signal that is received from the Input Interface. The video memory is written to every eighth field time and actual memory writes occur when line 121 is being output. This block determines when a new frame and a new horizontal line begins so that each one can be counted. To do this, the vertical blanking

signal is separated from the composite video. This is done by an RC timing network. Since horizontal blanking lasts for 10.9 microseconds and vertical blanking lasts for 1272.26 microseconds then, any pulse, in the composite SYNC, that lasts for more than 10.9 microseconds must be the vertical blanking pulse. These longer pulses are separated and used to indicate when a new frame begins. The vertical blanking pulses are counted and the composite SYNC pulses are counted. When eight vertical pulses and 121 horizontal pulses are received then a flag is set to indicate that it is time to write data in to the video memory for the rest of the field time. From this signal, write enables are generated and sent to the video memory.

Video Synchronization And Overlay Select

The function of this block is to provide the synchronization signals to the video memory during the read cycles and to output the selected video source. The block utilizes a special integrated circuit (IC), the MC1378 Motorola [6]. The MC1378 has the RS-170 video as an input and uses the SYNC information in the RS-170 video to produce timing signals to the video memory during the read cycle. The MC1378 must lock the video

memory read clock to the horizontal SYNC pulses of the RS-170 video. The locking is done by using the RS-170 horizontal SYNC to control a voltage controlled oscillator which in turn generates a 35.8 MHz clock. This clock is then divided to generate the video memory read clock. The 35 MHz clock is also divided by 2275 to produce the horizontal SYNC that is used in the composite video signal sent to the video monitor. Since the video memory read clock also generates the horizontal SYNC then the video memory data being read is synchronized with the incoming RS-170 video. The divide is done by using counters and combinational logic to detect the divide states.

When the RGB data is output from the video memory it is input to the MC1378 and then converted into RS-170 video. Therefore, internal to the IC are two RS-170 video signals. Now all that is needed is to select which video source is to be output. This is done by an input called the video select line. This line is controlled by the Overlay Select Control block. When this line is a logic 1, then the video from the video memory is output, otherwise the RS-170 video is output. The MC1378 contains a fast analog switch which does the video switching. Once the video is selected it is output to

the Video Monitor.

Overlay Select Control

This function is used to select what video is to be output from the MC1378. The select works by counting the occurrence of horizontal lines in the RS-170 video. When the line count is less than or equal to 120 then the RS-170 video will be selected otherwise the RGB video will be selected.

CHAPTER III

FRAME BUFFER DESIGN

Input Interface

This block converts the RGB data to TTL levels and strips the composite SYNC from the Green line. A functional block diagram is shown in Figure 5. As shown in Figure 5, the voltage level conversion is done using voltage comparators. These comparators compare the color input voltage level to a reference voltage level and output a logic 1 or 0 when the input voltage is greater than the reference or less than the reference. Since the video data is changing at a rate of 15.4 MHz fast comparators must be used. A good choice for a comparator is the AM687 made by Advanced Micro Devices. This chip can detect low-level signals of 5 millivolts and has a propagation delay of 15 nanoseconds [7]. The three comparators are set to have a threshold voltage of 0.4 volts for the color converters. One comparator for each color channel is needed. The voltage threshold is set by a resistor divider network.

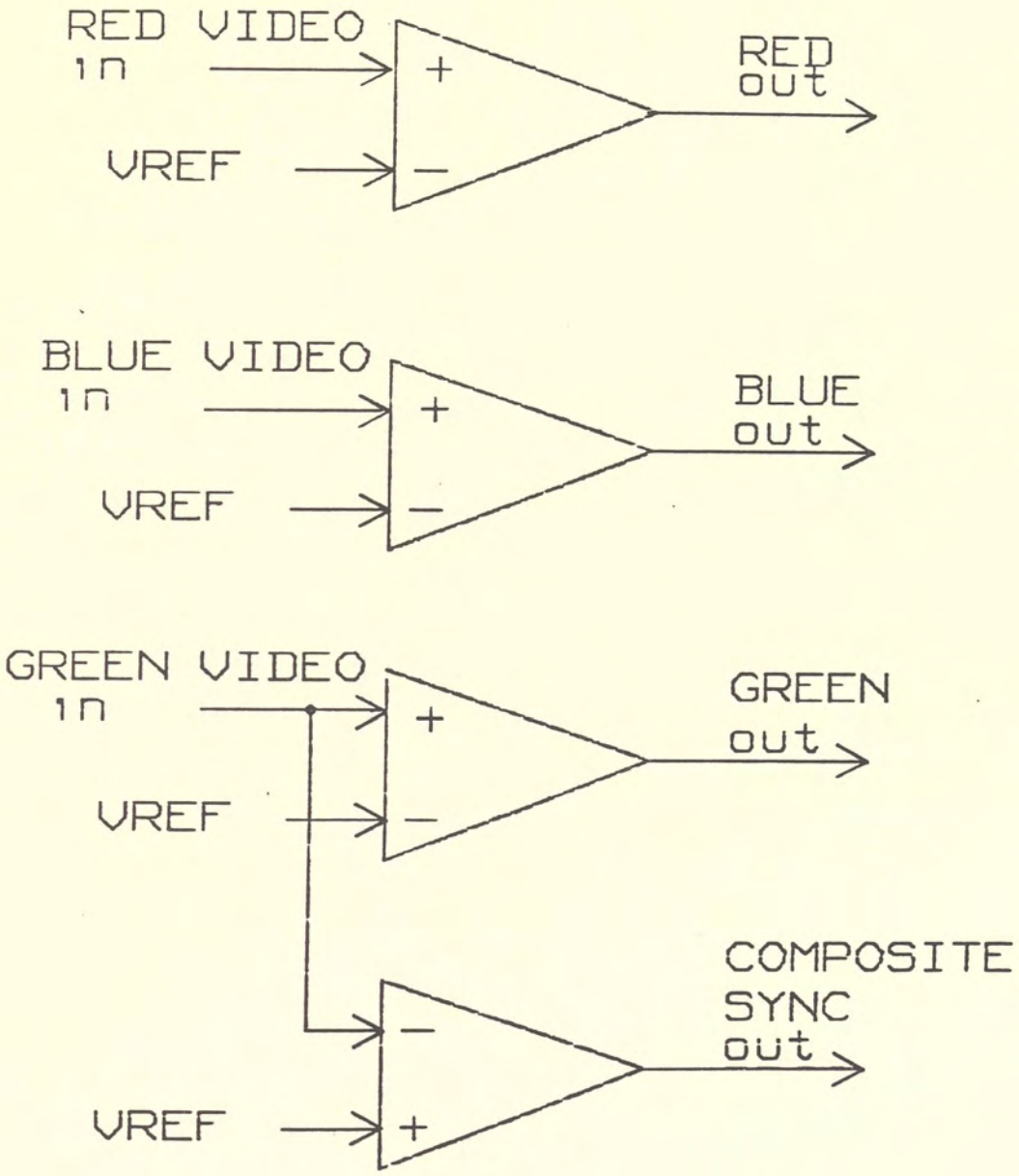


Figure 5. Input Interface block diagram.

The composite SYNC separator is also implemented using the AM687 comparator. The threshold voltage for the comparator is set to zero volts. This is due to the fact that the blanking level is 0.0 volts and the horizontal SYNC is -0.3 volts. Any voltage equal to or less than 0.0 volts will cause a logic 1 to be output by the comparator. This comparator is set up as an inverting comparator because the output goes to a logic 1 when the input voltage is less than or equal to the reference level. The comparator design does not need to include hysteresis since the inputs are fast changing signals. Each of the RGB inputs are terminated with a 75 Ohm resistor for impedance matching.

Video Memory

The functional block diagram of the video memory is shown in Figure 6. As shown in Figure 6, the actual data path in the video memory is repeated three times. This provides one path for each color. The logic that is common to all three sections are the address generation logic blocks. Each Video Memory section contains a 24K X 4 memory, a pixel block register and a shift register.

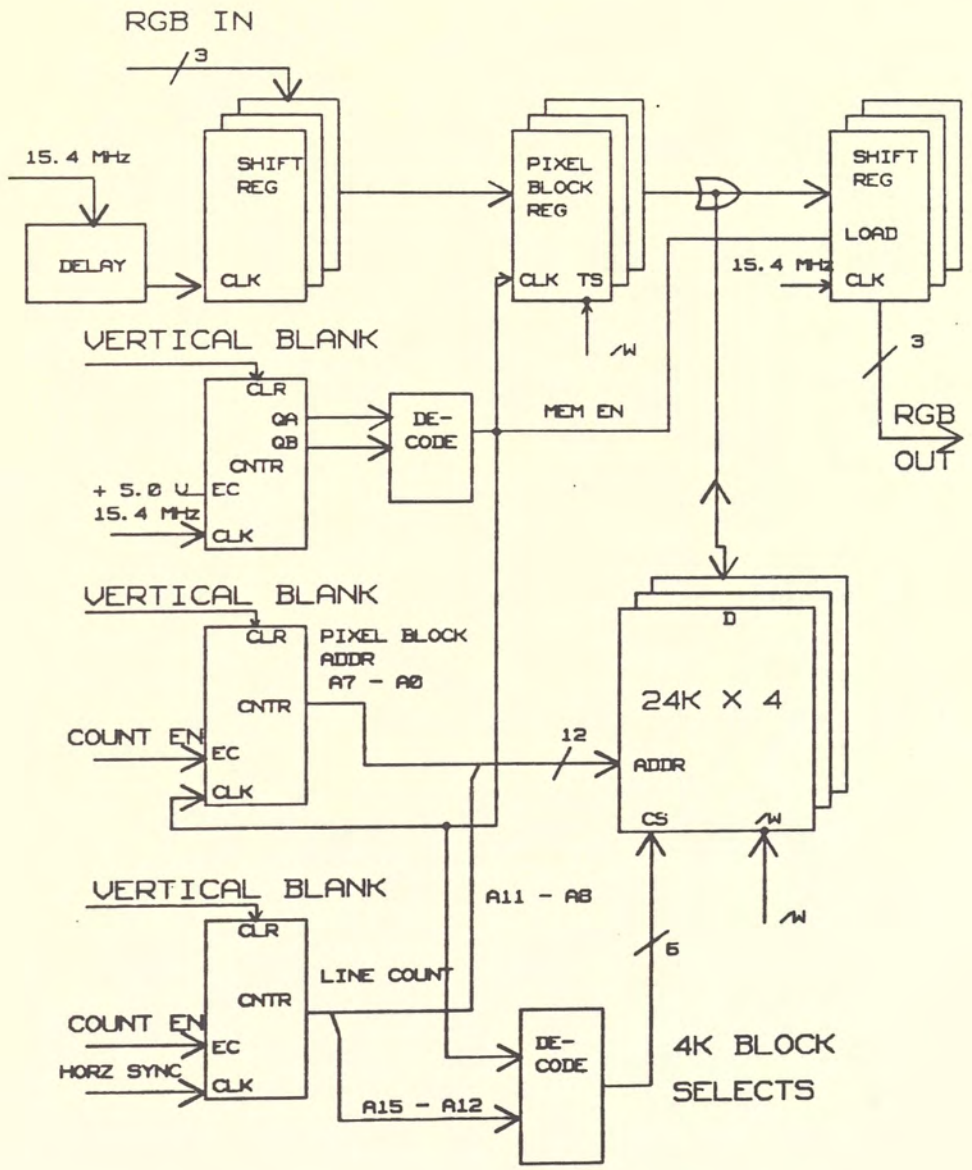


Figure 6. Video Memory block diagram.

Four bits of color data are stored in the shift register. The clock on the shift register is a 15.4MHz clock derived from the MC1378 master clock. The clock goes through an adjustable time delay so that its phase can be manually adjusted. This insures that the clock will catch the incoming data. A 74LS95 4 bit shift register should be used because it can work up to 35 MHz and it uses low power [8]. Once four pixels are loaded into the shift register then the pixel block is transferred to a holding register where it is held until the block is written into the video memory. Note that Figure 6 shows that the holding register is connected to the memory data bus. This means that the holding register must have outputs that are tri-state because during the read cycle the data is coming from the memory and not the holding register. Therefore, the register outputs should only be enabled during the write cycle. This control comes from the Video Memory Control block. A counter and a decoder are used to determine when the pixel block is to be loaded to the holding register. This function is done by counting the shift register clocks. The counter is cleared by the vertical blanking pulse and then it begins to count. When a count of 4 is detected on the counter's output then the holding

register is loaded. The decode is done by ANDing the two lower bits of the counter together. This operation will go on during read and write cycles.

A 74LS163A is used because this counter is clearable and can work at 15.4MHz speeds [9]. The address to the memory is generated by four counters. These counters are used for both read and write cycles. During the write cycles the counters are controlled by the horizontal and vertical SYNC from the PRO 350. During the read cycles the counters are controlled by the horizontal and vertical SYNC signals generated from the RS-170 video signal. This switching is done in the Video Memory Control block. The address counters generate address bits 2E00 - 2E15. The lower 8 address bits are the pixel block address. This means that up to 256 pixel blocks can be stored. The upper eight address bits form the line number horizontal line number. Up to 256 lines of 4 bit data can be stored. For example an address of 0420 would mean pixel block 20 for horizontal line 4. The address counters are cleared at the beginning of each field by the vertical blanking pulse and not enabled to start counting until it is time to write or read the memories. This sets the address back to the first horizontal line. The pixel block address counters

increment every time the pixel block register is loaded.

The line address counters are incremented by the horizontal SYNC pulses. The counters used for this function should also be the 74LS163A counters. The write to the memory will occur when write enables are received from the Video Memory Control block. Otherwise the video memories are being read and the pixel block register is disabled. The memory chips chosen for this memory are IMS1421-40 parts made by INMOS [10]. This chip was chosen for its fast write cycle times and for its 4K X 4 organization. Six of these chips are used for each color for a total of 18 memory chips. Six memory chips are all connected in parallel to produce the memory for one color. Therefore, out of the six only one chip is active at any one time. This is controlled by the chip selects and write enables. These signals are produced in the Video Memory Control block. The four MSB address bits are decoded with a 3 to 8 decoder to produce 4K block selects. These selects are ANDed with the pixel block register load signal to produce a signal that will cause the data to be written into or read out of a particular memory chip. The read or write is done based on the state of the memory write enable. This write enable is generated in the Video Memory Controller.

The pixel block register load signal is used to indicate when a new pixel block is in the pixel block register or when it is time to read out a new pixel block out of the video memory. Each chip has twelve address lines and four data I/O lines. The data lines are used as inputs during write cycles and outputs during read cycles.

When the data that is read out of the memory the four bits are stored in a shift register and then shifted out one at a time to produce a pixel stream. This shift register used is also the 74LS95. The RGB data is then sent to the Video SYNC And Overlay Select block.

Video Memory Control

This block contains the logic that is used to control the Video Memory block. A functional block diagram is shown in Figure 7. There are three main functions to this block. First, the vertical blank signal must be separated from the RGB composite SYNC, secondly the memory write enable must be generated, and third, the RS-170 and the RGB horizontal SYNC and vertical blank signals must be switched so they can be used to control the Video Memory address counters.

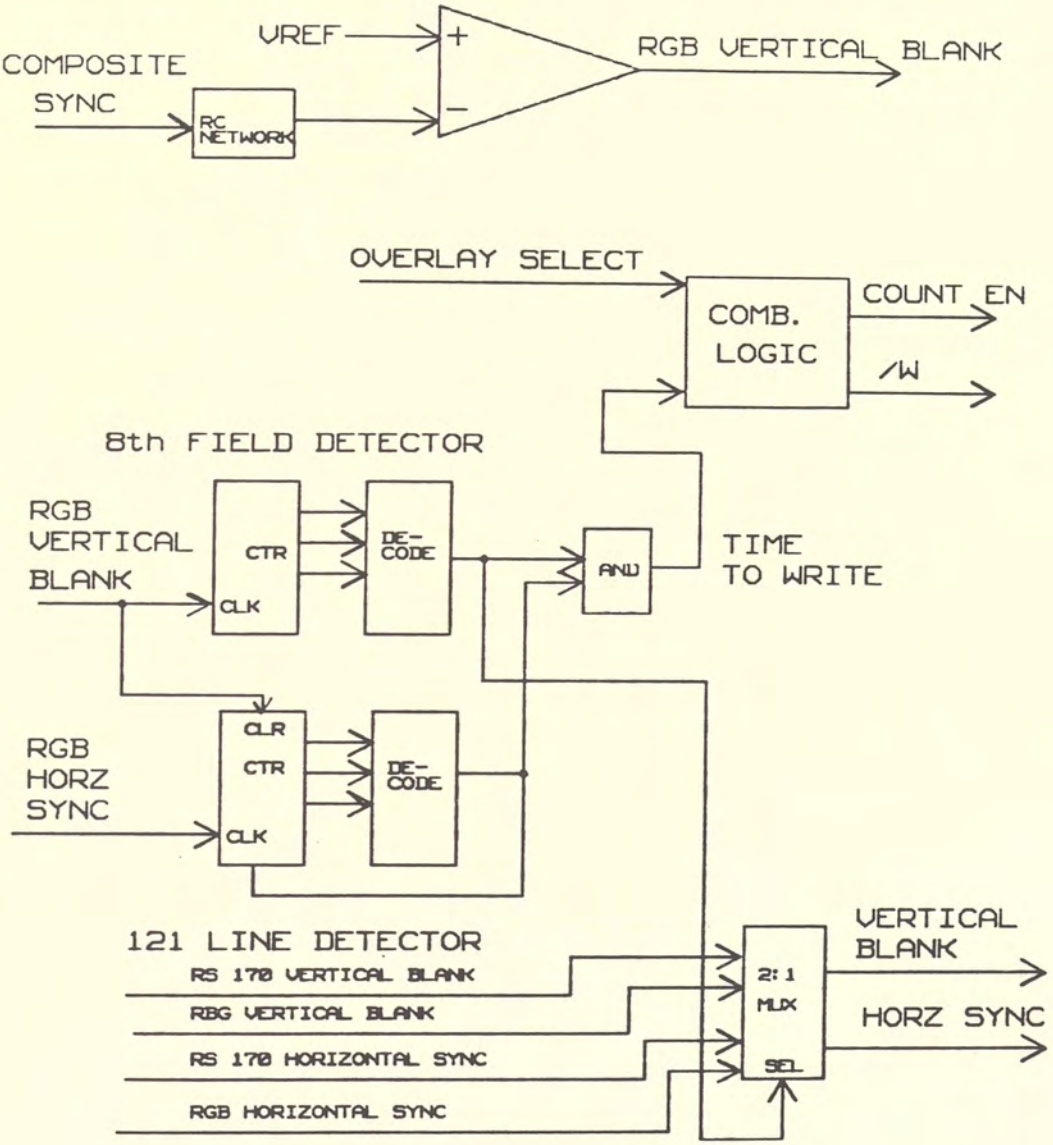


Figure 7. Video Memory Control block diagram.

The function that separates the RGB vertical blank signal from the RGB composite SYNC is shown at the top of Figure 7. The separating is done by checking the length of pulse widths in the composite SYNC. The composite SYNC will be a pulse train made up of pulses for horizontal SYNC and vertical blank signals. The horizontal SYNC pulses will be 10.9 microseconds in width and the vertical blanking pulses are 1272 microseconds in width. Therefore, any pulse that lasts longer than 10.9 microseconds must be a vertical blank pulse. The separation is done using a time delay function made up of a resistor capacitor network and the high input impedance of a voltage comparator. The time delay works by charging a capacitor through a resistor such that the charging pulse must be high for at least 12 microseconds before the capacitor will charge up to the reference voltage level of the comparator. When the vertical blanking pulse is present the capacitor will charge and the comparator output will go low otherwise the output is high.

The logic that generates the memory write enables is shown in the middle of Figure 7. The Video Memory is only written to every eighth RGB field time and when the line count is 121 or greater.

The eighth field detection and line detect is done by counting RGB vertical blank pulses and RGB horizontal SYNC pulses. The RGB blanking pulses are counted using the blanking pulse as the counters' clock. The three lower bits are ANDed together and will go high for every eighth vertical blank pulse. The line count is done by using the RGB horizontal SYNC as the counters' clock. Two counters are cascaded together and their outputs are decoded to produce a high output when line 121 is reached. The two decoder outputs are ANDed together to produce a signal called TIME TO WRITE. When this signal is high then the video memory is put into the write mode. This signal will stay high for the rest of the field time. The TIME TO WRITE will then enable the address counters to start counting and will pull the actual chip write enables low so that memory writes can take place. When a write is not done the TIME TO WRITE signal will force the chip write enables high to indicate that a read cycle is being done. The address counters will then be enabled to start counting when an overlay select signal is received from the Overlay Select Control block.

The third function of this block is the horizontal SYNC and the vertical blank select. This select is needed so the memory address counters can be in SYNC with the RGB video during write cycles and in SYNC with the RS-170 video during the read cycles. This function is done using a mutiplexer whose control is the eighth-field-detect signal. When the PRO 350 starts outputting the eighth field the mutiplexer will switch and send the memory address counters the RGB vertical blank and horizontal SYNC signals. The blanking pulse will clear the address counters and then they will start counting when they are enabled by the TIME TO WRITE signal. When it is time to read the RS-170 video signals are selected. This function is shown at the bottom of Figure 7.

Video SYNC And Overlay Select

The functional block diagram is shown in Figure 8. As shown in Figure 8 this block uses the MC1378 IC. The MC1378 has two video inputs, one for the RGB video and one for the RS-170 video, and one video output. The video output is the overlayedd video in the RS-170 video format. The RGB video input signals come from the video memory and have a level of 5 volts. The MC1378 can only

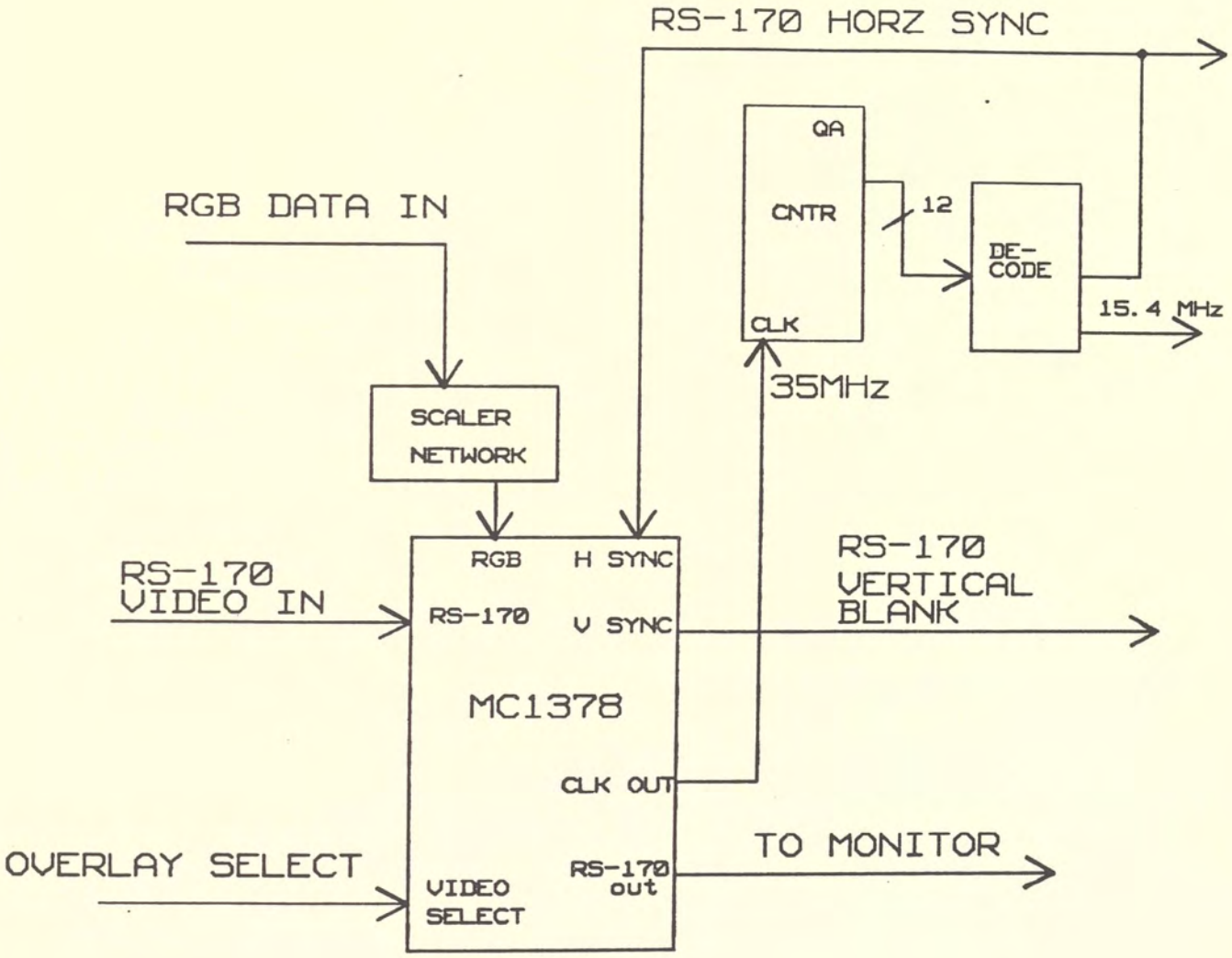


Figure 8. Video SYNC And Overlay Select block diagram.

accept a voltage of 1.0 volts or less and therefore, the RGB signals are translated from TTL levels to 1.0 volts or less by a resistor divider network.

The SYNC signals from the input RS-170 video is used internal to the MC1378 to produce a 36MHz clock that is locked to the SYNC signals. This clock is then divided to form the clock that is used in the Video Memory Control and the Video Memory blocks. The clock is also divided by 2275 to produce the horizontal SYNC for the input RS-170 video. This SYNC is then fed back into the IC to produce the vertical SYNC. The horizontal and vertical SYNC are then used to control the video memory address counters during read cycles. The SYNC signals are also used in the Overlay Select Control block. The MC1378 gets an input from the Overlay Select Control block which is the overlay select signal. This signal selects which video source should be output. When it is a high level then the RGB video is selected, when low the RS-170 video is selected. The video switching is done internal to the MC1378 by a fast video switch. The color encoding for the RGB data is also done internal to the MC1378. The output video is then sent to the Video Monitor. The MC1378 video output is strong enough to drive a monitor directly.

A detailed description of the MC1378 and a suggested circuit design is given by Motorola [6].

Overlay Select Control

The function of this block is to control when the overlay is to take place. For this project, the overlay takes place when the RS-170 video is outputting line 121 or greater. Therefore, this function is designed using a counter that counts the occurrences of RS-170 horizontal SYNC pulses. When the count reaches 121 then the overlay select line is sent high to select the RGB video. If the video memory is in a write cycle then no video will be output. The line counter is reset by the RS-170 vertical blanking pulse. The block diagram for this function is shown in Figure 9.

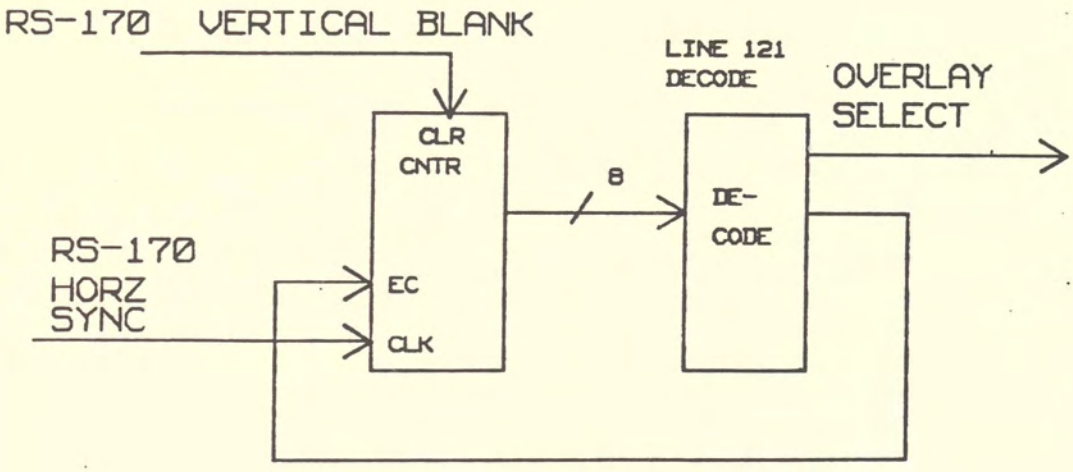


Figure 9. Overlay Select Control block diagram.

CHAPTER IV

CONCLUSIONS AND RECOMMENDATIONS

The frame buffer method presented is a very good method of synchronizing two video sources when it is not possible to modify a piece hardware. This method, however, is the least desirable of the two methods for video synchronizing. This is due to the amount of hardware needed for the frame buffer method.

A major problem with the design presented here is that the video memory is updated at a 7.5 Hz rate and that the memory does not output data during write cycles. This slow update rate means that the video data produced by the PRO 350 should not contain motion that is faster than 7.5 Hz. The slow update rate and the problem of reading and writing at the same time can be solved be making the video memory into a ping/pong memory. This will will allow the video memory to be updated at a 60Hz rate.

The hardware presented for this design only stores half of the video coming from the PRO-350. An improvement would be to increase the memory size so that all the video could be stored. This would make this frame buffer more general.

If the memory size is to be increased then dynamic memories should be used. This will allow a dense memory to be made with just as many memory chips as are used now. The only draw back is to design the refresh control circuits. Another improvement could be to do a pixel by pixel overlay instead of a line by line overlay. This is done by controlling the overlay select with a pixel pattern that is stored in a memory. The memory can be added to the overlay select control logic. The overlay select on the MC1378 can accept an analog input and therefore, the chip could be used to do fading as well as overlaying.

If the hardware described in this report is to be built care must be taken when considering the board layout. The video lines should be kept away from logic paths and clock lines to insure that noise pick up is minimal. The clock strings should flow in one direction and be terminated at the end with a 150 OHM resistor. This keeps reflections at a minimum. The power lines should be decoupled with 0.01 microfarad capacitors to filter out high frequency noise.

When planning to build this hardware, a fair amount of debug time will be needed. The circiutry is very sensitive and may require tweaking.

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