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A Signal Conditioner for Speech Processing

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A SIGNAL CONDITIONER FOR SPEECH PROCESSING

BY

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THESIS

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ABSTRACT

This thesis describes the design, implementation and testing of an analog signal conditioner for use in processing of speech signals. The signal conditioner provides gain and bandwidth control for the speech signal and also indicates the signal level. It is designed to be used in conjunction with a digital speech processor and has ports for a microphone or other signal source, an input signal monitoring device such as an oscilloscope, and interfaces to the digital speech processor. Signal bandwidth control is provided by a variable cutoff frequency lowpass switched capacitor filter, which is driven by a clock. In this thesis, the speech signal is examined and is related to the problem at hand. An overall description of the signal conditioner is then presented, emphasizing each of the individual building blocks in the system. A description of switched capacitor filter theory and application follows, and signal conditioner system test results and conclusions are given. It was found that the system performance satisfied the desired specifications that were laid out when the system was first conceived.

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CHAPTER I

INTRODUCTION

The Speech Signal and Its Properties

In most engineering applications, the speech signal is modeled as a series of quasi-periodic impulses or a noise source that excites the vocal tract, which runs from the glottis in the center of the larynx to the lips. The quasi-periodic impulses correspond to the pulsed vibrations of the vocal folds that are characteristic of voiced sounds, such as vowels; the noise source corresponds to the unvoiced sounds, such as "s," "f," "k," or "p," which are caused by a build-up and release of air pressure in the vocal tract cavities, or the forcing of air through constricted vocal tract pathways. The speech signal is equal to the convolution of the vocal tract excitation signal and the vocal tract impulse response, as the system diagram in Figure 1 illustrates.

In Figure 1, e(t) is the vocal tract excitation, v(t) is the vocal tract time-domain characteristic function (impulse response), and s(t) is the speech signal. The time and frequency domain representations of the signals are shown. In the frequency domain, the vocal tract transfer function, $V(\omega)$, contains peaks that correspond to the resonant frequencies of the vocal tract. The vocal tract can be thought of as an acoustic

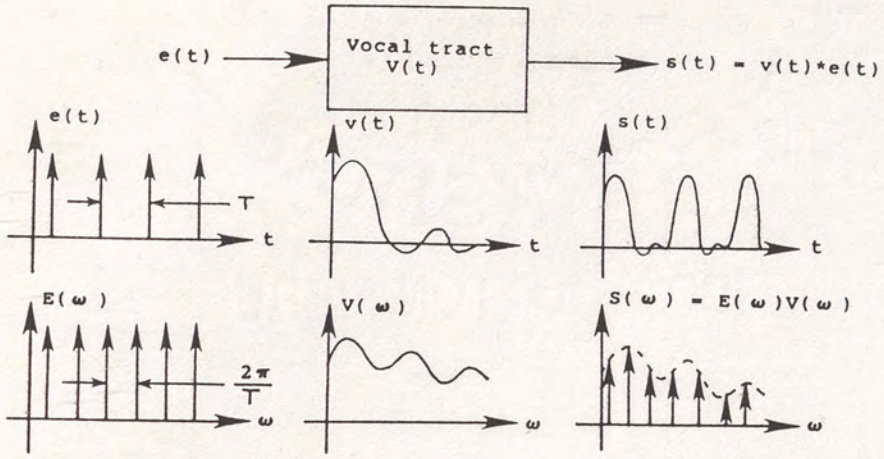


Figure 1. System representation of speech signal (Oppenheim 1978).

tube, with critical or resonant frequencies dependent on the size and shape of the tube. These resonant frequencies are called formant frequencies. Every sound in voiced speech, such as the short "a" in "hat" or the long "e" in "beet," has its own characteristic vocal tract shape and its own set of formant frequencies. The transfer function, $V(\omega)$, then, is determined by the particular sound being spoken, since the formant frequencies of the spoken sound define the shape of the transfer function. Shown in Figure 2 is the vocal tract transfer function for the voiced vowel "AE" (short "a"). Table 1 shows the first three formant frequencies for several voiced vowel sounds.

The vocal tract excitation signal for vowels is a series of pulses separated by a time period, T, referred to as the pitch period. In the frequency domain, the vocal tract excitation

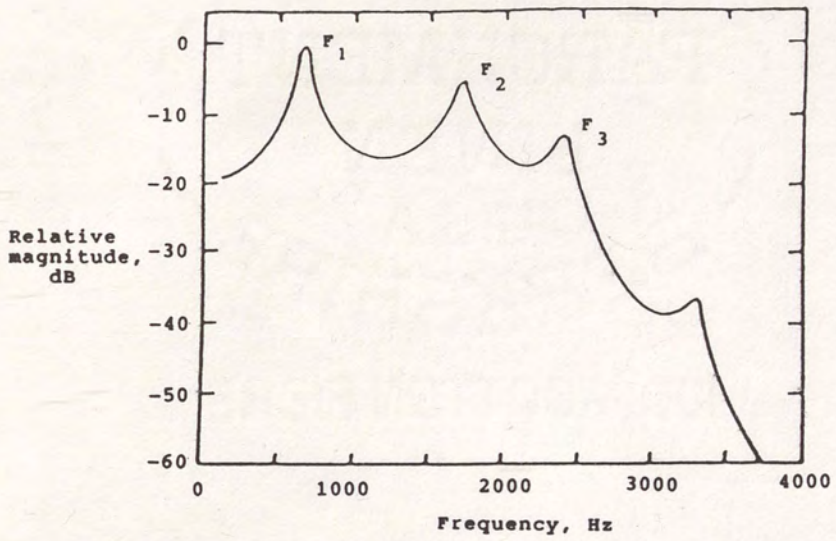


Figure 2. Vocal tract transfer function for the voiced vowel sound "AE" (short "a").

TABLE 1

FORMANT FREQUENCIES FOR SEVERAL VOICED VOWELS

VOWEL	TYPEWRITTEN SYMBOL FOR VOWEL	TYPICAL WORD	FIRST THREE FORMANT FREQUENCIES F_1 (HZ)	F_2 (HZ)	F_3 (HZ)
long "e"	IY	beet	270	2290	3010
short "e"	E	bet	530	1840	2480
long "o"	OO	boot	300	870	2240
short "o"	A	hot	730	1090	2440
short "u"	UH	but	520	1190	2390
short "i"	I	bit	390	1990	2550

SOURCE: Rabiner and Gold (1975)

signal is represented by a series of impulses (discrete frequencies) separated by $2\pi/T$, the pitch frequency. The speech signal is equal to the convolution of the vocal tract excitation and the vocal tract impulse response in the time domain, or the product of the excitation spectrum and the vocal tract transfer function in the frequency domain. Figure 3 shows the spectrum for the voiced vowel in Figure 2, with a pitch period of 0.005 sec.

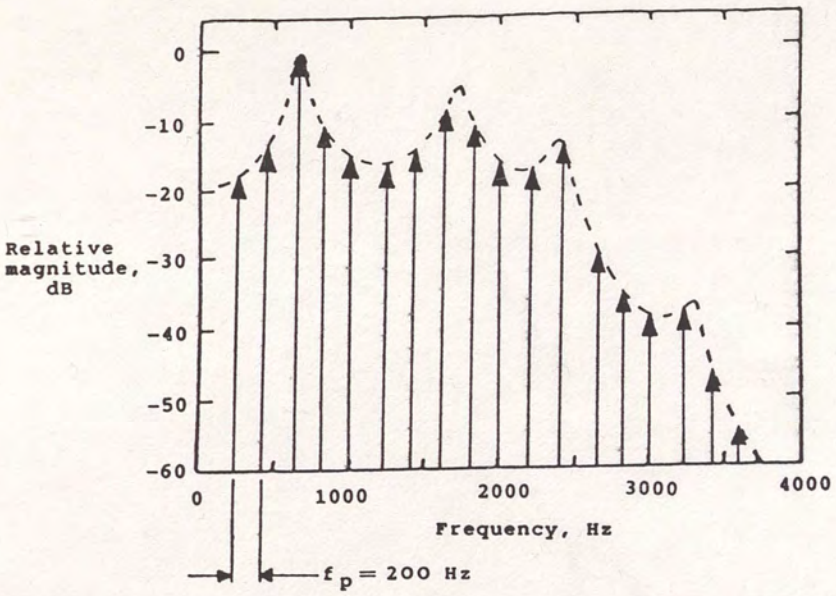


Figure 3. Spectrum for the voiced vowel in Figure 2, with a pitch period of 0.005 sec.

Figure 3 gives good insight into how speech signals in general behave in the frequency and time domain. What Figure 3

represents is a series of harmonics (sinusoids) separated by the pitch frequency, f_p, whose amplitudes are determined by the vocal tract transfer function. The engineering model of the speech signal, then, is a series of discrete sinusoids whose amplitudes are distributed according to the vocal tract transfer function, which in turn is defined by the formant frequencies.

In human speech, different sounds, both voiced and unvoiced, with varying pitch harmonics, are combined sequentially to form words. This means that the speech signal spectrum will change over time, often fairly rapidly. Therefore, the time-domain speech signal cannot be analyzed using conventional Fourier transform techniques. To analyze speech signals, the short-time Fourier transform is used (Oppenheim 1978). In the short-time Fourier transform, the speech signal is assumed to be a sampled signal represented by a sequence, s(n). It is defined by:

$$s(\omega,n) = \sum_{k=-\infty}^{\infty} s(k)h(n - k)e^{-j\omega k} \qquad (1)$$

Here, s(k) is the sampled speech function and h(n - k) is a window function centered about k = n. $S(\omega,n)$, then, is basically the Fourier transform of a windowed portion of the speech signal, s(k), as the window moves along the k-axis in time. It is apparent that equation (1) is simply a convolution of the speech signal (modulated by $e^{-j\omega n}$) and the window function, h(n).

$$s(\omega,n) = [s(n)e^{-j\omega n}]*h(n) \tag{2}$$

In the frequency domain, though, the speech signal is represented by a series of discrete frequencies (see Figure 3). This means that the short-time Fourier transform of a speech signal can be computed using the discrete Fourier transform (DFT). Specifically, if $\omega = 2\pi r/N$, $r = 0, 1, \ldots, N-1$, then:

$$S(\omega,n) = \sum_{k=-\infty}^{\infty} s(k)h(n-k)e^{-j\frac{2\pi}{N}rk} \quad ; \; k = \ell+n, \; n = k-\ell \tag{3}$$

$$S(\omega,n) = \sum_{\ell=-\infty}^{\infty} s(\ell+n)h(-\ell)e^{-jr\left[\frac{2\pi}{N}\ell + \frac{2\pi}{N}n\right]} \tag{4}$$

$$= e^{-j\frac{2\pi}{N}rn} \sum_{\ell=-\infty}^{\infty} s(\ell+n)h(-\ell)e^{-j\frac{2\pi}{N}\ell r} \tag{4a}$$

$$= e^{-j\frac{2\pi}{N}rn} \sum_{m=-\infty}^{\infty} \sum_{\ell=mN}^{mN+N-1} s(\ell+n)h(-\ell)e^{-j\frac{2\pi}{N}\ell r} \tag{4b}$$

$$S(\omega,n) = e^{-j\frac{2\pi}{N}rn} \sum_{k=0}^{N-1} \sum_{m=-\infty}^{\infty} s(n+k+mN)h(-k-mN)e^{-j\frac{2\pi}{N}rk} \tag{5}$$

Equation (4b) is equation (4a), with the summation broken up into equal intervals of length, N; equation (5) results from changing the order of summation in equation (4b) and taking advantage of

the periodicity of $\exp[-j(2\pi/N)\ell r]$. Equation (5) is the discrete Fourier transform of the inner sequence:

$$\tilde{s}(k,n) = \sum_{m=-\infty}^{\infty} s(n + k + mN)h(-k - mN)$$

Thus, the short-time Fourier transform of a speech signal can be determined by sampling the speech signal over the range of the window function, dividing this sequence up into equal intervals of length, N, computing $\tilde{s}(k,n)$ for these intervals, and calculating the N-point DFT of $\tilde{s}(k,n)$. The N-point DFT can be calculated quickly and efficiently using the fast-Fourier transform (FFT), which is essentially an optimized computer program implementation of equation (5). The FFT is used extensively in the processing of speech signals because of its adaptability to digital signal processing methods.

The Research Problem

The main goal of this project is to come up with a method of pre-conditioning an audio speech signal so that it can be processed properly and efficiently by a digital speech processor. The characteristics of the speech signal required to meet this objective are determined by the properties of the digital speech processor itself, and the end results desired from the speech processing. To illustrate this point, it is helpful to examine the basic properties of the digital speech processor.

A digital speech processor consists of an analog-to-digital (A/D) converter, digital circuitry that manipulates the digitized speech signal and a digital-to-analog (D/A) converter. The A/D converter quantizes the input analog speech signal into discrete levels, and then converts these levels into digital words. To do this, the A/D converter samples the time domain analog input signal and holds at this value until a full digitizing cycle is completed. When a digital word representing the analog value is generated, the A/D converter samples the input signal again and holds at the new value until the new digitizing cycle is completed, and so on. The sampling rate of the A/D converter is governed by the Nyquist criterion, which states that:

$$f_s > 2W \tag{6}$$

where f_s is the sampling frequency of the A/D converter and W is the bandwidth of the speech signal. If equation (6) is violated, aliasing of the input signal will occur. In other words, the bandwidth of the input speech signal must be limited to one-half the sampling rate of the A/D converter to avoid aliasing errors. Therefore, any pre-conditioning that is done on the speech signal must include some sort of bandwidth control. The digital speech processor may have an antialiasing lowpass filter built in, which bandlimits the input speech signal, or it may not. It may have a variable sampling rate that is dependent on the processing

circuitry, or it may have a feature where narrow bandwidth speech signals are digitized and processed more quickly than wide bandwidth speech signals. In these cases, the signal conditioner should have a variable bandwidth control, i.e., a variable cutoff frequency lowpass filter.

In addition to bandwidth control, a speech signal conditioner should have a gain control that allows the signal level to be adjusted to a value that takes full advantage of the A/D dynamic range without "overdriving" the A/D converter. To illustrate this point, consider a sinusoidal signal input into an A/D converter, with an amplitude that is a little bit less than two quantizing level increments. As shown in Figure 4, this small-amplitude sine wave will be quantized and digitized in the A/D converter as a square wave with an amplitude equal to two quantizing level increments.

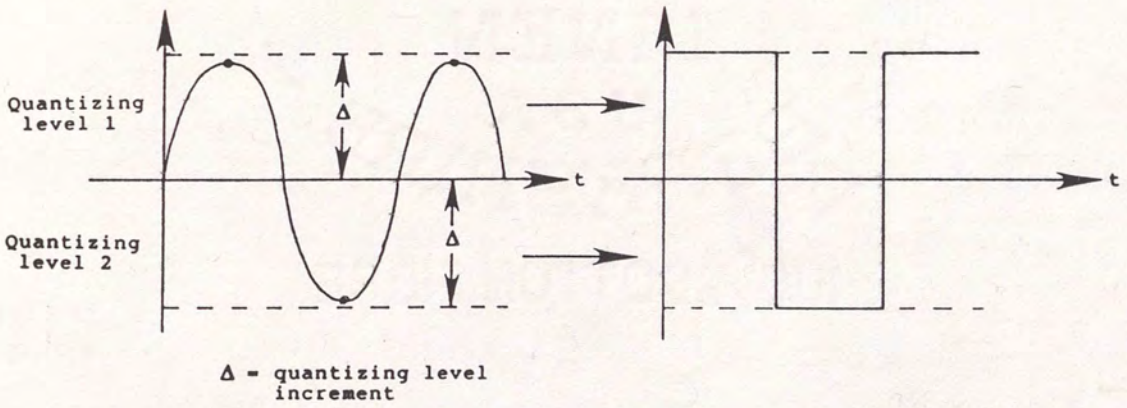


Figure 4. (a) Small signal sine wave with amplitude slightly less than two quantizing level increments, centered about the quantizing threshold, (b) Output of A/D converter with signal in (a) as input (Oppenheim 1978).

The quantizing noise (the difference between the actual signal level and the quantized signal level) is very large here; the output signal to quantizing noise ratio, therefore, is very low. This means that the quantized signal will be a poor representation of the actual signal (Shanmugam 1979). This can be illustrated mathematically as follows (Rabiner and Schafer). The output signal to quantizing noise ratio can be written as:

$$SNR = \frac{E\{x^2(n)\}}{E\{e^2(n)\}} \tag{7}$$

where x(n) is the unquantized signal sample, e(n) is the quantization error or noise, $E\{x^2(n)\}$ is the signal power, and $E\{e^2(n)\}$ is the noise power. If the noise is assumed to be uniformly distributed over the quantization interval, which is the case for sampled speech signals if the quantization interval is small, the noise power becomes:

$$E\{e^2(n)\} = \frac{\Delta^2}{12} \tag{8}$$

The quantization interval increment, Δ, is:

$$\Delta = \frac{2x_{max}}{2^N} \tag{9}$$

where $2X_{max}$ is the peak-to-peak quantizer range and N is the number of bits that can represent the quantizing levels. Combining equations (7), (8) and (9) yields:

$$SNR = 3\left[\frac{2^{2N}}{\frac{x_{max}^{2}}{E\{x^{2}(n)\}}}\right]$$

$$SNR_{dB} = 6N - 10 \log\left[\frac{x_{max}^{2}}{E\{x^{2}(n)\}}\right] + 4.77$$

For the quantization scheme in Figure 4, N is equal to 1, and $X_{max}^{2}/E\{x^{2}(n)\}$ is very large. This means that the output signal to quantizing noise level is much less than 0 dB, which is a very poor noise figure. The input signal, then, must be amplified so that it maximizes the signal to quantization noise level. The degree of amplification required will depend on such factors as the type of transducer device used at the input of the voltage amplifier, and the A/D conversion dynamic range ($2X_{max}$). The input transducer device will most likely be a microphone or a speech-activated diaphragm structure (like a telephone receiver or intercom speaker). The output signal levels from these devices are very low, on the order of 100 millivolts peak-to-peak. In order to drive an A/D converter, this would have to be amplified to, say, 4 or 5 volts. This would require a fairly high-gain, stable voltage amplifier (pre-amplifier), with

an adjustable gain control to compensate for the variations in the input signal level.

Other desirable features of a speech signal conditioner include a signal level indicator, a power amplifier that can drive a set of headphones or speakers, and a way of switching the input to the signal conditioner from the transducer device to the output of the digital speech processor. The power amplifier takes the signal from the voltage amplifier and converts it into a power signal that can drive the cone of a headphone speaker or loudspeaker; this voltage-to-power conversion is necessary because the signal from the voltage amplifier does not have enough current to excite the speaker coils. The signal level indicator should show the instantaneous peak level of the speech signal after it has been amplified by the voltage amplifier, and have a fairly wide range (30 to 40 dB). It should also show when the signal goes above a certain reference level.

CHAPTER II

SIGNAL CONDITIONER SYSTEM OVERVIEW

System Description

The signal conditioner designed, built, and tested for this project is a dual-channel system with a variety of features for analog processing of speech signals. A block diagram of the system is shown in Figure 5. The channels are identical and contain the following components: a voltage preamplifier, a variable cutoff frequency switched capacitor lowpass filter driven by a clock, and a post-processing linear phase lowpass filter. Each channel also contains a set of three interconnected switches that controls the signal flow through the system. In Figure 5, the signal flow is as follows: When the switches are set to position 1, the signal goes from the transducer to the voltage amplifier, then through the variable cutoff and linear phase lowpass filters to the A/D input of the digital speech processor. When the switches are set to position 2, the signal comes from the D/A output of the digital speech processor through the variable cutoff and linear phase lowpass filters, to the power amplifier, speakers, and signal level indicator. This is a fairly straightforward signal conditioning system that has all the characteristics outlined in the previous chapter. In the following sections, the individual building blocks of the system

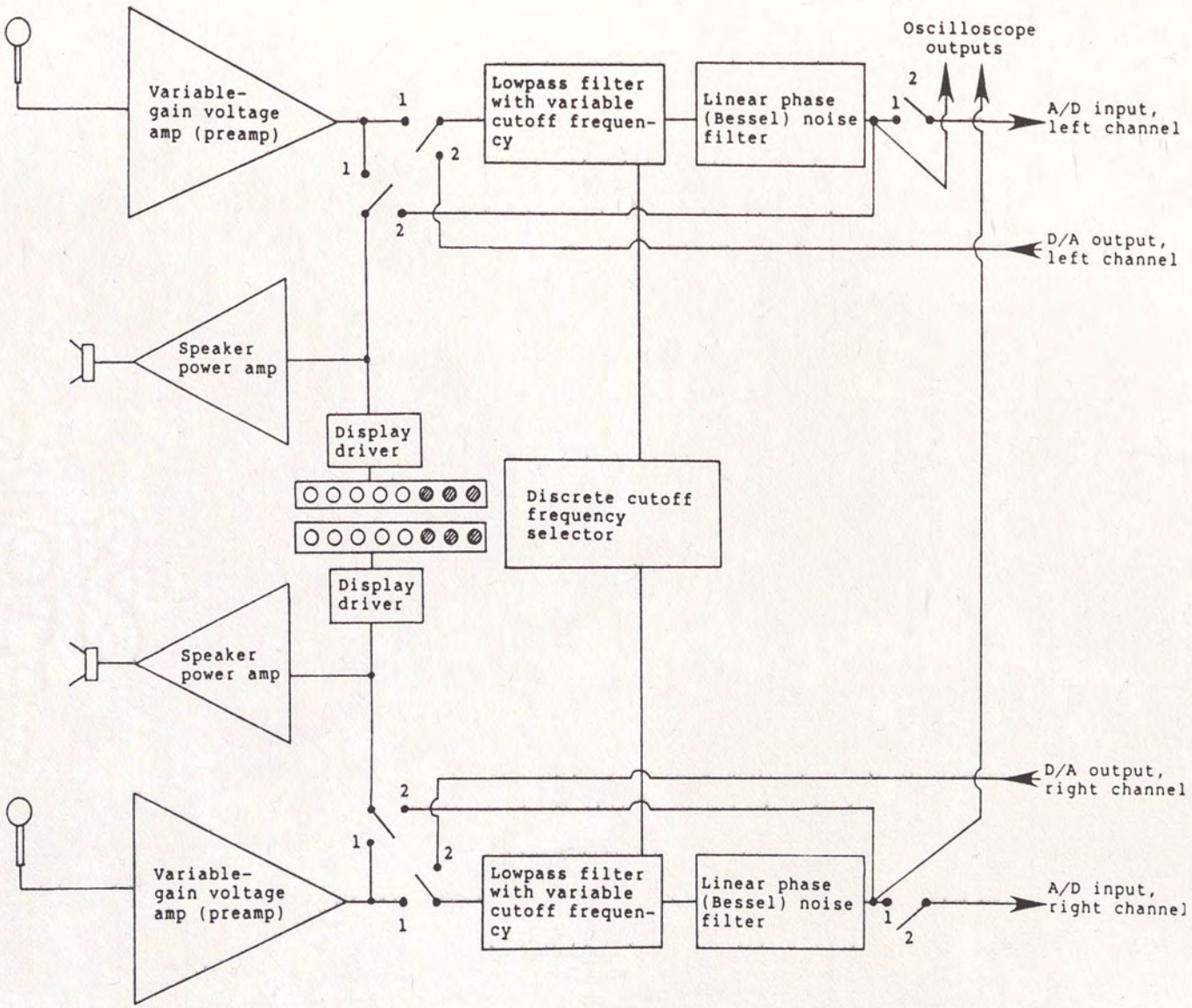


Figure 5. Block diagram of signal conditioner.

are examined, and are related to the overall operation of the system. The variable cutoff and linear phase lowpass filters are examined first, followed by the voltage amplifier, signal level indicator, and audio power amplifier. More information on the lowpass filters and voltage amplifier can be found in Chapter III and in the Appendix.

Signal Conditioner Components

Lowpass Filters

The signal conditioner shown in Figure 5 has two lowpass filters: a variable cutoff frequency linear phase switched capacitor lowpass filter, and a linear phase lowpass noise filter connected to the output of the switched capacitor filter. The switched capacitor filter is an EG&G Reticon R5613 linear phase lowpass filter, and is a self-contained circuit on an IC dual inline package. The cutoff frequency of the R5613 is tuneable, and is controlled by an external clock signal. The cutoff frequency is proportional to the clock signal frequency; the higher the clock frequency, the higher the filter cutoff frequency, and vice versa. The clock that drives the switched capacitor filter is a digital circuit consisting of a crystal clock oscillator, a decade counter, and two binary counters. The decade and binary counters divide the crystal clock oscillator frequency down to the switched capacitor filter clock frequencies, which, in turn, adjust the filter to the desired

cutoff frequencies. There are five cutoff frequencies that the switched capacitor filter can be set to. They are: 1.19 KHz, 2.38 KHz, 4.77 KHz, 5.96 KHz and 9.53 KHz. The corresponding clock frequencies are related to these corner frequencies by the following formula:

$$f_{clock} = 128 f_{corner}; \qquad f_{corner} = f_{clock}/128 \tag{10}$$

This means that the clock frequencies used for the switched capacitor filter are approximately 153 KHz, 305 KHz, 610 KHz, 763 KHz and 1.22 MHz. Equation (10) is true for any clock and corner frequency, for the R5613.

The operation of the switched capacitor filter is as follows. The clock signal is broken up into two alternating switching signals. These signals are sent to two MOSFET switches that are connected to either side of a capacitor. These MOSFET switches alternately switch on and off, which causes the capacitor to charge and discharge. This charging and discharging causes a current to flow through the capacitor, making it behave like a resistor. The effective resistance of the switched capacitor is:

$$R_{eff} = T/C \tag{11}$$

where T is the clock period in seconds and C is the capacitance of the capacitor. The derivation of equation (11) can be found

in Chapter III. Several switched capacitors can be combined with conventional capacitors and operational amplifiers to form active filters; these filters have no resistive elements and, hence, can be implemented entirely on an IC chip. No external resistors or capacitors are needed. The fact that the effective resistances of the switched capacitors are linear functions of the clock period means that the overall frequency response of the filter can be altered by varying the clock frequency. It is seen from equation (11) that a change in the clock period (or clock frequency) will result in a change in the effective resistance of the switched capacitor. If a series of switched capacitors is incorporated into an active filter, and all of these switched capacitors are tied to the same clock, varying the clock frequency will change the effective resistances of the switched capacitors concurrently, causing the transfer function of the filter to vary. This, in turn, will cause the critical frequencies of the filter to change. The R5613 lowpass filter operates on this principle. A more detailed analysis of the switched capacitor lowpass filter is found in Chapter III, along with a summary of the physical and electrical properties of several commercially available switched capacitor lowpass filters.

The linear phase lowpass filter shown in Figure 5 is a fixed active filter with a cutoff (3 dB) frequency of 30.3 KHz. The main purpose of this filter is to eliminate the stray signals

emanating from the digital clock that drives the switched capacitor filter, while passing through the desired audio signal with as little distortion as possible. Specifically, this filter is a fifth-order Sallen and Key active linear phase filter, and is described in more detail in appendices A and B. This filter has a rolloff in the stopband of 25.4 dB per octave, and an attenuation of 37.7 dB at 100 KHz. This means that any spurious clock signals will be effectively removed by the filter from the output audio signal, since the lowest clock frequency used for the switched capacitor filter is roughly 153 KHz.

Voltage Amplifier

The voltage amplifier used in the signal conditioner is a two-stage, non-inverting operational amplifier system that utilizes a single op amp for each stage. The first stage has a fixed gain of 5 (14 dB) and the second stage has a variable gain that ranges from approximately unity to 10 (10 dB). The amplifier takes the input microphone signal and amplifies it for input into the switched capacitor filter. The gain of the amplifier is essentially flat from d.c. to 100 KHz. The 3 dB frequency is 530 KHz; the crossover frequency (the frequency where the gain falls to unity) is 2.1 MHz. Each op amp stage has a single voltage series feedback resistive loop; gain control for the second stage is provided by a 10 KΩ trimpot. DC offset adjustment is provided by a voltage divider circuit connected to

the inverting input port of the two-stage op amp system. More information on the design and characteristics of the voltage amplifier, including a schematic diagram, is given in Appendix B.

Signal Level Display

The LED signal level display shows the instantaneous amplified signal level from the voltage amplifier and consists of a National Semiconductor LM3915 display driver and eight LEDs arranged horizontally in a bar graph format. Each LED is set to illuminate at a certain signal voltage level. Signal levels below 5 V peak (10 V peak-to-peak for a pure sinusoidal signal) will register on the red LEDs; signal levels at or above 5 V peak will register on the yellow LEDs. The 0 dB reference level is 5 V peak; all other levels are normalized to this value. The reference level can be adjusted via a 10 K Ω trimpot located on the signal conditioner front panel. The maximum signal level that can be displayed is approximately 10 V peak (20 V peak-to-peak, pure sinusoidal signal), or 6 dB above the reference. Appendix B contains more information on the signal level display.

Audio Amplifier

The audio power amplifier used in the signal conditioner is a National Semiconductor LM388N-2 power amplifier that can deliver up to 2.25 watts nominal into an 8 Ω speaker load. The purpose of this power amplifier is to convert the voltage signal from the

voltage amplifier into a power signal that can drive the cone of a loudspeaker. The amplifier has low total harmonic distortion (less than 0.4% from 20 Hz to 20 KHz with an output power level of 0.5 W, load impedance of 3 Ω, and 12 V supply voltage). It has an internal voltage gain of 20 (26 dB) from dc to 100 KHz that can be increased to 200 with the addition of an external resistor and capacitor between pins 2 and 6 on the amplifier IC DIP, or a capacitively coupled resistor connected to pin 6. The power supply rejection ratio is better than 20 dB over the operating frequency range; the power dissipation is typically less than 1 W (National Semiconductor Corporation 1980). More information on the audio power amplifier is contained in Appendix B.

Additional Comments

The signal conditioner circuitry is powered by a quad power supply that gives the following supply voltages: + 8 V and - 8 V for the voltage amplifier, switched capacitor filter, and linear phase filter; +12 V for the LED display driver and audio power amplifier; and +5 V for the digital clock circuitry and LEDs. There is a bus bar that serves as a dual ground for the circuit components; one ground is the audio signal ground, and the other is the digital logic ground. These grounds are connected together at the power supply in what is called a "star ground" configuration. This grounding technique eliminates ground loop

noise between the signal and logic grounds. A circuit schematic of the entire signal conditioner, including the grounding circuits, is shown in Appendix C.

CHAPTER III

SWITCHED CAPACITOR FILTERS

Basic Theory

The switched capacitor filter outlined in Chapter II is an active RC-type filter where the resistors are replaced by capacitors that are periodically charged and discharged using metal oxide semiconductor (MOS) field effect switching transistors. These switching transistors are driven by alternating clock signals, whose frequencies are much greater than the operating frequency range of the filter. The switched capacitors behave like resistors, with resistance values that are functions of the clock frequency. When the clock frequency is changed, the effective resistance of the switched capacitor is changed, causing the poles of the filter transfer function to move around in the complex plane. This results in a change in the filter cutoff frequency. The operation of the switched capacitor as a filter resistor is as follows (Gregorian and Themes 1986). Consider two MOSFET switches, each with a clock signal input into its gate, and a capacitor between the switches, as shown in Figure 6. In Figure 6, ϕ_1 and ϕ_2 are non-overlapping, alternating clock signals, each with period T. T' is the period of the clock signal that is the sum of ϕ_1 and ϕ_2, and is usually equal to T/2.

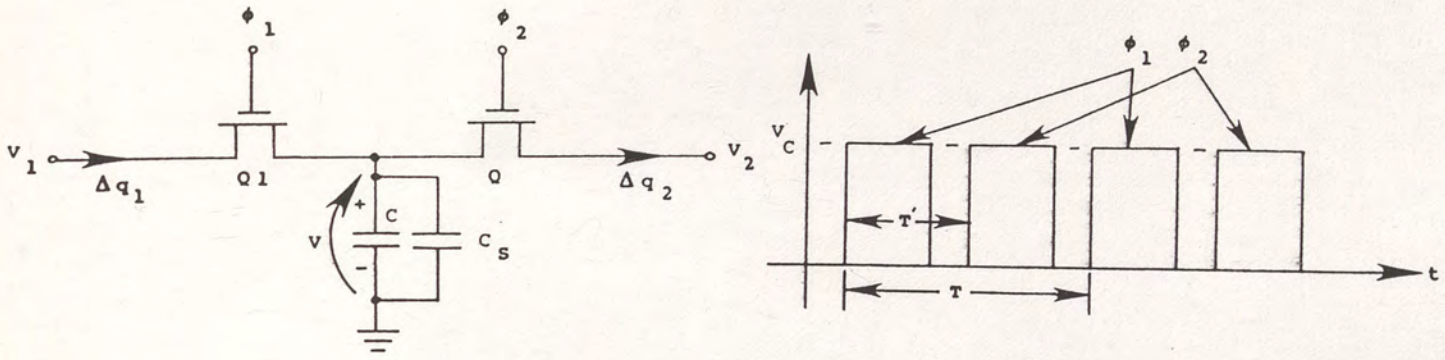


Figure 6. Circuit and timing diagram for switched capacitor.

This composite clock signal is the external clock that is input into the switched capacitor filter with a frequency of 1/T' that is referenced to the cutoff frequency of the filter. C_s is the stray capacitance caused by the source/drain to ground capacitance of the Q1,Q2 combination at the positive capacitor node. To begin, it is assumed that the capacitor is charged to V_2 ($V = V_2$). ϕ_1 rises from 0 to V_c, causing Q1 to turn on. A charge Δq_1 flows into the capacitor, where $\Delta q_1 = CV = C(V_1 - V_2)$. ϕ_1 goes to zero, causing Q1 to turn off. The voltage across the capacitor changes from $V_1 - V_2$ to V_1. Now ϕ_2 rises to V_c, causing Q2 to turn on. The voltage across the capacitor goes from V_1 to $V_1 - V_2$, and a charge Δq_2 flows through the capacitor, where $\Delta q_2 = CV = C(V_1 - V_2)$. But $C(V_1 - V_2) = \Delta q_1$, which implies that a charge equal to $C(V_1 - V_2)$ flows from the V_1 node to the V_2 node during each sampling period T. The average current flowing from V_1 to V_2 during the sampling period is:

$$i_{average} = \frac{dq}{dt} = \frac{\Delta q_1}{T} = \frac{C(V_1 - V_2)}{T}$$

$$= \frac{C}{T} (V_1 - V_2) \qquad (12)$$

Equation (12) is in the form of Ohm's Law; thus, it can be rewritten:

$$i_{average} = \frac{1}{R} (V_1 - V_2)$$

which yields

$$\frac{1}{R} = \frac{C}{T}$$

or

$$R = \frac{T}{C}$$

This is equation (11) in Chapter II. The switched capacitor in Figure 6, then, is essentially a resistor between points V_1 and V_2 whose resistance is a function of the clock frequency 1/T, as shown in Figure 7.

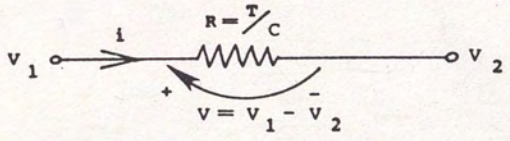


Figure 7. Equivalent resistance of switched capacitor.

The stray capacitance C_s can seriously affect the performance of the switched capacitor by introducing a reactive component in the effective impedance, resulting in phase changes in the filtered signal. To compensate for the stray capacitance, four MOSFET switches are used instead of two in the following configuration, shown in Figure 8.

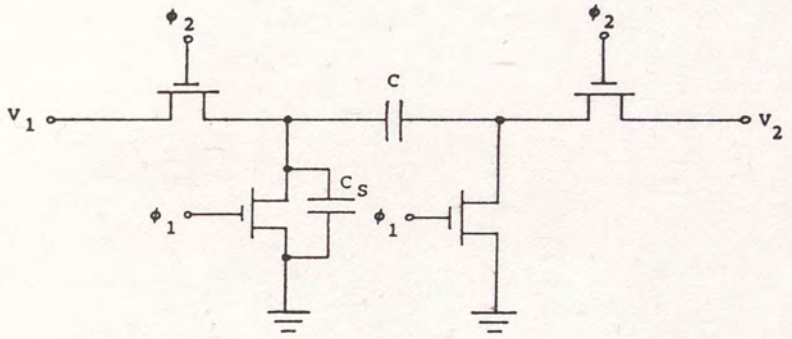


Figure 8. Stray insensitive configuration for switched capacitor.

In Figure 8, the stray capacitance is switched in and out at the same rate as the switching capacitor C. Hence, it "blends in" with the switched capacitor and does not affect the operation of the circuit. This type of circuit is commonly used in switched capacitor filters.

A very basic type of switched capacitor circuit is the switched capacitor integrator, which is shown below in Figure 9. This integrator behaves like a regular resistive/capacitive integrator, as will be proven.

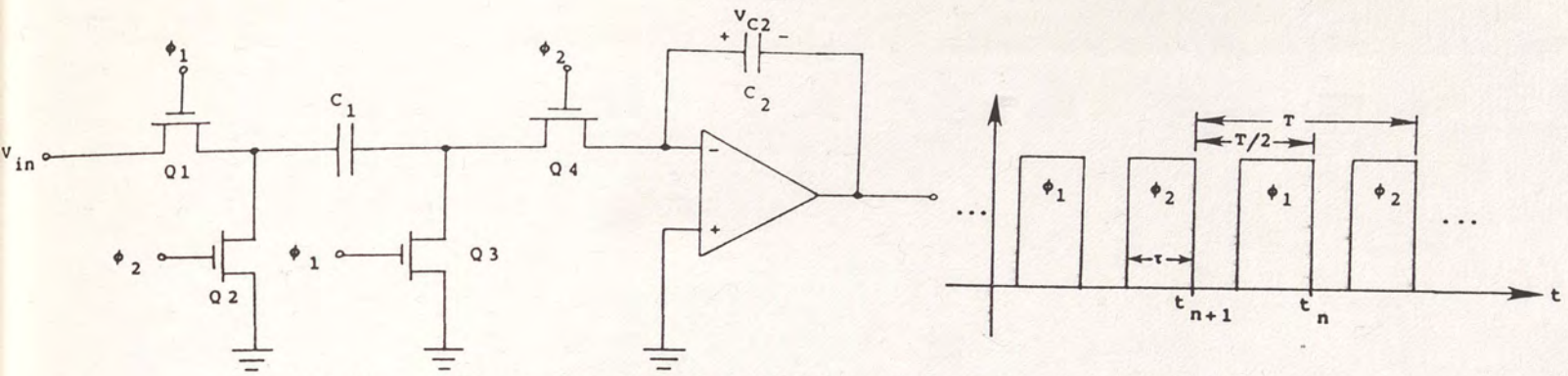


Figure 9. Stray insensitive switched capacitor integrator and clock waveform for MOSFET switches. C_1 is the switched capacitor.

An expression for the transfer function $V_{in}(s)/V_{out}(s)$ for the circuit in Figure 9 will be derived by first finding a difference equation that relates $V_{out}(t)$ to $V_{in}(t)$, then using the z-transform method to convert this difference equation into an s-domain transfer function (Gregorian and Themes 1986). At $t = t_n - \tau$ (which is the leading edge of the ϕ_1 pulse), Q1 and Q3 turn on, causing the voltage across C_1 to go to V_{in}. At $t = t_n$ (which is the trailing edge of the ϕ_1 pulse), Q1 and Q3 turn off, and C_1 charges to $\Delta q_1(t_n) = C_1 V_{in}(t_n)$. At $t = t_n + T/2 - \tau$ (which is the leading edge of ϕ_2). Q2 and Q4 turn on, and C_1 discharges through the virtual ground of the op amp. This causes the charge $\Delta q_2(t_n + T/2 - \tau) = \Delta q_1(t_n) = C_1 V_{in}(t_n)$ to flow into C_2, resulting in a voltage change $\Delta V_{C2}(t + T/2 - \tau)$ across C_2. Here

$$\Delta V_{C2}\left(t + \frac{T}{2} - \tau\right) = \frac{Q}{C} = \frac{\Delta q_2\left(t_n + \frac{T}{2} - \tau\right)}{C_2}$$

$$= \frac{C_1 V_{in}(t_n)}{C_2} = \left(\frac{C_1}{C_2}\right) V_{in}(t_n) \qquad (13)$$

But ΔV_{C2} $(t + T/2 - \tau)$ is also the negative of the change in output voltage V_{out} (t) between successive ϕ_1 or ϕ_2 clock pulses, which means that equation (13) can be rewritten:

$$\left(\frac{C_1}{C_2}\right) V_{in}(t_n) = -\left[V_{out}(t_{n+1}) - V_{out}(t_n)\right]$$

which yields

$$V_{out}(t_{n+1}) - V_{out}(t_n) = -\left(\frac{C_1}{C_2}\right) V_{in}(t_n) \qquad (14)$$

Equation (14) is a first-order difference equation that can be solved using the z-transform. $V_{in}(t_n)$ and $V_{out}(t_n)$ are forward-delayed signals, referenced to V_{out} (t_{n+1}); since a forward delay of one interval in the time domain transforms to a multiplication by 1/z in the z-domain, equation (14) in the z-domain is:

$$V_{out}(z) - \frac{1}{z} V_{out}(z) = -\frac{1}{z}\left(\frac{C_1}{C_2}\right) V_{in}(z)$$

After some algebra, this becomes:

$$V_{out}(z)(z - 1) = -\left(\frac{C_1}{C_2}\right) V_{in}(z)$$

which yields

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{-C_1/C_2}{z - 1} \tag{15}$$

Equation (15) is the z-domain transfer function of the integrator in Figure 9. To convert it to the s-domain, the matched-**z** transform,

$$Z = e^{sT}$$

is used, where T is the delay between successive pulses of the clock signal ϕ_1 or ϕ_2. Equation (15) can thus be written in the s-domain as

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-C_1/C_2}{e^{sT} - 1} \tag{16}$$

Now e^{sT} can be expanded in a Taylor series as follows.

$$e^{sT} = 1 + sT + \frac{(sT)^2}{2!} + \frac{(sT)^3}{3!} + \ldots \tag{17}$$

Equation (16) then becomes

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-C_1/C_2}{\left[1 + sT + \frac{(sT)^2}{2!} + \frac{(sT)^3}{3!} + \ldots\right] - 1}$$

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-C_1/C_2}{sT + \frac{(sT)^2}{2!} + \frac{(sT)^3}{3!} + \ldots} \tag{18}$$

In most practical switched capacitor circuits, as stated before, the clock frequency will be much greater than the frequency of the signal. This means that sT will be much less than 1, and equation (18) can thus be written

$$\frac{V_{out}(s)}{V_{in}(s)} \cong \frac{-C_1/C_2}{sT} = \frac{-C_1/C_2\ T}{s} \tag{19}$$

Recalling that the effective resistance of a switched capacitor is the clock period divided by the capacitance, Equation (19) becomes

$$\frac{V_{out}(s)}{V_{in}(s)} \cong \frac{-(1/R)(1/C_2)}{s} = \frac{-1/RC_2}{s}$$

which is the transfer function for an integrator containing a resistor R, an op amp, and an integrating capacitor C_2.

The derivation of the transfer function for the switched capacitor integrator shows that the implementation of a switched capacitor filter can be achieved simply by replacing the resistors of the corresponding resistive filter with switched capacitors. Mathematically, this means replacing the s variable in the resistive filter transfer function with (z - 1)/T. This is called the forward-Euler transformation, and is derived from

the z-to-s transformation and the Taylor series expansion in equation (17).

$$Z = e^{sT} = 1 + sT + \frac{(sT)^2}{2!} + \frac{(sT)^3}{3!} + \ldots$$

$$\cong 1 + sT$$

$$sT = z - 1$$

$$s = \frac{z - 1}{T}$$

Practical switched capacitor implementation, however, involves more than just replacing the resistors of the corresponding resistive filter with switched capacitors. Often the network topology of the switched capacitor filter is altered to minimize the number of MOSFET switches, and to ameliorate the stray capacitance effects. The altered circuit, though, will have the same transfer function and electrical characteristics as its resistive counterpart.

Filter Types

Just as there are many different types of resistive active filters, there are many varieties of switched capacitor filters. In fact, any filter type that can be realized with resistors, capacitors, and active elements can be realized with switched capacitors. A fairly simple lowpass filter is the biquad lowpass filter (Gregorian and Themes 1986), shown below in Figure 10.

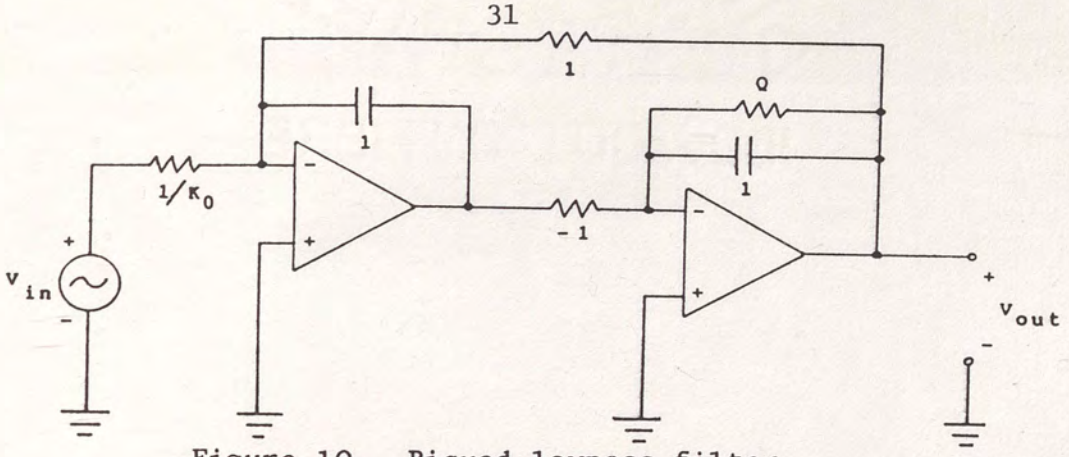


Figure 10. Biquad lowpass filter.

The transfer function for this lowpass filter is

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{1}{\frac{s^2}{K_o} + \frac{s}{K_o Q} + 1} \tag{20}$$

In equation (20), Q is the quality factor and is related to the steepness of the filter rolloff. K_o is a constant. The element values are normalized to a cutoff frequency of 1 rad/sec. The switched capacitor circuit for Figure 10 is shown in Figure 11.

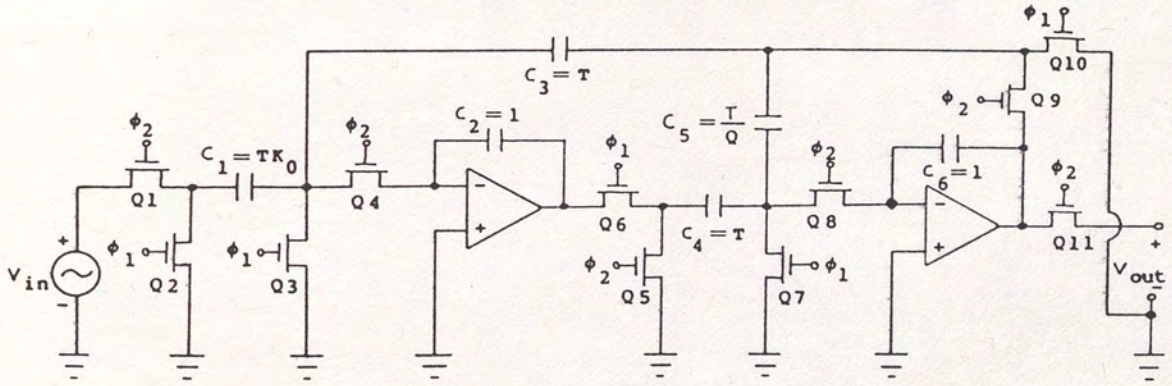


Figure 11. Switched capacitor implementation of biquad lowpass filter. T is the period of either clock signal in seconds.

The capacitors in the circuit of Figure 11 are normalized to ω_o = 1 rad/sec. The switching capacitors C_1, C_3, C_4 and C_5 have much smaller capacitances than the integrating capcitors C_2 and C_6, since the clock period T is a very small number. In Figure 11, Q3 and Q4 serve as switches for C_1 and C_3; C_3 shares switches Q9 and Q10 with C_5. This combining of switched capacitors reduces the number of MOSFETS from 16, if each switched capacitor had its own set of switches, to 11. The circuit in Figure 11 could be designed as a Butterworth, Chebyshev, elliptical or Bessel (linear phase) filter by setting the denominator equal to the appropriate polynomial function and solving for K_o and Q. These values would be substituted into the capacitor values in Figure 11 and the resulting capacitances would be normalized to the desired cutoff frequency.

Another type of switched capacitor filter that is commonly used is the ladder filter, so named because the active elements and switched capacitors are arranged like the rungs of a ladder. A fifth-order elliptic lowpass switched capacitor ladder filter that uses a clock signal like that shown in Figure 9 is shown in Figure 12.

The circuit in Figure 12 basically consists of five switched capacitor integrators similar to the one shown in Figure 9. C_2, C_5, C_8, C_{13} and C_{18} are the integrating capacitors; C_7, C_{11}, C_{15} and C_{19} are feedforward and feedback loop capacitors. C_1, C_3, C_4, C_6, C_9, C_{10}, C_{12}, C_{14}, C_{16} and C_{17} are the switching

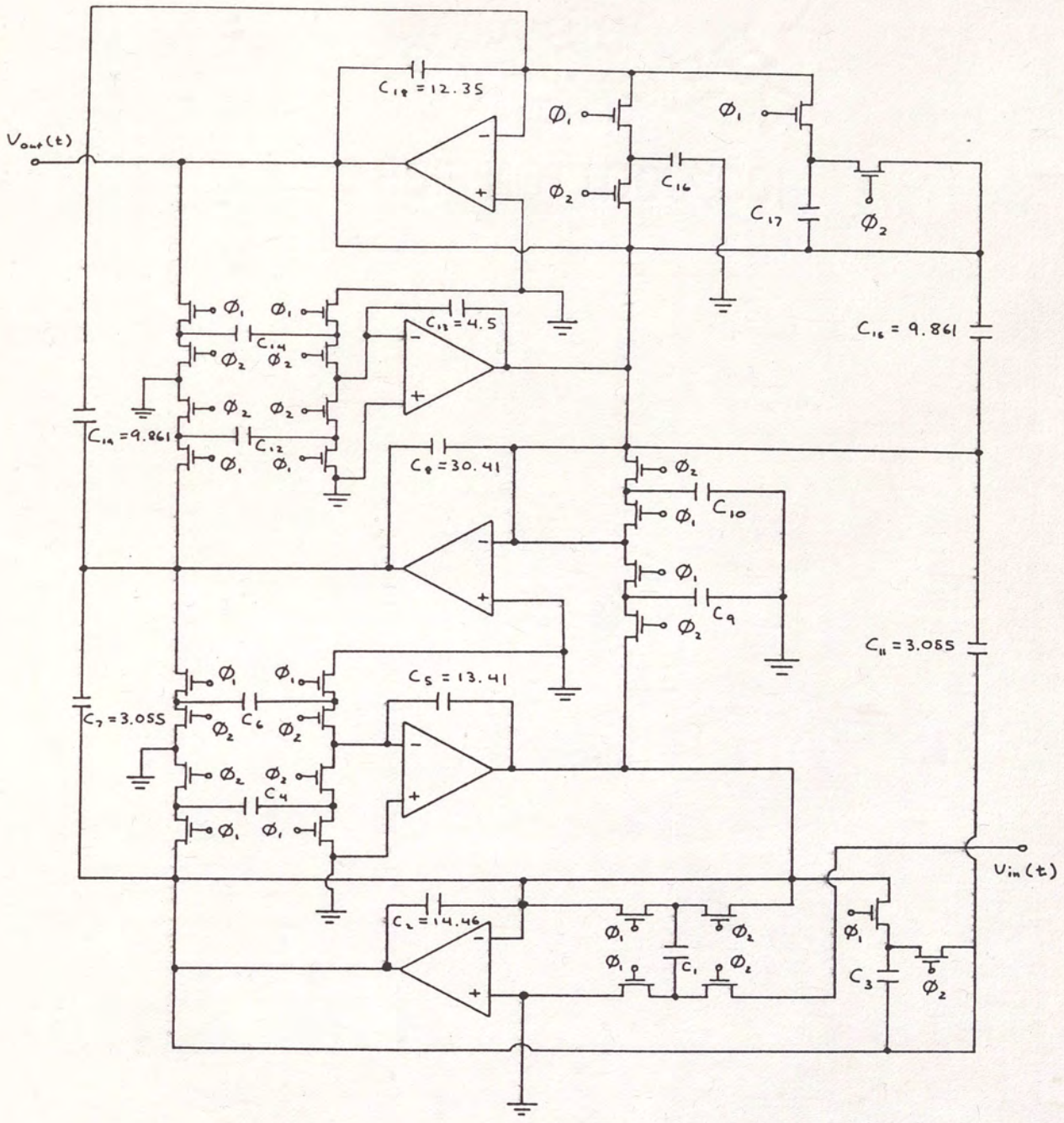


Figure 12. Fifth-order elliptic switched capacitor lowpass ladder filter. All capacitor values are normalized to a cutoff frequency of 1 rad/sec and are equal to 1 unless specified otherwise.

capacitors controlled by the ϕ_1 and ϕ_2 clock signals. The analysis of the circuit proceeds as follows (Lee and Jenkins 1981). The circuit is broken up into its constituent integrator parts, and the output voltages from the integrators are obtained by iteratively solving the following matrix difference equations for the output voltage vectors $V_{out}(n - 1/2)$ and $V_{out}(n)$:

For clock signal ϕ_1:

$$V_{out}(n - 1/2) = ([I] + [D_1])^{-1} [([F] - [A_1][B_2])V(n-1) - [E_1]V_{in}(n - 1/2) + ([G_1] - [A_1][C_2])V_{in}(n - 1)] \quad (21)$$

For clock signal ϕ_2:

$$V_{out}(n) = ([I] + [D_2])^{-1} [([F] - [A_2][B_1])V(n - 1/2) - [E_2]V_{in}(n) + ([G_2] - [A_2][C_1])V_{in}(n - 1/2)] \quad (22)$$

In equations (21) and (22), [I] is the identity matrix, $[A_1]$, $[A_2]$, $[B_1]$, $[B_2]$, $[C_1]$ and $[C_2]$ are matrices whose elements depend on the parallel switched capacitor values, $[D_1]$, $[D_2]$, $[E_1]$, $[E_2]$, [F], $[G_1]$ and $[G_2]$ are matrices whose elements depend on the series switched capacitor and integrating capacitor

values, and $V_{in}(n - 1)$ and $V_{in}(n - 1/2)$ are the input voltage vectors. The input voltage vectors are set to a certain value for a specific time (like a sample and hold input), equations (21) and (22) are solved for the output voltage vectors, and the output voltage vectors are used to determine the overall system time domain response of the filter to the input. The input vector is set to the next value, and the process is repeated. The resulting time domain responses can be converted to the frequency domain using a fast Fourier transform technique, or the frequency response can be calculated directly by converting equations (21) and (22) to the z-domain and s-domain using the techniques outlined for the switched capacitor integrator.

There are several commercially available switched capacitor filters. All of these filters are self-contained in IC DIPs and do not require external capacitors or resistors. All the filters require dual (positive and negative) power supplies and have a clock input port. The first filter that will be examined is the Motorola MC145414 dual tuneable lowpass filter. This filter is packaged in a 16 pin DIP and contains two fifth-order elliptic switched capacitor lowpass filters. One filter has unity-gain; the other has a fixed gain of approximately 18 dB. Two uncommitted op amps are also provided, which can be used for other active circuits that are utilized in conjunction with the switched capacitor filters. The switched capacitor filters are powered by a dual power supply that can range from ± 5 V (10 V

spread) to ± 8 V (16 V spread). The maximum input or output signal level for the filters is determined by the maximum power supply rating, and is 16 V peak-to-peak. The clock inputs to the switched capacitor filters are CMOS or TTL compatible; the filter cutoff frequency is equal to the clock frequency divided by 35.56. The filters have typically less than 1.0 dB ripple in the passband, for a given cutoff frequency. The rolloff in the stopband is very steep, in excess of 120 dB per octave (Motorola Semiconductor Products, Inc. 1985).

The second switched capacitor filter that will be examined is also made by Motorola. It is the MC145415 dual tuneable linear phase lowpass filter. This filter is similar in physical design and operation to the MC145414; there are differences, however, in its electrical characteristics. First, the filter can operate with a lower supply voltage than the MC145414 (± 2.5 V lower limit compared to ± 5 V lower limit). Secondly, the filter clock input is CMOS compatible only. Thirdly, the clock frequency to filter cutoff frequency ratio is 64 instead of 35.56. Like the MC145414, the MC145415 consists of a unity-gain switched capacitor filter, a switched capacitor filter with a fixed gain of 18 dB, and a pair of uncommitted op amps. However, the filters are fifth-order linear-phase instead of elliptical. The maximum input or output signal for the filters is 16 V peak-to-peak, the same as the MC145414. The stopband rolloff is

not as steep as the rolloff for the MC145414, roughly 45 dB per octave.

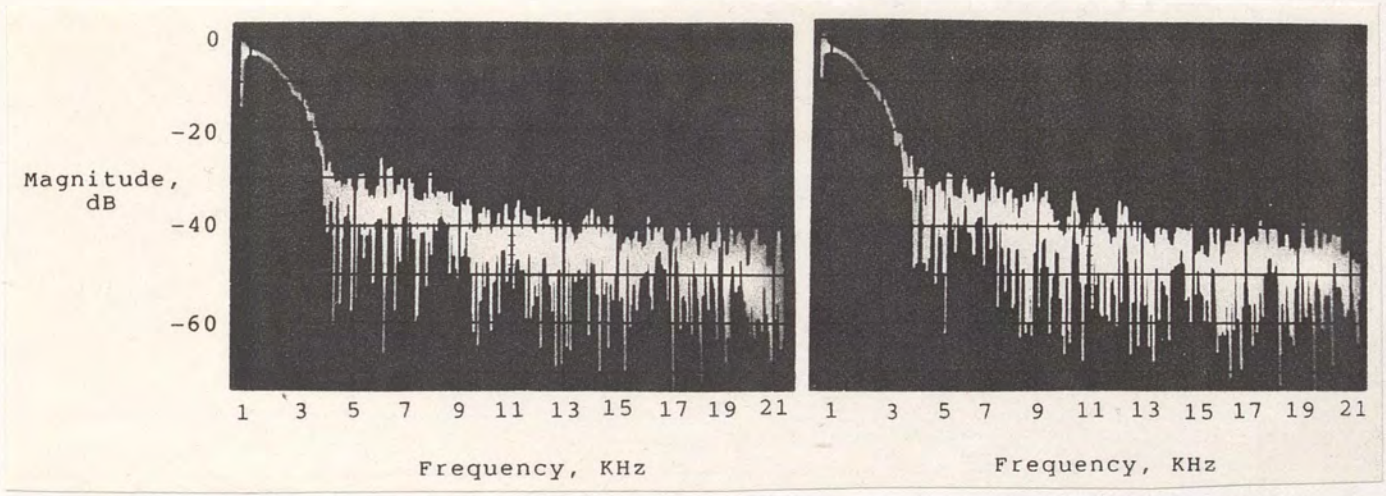
The third and fourth switched capacitor filters that will be examined are the R5609 and R5613 lowpass filters, both made by EG&G Reticon. Unlike the Motorola filters, the R5609 and R5613 contain only one switched capacitor filter, which has unity gain. The clock input to the filter is TTL or CMOS compatible; there is a clock/2 (half clock frequency) output that can be used to drive other switched capacitor or digital circuits. The R5609 and R5613 are each contained in an 8 pin IC DIP, with pins for signal in, signal out, positive supply, negative supply, clock in, clock/2 out, and reference voltages. There are no extra op amps in the R5609 and R5613 ICs, as there are in the Motorola chips. The power supply ranges for the R5609 and R5613 are $\pm$5 V (10 V spread) to $\pm$ 10 V (20 V spread), which means that the maximum input or output signal level for the filters is 20 V peak-to-peak. The R5609 is a seventh-order elliptic lowpass filter with a clock frequency to cutoff frequency ratio of 100 and a rolloff in the stopband in excess of 120 dB per octave. The R5613 is a linear-phase (Bessel) lowpass filter with a clock frequency to cutoff frequency ratio of approximately 128 and a rolloff in the stopband that varies from 20 dB per octave near the corner frequency to 120 dB per octave farther out in the stopband (EG&G Reticon 1982).

CHAPTER IV

RESULTS

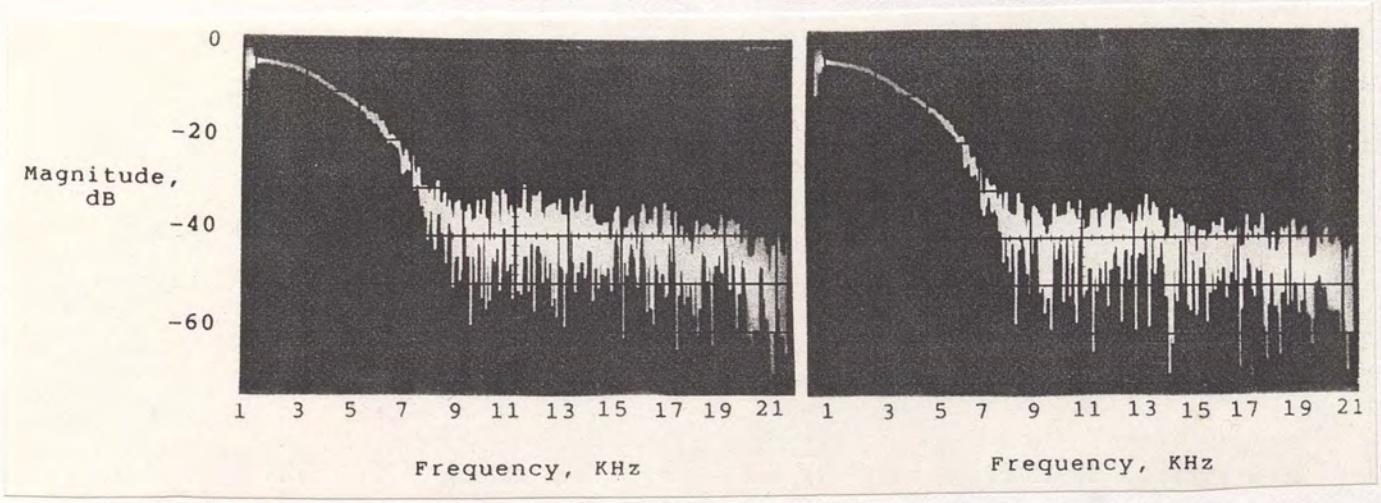
Performance Analysis of Signal Conditioner

The signal conditioner was constructed and brought up to working order and then was put through a series of tests using a Tektronix 5L4N Spectrum Analyzer to see how well it performed; i.e., how well it bandlimited the input signal from the spectrum analyzer at the various cutoff frequencies. The spectrum analyzer output port was connected to the FROM D/A port on the left channel of the signal conditioner, with the frequency range set to 1 to 21 KHz. The signal conditioner was set to output mode and the SCOPE OUT port on the signal conditioner was connected to the spectrum analyzer input port. The frequency response of the signal conditioner was displayed and photographed at each of the signal conditioner cutoff frequencies. These measurements were repeated for the right channel. The step response of the left channel of the signal conditioner was measured and photographed by inputting a 500 Hz, 5 V peak-to-peak square wave into the FROM D/A port, and connecting the SCOPE OUT port to an oscilloscope. This was repeated for the right channel. Figures 13 through 18 show the results of these tests. For the spectrum analyzer plots, the input signal level reference is at 0 dB.



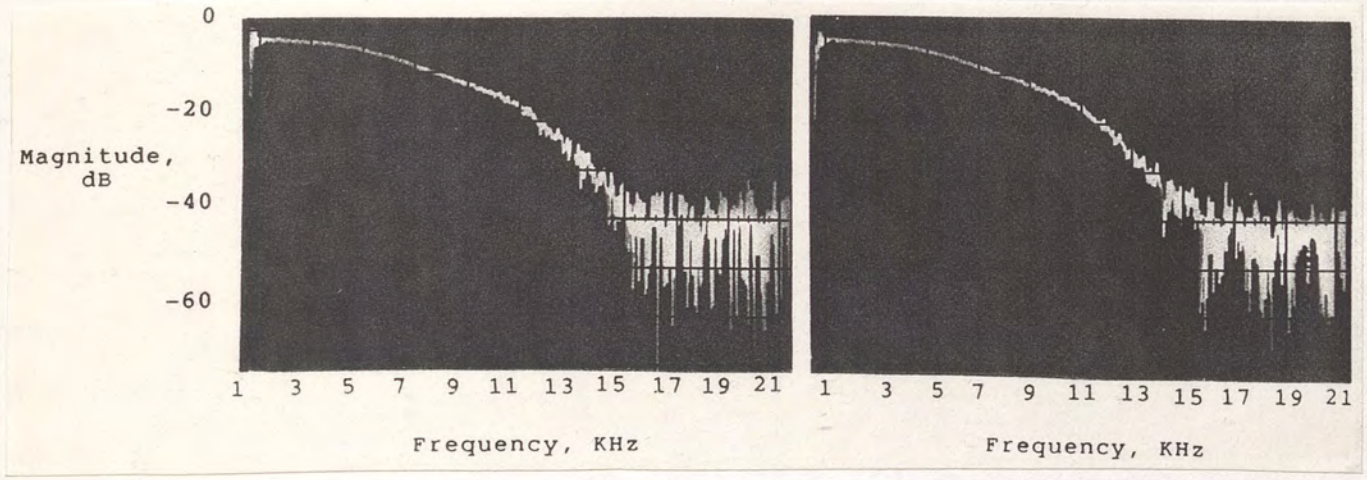
(a) (b)

Figure 13. (a) Left channel signal frequency response with cutoff frequency set to 1.19 KHz. (b) Right channel signal frequency response with cutoff frequency set to 1.19 KHz.



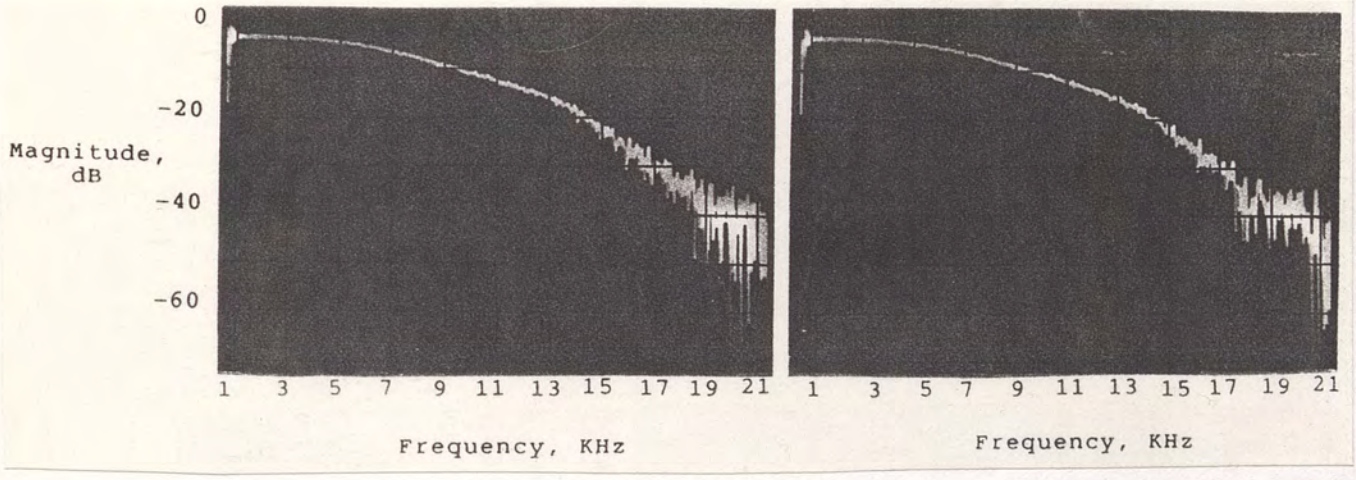
(a) (b)

Figure 14. (a) Left channel signal frequency response with cutoff frequency set to 2.38 KHz. (b) Right channel signal frequency response with cutoff frequency set to 2.38 KHz.



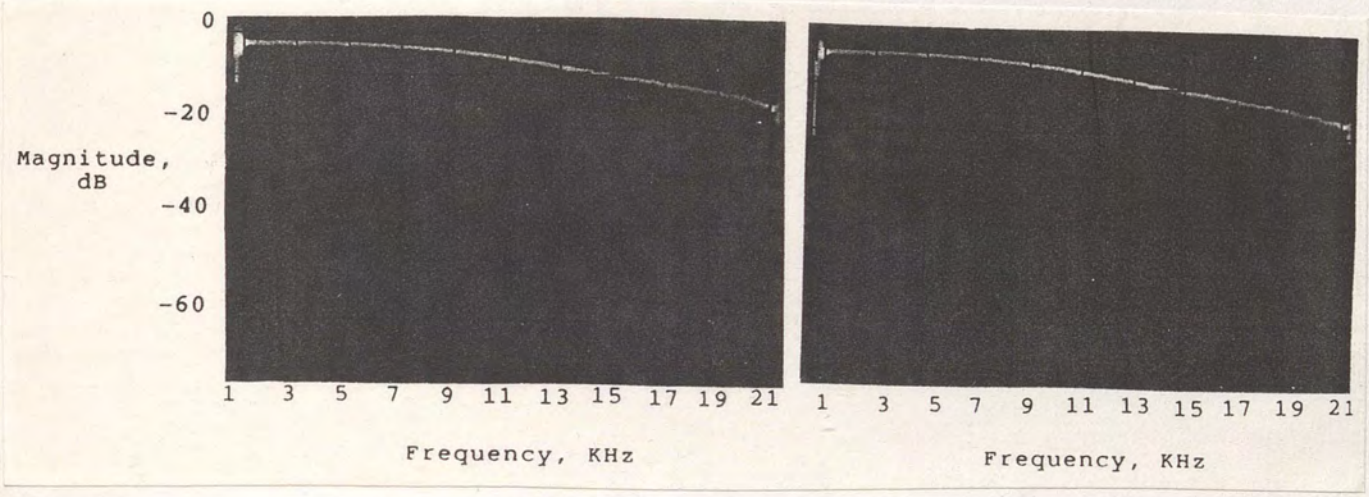
(a) (b)

Figure 15. (a) Left channel signal frequency response with cutoff frequency set to 4.77 KHz. (b) Right channel signal frequency response with cutoff frequency set to 4.77 KHz.



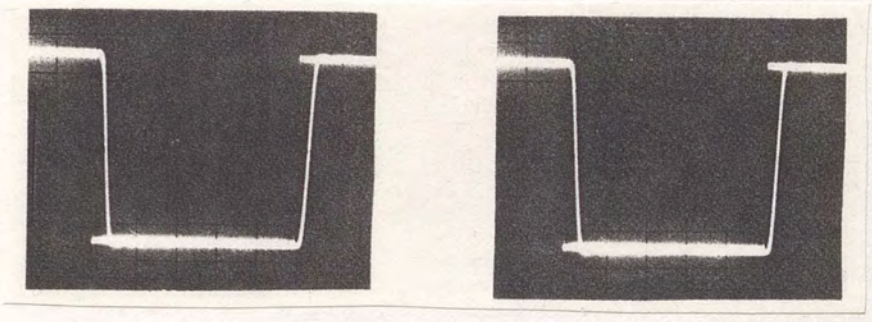
(a) (b)

Figure 16. (a) Left channel signal frequency response with cutoff frequency set to 5.96 KHz. (b) Right channel signal frequency response with cutoff frequency to 5.96 KHz.



(a) (b)

Figure 17. (a) Left channel signal frequency response with cutoff frequency set to 9.53 KHz. (b) Right channel signal frequency response with cutoff frequency set to 9.53 KHz.



(a) (b)

Figure 18. (a) Step response of left channel. (b) Step response of right channel.

Further Work

The signal conditioner will be used in conjunction with a digital speech processor to condition and optimize both input microphone speech signals and the digitally processed speech signals from the digital to analog output of the speech processor. One modification to the signal conditioner needs to be made, however: the vector boards that contain the signal conditioner circuits must be replaced with standard printed circuit boards to insure structural soundness and durability, and consistent electrical performance. Basically, the circuit components will be removed from the vector boards and the vector boards themselves will be unbolted from the bottom of the cabinet. The circuit components will be soldered onto the PC boards, and the PC boards will be bolted to the cabinet bottom, in the same locations as the vector boards were. The component soldering will be done by a technician using special techniques. This is necessary because of the delicate nature of some of the components, especially the CMOS devices.

APPENDICES

APPENDIX A

LOWPASS FILTER THEORY

Introduction

An essential component of any analog signal processing system is a variable cutoff frequency lowpass filter that can be used to adjust the bandwidth of the signal. The lowpass filter lets through signals whose frequencies are below a certain cutoff frequency, and rejects signals whose frequencies are above this cutoff frequency. Figure A1 shows the ideal magnitude and phase response (transfer function) of a lowpass filter.

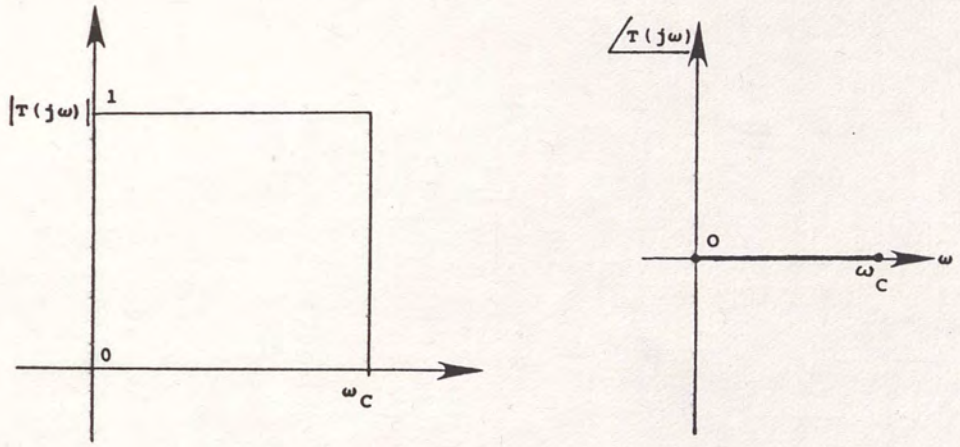


Figure A1. Magnitude and phase response of ideal lowpass filter.

The magnitude and phase responses in Figure A1 cannot be realized with systems made up of a finite number of elements. Therefore, mathematical approximations to these responses must be used in

the design of practical lowpass filters. These approximating functions will be of the following form:

$$\left|T\left(j\,\frac{\omega}{\omega_c}\right)\right|^2 = \frac{1}{1 + A\left[\left(\frac{\omega}{\omega_c}\right)^2\right]} \qquad \text{(A1)}$$

In equation (A1), ω is the radian frequency variable, ω_c is the cutoff frequency or break frequency, and $|T(j\omega/\omega_c)|^2$ is the magnitude-squared or power response of the filter. The power response is used here because lowpass filter critical frequencies are usually expressed in terms of power; the cutoff frequency ω_c is often referred to as the half power frequency, but it may be something else, depending on the type of filter under consideration. The function $A[(\omega/\omega_c)^2]$ exhibits a lowpass characteristic; that is, it is zero for $\omega = 0$, 1 (or some other value) for $\omega = \omega_c$, and infinite for $\omega = \infty$.

Butterworth Filters

A Butterworth filter is a filter whose power response is defined by

$$\left|T\left(j\,\frac{\omega}{\omega_c}\right)\right|^2 = \frac{1}{1 + \left[\left(\frac{\omega}{\omega_c}\right)^2\right]^n} = \frac{1}{1 + \left(\frac{\omega}{\omega_c}\right)^{2n}} \qquad \text{(A2)}$$

Equation (A2) is equation (A1) with $A[(\omega/\omega_c)^2]$ equal to

$[(\omega/\omega_c)^2]^n$. The value n is the order of the filter. At $\omega = \omega_c$ (the filter cutoff frequency):

$$\left|T\left(j\,\frac{\omega_c}{\omega_c}\right)\right|^2 = \frac{1}{1 + \left(\frac{\omega_c}{\omega_c}\right)^{2n}} = \frac{1}{1 + (1)^{2n}} = \frac{1}{1+1} = \frac{1}{2}$$

Thus, ω_c is the half-power (3 dB) cutoff frequency of the Butterworth filter. Figure A2 shows typical power responses for Butterworth filters, for a low value of n (low-order filter) and a high value of n (high-order filter).

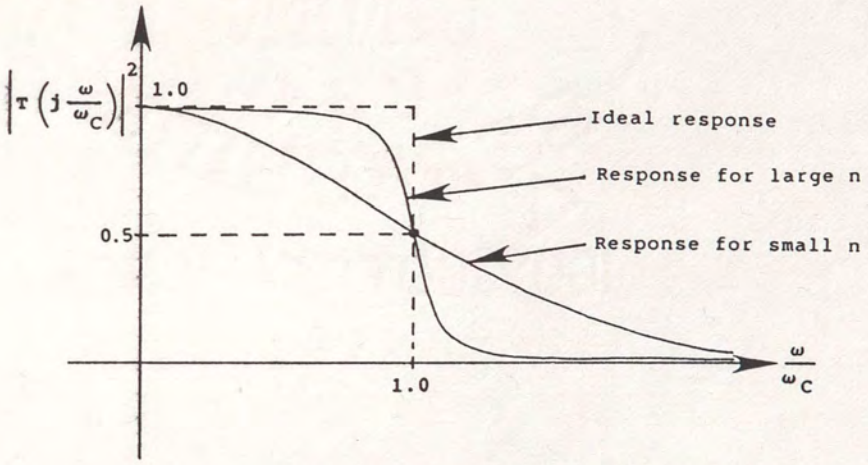


Figure A2. Butterworth filter responses for small and large values of the filter order n.

In Figure A2, it is seen that if the filter order is large, the filter response approximates the ideal response very well. The number of energy-storing elements (capacitors and inductors) in a Butterworth filter is equal to the filter order n; thus, a high-order filter with a response like that in Figure A2 would require a large number of capacitors and inductors. This is not

always practical, and there may have to be a tradeoff between the filter circuit complexity and the filter response.

The design of a Butterworth filter involves several steps. First, the locations of the poles of the Butterworth power response function in the s-plane are determined. The left-hand plane poles are retained to insure that the filter is causal and stable; these poles are used to generate the s-domain voltage transfer function. This function is then used to generate a filter circuit using various methods of network synthesis. Finally, the element values in this circuit are adjusted for the desired filter cutoff frequency. From equation (A2)

$$|T(s)|^2 = \frac{1}{1 + \left(\frac{s}{j}\right)^{2n}}, \quad s = j\frac{\omega}{\omega_c}, \quad \frac{\omega}{\omega_c} = \frac{s}{j}$$

$$|T(s)|^2 = \frac{1}{1 + (-j)^{2n}\, s^{2n}} = \frac{1}{1 + [(-j)^2]^n\, s^{2n}} = \frac{1}{1 + (-1)^n\, s^{2n}}$$

The poles of $|T(s)|^2$ are the solutions of the equation

$$(-1)^n\, s^{2n} + 1 = 0$$

Dividing both sides of this equation by $(-1)^n$ and transposing yields

$$s^{2n} = -(1)^{-n} = (-1)(-1)^{-n} = (-1)^{-1}(-1)^{-n} = (-1)^{-(n+1)}$$

or

$$s^{2n} = e^{j\pi(n+1)} = e^{j\pi(2k+1+n)} \tag{A3}$$

The roots (poles) of equation (A3) are

$$s_m = e^{j\left[\left(\frac{2k+1}{2n}\right)\pi + \frac{\pi}{2}\right]} = \cos\left[\left(\frac{2k+1}{2n}\right)\pi + \frac{\pi}{2}\right] + j \sin\left[\left(\frac{2k+1}{2n}\right)\pi + \frac{\pi}{2}\right]$$

$$= -\sin\left(\frac{2k+1}{2n}\right)\pi + j \cos\left(\frac{2k+1}{2n}\right)\pi,$$

$$m = 1, 2, 3, \ldots, 2n; \quad k = 0, 1, 2, \ldots, 2n-1$$

The poles that lie in the left-hand plane are

$$s_m = -\sin\left(\frac{2k+1}{2n}\right)\pi + j \cos\left(\frac{2k+1}{2n}\right)\pi, \tag{A4}$$

$$m = 1, 2, 3, \ldots, n; \quad k = 0, 1, 2, \ldots, n-1$$

Now, the power response transfer function $|T(s)|^2$ can be written

$$|T(s)|^2 = \frac{1}{B_n(s)B_n(-s)} = T(s)T^*(-s)$$

where $B_n(s)$ is a polynomial in s, and is referred to as the Butterworth polynomial of order n. The poles in equation (A4) are the roots of this polynomial. This means that $B_n(s)$ can be written

$$B_n(s) = \prod_{m=1}^{n} (s - s_m) = \prod_{k=0}^{n-1} \left[s + \sin\left(\frac{2k+1}{2n}\right)\pi - j \cos\left(\frac{2k+1}{2n}\right)\pi\right] \tag{A5}$$

The voltage transfer function is

$$T(s) = \frac{1}{B_n(s)} \tag{A6}$$

To design a Butterworth filter of a given order n, then equation (A5) would be used to calculate the factored form of $B_n(s)$, which would be multiplied out to generate the polynomial form. This polynomial would be substituted into equation (A6) to generate the voltage transfer function T(s) for the filter. Using network synthesis, this transfer function would be converted into a filter circuit containing capacitors, inductors or possibly active devices. For example, if a third-order Butterworth filter is desired, the Butterworth polynomial becomes

$$B_3(s) = \prod_{k=0}^{2} [s + \sin(\frac{2k+1}{6})\ \pi - j\ \cos(\frac{2k+1}{6})\pi]$$

$$B_3(s)=[s+\sin(\frac{\pi}{6})-j\ \cos(\frac{\pi}{6})][s+\sin(\frac{\pi}{2})-j\ \cos(\frac{\pi}{2})][s+\sin(\frac{5\pi}{6})-j\ \cos(\frac{5\pi}{6})]$$

$$= (s + 0.5 - j\ 0.86603)(s + 1)(s + 0.5 + j\ 0.86603) \tag{A7}$$

$$= (s^2 + s + 1)(s + 1)$$

$$= s^3 + 2s^2 + 2s + 1$$

From equation (A6), the voltage transfer function is

$$T(s) = \frac{1}{s^3 + 2s^2 + 2s + 1}$$

Now, a circuit that has this transfer function needs to be found. A common method for doing this uses the impedance-conversion technique, where the transfer function T(s) is converted into a driving-point or input impedance function Z(s). This method mathematically places a unit load impedance and a unit source impedance at the output and input ports of the circuit, and is executed by putting the even-power terms of the Butterworth polynomial in the numerator of Z(s), and the odd-power terms in the denominator. The coefficient of the highest-power term is incremented by one. Carrying out the above steps for T(s) yields

$$z(s) = \frac{2s^2 + 1}{2s^3 + 2s} = \frac{1}{\frac{2s^3 + 2s}{2s^2 + 1}} = \frac{1}{\frac{s(2s^2 + 1) + s}{2s^2 + 1}}$$

$$= \frac{1}{s + \frac{1}{\frac{2s^2 + 1}{s}}} = \frac{1}{s + \frac{1}{2s + \frac{1}{s}}} \qquad \text{(A8)}$$

Examination of equation (A8) shows that the circuit will contain, going from right to left, a parallel capacitance, a series inductance, and another parallel capacitance. The normalized or unscaled element values are the coefficients of the s-terms in equation (A8). The filter circuit is shown below in Figure A3. This filter is for a cutoff frequency of 1 rad/sec, with a source and load impedance of 1Ω. For more realistic values of cutoff

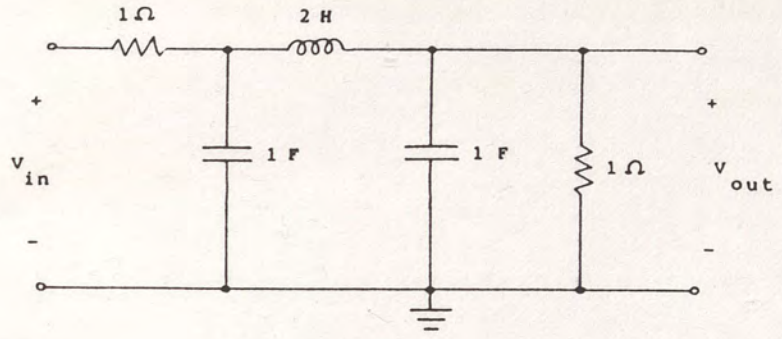


Figure A3. Third-order Butterworth filter with normalized element values.

frequency and source and load impedance, the element values are multiplied by the following scale factors:

$$k_{inductor} = \frac{z}{\omega_c}; \; k_{capacitor} = \frac{1}{z\omega_c} \qquad \text{(A9)}$$

Here Z is the source and load impedance for the filter.

The Butterworth filter shown in Figure A3 is a passive circuit, since it contains only energy-storing or energy-dissipating elements (capacitors and inductors). Circuits like these may not be suitable for some applications, such as audio, because of the relatively large inductor and capacitor values that are required; such large inductors and capacitors would be difficult to realize physically. An alternative would be to use an active device in the filter. The most common active device used for this purpose is the operational amplifier, or op amp. The op amp has an inverting and non-inverting input, very high input impedance, very low output impedance, and very high gain.

These characteristics make it possible to realize almost any type of transfer function by connecting resistors and capacitors to the input and output terminals of the op amp in a certain way. A very common active lowpass filter that uses an op amp is the Sallen and Key filter, first proposed by R.P. Sallen and E.L. Key in 1955. Basically, the Sallen and Key filter is a unity-gain, low output impedance circuit; this makes it ideal for integration into more complex systems (such as the signal conditioner). A second-order Sallen and Key filter is shown in Figure A4.

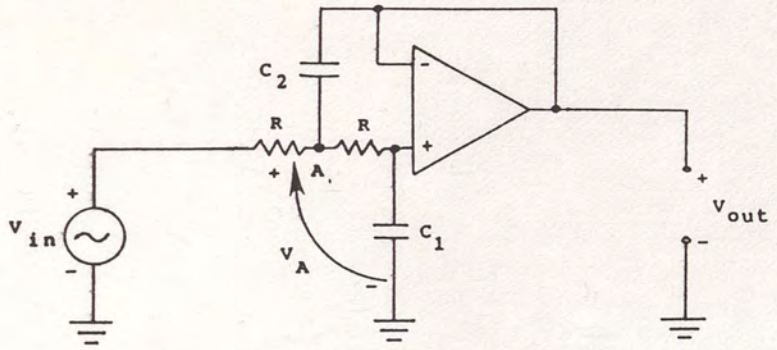


Figure A4. Second-order Sallen and Key filter.

Using node analysis, the equations for this circuit are

$$GV_{in}(s) = (2G + C_2 s)V_A - (G + C_2 s)V_{out}(s)$$

$$0 = -GV_A + (G + C_1 s)V_{out}(s)$$

where $G = 1/R$ and V_A is the voltage from ground to point A. Solving for $V_{out}(s)/V_{in}(s)$ yields the transfer function for this circuit:

$$T_2(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{R^2C_1C_2s^2 + 2RC_1s + 1} \qquad \text{(A10)}$$

Equation (A10) is in the standard voltage transfer function format shown in equation (A6); to get the normalized Butterworth element values, the denominator of equation (A10) is set equal to the second-order Butterworth polynomial $B_2(s) = s^2 + 1.41421s + 1$. This yields

$$C_1C_2 = 1$$

$$2C_1 = 1.41421$$

assuming $R = 1\Omega$. Solving these equations gives the normalized capacitor values $C_1 = .70711F$ and $C_2 = 1.41421F$; these values are converted to real values using the capacitor scaling factor in equation (A9). In this case, Z is the resistor R in Figure A4, and is usually set to a convenient value, such as 1 $K\Omega$. In Figure A4, if an RC filter section is placed between the left-most resistor and the source, the third-order Sallen and Key filter results. This circuit is shown in Figure A5.

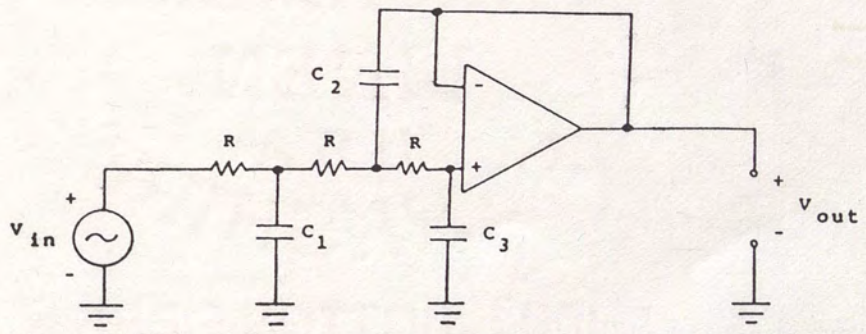


Figure A5. Third-order Sallen and Key filter.

Using techniques similar to those applied to the second-order circuit, the transfer function for this circuit can be found. It is

$$T_3(s) = \frac{1}{R^3C_1C_2C_3s^3 + 2R^2(C_1C_3 + C_2C_3)s^2 + R(C_1 + 3C_3)s+1} \qquad \text{(A11)}$$

As was done with the second-order circuit, the denominator of equation (A11) is set equal to the third-order Butterworth polynomial given by equation (A7). With R = 1 , this yields

$$C_1C_2C_3 = 1$$

$$C_1C_3 + C_2C_3 = 1$$

$$C_1 + 3C_3 = 2$$

Solving this set of simultaneous equations gives the normalized Butterworth capacitor values. After some algebra, the above equations can be written

$$C_1^3 - 2C_1^2 + 3C_1 - 3 = 0 \qquad \text{(A12)}$$

$$C_3 = \frac{2}{3} - \frac{1}{3}C_1$$

$$C_2 = \frac{1}{C_1C_3}$$

Equation (A12) is a cubic equation that can be solved iteratively on a computer or pocket calculator. The resulting value for C_1 is substituted into the expressions for C_2 and C_3, which yields

$$C_1 = 1.39300F$$
$$C_2 = 3.54784F$$
$$C_3 = 0.20234F$$

These values would be scaled to the actual cutoff frequency and resistance levels using equation (A9). The resulting circuit has exactly the same electrical properties as the passive Butterworth filter shown in Figure A3.

Some final comments need to be made concerning Butterworth filters. First, the procedures outlined in the preceding paragraphs are fairly involved and involve a lot of computation, even for a relatively simple filter. For a higher-order filter (n = 7 or 8), they become prohibitive. Fortunately, tables of Butterworth inductor and capacitor element values are available. In addition, computer programs that analyze and synthesize filters have been written; these programs run on most personal and main-frame machines. The second subject that needs to be brought up concerns the pole-zero diagram of the Butterworth filter. This is important if a stability or root-locus analysis is done on the filter. Also, it gives a graphical insight into how the filter behaves at various frequencies. It is recalled

that the poles of the Butterworth power response $|T(s)|^2$ are given by

$$s_m = -\sin(\frac{2k+1}{2n})\pi + j\cos(\frac{2k+1}{2n})\pi, \qquad \text{(A13)}$$

$$m = 1, 2, 3, \ldots, 2n; \; k = 0, 1, 2, \ldots, 2n-1$$

It is seen that equation (A13) describes a circle centered about the origin with radius 1 (the unit circle). The pole diagram of the Butterworth filter, then, is given by Figure A6.

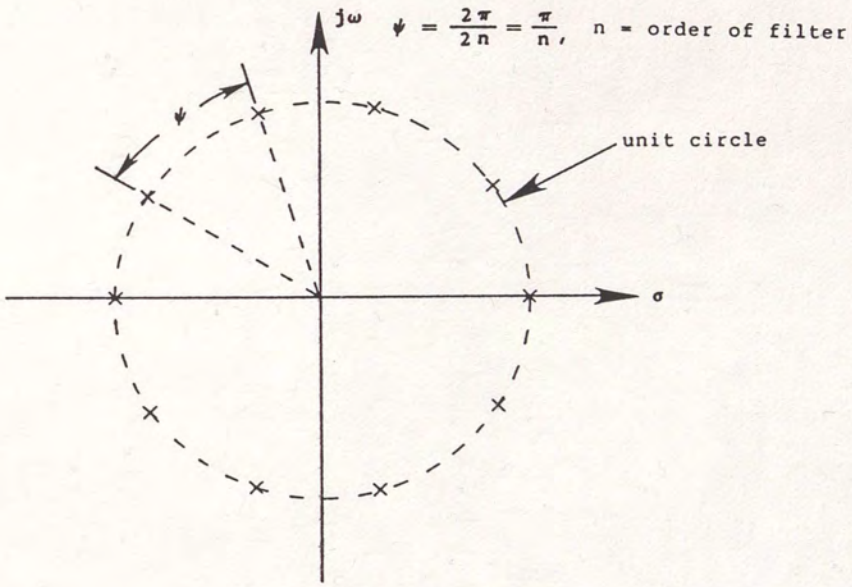


Figure A6. Pole diagram for Butterworth filter. All the poles lie on a unit circle of radius 1.

The pole diagram of the third-order Butterworth filter represented by Figure A3 or Figure A5 is shown in Figure A7.

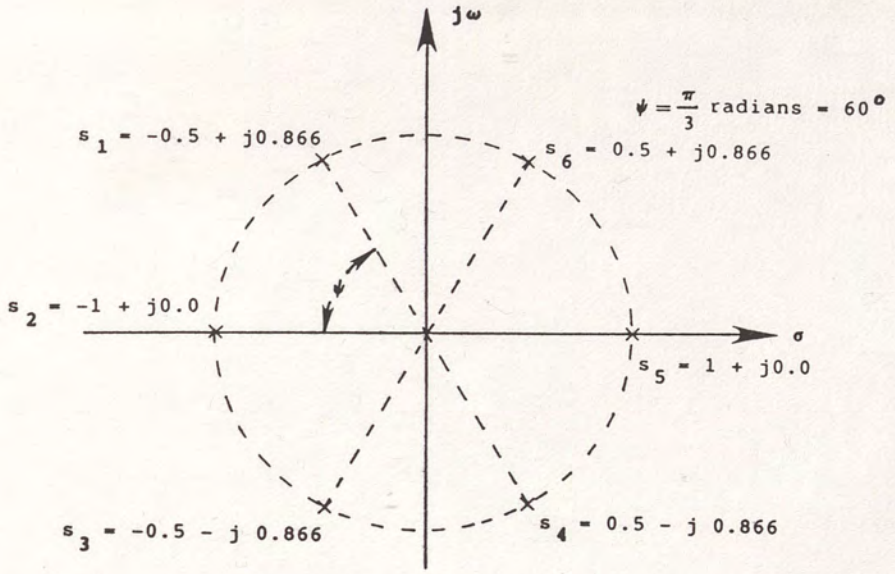


Figure A7. Pole diagram for third-order Butterworth filter.

Equiripple (Chebyshev) Filters

The Butterworth filter detailed in the previous section has a fairly good passband response and a fairly steep rolloff in the transition region (the region near the cutoff frequency). For some applications, though, the attenuation near the cutoff frequency for the Butterworth filter might be too high; for example, the third-order Butterworth filter in Figure A3 or Figure A5 at $\omega/\omega_c = 0.9$ has a power response value of

$$\left|T\left(j\,\frac{\omega}{\omega_c}\right)\right|^2_{\frac{\omega}{\omega_c}=0.9} = \frac{1}{1 + (0.9)^{(2)(3)}} = \frac{1}{1 + (0.9)^6}$$

$$= \frac{1}{1.53144} = 0.65298 = -1.85 \text{ dB}$$

So at 90% of the cutoff frequency, the third-order Butterworth filter attenuates the signal power by almost 2 dB. This is a

fairly significant reduction. To reduce the attenuation of a lowpass filter in the transition region, a ripple that oscillates evenly above and below a certain mean value in the passband is introduced, causing the response in the transition region to increase. This is shown in Figure A8.

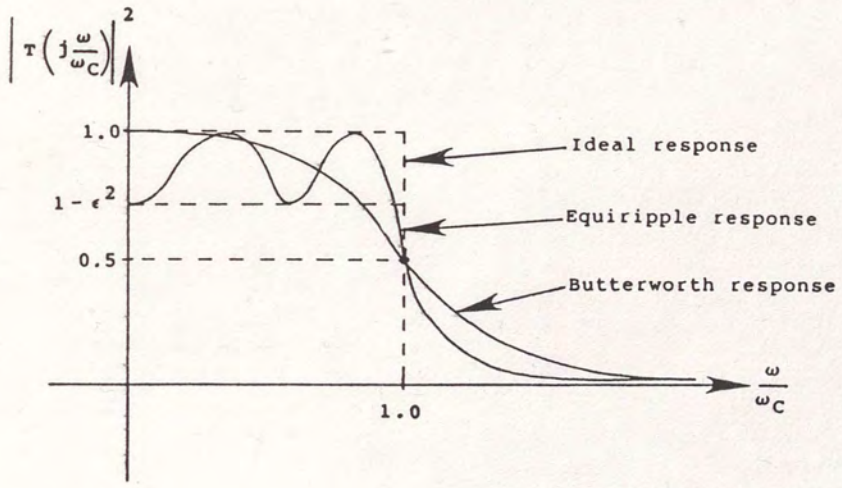


Figure A8. Comparison of Butterworth and equiripple responses.

In Figure A8, it is seen that the response of the equiripple filter falls off more steeply than the response of the Butterworth filter in the transition region. Thus, it approximates the ideal lowpass filter response more closely than the Butterworth response. ε is the ripple factor, usually expressed in decibels.

$$\text{Ripple factor in dB} = R_{dB} = 10 \log (\varepsilon^2 + 1) \qquad \text{(A14)}$$

Solving equation (A14) for ε^2 yields

$$\varepsilon^2 = 10^{R_{dB}/10} - 1 \tag{A15}$$

The power response function for the equiripple filter, from equation (A1), is

$$\left|T\left(j\frac{\omega}{\omega_c}\right)\right|^2 = \frac{1}{1 + \varepsilon^2 C_n^2\left(\frac{\omega}{\omega_c}\right)} \tag{A16}$$

where ε^2 (the square of the absolute-value ripple factor) is defined by equation (A15) and ω_c is the 3 dB cutoff frequency. $C_n(\omega/\omega_c)$ describes a class of polynomials called the Chebyshev polynomials, which are defined by the following recursive relationship

$$C_0\left(\frac{\omega}{\omega_c}\right) = 1$$

$$C_1\left(\frac{\omega}{\omega_c}\right) = \frac{\omega}{\omega_c}$$

$$C_2\left(\frac{\omega}{\omega_c}\right) = 2\left(\frac{\omega}{\omega_c}\right)\left(\frac{\omega}{\omega_c}\right) - 1 = 2\left(\frac{\omega}{\omega_c}\right)^2 - 1$$

$$C_3\left(\frac{\omega}{\omega_c}\right) = 2\left(\frac{\omega}{\omega_c}\right)\left[2\left(\frac{\omega}{\omega_c}\right)^2 - 1\right] - \frac{\omega}{\omega_c} = 4\left(\frac{\omega}{\omega_c}\right)^3 - \frac{\omega}{\omega_c}$$

$$\vdots$$

$$C_{n+1}\left(\frac{\omega}{\omega_c}\right) = 2\left(\frac{\omega}{\omega_c}\right)C_n\left(\frac{\omega}{\omega_c}\right) - C_{n-1}\left(\frac{\omega}{\omega_c}\right) \tag{A17}$$

Equation (A17) can be used to generate Chebyshev polynomials of any order. Because the power response of the equiripple filter

is defined in terms of Chebyshev polynomials, the equiripple filter is often called a Chebyshev filter. The design of a Chebyshev filter follows the same procedure as the Butterworth filter design: the left-hand plane poles of the s-domain power response function are determined; these poles are used to generate a voltage transfer function similar in form to equation (A6); finally, this transfer function is related to a filter circuit similar to Figure A3 or Figure A5. Noting that

$$s = j\frac{\omega}{\omega_c} \Rightarrow \frac{\omega}{\omega_c} = \frac{s}{j}$$

Equation (A16) becomes

$$|T(s)|^2 = \frac{1}{1 + \varepsilon^2 C_n^2\left(\frac{s}{j}\right)}$$

The poles of this function are

$$s_m = -\frac{\sinh \phi}{\cosh \psi} \sin\left(\frac{2k+1}{2n}\right)\pi + j\frac{\cosh \phi}{\cosh \psi} \cos\left(\frac{2k+1}{2n}\right)\pi \qquad \text{(A18)}$$

$$\phi = \frac{1}{n}\sinh^{-1}\left(\frac{1}{\varepsilon}\right); \psi = \frac{1}{n}\cosh^{-1}\left(\frac{1}{\varepsilon}\right); m=1,2,3,\ldots,2n; k=0,1,2,\ldots,2n-1$$

The left-hand plane poles are those poles where K = 0, 1, 2, ..., n-1, in equation (A18). The s-domain power response function can be rewritten

$$|T(s)|^2 = \frac{1}{K_n(s)K_n(-s)} = T(s)T^*(-s)$$

where $K_n(s)$ is a polynomial in s that is not a true Chebyshev polynomial but is related to the Chebyshev polynomial. Here,

$$K_n(s) = \prod_{m=1}^{n} (s - s_m)$$

$$= \prod_{k=0}^{n-1} [s + \frac{\sinh\phi}{\cosh\psi} \sin(\frac{2k+1}{2n})\pi - j \frac{\cosh\phi}{\cosh\psi} \cos(\frac{2k+1}{2n})\pi] \quad \text{(A19)}$$

$$\phi = \frac{1}{n} \sinh^{-1}(\frac{1}{\varepsilon}); \quad \psi = \frac{1}{n} \cosh^{-1}(\frac{1}{\varepsilon})$$

The voltage transfer function is given by equation (A6); namely,

$$T(s) = \frac{1}{K_n(s)} \quad \text{(A20)}$$

This transfer function is then converted into a filter circuit, in the same manner as was done for the Butterworth transfer function.

Using equations (A19) and (A20), a Chebyshev filter circuit can be generated, for a given order n and ripple factor R_{dB}. The procedure is as follows. It is desired to generate a third-order Chebyshev (equiripple) filter circuit with a ripple factor of 0.5 dB. First, the absolute ripple factor ε^2 is calculated from equation (A15)

$$\varepsilon^2 = 10^{\frac{0.5}{10}} - 1 = 1.12202 - 1 = 0.12202$$

$$\varepsilon = \sqrt{0.12202} = 0.34931$$

From equation (A19)

$$\phi = \frac{1}{3} \sinh^{-1} \left(\frac{1}{0.12202}\right) = \frac{1}{3} \cdot \sinh^{-1} (8.19538) = 0.93347$$

$$\psi = \frac{1}{3} \cosh^{-1} \left(\frac{1}{0.12202}\right) = \frac{1}{3} \cdot \cosh^{-1} (8.19538) = 0.93099$$

$$\sinh \phi = \sinh(0.93347) = 1.07507$$

$$\cosh \phi = \cosh(0.93347) = 1.46825$$

$$\cosh \psi = \cosh(0.93099) = 1.46559$$

$$C_3(s) = \left[s + \left(\frac{1.07507}{1.46559}\right) \sin\left(\frac{\pi}{6}\right) - j\left(\frac{1.46825}{1.46559}\right) \cos\left(\frac{\pi}{6}\right)\right]$$

$$x \left[s + \left(\frac{1.07507}{1.46559}\right) \sin\left(\frac{\pi}{2}\right) - j\left(\frac{1.46825}{1.46559}\right) \cos\left(\frac{\pi}{2}\right)\right]$$

$$x \left[s + \left(\frac{1.07507}{1.46559}\right) \sin\left(\frac{5\pi}{6}\right) - j\left(\frac{1.46825}{1.46559}\right) \cos\left(\frac{5\pi}{6}\right)\right] \quad \text{(A21)}$$

$$C_3(s) = (s+0.36677 - j0.8676)(s+0.73354)(s+0.36677+j0.8676)$$

$$= s^3 + 1.46708s^2 + 1.42083s + 0.64753$$

$$= 0.64753 \, (1.54433s^3 + 2.26566s^2 + 2.19423s + 1)$$

The voltage transfer function is

$$T(s) = \frac{1}{0.64753 \, (1.54433s^3 + 2.26566s^2 + 2.19423s + 1} \quad \text{(A22)}$$

$$= \frac{1.54433}{1.54433s^3 + 2.26566s^2 + 2.19423s + 1}$$

This function is not in the standard filter function form because at s = 0, it is not equal to 1. To rectify this, T(s) is normalized to unity, which yields

$$T(s)_{norm} = \frac{1}{1.54433s^3 + 2.26566s^2 + 2.19423s + 1} \qquad \text{(A23)}$$

The poles of equation (A23) are still those expressed in equation (A21); this means that equation (A23) describes the same system as equation (A22) does. It is seen that equation (A23) is in the form of the Sallen and Key lowpass filter circuit transfer function

$$T_3(s) = \frac{1}{R^3C_1C_2C_3s^3 + 2R^2(C_1C_3+C_2C_3)s^2 + R(C_1+3C_3)s + 1} \qquad \text{(A24)}$$

Setting equation (A24) equal to equation (A23) yields, with R = 1Ω:

$$C_1C_2C_3 = 1.54433$$

$$C_1C_3 + C_2C_3 = 1.13283$$

$$C_1 + 3C_3 = 2.19423$$

After some algebra,

$$0.37761C_1^3 - 0.82856C_1^2 + 1.13283C_1 - 1.54483 = 0 \qquad \text{(A25)}$$

$$C_3 = 0.73141 - 0.33333C_1$$

$$C_2 = \frac{1.54433}{C_1 C_3}$$

Solving equation (A25) iteratively for C_1, and substituting this value into the equations for C_2 and C_3 gives

$$C_1 = 1.79300F$$
$$C_2 = 8.08187F$$
$$C_3 = 0.06901F$$

As was done before, these values are scaled to the desired impedance level and cutoff frequency. The result is a Sallen and Key lowpass Chebyshev 0.5 dB ripple filter, with the circuit diagram given by Figure A5.

The pole-zero diagram of the Chebyshev filter needs to be derived. To do this, equation (A18) is broken up into real and imaginary equations:

$$s_m = \sigma_k + j\omega_k = - A \sin \mu + B \cos \mu$$

$$\sigma_k = - A \sin \mu \qquad \text{(A26)}$$

$$\omega_k = B \cos \mu \qquad \text{(A27)}$$

where:

$$A = \frac{\sinh \phi}{\cosh \psi}; \quad B = \frac{\cosh \phi}{\cosh \psi}$$

$$\mu = \left(\frac{2k+1}{2n}\right)\pi$$

Dividing equation (A26) by A and equation (A27) by B and squaring both equations yields

$$\frac{\sigma_k^2}{A^2} = \sin^2 \mu \qquad \text{(A28)}$$

$$\frac{\omega_k^2}{B^2} = \cos^2 \mu \qquad \text{(A29)}$$

Adding equations (A28) and (A29) gives

$$\frac{\sigma_k^2}{A^2} = \frac{\omega_k^2}{B^2} = \sin^2 \mu + \cos^2 \mu$$

or

$$\frac{\sigma_k^2}{A^2} + \frac{\omega_k^2}{B^2} = 1 \qquad \text{(A30)}$$

Equation (A30) is the equation of an ellipse with its major axis parallel to the $j\omega$ axis and its minor axis parallel to the σ axis. Thus, the poles of the Chebyshev filter will lie on an ellipse as shown in Figure A9.

The pole diagram for the third-order Sallen and Key filter whose transfer function is given by equation (A23) is shown in Figure A10.

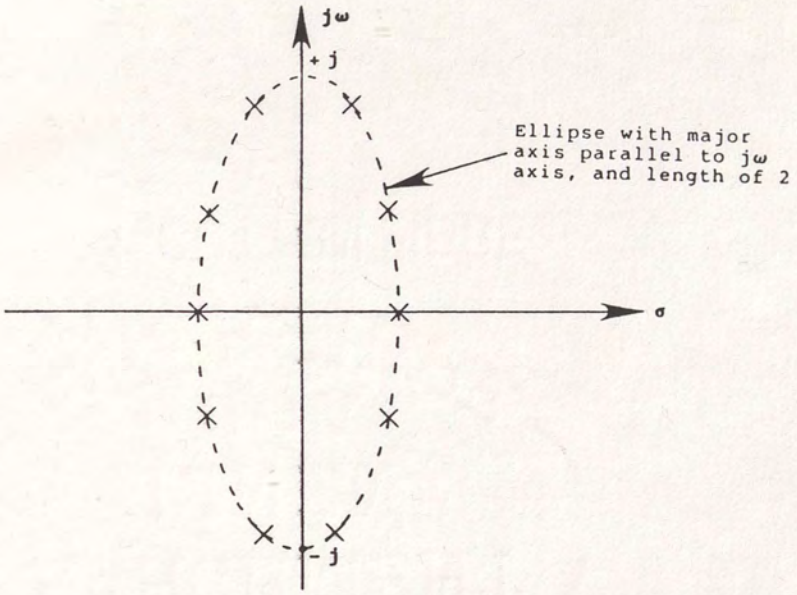


Figure A9. Pole diagram for Chebyshev filter.

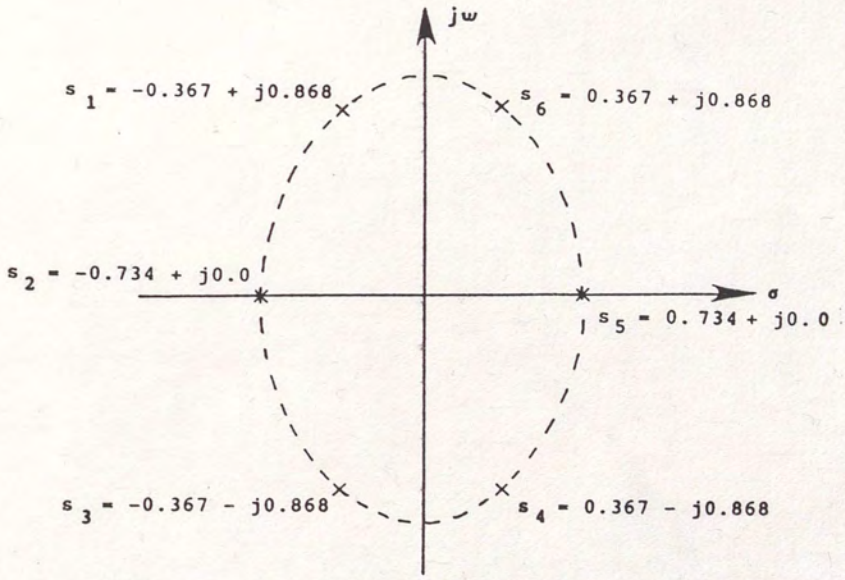


Figure A10. Pole diagram for third-order Chebyshev Sallen and Key filter, with 0.5 dB ripple.

Passband/Stopband Equiripple (Elliptic) Filters

The passband/stopband equiripple filter, often called the elliptic filter, contains a ripple in both the passband and the stopband. This results in a very steep slope in the filter transition region, as shown below in Figure A11.

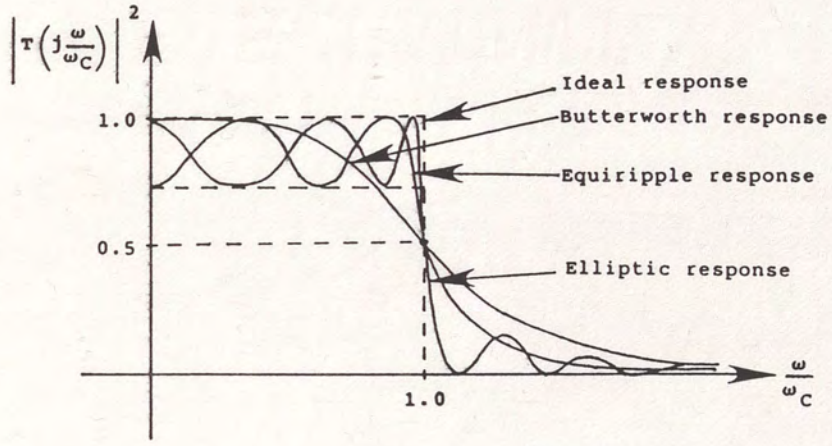


Figure A11. Comparison of Butterworth, equiripple (Chebyshev) and elliptic filters.

In Figure A11, it is evident that the elliptic filter has points in the stopband where the response goes to zero. These points correspond to the zeros of the elliptic filter transfer function. The power response function for the elliptic filter is

$$\left|T\left(j\ \frac{\omega}{\omega_c}\right)\right|^2 = \frac{1}{1 + \varepsilon^2 R_n^{\ 2}(\omega)}$$

where ε is the ripple factor (defined in the previous section), and $R_n(\omega)$ is the Chebyshev rational function (CRF). The CRF is

usually defined in terms of the complex variable, z, where $z = x + jy$.

$$R_n^2(\omega) = T(z)T(-z) = \frac{\left[\prod_{i=1}^{N} (z_i - z)\right]^2}{\prod_{i=1}^{N} (z_i^2 - z^2)} \tag{A31}$$

Equation (A31) is an even function of z. The z_i's are the singularities of the function; N is the number of transmission zeros in the elliptic filter power response function. To be of any use in filter design, though, equation (A31) must be transformed to the s-domain. This can be accomplished by using the following s-to-z mapping function:

$$z^2 = \frac{s^2 + 1}{s^2} \tag{A32}$$

The result of this substitution will be a rational function R(s)R(-s) whose poles and zeros will be related to the singularities of T(z)T(-z).

$$R(s)R(-s) = \left.\frac{\left[\prod_{i=1}^{N} (z_i - z)\right]^2}{\prod_{i=1}^{N} (z_i^2 - z^2)}\right| z^2 = \frac{s^2+1}{s^2} \tag{A33}$$

The voltage transfer function will be

$$T(s) = \frac{1}{\Omega(s)} \tag{A34}$$

where $\Omega(s)$ is defined by the relation

$$\Omega(s)\Omega(-s) = 1 + \varepsilon^2 R(s)R(-s) \qquad \text{(A35)}$$

The number of transmission zeros is related to the order, n, of the elliptical filter by the following formula:

$$N = \begin{cases} \frac{n}{2} + 1, & n \text{ odd} \\ \\ \frac{n}{2}, & n \text{ even} \end{cases}$$

The design of an elliptical filter is as follows. The s-domain transmission zeros for the filter are first specified; they will be a function of the filter response parameters (cutoff frequency, transition rolloff, filter ripple). These transmission zeros are then converted to CRF z-domain singularities using equation (A32). (For any elliptical lowpass filter, there will be a transmission zero at $s = \infty$; this converts to the singularity $z = 1$.) Equation (A33) is used to generate the rational function $R(s)R(-s)$; finally, equations (A35) and (A34) are used to calculate the voltage transfer function. Using the network synthesis methods outlined previously, this transfer function is converted into a filter circuit. The topology of this circuit will be different from the Butterworth and Chebyshev topologies, because the elliptical filter transfer function has terms in the numerator as well as the denominator.

Maximally Flat Time Delay (Bessel) Filters

Introduction

In the previous sections, filters whose power response functions approximated the ideal lowpass characteristic were investigated. In many filter applications, however, it is desirable that the time delay in the filter passband between the filter input and filter output be constant. In other words, the filter should have the time delay response shown below in Figure A12.

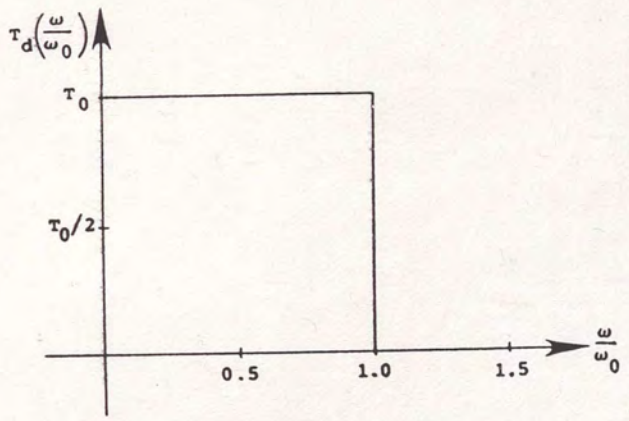


Figure A12. Ideal lowpass filter time delay response.

In Figure A12, ω_0 is the reciprocal of the time delay T_o ($\omega_o = 1/T_o$). In the passband of this filter, if an input x(t) is applied, the output y(t) will be a scaled, shifted version of x(t); that is, $y(t) = K\, x\,(t - T_o)$. If a signal $u(t) = \sin\omega t$ is sent through the filter, the output will be $y_1(t) = \sin[\omega (t - T_o)]$ $= \sin(\omega t - \omega T_o)$. If the frequency of u(t) is doubled [u(t) = sin

$2\omega t]$, the output is $y_2(t) = \sin[2\omega(t - T_o)] = \sin(2\omega t - 2\omega T_o)$. It is seen that the phase shift of $y_2(t)$ is twice the phase shift of $y_1(t)$; when the frequency is doubled, the phase shift doubles. Thus, the constant time delay lowpass filter has a linear phase characteristic. This property can also be deduced from the relation between time delay and phase, which is

$$T_d\left(\frac{\omega}{\omega_o}\right) = -\frac{d\,\beta\left(\frac{\omega}{\omega_o}\right)}{d\,\frac{\omega}{\omega_o}} = \beta'\left(\frac{\omega}{\omega_o}\right)$$

where $\beta(\omega/\omega_o)$ is the characteristic phase function of the filter. If $T_d(\omega/\omega_o)$ is constant, then $\beta(\omega/\omega_o)$ must be a linear function, since the derivative of a linear function is a constant. As was the case with the ideal power response characteristic, the ideal time delay characteristic cannot be realized with a finite number of realizable filter elements. An approximation function must be used. In the following sections, this approximation function will be generated and applied to lowpass filter circuits.

The Bessel Polynomial Approximation

If a signal x(t) is input into a constant time delay filter, the output will be

$$y(t) = Kx(t - T_o) \qquad \text{(A36)}$$

where K is an attenuation factor and T_o is the time delay. Taking the Laplace transform of both sides of equation (A36) yields

$$y(s) = Kx(s)e^{-sT_o} \tag{A37}$$

With $T_o = 1$ (unity time delay), equation (A37) can be rewritten:

$$y(s) = Kx(s)e^{-s} \tag{A38}$$

Solving equation (A38) for the transfer function T(s) yields

$$T(s) = \frac{y(s)}{kx(s)} = e^{-s}$$

The transfer function for the constant time delay filter, then, is $T(s) = e^{-s}$. Since

$$\sinh s = \frac{e^{s} - e^{-s}}{2} \; ; \; \cosh s = \frac{e^{s} + e^{-s}}{2}$$

the transfer function can be written

$$T(s) = \frac{1}{\sinh s + \cosh s} \tag{A39}$$

A polynomial can be generated from the denominator of equation (A39) by expanding sinh s and cosh s in an infinite series:

$$\sinh s = s + \frac{s^3}{3!} + \frac{s^5}{5!} + \frac{s^7}{7!} + \ldots$$

$$\cosh s = 1 + \frac{s^2}{2!} + \frac{s^4}{4!} + \frac{s^6}{6!} + \ldots$$

Equation (A39) then becomes

$$T(s) = \frac{1}{1 + s + \frac{s^2}{2!} + \frac{s^3}{3!} + \frac{s^4}{4!} + \frac{s^5}{5!} + \frac{s^6}{6!} + \ldots} \qquad \text{(A40)}$$

The order of T(s) is the exponent of the highest power term in the denominator. Substituting $s = j(\omega/\omega_o)$, equation (A40) becomes

$$T\left(\frac{\omega}{\omega_o}\right) = \frac{1}{1+j\frac{\omega}{\omega_o} - \frac{\omega^2}{2!\omega_o^2} - j\frac{\omega^3}{3!\omega_o^3} + \frac{\omega^4}{4!\omega_o^4} + j\frac{\omega^5}{5!\omega_o^5} - \frac{\omega^6}{6!\omega_o^6} - \ldots} \qquad \text{(A41)}$$

Equation (A41) can be rewritten

$$T\left(\frac{\omega}{\omega_o}\right) = \frac{1}{\left(1 - \frac{\omega^2}{2!\omega_o^2} + \frac{\omega^4}{4!\omega_o^4} - \frac{\omega^6}{6!\omega_o^6} + \ldots\right) + j\left(\frac{\omega}{\omega_o} - \frac{\omega^3}{3!\omega_o^3} + \frac{\omega^5}{5!\omega_o^5} - \ldots\right)} \qquad \text{(A42)}$$

The magnitude and phase of equation (A42) are

$$T\left(\frac{\omega}{\omega_o}\right) = \frac{1}{\sqrt{\left(1 - \frac{\omega^2}{2!\omega_o^2} + \frac{\omega^4}{4!\omega_o^4} - \frac{\omega^6}{6!\omega_o^6} + \ldots\right)^2 + \left(\frac{\omega}{\omega_o} - \frac{\omega^3}{3!\omega_o^3} + \frac{\omega^5}{5!\omega_o^5} - \ldots\right)^2}} \qquad \text{(A43)}$$

$$T\left(\frac{\omega}{\omega_o}\right) = \tan^{-1}\left[-\frac{\omega}{\omega_o}\left(\frac{1 - \frac{\omega^2}{3!\omega_o^2} + \frac{\omega^2}{5!\omega_o^4} - \cdots}{1 - \frac{\omega^2}{2!\omega_o^2} + \frac{\omega^2}{4!\omega_o^4} - \cdots}\right)\right] \qquad \text{(A44)}$$

Equations (A43) and (A44) were programmed on a computer and the program was run for a third-order constant time delay filter with a delay of 100 μsec (corresponding to a cutoff frequency ω_o of 10 KHz). The magnitude and phase were plotted from 10 KHz to 1 MHz and are shown in Figure A13.

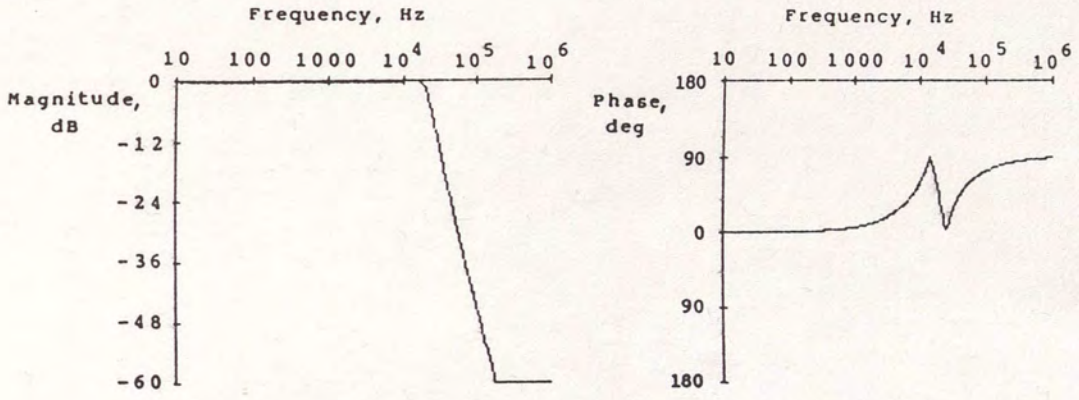


Figure A13. Magnitude and phase response of third-order constant time delay filter with 100 μsec time delay.

Although equations (A43) and (A44) give a good insight into the behavior of constant time delay filters of various orders, they are not much help in the actual synthesis and design of such filters. In this case, a polynomial similar in form to the Butterworth polynomial in equation (A5) needs to be generated. The denominator of equation (A39) can be rewritten

$$\sinh s + \cosh s = s^n[L_n(\tfrac{1}{s}) + M_n(\tfrac{1}{s})] \qquad \text{(A45)}$$

where $L_n(1/s)$ and $M_n(1/s)$ are defined by

$$\frac{L_n(\frac{1}{s})}{M_n(\frac{1}{s})} = \text{nth order approximation to } \frac{\sinh s}{\cosh s}$$

$$= \frac{1}{s} + \cfrac{1}{\frac{3}{s} + \cfrac{1}{\frac{5}{s} + \cfrac{\quad}{\quad \vdots \quad + \cfrac{1}{\frac{2n-1}{s}}}}}$$

Here (sinh s/cosh s) is the phase angle of the ideal constant time delay transfer function $T(s) = e^{-s}$. $L_n(1/s)$ and $M_n(1/s)$ are generated using the recursive relations

$$L_{-1} = L_o = 1$$

$$M_{-1} = M_o = 1$$

$$L_n(\tfrac{1}{s}) = \frac{2n-1}{s} L_{n-1}(\tfrac{1}{s}) + L_{n-2}(\tfrac{1}{s})$$

$$M_n(\tfrac{1}{s}) = \frac{2n-1}{s} M_{n-1}(\tfrac{1}{s}) + M_{n-2}(\tfrac{1}{s})$$

The sum of $L_n(1/s)$ and $M_n(1/s)$ is another polynomial, referred to as the Bessel polynomial. This polynomial is defined by the same recursive formula as the formula for $L_n(1/s)$ and $M_n(1/s)$; namely,

$$w_n(\tfrac{1}{s}) = L_n(\tfrac{1}{s}) + M_n(\tfrac{1}{s}) = \frac{2n-1}{s} w_{n-1}(\tfrac{1}{s}) + w_{n-2}(\tfrac{1}{s}) \qquad \text{(A46)}$$

with $w_{-1}(1/s) = w_o(1/s) = 1$. Equation (A46) can also be written as a sum:

$$w_n(\tfrac{1}{s}) = \sum_{k=0}^{n} \frac{(n+k)!}{(n-k)!k!(2s)^k} \qquad \text{(A47)}$$

Combining equations (A39), (A45), (A46) and (A47), the transfer function of the constant time delay lowpass filter can be written in terms of Bessel polynomials as

$$T(s) = \frac{1}{s^n w_n(\tfrac{1}{s})} = \frac{1}{\sum_{k=0}^{n} \frac{(2n-k)!s^k}{2^{n-k}\, k!(n-k)!}} \qquad \text{(A48)}$$

This formula can be used to generate a transfer function of any order, whose denominator will be a polynomial in s similar to the Butterworth or Chebyshev polynomial. Since the constant time delay filter transfer function is defined in terms of Bessel polynomials, this filter is often called a Bessel filter. It is also called a maximally flat delay filter. For a third-order Bessel filter, the transfer function is

$$T_3(s) = \frac{1}{(\frac{6!}{8.1.3!})(1) + (\frac{5!}{4.1.2!})s + (\frac{4!}{2.2!1})s^2 + (\frac{3!}{1.3!1})s^3} \qquad \text{(A49)}$$

$$= \frac{1}{s^3 + 6s^2 + 15s + 15}$$

Properties of the Bessel Filter

Bessel polynomials are most frequently used to characterize Bessel filter transfer functions, since they are in a fairly convenient form (at least for low orders of n) and are extensively tabulated. The real reason for using Bessel polynomials, though, is their relation to the well-known Bessel functions; this relation makes it possible to derive a fairly straightforward formula for the time delay of the Bessel filter as a function of frequency and filter order n. Indeed, when $s = j(\omega/\omega_o)$,

$$\omega_n\left(\frac{1}{j\,\frac{\omega}{\omega_o}}\right) = j^{-n}\sqrt{\frac{\pi\,\frac{\omega}{\omega_o}}{2}}\; e^{j\,\frac{\omega}{\omega_o}}\left[(-1)^n\, J_{-(n+\frac{1}{2})}\left(\frac{\omega}{\omega_o}\right) - jJ_{(n+\frac{1}{2})}\left(\frac{\omega}{\omega_o}\right)\right] \quad \text{(A50)}$$

where $J_{\pm(n+1/2)}(x)$ is the half-order Bessel function defined by:

$$J_{\pm(n+1/2)}(x) = \sum_{k=0}^{\infty} \frac{(-1)^k}{k!\,\Gamma[\pm(n+1/2)+k+1]}\left(\frac{x}{2}\right)^{\pm(n+1/2)+2k}$$

Equation (A50) can be used to derive the time delay of the Bessel filter, which is

$$T_d\left(\frac{\omega}{\omega_o}\right) = T_o\left[1 - \frac{1}{\left(\frac{\omega}{\omega_o}\right)^2\left[\frac{\pi\omega}{\omega_o}\, J^2_{-(n+1/2)}\left(\frac{\omega}{\omega_o}\right) + J^2_{(n+1/2)}\left(\frac{\omega}{\omega_o}\right)\right]}\right] \quad \text{(A51)}$$

Equation (A51) can be expanded in a McLaurin series, where the terms are of the form $K(\omega/\omega_o)^n$.

$$T_d\left(\frac{\omega}{\omega_o}\right) = T_o\left[1 - \left(\frac{2^n n!}{(2n)!}\right)^2\left(\frac{\omega}{\omega_o}\right)^{2n} + \left(\frac{2^n n!}{(2n)!}\right)\left(\frac{\omega}{\omega_o}\right)^{2n+2}\left(\frac{1}{2n-1}\right)\right. \quad \text{(A52)}$$

$$\left. - \left(\frac{2^n h!}{(2n)!}\right)^2\left(\frac{\omega}{\omega_o}\right)^{2n+4}\left(\frac{2(n-2)}{(2n-1)^2(2n-3)}\right) + \cdots\right]$$

From equation (A52), it is seen that when $\omega/\omega_o = 0$, $T_d(\omega/\omega_o) = T_o$. Usually, three or four terms of equation (A52) are sufficient to characterize the filter time delay accurately. For the third-order Bessel filter, whose transfer function is given by equation (A49), the time delay becomes

$$T_{d,3}\left(\frac{\omega}{\omega_o}\right) = T_o\left[1 - \left(\frac{8.3!}{6!}\right)^2\left(\frac{\omega}{\omega_o}\right)^6 + \left(\frac{8.3!}{6!}\right)\left(\frac{1}{5}\right)\left(\frac{\omega}{\omega_o}\right)^8\right.$$

$$\left. - \left(\frac{8.3!}{6!}\right)^2\left(\frac{2}{25.3}\right)\left(\frac{\omega}{\omega_o}\right)^{10}\right]$$

$$T_{d,3}\left(\frac{\omega}{\omega_o}\right) = T_o\left[1 - 0.06667\left(\frac{\omega}{\omega_o}\right)^6 + 0.01333\left(\frac{\omega}{\omega_o}\right)^8 - 0.00178\left(\frac{\omega}{\omega_o}\right)^{10}\right]$$

At $\omega/\omega_o = 1$ (the cutoff frequency), the time delay of the third-order Bessel filter is

$$T_{d,3} = T_o(1 - 0.06667 + 0.01333 - 0.00178)$$

$$= 0.94489\ T_o$$

It is seen that the time delay varies only slightly over the passband of the filter (less than 5%). Hence, with a relatively simple filter, it is possible to get a time delay that is nearly constant.

The synthesis of a Bessel filter follows the same procedure as the synthesis of the filters outlined in the previous sections. Thus it is possible to construct a Bessel Sallen and Key filter circuit by equating equation (A48) with the Sallen and Key transfer function, and solving for the normalized capacitor values. In fact, the output noise filter in the signal conditioner outlined in Chapter II is a fifth-order linear phase Sallen and Key lowpass filter which consists of a third-order Bessel filter and a second-order Bessel filter cascaded together as shown in Figure A14.

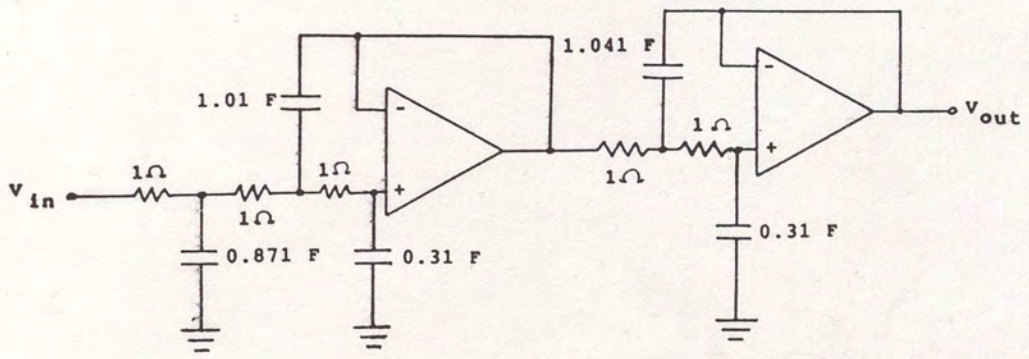


Figure A14. Fifth-order Sallen and Key lowpass noise filter for signal conditioner.

The capacitor values in Figure A14 are normalized values and were obtained from a table of Bessel filter elements. The maximally

flat time-delay property of the circuit in Figure A14 makes it ideal for post-filtering of the speech signal in the signal conditioner, since the difference between the time delays of the frequency components of the speech signal is so small. This means that the speech signal can be sent from the variable-frequency lowpass filter through this filter to the A/D input of the digital speech processor with almost no amplitude or phase distortion. Another desirable property of the Bessel filter is the fact that it has no overshoot at the output when its input is a step function. This makes it ideally suited for applications where over-damping is important, such as voltage spike protection circuitry. The time-domain impulse response of the Bessel filter dies down almost immediately after the initial response pulse; there is almost no oscillation or "ringing." While the Bessel filter has very desirable time delay, phase and step responses, it has decidedly poorer magnitude response than the Butterworth, Chebyshev or elliptical lowpass filters in that the rolloff in the transition region is not as steep. This means that the Bessel filter will need more elements than the Butterworth, Chebyshev or elliptical filter to realize a desired rolloff characteristic. This may not be a serious disadvantage, since Bessel filter circuits (such as the Sallen and Key circuit) are easily built with relatively inexpensive components.

The s-plane pole-zero diagram of the Bessel filter, interestingly enough, is somewhat similar to the Butterworth

pole-zero diagram, in that all the Bessel filter poles lie on a circle. However, the vertical separation distances between the Bessel filter poles are different from the Butterworth filter pole separation distances. In addition, the angles between successive pole radius vector pairs are not the same; these angles are the same for the Butterworth pole radius vector pairs. Figure A15 shows the s-plane pole-zero diagram for a Bessel filter.

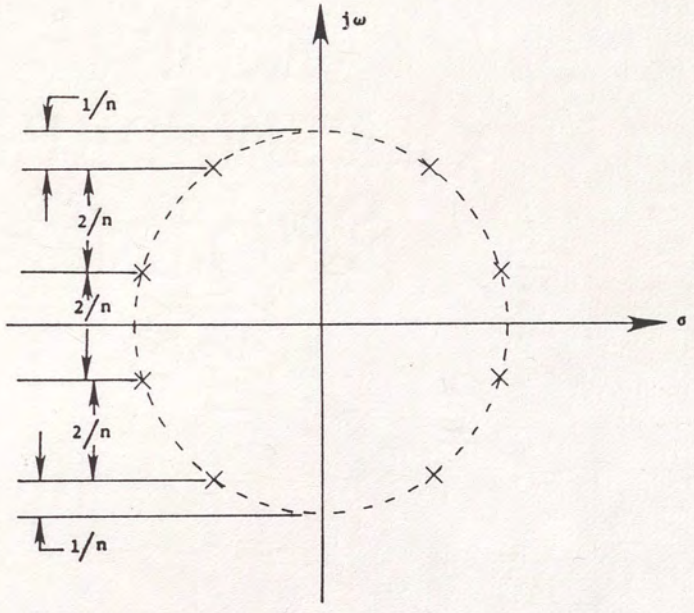


Figure A15. Pole diagram for Bessel filter.

In Figure A15, n is the order of the filter. The pole locations in Figure A15 are approximate, and are derived empirically from the Bessel polynomial roots.

APPENDIX B

DESIGN PROCEDURES

This appendix contains the design and test procedures for the five main sub-systems of the signal conditioner, which are the voltage amplifier, the switched capacitor filter, the linear phase output noise filter, the audio power amplifier and signal level display, and the quad power supply. Design equations and circuit schematics for the sub-systems are given, along with design and testing procedures. Performance characteristics for the sub-systems are given.

Voltage Amplifier

The design requirement here was to come up with a way of amplifying the voltage signal from a microphone, which ranges from about 50 mV peak-to-peak to 250 mV peak-to-peak, to a level that is acceptable to the input port of an A/D converter (8 to 10 V peak-to-peak). The easiest and most effective way to do this is to use an operational amplifier with a single resistive feedback loop as shown in Figure B1. The circuit in Figure B1 is a non-inverting, high input impedance, low output impedance amplifier that uses voltage series feedback. The gain of this amplifier is

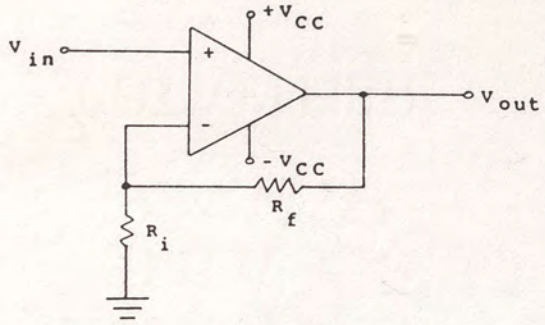


Figure B1. Voltage amplifier consisting of an op amp and a single feedback loop.

$$A_v = 1 + \frac{R_f}{R_i} \qquad \text{(B1)}$$

The voltage amplifier for the signal conditioner consists of a two-stage operational amplifier, with each stage similar to the circuit in Figure B1. The first stage acts as a fixed gain preamplifier, with a gain of 5 (14 dB). This stage amplifies the input microphone signal to around 1 V peak-to-peak; this signal can then be amplified to the required range of 8 to 10 V peak-to-peak by the second stage with only a modest gain. This is advantageous since it cuts down on the d.c. offset voltage of the second stage. The gain of the second stage is variable and can range from approximately unity to 10 (10 dB). This means that the overall gain of the two-stage amplifier can range from 5 (14 dB) to 50 (24 dB). Gain adjust in the second stage is accomplished via a 10 KΩ trimpot in the resistive feedback loop. The operational amplifier used in each stage of the voltage amplifier is the Texas Instruments TL08X JFET op amp. This op

amp features a large maximum output voltage swing (10 V or 20 V peak-to-peak, to 13.5 V or 26 V peak-to-peak, depending on load impedance, with the supply voltage set to ± 15 V), a very high input resistance (10^{12} Ω), high common mode rejection ratio (almost 86 dB), low input noise voltage, low total harmonic distortion (less than 0.004% from d.c. to 10 KHz), and a fairly wide operating bandwidth (d.c. to approximately 300 KHz, with ±10 V supply voltages and a load impedance of 10 KΩ). The op amp is available in a quad 14 pin IC DIP (the TL084), which contains four amplifiers on one chip; this is the IC chip used for the two-stage voltage amplifier (Texas Instruments, Inc. 1980).

The implementation and testing procedures for the voltage amplifier for one channel are as follows. For the first stage, equation (B1) was used to calculate the value of the feedback resistor R_f required to yield a voltage gain of 5, with R_i = 1 KΩ.

$$A_v = 5 = 1 + \frac{R_f}{R_i} = 1 + \frac{R_f}{1\ k\Omega}$$

$$\frac{R_f}{1\ k\Omega} = 5 - 1 = 4$$

$$R_f = (4)(1\ k\Omega) = 4\ k\Omega$$

The single stage amplifier was then implemented using a 3.9 K resistor for R_f (the closest standard resistor value to 4 KΩ). A 1 KHz, 200 mV peak-to-peak sinusoidal signal was input into the

amplifier and the output was monitored on an oscilloscope. The output signal level was 1 V peak-to-peak, and the voltage gain of the amplifier was

$$A_v = \frac{1 \text{ V peak-to-peak}}{0.2 \text{ V peak-to-peak}} = 5$$

which was the desired value. The second stage of the amplifier was implemented with a 10 K Ω trimpot and a 100 Ω resistor inserted into the feedback loop. The output signal from the first stage was connected to the input of the second stage, and the output from the second stage was monitored on an oscilloscope. The 10 K Ω trimpot was set to maximum (roughly 9 KΩ); the output peak-to-peak signal level was recorded and the overall voltage gain was calculated from

$$A_{v,\text{overall}} = \frac{\text{output peak-to-peak voltage}}{0.2 \text{ V}} \qquad \text{(B2)}$$

Various resistors were substituted for the 100 Ω resistor and the output signal amplitude was measured for each of these resistances. The 10 KΩ trimpot was varied from minimum to maximum resistance and the change in output level was observed. It was found that using the 100 Ω resistor in the feedback loop resulted in the widest output level dynamic range, with an adequate level of maximum amplification. The voltage gain at

maximum amplification, from equation (B2), was 50. The entire two-stage amplifier is shown in Figure B2.

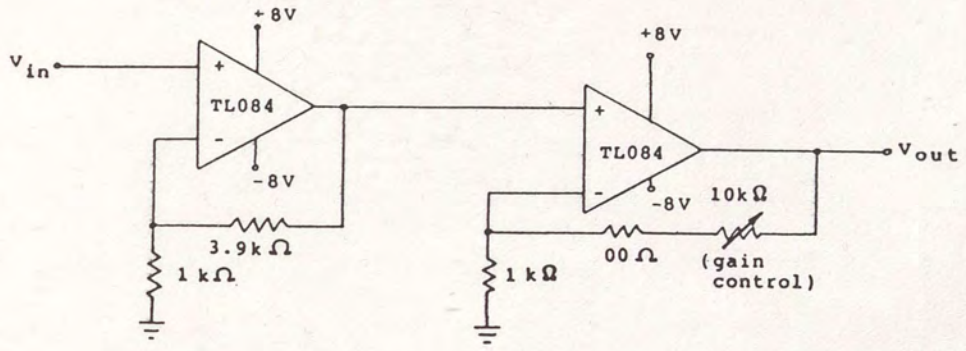


Figure B2. Two-stage voltage amplifier for signal conditioner. D.C. bias offset circuit is not shown.

To eliminate the d.c. offset in the first stage of the amplifier, a voltage divider circuit was connected to the inverting input of the op amp. This circuit is shown below in Figure B3.

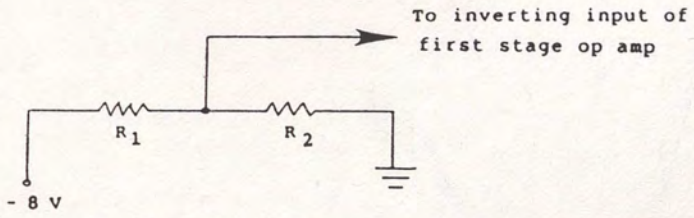


Figure B3. Voltage divider d.c. offset circuit for first stage amplifier.

R_1 and R_2 were adjusted until the d.c. offset at the output signal was zeroed out. The final values of R_1 and R_2 were 100KΩ and 51 Ω, respectively. The d.c. offset circuit reduced the gain

of the first stage of the amplifier; this loss of gain was corrected by putting a 6.2 KΩ resistor in place of the 3.9 KΩ resistor in the first stage feedback loop.

A circuit identical to Figure B2 with a d.c. offset circuit similar to Figure B3 was built and tested for the other channel. The d.c. offset resistors R_1 and R_2 for this circuit were 100KΩ and 100 Ω, respectively. This voltage amplifier and the one mentioned previously were wired on separate TL084 op amp ICs; the bottom pair of op amps on each TL084 chip were used. The op amps were wired in this fashion to reduce the interference and crosstalk between the input and output signals of the two circuits. Figure B4 shows the voltage amplifiers for both channels of the signal conditioner, including d.c. offset circuits.

Switched Capacitor Filter

The switched capacitor filter for the signal conditioner had to bandlimit the amplified output from the voltage amplifier to one of five cutoff frequencies: 1.25 KHz, 2.5 KHz, 5 KHz, 6 KHz and 10 KHz. The design of this filter involved two main objectives: (1) choosing a switched capacitor filter best suited for the design requirements and (2) coming up with a way of generating the required clock signals that would tune the switched capacitor filter to the desired cutoff frequencies. The four possible candidates for the switched capacitor filter were

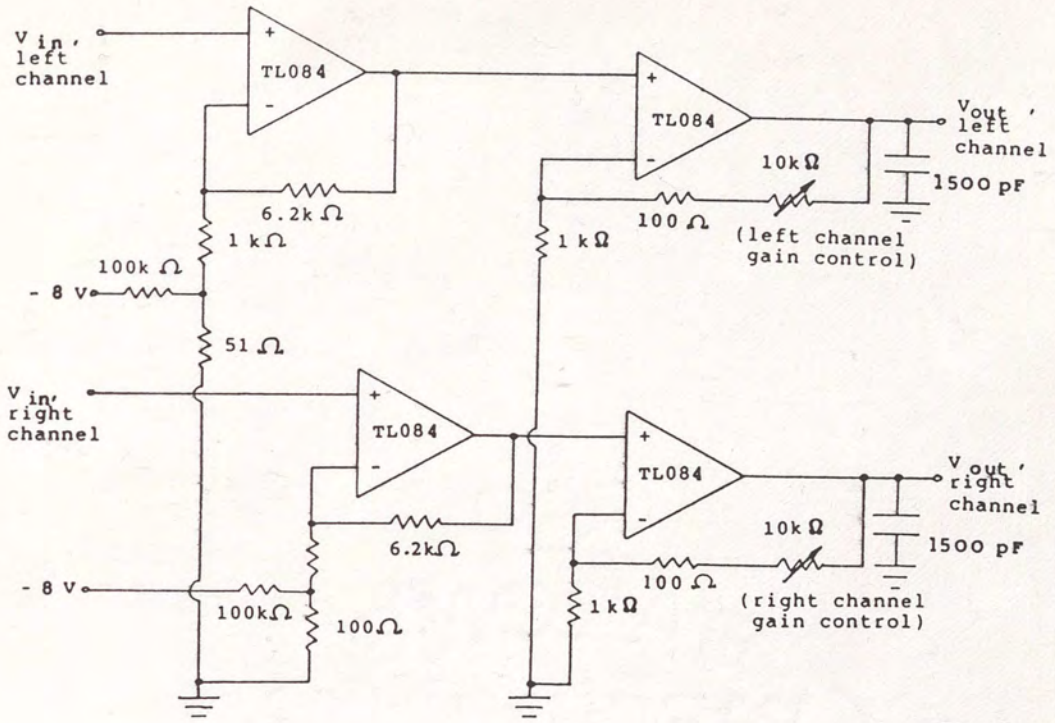


Figure B4. Left and right channel voltage amplifiers.

the Motorola M145414, the Motorola M145415, the EG&G Reticon R5609 and the EG&G Reticon R5613 switched capacitor lowpass filters. Extensive research indicated that these were the only commercially available switched capacitor lowpass filters. Chapter III gives some information on these filters; Table 2 gives more concise information.

Looking at Table 2, it is obvious that the EG&G Reticon filters would work better than the Motorola filters for

relatively large signals (10-16 V peak-to-peak), due to their expanded supply voltage range. Also, their extended cutoff frequency selection range makes these filters more suited to applications where wide signal bandwidth selectivity is required. Even though the cutoff frequency selection range of the Motorola filters is the same as the desired cutoff frequency range of the signal conditioner, it would be more advantageous to use the EG&G Reticon filters in the signal conditioner, at least from this standpoint. From Table 2, it is seen that the Motorola MC145414 has an odd clock to cutoff frequency ratio; this means that the clock that drives the filter would have to be an unusual and not easily implementable design. The MC145415 has a clock to cutoff frequency ratio that lends itself more easily to simple and efficient clock design, but its clock signal input is CMOS compatible only. It would be better to use a TTL type clock driver than a CMOS clock driver, because of the inherent difficulties of system design and implementation with CMOS circuits. From the above observations, it is apparent that the EG&G Reticon switched capacitor filters would be better suited for use in the signal conditioner. The choice of which EG&G Reticon filter to use depends on the type of filtering desired for the bandlimited speech signal. Figures B5 and B6 show the magnitude and time delay response, respectively, of the EG&G Reticon R5609 and R5613 filters.

TABLE 2

SWITCHED CAPACITOR FILTER CHARACTERISTICS

FILTER	TYPE	MAXIMUM/ MINIMUM SUPPLY VOLTAGE	CLOCK SIGNAL INPUT	STOPBAND ROLLOFF (TYPICAL)	CUTOFF FREQUENCY SELECT RANGE	CLOCK TO CUTOFF FREQUENCY RATIO	FEATURES
Motorola MC145414	Fifth-order Elliptic Lowpass	8 V	CMOS or TTL	120 dB per octave	1.25 KHz to 10 KHz	35.56	Two filters are included (18 dB and unity gain); extra uncommitted op amp provided
Motorola MC145415	Fifth-order Linear phase Lowpass	8 V	CMOS	45 dB per octave	1.25 KHz to 10 KHz	64	Same as the MC145414
EG&G Reticon R5609	Seventh-order Elliptic Lowpass	10 V	CMOS or TTL	120 dB per octave	50 Hz to 20 KHz	100	Very easy to apply; does not need external circuitry to set the electrical parameters
EG&G Reticon R5613	Linear phase Lowpass	10 V	CMOS or TTL	20 dB per octave to 120 dB per octave	50 Hz to 20 KHz	128	Same as the R5609

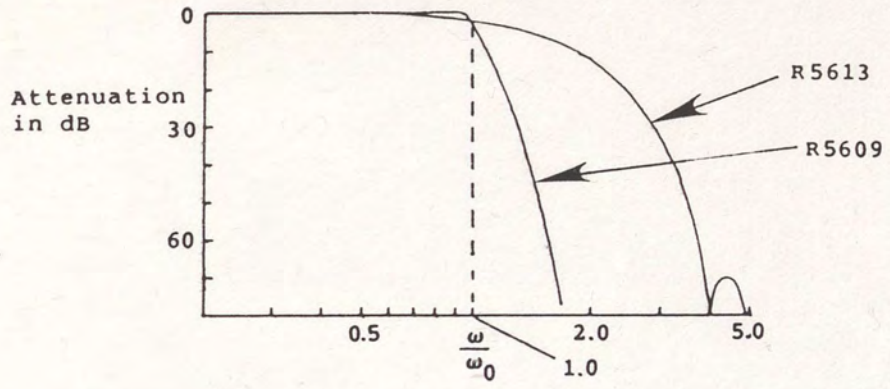


Figure B5. Magnitude responses of EG&G Reticon R5609 and R5613 switched capacitor lowpass filters (EG&G Reticon 1982).

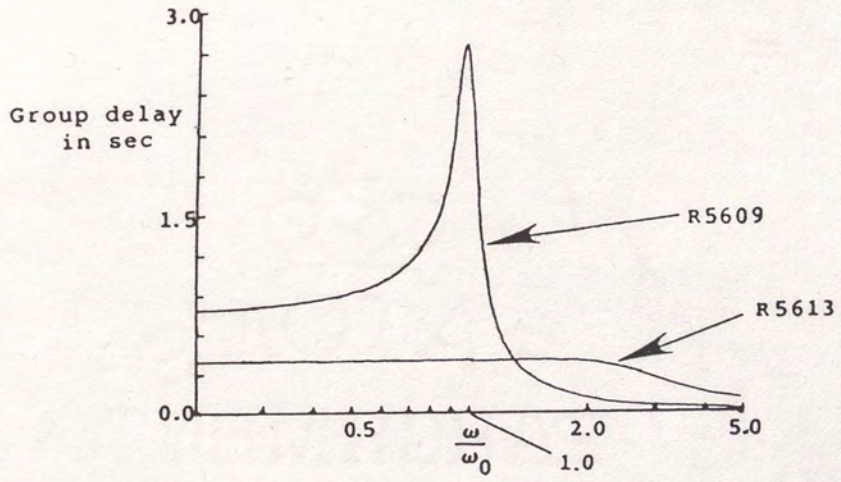


Figure B6. Group delay responses of EG&G Reticon R5609 and R5613 switched capacitor lowpass filters (EG&G Reticon 1982).

From figures B5 and B6, it is seen that the R5609 filter has a better magnitude response than the R5613; the time delay response of the R5609, though, is much worse. From d.c. to roughly half the cutoff frequency, the time delay of the R5609 does not vary that much. From this point onward, however, the time delay becomes highly nonlinear. This means that signals that are passed through the R5609 that have frequencies less than half the cutoff frequency will experience little phase distortion, whereas signals whose frequencies are greater than half the cutoff frequency will contain significant phase distortion, especially if the signal frequencies are near the cutoff frequency. Phase distortion in a speech signal will cause problems in the digital processing of the signal, if the speech processor has an A/D conversion system. The phase distortion of the signal can be eliminated by using the R5613 filter; however, the more gradual rolloff of the R5613 may cause some unwanted high frequency components of the signal to pass through. The phase distortion of the R5609 filter, though, is too excessive for speech signal filtering; this means the R5613 filter is the only logical choice for the signal conditioner switched capacitor lowpass filter.

With the R5613 switched capacitor filter chosen as the signal conditioner variable cutoff frequency lowpass filter, the clock that drives this filter had to be designed. The specified filter cutoff frequencies were 1.25 KHz, 2.5 KHz, 5 KHz, 6 KHz and 10

KHz. Since the required filter clock frequency for the R5613 is 128 times the cutoff frequency, the clock frequencies needed were 160 KHz, 320 KHz, 640 KHz, 768 KHz and 1.28 MHz. These clock signals could be generated in a variety of ways. The method chosen was to use a stable 12.2 MHz crystal clock oscillator (the Motorola K1100AM clock oscillator) in conjunction with a decade counter and two binary counters. The decade and binary counters used were the Texas Instruments SN74LS190 and SN74LS191 counters, respectively. The '190 counter has four output ports that count up or down in binary coded decimal; that is, they count in the sequence ..., 0000, 0001, 0010, ..., 1000, 1001, 0000, 0001, ..., forward or backward, with each count taking place on a positive transition of an input clock signal. To initiate the count, four data ports are set to the desired starting value, and a load signal is sent to a LOAD pin. The output counting ports are all synchronously timed to the clock signal. The '191 counter is similar to the '190; the '191 counts in hexadecimal instead of BCD (..., 0000, 0001, ..., 1110, 1111, 0000, 0001, ...). Figure B7 shows the timing diagrams for the '190 and '191 counters. Here, A, B, C and D are the data ports and are set to a starting value of 0000; Q_A, Q_B, Q_C and Q_D are the output count ports. For simplicity, only the data ports and output count ports are shown.

From Figure B7, it is seen that Q_C on the '190 (pin 6) yields $f_c/10$, where f_c is the clock frequency. Q_A on the '190 or

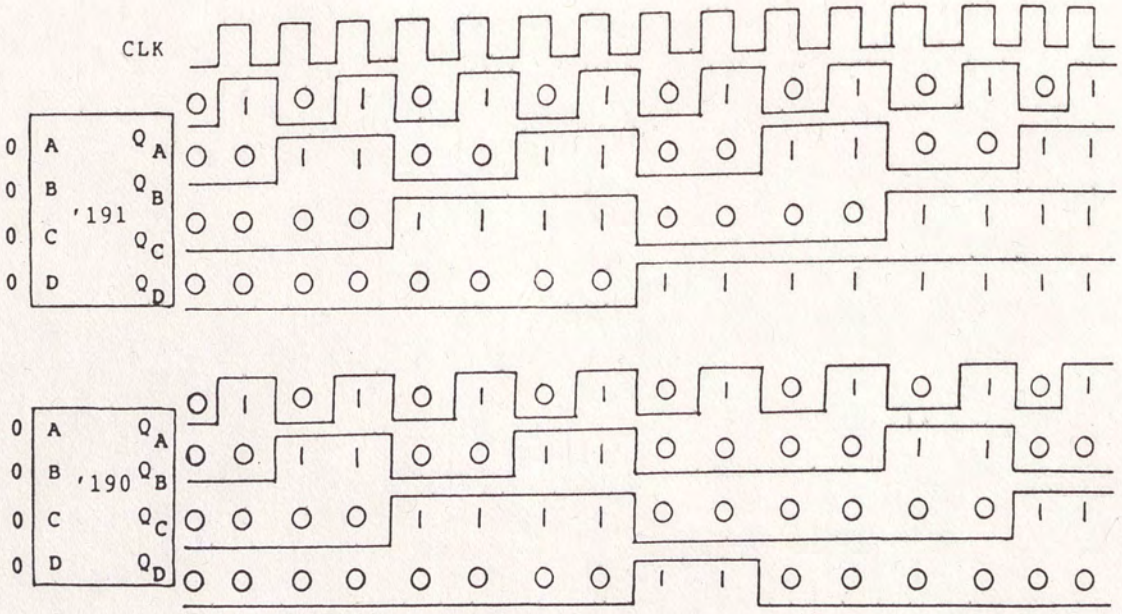


Figure B7. Timing diagrams for the SN74LS190 and SN74LS191 synchronized counters.

the '191 (pin 3) both yield $f_c/2$; Q_B on the '191 (pin 2) gives $f_c/4$. Finally, Q_C on the '191 (pin 6) gives $f_c/8$, and Q_D on the '191 (pin 7) yields $f_c/16$. The reference clock frequency of 12.2 MHz can be factored as follows.

$$12.2 \text{ MHz}/10 = 1.22 \text{ MHz} \quad \text{(B3)}$$

$$12.2 \text{ MHz}/16 = 763 \text{ KHz} \quad \text{(B4)}$$

$$12.2 \text{ MHz}/10/2 = 610 \text{ KHz} \quad \text{(B5)}$$

$$12.2 \text{ MHz}/10/4 = 305 \text{ KHz} \quad \text{(B6)}$$

$$12.2 \text{ MHz}/10/8 = 153 \text{ KHz} \quad \text{(B7)}$$

These clock signals are very close to the desired switched capacitor filter clock signals. Using equations (B3) through (B7), along with Figure B7, a circuit that generates these clock signals can be derived. This circuit, shown in Figure B8, was the one used for the R5613 switched capacitor filter.

Linear Phase Filter

The output linear phase noise filter is primarily designed to filter out the stray clock signals emanating from the switched capacitor filter clock driver that ripple through the filter to the output. The filter is a fifth-order linear phase Sallen and Key circuit and is shown in Appendix A, Figure A14; it was designed using a "cookbook" procedure. First, it was determined that the filter have a cutoff (3 dB) frequency of 25 KHz, with 40

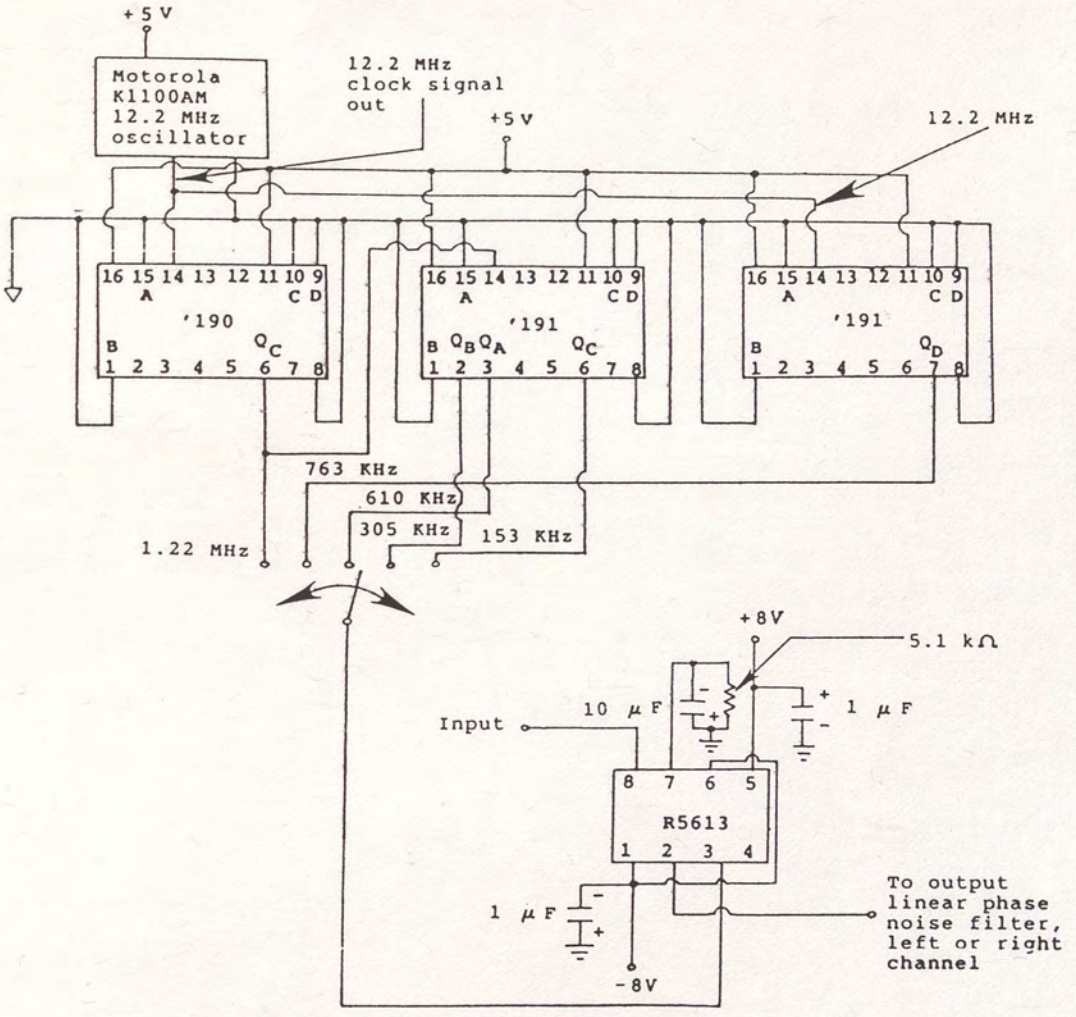


Figure B8. Circuit for generating 153 KHz, 305 KHz, 610 KHz, 763 KHz and 1.22 MHz clock signals.

dB of attenuation at 100 KHz. This would insure adequate attenuation of the stray clock signals. Then, a lowpass steepness factor was calculated.

$$A_s = \frac{\text{40 dB attenuation frequency}}{\text{3 dB attenuation frequency}}$$

$$= \frac{100 \text{ KHz}}{25 \text{ KHz}} = 4$$

Using the Bessel filter stopband attenuation plot shown in Figure B9, the order of the filter required to achieve this attenuation was determined. From the plot, a fifth-order (n = 5) filter could meet the requirements. The actual filter circuit consisted of a third-order Bessel Sallen and Key filter cascaded with a second-order Bessel Sallen and Key filter. These filters are shown in figures A5 and A4, respectively, in Appendix A. The normalized capacitor values for these filters were found from a table of Bessel active lowpass filter element values displayed in Table 3.

The normalized fifth-order filter values, therefore, were

$$C_1' = 1.01F$$

$$C_2' = 0.8712F$$

$$C_3' = 0.3095F$$

$$C_4' = 1.041F$$

$$C_5' = 0.31F$$

$$R = 1$$

TABLE 3

NORMALIZED BESSEL FILTER ELEMENT VALUES

FILTER ORDER N	C_1	C_2	C_3
2	0.9066	0.68	--
3	1.423	0.988	2.538
4	0.7351	0.6746	--
	1.012	0.39	--
5	1.01	0.8712	0.3095
	1.041	0.31	--
6	0.6352	0.61	--
	0.7225	0.4835	--
	1.073	0.2561	--
7	0.8532	0.7792	0.3027
	0.725	0.4151	--
	1.1	0.2164	--
8	0.5673	0.554	--
	0.609	0.4861	--
	0.7257	0.359	--
	1.116	0.1857	--

SOURCE: Williams (1981)

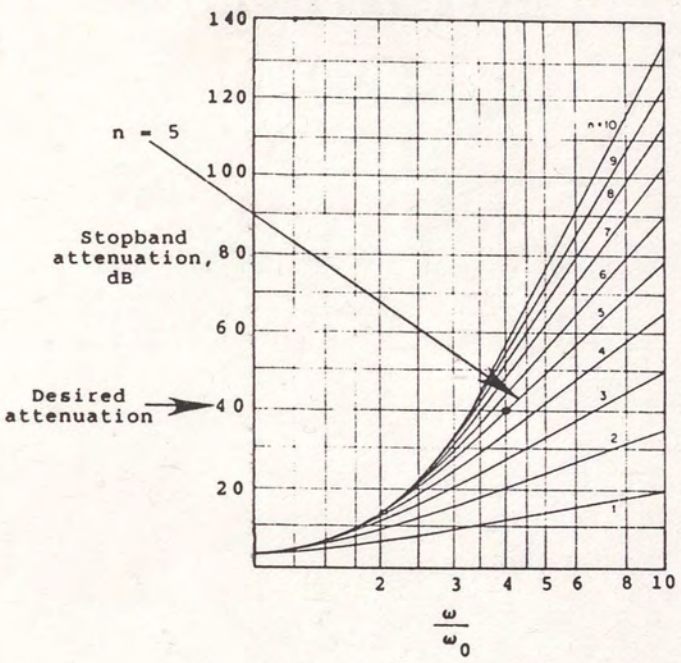


Figure B9. Stopband attenuation versus normalized frequency for various orders of Bessel filters (Williams 1981).

Setting R = 1 K Ω, the denormalized capacitor values were calculated using equation (A9) in Appendix A.

$$C_1 = \frac{C_{1'}}{R\omega_c} = \frac{1.01}{(10^3)(2\pi)(2.5 \times 10^4)} = 6.43 \times 10^{-9} \text{ F} = 6.43 \text{ nF}$$

$$C_2 = \frac{0.8712}{(10^3)(2\pi)(2.5 \times 10^4)} = 5.55 \text{ nF}$$

$$C_3 = \frac{0.3095}{(10^3)(2\pi)(2.5 \times 10^4)} = 1.97 \text{ nF}$$

$$C_4 = \frac{1.041}{(10^3)(2\pi)(2.5 \times 10^4)} = 6.63 \text{ nF}$$

$$C_5 = \frac{0.31}{(10^3)(2\pi)(2.5 \times 10^4)} = 1.97 \text{ nF}$$

The filter was constructed and tested using two TL084 op amps and standard capacitor values that were closest to the values calculated above. An identical filter was built for the other channel and both filters were connected to the outputs of the left and right voltage amplifiers. The voltage amplifier and linear phase filter were tested with a 0.2 V peak-to-peak input signal; it was found that the filters had almost no effect on the amplified left and right signal levels. The circuit diagram for the filter (left or right channel) is shown in Figure B10.

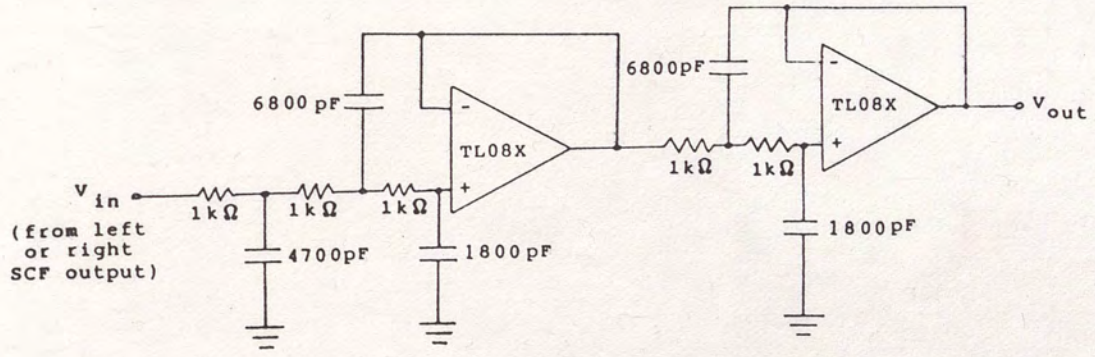


Figure B10. Linear phase output noise filter.

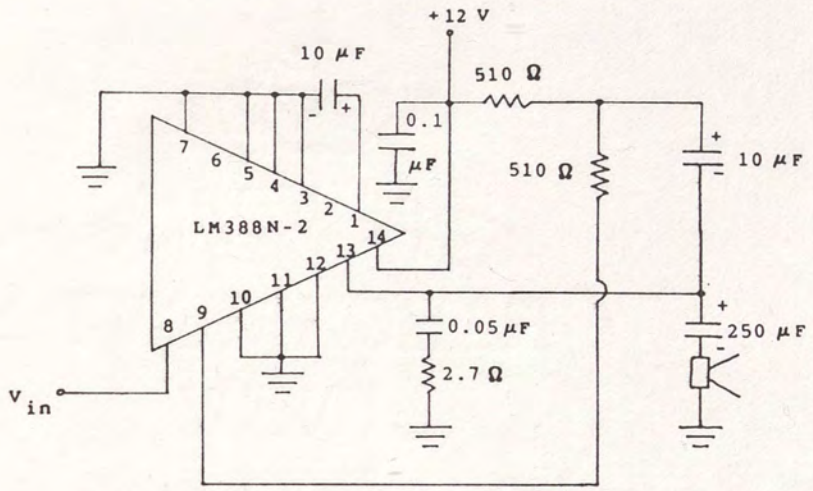


Figure B11. Audio amplifier circuit for signal conditioner, left or right channel (National Semiconductor Corp. 1980).

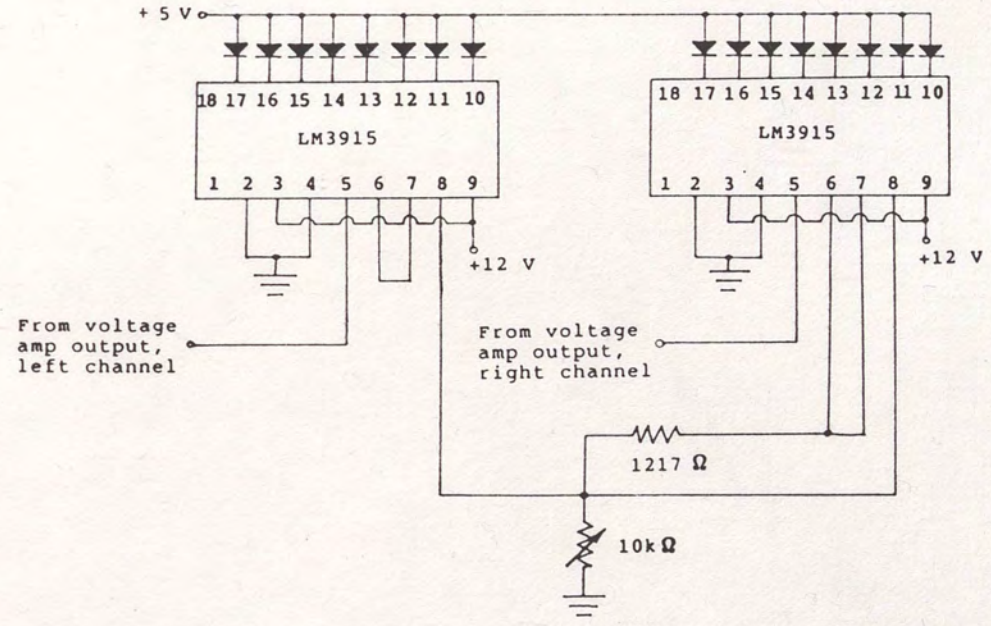


Figure B12. Signal level display circuit for signal conditioner, left and right channels (National Semiconductor Corp. 1980).

Audio Amplifier and Signal Level Display

The audio amplifier and signal level display circuits were essentially implementations of the application circuits given in the manufacturers' device data sheets. The circuits are shown in figures B11 and B12.

Since the audio amplifier had a maximum input signal voltage swing of ±0.4 V (0.8 V peak-to-peak), the signal from the voltage amplifier had to be attenuated before it could be sent to the audio amplifier. This was accomplished by connecting a voltage divider to the audio amplifier input, as shown in Figure B13. This circuit has an attenuation factor of 0.02913 (30.7 dB); thus, a voltage signal with an amplitude of 10 V peak-to-peak input at node A will be reduced to 0.29 V peak-to-peak at node B. This is well within the operating range of the audio amplifier. One advantage of this circuit is that it has a load impedance of 300 Ω at node B looking backward towards node A. This is very close to the load impedance of a microphone; therefore, it makes the circuit very well suited for use with an audio amplifier, since audio amplifier inputs are usually matched to microphone-type loads.

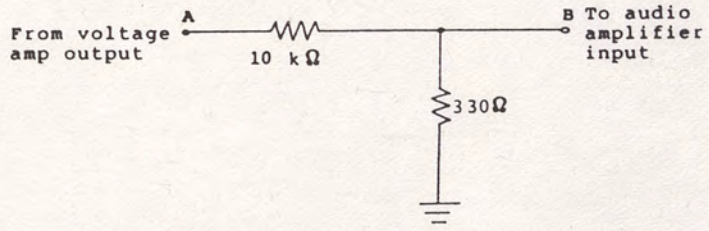


Figure B13. Signal attenuator circuit for audio amplifier.

The signal display circuit shown in Figure B12 was basically a straight implementation of the circuit schematic in the National Semiconductor linear circuits data book, with a few exceptions. First, only eight LEDs were used, instead of ten. Second, a 1217 Ω resistor and 10 KΩ trimpot were used for the input level reference resistors, instead of the 1.24 KΩ and 8.06 KΩ resistors shown in the data sheet schematic. Third, it was not necessary to tie pins 6 and 7 of the left channel LM3915 to the reference voltage on the high side of the 1217Ω resistor.

Power Supply

The last major component of the signal conditioner that had to be designed was the power supply. To begin, the supply voltages required by the various ICs had to be determined. A supply of +5 V (digital logic "high") was needed for the clock circuit components. For the analog signal conditioning circuits (the voltage amplifier, switched capacitor filter and output linear phase noise filter), a +8 V supply and a -8 V supply were used. This supply range was chosen because it was comfortably within the switched capacitor filter supply range (±10 V). For the audio amplifiers and LED display drivers, a +12 V supply was needed; finally, a +5 V supply was needed for the 16 LEDs. The four supply voltages that were required, then, were +5 V, +8 V, +12 V and -8 V. The load currents for these supplies were calculated as follows.

Load current for +5 V supply = supply current for K1100A clock oscillator + 3 supply current for counters + 16 LED current

Load current for +8 V supply = 8 supply current for TL084 op amp + 2 supply current for switched capacitor filter

Load current for +12 V supply = 2X supply current for LM3915 display driver + 2X supply current for LM388N-2 audio amplifier

Load current for -8 V supply = load current for +10 V supply

The load currents for the ICs were obtained from the data sheets for the devices; the LED current was calculated using the following equation.

$$\text{LED Current} \cong 10\left(\frac{1.25}{R_1}\right);\ R_1 \text{ is the program resistor for the LM3915 LED display driver}$$

$$\text{LED Current} = (10)\left(\frac{1.25}{1217}\right) = 10.3 \text{ mA}$$

So the load currents for the four supplies were:

Load current for +5 V supply = 60 mA+(3)(35 mA)+(16)(10.3 mA)
= 0.2698 A

Load current for +8 V supply = load current for -10V supply
= (8)(2.8 mA) + (2)(16 mA)
= 0.0544 A

Load current for +12 V supply = (2)(9.2 mA) + (2)(250 mA)
= 0.5184 A

The four power supplies would each be like that shown below in Figure B14.

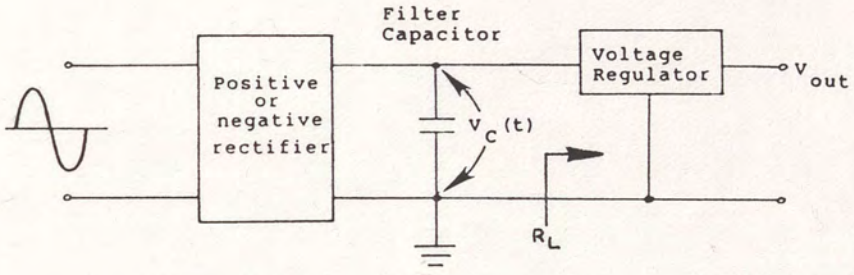


Figure B14. Block diagram of signal conditioner power supply. R_L is the load resistance seen by the filter capacitor.

The voltage regulators that were chosen were the 7805 5 V positive regulator for the +5 V supply, the 7812 12 V positive regulator for the +12 V supply, the 7808 positive adjustable regulator for the +8 V supply and the 7908 negative adjustable regulator for the -8 V supply. All of these regulators had good output voltage regulation and high output current capability (up to 1.5 A).

The power supply filter capacitors had to be designed next. First, a formula for the filter capacitance in terms of the supply voltage, supply current, minimum rectified voltage swing and transformer voltage had to be derived (see Figure B15).

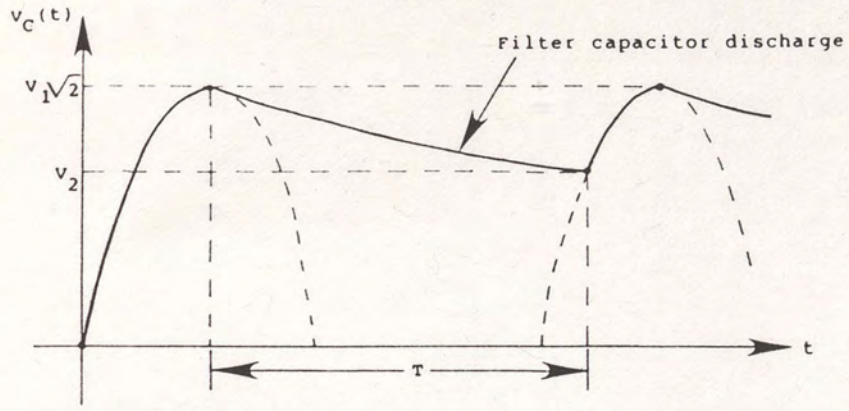


Figure B15. Rectified output voltage at filter capacitor. V_1 is the transformer voltage; V_2 is the minimum voltage swing.

From Figure B15,

$$T = \text{time for capacitor to discharge from } V_1\sqrt{2}/2 \text{ to } V_2$$

$$= \left(\frac{3}{4}\right)\left(\frac{1}{60}\right) + \frac{1}{(2\pi)(60)} \sin^{-1}\left(\frac{2V_2}{V_1\sqrt{2}}\right)$$

$$= 0.0125 + 0.002653 \sin^{-1}\left(\frac{2V_2}{V_1\sqrt{2}}\right)$$

$$V_2 = V_1\sqrt{2}\, e^{-T/R_L C}, \quad R_L = \frac{\text{regulator voltage}}{\text{regulator load current}} = \frac{V_o}{I_o}$$

Combining these equations yields

$$C = -\frac{0.0125 + 0.002653 \sin^{-1}\left(\frac{2V_2}{V_1\sqrt{2}}\right)}{\frac{V_o}{I_o} \ln\left(\frac{2V_2}{V_1\sqrt{2}}\right)} \qquad \text{(B8)}$$

With the regulator supply voltages and load currents given previously, the four filter capacitor values required are, from equation (B8):

$C = 2510.31\ \mu F$ for +5 V supply

$C = 316.35\ \mu F$ for +8 V, -8 V supplies

$C = 2009.74\ \mu F$ for +12 V supply

Here, V_1 is the transformer voltage rating (25.52 V) and V_2 is 75 percent of the peak voltage $V_1\sqrt{2}/2$ (13 V).

Finally, the bridge rectifier, transformer and fuse current ratings for the entire power supply circuit were determined by summing the load currents of the individual voltage supplies, and picking the next highest standard current rating.

Total load current = load current for +5 V supply
+ 2 load current for +10 V supply
+ load current for +12 V supply

$= 0.2698\ A + (2)(0.0544\ A) + 0.5184\ A$

$= 0.897\ A$

Current rating for rectifier, transformer and fuse $\geq$ 1.0 A

The power supply is shown in Figure B16. The filter capacitor values used were standard values that were closest to the calculated values.

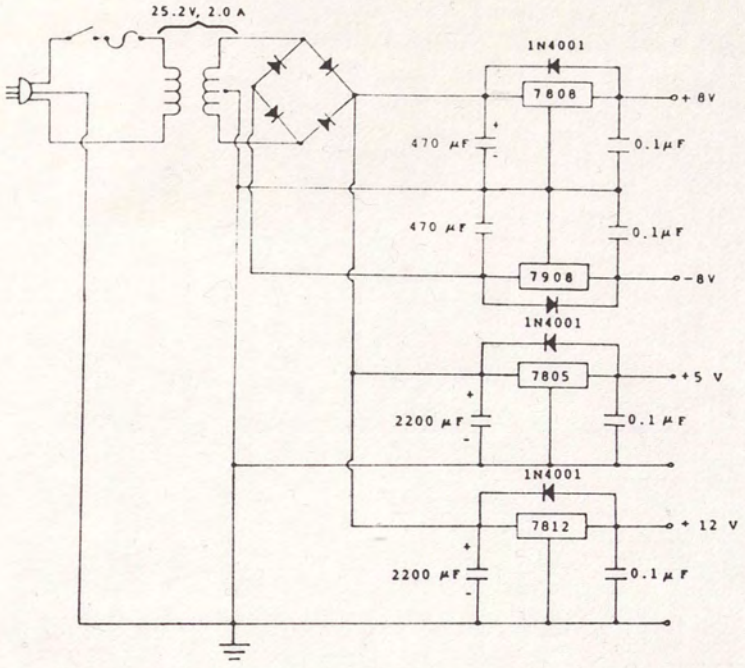


Figure B16. Signal conditioner quad power supply.

APPENDIX C

PHYSICAL SYSTEM DESCRIPTION

This appendix contains a diagram and a photograph of the signal conditioner, along with a schematic diagram. The diagram is shown below in Figure C1; the photograph is shown in Figure C2. The circuit schematic is shown in Figure C3.

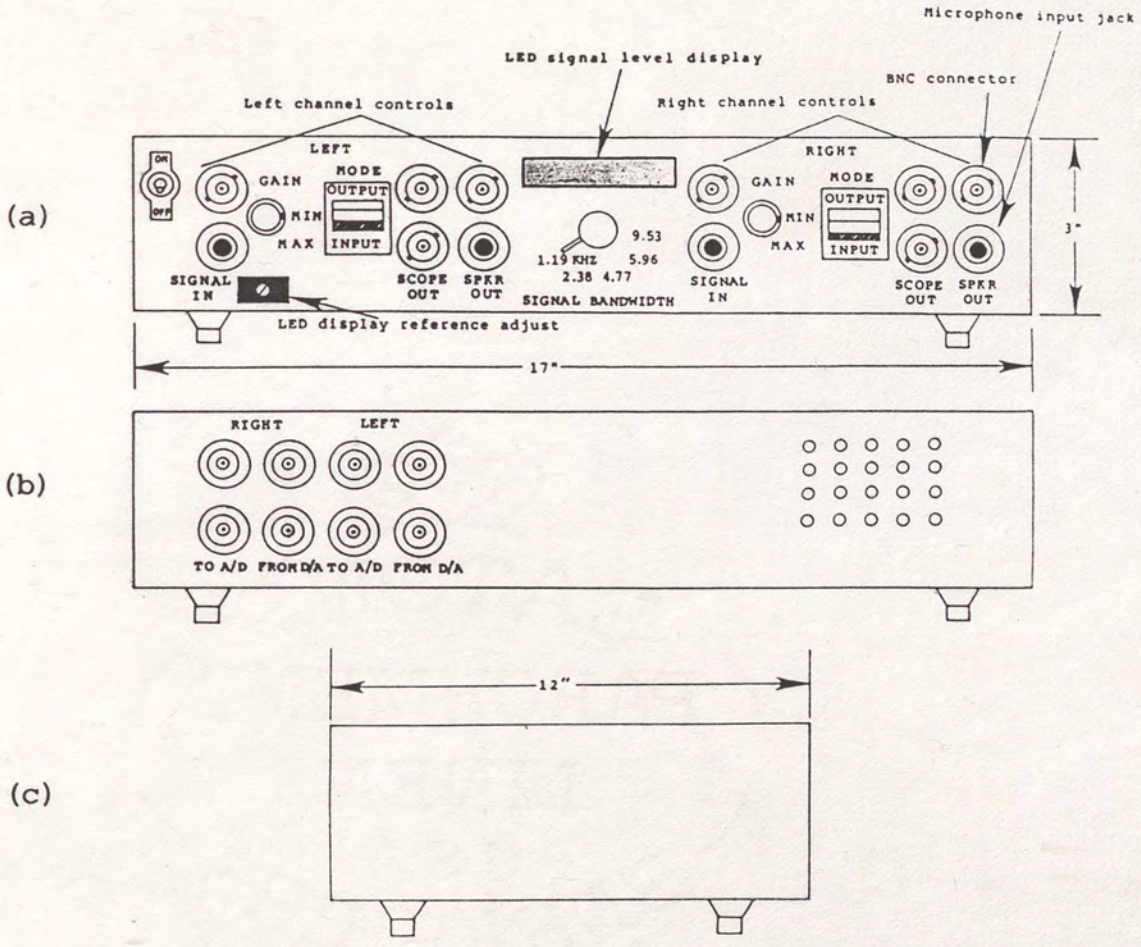


Figure C1. (a) Front view of signal conditioner, (b) Back view and (c) Side view.

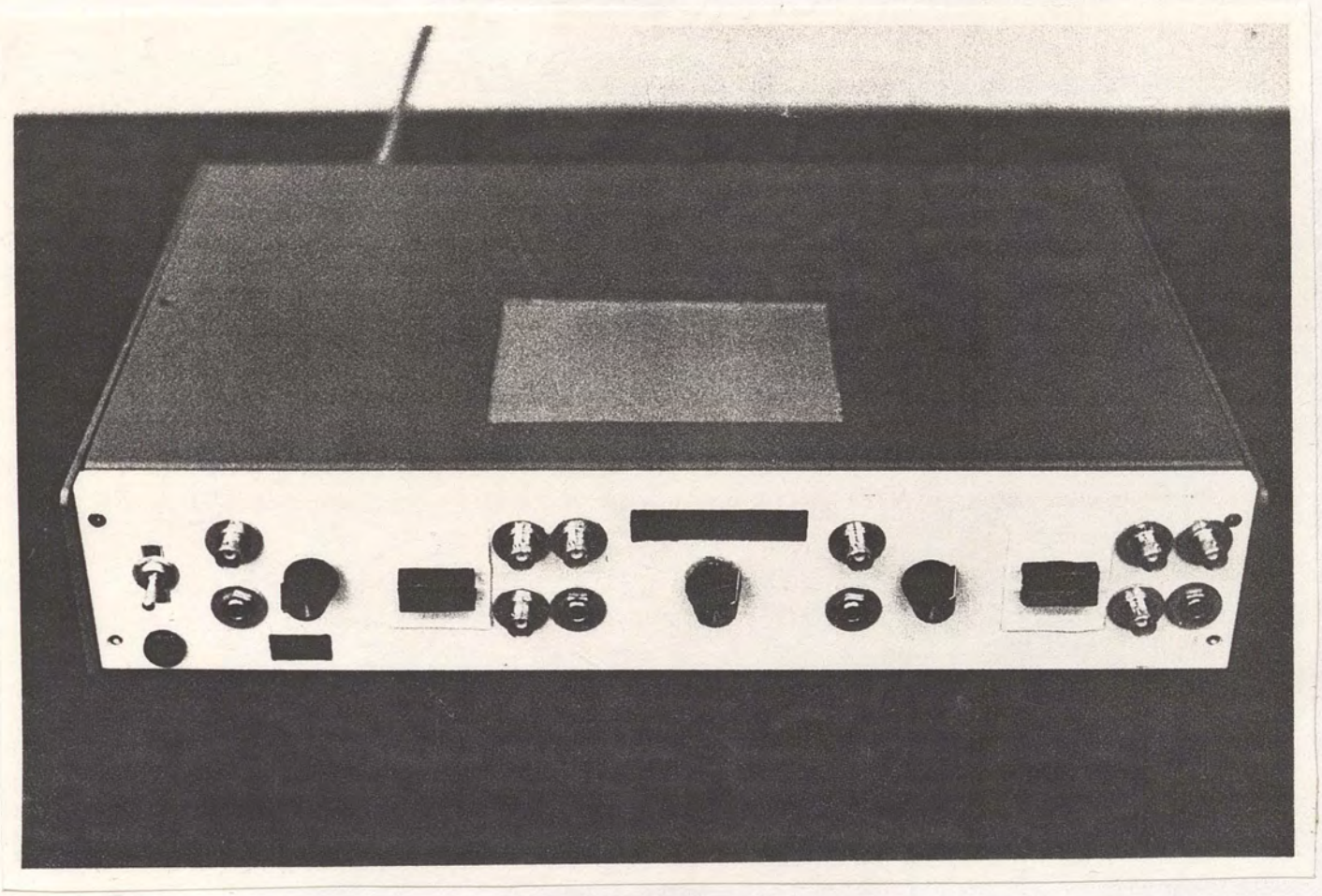


Figure C2. Photograph of signal conditioner.

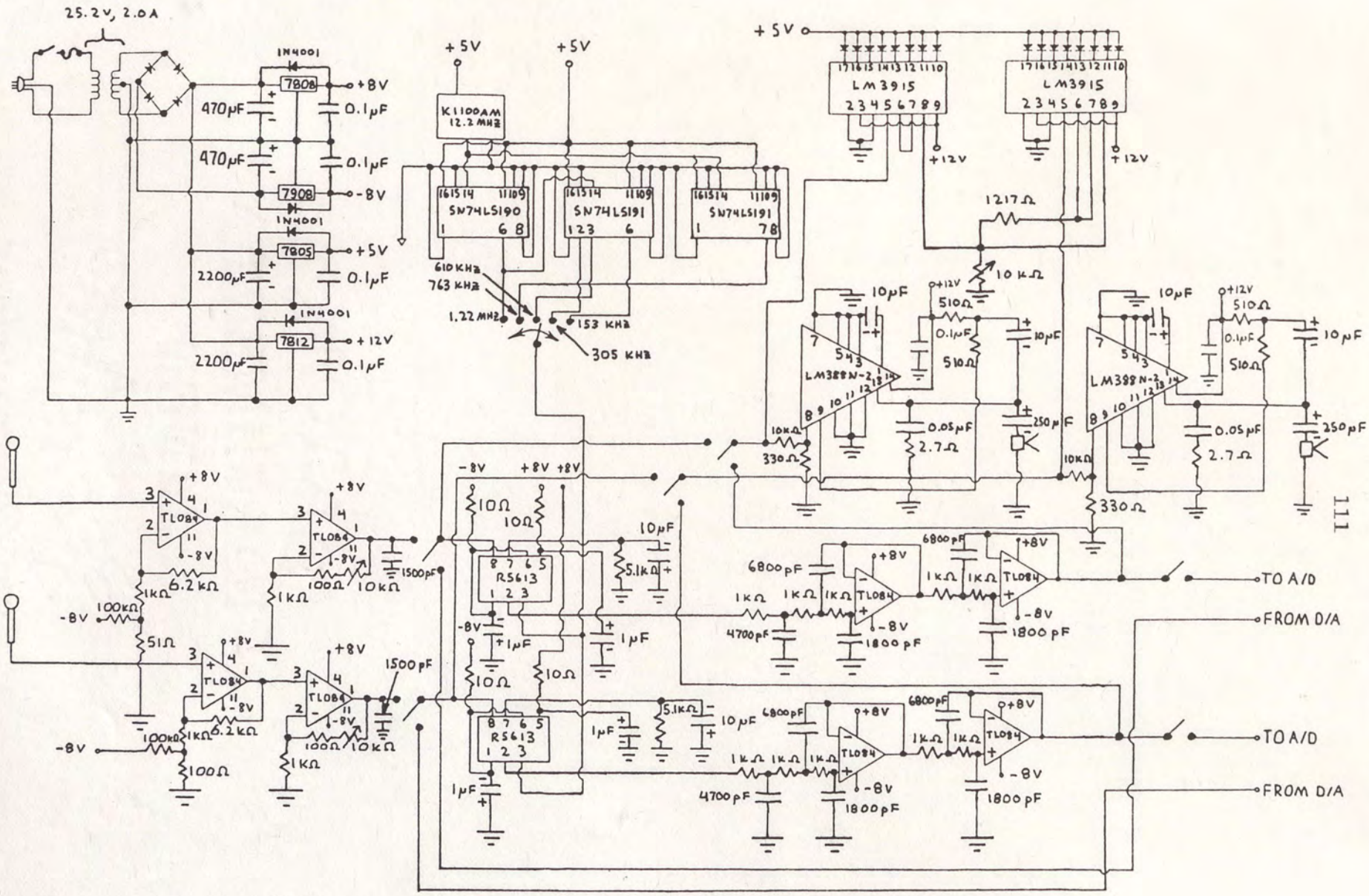


Figure C3. Schematic diagram of signal conditioner.

APPENDIX D

OPERATIONAL SYSTEM DESCRIPTION

The signal conditioner is easy to operate. To process a microphone speech signal, the MODE rocker switch is set to INPUT, and the microphone is connected to the SIGNAL IN jack. The TO A/D output jack on the back panel is connected to the A/D input port on the digital speech processor. Speech signal gain and bandwidth are adjusted via the GAIN and SIGNAL BANDWIDTH control knobs. The speech signal can be monitored on an oscilloscope and/or heard through a loudspeaker by connecting these devices to the SCOPE OUT and SPKR OUT jacks.

To monitor a speech signal from the digital speech processor, the D/A output port on the speech processor is connected to the FROM D/A jack on the back panel of the signal conditioner. The MODE switch is set to OUTPUT; the signal can now be examined with an oscilloscope or heard through a loudspeaker by connecting these devices to the appropriate output jacks on the front panel. The above procedures can be done on either channel, or both channels, since the left and right channels are independent, except for the signal bandwidth control, which is common to both channels.

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