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THE DESIGN OF A QPSK MODEM AND THE PROBABILITY OF ERROR ANALYSIS FOR AN SCA BASED DIGITAL COMMUNICATION SYSTEM

BY

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THESIS

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ABSTRACT

An analysis of the probability of error for an SCA based digital communication system is developed. QPSK modulation and the signal to noise ratio degradation due to the SCA transmission are analyzed to predict the performance of the system in terms of probability of error. The design and analysis of a QPSK modem, a pseudorandom generator, and a pseudorandom correlator are also presented in this thesis.

ACKNOWLEDGMENTS

I would like to acknowledge and thank the many people who have contributed to the completion of this thesis. First, I would like to dedicate this thesis to my parents, Said and Yamina Guediri, my brother, Farid, and all of my family including my sisters, Nafissa and Fatiha, because of the love and moral support they have given me throughout my entire life.

Special thanks are extended to the Electrical Engineering Department of UCF and all the members of its office, for being friendly and kind enough to allow me the use of their facilities.

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TABLE OF CONTENTS

LIST OF FIGURES

I. INTRODUCTION

The Subsidiary Communications Authorization often called SCA, permits a commercial FM station to add another broadcasting channel in addition to the monophonic and stereo channels [1]. The SCA transmissions carry no commercial messages and are intended for private subscribers who pay a fee for background music in stores, physicians' offices, etc. In contrast, the other FM transmissions are for general public use and are supported by commercial advertisements. SCA is the only Federal Communications Commission (FCC) approved channel for broadcasting digital data. Therefore, with the sharp increase in the number of computers for the home and small office, the use of the SCA channel for broadcasting digital data is becoming increasingly important. This thesis presents a design for an SCA based digital communication system, and an examination of important parameters, such as the probability of error, and the signal to noise ratio.

The broadcast of digital data in a commercial environment must also comply to the rules and regulations imposed by the FCC. The commercial FM band illustrated in figure 1, shows the broadcast baseband spectrum including the SCA portion, which extends from 59 to 75 Kilohertz. The preliminary block diagram of a commercial system for broadcasting over the SCA channel is shown in figure 2.

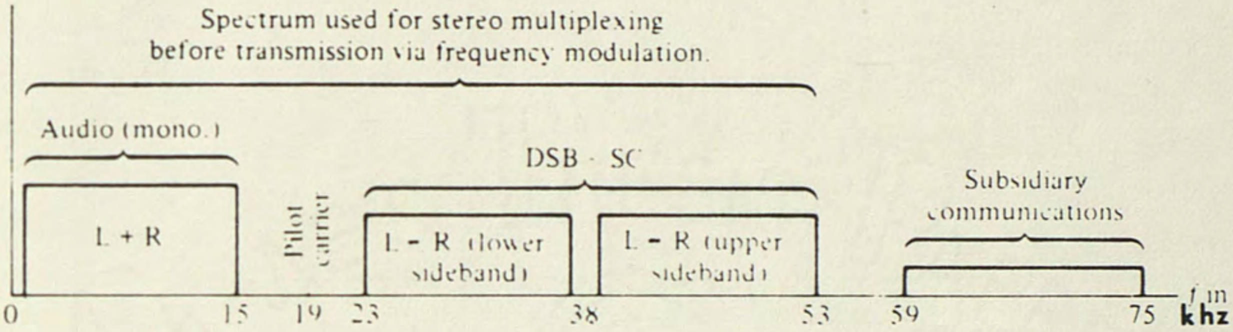


Figure 1. Spectrum of a stereo-multiplex system [1].

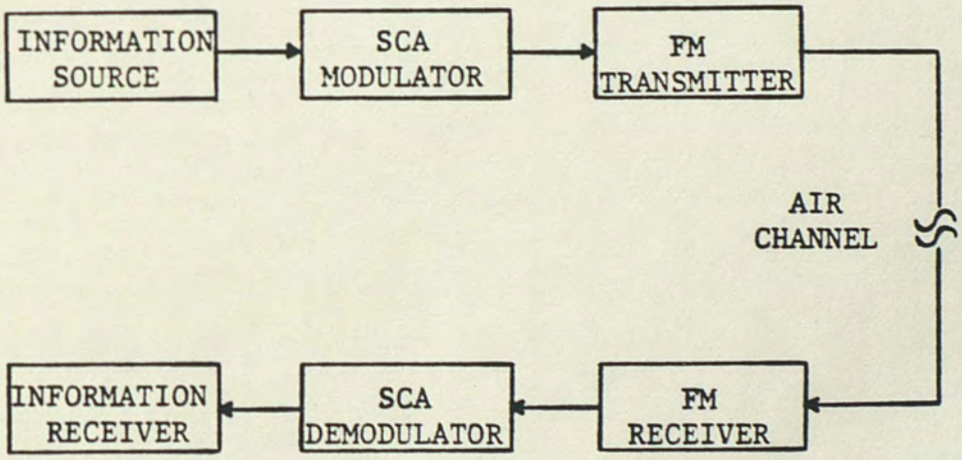


Figure 2. Commercial system for SCA broadcasting.

The information source typically provides analog signals (eg., voice, music), which are frequency modulated

(FM), and transmitted via the air channel. The FM signals are demodulated and presented to an information receiver, which is also an analog device.

In order for digital data to be transmitted over the SCA channel, a digital information source, a digital receiver, and a digital modulator/demodulator (ie, modem) are added, as illustrated in figure 3.

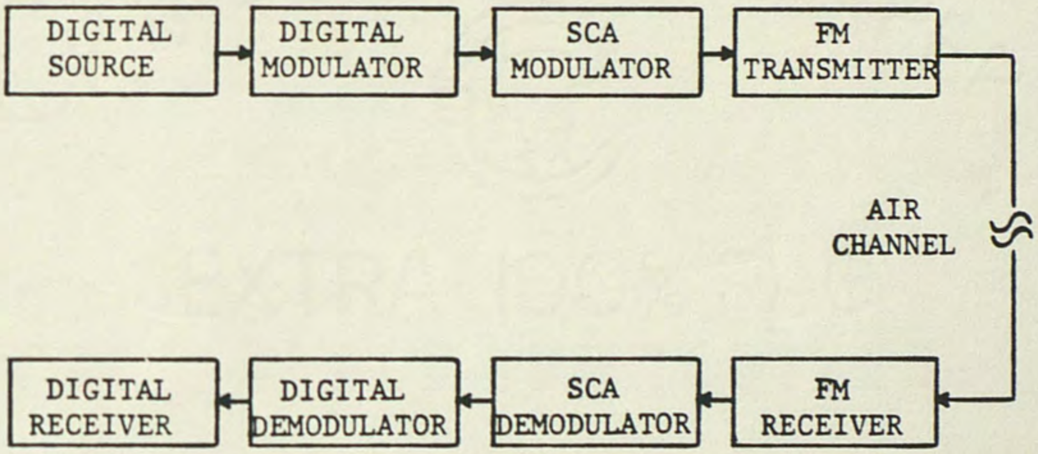


Figure 3. SCA based digital communication system.

There are many digital modulation techniques. The choice of a technique for a particular system is critical in the performance of the entire system. The quadrature phase shift keying (ie, QPSK) modulation scheme is investigated in this report. The advantages that a QPSK scheme offers, with respect to other modulation schemes, are also addressed in this report. The most important parameters in the design of a digital communication system are information capacity, and probability of error.

The emphasis of this report is on probability of error computation of the overall system. The design and probability of error characteristics of a QPSK system are discussed in chapter II. Chapter III introduces the SCA components, analyzes the entire SCA based digital communication system, and evaluates the corresponding probability of error.

II. MODEM DESIGN

In this chapter the design of a modulator and demodulator for the SCA based digital communication system is presented. The choice of a QPSK modem is discussed, The design process is outlined, and the detailed design is included in the appendix. The theoretical and experimental probability of error for a QPSK modem is presented.

QPSK Modulation Scheme

The choice of a modulation technique for digital data transmission is heavily dependent on the application. M-ary phase shift keying (PSK) schemes are optimum for high speed data transmission and bandwidth conservation at the expense of transmitter power [2]. Information rate and bandwidth limitations are important factors in the design of an SCA based digital communication system. Therefore, an M-ary PSK scheme has been selected to obtain a considerable information rate, with the appropriate value of M selected for an optimum power/bandwidth tradeoff.

Table 1 provides a comparison of bandwidth and power ratios between M-ary PSK schemes for a fixed probability of error [2].

Table 1
Comparison of Power Bandwidth Requirements
for M-ary PSK Scheme. Pe = .0001

Value of M	$\frac{(\text{Bandwidth})_M}{(\text{Bandwidth})_b}$	$\frac{(S_{av})_M}{(S_{av})_b}$
4	0.5	0.34 dB
8	0.333	3.91 dB
16	0.25	8.52 dB
32	0.2	13.52 dB

It is obvious from table 1, that the QPSK scheme (ie, M = 4) offers the best tradeoff between power (Sav) and bandwidth requirements. For this reason, QPSK modulation is used in this particular design. In addition, it is widely used in practice. For M greater than 4, power requirements become excessive, and the complexity of the equipment becomes impractical. The QPSK modulation scheme is illustrated in figure 4, where $m_i(t)$ provided by the digital source, represents the input to the QPSK modulator.

QPSK Modulator Design

The block diagram of a parallel realization for a QPSK modulator is shown in figure 4, along with typical signal waveforms.

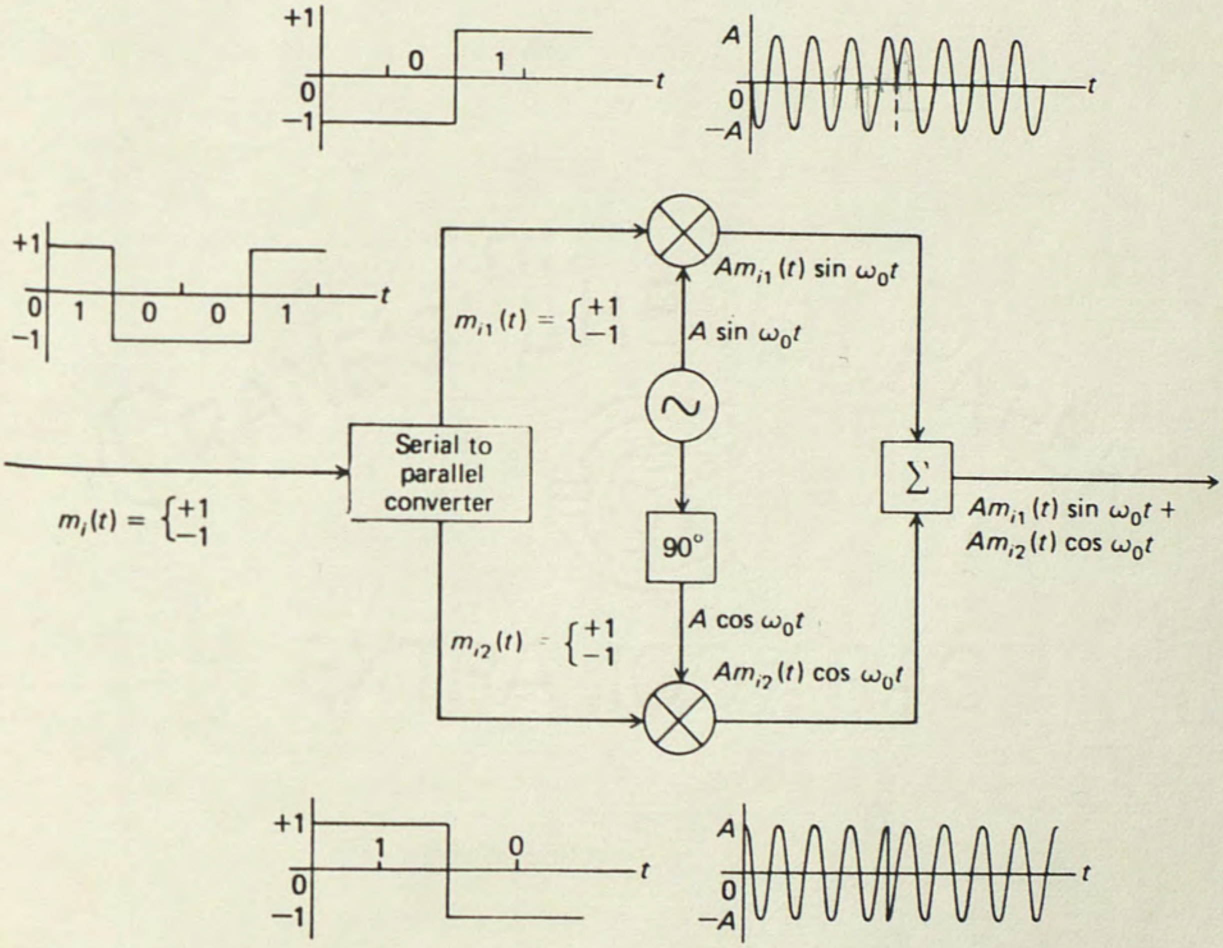


Figure 4. Modulator and typical waveforms for QPSK.

Given a serial digital input as illustrated in figure 4, the serial to parallel converter (SPC) stores and presents two bits at a time, each bit on a separate channel. Shottky TTL gates are used for the design of the SPC in order to achieve high speed data manipulation. A clock generated from the local oscillator is used to ensure correct synchronization. In this particular design, the clock rate is arbitrarily chosen to be smaller than the local oscillator frequency by a factor of eight.

Once the two bits are presented to the two separate channels, modulation is performed by two separate carriers. The carriers are 90 degrees out of phase in order to achieve QPSK. After modulation, the two channels are summed and transmitted as one QPSK signal. The complete design of a QPSK modulator is presented in the appendix (figure 12). The modulator design presented in the appendix uses a PJFET along with an operational amplifier to perform the multiplication necessary for modulation between the local carrier, and the data bit transmitted on one of the channels.

PSK and QPSK waveforms are included respectively in figure 13 and 14 of the appendix. For a PSK signal, a phase shift of 180 degrees occurs at every bit transition (ie, from a "1" to a "0" or vis-versa). As for a QPSK signal, the phase change is only 90 degrees, and it occurs at every symbol transition. Each symbol is represented by a dibit (ie, 00, 01, 10, or 11). The power spectrum of the QPSK signal is also shown in the appendix (figure 15 and 16).

QPSK Demodulator Design

The QPSK demodulator is shown in figure 5. The QPSK input signal is

$$A\, m_{i1}(t)\ \sin(w_o t) + A\, m_{i2}(t)\ \cos(w_o t)\ .$$

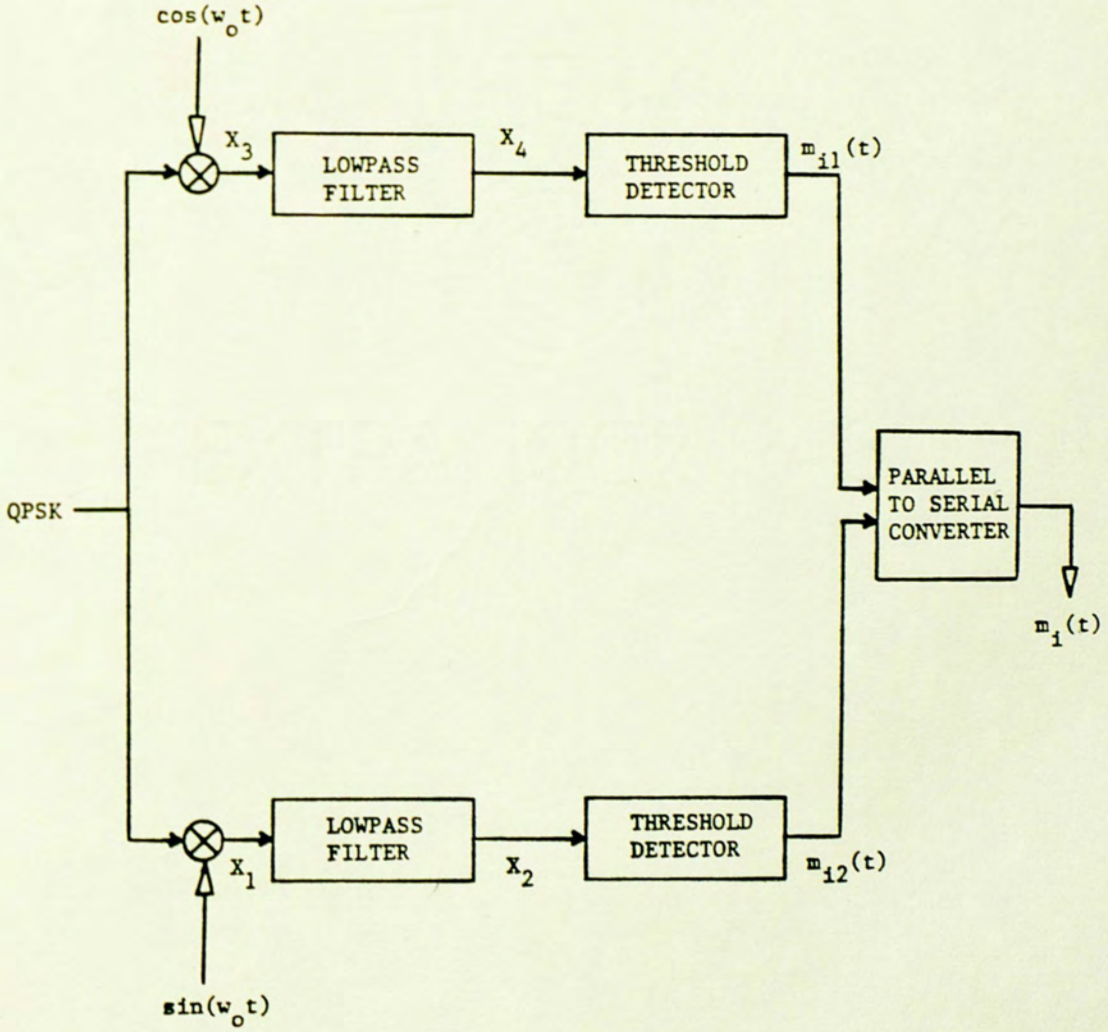


Figure 5. Block diagram for a QPSK demodulator.

The signal at point X1 in the lower channel is

$$X_1 = A\left[m_{i1}(t)\ \sin(w_o t) + m_{i2}(t)\ \cos(w_o t)\right]\left[\sin(w_o t)\right]$$

or

$$X_1 = A\left[(1/2)\ m_{i1}(t) - (1/2)\ m_{i1}(t)\ \cos(2w_o t)\right.$$
$$\left. + (1/2)\ m_{i2}(t)\ \cos(2w_o t)\right].$$

At the output of the lowpass filter, the signal becomes

$$X_2 = (A/2)\ m_{i1}(t).$$

Similarly, the signal X4 in the upper channel is

$$X_4 = (A/2)\ m_{i2}(t).$$

The zero threshold detectors detect the presence of a +1 or a -1 depending on whether the input signal is above or below the 0 volt level. The outputs of the threshold detectors ($m_{i1}(t)$ and $m_{i2}(t)$) are two digital signals which are presented to a parallel to serial converter in order to retrieve m (t), the original serial digital data. A detailed design of the QPSK demodulator is presented in figure 17 of the appendix. Important aspects of the demodulator design presented in the appendix are as follows:

1. Synchronization: Under normal conditions, the

local carriers at the receiver must be retrieved from the QPSK signal in order to achieve synchronization with the transmitter. The Phase locked loop is widely used for carrier extraction purposes. In this particular design however, the carriers are extracted directly from the transmitter to avoid an increased complexity of the design.

2. Filtering: The design of the lowpass filter is dependent on the data rate of the transmitting digital data source. For a given experimental data rate of 660 bits/sec, a cut-off frequency of 1 kilohertz was required to perform the filtering on each separate channel.

3. Parallel to serial conversion: The parallel to serial converter circuit shown in the appendix is the result of an original design, whose primary function is to convert a parallel loading of two bits, to a single serial output bit which represents the data transmitted. Note that a timing extraction circuit is again necessary to achieve synchronization. However, to avoid complex circuitry, the clock at the transmitter is also used at the receiver therefore synchronizing the system. The steps for designing the PSC are shown in detail in the appendix (page 37 and 38).

Theoretical Probability of Error

The relationship between the probability of error of an ideal QPSK system, and the signal to noise ratio at the receiver input [3] is expressed as

$$P_{eo} = \text{erfc}\left(\sqrt{E_o/(2N_o)}\right) \qquad (1)$$

where

$$E_o = A^2/R_s$$

and

$$N_o = \eta B \,.$$

Each term is defined as follows:

Eo= average energy per character at the receiver

A = amplitude of the QPSK signal

Rs= baud rate

B = noise bandwidth

η = power spectral density of the noise.

A graph of the probability of error versus the signal to noise ratio is shown in figure 8. The test set-up for the experimental probability of error of the QPSK modem designed and implemented in this report, is presented in the next section. The measured probability of error is also plotted in figure 8.

Test Set-up for Experimental Probability of Error

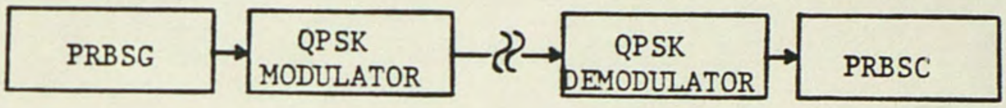


Figure 6. QPSK digital transmission.

Throughout communications theory, performance is calculated based on a random channel. When testing communication systems, there must be a convenient way to simulate a true random channel, and yet still be able to have prior knowledge of the data being transmitted so that individual errors can be detected. One simple way to achieve this is to use a pseudorandom bit sequence generator (PRBSG) as a random digital data source. This is shown in figure 6. The schematic of a generator which was designed and implemented is illustrated in the appendix (figure 18), along with a photograph of the data generated from the generator (figure 19). Note that while a pseudorandom sequence is generated at the transmitting end, another identical pattern is generated for comparison and error count at the receiving end. This is easily done by using an identical generator provided with a synchronizing circuit. The schematic of a pseudorandom bit sequence correlator (PRBSC) which was designed and implemented is shown in figure 20 of the appendix. An error insertion circuit is also provided as part of the PRBSG for testing purposes, and the errors are detected by the PRBSC at the receiver end.

One way to simulate the effects of a random channel upon the performance of a digital communication system, is to introduce random noise at the receiving end of the system. This technique can easily be implemented as shown in figure 7.

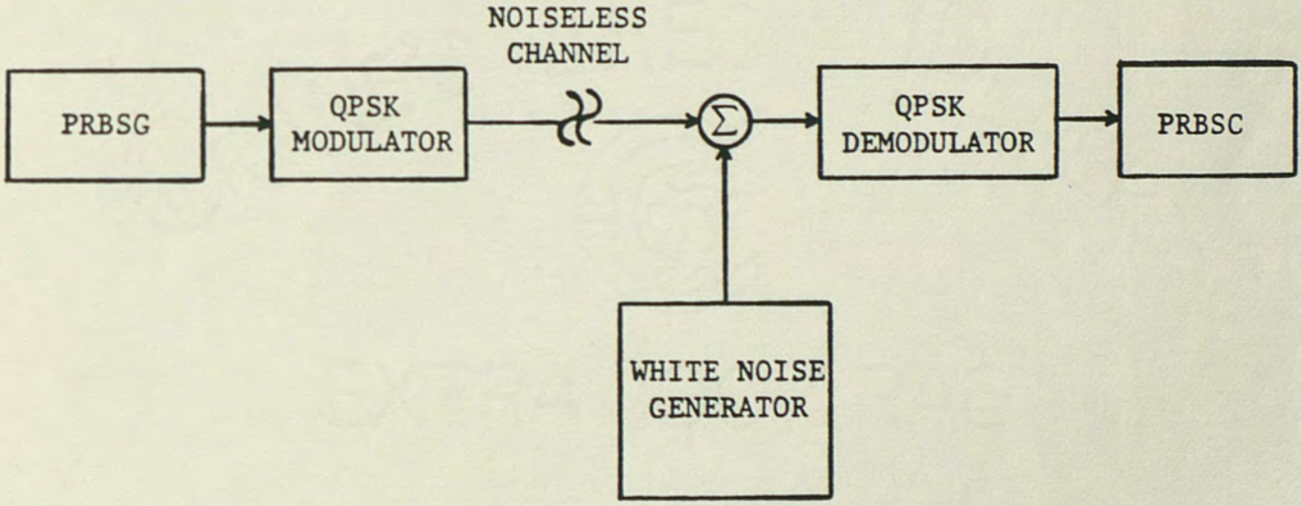


Figure7. Experimental QPSK transmission.

Given the noise power (No) induced by the noise generator, and the amplitude of the QPSK signal, along with the sampling rate, the experimental probability of error can be determined.

The probability of error of the experimental set-up is defined as

$$Pe = [\text{Bit Error Rate}] / [\text{Baud Rate}]$$

The bit error rate (BER) is determined by counting the number of errors for a given time interval. Many samples must be taken in order to obtain a statistically acceptable average. As for the baud rate, it is easily determined from the data rate of the pseudorandom generator. The relationship is given by [2]

$$R_s = (1/2)R_b$$

where R_b is defined as the data rate in bits per second, and Rs the Baud rate in symbols per second. Note that by varying the noise power from the generator, and keeping the QPSK signal at a fixed value, different values of signal to noise ratio can be generated, and therefore the experimental error probability function can be plotted, as illustrated in figure 8. The experimental results were obtained using a 200 mv QPSK signal, and a baud rate of 330.

In figure 8, the ideal and experimental QPSK systems are compared on the bases of probability of error. The experimental results were limited to error probabilities less than 0.001 in order for the measurements to be statistically accurate, and to focus attention on systems which operate at a relatively low probability of error.

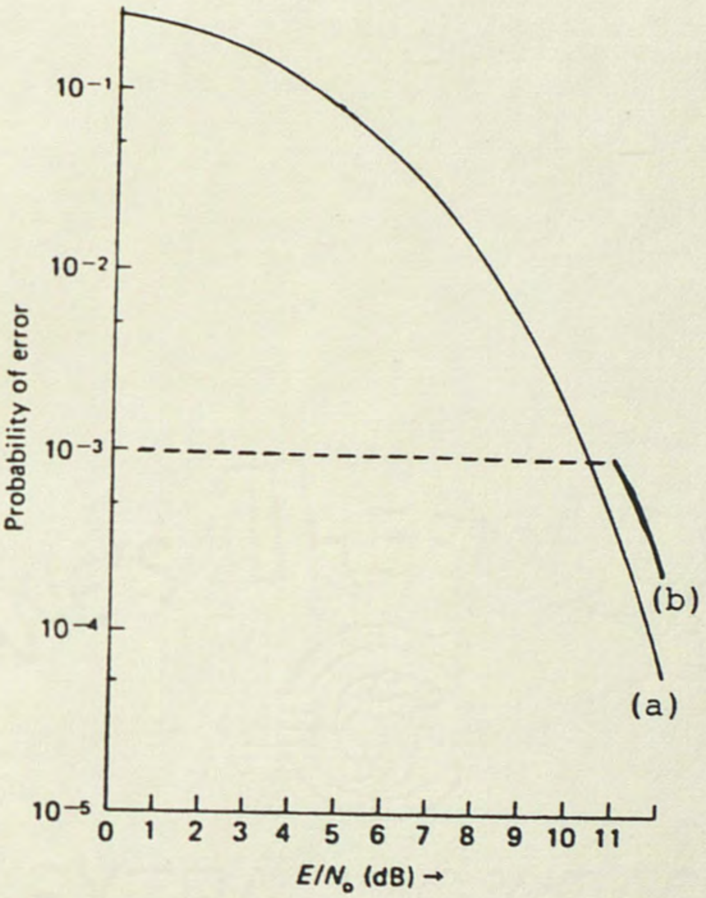


Figure 8. Probability of error for
(a) ideal QPSK [3]
(b) experimental QPSK.

It is obvious from figure 8, that for a given SNR the probability of error of the experimental QPSK system is slightly larger than the probability of error of the ideal QPSK system. This is mainly due to the presence of non-ideal elements in the design of the QPSK.

III. PROBABILITY OF ERROR FOR SCA

This chapter presents an analysis of the probability of error for an SCA based digital communication system, which uses QPSK as a modulation scheme. The SCA transmission scheme model uses narrowband frequency modulation (NBFM). The signal to noise ratio degradation due to transmission via the SCA channel is examined, and the impact of the degradation upon the performance of the system, in terms of the probability of error, is presented.

Model of an SCA Based Communication System

For the system shown in figure 9 the signal to noise ratio (SNR)o at the receiver input, can be written

$$(SNR)_o = (E_o/N_o) = (A^2/N_oR_s) \tag{2}$$

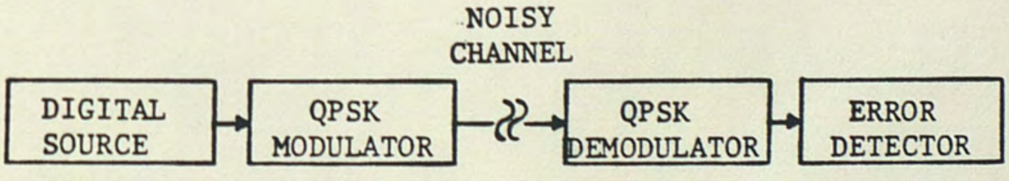


Figure 9. QPSK system .

where A is the amplitude of the QPSK signal, Rs is the baud rate, and No is the noise power at the receiver.

Data transmission is accomplished via the SCA channel, as illustrated in figure 10.

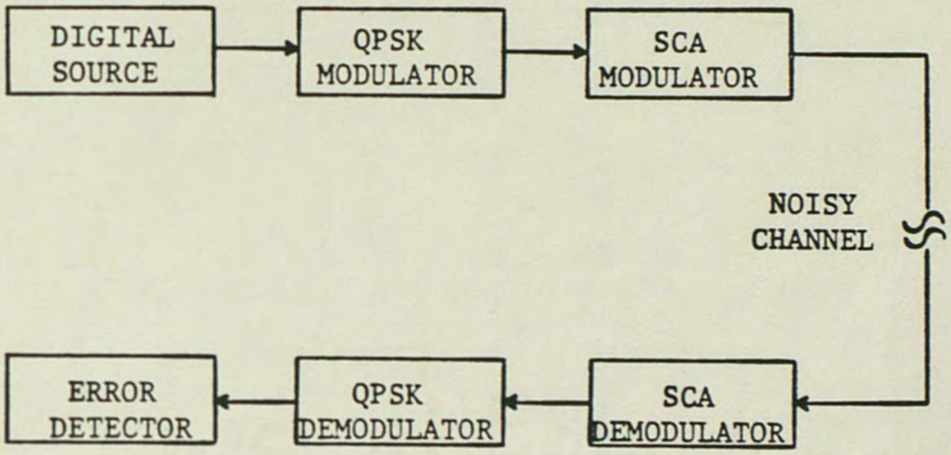


Figure 10. SCA based communication system .

As noted previously, the Federal Communications Commission (FCC) reserves a portion of the broadcast baseband spectrum, uniquely for SCA transmission. This particular portion extends from 59 to 75 kilohertz, and uses an SCA subcarrier typically placed at 67 kilohertz [1,5]. FCC rules and regulations require that the SCA signal must be frequency modulated, and that the maximum symmetrical deviation does not exceed plus or minus 8 kilohertz, in order for the information to be entirely contained within the allowed SCA spectrum [6,7].

FCC also requires that no interference must be caused to the baseband spectrum, by SCA signals. Therefore, any signal caused by the SCA transmission in the 0 to 59 kilohertz range, must be 60 dB below the main channel audio signal at its maximum amplitude. Also, the maximum allowed amplitude of the SCA carrier must be 20 dB below this maximum, therefore setting a 40 dB difference between the SCA carrier level, and the SCA signals in the 0 to 59 kilohertz range.

Since the SCA signal must be frequency modulated, it can be represented by an FM signal. For the case of a sinusoidal message, such a signal [3] can be written

$$X(t) = A_c \sum_{n=-\infty}^{\infty} J_n(\beta) \cos(w_c + nw_m)t$$

where

A_c= amplitude of the SCA carrier

w_c= carrier frequency

w_m= message frequency

β = modulation index.

However, SCA signals must be entirely contained within the SCA channel allocated by the FCC. Therefore, narrowband frequency modulation (NBFM) must be used to confirm the bandwidth limitations imposed. This task can easily be accomplished by choosing a modulation index much smaller than one, which in the case of a sinusoidal message will lead us to a reduced version of X(t) written as [3]

$$X(t) = A_c \cos(w_c t) + (A_c \beta/2A)\left[c0s(w_c + w_m)t - \cos(w_c - w_m)t\right].$$

As the equation of X(t) shows, the bandwidth of the FM signal has been reduced using the NBFM approximation. Also, the modulation index can be written

$$\beta = (Af_d/f_m) \ll 1$$

where

A = amplitude of the message

f_d = frequency deviation constant (HZ/V).

Note that the modulation index, β , is defined only for sinusoidal modulation.

SNR Degradation

The signal to noise ratio relationship for a NBFM signal at the input of the QPSK demodulator, is [3]

$$(SNR)_1 = 3D^2\, \overline{m_n^2(t)} \left[P_t/(N_o W)\right] \tag{3}$$

where the deviation ratio, D, is defined as

D = [peak frequency deviation]/[bandwidth of the message]

which is

$$D = (Af_d/W) \ll 1$$

where

A = amplitude of the QPSK signal

W = bandwidth of the QPSK signal.

P_t represents the power transmitted, and is defined as

$$P_t = A_c^2/2$$

where A_c is the amplitude of the SCA subcarrier.

$\overline{m_n^2(t)}$ is the mean square value of the normalized QPSK message.

As presented previously a QPSK signal can also be written as

$$m(t) = A\, m_{i1}(t) \cos(w_o t) + A\, m_{i2}(t) \sin(w_o t)$$

from which the normalized version is

$$m_n(t) = m_{i1}(t) \cos(w_o t) + m_{i2}(t) \sin(w_o t)$$

and the mean square value is

$$\overline{m_n^2(t)} = \lim_{T\to\infty} (1/T) \int_{-T/2}^{T/2} |m_n(t)|^2 dt .$$

With simplification the above reduces to

$$\overline{m_n^2(t)} = 1 .$$

With substitution of all of the terms previously defined from equation 3, the SNR can be expressed as

$$(SNR)_1 = (3/2)(A^2 f_d^2 A_c^2)\Big/(W^3 N_o) \cdot \tag{4}$$

Note that the presence of NBFM will introduce a signal to noise ratio degradation into the QPSK system. Therefore, equations 2 and 3 can be correlated as follows:

$$(SNR)_1 = X_d \; (SNR)_o \tag{5}$$

where X_d (which is smaller than one) represents the signal to noise ratio degradation factor.

The substitution of equations 2 and 4 into equation 5, results in

$$(3/2)(A^2 f_d^2 A_c^2)\Big/(W^3 N_o) = X_d \left[A^2\Big/(N_o R_s) \right]$$

which can be simplified to

$$X_d = (3/2)\ (A_c^2\ f_d^2\ R_s)/(W^3)\ . \tag{6}$$

Probability of Error for the System

Equation 1 (page 12), which presents the relationship between the probability of error of an ideal QPSK modem, and the signal to noise ratio at the receiver input, is expressed as

$$P_{eo} = \operatorname{erfc}\left(\sqrt{(1/2)(SNR)_o}\right) . \tag{7}$$

Transmission via the SCA channel induces a SNR degradation at the receiving end of the QPSK system. Therefore, from equation 5, the probability of error for the SCA based digital communication system is expressed as

$$P_{el} = \operatorname{erfc}\left(\sqrt{(1/2)(SNR)_1}\right) \tag{8}$$

where

$$(SNR)_1 = X_d\ (SNR)_o$$

and

$$X_d = (3/2)\ (A_c^2\ f_d^2\ R_s)\Big/(W^3)\ .$$

The substitution of (SNR) into equation 8, results in

$$P_{el} = \mathrm{erfc}\left(\sqrt{(1/2)\ X_d\ (SNR)_o}\right)$$

where $(SNR)_o$ for the QPSK modem is:

$$(SNR)_o = A^2/(N_o R_s)\ . \tag{9}$$

The probability of error for the SCA based digital communication system can also be expressed in terms of the parameters associated with the SNR degradation factor. The substitution of X_d (from equation 6) into equation 9, results in

$$P_{el} = \mathrm{erfc}\left(\sqrt{(3/4)(A_c^2 f_d^2 R_s)(SNR)_o\ /\ (W^3)}\right)\ . \tag{10}$$

For a given digital communication system based on a QPSK modem, and an SCA transmission scheme, the total probability of error of the system can be determined from equation 10. The procedure involves the computation of the signal to noise ratio for the QPSK modem (ie, SNR_o), and the signal to noise degradation factor due to the SCA transmission scheme (ie, X_d). The designer's choice of the parameters associated with the system must take into consideration the constraints imposed by FCC regulations. These constraints involve power and bandwidth limitations.

The probability of error versus the SNR is plotted in figure 11 for different values of the signal to noise degradation factor. These values are chosen arbitrarily to illustrate the impact of an SCA transmission scheme upon the performance of a digital communication system in terms of the probability of error.

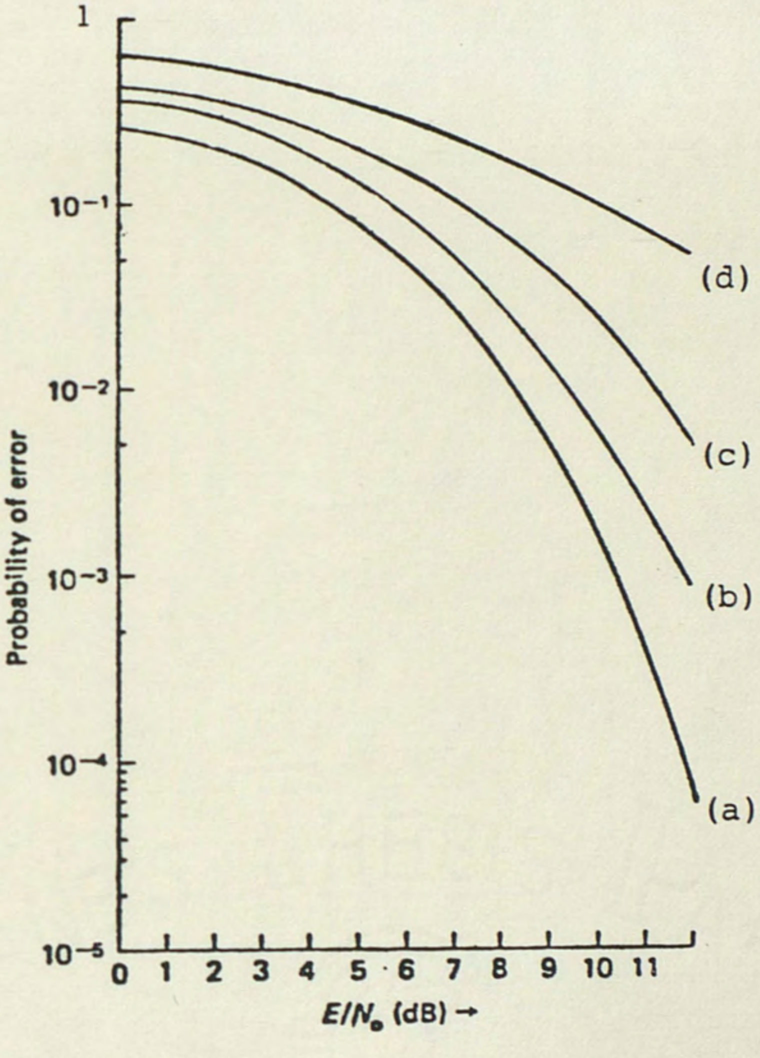


Figure 11. Probability of error for
(a) ideal QPSK
(b) SCA given X_d = 75%
(c) SCA given X_d = 50%
(d) SCA given X_d = 25%

IV. SUMMARY, CONCLUSIONS, AND FUTURE STUDY

The probability of error relationship developed in this thesis, and the graphs generated in figure 11, offer a suitable guideline for SCA based digital communication system designers. The results obtained can be used to predict the performance of a one-way information transmission system using the SCA channel.

The analysis presented in this thesis also offers a potential base for future study, such as digital data transmission for home computers, weather map transmission, and teletex-type service. Regardless of the application, the reception must be accomplished by a suitable FM receiver and an SCA demodulator.

Digital data transmission via the SCA channel is very sensitive to signal to noise ratio degradation, as seen from figure 11. However, the SCA channel offers many advantages with respect to the conventional telephone line channel. Some of these advantages include the ability to reach several destinations with a single transmission, the possibility of increasing the transmission rate, and a reduced transmission cost.

APPENDIX

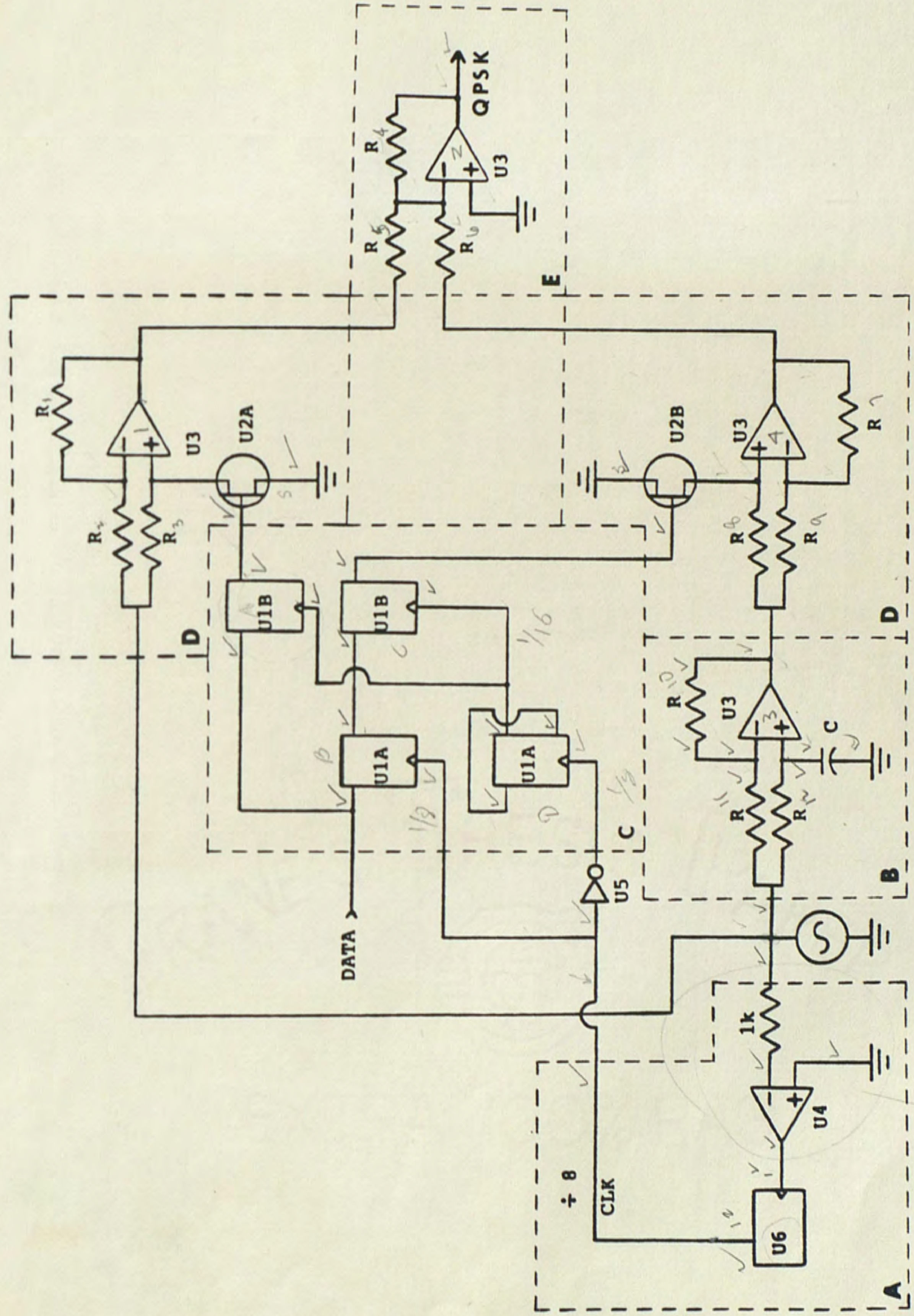


Figure 12. QPSK modulator circuit design.

QPSK modulator. The basic parts list is as follows:

U1	74LS74	D-flip-flop
U2	2N 3909	P-JFET
U3	TL084	Biquad
U4	LF351	Op-amp
U5	74LS06	Hex-inverter
U6	74LS161	4-bit counter

QPSK modulator. Each block is defined as follows:

A = synchronizer

B = carrier phase shifter

C = serial to parallel converter

D = PSK modulator

E = analog summer.

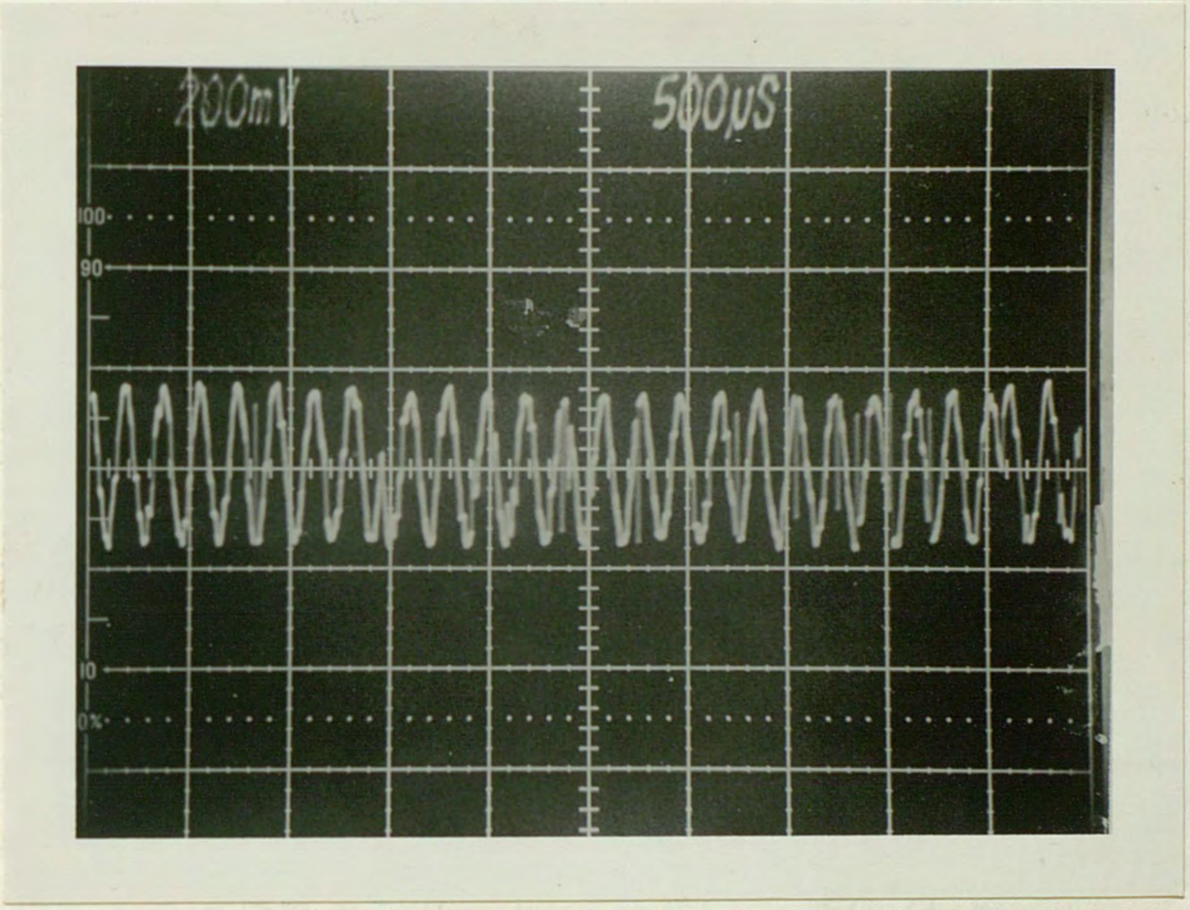


Figure 13. PSK waveform.

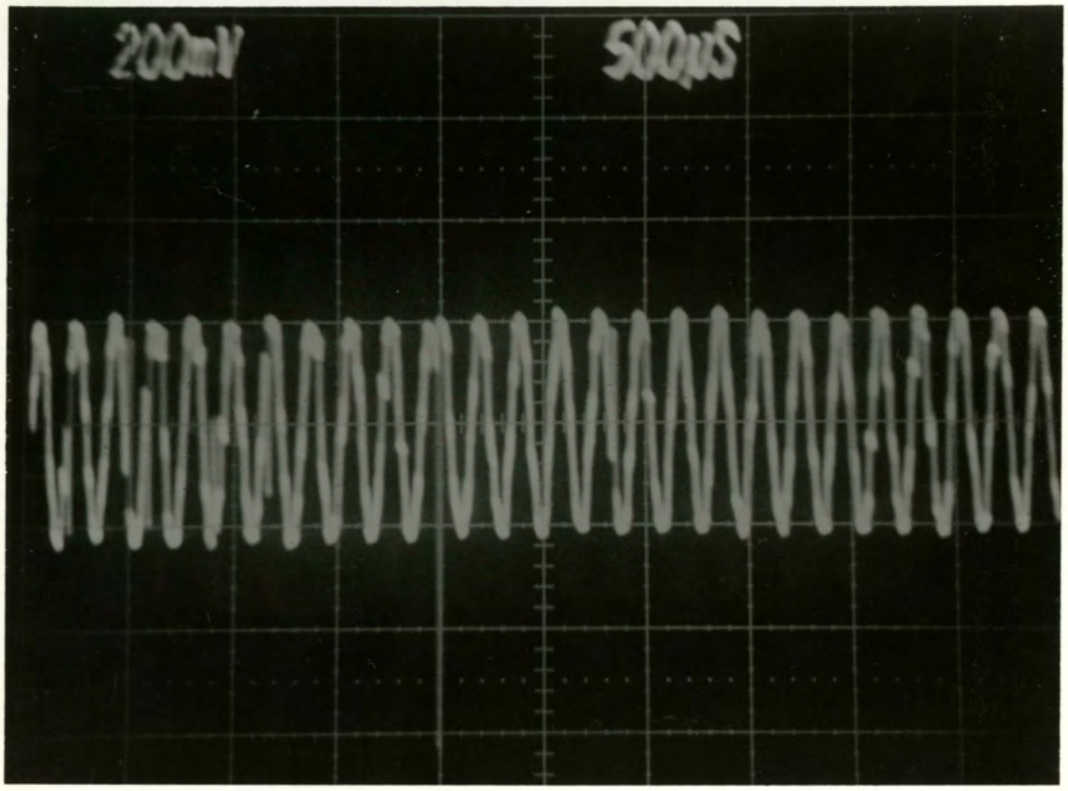


Figure 14. QPSK waveform.

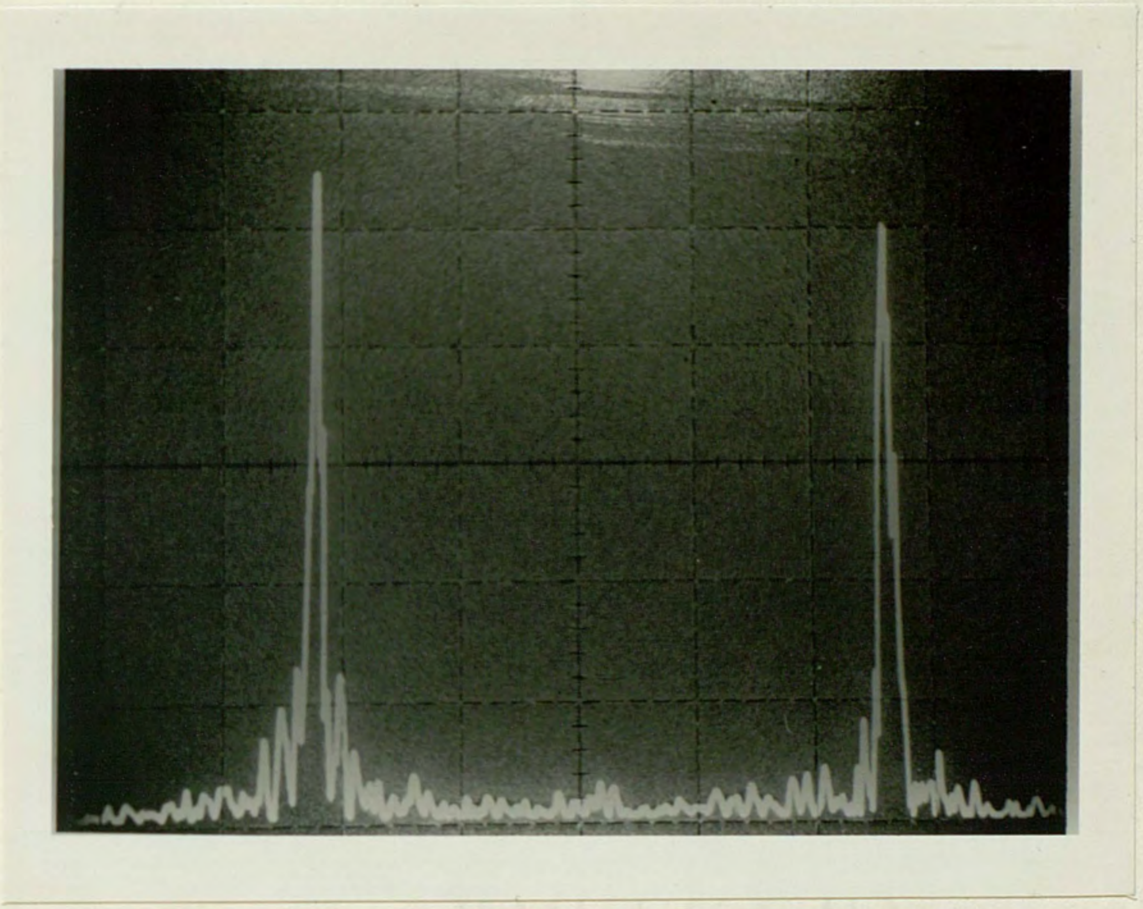
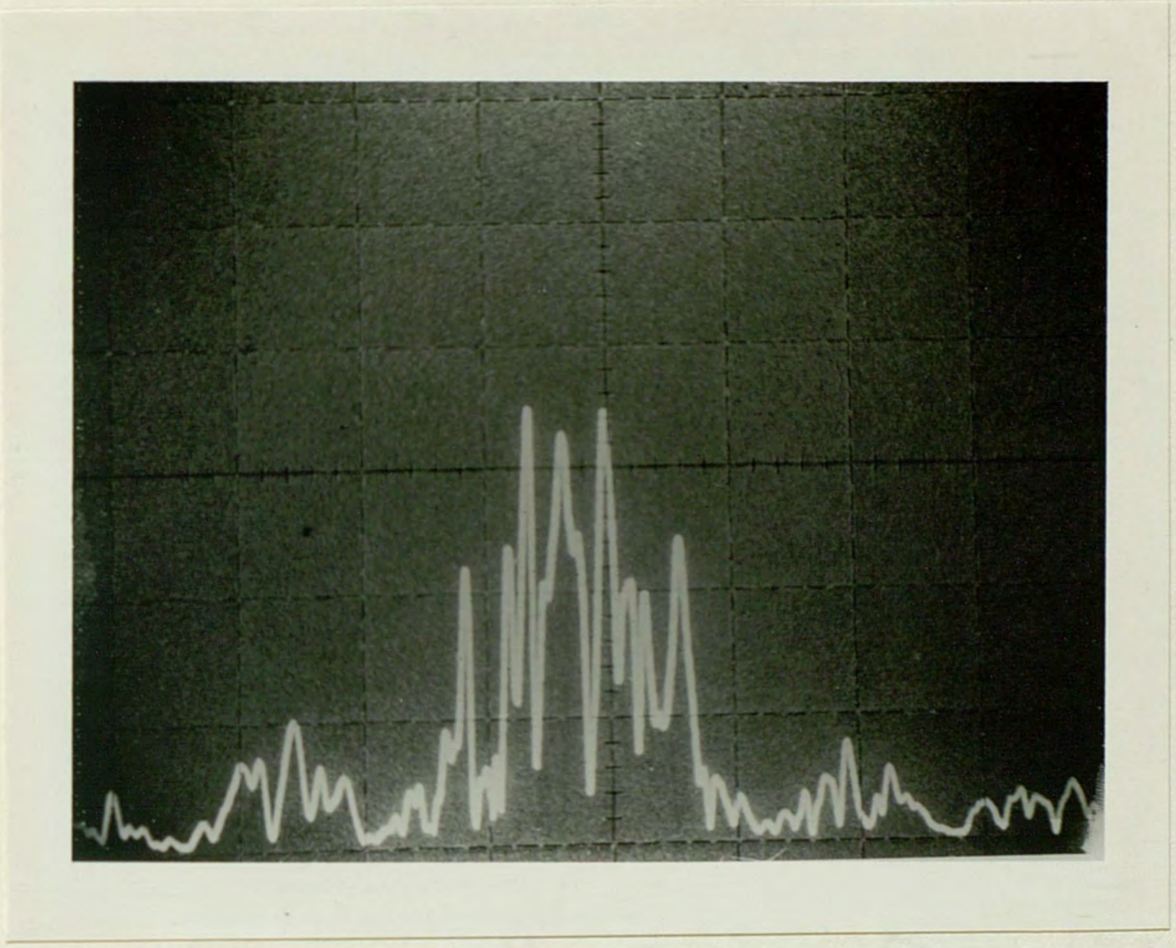


Figure 15. QPSK two sided power spectral density (PSD).



500 hz / div

Figure 16. PSD at the carrier frequency.

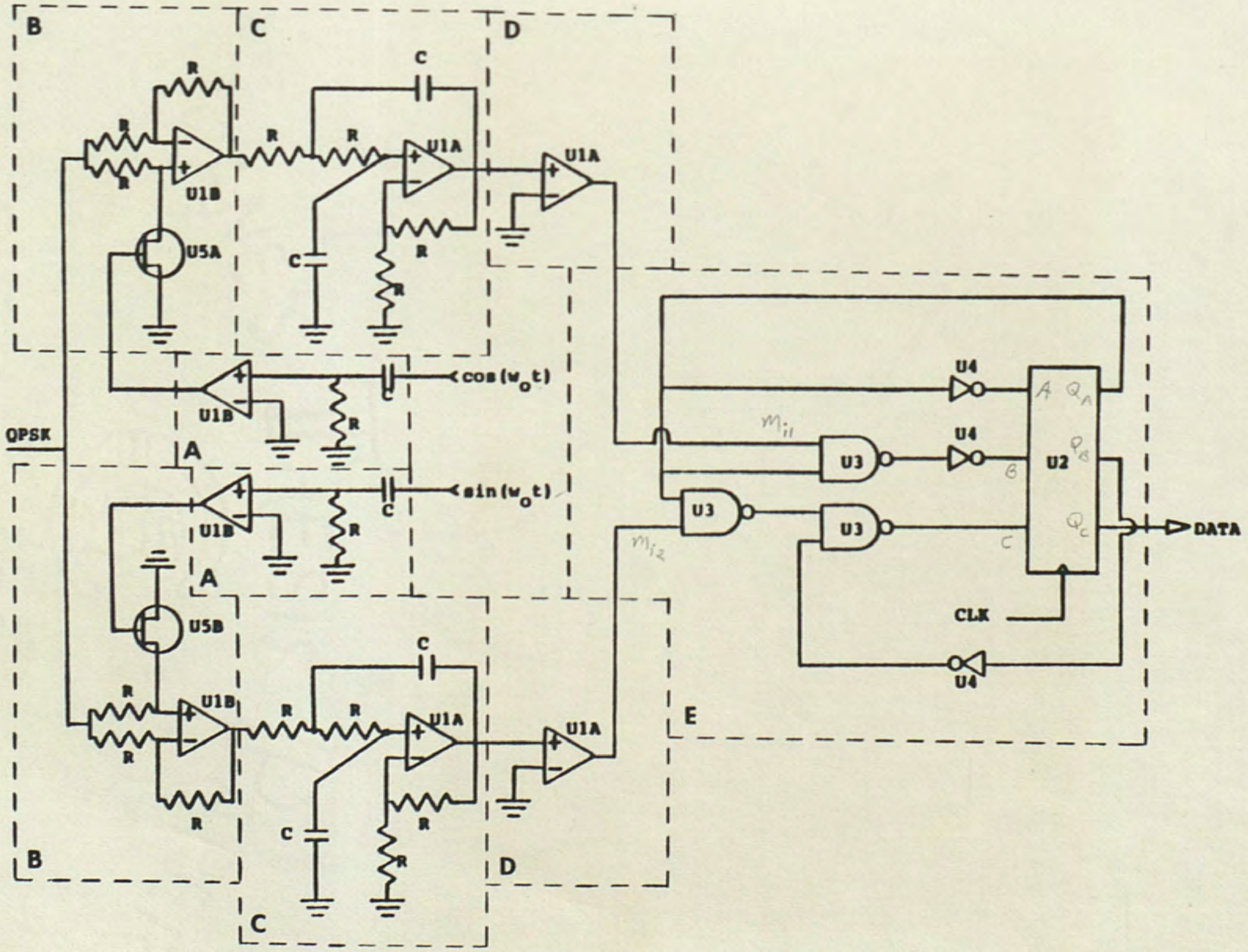


Figure 17. QPSK demodulator circuit design.

QPSK demodulator. The basic parts list is as follows:

U1	TL084	LF347	~~Bi~~Quad - op amp.
U2	74LS95		4-bit shift register
U3	74LS00		NAND gate
U4	74LS06	04	Hex-inverter
U5	2N 3909		P-JFET

QPSK demodulator. Each block is defined as follows:

A = square wave carrier generator

B = multiplication of QPSK and local carrier

C = lowpass filter

D = threshold detector

E = parallel to serial converter.

Parallel to Serial Converter (PSC)

The state table is as follows:

	$m_{i1}(t)$ $m_{i2}(t)$				Output
States	00	01	10	11	Z
a	e	e	e	e	0
b	e	e	e	e	1
c	d	d	d	d	0
d	d	d	d	d	1
e	a	b	c	d	0
f	a	b	c	d	1

The state transition table is as follows:

	present state	$m_{i1}(t)$ $m_{i2}(t)$				output
states	$Q_AQ_BQ_C$	00	01	10	11	Z
a	000	100	100	100	100	0
b	001	100	100	100	100	1
c	010	101	101	101	101	0
d	011	101	101	101	101	1
e	100	000	001	010	011	0
f	101	000	001	010	011	1

The input equations to the PSC are

$$D_A = \overline{Q_A}$$

$$D_B = Q_A \cdot m_{i1}$$

$$D_C = (Q_A \cdot m_{i2}) + Q_B \; .$$

The output equation for the PSC is

$$Z = Q_C \; .$$

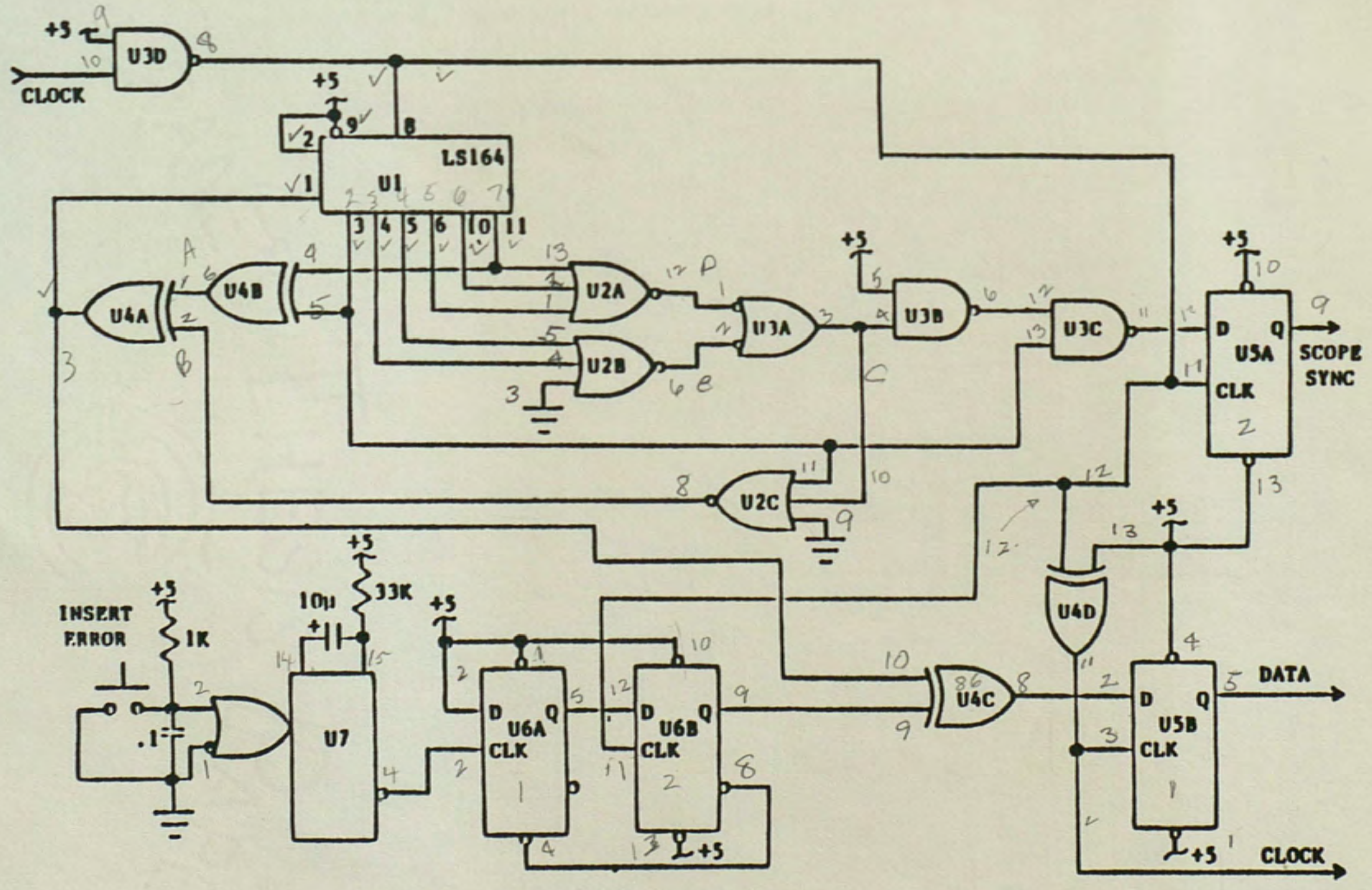


Figure 18. Pseudorandom generator circuit design [4].

PRBSG. The basic parts list is as follows:

U1	74LS164	8-bit shift register
U2	74LS27	NOR gate
U3	74LS00	NAND gate
U4	74LS86	Exclusive-OR gate
U5	74LS74	D-flip-flop
U6	74LS74	D-flip-flop
U7	74LS221	Monostable multivibrator.

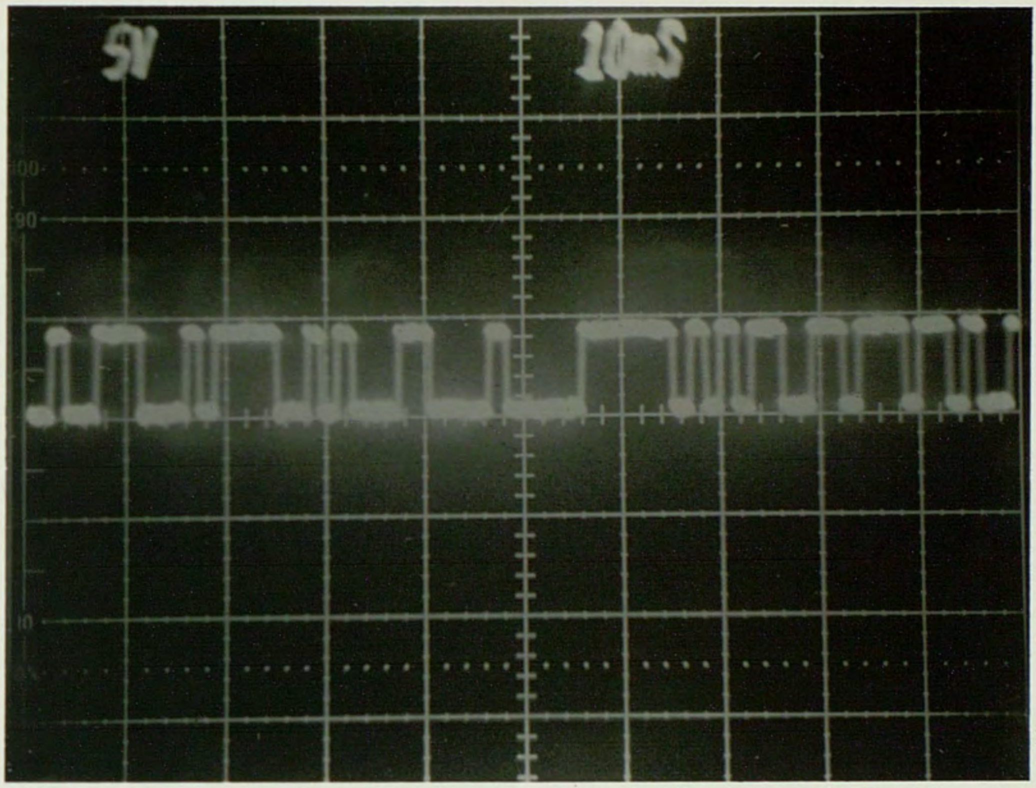


Figure 19. random data generated by the PRBSG.

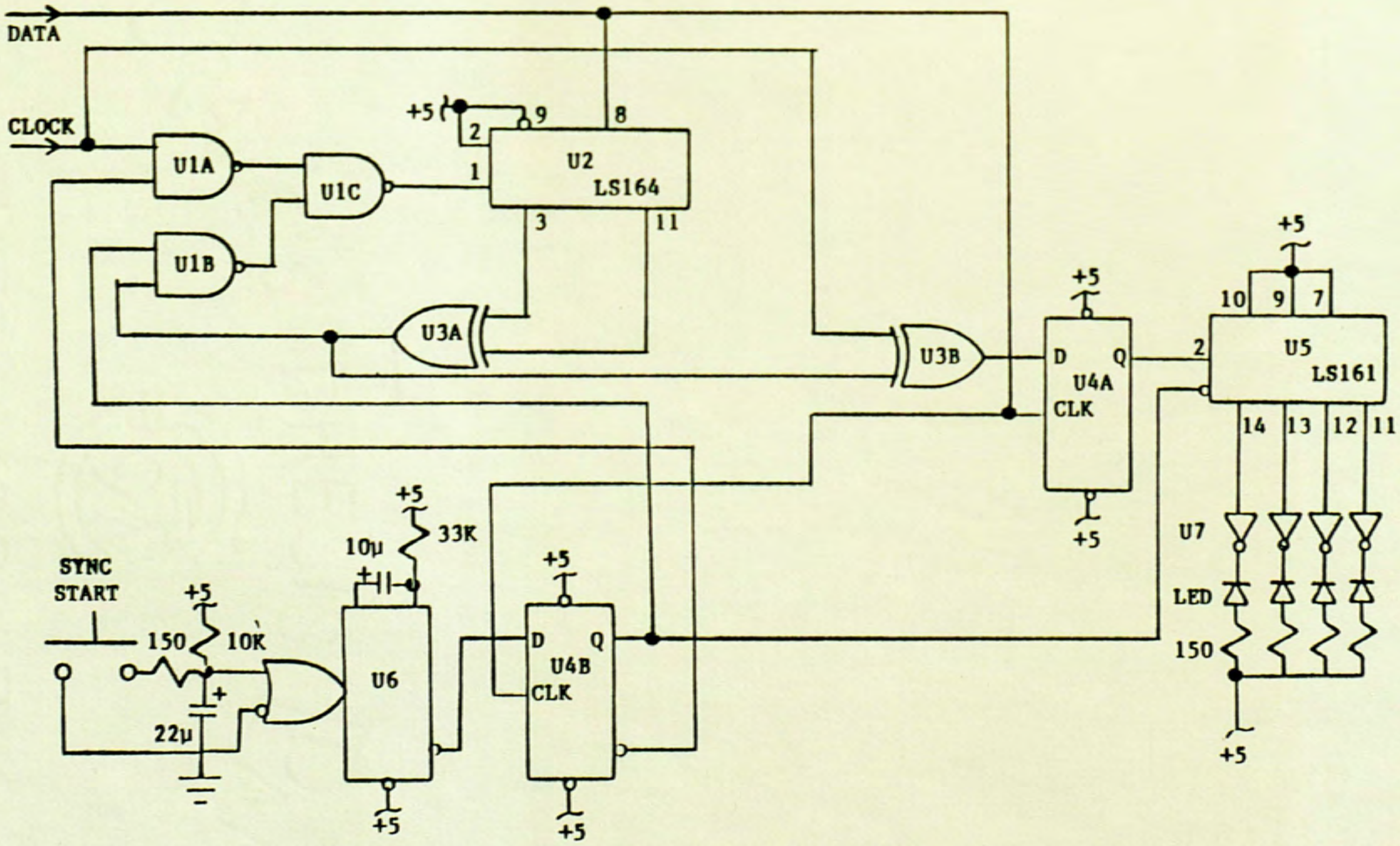


Figure 20. Pseudorandom correlator circuit design [4].

PRBSC. The basic parts list is as follows:

U1	74LS00	NAND gate
U2	74LS164	8-bit shift register
U3	74LS86	Exclusive-OR gate
U4	74LS74	D-flip-flop
U5	74LS161	4-bit counter
U6	74LS221	Monostable multivibrator
U7	74LS06	Hex-inverter.

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