STARS

University of Central Florida
STARS

Retrospective Theses and Dissertations

2001

Low voltage regulator modules and single stage front-end converters

Wei Gu
University of Central Florida

Part of the Electrical and Computer Engineering Commons
Find similar works at: https://stars.library.ucf.edu/rtd
University of Central Florida Libraries http://library.ucf.edu

This Doctoral Dissertation (Open Access) is brought to you for free and open access by STARS. It has been accepted for inclusion in Retrospective Theses and Dissertations by an authorized administrator of STARS. For more information, please contact STARS@ucf.edu.

STARS Citation
Gu, Wei, "Low voltage regulator modules and single stage front-end converters" (2001). *Retrospective Theses and Dissertations*. 1188.
https://stars.library.ucf.edu/rtd/1188

UNIVERSITY OF CENTRAL FLORIDA LIBRARIES
3 2103 01134 8863

LOW VOLTAGE REGULATOR MODULES AND SINGLE STAGE FRONT-END CONVERTERS

By
Wei Gu

2001

UCF

LOW VOLTAGE REGULATOR MODULES AND SINGLE STAGE FRONT-END CONVERTERS

by

WEI GU

B.S. Zhejiang Univeristy, 1993
M.S. Institute of Modern Physics, Chinese Academy of Science, 1996
Ph.D. Institute of Modern Physics, Chinese Academy of Science, 1999

A dissertation submitted in partial fulfillment of the requirements
for the Degree of Doctor of Philosophy
in the School of Electrical Engineering and Computer Science
in the College of Engineering and Computer Science
at the University of Central Florida
Orlando, Florida

Fall Term
2001

Major Professor: Issa Bataresh

ABSTRACT

Evolution in microprocessor technology poses new challenges for supplying power to these devices. To meet demands for faster and more efficient data processing, modern microprocessors are being designed with lower voltage implementations. More devices will be packed on a single processor chip and the processors will operate at higher frequencies, exceeding 1GHz. New high-performance microprocessors may require from 40 to 80 watts of power for the CPU alone. Load current must be supplied with up to 30A/μs slew rate while keeping the output voltage within tight regulation and response time tolerances. Therefore, special power supplies and Voltage Regulator Modules (VRMs) are needed to provide lower voltage with higher current and fast response.

In the part one (chapter 2,3,4) of this dissertation, several low-voltage high-current VRM technologies are proposed for future generation microprocessors and ICs. The developed VRMs with these new technologies have advantages over conventional ones in terms of efficiency, transient response and cost.

In most cases, the VRMs draw currents from DC bus for which front-end converters are used as a DC source. As the use of AC/DC frond-end converters continues to increase, more distorted mains current is drawn from the line, resulting in lower power factor and high total harmonic distortion. As a branch of active Power factor correction (PFC) techniques, the single-stage technique receives

particular attention because of its low cost implementation. Moreover, with continuously demands for even higher power density, switching mode power supply operating at high-frequency is required because at high switching frequency, the size and weight of circuit components can be remarkably reduced. To boost the switching frequency, the soft-switching technique was introduced to alleviate the switching losses.

The part two (chapter 5,6) of the dissertation presents several topologies for this front-end application. The design considerations, simulation results and experimental verification are discussed.

ACKNOWLEDGMENTS

I sincerely thank my advisor, Dr. Issa Batarseh for his guidance, encouragement and support throughout the course of this work. His decent personality has set up an example for my life. His extensive knowledge, vision and creative thinking have been a source of inspiration for me.

I would also like to thank Dr. Peter Kornetzky, Dr. Wei Huai and Dr. Guangyong Zhu for many enlightening discussions, suggestions, and encouragement.

I wish to express my deepest appreciation to my fellow students Dr. Shiguo Luo, Dr. Chris Iannello, Mr. Weihong Qiu and Dr. Wenkai Wu. I am grateful to the Florida Power Electronics Center members, Mr. Jaber Abu Qahouq and Miss Manasi Soundalgekar for their help and cooperation.

My special thanks go to my committee members: Dr. Takis Kasparis, Dr. Tom Wu, Dr. Xin Li, and Dr. Jamal Nayfeh.

Finally, my heartfelt appreciation goes to my parents and my wife for their love.

This work is supported by NSF grant, NASA STTR research grant, and University of Central Florida.

TABLE OF CONTENTS

CHAPTER ONE : INTRODUCTION 1

1.1 Background 1

1.2 Voltage Regulator Module 3

1.2.1 Non-isolated VRM 4

1.2.2 High-Input-Voltage VRM 7

1.3 PFC Single Stage AC/DC Converter 11

1.3.1 Power Factor Correction Methods 11

1.3.2 Soft-switching Technique 15

1.4 Dissertation Outline 18

1.4.1 Interleaved Synchronous Buck Regulator with Hysteresis Control 18

1.4.2 New Interleaved Half-bridge Converter with Peak Current Control 19

1.4.3 Low Voltage PWM FB-ZVS DC/DC Converter 19

1.4.4 A Dual Output Low-Voltage Converter 20

1.4.5 PFC Single Stage AC/DC Converter 20

1.4.6 A New Single Stage Topology 20

CHAPTER TWO : A NOVEL INTERLEAVED SYNCHRONOUS BUCK REGULATOR 21

2.1 Synchronous Buck Regulator With Hysteresis Control 21

2.2 Novel Interleaved Synchronous Buck Regulator 22

2.2.1 Operation Principle 25

2.2.2 Design Consideration 26

2.2.3 Simulation and Experimental Results 30

CHPATER THREE : A NOVEL INTERLEAVED HALF-BRIDGE CONVERTER 40

3.1 Half-bridge Converter With Peak Current Control 40

3.2 Novel Interleaved HB Converter 42

3.2.1 Operation Principle 42

3.2.2 Design Consideration 44

3.2.3 Simulation and Experimental Results 45

3.3 Summary..... 50

CHAPTER FOUR : LOW VOLTAGE DC/DC CONVERTERS 51

4.1 Low-voltage PWM FB-ZVS Converter 51

4.1.1 Operation Principle 51

4.1.2 Controller Design Consideration 58

4.1.3 Simulation Results 58

4.2 A Low-voltage Dual Output DC/DC Converter 61

4.2.1 Multiple Output Converters 61

4.2.2 Family I: Solutions without post regulator 62

4.2.3 Family II: Solutions with post regulation 64

4.2.4 Family III: Equally controlled outputs 66

4.2.5 Operating Analysis 68

4.3 Summary 71

CHAPTER FIVE : A NOVEL SOFT-SWITCHING SINGLE STAGE CONVERTER 72

5.1 Introduction 72

5.2 Power Factor Correction 74

5.2.1 CCM Shaping Technique 76

5.2.2 DCM Shaping Technique 78

5.3 Single Stage Hard-switching Topology 81

5.3.1 Single Stage Topology 81

5.3.2 Limitations of Hard-switching 84

5.4 Novel Soft-switching Methods 85

5.4.1 Operation Principles 85

5.4.2 Simulation and Experimental Results 92

5.5 Summary 95

CHAPTER SIX : A NEW SINGLE SWITCH SINGLE STAGE TOPOLOGY 96

6.1 A Novel Single Stage AC/DC Converter 96

6.1.1 Operation Principle 96

6.1.2 Simulation and Experimental Results 99

6.2 Summary 102

CHAPTER SEVEN : CONCLUSIONS 107

APENDIX: MATHCAD CODES FOR COMPENSATOR DESIGN 120

LIST OF REFERNCES 156

LIST OF FIGURES

Figure1-1: Two Choices for Computer Power Supply 2

Figure 1-2: Typical output voltage transient (top) and load current (bottom) 4

Figure 1-3: Practical VRM load model 4

Figure 1-4: Buck converter for low voltage/high current applications 5

Figure 1-5: Diagram for hysteretic control 6

Figure 1-6: Topologies for low voltage/high current application 10

Figure 1-7: Block diagrams of power factor correction circuits (a) passive power factor correction, (b) active two-stage, (3) single stage 14

Figure 2-1: General layout out interleaved converters and its waveforms 23

Figure 2-2: General layout for the interleaved synchronous buck converter 24

Figure 2-3: Current waveforms and gate signals of the upper-side MOSFETs 25

Fig. 2-4: Output ripple for the hysteretic controlled circuit 27

Figure 2-5: Estimation of switching frequencies 29

Figure 2-6: Inductor current runaway 29

Figure 2-7: Without current sharing, current difference is around 4A (total current: 26A) 31

Figure 2-8: With current sharing, current difference is around 0.2A 32

Figure 2-9: General Layout with TPS5211 Controller Method 33

Figure 2-10: Without current sharing, current difference is around 4A (total current: 26A). 34

Figure 2-11: With current sharing, current difference is around 0.3A 34

Figure 2-12: Schematics, (a) sequence circuit, (b) reset and protection circuit 35

Figure 2-13: simulation result 36

Figure 2-14: Interleaved hysteretic controlled converter prototype 37

Figure 2-15: Some preliminary results. 38

Figure 3-1: Distributed power system 40

Figure 3-2: Proposed layout for the interleaved half-bridge converter 43

Figure 3-3: Schematic of phase shift circuit 46

Figure 3-4: Simulation Results for interleaved half-bridge converter 46

Figure 3-5: Half-bridge Prototype 48

Figure 3-6: MOSFETS' gate signals at light load 48

Figure 3-7: MOSFETS' gate signals at heavy load 49

Figure 3-8: Voltage across the output diodes 49

Figure 3-9: Sensed current and external ramp signal 49

Figure 4-1: FB-ZVS-PWM converter and primary waveforms 52

Figure 4-2: Operation modes of FB-ZVS-PWM converter 54

Figure 4-3: Q4 voltage at different load current 56

Figure 4-4: Voltage control simulation result 59

Figure 4-5: Part of the schematic for hysteretic control outer loop 59

Figure 4-6: Voltage control with a hysteretic outer loop simulation result 60

Figure 4-7: Average current control simulation result 60

Figure 4-8: Multi-output Flyback Converter 64

Figure 4-9: Secondary side post regulator 66

Figure 4-10: General layout of the new dual output converter 67

Figure 4-11: General layout of the new converter and a forward converter 69

Figure 4-12: Some simulation results for the new converter 71

Figure 5-1: Classification of PFC conducted schemes 75

Figure 5-2: Block diagram of PFC converter with CCM shaping technique 77

Figure 5-3: DCM input pre-regulator in two-stage AC/DC power supply 79

Figure 5-4: DCM input corrector in single-stage AC/DC power supply 80

Figure 5-5: Basic circuit schematic of the converter 82

Figure 5-6: Theoretical key waveforms of the converter 83

Figure 5-7: Proposed soft-switching topology 85

Figure 5-8: Main Switching Waveforms 86

Figure 5-9: Modes of Operation 89

Figure 5-10: Simulation Results..... 93

Figure 5-11: Input current (1A/div) and input voltage (100V/div) 94

Figure 5-12: Main switch ,current (2A/div) and voltage (100V/div) 94

Figure 5-13: Auxiliary switch, S_a, Current (upper trace 1A/div) and voltage

(lower trace 200v/div) 95

Figure 6-1: Proposed single stage topology with lower stress 97

Figure 6-2: Operation Mode of the proposed single stage topology 97

Figure 6-3: Main waveforms 98

Figure 6-4: Simulation results 100

Figure 6-5: Experimental results 101

Figure 6-6 Power factor vs. input voltage with different loads 101

Figure 6-7: Efficiency vs. input voltage (low trace: hard-switching converter in chapter 5, top trace: new converter) 101

CHAPTER ONE

INTRODUCTION

1.1 Background

In recent years, with fast improvement in CPU speed, on-board distributed low voltage DC/DC converters have been increasingly used as the CPU power supply. Because of the increased requirement for high-performance microprocessors 40 to 80 watts are necessary to power the CPU alone and load current must be supplied with up to 30A/us slew rate while keeping the output voltage within tight regulation and response time tolerances [1,2,3]. Therefore, load regulation and dynamic performance became noticeable and it is necessary to improve power quality when designing the distributed low voltage DC/DC converters for CPU power supply.

In order to satisfy the increasingly stringent power requirements, three advanced power conversion circuit schemes are designed to meet the requirements for next generation of computers. The proposed computer power supply is shown in Figure 1-1 and it is composed of front-end converter and Voltage Regulator Modules (VRMs). The function of the front-end converter is equivalent to a rectifier plus a unit PFC and a DC/DC converter. The output voltage of the front-end converter can be $48V$ for isolated VRM or 5-$12V$ for non-isolated VRM. For both isolated and non-isolated VRMs,

interleaved technology is used to increase dynamic performance and decrease input and output current ripple.

In recent years, DC distributed power system (DPS) has been extensively used in mainframe computer, communication and military systems. However, the basic concepts and design philosophy can be tailored for developing future computer system power supply. In Figure 1-1, the output voltage of the single stage PFC can be 48V for isolated dc/dc converters or 5-12V for non-isolated VRMs.

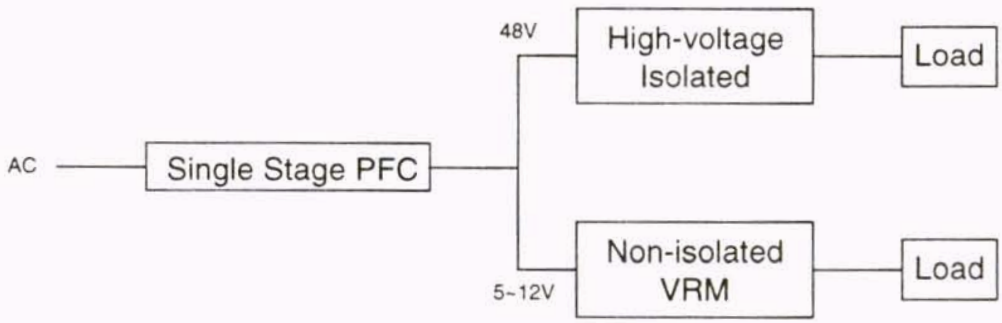


Figure1-1: Two Choices for Computer Power Supply

For the new and future generation computer power supplies, the off-board silver-box is still kept to interface the utility [4, 5]. This part is analogous to a bulk power system in communication DPS. An internal DC bus is generally can be found in the bulk power supply. The functions of this bulk power supply are to generate proper bus voltage for the on board VRMs and to directly support some regular loads where their specifications are relatively looser. To comply with the present regulatory standards, some low power level low-cost ac-dc converters with power factor correction (PFC) and

electrical isolation can be considered as options. Normally, the VRMs should be placed close to or packaged on the units that need restrictedly regulated supplies to minimize the affects due to the parasitic parameters.

1.2 Voltage Regulator Module

This research aims at evaluating system architecture of new generation computer power supplies and exploring new low-voltage converters to meet the more stringent load requirements. Efforts are focus on investigating several new low-voltage high-current and fast transient VRMs. The resultant technology will have extensive commercial applications in servers, personal computers and Internet equipment. It is found that with the more aggressive power management needed, the problems with current approaches become more apparent.

Normally, the VRM is a buck converter. Synchronous rectification technique is generally used to decrease the conduction loss due to high output current. The maximum current slew rate for PENTIUM® II processor can be 30A/μs, which means even a VRM with 1MHz switching frequency (switching period is 1μs) has no chance to respond to a fast current change. Therefore, the control circuit mainly gives the treatment for transient output voltage deviation during the interval after the rising time of the load current (segment 4 in Figure 1-2) [3]. A good output response will bring the output voltage back within the static tolerance as fast as possible. The first spike V_1 is dominated by loop 1 as

L1 in Figure 1-3, the second spike V_2 is dominated by loop 3 (L3), and the third spike V_3 is dominated by loop 4 (L4).

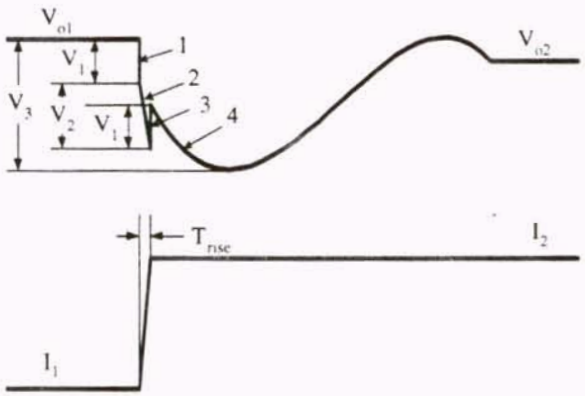


Figure 1-2: Typical output voltage transient (top) and load current (bottom)

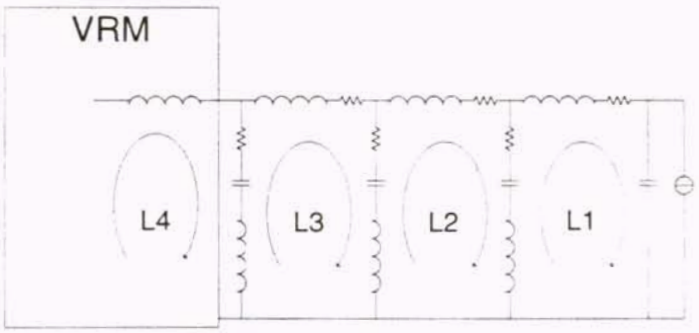


Figure 1-3: Practical VRM load model

1.2.1 Non-isolated VRM

Figure 1-4 shows the buck converters used in the VRMs along with their main switching waveforms. The low-side switch in the conventional buck is a diode and is replaced by a MOSFET because of its lower ON resistance to reduce the conduction loss.

Both the conventional buck and the synchronous buck can work in either Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM) which is also called Quasi-square Wave Converter (QSW). For DCM, faster transient response is achieved at the expense of higher ripple and lower efficiency when compared to the CCM case.

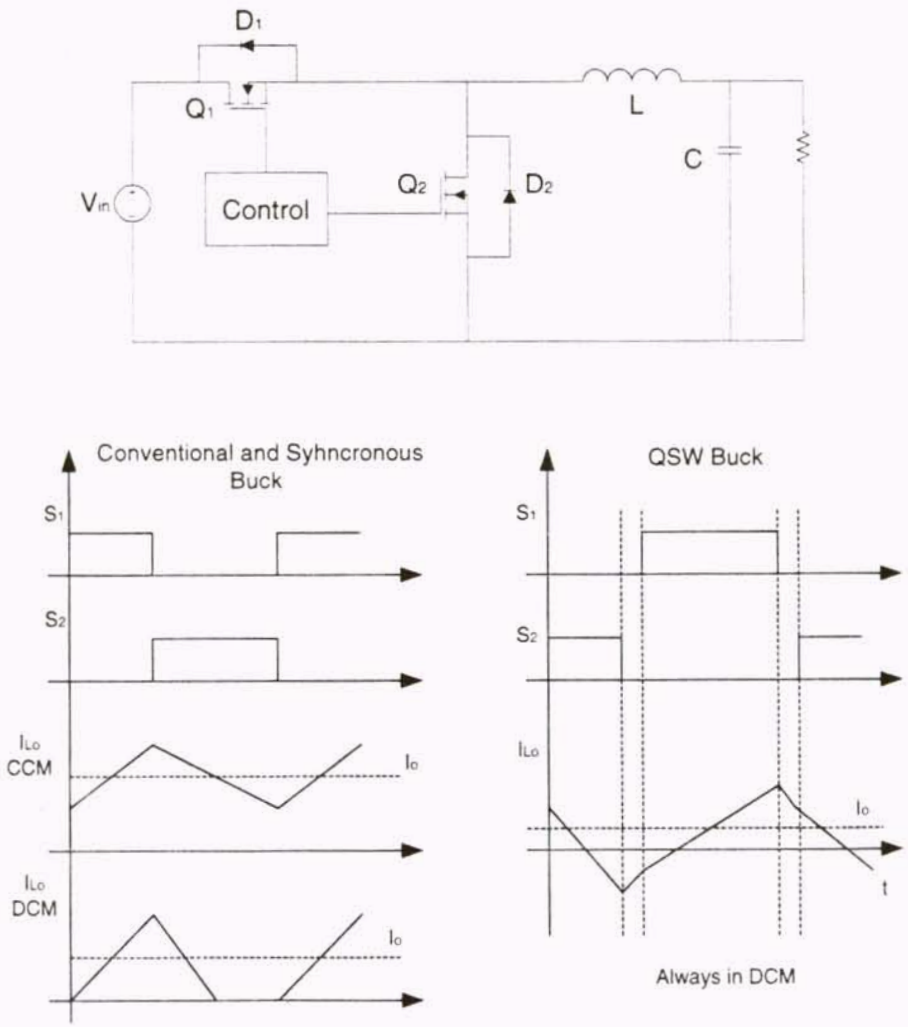


Figure 1-4: Buck converter for low voltage/high current applications

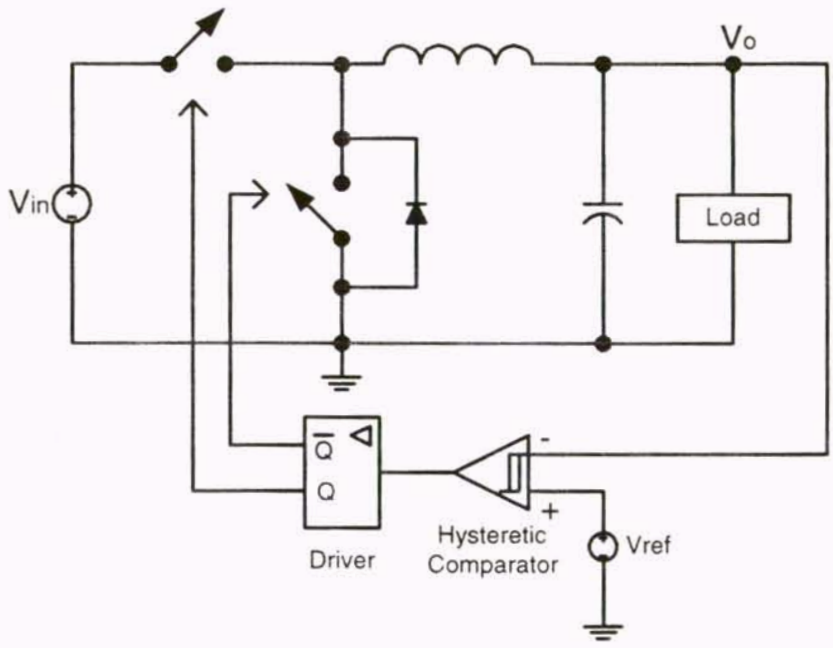


Figure 1-5: Diagram for hysteretic control

To control the output voltage ripple and maintain it within a hysteretic band centered about a reference voltage, the hysteretic method can be used as show in Figure 1-5. This type of controller tracks the output voltage and keeps it between a maximum voltage (V_H) and a minimum voltage (V_L) to limit the voltage ripple. The controller will turn on the high-side switch and turn off the low-side switch if the output voltage drops below V_L, and it will turn off the high-side switch and turn on the low side switch if the output voltage exceeds V_H.

The hysteretic controller keeps following the output voltage to produce the required control signals for the switches. If output-current or input-voltage transients occurs, the hysteretic controller will keeps turning on and off the switches until it corrects the output voltage.

1.2.2 High-Input-Voltage VRM

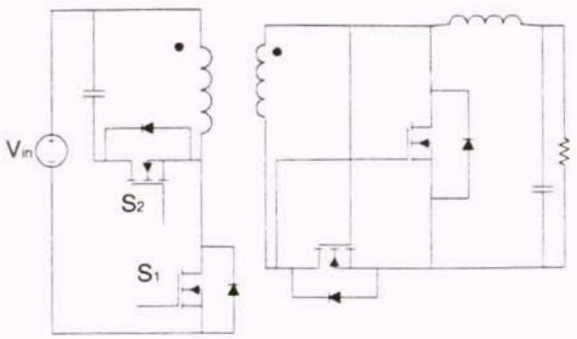
Most of today's VRMs draw power from a 5V output of a silver box. This silver box concept has existed for more than two decades. However, its loads, such as microprocessors and memory chips, keep updating every eighteen months [3]. Since the silver box output can not meet the strict transient and efficiency requirements from these kinds of loads, the high-input-voltage VRMs are expected to be placed between the loads and the silver box output.

To further increase their processing speed and decrease the power consumption, the operating voltages of the next generation of computer microprocessors will be reduced to around 1V. It is expected that today's processors will require much more power and will present even more dynamic loads than today's microprocessors. To keep the distribution losses low at an increased power level, the input voltage of the new generation VRMs has to be increased.

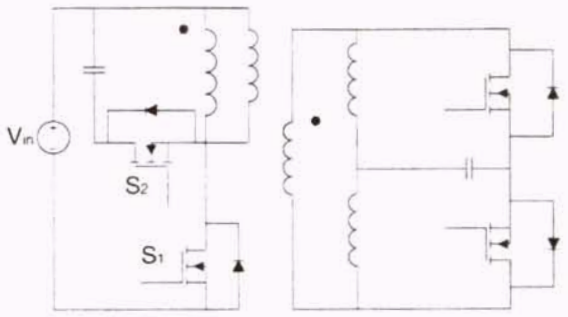
In this section, we present several existing topologies with a high input voltage for a reduced distribution loss.

In Figure 1-6(a), the output inductor current flows through the synchronous rectifier in its secondary, so the switch current ripple cannot be cancelled compared with other two channel output inductors. This means we must compromise between transient performance and output current ripple. In Figure 1-6(b), this topology has high efficiency but low close loop bandwidth. Furthermore, this topology will cause transformer core saturation and consequently increase the switch stress. In Figure 1-6(c) and (d), half bridge topology has low switch voltage stress and high efficiency. However its efficiency is still lower than push-pull topology due to its low turns ratio and high primary conduction loss. For (d), the series capacity in primary can block dc current and prevent core saturation. In Figure 1-6(e), the switch voltage is clamped at two times input voltage and its input current ripple is half of half bridge and push-pull topology.

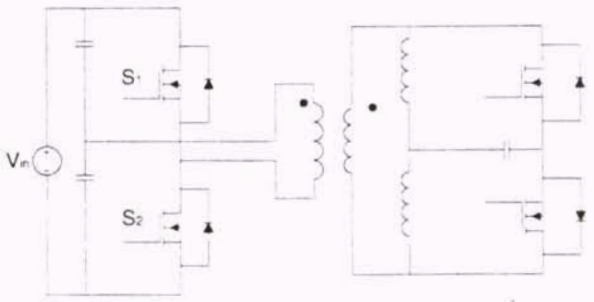
The push-pull forward, asymmetrical half-bridge, and full-bridge (introduced later) topologies are well-suited for the low-voltage/high-current applications with the current-doubler in the secondary side. Due to the low current stress and two times voltage stress in push-pull forward topology in primary, it is more suited for the low-voltage/high-current on-board converters operating from 12V than from 48V. Among considered topologies, the bridge topology seems to be a good choice for the on-board converter with the 48V input. Using phase-shift control, a full-bridge topology with zero-voltage-switching of the primary switches will be presented in the following part.



a) Active clamp forward

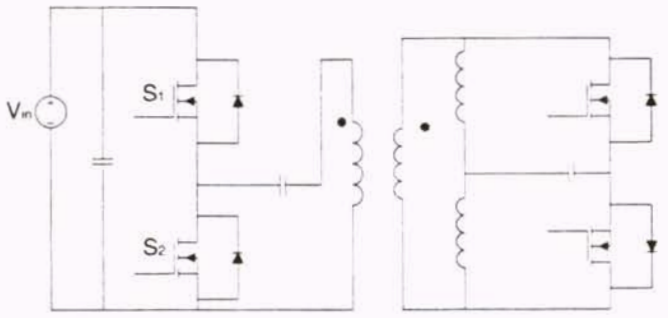


(b) Flyback forward converter

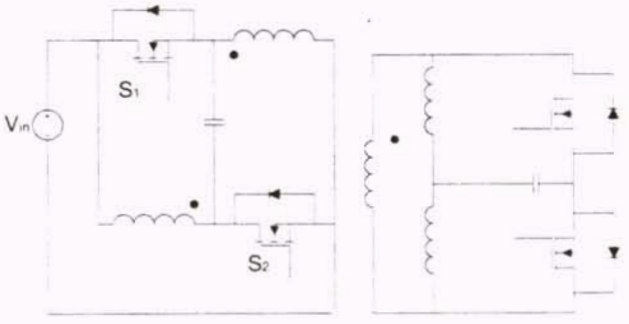


(c) Symmetrical half bridge

UCF LIBRARY, ORLANDO, FL 32816



(d) Asymmetrical half bridge



(e) Push-pull forward

Figure 1-6: Topologies for low voltage/high current application

1.3 PFC Single Stage AC/DC Converter

Traditional diode rectifiers used in front of the electronic equipment draw pulsed current from the utility line, which deteriorates the line voltage, produce radiated and conducted electromagnetic interference, leads to poor utilization of the capacity of the power sources. In compliance with IEC 1000-3-2 harmonic regulation, many power factor corrected (PFC) ac-dc rectifiers have been proposed in recent years [6]. In a single-stage PFC, input-current shaping, isolation, and fast output regulation are performed in a single stage. This method provides a compromise between the performance and cost. Comprehensive comparisons of the three approaches at manufacture cost and performance have shown that the single-stage PFC is a cost-effective solution for low power applications.

1.3.1 Power Factor Correction Methods

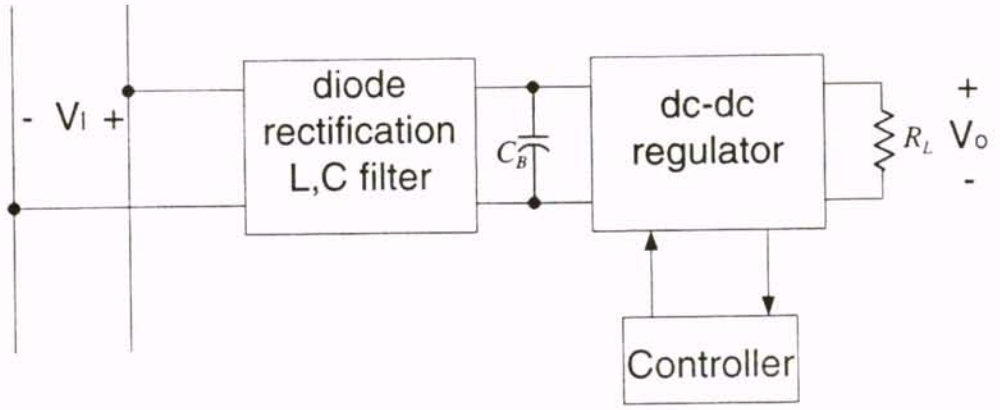
Generally, three PFC approaches are commonly used in current power supply product with high power factor features, i.e., passive approach, active two-stage and single-stage PFC approaches. Each one has its merits and limitations and applicable field. Figure 1-7(a) shows the block diagram of a passive PFC scheme. In this approach, a full-bridge rectifier with a LC filter is used to meet the line current harmonic limit. Generally, choke L of the low-frequency filter can be placed either on the dc or ac side of rectifier.

UCF LIBRARY, ORLANDO, FL 32816

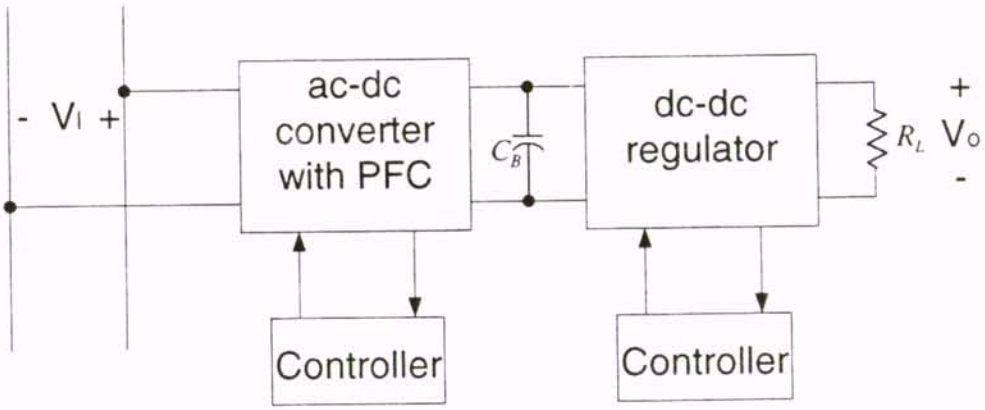
The block diagram of the active two-stage approach is shown in Figure 1-7(b). In this approach, two converters are used to achieve PFC and wide bandwidth regulation of the output voltage. An ac/dc converter is connected to the line to provide good input power factor and generator a roughly regulated dc voltage. Usually this voltage cannot directly supply the load since it contains intolerable second harmonic content. Therefore, a dc/dc converter is cascaded to tightly regulate the output voltage. These two power stages are controlled separately.

Today, there are many active single-stage PFC approaches available. Figure 1-7(c) shows a typical block diagram of an active PFC scheme. This approach combines the power factor correction converter and the voltage regulation converter in one stage. The underlying strategy of this scheme is to design the circuit in such a way that it allows its PFC circuit and voltage regulation circuit to share the same power switch. Typically, the input circuit in one-stage PFC power supplies uses DCM voltage follower technique, in which the peak of the input current is proportional to the instantaneous line voltage automatically. The average input current per switching cycle (i.e. line current) is therefore tracing the line voltage in shape and phase.

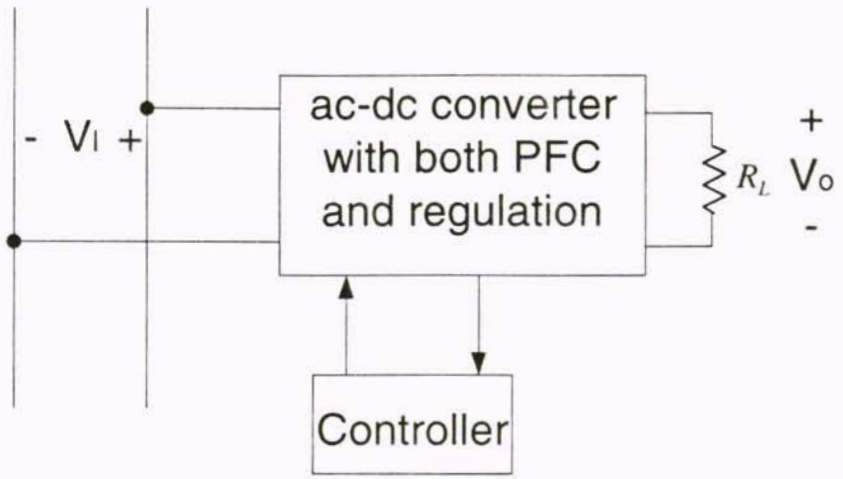
Compared to the active techniques, the major advantages of the passive PFC technique are higher efficiency, high reliability and relative lower cost. The major drawback of the approach is a relative large size choke. In addition, bulk capacitor voltage has a big variation with input voltage. The varying voltage has a detrimental effect on optimization of dc/dc converter.


- Vi +
diode
rectification
L,C filter
C_B
dc-dc
regulator
R_L
+
Vo
-
Controller

(a)


- Vi +
ac-dc
converter
with PFC
C_B
dc-dc
regulator
R_L
+
Vo
-
Controller
Controller

(b)



(c)

Figure 1-7: Block diagrams of power factor correction circuits (a) passive power factor correction, (b) active two-stage, (3) single stage.

In two-stage scheme, the first stage provides a regulated intermediate bus voltage. Due to the relative constant bus voltage, the design of the second stage, dc/dc converter, can be optimized. In addition, because of a relative high bus voltage, the capacitance of the bulk capacitor can be minimized for a given hold-up time requirement. However, the two-stage approach suffers from an increased circuit complexity and cost since it requires two power stages and two controllers.

Due to the simplified power stage and control circuit of the single-stage scheme, it is attractive to many applications with cost and size restrictions. The major deficiency of single-stage circuit is that the bulk capacitor voltage varies with the line voltage and load

current. Due to this drawback, in some single-stage circuit, the peak voltage of the bulk capacitor is above 450V, which makes these circuits impractical because of high cost of high-voltage stage capacitors. Performance and cost-effectiveness are penalized because of varying capacitor voltage, especially in applications requiring a hold-up time such as computer power supplies.

1.3.2 Soft-switching Technique

To accommodate the ever-increasing demand for smaller size, lighter weight, and higher efficiency power supplies, switching-mode power conversion technologies have evolved from the conventional pulse-width-modulated (PWM) converter to resonant converters, quasi-resonant converters (QRCs), multi-resonant converters (MRCs), and most recently to soft-switching PWM converters [7]. Due to circuit parasitics and hard-switching condition, operation of a PWM converter involves high switching losses, switching stresses, and switching noises. These are the major factors that restrict PWM converters from operating at a higher frequency for size/weight reduction and performance improvement.

With the available devices and circuit technologies, PWM converters generally have been designed to operate with 50-200kHz switching frequency. In this frequency range, the power supply is deemed optimal in weight, size, efficiency, reliability, and cost. In more recent applications such as adaptor, notebook, and laptop computers where high power density is of primary concern, it is desirable to push the conversion frequency as high as the upper hundreds of kilohertz to lower-megahertz range. However, higher

switching frequency invariably results in increased switching losses. The switching loss at turn-off is primarily caused by the leakage inductance of the power transformer. As the semiconductor device turns off, the sharp di/dt induces high voltage spike across the leakage inductance. To reduce switching stress, dissipative snubbers are typically used. At turn-on, switching losses are mainly caused by abrupt discharging of the energy stored in the parasitic capacitance of the semiconductor devices. When the transistor is turned on, the energy stored in its output capacitance is dissipated in the device. Also, turn-on at high voltage levels induces a severe switching noise coupled through the Miller capacitance into the drive and control circuits. The aforementioned detrimental effects of the circuit parasitics become much more pronounced as the switching frequency is increased.

To improve switching conditions for semiconductor devices in switched-mode converters, several resonant techniques were proposed. The traditional series and parallel resonant converters, class-E quasi-resonant converters, multi-resonant converters, and resonant dc link converters are included in this category. By incorporating certain types of resonant network into a PWM topology, numerous resonant converters can be formed, offering a zero-voltage switching (ZVS) or zero-current switching (ZCS) condition for the switches. This improvement significantly reduces switching losses and enables the converter to operate at a higher switching frequency. However, due to the resonant nature of the current and voltage waveforms, the operation of resonant converters usually involves high circulating energy which results in a substantial increase in conduction losses. For instance, the ZVS-QRC technique employs an LC resonant network to shape the switch voltage waveform so that the power switch is operated with ZVS. Although

the switching loss is reduced, the transistor suffers from an excessive voltage stress that is proportional to the load range. The ZVS-MRC technique utilizes a multi-element resonant network to implement ZVS for both the active and passive switches. The unique arrangement of the multi-resonant network is aimed at absorption of all major parasitic components, including transistor output capacitance, diode junction capacitance, and transformer leakage inductance. This allows the ZVS-MRCs to operate at high frequencies while each semiconductor device in the circuit can operate at its switching condition. Nevertheless, both the active and passive switches in a ZVS-MRC are subjected to peak voltage and current stresses significantly higher than those in their PWM counterparts. Another major limitation of the resonant converters is variable frequency operation. For converters operating with a wide input voltage range and load, the switching frequency range is also wide. As a result, the optimum design of the magnetic components (inductors and transformers) and EMI and output filters is difficult to achieve. In addition, the bandwidth of the closed-loop control is compromised, since it is determined by minimum switching frequency. Therefore, to attain a greater benefit from high-frequency operation, it is desirable to operate the converter at a fixed frequency. Although a number of constant-frequency resonant converters operating under either ZVS or ZCS have been proposed, operation of these converters still involves high circulating energy.

As a compromise between the PWM and resonant techniques, the soft-switching PWM techniques were proposed aimed at achieving soft-switching without a significantly increase in circulating energy. Generally, a soft-switching converter utilizes some form of resonant technique to soften the switching transition. When the switching

transition is completed, the converter reverts back to the familiar PWM mode of operation so that the circulatory energy can be minimized. Meanwhile, the switching frequency of the converter is kept fixed so that the circuit optimization can be easily attainable.

1.4 Dissertation Outline

The primary objectives of this dissertation are to develop advanced topologies and control technologies for low-voltage VRMs, and single stage front-end converters. The major contributions will be:

a) a proposed interleaved synchronous buck regulator with hysteresis control

b) a proposed interleaved half-bridge converter with peak current control

c) a proposed high-power low-voltage converter

d) a proposed dual or multiple output low-voltage converter

e) a proposed soft-switching method for an existing single stage front-end converter

f) a proposed single stage front-end converter with lower power device stress and higher efficiency.

1.4.1 A Novel Interleaved Synchronous Buck Regulator with Hysteresis Control

Next-generation microprocessors need lower-voltage, faster-response and higher-power-density power supplies. It's well known that interleaving technique and hysteretic

control are suitable for this task. In chapter two, by combining the interleaving techniques and hysteretic control, an interleaved synchronous buck regulator is explored and proposed. The simulation and experimental results suggest a promising future for low voltage application.

1.4.2 A Novel Interleaved Half-bridge Converter with Peak Current Control

An interleaved low-voltage half-bridge converter is proposed in this paper. With a Master-Slave peak current control, charge balances of the main transformers are automatically achieved. Thus current runaway is avoided without additional correction circuit. It is shown that the steady state analysis and simulation results are in a good agreement. A 48V input, 1.5V/60A output prototype is built to verify the proposed control method.

1.4.3 A High-Power Low-Voltage Converter

As the power consumption of high-performance microprocessors increases, the advantage of phase shift full-bridge converter for this application becomes apparent. Voltage control, peak current control and average current control are studied under transient response. The simulation results are discussed.

1.4.4 A Dual Output Low-Voltage Converter

In the telecommunication area, dual output or multiple DC/DC converters have a wide application. A new dual or multiple output DC/DC converter is proposed. In this converter, each output is controlled separately while the control signal for the main switch is from the output with the largest duty ratio. This method not only provides an alternative way for this application without patent issues, but also simplifies the traditional approaches by getting rid of the dummy load.

1.4.5 PFC Single Stage AC/DC Converter

A new single-stage power factor correction converter with the soft-switching of the main switch is proposed. High frequency operation of the proposed converter makes the ac-dc power supply possible to be minimized in size and weight.

1.4.6 New Single Stage Topology

A new single-stage, single-switch technique that combines the boost-like input-current shaper is described. In this technique, the boost inductor can operate in both the discontinuous and continuous conduction modes. By controlling the turns ratio of the windings, the input current harmonic contents can be reduced to comply with EN61000-3-2 limits.

CHAPTER TWO

A NOVEL INTERLEAVED SYNCHRONOUS BUCK REGULATOR

2.1 Synchronous Buck Regulator with Hysteresis Control

New high-performance microprocessors may require from 40 to 80 watts of power for the CPU alone [1]. Load current must be supplied with up to 30A/μs slew rate while keeping the output voltage within tight regulation and response time tolerances. Conventional synchronous regulator control techniques include PWM voltage control, PWM current control and variable frequency current control. CPU power supplies that are designed using these types of control methods require additional bulk storage capacitors to maintain output voltage within the regulation limits during the high di/dt load transients because of the limited bandwidth of the controller. Some controllers add a fast loop around the slower main control loop to improve the response time, but output voltage must deviate outside a fixed tolerance band before the fast loop becomes active[2].

Hysteretic control, also called bang-bang control or ripple regulator control, maintains the output voltage within the hysteresis band centered about the internal reference voltage. If the output voltage reaches or exceeds the reference plus one-half of the hysteresis band, the controller turns off the high-side MOSFETs and turns on the low-side MOSFETs. This is the power stage off-state, and it causes the output voltage to

decrease. When the output voltage is at or below the level of the reference minus one-half of the hysteresis band, the power stage is in off-stage. This hysteretic method of control keeps the output voltage within the hysteresis band around the reference voltage. Thus the output voltage is corrected as quickly as the output filter allows.

Unlike PWM-controlled power supplies, the output filter design is driven primarily by the need to provide satisfactory output voltage performance in response to fast load transients encountered when supplying power to next-generation microprocessors [2]. A smaller output filter is desired for fast response but leads to higher ripple which means higher switching frequency for the MOSFETs in a hysteretic control converter.

In a single module the switching frequency could reach such a large value that makes a small inductor value impractical to meet both the steady state and transient requirements. Thus an interleaved synchronous regulator that naturally cancels the output current ripple while achieving fast response is proposed to meet future requirements.

2.2 Novel Interleaved Synchronous Buck Regulator

It comes interleaved technique to reduce output ripple while maintaining transient performance and limiting inductor value [3]. The essential principle for interleaved technique is to parallel switches and inductors between input voltage and output capacity. The reason for reducing current ripple by interleaved technique is phase shifting among the different switches and they generate corresponding current delay in respective

inductors. Obviously, output current is summary of all branches and the total current ripple can be cancelled significantly due to the phase shifting of each branch current. This is illustrated in Figure 2-1. In general, interleaved technique is tantamount to increasing switching frequency while the effective output inductor is reduced due to parallel.

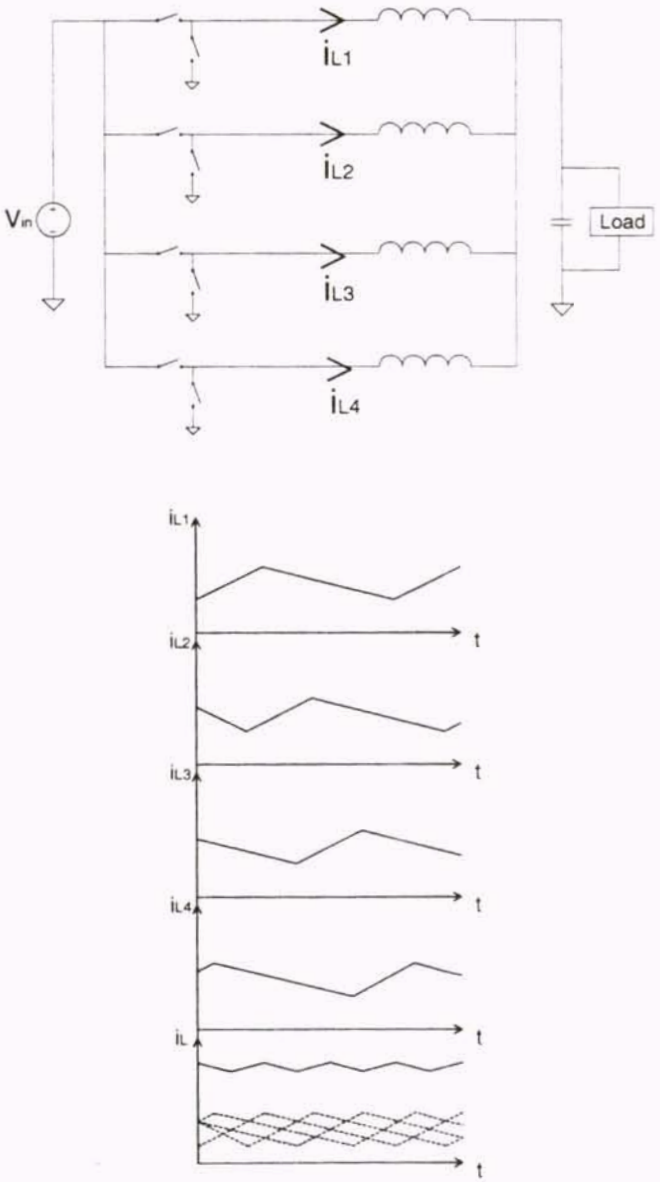


Figure 2-1: General layout out interleaved converters and its waveforms

UCF LIBRARY, ORLANDO, FL 32816

Utilizing interleaving technique, the output current of the converter can ramp fast than a single converter, and heat is spread among multiple components. But this technique is difficult to be applied to hysteretic controlled converter as the switching frequency is always changing and there is no synchronizing clock signal inside the control chip. This proposed method adopts a novel way to achieve multiphase regardless of the varying switching frequency.

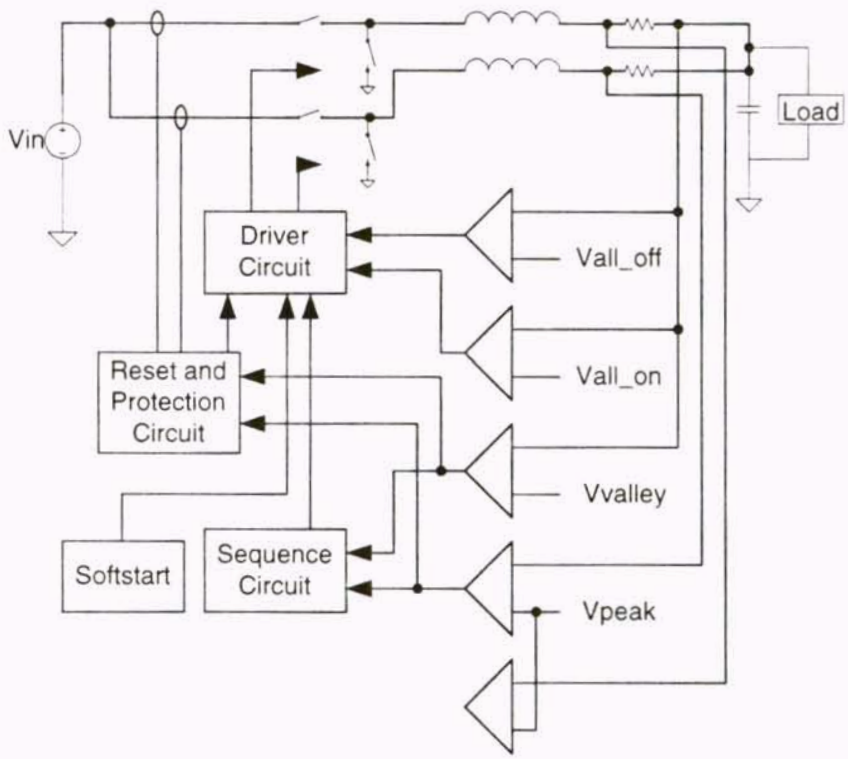


Figure 2-2: General layout for the interleaved synchronous buck converter

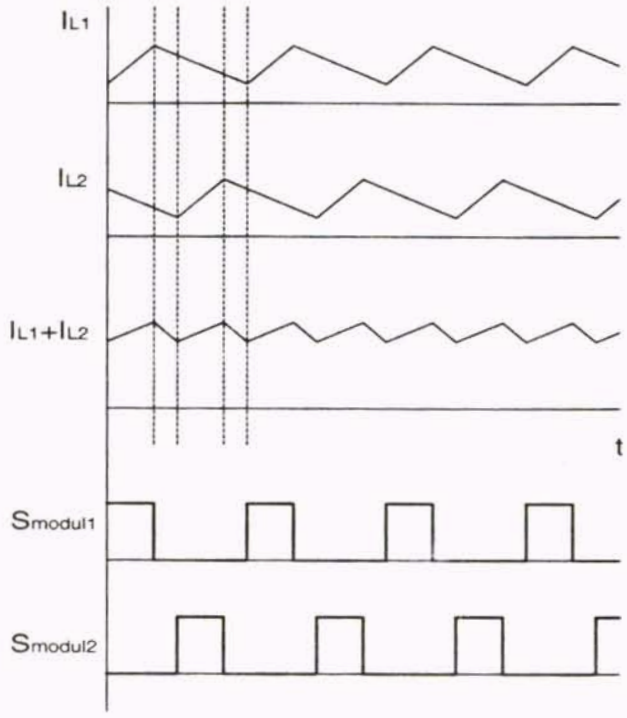


Figure 2-3: Current waveforms and gate signals of the upper-side MOSFETs

2.2.1 Operation Principle

The general circuit layout and typical waveforms are shown in Figures 2-2 and 2-3. Only a 2-module converter is presented for simplicity. In Figure 2-2, V_{peak} and V_{valley} are the hysteresis band boundary and Vall_on and Vall_off are the voltage levels below or above which all the switches will be on or off. The same comparators are used for all modules and interleaving is achieved through sequence circuit only. Reset circuit is activated during the large load transient using the same current probes for the MOSFETs protection circuit. For a 2-module interleaved converter, only a toggle is needed to obtain the desired sequence. The high-side switch of first module is turned on when the output

voltage hits the V_{valley} and then the high-side switch of second module is turned on at the next time the output voltage hits the V_{valley}. When the output voltage hits the upper boundary V_{peak}, both of the switches are turned off . Thus the two main switches work alternately with 180° phase shift. Figure 2-3 shows the waveforms of output inductor currents and switching driver signals.

During the startup, since the output voltage is lower than V_{all_on}, both high-side MOSFETs are on until output voltage exceeds that value. At this time, the output voltage is smaller than V_{peak}, so one high-side switch is already on and the other is off. The output voltage keeps increasing until it exceeds V_{peak}. Then both high-side switches are off and the output voltage goes down until it's smaller than V_{valley}, which would start another cycle.

After the elements of the output filter are determined, the power supply switching frequency must be estimated. If the estimated switching frequency is too high, the switching losses in the power MOSFETs will be high, resulting in less than optimum efficiency. If the estimated switching frequency is too low, the inductor value may be too high, resulting in unsatisfactory transient response.

UCF LIBRARY, ORLANDO, FL 32816

2.2.2 Design Consideration

To accurately predict the switching frequency of a hysteretic regulator, the output voltage ripple must be investigated as shown in Figure 2-4. The three elements of the capacitor that contribute to ripple are ESR, ESL, and capacitance.

$$V_{p-p}(t) = V_C(t) + V_{ESR}(t) + V_{ESL}(t) \qquad (2\text{-}1)$$

From [4,5], the equation for the switching frequency of one power stage converter is:

$$f_{s0} = \frac{V_O \times (V_I - V_O) \times (ESR - t_{del} / C_O)}{V_I \times (V_I \times ESR \times t_{del} + Hyst \times L - ESL \times V_I)} \tag{2-2}$$

where V_I is the input voltage, V_O is the output voltage, and tdel is the delay of the control circuit. For a 2-module interleaved converter, the ripple cancellation should be taken into account during the prediction.

The hysteresis band is equal to the difference between the peak-peak values of the V_O ripple (Vp-p), at the times $t_{on} - t_{del}$ and $t_{off} - t_{del}$, and given by,

$$Hyst = V_{p-p}(t_{on} - t_{del}) - V_{p-p}(t_{off} - t_{del}) \tag{2-3}$$

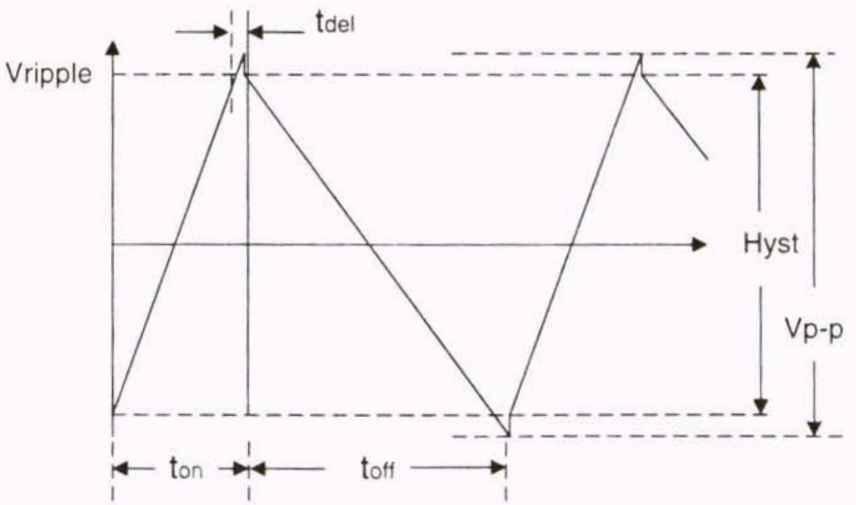


Fig. 2-4: Output ripple for the hysteretic controlled circuit

Based the above equations, the following equation for the switching frequency of a 2-module converter can be derived:

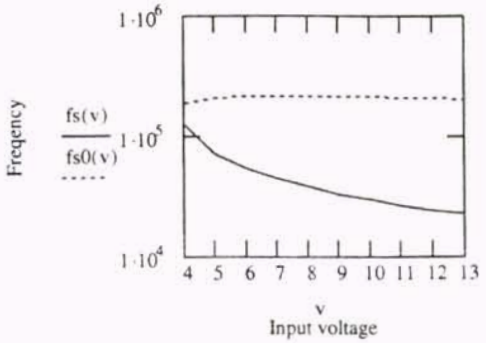
$$f_s = \frac{V_O^2 \times (V_I - V_O)^2 \times (ESR - t_{del}/C_O)}{2V_I V_O \times (V_I - V_O) \times (V_I \times ESR \times t_{del} - ESL \times V_I) + 2V^2_I \times (V_I - 2V_O) \times Hyst \times L} \quad (2\text{-}4)$$

Figure 2-5(a) and (b) give theoretical estimate of the switching frequencies against the input voltage or hysteresis band voltage.

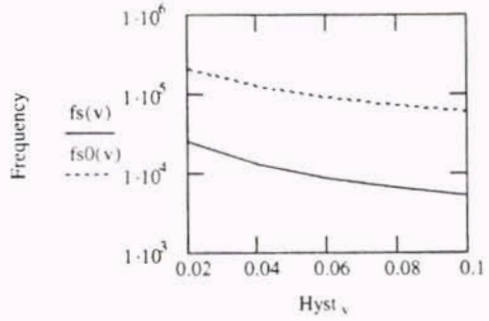
Three Os-con 820-μF, 4-V capacitors were used in this example circuit. ESR and ESL for each capacitor were 8mΩ, and 4.8nH, respectively. The other values that were substituted are the following: L=0.5μ, Hyst=20mV, tdel=0.8μs.

It can be shown that the output voltage would break out from the hysteretic band during large transient, and fail to reenter the band in some cases. Though the output voltage remains at a certain value, it is possible that the inductor currents I_{L1} and I_{L2} would runaway as showed in Figure 2-6. As for a hysteretic voltage control, the switches are only changing status according to the output voltage. This is because with a simple sequence circuit, after the large transient the status of the sequence circuit goes abnormal under certain conditions.

UCF LIBRARY, ORLANDO, FL 32816



(a) freq. vs input voltage



(b) freq. vs Hyst

Figure 2-5: Estimation of switching frequencies

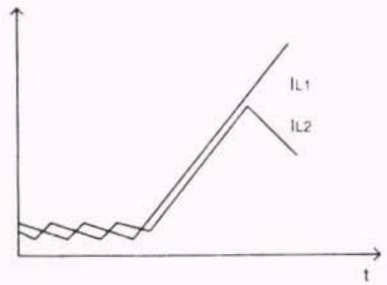


Figure 2-6: Inductor current runaway

This problem can be solved by adding a resetting circuit that locks the output of the sequence circuit and takes over control when either of the inductor currents reaches certain value. The power stage with the runaway current is turn off and only the other power converter is working to regulator the output voltage until both currents become the same again.

Due to the strict cost, size and efficiency requirements and integration purpose, the current sharing becomes more critical in the VRM design. For a two-module multiphase converter, the duty ratios are

$$D_1 = \frac{V_o - I_{o1} \times R_{on1}}{V_{in}} \tag{2-5}$$

and

$$D_2 = \frac{V_o - I_{o2} \times R_{on2}}{V_{in}} \tag{2-6}$$

I_{o1} and I_{o2} are the output currents for the two modules. R_{on1} and R_{on2} are the on resistances of the two high-side MOSFETs for the two modules. For the voltage control, we have, roughly, $D_1 = D_2$. Therefore, $I_{o1} \times R_{on1} = I_{o2} \times R_{on2}$. Usually, there is 20% difference for the on resistances of the MOSFETs. The larger the load current, the worse the current sharing results.

2.2.3 Simulation and experimental results

In Figure 2-2, two small resistors are added between the output inductors and the output. The feedback signal, which is used to compare with the reference V_{peak}, is not

UCF LIBRARY, ORLANDO, FL 32816

from the output node, but from the nodes between the two inductors and added resistors. As such, the current information is introduced into the control loop and current sharing is achieved.

Figure 2-7 shows the two current waveforms and output voltage ripple. Without current sharing (without adding the two small resistors), the current difference is around 4A out of the total current 26A with a 57% ON resistance difference. Figure 2-8 shows there is 0.2A difference with current sharing (the value of the added resistors is 0.001Ω).

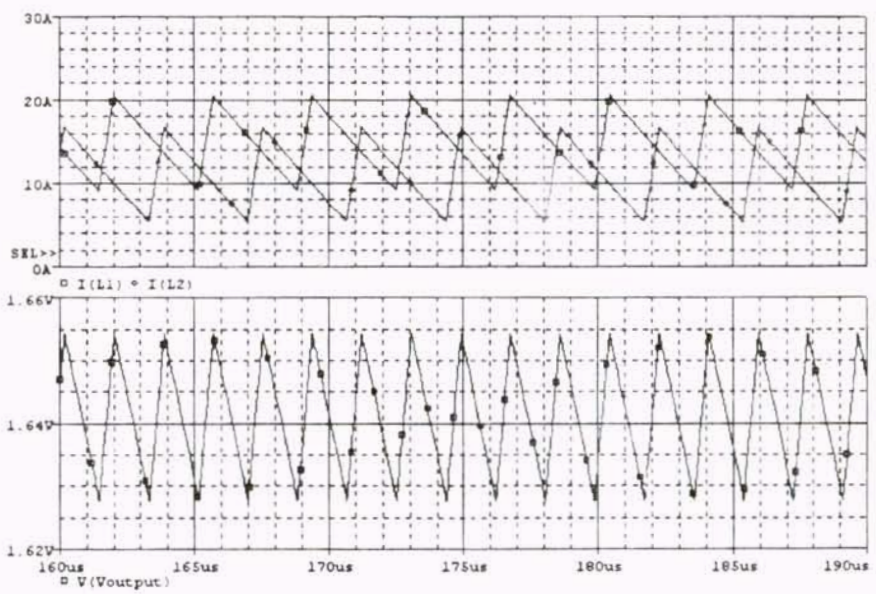


Figure 2-7 Without current sharing, current difference is around 4A (total current: 26A)

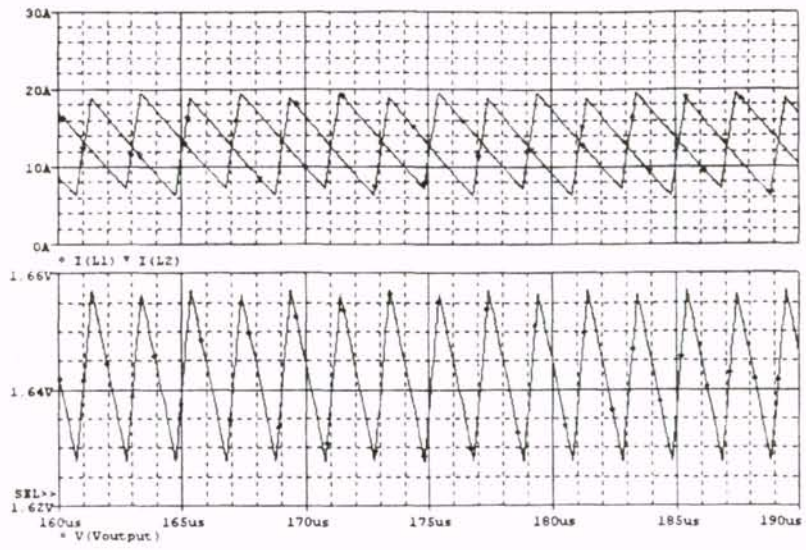
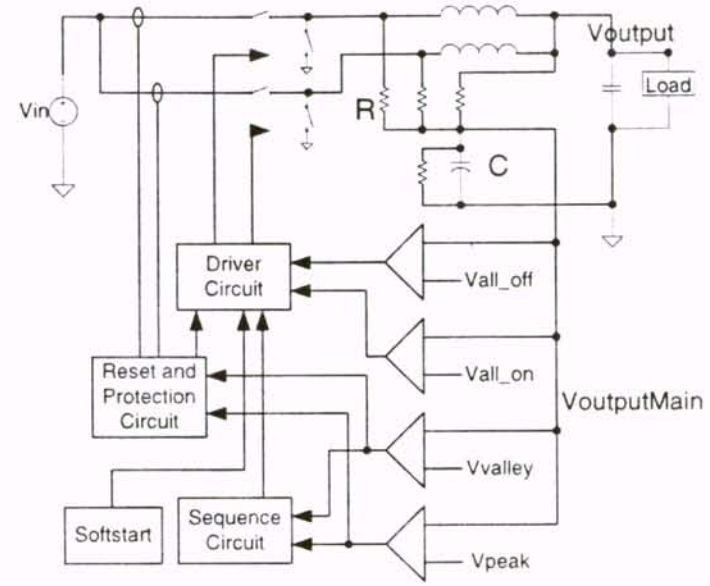


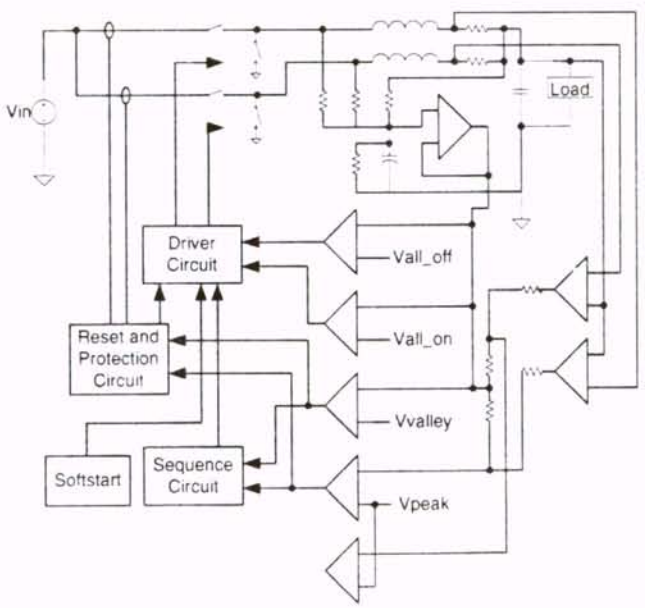
Figure 2-8 With current sharing, current difference is around 0.2A

The operation of the single phase hysteretic controller TPS5211 differs from a regular hysteretic controller. The additional ramp signal through the input of the hysteretic comparator is formed by R and C, as shown in Figure 2-9(a). The two signals are summed through the inputs of the comparator. The two signals are the ramp signal from R-C circuitry (the other module is the same) and the signal from the output converter. By proper selection of R and C, one can get the amplitude of an additional ramp signal which is greater than the output ripple of the converter. As a result, the switching frequency is greater while the output ripple becomes lower.

Figure 2-10 shows the two current waveforms and output voltage ripple. Without current sharing, the current difference is around 4A out of the total current 26A with a 57% ON resistance difference. Figure 2-11 shows there is 0.3A difference with current sharing with the general layout as show in Figure 9(b).



(a)



(b)

Figure 2-9 General Layout with TPS5211 Controller Method

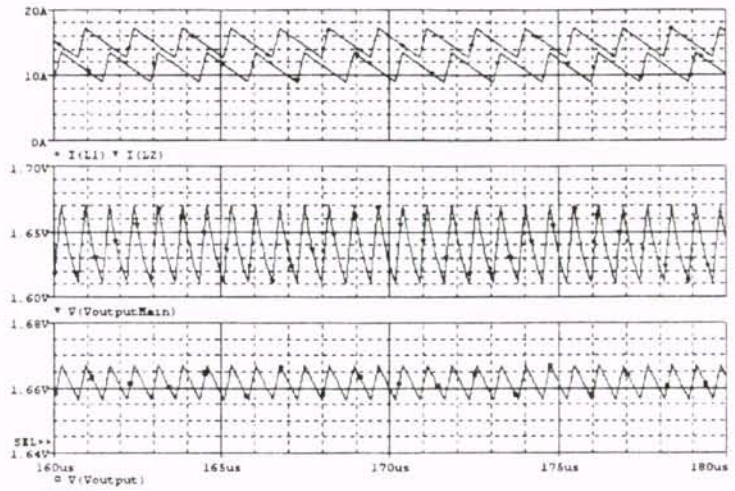


Figure 2-10 Without current sharing, current difference is around 4A (total current: 26A).

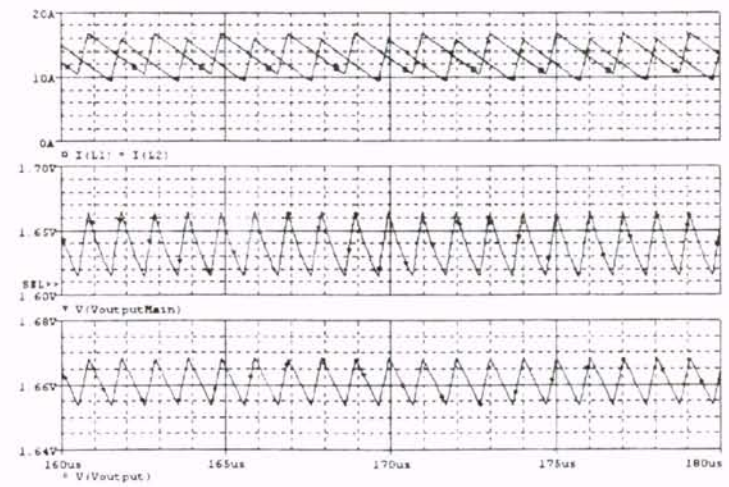
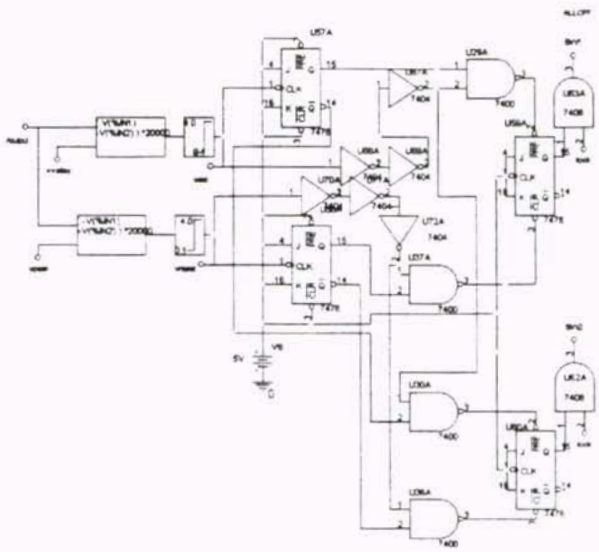
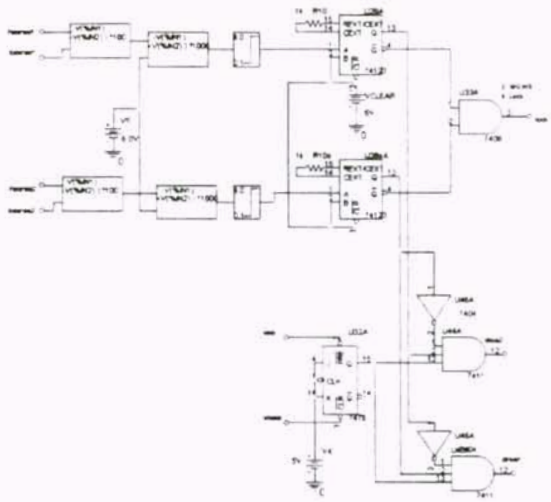


Figure 2-11 With current sharing, current difference is around 0.3A



(a)



(b)

Figure 2-12 Schematics, (a) sequence circuit, (b) reset and protection circuit

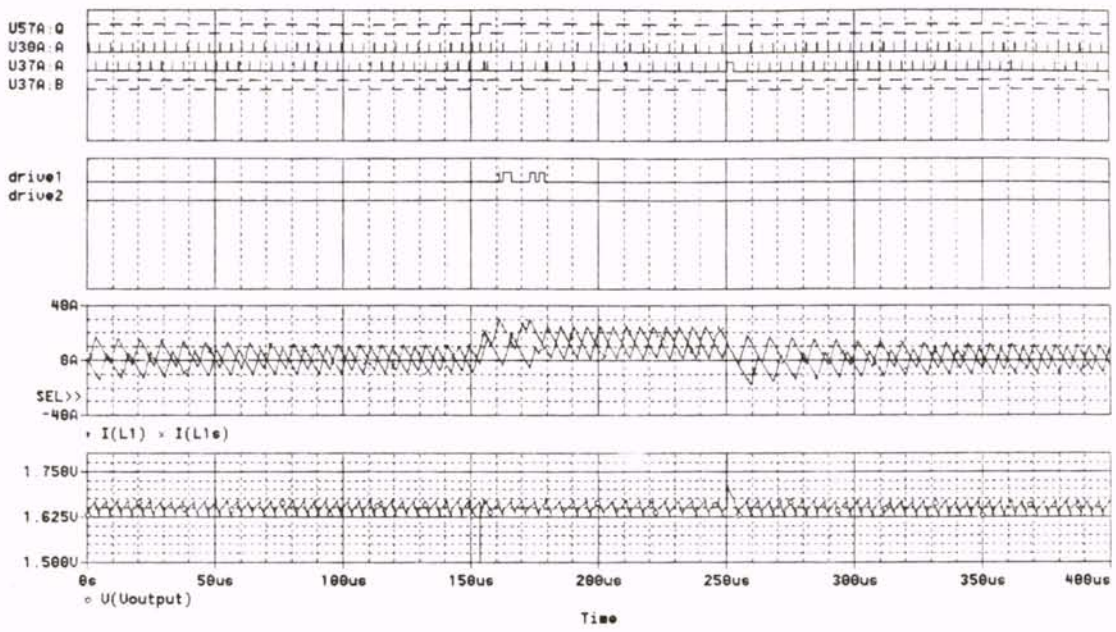


Figure 2-13 simulation result

A 5-12V input, 1.65V output 2-module interleaved converter with a maximum output current 26A is designed. Figure 2-12 shows the schematics. Simulation results are shown in Figure 2-13. Load transient from 10% load to full load and from full load to 10% load occurs at 152μs and 250μs, respectively.

During the load transient from 10% load to full load, one high-side switch remains on until the current flowing through the switch reaches the maximum value allowed. The reset circuit is triggered and this switch is turned off while the other high-side switch is turned on. Drive1 and Drive2 waveforms in Figure 2-13 are the reset signals leading to the changes of switches' status. The output signal denoted as U57A:Q is the output waveform of the upper JK trigger in Figure 2-13. The simulation and PCB

layout design example presented here is based on the software OrCAD Family 9.2. The main components used in the prototype testing are listed below:

MOSFET: SI4410DY ,

Output capacitor: OSCON 820uF (3×),

Output inductors: 16A, 0.5uH,

Magnetics 55121-A2, 4-turns, 17AWG wire,

Current sense resistor: MP916,

Comparator: Lt1721.

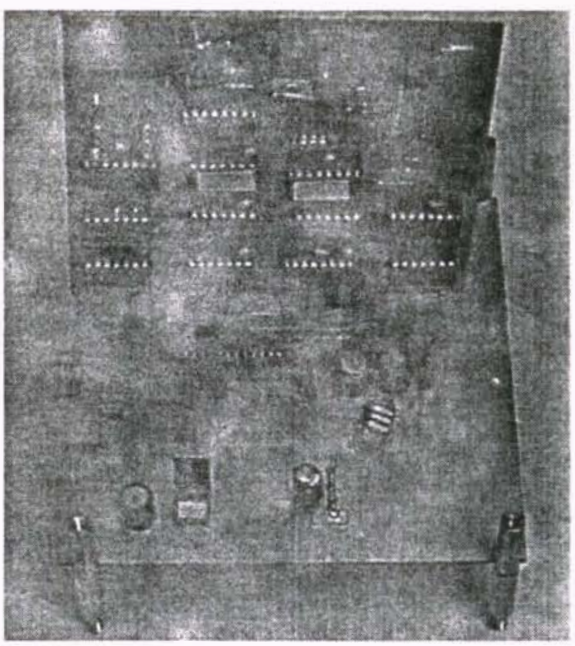
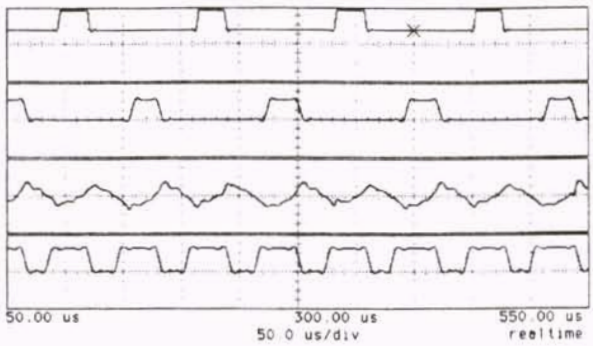
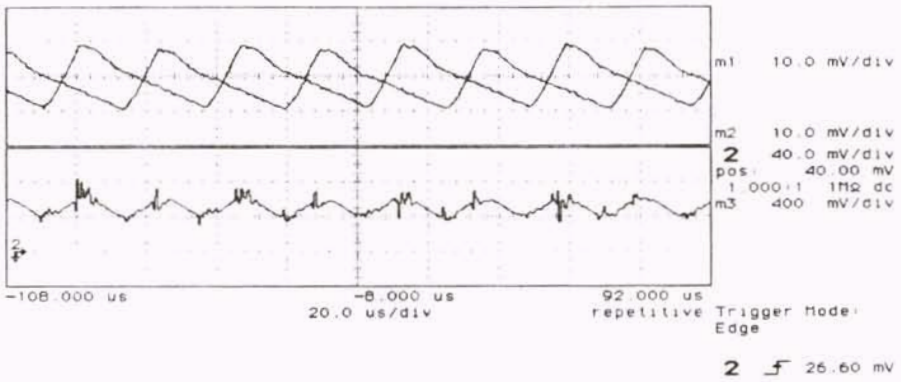


Figure 2-14: Prototype



(a)



(b)

Figure 2-15 Some preliminary results.

The upper two waveforms in Figure 2-15(a) are the experimental waveforms for the drive signals for high-side MOSFETs of the two power stages. The third waveform is the output ripple. We can see the some part of the ripple that is caused by the delay of the control circuit. The lower waveform is the one comparator output, which has a frequency twice the switching frequency of either of the power stages. Figure 2-15(b) shows the two interleaved output currents and total output ripple.

An interleaved buck converter with hysteresis voltage control for two power stages is presented. The method for interleaving can be easily applied to large number of VRM modules by modifying the sequence circuit. With the integration of the output inductors, and design of mixed-signal chips for the control and driver circuit, the efficiency and performance should be improved which make this interleaved synchronous buck regulator a potent competitor in the future.

CHPATER THREE

A NOVEL INTERLEAVED HALF-BRIDGE CONVERTER

3.1 HB Converter With Peak Current Control

Most of today's Voltage Regulation Modules (VRMs) draw power from a 5V output of a silver box, which in the future will be replaced by a distributed power system with high-voltage bus (12V or 48V) due to the point-of-use regulation as shown in Figure 3-1 [1].

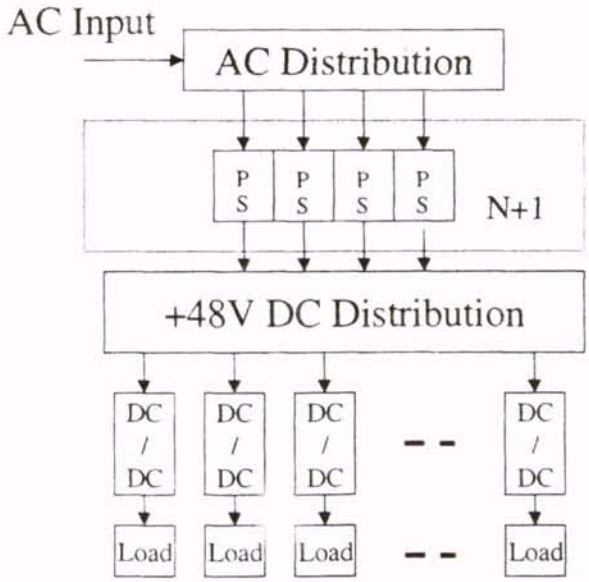


Figure 3-1: Distributed power system

Meanwhile, high-input-voltage and high-performance dc/dc converters will replace most of today's VRMs that use synchronous rectifier buck topology that needs large input capacitor and has asymmetrical transient response [2]. Moreover, the new VRMs converter design challenges are exasperated by the need for high-performance microprocessors that may require 40 to 80 watts for the CPU alone, with load current must be supplied with up to 30A/μs slew rate while keeping the output voltage within tight regulation and response time tolerances.

Conventional control techniques include PWM voltage control, PWM current control and variable frequency current control. When properly compensated, the small-signal dynamic performance of the buck regulator with conventional duty ratio control [3] may be nearly as good as that of the same regulator with current-mode duty cycle control. However, there is a dramatic difference when large-signal dynamic conditions are considered. When large dynamic load changes are made, the output voltage must change significantly, driving the error amplifier beyond its linear range. This temporarily opens the control loop and charges the compensation capacitors to voltages that are totally unrelated to normal operation. Hence, the compensation capacitors necessary for good small-signal performance will cause poor large-signal performance. In contrast, current-mode control achieves excellent small- and large- signal performance because large compensation capacitors are not required.

When peak current control is applied to half bridge topology, the unbalanced charge in each half cycle will cause a voltage to build up across any series capacitors. Unfortunately, the direction of the voltage buildup is such that it tends to reinforce the

original volt-second asymmetry, and a runaway situation quickly develops. Though there is a solution to this problem, using an auxiliary transformer winding made of small diameter wire with the same number of turns as the primary winding, and two small high voltage diodes, system performance could be affected due to the additional circuit. Thus, we propose a new control method to be known as master-slave peak current control that requires no correction circuit. Unlike existing converters where smaller output filter is used to achieve fast response at the expense of higher ripple, this interleaved half-bridge topology that naturally cancels the output current ripple without having to use large output filter.

3.2 Novel Interleaved Half-Bridge Converter with Peak Current Control

3.2.1 Operation Principle

The schematic of the proposed interleaved half-bridge converter with master-slave peak current control is shown in Figure 3-2.

The switching sequence for S_1, S_4, S_2 and S_3 with 90° degree phase shift is shown in Table 3-1. The switch ON and OFF times of S_1 and S_2 is determined by PWM controller like conventional half-bridge converter while S_3 and S_4 are controller by the ON or OFF signal of S_1 and S_2 with phase shift. The duty ratio of S_1 is shifted by 90° degree to control S_4 and the duty ratio of S_2 is shifted by 90° degree to control S_3. Thus, the interleaving is realized by phase shift of the control circuit.

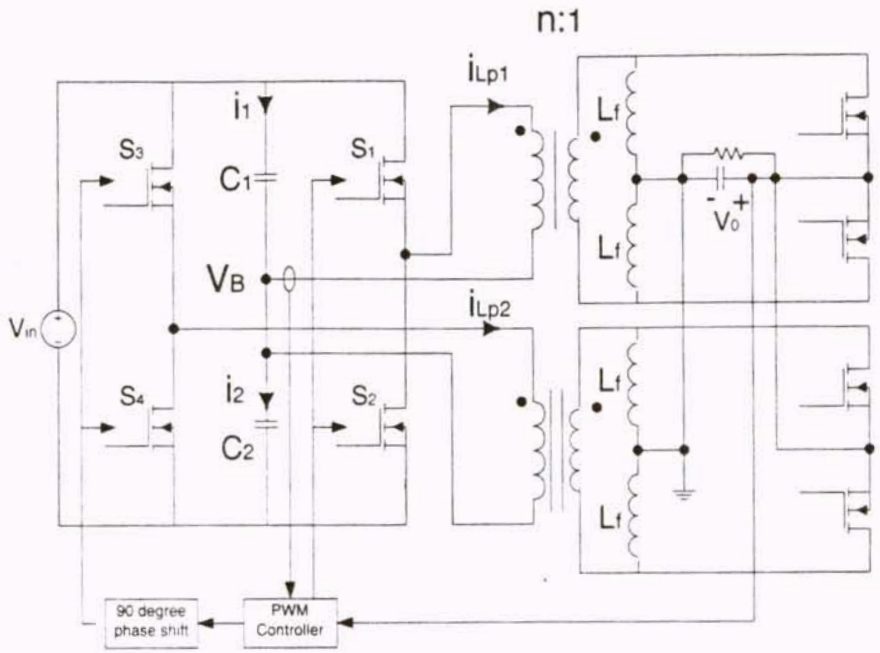


Figure 3-2 Proposed layout for the interleaved half-bridge Converter

Table 2-1: The switching sequence

Time	0°	90°	180°	270°
Switch	S_1	S_4	S_2	S_3
Duty Radio Decided by	PWM Controller	Duty Radio of S_1	PWM Controller	Duty Radio of S_3

3.2.2 Design Consideration

The control sequence also solves the problem of unbalanced charge due to peak current control. This can be explained by the equations given below. V_{in} is the input voltage, V_B is the voltage of the node connecting two bulk capacitors, i_1 and i_2 are the capacitor currents of C_1 and C_2, L_f is the output inductor, L_{lk} is the leakage inductor of the main transformer, T is the period of cycle and D is the duty ratio of switch S_1.

First, we assume that C_1 and C_2 are large and equal (C_1=C_2=C), hence: $V_B = \frac{V_{in}}{2}$. We also assume the bulk capacitors are charged linearly, and there is small perturbation causing $V_B = \frac{V_{in}}{2} - \Delta V_B$. When S_2 is on, the capacitor current, i_2, is given by,

$$i_2 = \frac{V_B - nV_0}{L_{lk} + n^2 L_f} DT = \frac{\frac{V_{in}}{2} - \Delta V_B - nV_0}{L_{lk} + n^2 L_f} DT \tag{3-1}$$

resulting in V_B being reduced by ΔV_{B2} that is expressed as

$$\Delta V_{B2} = \frac{1}{C} \int I_2 dt . \tag{3-2}$$

As switch S_3 is turned on after 90° delay of the turn-on of S_2, the current flowing through bulk capacitor C_1 is given by,

$$i_1 = \frac{V_{in} - nV_0 - (V_B - \Delta V_{B2})}{L_{lk} + n^2 L_f} DT \tag{3-3}$$

Approximately, the voltage increment of V_B is given by:

$$\Delta V_{B1} = \frac{1}{C}\int i_1 dt = \frac{1}{C}\int (i_2 + \frac{\Delta V_{B2} + \Delta V_B}{L_{lk} + n^2 L_f} DT)dt > \Delta V_{B2} \tag{3-4}$$

Hence, V_B is increased to offset ΔV_B, so V_B is kept constant around $\frac{V_{in}}{2}$.

In the other case when $V_B = \frac{V_{in}}{2} + \Delta V_B$, similarly we can get V_B is brought down to $\frac{V_{in}}{2}$ in each cycle. Thus charge balance is achieved as V_B is kept almost constant.

3.2.3 Simulation and Experimental Results

Figure 3-3 is the phase shift circuit that shifts the PWM control signal for S_1 and S_2 one-quarter period of cycle to control the switch S_3 and S_4, respectively. The controller design files are in Appendix [4,5,6,7,8,9,10,11,12].

The upper waveform in Figure 3-4 is the currents of output inductors. The middle waveform is the current of the primary winding of the main transformer i_{Lp1} and i_{Lp2}. The lower waveform is output voltage V_0 during load change. From the simulation result we can see even with modest output capacitance (3280uF), the voltage drop is small and back to normal value within 60μs which can not be achieved with voltage mode control.

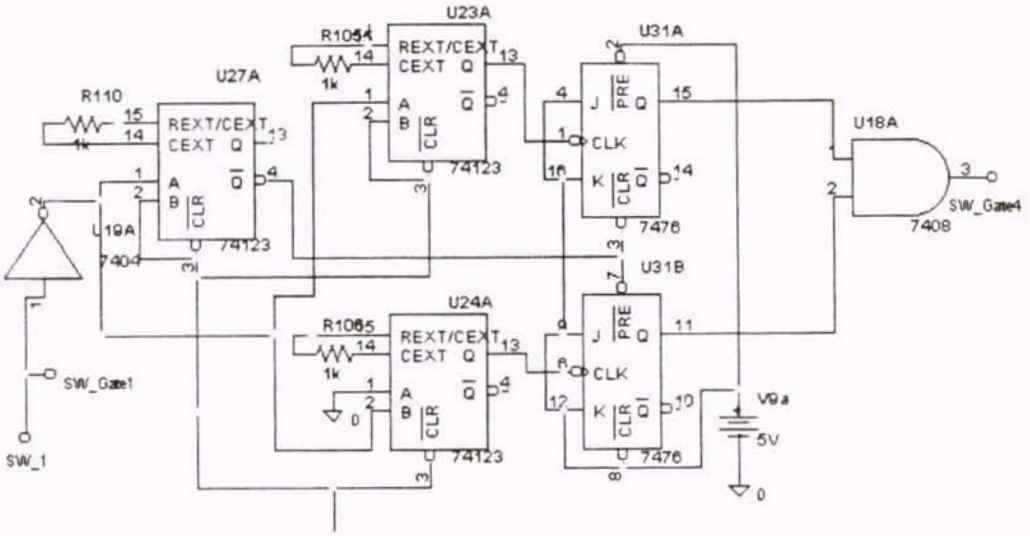


Figure 3-3 Schematic of phase shift circuit

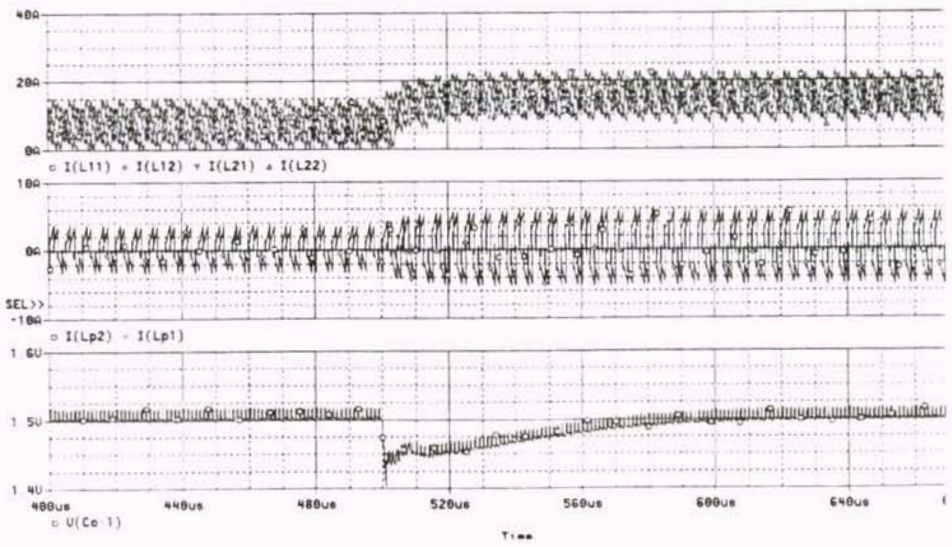


Figure 3-4 Simulation Results

The simulation and PCB layout design software is OrCAD Family 9.2. The main components used in the prototype in Figure 3-5 are listed below:

MOSFET: HUF75639P,

Inductor: 55121-A2, 4 turns,

Output Capacitor: OSCON,

Drive: HIP4081A,

Current transformer: Coilcraft CS4050V-01,

PWM controller: UC3825.

Figures 3-6 and 3-7 show the gate signals of the four main MOSFETs in the power stage at light and heavy load, respectively. In one cycle the gate signals are shifted 90 degrees from each other. It's noted the duty ratio is different between two cases as the output inductors are in the discontinuous conduction mode. Figure 3-8 is the voltage waveforms of the four rectifier diodes. In the DCM, after the output inductor current drops to zero, the diode is off again, unlike in the CCM, the diodes are turned off once in each cycle. Figure 3-9 is the sensed current of primary winding and the external ramp signal used for the peak current control.

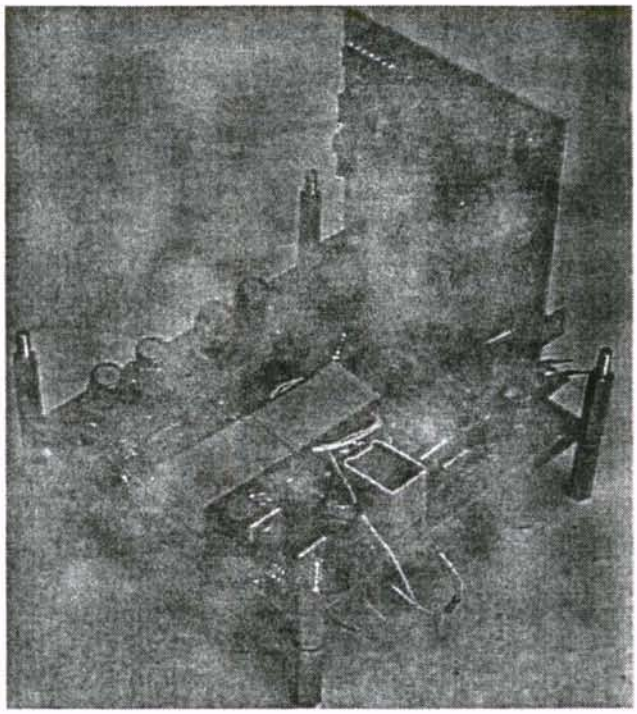


Figure 3-5 Half-bridge Prototype

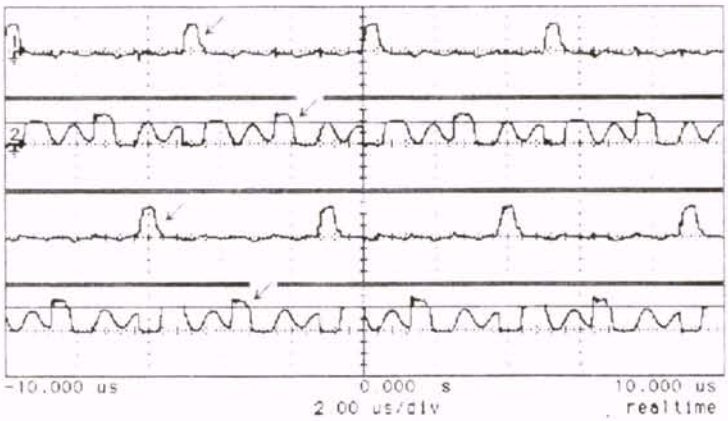


Figure 3-6 MOSFETS' gate signals at light load

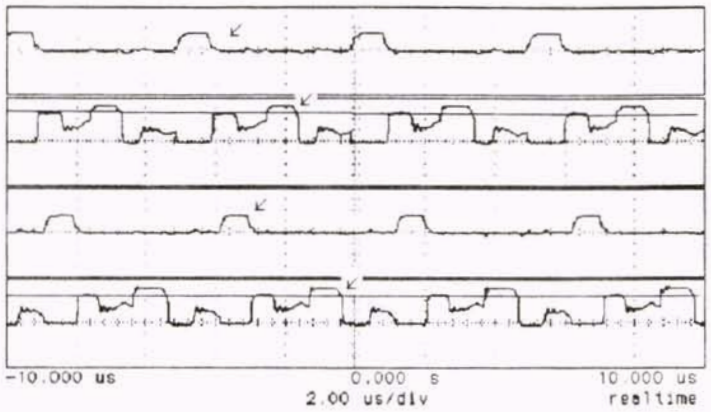


Figure 3-7 MOSFETS' gate signals at heavy load

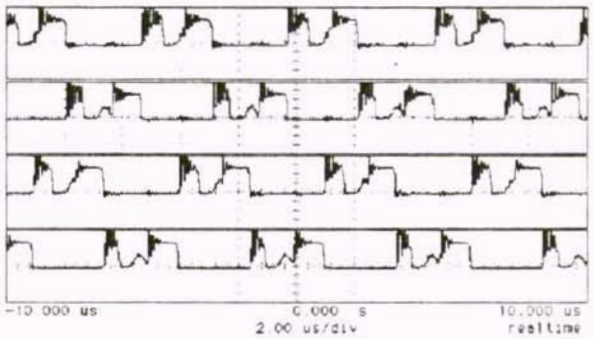


Figure 3-8 Voltage across the output diodes

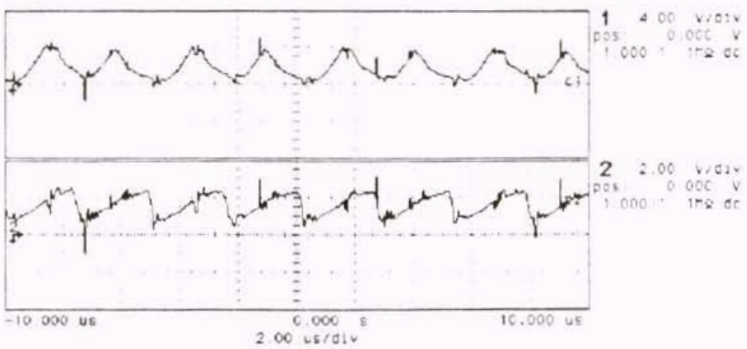


Figure 3-9 Sensed current and external ramp signal

3.3 Summary

Using a new method of master-slave peak current control, charge balance is automatically achieved and current runaway is avoided without additional correction circuitry, resulting in increased efficiency. We present two interleaved half-bridge power stage that naturally cancels the output current ripple while achieving fast response. With the integration of the output inductors and design mixed-signal chips for the control and driver circuit, the efficiency and performance are readily improved.

CHAPTER FOUR

LOW VOLTAGE DC/DC CONVERTERS

4.1 A High-Power Low-Voltage PWM FB-ZVS Converter

Compared with the other bridge topologies introduced before, a full-bridge isolated converter is presented here as shown in Figure 4-1. It has low current stress of the push-pull topology, low voltage stress of the half-bridge topology and high transformer turn ratio which means smaller primary side current [1]. At high frequencies the soft-switching of the primary switches is required to maintain high efficiency.

In some application in the future, when the output voltage could be as low as 0.5V, the output current could be as high as 200A. The FB-ZVS becomes a very suitable topology for this application.

4.1.1 Operation Principle

The operation of this converter can be divided into 4 modes in figure 4-2 [2].

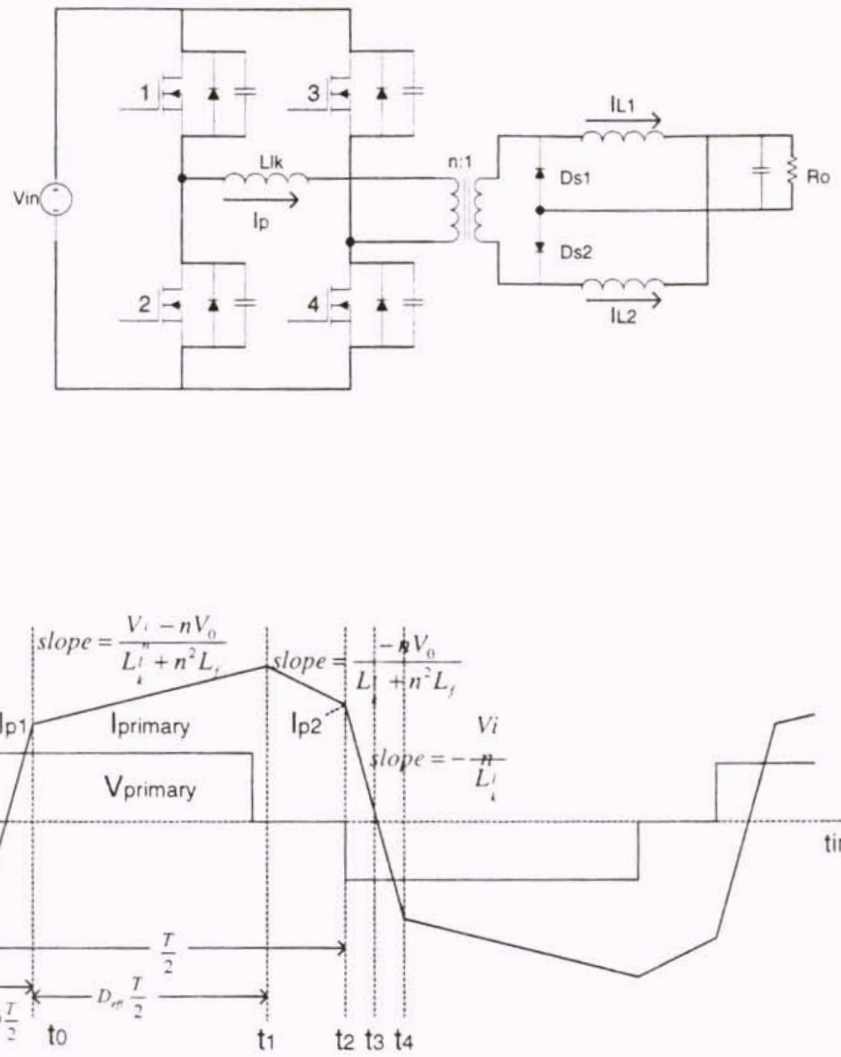
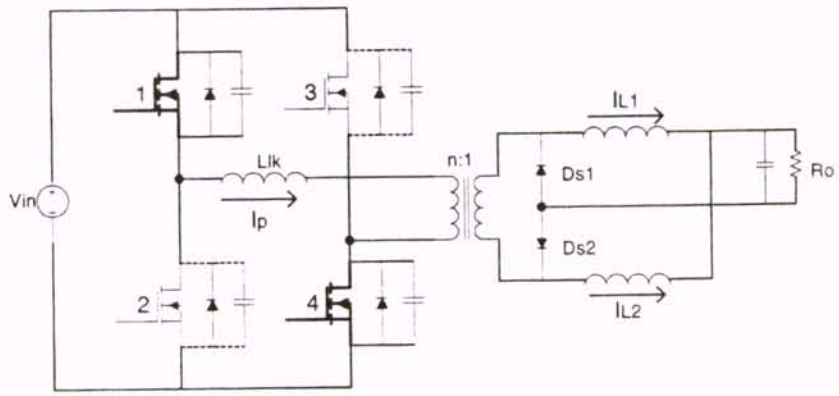
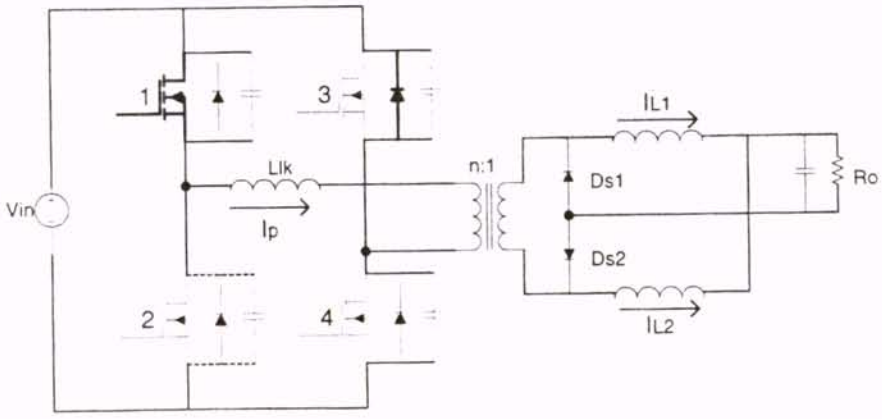


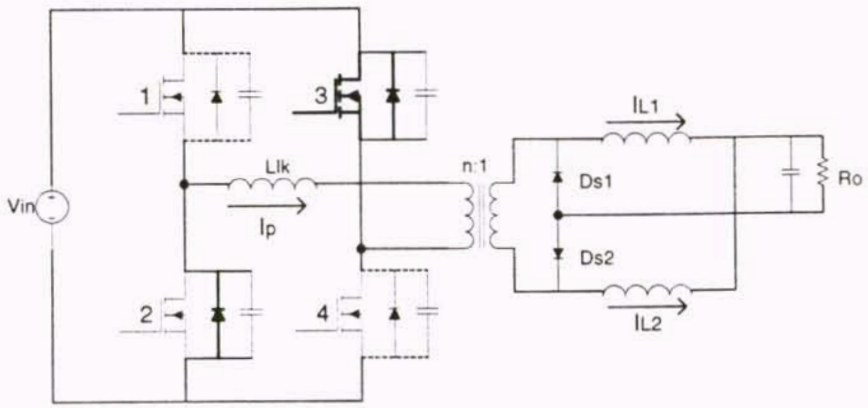
Figure 4-1 FB-ZVS-PWM converter and primary waveforms



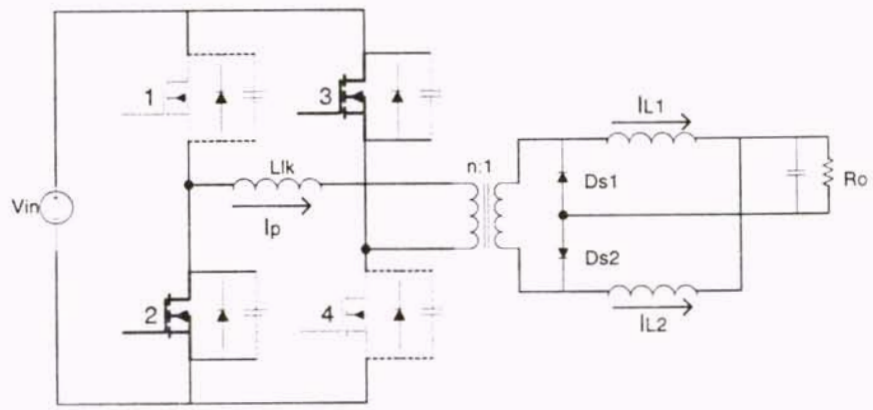
MODE I



MODE II



MODE III



MODE IV

Figure 4-2 Operation modes of FB-ZVS-PWM converter

Mode 1: With Q1 and Q4 initially conducting, the primary voltage is $V_p = V_{in}$. The current I_{L1} will ramp up linearly while I_{L1} will ramp down linearly. L_f is the filter inductor.

$$i_p = \frac{V_{in} - nV_0}{L_{lk} + n^2 L_f}(t - t_0) + i_p(t_0) \tag{4-1}$$

Mode 2: When Q4 is turned off at t_1, the energy stored in the output filter inductor L1 charges the junction capacitor of Q4 and discharges the junction capacitor of Q3 causing the anti-parallel diode of Q3 to conduct. Once it conducts, Q3 can be turned on under ZVS.

$$i_p = \frac{-nV_0}{L_{lk} + n^2 L_f}(t - t_1) + i_p(t_1) \tag{4-2}$$

Since the energy available for achieving ZVS for the leading leg is the output filter energy, ZVS is possible over a wide load range.

Mode 3: When Q1 is turned off at t_2, the energy stored in the leakage and magnetizing inductance charges the junction capacitor of Q1 and discharges the junction capacitor of Q2 causing the anti-parallel diode of Q2 to conductor. At this point, Q2 can be turned on under ZVS.

$$i_p = -\frac{Vin}{L_{lk}}(t - t_2) + i_p(t_2) \tag{4-3}$$

Since the energy stored in the leakage and magnetizing inductance is less than output filter energy, the soft switching range is limited. Increasing the leakage inductance

extends the soft switching range of the converter but adversely affects the effective duty cycle.

Mode 4: The cycle is completed when the primary current I_p reaches the reflected secondary filter current.

The required dead time for Q2 and Q4 depends on the load. The energy in L_{lk} has to be:

$$E = \frac{1}{2} L_{lk} I_{p2}^2 > C_{oss} V_{in}^2 + \frac{1}{2} C_{TR} V_{in}^2 \tag{4-4}$$

where I_{p2} is the current through the primary at time t_2, C_{oss} is the output capacitance of the MOSFET and C_{TR} is the transformer winding capacitance.

$$\delta\tau_{\max} = \frac{T}{4} = \frac{\pi}{2}\sqrt{L_{lk} C} \tag{4-5}$$

where $C = C_{oss} + C_{TR}$. Figure 4-3 presents details of the voltage across Q4 at turn-off (time t_2) for three different values of load current.

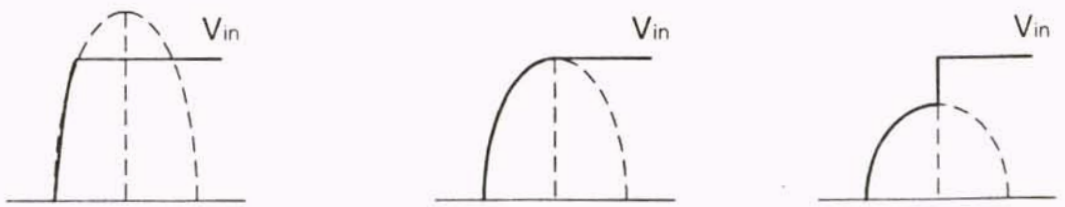


Figure 4-3 Q4 voltage at different load current

For Q1 and Q3:

The value of the dead time, $\delta\tau_1$, can be determined from the equation

$$C_{oss}V_{in} + C_{TR}V_{in} = I_p\delta\tau_1 \tag{4-6}$$

The critical current required in the primary to achieve ZVS can be calculated from

$$I_{crit} = \sqrt{\frac{2}{L_{lk}}(C_{oss}V_{in}^2 + \frac{1}{2}C_{TR}V_{in}^2)} \tag{4-7}$$

The available current through L_{lk} at time t_2 can be calculated as

$$I_{p2} = \frac{1}{n}(I_{load} + \frac{\Delta I}{2} - \frac{V_{out}}{L_f}(1-D)\frac{T}{2}) \tag{4-8}$$

Finally, ZVS is achieved for values of load current such that

$$I_{p2} > I_{crit} \tag{4-9}$$

The voltage gain of the ZVS-PWM converter can be expressed as:

$$\frac{V_{out}}{V_{in}} = \frac{1}{n}D_{eff} \tag{4-10}$$

where $D_{eff} = D - \Delta D$, and ΔD is the loss of duty cycle due to the finite slope of the rising and falling edges of the primary current. Looking at Fig. 14, ΔD can be expressed as:

$$\Delta D = \frac{I_1 + I_2}{\frac{V_{in}}{L_{lk}}\frac{T}{2}} = \frac{1}{n\frac{V_{in}}{L_{lk}}\frac{T}{2}}(2I_{load} - \frac{V_{out}}{L_f}(1-D)\frac{T}{2}) \tag{4-11}$$

Then

$$D = \frac{1 + \frac{4L_{lk} f_s}{n^2 R_{load}} - \frac{L_{lk}}{n^2 L_f}}{\frac{1}{D_{eff}} - \frac{L_{lk}}{n^2 L_f}} \tag{4-12}$$

For a maximum duty cycle of the converter: $1 \geq D_{\max} \geq D$

4.1.2 Controller Design Consideration

Four different control methods: voltage control, voltage control with a hysteretic outer loop, peak current control and average current control. The controller design files are in Appendix. The voltage control compensator is a two-pole, two zero structure.

4.1.3 Simulation Results

Figures 4-4, 4-6 and 4-7 show the simulation results of a phase-shift full-bridge converter. During the same load transient, the output voltage drop of the same converter with voltage control is 1.2V, the one with voltage control plus a hysteretic outer loop is 1V and the converter with average current control is 0.75V. Therefore, average current control method has the fastest transient compared to other two methods, and should be recommended for low voltage application. Figure 4-5 shows the control circuit used in the hysteretic outer loop.

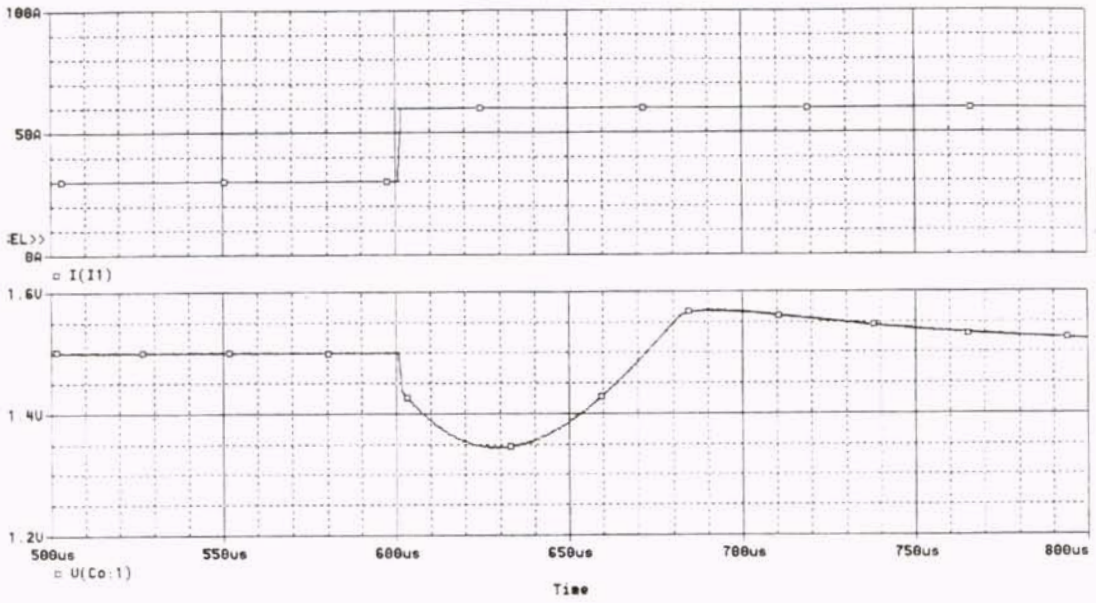


Figure 4-4 Voltage control simulation result

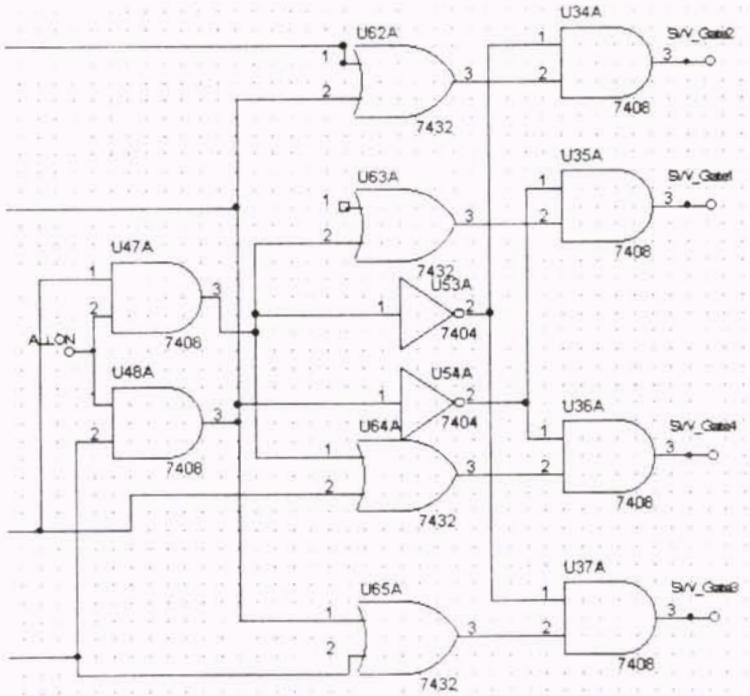


Figure 4-5 Part of the schematic for hysteretic control outer loop

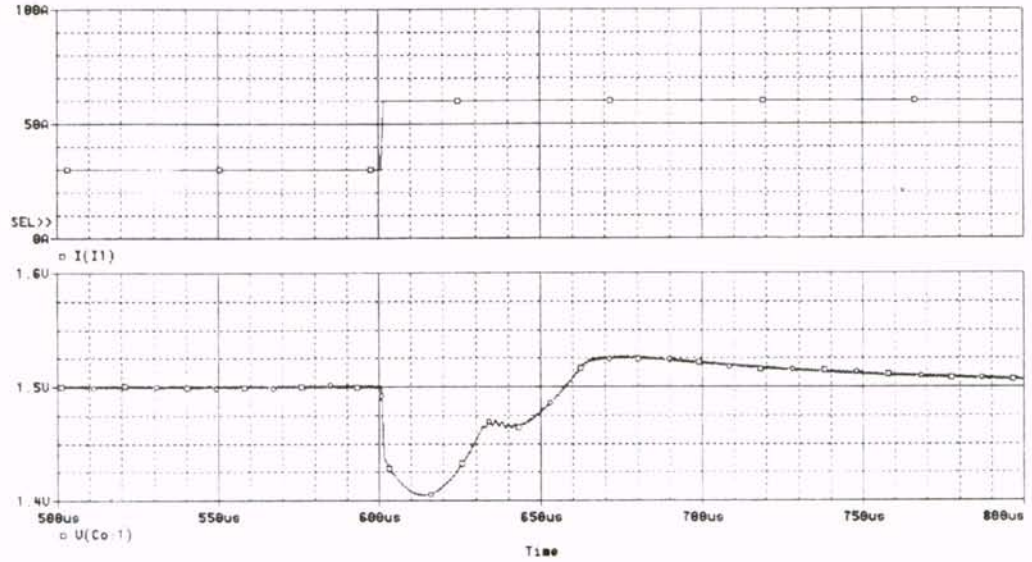


Figure 4-6 Voltage control with a hysteretic outer loop simulation result

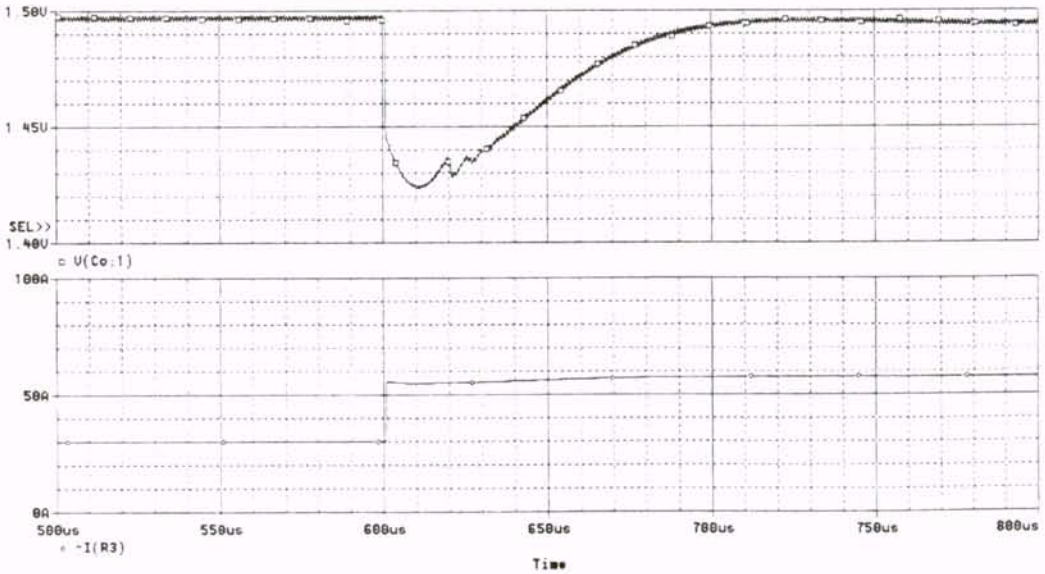


Figure 4-7 Average current control simulation result

4.2 A Low-voltage Dual Output DC/DC Converter

4.2.1 Multiple Output Converters

Designing multi-output converters presents a remarkable challenge for the power supply designer. There is no comparable power supply design task where specification, topology selection and the choice of output voltage regulation technique would have a more profound effect on the performance, cost and complexity of the final circuitry [3].

Multi-output circuits provide isolation and several output voltages using one high frequency isolation transformer as opposed to individual power modules for each output as it is frequently done in distributed power systems. The decreased system complexity of the multi-output approach is realized primarily at the expense of output voltage regulation accuracy. Several approaches have been explored for multi-output converters to address complexity, overall efficiency, output voltage and cross-regulation issues. These circuit solutions can be divided into three different groups.

The first group of multi-output converters regulate their main output, from which the feedback signal is generated, with very good accuracy. Their auxiliary outputs are regulated with lesser accuracy since they are not part of a closed loop regulation scheme. These solutions tend to be the most economical ones but their application can be limited because of their inadequate output voltage accuracy. The best known topologies of this category are the flyback and forward converters.

The second circuit family provides a remedy for those applications where tight voltage regulation of each output is necessary. These approaches can be based on almost

any topology since they are utilizing some sort of post regulation technique to regulate the auxiliary outputs of a multiple output converter. Accordingly, these solutions are differentiated by the post-regulation technique they are employing. Post regulation of the auxiliary outputs can be achieved by linear post-regulators, individual DC/DC converters, magamp circuits or switch mode Secondary Side Post Regulators(SSPR). All of these techniques are based on closed loop output voltage regulation of their respective outputs.

The third circuit family as introduced here is that all the outputs are regarded equal in terms of control priority. Each output has a chance to be the main output depending on the load conditions while all the outputs operate separately without affecting one another. The number of PWM controller used in this family is the same as that of the secondary family where post-regulation is used.

4.2.2 Family I: solutions without post regulator

Generally, any isolated topology with several secondary windings in the transformer can provide multiple output voltages. These circuits employ a single primary side power stage including the input filter, energy storage capacitor, a high frequency power switch, usually a MOSFET transistor and a PWM controller. On the secondary side, isolated by the transformer, are the output components, rectifiers, energy storage capacitors and output inductors where it is applicable. Among those outputs, one is distinguished as the main output whose output voltage is regulated by a feedback loop. The fundamental element of the feedback loop is the voltage error amplifier. Its output provides the feedback signal that is transmitted to the primary side over the isolation

barrier. On the primary side, the feedback signal is received by the PWM controller and ultimately determines the duty-cycle of the power switch. It is important to emphasize, that in all of these cases, there is only one controlled quantity, the duty-cycle of the MOSFET, which allows control of only one output parameter, which is the output voltage of the main output. Thus, the output voltage of the main output is accurately regulated.

On the other hand, the auxiliary outputs are not directly regulated by the PWM modulator. The nominal auxiliary output voltages are determined by the turns ratio of the output windings. Their voltage regulation accuracy is a function of the coupling among the secondary windings, the voltage drop difference among the rectifier diodes and the voltage drop on the parasitic resistance of the series components of those outputs. These parasitic resistive components, secondary winding resistance, rectifier diode equivalent series resistance, the resistance of the output inductor and the wiring of trace resistance represent a load dependent voltage drop between the secondary winding and the actual output of the power supply. As the load current changes, the auxiliary output voltages will vary accordingly, causing the well know cross regulation error.

Figures 4-8 shows the flyback converter with multiple output windings.

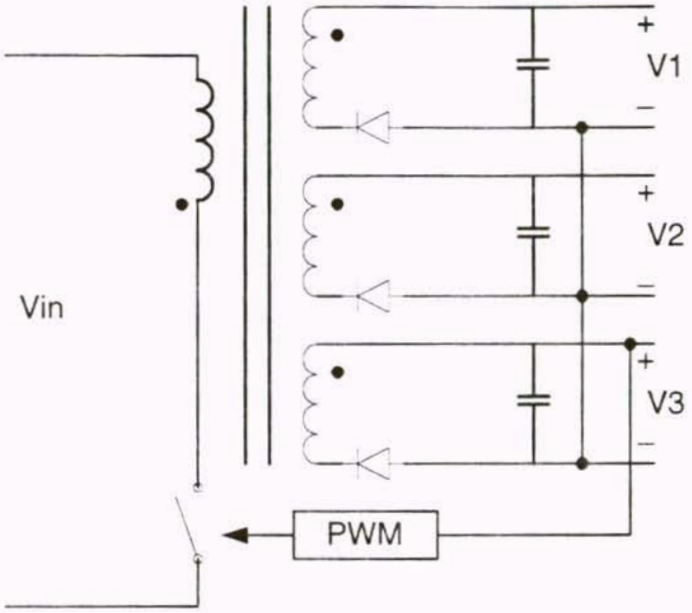


Figure 4-8 Multi-output Flyback Converter

4.2.3 Family II: solution with post regulation

In many applications, especially at lower output voltages, adequate output voltage tolerances can not be achieved without some sort of post regulation of the auxiliary outputs. These power supplies might employ any topology with multiple output windings. The main output is still regulated by direct feedback and pulse width modulation of the primary switch in the isolating power stage. Once post regulation is considered, tight cross regulation among the outputs is not critical.

The four most popular post regulation techniques are linear post regulator, dc/dc switching post regulator, magamp post regulator, and secondary side post regulator.

Linear post-regulators are extensively used for low current outputs. Since linear regulators require a minimum voltage drop across the pass element, their application is usually restricted by power dissipation at higher output currents. This voltage drop together with the load current represent a relatively large variable power loss. The technique still has the advantages of simple, cost effective and highly integrated at low currents. Voltage regulation is independent from the main converter's duty-ratio and output noise is very low.

Another technique employs two cascaded switch mode power converters. Since the second dc/dc converter that acts as the post regulator works from a semi-regulated input voltage, its operating conditions and efficiency can be easily optimized.

Magamp post regulator is very popular in medium to high power application. The saturable reactor in the magamp post regulator functions as a magnetic switch. Before the core of the magamp inductor saturates, it represents a large impedance in series to the secondary winding of the isolation transformer preventing power transfer to that output. By properly positioning the operating point of the magnetic core on the B-H curve, a variable portion of the secondary pulse can be blocked. Thus the effective duty-ratio for the buck inductor can be further modulated, allowing precise regulation of the auxiliary output voltage. The disadvantages are large number of inductive components and auxiliary output duty-cycle is limited by the main output duty-ratio.

Figure 4-9 shows a secondary side post regulator circuit diagram. Output V2 is controlled by main PWM while the auxiliary output V1 is controlled by a buck controller. The are compatible with higher switching frequencies, allow easy operation at light load and in short circuit conditions. The most significant shortcoming is that auxiliary output duty-cycle is limited by the main output duty-ratio.

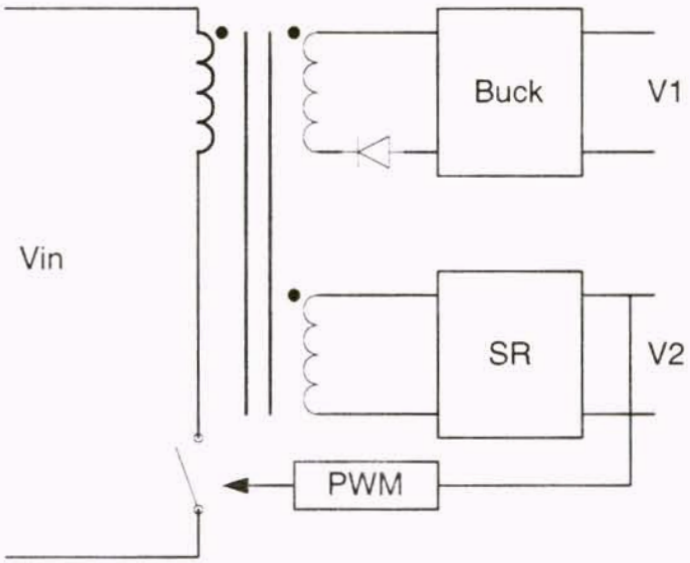


Figure 4-9 Secondary side post regulator

4.2.4 Family III: equally controlled outputs

In the telecommunication area, dual output or multiple DC/DC converters have a wide application. The outputs need to be regulated separately to meet the stringent requirements for all of them. The traditional approach is to use one PWM controller for main output by regulating the duty ratio of the main switch, while using other PWMs for

the rest of the outputs. The success of the method is based on the main output having the largest duty ratio. Thus a dummy load is required for the main output to guarantee its continuous conduction mode operation, otherwise the duty ratio could be reduced to accommodate the discontinuous conduction mode.

A new dual or multiple output DC/DC converter is proposed. In this converter, each output is controlled separately while the control signal for the main switch is from the output with the largest duty ratio. Figure 4-10 shows the general layout of the new converter. This method not only provides an alternative way for this application, but also simplifies the traditional approaches by getting rid of the dummy load.

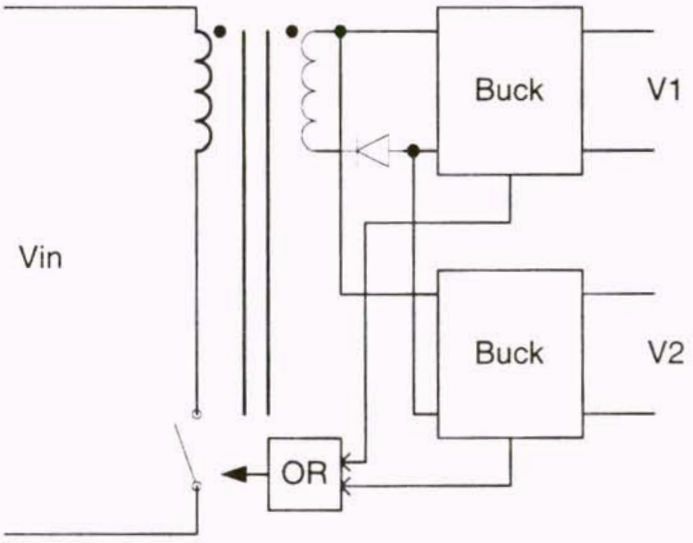
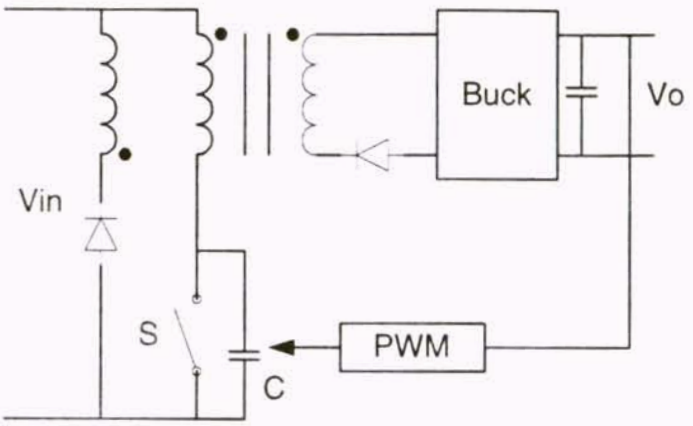


Figure 4-10 General layout of the new dual output converter

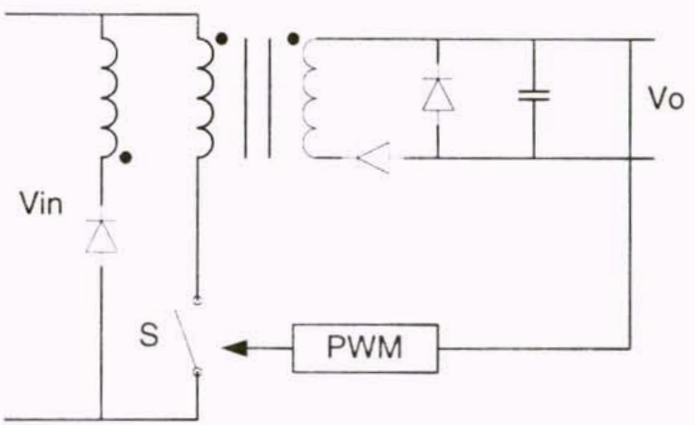
4.2.5 Operating analysis

The operation of the new converter as shown in Figure 4-10(a) is basically the same as a forward converter in Figure 4-10(b). For a forward converter, with a drive signal as show in Figure 4-11(a), the drain voltage of the switch S is shown in Figure 4-11(b). When the switch is turned off, the drain voltage is resonated to a high value and then returns to Vin as the voltage on the primary winding of the transformer is zero. Resonance ends when the drain voltage of S becomes Vin.

For the new converter, resonance continues when the drain voltage hits Vin because unlike the forward converter, whose resonant energy could be transferred to the secondary, this converter's resonant energy stays on the primary side. As such, the drain voltage of S could reach zero and go up again as show in Figure 4-12(b). So if an additional capacitor C is added in the circuit as shown in Figure 4-11(a), the drain voltage of S could be zero when the next drive signal comes, achieving zero voltage switching for the main switch S as shown in Figure 4-12(c). Moreover, the additional capacitor is working as a snubber during turning off. The upper traces in Figure 4-12(b) and (c) are feedback error voltage and PWM ramp voltage which decide the duty ratio.



(a)

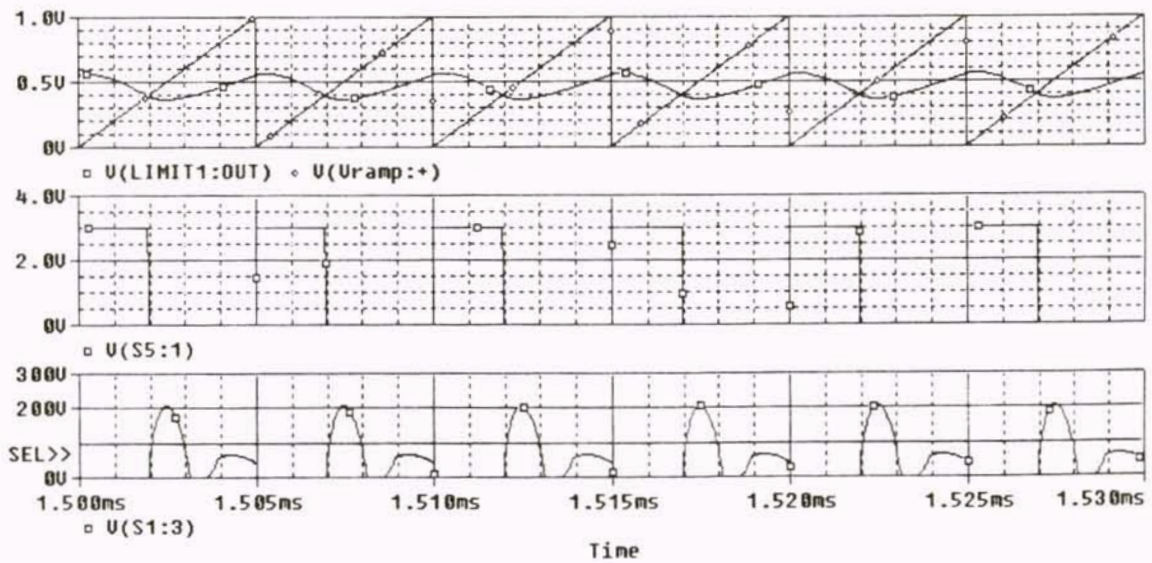


(b)

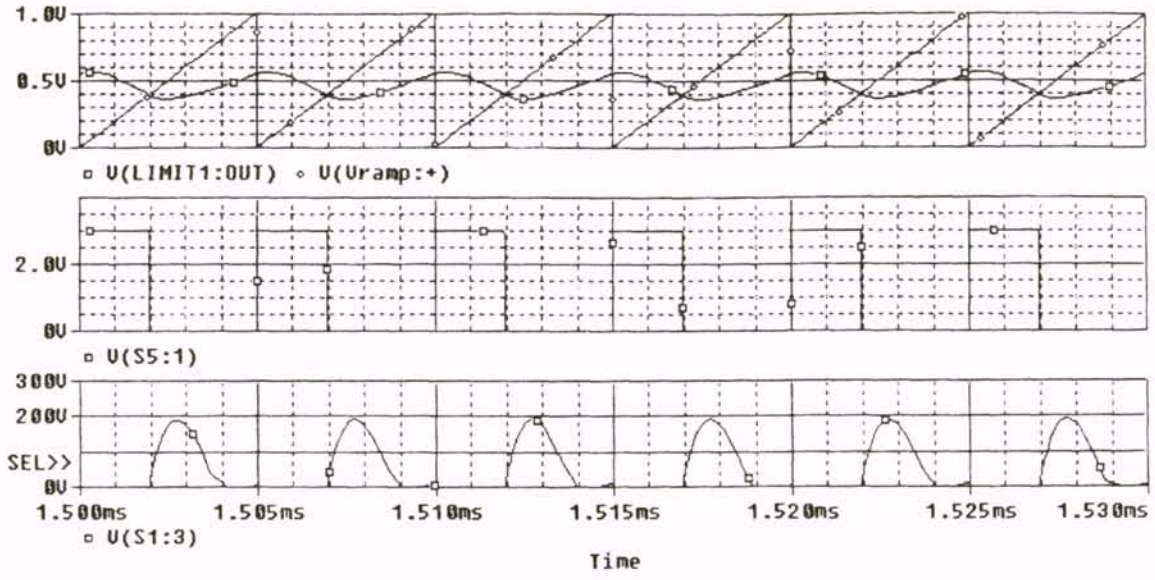
Figure 4-11 General layout of the new converter and a forward converter

4.0V
2.0V
0V
V(S1:1)
200V
0V
SEL>>
-200V
1.500ms
1.505ms
1.510ms
1.515ms
1.520ms
1.525ms
1.530ms
V(S1:3)
Time

(a)


1.0V
0.5V
0V
V(LIMIT1:OUT)
V(Vramp:+)
4.0V
2.0V
0V
V(S5:1)
300V
200V
SEL>>
0V
1.500ms
1.505ms
1.510ms
1.515ms
1.520ms
1.525ms
1.530ms
V(S1:3)
Time

(b)



(c)

Figure 4-12 Some simulation results for the new converter

4.3 Summary

As the power consumption of high-performance microprocessors increases, the advantage of phase shift full-bridge converter for this application becomes apparent. Due to soft-switching, the high density could be reached which is so important where the real estate for dc/dc converter is precious.

A new dual or multiple output converter is proposed. With this method, the converter is simplified and redundancy is improved as the main switch could be controlled by any of the output.

CHAPTER FIVE

A NOVEL SOFT-SWITCHING SINGLE STAGE CONVERTER

5.1 Introduction

As the use of power supplies continues to increase, more distorted mains current is drawn from the line, resulting in lower power factor and high total harmonic distortion. Power factor correction (PFC) is becoming more and more common in single-phase off-line switching-mode power supplies, not only because low power factor limits the maximum available power drawn from mains, but also agency regulation requires that the harmonic current of the line current of mains-connected equipment remains below certain limits. For years a great deal of effort has been made to develop efficient and cost-effective power factor correction schemes. As a branch of active PFC techniques, the single-stage technique receives particular attention because of its low cost implementation [1].

The classical definition of power factor is applicable only to pure sinusoidal waveforms is given below:

$$PF_{disp} = \cos\phi = \frac{P}{V_{rms(\sin e)} I_{rms(\sin e)}} \tag{5-1}$$

where P is the average power (averaged over a period), $V_{rms(sine)}$ is the rms voltage ($=V_p/\sqrt{2}$), $I_{rms(sine)}$ is the rms current ($I_p/\sqrt{2}$), and ϕ is the phase angle between voltage and current.

The cause of less than unity power factor is a phase shift between the fundamental component of the current and the voltage and/or the presence of higher harmonics in the voltage and/or the current. Accordingly, the power factor can be written as

$$PF = PF_{disp} PF_{dist} \tag{5-2}$$

where PF_{dist} is the distortion factor.

In the practically important case where the voltage is a pure sine wave, the distortion factor has the following relationship with the total harmonic distortion (THD):

$$PF_{dist} = \frac{1}{(1 + THD^2)^{1/2}} \tag{5-3}$$

In switching-mode power supplies the distortion factor usually dominates, and determines the overall power factor.

The lower power factor and the related high line-current distortion of the front end rectifiers of switching-mode power supplies have several undesirable effects.

(a) The maximum obtainable rectifier power from a wall outlet is reduced to rated power times the power factor.

(b) The harmonic currents cause excess wiring and power transformer losses in the utility network.

(c) The voltage waveform is flattened due to the high peak currents. This can cause malfunction of other equipment connected to the same branch.

(d) The harmonics can excite resonance in the power system that might lead to excessive peak voltages and rms currents, damaging the power-factor-correcting capacitors and causing insulator flash-overs.

(f) The excessive low-frequency conducted EMI can interfere with other equipment.

Moreover, with the residential industry and defense industry continuously demanding for even higher power density, switching mode power supply operating at high-frequency is required because at high switching frequency, the size and weight of circuit components can be remarkably reduced. But with the increasing of switch frequency, the switching loss becomes intolerable, resulting in very low conversion efficiency. Furthermore, the presence of leakage inductance in the high-frequency transformer and junction capacitance in the semiconductor devices causes the power devices to turn-off and turn-on with more energy loss and noise. Because of this reason, the switching frequency of the traditional SMPS (Switching Mode Power Supplies) is limited to 100kHz. To boost the switching frequency, the soft-switching technique, was introduced to alleviate the switching losses.

5.2 Power Factor Correction

Research in improving system power factor has resulted in countless circuit topologies and control strategies. They can be mainly categorized into discontinuous

conduction mode (DCM) shaping technique and continuous conduction mode (CCM) shaping technique. The recent research interest in DCM shaping technique is focused on developing PFC circuit topologies with a single power switch, result in single-stage single-switch converter (so-called S^4-converter). The CCM shaping technique emphasizes on the control strategy to achieve unity power factor. The hot topics in this line of research are concentrated on reducing the complexity of the control circuit and enhancing dynamic response of the system, resulting in some new control methods. Figure 5-1 shows a classification of these conducted schemes based on conduction-mode and system configuration types.

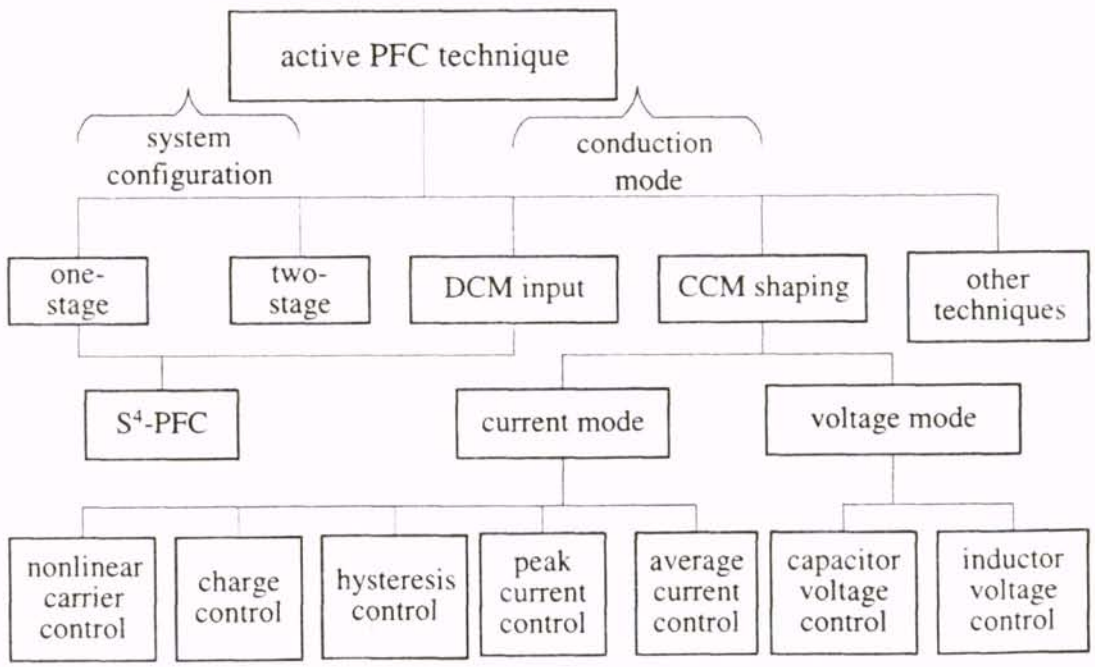


Figure 5-1: Classification of PFC conducted schemes

Like other power electronic apparatus, the core of a PFC unit is its converter, which can operate either in DCM or in CCM. The benefit from DCM technique is that low cost power supply can be achieved because of its simplified control circuit. However, the peak input current of DCM converter is at least twice as high as its corresponding average input current, which causes high current stresses on switches, resulting in intolerable conduction and switching losses as well as transformer copper losses. In practice, DCM technique is only suitable for low to medium level power application, whereas, CCM is used in high power cases. However, a converter operating in CCM does not have PFC ability inherently, i.e. unless a certain control strategy is applied, the input current will not follow the waveform of line voltage. This is why most of the research activities in improving power factor under CCM condition have been focused on developing new current shaping control strategies. Depending on the system variable being controlled (either current or voltage) PFC control techniques may be classified as current control and voltage control. Current control is the most common control strategy since the primary objective of PFC is to force the input current to trace the shape of line voltage.

5.2.1 CCM Shaping Technique

To achieve both PFC and output voltage regulation by using a converter operating in CCM, multi-loop controls are generally used. Figure 5-2 shows the block diagram of AC/DC PFC converter with CCM shaping technique. Where, H_f is a line voltage

compensator, H_x is a controlled variable compensator, and $x(t)$ is the control variable that can be either current or voltage.

Normally, in order to obtain a sinusoidal line current and a constant DC output voltage, line voltage $v_{line}(t)$, output voltage V_o and a controlled variable $x(t)$ need to be sensed. Depending on whether the controlled variable $x(t)$ is a current (usually the line current or the switch current) or a voltage (related to the line current), the control technique is called "current mode control" or "voltage mode control" respectively. In Figure 5-2, two control loops have been applied; the feedforward loop and the feedback loops. The feedforward loop, also called "inner loop" keeps the line current to follow the line voltage in shape and phase, while the feedback loop also called "outer loop" keeps the output voltage to be tightly controlled. These two loops share the same control command generated by the product of output voltage error signal and the line voltage (or rectified line voltage) signal.

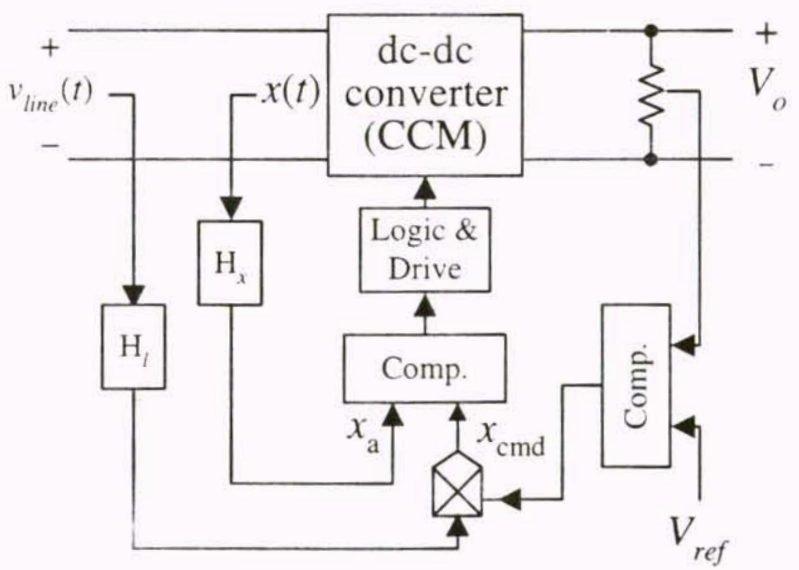


Figure 5-2: Block diagram of PFC converter with CCM shaping technique

In recent years, a lot of control strategies have been proposed in the open literature. The research objective of these techniques is mainly targeted to simplify control circuitry (eliminate current sensor, multiplier and inner loop error amplifier) and achieve better performance such as good stability and fast dynamic response.

Generally speaking, by using CCM shaping technique, the input current can trace the wave shape of the line voltage well. Hence the power factor can be improved with increase efficiently. However, this technique involves design of complicated control circuits. Multi-loop control strategy is needed to perform input current shaping and output regulation. In most CCM shaping techniques, current sensor and multiplier are required, which result in higher cost in practical applications. In some cases, variable frequency control is inevitable, resulting in additional difficulties in its closed-loop design.

5.2.2 DCM Shaping Technique

To get rid of the complicated control circuit invoked by CCM shaping technique and reduce the cost of the electronic interface, DCM input technique can be adopted in low power to medium power level applications.

In DCM, the inductor current of the core converter is not a valid state variable since its state in a given switching cycle is independent of the value in the previous switching cycle. The peak of the inductor current is tracking the line voltage automatically, resulting in sinusoidal-like average input current (line current). The benefit of using DCM input circuit for PFC is that no feedforward control loop is required.

However, the input inductor operating in DCM can not hold the excessive input energy because it must release all its stored energy before the end of each switching cycle. As a result, a capacitor is used to balance the instantaneous power between the input and output. In addition, in DCM, the input current is normally a train of triangular pulses with nearly constant duty ratio. An input filter is necessary for smoothing the pulsating input current.

In two-stage PFC power supply, the DCM converter is connected in front of the AC line to achieve high input power factor and provide a roughly regulated DC bus voltage, as shown in Figure 5-3. This stage is also known as "pre-regulator". The duty ratio of the pre-regulator should be maintained relatively stable so that high power factor is ensured. To stabilize the DC bus voltage, a bank capacitor is used at the output of the pre-regulator. The second stage is a DC/DC converter, called post-regulator, with its output voltage being tightly controlled. This stage can operate either in DCM or in CCM. CCM is normally preferred to reduce the output voltage ripple.

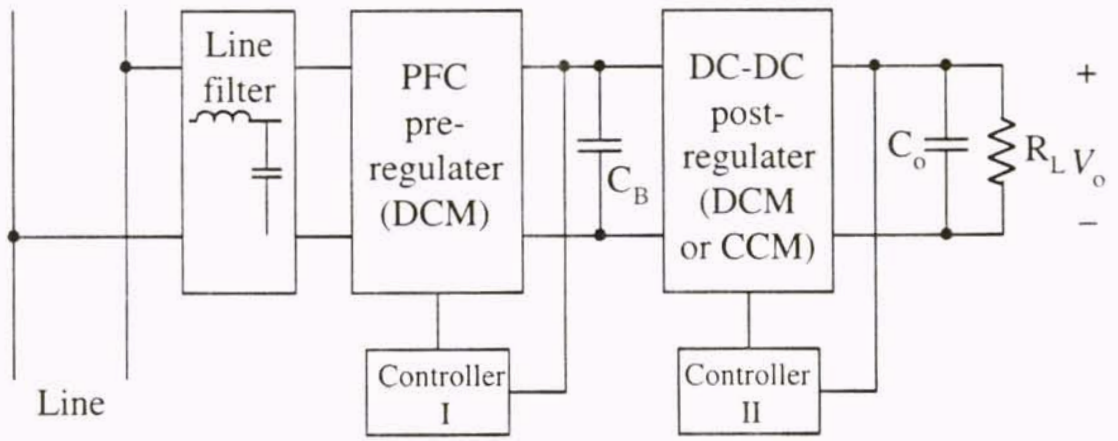


Figure 5-3: DCM input pre-regulator in two-stage AC/DC power supply

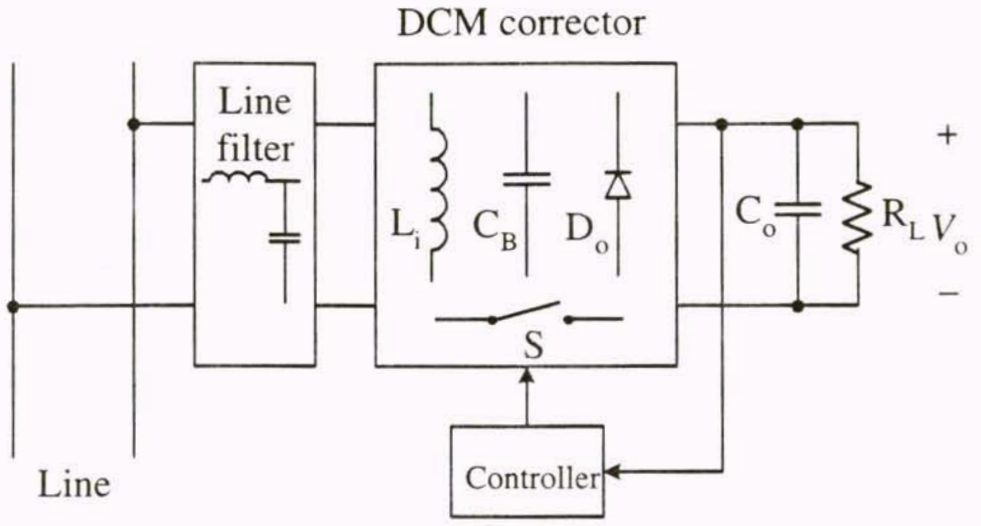


Figure 5-4: DCM input corrector in single-stage AC/DC power supply

DCM input technique is widely used in single-stage power factor correction circuit configurations. Using a basic converter (usually boost or flyback converter) operating in DCM combining with another isolation converter can form a single-stage power factor correction circuit. A storage capacitor is required to hold the DC bus voltage in these combinations. Unlike the two-stage PFC circuit, in which the bus voltage is controlled, the single-stage PFC converter has only one feedback loop from the output. Figure 5-4 shows the diagram of single-stage circuit.

The DCM input circuit can be one of the basic DC-DC converter topologies. However, when they are applied to the rectified line voltage, they may draw different shapes of average line current. In order to examine the PFC capabilities of the basic converters, we first investigate their input characteristics. As the input currents of these converters are discrete when they are operating in DCM, only averaged input currents are considered. Since switching frequency is much higher than the line frequency, we assume the line voltage is constant in a switching cycle. In steady state operation, the output

voltage is nearly constant and the variation in duty ratio is slight. Therefore, constant duty ratio is considered in deriving the input characteristics. By finding the average input current in switching cycle with the line voltage kept as time variable over one cycle, the input current waveform for each basic converter can be qualitatively inspected.

After study of all the eight basic converters, i.e., buck, boost, buck-boost, flyback, forward, Cuk, Sepic and Zeta converters, we conclude that all the eight basic converters except forward converter have good inherent PFC capability and are suitable for DCM PFC usage. For the forward converter, when it is connected to the rectified line voltage, the demagnetizing current through the 3rd winding (reset winding) is blocked by the rectifier diodes. Therefore, forward converter is not suitable for PFC purpose unless a certain circuit modification is applied. Boost converter and flyback converter are especially suitable for single-stage PFC scheme because they have minimum component count and grounded switch drive, and their power switches are easy to be shared with the output DC-DC converter. The other converters could also be used to perform certain function such as circuit protection and small output voltage ripple.

5.3 Single Stage Hard-Switching Topology

5.3.1 Single Stage Topology

An AC/DC converter is presented in this section [2], aimed at overcoming the above difficulties. The S^4 converter utilizes a DCM boost circuit as an input stage to perform PFC and a forward circuit as an output stage to provide electrical isolation. Two

storage capacitors have been employed to enhance the PFC capability of the boost circuit and to relieve the voltage spike produced by the power transformer. The voltages across the storage capacitors are kept at lower levels. Theoretical analysis and experimental results show that the converter has enough line regulation capability to be applied to universal input.

The AC/DC converter is shown in Figure 5-5. The input circuit is a boost circuit (formed by choke inductor L, diode D_1 and switch S). The switched-capacitor network consists of capacitors C_{s1} and C_{s2} and diode D_2, serving as a load to the input circuit, and as a source to the output forward circuit (formed by transformer Tr and diode D_3). The two primary windings of the forward transformer are designed with the same turn ratio referring to the secondary winding (1:1:*n*). Inductances L_1 and L_2 (L_1 = L_2) are the leakage inductances of the forward transformer. It can be shown that, in steady-state, the converter has four operation modes during one switching cycle. The converter key waveforms are shown in Figure 5-6.

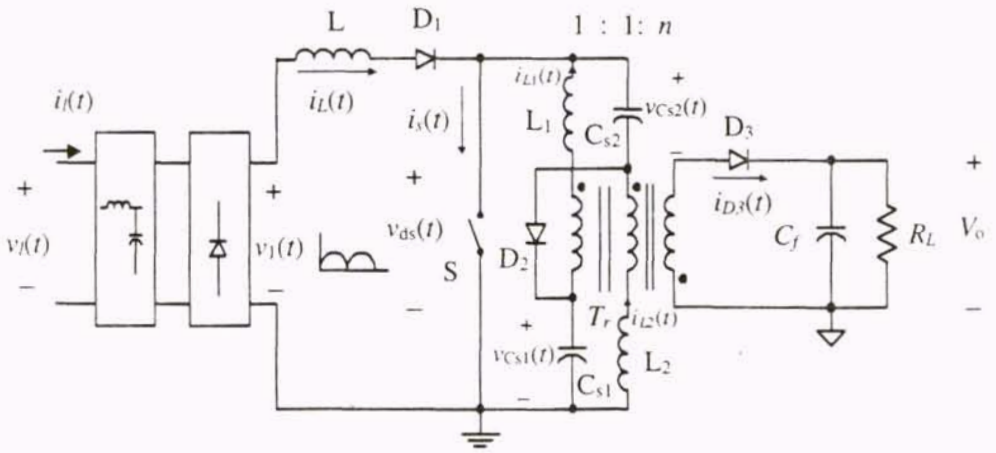


Figure 5-5: Basic circuit schematic of the converter

Notice that in one switching cycle, the line voltage can be considered as a constant voltage in the equivalent circuits. Capacitors C_{s1} and C_{s2} are designed to be large and equal. Hence, in the steady-state analysis, each capacitor voltage is approximated by a DC source $V_{Cs1} = V_{Cs2} = V_{Cs}$.

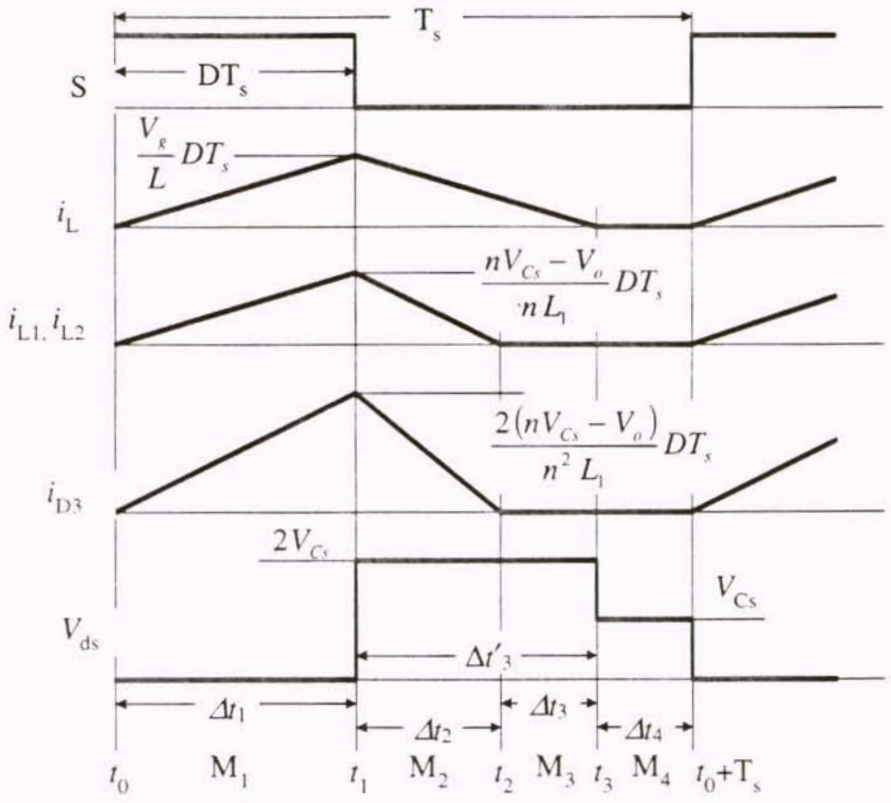


Figure 5-6: Theoretical key waveforms of the converter

5.3.2 Limitations of Hard-switching

With the available devices and circuit technologies, PWM converters generally have been designed to operate with 50-200kHz switching frequency. In this frequency range, the power supply is deemed optimal in weight, size, efficiency, reliability, and cost. In more recent applications such as adaptor, notebook, and laptop computers where high power density is of primary concern, it is desirable to push the conversion frequency as high as the upper hundreds kilohertz to lower-megahertz range. However, higher switching frequency invariably results in increased switching losses. The switching loss at turn-off is primarily caused by the leakage inductance of the power transformer. As the semiconductor device turns off, the sharp di/dt induces high voltage spike across the leakage inductance [3, 4]. To reduce switching stress, dissipative snubbers are typically used. At turn-on, switching losses are mainly caused by abrupt discharging of the energy stored in the parasitic capacitance of the semiconductor devices. When the transistor is turned on, the energy stored in its output capacitance is dissipated in the device. Also, turn-on at high voltage levels induces a severe switching noise coupled through the Miller capacitance into the drive and control circuits. The aforementioned detrimental effects of the circuit parasitic become much more pronounced as the switching frequency is increased.

5.4 Novel Soft-Switching Methods

5.4.1 Operation Principles

The proposed soft-switching converter in Figure 5-7 is based on the hard-switching single-stage PFC converter with two bulk capacitor proposed in previous section. Besides achieving zero-voltage transition (ZVT), the circuit also using an extra winding on the transformer core as a snubber to lower the voltage and the current stresses of switches.

The main waveforms and the schematic simulation are shown in Figure 5-7 and Figure 5-8, respectively. It is noted that the simulated waveforms are the same as theoretical waveforms. Also, the ZVS and ZCS are achieved for the main switch and auxiliary switch, respectively.

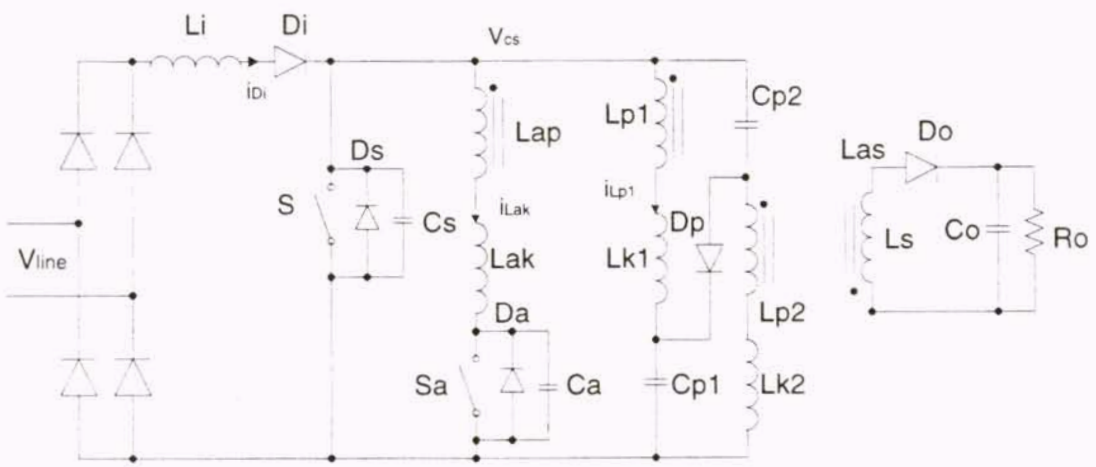


Figure 5-7 Proposed soft-switching topology

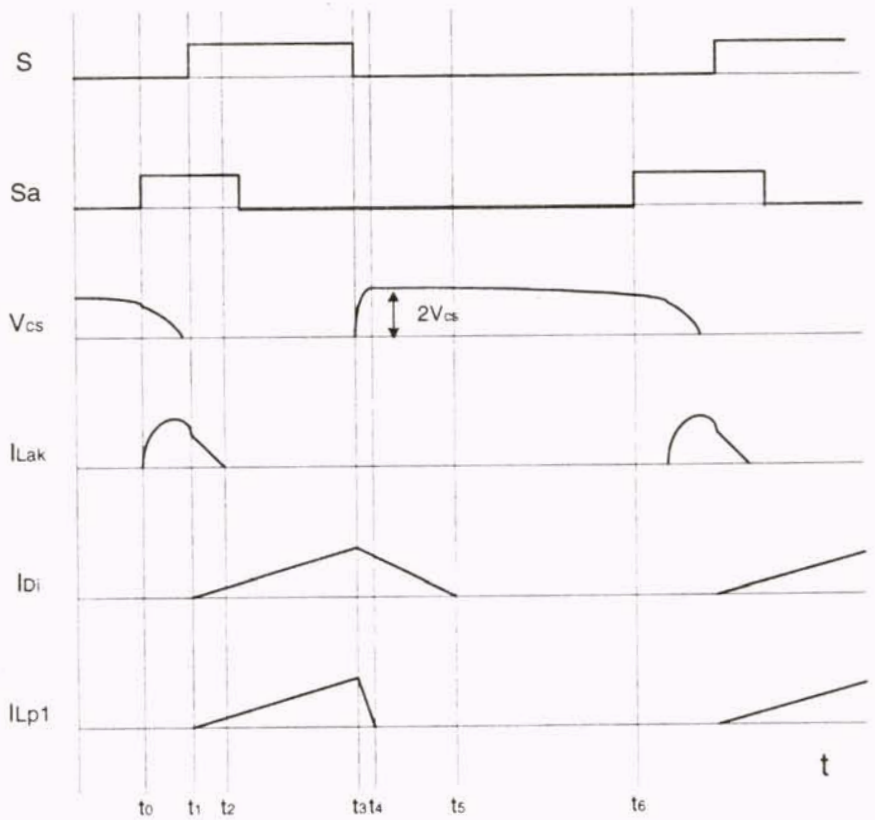
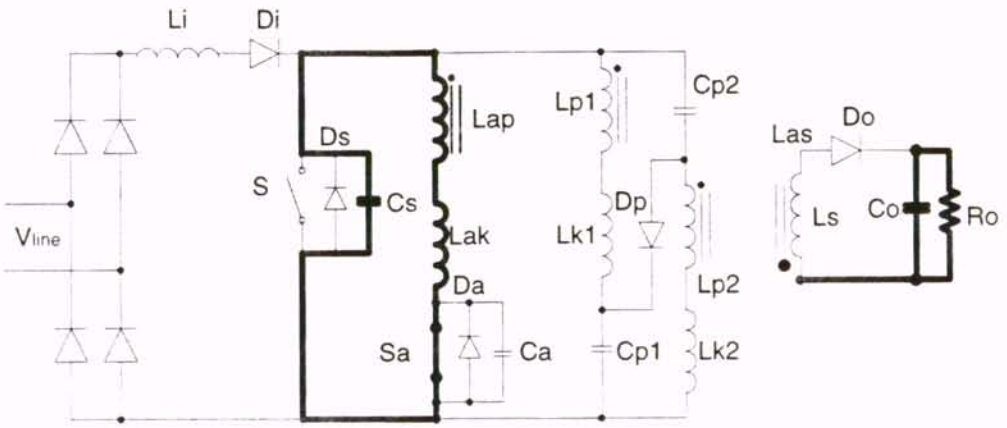
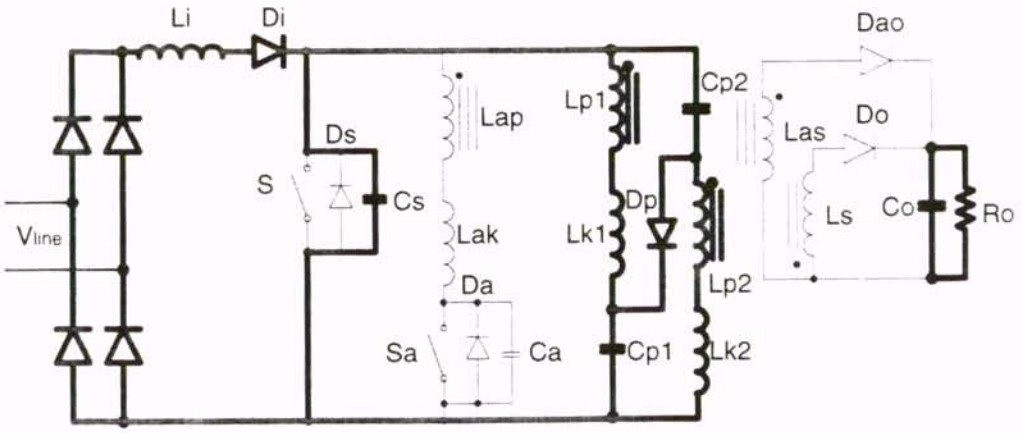


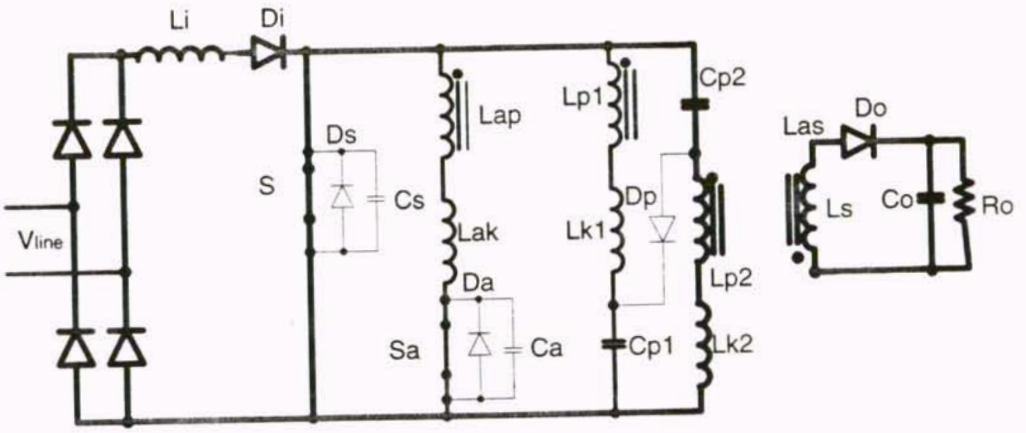
Figure 5-8: Main Switching Waveforms



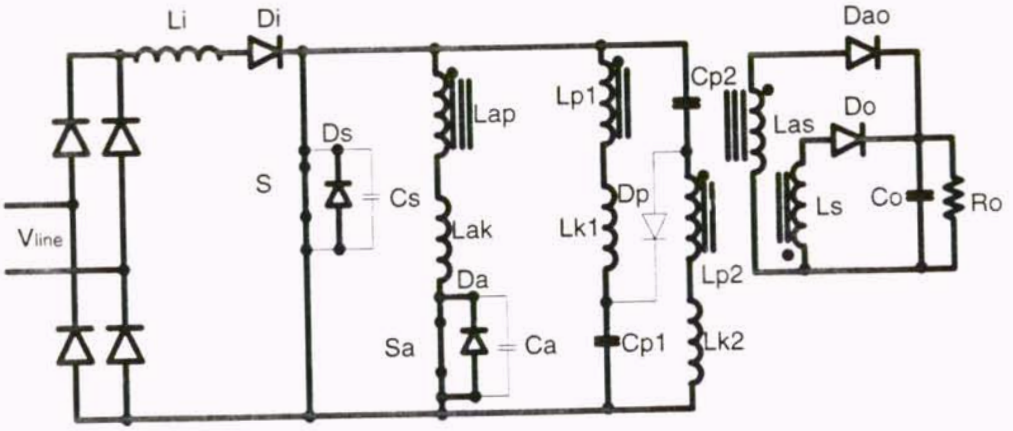
(a) Mode 1



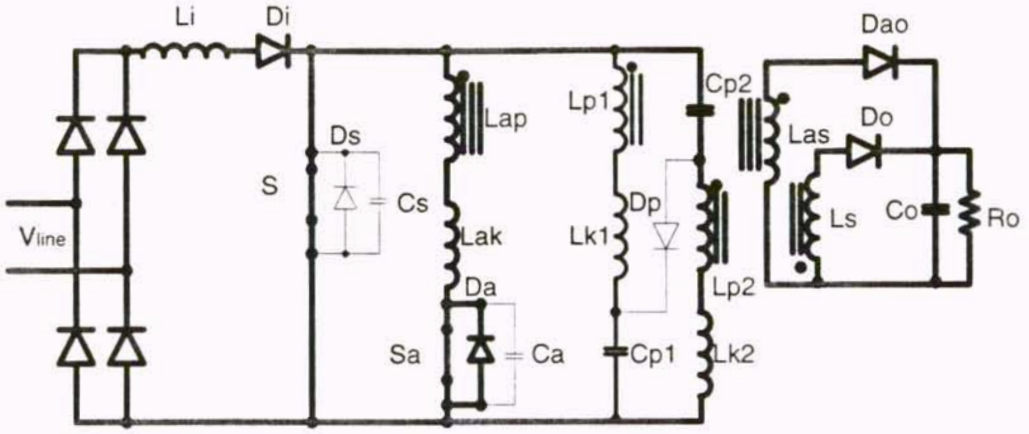
(b) Mode 2



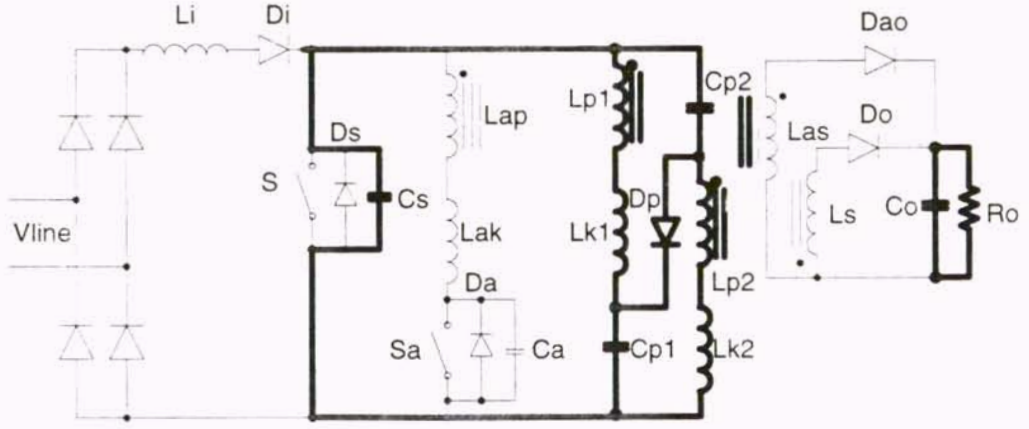
(b) Mode 3



(d) Mode 4



(e) Mode 5



(f) Mode 6

Figure 5-9: Modes of Operation

Mode 1: $t_0 < t < t_1$

Initially, it is assumed that S was OFF and C_S was charged to $2V_{Cs}$. At $t = t_0$, the auxiliary switch S_a is turned ON. C_s, C_a, and L_{ak} form a resonant tank as shown in Figure 5-9(a). At the end of this mode ($t = t_1$), the capacitor voltage of the main switch S hits zero. D_{ao} starts to conduct when the auxiliary switch is turned ON, and the energy is transferred from the primary winding to the secondary winding. After that, S is ready to be turned ON at ZVS.

Mode 2: $t_1 < t < t_2$

After turning S on at $t = t_1$, the diode D_i conducts and the source voltage is applied to the input choke inductor L_i, causing the current through the choke inductor to charge up linearly. During this mode, the energy is transferred from the source to the choke inductor. The period ends when the leakage inductor current I_{Lak} reaches zero and D_{ao} is turned OFF. The choke current continues to charge up linearly.

Mode 3: $t_2 < t < t_3$

This mode is a freewheeling mode as shown in Figure 5-9(c). The auxiliary switch is turned OFF in this period.

Mode 4: $t_3 < t < t_4$

At $t = t_3$, S is turned off. The main switch output capacitor C_s is quickly charged up by the current i_{Li} to $2V_{Cs}$ (clamped by the conduction of D_p). Under the constraint of KCL, both the storage capacitors, C_{p1} and C_{p2} are being charged by the current $i_{Lp1} + i_{Lp2}$ during this operation period. With the inductor current i_{Li} decreasing linearly,

magnetic energy stored in the choke is being converted into electric energy and being stored into the storage capacitors. Thus the energy loss of the storage capacitors during Mode 2 is being recovered.

Mode 5: $t_4 < t < t_5$

The choke inductor current, I_{L_r} continues to decrease linearly. Owing to the existence of diode D_o, the primaries of the transformer present very high impedance with the currents through the windings can be negligible. This period ends when the choke inductor current reaches zero.

Mode 6: $t_5 < t < t_0 + T_s$

This is a free-wheeling stage for regulation purpose.

Soft-switching is maintained for wide line and load range, which is a unique feature for ZVT. In mode 1, the differential voltage across the main switch is equal to $2V_{Cs}$, where:

$$V_{Cs} = V_0 \cos(\frac{1}{\sqrt{L_{ak} C_s}} t) \tag{5-4}$$

V_0 is the V_{cs} at $t = 0$. For ZVS, V_{cs} drops to zero before the mode 2 begins. So we will get:

$$t_1 - t_0 > \frac{\pi}{2} \sqrt{L_{ak} C_s} \tag{5-5}$$

The right side of the above inequality is a constant, which means for this converter, soft-switching operation will be ensured for the whole load and line range as long as we choose proper values for the time delay between the gate signals of main and auxiliary switches and the leakage inductance of the transformer.

This single stage converter can be regarded as a combination of a boost converter in a DCM mode and a forward converter. Using the model in [5], we design a compensator with which the crossover frequency of the loop gain is a few kilohertz. The control chip is UC3825. Compared to the other type single-stage converter, like isolated SEPIC using UC3854 [6], or flyback converter with charge control, this converter exhibits better transient response and load regulation with a smaller bulk capacitor for certain holdup requirement.

5.4.2 Simulation and Experimental Results

A 50W 500kHz prototype has been built in the laboratory to experimentally verify the theoretical analysis and simulation results. It is clear that the experiment result agrees well with the analysis and computer simulation.

Using the component values from the above design example, Pspice circuit is simulated to produce the result shown in Figure 5-10. And tc verify the steady state operation of the proposed converter, a 110V/60Hz input, 28V@3.5A output experimental prototype was built. The following key components were used in the implementation of the experimental circuit:

Input inductor Li = 35uH, 3F3 RM10 core,

Transformer — Philips 3F3 RM12 core,

$N_{p1}= N_{p2}= N_{ap}$=16T, $L_{ak}=L_{k1}=L_{k2}$=3uH,

Switches — S: IXFH20N60,

Sa: IXTP3N90A,

Storage Capacitors — 220uF/250V,

Diodes — D_i, D_L, D_p: DSEI 1210A,

Low voltage rectifier diode D_0 — 30CPQ060,

Switching frequency — 500kHz.

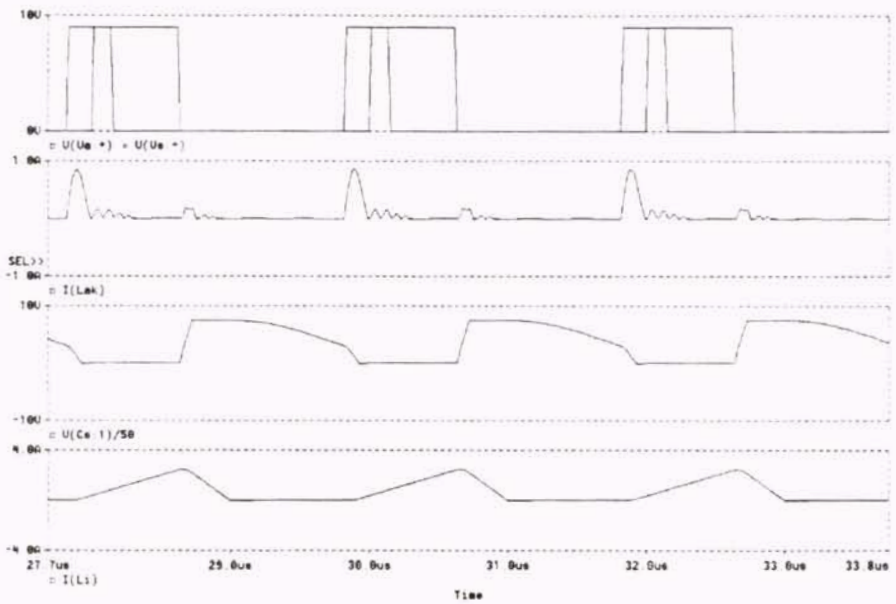


Figure 5-10: Simulation Results

Figure 5-11 gives the measured line voltage and current waveforms, resulting in power factor of 0.987. In Figure 5-12, the voltage across the main switch and its drain current are shown. As shown, just before *S* is turned *ON*, its body diode carries the reverse current, hence, achieved zero-voltage turn *ON*. Finally, Figure 5-13 shows the auxiliary switch, S_a, current and voltage. From Figure 5-10 we can estimate $\Delta t_2 \approx 50$nsec, from the theoretical calculation $\Delta t_2 \approx 55$nsec and the simulation gives about 65nsec witch are in a good agreement .

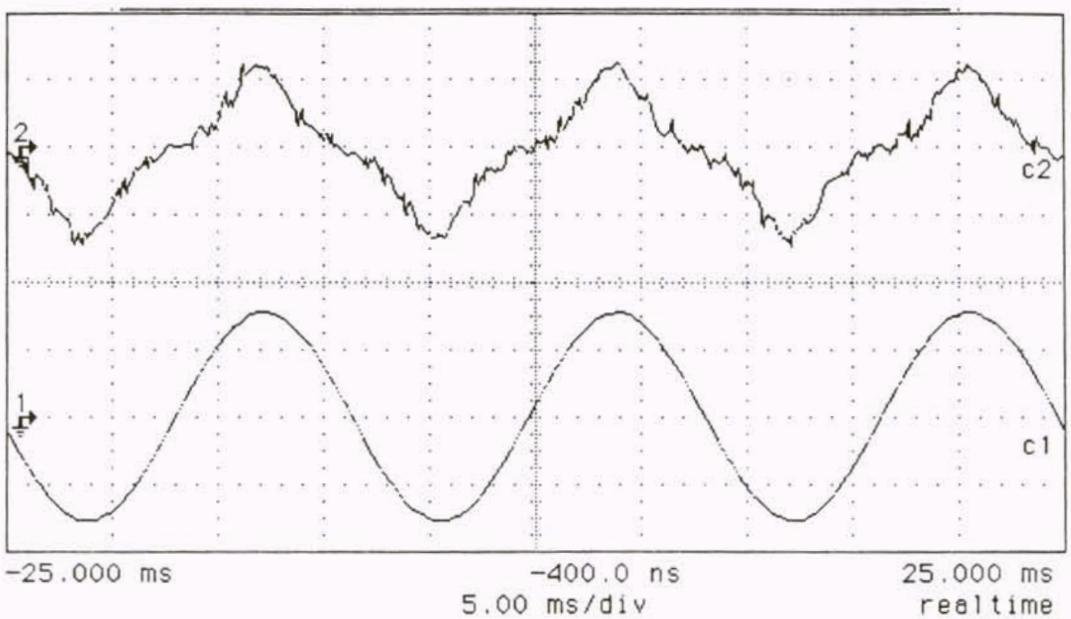


Figure 5-11: Input current (upper trace 1A/div) and input voltage (lower trace 100V/div)

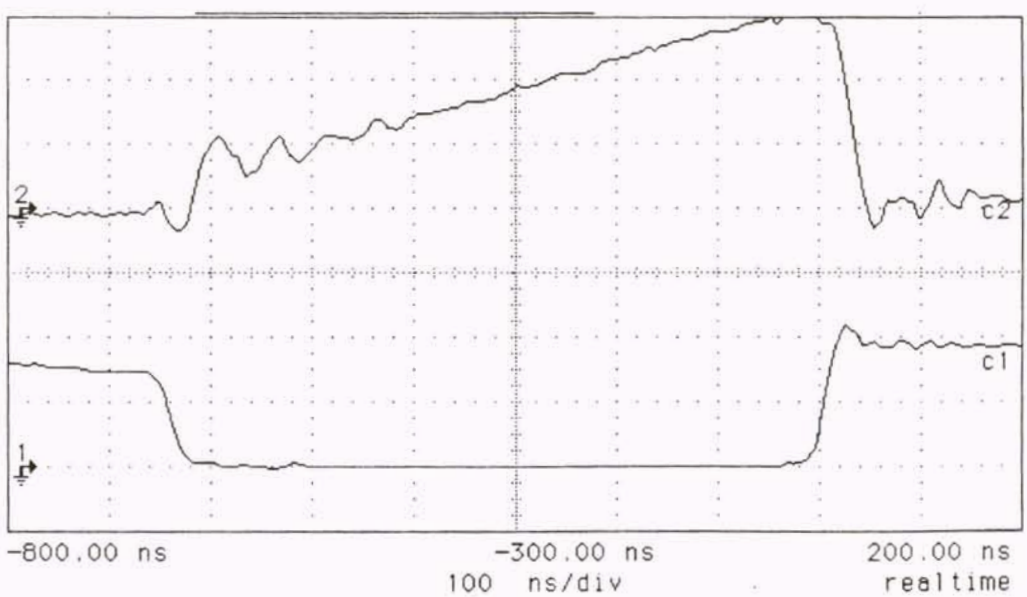


Figure 5-12 Main switch ,current (upper trace 2A/div) and voltage (lower trace 100V/div)

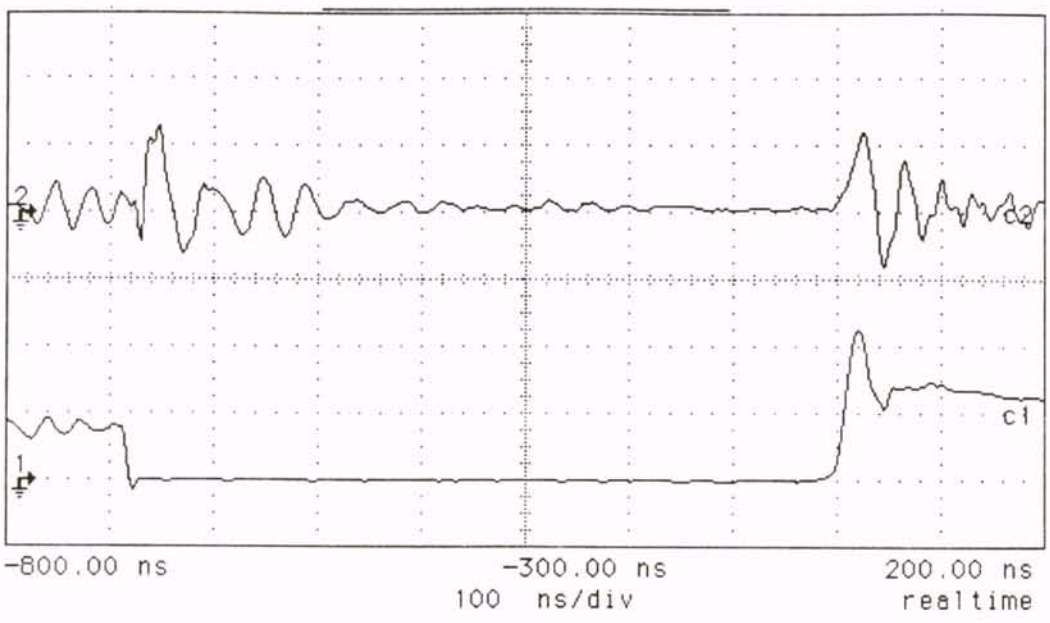


Figure 5-13 Auxiliary switch, S_a, Current (upper trace 1A/div) and voltage (lower trace 200v/div)

5.5 Summary

Due to high frequency operation, the proposed soft-switching converter makes the AC-DC front-end power supply possible to be minimized in size and weight. At the same time, the active single-stage PFC techniques help to reduce the component count and cost. Therefore, for the low power application, this proposed converter could be considered as a strong competitor.

CHAPTER SIX

A NEW SINGLE SWITCH SINGLE STAGE TOPOLOGY

6.1 A NOVEL SINGLE SWITCH SINGLE STAGE AC/DC CONVERTER

Due to the ability to keep a relatively low voltage on the energy-storage capacitor, this technique is suitable for the universal line voltage application.

For the forward and flyback converter-type, a direct transfer of part of the input energy is achieved by the winding that appears in series with the boost inductor during the on and off time, respectively.

6.1.1 Operation Principle

Figure 6-1 shows the proposed topology. In mode 1, when the input line voltage is lower than a set value, the voltage across Li2 is lower than Li3, so the diode in series with Li3 is turned off as show in Figure 6-2. In mode 2, the input line voltage increases to turn off the diode in series with Li3 while the diode with Li2 is turned off and direct energy transfer happens.

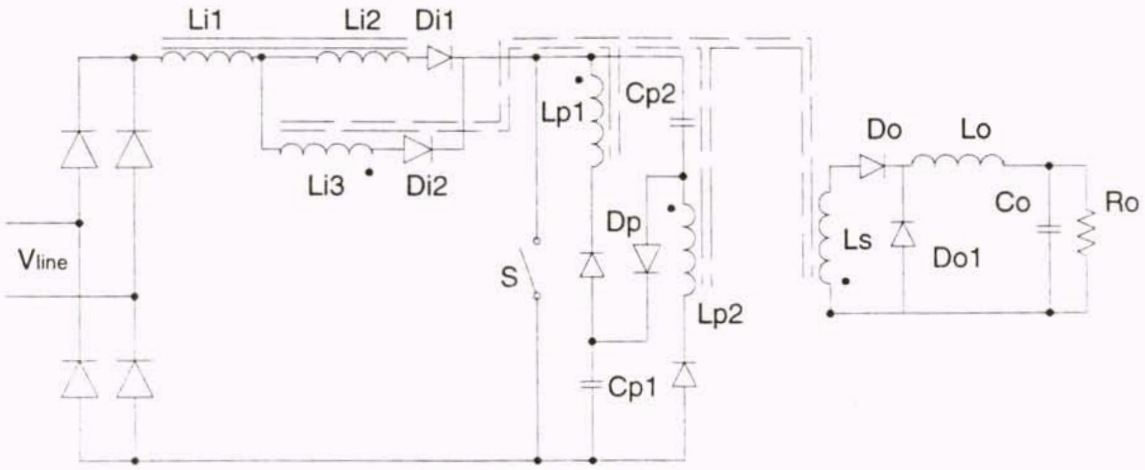


Figure 6-1 Proposed single stage topology with lower stress

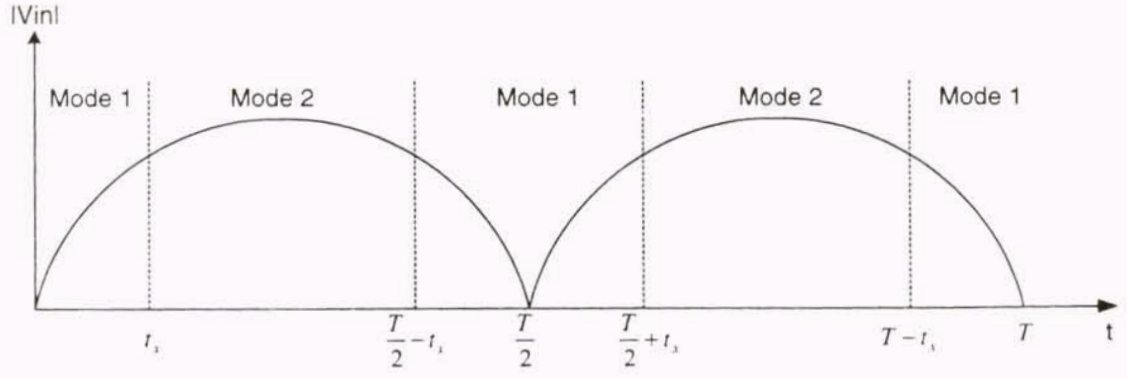


Figure 6-2 Operation Mode of the proposed single stage topology

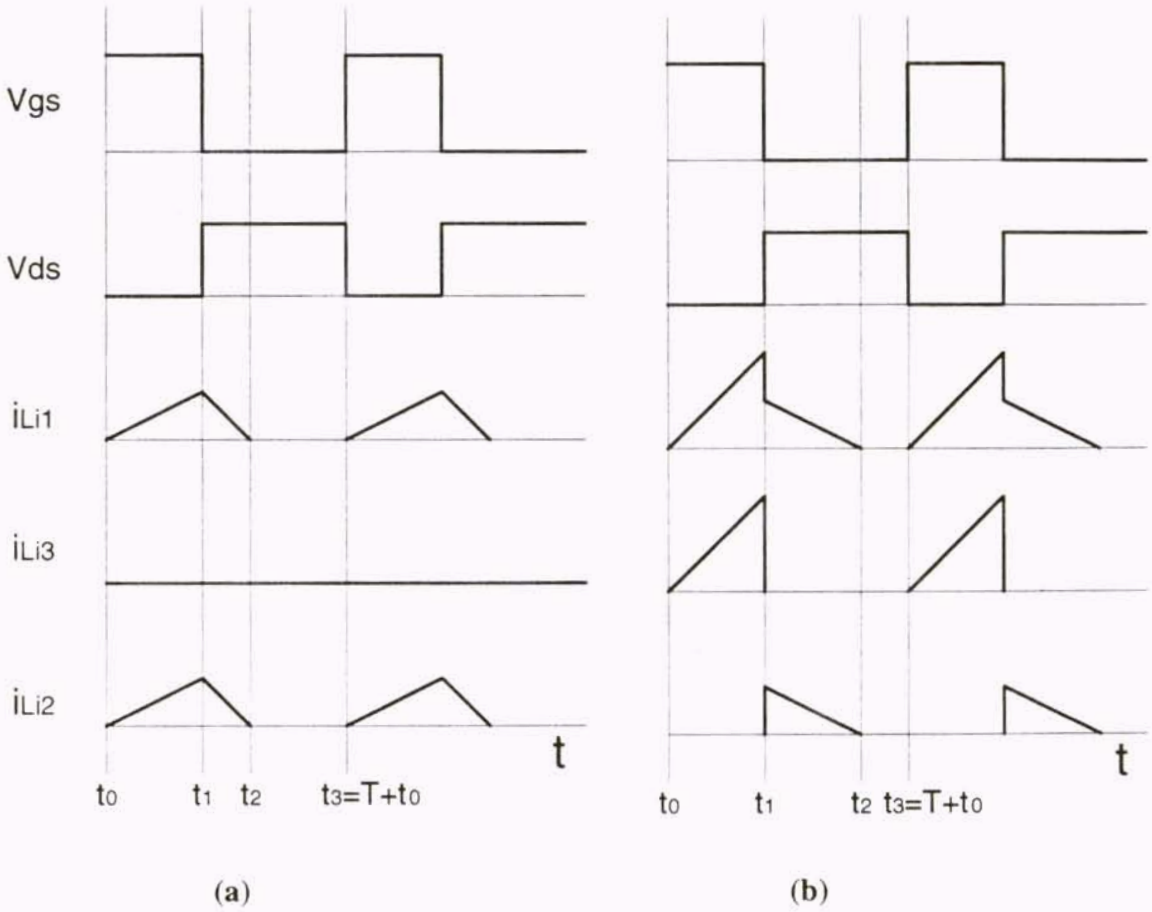


Figure 6-3 Main waveforms

Figure 6-3(a) shows the main waveforms in mode 1 and Figure 6-3(b) shows the main waveforms in mode 2. In both modes, the current i_{L1} is the sum of the current i_{L2} and i_{L3}.

$t_0 < t < t_1$:

After turning S on at $t = t_0$, the diode D_{f1} conducts and the source voltage is applied to the input choke inductor L_{i1}, causing the current through the choke inductor to charge up linearly. During this period, the energy is transferred from the source to the

choke inductor. For mode 2, when the line voltage in high, some of the energy is transferred to the secondary as there is current on L_{i3}.

$t_1 < t < t_2$:

At $t = t_1$, S is turned off. The Diode Di2 is turned off. The energy in the choke Li1 is discharge though Li2 in both modes.

$t_2 < t < t_3$:

This is a free-wheeling stage for regulation purpose.

6.1.2 Simulation and Experimental Results

Figure 6-4 shows the simulation results in mode 2 and Figure 6-5(a) shows the experimental results, which are well agreed with the theoretically analysis.

Figure 6-4(b) shows input voltage waveform and input current waveform.

Figure 6-6 is power factor against the input voltage.

Figure 6-7 is the efficiency against the input voltage.

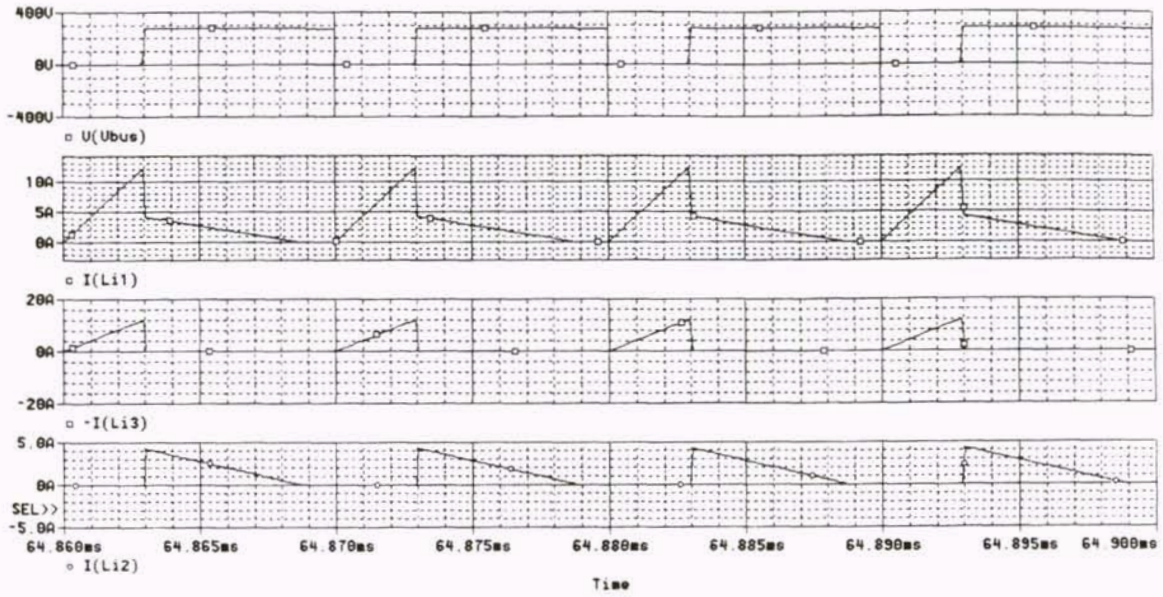
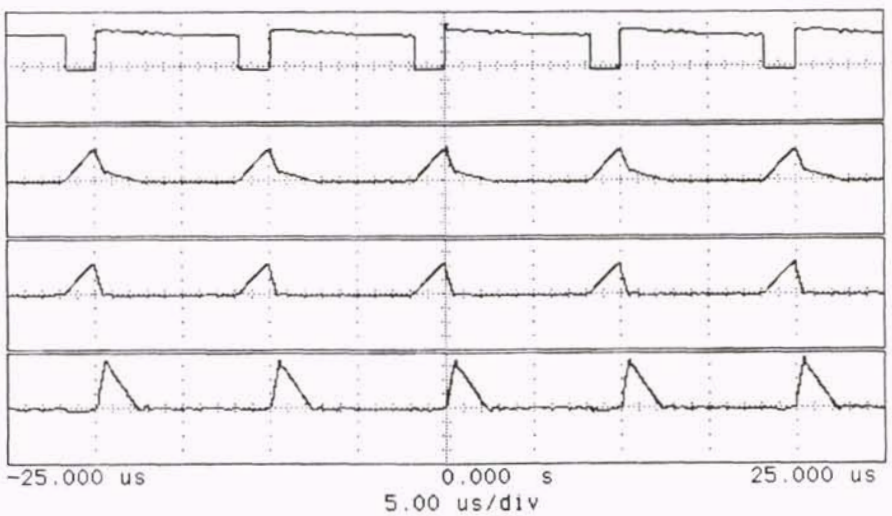
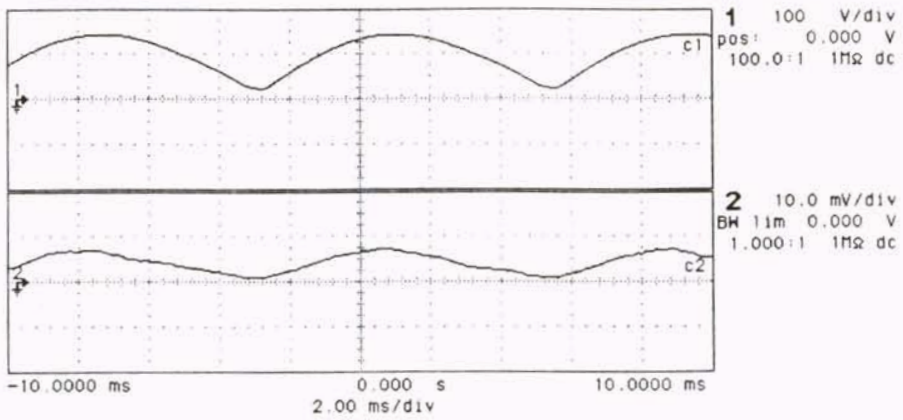


Figure 6-4 Simulation results



(a)



(b)

Figure 6-5 Experimental results

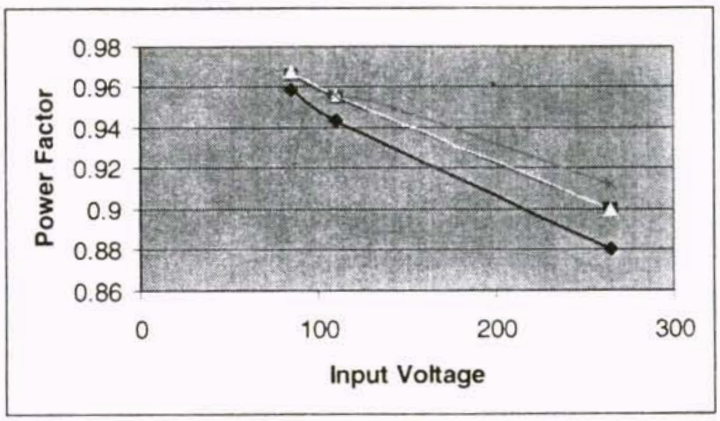


Figure 6-6 Power factor vs. input voltage with different loads

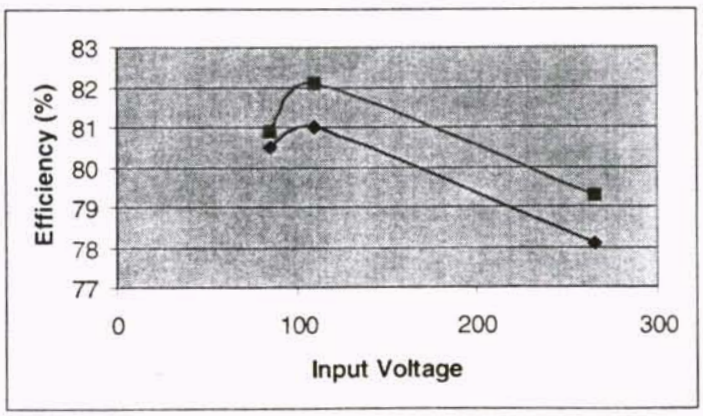


Figure 6-7 Efficiency vs. input voltage (low trace: hard-switching converter in chapter 5, top trace: new converter)

6.2 Summary

A new single-stage, single-switch technique that combines the boost-like input-current shaper with a discontinuous-conduction-mode dc/dc output stage is introduced in Chapter 6. With this technique, the boost inductor can operate in both the discontinuous and continuous conduction modes. By controlling the turn-ration of the windings, the input current harmonic contents can be reduced to comply with IEC-1000-3-2 limits. As part of the energy to the output is taken directly from the line, the power device stress is reduced and efficiency is improved.

CHAPTER SEVEN

CONCLUSIONS

Future generations of microprocessors are expected to operate at a much lower voltage, 1~2V, a much higher current, 50-100A. For other applications like semiconductor chip burn-in equipment, the voltage will go to 0.5V and the output current will be 240A. The future generation of Voltage Regulator Modules (VRM) has to be improved dramatically to meet future challenges, such as faster transient slew rate, tighter voltage tolerance and higher conversion efficiency. Furthermore, there is also a strong need for a significantly higher power density, with much-reduced capacitor and inductor size, suitable for integration with the processor.

Low-voltage power management issues are becoming increasingly more critical in state-of-the-art computing system. The current generation of high-speed CMOS processor (e.g. Alpha, Pentium, Power PC) operate at above 300MHz with 2.5 to 3.3V output voltage. Future processors will be designed with even lower logic voltages down to 1.1~1.5V, and an increase in current demand from 13A to 50~100A. Meanwhile, the operating frequency will increase above 1 GHz. For future generation processors, the high transient current-slew-rate (several Amperes per Nanosecond) will result in significant voltage transient. To ensure proper operation, a more stringent voltage regulation from 5% to 2% regulation is imposed. These demands in turn require a special power supply, voltage regulator module (VRM), to provide lower voltages with higher

current and fast transient response capability for microprocessors. This dissertation proposes and verifies several new techniques for this low-voltage power management application.

The interleaved synchronous buck regulator with hysteresis control presented in Chapter 2 achieves a very fast transient response and high power density. With the interleaving technique, both the VRM input current ripple and output current ripple are cancelled. Both the VRM input and output filter sizes can be reduced dramatically. Also with the hysteretic control, fast response of the VRM is guaranteed. This VRM is well-suited for future microprocessor applications, where the transient response and converter size are primary concerns.

Chapter 3 presents two interleaved half-bridge power stage that naturally cancels the output current ripple while achieving fast response. Using a new method of master-slave peak current control, charge balance is automatically achieved and current runaway is avoided without additional correction circuitry, resulting in increased efficiency.. With the integration of the output inductors and design mixed-signal chips for the control and driver circuit, the efficiency and performance are readily improved.

The high-input-voltage VRM topology, phase-shift full bridge converter that can be used in high-bus-voltage distributed power system is investigated in Chapter 4. This topology can achieve a high efficiency. Compared with conventional high-voltage VRM topologies, it has small input and output current ripples, low device stress and high efficiency. Since it is only a second-order system, this topology can have a fast transient response with a small filter inductance and capacitance. In addition, its transformer and inductors can be easily integrated. In addition with a small filter capacitance and high

efficiency, a very high power density can be achieved. As a result, compared with conventional high-input-voltage VRM topologies, this topology is cost-effective and has a high performance. Also the dual or multiple output topology provides a competitive way for this application and has advantages over existing products in terms of efficiency, reliability and flexibility.

Traditional diode rectifiers used in front of the electronic equipment draw pulsed current from the utility line, which deteriorates the line voltage, produce radiated and conducted electromagnetic interference, leads to poor utilization of the capacity of the power sources. In compliance with IEC 1000-3-2 harmonic regulation, many power factor corrected ac/dc rectifiers have been proposed in recent years. In a single-stage PFC, input-current shaping, isolation, and fast output regulation are performed in a single stage. This method provides a compromise between the performance and cost. Comprehensive comparisons of the three approaches at manufacture cost and performance have shown that the single stage PFC is a cost effective solution for low to median power applications.

In Chapter 5, a proposed soft-switching converter makes the AC-DC front-end power supply possible to be minimized in size and weight due to high frequency operation. At the same time, the active single-stage PFC techniques help to reduce the component count and cost. Therefore, for the low power application, this proposed converter could be considered as a strong competitor.

A new single-stage, single-switch technique that combines the boost-like input-current shaper with a continuous-conduction-mode dc/dc output stage is introduced in Chapter 6. With this technique, the boost inductor can operate in both the discontinuous

and continuous conduction modes. By controlling the turn-ration of the windings, the input current harmonic contents can be reduced to comply with IEC-1000-3-2 limits. As part of the energy to the output is taken directly from the line, the power device stress is reduced and efficiency is improved.

My future work will be focusing on the low voltage, high current converters, distributed power system and Power Factor Correction circuits. Advanced system architecture needs to be further explored in order to meet the future demands. So do topologies, control method and packaging which contribute the success of the power electronics, an enabling technology.

APENDIX

MATHCAD CODES FOR COMPENSATOR DESIGN

(1) Average Current Control

Control loop design:

Power stage parameters

$v_g := 14 \qquad v_0 := 5 \qquad R := 1 \qquad L := 37.5 \cdot 10^{-6} \qquad C := 380 \cdot 10^{-6} \qquad R_c := 0.02$

$F_s := 0.05 \cdot 10^6 \qquad D := \frac{v_0}{v_g} \qquad T_s := \frac{1}{F_s}$

Current loop element values

$R_i := 0.1$

$R_1 := 2200$

$R_f := 30500$

$C_{fz} := 5.8 \times 10^{-9}$

$C_{fp} := 220 \cdot 10^{-12}$

Supplemary values

$S_e := 5 \cdot 10^4$

$S_{n0} := 10^5$

Modulator Gain

$$\omega_i := \frac{1}{R_1 \cdot (C_{fp} + C_{fz})} \qquad \omega_z := \frac{1}{R_f \cdot C_{fz}} \qquad \omega_p := \frac{C_{fz} + C_{fp}}{R_f \cdot C_{fz} \cdot C_{fp}}$$

$\omega_z = 5.653 \times 10^3 \qquad \omega_p = 1.547 \times 10^5 \qquad \omega_i = 7.551 \times 10^4$

$$S_n := \omega_i \cdot S_{n0} \cdot \left[D \cdot T_s + \left(\frac{1}{\omega_z} - \frac{1}{\omega_p} \right) \cdot \left(1 - e^{-\omega_p \cdot D \cdot T_s} \right) \right] \qquad S_n = 9.145 \times 10^5$$

$$F_m := \frac{1}{(S_e + S_n) T_s} \qquad F_m = 0.052$$

Sampling Gain

$$\omega_n := \frac{\pi}{T_s} \qquad Q_z := \frac{-2}{\pi} \qquad \omega_n = 1.571 \times 10^5$$

$$H_e(s) := 1 + \frac{s}{\omega_n \cdot Q_z} + \frac{s^2}{\omega_n^2}$$

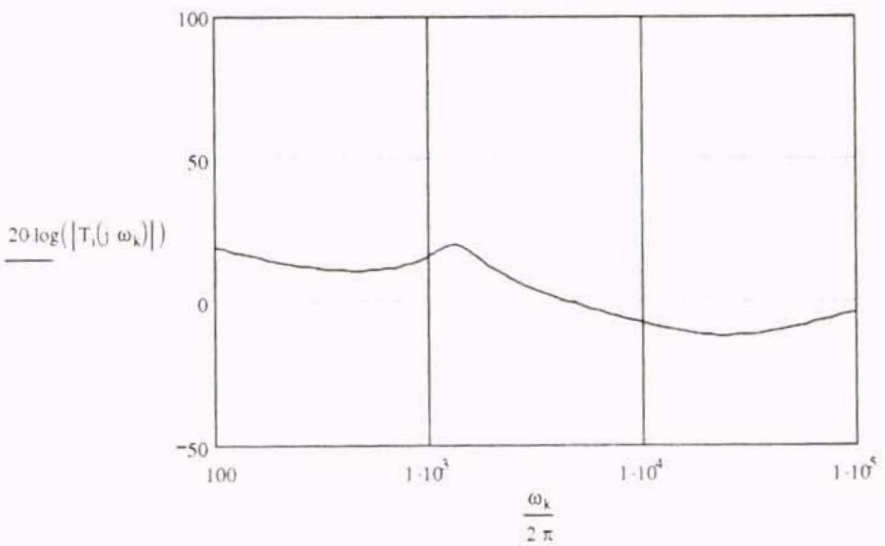
Control loop gain

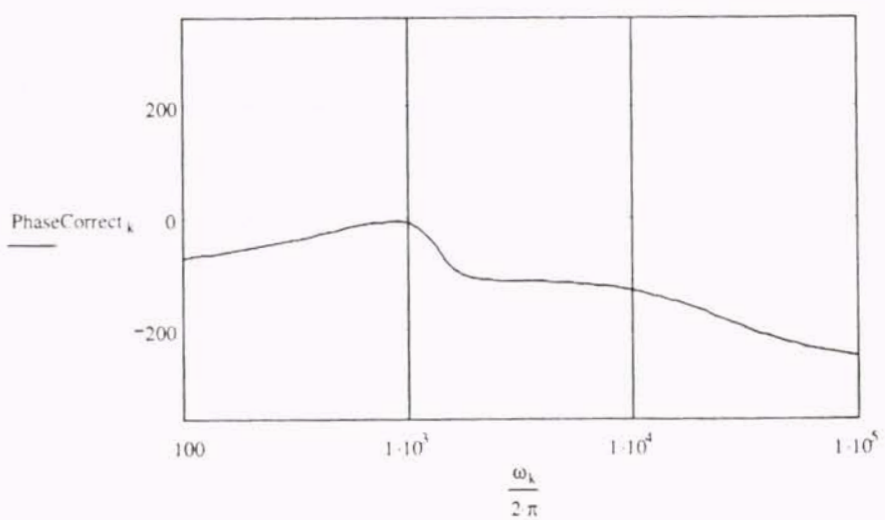
$$T_i(s) := \frac{F_m \cdot R_i \cdot v_g}{R} \cdot \frac{(1 + s \cdot R \cdot C)}{1 + s \cdot \left(\frac{L}{R} + C \cdot R_c\right) + s^2 \cdot L \cdot C} \cdot H_e(s) \cdot \frac{\omega_i \cdot \left(1 + \frac{s}{\omega_z}\right)}{s}$$

$k := 0 .. 225 \qquad \omega_k := 10^{-1+\frac{k}{25}}$

$$RawPhase_k := \frac{\arg\left(T_i\left(j \cdot \omega_k\right)\right)}{deg}$$

$$PhaseCorrect_k := \begin{cases} RawPhase_k & \text{if } -180 \le RawPhase_k \le 0 \\ \left(RawPhase_k - 360\right) & \text{if } 0 < RawPhase_k \le 180 \end{cases}$$





Control to output Gain

$$C_x := \frac{1}{F_m \cdot v_g \cdot \omega_i \cdot R_i} \qquad Q_p := \frac{Q_z}{1 + Q_z \cdot L \cdot C_x \cdot \omega_n \cdot \omega_z}$$

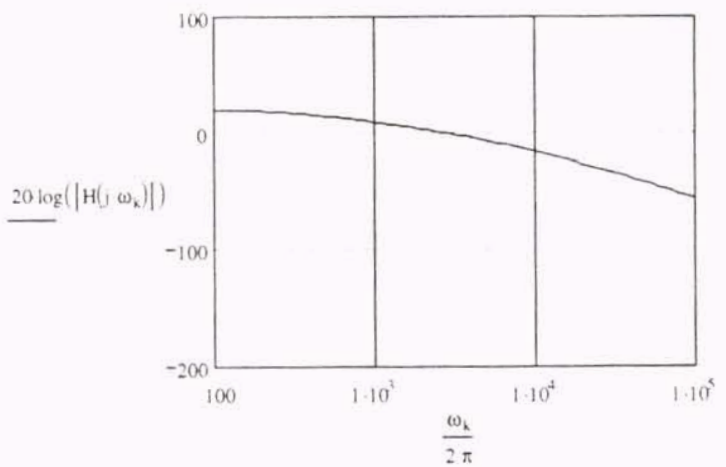
$$F_h(s) := \frac{1}{1 + \frac{s}{\omega_n \cdot Q_p} + \frac{s^2}{\omega_n^{\,2}}}$$

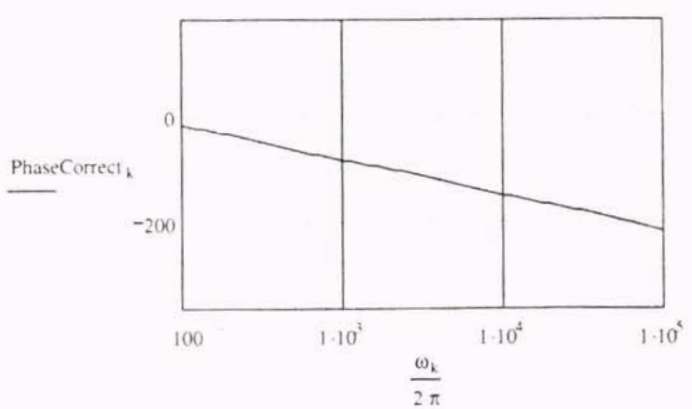
$$H(s) := \frac{R}{R_i} \cdot \left[\frac{1 + s \cdot R_c \cdot C}{\left[1 + s \cdot R \cdot (C + C_x)\right] \cdot \left(1 + \frac{s}{\omega_p}\right)} \cdot F_h(s) \right]$$

$$k := 0 .. 225 \qquad \omega_k := 10^{-1 + \frac{k}{25}}$$

$$RawPhase_k := \frac{\arg(H(j \cdot \omega_k))}{deg}$$

$$PhaseCorrect_k := \begin{cases} RawPhase_k & \text{if } -180 \le RawPhase_k \le 0 \\ (RawPhase_k - 360) & \text{if } 0 < RawPhase_k \le 180 \end{cases}$$





(2) Peak Current Control

Control loop design

Power stage parameters

$v_g := 11 \qquad v_0 := 5 \qquad R := 1 \qquad L := 37.5 \cdot 10^{-6} \qquad C := 400 \cdot 10^{-6} \qquad R_c := 0.014$

$F_s := 0.05 \cdot 10^6 \qquad D := \frac{v_0}{v_g} \qquad T_s := \frac{1}{F_s} \qquad D_{prime} := 1 - D \qquad R_i := 0.33$

$m_c := 2$

Sampling Gain

$\omega_n := \frac{\pi}{T_s} \qquad Q_z := \frac{-2}{\pi}$

$H_e(s) := 1 + \frac{s}{\omega_n \cdot Q_z} + \frac{s^2}{\omega_n^2} \qquad \omega_n = 1.571 \times 10^5$

Current loop Gain

$\omega_0 := \frac{1}{\sqrt{L \cdot C}} \qquad Q_p := \frac{1}{\omega_0 \cdot \left(\frac{L}{R} + C \cdot R_c\right)}$

$Delta(s) := 1 + \frac{s}{\omega_0 \cdot Q_p} + \frac{s^2}{\omega_0^2} \qquad \omega_0 = 8.165 \times 10^3$

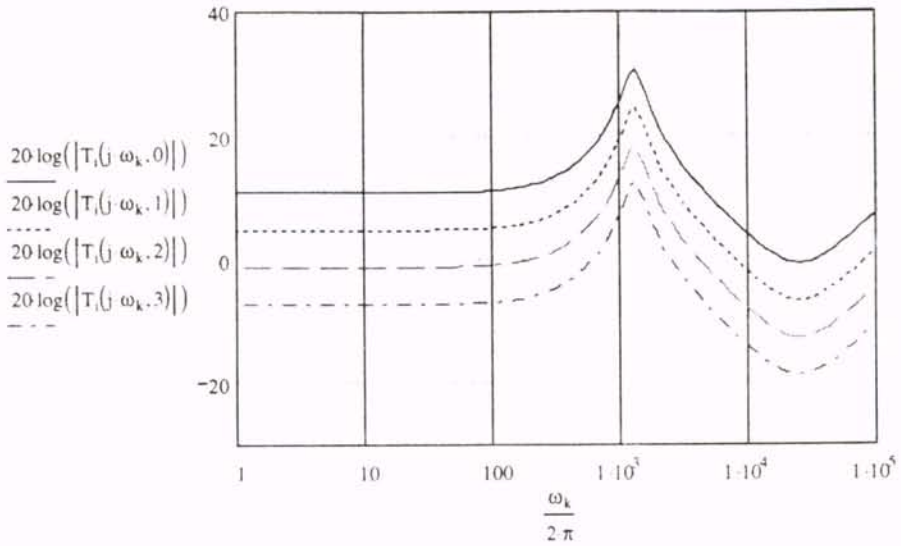
$kk := 0..5 \qquad m_{c_{kk}} := 2^{kk}$

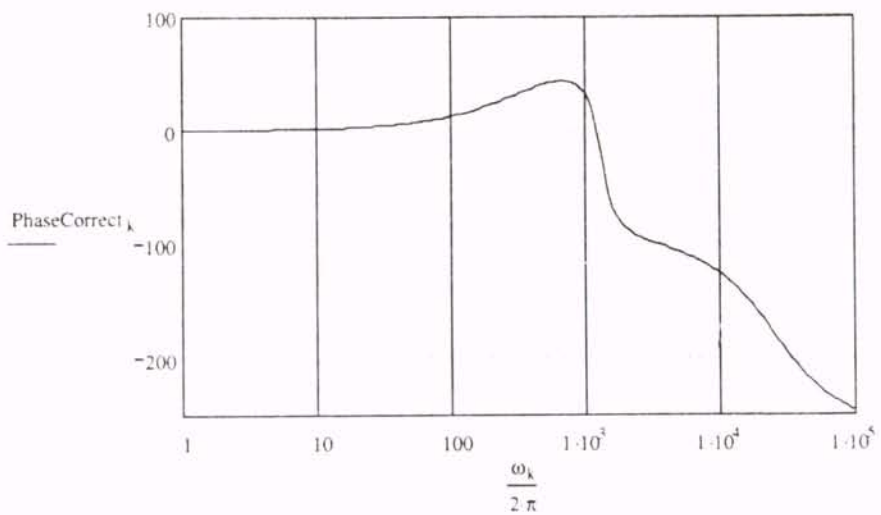
$T_i(s, kk) := \frac{L}{R \cdot D_{prime} \cdot T_s \cdot m_{c_{kk}}} \cdot \frac{1 + s \cdot R \cdot C}{Delta(s)} \cdot H_e(s)$

$k := 0..225 \qquad \omega_k := 10^{-1 + \frac{k}{25}}$

$RawPhase_k := \frac{\arg\left(T_i\left(j \cdot \omega_k, kk\right)\right)}{deg}$

$$PhaseCorrec_k := \begin{cases} \left(RawPhase_k\right) & \text{if } \left[\left(0 < RawPhase_k \le 180\right) \wedge \omega_k < 10^4\right] \\ RawPhase_k & \text{if } -180 \le RawPhase_k \le 0 \\ \left(RawPhase_k - 360\right) & \text{if } \left[\left(0 < RawPhase_k \le 180\right) \wedge \omega_k > 10^4\right] \end{cases}$$


40
20
0
-20
20·log(|T_i(j·ω_k,0)|)
20·log(|T_i(j·ω_k,1)|)
20·log(|T_i(j·ω_k,2)|)
20·log(|T_i(j·ω_k,3)|)
1
10
100
1·10^3
1·10^4
1·10^5
ω_k / 2π


100
0
-100
-200
PhaseCorrect_k
1
10
100
1·10^3
1·10^4
1·10^5
ω_k / 2π

Control to output Gain

$$kk := 0..5 \qquad m_{c_{kk}} := 2^{kk}$$

$$\omega_p(kk) := \frac{1}{C \cdot R} + \frac{T_s}{L \cdot C}\left(m_{c_{kk}} \cdot D_{prime} - 0.5\right)$$

$$F_p(s, kk) := \frac{1 + s \cdot C \cdot R_c}{1 + \frac{s}{\omega_p(kk)}}$$

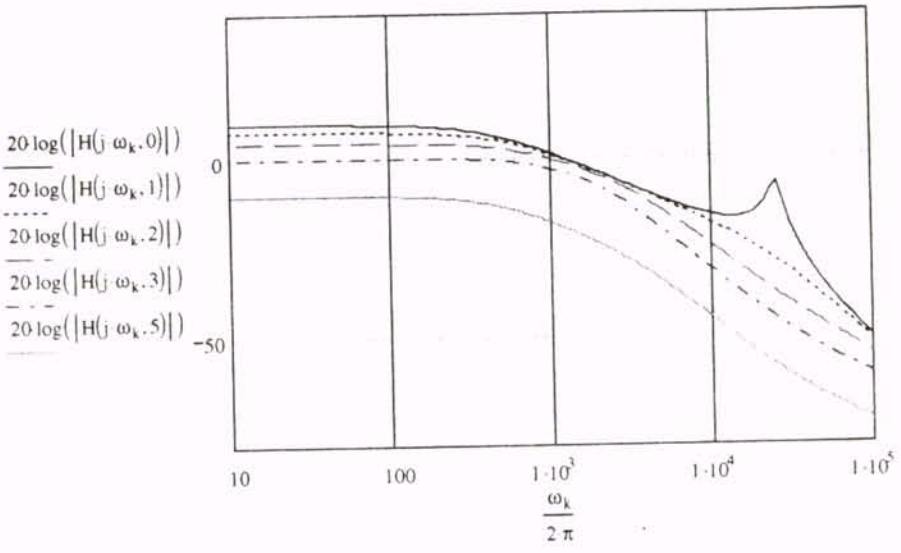
$$Q(kk) := \frac{1}{\pi \cdot \left(m_{c_{kk}} \cdot D_{prime} - 0.5\right)}$$

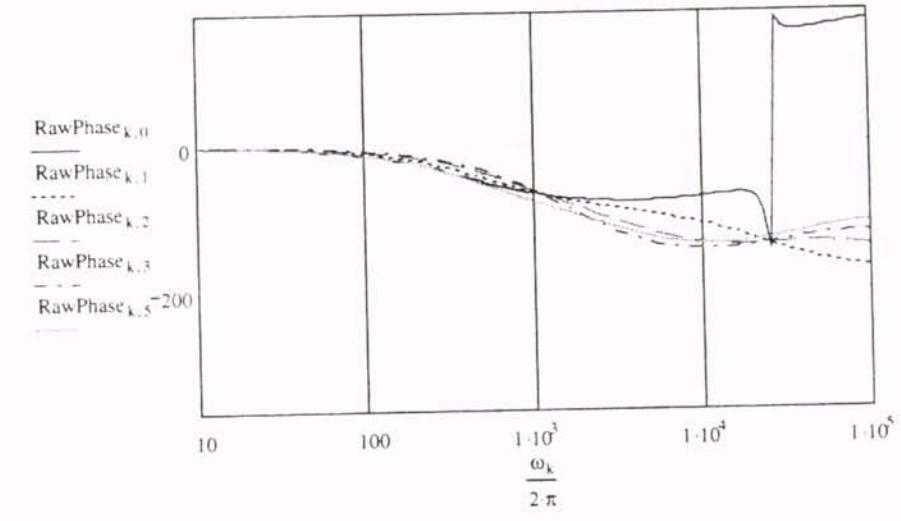
$$F_h(s, kk) := \frac{1}{1 + \frac{s}{\omega_n \cdot Q(kk)} + \frac{s^2}{\omega_n{}^2}}$$

$$k := 0..225 \qquad \omega_k := 10^{-1 + \frac{k}{25}}$$

$$H(s, kk) := \frac{R}{R_i} \cdot \frac{1}{1 + \frac{R \cdot T_s}{L}\left(m_{c_{kk}} \cdot D_{prime} - 0.5\right)} \cdot F_p(s, kk) \cdot F_h(s, kk)$$

$$RawPhase_{k,kk} := \frac{\arg\left(H\left(j \cdot \omega_k, kk\right)\right)}{deg}$$


20·log(|H(j·ω_k,0)|)
20·log(|H(j·ω_k,1)|)
20·log(|H(j·ω_k,2)|)
20·log(|H(j·ω_k,3)|)
20·log(|H(j·ω_k,5)|)
0
-50
10
100
1·10^3
1·10^4
1·10^5
ω_k / 2π


RawPhase_k,0
RawPhase_k,1
RawPhase_k,2
RawPhase_k,3
RawPhase_k,5
0
-200
10
100
1·10^3
1·10^4
1·10^5
ω_k / 2π

(3) Voltage Control

TWO POLE TWO ZERO COMENSATOR DESIGN:

Power converter component values:

$V_{in} := 48$ $f_s := 500000$ $R := 0.055$ $L := 2 \cdot 10^{-6}$

$n := \frac{1}{7}$ $C := 1000\ 10^{-6}$ $L_{lk} := 1 \cdot 10^{-6}$

$R_d := 4 \cdot n^2 \cdot L_{lk} \cdot f_s$ $\frac{R_d}{R} = 0.742$ $f_{esr} := 50000$ $f_{xo} := 100000.$ Crossover frequency

$$H(s) := \frac{n \cdot V_{in} \cdot \left(1 + \frac{s}{f_{esr} \cdot 2 \cdot \pi}\right)}{\left(s^2 \cdot L \cdot C\right) + s\left(\frac{L}{R} + R_d \cdot C\right) + \frac{R_d}{R} + 1}$$

$h_0 := 20 \cdot \log\left(\left|H\left(j \cdot 2\pi \cdot f_{xo}\right)\right|\right)$ simplify $\rightarrow -34.232468505174949769$ Gain of the control-to-output function at f_{xo}

Given

$$3 = 20 \cdot \log(H(0)) - 20 \log\left[\left|\frac{n \cdot V_{in} \cdot \left(1 + \frac{i \cdot f_{fp} \cdot 2\pi}{f_{esr} \cdot 2 \cdot \pi}\right)}{\left[\left(i \cdot f_{fp} \cdot 2\pi\right)^2 \cdot L \cdot C\right] + i \cdot f_{fp} \cdot 2\pi \left(\frac{L}{R} + R_d \cdot C\right) + \frac{R_d}{R} + 1}\right|\right]$$

Find(f_{fp})

$f_{fp} := 14043$ 3db frequency

Change the value manually(#1)

We have this in mind: the magnitude of the compensator gain at the crossover frequency is equal to 0.
Thus the overall gain is zero at the crossover.

$f_{z1} := \frac{f_{fp}}{5}$ $f_{z2} := 1.2 \cdot f_{fp}$ $f_{p1} := f_{esr}$ $f_{p2} := 1.5 \cdot f_{xo}$

$\omega_{z1} := 2 \cdot \pi \cdot f_{z1}$ $\omega_{z2} := 2 \cdot \pi \cdot f_{z2}$ $\omega_{p1} := 2 \cdot \pi \cdot f_{p1}$ $\omega_{p2} := 2 \cdot f_{p2} \cdot \pi$

$C_1 := 3.185 \cdot 10^{-9}$ $C_2 := 0.38 \cdot 10^{-9}$ $C_3 := 10 \cdot 10^{-9}$ $R_1 := 1 \cdot 10^{3}$ $R_2 := 11000$ $R_3 := 750$

Five equations for five unknows (Solver Function used to find component values from desired corner Frequencies)

Given

$$\omega_{p1} = \frac{1}{R_2 \frac{C_1 \cdot C_2}{C_1 + C_2}} \qquad \omega_{z1} = \frac{1}{R_2 \cdot C_2} \qquad \omega_{z2} = \frac{1}{(R_1 + R_3)\, C_3} \qquad \omega_{p2} = \frac{1}{R_3 \cdot C_3}$$

$$-20\log\left[\left|\frac{-1}{2} \cdot i \frac{(2 \cdot i \cdot R_2 \cdot \pi \cdot f_{x0} \cdot C_2 + 1)}{(\pi \cdot f_{x0})} \left[\frac{\left[2 \cdot i \cdot (R_3 \cdot C_3 + R_1 \cdot C_3) \cdot \pi \cdot f_{x0} + 1\right]}{\left[(2 \cdot i \cdot R_2 \cdot \pi \cdot f_{x0} \cdot C_2 \cdot C_1 + C_1 + C_2)(2 \cdot i \cdot R_3 \cdot \pi \cdot f_{x0} \cdot C_3 + 1) \cdot R_1\right]}\right]\right|\right] = h_0$$

$$A := \text{Find}(R_1, R_2, C_1, C_2, C_3, h_0)\ \text{simplify} \rightarrow \begin{bmatrix} 5652.3765621798811719 \\ \frac{(5.4345060128353252670 \cdot 10^{-5})}{C_2} \\ 6.2216122741197414991 \cdot 10^{-2} \cdot C_2 \\ C_2 \\ 1.4147106052612918735 \cdot 10^{-9} \\ 154.2128247077653946 - 4.3429448190325182765 \ln\left(\frac{1}{C_2^2}\right) \end{bmatrix}$$

Simplify the result:

Given

$h_0 = 154.2128247077653946 - 4.3429448190325182765 \ln\left(\frac{1}{C_2^2}\right)$ Change the value manually(#2

$\text{Find}(C_2) \rightarrow \left[-(3.7821203067804134068 \cdot 10^{-10})\ \ 3.7821203067804134068 \cdot 10^{-10}\right]$

$C_2 := 3.7821203067804134068 \cdot 10^{-10}$ Change the value manually(#3

$R_1 := A_0$

$C_3 := A_4$

$R_2 := \frac{(5.4345060128353252670 \cdot 10^{-5})}{C_2}$ Change the value manually(#4

$C_1 := 6.2216122741197414991 \cdot 10^{-2} \cdot C_2$ Change the value manually(#5

$R_1 = 5.652 \times 10^{3}$ $R_2 = 1.437 \times 10^{5}$ $C_1 = 2.353 \times 10^{-11}$ $C_2 = 3.782 \times 10^{-10}$ $C_3 = 1.415 \times 10^{-9}$

$$\omega_{z1} := \frac{1}{R_2 C_2} \qquad \omega_{p1} := \frac{1}{R_2 \frac{C_1 C_2}{C_1 + C_2}} \qquad \omega_{p2} := \frac{1}{R_3 C_3} \qquad \omega_{z2} := \frac{1}{(R_1 + R_3) C_3} \qquad G_o := \frac{1}{R_1 (C_1 + C_2)}$$

$\omega_{z1} = 1.84 \times 10^{4}$ $\omega_{p1} = 3.142 \times 10^{5}$ $\omega_{p2} = 9.425 \times 10^{5}$ $\omega_{z2} = 1.104 \times 10^{5}$ $G_o = 4.404 \times 10^{5}$

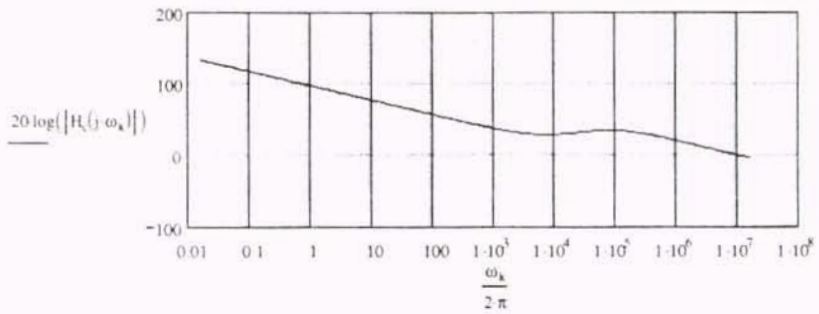
$$H_c(s) := G_o \frac{\left(\frac{s}{\omega_{z1}} + 1\right)\left(\frac{s}{\omega_{z2}} + 1\right)}{s\left(\frac{s}{\omega_{p1}} + 1\right)\left(\frac{s}{\omega_{p2}} + 1\right)}$$

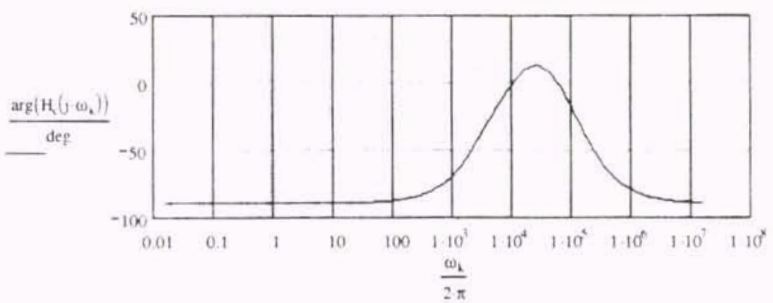
Note minus sign canceled by minus sign on summe in control loop.

$20 \log\left(\left|H_c(j \cdot f_{xo} \cdot 2\pi)\right|\right)$ simplify→ 34.232468505174949769

If this value is close to 0 then proceed.
If not, go back and change the value of C

$k := 0 .. 225$ $\omega_k := 10^{-1 + \frac{k}{25}}$





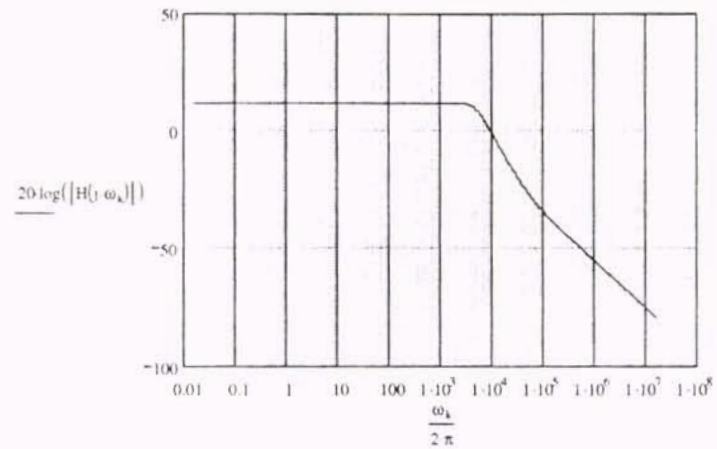
$$G_c(s) := G_o \frac{\left(\frac{s}{\omega_{z1}} + 1\right)\left(\frac{s}{\omega_{z2}} + 1\right)}{s\left(\frac{s}{\omega_{p1}} + 1\right)\left(\frac{s}{\omega_{p2}} + 1\right)} \text{ float, 4} \rightarrow 4.404 \cdot 10^{5} \left(5.435 \cdot 10^{-5} s + 1.\right) \frac{\left(9.058 \cdot 10^{-6} s + 1.\right)}{\left[s\left(3.183 \cdot 10^{-6} s + 1.\right)\left(1.061 \cdot 10^{-6} s + 1.\right)\right]}$$

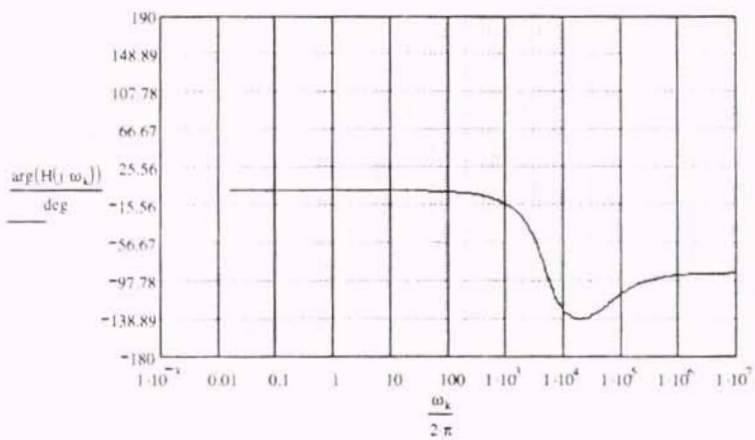
The following part: control-to-output transfer function, compensator transfer function and loop gain

Open Loop Control-to-output Transfer Function

$$H(s) := \frac{n \cdot V_{in}\left(1 + \frac{s}{50000 \cdot 2 \cdot \pi}\right)}{\left(s^2 \cdot L \cdot C\right) + s \cdot \left(\frac{L}{R} + R_d \cdot C\right) + \frac{R_d}{R} + 1}$$

$k := 0 .. 225 \qquad \omega_k := 10^{-1 + \frac{k}{25}}$





Compensator Transfer Function:

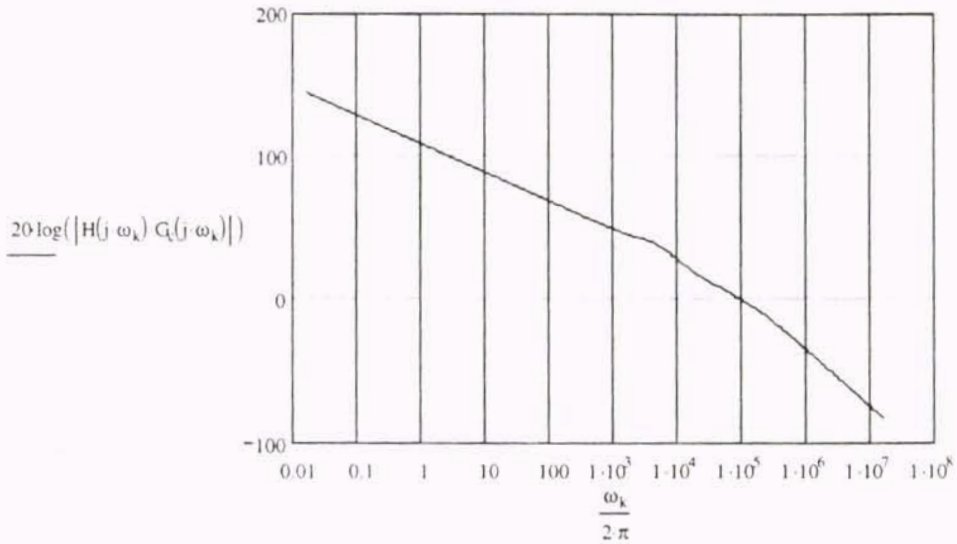
$$G_c(s)\ \text{float},4 \rightarrow \left(23.94 \cdot s + 4.404 \cdot 10^{5}\right) \cdot \frac{\left(9.058 \cdot 10^{-6} \cdot s + 1.\right)}{\left[s \cdot \left(3.183 \cdot 10^{-6} \cdot s + 1.\right) \cdot \left(1.061 \cdot 10^{-6} \cdot s + 1.\right)\right]}$$

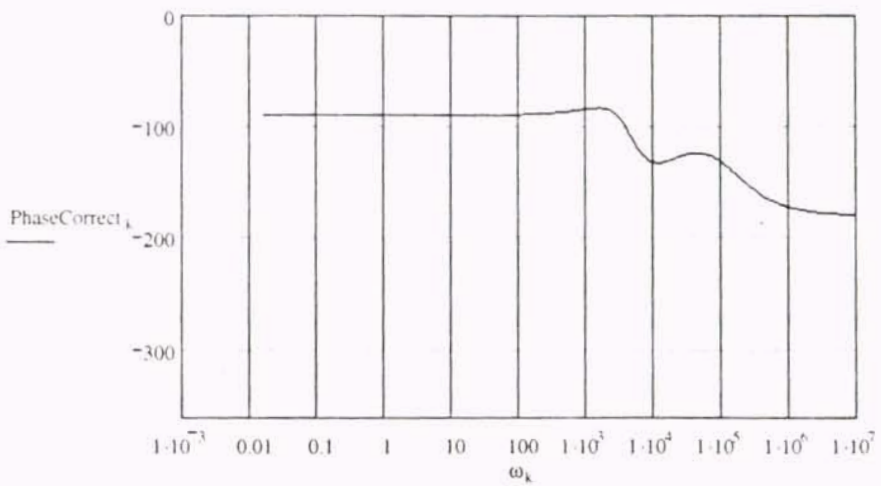
Loop Gain

$k := 0 .. 225 \qquad \omega_k := 10^{-1+\frac{k}{25}}$

$$\text{RawPhase}_k := \frac{\arg\left(H\left(j \cdot \omega_k\right) \cdot G_c\left(j \cdot \omega_k\right)\right)}{\text{deg}}$$

$$\text{PhaseCorrect}_k := \begin{cases} \text{RawPhase}_k & \text{if } -180 \le \text{RawPhase}_k \le 0 \\ \left(\text{RawPhase}_k - 360\right) & \text{if } 0 < \text{RawPhase}_k \le 180 \end{cases}$$





LIST OF REFERNCES

INTRODUCTION

[1] M. Zhang, M. Jovanovic and F.C. Lee, "Design Considerations for Low-Voltage On-board DC/DC Modules for Next Generations of Data Processing Circuits," IEEE Transactions on Power Electronics, Vol.11, No.2, March 1996.

[2] Xunwei Zhou, Xingzhu Zhang, Jiangang Liu, Pit-Leong Wong, Jiabin Chen, Ho-Pu Wu, Luca Amoroso, Fred C. Lee, and Dan Y. Chen, "Investigation of Candidate VRM Topologies for future Microprocessors," IEEE APEC '98 conf.

[3] Xunwei Zhou, "Low-Voltage High-Efficiency Fast Transient Voltage Regulator Modules", Ph.D. Dissertation, Virginia Polytechnic Inst. State Univ., Blackburg, 1999.

[4] A. Rozman and K. Fellhoelter, "Circuit Considerations for Fast Sensitive, Low-voltage Loads in a Distributed Power System," IEEE APEC'95 conf.

[5] W.A. Tabisz, M. M. Jovanovic, F. C. Lee, "Present and Future of Distributed Power System," APEC '92, pp. 11-18.

[6] R. Redl, "Power-factor Correction in single-phase switching-mode power supplies – an overview", INT. J. ELECTRONICS, 1994, vol 77, no. 5, 555-582.

[7] Guichao Hua, "Soft-switching Techniques for Pulse-width-modulated Converters". Ph.D. Dissertation, Virginia Polytechnic Inst. State Univ., Blackburg, 1994.

A NOVEL INTERLEAVED SYNCHRONOUS BUCK REGULATOR

[1] Xunwei Zhou, "Low-Voltage High-Efficiency Fast Transient Voltage Regulator Modules", Ph.D. Dissertation, Virginia Polytechnic Inst. State Univ., Blackburg, 1999.

[2] Rais Miftakhutdinov, "Analysis and Optimization of Synchronous Buck Converter at High Slew Rate Load Current Transients," in IEEE PESC 2000, pp.714-720.

[3] Brett A. Miwa, David M. Otten and Martin F. Schlecht, "High efficiency Power Factor Correction Using Interleaving Techniques," IEEE APEC'92, pp. 557-568.

[4] "Designing Fast Response Synchronous Buck Regulators Using the TPS 5210", Application Report, Texas Instrument, March 1999.

[5] "Synchronous Buck EVM Using the TPS5211", User's Guide, Texas Instrument, June 2000.

A NOVEL INTERLEAVED HALF-BRIDGE CONVERTER

[1] M. Zhang, M. Jovanovic and F.C. Lee, "Design Considerations for Low-Voltage On-board DC/DC Modules for Next Generations of Data Processing Circuits," IEEE Transactions on Power Electronics, Vol.11, No.2, March 1996.

[2] Xunwei Zhou, "Low-Voltage High-Efficiency Fast Transient Voltage Regulator Modules", Ph.D. Dissertation, Virginia Polytechnic Inst. State Univ., Blackburg, 1999.

[3] Keith billings, switchmode power supply handbook, McGraw-Hill, 1999, ISBN 0-07-006719-8.

[4] Wei Tang, Fred C. Lee, and Raymond B. Ridley, "Small Signal Modeling of Average Current-Mode Control", IEEE Trans. On Power Electronics, Vol. 8, No. 2, April 1993, pp. 112-119.

[5] R.B. Ridley, "A New, Continuous-Time Model for Current-Mode Control", Proceedings of the Power conversion and Intelligent Motion, October 16-19, 1989, pp. 455-464.

[6] David J. Perreault and George C. Verghese, "Time-Varying Effects and Averaging Issues in Models for Current-Mode Control", IEEE Trans. On Power Electronics, Vol. 12, No. 3, May 1997, pp. 453-461.

[7] J. Sun and R. Bass, "Modeling and Practical Design Issues for Average Current Control", IEEE Applied Power Electronics Conference, March 1999, pp. 980-986.

[8] Robert W. Erickson, " Fundamentals of Power Electronics", Chapman & Hall, 1997.

[9] Lloyd H. Dixon, "Average Current Mode Control of Switching Power Supplies", Unitrode Power Supply Design Seminar Manual, 1990.

[10] Philip Cooke, "Modeling Average Current Mode Control", IEEE Applied Power Electronics Conference, March 2000, pp. 256-262.

[11] R.D. Middlebrook, "Modeling Current-Programmed Buck and Boost Regulators", IEEE Trans. On Power Electronics, Vol. 4, No. 1, January 1989, pp. 36-52.

[12] Raymond B. Ridley, Bo H. Cho and Fred C. Lee, "Analysis and Interpretation of Loop Gain of Multiloop-Controlled Switching Regulations", IEEE Trans. On Power Electronics, Vol. 3, No. 4, October 1988, pp. 489-498.

LOW VOLTAGE PWM FB-ZVS DC/DC CONVERTER

[1] Yuri Panov and Milan M. Jovanovic, "Design and Performance Evaluation of Low-Voltage/High-Current Dc/Dc On-Board Modules", IEEE Applied Power Electronics Conf. Proc., Feb. 1999, pp. 545-552

[2] J. Sabate et al, Design consideration for high-voltage high-power full-bridge ZVS PWM converter, 1990 IEEE

[3] Laszle Balogh, "140W, multiple output, high density dc/dc converter", Unitrode Seminar 1200.

A NOVEL SOFT-SWITCHING SINGLE STAGE CONVERTER

[1] R. Redl, "Power-factor correction in single-phase switching-mode power supplies-an overview", Int. J. Electronics, Vol. 77, No. 5, 555-582, 1994.

[2] P. Kornetzky, H. Wei, G. Zhu and I. Bartarseh, "A Single-Switch AC/DC Converter with Power Factor Correction," Proceedings of PESC97, pp. 527-525,1997.

[3] G. Hua, C.S. Leu, Y. Jiang, and Fred C. Lee, "Novel Zero-Voltage-Transition PWM Converters," Proceedings of PESC92, pp. 55-61, 1992.

[4] J.P. Gegner and C. Q. Lee, "Zero-voltage-Transition Converters Using an Inductor Feedback Technique", Proceedings of PESC94, pp. 590-596, 1994.

[5] G. Zhu, H. Wei, P. Kornetzky, and I. Batarseh, "Small-signal Modeling of a Single-switch AC/DC Power-factor-correction Circuit", IEEE Transactions on power electronics. Vol. 14, No. 6, 1142-1148, November 1999.

[6] G.C. Hua, W.A. Tabisz, C.S. Leu, N. Dai, R. Watson, and F.C. Lee, "Development of a DC distributed power system", IEEE Applied Power Electronics Conf. (APEC) Proc., pp 763-769, 1994.

NEW SINGLE STAGE TOPOLOGY

[1] Chongming Qiao and Keyue M. Smedley, "A Topology Survey of Single-Stage Power Factor Corrector with a Boost Type Input-Current-Shaper," IEEE Applied Power Electronics Conf. (APEC) Proc., 2000.

[2] L. Huber and M. M. Jovanovic, "Single-Stage, Single-Switch, Isolated Power Supply Technique with Input-Current Shaping and Fast Output-Voltage Regulation for Universal Input-Voltage-Range Applications," Conference Record IEEE-APEC'97, pp.272-280.

[3] J. Qian, Q. Zhao, and F. C. Lee, "Single-Stage Single-Switch Power Factor Correction (S4-PFC) AC/DC Converters with DC Bus Voltage Feedback for Universal Line Applications," Conference Record of IEEE-Apec'98, pp. 223-229.

[4] Fu-Sheng Tsai, Peter Markowski, Eugene Whitcomb, "Off-Line Converter with Input Harmonic Current Correction", IEEE Applied Power Electronics Conf. (APEC) Proc., pp 120-124, 1996.

DATE DUE

NOV 25 2003

NOV 15 2003

Printed
in USA