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Ultra-Efficient Cascaded Buck-Boost Converter

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ULTRA-EFFICIENT CASCADED BUCK-BOOST CONVERTER

by

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ABSTRACT

This thesis presents various techniques to achieve ultra-high-efficiency for Cascaded-Buck-Boost converter. A rigorous loss model with component nonlinearities is developed and validated experimentally. An adaptive-switching-frequency control is discussed to optimize weighted efficiency. Some soft-switching techniques are discussed. A low-profile planar-nanocrystalline inductor is developed and various design aspects of core and copper design are discussed. Finite-element-method is used to examine and visualize the inductor design. By implementing the above, a peak efficiency of over 99.2 % is achieved with a power density of 6 kW/L and a maximum profile height of 7 mm is reported. This converter finds many applications because of its versatility: allowing bidirectional power flow and the ability to step-up or step-down voltages in either direction.

Dedicated to my family, friends and mentors

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Anirudh Pise

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CHAPTER 1 INTRODUCTION

Worldwide attention has been paid to the use of renewable energy because of the fast growth in energy consumption and pollution resulting from the conventional energy, such as coal and oil. In renewable energy and battery applications including photovoltaics (PV), a DC-DC buck/boost converter is commonly used to regulate the output voltage from a variable voltage source in order to maximize solar energy harvesting [1]. Among all the buck/boost converters, the bi-directional Cascaded Buck-Boost (CBB) converter can achieve the highest efficiency due to its low voltage and current stresses [2]. It is also a promising option for renewable energy system due to its low cost and high system level performance [3]. The bi-directional CBB converter is the core to interconnect the DC sources and energy storage devices as well as managing the power flow [4]. Because of unstable irradiation and shading on PV modules, improving efficiency at light load is advantageous [5-8]. Some methods have been developed in [9-12] to improve light load efficiency. However, the control circuits in [9,10,12] are too complex and the switching frequency cannot be predicted with the use of pulse frequency modulation technique. In addition, undesired switching noise may be generated [11]. In [13], variable switching frequency has been applied to a buck converter at light loads resulting in an efficiency improvement due to reduced gate driver losses, however, this technique is applied to a fixed input voltage. Power Electronic System Laboratory in ETH Zurich has proposed a novel method and control concept to ensure a Zero Voltage Switching (ZVS) on all semiconductor switches by determining a zero voltage across the power MOSFETs (Metal-

Oxide-Semiconductor-Field-Effect-Transistor) with analog comparators in order to improve the efficiency on bi-directional multi-phase cascaded buck-boost converter [14]. Nevertheless, the benefits of this method can only come out on high power applications.

In this thesis, an adaptive switching frequency technique is proposed to improve efficiency at both light loads and heavy loads. A detailed loss model including the effects of component nonlinearities for a CBB converter prototype is developed. For the prototype design, it was observed that the major losses were in the inductor. In order to mitigate the losses in the inductor, an optimum frequency is to be selected. The efficiency is seen to taper off when switching frequency deviates from the optimum value. The loss model is used to find the tradeoff between switching frequency and inductor current ripple so that the inductor core loss is minimized. Higher switching frequency increases MOSFET switching losses but reduces conduction losses due to lower inductor current ripple.

This thesis first introduces the cascaded buck-boost converter topology. A detailed power loss model that identifies the component nonlinearities is demonstrated in Chapter 2. According to the power loss model, the proposed adaptive switching frequency technique is presented by developing a numerical calculation algorithm in Chapter 3. The detailed experimental results are provided to verify the accuracy of the power loss model and reveal that the converter efficiency, especially the light load efficiency can be significantly improved by applying the proposed adaptive switching frequency technique.

In Chapter 4, Zero-Voltage-Transition Cascaded Buck-Boost Converter is discussed. Mode by mode analysis is done in both buck mode and boost mode. In Chapter 5, Nanocrystalline inductor design is discussed with finite element analysis. Lastly, Chapter 6, provides the conclusion and final remarks.

CHAPTER 2 CASCADED BUCK-BOOST CONVERTER LOSS MODELLING

2.1 Introduction

The well –known Cascaded Buck-Boost (CBB) converter topology is shown in Fig. 2-1 below. The converter can work bi-directionally in two modes: buck mode and boost mode. In forward direction (left to right), PV system is used to charge batteries and in reverse direction (right to left), the converter is allowed to operate any devices that would typically be powered from batteries. With the ability to reverse the operating direction and thereby the power transmission, the bi-directional cascaded buck-boost converter is being extensively used to achieve the power transfer between two DC sources in either direction.

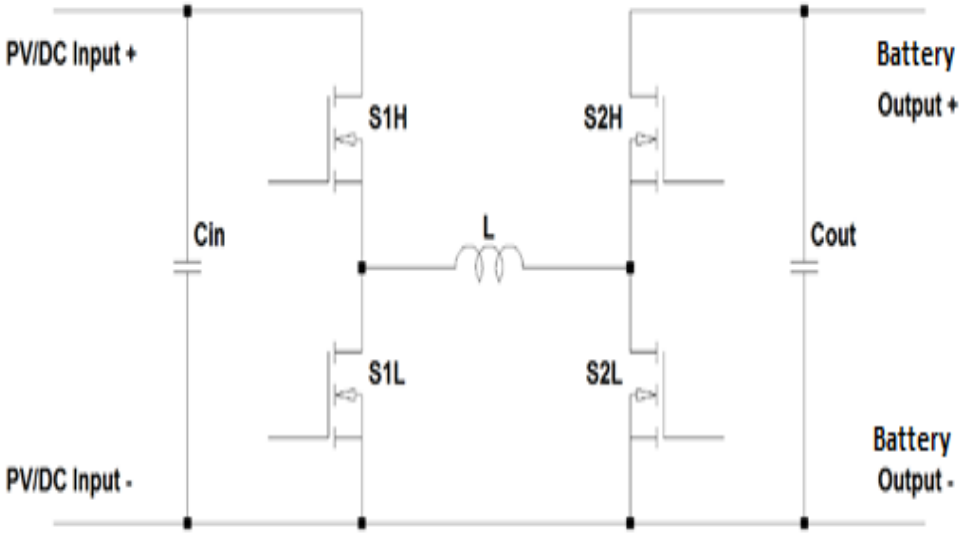

Figure 2-1 Cascaded Buck-Boost Converter

For simplicity, operation in the forward direction is described. In buck mode, S1H is the high side switch and S1L is the low side switch. S2H is kept at 100 % duty cycle and S2L

is kept at 0 % duty cycle. In boost mode, S2H is the high side switch and S2L is the low side switch. S1H is kept at 100 % duty cycle and S1L is kept at 0 % duty cycle. The operation in reverse direction is straightforward where the topology works in both buck and boost modes.

2.2 Power Loss Analysis

The high-frequency loss model consists of three sections: MOSFET losses, filter inductor losses, and filter capacitor losses. The MOSFET losses include turn-on loss, turn-off loss, conduction loss, parasitic capacitance loss, body diode loss and body diode reverse recovery loss. Filter inductor losses consist of core losses, AC winding loss, and DC winding loss. Filter capacitor losses are determined by ESR and RMS ripple current. These three loss models are demonstrated in Figs.2 -2 to Figs. 2-4.

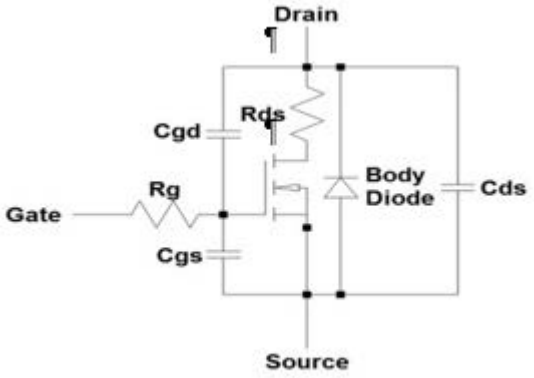

Figure 2-2 MOSFET Model

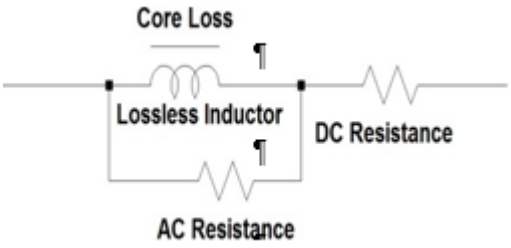

Figure 2-3 Inductor Model

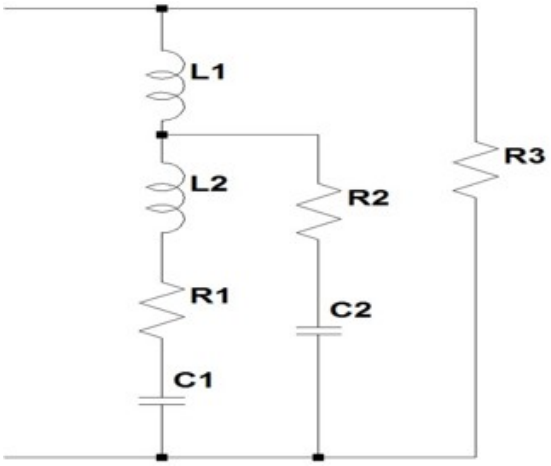

Figure 2-4 Capacitor Model

MOSFET turn-on and turn-off losses can be calculated as follows [15]:

$$\begin{cases} P_{turn-on} = 0.5 \times V \times I \times f_{sw} \times \left[-t_g \times \ln \dfrac{\left(1 - \frac{1}{g \times (V_{drive} - V_t)}\right)}{+V\left(\frac{R_{drive} C_{gd}}{V_{drive} - \left(V_t + \frac{1}{g}\right)}\right)} \right] \\ P_{turn-off} = 0.5 \times V \times I \times f_{sw} \times \left[V\left(\frac{R_{drive} C_{gd}}{V_t + \frac{1}{g}}\right) + t_g \times \ln \frac{\frac{1}{g} + V_t}{V_t} \right] \end{cases} \quad (2\text{-}1)$$

where V is the applied voltage across the drain-source of the MOSFET, I is the current through the MOSFET, f_{sw} is the switching frequency, t_g is the time constant, V_{drive} is gate

drive voltage, V_t is gate threshold voltage, R_{drive} is drive resistance, C_{gd} is gate to drain capacitance, and g is transconductance.

The dead-time between switching transition can lead to unnecessary power loss. It is the amount of time that both MOSFETs are off. During this period, the diode (body diode or parallel Schottky diode) is in forward conduction [16]. The power loss is given as:

$$P_{diode-deadtime} = V_F \times I \times f_{sw} \times t_{dead-time} \quad (2\text{-}2)$$

where V_F is the diode voltage drop and $t_{dead-time}$ is MOSFETs' dead time.

The dead time can be optimized to reduce conduction losses in MOSFET body diode [17]. The need for a Schottky diode in parallel with the MOSFET body diode (S1L MOSFET for Buck, S2H MOSFET for Boost) is eliminated with this technique since it provides no significant conduction loss benefits, and only serves to increase output parasitic capacitance of the switch ($C'_{\mathrm{DS}} = C_{\mathrm{DS}} + C_{\mathrm{Schottky}}$).

Parasitic capacitance loss and body diode reverse recovery loss are typically much smaller compared to turn-on and turn-off losses. Although their proportional influence on efficiency is low, they can still be significant due to where the dissipation occurs. They can be obtained by the following [16]:

$$P_{coss} = 0.5 \times C_{oss} \times V^2 \times f_{sw} \quad (2\text{-}3)$$

$$P_{qrr} = Q_{rr} \times V \times f_{sw} \quad (2\text{-}4)$$

where V is the drain-source voltage, C_{oss} is the MOSFETs output capacitance ($C_{ds} + C_{gd}$), and Q_{rr} is the body diode's reverse recovery charge.

In fact, MOSFET parasitic capacitances vary nonlinearly with drain to source voltage. These nonlinearities are modeled by using MATLAB to curve fit select points from the datasheet. Similar curve fitting is also performed to determine the equivalent series resistance (ESR) of the filter capacitor versus operating frequency.

The capacitor ESR loss is given as:

$$P_{cap-ESR} = ESR \times {I_{ac}}^2 \quad (2\text{-}5)$$

where I_{ac} is the RMS ripple current flowing through the capacitor.

Inductor losses include core loss and conduction loss. Core loss is determined by modified Steinmetz equation. Conduction loss can be calculated apart as AC winding loss and DC winding loss. DC winding loss can be obtained by a simple function of RMS current and inductor DC resistance. AC winding loss consists of skin effect loss and proximity effect loss, which are more complex to be calculated and they can significantly increase the inductor AC resistance. Inductor AC resistance is usually much larger than inductor DC resistance. In order to make calculation simpler and the loss model more accurate, inductor loss expressions are directly provided by the manufacturer [18-19]:

$$P_{core} = K_0 \times {f_e}^{K_f - 1} \times {B_{pk}}^{K_b} \times f_{sw} \times 10^{-14} \quad (2\text{-}6)$$

$$P_{AC} = K_1 \times {I_{ac}}^2 \times \sqrt{f_{sw}} \times R_{oper} \quad (2\text{-}7)$$

$$P_{DC} = {I_{dc}}^2 \times R_{oper} \quad (2\text{-}8)$$

where K_0 is core constant, K_1 is AC loss constant, K_f is frequency constant, K_b is flux density constant, f_e is effective frequency, B_{pk} is peak flux density and R_{oper} is operational resistance.

Inductor linear curve fitting is used during numerical calculation to determine filter inductance versus current. These fitted curves are used by the loss model for accurate loss prediction and these modeled losses are used in selecting the optimum switching frequency which corresponds to lowest total loss. The various non-linear behavior is as shown in Figs. 2-5 to Figs. 2-7.

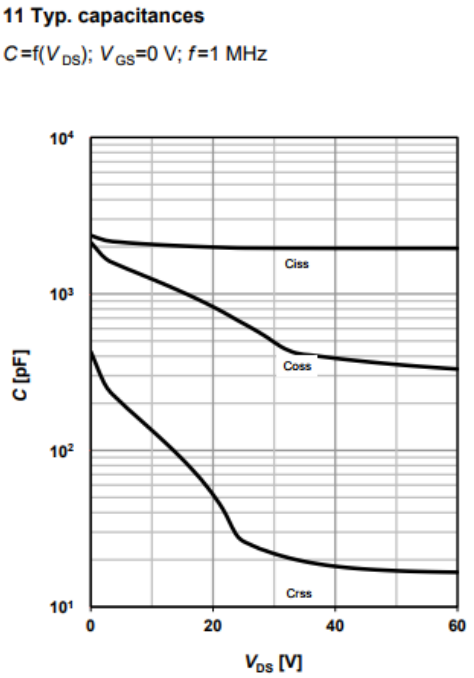

Figure 2-5 MOSFET Capacitance non-linearity with Drain Source Voltage [24]

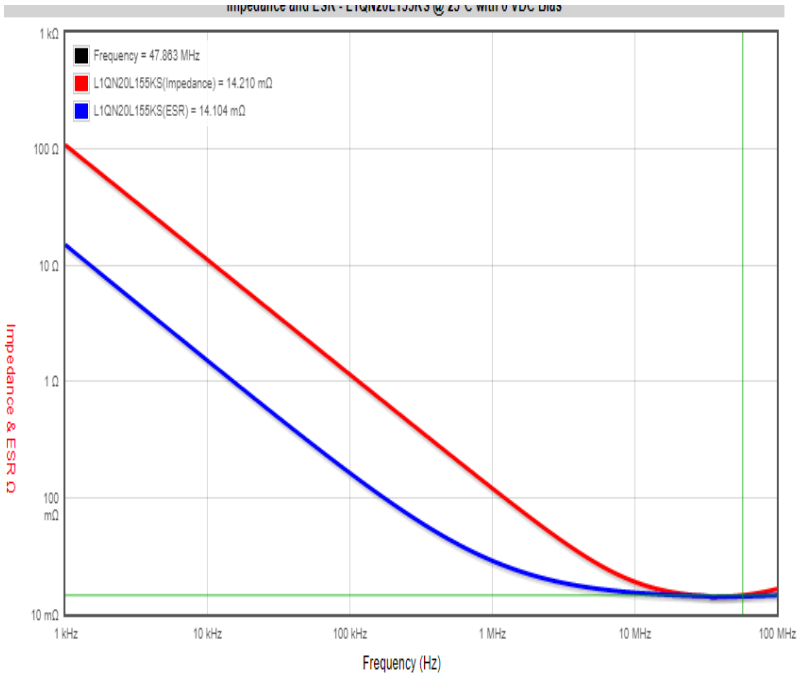

Figure 2-6 Capacitor Impedance and ESR non-linearity with frequency [25]

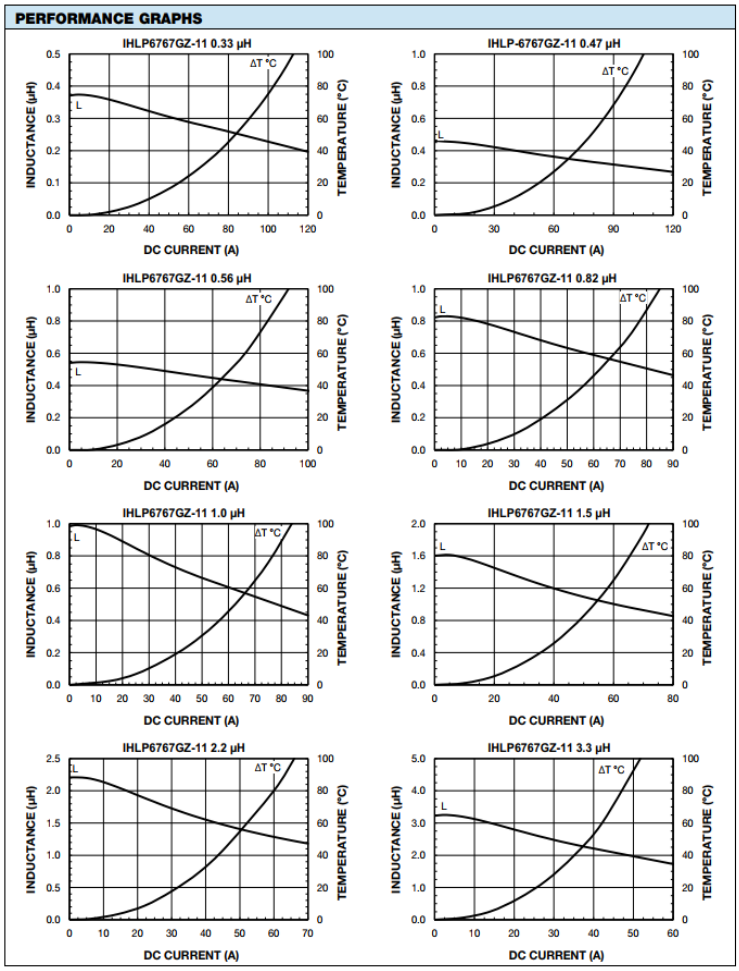

Figure 2-7 Inductance non-linearity with DC current [26]

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CHAPTER 3 ADAPTIVE SWITCHING FREQUENCY TECHNIQUES

3.1 Introduction

In [20], it demonstrates that switching losses are dominant at light loads while conduction losses are dominant at heavy loads under fixed switching frequency. Lower switching frequency can result in lower MOSFET switching loss and driving loss. What's more, switching loss and driving loss are increasing with increasing switching frequency while conduction losses will decrease due to lower RMS and ripple currents. However, conduction loss will increase with the increase of load current. Therefore, it is significant to find the tradeoff between switching frequency and load current. Also, according to the loss model, it can be deduced that there exists a strong correlation between switching frequency and total losses. Nevertheless, the optimal switching frequency that achieves the lowest total loss is related to many nonlinear parameters that will make the optimal switching frequency different at different loads. Fig. 3-1 shows that for different load current in CBB converter, there exists an optimal switching frequency range leading to maximum efficiency.

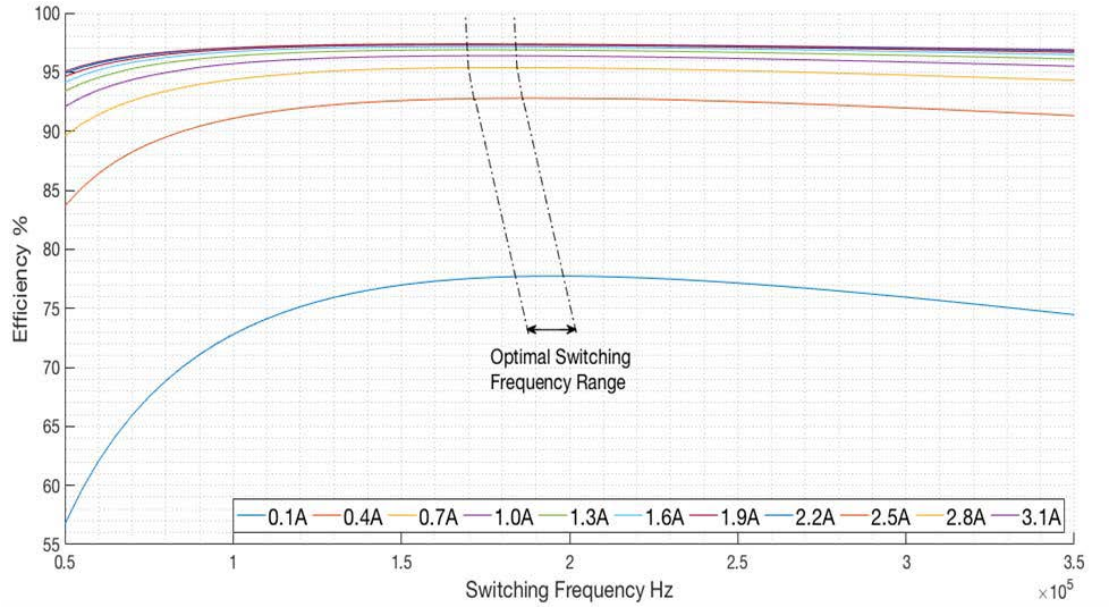

Figure 3-1 Optimized switching frequency range at different loads

3.2 Adaptive Switching Frequency Technique

An adaptive switching frequency technique that adjusts the switching frequency within a certain range is proposed to achieve the optimized switching frequency by taking those nonlinear parameters into consideration. Fig.3-2 shows the algorithm to find the optimal switching frequency. Since the proposed CBB converter has variable input voltage, the algorithm will consider the influence of input voltage as well.

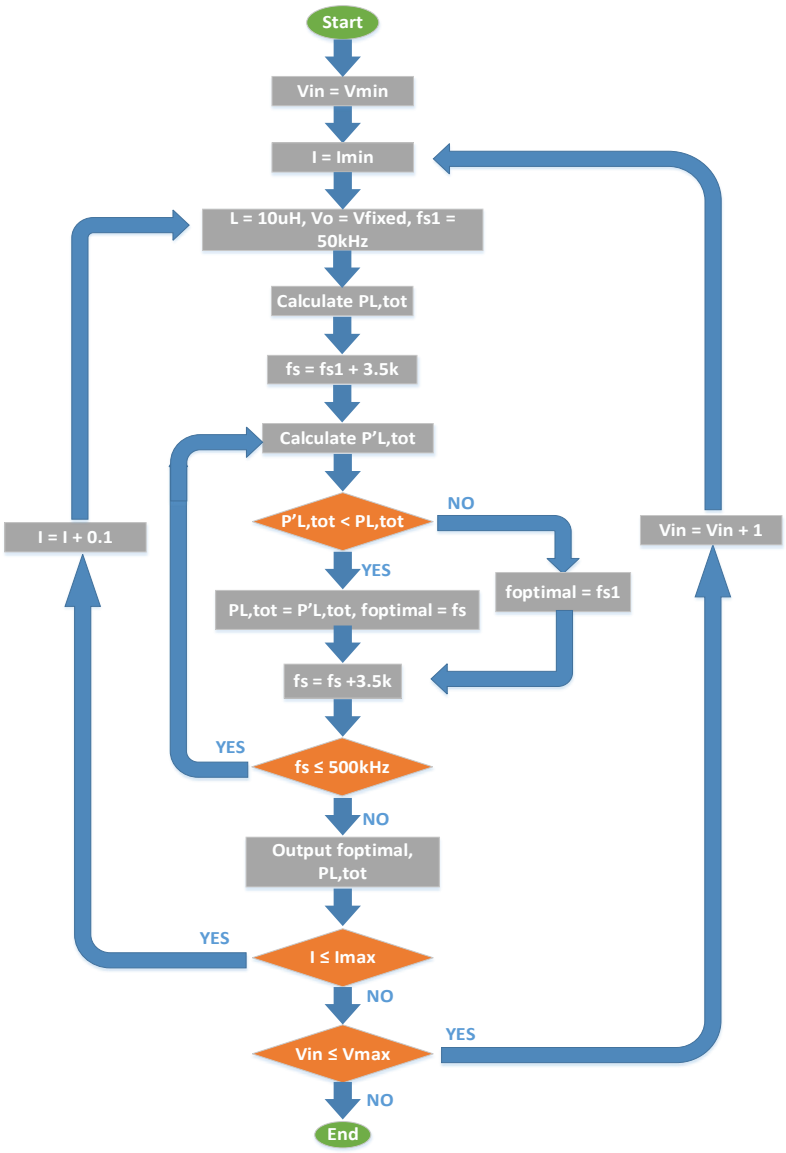

Figure 3-2 Optimal frequency estimation algorithm

The program starts from the minimum current point under each certain input voltage. $P_{L,tot}$ (total loss) is used as an indication of the converter efficiency because the maximum efficiency occurs when the total loss is minimized. The total loss at minimum switching frequency is used to work as the base point and 3.5kHz is selected as the switching

frequency adjusting step to calculate the new total loss. The program will automatically compare the difference between the new total loss and the previous total loss. If the new total loss is smaller, it will replace the previous total loss and be stored as new base point and the relevant switching frequency will be stored as the optimal switching frequency. After storing the value of new total loss and switching frequency, the program will increment f_{sw} and update it. If the new total loss is larger, the program will directly pass it and proceed to next switching frequency. The comparison will repeat until the switching frequency loop is finished, and then it will go to next current rate and repeat the same process. The progress will be repeated until all the variables reach the maximum values. For further improvement of efficiency, the algorithm also considers the converter switching between DCM mode and CCM mode based on the load. During the calculation, when the algorithm detects that the inductor current minimum point reaches zero, it will force the converter to operate in DCM mode. Operating in DCM at light load can prevent inductor current from going negative. This will help to reduce the conduction loss and lead to lower switching loss because the synchronous diode can be turned off at zero current.

MOSFET loss, inductor loss and capacitor loss in the proposed CBB converter were calculated for buck mode and boost mode individually. For the buck mode, the switching frequency was varied from 50 kHz to 500 kHz and the losses were computed with input voltage ranging from 25 V to 60 V and output current ranging from 0.1A to 6 A with the output voltage fixed at 15 V. The switching frequencies corresponding to lowest losses were determined as shown in Fig. 3-3.

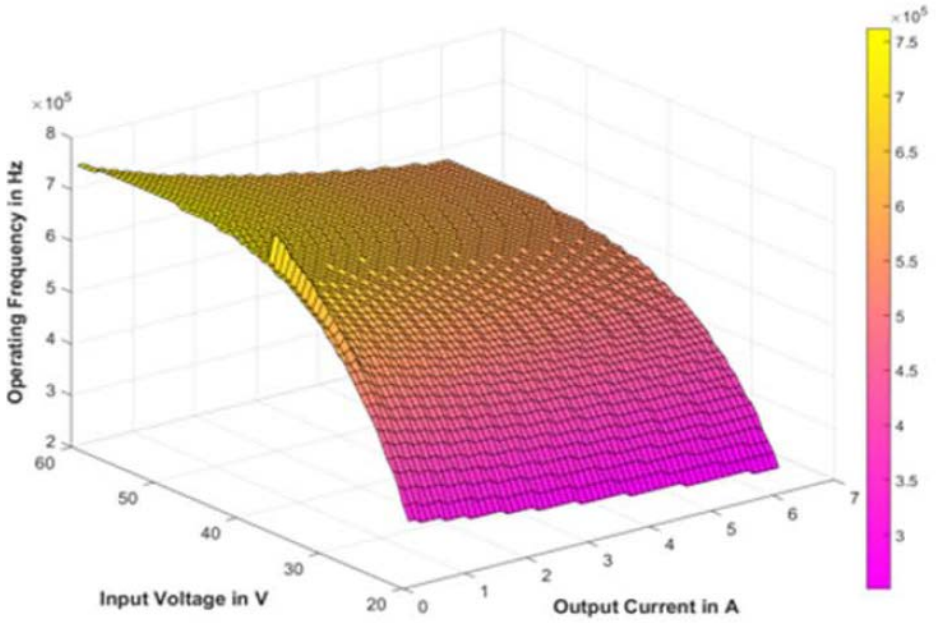

Figure 3-3 Optimized switching frequency with varying input voltage and load for buck mode

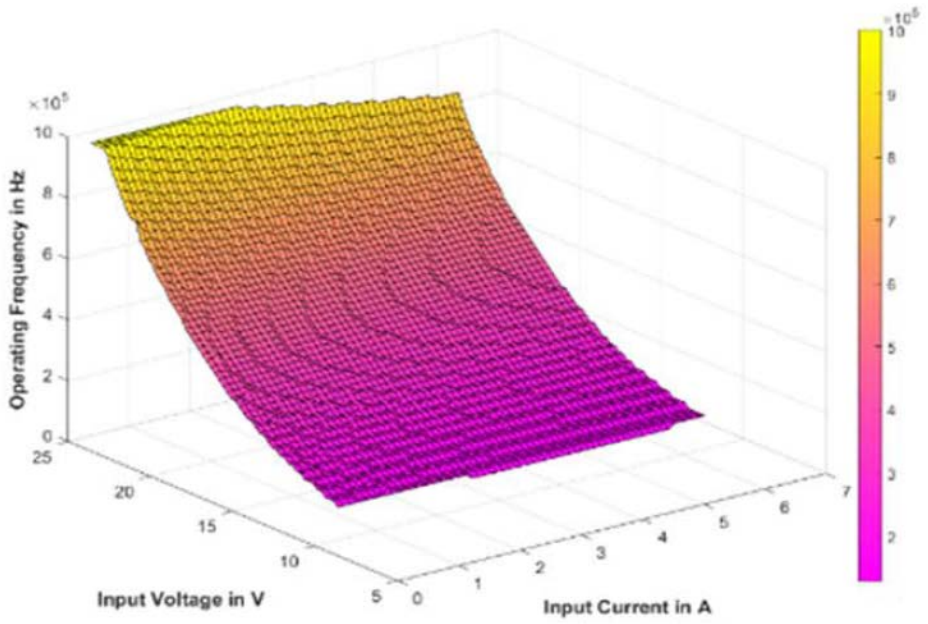

Figure 3-4 Optimized switching frequency with varying input voltage and load for boost mode

The same process was repeated for boost mode, where the switching frequency was varied from 50 kHz to 500 kHz and the losses were computed with an input voltage ranging from 9V to 24V and input current ranging from 0.1A to 6A with the output voltage fixed at 33 V. The optimum frequency for boost mode is shown in Fig. 3-4. The losses for both modes with standard PWM and with optimized frequency are shown in Fig. 3-5 to Fig. 3-8.

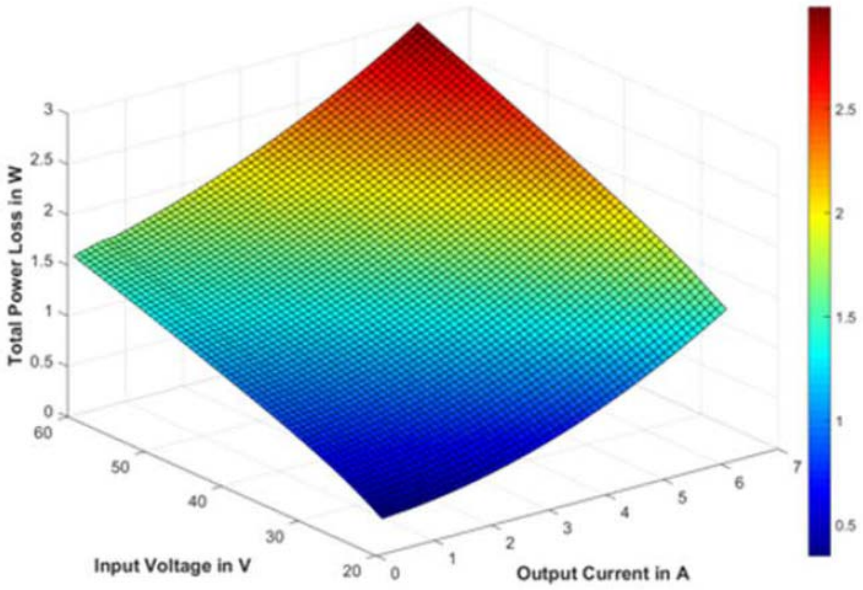

Figure 3-5 Total power loss at optimized frequency with varying input voltage and load for buck mode

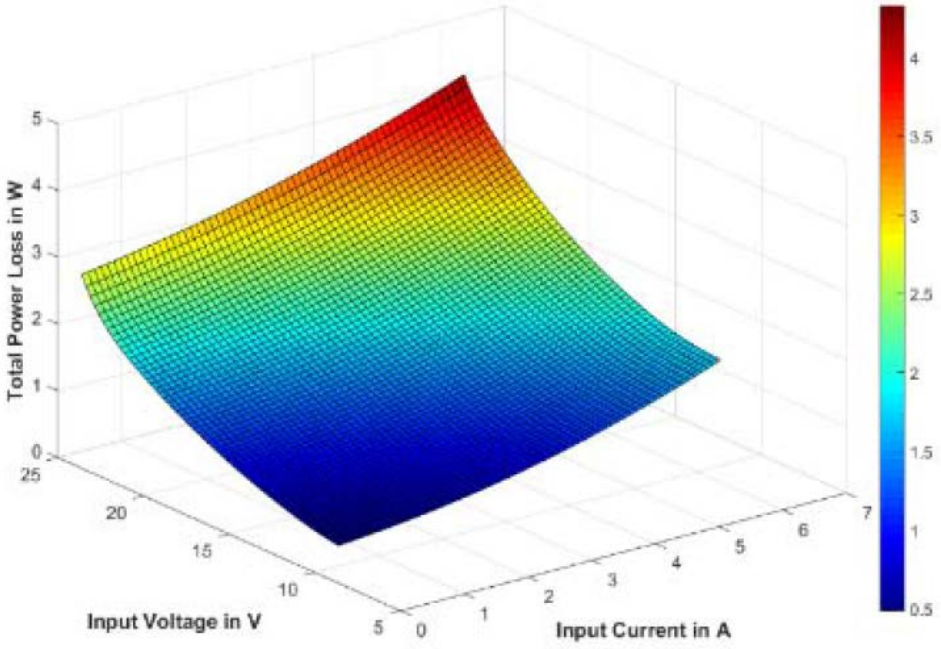

Figure 3-6 Total power loss at optimized frequency with varying input voltage and load for boost mode

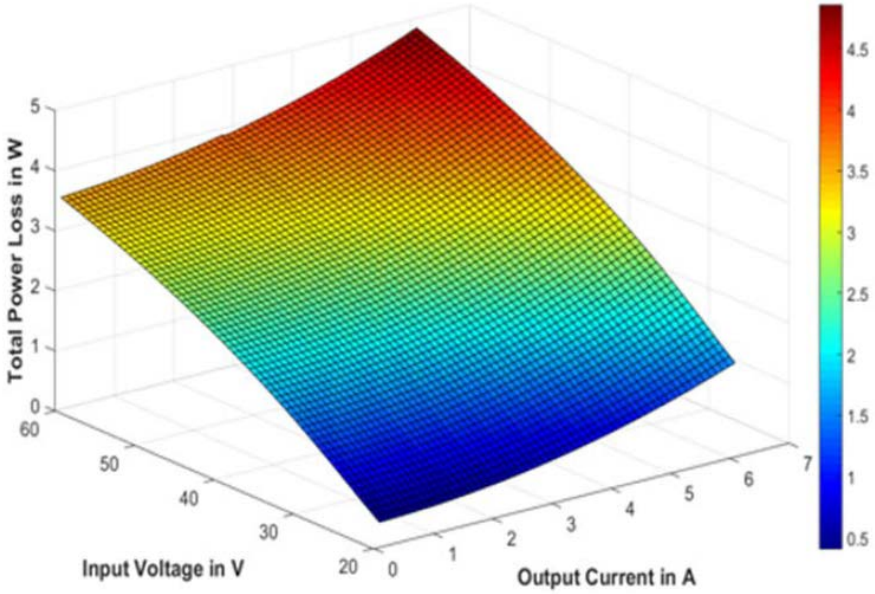

Figure 3-7 Total power loss at 100 kHz frequency with varying input voltage and load for buck mode

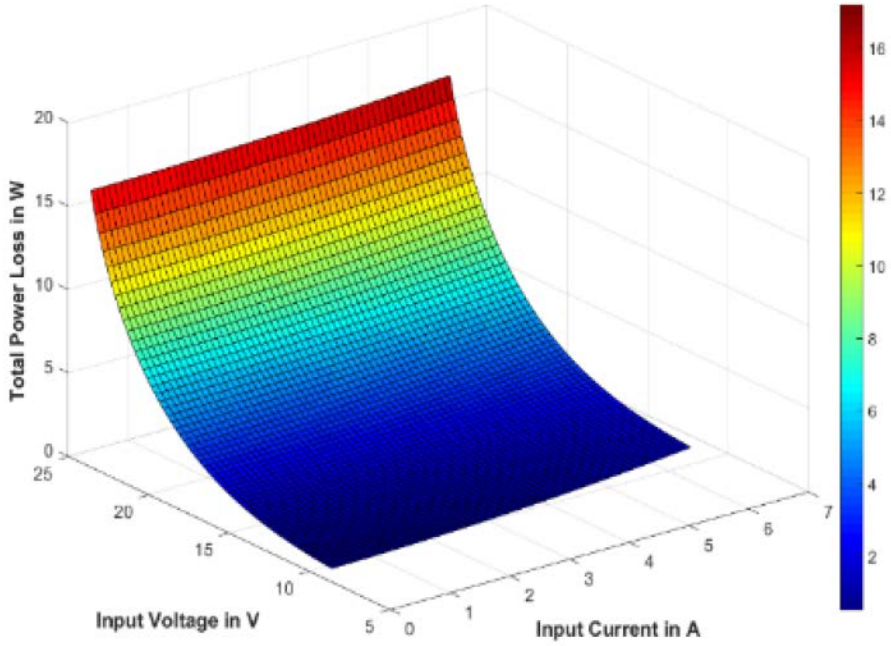

Figure 3-8 Total power loss at 100 kHz frequency with varying input voltage and load for boost mode

3.3 Experimental Results

To verify the frequency selection technique, a 100 W CBB converter prototype has been built and tested in the laboratory. Table 1 shows the final designed parameters and selected components of the prototype based on the design specifications. The adaptive switching frequency technique is realized with the help of software called “ApECOR Interface Suite v1.90”. The software can automatically run the desired optimal switching frequency obtained from the Matlab code. Experimental measurements were first made in buck mode with three different input values: 25 V, 35 V and 40 V; and fixed 15 V output voltage over the entire 100 W range with 100 kHz constant frequency and with the adaptive switching frequency technique discussed above.

Table 3-1:Experimental Details

Parameter	Value	Description
L	$2 \times 10\mu H$	IHLP-6767GZ-11
C_{in}, C_{out}	$33\mu F$	50V Ceramic Capacitor
$S1H, S1L. S2H, S2L$	BSC028N06NS	$60V/100A\ \ R_{ds_{on}} = 2.8m\Omega$
DSC	dsPIC33EP64MC506	High-speed Current-mode PWM Controller

The optimal switching frequency versus output power for each case in buck mode is shown in Fig. 3-9 to Fig. 3-11.

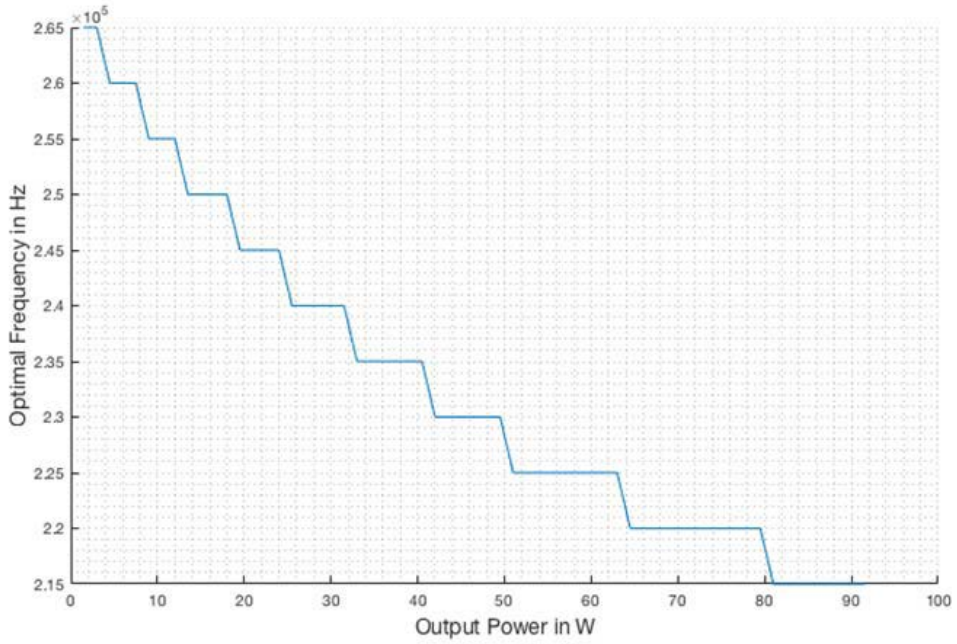

Figure 3-9 Frequency vs output power at 25V input and 15 V output

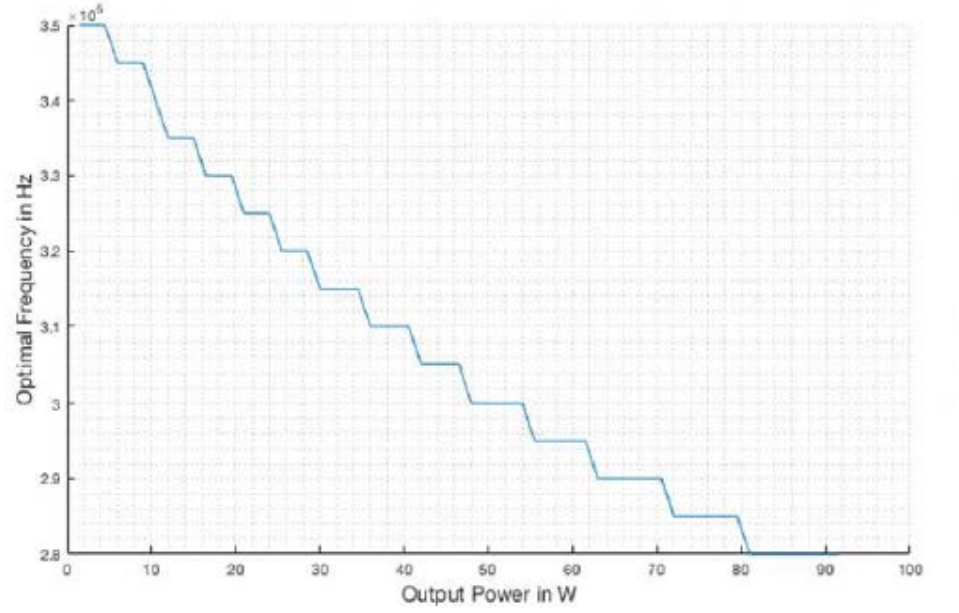

Figure 3-10 Frequency vs output power at 35 V input and 15 V output

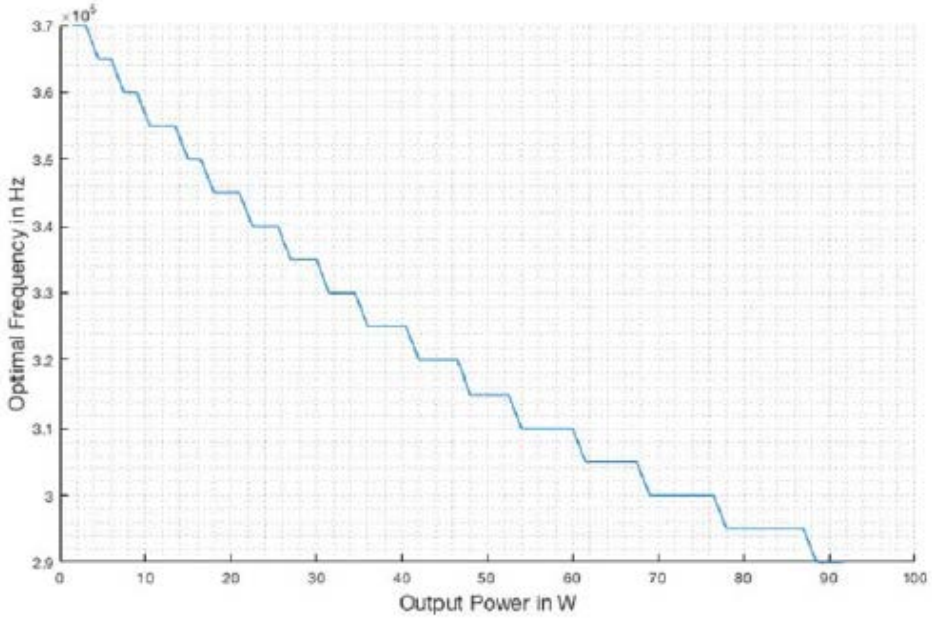

Figure 3-11 Frequency vs output power at 40 V input and 15 V output

From Fig. 3-12 to Fig. 3-14, it is obvious that the measured losses matched the theoretical prediction and a great efficiency improvement at light load can be noted. With higher input voltage (smaller duty cycle), the efficiency improvement is more significant. The same process for boost mode has been repeated with three different input values at 12 V, 16.5 V and 20 V; and fixed 33 V output voltage over the entire 100 W range with 100 kHz constant frequency and with the adaptive switching frequency technique.

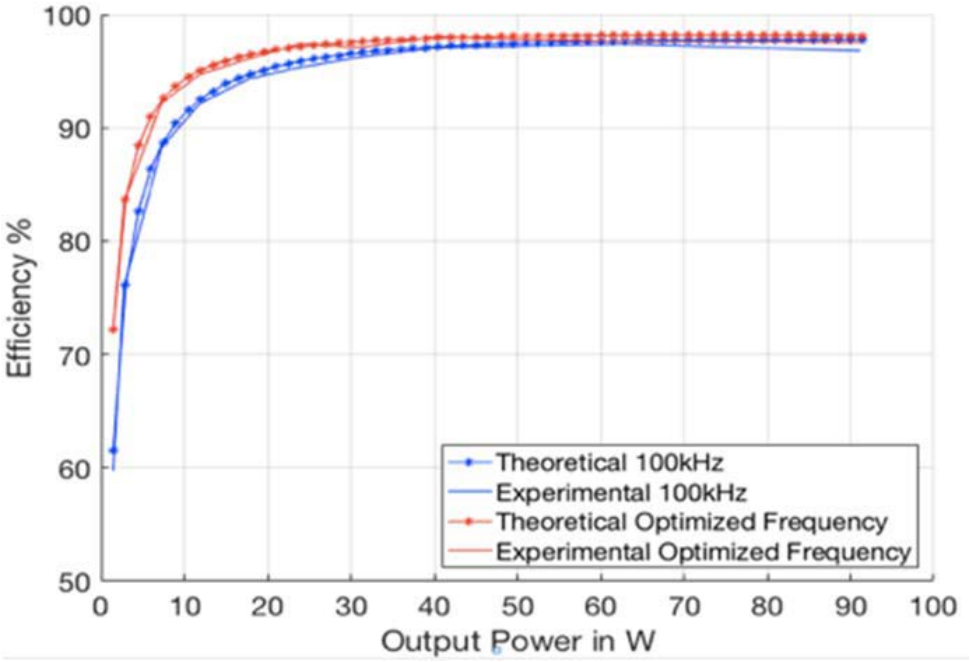

Figure 3-12 Theoretical and experimental efficiency at 25 V input and 15 V output

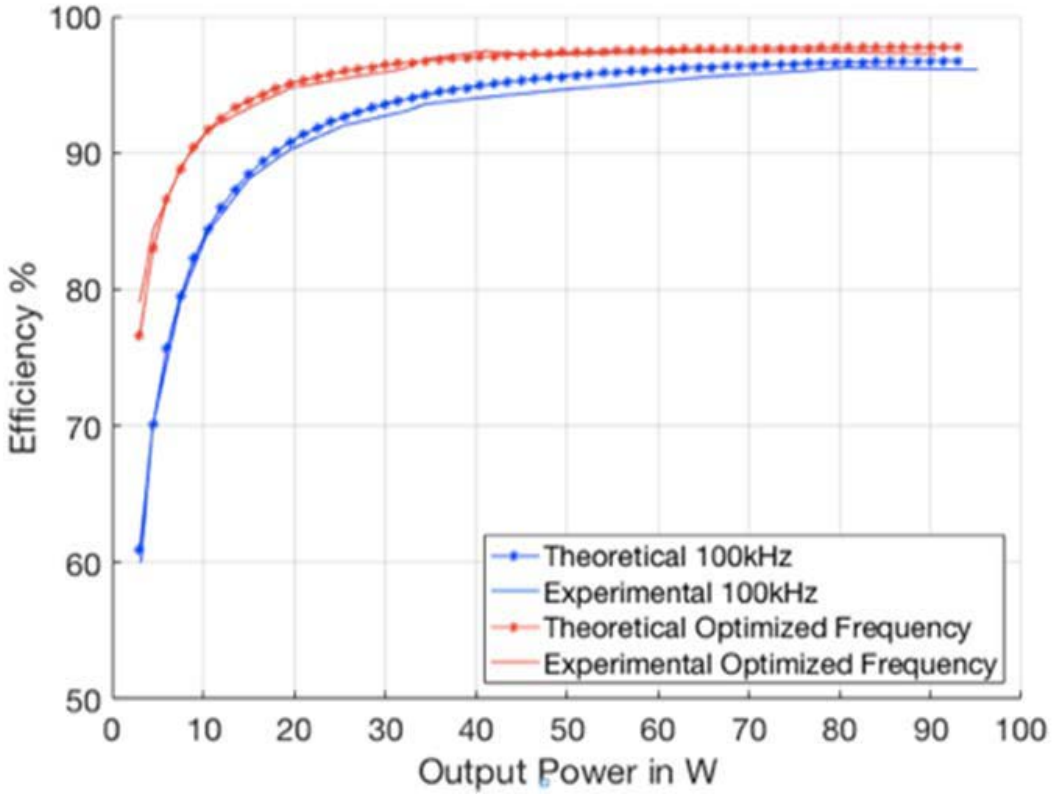

Figure 3-13 Theoretical and experimental efficiency at 35 V input and 15 V output

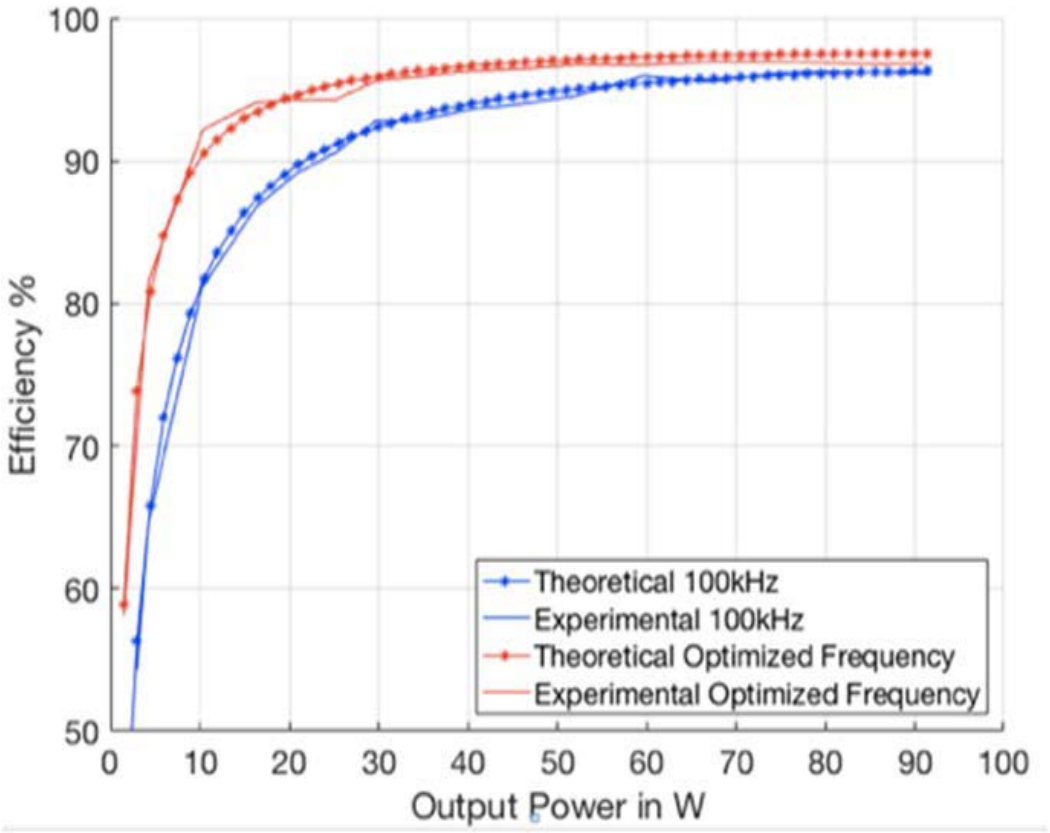

Figure 3-14 Theoretical and experimental efficiency at 40 V input and 15 V output

Fig. 3-15 to Fig. 3-17 shows the optimal switching frequency at each power point for three cases in boost mode. From Fig. 3-18 to Fig. 3-20, it is apparent that the experimental results were close to the theoretical analysis and a great light load efficiency improvement can be noticed. The higher the input voltage is duty cycle), the more efficiency improvement will be achieved. To verify the optimal switching frequency obtained from the above-mentioned techniques gives the highest operating efficiency, experimental measurements were performed at the frequencies slightly lower (-3.5 kHz) and higher (+3.5 kHz) than the optimal switching frequency for the cases when input voltage is 35 V and output voltage is 15 V for buck mode and when input voltage is 16.5 V and output voltage is 33 V for

boost mode. It was observed from both cases that efficiency began to drop with deviation from calculated optimal switching frequency as shown in Fig. 3-21 and Fig. 3-22.

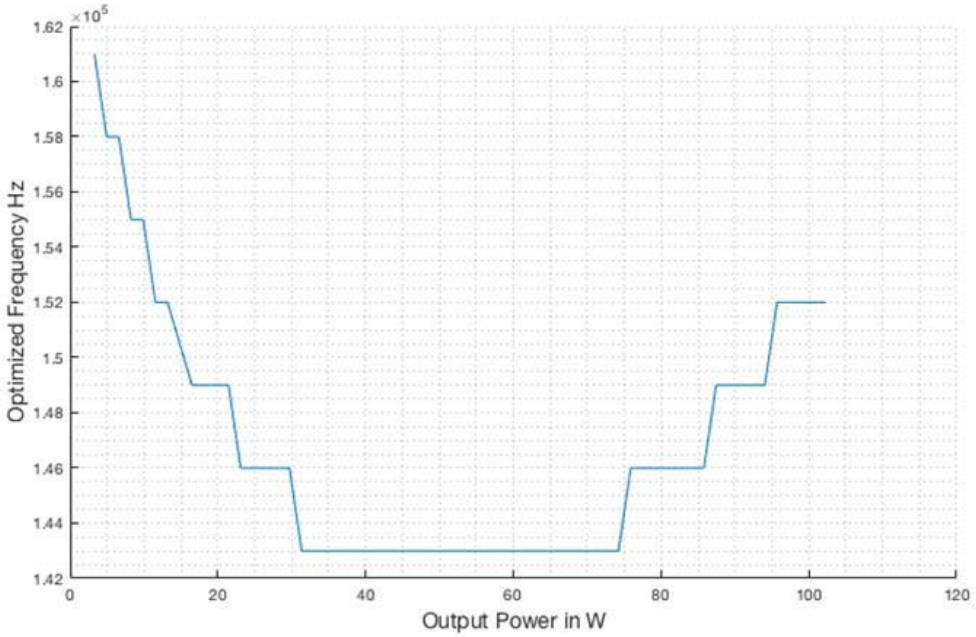

Figure 3-15 Frequency vs output power at 12 V input and 33 V output

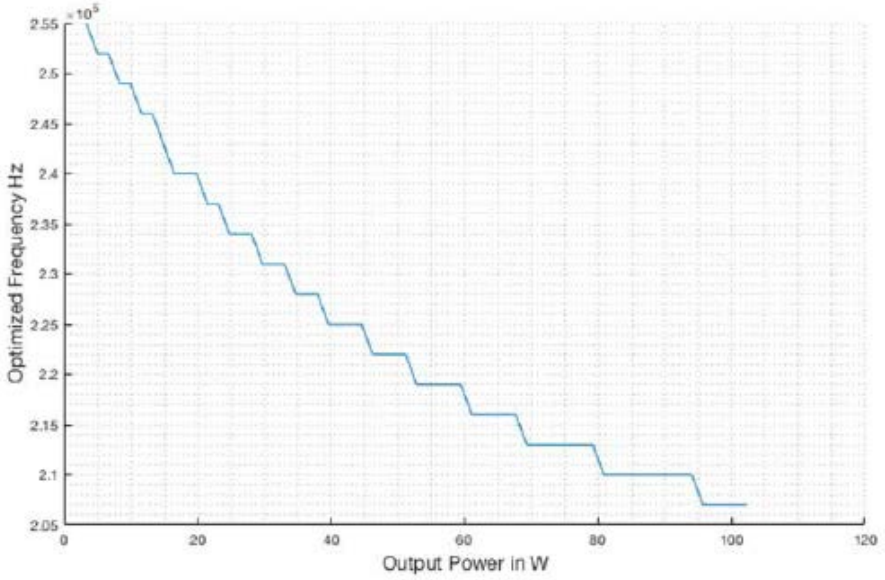

Figure 3-16 Frequency vs output power at 16.5 V input and 33 V output

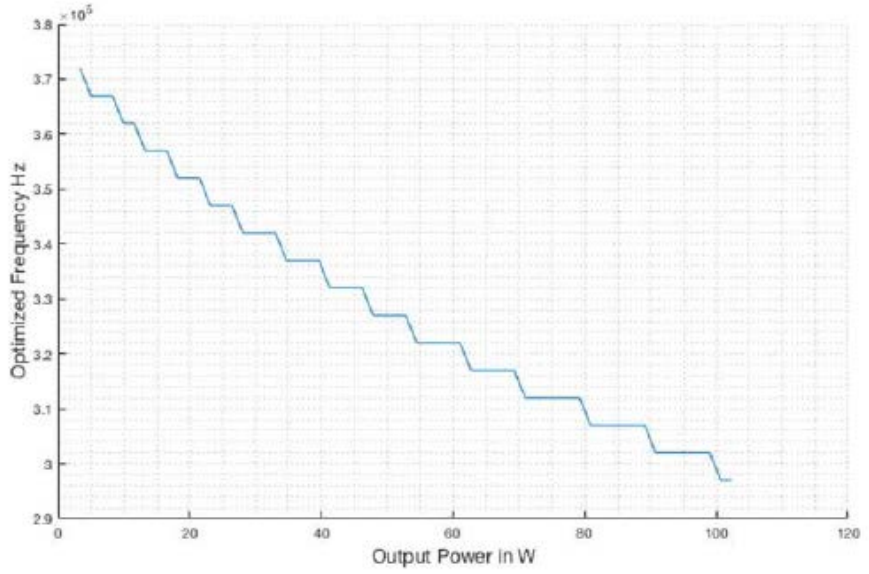

Figure 3-17 Frequency vs output power at 20 V input and 33 V output

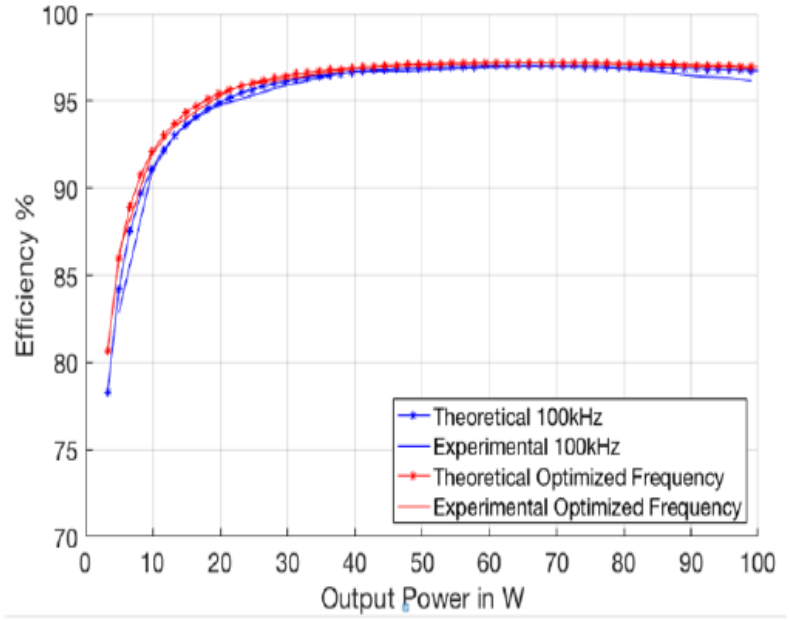

Figure 3-18 Theoretical and experimental efficiency at 12 V input and 33 V output

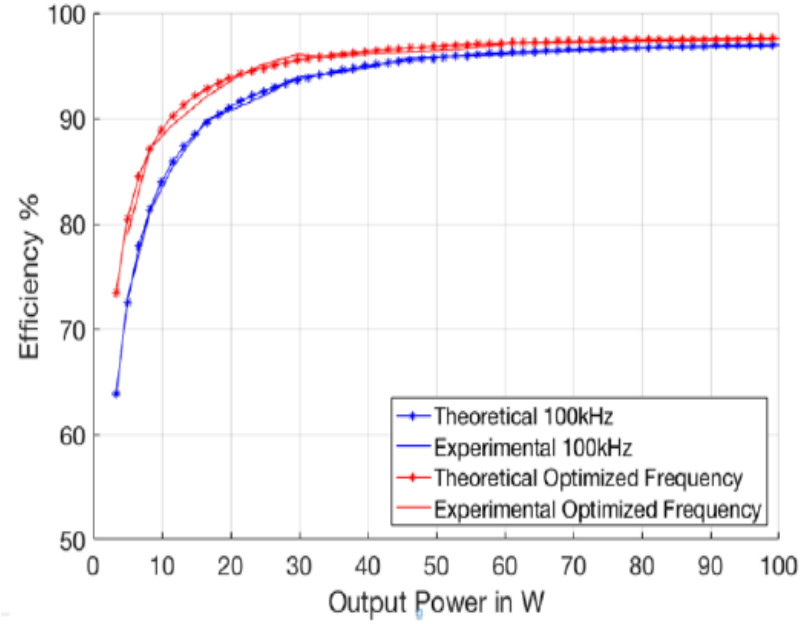

Figure 3-19 Theoretical and experimental efficiency at 16.5 V input and 33 V output

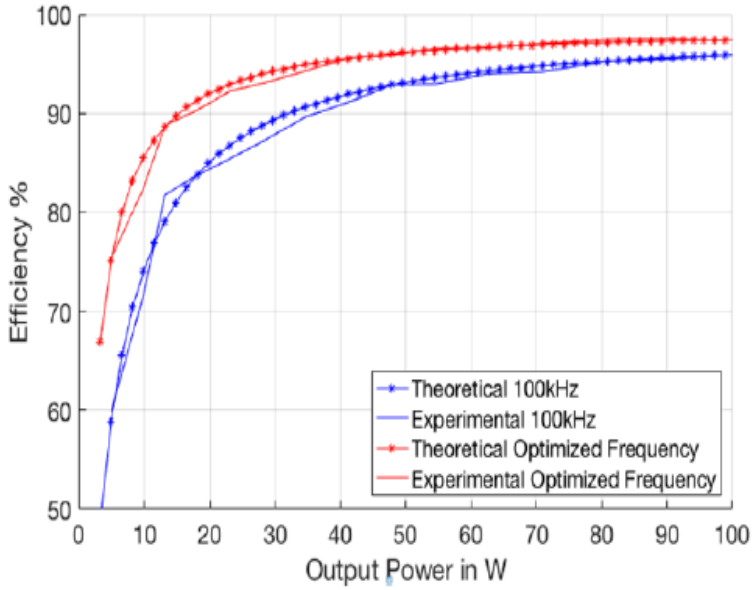

Figure 3-20 Theoretical and experimental efficiency at 20 V input and 33 V output

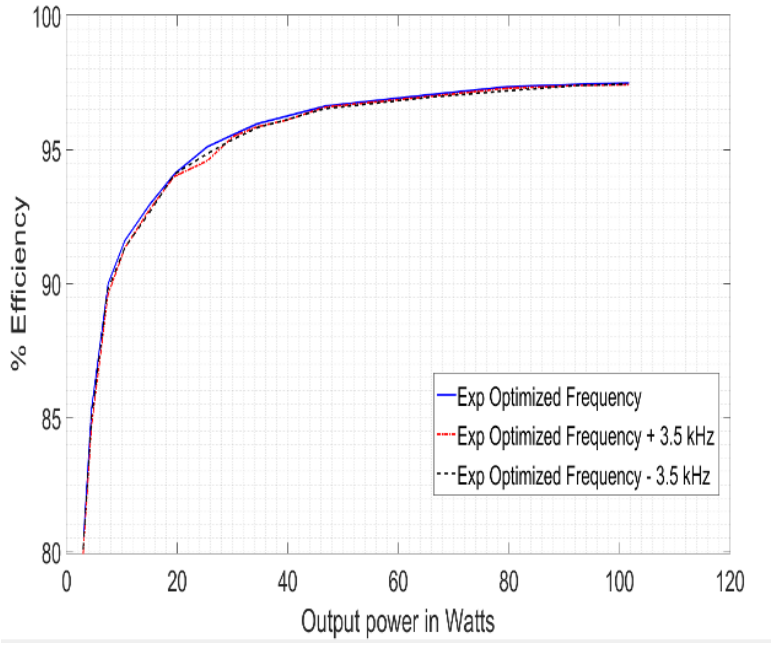

Figure 3-21 Test of optimal frequency in buck mode

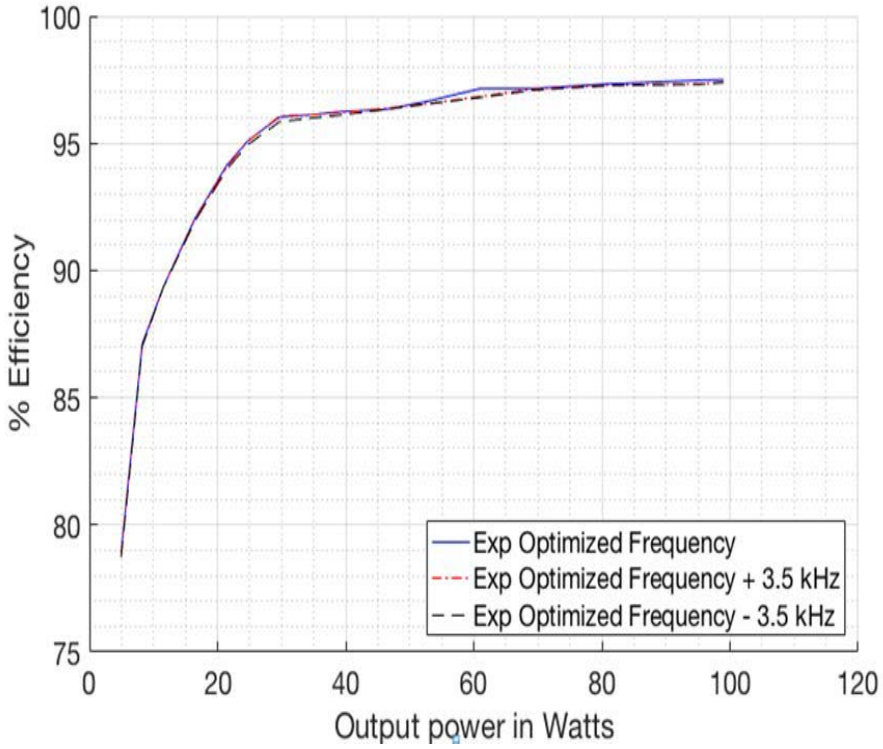

Figure 3-22 Test of optimal frequency in boost mode

The maximum efficiencies for buck mode were 98.06 %, 97.48 % and 96.94 % at 25 V input, 35 V input and 40 V input individually. And the maximum efficiencies for boost mode were 97.22 %, 97.84 % and 97.51 % at 12 V input, 16.5 V input and 20 V input, respectively. The maximum efficiency improvement at light load (10 W) is around 10%. The experimental waveforms at light load and full load are shown in Fig. 3-23 and Fig. 3-24 separately. The prototype is shown in Fig. 3-25.

Figure 3-23 Experimental waveforms at light load

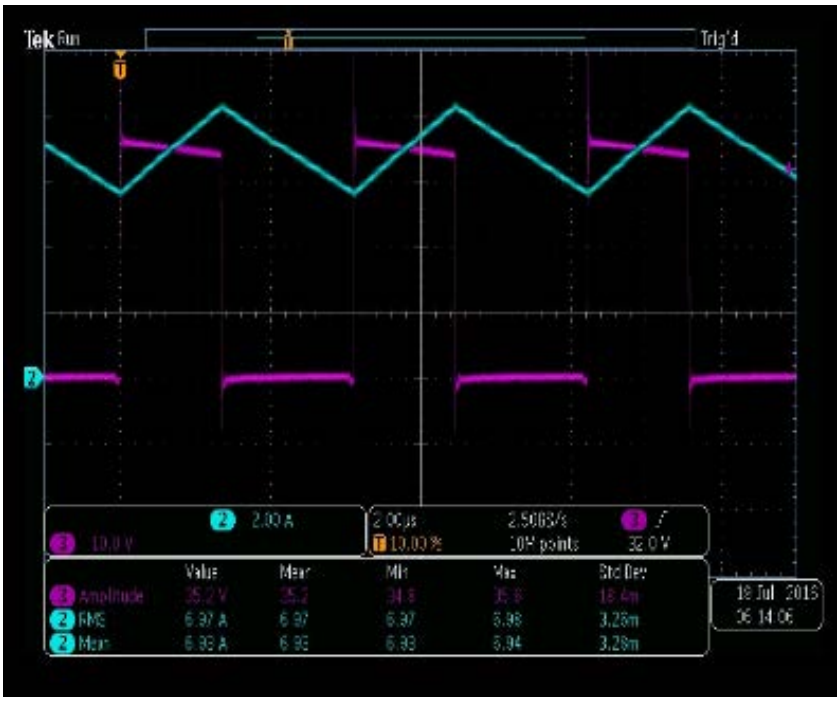

Figure 3-24 Experimental waveforms at full load

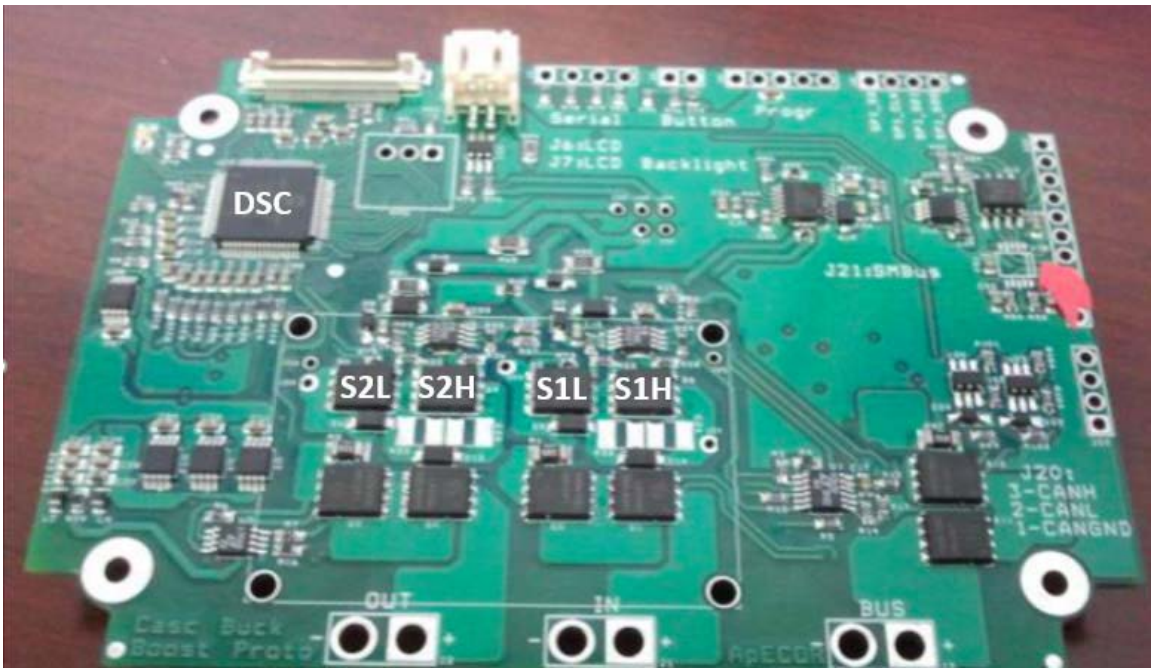

Figure 3-25 CBB converter prototype

3.4 Summary

A detailed and accurate loss model including the effects of component nonlinearities for Cascaded Buck-Boost (CBB) converter is developed in this thesis. The theoretical loss model is found to match closely with the simulated and experimental results. A technique to adjust switching frequency optimally and dynamically with load and PWM duty cycle for efficiency improvement is presented. The optimal switching frequency results in the lowest converter total power loss (maximum efficiency). The efficiency improvement is significant, especially at light load and higher input voltage. The experimental results show that the maximum efficiency can reach 98.06% for buck mode and 97.84% for boost mode,

and the power efficiency is improved by 10% when the output power is 10 W. The efficiency improvement is achieved through firmware and without additional circuit components. The described technique can be applied to any MOSFET and filter component combination.

3.5 Reference:

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CHAPTER 4 ZERO VOLTAGE TRANSITION CASCADED BUCK BOOST CONVERTER

The following figure shows Zero Voltage Transition (ZVT) CBB converter.

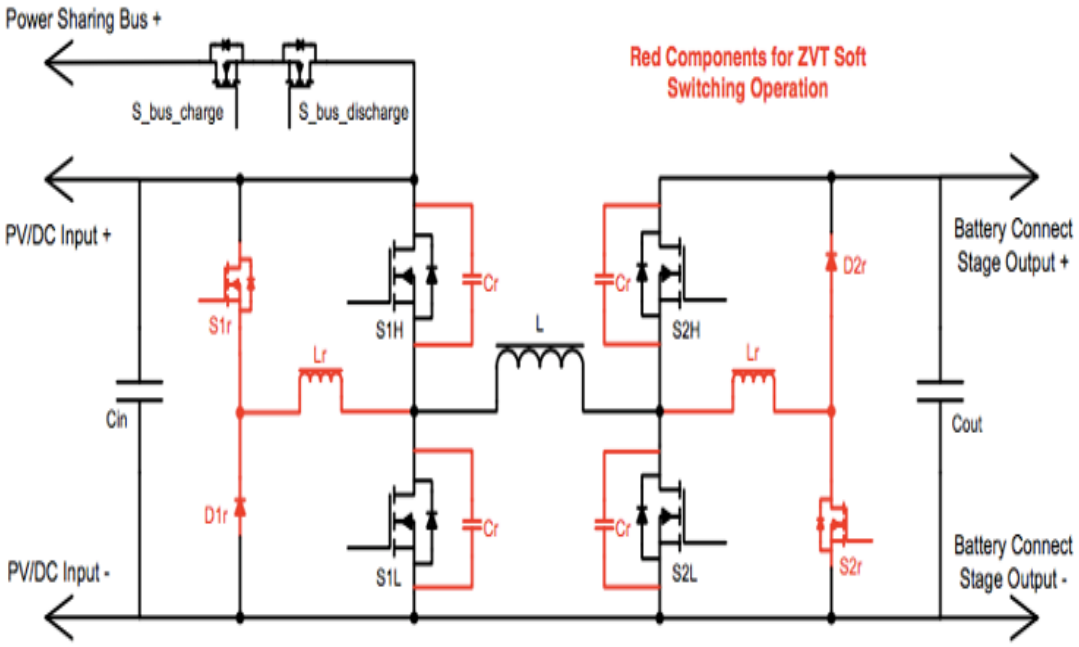

Figure 4-1 ZVT CBB Converter

S1H,S2H,S1L and S2L are the main switches while S1r,S2r,D1r and D2r are the switches used to create resonance and thereby achieve soft switching. The various modes of operation are discussed as follows:

4.1 Buck Mode Analysis

Mode I ($t_0 \leq t < t_1$)

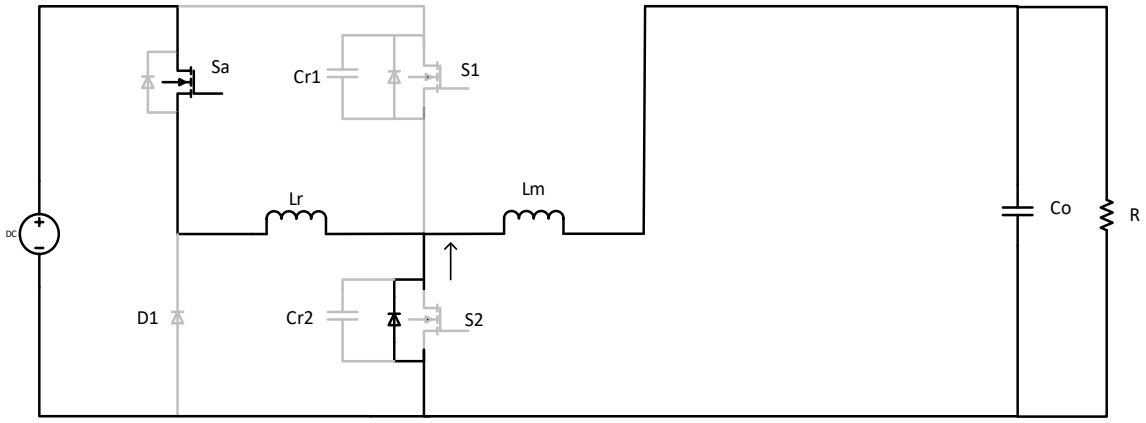

Figure 4-2 Mode I of ZVT Buck Converter

During the previous time t_0, the main switch S_1 and the auxiliary switch S_a were turned off. So the current flowing through the main inductor will go through the parallel diode of switch S_2. At this point, capacitor C_{r1} is charged to input voltage as V_{in}. At t_0, the auxiliary switch S_a is turned on. The current through resonant inductor L_r is linearly increased until it reaches the same value as that in main inductor L_m at t_1. At the same time, the body diode of S_2 is turned off with ZCS. The mathematic equations are showing below.

$$L_m \frac{di_L}{dt} = -V_0 \rightarrow i_L(t) = \frac{-V_0}{Lm}(t - t_0) + I_0 \quad (4\text{-}1)$$

$$L_r \frac{di_{Lr}}{dt} = V_{in} \rightarrow i_{Lr}(t) = \frac{V_{in}}{L_r}(t - t_0) \quad (4\text{-}2)$$

$$i_L(t_0) = I_0, i_{Lr}(t_0) = 0 \quad (4\text{-}3)$$

$$i_L(t_1) = I_1, i_{Lr}(t_1) = I_{r1}, v_{cr1}(t_1) = V_{in}, v_{cr2}(t_1) = 0 \quad (4\text{-}4)$$

Mode II ($t_1 \leq t < t_2$)

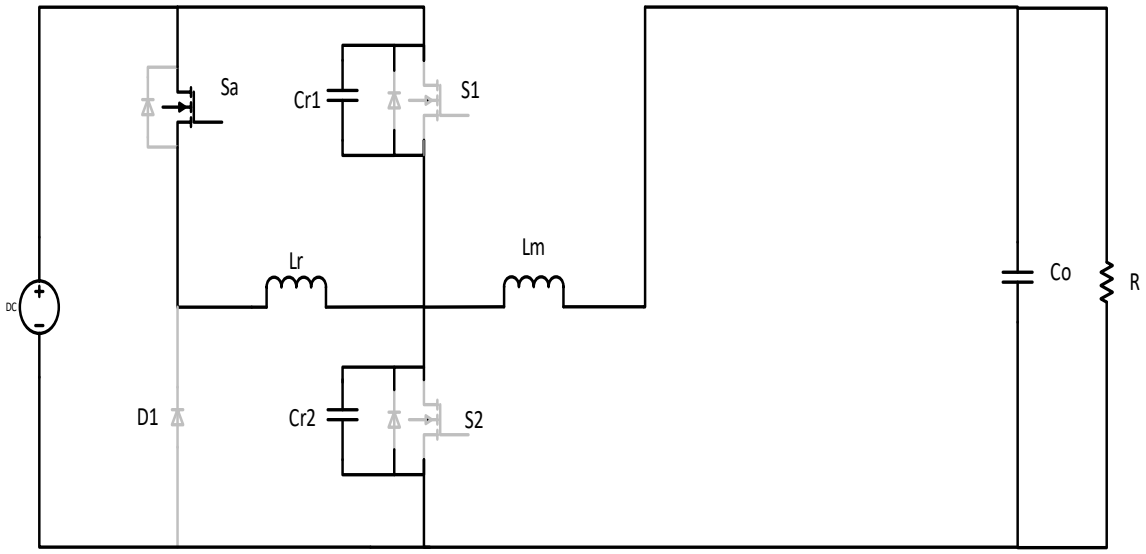

Figure 4-3 Mode II of ZVT Buck Converter

In this time interval, resonant current continues to increase due to the resonance between L_r and C_{r1}. C_{r1} is discharged until the resonance brings its voltage to zero at t_2 at which time the parallel diode of S_1 will conduct. And since voltage between C_{r1} and C_{r2} is equal to input voltage, C_{r2} will be charged to V_{in} at t_2.

$$\begin{cases} i_{Lr} + C_r \frac{dv_{cr}}{dt} = I_1 \\ L_r \frac{di_{Lr}}{dt} = v_c \end{cases} \rightarrow \begin{cases} i_{Lr}(t) = \frac{V_{in}}{Z_0} sin\omega_o(t - t_1) + I_1 \\ v_{cr1}(t) = V_{in} cos\omega_o(t - t_1) \end{cases} \quad (4\text{-}5)$$

where $Z_0 = \sqrt{\frac{L_r}{C_r}}, \omega_0 = \frac{1}{\sqrt{L_r C_r}}, C_r = C_{r1} + C_{r2}$ (4-6)

$$v_{cr2}(t) = V_{in} - v_{cr1}(t) = V_{in} - V_{in} cos\omega_o(t - t_1) \quad (4\text{-}7)$$

$$i_L(t_2) = I_1, i_{Lr}(t_2) = I_{r2}, v_{cr1}(t_2) = 0, v_{cr2}(t_2) = V_{in} \quad (4\text{-}8)$$

Mode III ($t_2 \leq t < t_3$)

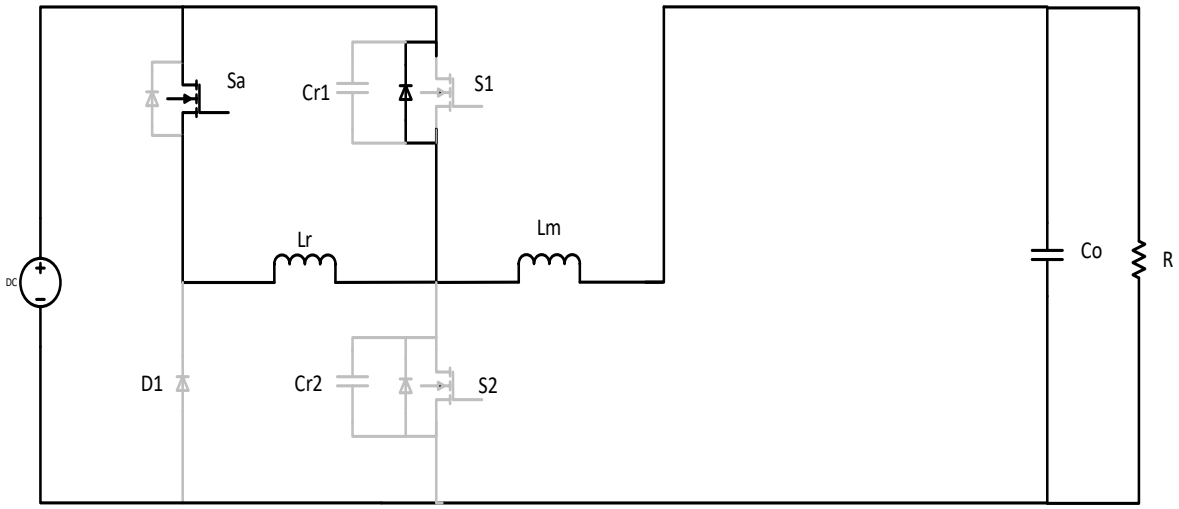

Figure 4-4 Mode III of ZVT Buck Converter

The parallel diode of S_1 is on in this mode. The accumulated energy in resonant tank is transferred through auxiliary switch and the parallel diode. In order to achieve Zero Voltage Switching (ZVS), the turn on signal of S_1 should be applied while its diode is conducting. Besides, the time delay between S_1 and S_a gate signals T_{delay} has to satisfy the following equation,

$$T_{delay} \geq (t_1 - t_0) + (t_2 - t_1) = \frac{L_r I_1}{V_{in} - V_0} + \frac{\pi}{2}\sqrt{L_r C_{r1}} \quad (4\text{-}9)$$

Here the delay time interval in this mode is set to 0.1% of the one switching cycle.

The mathematical equations for this mode are given as follows:

$$L_m \frac{di_L}{dt} = V_{in} - V_o \rightarrow i_L(t) = \frac{V_{in} - V_o}{L}(t - t_2) + I_1 \quad (4\text{-}10)$$

Since resonant inductor is not either charging or discharging, the current flowing through will be the same as the end of the last mode.

$$i_L(t_3) = I_2, i_{Lr}(t_3) = I_{r2}, v_{cr1}(t_3) = 0, v_{cr2}(t_3) = V_{in} \quad (4\text{-}11)$$

Mode IV ($t_3 \leq t < t_4$)

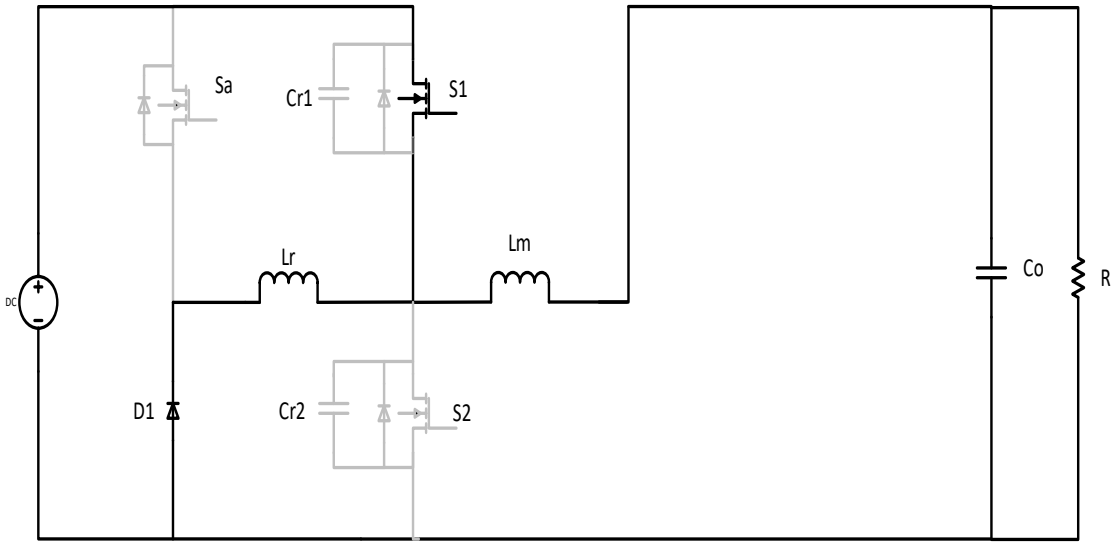

Figure 4-5 Mode IV of ZVT Buck Converter

In previous mode, the main switch S_1 was turned on. So, the current is flowing via S_1 instead of the body diode of S_1. At the beginning of this mode, t_3, the auxiliary switch S_a is turned off under hard switching and this will force the diode D1 to be on in order to transfer the energy in resonant inductor L_r. Voltage between S_a is clamped to V_{in} due to the conduction of diode D. L_r current decreases linearly until it reaches zero at t_4.

$$L_m \frac{di_L}{dt} = V_{in} - V_o \rightarrow i_L(t) = \frac{V_{in} - V_o}{L}(t - t_3) + I_2 \quad (4\text{-}12)$$

$$L_r \frac{di_{Lr}}{dt} = -V_{in} \rightarrow i_{Lr}(t) = \frac{-V_{in}}{L_r}(t - t_3) + I_{r2} \quad (4\text{-}13)$$

$$i_L(t_4) = I_3, i_{Lr}(t_4) = 0, v_{cr1}(t_4) = 0, v_{cr1}(t_4) = V_{in} \quad (4\text{-}14)$$

Mode V ($t_4 \leq t < t_5$)

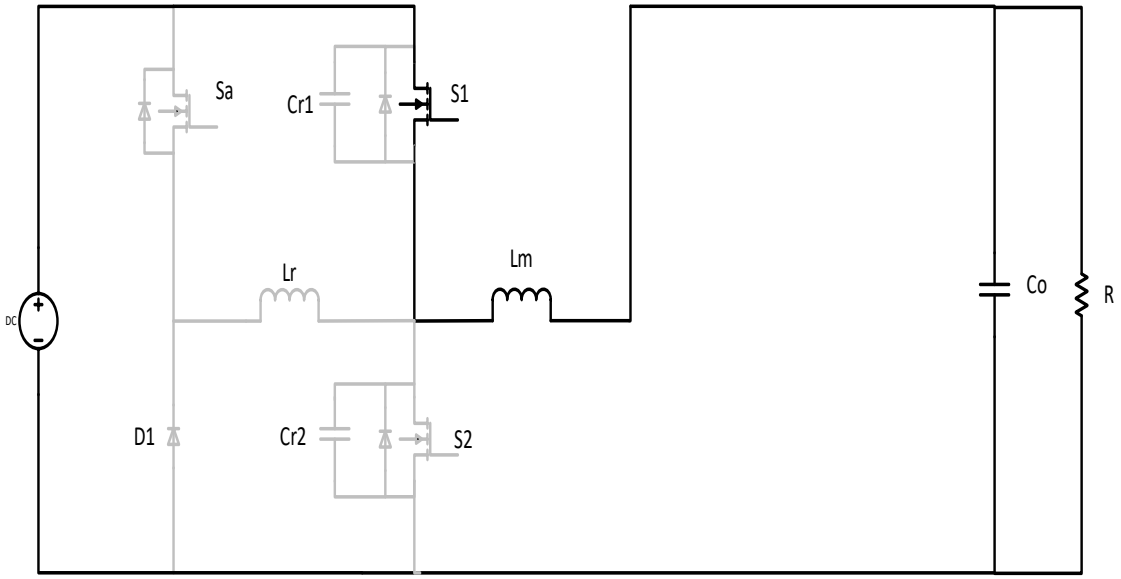

Figure 4-6 Mode V of ZVT Buck Converter

After L_r current drops to zero, the diode D1 will turn off at t_4. The operation of the circuit in this mode is identical to that of the PWM buck converter.

$$L_m \frac{di_L}{dt} = V_{in} - V_o \rightarrow i_L(t) = \frac{V_{in} - V_o}{L}(t - t_4) + I_3 \quad (4\text{-}15)$$

$$i_L(t_5) = I_4, i_{Lr}(t_5) = 0, v_{cr1}(t_5) = 0, v_{cr2}(t_5) = V_{in} \quad (4\text{-}16)$$

Mode VI ($t_5 \leq t < t_6$)

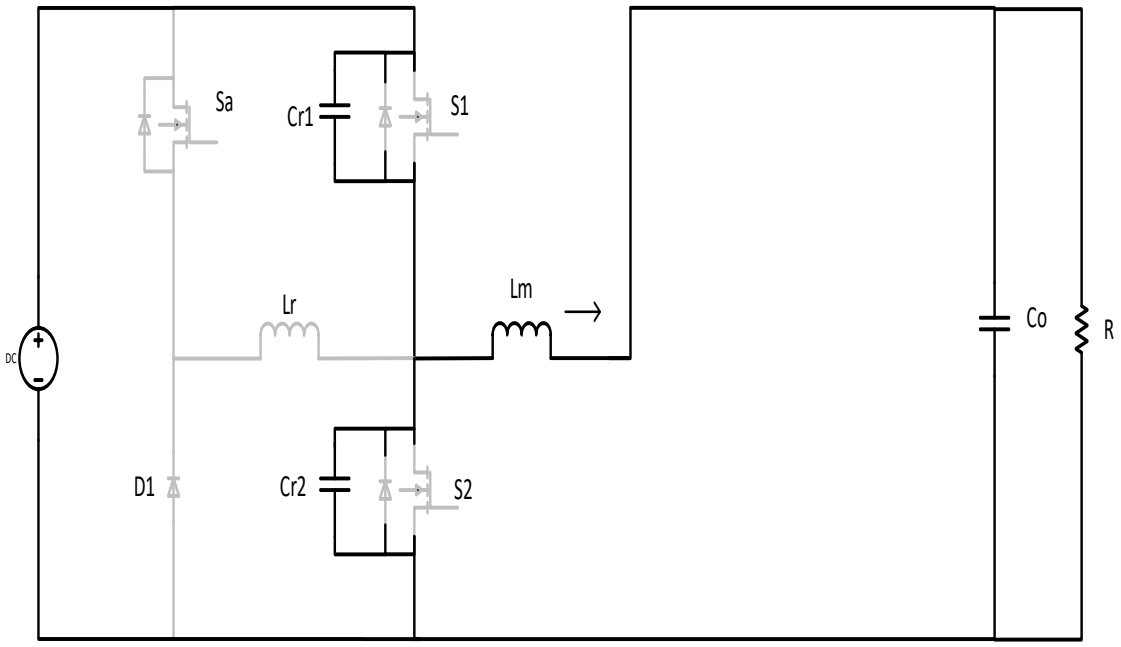

Figure 4-7 Mode VI of ZVT Buck Converter

At t_5, the main switch S_1 is turned off under ZVS and its parallel capacitor begins to be charged by main inductor L_m. At the end of this mode, the resonant capacitor is charged completely and the voltage across it is equal to input voltage. Capacitor C_{r2} is discharged to zero. At this time, the body parallel diode of switch S_2 is turned on smoothly under ZVS.

$$\begin{cases} i_{Lm} + C_r \frac{dv_{cr}}{dt} = I_4 \\ L_m \frac{di_{Lm}}{dt} = V_{in} - v_{cr3} - V_0 \end{cases} \rightarrow$$

$$\begin{cases} i_{Lm}(t) = \frac{V_{in}-V_0}{Z_0} sin\omega_o(t-t_5) + I_4 cos\omega_o(t-t_5) \\ v_{cr1}(t) = -[(V_{in}-V_0)cos\omega_o(t-t_5) - I_4 Z_0 sin\omega_o(t-t_5)] + V_{in} - V_0 \end{cases} \quad (4\text{-}17)$$

where $Z_0 = \sqrt{\frac{L_m}{C_r}}, \omega_0 = \frac{1}{\sqrt{L_m C_r}}, C_r = C_{r3} + C_{r4}$ (4-18)

$$v_{cr2}(t) = V_{in} - v_{cr1}(t) = [(V_{in} - V_0)cos\omega_o(t - t_5) - I_4 Z_0 sin\omega_o(t - t_5)] + V_0 \quad (4\text{-}19)$$

$$i_L(t_6) = I_5, i_{Lr}(t_6) = 0, v_{cr1}(t_6) = V_{in}, v_{cr2}(t_6) = 0 \quad (4\text{-}20)$$

Mode VII ($t_6 \leq t < t_7$)

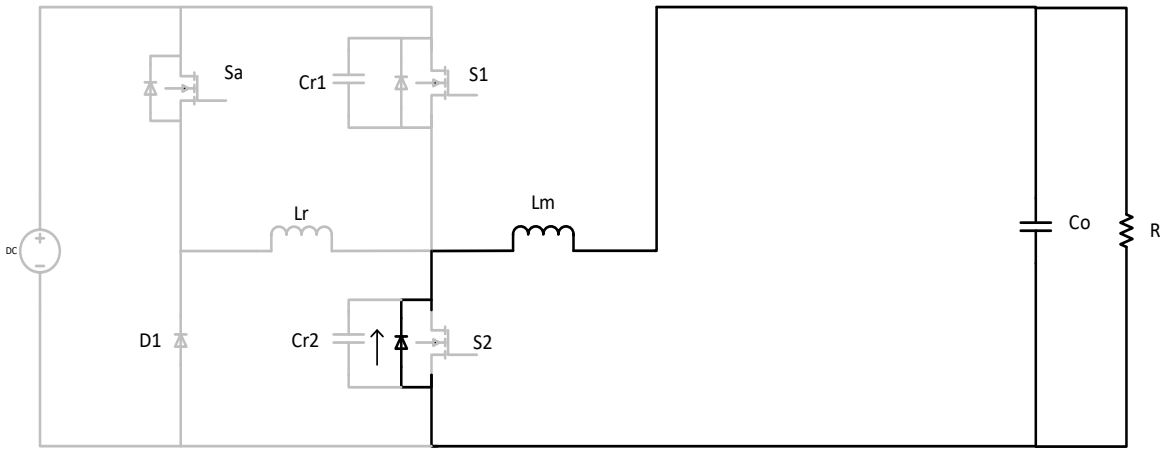

Figure 4-8 Mode VII of ZVT Buck Converter

In this mode, all switches are turned off. Therefore, current in the main inductor L_m is flowing through the body parallel diode of switch S_2. So, this mode is identical to the freewheeling stage of the buck PWM converter. At t_7, the auxiliary switch S_a is turned on again, starting another switching cycle.

The mathematical equation in this mode is

$$L_m \frac{di_L}{dt} = -V_0 \rightarrow i_L(t) = \frac{-V_0}{L}(t - t_6) + I_5 \quad (4\text{-}21)$$

$$i_L(t_7) = I_6 = I_0, i_{Lr}(t_7) = 0, v_{cr1}(t_7) = V_{in}, v_{cr2}(t_7) = 0 \quad (4\text{-}22)$$

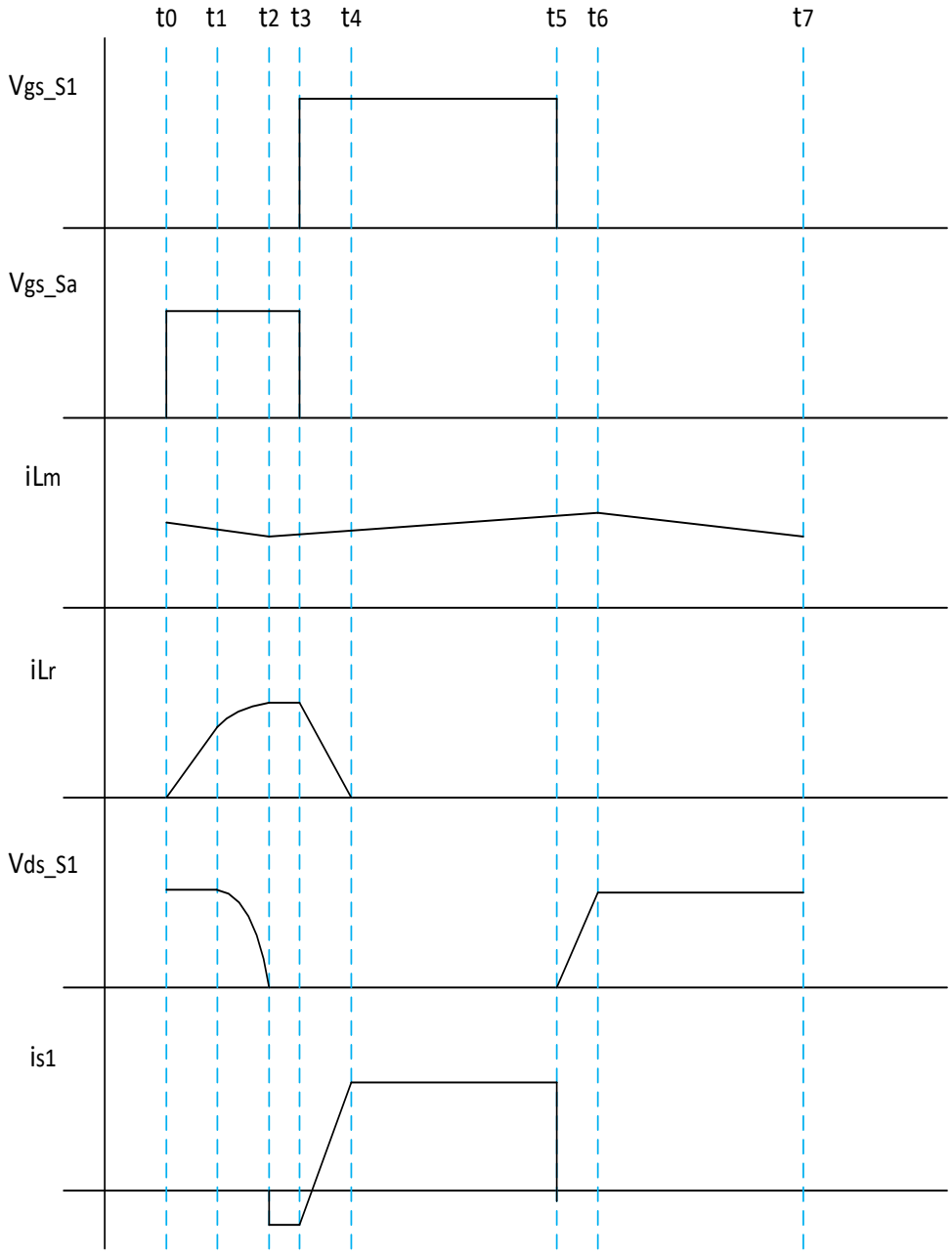

Figure 4-9 Waveform of ZVT CBB converter in Buck Mode

The following figure. shows a plot of gain vs normalized frequency (fns).

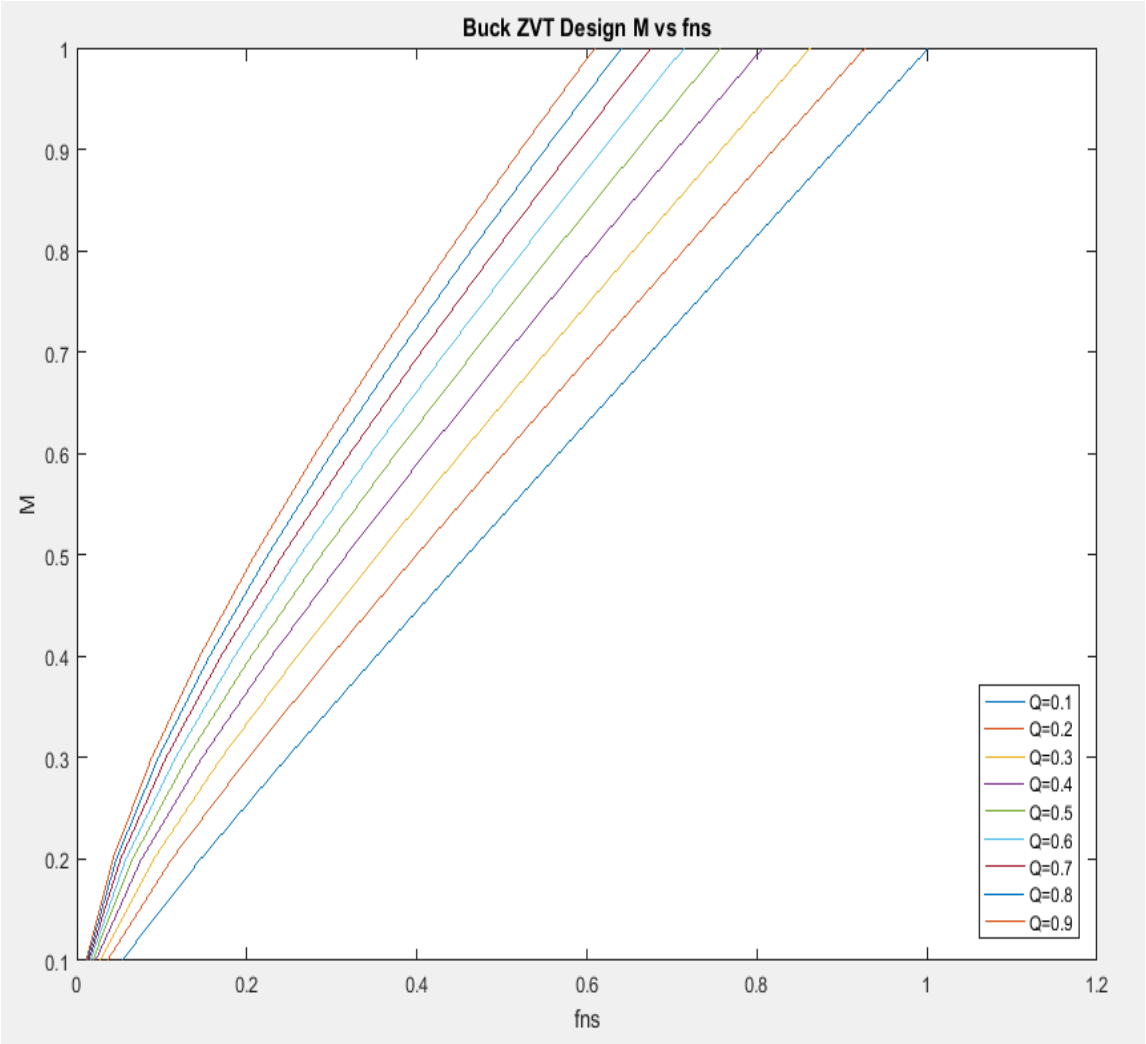

Figure 4-10 Gain vs Normalized frequency ZVT CBB converter in Buck mode

Assume DC voltage source and main inductor as a current source.

Then the time interval for each mode is given as

$$Mode\ I\ time\ interval: t_1 - 0 = \frac{L_r I_o}{V_{in}}$$

$$Mode\ II\ time\ interval: t_2 - t_1 = \frac{\pi}{2\omega_o}$$

$$Mode\ III\ time\ interval: t_3 - t_2 = k_1 T_s$$

$$Mode\ IV\ time\ interval: t_4 - t_3 = \frac{1}{\omega_o} + \frac{L_r I_o}{V_{in}}$$

$$Mode\ V\ time\ interval: t_5 - t_4 = k_2 T_s$$

$$Mode\ VI\ time\ interval: t_6 - t_5 = \frac{V_{in} C_r}{I_o}$$

$$Mode\ VII\ time\ interval: t_7 - t_6$$
$$= T_s - (t_1 - 0) - (t_2 - t_1) - (t_3 - t_2) - (t_4 - t_3) - (t_5 - t_4) - (t_6 - t_5)$$

In the above time intervals, set $k_1 = 0.1\%, k_2 = \left[0.9DT_s - \frac{1}{\omega_o} + \frac{L_r I_o}{V_{in}}\right] / T_s$.

By applying energy balance equation which is $E_{in} = E_{out}$, consequently

$$f_{ns} = \frac{(0.1*M - 0.001)*2*\pi}{\frac{\pi}{2} - 1 + \frac{Q}{2*M}} \qquad (4\text{-}23)$$

4.2 Boost Mode Analysis

In this section, the operation of the ZVT CBB converter in boost mode is analyzed as follows:

Mode I ($t_0 \leq t < t_1$)

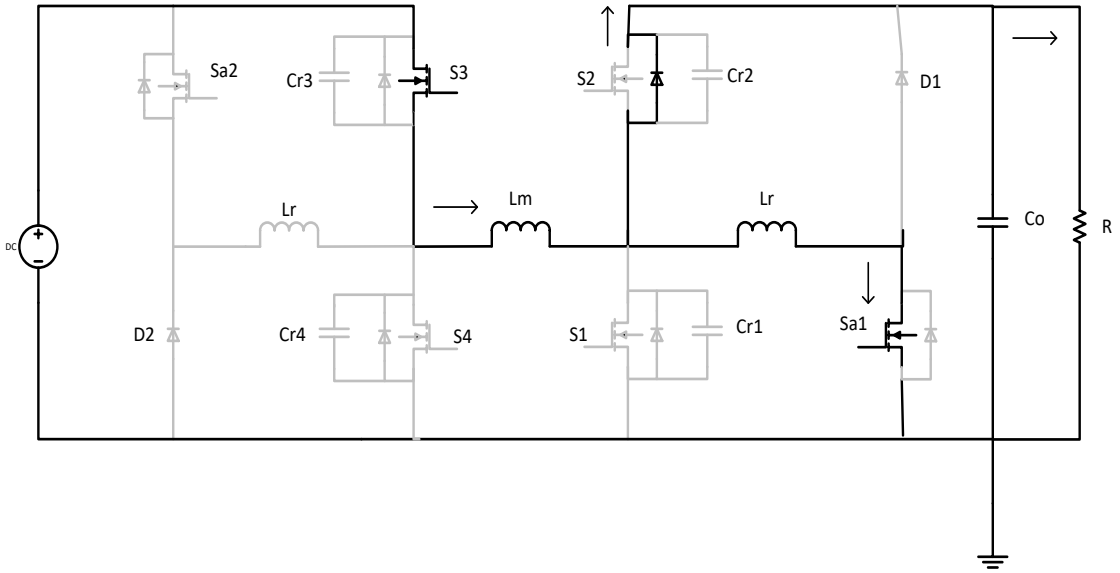

Figure 4-11 Mode I of ZVT Boost Converter

During the previous time t_0, the main switch S_1 and the auxiliary switch S_{a1} were turned off. So the current flowing through the main inductor will go through the parallel diode of switch S_2. At this point, capacitor C_{r1} is charged to output voltage as V_0. At t_0, the auxiliary switch S_{a1} is turned on. The current through resonant inductor L_r is linearly increased until it reaches the same value as that in main inductor L_m at t_1. At the same time, the body diode of S_2 is turned off with zero current switching (ZCS). The mathematical equations are showing below.

$$L_m \frac{di_L}{dt} = V_{in} - V_0 \rightarrow i_L(t) = \frac{V_{in}-V_0}{L}(t - t_0) + I_0 \quad (4\text{-}24)$$

$$L_r \frac{di_{Lr}}{dt} = V_0 \rightarrow i_{Lr}(t) = \frac{V_0}{L_r}(t - t_0) \quad (4\text{-}25)$$

$$i_L(t_0) = I_0, i_{Lr}(t_0) = 0 \quad (4\text{-}26)$$

$$i_L(t_1) = I_1, i_{Lr}(t_1) = I_{r1}, v_{cr1}(t_1) = V_0, v_{cr2}(t_1) = 0 \quad (4\text{-}27)$$

Mode II ($t_1 \leq t < t_2$)

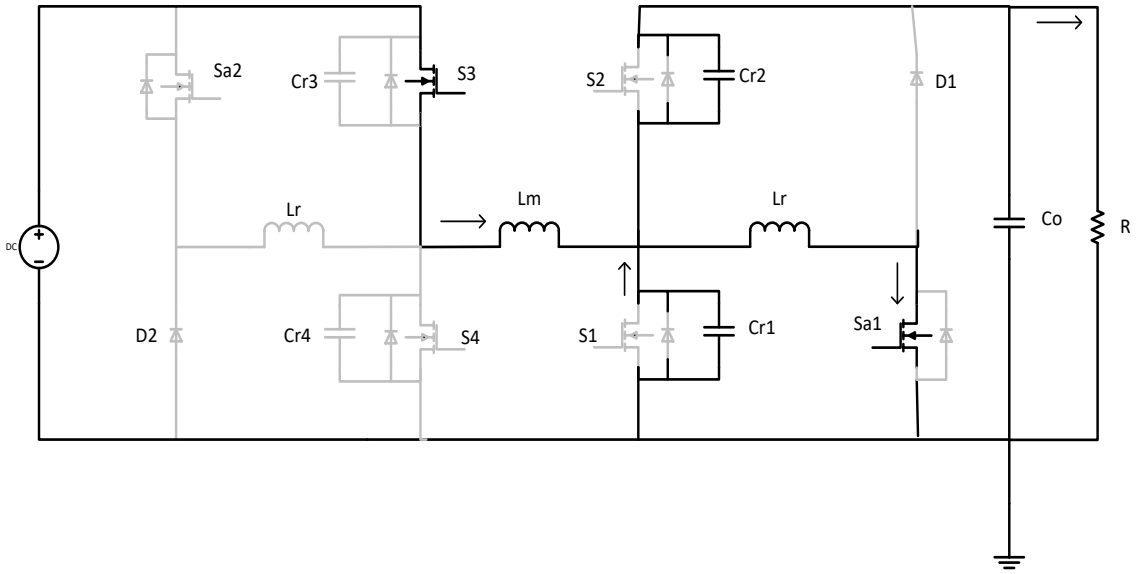

Figure 4-12 Mode II of ZVT Boost Converter

In this time interval, resonant current continues to increase due to the resonance between L_r and C_{r1}. C_{r1} is discharged until the resonance brings its voltage to zero at t_2 at which time the parallel diode of S_1 will conduct. And since voltage between C_{r1} and C_{r2} is equal to output voltage, C_{r2} will be charged to V_0 at t_2.

$$\begin{cases} i_{Lr} + C_r \frac{dv_{cr1}}{dt} = I_1 \\ L_r \frac{di_{Lr}}{dt} = v_{cr1} \end{cases} \rightarrow \begin{cases} i_{Lr}(t) = \frac{V_0}{Z_0} sin\omega_o(t - t_1) + I_1 \\ v_{cr1}(t) = V_o cos\omega_o(t - t_1) \end{cases} \quad (4\text{-}28)$$

where $Z_0 = \sqrt{\frac{L_r}{C_r}}, \omega_0 = \frac{1}{\sqrt{L_r C_r}}, C_r = C_{r1} + C_{r2}$ (4-29)

$$v_{cr2}(t) = V_o - v_{cr1}(t) = V_o - V_o cos\omega_o(t - t_1) \quad (4\text{-}30)$$

$$i_L(t_2) = I_1, i_{Lr}(t_2) = I_{r2}, v_{cr1}(t_2) = 0, v_{cr2}(t_2) = V_0 \quad (4\text{-}31)$$

Mode III ($t_2 \leq t < t_3$)

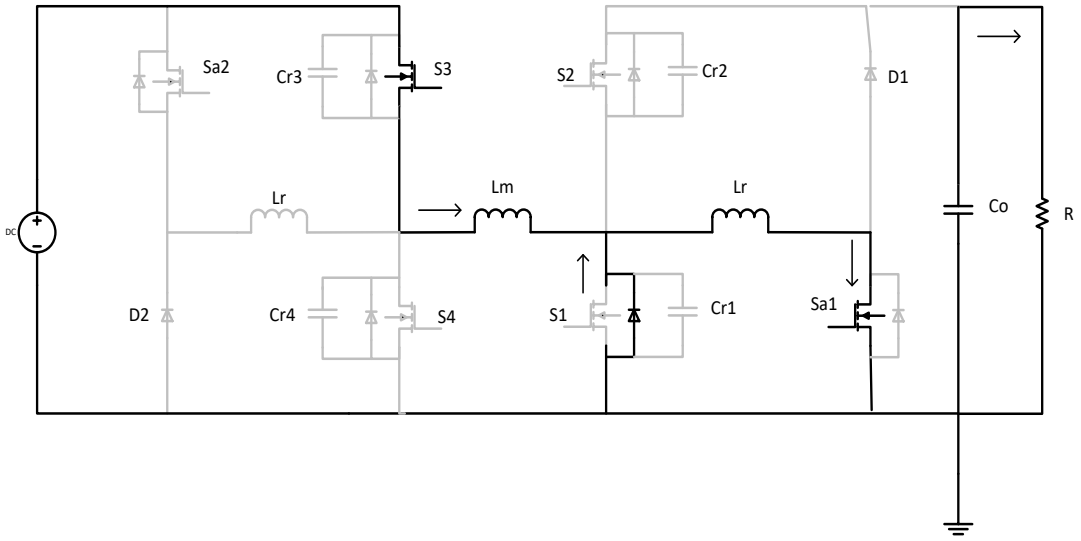

Figure 4-13 Mode III of ZVT Boost Converter

The parallel diode of S_1 is on in this mode. The accumulated energy in resonant tank is transferred through auxiliary switch and the parallel diode. In order to achieve ZVS, the turn on signal of S_1 should be applied while its diode is conducting. Besides, the time delay between S_1 and S_{a1} gate signals T_{delay} has to satisfy the following equation,

$$T_{delay} \geq (t_1 - t_0) + (t_2 - t_1) = \frac{L_r I_1}{V_o} + \frac{\pi}{2}\sqrt{L_r C_{r1}} \quad (4\text{-}32)$$

Usually, the time interval is set to 0.1% of the one switching cycle.

The mathematical equations for this mode are given as follows:

$$L_m \frac{di_L}{dt} = V_{in} \rightarrow i_L(t) = \frac{V_{in}}{L}(t - t_2) + I_1 \quad (4\text{-}33)$$

Since resonant inductor is not charging or discharging, the current flowing will be the same as the end of the last mode.

$$i_L(t_3) = I_2, i_{Lr}(t_3) = I_{r2}, v_{cr1}(t_3) = 0, v_{cr2}(t_3) = V_0 \quad (4\text{-}34)$$

Mode IV ($t_3 \leq t < t_4$)

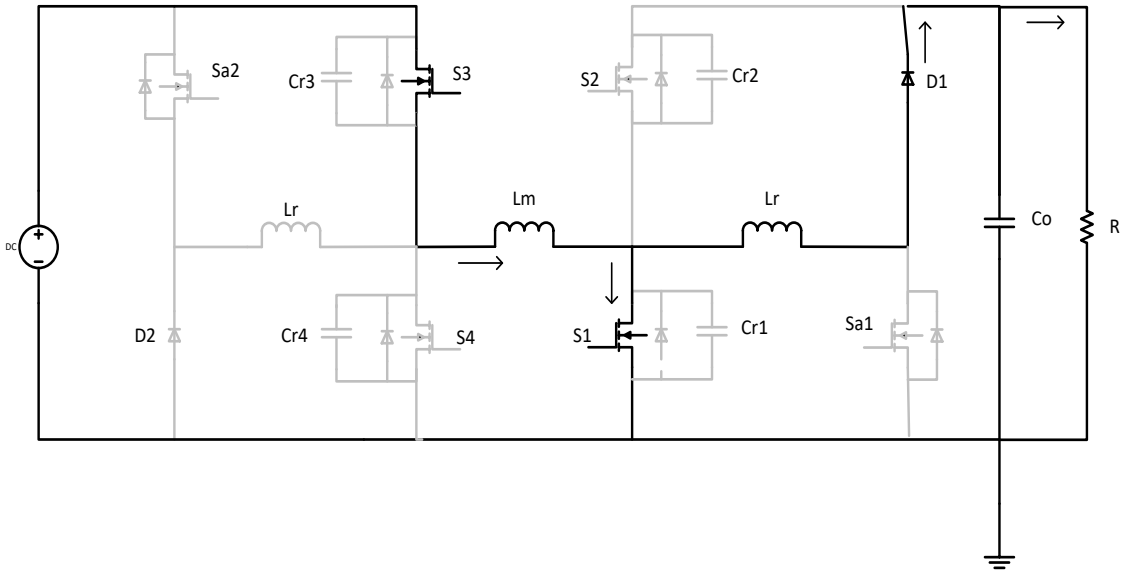

Figure 4-14 Mode IV of ZVT Boost Converter

In previous mode, the main switch S_1 was turned on. So the current is flowing via S_1 instead of the body diode of S_1. At the beginning of this mode, t_3, the auxiliary switch S_{a1} is turned off under hard switching and this will force the diode D to be on in order to transfer the energy in resonant inductor L_r. Voltage between S_{a1} is clamped to V_0 due to the conduction of diode D. L_r current decreases linearly until it reaches zero at t_4.

$$L_m \frac{di_L}{dt} = V_{in} \rightarrow i_L(t) = \frac{V_{in}}{L}(t - t_3) + I_2 \quad (4\text{-}35)$$

$$L_r \frac{di_{Lr}}{dt} = -V_o \rightarrow i_{Lr}(t) = \frac{-V_o}{L_r}(t - t_3) + I_{r2} \quad (4\text{-}36)$$

$$i_L(t_4) = I_3, i_{Lr}(t_4) = 0, v_{cr1}(t_4) = 0, v_{cr2}(t_4) = V_0 \quad (4\text{-}37)$$

Mode V ($t_4 \leq t < t_5$)

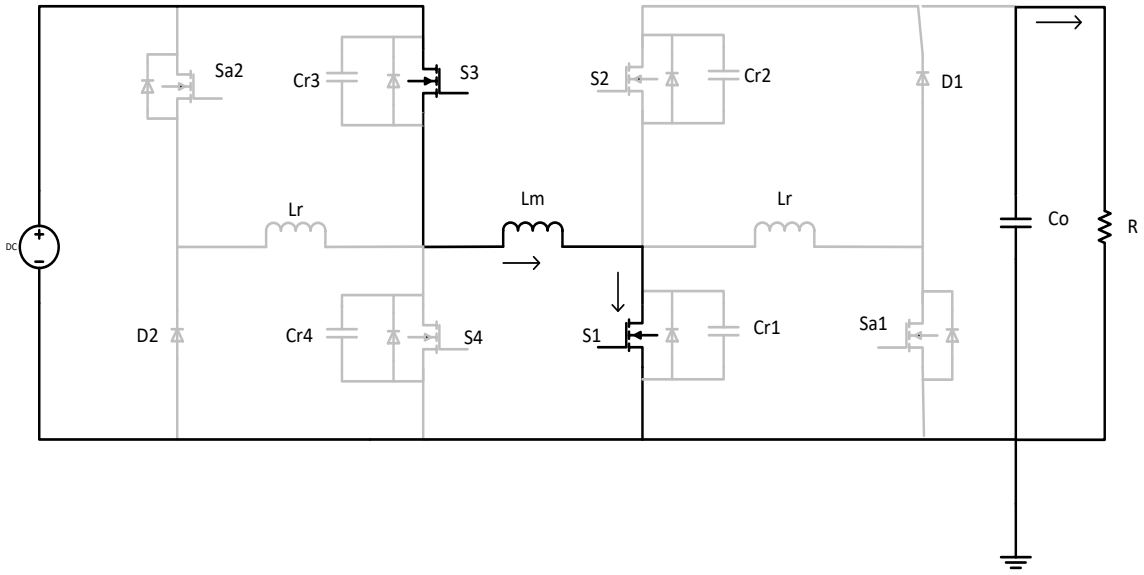

Figure 4-15 Mode V of ZVT Boost Converter

After L_r current drops to zero, the diode D will turn off at t_4. The operation of the circuit in this mode is identical to that of the PWM boost converter.

$$L_m \frac{di_L}{dt} = V_{in} \rightarrow i_L(t) = \frac{V_{in}}{L}(t - t_4) + I_3 \quad (4\text{-}38)$$

$$i_L(t_5) = I_4, i_{Lr}(t_5) = 0, v_{cr1}(t_5) = 0, v_{cr2}(t_5) = V_0 \quad (4\text{-}39)$$

Mode VI ($t_5 \leq t < t_6$)

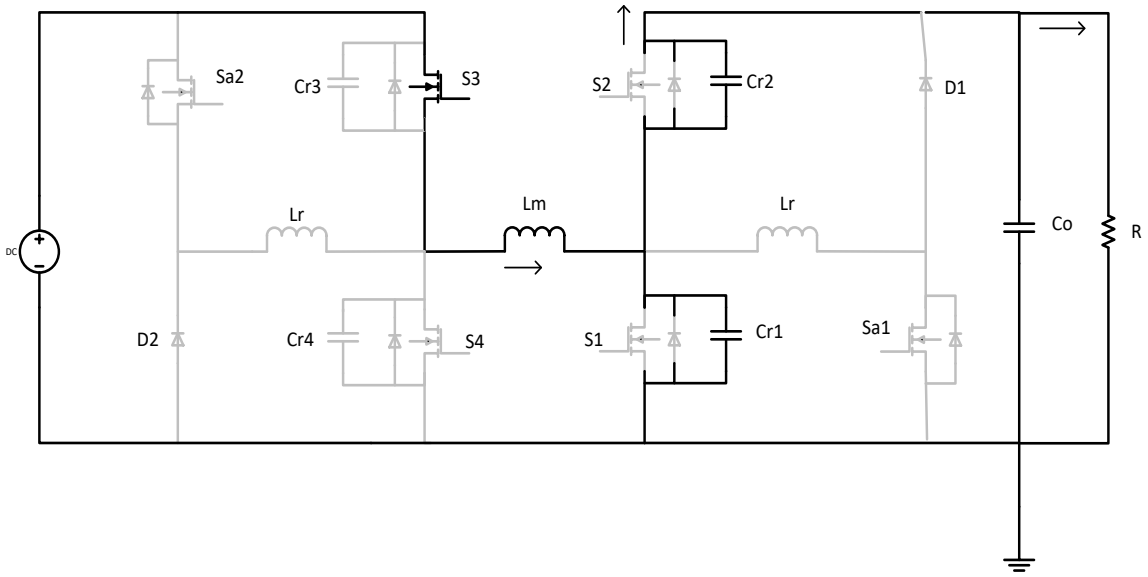

Figure 4-16 Mode VI of ZVT Boost Converter

At t_5, the main switch S_1 is turned off under ZVS and its parallel capacitor begins to be charged by main inductor L_m. At the end of this mode, the resonant capacitor is charged completely and the voltage across it is equal to output voltage. Capacitor C_{r2} is discharged to zero. At this time, the body parallel diode of switch S_2 is turned on smoothly under ZVS.

$$i_L(t) = C_{r1}\frac{dv_{cr1}}{dt} \rightarrow v_{cr1}(t) = \frac{1}{C_{r1}}\int i_L(t)\,dt = V_o \quad (4\text{-}40)$$

$$i_L(t_6) = I_5, i_{Lr}(t_6) = 0, v_{cr1}(t_6) = V_0, v_{cr2}(t_6) = 0 \quad (4\text{-}41)$$

Mode VII ($t_6 \leq t < t_7$)

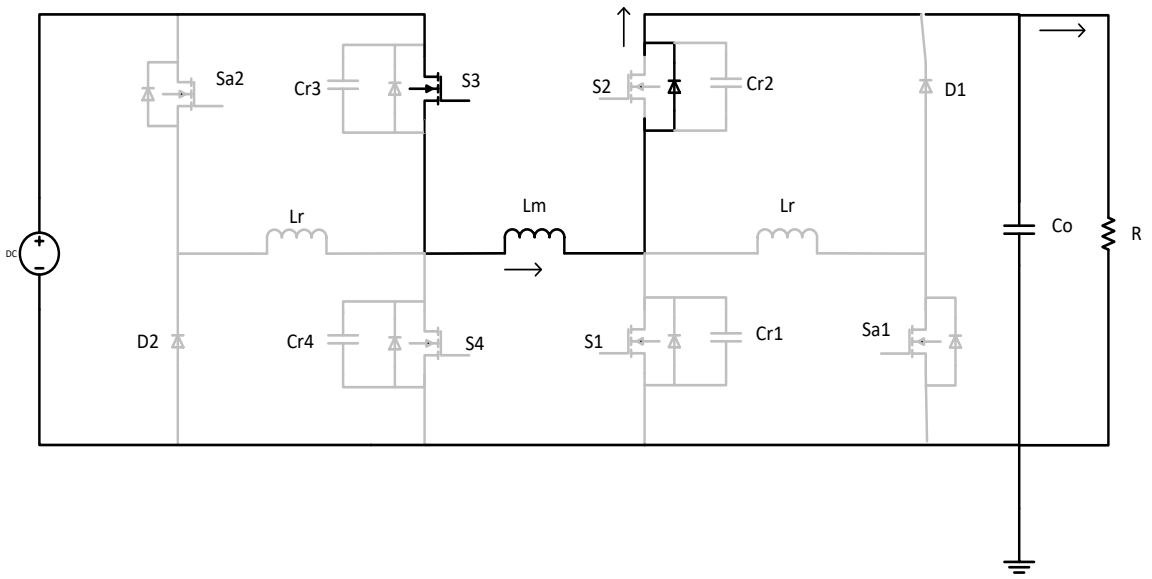

Figure 4-17 Mode VII of ZVT Boost Converter

In this mode, all switches are turned off. Therefore, current in the main inductor L_m is flowing through the body parallel diode of switch S_2. So this mode is identical to the freewheeling stage of the boost PWM converter. At t_7, the auxiliary switch S_{a1} is turned on again, starting another switching cycle.

The mathematical equation in this mode is described as follow:

$$L_m \frac{di_L}{dt} = V_{in} - V_0 \rightarrow i_L(t) = \frac{V_{in}-V_0}{L}(t - t_6) + I_5 \quad (4\text{-}42)$$

$$i_L(t_7) = I_6 = I_0, i_{Lr}(t_7) = 0, v_{cr1}(t_7) = V_0, v_{cr2}(t_7) = 0 \quad (4\text{-}43)$$

In order to make the calculation easier and since the main inductor is far larger than the resonant inductor, simplify the boost topology into the following (consider DC voltage source and main inductor as a current source)

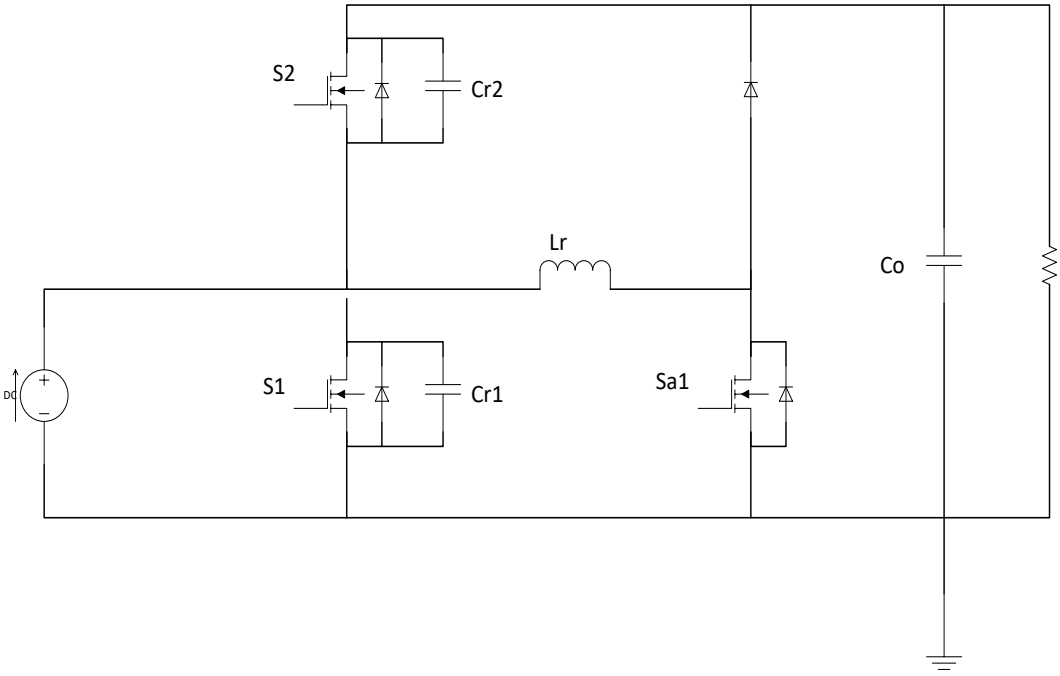

Figure 4-18 Mode VIII of ZVT Boost Converter

Then the time interval for each mode is given as follows:

$$Mode\ I\ time\ interval: t_1 - 0 = \frac{L_r I_{in}}{V_o}$$

$$Mode\ II\ time\ interval: t_2 - t_1 = \frac{\pi}{2\omega_o}$$

$$Mode\ III\ time\ interval: t_3 - t_2 = k_1 T_s$$

$$Mode\ IV\ time\ interval: t_4 - t_3 = \frac{1}{\omega_o} + \frac{L_r I_{in}}{V_o}$$

$$Mode\ V\ time\ interval: t_5 - t_4 = k_2 T_s$$

$$Mode\ VI\ time\ interval: t_6 - t_5 = \frac{V_o C_r}{I_{in}}$$

$$Mode\ VII\ time\ interval: t_7 - t_6$$
$$= T_s - (t_1 - 0) - (\,t_2 - t_1) - (t_3 - t_2) - (t_4 - t_3) - (t_5 - t_4) - (\,t_6 - t_5)$$

In the above time intervals, set $k_1 = 0.1\%, k_2 = \left[0.9DT_s - \frac{1}{\omega_o} + \frac{L_r I_{in}}{V_o}\right]/T_s$.

By applying energy balance equation which is $E_{in} = E_{out}$, consequently,

$$\frac{f_{ns}}{2\pi}\left(\frac{\pi}{2} - 1 + \frac{Q}{2M}\right) = 0.099 - \frac{0.1}{M} \qquad (4\text{-}44)$$

Where $f_{ns} = \frac{f_s}{f_o}, Q = \frac{R}{Z_o}, M = \frac{V_o}{V_{in}}$

Plotting the above the gain versus normalized frequency curve of the ZVT CBB converter in boost mode is shown as follows in Fig. 4-19.

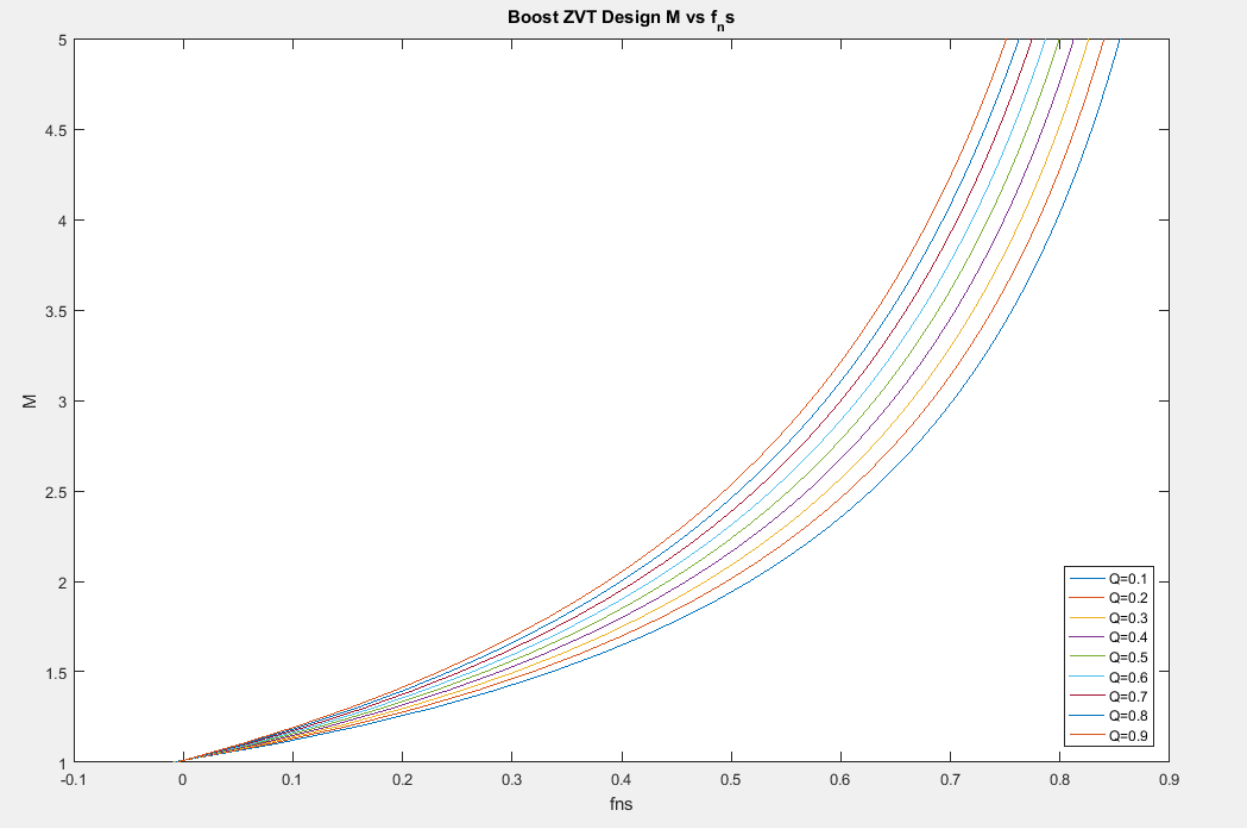

Figure 4-19 Gain vs Normalized frequency (fns) ZVT CBB converter in Boost mode

4.3 Example Design

- $V_{in} = 13V$
- $V_o = 30V$
- $L = 20\mu H$
- $C = 33\mu F$
- $P_o = 100W$
- $f_{sw} = 133kHz$

Then the voltage gain is

$$M = \frac{V_o}{V_{in}} = \frac{30}{13} = 2.3$$

Choose Q=0.7, from the curve in Fig. 4-19 $f_{ns} = 0.48$

Based on

$f_{ns} = \frac{1}{2\pi\sqrt{L_r C_r}}$, (4-45)

$Q = \frac{R}{Z_o}$ and (4-46)

$Z_o = \sqrt{\frac{L_r}{C_r}}$.(4-47) (4-48)

It is found that

$$\begin{cases} L_r = 7.4\mu H \\ C_r = 44.7nF \end{cases} \rightarrow \begin{cases} L_r = 7.4\mu H \\ C_{r1} = 22.35nF \\ C_{r2} = 22.35nF \end{cases}$$

In the ZVT circuit design, the resonant inductor is designed to provide soft turn-off of the upper MOSFET body diode. The resonant capacitor is selected to provide soft switching of the low side MOSFET. The resonant inductor controls the di/dt of the diode by providing an alternate current path for the boost inductor current. When the auxiliary switch turns on, the input current is diverted from the boost diode to the resonant inductor. The resonant value can be calculated by determining how fast the diode can be turned off. The diode's turn-off time is given by its reverse recovery time. A good initial estimate is to allow the inductor current to ramp up to the diode current within three times the diode's specified reverse recovery time. The reverse recovery of the diode is partially a function of its turn-off di/dt. If a controlled di/dt is assumed, the reverse recovery time of this diode can be estimated to be approximately 60 ns.

The duty cycle is

$$D = 1 - \frac{V_{in}}{V_o} = 1 - \frac{13}{30} = 0.567$$

The output current is

$$I_o = \frac{P_o}{V_o} = \frac{100}{30} = 3.33A$$

The input current is

$$I_{in} = I_o\left(\frac{1}{1-D}\right) = 3.33 * \frac{1}{1-0.567} = 7.7A$$

The current ripple in the main inductor is given by

$$\Delta i_L = \frac{V_{in}}{L} DT_s = \frac{13}{20\mu}(0.567)\frac{1}{133k} = 2.77A$$

So, the peak input current is

$$I_{in\_peak} = I_{in} + \frac{1}{2}\Delta i_L = 9.085A$$

Then,

$$\frac{di}{dt} = \frac{I_{in\_peak}}{3t_{rr}} = 5.05 * 10^7 A/s$$

Therefore, the resonant inductance is

$$L_r \geq \frac{V_o}{\frac{di}{dt}} = \frac{30}{5.05 * 10^7} = 0.59\mu H$$

Since the partial energy stored in resonant inductor comes from the resonant capacitor and the other comes from the main inductor, the total peak energy stored in resonant inductor should be larger than that in the resonant capacitor.

Peak energy stored in resonant inductor is given as

$$E_{Lr} = \frac{1}{2} L_r {i_{Lr\_peak}}^2 \quad (4\text{-}49)$$

Energy stored in resonant capacitor is

$$E_{Cr} = \frac{1}{2} C_r {V_o}^2 \quad (4\text{-}50)$$

Therefore,

$$\frac{1}{2} C_r {V_o}^2 < \frac{1}{2} L_r {i_{Lr\_peak}}^2 \quad (4\text{-}51)$$

Because the peak current flowing through resonant inductor is larger than the peak input current, simply select I_{in_peak} for the calculation. According to mathematical insight, if the inequalities

$$\frac{1}{2}C_r{V_o}^2 < \frac{1}{2}L_r{i_{in\_peak}}^2 \quad (4\text{-}52)$$

and

$$\frac{1}{2}L_r{i_{in\_peak}}^2 < \frac{1}{2}L_r{i_{Lr\_peak}}^2 \quad (4\text{-}53)$$

are true, then,

$$\frac{1}{2}C_r{V_o}^2 < \frac{1}{2}L_r{i_{Lr\_peak}}^2 \quad (4\text{-}54)$$

is also correct.

Hence,

$$C_r < \frac{L_r{i_{in\_peak}}^2}{{V_o}^2} = 54\ nF$$

Thus, the choice for $L_r = 7.4\ \mu H\ and\ C_r = 44.7\ nF$ meet the above requirement.

Further, the design may be verified by changing two different variations:

Load power changes by +/- 30% and load current is the same

Average input voltage changes by +/- 20%

For (I)

$M_{min} = 2.3 * (1 - 30\%) = 1.61$

$M_{max} = 2.6 * (1 + 30\%) = 2.99$

From the gain-fns curve in Fig. 4-19, f_{ns} changes from 0.283 to 0.59; therefore, this means switching frequency should change from 78.4kHz to 163.4 kHz.

For (II)

$V_{in,min} = 13 * (1 - 20\%) = 10.4V$

$V_{in,max} = 13 * (1 + 20\%) = 15.6V$

So,

$M_{min} = \frac{30}{15.6} = 1.92$

$M_{max} = \frac{30}{10.4} = 2.88$

From the curve in Fig. 4-19, f_{ns} changes from 0.385 to 0.575; therefore, this implies switching frequency should change from 106.6kHz to 159.3 kHz.

Next, to verify theoretical calculation and simulation measurement match a point from each condition is selected. The simulation circuit is built by PSIM 10.0.6 and shows as the following:

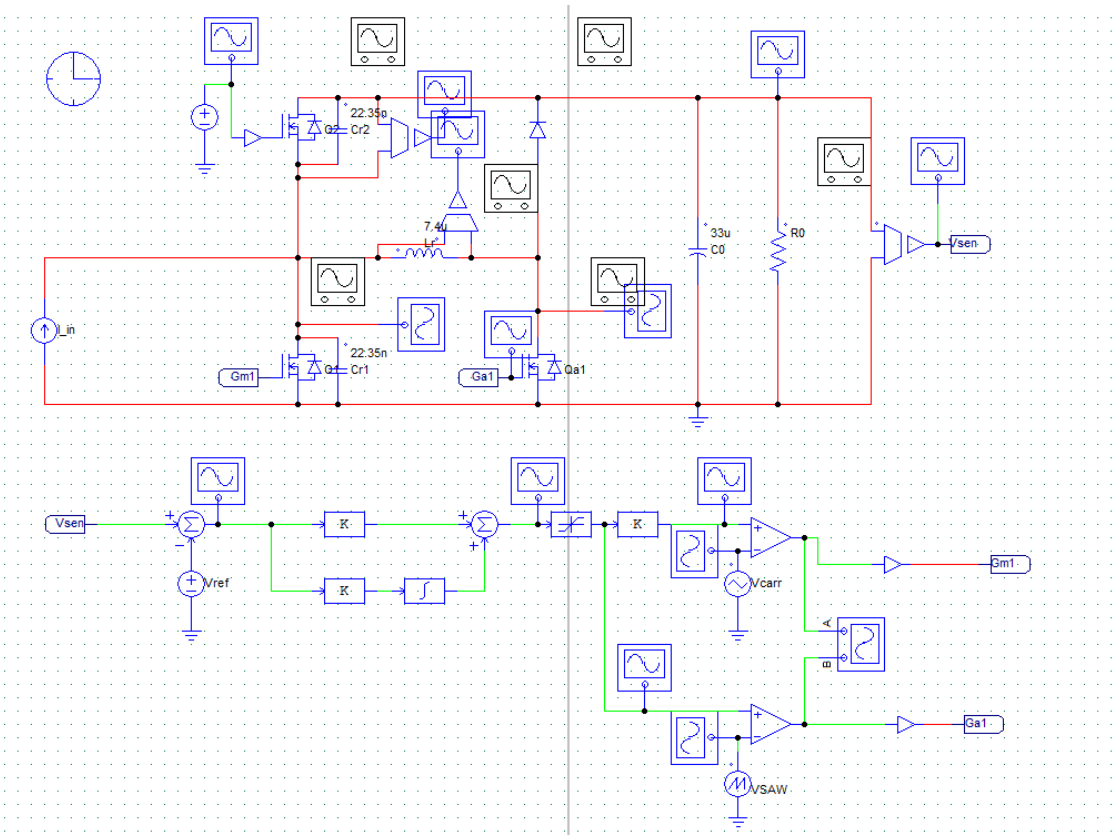

Figure 4-20: Simulating ZVT boost converter example design

When load power changes by – 30 %, we have changed $V_o = 21\,V, f_s = 78.4\,kHz, T_s = 12.76\,\mu s$

Table 4-1: Time interval calculation for – 30 % change in output voltage

	Theoretical calculation	Simulation measurement
Mode I time interval	1.89us	1.8752us
Mode II time interval	0.903us	0.9029us

Mode III time interval	12.76ns	14.2064ns
Mode IV time interval	2.47us	2.4615us
Mode V time interval	1.894us	1.8972us
Mode VI time interval	0.175us	0.1780us
Mode VII time interval	5.415us	5.4208us

When average input voltage changes by + 20 %, we have changed $V_{in} = 15.6\,V, f_s = 106.6\,kHz, T_s = 9.38\,\mu s$

Table 4-2: Time interval calculation for + 20 % change in input voltage

	Theoretical calculation	Simulation measurement
Mode I time interval	1.58us	1.584us
Mode II time interval	0.903us	0.886us
Mode III time interval	9.38ns	10.286ns
Mode IV time interval	2.16us	2.161us
Mode V time interval	1.89us	1.890us
Mode VI time interval	0.21us	0.206us

Mode VII time interval	2.63us	2.643us

From the above tables, it is clear that the theoretical calculation matches with simulation measurement. Therefore, the curve aforementioned is valid and can be used for ZVT designing.

4.4 Reference:

[1] I. Batarseh, “Power Electronics Circuits,” John Wiley & Sons, Inc., 2004

[2] G. Hua (1994), “Soft Switching Techniques For Pulse-Width-Modulated Converters.” (Published Doctoral Dissertation) Virginia Polytechnic Institute and State University, Blacksburg, Virginia, USA.

CHAPTER 5 INDUCTOR DESIGN

5.1 Introduction

With the ever-growing need for higher power density, higher efficiency, and higher temperature operation, the converter design process tends to convolve rather complexly. Various soft-switching techniques are presented in [1][2] to eliminate switching losses either naturally via passive components or via forced commutation with active and passive components. However, at low-power (200 W) the previously-presented techniques are often less effective, as these resonant passive and/or active components have their own additive losses. Further, the techniques introduced in [1][2] are designed at narrow load range with rather involved controls in place making them hard to implement for design requiring high weighted efficiency.

Techniques presented in [3]–[5] use the loss model to find switching frequency corresponding to lowest loss, and are implemented with controls to switch at these optimized frequencies. But there are no explicit details provided to test the robustness of their loss model, and no components are optimized. Further, in [6], Nanocrystalline material characterization is performed and many design criteria may be inferred. In [7], Nanocrystalline core is used to design high power inductor for electric vehicles while in [8], insights for modeling core losses and copper losses are presented.

In this thesis, a loss model for buck-cascaded-boost topology is developed with component non-linearity and robustness of the loss model is validated experimentally. This loss model

is utilized to determine switching frequencies corresponding to lowest total loss. These theoretical gains in efficiency are validated experimentally. Since most of the losses are in the inductor, a new ultra-efficient low profile nanocrystalline based inductor is designed [9]–[17] and developed. Finite Element Analysis Methods (FEA) was used to analyze the design.

5.2 Buck-Cascaded-Boost Loss Model

A Buck-Cascaded-Boost converter is as shown in earlier. There are two modes of operation: in Buck mode, S1H and S1L are the switching MOSFETs while S2H and S2L are at 100% and 0% duty respectively, in boost mode S2H and S2L are the switching MOSFETs with S1H and S1L at 100 % and 0 % duty respectively. A comprehensive loss model is developed with component nonlinearities (i.e. C_{iss} v/s V_{DS}, C_{oss} v/s V_{DS}, C_{rss} v/s $V_{DS,}$ inductance v/s current etc.). The loss model is validated experimentally as shown in Fig. 5-1, it is found that the loss model is accurate with a maximum error of ±1.51 W at full load.

An adaptive frequency control is developed to achieve the highest efficiency. Based on the loss model, switching frequency that corresponds to lowest total loss across the load range are calculated theoretically. A control system with look-up table is used to adopt switching frequency as a function of load. The theoretical efficiency improvement is found to match experimental result as shown in Fig. 5-1.

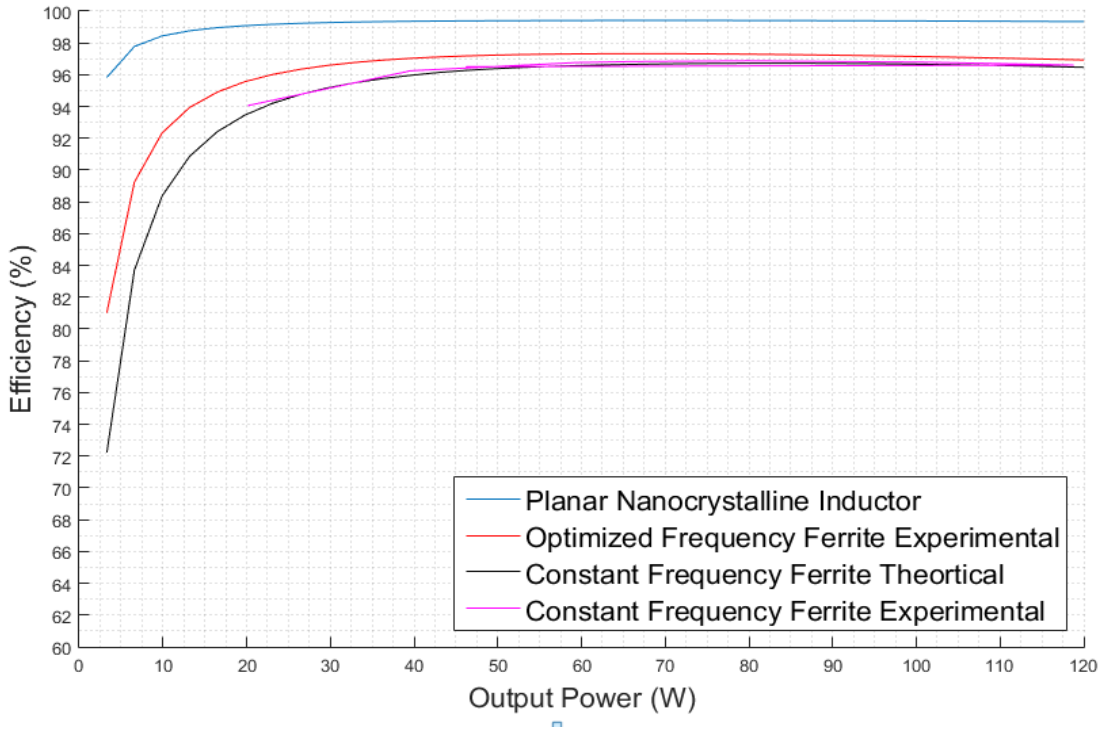

Figure 5-1 Various Loss curves across the load range.

It is realized that the efficiency cannot be improved beyond this point based on the above method or by other methods given in [3]–[5]. Fig. 5-2 shows the breakdown of losses at full load in boost mode where the losses are maximum. Consequently, to further improve efficiency, the inductor must be redesigned.

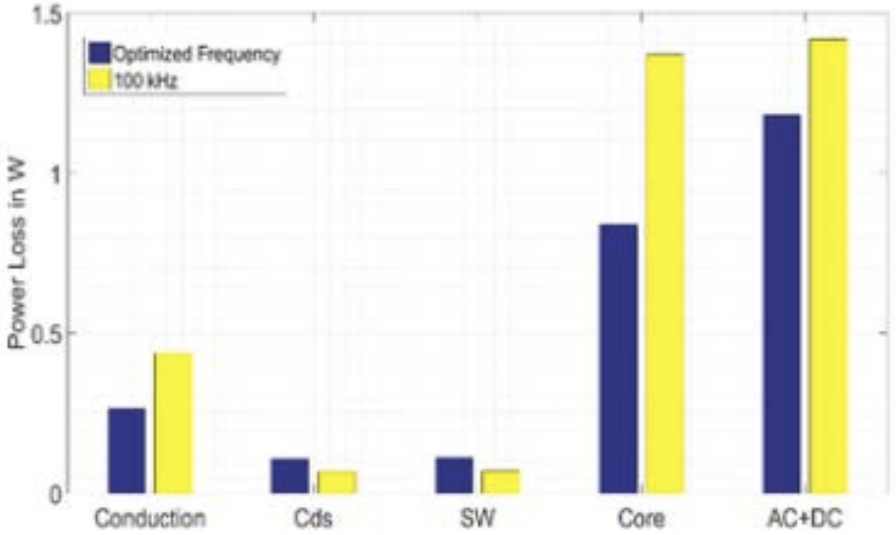

Figure 5-2 Breakdown of Losses at optimized and fixed frequency

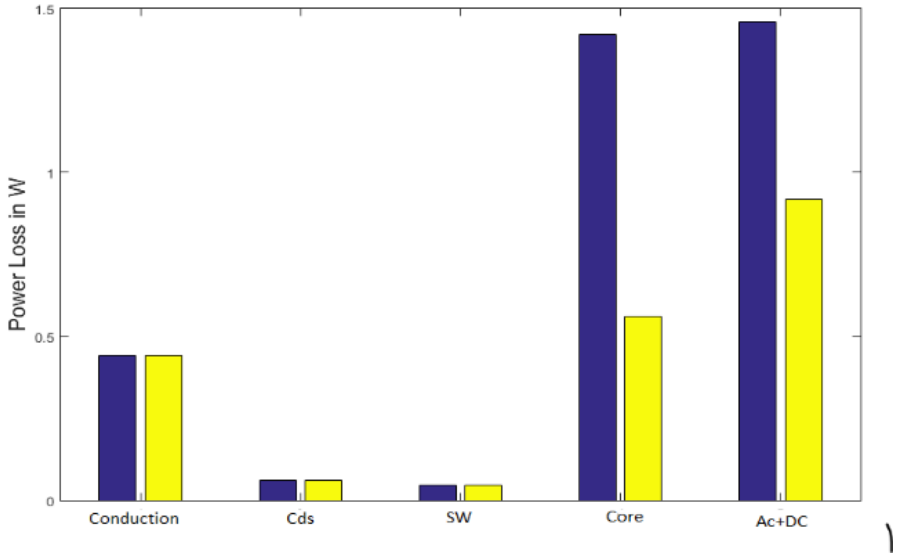

Figure 5-3 Breakdown of Losses at optimized and fixed frequency with Nanocrystalline Inductor

5.3 Planar-Nanocrystalline-Inductor Design

Nanocrystalline material (Metglas FT3W-L) was used to design the inductor. The nanocrystalline core is selected as it has high saturation flux density, high permeability, low loss density and high Curie temperature[12].

Figure 5-4 Pseudo-EE Nanocrystalline

However, such cores are complicated to make and are generally expensive. Thus, a pseudo-EE shape core geometry formed by stacking cut C-cores is proposed with low profile height as shown in Fig. 4.

Detailed analyses including proximity effect, skin effect, and fringing flux were carried for winding design with copper. Fig. 5-5 shows the loss plot with multiple layers winding and it is inferred that a single foil design with 0.6 mm thickness provides lowest loss for the given window geometry. The efficiency of the planar nanocrystalline inductor with adaptive frequency is as shown in Fig. 5-1, a clear improvement in efficiency seen, the loss breakdown with the Nanocrystalline core is shown in Fig. 5-3. The prototype used is shown

in Fig. 5-4 and experimental waveform of switch node voltage with inductor current is shown in Fig. 5-6.

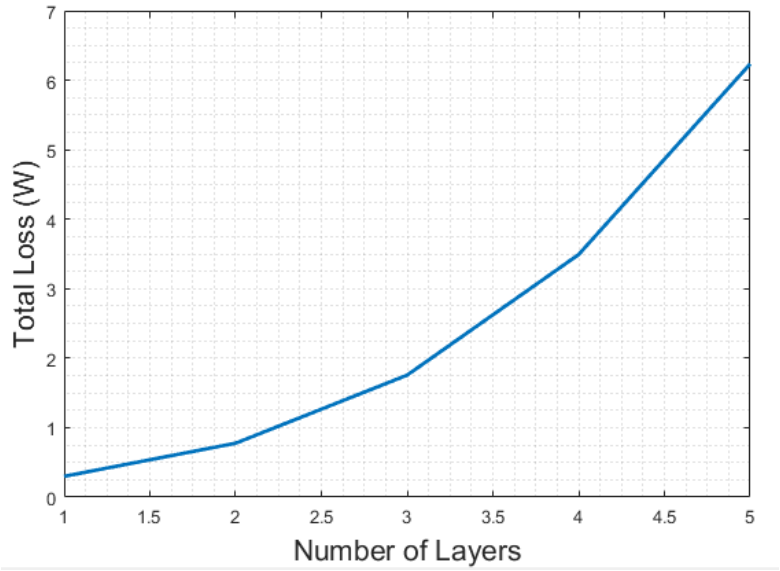

Figure 5-5 Total loss with multilayer windings

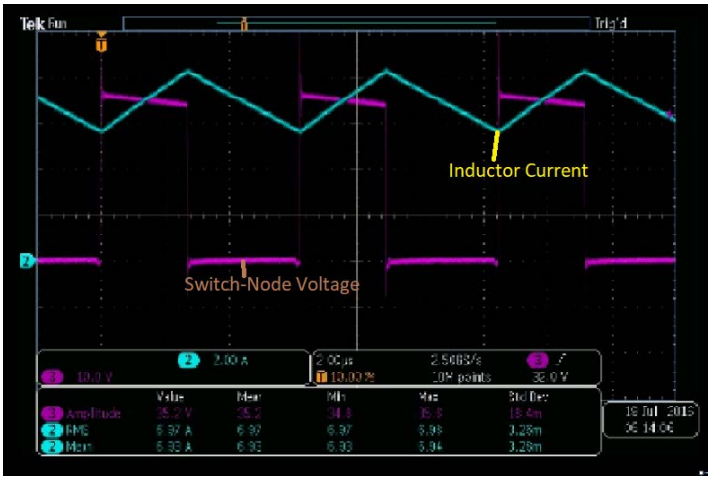

Figure 5-6 Experimental Waveform

The nanocrystalline core dimensions are shown as follows in Fig. 5-7 to Fig. 5-10.

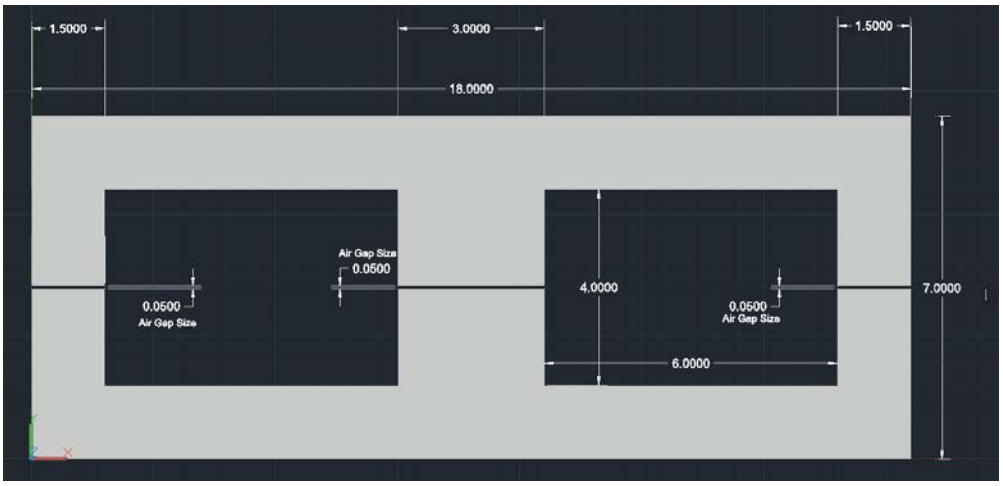

Figure 5-7 Front-View with Dimension

Figure 5-8 Top View of designed inductor

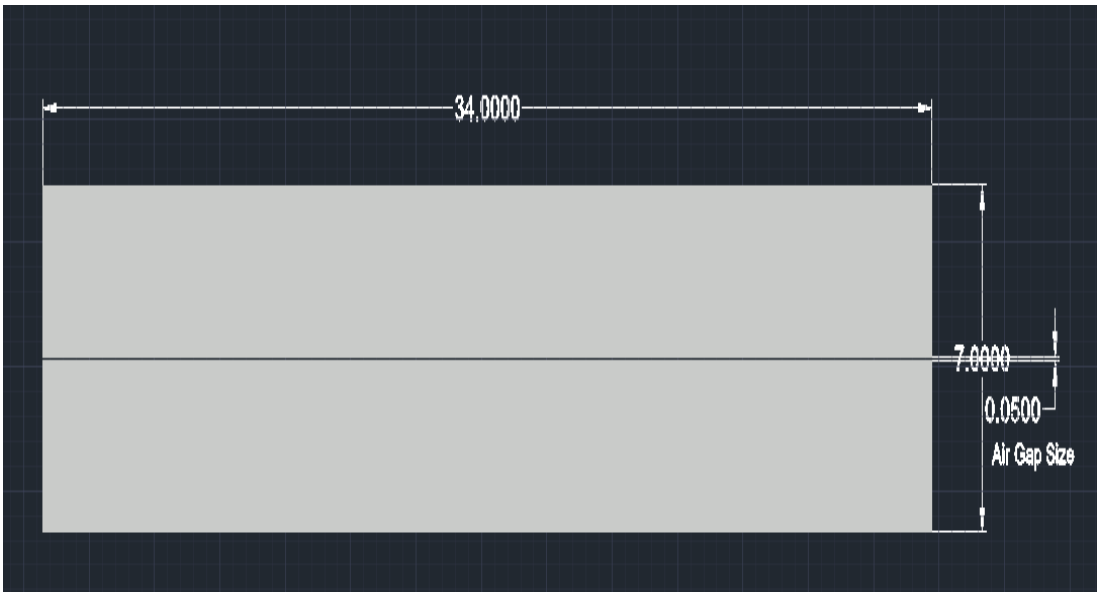

Figure 5-9 Side View of the designed inductor

Core dimensions:

Length: 34mm

Width: 18mm

Side leg width: 1.5mm

Air gap: 0.05mm

Height: 7mm

Window width: 6mm

Window height: 4mm

Center leg width: 3mm

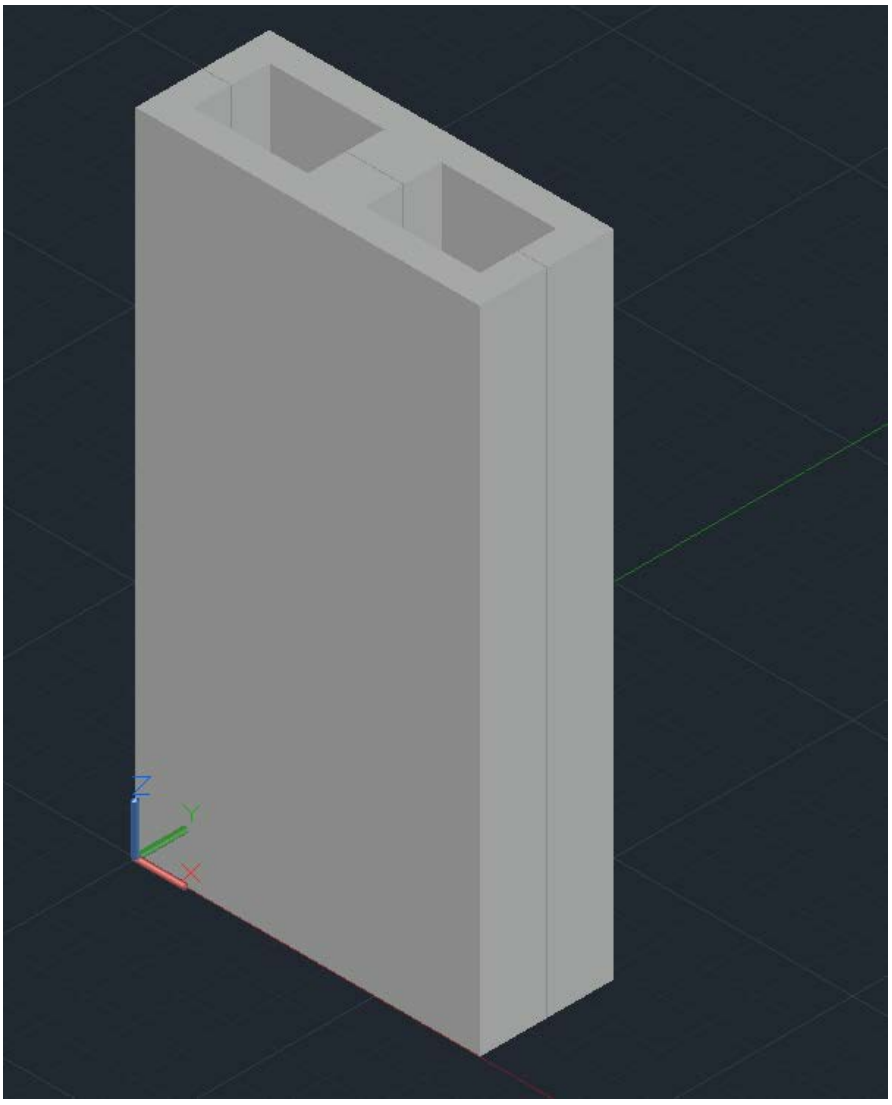

Figure 5-10 3-D projection of the Inductor

The copper layer winding plan is shown as follows in Fig. 5-11 to Fig. 5-16

Figure 5-11 Layer 1 of the designed inductor

Figure 5-12 Layer 2 of the designed inductor

Figure 5-13 Layer 3 of the designed inductor

Figure 5-14 Layer 4 of the designed inductor

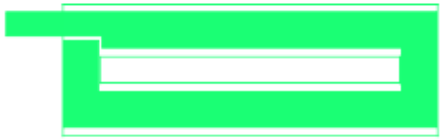

Figure 5-15 Layer 5 of the designed inductor

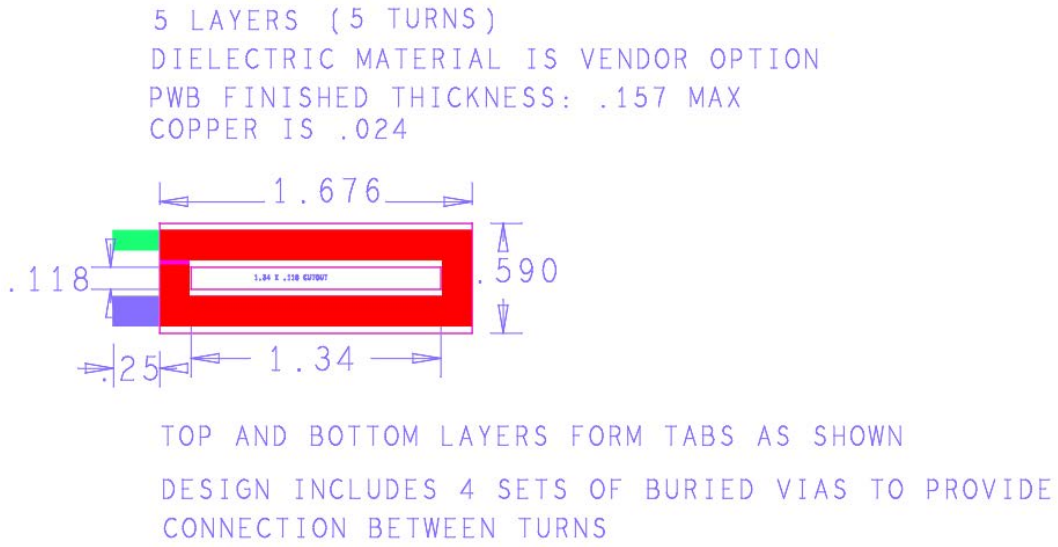

Figure 5-16 Winding layouts of the inductor

Figure 5-17 Prototype with the designed cores

Detailed analyses including proximity effect, skin effect, and fringing flux were carried for winding design with copper. Fig. 5-5 shows the loss plot with multiple layer winding and it is inferred that a single foil design provides the lowest loss for this window geometry. By considering the factors such as window height, insulation, manufacturing, etc. this inductor turns out to have 5 turns, total giving around 2.6 mΩ.

Finite Element Analysis (FEA) method was used to analyze the design in Ansys Maxwell. Fig. 5-18 to Fig. 5-23shows core loss, winding loss, magnetic flux density vector, current density vector, ohmic loss distribution and total loss distribution for boost mode respectively. Fig. 5-24 to Fig. 5-29 shows the same plots but for buck mode. In the FEA model, an actual buck/boost converter was used to drive the inductor at the design voltage and current. Note that, Core loss equation is provided by manufacturer (MK Magnetics, Inc) as the following: where K_0 is core constant, K_1 is frequency constant, K_2 is flux density constant, f_{sw} is switching frequency, and B_{pk} is peak flux density. Winding losses equations are given below and where F_f is conductor resistance increasing factor due to skin effect, G_f is the amount of winding losses due to proximity effect, R_{dc} is copper DC resistance, I_{pk} is peak current, H_{avg} is the average magnetic field strength, M is the number of layers, and N is the number of turns.

$$P_{core} = mass \times K_0 \times {f_{sw}}^{{f_{sw}}^{K_1}} \times {B_{pk}}^{K_2} \quad (5\text{-}1)$$

$$P_{proximity-effect} = G_f \times R_{dc} \times {H_{avg}}^2 \times N \quad (5\text{-}2)$$

$$P_{skin-effect} = F_f \times R_{dc} \times {I_{pk}}^2 \times M \times N \quad (5\text{-}3)$$

FEA method was used to analyze the design. Fig. 5-18 to Fig. 5-23 shows core loss, winding loss, current density vector, magnetic flux density vector, ohmic loss distribution and total loss distribution respectively.

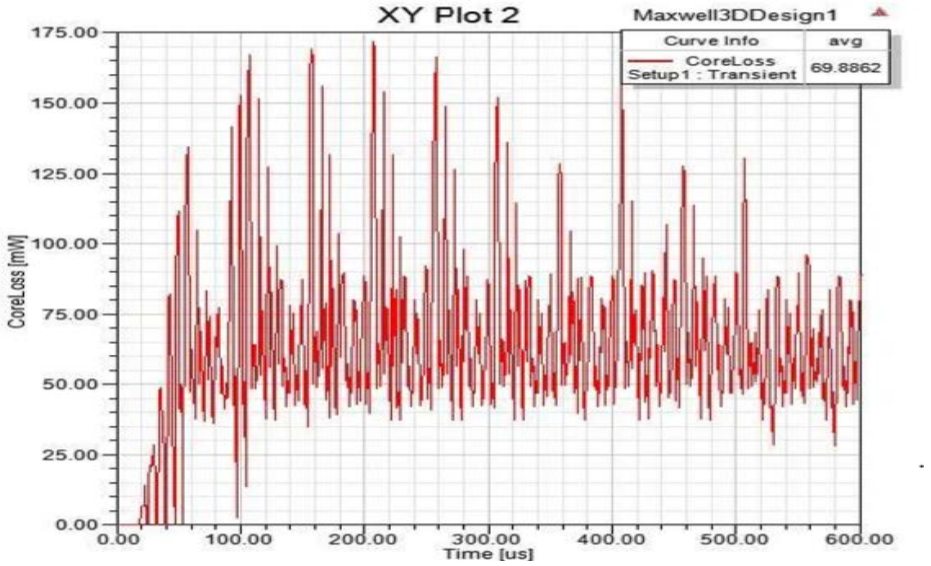

Figure 5-18) Core Loss in Buck mode

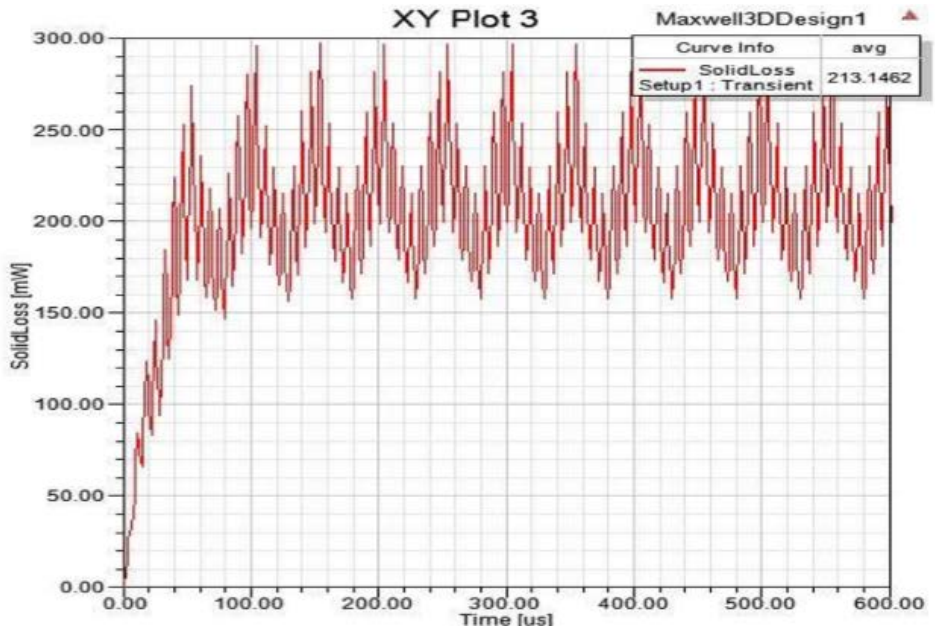

Figure 5-19 Winding Loss in Buck mode

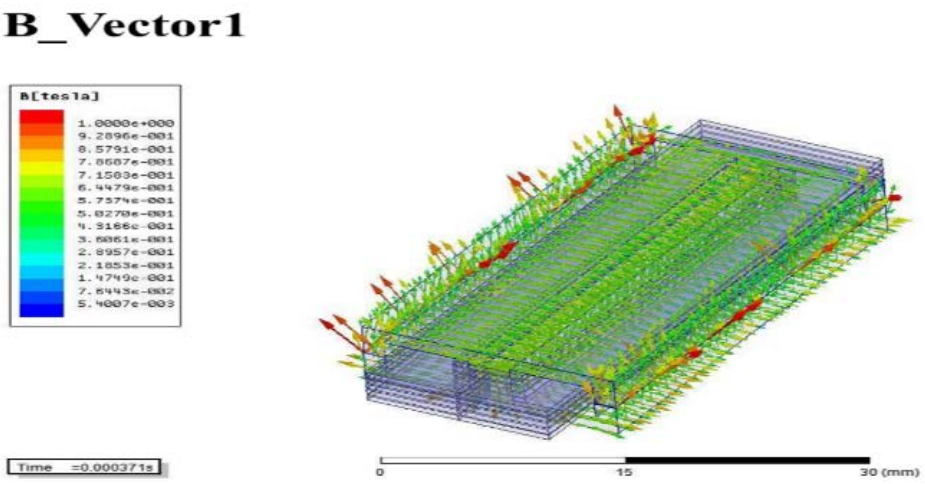

Figure 5-20 Magnetic Flux Density Vector in Buck mode

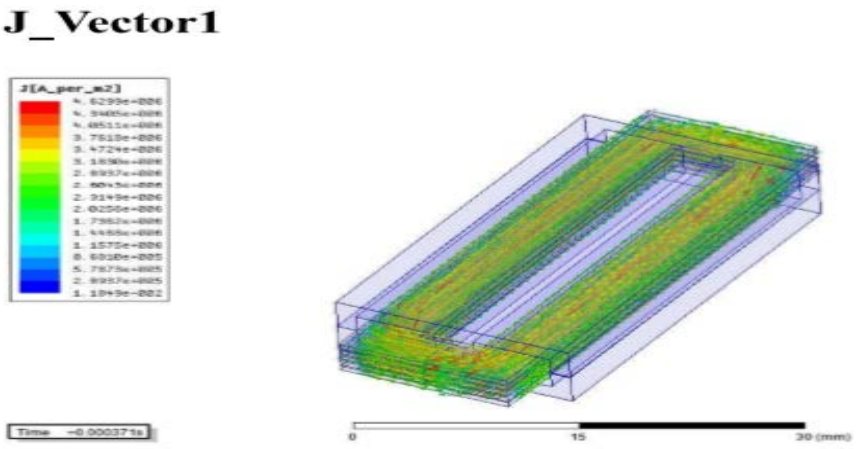

Figure 5-21 Current Density Vector in Buck mode

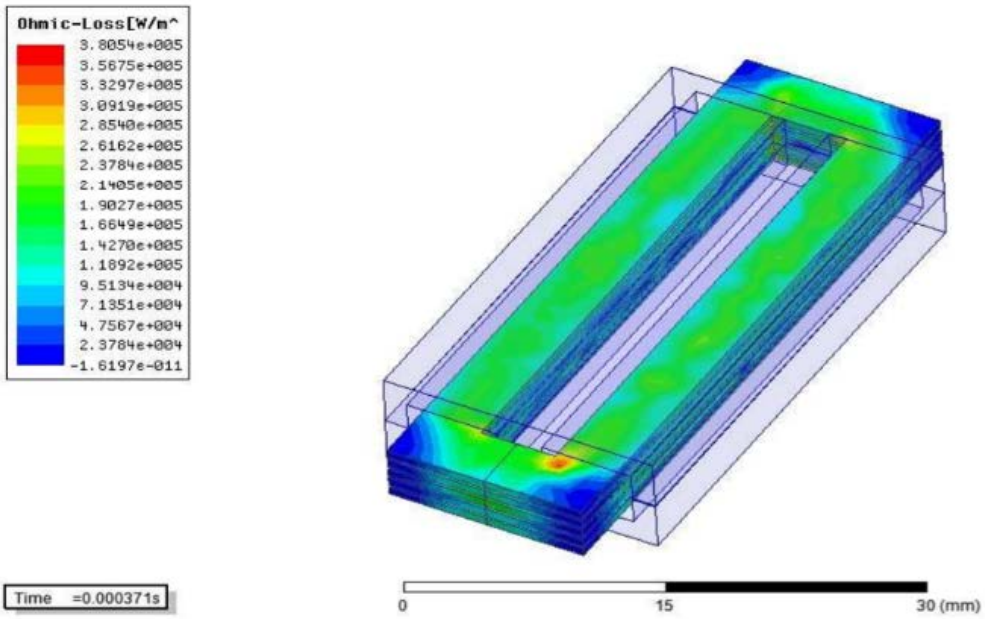

Figure 5-22 Ohmic Loss Distribution in Buck mode

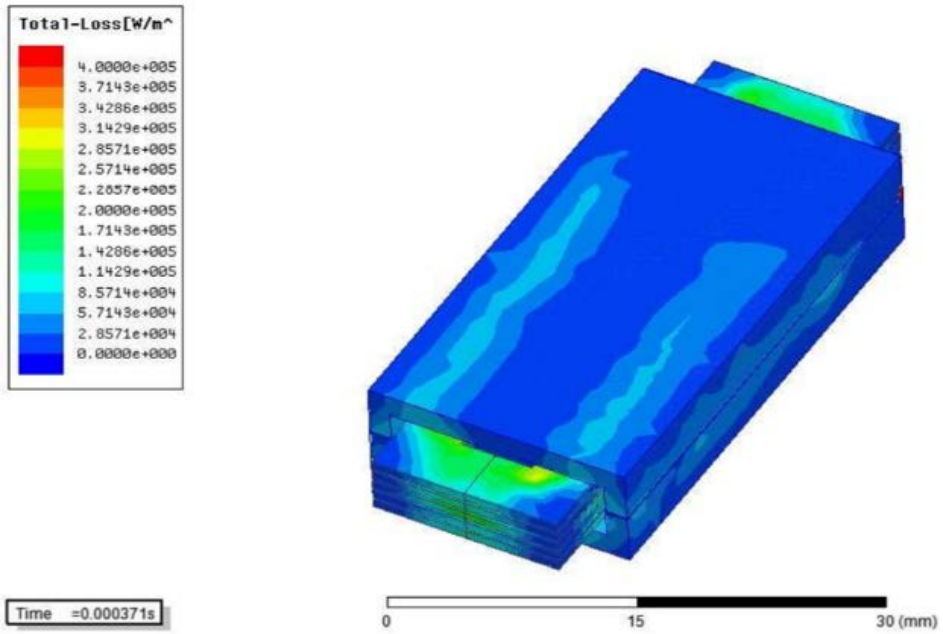

Figure 5-23 Total Loss Distribution in Buck mode

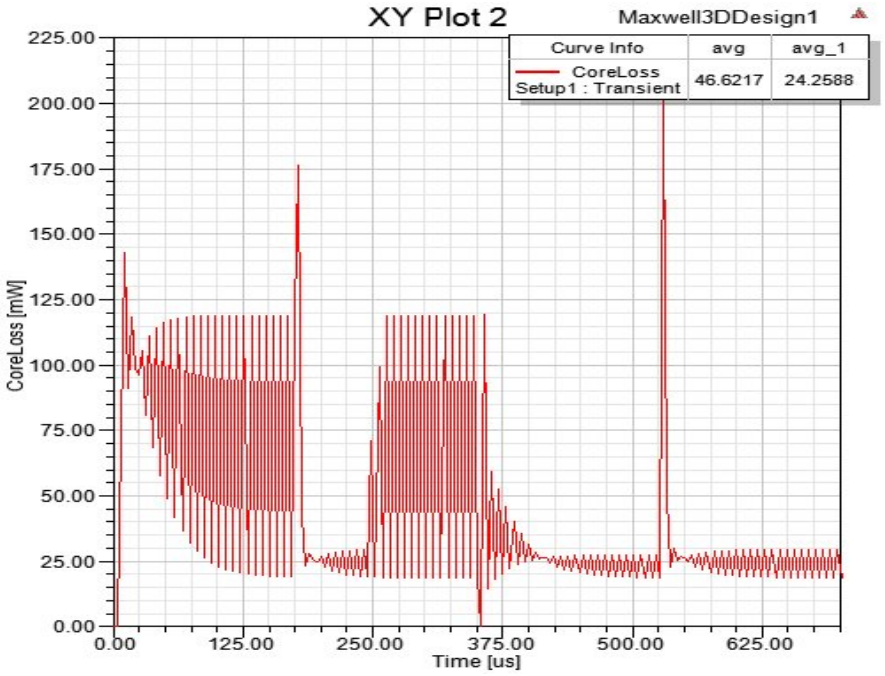

Figure 5-24 Core Loss in Boost mode

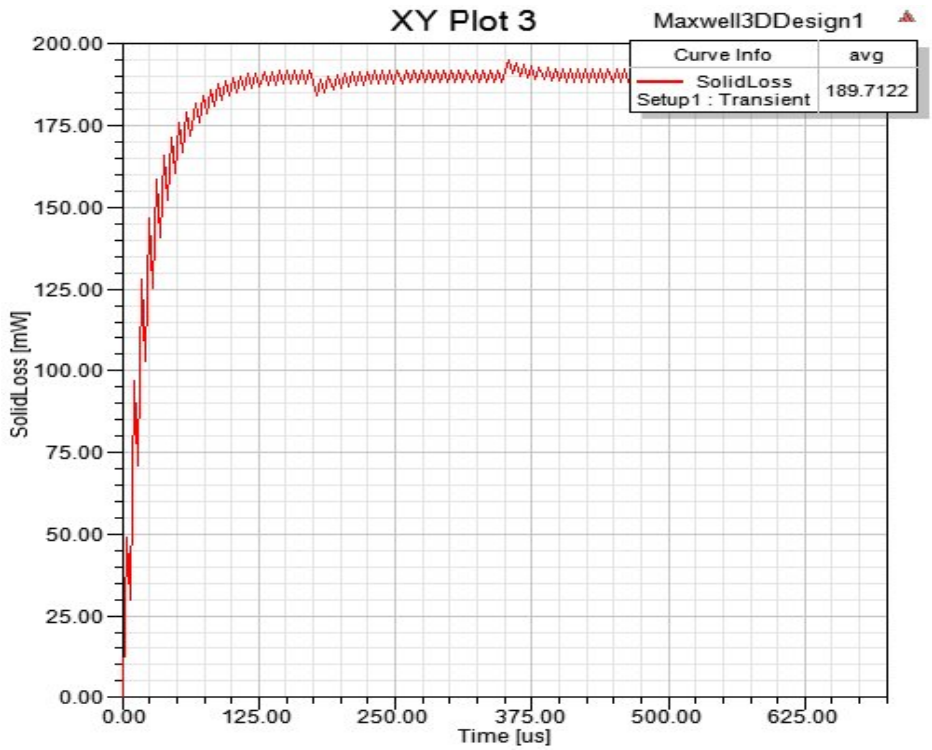

Figure 5-25 Winding Loss in Boost mode

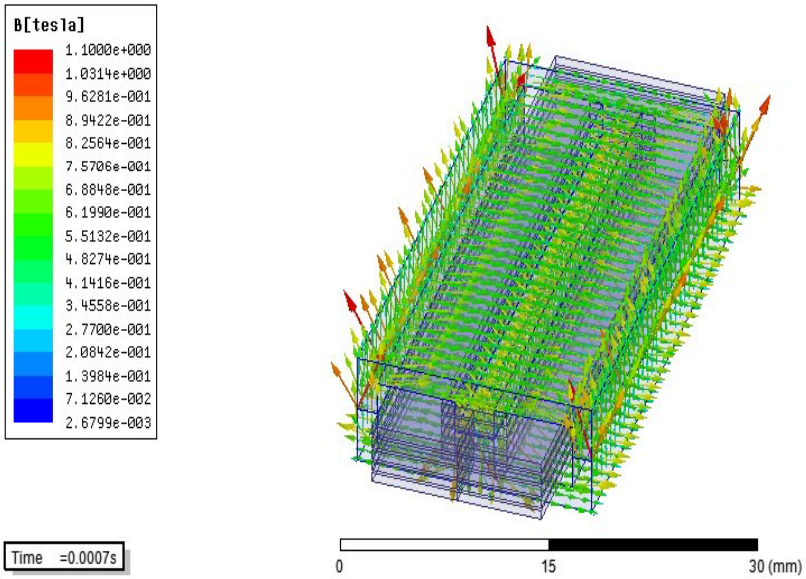

Figure 5-26 Magnetic Flux Density Vector in Boost mode

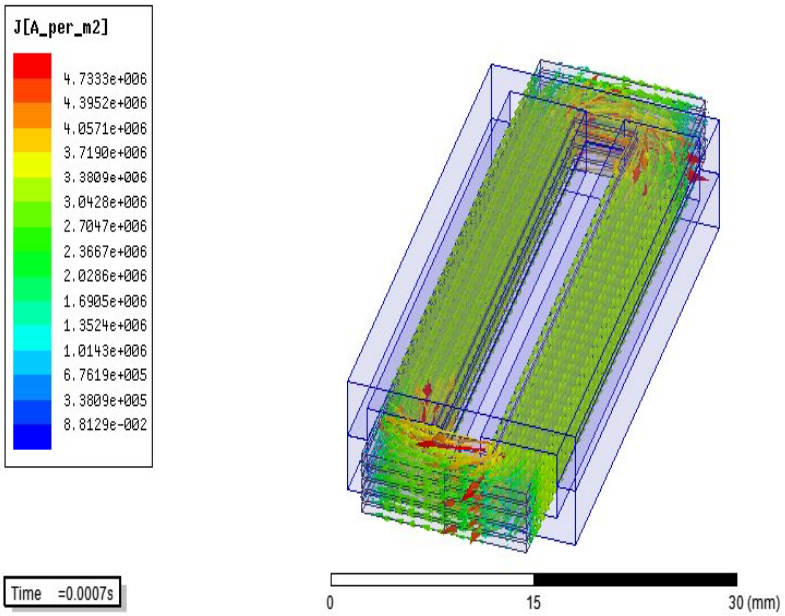

Figure 5-27 Current Density Vector in Boost mode

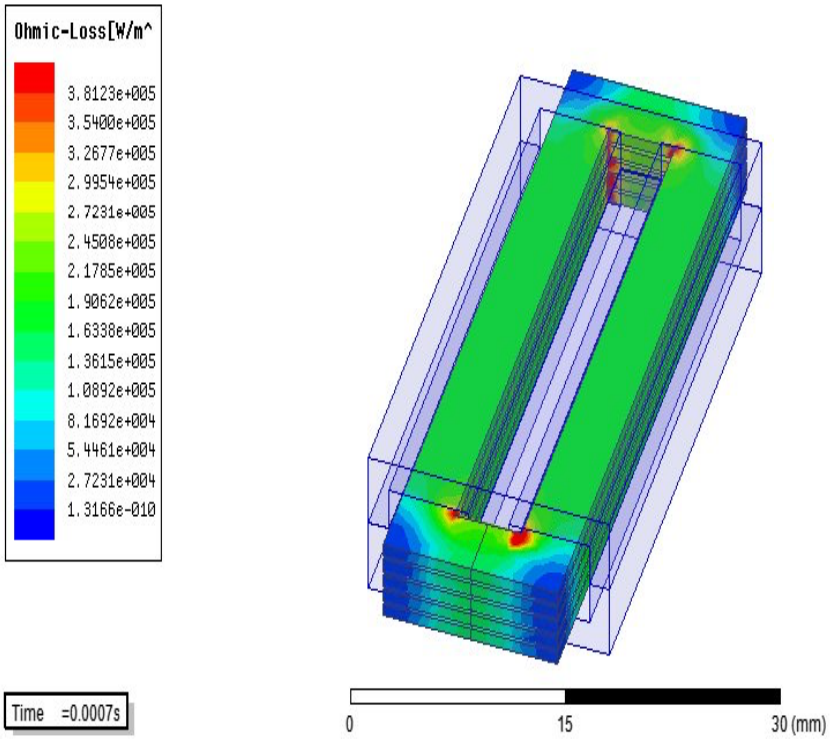

Figure 5-28 Ohmic Loss Distribution in Boost mode

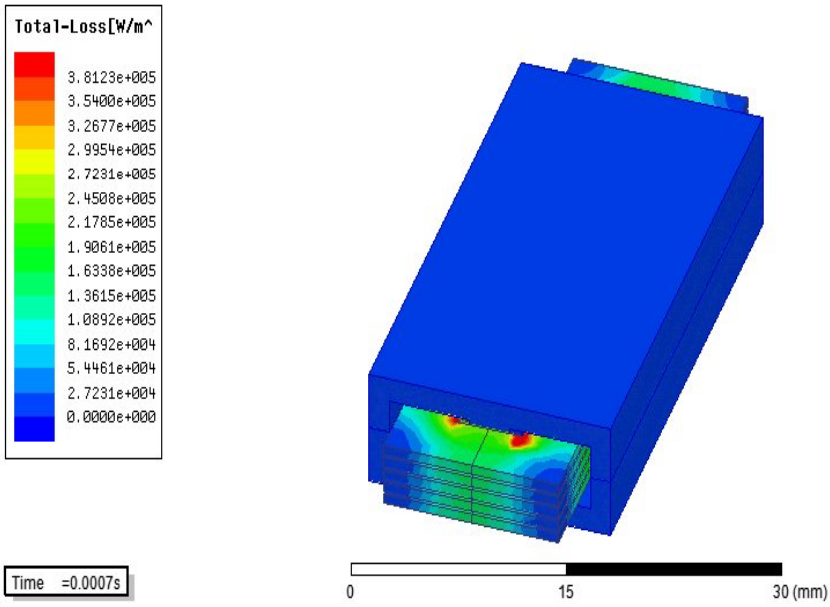

Figure 5-29 Total Loss Distribution in Boost mode

5.4 Practical Implementation:

As the designed part aimed at high fill factor, a printed circuit board was designed but was discarded for practical implementation because of cost and lead time. Further, laser cutting the winding out of a copper foil was also considered, however, the design was modified to have three turns and a longitudinal length of 51 mm (old dimension was 34 mm). This achieved about 26 μH. The experimental result for 12 V and 16.5 V output is shown as follows in Fig. 5-30. As it can be seen the designed part achieved a peak efficiency of over 99%. The designed part also achieved over 99 % efficiency at various other operating points such as 16.5 V to 33 V, 33 V to 16.5 V etc.

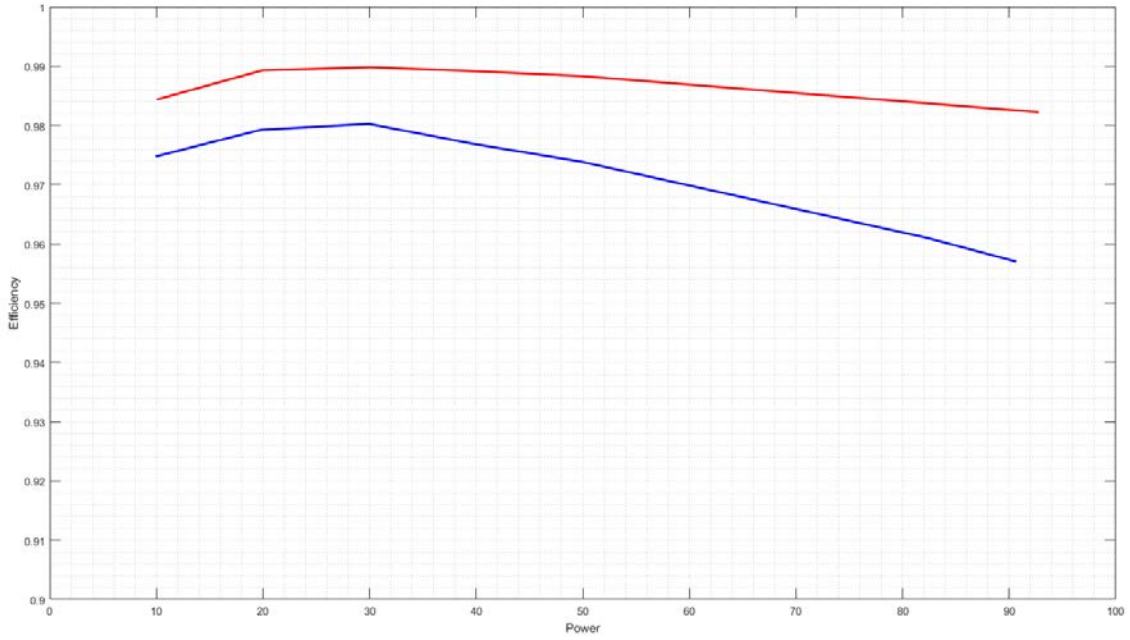

Figure 5-30 Experimental result with Nanocrystalline inductor (red) and Vishay inductor (blue) with output power in boost mode (12 V to 16.5 V).

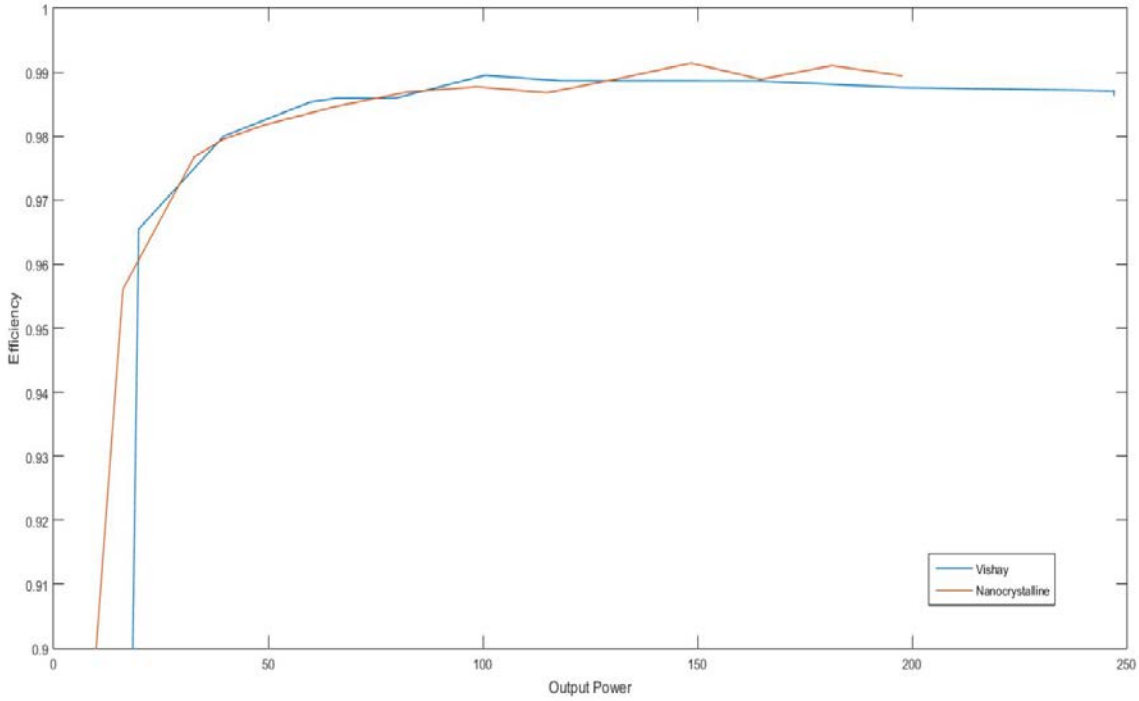

Figure 5-31 Experimental result with a Nanocrystalline inductor (red) and Vishay inductor (blue) with output power in buck mode (36 V to 33 V).

5.5 Reference:

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CHAPTER 6 CONCLUSION

An ultra-high efficiency Buck-Cascaded-Boost converter is designed with CEC weighted efficiency of 99.25 % and peak efficiency of 99.43 % with a power density of 6 kW/L and a height of only 7 mm. The optimization in efficiency is accomplished by developing a robust loss model and finding frequencies that correspond to lowest losses. These frequencies are incorporated with an adaptive-switching-frequency control technique. As the major losses are seen in the inductor, a planar-nanocrystalline inductor is developed and several design insights about the core and copper design are remarked. The inductor design is also validated and visualized with FEA method. Further experimental results and comprehensive details are discussed in this thesis.

APPENDIX A: DATASHEETS

MOSFET: BSC039N06NS

Link:https://www.infineon.com/dgdl/Infineon-BSC039N06NS-DS-v02_01-en.pdf?fileId=db3a30433727a44301372c3adce949c7

Inductor: IHLP6767GZ-01

Link: http://www.vishay.com/docs/34000/34000.pdf

Nanocrystalline Material: Metglas FT-3W

Link: https://metglas.com/wp-content/uploads/2016/12/FT-3W-Datasheet-Nov_2015.pdf

APPENDIX B: INDUCTOR DESIGN DETAILS

Airgap: 0.05 mm

Fringe Factor: 1.0046

L=30 μH

L = 22 μH (Practical)

Energy in the gap: 0.8455 mJ

Percentage of energy in the air gap: 94 %

$B_{peak} = 0.6105\ T$

$\Delta B = 0.1284\ T$

Ae=3*51 mm^2

Le=26 mm

$R_{dc} = 3.5\ m\Omega$

$R_{dc} = 4.5\ m\Omega\ (Practical)$

Skin effect=0.0327

Proximity Effect=0.2923

APPENDIX C: EXPERIMENTAL SETUP

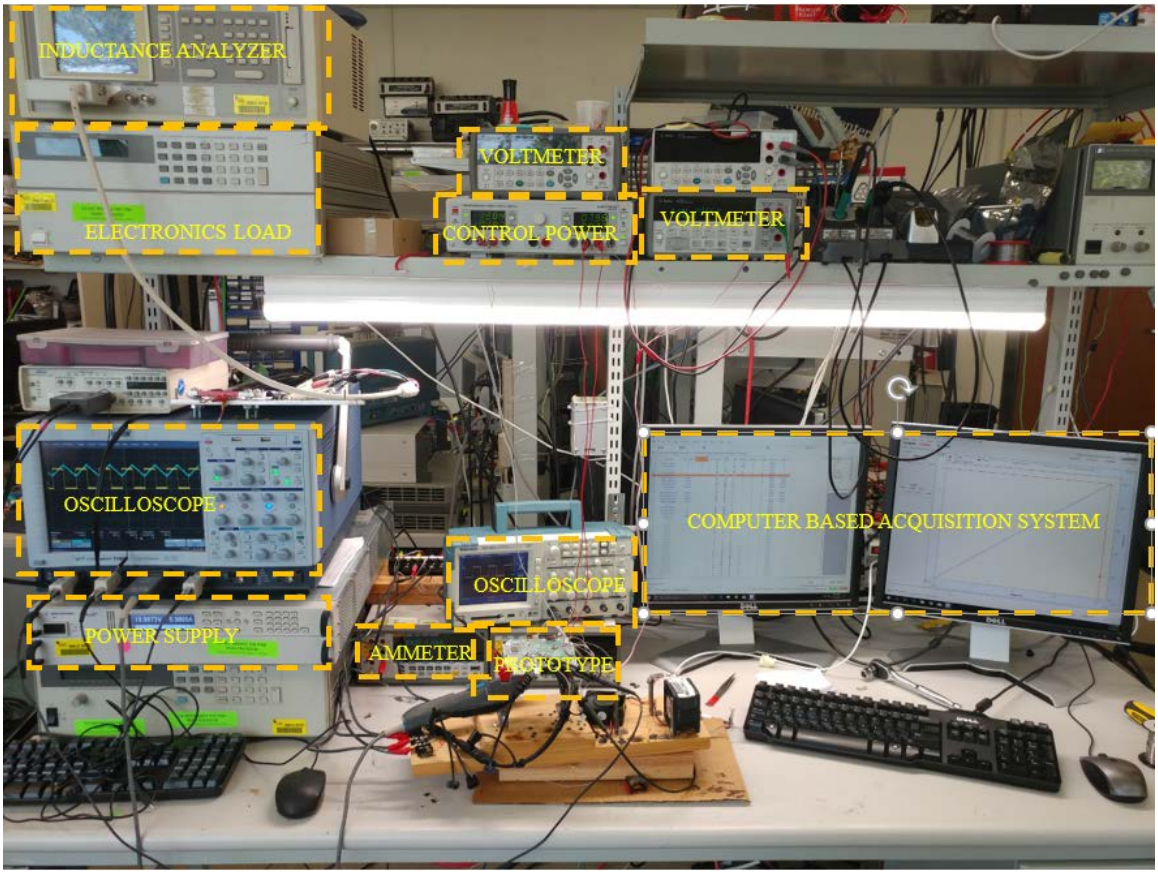

Figure A-0-1: Experimental setup

Description: Two voltmeters are used to measure input and output voltages and two ammeters are used to measure input and output currents. Power supply provide input power and the electronics load acts as load. An external power supply is used to supply control power. All the systems are connected to a PC (GPIO) with Agilent connection expert and APECOR interface suite. This forms the data acquisition system. All the efficiency curves are plotted by automation.