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HIGH QUALITY GATE DIELECTRIC/MoS_2 INTERFACES PROBED BY THE CONDUCTANCE METHOD

by

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ABSTRACT

Two-dimensional materials provide a versatile platform for various electronic and optoelectronic devices, due to their uniform thickness and pristine surfaces. We probe the superior quality of 2D/2D and 2D/3D interfaces by fabricating molybdenum disulfide (MoS_2)-based field effect transistors having hexagonal boron nitride (h-BN) and Al_2O_3 as the top gate dielectrics. An extremely low trap density of ~7×10^{10} states/cm^2-eV is extracted at the 2D/2D interfaces with h-BN as the top gate dielectric on the MoS_2 channel. 2D/3D interfaces with Al_2O_3 as the top gate dielectric and SiO_x as the nucleation layer exhibit trap densities between 7×10^{10} and 10^{11} states/cm^2-eV, which is lower than previously reported 2D-channel/high-κ-dielectric interface trap densities. The comparable values of trap time constants for both interfaces imply that similar types of defects contribute to the interface traps. This work establishes the case for van der Waals systems where the superior quality of 2D/2D and 2D/high-κ dielectric interfaces can produce high performance electronic and optoelectronic devices.

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CHAPTER 1: INTRODUCTION TO 2D MATERIALS

The scaling of silicon has reached its saturation making Moore's law obsolete. Increased rates of data transfer and performance are the main advantages of transistor scaling. But this transistor scaling comes at a price of pronounced short channel effects, such as increased leakage current, high static power dissipation etc.[1] Because of these aforementioned reasons, substitutes for conventional channel material becomes very critical. Numerous technologies have been studied for decades. With the isolation of single layer of graphene in 2004, two dimensional (2D) materials gained widespread recognition. Graphene is a 2D semi-metallic material with very high carrier mobility >50000 cm^2/V-s at room temperature having applications in high-speed electronic devices.[2, 3] However, the absence of band-gap in graphene *i.e,* the absence of OFF state in the graphene field effect transistors (g-FETs) has inspired further exploration of layered materials. Hence, other groups of 2D materials, such as Transitional metal dichalcogenides (TMDCs), hexagonal boron nitride (h-BN), black phosphorus etc. which possess a bandgap have gained prominence in electronic and optoelectronic applications. In this chapter, we discuss TMDCs in detail, with an emphasis on interface states in these 2D materials.

1.1 Transition metal dichalcogenides (TMDC)

The library of TMDCs consists of several members - MoS_2, WS_2, $MoSe_2$, WSe_2, $MoTe_2$, WTe_2, etc. which is aptly described in the periodic table as shown in the Figure 1.[4] The family of TMDCs offer various materials ranging from semiconductors (MoS_2, WSe_2), metals (TaS_2) and superconductors (FeSe, $NbSe_2$). Moreover, the bandgaps of these materials are tunable with the number of layers. For example, monolayer MoS_2 has a bandgap of 1.8 eV, with its bandgap decreasing with increasing layer numbers. Multilayer MoS_2 has a bandgap of 1.2 eV. Also, most of these TMDCs are direct bandgap at the monolayer level, and become indirect bandgap semiconductors with increasing layer numbers.

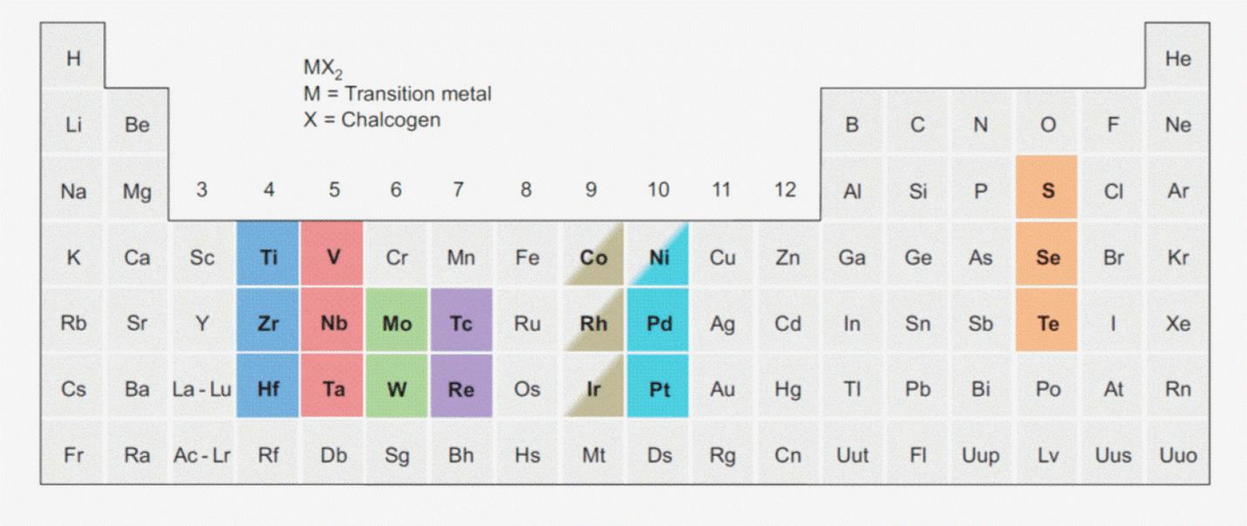

Figure 1: Periodic table depicting the TMDC library available with highlighted fields for chalcogen and transition metal atoms.

1.1.1 Crystal Structure of TMDC

2D materials consist of a layer of transition metal M bounded to two layers of chalcogen atom X forming MX_2 which can be semi-conducting, super-conducting or semi-metallic in nature.

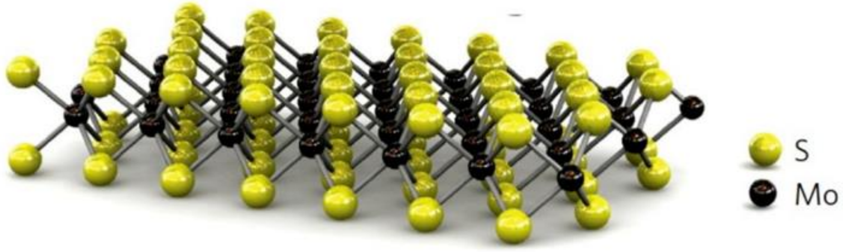

Figure 2: Crystal structure of MoS_2.

Crystalline TMDCs consists of chemically and mechanically robust monolayers of MX_2 bounded by weak van der Waals forces. Typically, a monolayer of TMDC are a few angstroms thick. The aforementioned weak van der Waals forces enable the facile exfoliation of atomically thin layers of TMDCs. This also aides in the assembly of distinct 2D materials to form heterojunctions. The early work started with the mechanical exfoliation of a single layer MoS_2 in 1966 using an adhesive tape[5] followed by chemical exfoliation.[6] Monolayer of MoS_2, an extensively studied material is ~0.65 nm thick and is shown in Figure 2. Other TMDCs like WS_2, WSe_2 have also been studied extensively for various electronic and opto-electronic applications.

1.1.2 2D Materials as Next Generation Channel Material

Most of the TMDCs have a bandgap in the range of 1-2 eV which makes them perfect for electronic and optoelectronic applications. This tunable band gap enables large switching ratios in the electronic devices. The fact that these materials have a relatively high carrier mobility enables them to be used as channel material for electronic devices.

The narrow mobile charge distribution due to the confinement of the charge carriers to the atomically thin semiconductors has garnered scientific interest. This confinement is modulated easily by the gate voltage which provides excellent gate electrostatics in devices with 2D materials as the channel.[7]

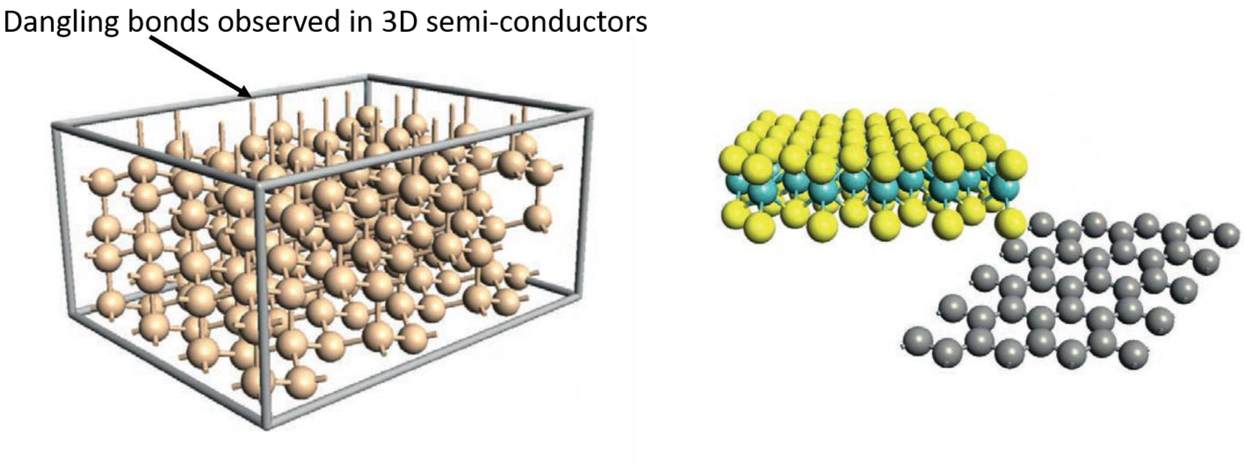

Figure 3: Figure showing surface morphology comparison of 3D and 2D semiconductors.

Furthermore, the surface morphology plays a significant role in advocating layered materials as next generation channel material due to the absence of out-of-plane dangling bonds indicating their pristine surfaces shown in the Figure 3. Conventional 3D semiconductors have out-of-plane dangling bonds which act as trap sites resulting in the performance degradation of the FETs. However, in 2D materials, the absence of out-of-plane dangling bonds is a clear indication of a high-quality interface with reduced interface traps. So, 2D material-based semiconductor system is capable of possessing a perfect trap-free interface which is critical for future electronic and optoelectronic applications.

1.2 Interface states in 2D materials

1.2.1 Interface states

A high-quality interface is required for a low subthreshold swing (SS) in field effect transistors, low dispersion in high frequency devices, high performance in solar cells and increased efficiency in optoelectronic devices. The full potential of the gate dielectric cannot be realized often, due to the potential drop across interface traps between the gate dielectric and the semiconductor. Therefore, it becomes essential to have an insight about the interface states of any semiconductor system for high performance devices.

Interface states arise from the trapped charges at the semiconductor/dielectric interface. These charges can be mobile ionic or fixed charges within the dielectric created during the fabrication process. The trap centers for the charges originate from the presence of dangling bonds in 3D semiconductors. These trap centers play an active role in determining the electronic properties of the device.

1.2.2 Interface Trapped Charges

It has been stated that interface-trapped charge Q_{it} are present within the forbidden energy gap due to the interruption of the periodic lattice structure of a crystal.[8] An interface trap becomes a donor interface trap by donating an electron and an acceptor interface trap by receiving an electron. The following expressions represent the distribution functions for the interface traps which are similar to those for the bulk impurity levels.

$$F_{SD}(E_t) = \frac{1}{1+g\exp\left(\frac{E_F-E_t}{kT}\right)} \tag{1.1}$$

For the donor interface traps where E_t is the interface trap energy and g ground state degeneracy. The g for the acceptor trap is 2 and for the donor trap is 4.

$$F_{SD}(E_t) = \frac{1}{1+\frac{1}{g}\exp\left(\frac{E_F-E_t}{kT}\right)} \tag{1.2}$$

The interface trap levels move with the conduction and the valence bands whereas the Fermi level remains fixed as the voltage bias is applied.[8] The movement of the trap levels is either up or down and when the interface trap crosses the Fermi level, the change in the charge occurs. This change in the charge contributes to the capacitance of metal-insulator-semiconductor (MIS) and the change is reflected in the capacitance-voltage curve shown in the Figure 4.

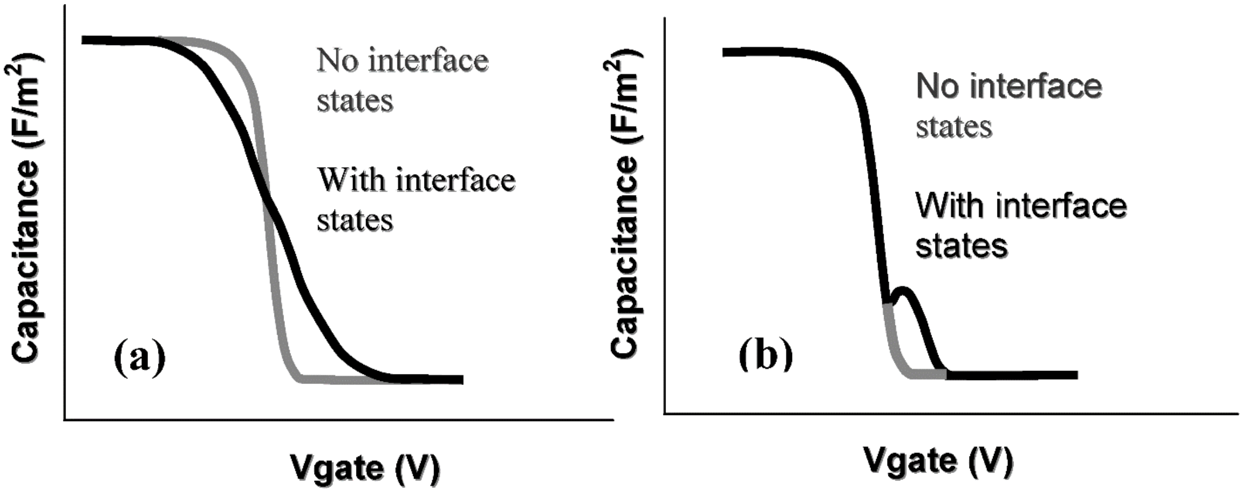

Figure 4: Capacitance stretch-out observed in the MOS-C with the presence of interface states.

1.2.3 Origin of Interface states in 2D materials

It is believed that the absence of out-of-plane dangling bonds contributes to high quality 2D channel/dielectric interface. However, the inherent defects present in the 2D materials will play a significant role in introducing the trap centers which degrades the performance of the device.

1.2.3.1 Defects in MoS$_2$

Despite the fact that a number of TMDCs show semiconducting behavior, MoS$_2$ is the most widely studied. This is due its availability in nature and the ease with which it can be mechanically exfoliated. The origin of the defects in MoS$_2$ has been extensively studied. During mechanical exfoliation of MoS$_2$, it has been observed that pits are formed on the surface of the material.[9] This variation in the morphology is one of the reasons for the formation of defects. Furthermore, the defects in MoS$_2$ are also caused by stoichiometric variations in the same layer of the material. These stoichiometric variations are because of the sulfur vacancies[9, 10] observed in the lattice of MoS_2 and also due to the presence of impurities like alkali metals[9] in the bulk crystal. Presence of these defects give rise to interface traps in the energy gap of the semiconductor. This degrades the performance of the device by causing the local carrier depletion and hence decreases the current in the devices. So, it becomes very critical to quantify the density of the interface states (D_{it}).

1.3 Objective of the Thesis

In this thesis we investigate the quality of MoS_2/ dielectric interface by quantifying the interface states using the conductance method. The experiment is conducted by using the MoS_2 FETs as the test structures to implement the conductance technique. We investigate the interface traps at MoS_2/h-BN and MoS_2/Al_2O_3 interface.

1.4 Overview of thesis

This work emphasizes on the extraction of density of interface traps (D_{it}) in MoS_2 based system. Chapter two deals with the extraction technique used in this work and the literature survey on the various techniques used to extract D_{it} in MoS_2 systems. Chapter three consists of detailed description of the device structure and fabrication. Chapter four deals with the experimental results, which include C-V, G-V characterizations of the devices, interface trap extraction, and effect of forming gas annealing on trap densities. Chapter five explains the future scope of this work.

CHAPTER 2: THE CONDUCTANCE METHOD

In this chapter we discuss the techniques by which D_{it} can be extracted in a semiconducting system. The conductance technique for D_{it} extraction is emphasized here, and its advantages over other techniques are noted. Finally, we provide a comprehensive overview of the interface trap densities extracted using various techniques for MoS_2-based devices that are reported in the literature.

2.1 D_{it} Extraction Techniques

Various techniques are implemented to extract D_{it}. The D_{it} is extracted using a Metal-Semiconductor-Oxide Capacitor (MOS-C). There are several techniques to extract the D_{it} such as low frequency methods and high frequency methods.

2.1.1 Low frequency Method (Quasi-static C-V)

The low frequency method is also known as the Quasi-Static Capacitance-Voltage (C-V) method.[11] In this method a low frequency C-V curve is compared with a high frequency C-V curve where the traps are assumed to be unresponsive. The low frequency capacitance denoted by C_{lf} is given by equation 2.1 for the depression-inversion region. Here, C_{ox} is the oxide capacitance, C_S is the semiconductor capacitance and the interface capacitance is given by C_{it}. Followed by this, the D_{it} is extracted by the equation 2.2[11]

$$C_{lf} = \left[\frac{1}{C_{ox}} + \frac{1}{C_S + C_{it}}\right]^{-1} \tag{2.1}$$

$$D_{it} = \frac{1}{q^2}\left[\frac{C_{ox}C_{lf}}{C_{ox} - C_{lf}} - C_S\right] \tag{2.2}$$

The C_S is calculated as a function of surface potential ϕ_S and gate voltage which introduces uncertainty in the estimation of C_S. Therefore, a simplified approach called as Castagné and Vapille method is used.[11]

2.1.2 Castagné and Vapille method

In this approach, the C_S is calculated from the high-frequency C-V curve given in the equation 2.3 where C_{hf} is the high frequency capacitance.[11]

$$C_S = \frac{C_{ox}C_{hf}}{C_{ox}-C_{hf}} \tag{2.3}$$

By substituting equation 2.3 in 2.1, the D_{it} is extracted as a function of capacitances at low and high frequencies as shown in equation 2.4.

$$D_{it} = \frac{C_{ox}}{q^2}\left[\frac{C_{lf}/C_{ox}}{1-C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1-C_{hf}/C_{ox}}\right] \tag{2.4}$$

2.1.3 Terman Method

This is one of the high-frequency methods employed to extract D_{it}. Here the capacitance is measured at high frequency assuming that interface traps do not respond to the high frequency ac signal but respond only to the slowly varying dc voltage.[11] The high frequency C-V stretch out is observed as a function of varying gate voltage. The stretch-out is due to the change in the trap occupancy. The D_{it} is given by the equation 2.5

$$D_{it} = \frac{C_{ox}}{q^2}\left[\frac{d\Delta V_G}{d\phi_S}\right] \tag{2.5}$$

This technique is applicable for extracting the D_{it} of 10^{10} /cm^2-eV and above. The technique tends to be inaccurate for thin dielectrics with non-negligible interface state capacitance, since it assumes the interface state capacitance to be zero.

2.1.4 Gray-Brown Method

This is a high-frequency capacitance technique measured at reduced temperatures. Typically, the measurements are performed at 77 K with a measurement frequency of 200 MHz. The reduction in the temperature causes the Fermi level to shift towards the majority carrier band edge and also increases the interface trap time constant (τ_{it}).[11]

2.2 Conductance technique for D_{it} extraction

In the conductance technique, the D_{it} is determined in the depletion and weak inversion region of the band-gap. This is a comprehensive extraction technique since it provides information regarding the surface potential fluctuations along with the capture cross-sections of the majority carriers. This technique is implemented by measuring the parallel conductance of the MOS-C as a function of frequency and the bias voltage applied. A more accurate estimate D_{it} is obtained since it is implemented using the parallel conductance.

The conductance technique, introduced by Nicollian and Goetzberger in 1967, is a sensitive method which yields accurate estimate of D_{it}. This technique is capable of determining the D_{it} of 10^9 /cm^2-eV and lower because of the response of the interface traps for applied bias voltage and frequency. This technique does not require any modeling to extract the D_{it} values, and the D_{it} can be obtained directly from the experimental results. The conductance method involves measuring the parallel conductance as a function of frequency and the bias voltage applied. The interface trap density is derived from the loss mechanism of the charge carriers by the capture and emission through the interface traps. The conductance method does not necessarily require a MOS-C structure and can be implemented on FET structures directly.

The simplified circuit of MOS-C shown in the Figure 5(a) consists of 3 different capacitances, C_{ox} is the oxide capacitance, C_S is the semiconductor capacitance and the interface capacitance is given by C_{it}. At the semiconductor/dielectric interface, the capture and emission of the charge carriers is due to the interface traps implying the process to be lossy which is represented by R_{it}. Figure 5(a) represents the simplified circuit. Here the R_{it} and C_{it} are replaced by a parallel conductance as shown in Figure 5(b) and C_S is replaced by C_P.

$$C_P = C_S + \frac{C_{it}}{1+(\omega\tau_{it})^2} \tag{2.6}$$

Here, $C_{it} = q^2 D_{it}$, $\omega = 2\pi f$ (f: measurement frequency), the interface trap time constant is given by τ_{it}; $\tau_{it} = R_{it}C_{it}$

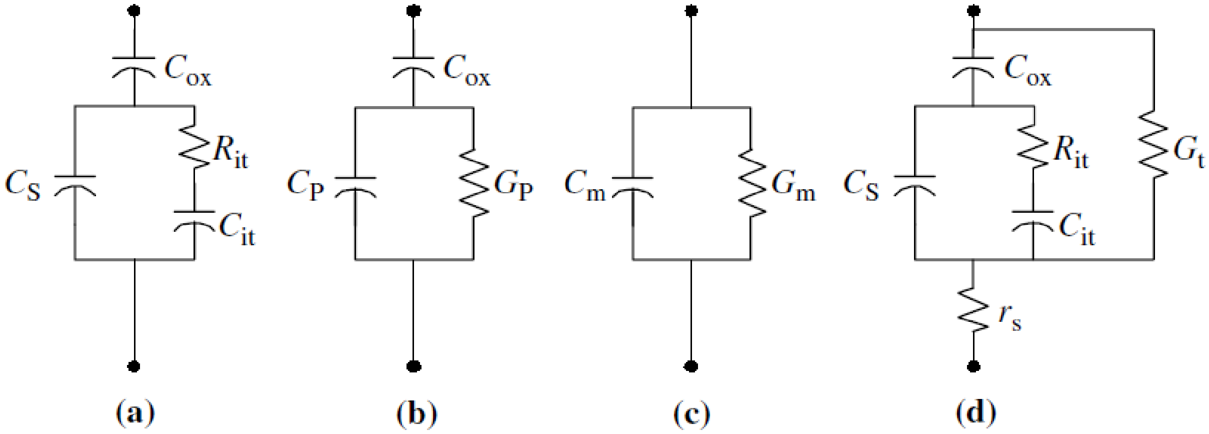

Figure 5 : Equivalent circuits used for implementing conductance techniques. (a) simplified MOS-C circuit for conductance measurements. (b) simplified circuit derived from (a). (c) measurement circuit. (d) measurement circuit including the tunnel conductance and G_t and series resistance r_s.

The parallel conductance is then divided by ω to give the equation,

$$\frac{G_P}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \tag{2.7}$$

The above equation is for the interface traps in one energy level. However, the interface traps at SiO_2/Si interface are distributed throughout the energy gap of Si. Therefore, the parallel conductance is normalized due to constant time dispersion. This normalization is carried out because the charge capture and emission are caused by the traps which are a few kT/q levels above and below the Fermi level. The normalized conductance is given below.

$$\frac{G_P}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}}\ln[1 + (\omega\tau_{it})^2] \tag{2.8}$$

The equations 2.7 and 2.8 indicate that the conductance is relatively easy to interpret than the capacitance due to the absence of C_S. The measured conductance is normalized and is a function of ω. Peak $\frac{G_P}{\omega}$ is obtained when $\omega = \frac{1}{\tau_{it}}$ and the corresponding D_{it} is given by $D_{it} = \frac{2\,G_P}{q\omega}$. From the above equation, $\omega \approx \frac{2}{\tau_{it}}$ and $D_{it} \approx \frac{2.5\,G_P}{q\omega}$ at maximum. Therefore, the D_{it} is determined at the maximum peak in $\frac{G_P}{\omega}$ plot against ω. For the corresponding ω, τ_{it} is calculated which provides an insight regarding the type of the traps at the interface.

From the Figure 6, it is evident that the $\frac{G_P}{\omega}$ plot is broader when compared to the trap profile extracted from the equation 2.8. It is attributed to the dispersion in the interface time constant caused by the surface potential fluctuations. These fluctuations are caused by the non-uniformities in the oxide charges, interface traps and doping density.

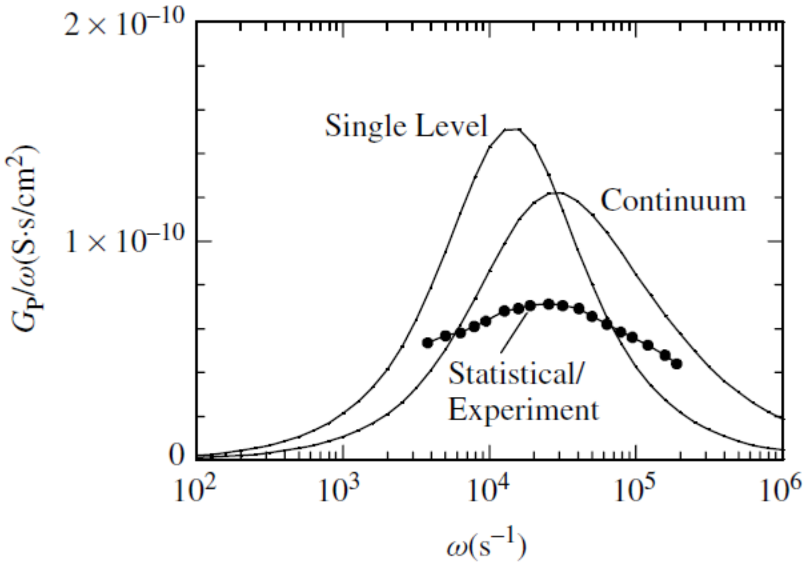

Figure 6 : $\frac{G_P}{\omega}$ *v/s* ω plot obtained from the equation 2.7 (single level) and 2.8 (continuum) and the experimental data.

Therefore, surface potential fluctuations need to be accounted for the extraction of the trap profile. In such cases, $\frac{G_P}{\omega}$ is given by,

$$\frac{G_P}{\omega} = \int_{-\infty}^{\infty} \frac{D_{it}}{\omega\tau_{it}} \ln\left[1 + (\omega\tau_{it})^2\right] P(U_S)\, dU_S \tag{2.9}$$

Where, $P(U_S)$ is the surface potential fluctuation probability distribution which is given by,

$$P(U_S) = \frac{1}{\sqrt{(2\pi\sigma^2)}} \exp\left(-\frac{(U_S - \bar{U}_S)^2}{2\sigma^2}\right) \tag{2.10}$$

Where, σ is the standard deviation whereas, $\bar{U}_S$ is the normalized mean surface potential.

Therefore, the expression for the D_{it} as a function of $\frac{G_P}{\omega}$ is given by

$$D_{it} \approx \frac{2.5}{q} \left(\frac{G_P}{\omega}\right)_{max} \tag{2.11}$$

The parallel conductance of a device is measured simultaneously with the parallel capacitance. Therefore, assuming negligible series resistance, $\frac{G_P}{\omega}$ can be calculated in terms of measured capacitance C_m, measured conductance G_m and the oxide capacitance C_{ox} which is given by

$$\frac{G_P}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \tag{2.12}$$

During the conductance measurements, the signal amplitude is kept at 50 mV or lower to prevent harmonics. The presence of these harmonics in the signal frequency can give false conductance values. One more noteworthy point would be that, for given D_{it} the corresponding conductance depends on the area of the device. For thin oxides, the series resistance will be considered. So, now the circuit consists of tunnel conductance G_t and series resistance r_s. Therefore, $\frac{G_P}{\omega}$ is given as

$$\frac{G_P}{\omega} = \frac{\omega (G_C - G_t) C_{ox}^2}{G_C^2 + \omega^2 (C_{ox} - C_C)^2} \tag{2.13}$$

Where,

$$C_C = \frac{C_m}{(1 - r_s G_m)^2 + (\omega r_s C_m)^2} \tag{2.14}$$

$$G_C = \frac{\omega^2 r_s C_m C_C - G_m}{r_s G_m - 1} \tag{2.15}$$

where, C_m and G_m are the measured capacitance and conductance. The series resistance is obtained by measuring the conductance and the capacitance in the accumulation region which is given by

$$r_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \tag{2.16}$$

where the G_{ma} and C_{ma} are the conductance and the capacitance measured in accumulation region. To determine the tunnel conductance, equation 2.15 is considered as $\omega \rightarrow 0$, equation 2.13 is reduced to equation 2.12, where $r_s = G_t = 0$.

2.3 Advantages of Conductance technique

The D_{it} extracted by conductance technique is accurate when compared with the capacitance methods. The complexity increases when the D_{it} is extracted by the capacitance methods because, the capacitance of a MOS-C consists of oxide capacitance, semiconductor capacitance, depletion-layer capacitance and interface capacitance. Therefore, extracting the D_{it} as a function of voltage and frequency through the capacitance measurements might give rise to inaccuracies because the difference of the capacitance needs to be calculated. This is not the case in the conductance technique, since the conductance is directly translatable to the response of the interface traps as the function of voltage and frequency.

The conductance technique is capable of probing the D_{it} of ~10^9 states/cm^2-eV and lower and entire band gap. This technique is capable of probing the interface traps in depletion and weak-inversion region.

The D_{it} is extracted based on the measured conductance of the MOS-C. No assumptions are made to quantify the D_{it}. Also, no model is used to extrapolate the D_{it} from the measured capacitance of the MOS-C as in the case of Terman Method. It is because of these advantages that we chose to use the conductance technique to analyze the interface states in MoS2-based FETs.

2.4 Literature on D_{it} characterization of MoS_2

Many different techniques have been used to extract D_{it} for MoS_2 based devices. Table 1 summarizes the D_{it}values obtained and the techniques used to extract the D_{it}.

Table 1: D_{it} values for MoS_2-based devices reported in literature.

Device Structure	Thickness	Type of MoS_2	Method of D_{it} Extraction	D_{it} Value (states/cm^2-eV)
MoS_2/ HfO_2[12]	7-layer MoS_2 13 nm HfO_2 4-layer MoS_2 8 nm HfO_2	Exfoliated	High low frequency method and multi-frequency	1.2×10^{13} $2\times10^{11} – 2 \times 10^{13}$
MoS_2/ HfTiO[13]	50-layers (32.5 nm) MoS_2 39.65nm HfTiO	Transferred by scotch tape	From SS	5.58×10^{12}
MoS_2/ Al_2O_3[14]	1-layer (0.85 nm) MoS_2 1nm Al_2O_3 seeding layer 15 nm Al_2O_3 dielectric	CVD		1.6×10^{13}
MoS_2/h-BN[15]	Single or bilayer MoS_2	Exfoliated by scotch tape	observed noise magnitude	6×10^{10} - 1×10^{12}
MoS_2/h-BN[16]	Tri-layer MoS_2	Exfoliated	High low frequency method and multi-frequency	$\sim10^{12}$
MoS_2/ZrO_2[17]	Few layers MoS_2 5.8nm ZrO_2	Transferred	From SS	1.7×10^{12}
MoS_2/ HfO_2[18]	Monolayer to tri-layer (0.7nm to 2.1nm) MoS_2 10nm HfO_2	Exfoliated	From SS	5×10^{12}
MoS_2/ Al2O_3[19]	30nm MoS_2 50nm Al_2O_3	Exfoliated	From SS	2.6×10^{11}

Device Structure	Thickness	Type of MoS_2	Method of D_{it} Extraction	D_{it} Value (states/cm^2-eV)
MoS_2/SiN_x[20]	140-layers MoS_2 250nm SiN_x	Exfoliated	From SS	1.14×10^{13}
$MoS_2/SiO_x/SiN_x$ [20]	125-layers MoS_2 50nm SiO_x 200nm SiN_x	Exfoliated	From SS	2.13×10^{12}
MoS_2/thermal SiO_2[20]	154-layers MoS_2 100 nm SiO_2	Exfoliated	From SS	3.32×10^{12}
MoS_2/Al_2O_3[21]	7 – 8 nm MoS_2 10 nm Al_2O_3	Exfoliated	Terman	1×10^{12}
MoS_2/HfO_2[21]	7 – 8 nm MoS_2 10 nm HfO_2	Exfoliated	Terman	2×10^{12}
MoS_2/HfO_2[10]	Monolayer MoS_2 5 nm HfO_2	CVD	High-low frequency method	7.03×10^{11}
MoS_2/Al_2O_3[22]	11.3 nm MoS_2 30 nm Al_2O_3	Exfoliated	Low Frequency Noise characterization	1.8×10^{12}
MoS_2/Al_2O_3[23]	15nm MoS_2 16nm Al_2O_3	Exfoliated	using CNF Model	2.4×10^{12}

2.5 Chapter Summary

In summary, we have discussed different techniques that can be employed to extract the D_{it}. Of all the techniques discussed, conductance technique is the most reliable method. Therefore, we have employed this technique to extract D_{it} at MoS_2/h-BN and MoS_2/Al_2O_3 devices. From the overview of the different techniques employed to study the D_{it} in the MoS_2 based systems, it can be understood that the conductance technique has not been employed yet to extract MoS_2 D_{it}.

CHAPTER 3: MoS_2 FET DEVICE FABRICATION

In this chapter we discuss the structure of the MoS_2 transistor adapted for the D_{it} extraction. We have fabricated MoS_2 transistors with 2D h-BN as the gate dielectric to investigate a 2D/2D interface. 2D/3D interfaces have also been fabricated using Al_2O_3 as the high-κ gate dielectric. The specific steps in the device fabrication are outlined here.

3.1 Device Structure

For the D_{it} extraction, the 2D channel considered is MoS_2 and h-BN is the 2D dielectric used. The D_{it} is also extracted at MoS_2 channel/ hi-k dielectric like Al_2O_3. To quantify the density interface states in 2D channel/ dielectric interface, dual gated MoS_2 Field Effect Transistor (FET) is fabricated.

3.1.1 Device Schematic

The schematic of the MoS_2 /h-BN FET is as shown in the Figure 7. The top gate contact is patterned such that there are underlapped regions near the source and drain. These regions are kept populated with electrons using the back gate voltage, so that series resistance can be minimized during capacitance and conductance measurements. The optical microscope image of the MoS_2/h-BN device is shown Figure 8.

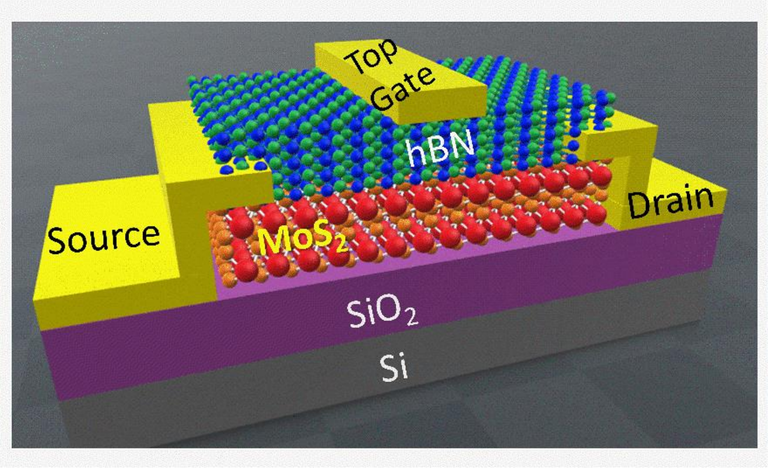

Figure 7 : Device schematic of MoS_2/h-BN FET.

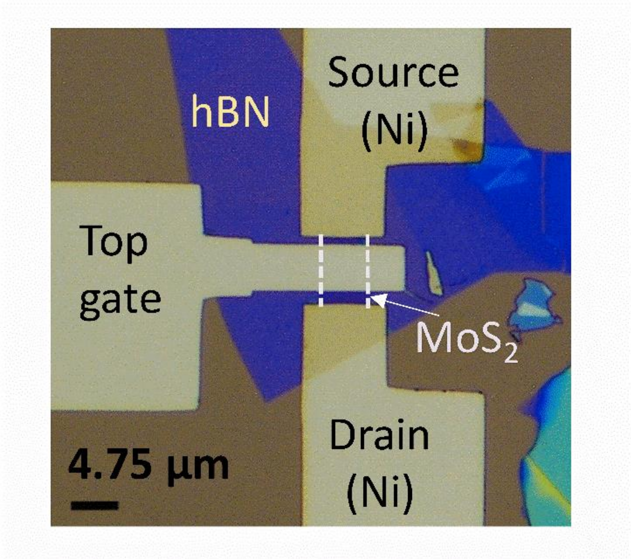

Figure 8 : Optical microscope image of MoS_2/h-BN device.

3.1.2 Scanning Electron Microscopy (SEM) of MoS_2 FET

The SEM image of the complete device is shown in the Figure 9. The SEM was performed with Zeiss Ultra 55 SEM.

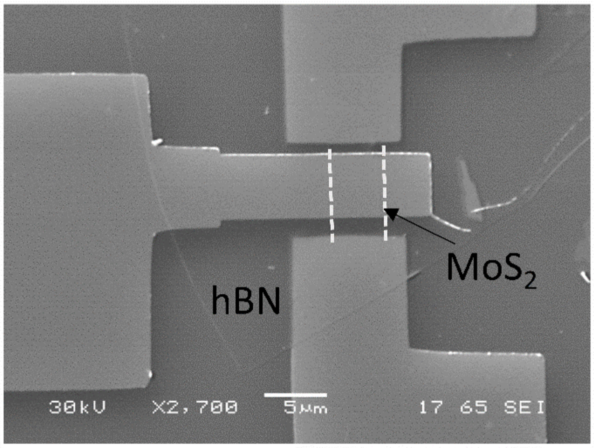

Figure 9 : SEM image of the MoS$_2$/h-BN device.

3.1.3 Transmission Electron Microscopy (TEM) of MoS$_2$ FET

To confirm the quality of layer stacking, cross-sectional transmission electron microscopy (TEM) is performed on a representative device with monolayer MoS$_2$ as the channel. Initially, a cross-section sample was lifted off using Helios Nanolab 600 Dual Beam Focused Ion Beam Milling System followed by the TEM characterization using JEOL 2010F operated at 200 kV acceleration voltage. Figure 10 shows the cross-sectional TEM micrograph of the MoS$_2$/h-BN layer stacked on SiO$_2$ substrate followed by Nickel top gate. Monolayer MoS$_2$ can be clearly seen on the SiO$_2$ substrate. Multilayer structure stacked on the MoS$_2$ layer had a interlayer spacing of ~0.34 nm corresponding to h-BN, and the van der Waals interface between MoS$_2$ and h-BN was clean, highly coherent and free of any structural disorders.

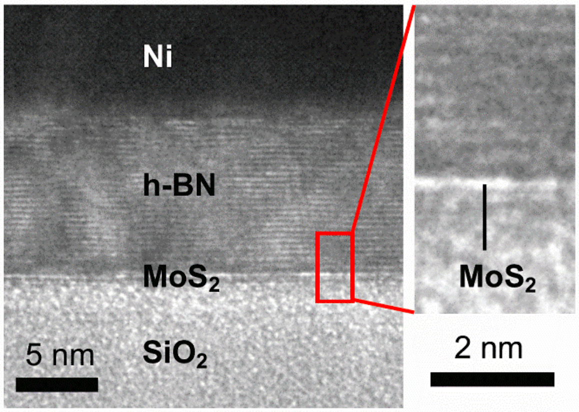

Figure 10 : cross sectional TEM of a representative monolayer MoS_2 FET with h-BN dielectric. (Courtesy: Supriya Koul and Professor Akihiro Kushima, UCF)

3.2 Fabrication procedure

The MoS_2 FETs are fabricated using multiple lithography processes. E-beam lithography is used to fabricate dual gated MoS_2 FETs.

3.2.1 Alignment marks patterning using photolithography

The starting substrate for the device fabrication is 260 nm thermally grown SiO_2 on p+ Si wafers.. The device fabrication starts with the alignment marks patterning using conventional photolithography on the SiO_2/Si substrate. These marks are used to locate 2-7 nm thick MoS_2 flakes, and are used during e-beam lithography for the alignment. The patterning is carried out with positive resist S1813 from Microposit. The resist is spin-coated at a speed of 4500 rpm with an acceleration of 300 rpm/sec for 1 minute. The soft-baking is carried out for spin-coating for 1 min at 115 ºC. MJB 4 Karl Suss Aligner is used for the alignment and exposure. The exposure dose is 10.21 mJ/cm^2 and the exposure is done for 9 s. After the exposure, the patterns are developed in CD-26 resist developer for 35 s.

3.2.2 Mechanical Exfoliation of MoS_2 flakes

The device fabricated consists of MoS_2 flake (SPI supplies) 3-10 layers thick as the channel material. The MoS_2 flake is isolated by mechanical exfoliation using Scotch-tape method where few layers of MoS_2 are cleaved from the bulk MoS_2 using scotch tape and then transferred on the patterned Si/SiO_2 substrate. After the exfoliation, the flakes of desired thickness are located on the substrate.

3.2.3 Back-gated MoS_2 FET fabrication

The patterning of the device is carried out by e-Beam lithography. This lithography procedure requires the mask design for individual flakes. The sample is spin-coated with MicroChem 950 PMMA C4 e-beam resist (positive). The spin coating is done at 2 different speeds. At first, the resist is spun at 500 rpm for 30 s followed by 4000 rpm for 30 s. The sample is then soft-baked at 130 °C for 3 mins. The e-beam lithography is carried out using Zeiss Ultra 55 scanning electron microscope (SEM) integrated with Nanometer Pattern Generation System (NPGS). The contact fingers are smaller and are written at a current ~ 100 nA with a dose of 350 $\mu C/cm^2$ while the contact pads which are larger are written with a current of ~1.4 nA and the similar dose as before. Then, the development is done by immersing the sample in a mixture of MIBK: IPA in the ratio of 1:3 for 45 seconds followed by an IPA bath for 1 min.

The evaporation is carried out after the patterning for the lift-off of the metal. The e-beam evaporation is carried out in Thermionics system. 30 nm of Nickel is deposited at a pressure of 4×10^{-6} Torr as the contact metal. After the deposition, lift-off is carried out by immersing the sample in the Acetone bath at 60 °C for 25 mins. This completes the fabrication of back-gated MoS_2 FET.

3.2.4 Top-gated MoS_2 FET fabrication

3.2.4.1 Dielectric deposition by dry transfer of h-BN flakes

The top-gated FET fabrication procedure is explained as follows. For the fabrication of the MoS_2 FET with h-BN top gate dielectric, a dry transfer technique is used. For the dry transfer of h-BN, mechanical exfoliation of h-BN using scotch tape is carried out on the visco-elastic stamp. Followed by this, mapping of h-BN flakes of thickness ~13 nm is carried out. After this, the h-BN flakes are transferred on the MoS_2 channel. Then, the top gate contact is patterned using e-beam lithography and 30 nm Ni is deposited as the contact metal followed by lift-off in an acetone bath. This marks the end of the MoS_2/ h-BN device fabrication.

3.2.4.2 Dielectric deposition by Atomic Layer Deposition (ALD)

Due to the absence of dangling bonds, the deposition of dielectrics by Atomic Layer Deposition (ALD) is not uniform. Therefore, nucleation layer is deposited prior to ALD for functionalizing the top surface of MoS_2.[24-26] This nucleation layer aides for the uniform deposition of the dielectric. Two different nucleation layers, such as AlO_x and SiO_x of 1.5 nm thickness are deposited.

For the seeding layer deposition, 1.5 nm Al and SiO_x is e-beam evaporated and left to oxidize in air for a few minutes. The stoichiometric composition of the oxide layer formed is AlO_x and SiO_x. Followed by this, ALD (Cambridge Nanotech) is carried out. 8.5 nm thick Al_2O_3 is deposited at 250 °C at 85 mTorr using Trimethylaluminium (TMA) and H_2O precursors. After the dielectric deposition, the top-gate is patterned by e-beam lithography and 30 nm Ni e-beam evaporated as the contact metal, followed by lift-off.

3.3 Chapter Summary

Dual gated MoS_2 FETs are fabricated. 3 types of devices were fabricated for the D_{it} extraction. Devices with Al_2O_3 gate dielectric were fabricated using AlO_x and SiO_x seeding layer. MoS_2 FETs with h-BN gate dielectric were also fabricated.

CHAPTER 4: EXPERIMENTAL RESULTS

In this chapter, we report the capacitance-voltage and conductance-voltage characteristics of the fabricated devices. We extract the interface trap densities using the conductance method for the MoS_2 FETs. Initially, the D_{it} was extracted for the pristine devices and is followed by the studies of effect of forming gas annealing on the D_{it}.

4.1 Pristine device characteristics

Before the dielectric deposition and further processing, the characteristics of the back-gated MoS_2 FET is tested to investigate the conductivity of the MoS_2 flake because the micro-tears between the electrodes will cause the open circuit restricting the flow of the current. The back-gated current-voltage (I-V) characteristics of a representative MoS_2 FET shown in the Figure 11.

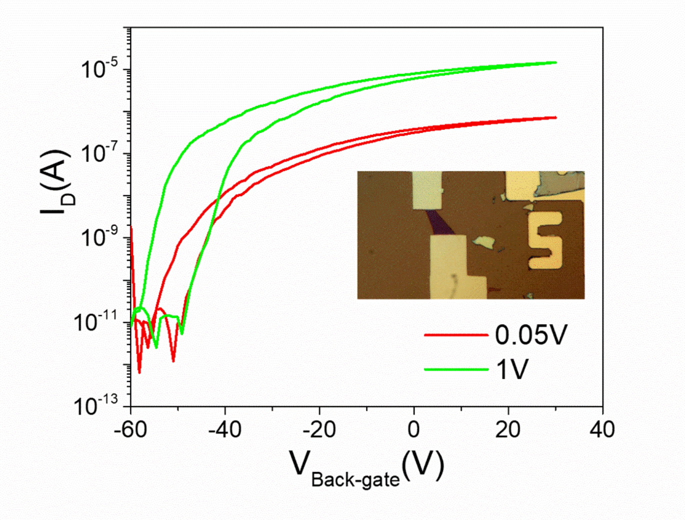

Figure 11 : Back-gated I-V of MoS_2 FET. Inset: The device on which the back-gated I-V characterization was performed.

4.1.1 Current-Voltage (I-V) Characteristics

After the completion of fabrication of the top-gated devices, the electrical measurements were performed on the devices. At first the top-gated I-V is carried out. For this measurement, the bias is applied on the top-gate by keeping the back-gate at 0 V. Figures 12, 13 and 14 show the transfer characteristics of the FETs with AlO_x/Al_2O_3, SiO_x/Al_2O_3 and h-BN top gate dielectrics, respectively at $V_D = 50\, mV\ \&\ 1\, V$. The subthreshold swing (SS) is calculated from the I-V characteristics. The SS of the MoS_2 FET with AlO_x/Al_2O_3 gate dielectric is 160 mV/decade (Figure 12), with SiO_x/ Al_2O_3 gate dielectric is 180 mV/decade (Figure 13) while the SS of the device with h-BN gate dielectric is 140 mV/decade (Figure 14).

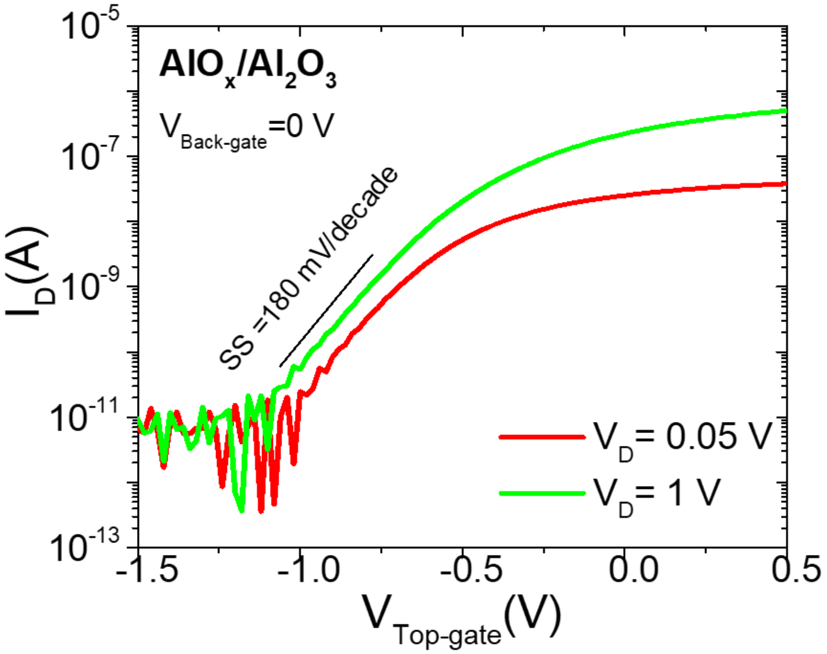

Figure 12 : Transfer characteristics of top-gated MoS_2 /Al_2O_3 device with AlO_x seeding layer.

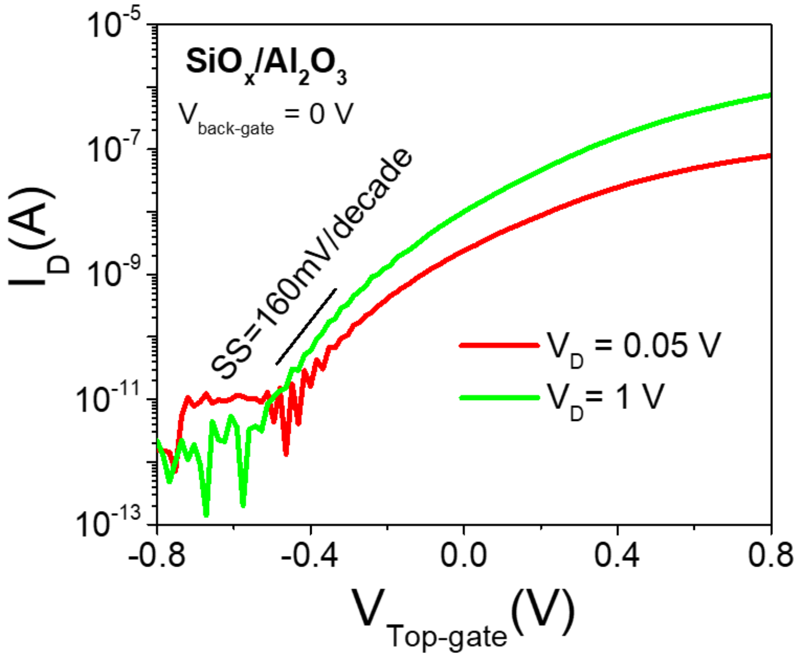

Figure 13 : Top-gated transfer characteristics of MoS_2 /Al_2O_3 device with SiO_x seeding layer.

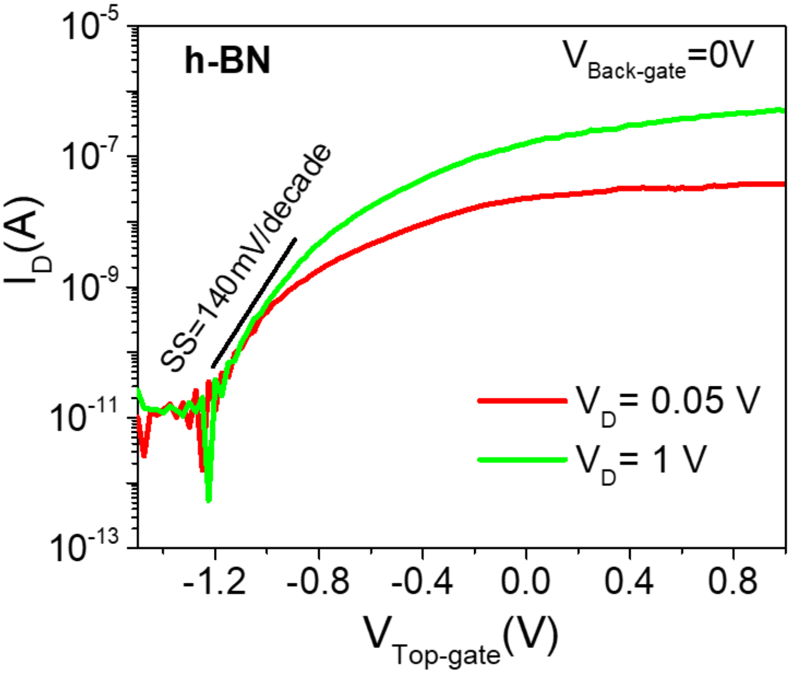

Figure 14 : Top-gated transfer characteristics of MoS_2 FET with h-BN dielectric.

After the I-V characterization, Capacitance-Voltage (C-V) measurements are carried out. For these measurements, we shorted the source and drain and connected them to the 'low' terminal of the capacitance measurement unit (CMU). We modified the bias on the 'high' terminal of the capacitance measurement unit that was connected to the top gate electrode. The back gate was grounded at 0 V. Since in our depletion mode MoS_2 FET, the channel is quite populated with electrons at V_{BG} = 0 V, keeping the underlapped channel regions conductive.

4.1.2 C-V and G-V characteristics

Figure 15 shows the equivalent circuit model of the capacitances and resistances that come into play while measuring the capacitance between the gate electrode and the source/drain electrodes. The MoS_2 FET consists of various capacitances semiconductor capacitance C_{body}, interface capacitance C_{it} and oxide capacitance C_G represented by C_m and corresponding conductance G_m.

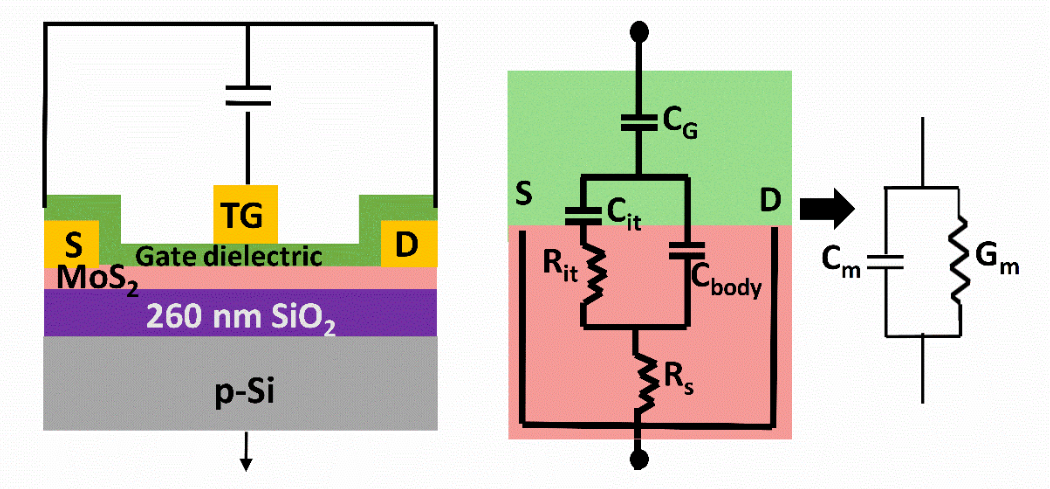

Figure 15 : Capacitance model for the MoS_2 FET.

Before, the measurements the CMU is calibrated first. The CMU is first open calibrated by keeping all the terminals open. Followed by this, the short calibration is performed by connecting the top-gate terminal and the common source and drain terminal on a metal bar. The calibration is performed for the frequencies ranging between 1 kHz to 5 MHz. After this, the C-V program is executed in open circuit to make sure the RMS value of the capacitance as measured by the CMU is ~0 F. The device is always swept from accumulation to depletion region for multiple discrete frequencies *viz.*,1 kHz, 5 kHz, 10 kHz, 20 kHz, 50 kHz, 100 kHz and 200 kHz. The gate voltage is superimposed with an ac signal of amplitude 50 mV. The measurements were done with high integration factor (slow) which allows the interface traps to respond to the applied bias. The C-V characteristics of the pristine MoS_2/Al_2O_3 devices with AlO_x and SiO_x, and the MoS_2/h-BN device are shown in the Figures 16, 17 and 18 respectively.

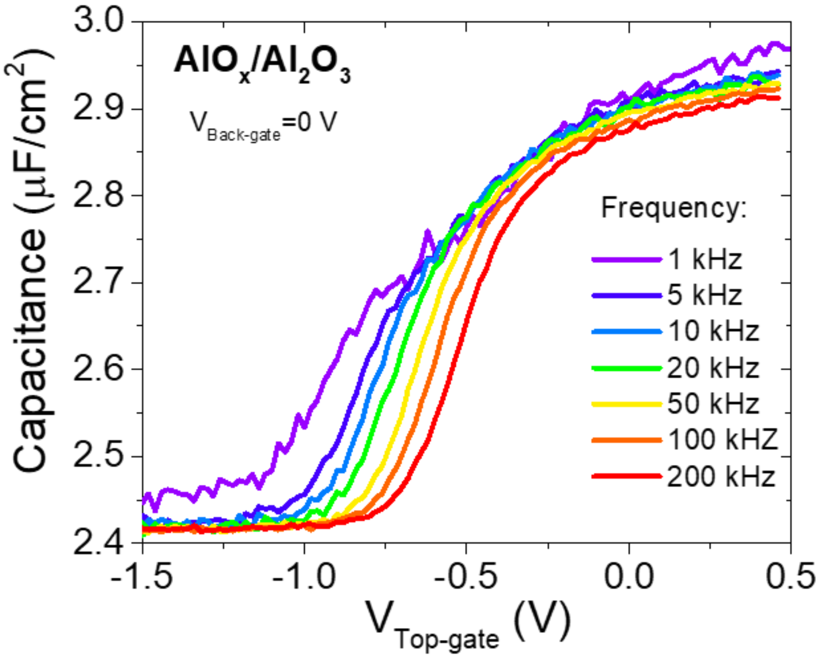

Figure 16 : C-V plots for pristine MoS_2 FET with AlO_x/Al_2O_3 gate dielectric.

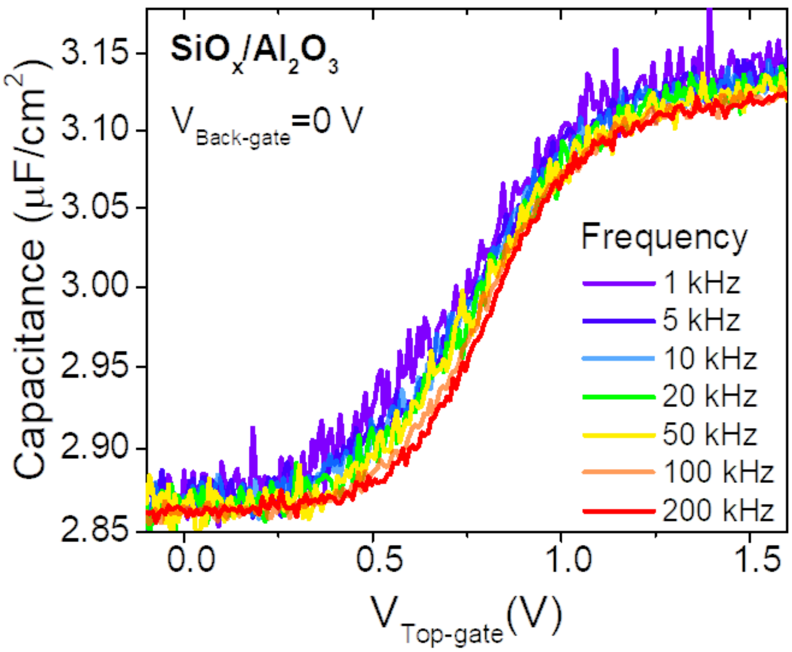

Figure 17 : C-V plots for pristine MoS_2 FET with SiO_x/Al_2O_3 gate dielectric.

As observed from the plots the dispersion in the depletion region is a clear signature of the interface trap response to the applied gate bias. The high capacitance in the accumulation region is attributed to the parasitic capacitances because of the un-gated region adjacent to source and drain. The Al_2O_3 device with AlO_x seeding layer show more dispersion in comparison with other two devices indicating that AlO_x seeding layer has more traps.

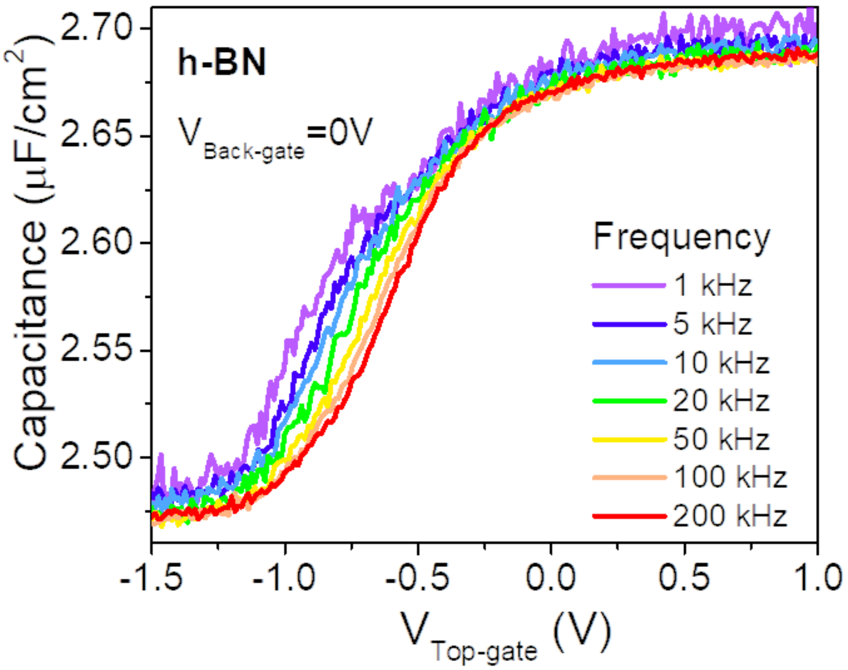

Figure 18 : Pristine C-V plots for h-BN dielectric device.

The conductance-voltage (G-V) characteristics are shown in the Figures 19, 20 and 21 for AlO_x/Al_2O_3, SiO_x/Al_2O_3 and h-BN gated devices respectively. The conductance variation as a function of frequency is observed. Distinct increase in the peak is observed with the increase in frequency. Also, the device with AlO_x seeding layer shows the maximum conductance of 53 nS at 200 kHz when compared to SiO_x and h-BN device at the same frequency.

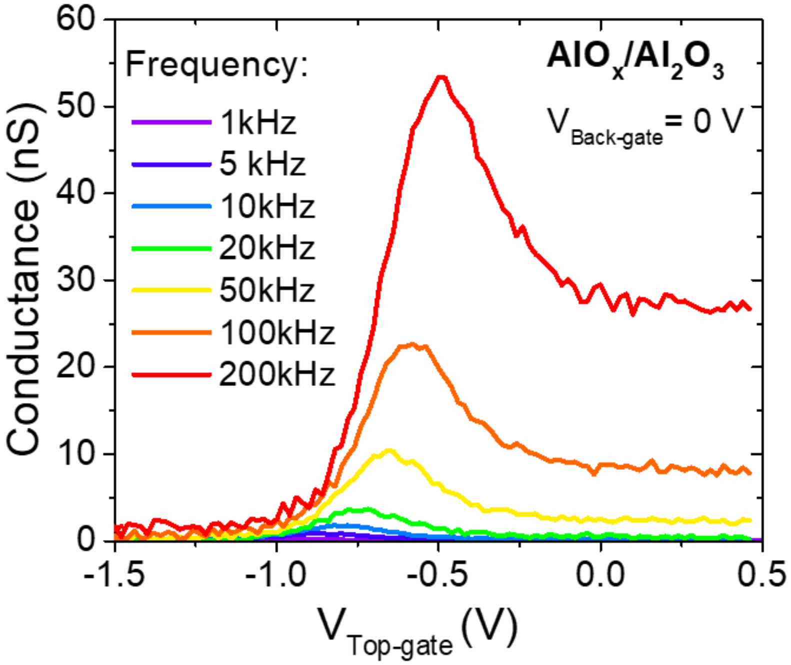

Figure 19 : G-V characteristics for pristine MoS_2 FET with AlO_x/Al_2O_3 gate dielectric.

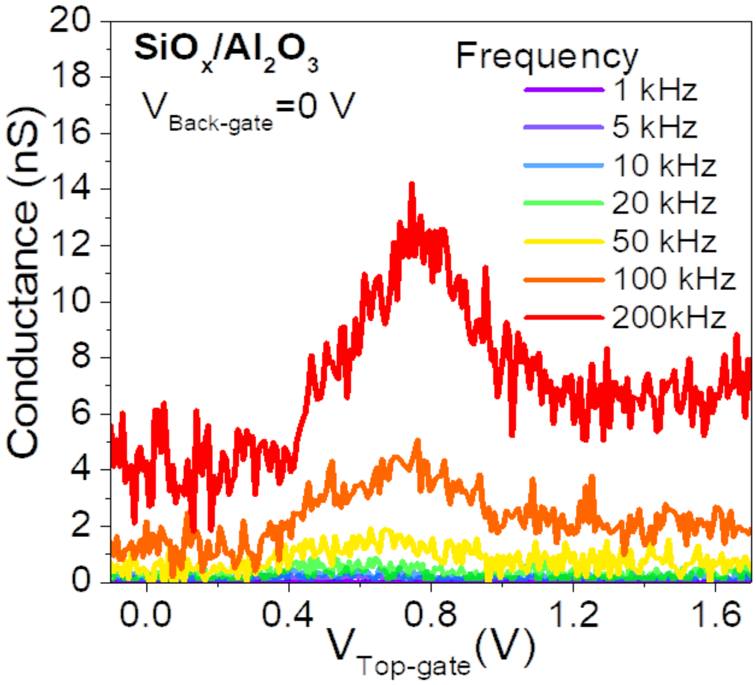

Figure 20 : G-V characteristics for pristine MoS_2 FET with SiO_x/Al_2O_3 gate dielectric.

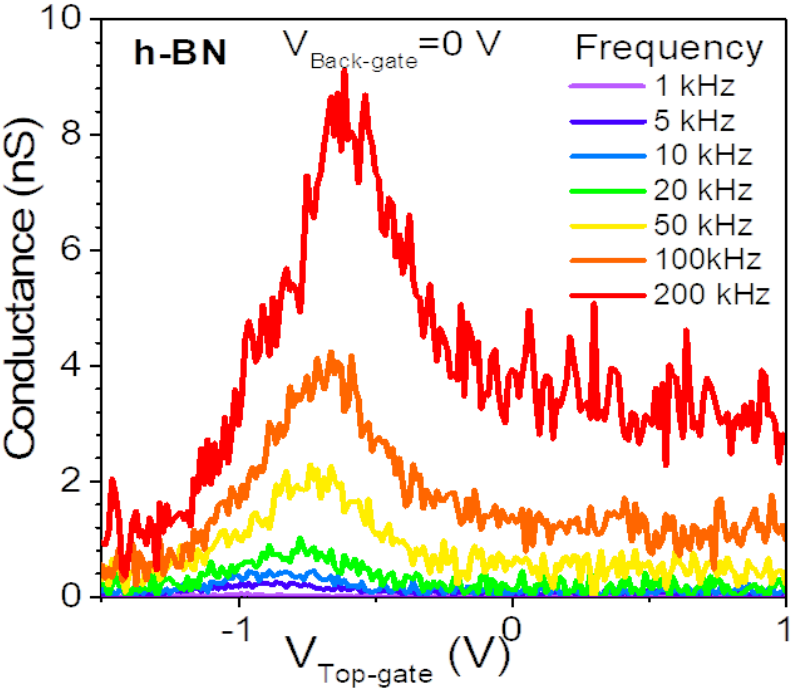

Figure 21 : G-V characteristics for pristine MoS_2 FET with h-BN gate dielectric.

After the C-V measurements, the capacitance and conductance are measured at a constant voltage bias as a function of frequency. Now the conductance technique is implemented to extract the D_{it}.

4.1.3 D_{it} extraction for pristine devices using the conductance technique

The conductance method was implemented at room temperature in air. The corrected capacitance C_c and conductance G_c need to be extracted first since the device possesses series resistances from the ungated regions and from the contacts. The series resistance is obtained by biasing the device in accumulation, and then the following expression is applied:

$$R_S = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \tag{4.1}$$

G_{ma} and C_{ma} are the measured conductance and capacitance, respectively, in the accumulation region, $\omega = 2\pi \times$ frequency. Followed by this, the series resistance factor denoted by a is calculated as $a = G_m - (G_m^2 + \omega^2 C_m^2)R_S$, where G_m and C_m are the measured conductance and capacitance, respectively. G_c and C_c can be then calculated as:

$$G_C = \frac{(G_m^2+\omega^2 C_m^2)a}{a^2+\omega^2 C_m^2} \tag{4.2}$$

$$C_C = \frac{(G_m^2+\omega^2 C_m^2)C_m}{a^2+\omega^2 C_m^2} \tag{4.3}$$

Now G_p/ω can be calculated as follows:

$$\frac{G_p}{\omega} = \frac{\omega G_C C_G^2}{G_C^2+\omega^2(C_G-C_C)^2} \tag{4.4}$$

Here, G_p is the equivalent parallel capacitance, C_G is the gate capacitance, which not only involves the gate dielectric capacitance, but also the quantum capacitance of MoS_2. We take C_G as the capacitance in the accumulation region of the C-V curves.

Finally, D_{it} is calculated as: $D_{it} = \frac{2.5}{q}\frac{G_p}{\omega}$ at the maximum.

Figures 22, 23 and 24 shows the G/ω–f curves for gate voltages varied from depletion to accumulation in pristine MoS_2 FETs with AlO_x/Al_2O_3, SiO_x/Al_2O_3 gate dielectric and h-BN gate dielectric respectively. As observed from the plots, G/ω peak positions are voltage dependent, which clearly indicates that the Fermi level is unpinned. This confirms that the conductance method can be used to determine the interface trap density.[27] In certain cases of III-V/hi-κ interfaces, the Fermi level is pinned and the conductance peak does not change with the gate voltage applied, causing the conductance method to be inapplicable there.[27] At flat band condition, the Fermi level is close to the conduction band edge. Any voltage applied below the flat band condition directly translates to how much the Fermi level moves into the bandgap. From Figures 22 and 23 it can be inferred that for Al_2O_3 gate dielectric, the peak is observed to shift towards right as the Fermi level moves further into the band gap while the h-BN dielectric device in Figure 24 exhibits the left shift in the maximum peak.

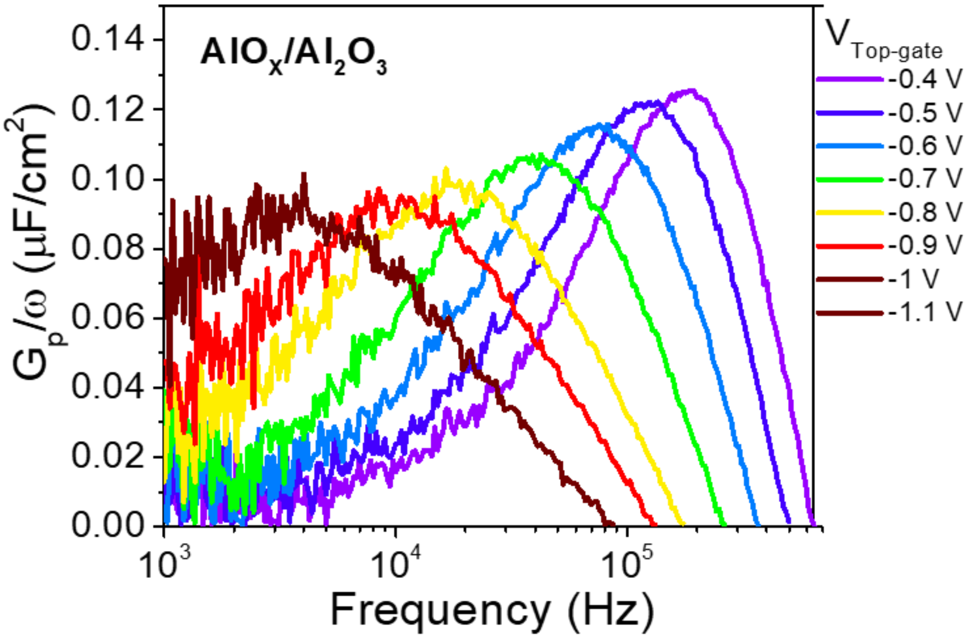

Figure 22 : *G/ω–f* curves for gate voltages varied from depletion to accumulation for pristine MoS_2 FET with AlO_x seeding layer.

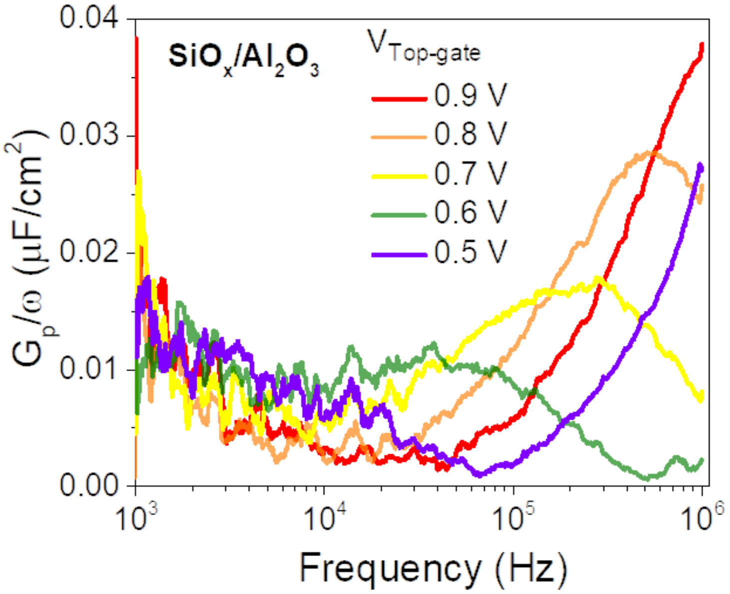

Figure 23 : *G/ω–f* curves for gate voltages varied from depletion to accumulation for pristine device with SiO_x seeding layer.

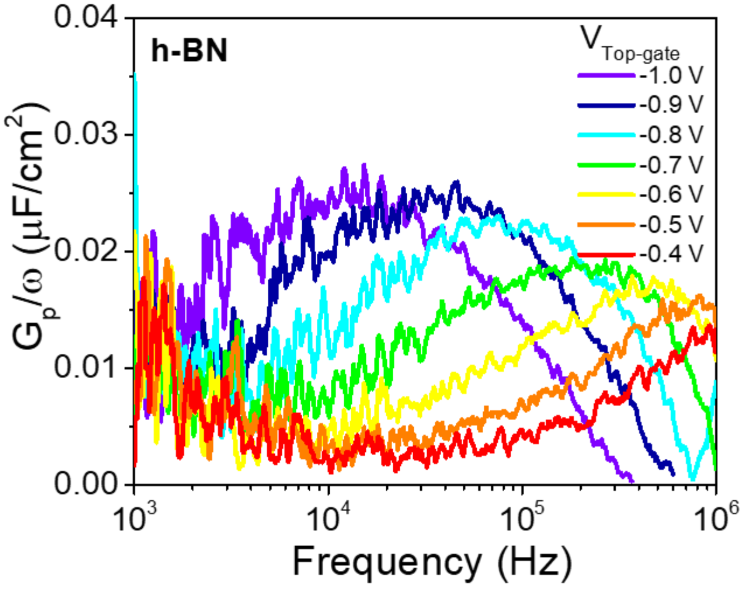

Figure 24 : *G/ω–f* curves for gate voltages varied from depletion to accumulation for pristine h-BN device.

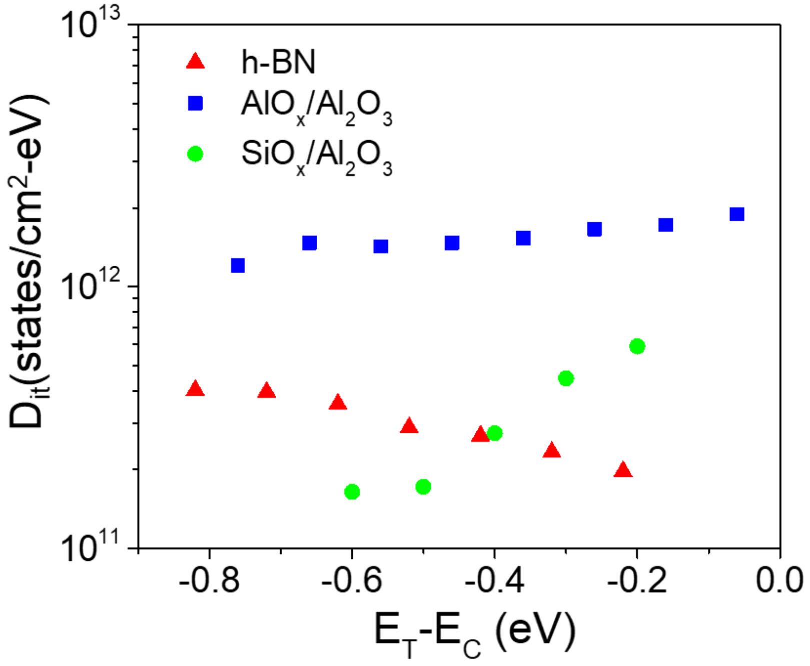

Figure 25 : D_{it} v/s trap position for the pristine Al_2O_3 and h-BN devices.

The extracted D_{it} values as a function of the trap position (E_T–E_c) for the Al_2O_3 and h-BN gated devices as shown in the Figure 25. At midgap, the D_{it} extracted for pristine AlO_x/Al_2O_3 device is ~ 1.1×10^{12} states/cm^2-eV and is nearly constant through the band-gap. Whereas, the pristine SiO_x/Al_2O_3 gate dielectric exhibited the D_{it} of 5.9×10^{11} states/cm^2-eV near the conduction band edge and 1.6×10^{11} states/cm^2-eV near the valence band edge. From this it can be inferred that the device with SiO_x seeding layer exhibits lower D_{it} when compared with the AlO_x seeding layer device. For a 2D h-BN dielectric device, it is seen that the D_{it} is 4×10^{11} states/cm^2-eV near the valence band edge which is relatively higher than the D_{it} near conduction band edge which is 2×10^{11} states/cm^2-eV. While the D_{it} profile looks slightly different for the device with h-BN dielectric, the D_{it} values are similar to the case with SiO_x/Al_2O_3, the midgap D_{it} is lower 10^{11} states/cm^2-eV. The AlO_x/Al_2O_3 devices exhibit the mid-gap D_{it} of 1.5×10^{12} states/cm^2-eV.

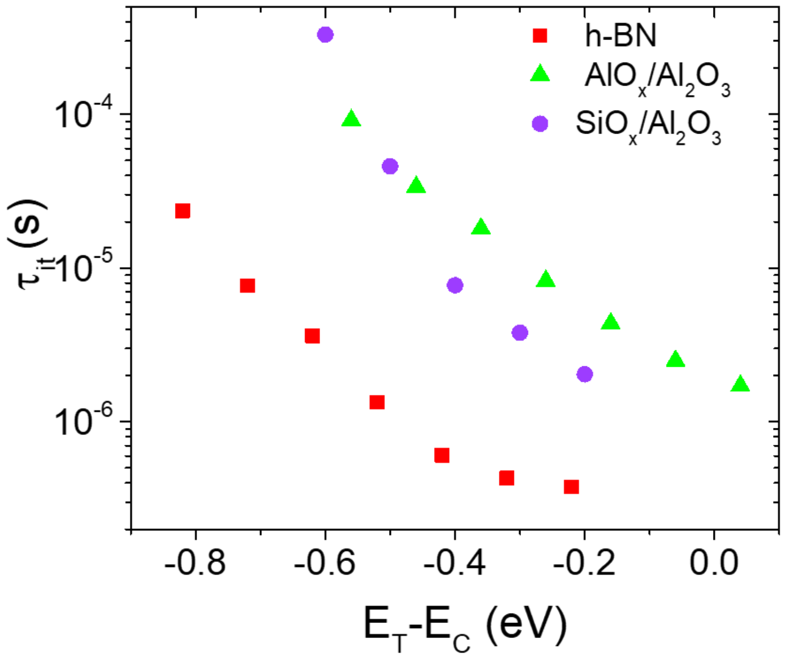

Figure 26 : Trap time constants v/s trap position for the pristine Al_2O_3 and h-BN devices.

The trap time constants are also plotted in Figure 26 and the interface trap time constants can be obtained from the relation: $\tau_{it} = 2/\omega$, where ω is the radial frequency corresponding to the peak of the G/ω *vs.* f curve.[11] The interface trap time constants for the $MoS_2/SiO_x/Al_2O_3$ and MoS_2/h-BN interfaces are similar, signifying that similar defects contribute to the interface traps in these devices. The identity of defects in MoS_2 causing interface trap formation is debatable. Several reports indicate that the interface traps in MoS_2 based FETs originate from the sulfur vacancies in MoS_2.[28, 29]

4.2 Effect of forming gas annealing

Since the AlO_x/Al_2O_3 device exhibited relatively higher midgap D_{it} of 1.5×10^{12} states/cm^2-eV compared to SiO_x and h-BN devices, further studies were conducted on the latter types with low D_{it} values. Forming gas annealing is known to reduce D_{it} in silicon-based devices. This is why we subjected the SiO_x/Al_2O_3 and h-BN gated devices to forming gas annealing (FGA) to study its effect on D_{it}. The devices were annealed in forming gas composed of 10% H_2, 90% N_2. The MoS_2/ h-BN devices were annealed at 250 ºC for 2 h with the ramp time of 30 mins. The MoS_2/Al_2O_3 devices were annealed for 30 mins at 120 ºC. A lower annealing temperature and duration was chosen for the Al_2O_3-gated devices since they showed increased gate leakage for higher annealing temperatures and durations.

4.2.1 I-V Characteristics post FGA

After annealing, the devices were tested for transfer characteristics shown in the Figure 27 and we saw the substantial decrease in the SS indicating that the defects are passivated by forming gas. The SS of the h-BN device decreased from 140 mV/decade to 100 mV/decade. The SS of SiO_x/Al_2O_3 decreased from 160 mV/decade to 95 mV/decade.

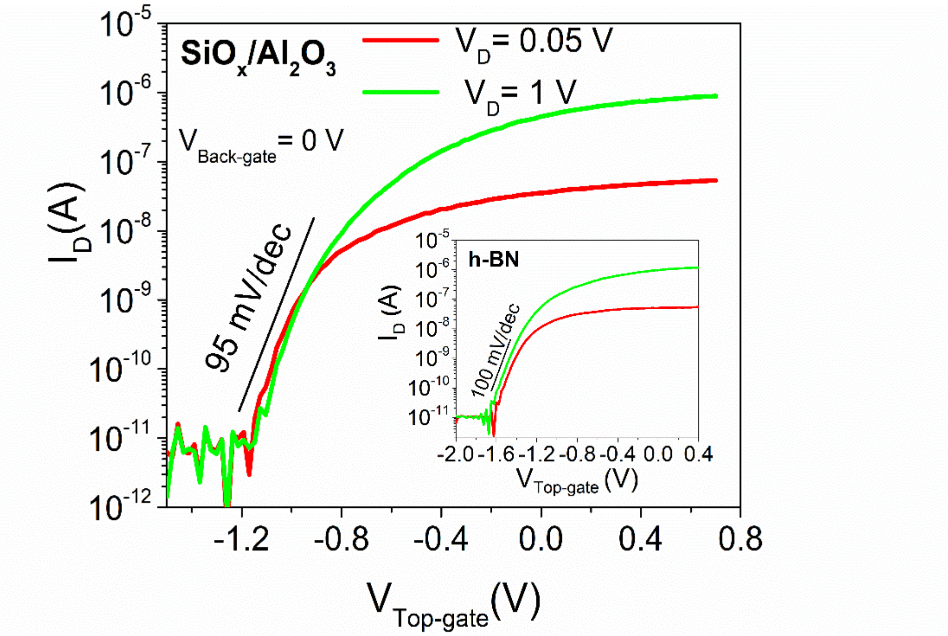

Figure 27 : Post FGA transfer characteristics for MoS_2 FET with Al_2O_3 gate dielectric with SiO_x seeding layer. Inset: Transfer characteristics for MoS_2/h-BN device.

D_{it} is extracted analytically from the SS, using circuit models. The following analytical expression is used to extract D_{it},[30, 31]

$$SS = \frac{2.3kT}{q}\left(1 + \frac{C_{it}}{C_{tg}} + \frac{C_{body}}{C_{tg}} - \frac{\frac{C_{body}^2}{C_{tg}C_{SiO_2}}}{1+\frac{C_{it}}{C_{SiO_2}}+\frac{C_{body}}{C_{SiO_2}}}\right) \tag{4.5}$$

Here, C_{it} is the interface trap capacitance. C_{tg} is the capacitance of the top gate dielectric, given by $C_{tg} = \epsilon_{tg}/t_{tg}$, where ϵ_{tg} is the dielectric constant and t_{tg} is the thickness of the top gate dielectric. For h-BN, C_{tg} = 0.204 μF/cm^2, assuming ϵ_{h-BN} = 3,[32] and the thickness of the h-BN flake, $t_{h\text{-}BN}$ is measured by atomic force microscopy to be 13 nm. For Al_2O_3, C_{tg} = 0.387 μF/cm^2, considering the gate dielectric stack thickness $t_{Al_2O_3}$ = 9.5 nm and a nucleation layer t_{SiO_x} = 1.5 nm, with $\epsilon_{Al_2O_3}$ = 5 (experimental) and assuming ϵ_{SiO_x} =3.9. $C_{SiO_2} = \epsilon_{SiO_2}/t_{SiO_2}$=0.013 μF/cm^2, given ϵ_{SiO_2}= 3.9, and the thickness of SiO_2 is 260 nm. $C_{body} = C_{MoS_2} = \epsilon_{MoS_2}/t_{MoS_2}$= 1.26 μF/cm^2, using ϵ_{MoS_2} = 4,[33] and thickness of 4-layer MoS_2 flake is 2.8 nm. For the h-BN device with SS = 100 mV/dec, a D_{it} of 4×10^{11} states/cm^2-eV is extracted using equation (4.5). Similarly, for Al_2O_3 device with SS = 95 mV/dec, a D_{it} of 6×10^{11} states/cm^2-eV is extracted. The interface trap densities thus obtained are impressive and are comparable with the highest quality of Si/high-κ dielectric interfaces.[34-36] Thus, our MoS_2/h-BN and $MoS_2/SiO_x/Al_2O_3$ interfaces can yield high quality, low-D_{it} interfaces after only a mild forming gas annealing.

4.2.2 Post FGA C-V and G-V characteristics

The capacitance and conductance of the top-gated MoS_2 FETs were examined next. Figures 28 and 29 show the capacitance-voltage and conductance-voltage characteristics as a function of frequency for SiO_x/Al_2O_3 and h-BN top-gated device, respectively. Both the C-V curves do not show any significant frequency dependence in the depletion region from 1 kHz to

500 kHz, indicating the presence of few interface traps. The absence of sharp peaks in the parallel conductance *vs*. top gate voltage curves are also indicative of low D_{it}.[37, 38] The high capacitance in the accumulation region is attributed to parasitic capacitances due to the ungated regions adjacent to the source and drain. The frequency dispersion in the accumulation region for the SiO_x/Al_2O_3 gated device is attributed to border traps.[10, 39] It is worth noting that the h-BN-gated device does not show frequency dispersion in the accumulation region, indicating a lower density of border traps in h-BN compared to SiO_x/Al_2O_3. The dispersion in the depletion and deep depletion regions are due to the interface traps.

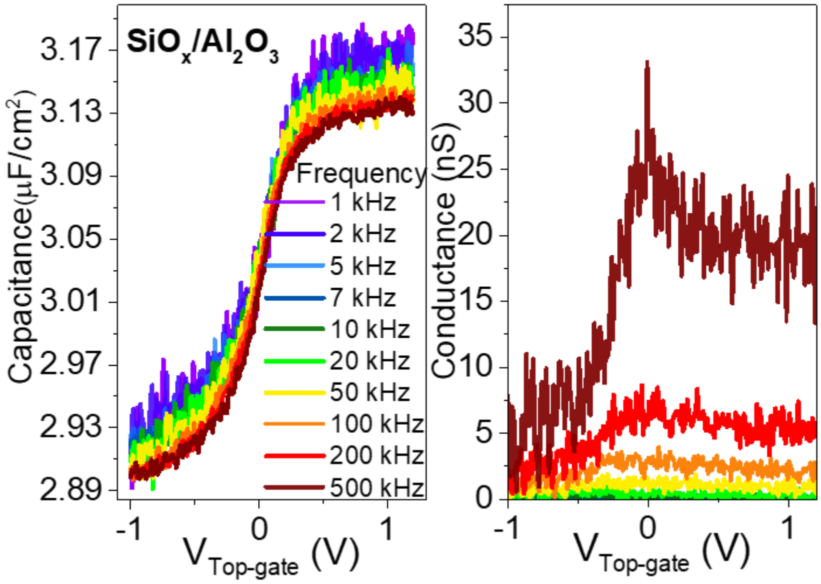

Figure 28 : Post FGA C-V and G-V characteristics of SiO_x/Al_2O_3 device showing relatively reduced frequency dispersion in the depletion region

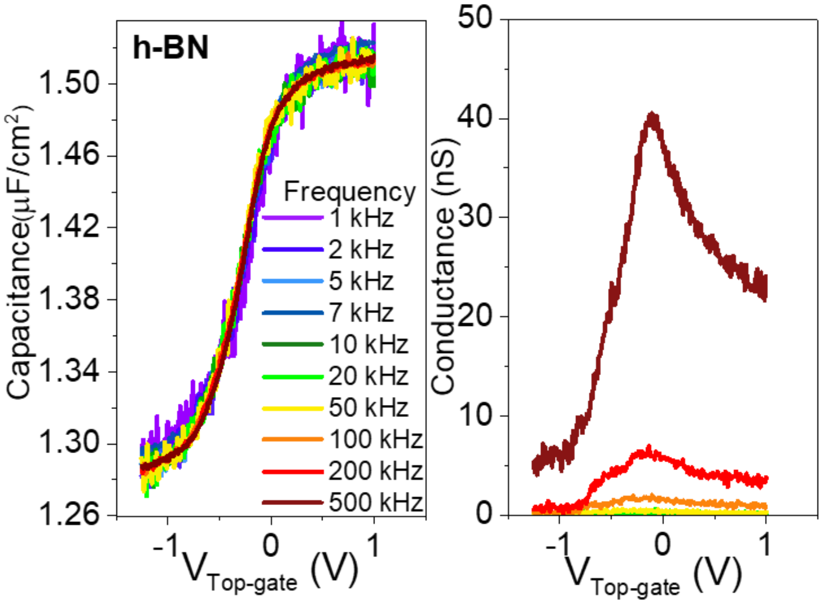

Figure 29 : Post FGA C-V and G-V characteristics of h-BN device showing relatively reduced frequency dispersion in the depletion region

4.2.3 Post FGA D_{it} extraction by conductance method

Figure 30 shows the G/ω–f curves for gate voltages varied from depletion to accumulation in an MoS_2 FET with SiO_x/Al_2O_3 gate dielectric and h-BN gate dielectric. Figure 30 shows the extracted D_{it} values and interface trap time constants as a function of the trap position (E_T–E_c) for the SiO_x/Al_2O_3 and h-BN gated devices.

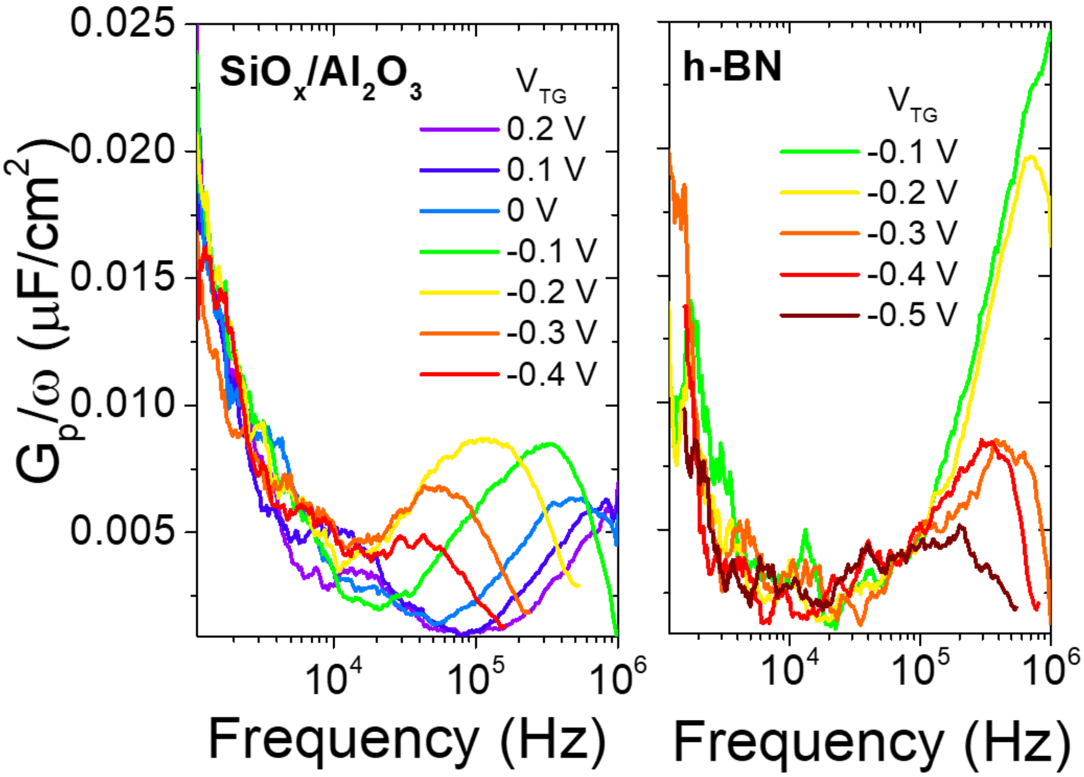

Figure 30 : Post FGA *G/ω–f* curves for gate voltages varied from depletion to accumulation in an MoS_2 FET with SiO_x/Al_2O_3 gate dielectric and h-BN gate dielectric.

For the device with SiO_x/Al_2O_3 gate dielectric, the *G/ω* peak increases as the gate voltage is swept from flat band to depletion, indicating the increase in D_{it} as the Fermi level shifts further into the band gap from the conduction band edge. An opposite trend is observed below the midgap. In case of the device with h-BN gate dielectric, the *G/ω* peak gets reduced from flat band to depletion.

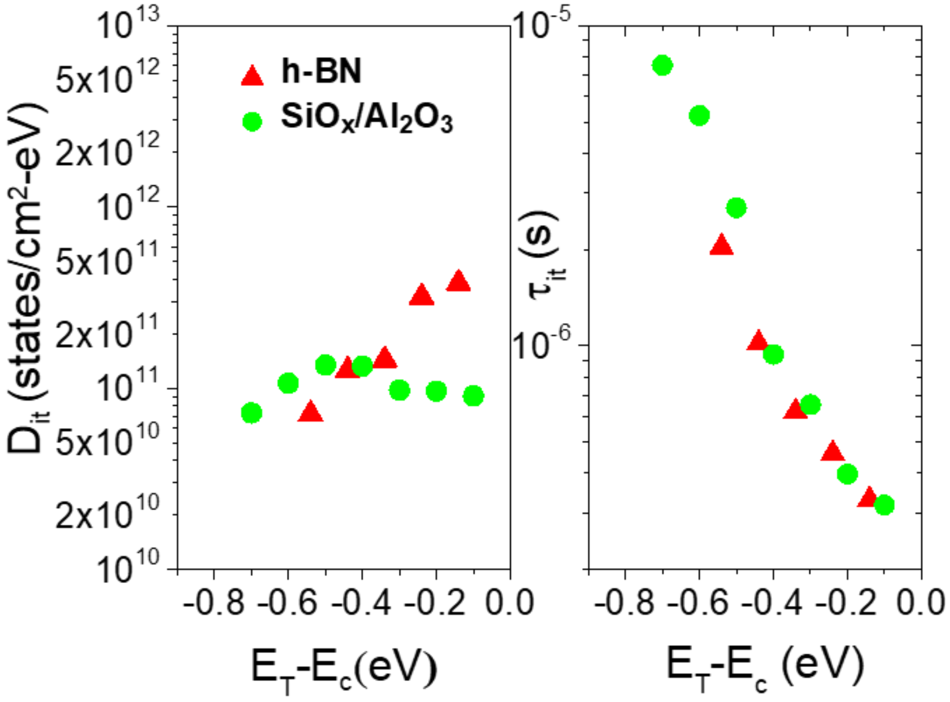

Figure 31 : Post FGA D_{it} v/s trap position exhibiting the decrease in the D_{it} for the SiO_x/Al_2O_3 and h-BN devices.

The post FGA D_{it} and τ_{it} profiles of SiO_x/Al_2O_3 and h-BN devices are shown in the Figure 31. At midgap, the D_{it} extracted for SiO_x/Al_2O_3 gate dielectric is ~1.3×10^{11} states/cm^2-eV, while the D_{it} is 9×10^{10} states/cm^2-eV near the conduction band edge, and the D_{it} is 7×10^{10} states/cm^2-eV near the valence band edge. While the D_{it} profile looks slightly different for the device with h-BN dielectric, the D_{it} values are similiar to the case with SiO_x/Al_2O_3, with a midgap D_{it} for this 2D/2D interface being ~7×10^{10} states/cm^2-eV. At least two devices of each type showed similar characteristics. The low value of D_{it} obtained for MoS_2/h-BN interface is due to the absence of dangling bonds at 2D/2D interface. In our device structure, the MoS_2 layers are encapsulated by the h-BN top gate, leaving no free surfaces for increased trap states. D_{it} for monolayer and tri-layer MoS_2 with h-BN underneath MoS_2 was extracted by Chen et al., to be in the range of 10 states/cm^2-eV, despite the capacitance-voltage characteristics showing no frequency dispersion. We believe that the implementation of the conductance method helps us in extracting the low D_{it} values from these MoS_2/h-BN systems accurately. It is well-known that the inclusion of a nucleation layer increases the interface traps. However, our experiments show that the interface quality of a 2D/high-κ system where SiO_x is used as the nucleation layer for ALD of Al_2O_3 exhibits D_{it} values close to the 2D/2D dangling-bond-free interface enabled by h-BN on MoS_2. The observation of low D_{it} values using SiO_x nucleation layer could be due to its ability to facilitate faster reactions between surface hydroxyl groups and ALD precursors.[40] The D_{it} values we obtained from the SS analysis are in the ballpark of the D_{it} values extracted using the conductance method. The low D_{it} clearly establishes the superior quality of 2D/2D van der Waals interface and 2D/high-κ interfaces for realizing high performance and reliable (opto)electronic devices. The interface trap time constants can be obtained from the relation: $\tau_{it} = 2/\omega$, where ω is the radial frequency corresponding to the peak of the G/ω *vs.* f curve. The interface trap time constants for the $MoS_2/SiO_x/Al_2O_3$ and MoS_2/h-BN interfaces are similar, signifying that similar defects contribute to the interface traps in these devices. The identity of defects in MoS_2 causing interface trap formation is debatable.[41] Several reports indicate that the interface traps in MoS_2 based FETs originate from the sulfur vacancies in MoS_2.[10]

4.3 Chapter Summary

In summary, we report high-quality interfaces in a semiconductor system, enabled by 2D/2D and 2D/high-κ-dielectric systems. Using the conductance method, a midgap interface trap density as low as 7×10^{10} states/cm^2-eV can be obtained by MoS_2/h-BN device. The D_{it} varies from 7×10^{10} to 10^{11} states/cm^2-eV at an MoS_2/Al_2O_3 interface if SiO_x is used as the nucleation layer.

CHAPTER 5: CONCLUSION

This thesis investigates the interfaces properties of MoS_2 with top gate dielectrics, such as 2D h-BN and Al_2O_3 high-κ dielectric. The ALD of Al_2O_3 was enabled by the deposition of AlO_x and SiO_x as the nucleation layers. The D_{it} is probed and quantified using one of the most reliable methods – the conductance technique. From this study, we observe that 2D MoS_2 with 2D dielectric h-BN and hi-k dielectric Al_2O_3 enables a high quality semiconductor system. We also report the effect of seeding layer on the D_{it}. From the extracted D_{it}, it is observed that using AlO_x seeding layer introduces a D_{it} of 1×10^{12} states/cm^2-eV, whereas the D_{it} of the interface with SiO_x seeding layer 7×10^{10} to 10^{11} states/cm^2-eV comparable with the midgap D_{it} of 7×10^{10} states/cm^2-eV extracted from MoS_2/h-BN after mild forming gas annealing. This clearly indicates that the layered materials result in high-quality interfaces with both 2D dielectric and hi-k dielectric, reinforcing their potential as channel material for various high performance and reliable electronics and optoelectronics.

5.1 Future Scope

This thesis emphasizes on quantifying the density of interface traps using the conductance technique. However, the origin of interface states is believed to be the inherent defects present in the material. Therefore, a more comprehensive study is required to shed the light on the genesis of the traps at 2D/2D interface. Also, a detailed study is required for regarding the decrease in the interface traps with SiO_x seeding layer. The locations of the interface traps extracted by the conductance technique needs to be accurately determined using modeling of the MoS_2 bandgap. The effect of border traps needs to be quantified and compared with the effect of interface traps. The D_{it} needs to be extracted using other techniques mentioned in Chapter 2, and a comparison needs to be made of the efficiency of these techniques.

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