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Investigation of different dielectric materials as gate insulator for MOSFETs

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INVESTIGATION OF DIFFERENT DIELECTRIC MATERIALS AS GATE INSULATOR FOR MOSFET

by

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ABSTRACT

The scaling of semiconductor transistors has led to a decrease in thickness of the silicon dioxide layer used as gate dielectric. The thickness of the silicon dioxide layer is reduced to increase the gate capacitance, thus increasing the drain current. If the thickness of the gate dielectric decreases below 2nm, the leakage current due to the tunneling increases drastically. Hence it is necessary to replace the gate dielectric, silicon dioxide, with a physically thicker oxide layer of high-k materials like Hafnium oxide and Titanium oxide. High-k dielectric materials allow the capacitance to increase without a huge leakage current.

Hafnium oxide and Titanium oxide films are deposited by reactive magnetron sputtering from Hafnium and Titanium targets respectively. These oxide layers are used to create metal-insulator-metal (MIM) structures using aluminum as the top and bottom electrodes. The films are deposited at various O_2/Ar gas flow ratios, substrate temperatures, and process pressures. After attaining an exact recipe for these oxide layers that exhibit the desired parameters, MOS capacitors are fabricated with n-Si and p-Si substrates having aluminum electrodes at the top and bottom of each. Comparing the parameters of Hafnium oxide- and Titanium oxide- based MOS capacitors, MOSFET devices are designed with Hafnium oxide as gate dielectric.

To my grandparents, my parents and my uncle

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LIST OF ACRONYMS/ABBREVIATIONS

Å	Angstrom
Al	Aluminum
Ar	Argon
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductor
C_{ox}	Oxide Capacitance
DC	Direct Current
E_g	Band gap
ε_o	Relative Permittivity of free space, 8.85
g_m	Transconductance
HfO_2	Hafnium dioxide
I_D	Drain Current
JFET	Junction Field–Effect Transistor
k	Dielectric Constant
L	Channel Length
LCR	Inductance, capacitance and resistance
MIM	Metal-Insulator- Metal
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
N_A	Acceptor doping concentration, atoms/cm^3
N_D	Donor doping concentration, atoms/cm^3
PACVD	Plasma Assisted Chemical Vapor Deposition

PECVD	Plasma Enhanced Chemical Vapor Deposition
PR	Photoresist
PVD	Physical Vapor Deposition
Q_f	Fixed oxide charges
Q_i	Interface trapped charges
Q_m	Mobile oxide charges
Q_t	Oxide trapped charges
RF	Radio Frequency
rpm	Rotations per minute
RTA	Rapid Thermal Annealing
SiO_2	Silicon dioxide
TiO_2	Titanium dioxide
T_{ox}	Oxide Thickness
V_{DS}	Drain to Source Voltage
V_G	Gate Voltage
VLSI	Very Large Scale integration
V_T	Threshold Voltage
W	Channel Width
X_j	Junction Depth

CHAPTER 1: INTRODUCTION

1.1: Background

The exponential increase of number of transistors on an integrated circuit over time was first predicted by Moore's Law (as shown in Figure 1.1). Since the early 1970s, the metal-oxide-semiconductor-field-effect-transistor (MOSFET) has been recognized as the most promising device in VLSI circuits, because of its simpler structure, lower cost to fabricate and lower power consumption compared to bipolar and junction field–effect transistor (BJTs and JFETs). The demand for integrated circuits in the industry with greater functionality and lower cost performance requires an increase in chip density which demands scaling of the device. Scaling of silicon dioxide dielectric was once been viewed as an effective approach to enhance transistor performance in complementary-metal-oxide-semiconductor (CMOS). In past few decades, reduction of the thickness of gate dielectric below 2 nm, which is close to the physical limit, has led to huge increase in gate leakage current due to obvious tunneling effect. On further scaling of the device, the leakage currents through Silicon dioxide (SiO_2), currently used dielectric, are intolerable due to high power consumption and low breakdown voltage.

To continue the downward scaling, high-k dielectric materials are currently in consideration for gate dielectric in MOSFET devices which play a major role in affecting threshold voltage (V_T). As the name suggest, these material have high dielectric constant (high-k) which improves the oxide capacitance, has low gate leakage current thus providing better stability to the device, lower power dissipation and higher breakdown voltage.

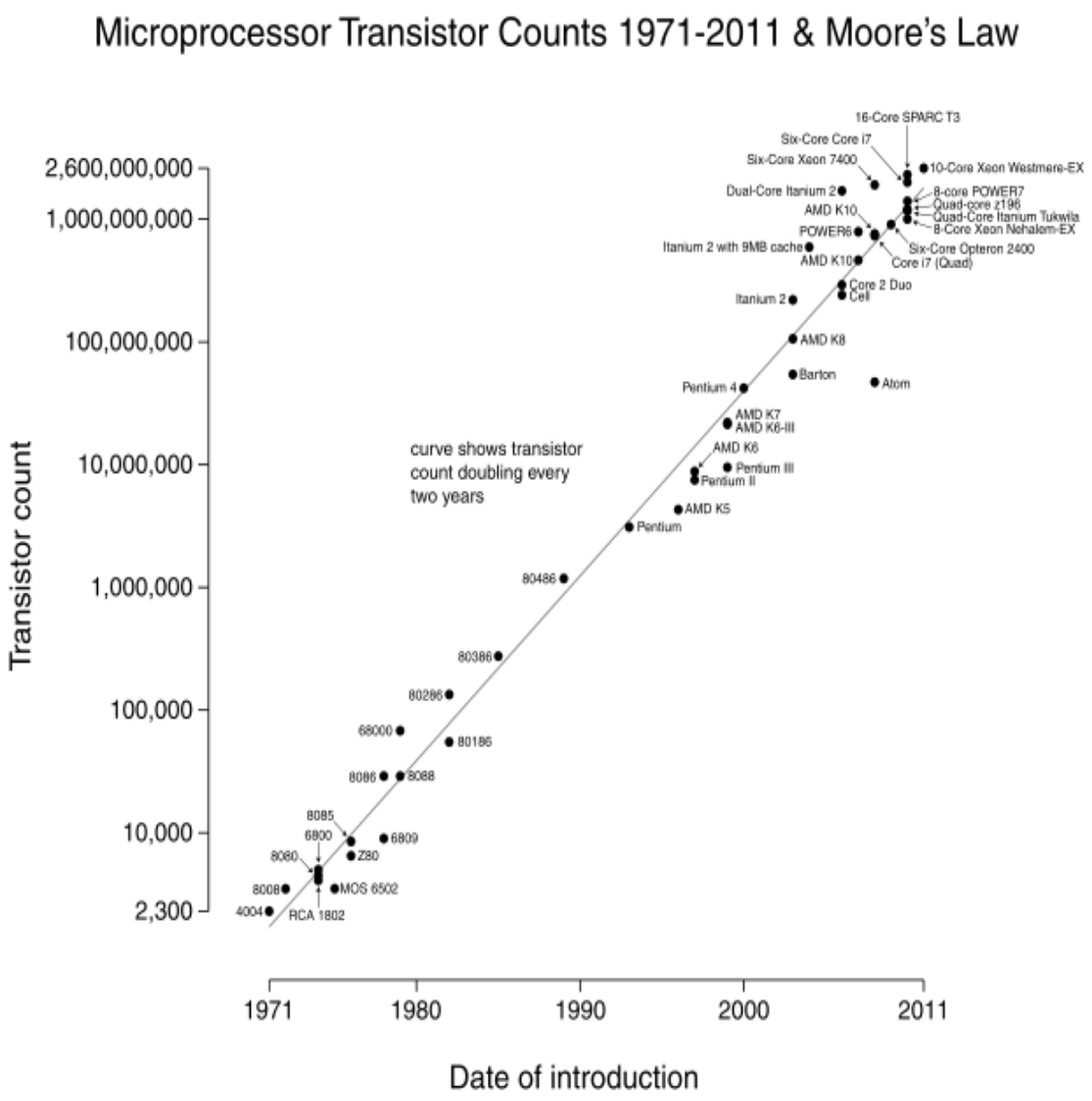


Figure 1.1 Enhanced performance Trend as predicted by Moore's Law [1].

1.1.1: Limitation of SiO_2

Advances in scaling and technology have led to reduction in the size of the transistors. Reduction in size of transistor leads to change in field, to maintain field the capacitance of the gate has to be increased. This can be done by reducing the thickness of the gate oxide. As the thickness goes below 20Å, tunneling effect through potential barrier can lead to high leakage current, thus leading to circuit instability and high power dissipation. There is a good chance of dielectric breakdown, which may lead to defects; non-uniformity in the film thickness, dopant penetration into the substrate, increase in interface trap charges (Q_i) and oxide trapped charges (Q_t). Silicon dioxide has been extensively used as gate dielectric for many years [2]. Because of all the above reasons, there is need to find alternative high-k dielectric materials which can solve the problem listed in this section.

1.2: What are dielectric materials?

Dielectric materials are substances which are poor conductors of electricity. They are also called as insulators with an effective support of electrostatic fields. The flow of current is kept to a minimum between opposite charged poles without interrupting the electrostatic lines of flux; electrostatic field can also store energy. Important properties of a dielectric are its ability to support an electrostatic field while dissipating minimal energy in the form of heat, the extent to which a substance concentrates the electrostatic lines of flux. Substances with a low dielectric constant include a perfect vacuum, dry air, and most pure, dry gases such as helium and nitrogen. Materials with moderate dielectric constants include ceramics, distilled water, paper, mica, polyethylene, and glass. Metal oxides, in general, have high dielectric constants [3].

1.3: High-k dielectric materials

Dielectric materials with high dielectric constants are used as gate dielectric in MOSFETs. The dielectric materials examined in this study in detail are hafnium oxide and titanium oxide. High-k dielectric material gives high value of oxide capacitance (C_{ox}) which may influence the threshold voltage (V_T) and working of the device. The dielectric constants of these materials totally depend upon the way they are deposited over the silicon substrate. The dielectric layers with higher electrical permittivity are used for thicker films to reduce the leakage current and improve upon the reliability of the gate dielectric layer with electrical thickness equal to ultra-thin SiO_2 layer [4].

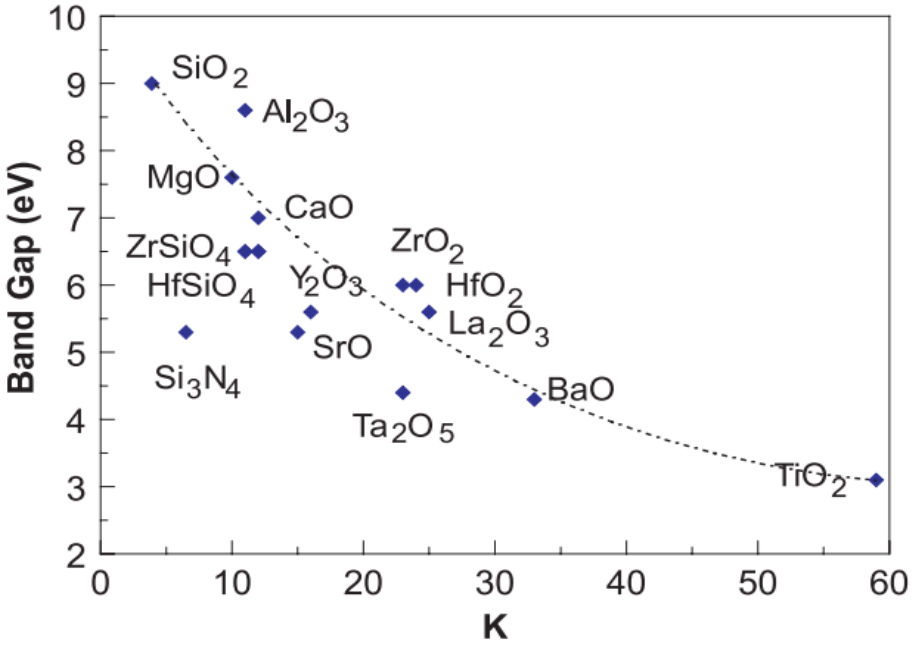


Figure 1.2 Plot of dielectric constants of various oxides vs. band gap (Eg) [5].

There are many dielectric materials whose dielectric constant is more than 3.9 (SiO_2 dielectric constant) as shown in the Figure 1.2.

1.3.1: High-k dielectric materials: Properties and Challenges

High-k dielectric materials are chosen with following properties,

- High Permittivity
- High Barrier height
- Reduce the leakage current
- Lower the power consumption
- Lower direct tunneling effect
- Stable over silicon substrates
- Compatible with the gate metal
- Compatibility with process.

For limiting the leakage current, barrier height should also be taken into consideration. Figure 1.3 shows the energy band diagram for ideal MOS before and after contact.

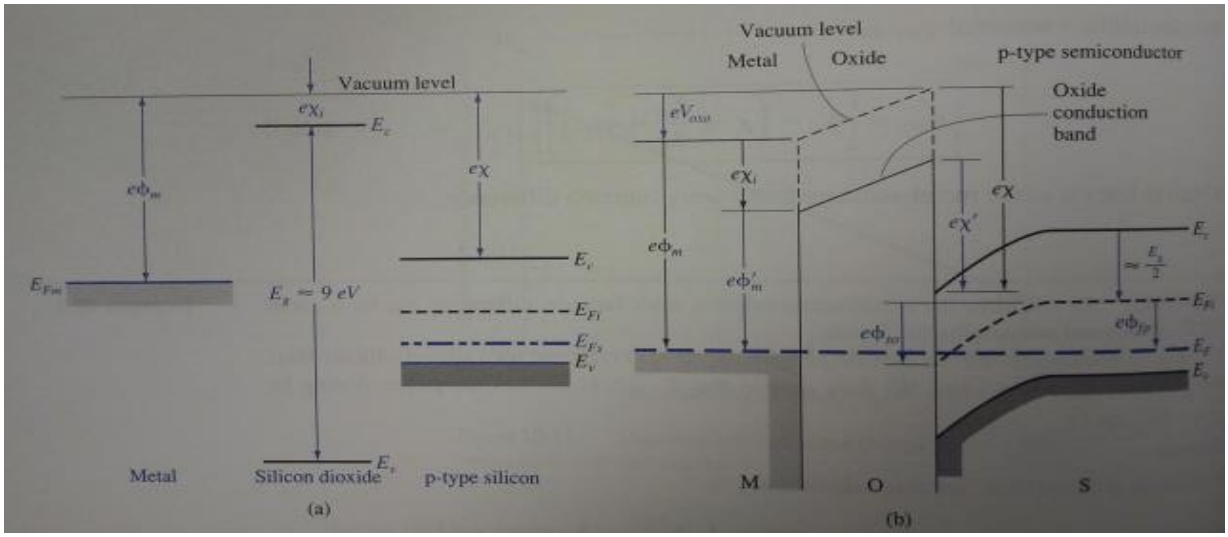


Figure 1.3 (a) Energy levels in a MOS system prior to contact and (b) energy- band diagram through the MOS structure in thermal equilibrium after contact [6].

The challenges of high-k dielectric material are

- Mobility degradation
- Fixed charges.
- Hot carrier effects due to reduced energy barrier for electrons and holes.
- Diffusion of oxygen and dopant on to the silicon substrate
- Charge trapping and threshold voltage (V_T) shifts

CHAPTER 2: OPERATION OF MOSFET

2.1: Introduction of MOSFETs

MOSFETs are metal-oxide-semiconductor field effect transistors. It is a voltage controlled device as compared to BJT which is a current controlled device. It is also called unipolar device as the current in MOSFET is account of transported of only one carrier i.e. major-carriers (holes in p-channel MOS and electrons in n-channel MOS). MOSFET consists of four terminal gate, source, drain and substrate terminals. The substrate terminal is often connected to the source terminal. The source and drain are heavily doped regions to reduce their resistance and are back to back p-n junctions in which depletion region is entirely into the substrate. They are important devices for microprocessors, VLSI circuits and DRAM cells. They are also used in power applications, communications and in the computer industry.

There are three main metal contacts – source, drain and gate. Source and drain metal contacts are connected to diffused regions of the device whereas gate metal contact is connected over the insulated region. The gate electrode material is critical as it helps in deciding the threshold voltage (V_T) of the device. It is usually made of aluminum or poly-silicon according to design specifications. The gate electrode is isolated from substrate by a dielectric which is an oxide usually of SiO_2 or any other high-k dielectric oxide. The oxide reduces the leakage current; however, there may be interface trap charges near the oxide-semiconductor interface. This may degrade device performance.

2.2: Principle of Operation

An n-channel MOSFET is shown in Figure 2.1. Two n^+ regions are formed in the p-type silicon using diffusion or implantation. The gate electrode and conducting channel (L) are separated with the help of silicon dioxide layer, which is beneath the gate and sandwiched between the drain and source regions.

The parameters are channel width (W), oxide thickness (T_{ox}), channel (L) which is the distance between two diffused regions, the doping concentration (N_D) and junction depth X_j. Field oxide is thick enough to isolate MOSFET from other devices in VLSI circuits.

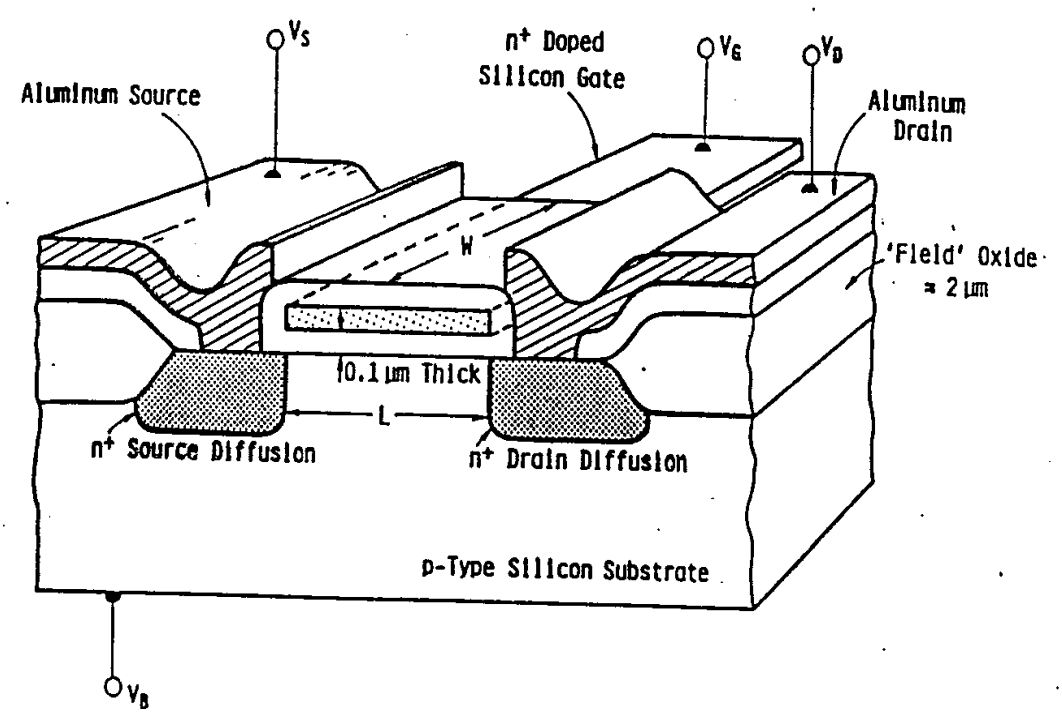


Figure 2.1 MOSFET cross-section [7]

The drain-source current is controlled by the gate voltage applied to the gate electrode. No current flows from drain to source if there is no conduction n-channel between them. When

no voltage is applied to the gate, no channel is formed hence no current flow through the device. So, MOSFET is considered in OFF state when no charge is applied to the gate relative to the p-substrate. When positive charge is applied to the gate voltage it repels the holes from the Si-SiO_2 interface and negative charges get induced in the Si substrate, by the formation of depletion region and thin surface region containing mobile electrons. These electrons from the channel in the device, allows current to flow from drain to source. MOSFET is considered in ON state when the channel is formed between drain and source. The drain current of device can be modulated by varying the gate voltage (V_G). The minimum gate voltage, at which thin layer of region of electrons is formed near the interface is called threshold voltage (V_T) [8].

The MOSFET is a gate controlled device, should have low leakage p-n junction and high quality to ensure better opertaion. Similary for a p-channel MOSFET, positive charges are induced in the Si substrate by applying a negative voltage on to gate metal. These holes from the channel of the field-effect-transistor, and allow current to flow from drain to source. Both n-channel and p-channel MOS transistors are used in many applications. However, n-channel MOS transistors are preferred because of the electron mobility in silicon substrates in more than mobility of holes in p-channel MOS transistors.

2.2.1: Importance of gate oxide

Moore's law suggests gate oxide thickness would be as low as 1.5 nm in the year 2006. As the scaling of devices continues and need for high speed processors, SiO_2 does not have the dielectric constant, k, to with stand scaling till 2006. If the thickness is reduced, hot electrons are high energy electrons which can tunnel through the oxide layer and become excess charge in the

oxide. This may lead to failure of the device with time. The effect of direct tunneling is shown in Figure 2.2.

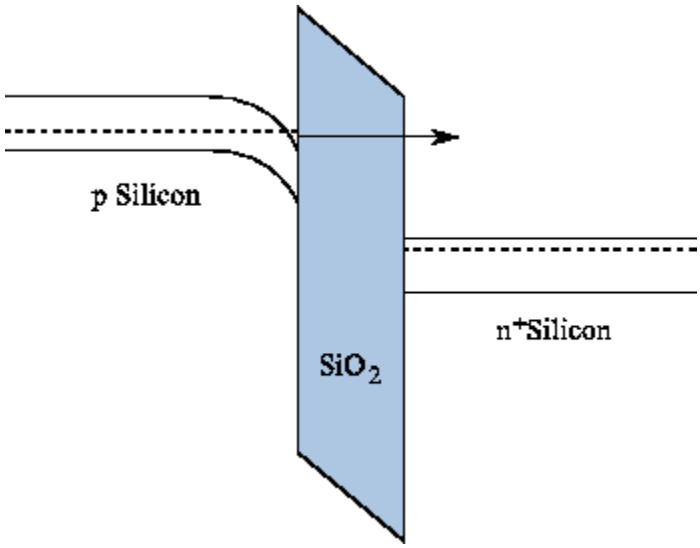


Figure 2.2 Direct tunneling effect [9].

The oxide capacitance (C_{ox}) is a parallel plate capacitor whose plates are separated by gate oxide thickness (T_{ox}). Here the two plates are gate metal electrode and the channel formed i.e. semiconductor region. Current flowing in the device is inversely proportional to the gate oxide thickness. Decreasing oxide thickness will also lead to electron tunneling and causing loss of voltage control in the gate. The oxide capacitance is given by the following equation.

$$C_{ox} = \frac{\varepsilon_o * k}{T_{ox}} \qquad (2.1)$$

Where C_{ox} is the oxide capacitance, k is the dielectric constant of the dielectric material used as gate oxide, ε_o is the relative permittivity of free space and T_{ox} is the oxide thickness. As it can be seen oxide thickness is a major factor in calculating oxide capacitance, reduction in the

thickness can lead to high leakage current. So to avoid thin oxide layer, lot of research on high-k material is going on which if used as the gate oxide will result in giving thicker oxides without reducing the capacitance and transconductance of the transistor.

2.2.2: Equivalent oxide thickness

The gate oxide thickness determines the good control of the MOSFET depending upon the oxide capacitance of the given film. Equivalent-oxide-thickness (EOT) is defined as the thickness of SiO_2 which can obtain same capacitance density as any other high-k dielectric oxide. Let us assume EOT to be equivalent oxide thickness needed, T_{DES} be the desired film thickness, ε_{SiO2} is the dielectric constant of SiO_2 and ε_{HIGHK} is the dielectric constant of high-k dielectric material to be used. EOT is given by following equations 2.2 and 2.3 [10].

$$EOT = \left(\frac{\varepsilon_{SiO2}}{\varepsilon_{HIGHK}}\right) * T_{DES} \quad (2.2)$$

$$EOT = \left(\frac{3.9}{\varepsilon_{HIGHK}}\right) * T_{DES} \quad (2.3)$$

The above equation shows oxide thickness of high-k material is more than that of SiO_2 which would yield the same gate oxide capacitance and have the same command over MOSFET.

2.2.3: Effect of charges in MOSFETs

There are four types of charges associated with MOS device. They are

- Interface trapped charges (Q_i)
- Fixed oxide charges (Q_f)
- Oxide trapped charges (Qt)

- Mobile oxide charges (Q_m)

Interface trapped charges are positive or negative charges which arise due to structural defects, oxidation induced effects, metal impurities, or through bond-breaking process. These charges are located at Si-SiO_2 interface. Interface trapped charges can be reduced by following proper cleaning procedure and be neutralized by low temperature anneals.

Fixed oxide charges occurs during oxidation where Si is removed from the surface and reacts with oxygen. Some ionic Si is left near the interface during oxidation is stopped, during which these ions combine with uncompleted Si bonds results in positive charge near the interface.

Oxide trapped charges occurs during contamination of the oxide with N_A which forms oxide and due to imperfections in the oxide SiO_2.

Mobile oxide charges occur when sodium ions introduce positive charges in the oxide. This charge is mainly contributed by ionic impurities such as Na^+, Li^+, K^+ and H^+. Negative ions and heavy metals contribute to these charges.

The effect of interface charges should be reduced to a minimum. The interface charges are more than (111) surfaces rather than in (100) surfaces. This is reason why MOSFETs are made on (100) Silicon [4].

2.2.4: Threshold voltage

Threshold voltage is the important parameter which determines the gate voltage required to induce the conducting channel for operation of the MOS device. The threshold voltage [6] for p-MOSFETs is given by equation 2.4.

$$V_T = \emptyset_{ms} - \frac{Q_i}{C_{ox}} - \frac{Q_d}{C_{ox}} + 2 * \emptyset_F \qquad (2.4)$$

The threshold voltage for NMOS is given by 2.5

$$V_T = \emptyset_{ms} - \frac{Q_i}{C_{ox}} + \frac{Q_d}{C_{ox}} + 2 * \emptyset_F \qquad (2.5)$$

Where V_T is the threshold voltage of the device, $\emptyset_{MS}$ is metal-semiconductor work function, Q_i is the interface trap charge between the substrate-oxide interface, Q_D is the depletion charge in MOS device, C_{ox} is the oxide capacitance of the dielectric material which is sandwiched between the substrate-oxide interface and $\emptyset_F$ is the Fermi potential of the substrate and depends upon the doping of the substrate.

The threshold voltage is controlled by the gate oxide thickness and doping concentration of the substrate, the threshold voltage remains negative for p-channel MOSFETs and for n-channel MOSFETs it may remain positive or negative some times.

The threshold voltage increases with increase in N_A or N_D which is a factor in Q_D and $\emptyset_F$ term. The interface charge Q_i should be kept to a minimum to have low threshold voltages. Similarly, materials having high dielectric constant value increase the oxide capacitance (C_{ox}) which in turn minimizes the threshold voltage (V_T). The threshold voltage should be around -1 to 1 volt for n-channel MOSFETs and 0 to -1 volt for p-channel MOSFETs.

2.2.5: Threshold Voltage Adjustment

The threshold voltage can be controlled by ion implantation. Precise quantities of boron impurities are added to the p-channel MOSFETs to reduce the donor ions in the n-substrate. This is done to reduce the depletion charge Q_D and to make threshold voltage less negative. Similarly, the boron implant is made shallow in a p-substrate of an n-channel MOSFETs to make threshold voltage less positive. The relationship between shift in threshold voltage ΔV_T and implanted dose Q_{im} is given by the following equation 2.6 [11]

$$\Delta V_T = \frac{q * Qim}{Cox} \qquad (2.6)$$

Where C_{ox} is the oxide capacitance and q is the electronic charge of an electron. This kind of adjustment is usually done in industries having large scale production of MOS devices. These are the reasons having thicker oxide thickness with high dielectric constant and withstand direct tunneling.

CHAPTER 3: LITERATURE REVIEW

High-k materials will be used to replace silicon dioxide in near future. The high-k materials which are the focus of this work are hafnium oxide (HfO_2) and titanium oxide (TiO_2). These materials were chosen because of their relevant structural and special properties. The dielectric constants of HfO_2 vary from 22 to 30 whereas the dielectric constant of TiO_2 vary from 40 to 86. The high-k layers are thick enough to prevent direct tunneling between the gate and silicon substrate. The increase in film thickness can reduce tunneling leakage current and improve reliability while scaling capacitance equivalent oxide thickness below the direct tunneling limit [12].

3.1: Hafnium oxide

Hafnium oxide is a high-k dielectric material whose average constant is around 22-25 [12,13]. It has high dielectric constant compare to SiO_2 dielectric films. It is thermally stable over silicon substrate and has a high energy band gap around 5.8 eV. It is used in nano-scaled CMOS and memory devices such as DRAM cells [14]. Hafnium oxide has higher electrical permittivity and improves the gate dielectric layer with its properties. It is used for low power applications and has uniform thickness over the substrate. The effects of direct tunneling are reduced by HfO_2 as gate oxide. The leakage current of HfO_2 is lower than the same equivalent oxide thickness of SiO_2 film. Because of the large barrier in HfO_2 holes (3.4eV) with respect to electrons (1.5eV), the injection of holes is much smaller than the injection of electrons for HfO_2 film. The hafnium oxide is able to withstand dynamic stress in a long term for MOS devices so that the time for breakdown increases and has less interface traps formed [15].

3.1.1: Deposition techniques of Hafnium oxide (HfO_2)

Hafnium oxide can be deposited using different methods. Different methods give different values dielectric constant of HfO_2. Few of the different methods are chemical-vapor-deposition (CVD) [16], reactive sputtering, ultraviolet ozone deposition (UVO) and atomic layer deposition [17]. These deposition techniques need very precise equipment which is costly. The technique that is used in this work is reactive sputtering. Different conditions were tried to achieve high dielectric constant. These conditions are briefly described in the Table 3, with the dielectric constant values that were achieved. During reactive sputtering, that is discussed in next chapter, the reactive gas used is O_2 may lead to formation of SiO_2 interfacial layer thus reducing the total gate capacitance. To avoid this condition, a thin layer of hafnium metal is sputtered directly thus cutting the interaction of oxygen with silicon. Later the usual sputtering of Hf with reactive gas was carried out to form HfO_2 layer. To remove any defect if present in the oxide layer after sputtering it is been advised to anneal the sample for 30 min at 450 with O2 gas flow.

3.2: Titanium oxide (TiO_2)

Titanium dioxide has recently been extensively studied oxides because of its remarkable optical and electrical properties. Studies on thin films of TiO_2 have reported dielectric constants that range from 40 to 86 [18]. It is believed that this variability is related to the presence of low-permittivity interfacial layers and to the dependence of permittivity on crystalline phase. It has a high dielectric as compared to SiO_2 and HfO_2. The bandgap of the material is reported to be between 3.0 and 3.5 eV, depending on the crystalline phase and purity. The impurities present in the oxide layer can cause formation of interfacial layer and also can lead to trapping of atoms.

These impurities can be partially annealed during the post-deposition heat treatments, but in general they serve as complementary sources of disorder-induced traps.

3.2.1: Deposition of Titanium oxide

Similar to hafnium oxide, titanium oxide can also be deposited by different methods. The dielectric constant also varies with different methods. The effective method of deposition is to get a titanium oxide layer deposited on silicon substrate with no interfacial layer and less interface trap charges. Various deposition techniques such as chemical vapor deposition, sol–gel deposition, and magnetron sputtering have been used to produce TiO_2 films. The magnetron sputtering technique has emerged as one of the most promising techniques. TiO_2 films were formed using different techniques as shown in Table 4. For TiO_2 sputtering technique, DC as well as RF sputtering was used. It has been observed that if DC sputtering is used it can lead to higher deposition rate as compared to RF [19].

CHAPTER 4: METHODOLOGY

In this chapter, the techniques and the procedure of fabricating MOSFET device, MOS capacitor, MIM devices are discussed. This chapter also discusses various equipment used in fabrication of above mentioned devices. It briefly outlines different electrical measurements like I-V Characteristics, C-V Characteristics, and Capacitance measurements.

Sputter deposition technique is used to deposit oxide film. Sputter deposition is a physical vapor deposition (PVD) method of depositing thin films by eroding material from a source, which reacts with the reactive gas and gets deposited onto a substrate. The advantage of sputtering is that the deposited films have the same composition as the source material.

Magnetron sputtering is a technique where strong electric and magnetic fields is used to trap electrons close to the surface of the target. Electric field supplied to the target could be either Direct Current (DC) or Radio Frequency (RF) depending on the targets used. DC biasing power source is used for metal targets whereas insulating targets can cause buildup of charges that is why RF biasing power source is used for it. Sputtering deposition sources (also called sputter "guns") create low pressure plasma by the excitation of an inert gas (typically argon) contained in a vacuum chamber at 1 to 50 mTorr. This process accelerates energetic ions towards the cathode target, striking it with kinetic energy up to several hundred electron volts. Thus ejecting material atoms from the target with approximately 90% left as neutral atoms and 10% as ions as a result of energy transfer. Gas phase collision between target atoms and argon atoms leads to scattering of the ejected material which reacts with reactive gas forming a distributed cloud. As the cloud migrates towards the substrate, the random approach angles result in deposition of a uniform film, even on surfaces that have micron-sized vertical structures.

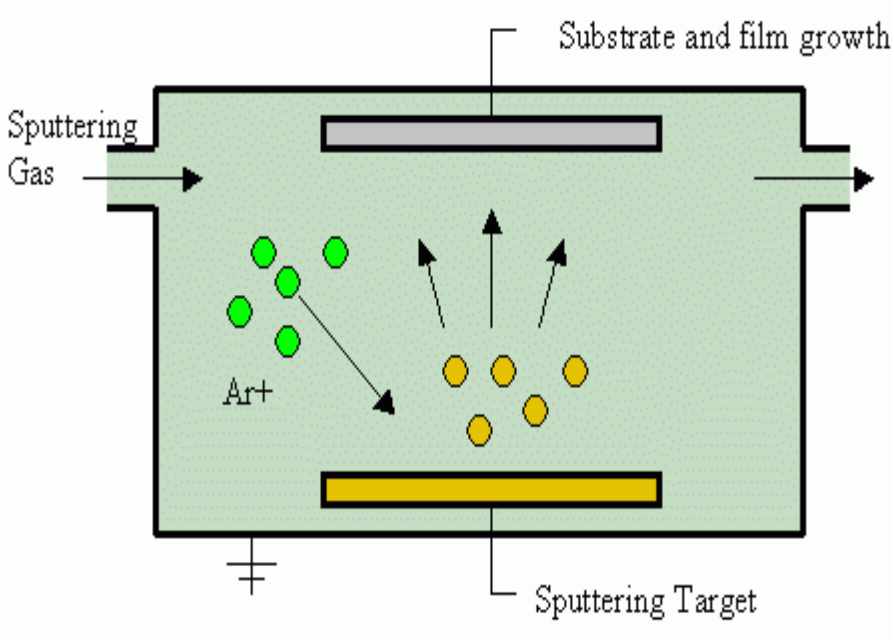


Figure 4.1 Sputtering Process Cartoon [20]

Thin films of HfO_2, and TiO_2 were deposited by reactive RF and DC magnetron sputtering in an ultra-high vacuum (UHV) system. Three inches Hf and Ti target, respectively, with a purity of 99.5% are used. The system base pressure was approximately 2×10^{-7} Torr and the purity of the process gas. Reactive sputtering was used where the deposited film is formed by chemical reaction between the target material and a reactive gas oxygen which is introduced into the vacuum chamber. Oxide and nitride films are fabricated using this technique. The composition of the film is controlled by changing gas flow ratios of inert and reactive gases. In this case oxygen was used as the reactive gas.

4.1: Ohmic contact for Germanium

Ohmic contact for Germanium wafer was performed, and is described in this section. The procedure for cleaning the substrate was obtained from the paper mentioned in Ref [21]. The substrate was initially dipped in DI (De-Ionized) water for 30 sec to dissolve the native oxide grown on the wafer and then it was followed by dipping in H_2O_2 solution with 30% concentration for 30 second to grow fresh oxide layer. Later, the sample was immersed in HF with 10% concentration for 10 min to remove the oxide giving us oxide free samples. Finally it was blow dried with N_2 gun. The sample is then ready for metallizing and plating.

4.1.1: Preparation of the base Al electrode

The wafer has two sides; top side is well polished and is considered the smooth side whereas the bottom is called as rough side. Usually the top side is used for fabrication of actual device whereas sometime the bottom is used as electrodes. In this process, the bottom part of the sample is aluminum electrode which is deposited in a vacuum thermal evaporation system. The chamber is initially under 50 mTorr or less pressure. To open evaporation chamber, pressure is released by opening the vent. Vent slowly releases the pressure and finally the sample holder can be removed. The samples are placed on the ceiling of the chamber and aluminum strips on the filament (placed on the bottom floor of the chamber) which is used for evaporating the strips by passing high current through it. Depending on the thickness of the film, the amount of Al wire used is determined. In this process a thick film is required so two pieces of Al wire (2.5 cm of length) each are used. After closing the evaporation chamber, it is roughed from atmosphere pressure (since the chamber was wide open) to the pressure of 50 mTorr with the help of a

mechanical pump (Backup pump). Then the mechanical pump is closed and the fore-line valve is opened. Cryo pump is used as the fore-line pump. Cryo pump is a high-vacuum pump which traps gases and vapor by condensing them on a cold surface, thus creating a vacuum. It helps in pumping down the system from 50 mTorr chamber pressure to 1 x 10^{-5} Torr. When the required pressure is achieved, a high current is passed from the filament by slowly incrementing the current from 0A to 35A. 35A is maintained for a minute for proper uniform deposition of Al on the substrate. After that another minute is left for degassing. Finally the chamber is opened by opening the vent again. Using this process an Al electrode is achieved on the bottom side of the sample.

To get a better electric contact the samples are annealed at different temperature for about 30 minutes with a flow of 10 cc of Ar gas. This process is called as post-deposition annealing. It helps in reducing stress as well as for inducing any desirable reaction between the deposited metal and semiconductor wafer.

4.1.2: Preparation of the plating solution

Electroless nickel plating on germanium wafer is used to have an ohmic contact. The plating solution was made up of following materials [22]:

Nickel Chloride, $NiCl_2.6H_2O$ (25gm/litre)

Sodium Hypophosphite, $NaH_2PO_2H_2O$ (25gm/litre)

TetraSodium pyrophosphate, $Na_4P_2O_7.10H_2O$ (50gm/litre)

For the process to take place, the solution has to maintain an overall pH between 9 and 11 at 90 to 95 ^oC. To maintain the pH of the solution a required amount of ammonia is added. The

deposition nearly takes place at the rate of 2000 Å per minute. The deposition of nickel is according to the Equations 4.1, 4.2 and 4.3

$$NiCl_2 \leftrightarrow Ni^{++} + 2Cl^- \quad (4.1)$$
$$H_2PO_2 + H_2O \leftrightarrow H_2PO_3^- + 2H^+ + 2e \quad (4.2)$$
$$Ni^{++} + 2e \leftrightarrow Ni \quad (4.3)$$

4.1.3: Electroless Plating Nickel

The samples obtained from the thermally evaporated Al with post-annealing will go under electroless plating of nickel to get an ohmic contact. To avoid plating of nickel to the Al deposited side, this side is covered with positive photoresist (PR). To apply photoresist, a spinner is used. The sample is placed on the spinner, it holds the sample with vacuum during the spin. Now the rpm and time of spinning is set as required. For this process the rpm is set to 3000 rpm and the spinning time is 30 seconds. Photoresist syringe is filled with Shipley 1813 positive photoresist, it is then poured over the Al deposited side of the wafer. After running the spinner a thick layer of photoresist is obtained. Extra photoresist is removed if present on the top side by acetone. The photoresist is harder, so that it does not dissolve in the plating solution, by placing the samples (the photoresist side facing up) on an Al hot plate in a Blue M oven which is at 100 ^{o}C for 10 minutes (hard bake). Samples are ready for electroless nickel plating. Heat the plating solution around 90^{o}C, now immerse the sample and add required amount of ammonia simultaneously. The sample was removed after a uniform Ni layer with required thickness was formed. It is thoroughly cleaned by rinsing it with DI water. The photoresist is removed using acetone before annealing. Ni plated sample is annealed at different temperature and time.

4.2: Fabrication of MIM devices

MIM stands for Metal-Insulator-Metal devices. The Corning glass slide is used as substrate to fabricate the MIM structure. A standard cleaning procedure is followed to clean the substrate it includes rinsing the substrate with acetone, followed by methanol and then DI (De-ionized) water. After rinsing properly to remove any organic debris/substances present on the slide, blow dry it with Nitrogen (N_2) gas jet.

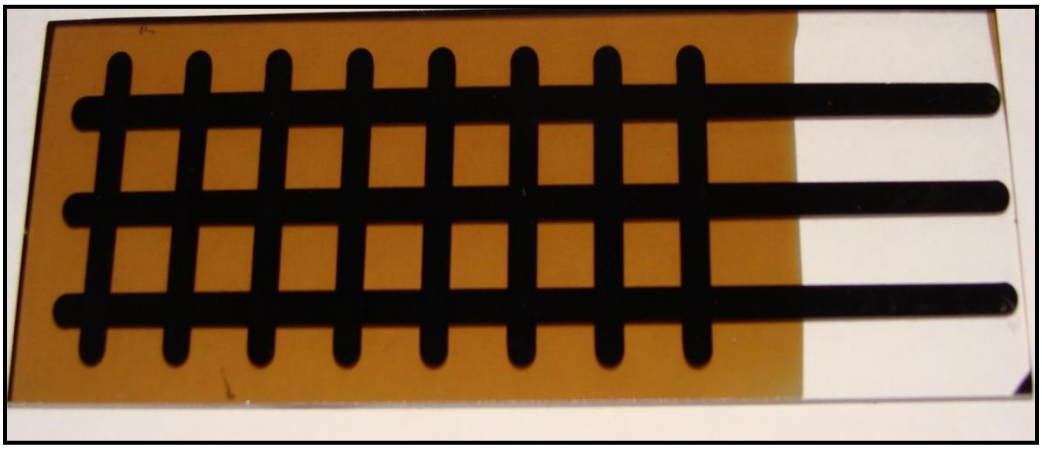


Figure 4.2 MIM structures (Al-oxide-Al) on a glass substrate [20]

4.2.1: Dielectric Sputter Deposition

The Aluminum electrodes of 3mm wide which run horizontally are deposited using Thermal Evaporation system as mentioned above in Section 4.1.1. The oxide film is deposited on a glass substrate by using sputtering technique. The sputtering system consists of 3 inch Hf and Ti targets which is used for deposition of the oxide film on the substrate by reactive sputtering. The base pressure of the chamber was achieved in the range of 2×10^{-7} Torr. The O_2/Ar gas flow ratio, R.F power, partial pressure and time of deposition were varied to grow an oxide film which gave the perfect dielectric constant. By changing the above mentioned parameters, O_2/Ar total

gas flow was kept constant at 20 sccm. The thickness of the oxide films obtained is measured by α-step Profilometer. The HfO_2 and TiO_2 thicknesses ranged from 300 Å - 2000 Å and 100 Å - 700 Å respectively. Thermocouple attached to the substrate holder was used to measure the temperature of the substrate and it was noted in steady state condition. The rotation speed of the substrate was set around 20 rpm.

First, the samples are loaded into the load lock system attached to a substrate holder and it is pumped down (roughing) from atmospheric pressure to 5×10^{-5} Torr. Then the samples are introduced to the main chamber from the load lock system by opening the valve between them and the substrate holder with the samples are placed to a pre-set distance from the target. The target is placed facing the substrate holder at an angle of 45^{o}C. When the samples are positioned accordingly, RF power is started from 0W to 200W in small incremental steps and made sure the plasma is sustained for the rest of the sputtering process. The desired O_2/Ar flow ratio is maintained and the partial pressure in the chamber and the desired temperature is maintained as required. Now the sputtering is started in the chamber by opening the lid covering the target and it is left open for the decided time for sputtering.

4.2.2: Metallization

Lastly, aluminum electrodes of 3mm width each running vertically were deposited on the oxide layer to form the top layer electrode of the MIM structures using the vacuum thermal evaporation method as explained previously. The substrates are dealt with same cleaning procedures before all three kinds of depositions.

4.3: Fabrication of MOS capacitor devices

MOS stands for Metal-Oxide-Semiconductor. A MOS capacitor is made up of semiconductor body or substrate, an insulator film, such as HfO_2 or SiO_2, and a metal as gate electrode. MOS capacitors are usually fabricated to learn the properties of the insulator film i.e. gate oxide. Si wafer were used as substrate to fabricate this structure with following information:

Orientation: (100)

Resistivity: 8.1 Ω/cm

Thickness: 575 -675 um

Sheet resistance: 120 Ω/square

Type: P and N

The general cleaning procedure for a Si wafer is used which involves scrubbing the substrate with Alconox (detergent) and DI water to remove bulk contamination. Rinse the substrate through with DI water to remove the detergent. The substrate is then rinsed in trichloroethane (TCE) to remove any contamination left. It is later rinsed with - acetone to remove any TCE residue, methanol to remove acetone residue and finally by DI water to remove methanol residue. The substrate is now dried with nitrogen gas jet. It is always good to make sure that there is no surface oxide before depositing the insulating film. The surface oxide if present will add an additional parasitic capacitance which may hinder the total capacitance value of the device. Hence an oxide etch is performed in Buffered Oxide Etch (BOE) 9:1 for 30 seconds in a plastic petri dish. This is to remove any native oxide present on the substrate. Finally clean the substrate with DI water and dry it with N_2 gun.

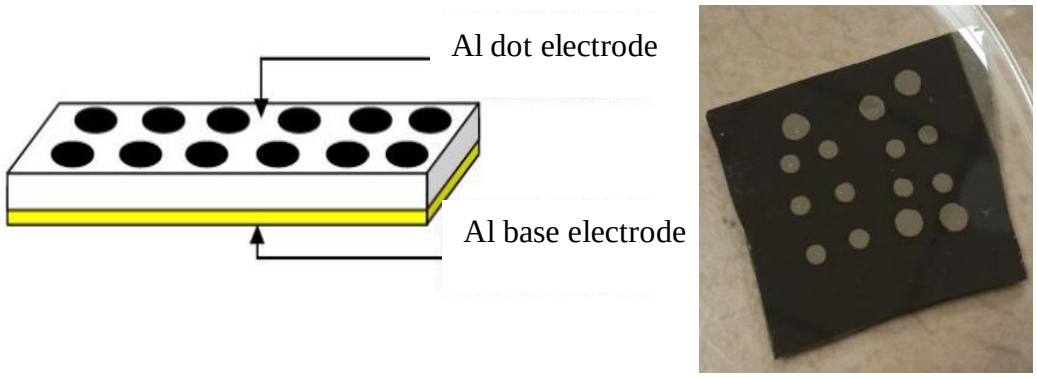


Figure 4.3 (a) Front-view of MOS capacitor (b) top-view of the fabricated MOS capacitor

4.3.1: Fabrication of MOS capacitor with HfO_2 as dielectric

The MIM device results as discussed in chapter 5 concluded that HfO_2 oxide film represented better properties compare to TiO_2, film, and the measured values were close to theoretical results. Hence MOS capacitors with HfO_2 were fabricated. In this section, MOS capacitor with HfO_2 as gate dielectric fabrication process is discussed. HfO_2 is deposited by sputtering technique on the cleaned Si substrate attained from the above process. The reactive sputtering process is same as discussed in Section 4.2.1. Rapid thermal annealing (RTA) at 600^oC was performed for 90 second after sputtering. After RTA, the bottom Al electrode is deposited using Thermal evaporation technique.

4.3.2: Metallization

Aluminum dot electrodes of different size were deposited using thermal evaporation technique on both types of samples. For aluminum dot electrode a shadow mask was used with different size circles. Then C-V characterization was performed on the final samples.

4.4: MOSFET fabrication

The p-type Si wafers were cleaned in the same process as discussed in Section 4.3. For fabrication of MOSFET device 4 level mask was used. Generally, the three level masks is enough for fabrication of MOSFET since same metal (aluminum) is used for source, drain and gate. The four level masks is designed for future use, the fourth level has the gate contact layout. Thus when the gate metal contact is different from the metal contacts of source and drain the four level mask is used. The design dimension of the device in each mask is given in the Appendix A.

4.4.1: Field oxide growth

This process is used to grow field oxide to serve as a mask during phosphorus diffusion. In this process wet oxidation furnace is used. For the field oxide to act as a mask, the thickness of oxide layer should be 4500Å or above. The wafer was loaded on a quartz boat and placed inside the furnace which was at 1100 ^{o}C for 45 min. Nitrogen gas with pressure 5 psi and 1 on flowmeter tube is passed through the steam bubbler into the furnace. It helps in pushing the water vapor into the furnace. The push and pull rate was 3 min each. The oxide grown reflected violet color, indicating that a 4800 Å SiO_2 has been grown, with the help of a color chart.

4.4.2: Negative PR process

NRP 1500P negative photoresist (PR) was spin coated at 3000 rpm for 30 seconds. It is soft baked at 150 ^{o}C in Blue M oven for 1 minute on a hot aluminum plate. Clear Field Mask#1 (Figure 4.5(A)) was used to define the source and drain diffusion areas using the Karl Suss mask aligner. The wafer was coated with negative PR is kept under the mask and after the hard contact

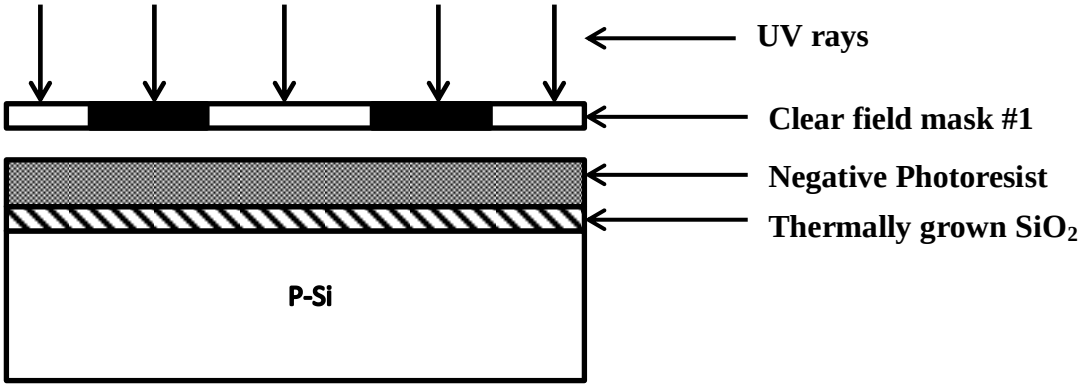
between the substrate and the mask, the photoresist is exposed Ultraviolet (UV) rays for 10 seconds. Thus, transferring the pattern from mask to the wafer as shown in Figure 4.5(B). The photoresist is then developed using the negative PR developer solution, i.e. RD5 for 30 seconds. After development the pattern is examined under the microscope to confirm the development was perfect.

4.4.3: Oxide Etch process

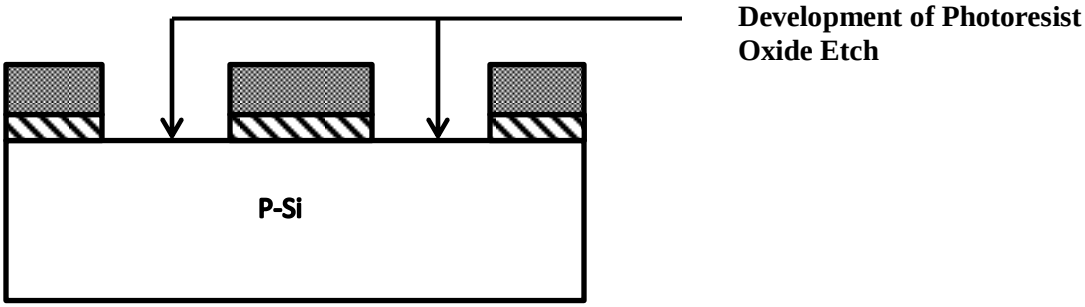
The source and drain windows opened in PR process is etched BOE (9:1). Since the other area other than source and drain region is covered by PR hence they are protected from etch. The field oxide thickness grown in the wet oxidation process is 4800Å. The etching rate of oxide etch for SiO_2 is 600 Å/min, thus the etching time for field oxide is 8 minutes. Thoroughly clean with water and blow dried with N_2 gun. Examine the device under the microscope to check for clean edges from oxide etch, if there are rough edges etch the oxide again. Strip the PR after clean edges are achieved with acetone, methanol and DI water. Use Plasma Etch if PR was not properly stripped.

4.4.4: Phosphorus Diffusion and Drive-in

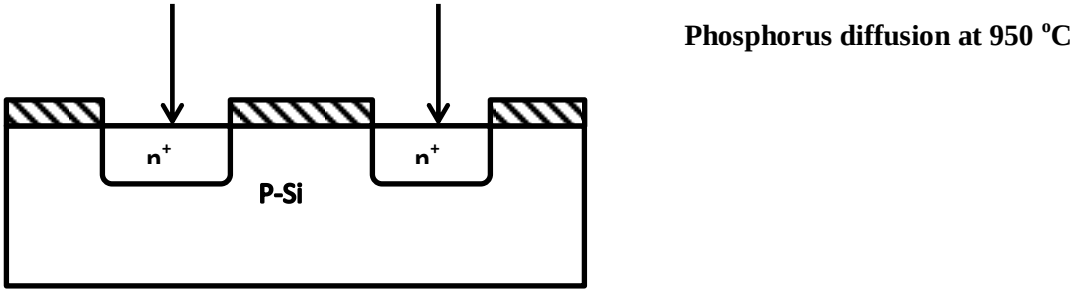
Place the device and control wafer (used to determine the) with phosphorus sources on quartz boat and the boat is loaded in the diffusion furnace which at 950 ^{o}C for 15 minutes. The pull and push time is 1 minute each. N_2 gas with pressure 5 psi and 4 on the flowmeter is passed into the furnace. The control wafer was tested for type and sheet resistance using four point probe. It indicated n-type dopant on the surface and sheet resistance was 29Ω/square.


UV rays
Clear field mask #1
Negative Photoresist
Thermally grown SiO_2
P-Si

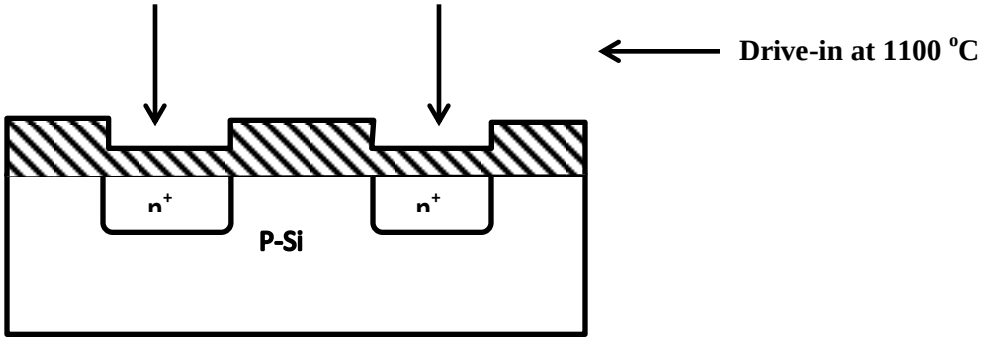
(A)


Development of Photoresist
Oxide Etch
P-Si

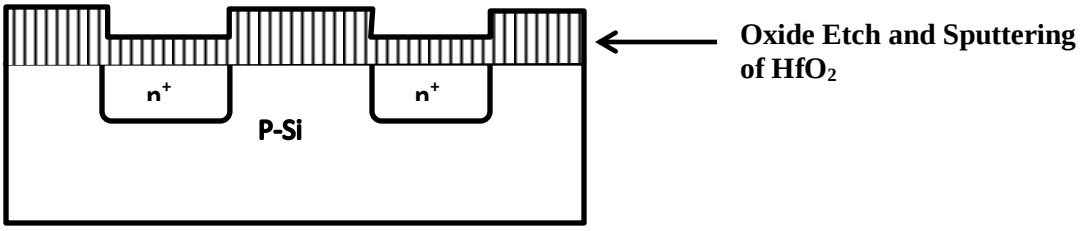
(B)


Phosphorus diffusion at 950 °C
n+
n+
P-Si

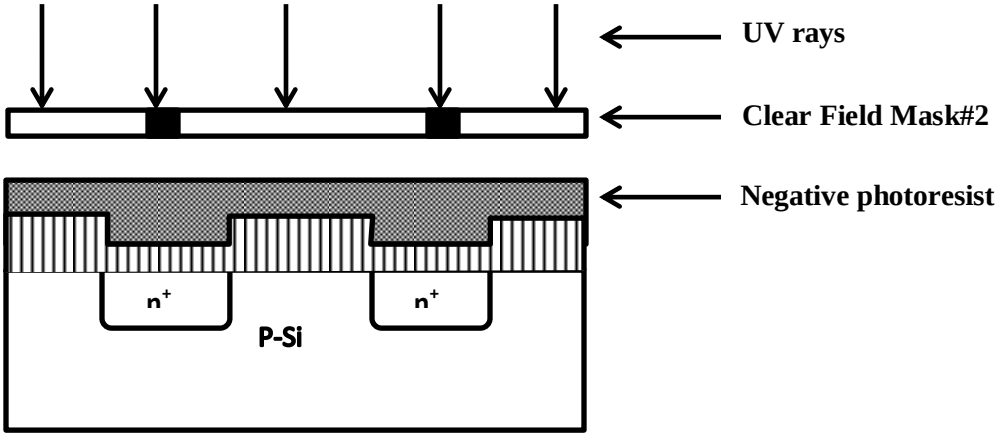
(C)


Drive-in at 1100 °C
n+
n+
P-Si

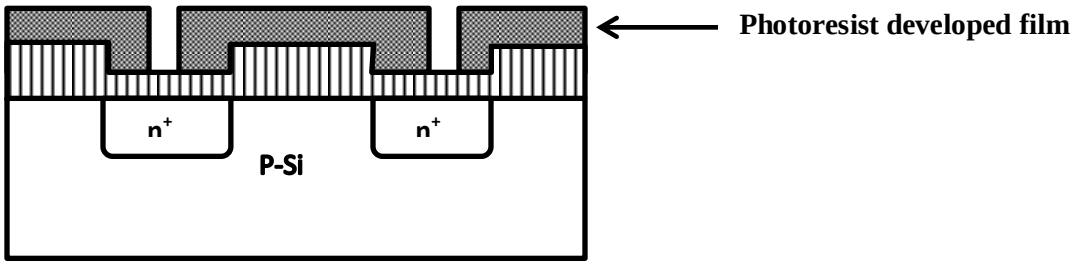
(D)


Oxide Etch and Sputtering of HfO_2
n^+
n^+
P-Si

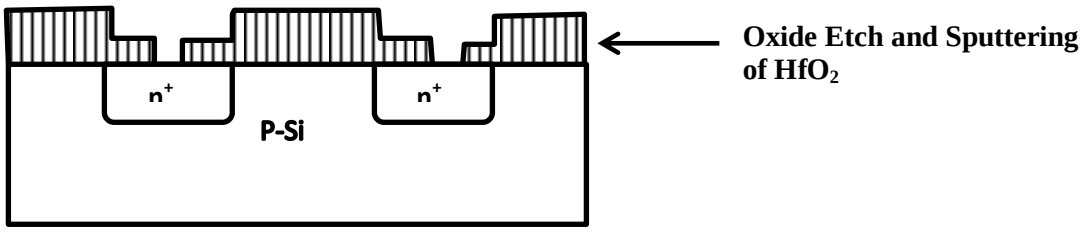
(E)


UV rays
Clear Field Mask#2
Negative photoresist
n^+
n^+
P-Si

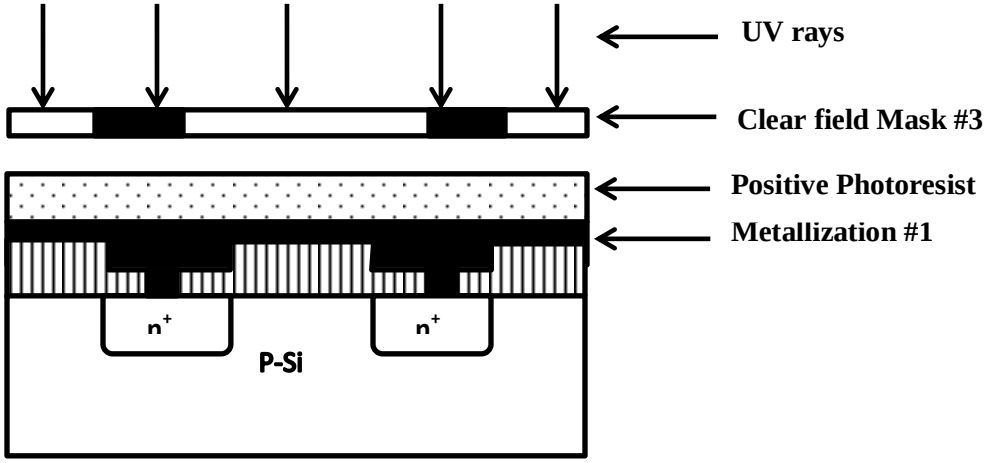
(F)


Photoresist developed film
n^+
n^+
P-Si

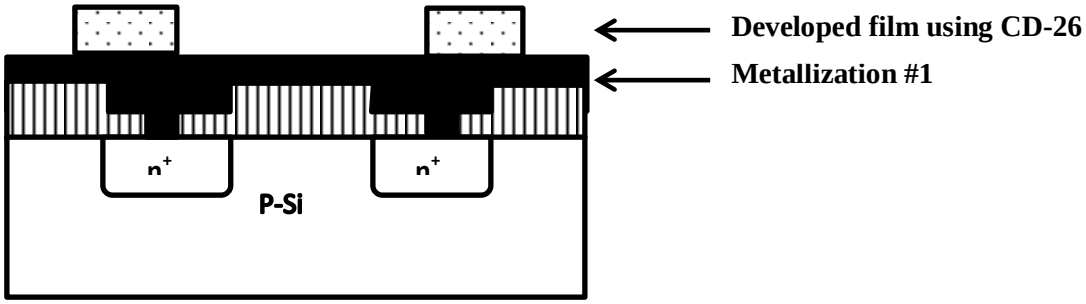
(G)


Oxide Etch and Sputtering of HfO_2
n^+
n^+
P-Si

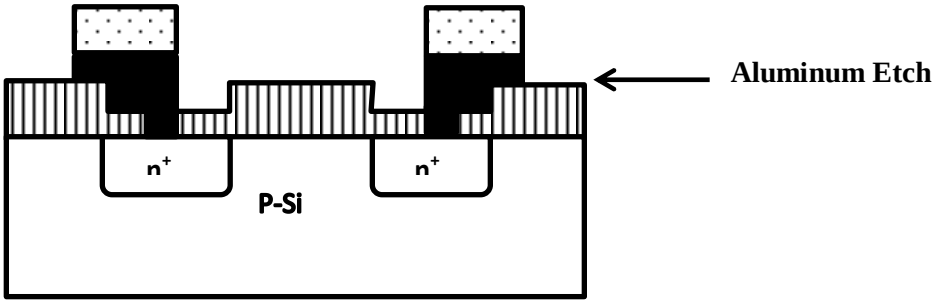
(G.1)


UV rays
Clear field Mask #3
Positive Photoresist
Metallization #1
n+
n+
P-Si

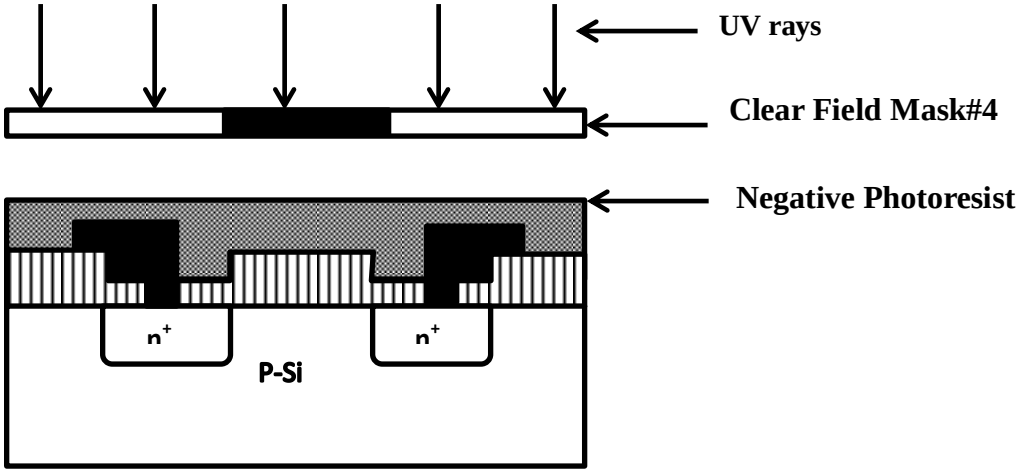
(H)


Developed film using CD-26
Metallization #1
n+
n+
P-Si

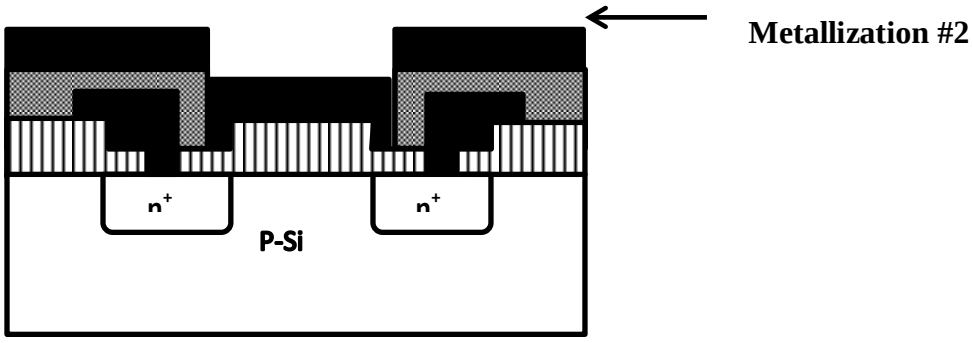
(I)


Aluminum Etch
n+
n+
P-Si

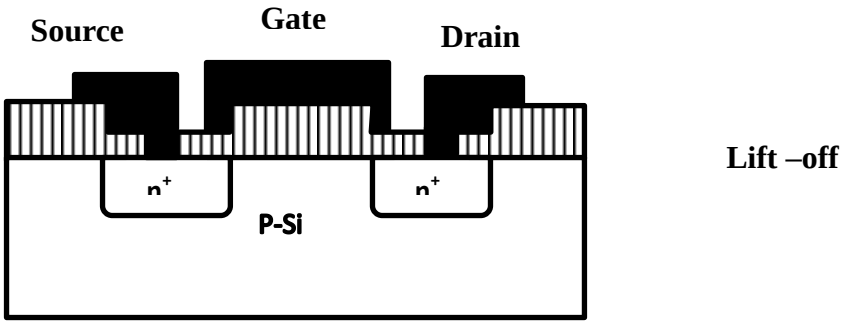
(J)



(K)



(L)



(M)

Figure 4.4 Fabrication Process Stepwise

Figure 4.5 Fabricated MOSFET devices with HfO_2 as gate dielectric

The wafers were then loaded in oxidation furnace at 1100 ^oC for 30 minutes for a drive-in process. The pull and push time was 3 minutes each. The color of the oxide on the control wafer was blue and it implies that a 3000Å was grown. The control wafer was then etched to remove the oxide grown for 3 minutes. The wafer was again tested for type and sheet resistance. It indicated n-type dopant on the surface and sheet resistance was 14Ω/square. This process is shown in the Figure 4.5(C) and (D).

4.4.5: Strip Oxide and Sputtering of HfO_2

SiO_2 is completely etched by immersing the device in BOE for 12 minutes. Make sure the oxide is completely etched by dewetting of water over the surface of the wafer while washing with DI water. HfO_2 film is sputtering on the device using reactive sputtering technique as described in Section 4.2.1. A glass substrate along with the device is placed in the sputtering

system. Hafnium target is at the bottom with a 45° inclined and the samples are placed on the top. The system pressure is kept at 12 mTorr with power supplied to the target is 200W. The desired O_2/Ar flow ratio i.e. 4:1 is maintained. Hf was sputtered by opening the lid covering the target and it is left open for the 1 hour. The rotation speed of the substrate was set around 20 rpm. The device after this process is shown in Figure 4.5(E). As the annealed samples showed better results in the C-V characteristics as discussed in Section 5.4, the sample was annealed at 500°C for 30 minute.

4.4.6: Negative PR process and Oxide Etch

The device was spin-coated with negative PR as before. Soft-bake at 150° C was performed in Blue M oven for 1 minute before it was exposed to UV rays. For this process Mask#2 (as shown in Figure 4.5(F)) was used and the mask was aligned with the wafer using Karl Suss mask aligner. After exposure, the sample was baked at 100 ° C for 1 minute. The sample was dipped in RD5 developed used to develop negative PR and examined under microscope to check the developed film. The sample was hard baked at 150 ° C for 3 minutes and then it was proceed to oxide etch. The oxide etch rate of BOE for HfO_2 is 60 Å/min and as the thickness profilometer defined 600Å as the thickness of the sputtered HfO_2 film, the sample was immersed in oxide etch for 10 minutes. Strip the PR after clean edges are achieved with acetone, methanol and DI water. This process is used to create via for the metal contact to the source and drain region on the wafer as shown Figure 4.5(G.1).

4.4.7: Metallization #1 and positive PR process

Aluminum was deposited on the device to form source and drain contacts. These contacts were deposited by thermal evaporation. This deposited aluminum was coated with positive PR-Shipley 1813 and then soft baked at 100° C for 3 minute in the oven. To create contacts the device was exposed to Mask#3 for 10 seconds. The PR was developed in CD-26 for 40 seconds and then examined under the microscope. The device was rinsed in DI water and blown dry before it sample was baked at 100° C for 10 minutes. The pattern developed is shown in Figure 4.5(J).

4.4.8: Aluminum Etch

The aluminum which is left uncovered by PR is etched by Aluminum etch (1:3 phosphoric acid and DI water). The etching solution, poured in a glass petri dish, is heated to keep the solution warm at 35° C. The etching of the pattern is monitored and etched till all the uncovered metal is etched away. The time can vary depending on the thickness of the metal. The device is removed after etching and rinsed thoroughly with DI water and blow dry with N_2 gas. After the etching process, PR is stripped using acetone, methanol, DI water and dried N_2 gas.

4.4.9: Negative PR process and Metallization #2

The final Mask#4 is used to deposit the gate electrode. The use of 4^{th} mask is that the gate metal deposited can be different as compare to source and drain electrodes. For this case aluminum is used, now spin-coat the device with negative PR. Follow the same process (as Mask #3) for soft bake, UV exposure, post- expo bake, developing of the film and hard-bake.

Table 4.1 Process step of fabrication

PROCESS FLOW	**EXACT TIMINGS AND MEASUREMENT**	**PROCESS PARAMETERS**
Clean P-Si	R_{sh} = 180Ω/square ρ = 8.1 Ω/cm	Alconox (detergent), trichloroethane (TCE), Acetone, Methanol and DI water.
Wet oxidation	Color: Violet Thickness: 4800 Å	@ 1100°C for 30 minutes. Pull and push time – 3 min
Opening window for n+ (Phosphorus) Diffusion Mask #1	Soft-bake (150°C) = 1min Post-expo (100°C)= 1min Developing = 30 sec Hard-bake (150°C)= 3 min Etch time = 8 min	Negative PR (NRP 1500P), Mask Aligner (Karl Suss, expo time= 10sec), developer = RD5 and oxide etch (BOE)
Phosphorus diffusion	R_{sh} = 29Ω/square	@950°C for 15 min Pull and push time – 1 min
Drive-in (wet oxidation)	R_{sh} = 14Ω/square	@1100°C for 20 min Pull and push time – 3 min
Stripping Oxide	Etch time =12 min	BOE(9:1)
Sputtering of HfO_2 @RT	Thickness = 603 Å	RF Power supply = 200W O_2:Ar = 4:1 Sputtering pressure=12 mTorr Sputtering time = 1 hour
Formation of Via and Oxide etch Mask #2	Soft-bake (150°C) = 1min Post-expo (100°C)= 1min Developing = 30 sec Hard-bake (150°C)= 3 min Etch time = 10 min	Negative PR (NRP 1500P), Mask Aligner (Karl Suss, expo time= 10sec), developer = RD5 and oxide etch (BOE)
Metallization #1	Evaporation time = 1 min Pressure = 2 * 10^{-5} Torr Filament Current = 35 A	Thermal Evaporation Al - 2 inch strip
Source and Drain electrode (Mask #3)	Soft-bake (100°C) = 3min Developing = 40 sec Hard-bake (100°C)= 10 min Etch time = 1:45 min	Positive PR (Shipley 1813), Mask Aligner (Karl Suss, expo time= 10sec), developer = CD - 26 and Aluminum etch
Formation of gate electrode and metallization #2 (Mask #4)	Soft-bake (150°C) = 1min Post-expo (100°C)= 1min Developing = 30 sec Hard-bake (150°C)= 3 min	Negative PR (NRP 1500P), Mask Aligner (Karl Suss, expo time= 10sec), developer = RD5 and Thermal Evaporation
Lift – off	Till all the PR is cleaned	Petri dish with acetone placed on water bath in Sonicator

The pattern developed by Mask #4 is shown in Figure 4.5(K). After hard-bake, Aluminum is deposited on the device by thermal evaporation. A layer of aluminum gets deposited on the device as shown in Figure 4.5(L).

4.4.10: Lift-off

The final process is lift-off, it is used to remove the deposited aluminum other than the gate electrode. The negative PR below the aluminum can be stripped using Sonicator. In a Sonicator, the device, immersed in acetone in a petri dish, is placed on a bath of water. Ultrasonic waves are passed through the water which helps in the PR. Thus giving a gate electrode with clear edges as shown in Figure 4.5. The whole fabrication process is explained in brief in Table 1.

4.5: Electrical Characterization

Thin film characterization and electrical characteristics measurement technique are discussed in this section. The thickness of the films sputtered are measured using the Veeco Dektak 150 profilometer; C-V measurements for MOS capacitors are done using the HP 4208 1MHz C-V plotter; Capacitance measurement using HP 4275A Multi Frequency LCR meter and Agilent U1701B Handheld Capacitance Meter; finally I-V characterization, V_T, measurement are done using the probe station and Tektronic curve tracer.

4.5.1: Dielectric constant measurement

The HP 4275A Multi-Frequency LCR meter is used to measure the capacitance of the MIM structures as shown in Figure 4.8. This instrument was connected to the probing station and software interfaced to the computer. The frequency of operation of this measurement is 1 MHz

as the capacitance measured was in the range of couple of nano farads which is a small value of capacitance. The samples are kept in the same probing station and connected to the probes which in turn are connected to the LCR meter. Calibration is done before the measurement of capacitance for each device.

Figure 4.6 Dielectric constant measurement (Courtesy: Agilent Technologies) [20]

Agilent U1701B Handheld Capacitance Meter is also used to determine the capacitance of the MIM structure as shown in Figure 4.9. This instrument has two probes which can be connected to the metal lines on the MIM structure and the reading of capacitance can be read from the display. Initially to calibrate the device, the probes are connected to each and the button "Range AUTO" is pressed. After calibration the probes are connected to the metal lines on MIM structures and the measurements are read. This method is used to cross check the capacitance value with the LCR meter.

By knowing the capacitance, the film thickness and the line width of the aluminum electrode, the dielectric constant is found. The results are given in the Table 3 and 4.

Figure 4.7 Agilent U1701B Handheld Capacitance Meter

4.5.2: Thickness measurement

The thickness was measured using Veeco Dektak 150 profilometer as shown in Figure 4.10. It is a surface profilometer that takes surface measurements using contact profilometry techniques. The Dektak 150 uses stylus profilometry technology, which is the accepted standard for surface topography measurements, roughness and step size. Here its property of two-dimensional surface profile measurements is used to measure the step height. The step is created by masking a small portion on a test sample during the sputtering process using a thin strip of aluminum foil as it can withstand the high temperature and its property of less diffusivity into the oxide layer during the

sputtering process. The scan length range used for measurement is 65mm and the stylus force was 15mg for a scan time of 30 second. The software profiling is done after the mechanical profiling if the profile obtained is off level. Then the Average step height is found out by placing the two cursors on either sides of the step obtained in the profile.

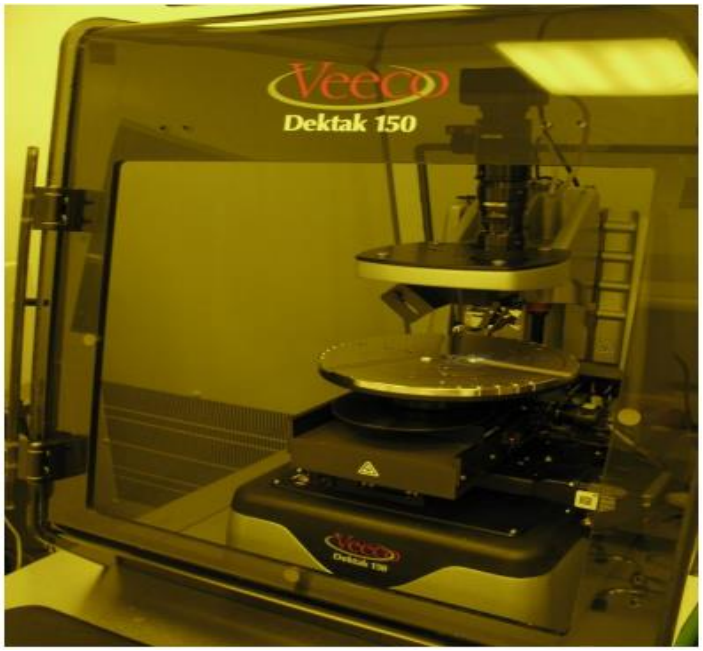


Figure 4.8 Veeco Dektak 150 profilometer (Courtesy: Veeco)

4.5.3: C-V characteristics measurement for MOS capacitor

Capacitance-Voltage measurement (C-V characteristics) was conducted with help of HP 4208 1MHz C-V plotter as shown in figure 4.9. This instrument is connected to a probing station. The samples were kept inside the probing station with two micro tip probes connected to the parameter analyzer. This parameter analyzer is interfaced to the computer. Hence all the measurements are performed through software interfaced computer. C-V characterization is done by taking the voltage sweep from -15V to 15V and subsequently logging the points on the

computer. These points are then plotted in MS Excel thus giving C-V characterization plot.

Figure 4.9 HP 4208 1MHz C-V plotter

4.5.4: MOSFET characteristics measurement

The MOSFET characteristics are explained in Chapter 2. The I_D versus V_{DS} plot gives the MOSFET characteristics. The gate, source and drain are connected to the appropriate terminal of Tektronix curve tracer type 577 as shown in figure 4.10. The gate bias is stepped up as required by specifying the steps on the step generator knob. The curves are plotted on the plotter screen and an image is taken. The graph from this image is extracted using a data extractor like OriginPro 9.1. The curve tracer is used to plot I_D versus V_{DS} and I_D versus V_{GS} curves.

To calculate the V_T from the graph, the gate and drain were tied together whereas the source was grounded. The curve plotted by the Tektronix curve tracer is I_D versus V_{GS} curve. The x-intercept of the tangent to the curve gave the threshold voltage of that particular device.

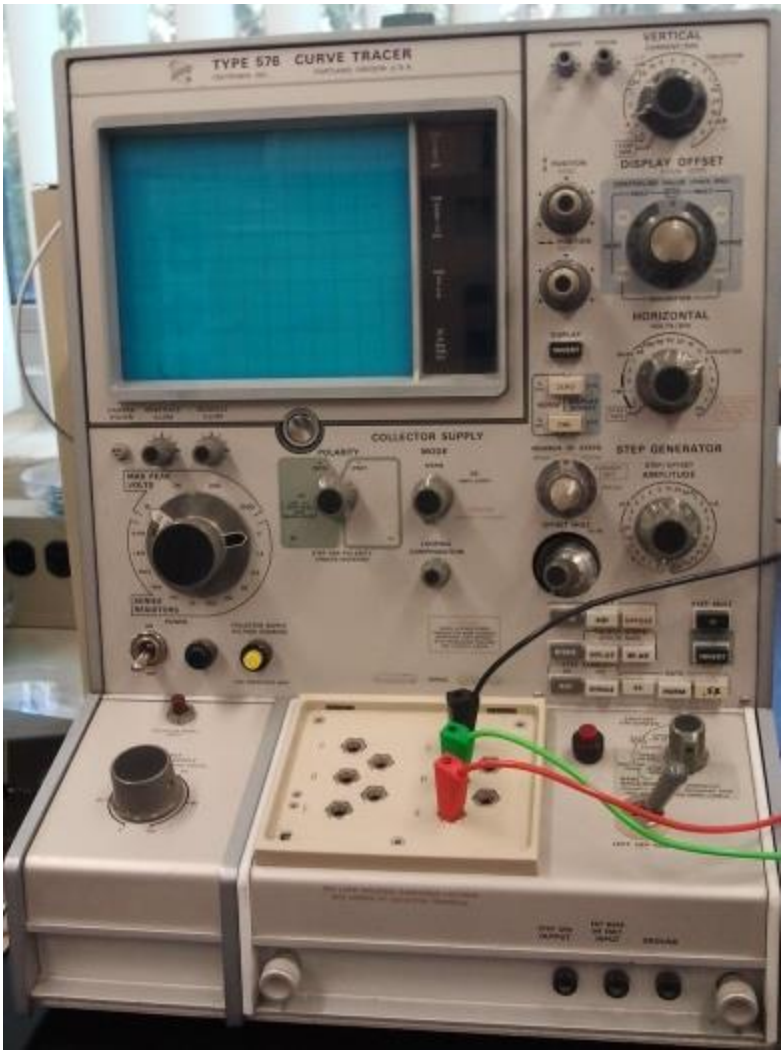


Figure 4.10 Tektronix curve tracer type 577

CHAPTER 5: RESULTS AND DISCUSSION

5.1: Electrical Studies

In this section various electrical properties like dielectric constant, V_T, Resistance are measured. The results of all the above mentioned devices are discussed.

5.2: Nickel plating devices

Electroless nickel plating was performed on Germanium wafers. Following table shows different types of samples that were fabricated. As the nickel plating was for a short period of time (because for longer period the metal started peeling out), the metal layer formed was very thin. Three samples with different annealing temperatures for nickel were used. Due to thin layer and high temperature, nickel got evaporated for Sample II and Sample III.

Table 5.1 Nickel plating results

	Sample I	**Sample II**	**Sample III**
Al –annealing temp	440	440	440
Ni – Annealing temp	450	500	550
Top	Ni	Ni	Ni
Bottom	Al	Al	Al
Bulk resistance	1012 ohm	1600 ohm	1033 ohm
After Al Annealing	15.9 ohm	23.5 ohm	5.25 ohm
After Ni plating	15.25 ohm	1.2 ohm	1.5 ohm
After Ni annealing	1.02 ohm	Ni Evaporated	Ni Evaporated

5.3: MIM device measurement

The capacitance was measured on eighteen different MIM devices formed on a single glass substrate. The dielectric constant can be determined using following equation,

$$C = \frac{\varepsilon_o * k * A}{d}$$

Where, C is the capacitance obtained from capacitance measurement instrument, A is the area which is 3mm square, d is the thickness of the oxide measured by Veeco. The dielectric constants found are displayed in the Table 3 and 4.

5.3.1: HfO_2 dielectric constant measurement

Using specific conditions for sputtering from different paper given in the reference list the following samples were fabricated. As shown in the results the first conditions gave a dielectric constant close to the theoretical value that is 22-25. This sputtering condition is further used in the MOS capacitor fabrication.

5.3.2: TiO_2 dielectric constant measurement

Using specific conditions for sputtering from different paper given in the reference list the following samples were fabricated. As shown in the results none of the conditions gave a dielectric constant close to the theoretical value. Hence no further samples for TiO_2 were fabricated.

As seen from the tables, the values are different than required. There can be many reasons for such outcomes. First one being, the sputtering system used in this research is different as compared to the ones used in the cited papers. Second being, contamination in the sample from the time the sample was fabricated till it goes for testing. Oxides are prone to absorption of water vapor.

Table 5.2 HfO_2 MIM device capacitance measurement

Type of reactive sputtering	**Sputtering temp**	**O_2 /Ar ratio**	**Power supply**	**Sputtering pressure (mTorr)**	**Thickness (Å)**	**Dielectric constant**
RF	RT	1:4	150W	2	1191	29.9
RF	RT	4:1	200W	12	352	135.23
RF	RT	5:20	150W	5	468	70.5
RF	RT	5:20	250W	2	1984	261.5
RF	RT	5:20	150W	2	1074	142.9
RF	RT	25:3	100W	2	410	55.07
RF	RT	18:3.6	200W	4	547	97.9

Table 5.3 TiO_2 MIM device capacitance measurement

Type of reactive sputtering	**Sputtering temperature**	**O_2 /Ar ratio**	**Power supply**	**Sputtering pressure (mTorr)**	**Thickness**	**Dielectric constant**
RF	RT	20:0	150W	50	34.9	0.49
RF	RT	2:18	120W	10	377.2	2.5
RF	RT	20:0	150W	30	206	17.17
RF	300	8:12	200W	4	655	25.01
RF	RT	24:6	75W	4	238	2.5
DC	RT	4:16	220W	1	442	12.27
RF	RT	10:10	288W	10	167	3.5

5.4: MOS capacitor measurement

C-V characterization is performed on the MOS capacitors. The conditions from Ref [23] are slightly changed to examine for better MOS capacitor behavior. The O_2/Ar ratio varies from 1:4, 6.7:13.3 to 10:10 at two different temperatures i.e. room temperature (RT) and 300°C. These conditions were performed on both NMOS and PMOS. These samples were further divided into two different types – annealed at 450°C for 20 min each with 10cc flow rate of Argon and other without annealing. These conditions are explained in simplified manner in the following Table 5.

Table 5.4 MOS capacitor result table

Ratio of O2/Ar at temperature	NMOS		PMOS	
	Without Annealing	Annealing	Without Annealing	Annealing
1:4 @ RT	Figure 5.6	Figure 5.7	Figure 5.8	No results
1:4 @ 300°C	Figure 5.9	Did not perform	Figure 5.10	Did not perform
6.5:13.5 @ RT	Figure 5.11	Figure 5.12	Figure 5.13	Figure 5.14
6.5:13.5@ 300°C	No results	Did not perform	No results	Did not perform
10:10 @ RT	No results	No results	Figure 5.15	Figure 5.16
10:10 @ 300°C	Figure 5.17	Did not perform	No results	Did not perform

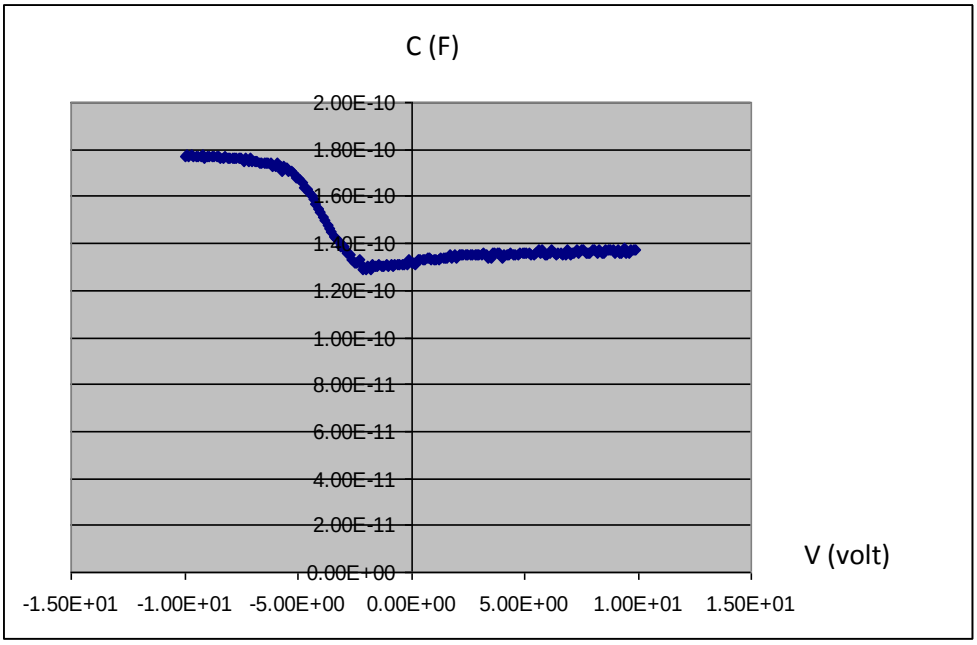


Figure 5.1 HfO_2 ($Ar:O_2$ = 4:16) @ RT without Annealing (NMOS)

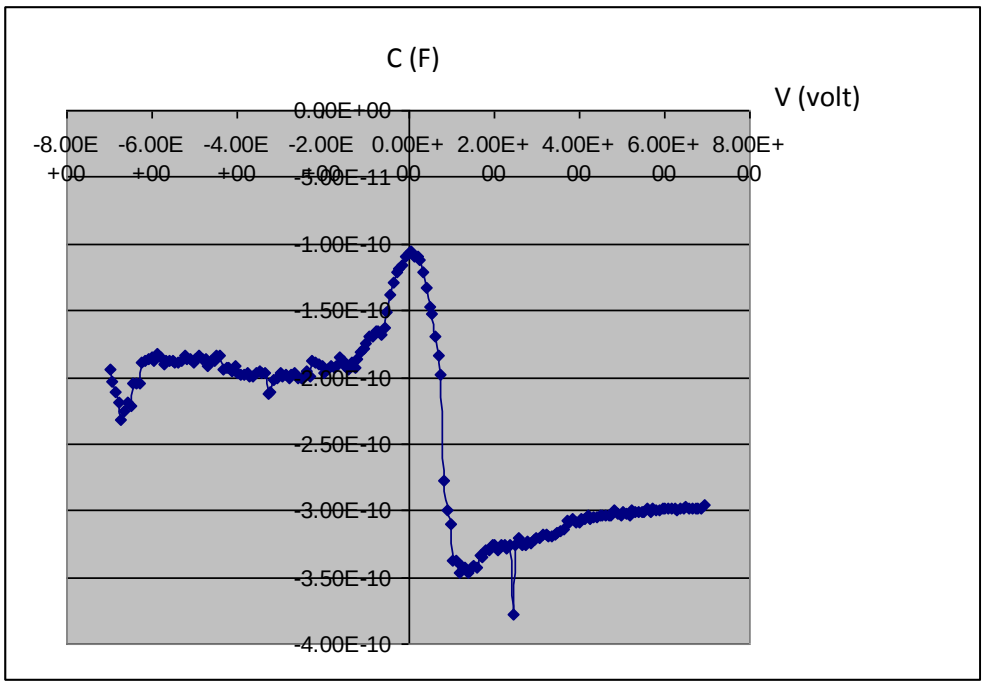


Figure 5.2 HfO_2 ($Ar:O_2$ = 4:16) @ RT with Annealing (NMOS)

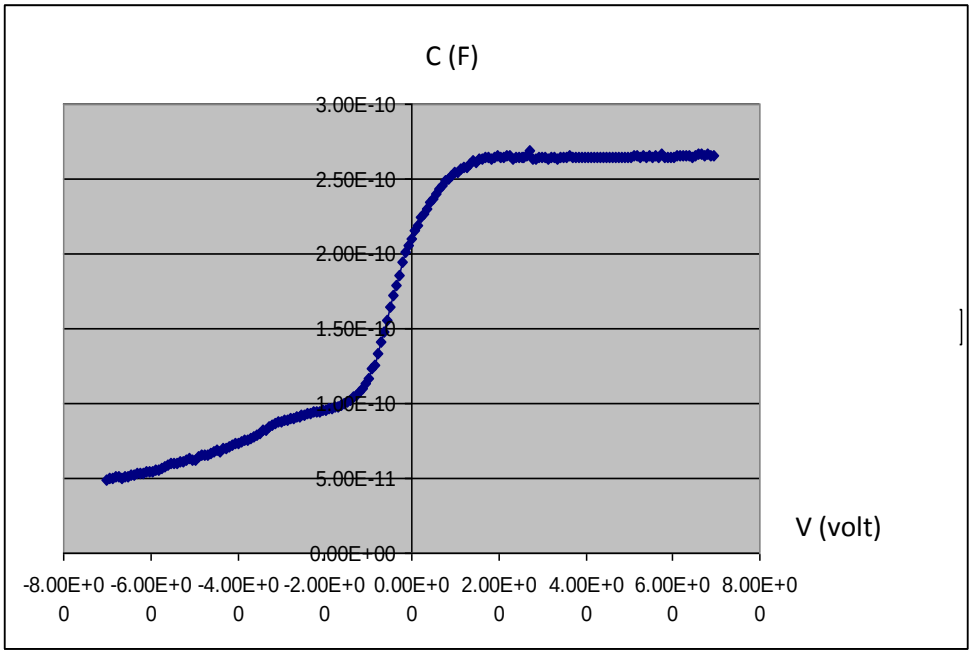


Figure 5.3 HfO_2 ($Ar:O_2$ = 4:16) @ RT without Annealing (PMOS)

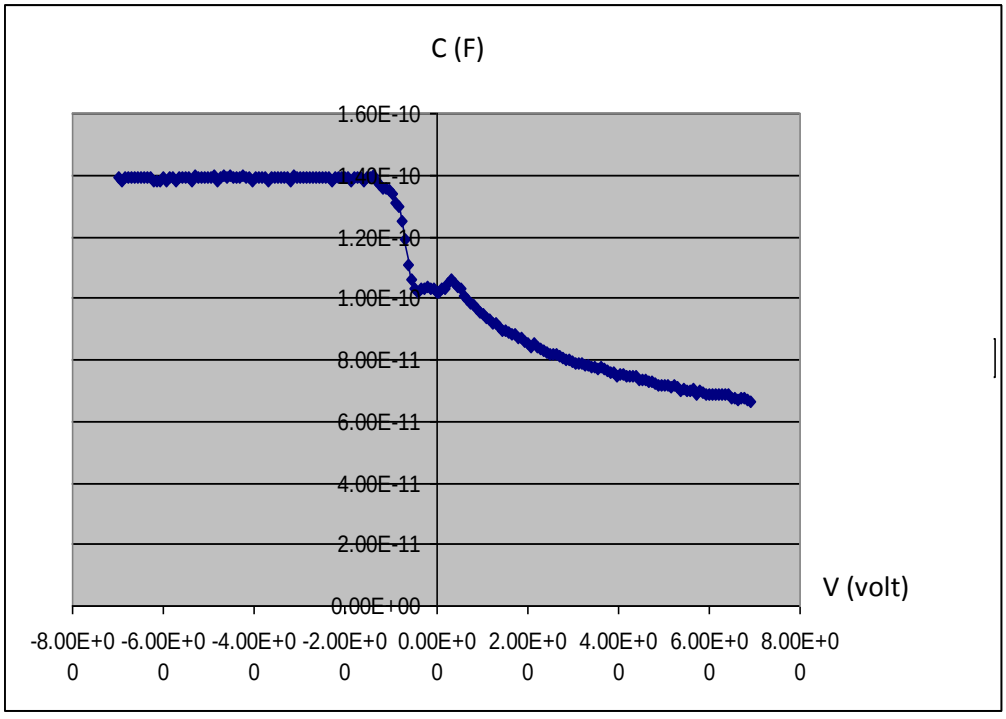


Figure 5.4 HfO_2 ($Ar:O_2$ = 4:16) @ 300°C without Annealing (NMOS)

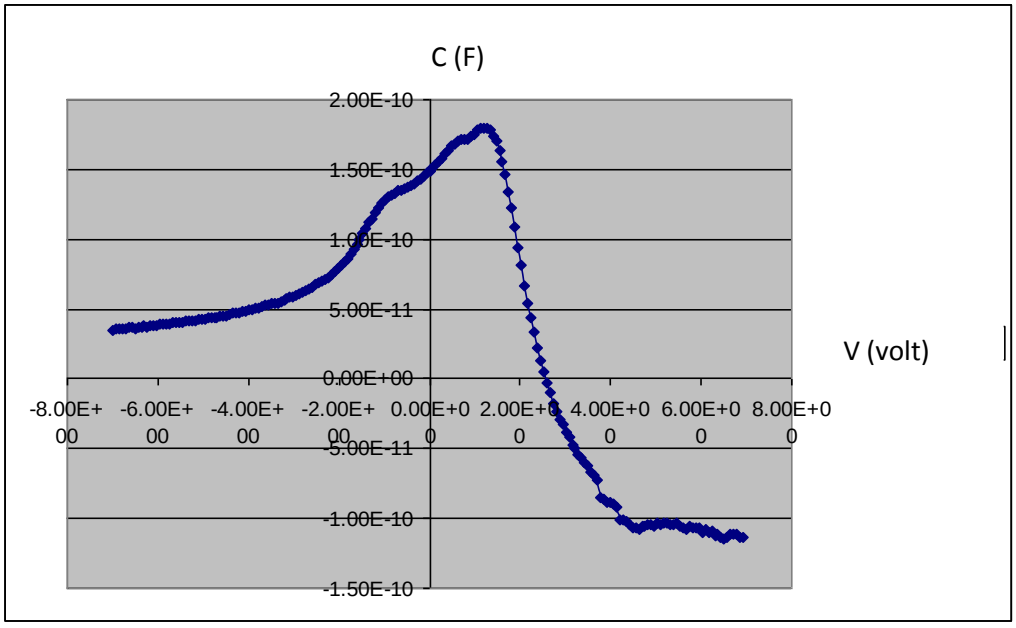


Figure 5.5 HfO_2 ($Ar:O_2$ = 4:16) @ 300°C without Annealing (PMOS)

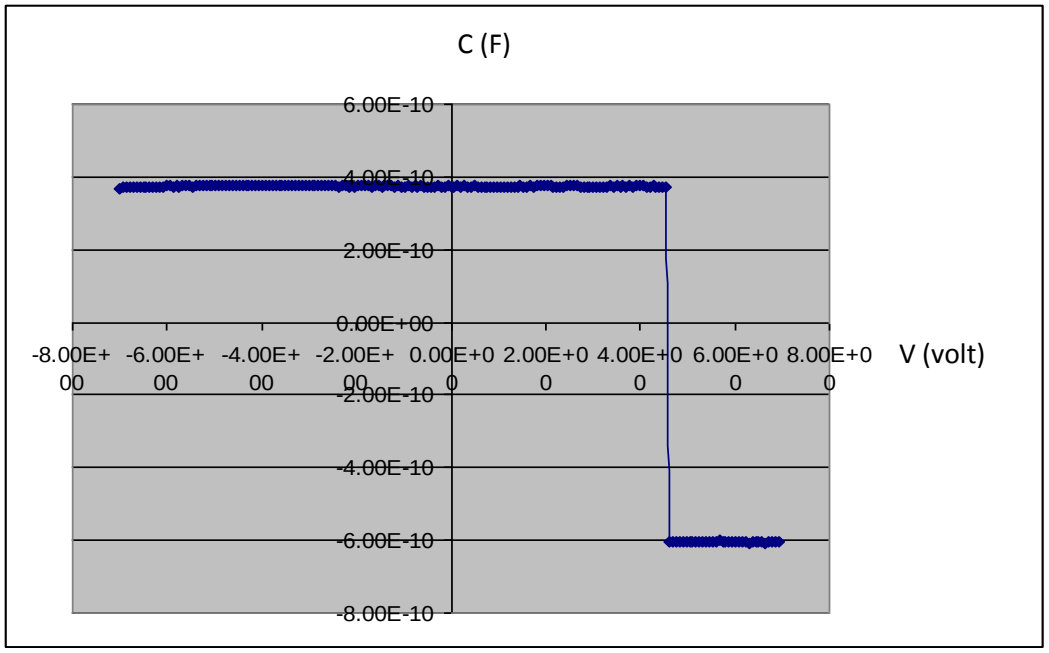


Figure 5.6 HfO_2 ($Ar:O_2$ = 6.7:13.3) @ RT without Annealing (NMOS)

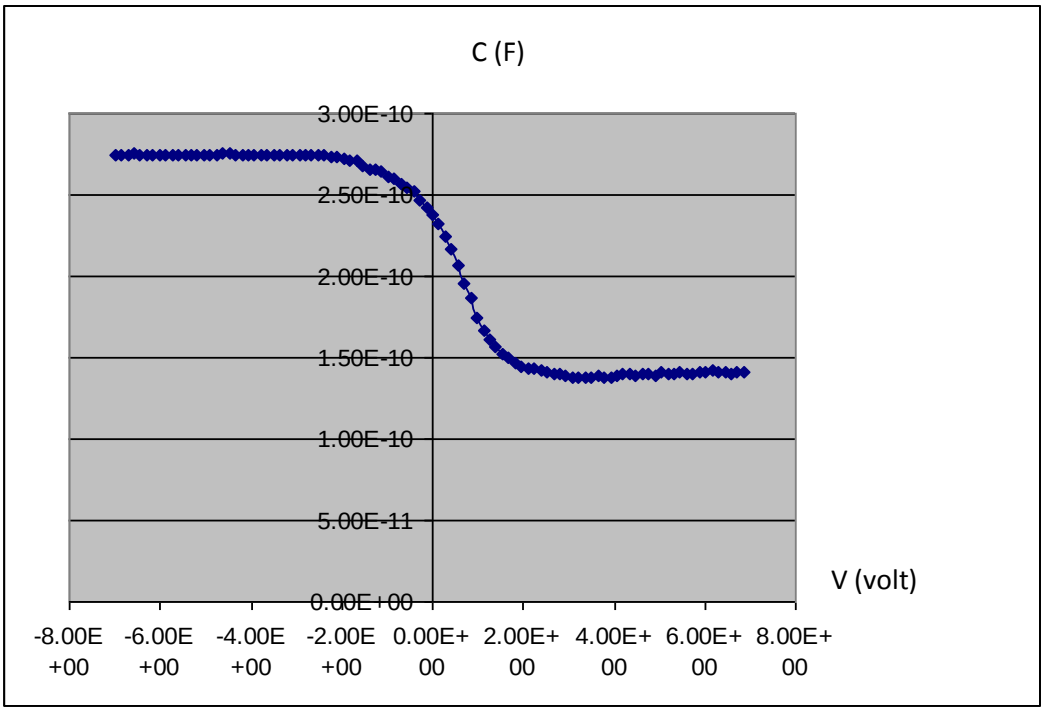


Figure 5.7 HfO_2 ($Ar:O_2$ = 6.7:13.3) @ RT with Annealing (NMOS)

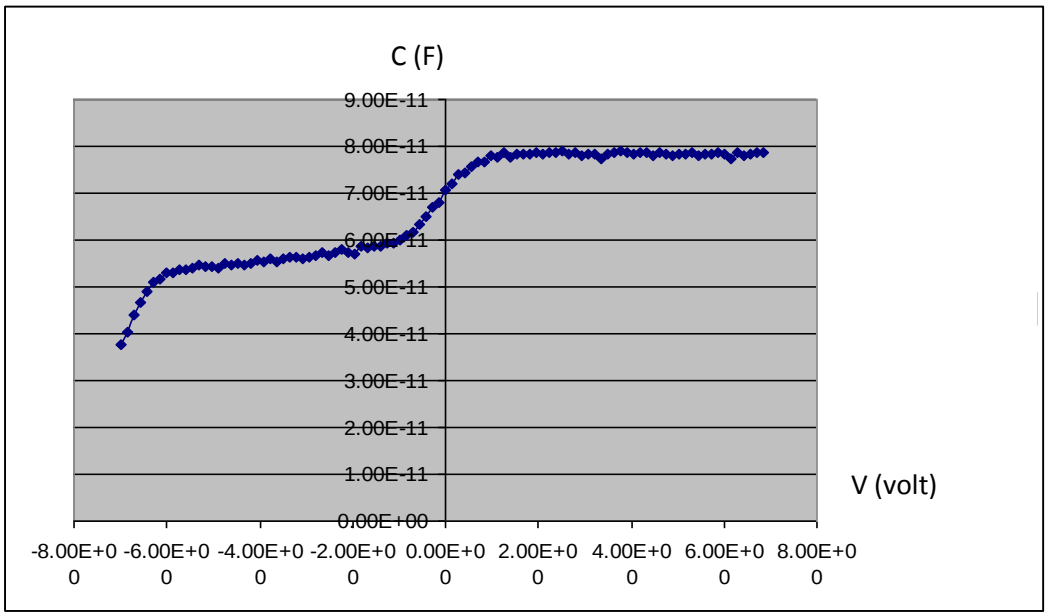


Figure 5.8 HfO_2 ($Ar:O_2$ = 6.7:13.3) @ RT without Annealing (PMOS)

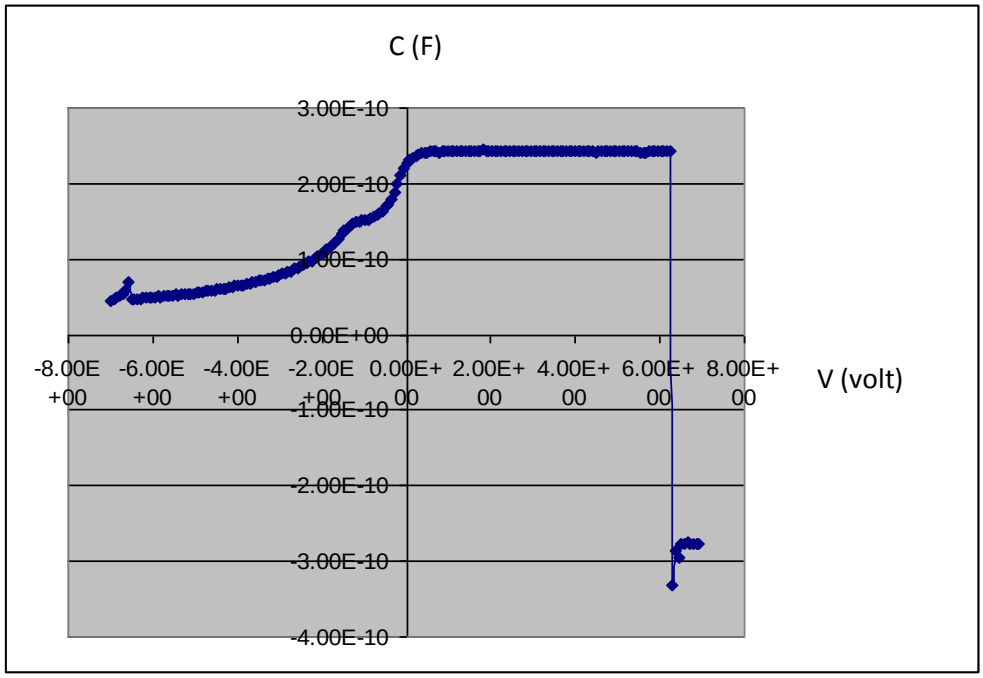


Figure 5.9 HfO_2 ($Ar:O_2$ = 6.7:13.3) @ RT with Annealing (PMOS)

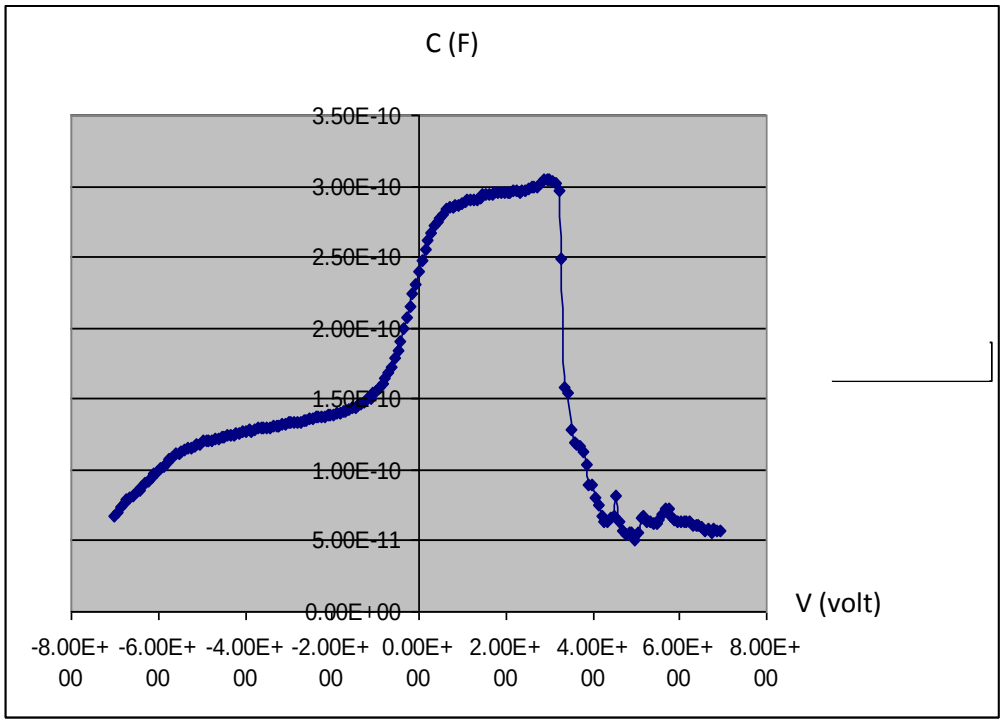


Figure 5.10 HfO_2 ($Ar:O_2$ = 10:10) @ RT without Annealing (PMOS)

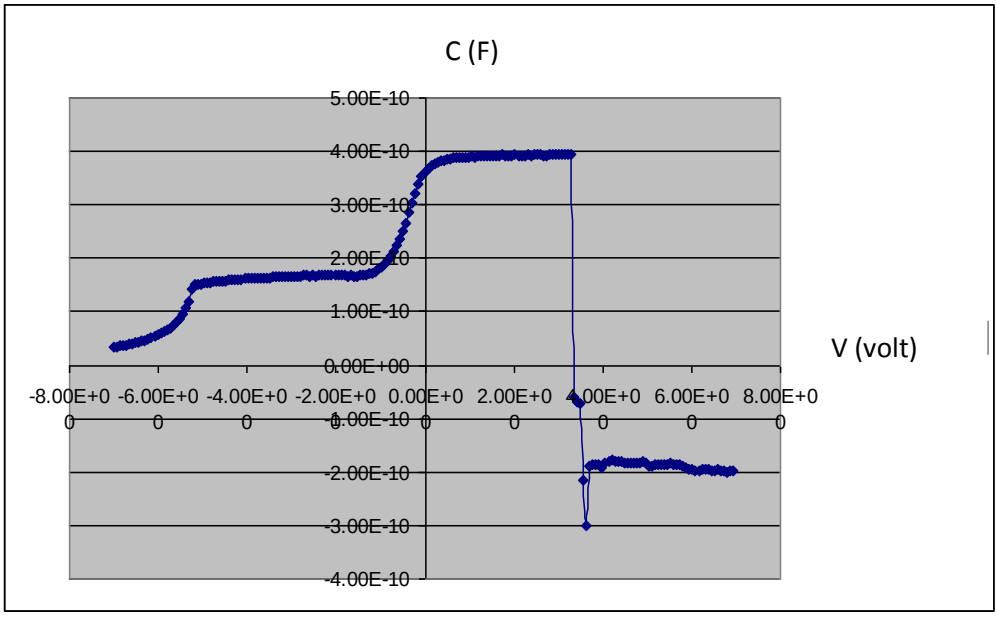


Figure 5.11 HfO_2 ($Ar:O_2$ = 10:10) @ RT with Annealing (PMOS)

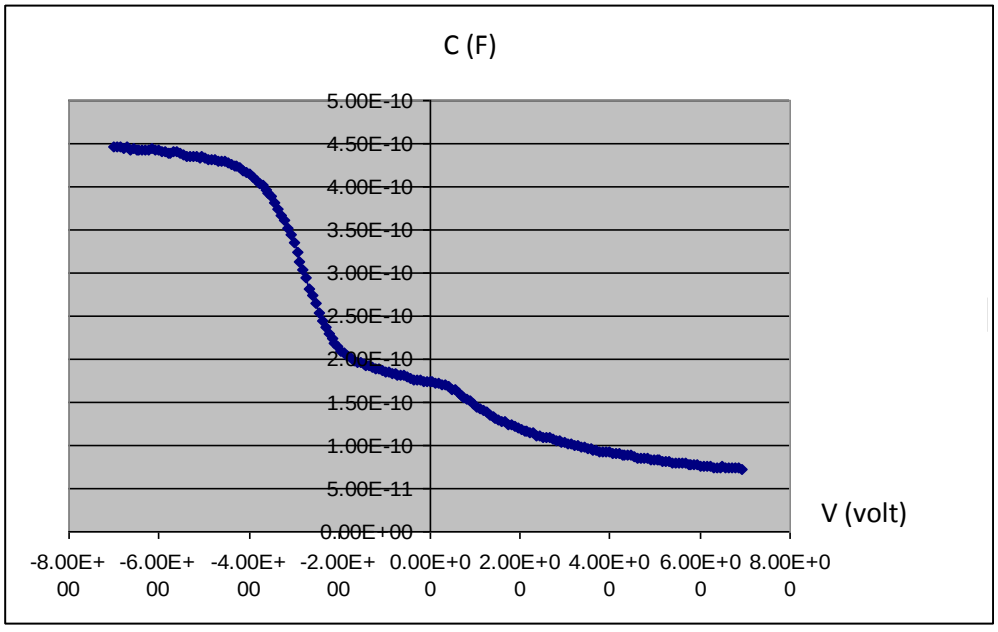


Figure 5.12 HfO_2 ($Ar:O_2$ = 10:10) @ 300°C without Annealing (NMOS)

The annealed samples showed smooth C-V characteristics, which may be due to the dielectric traps being annealed out. Annealing helped in reducing any defects formed during the sputtering of HfO_2.

5.5: MOSFET Measurement

In this section, the calculation for fabricated devices includes oxide thickness and V_T. Given below are the theoretical calculations followed by experimental results.

5.5.1: Theoretical Calculation

Si type	: p
Resistivity, ρ	: 8.1 Ω-cm
N_A for ρ = 8.1 Ω-cm	: 1.7 x 10^{15} atoms/cm^3 (Jaeger)
$ø_{ms}$ Al – p-Si	: -0.711 V

5.5.1.1: Built-in Voltage

$$ø_f = \frac{kT}{q} \ln \frac{N_A}{n_i}$$

$$= 0.0259 \ln \frac{1.7 * 10^{15}}{1.5 * 10^{10}}$$

$$= 0.3014\ V$$

5.5.1.2: Depletion Width

$$W = 2\sqrt{\frac{\varepsilon_{si}\emptyset_f}{qN_A}}$$

$$= 2\sqrt{\frac{11.8 * 8.85 * 10^{-14} * 0.3014}{1.6 * 10^{-19} * 1.7 * 10^{15}}}$$

$$= 0.8345\mu m$$

5.5.1.3: Charge/ unit area in the depletion region

$$Q_d = -qN_A W = -1.507 * 10^{-8}\frac{C}{cm^2}$$

5.5.1.4: Dielectric capacitance

$$C_i = \frac{\varepsilon_i}{d} = \frac{29 * 8.85 * 10^{-14}}{584 * 10^{-8}} = 4.39 * 10^{-7}\frac{F}{cm^2}$$

5.5.1.5: Threshold Voltage

$$V_T = \emptyset_{ms} + 2\emptyset_f - \frac{1}{C_i}(Q_i + Q_d)$$

$$= -0.711 + 2 * 0.3014 - \left(\frac{10^{12} * 1.6 * 10^{-19} - 1.507 * 10^{-8}}{4.39 * 10^{-7}}\right)$$

$$= -0.316\ volts$$

If Q_i goes below 10^{12} charges/cm^2, then we can see improvement in threshold voltage towards the positive voltage. As seen from graph and calculation, the results are different there could be several reasons for this kind of behavior.

- The dielectric constant can change depending on the formation of interfacial silicide or SiO_2 layer between the Si and Hf thus reducing the dielectric capacitance.
- Due to minor misalignment during the fabrication process, the gate electrode overlapping the diffused region is slightly offset and hence the drain current shown slightly different characteristics.

During the etching of HfO_2, clear edges were not obtained. The etching solution encroached PR covered areas, due to anisotropic etching behavior of BOE for HfO_2 further samples were not prepared. With the new mask and hafnium oxide as gate dielectric following graphs are obtained which present almost similar MOSFET characteristics as compare to devices with SiO_2 gate dielectric. Also as seen in Figure 5.19 and 5.20, I-V characteristics for MOSFET

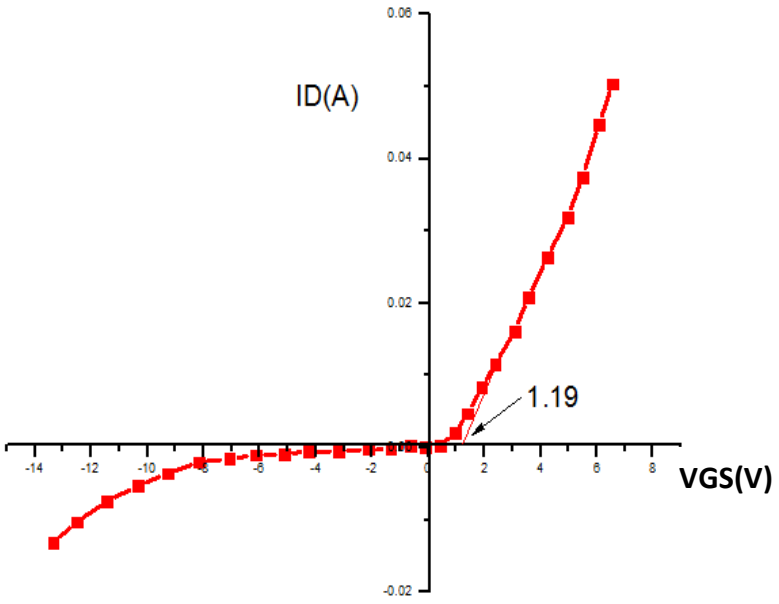


Figure 5.13 MOSFET ID versus VGS characteristics

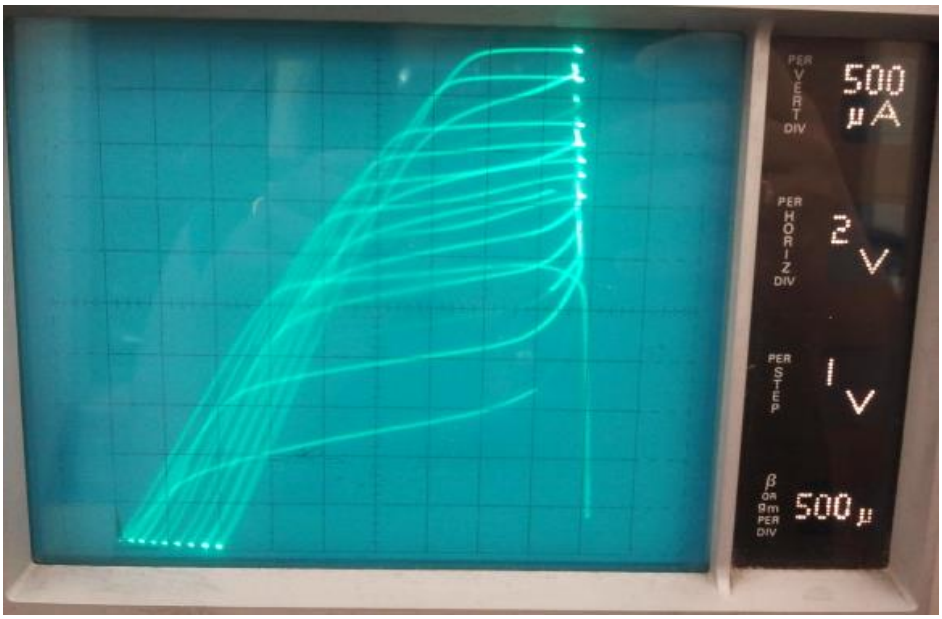


Figure 5.14 MOSFET I_D versus V_{DS} characteristic four level mask

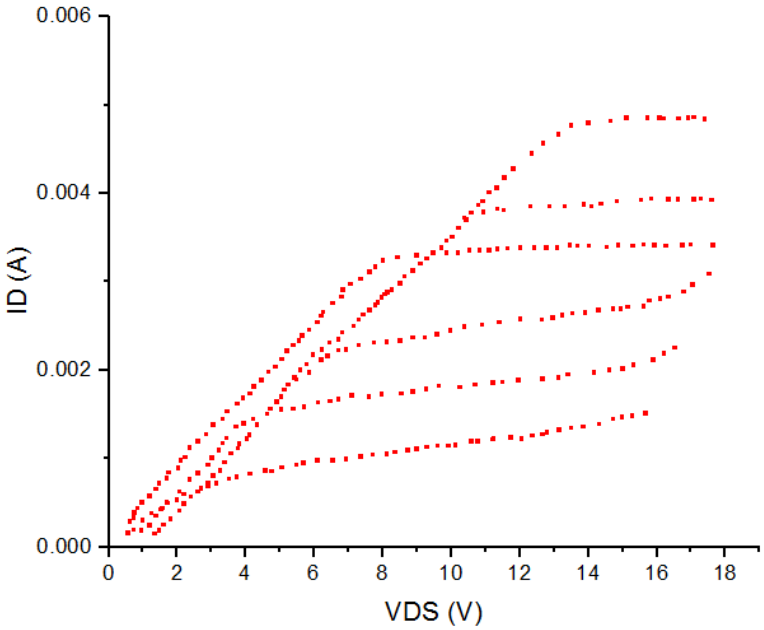


Figure 5.15 MOSFET I_D versus V_{DS} characteristic four level mask (Extracted data from image using Origin Pro)

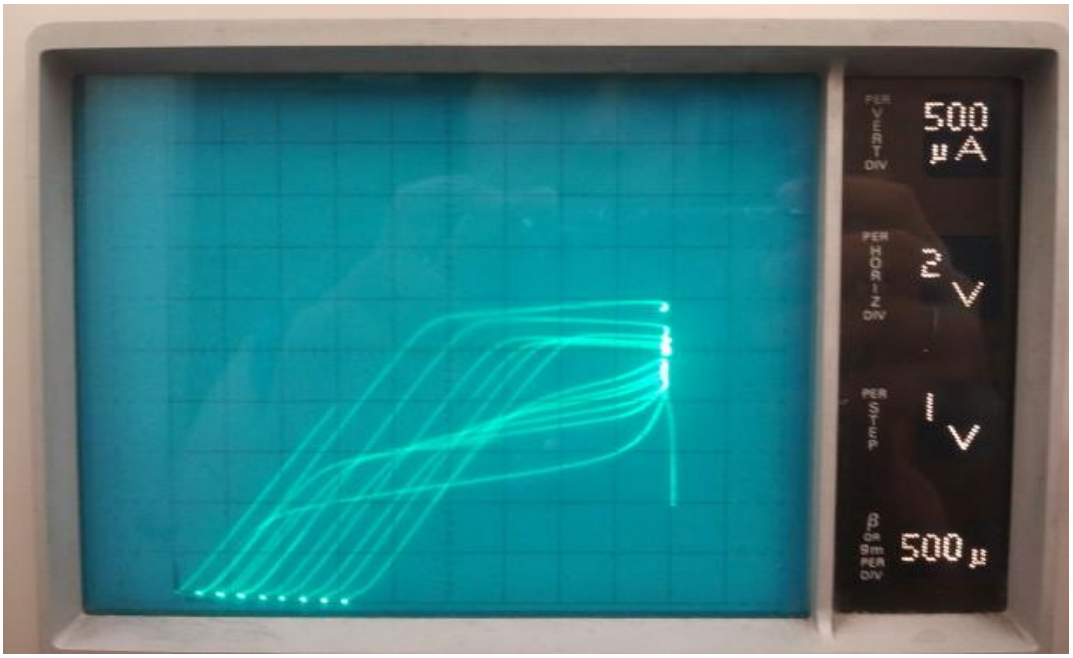


Figure 5.16 MOSFET I_D versus V_{DS} characteristic three level mask

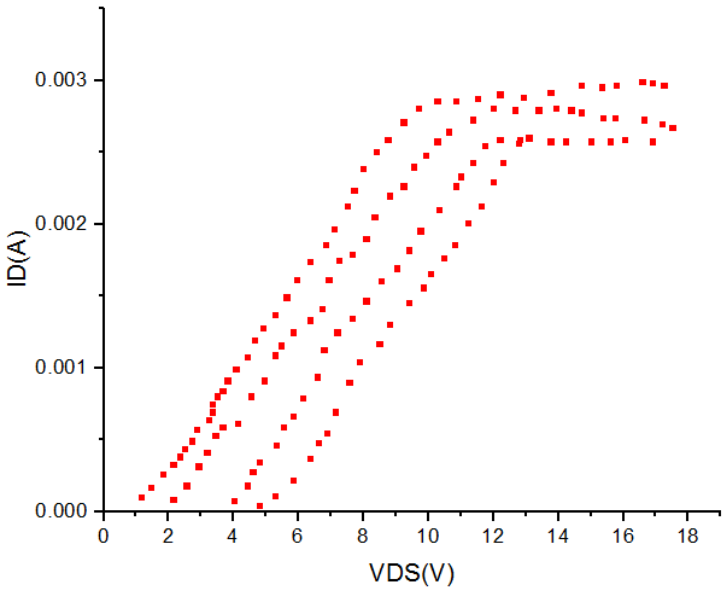


Figure 5.17 MOSFET I_D versus V_{DS} characteristic three level mask (Extracted data from image using Origin Pro)

CHAPTER 6: CONCLUSION

The main focus of this work was study of characteristics of high-k dielectric materials like hafnium dioxide and titanium dioxide. Initially MIM devices were fabricated to obtain the required dielectric constant for the given oxide. Oxide layer dielectric constant varies with the kind of technique used and the kind of parameters used in a given technique. In short dielectric constant of these oxide layers are technique oriented and process oriented. In my work, reactive sputtering was the technique used for formation of oxide layers. These oxide films were sputtered by changing the parameters like sputtering temperature, Ar/O_2 gas ratio, Power supply supplied to the substrate, etc. that are used during reactive sputtering technique. The defined parameters are shown in Table 3 and 4. As seen from the results for MIM devices, hafnium oxide dielectric contact ranges between 30 to 100 and titanium oxide dielectric constant ranges between 10 to 30. From the inferred results, one of the results [23] for hafnium oxide is close to the required range i.e 22-25. The sputtering technique mentioned in Ref [23] was further used in fabrication of MOS capacitor and MOSFET device.

During fabrication of MOS capacitor to obtain better results the Ar/O_2 ratio and substrate temperature were changed. As seen from the results, Ar/O_2 ratio 4:1 sample showed better result compared to any other samples. Finally this process was used to fabricate MOSFET device. The MOSFET design that was used in my work has four level masks. The fourth level mask is used when the gate metal contact is different than the drain and source metal contact. This mask was built for future work but in my work it was tested for MOSFET with HfO_2 as the gate dielectric. The new mask should similar characteristics as that of three level mask fabricated MOSFET device. The V_T that was obtained from graph and theoretical calculation should different results.

The reasons for this behavior could be formation of SiO_2 or silicide layer between Si and Hf. Also Q_i for the fabricated sample cannot be exactly estimated for theoretical calculation, so a value depending of the clean room condition is been considered.

The graphs I_D versus V_{DS} characteristics for both four and three level masks with HfO_2 as the gate dielectric are similar. Concluding that the four level masks is same as three level masks. Minor misalignment during the fabrication process i.e. overlapping of the gate electrode with the diffused region caused drain current in the I-V characteristics behave slightly differently.

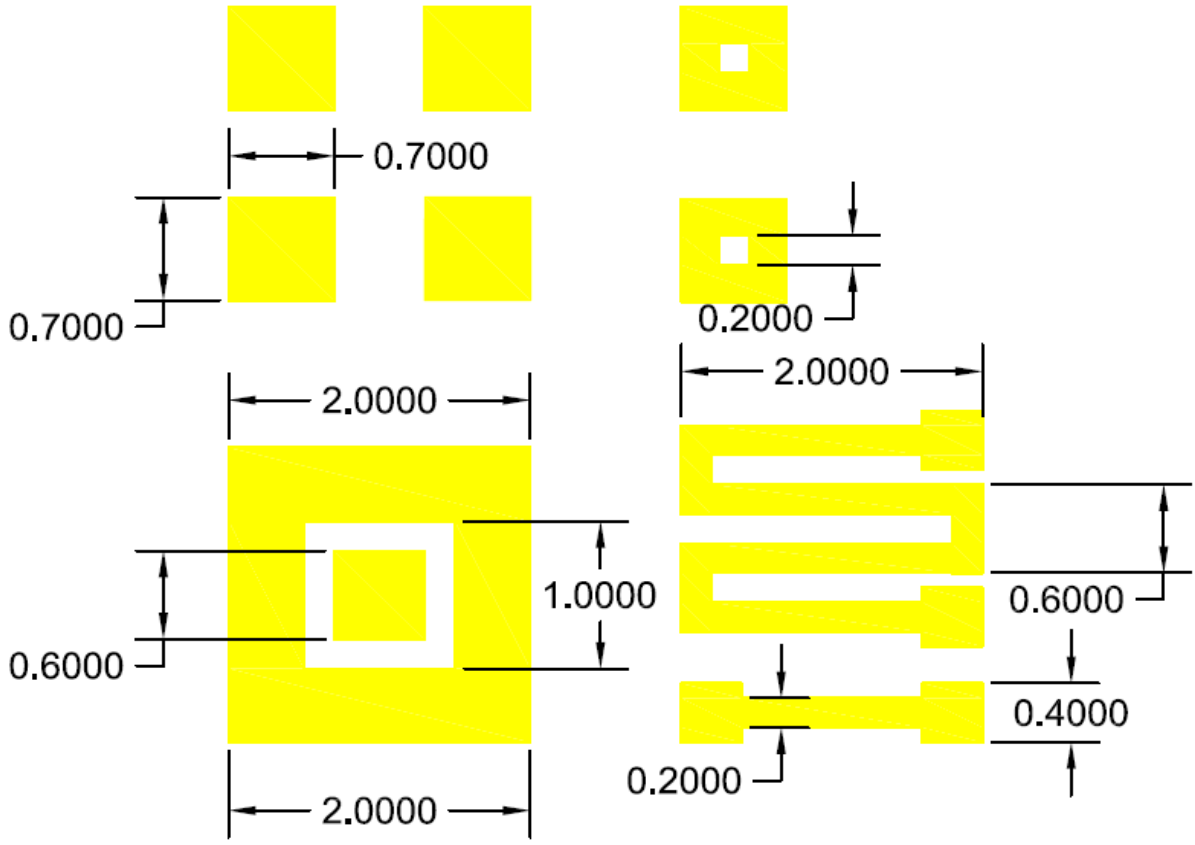
FUTURE WORK

The four level masks can be used to create sensors. The metal contacts of source-drain and gate can be separately placed. So the fourth layer mask can be used to deposit any metal other than Al. Metals like Al_2O_3, Si_3N_5 and Ta_2O_5 can be used to fabricate pH sensors [26].

Deposition of ZnO on the gate can be used to fabricate glucose sensor [30]. Glucose oxidase (GOD) is immobilized on ZnO layer and when it comes in contact with glucose in a solution, the electrochemical response from GOD induces a voltage change at the gate. The change in gate voltage leads to change in drain current thus helping to sense glucose in a solution. ZnO shows water and UV ray absorption property, so ZnO as gate electrode can also be used to fabricate humidity and UV sensors respectively.

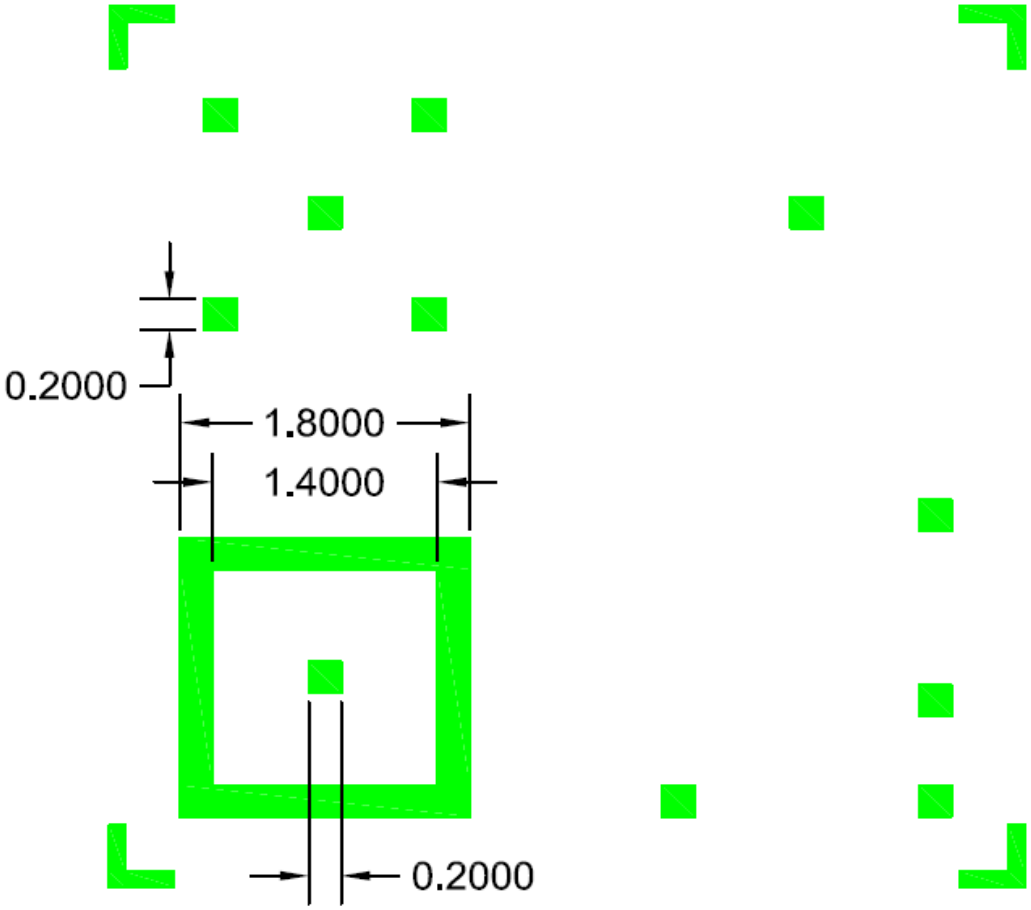
APPENDIX
MASK IMAGES

Mask #1



ALL DIMENSIONS ARE IN MILLIMETER (mm)

Mask #2



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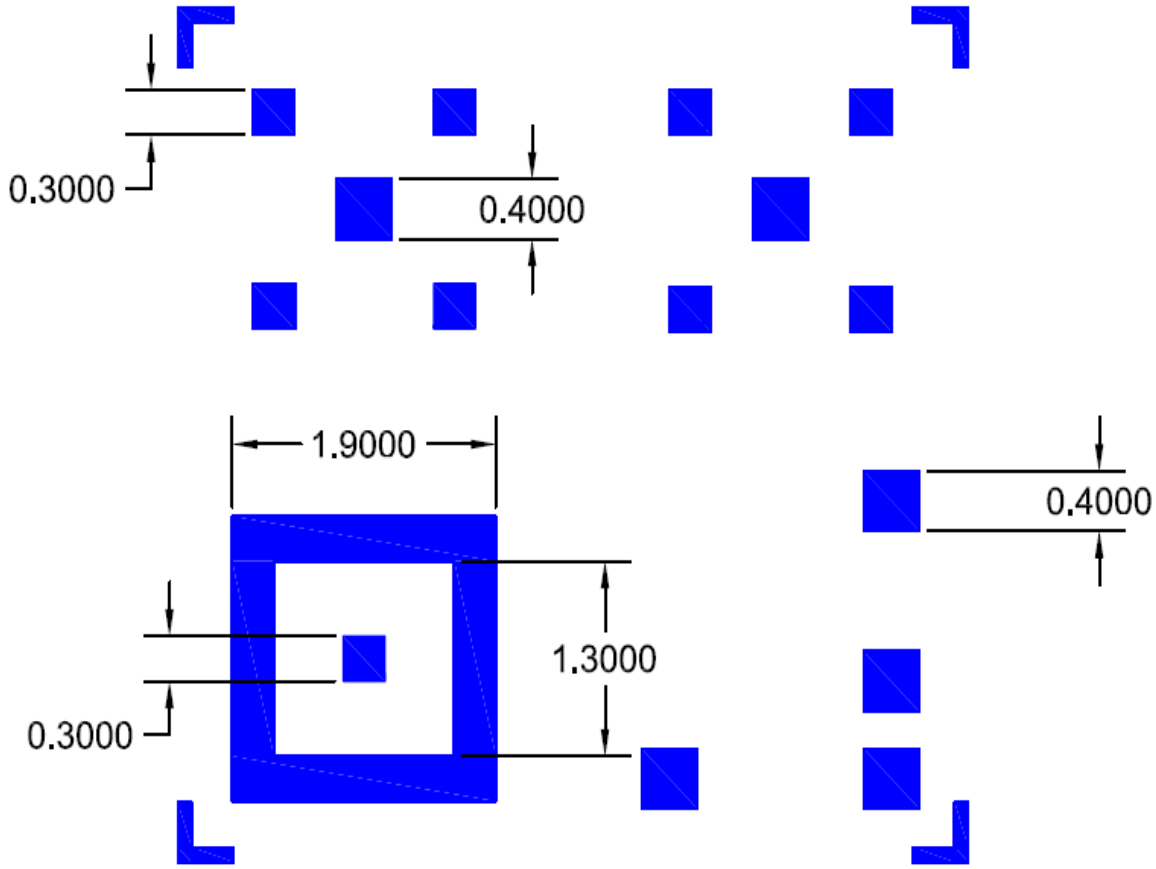

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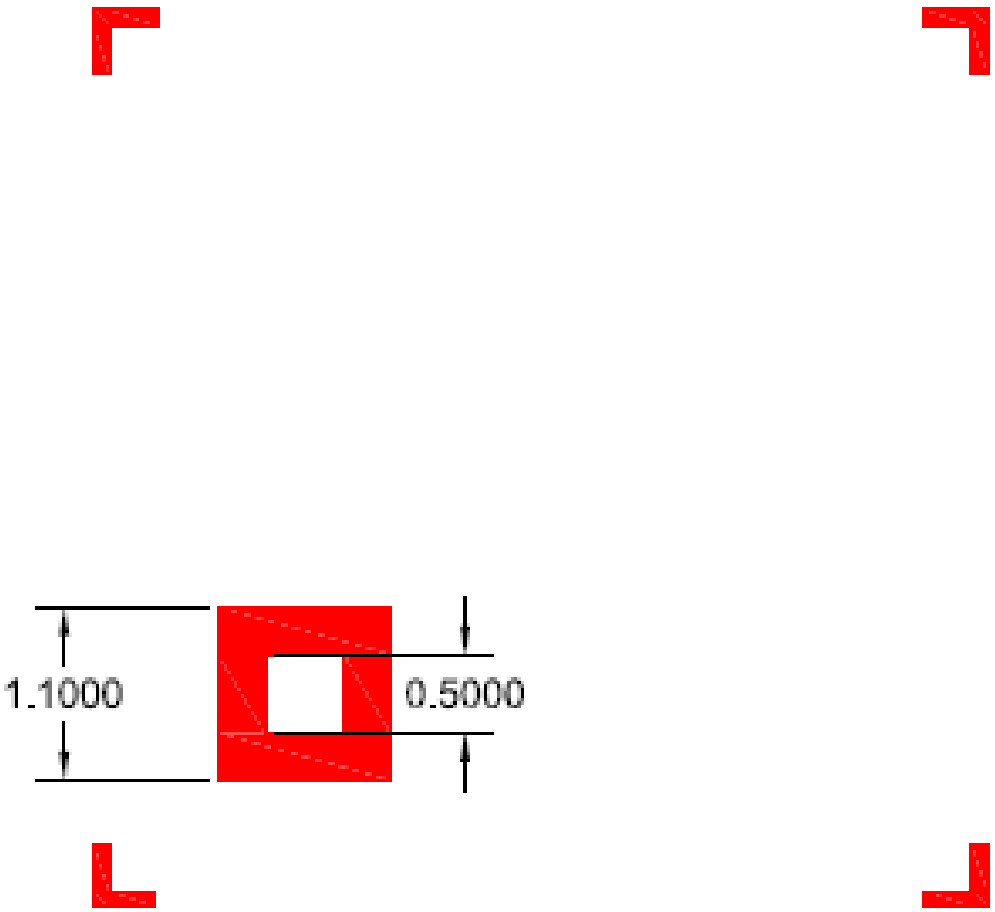
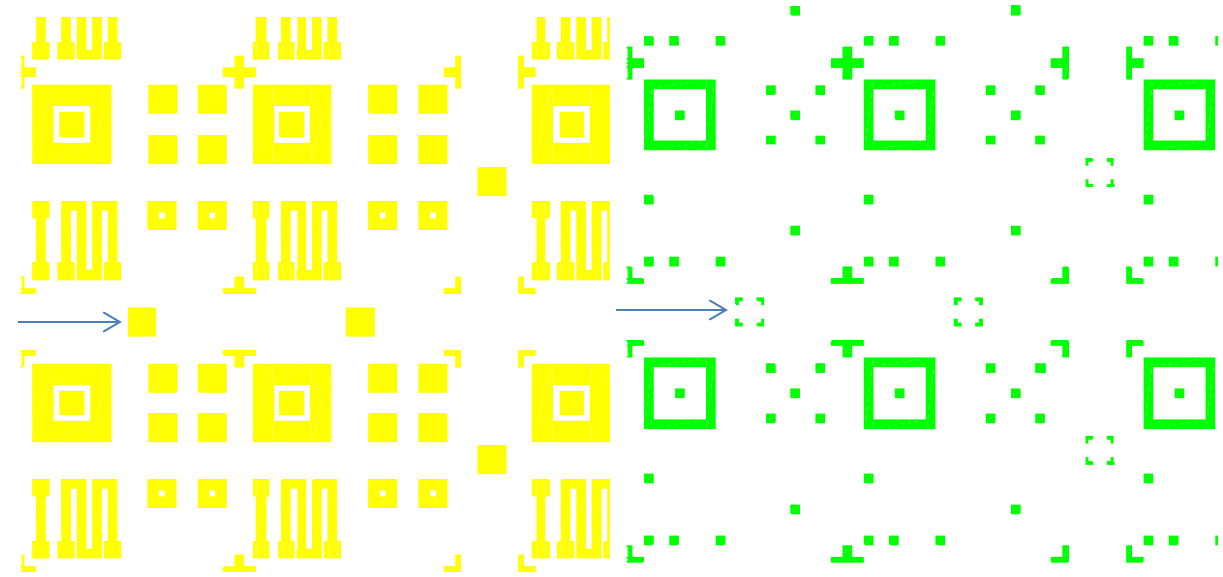
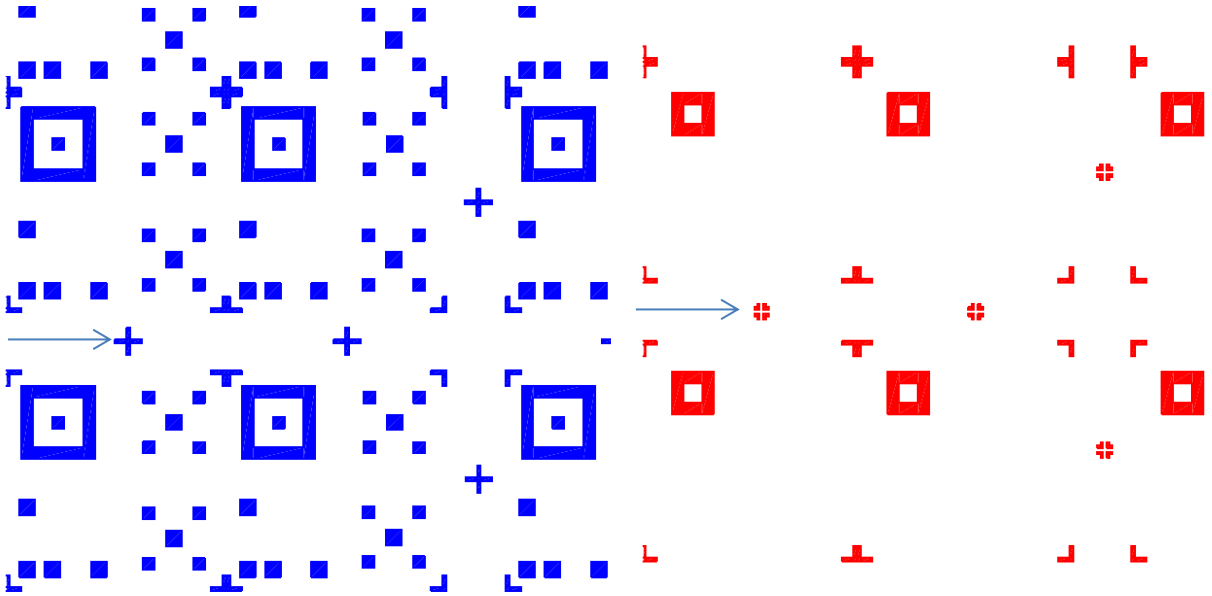
Mask #4



ALL DIMENSIONS ARE IN MILLIMETER (mm)

Arrowed objects are marker used for alignment





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