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Design And Characterization Of Noveldevices For New Generation Of Electrostaticdischarge (esd) Protection Structures

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DESIGN AND CHARACTERIZATION OF NOVEL DEVICES FOR NEW GENERATION OF ELECTROSTATIC DISCHARGE (ESD) PROTECTION STRUCTURES

by

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ABSTRACT

The technology evolution and complexity of new circuit applications involve emerging reliability problems and even more sensitivity of integrated circuits (ICs) to electrostatic discharge (ESD)-induced damage. Regardless of the aggressive evolution in downscaling and subsequent improvement in applications' performance, ICs still should comply with minimum standards of ESD robustness in order to be commercially viable. Although the topic of ESD has received attention industry-wide, the design of robust protection structures and circuits remains challenging because ESD failure mechanisms continue to become more acute and design windows less flexible. The sensitivity of smaller devices, along with a limited understanding of the ESD phenomena and the resulting empirical approach to solving the problem have yielded time consuming, costly and unpredictable design procedures. As turnaround design cycles in new technologies continue to decrease, the traditional trial-and-error design strategy is no longer acceptable, and better analysis capabilities and a systematic design approach are essential to accomplish the increasingly difficult task of adequate ESD protection-circuit design.

This dissertation presents a comprehensive design methodology for implementing custom on-chip ESD protection structures in different commercial technologies. First, the ESD topic in the semiconductor industry is revised, as well as ESD standards and commonly used schemes to provide ESD protection in ICs. The general ESD protection approaches are illustrated and discussed using different types of protection components and the concept of the ESD design window.

The problem of implementing and assessing ESD protection structures is addressed next, starting from the general discussion of two design methods. The first ESD design method

follows an experimental approach, in which design requirements are obtained via fabrication, testing and failure analysis. The second method consists of the technology computer aided design (TCAD)-assisted ESD protection design. This method incorporates numerical simulations in different stages of the ESD design process, and thus results in a more predictable and systematic ESD development strategy. Physical models considered in the device simulation are discussed and subsequently utilized in different ESD designs along this study.

The implementation of new custom ESD protection devices and a further integration strategy based on the concept of the high-holding, low-voltage-trigger, silicon controlled rectifier (SCR) (HH-LVTSCR) is demonstrated for implementing ESD solutions in commercial low-voltage digital and mixed-signal applications developed using complementary metal oxide semiconductor (CMOS) and bipolar CMOS (BiCMOS) technologies. This ESD protection concept proposed in this study is also successfully incorporated for implementing a tailored ESD protection solution for an emerging CMOS-based embedded MicroElectroMechanical (MEMS) sensor system-on-a-chip (SoC) technology.

Circuit applications that are required to operate at relatively large input/output (I/O) voltage, above/below the V_{DD}/V_{SS} core circuit power supply, introduce further complications in the development and integration of ESD protection solutions. In these applications, the I/O operating voltage can extend over one order of magnitude larger than the safe operating voltage established in advanced technologies, while the IC is also required to comply with stringent ESD robustness requirements. A practical TCAD methodology based on a process- and device- simulation is demonstrated for assessment of the device physics, and subsequent design and implementation of custom P_1N_1-P_2N_2 and coupled P_1N_1-P_2N_2//N_2P_3-N_3P_1 silicon controlled rectifier (SCR)-type devices for ESD protection in different circuit applications, including those applications

operating at I/O voltage considerably above/below the V_{DD}/V_{SS}. Results from the TCAD simulations are compared with measurements and used for developing technology- and circuit-adapted protection structures, capable of blocking large voltages and providing versatile dual-polarity symmetric/asymmetric S-type current-voltage characteristics for high ESD protection.

The design guidelines introduced in this dissertation are used to optimize and extend the ESD protection capability in existing CMOS/BiCMOS technologies, by implementing smaller and more robust single- or dual-polarity ESD protection structures within the flexibility provided in the specific fabrication process. The ESD design methodologies and characteristics of the developed protection devices are demonstrated via ESD measurements obtained from fabricated stand-alone devices and on-chip ESD protections. The superior ESD protection performance of the devices developed in this study is also successfully verified in IC applications where the standard ESD protection approaches are not suitable to meet the stringent area constraint and performance requirement.

To my wife Cecilia, my parents Ramón and Sonia, my Sister Nol,

my parents in law Hector and Cecilia, and

To my grandparents Ramón, Alda, Hector and Olga

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BiCMOS	Bipolar Complementary Metal-Oxide-Semiconductor
CAD	Computer Aided Design
ES	Embedded Sensor
EMS	Embedded MEMS Sensor
EMMI	Emission Microscopy
ESD	Electrostatic Discharge
EOS	Electrical Overstress
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide-Semiconductor
DFT	Design for Testing
DUT	Device Under Test
FA	Failure Analysis
FBJ	Forward Blocking Junction
GGMOS	Grounded Gate MOSFET
HBM	Human Body Model
HH-LVTSCR	High-Holding Low-Voltage-Trigger SCR
IC	Integrated Circuit
IEC	International Electrotechnical Commission

IEC-1000-4-2	International Electrotechnical Commission ESD standard
I/O	Input/Output
I-V	Current-Voltage
LVTSCR	Low Voltage Trigger SCR
LOCOS	Local Oxidation of Silicon
MEMS	MicroElectroMechanical Systems
MM	Machine Model
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
OBIC	Optical Beam Induced Current
RBJ	Reverse Blocking Junction
RF	Radio Frequency
SCR	Silicon Controlled Rectifier
SEM	Scanning Electron Microscopy
SIMS	Secondary Ion Mass Spectrometry
SoC	System-on-a-Chip
SPICE	Simulation Program with Integrated Circuit Emphasis
STI	Shallow Trench Isolation
TCAD	Technology Computer Aided Design
TLP	Transmission Line Pulse
VC	Virtual Component

LIST OF SYMBOLS

ρ	Density (g/cm^3)
C	Specific heat (J/g·K)
κ	Thermal conductivity of the material (W/cm·K)
H	Heat generation term (W/ cm^3)
$\bar{J}_n$	Electron current density (A/cm^2)
$\bar{J}_p$	Hole current density (A/cm^2)
E	Electric field (V/cm)
H_{GR}	Generation-recombination contribution (eV)
GR	Generation-recombination rate
E_g	Bandgap (eV)
q	Electron elementary charge ($1.602 \cdot 10^{-19}$ C)
$\varepsilon(\bar{r})$	Permittivity of the material (F/m)
Ψ	Electrostatic potential ($\bar{E} = -\nabla\Psi$)
$p(x)$	Hole density (atoms/cm^3)
$n(x)$	Electron density (atoms/cm^3)
N_D^+	Ionized donors concentration (atoms/cm^3)
N_A^-	Ionized acceptors concentration (atoms/cm^3)

ρ_f	Fix charge density (C/cm^2)
θ	Band structure parameter (eV)
χ	Electron affinity (4.05 eV in Silicon (Si) @ 300 K)
k	Boltzman's constant ($8.617 \cdot 10^{-5}$ eV/K)
T	Local lattice temperature (K)
N_C	Conduction band density of states (cm^{-3})
N_V	Valence band density of states (cm^{-3})
G	Generation rate ($cm^{-3} \cdot s^{-1}$)
α_n	Electron ionization rate (cm^{-1})
α_p	Hole ionization rate (cm^{-1})
R_{SRH}	Shockley-Read-Hall recombination rate ($cm^{-3} \cdot s^{-1}$)
R_{AUG}	Auger recombination rate ($cm^{-3} \cdot s^{-1}$)
τ_n	Minority electron lifetime (s)
τ_p	Minority hole lifetime (s)
n_i	Intrinsic concentration ($atoms/cm^3$)
n_1	Electron SRH concentration the trap level (cm^{-3})
p_1	Hole SRH concentrations trap level (cm^{-3})
C_n	Electron parameter in the Auger recombination rate ($cm^6 \cdot s^{-1}$)
C_p	Hole parameter in the Auger recombination rate ($cm^6 \cdot s^{-1}$)

μ_n	Electron mobility ($cm^2/V \cdot s$)
μ_p	Hole mobility ($cm^2/V \cdot s$)
μ_T	Net mobility ($cm^2/V \cdot s$)
μ_{SR}	Surface roughness scattering mobility term ($cm^2/V \cdot s$)
μ_{AP}	Acoustical- phonon scattering mobility term ($cm^2/V \cdot s$)
μ_{OIP}	Optical inter-valley phonons scattering mobility term ($cm^2/V \cdot s$)
$\mu_{Ln,p}$	Electron-, hole- low field mobility ($cm^2/V \cdot s$)
β	Fitting parameter in the mobility expression
E'	Electric field in the direction of the current flow (V/cm)
v_{sat}	Temperature-dependent saturation velocity (cm/s)

CHAPTER 1
INTRODUCTION

What makes integrated circuit (IC) technology unique? To answer this question, one just needs to think about the variety of circuit applications that are part of our daily activities and quality of life. From sophisticated entertainment systems [59], reconfigurable communication architectures [3], to advanced instruments for medical assessment and more recently electronic implants [71], the complexity of the countless emerging applications is driving the technology toward unimaginable levels of integration [19]-[20]. Ranging from cutting edge digital and RF (radio frequency) applications already using the 45-nm node [74], to high performance mixed-signal ICs based on a variety of fabrication processes, the technology is making possible vast storage of information and high speed processing capability, but also the development of smart power modules [10], [64], [97], [126] and system-on-a-chip (SoC) applications that can mix signal processing, multiple voltage interface, chemical sensors [2], [124]-[125], or even biological sensors [40] on the same chip.

Technological innovations in the semiconductor industry are driven by the ever changing customers' demands, in a competitive electronics market that has been continuously expanding. Even though innovation in the industry is not slowing down, the road toward new findings is becoming dimmer [47]. Fundamentally, the evolution in the downscaling of the physical dimensions is considered a main factor in obtaining lower cost-, while achieving better performance- and more compact- integrated circuits (ICs), all of them key for today's demanding applications. This evolution in turn is accompanied by changing reliability-related disadvantages. Reliability problems require time-consuming and complex integration of application- and

technology-adapted electrostatic discharge (ESD) protection structures, reassessment of the circuit design methodologies and more stringent design ground-rules.

Among the reliability issues, the problem of electrostatic discharge in the semiconductor industry is distinctive in the sense that it is an unavoidable event that drives the semiconductor devices out of the safe operating area, and it may happen at any time during manipulation and ordinary lifetime of the integrated circuits. The research presented in this dissertation looks for answers to address ESD-induced problems in ICs, by developing a systematic methodology to implement custom on-chip ESD solutions. To introduce the fundamental concepts employed in this study, the next sections provide an overview of the ESD phenomena, ESD models, traditional methods to provide ESD protection, the notion of ESD design window and a brief description of the dissertation contributions and content.

1.1. Implications of ESD in the Semiconductor Industry

An electrostatic discharge (ESD) is an event that transfers a finite amount of charge between objects brought into close contact. Depending on the object type, the process can result in a rapid- (hundreds of nanoseconds) and high- current pulse of several amps. The presence of electrostatic discharge affects the semiconductor industry considerably, and has become a topic of major interest and discussion [5], [96], [115]-[117]. Due to the small size of today's semiconductor devices, the large electric field induced during an ESD event would likely cause latchup, local melting, soft- or hard- damage, or destructive breakdown in sensitive isolation layers, such as thin gate oxide in CMOS technologies.

Damages associated with latchup and ESD stress have emerged as important obstacles in the technology downscaling process [4], [111]-[113]. Statistically, one-third to one-half of the

overall customer return is attributed to failure in the integrated circuits (ICs) due to ESD/EOS (electrostatic discharge/electrical overstress) [68]. Technological strategies have been developed to overcome the limitations imposed by the latchup problem, while the necessary ESD immunity is also reached. However, with increasingly demanding product applications and the required compatibility with existing systems, latchup prevention and ESD robustness are even more challenging and contradictory design considerations [113].

There are two general methods to reduce IC failure due to ESD. One consists of the usage of ionization apparatus, the proper handling and grounding of personnel and equipment during manufacturing, and the usage of safety packaged chips, i.e., to prevent ESD events from occurring [109]. The other method consists in connecting on-chip or external protection circuits to the pins of a packaged IC, which would divert high currents away from the internal circuitry and clamp high voltages during an ESD stress [25]. A chip manufacturer has partial control over a customer's handling of its product, and external protection circuits are commonly inefficient and costly solutions. The problem should be solved by incorporating effective on-chip protection circuitry. Since the spectrum of stresses under the label of EOS/ESD is broad, it is not possible to guarantee total EOS/ESD immunity. However, through the proper design of protection structures, the threshold of sustainable stress can be significantly increased, resulting in improved reliability of the ICs and electronics systems [116].

Electrical overstress is a class of event that affects IC products by exceeding maximum design operating conditions. EOS usually leads to gross damage in an integrated circuit resulting from high-energy events such as electrostatic discharge (ESD), electromagnetic pulses, or reversal of power and ground pins. Long EOS events can lead to damaged areas such as blown metal lines or cavities in the semiconductor due to local heating, typically with a relatively large

radius of damage. This damage leads to either a reduction in IC performance (e.g., increased leakage current on one or more pins) or total circuit failure. Figure 1.1 depicts typical EOS/ESD signatures in integrated circuits. Figure 1.1(a) shows a localized damage caused by an ESD-type short pulse of current (about 100 ns), Figure 1.1(b) depicts the amplified Scanning Electron Microscopy (SEM) image of the damage in (a), while Figure 1.1(c) shows a severe damage caused in a multiple-finger ESD device by a pulse of voltage in the order of few microseconds.

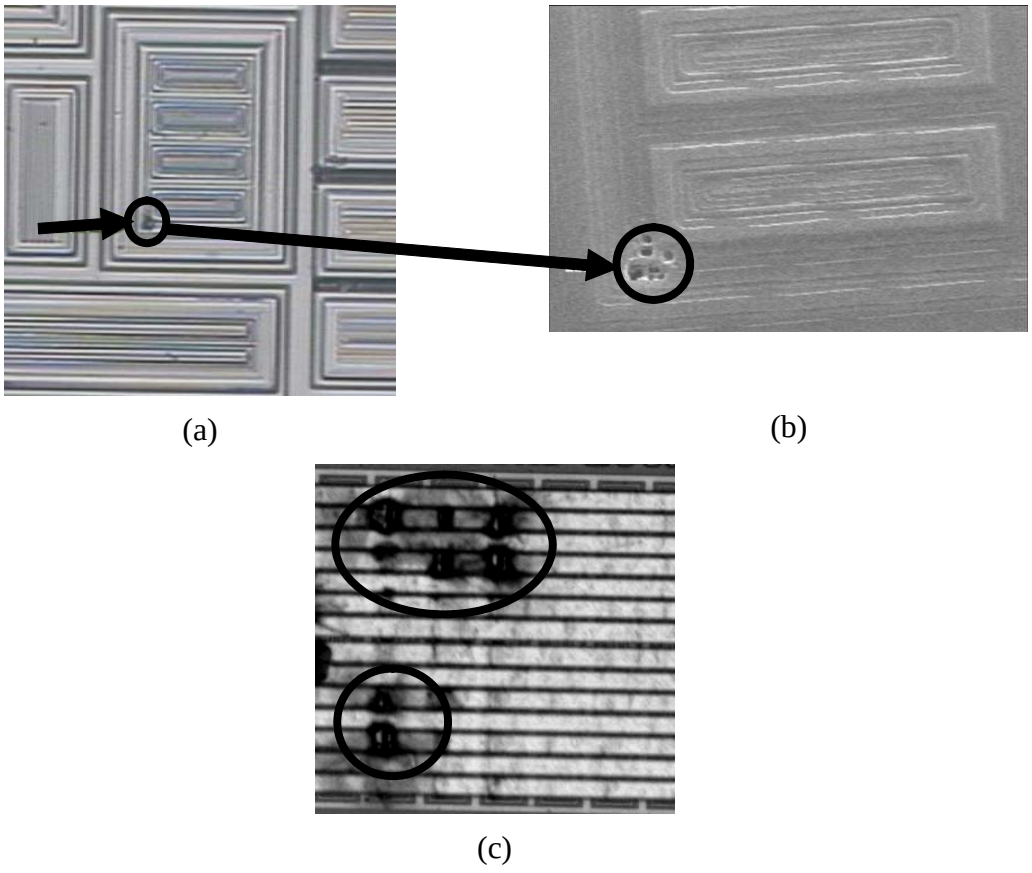


Figure 1.1. a) Micrograph of localized small-radius damage, b) Scanning Electron Microscopy (SEM) image of the damage, and c) EOS-type of damage in different areas of an ESD device.

The region of EOS phenomena with stress times of less than one nanosecond up to a few hundred nanoseconds is considered as electrostatic discharge (ESD). Although EOS covers a large range of phenomena including ESD, it is common to refer to the time range of 100 ns and

less as the ESD regime [76]. ESD usually leads to relatively subtle, localized damage sites extending to a relatively small radius.

There are two main dangers of ESD stress. One is the danger of gate oxide dielectric breakdown due to the high voltage seen during an ESD event. For instance, in a 0.25 μm CMOS technology with a SiO_2 (silicon oxide) gate dielectric in the order of 50 Å thick, assuming a dielectric strength close to $8 \cdot 10^6$ V/cm [39], a stress of 4 V is enough to cause oxide damage. In a typical CMOS technology, the thin gates of an input buffer are tied directly to the input pin, and thus are especially vulnerable to oxide breakdown. This condition gets even more critical as the technology scales down [4]. The other form of damage created by ESD stress is melting of material due to Joule heating [115], which refers to the resistive heat generated by a current. If the current density of an ESD event is sufficiently high, thermal runaway occurs, leading to either device failure, i.e., shorts and opens in junctions or metals, or the more subtle damage of increased leakage.

Dielectric failure and thermal failure are generally considered to be catastrophic, i.e., the IC is no longer functional after the ESD stress. However, there is another type of ESD damage referred to as soft failure. This failure consists of increased leakage current or reduced oxide integrity, without loss of functionality, due to earlier exposure of the circuit/device to ESD that does not result in an immediately detectable discrepancy [64]. A small damage could act as high-resistance filament across a diode junction, thereby increasing the leakage current to a significant but non-catastrophic level [43] [69].

1.2. Characterizing the ESD Performance in Integrated Circuits

In order to characterize the susceptibility of an IC to ESD damage, the IC must be tested using standard models which simulate real ESD events. The ESD models are represented as lumped circuit equivalents, so that testing is consistent and reliability can be defined as a quantitative attribute. ESD stress occurs during wafer fabrication, surface bonding, packaging, testing, or any other time the circuit comes in contact with a person or machine. Specific tests are designed to model particular events such as human- or machine- discharge to ground, field induction, cable interconnections, among other conditions encountered in the handling and operation of ICs.

Figure 1.2 shows a simplified schematic representation of the lumped circuit used as reference for the simulation of the ESD events. By selecting different values for the passive components, simulation of different ESD model standardized waveforms can be obtained.

1.2.1. Human Body Model (HBM)

The HBM is intended to represent the electrostatic discharge generated when a pre-charged human being approaches a component [42]. The HBM lumped circuit model is represented as a capacitor discharging through a resistor, with the capacitor $C_{ESD} = 100$ pF, the inductor $L_{ESD} \approx 7.5$ μH, and the resistor $R_{ESD} = 1.5$ kΩ.

1.2.2. Machine Model (MM)

The MM is intended to represent the interaction of electrical discharge from a pre-charged conductive source, such as metallic tools or machine, to the component [70]. In Japan, this model is widely used in the automotive industry. The standardized waveform for the MM is obtained by

incorporating in Figure 1.2, the capacitor $C_{ESD} = 200$ pF, the inductor $L_{ESD} \approx 1.5$ μH, and the resistor $R_{ESD} \approx 15$ Ω. Due to the low series resistance, the MM ESD event is faster than the HBM event. Typically, the failure signatures of the HBM and MM are similar, but the magnitude of the protection level obtained for the MM is normally 10 to 15 times lower than that obtained for the HBM.

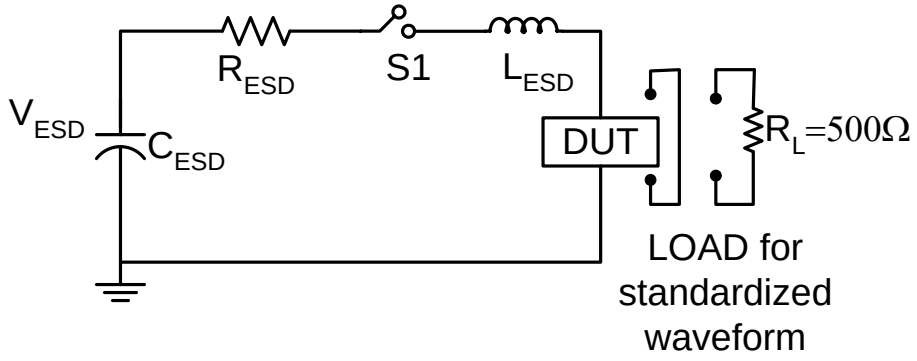


Figure 1.2. Simplified lumped circuit representation for ESD standards waveform simulation.

1.2.3. Charged Device Model (CDM)

The Charged Device Model represents the electrostatic discharge occurring between a chip and an external element via pin-discharging path. Different from HBM and MM, in the CDM it is the packaged integrated circuit that accumulates the charge on its package and/or die [16], [60]. The resulting damage due to such direct pin discharge is normally gate oxide breakdown. Because of the widespread use of automated manufacturing and testing line, as well as thinner gate oxides in advanced technologies, the CDM model has gained importance in more recent years [29], [77]. A typical CDM setup is shown in Figure 1.3. The CDM is the fastest of the ESD phenomena, and the equivalent lumped circuit typically includes, a capacitor $C_{ESD} = 6.8$ pF, an inductor $L_{ESD} < 1$-μH, and a resistor $R_{ESD} \approx 15$ Ω.

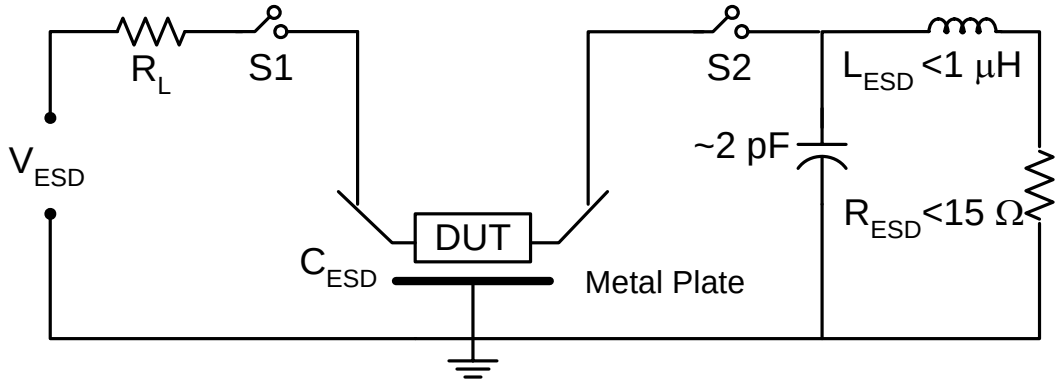


Figure 1.3. Simplified CDM lumped circuit representation.

1.2.4. System-Level ESD Standard IEC 1000-4-2

The IEC 1000-4-2 standard relates to equipment, systems, sub-systems and peripherals which may be involved in electrostatic discharge owing to environmental and installations conditions [45]. In this standard two different test procedures are defined, the air-gap test and the contact test. Commonly, the air-gap test is less repeatable than the contact test. In regular testing programs, circuits are tested powered up and powered down in order to guarantee functionality after stress, not only when the system is off but also during operation. Figure 1.4 shows the simplified schematic representation of the standard lumped circuit. The circuit components include, a capacitor $C_{ESD} = 150$ pF, an inductor $L_{ESD} \approx 0$ μH, and a resistor $R_{ESD} \approx 330$ Ω.

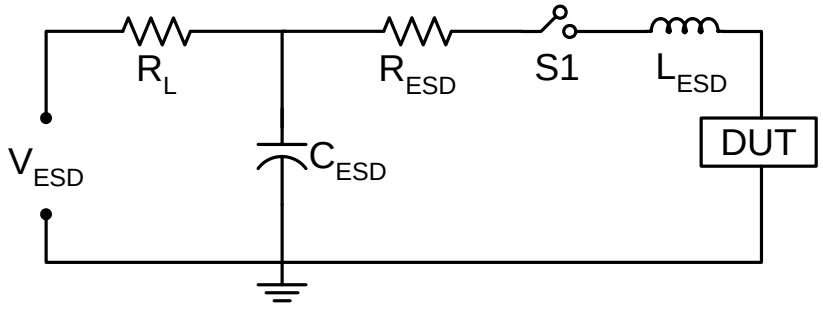


Figure 1.4. Simplified lumped circuit representation of the ESD standard IEC 1000-4-2.

Figure 1.5 compares the normalized current waveforms for the different ESD models previously discussed. Note that, consistent with the previous discussion, the CDM rise time is considerably faster than the other ESD standards, followed by the MM, IEC-1000-4-2 system level ESD, and the HBM showing the slowest rise time and decay time. Another important consideration is that for the case of the MM, the oscillating waveform results in high peaks of ESD current in both polarities, as a consequence, ESD structures designed to sustain the MM should be able to handle high dual-polarity peak of ESD current. If an ESD structure is able to sustain high ESD stress only for one voltage/current polarity, the HBM lumped circuit generates the kind of waveform that is more appropriate for characterization of the structure at a single polarity.

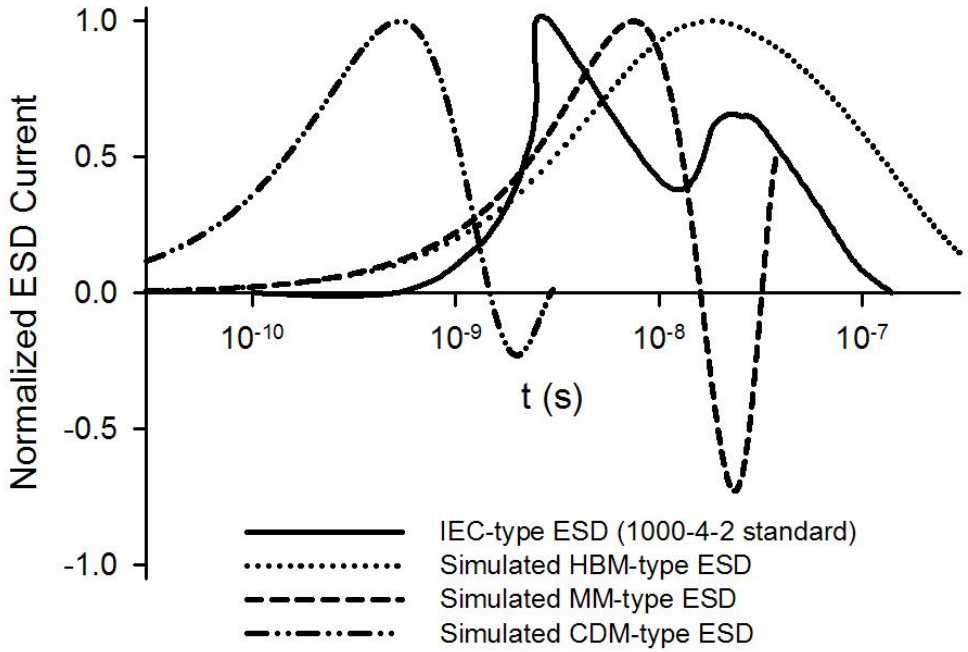


Figure 1.5. Superposed waveforms obtained for the standard ESD models (logarithmic time scale). Waveforms generated from SPICE simulation and IEC-1000-4-2 standard.

1.2.5. Transmission Line Pulse (TLP)

The generation of ESD current pulses for design, characterization, and optimization of ESD devices is possible with a charged coaxial transmission line. In this form of ESD testing, a transmission line cable is charged by a voltage source, and the transmission line pulse (TLP) system forces a trapezoidal current waveform in the device [104]. The pulse width of the TLP is a function of the length of the transmission line and the propagation velocity of the transmission line. For this method, the standard choice of pulse width has been determined based on the HBM model, i.e., the TLP current level gives an estimated HBM level [12], [61]. Figure 1.6 shows the measured current- and voltage- TLP waveform. This ESD characterization method allows for a closer estimation of the device conducting characteristics, even at elevated levels of current. It also provides an idea of the quasi-static behavior of the ESD device, since reliable data can be taken during the 100 ns time frame of the pulse width, having reduced effects of self-heating in the device. In this respect, the TLP curve below the second-breakdown point can be considered a good approach to a dc-simulated curve. However, it still represents the way the device responds to ESD stress because it reveals the operating points after the initial turn-on transient.

Additional to the previously discussed ESD characterization models, there are other ESD models proposed in the literature, which are extensions of the models previously discussed and are used in particular for specific system- or circuit- applications [5], [115], [117]. The previous discussion about the ESD models reflects how ESD events may occur in almost all the integrated circuit's settings, and depending on the condition, the type of ESD event is considerably different. In the next section, the concept of ESD design window and the standard approaches to provide ESD protection are discussed.

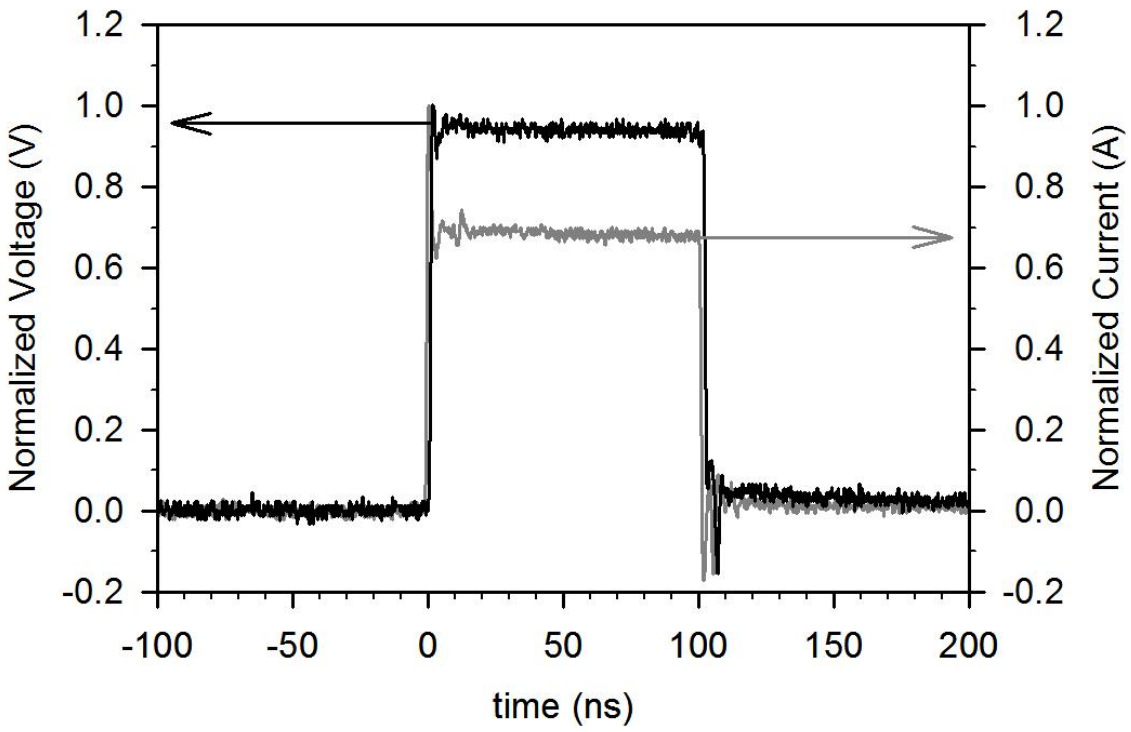


Figure 1.6. Measured current and voltage TLP waveforms.

1.3. Standard ESD Protection Design Schemes

The design and integration of electrostatic discharge (ESD) protection systems constitutes one of the fundamental and necessary steps in the manufacture of commercially viable and reliable integrate circuits (ICs). The increasing demand for state-of-the-art ICs is forcing the semiconductor industry to invest considerable resources in designing and developing effective on-chip ESD protection structures that must be realized within the available technology. The purpose of this section is two-fold. First, it discusses the ESD protection principle and the traditional devices used as ESD protection structures. Second, it describes the actual implementation of the on-chip ESD protection circuit using the concept of ESD design window.

In the previous discussion it was identified that the ESD events induce two main problems in the semiconductor devices and circuits, one is the thermal damage due to the elevated current applied during the ESD event, and the second is the oxide breakdown caused by the high electric field. Therefore, the principle of the ESD protection is 1) to safely discharge ESD current via a low impedance path, and 2) to clamp the pad voltage at a sufficiently low level. Additionally, the protection circuit itself should not become leaky and degrade chip performance. To avoid being damaged, the protection circuits should minimize self-heating by keeping current densities and electric fields in the silicon low, and prevent dielectric breakdown of the gate oxides in the protection circuit, by minimizing the voltage peaks across the oxides.

Electrostatic discharge protection circuits can be implemented by using different combinations of standard devices readily available in technology libraries. Given its simplicity, the junction diode is one of the circuit elements widely used for ESD protection. Diodes can be used as a protection device in either forward- or reverse- biasing. Either way, this device shows a simple turn-on that can clamp the level of voltage in a specific pad within a safe operating range. The junction diode, however, may be inefficient because it occupies a large area, especially when operated in reverse biasing, and consequently increases the size and cost of the chip. A large ESD protection component also responds slower and incorporates parasitic elements that degrade the performance of the -circuit and -ESD device itself.

The bipolar junction transistor (BJT) is also used in different IC's ESD protections [25], [32]. The collector of the BJT is normally connected to the protected pad, the emitter to one of the power rails, and an additional resistor between the base and emitter is incorporated. When the ESD pulse appears in the protected pad, the BJT can go into the snapback mode and create a low impedance discharge path that guarantees the integrity of the protected circuit. Due to the

conductivity modulation during the snapback, ESD protection clamps based on BJTs tend to be smaller than diode-based clamps. Additionally, the BJT is indirectly the underlying building element of many other protection structures. This is the case for MOSFET- and SCR (silicon controlled rectifier)-based ESD protection structures discussed below.

Another proven protection element more often used in CMOS technologies is the MOSFET. For example, the grounded gate N-MOSFET (ggNMOS) with minimum design channel length and gate-, source-, and bulk- contacts tied together to ground represents the key element of many ESD protection concepts. Beside its electrical properties, it is available at the beginning of the technology definition, characterized at the early stages of the development process, as well as area-effective if compared to the diode.

The operation of the ggNMOS during an ESD event is mainly controlled by the embedded NPN junction bipolar transistor (BJT), formed by the drain (n+), bulk (p), and source (n+), lateral structure [5]. As a result, the ggNMOS goes into snapback [6] during an ESD event and can be often self-protected. A similar concept applies to the PMOS. A drawback of an ESD device with MOS gate is that it can suffer long-term reliability problems if the pad operating voltage is higher than the pre-established voltage rating, or if a relatively large electric field is applied at the gate during the ESD event [69]. To overcome the reliability problems associated to the thin gate oxide, some technologies incorporate the so-called field oxide [5]. However, this is not a common practice in advanced technologies, and other design-adapted device structures need to be investigated within the flexibility provided by the specific process.

Implementing ESD protections by using the standard devices discussed above would result in more predictable while less complex designs in a pre-silicon phase. However, these standard devices do not necessarily allow for implementation of all the demanding ESD constraints

imposed by different technologies and circuit applications. Consequently, different device structures based on the SCR concept have been proposed in the literature using an experimental approach [54]. The SCR-based devices are not standard structures optimized in CMOS or BiCMOS processes, and even though these devices can be the most efficient structures in terms of ESD protection, it has been rather difficult to design functional SCR-based protection devices [22] and effective compact modeling techniques for this type of device are also required [94].

Although the SCR-type structures might serve as superior ESD protection components in CMOS/BiCMOS technologies, the embedded SCR in the CMOS/BiCMOS processes has been, instead, a cause of concern because of the latchup problem [115]. A parasitic SCR can be readily identified in a CMOS inverter, where it is formed by the two coupled BJTs, Q1 and Q2 in Figure 1.7. Thus, the challenge in the ESD design using SCR-based structures is to maintain a safe operation in the circuit without a latchup problem, while obtaining the advantage of the deep snapback and high conductivity modulation for high ratio of ESD protection per unit area.

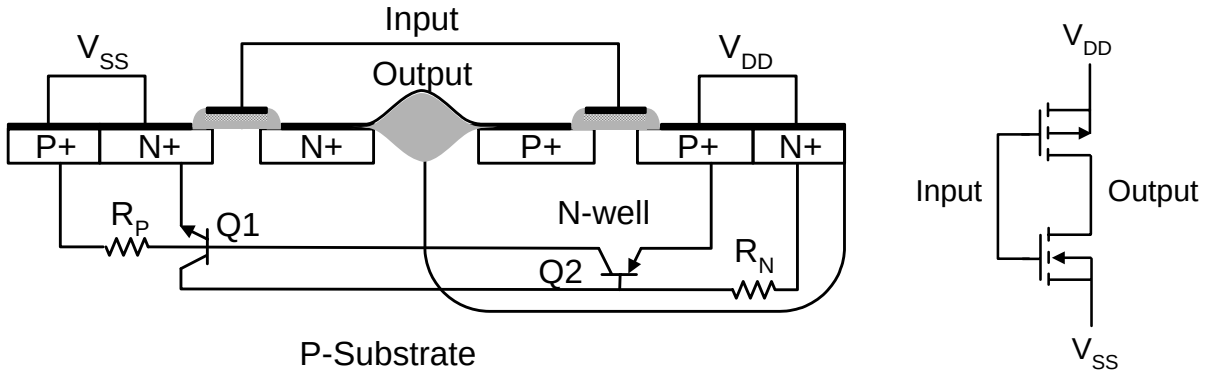


Figure 1.7. Cross-sectional view of a CMOS inverter and associated parasitic SCR.

The devices previously discussed from the ESD application perspective, can be used independently or combined to implement the actual ESD protection schemes. Figure 1.8 shows a block diagram representation of the different ESD pulsing modes. In practice, ESD pulses

applied to a bonding pad may be identified in different directions, i.e., from the I/O pad to V_{DD} and vice versa, from the I/O pad to V_{SS} and vice versa, and from V_{DD} to V_{SS} and vice versa [57], [87], [120]. ESD designs do not always need to include specific protection elements for each one of the ESD pulsing modes, but the protection must incorporate the necessary structures that guarantee a safe operating voltage in the core circuit I/Os, and create low impedance current paths during an ESD event between any pair of bond pads [91].

Figure 1.9 shows various examples of ESD protection schemes that can be implemented using different combinations of the standard devices previously discussed. Figure 1.9(a) shows a generic ESD protection block diagram and examples of diode, BJT and MOSFET protection elements. ESD protection can be also implemented using different combinations of SCR-based structures [24] following a similar idea. For example, assuming that the simplest diode structure is incorporated in the scheme, if the core circuit is powered up, diode D1 will turn-on and conduct current for any input voltage greater than $V_{DD} + V_D$, where V_D is the forward-junction voltage drop. Similarly, diode D2 will clamp the negative voltage below $V_{SS} - V_D$. If the chip is not powered-up and an ESD pulse is incident between the input and, e.g., V_{SS}, the voltage will be clamped at either the reverse breakdown voltage of the diode for a positive pulse or at $- V_D$ for a negative pulse. Similarly, the supply clamp provides a current path between V_{DD} and V_{SS} and vice versa during an ESD event in any of these two terminals.

On the other hand, if the PMOS (M1) and NMOS (M2) devices are used, the protection scheme behaves similarly. In this case, the drain substrate junctions take the place of the diodes. One major difference is that the drain substrate junction reverse breakdown triggers the MOS device into a snapback mode in which the drain voltage drops due to the turn-on of the lateral

parasitic bipolar transistor formed by the drain, channel, and source regions. A direct extension of the previous explanation can also be used for the BJT-based protection scheme.

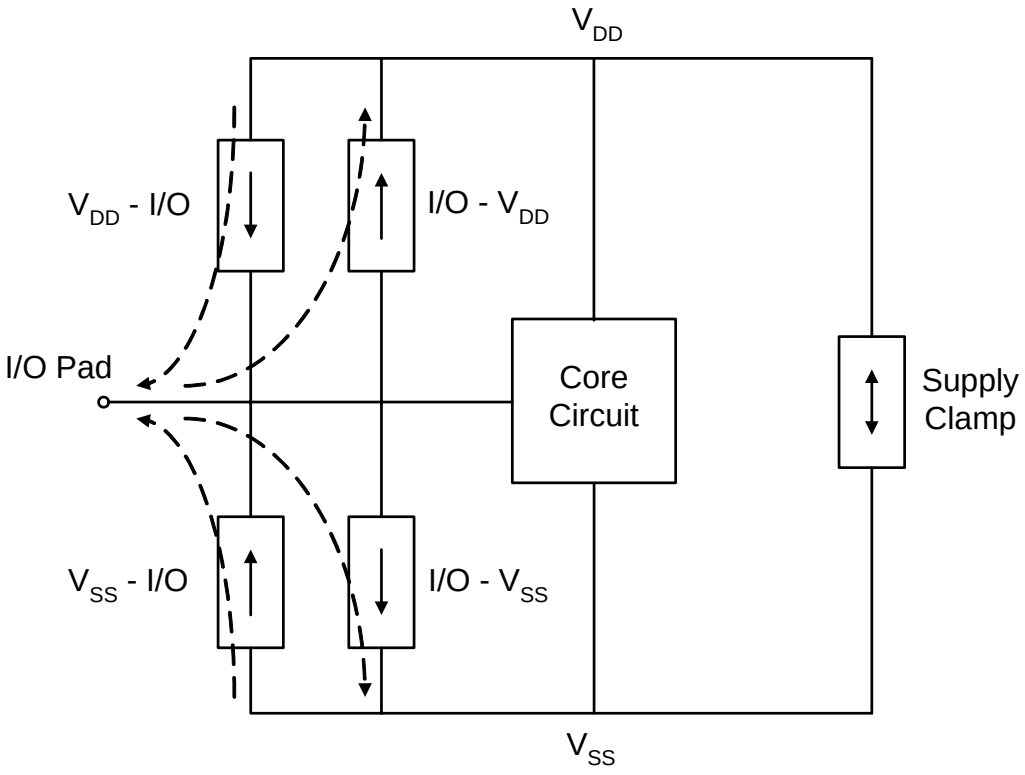
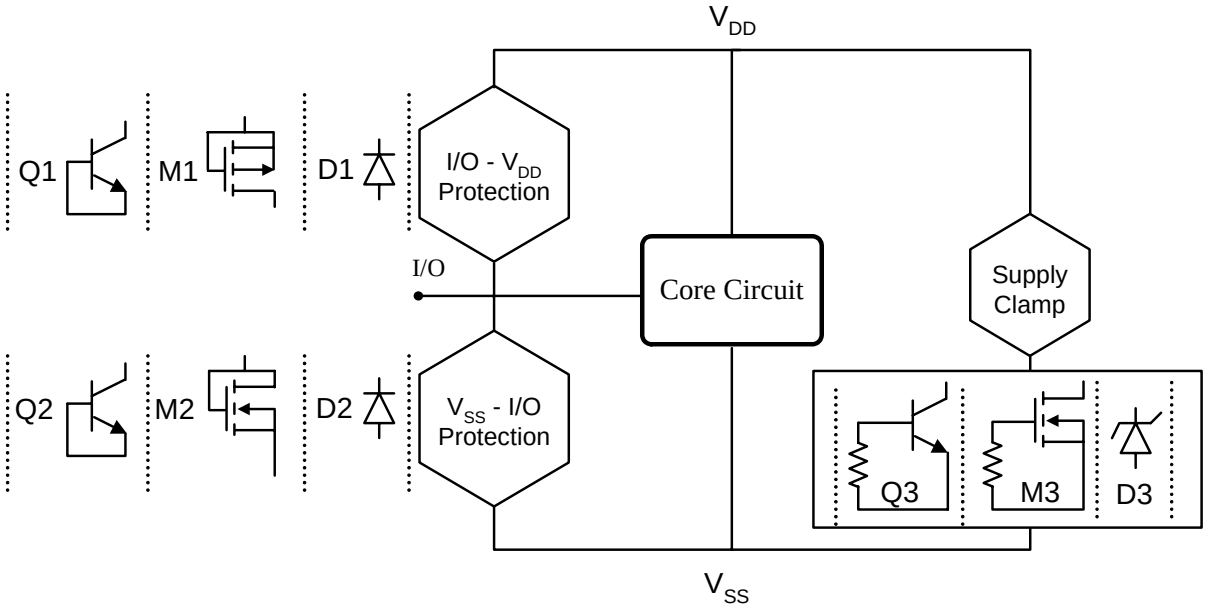


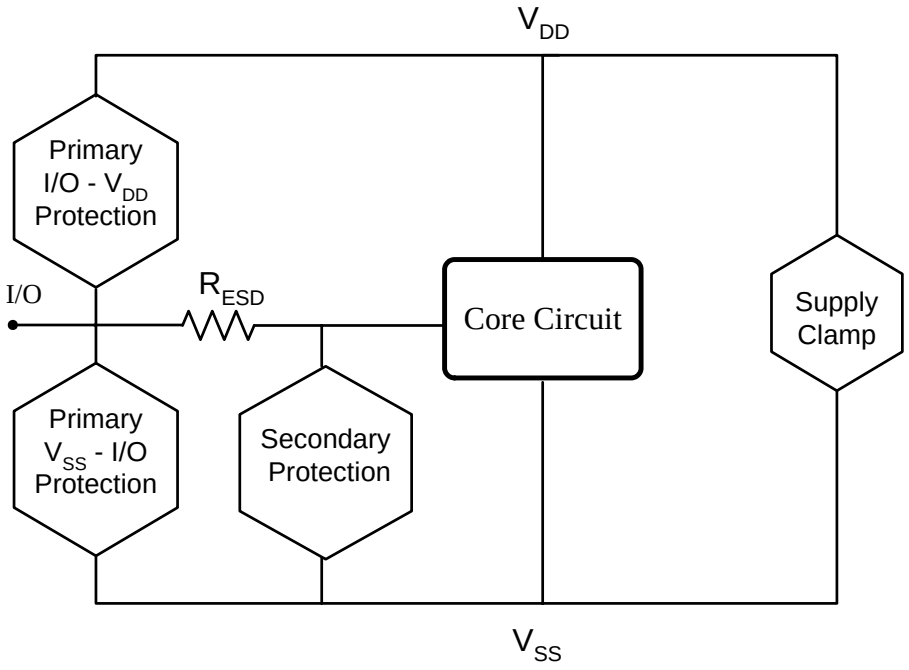
Figure 1.8. ESD pulsing modes.

The scheme shown in Figure 1.9(b) illustrates the condition where a redundant protection is considered. In this case, the ability of the pull-up and pull-down clamping is combined with an additional I/O ESD protection, e.g., ggNMOS, which is found especially useful for protecting the core circuit against fast rise time ESD events, such as CDM. This scheme can be considered an extension of the previous one, where a primary ESD protection (Figure 1.9(a)) and a secondary ESD protection are incorporated. The primary ESD protection can follow the same criteria previously discussed and combine different devices, while in the secondary ESD protection it is normally desirable to incorporate a device that would have the fastest response during the ESD event [117].

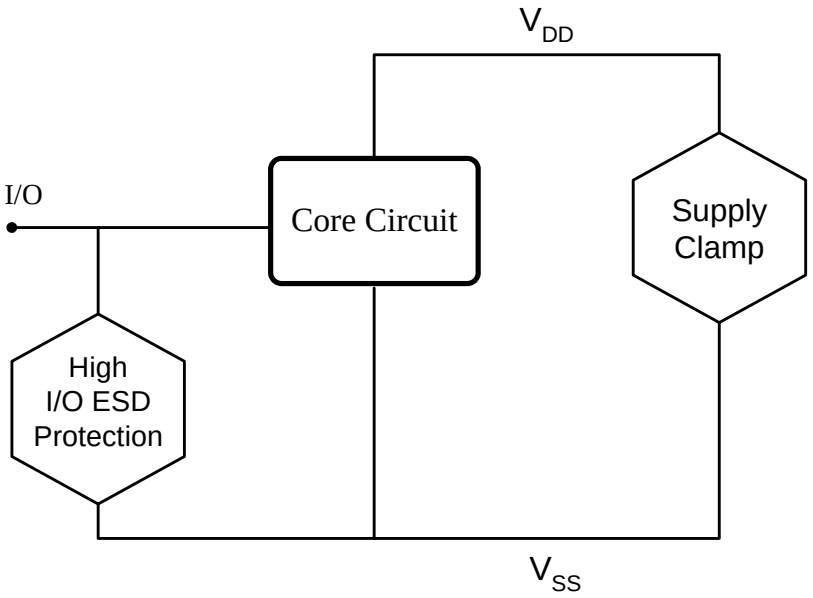
In the case of the scheme shown in Figure 1.9(c), the protection can be applied directly to the core circuit, or also combined with any of the two previous schemes, i.e., the core circuit can incorporate already a primary and even a secondary ESD protection. The V_{SS}-referenced ESD protection directly connected to the I/O pad (high I/O ESD protection) may be designed to operate 1) within the range of the core circuit voltages, which is the case for standard digital circuits, or 2) outside the core circuit bias voltage, which is a condition found in mixed-signal applications. For the latter condition, the set of alternative protection structures that can be used is reduced, which along with the normally required high ESD level of protection, makes this type of ESD design difficult to accomplish. Similar to the scheme in Figure 1.9(c), the schemes in Figure 1.9(a) and (b) can be also extended to circuit applications operating at I/O voltages outside the core circuit operating voltage, given that the protection elements are stacked or re-designed to conduct at the appropriate breakdown voltages.



(a)



(b)



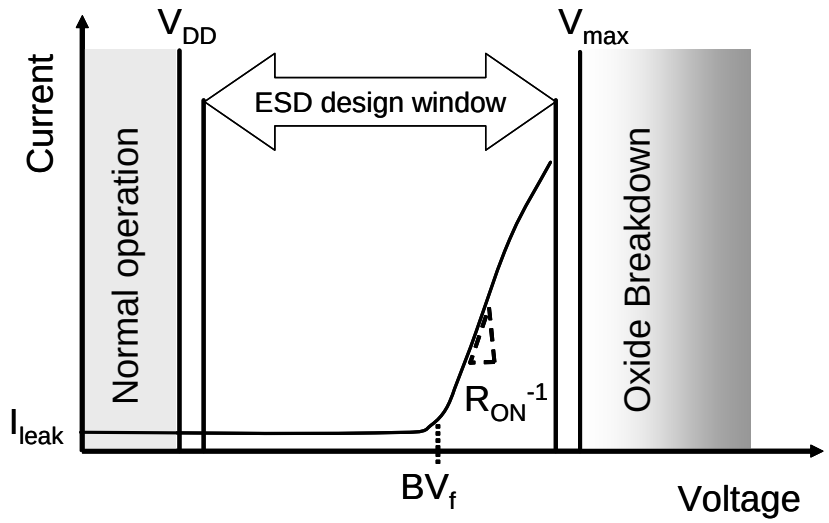
(c)

Figure 1.9. ESD Protection Schemes, a) pull-up, pull-down and supply clamp scheme, b) redundant primary and secondary ESD protection scheme, and c) V_{SS}-referenced high I/O ESD protection and supply clamp scheme.

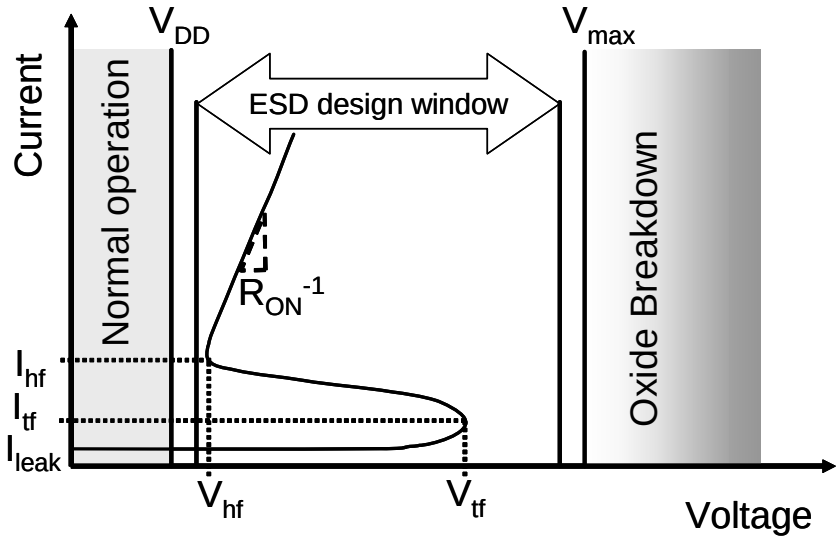
The previous schemes can be combined in different forms to implement effective off- or on-chip ESD protections. Once the protection scheme is defined, the operating voltages are constricted by several conditions, which are not only related to the technology reliability considerations, but also to the circuit application requirements. The definition of these ESD protection constraints is one of the crucial steps in a successful and effective ESD protection implementation. Subsequently, custom design effort of the protection structures will be based on this premise, which will be referenced hereafter as ESD design window.

The ESD design windows for each protection structure incorporated in the previously discussed protection schemes are generally different, and strongly affected by migration between technologies and circuit operating conditions. As an example, the supply clamp shown in Figure 1.9 has to fulfill certain electrical requirements summarized in Figure 1.10. These requirements are technology-dependent and may be different to the requirements of the I/O pad protection. Within the supply clamp design window, the ESD structure may depict different types of conductions, e.g., (a) junction breakdown-type characteristics, or (b) S-type I-V characteristics. Key considerations for the design of this specific protection component include: 1) low leakage current (I_{leak}) in the V_{SS} to V_{DD} operating voltage, 2) the breakdown voltage (BV_f), trigger voltage (V_{tf}), as well as the clamping voltage at the required ESD level, have to be kept below the range of voltage where oxide breakdown or breakdown of internal parasitic components take place, 3) the sustaining point (also called holding point) in the case of the S-type I-V characteristics has to be larger than the V_{SS} - V_{DD} plus a safety range; this avoids latchup problems or unintentional on-state condition in the protection devices, and 4) good robustness of the protection device, i.e., low power dissipation and high ratio of ESD protection per unit area.

Similar considerations need to be defined for any other structure incorporated in the protection scheme.



(a)



(b)

Figure 1.10. Examples of ESD design window a) junction breakdown-type conduction, b) S-type I-V characteristics.

From the previous discussion, it is possible to visualize the basic concepts involved in the IC's ESD protection design, as well as understand the complexity and numerous considerations involved in the design process. From the design engineer's perspective, the problem of ESD design can be considered out of the circuit-designer scope, and be qualified instead as a technology development problem that goes from the process definition, following with circuit and layout place and routing considerations, and even packaging constraints.

Even though the ESD design will always require technical expertise, a better understanding of the ESD problem and a systematic procedure to implement custom ESD protection devices, will make the design process more efficient, the manufacturing turn-around cycles shorter, and consequently, production of robust integrated circuits less costly. With this purpose, a methodology for the simulation, design and characterization of custom ESD protection devices for digital and mixed-signal applications is developed in this study. For more detailed information about ESD fundamental concepts and technology, references [5], [115]-[116], and [119] provide more documentation on this topic, and different points of view about alternative methods to address this reliability problem. In the next section, a summary of the contributions of this dissertation is presented.

1.4. Organization of the Dissertation and Contributions

The investigation presented in this dissertation provides a comprehensive study of the ESD protection development using SCR-type structures. It elaborates on a systematic methodology to define ESD test matrices, as well as simulate and implement custom ESD protection devices with symmetrical and asymmetrical S-type I-V characteristics, adapted to different CMOS/BiCMOS technologies and circuit applications. The design guidelines developed in this

research are based on TCAD (technology computer aided design) simulation and experimental studies accomplished in commercial technologies. The organization of the dissertation is as follows:

Two design methodologies employed in this study for the design of ESD protection devices are introduced in chapter 2. The design flow and strategies followed in an experimental approach and a TCAD-assisted ESD design are compared and discussed. The TCAD simulation is shown to be effective in providing valuable information in the ESD design process. Physical models and related equations incorporated in the electro-thermal TCAD ESD simulation are provided and discussed. The methodologies applied in this study have led to the generation of novel devices not previously developed in the CMOS/BiCMOS technologies under consideration.

Implementation of SCR-type devices for ESD protection in digital and mixed-signal applications operating at relatively low voltage, i.e., in the range of 1.5- to 5-V, is a very attractive solution. However, latchup, layout complexity, and high trigger voltage have been typical problems hindering the application of SCR-type devices for ESD design. Chapter 3 presents in detail the design guidelines for implementation of ESD protection systems employing a device called high-holding low-voltage-trigger silicon controlled rectifier (HH-LVTSCR). In this device, a low trigger voltage while a high holding voltage are demonstrated. A case study is presented for the implementation of multifinger devices with low trigger, high holding voltage, and high bidirectional ESD protection capability for the design of supply clamps and I/O protection components.

Chapter 4 assesses and extends the implementation of the HH-LVTSCR-concept developed in this study to different CMOS technologies. A case study is presented for the implementation of ESD protection systems for embedded MEMS sensor (EMS) multi-technology system-on-a-

chip (SoC) applications. The ESD protection system is developed starting from a new device design adapted to the technology, classification of ESD protection components, followed by the layout of customized multifinger protection cell, and final incorporation of the ESD protection devices in the existing EMS-SoC. The performance of the on-SoC protection is demonstrated via the standard ESD measurements previously discussed.

One of the roadblocks in the TCAD-assisted design of ESD protection structures is the convergence problems associated with the simulation of complex ESD devices. Chapter 5 demonstrates a new TCAD simulation procedure for implementation of symmetrical and asymmetrical ESD protection structures. Special emphasis is given to the discussion of the methodology employed to address convergence problems in steady-state simulations, while avoiding the time consuming transient or mixed-mode simulations discussed in chapter 2.

Implementation of gated SCR-based devices such as the HH-LVTSCR in chapter 3 and chapter 4 is acceptable as long as the pad operating voltage does not affect the integrity of the gate oxide. However, mixed-signal circuit applications are required to interface with external systems operating at a variety of voltages, frequently considerably higher/lower than the core circuit power supply, and at levels of voltage exceeding the safe operating area of the technology small devices. Chapter 6 extends the design methodology introduced in chapter 5, and presents measurements of different families of protection devices, fully customized for implementation of a wide range of ESD protection systems in commercial mixed-signal applications. The design guidelines discussed in that chapter allow for the adjustment of the critical parameters in the ESD protection device, custom layout, and effective integration in products where standard ESD solutions fail in providing the required robustness.

CHAPTER 2
METHODOLOGIES FOR THE DESIGN OF ELECTROSTATIC DISCHARGE (ESD) PROTECTION STRUCTURES

The rapid evolution of the semiconductor industry makes it increasingly difficult to maintain technology- and application- adapted on-chip ESD protection [4]-[5], [96], [116], since existing ESD solutions may need to be redesigned or even redefined within short time cycles. The design of protection circuits is commonly accomplished following an experimental approach. In the best scenario, this procedure may lead to a fast solution, but more often results in a long cycle of experiments and numerous test devices that may or may not lead to the required ESD protection solution. This uncertainty in the design of ICs' ESD protections is exacerbated in new technologies- and circuit- applications, in which the window for the protection devices is narrower [67], the devices are required to respond fast, incorporate minimum parasitic components [62], and occupy the minimum silicon area [89].

As the semiconductor industry evolves, changes are not only observed in the conception of the technology, but also in the companies' target and corporate strategies pursued to gain markets and establish benchmarks in specific sectors. These strategies have resulted in expansion of fabrication outsourcing to specialized foundries, and consequently, less number of IC design companies running in-house fabrication facilities. Using foundry processes, however, the designers are restricted to the specific technology and a pre-established process. Furthermore, they have also limited information to reformulate design rules or generate custom structures that may be necessary for implementation of different ESD protection designs.

Even though the implementation of application-specific ESD solutions at the process development phase provides a better possibility of reliable ESD design libraries, each condition for the designers and process type requires its own ESD design methodology [97]. The approaches can be either empirical, more systematic through the use of TCAD simulations, or alternatively combining experimental procedures and TCAD simulations. In this chapter, the design methodologies that combine the previous approaches are discussed.

2.1. ESD Protection Design Following an Experimental Approach

Similar to the methodology already established in the industry to optimize the technology performance and reach certain design goals, the efficient implementation of ESD protection devices also requires a disciplined characterization of the specific process, and pursues design strategies to comply with the design-specific requirements. In an effort to address the strategic ESD planning and provide a methodology to estimate ESD technology benchmarking, the SEMATECH working group has proposed standardized structures, testing and equipment that allow for ESD technology roadmap assessment [110].

SEMATECH working group's ESD assessment identifies standard structures provided in the process, evaluates ESD robustness of CMOS technology, and provides insights about possible strategies to improve the ESD performance. Besides this standard experimental method to evaluate and project the ESD capability of the technology, there are also other subsets of non-standard structures embedded in the processes. These structures can be also optimized to provide custom ESD protection, thereby increasing the amount of circuit applications that can be implemented in the specific technology. Evaluation and design of such custom ESD protection structures following an experimental approach, however, commonly require long development

cycles [97]. A comprenhesive flow diagram summarizing the FA (failure analysis) and redesign cycles of ESD development following an experimental approach is shown in Figure 2.1.

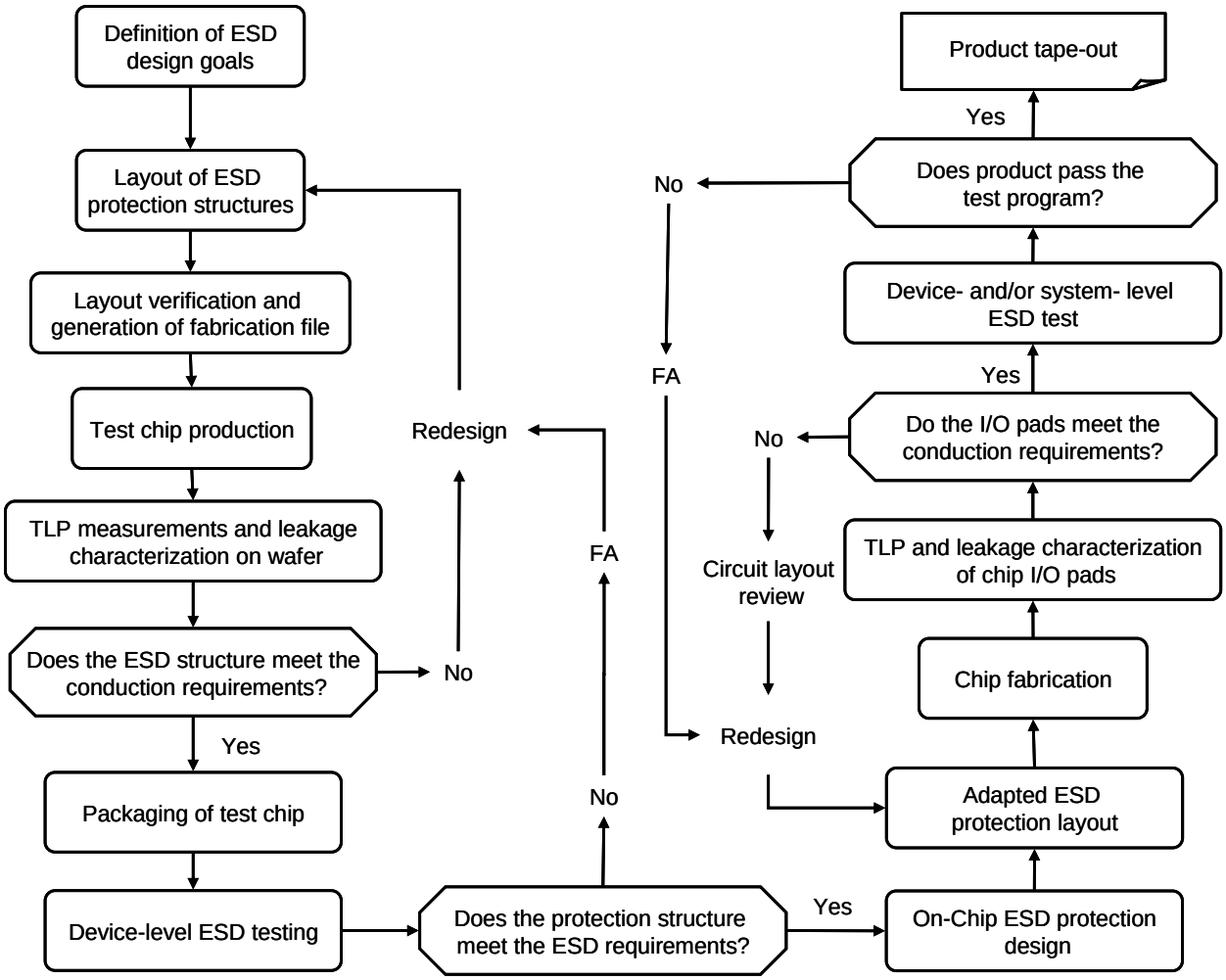


Figure 2.1. Experimental ESD design cycle.

As described in chapter 1, custom ESD protection devices need to depict specific conducting characteristics depending on the design window set by the technology- and the circuit application- requirements. Commonly, the ESD design library does not provide devices optimized for each circuit application or specific customers' demands. To address this limitation, structures are investigated by building matrices of test devices such as the one shown in

Figure 2.2 [94]. In this case, a well defined experimental matrix of devices can provide insights about possible solutions and failure limits, but it may also result in useless results.

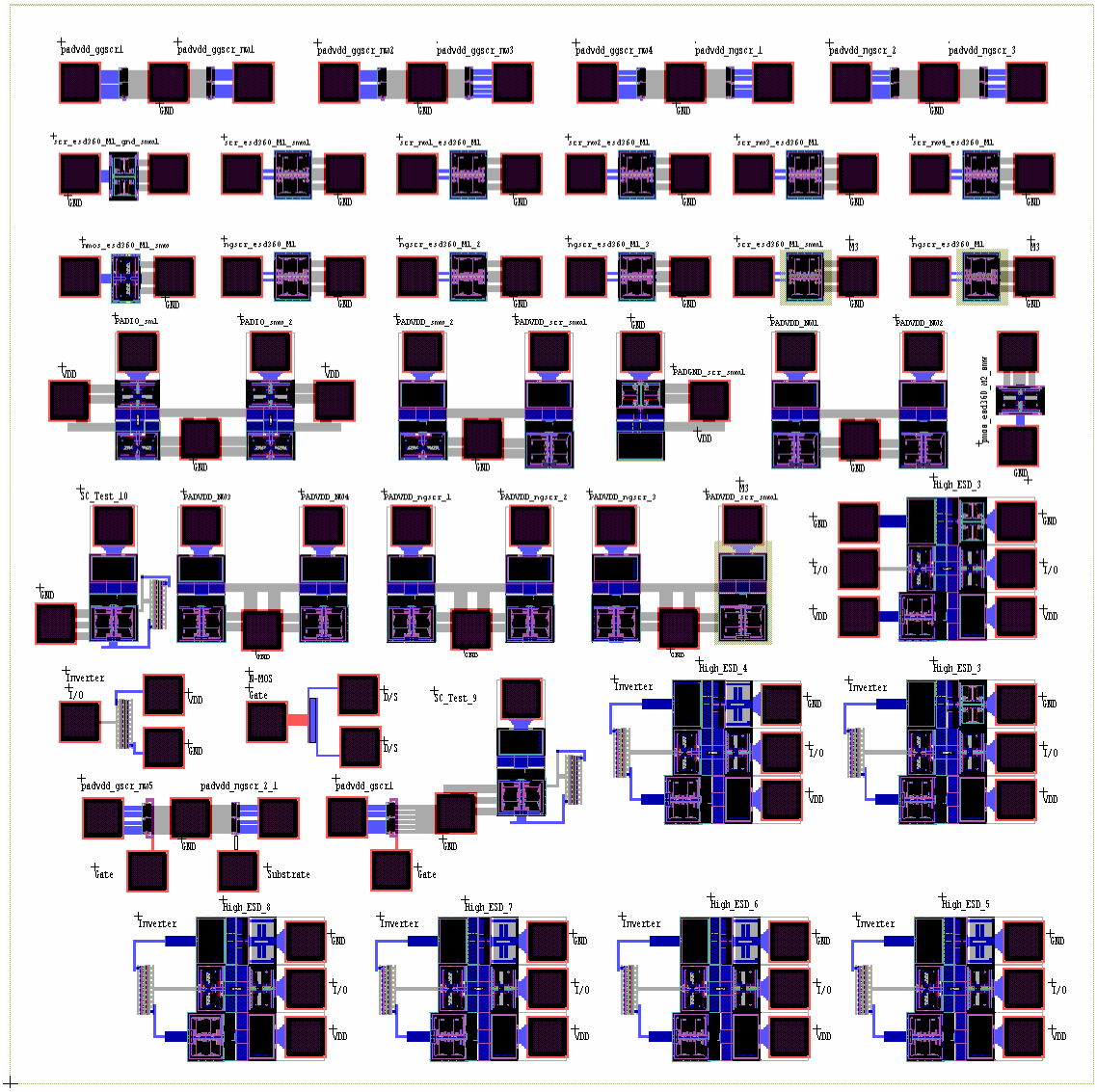


Figure 2.2. Layout top-view of an ESD experimental matrix.

Considering the elevated cost of processing and the necessary time for testing, a purely experimental approach for the design of ESD devices is accompanied by some disadvantages [97]. The uncertainty and drawbacks of the experimental approach lead to the search of alternative ways to obtain relevant design information. As it is described in the next section,

TCAD simulations can play an important role in reducing the uncertainty of the experimental approach trial-and-error characteristic, and thus support ESD protection design and expedite the development time.

2.2. ESD Protection Design Based on TCAD Simulations and Measurements

The use of TCAD tools for process assessment, or to gain insights about the performance of device structures without the need of costly fabrication runs, is vital to lead innovations and new developments. Even though this premise is followed in different areas of technology development, it is still not the case when it comes to the use of TCAD for ESD protection design and evaluation. The most common practice is to achieve ESD robust IC design by destructive testing and physical failure analysis (FA).

The design of ESD protection structures using TCAD simulation tools is a systematic method to evaluate in the pre-silicon phase 1) device's I-V characteristics, and 2) critical physical properties, such as current density, electric field, temperature distribution, and impact ionization rate, which are properties that cannot be directly assessed experimentally. Nowadays, there are different industry-standard TCAD tools that may provide different sets of models, numerical methods and flexibility to accomplish the simulation. In general, the TCAD device simulator uses a set of discrete fundamental equations, which correlate the electrostatic potential and carrier density within a finite element grid. In this study, the set of TCAD simulation and visualization tools are from Silvaco [7]-[8], [117].

TCAD-assisted ESD design is affected by the limitation in predictability of the TCAD tool, as well as in the measurement setups necessary to realize reliable calibration of the simulation. On the other hand, electro-dynamics, solid-state physics, and thermodynamics models are also

necessary in the simulation environment, resulting in complex differential equations systems for which a general solution is not possible. Instead, a discretization with a finite number of elements is used, and solutions are approximated by stable numerical solvers [7]. As a result, the mesh size, number of grid points, convergence and approximations establish a tradeoff in the utilization of the TCAD tool for ESD design. In the next sections and chapters, different methods are presented based on steady-state and transient simulations of the ESD device to assist in the design of custom protection structures, regardless of the complexity of the device structures or intrinsic limitations previously pointed out.

Figure 2.3 shows a flow diagram for a TCAD-guided ESD design, which also incorporates a reduced number of fabrication experiments. The TCAD methodology starts from the definition of the simulation environment, including: 1) process characterization, 2) simulation/calibration of the technology, 3) selection/calibration of the models for the device simulation, 4) simulation of the custom ESD protection device, 5) layout and fabrication, and 6) TCAD-assisted redesign. During the calibration, the focus of attention lies on the choice of physical models and appropriate parameters, which are obtained by fitting the measurement results. Calibration of the process simulation can be accomplished by defining the detailed flow of the technology, or by analytically approaching the different doping and isolating regions defined in the process. Figure 2.4 shows the cross-sectional view of a structure generated in one of the fabrication processes utilized in this study, using the simulation of the actual fabrication process. A sample cut-line of the doping profile for one of the regions in Figure 2.4 is shown in Figure 2.5, where the approximate analytically-generated doping profile is compared to the one obtained from the process simulation. In this case, the analytical simulation closely resembles the results of the process simulation and actual data measured via SIMS [21]. Different alternative methods can be

used for gathering information about the cross-sections [115], doping distributions and isolations characteristics [30], [38], [48], [58], [117]. This information can be subsequently utilized to define the input deck of the TCAD environment, even for those cases where foundry processes are being used and the process information is not available.

2.2.1. Physical Models Incorporated in the Device Simulation

In the previous section, simulations have been included in the design flow to take the place of large numbers of process runs and layout structures, thereby the time and cost of ESD technology development can be reduced. Due to the complexity of the device structures introduced in this study for the custom design of ESD protection systems, incorporation of electrothermal numerical simulation is necessary to assess the device behavior and critical physical phenomena in the design of ESD protection devices. The set of physical models used along with the thermal equation in device simulation are described below.

The classic heat flow equation is given by:

$$\rho \cdot C \cdot \frac{\partial T}{\partial t} = H + \nabla\left(\kappa(T) \cdot \nabla T\right) \qquad 2.1$$

where ρ is the density (g/cm^3), C is the specific heat (J/g·K), κ is the thermal conductivity of the material (W/cm·K), and H is the heat generation term (W/ cm^3) [115], [118]. In the electrothermal simulation [7], the heat generation term is modeled as:

$$H = \bar{J}_n \cdot E + J_p \cdot E + H_{GR} \qquad 2.2$$

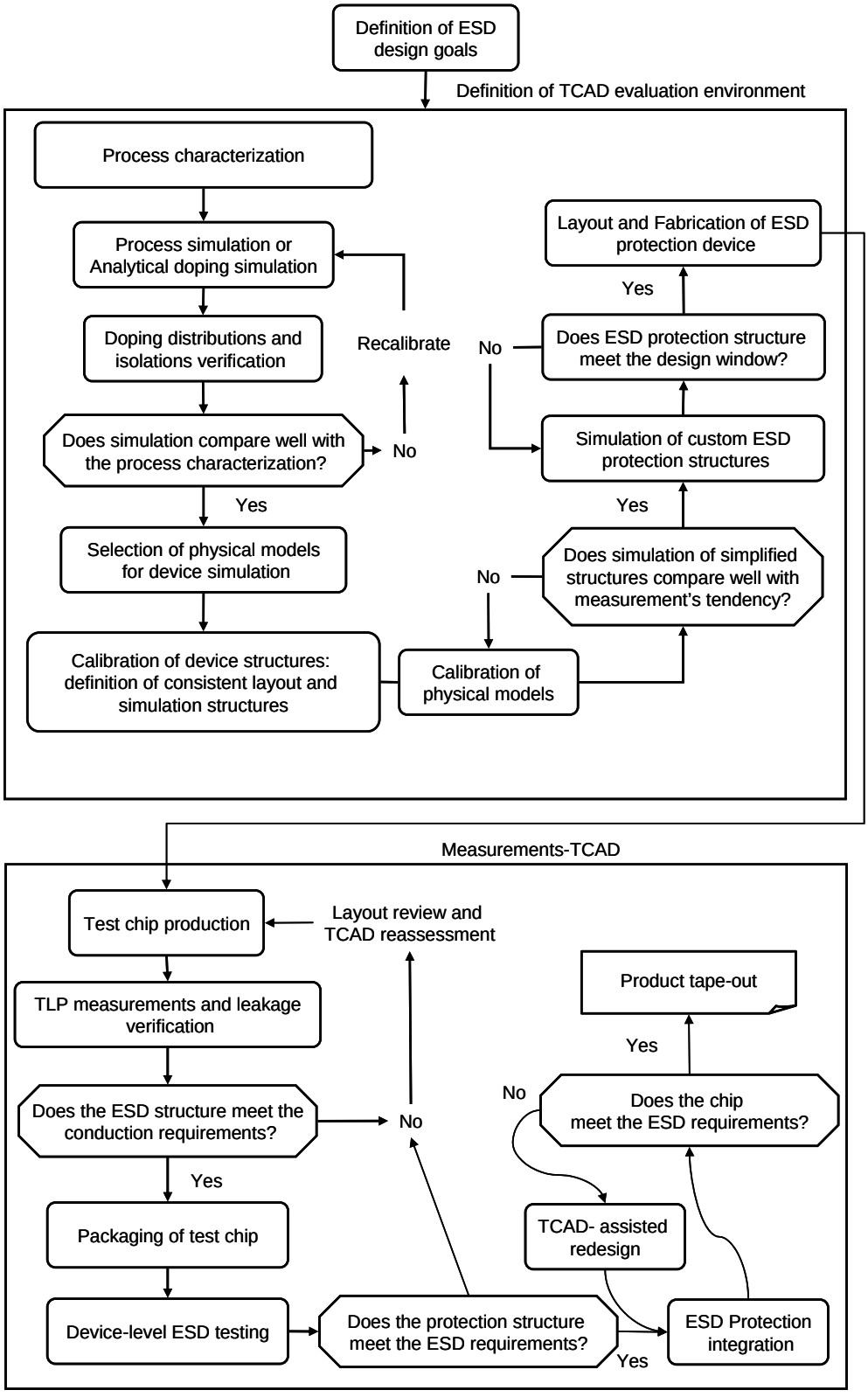


Figure 2.3. TCAD-guided ESD design.

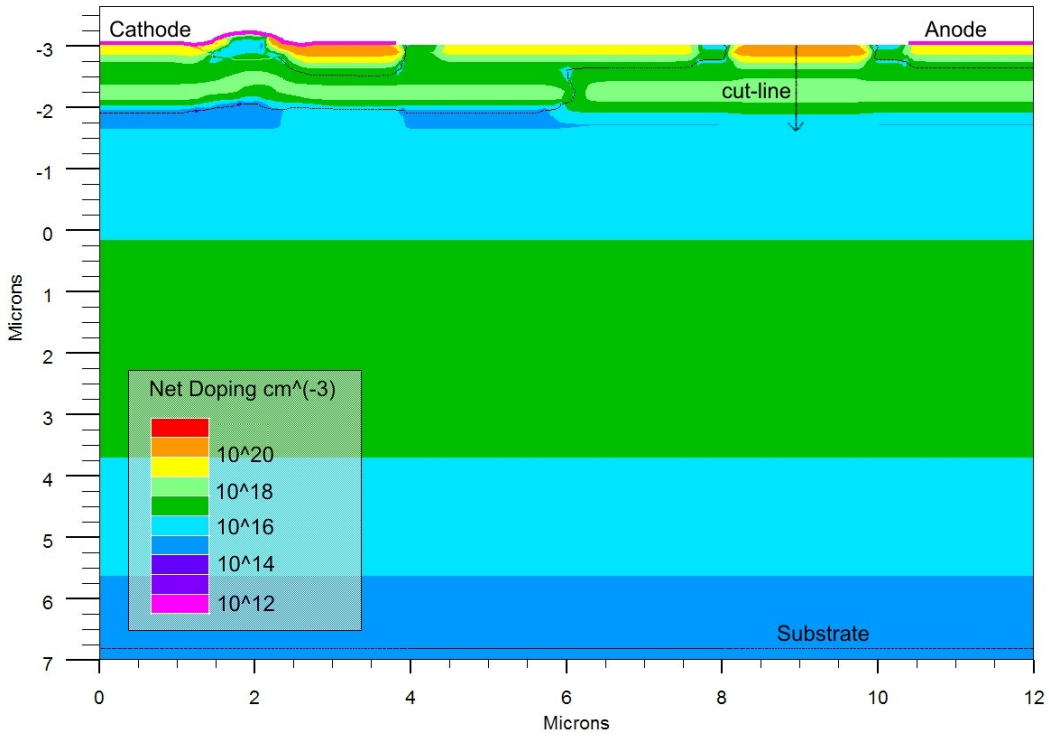


Figure 2.4. 2D Cross-sectional view of a custom ESD device generated using a process simulation.

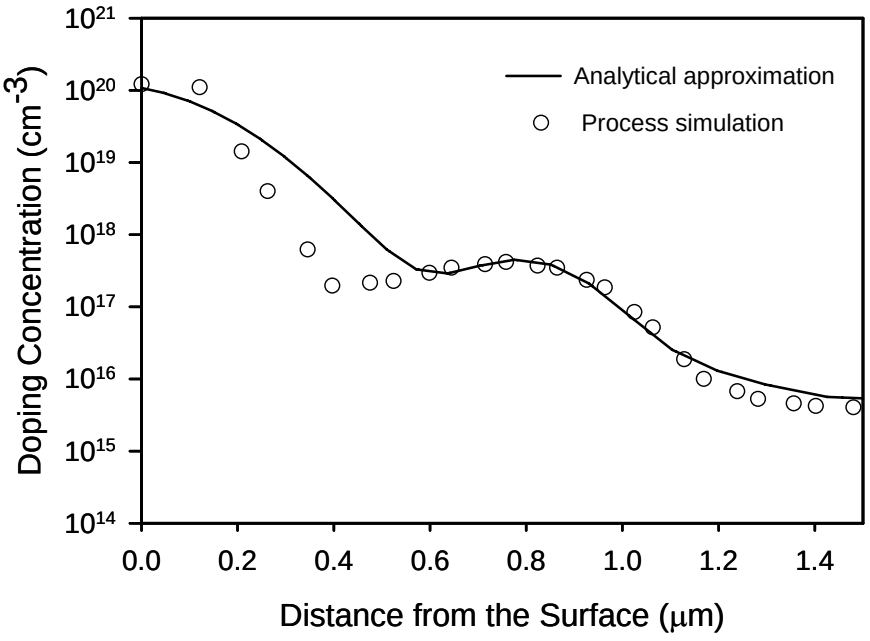


Figure 2.5. Example of N-well doping distribution generated analytically and via process simulation.

where $\bar{J}_n$, $\bar{J}_p$ are electron and hole current densities, E is the electric field, and H_{GR} is the generation recombination contribution expressed by:

$$H_{GR} = -GR \cdot E_g \tag{2.3}$$

where GR is the generation-recombination rate, which will be presented later, and E_g is the bandgap. Related to the bandgap definition, the simulation also incorporates the standard set of equations associated with the theory of carrier statistics, i.e., Fermic-Dirac/Boltzmann- statistics, effective density of states, intrinsic carrier concentration, and the bandgap narrowing [7].

The Poisson Equation

This equation is derived from Maxwell's equations and relates the space charge density to the electrostatic potential. Since the lattice temperature is no longer spatially constant [14], the Poisson equation is written as:

$$\nabla \cdot \nabla(\Psi - \theta) = -\frac{q}{\varepsilon(\bar{r})} \cdot \rho(x) - \rho_f = -\frac{q}{\varepsilon(\bar{r})} \cdot \left(p(x) - n(x) + N_D{}^+ - N_A{}^-\right) - \rho_f \tag{2.4}$$

where q is the electron elementary charge, $\varepsilon(\bar{r})$ is the permittivity of the material, Ψ is the electrostatic potential, the electric field relates to the electrostatic potential through $\bar{E} = -\nabla\Psi$, $n(x)$ and $p(x)$ are electron and hole densities, $N_D{}^+ - N_A{}^-$ corresponds to the net ionized impurity concentration, ρ_f .the fix charge density, and θ the band structure parameter given by:

$$\theta = \chi + \frac{E_g}{2q} + \frac{kT}{2q}\ln\left(\frac{N_C}{N_V}\right) \tag{2.5}$$

where χ is the electron affinity, *k* is Boltzman's constant, *T* is the local lattice temperature, and N_C and N_V are the conduction band and valence band density of states.

The Continuity Equation

This equation states the net conservation of charge principle in any possible volume of the semiconductor:

$$\frac{\partial n}{\partial t} = GR + \frac{1}{q}\nabla \cdot \bar{J}_n \qquad 2.6$$

$$\frac{\partial p}{\partial t} = GR + \frac{1}{q}\nabla \cdot \bar{J}_p \qquad 2.7$$

where *GR* represents the net generation/recombination rate. The parameters of the generation/recombination rate are also temperature dependent [7]. It can be expressed as:

$$GR = G - R_{SRH} + R_{AUG} \qquad 2.8$$

where *G* is the generation rate mainly dominated by impact ionization, and it is modeled by:

$$G = \frac{1}{q}\left(\alpha_n \bar{J}_n + \alpha_p \bar{J}_p\right) \qquad 2.9$$

in which α_n and α_p are the electron and hole ionization rates. To describe the dependence of the ionization rate on field and temperature, the simulation incorporates the model proposed by Selberherr [95]. R_{SRH} and R_{AUG} are the Shockley-Read-Hall- and Auger- recombination rates, respectively. These recombination rates are described by the general equations:

$$R_{SRH} = \frac{np - n_i^{\,2}}{\tau_p\left(n + n_1\right) + \tau_n\left(p + p_1\right)} \qquad 2.10$$

$$R_{AUG} = \left(C_n n + C_p p\right)\left(np - n_i^{\,2}\right) \qquad 2.11$$

where τ_n and τ_p are minority electron and hole lifetimes, n_i is the intrinsic concentration, n_1 and p_1 constants defined by the n/p concentrations associated to the trap level, and C_n, C_p are constant parameters. Additionally, the Shockley-Read-Hall recombination also incorporates the concentration dependent lifetime models as described in [7].

Current Density Equations

These equations describe the transport of charge. To consider changes in the spatial lattice temperature, additional thermal-diffusion terms are placed in the current density equations [14], [37]:

$$\bar{J}_n = qn\mu_n E + k\mu_n\left(T\bar{\nabla}n + n\bar{\nabla}T\right) \qquad 2.12$$

$$\bar{J}_p = qp\mu_p E - k\mu_p\left(T\bar{\nabla}p + p\bar{\nabla}T\right) \qquad 2.13$$

where μ_n and μ_p are the electron- and hole- mobility, respectively.

Mobility

The electron- and hole- mobility model incorporated in the simulation [63] considers the doping, temperature, parallel electric field and perpendicular electric field effects. In this mobility model, the field-, doping-, and temperature- dependent part of the mobility are represented by three components that are combined using the Mathiessen's rule:

$$\mu_T^{-1} = \mu_{SR}^{-1} + \mu_{AP}^{-1} + \mu_{OIP}^{-1} \qquad 2.14$$

where μ_{SR} accounts for the surface roughness scattering, μ_{AP} accounts for the acoustical-phonon scattering, and μ_{OIP} accounts for the optical inter-valley phonons scattering. These mobility terms are functions of different parameters, i.e., μ_{SR} is a function of the doping and electric field, μ_{AP} is a function of the doping, electric field and temperature, while μ_{OIP} is a function of the temperature and electric field [7]. In the case of a high electric field, the velocity saturates and the Caughey-Thomas expression is used to provide smooth transition between low-field and high field behavior [15]:

$$\mu_{n,p} = \mu_{Ln,p} \cdot \left(1 + \left(\frac{1}{1 + \left(\frac{\mu_{Ln,p} \cdot E'}{v_{sat}} \right)^{\beta}} \right) \right)^{\beta^{-1}} \qquad 2.15$$

where $\mu_{Ln,p}$ is the low field mobility, β is a fitting parameter, commonly 1 for electrons and 2 for holes, and *E'* is the electric field in the direction of the current flow. This mobility model is implicitly dependent on the lattice temperature *T* (K) through the temperature-dependent saturation velocity [7]:

$$v_{sat} = \frac{2.4 \cdot 10^7}{1 + 0.8 \cdot \exp\left(\frac{T}{600} \right)}. \qquad 2.16$$

The two-dimensional (2D) process and device simulators [7]-[8], [117] allow the user to create a 2D (two dimensional) cross-section of a semiconductor device, including definition of

silicon and oxide regions, doping profiles, and electrodes, and then simulate the I-V characteristics of the device. Coefficients for various mobility models, impact-ionization models, and material parameters can be slightly adjusted to calibrate simulations to experimental data, but even non-calibrated simulations can offer the necessary qualitative understanding and tendencies in the device performance with changes in the structure. The numerical analysis using the previous set of physical models, allows the user to examine many physical properties at all the locations in the ESD device for any simulated I-V point and thermal border condition.

2.2.2. Steady-State and Transient Simulation

In addition to predicting I-V curves, simulations can identify the point of device failure by monitoring the electric field, temperature, and other properties throughout the device. Transient simulations can be used to approach tests such as the human-body model, charged-device model, and transmission-line pulsing, by using simplified waveforms (see Figure 2.6), while steady-state I-V sweeps are useful in predicting junction breakdown voltages, or even S-type I-V characteristics of ESD protection devices.

A curve-tracing technique is used to automate the steady-state simulation of complex I-V curves. Automation of complex simulations, such as latchup or snapback, saves the time and effort needed to manually change simulation boundary conditions any time there is a sharp turn in the I-V curve. This algorithm is discussed in chapter 5. Figure 2.7 shows a schematic example of the simulation setup, and example I-V steady-state simulation results for one of the devices studied in this work. The 2D contours of lattice temperature, conduction current density and impact generation rate at the two points indicated in Figure 2.7(b) are depicted in Figure 2.8. In this case, the snapback characteristics are predicted, along with the changes in the 2D contours at different operating conditions. Similar contours can be obtained for the other physical parameters

of the device previously discussed, and tendencies with changes in the device cross-section can be evaluated. Examples of TCAD input decks implemented in this study are provided in the Appendix.

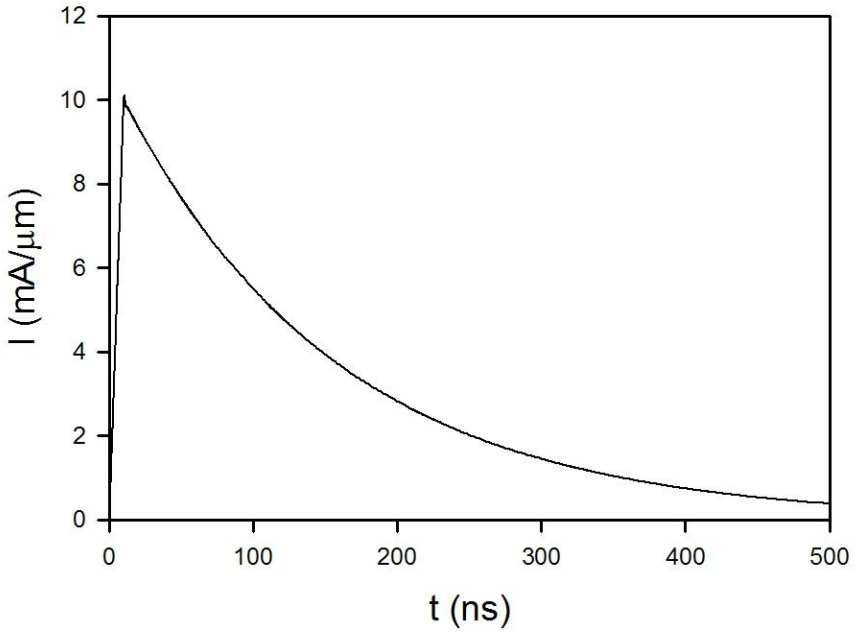
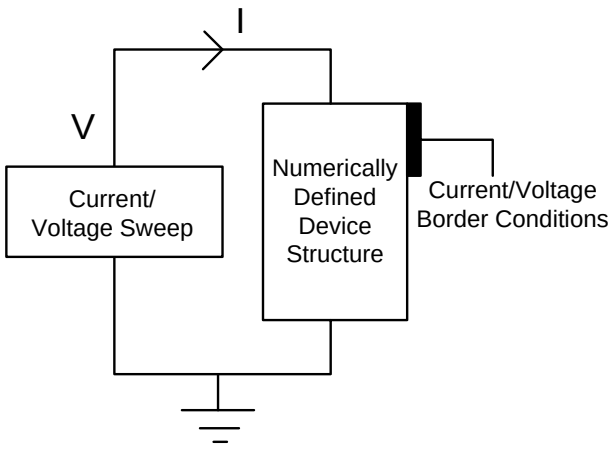
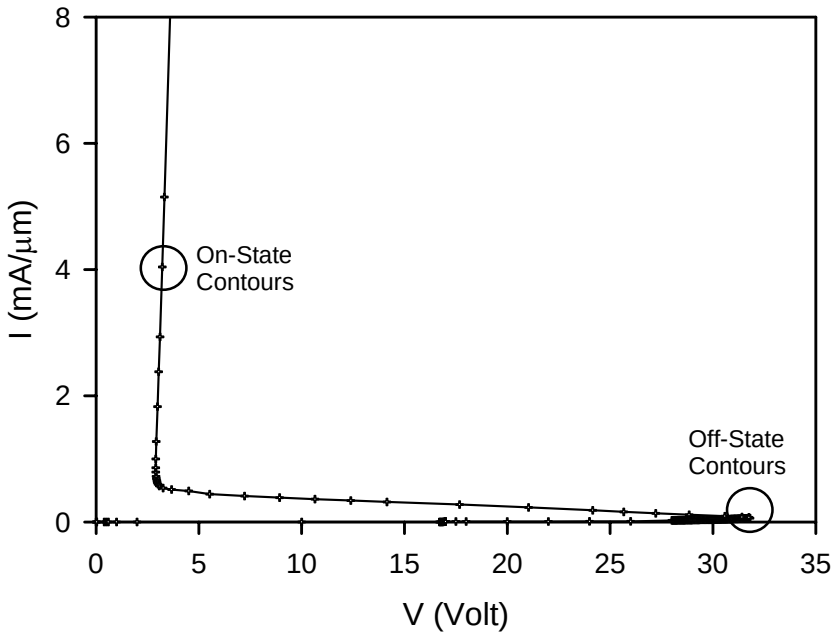


Figure 2.6. TCAD-simulated transient waveform using 10 ns rise time and 150 ns decay time. This is the approximate transient characteristic of an HBM event.

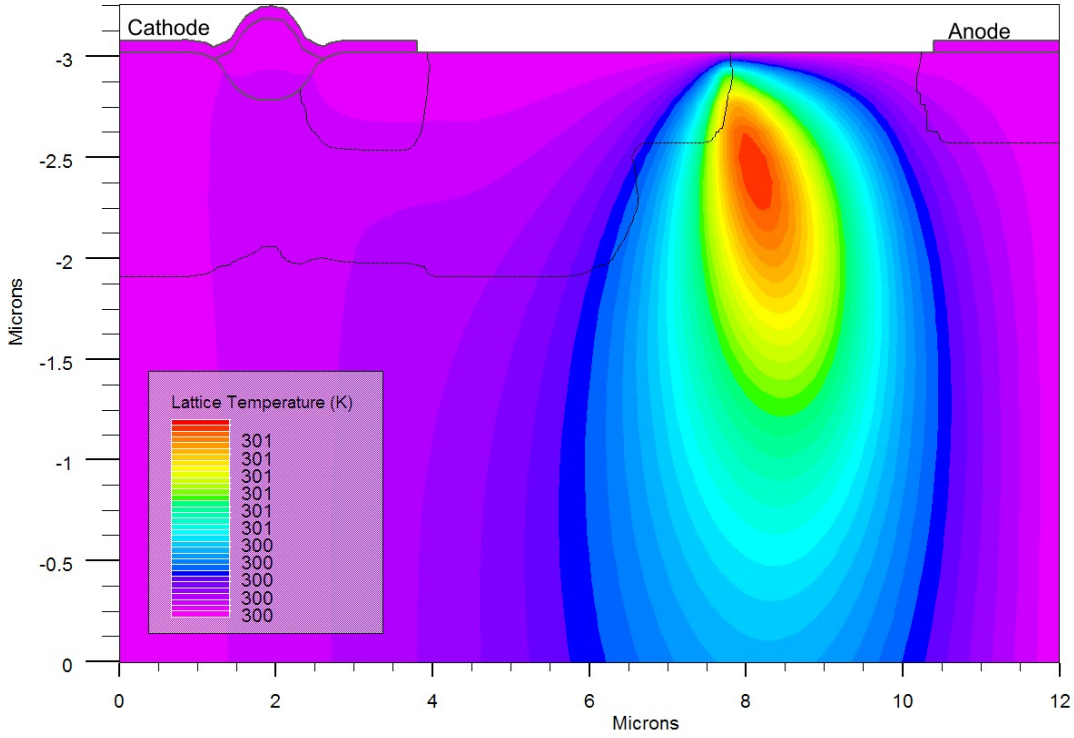


(a)

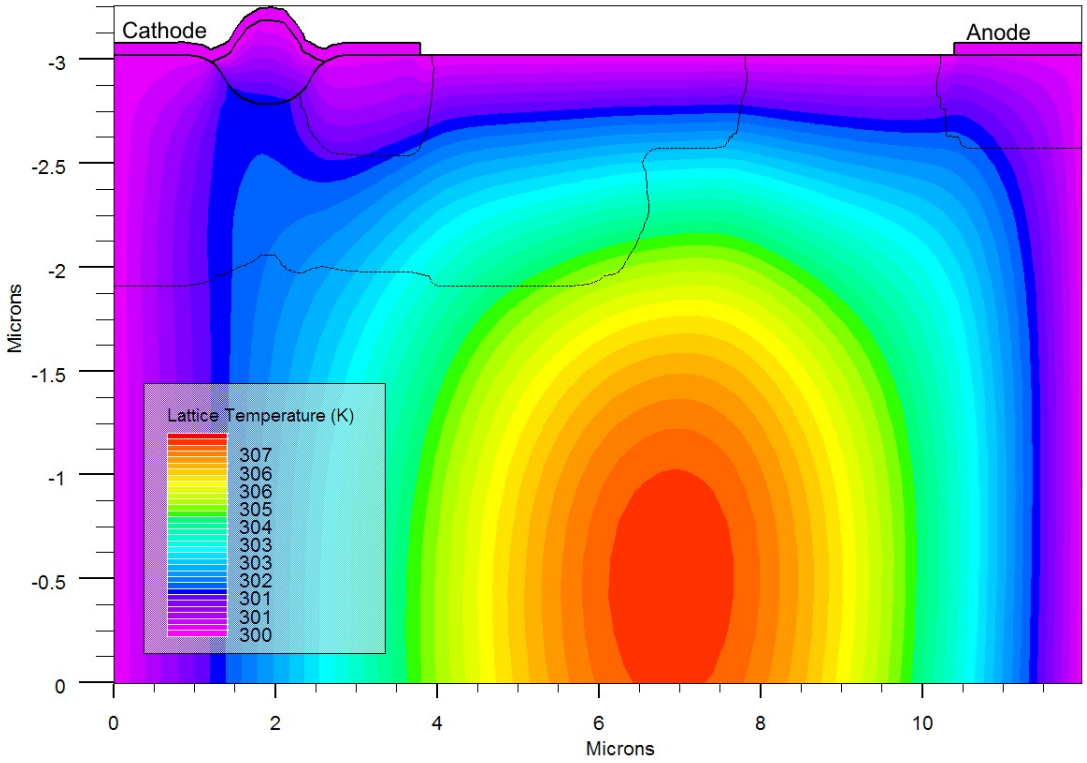


(b)

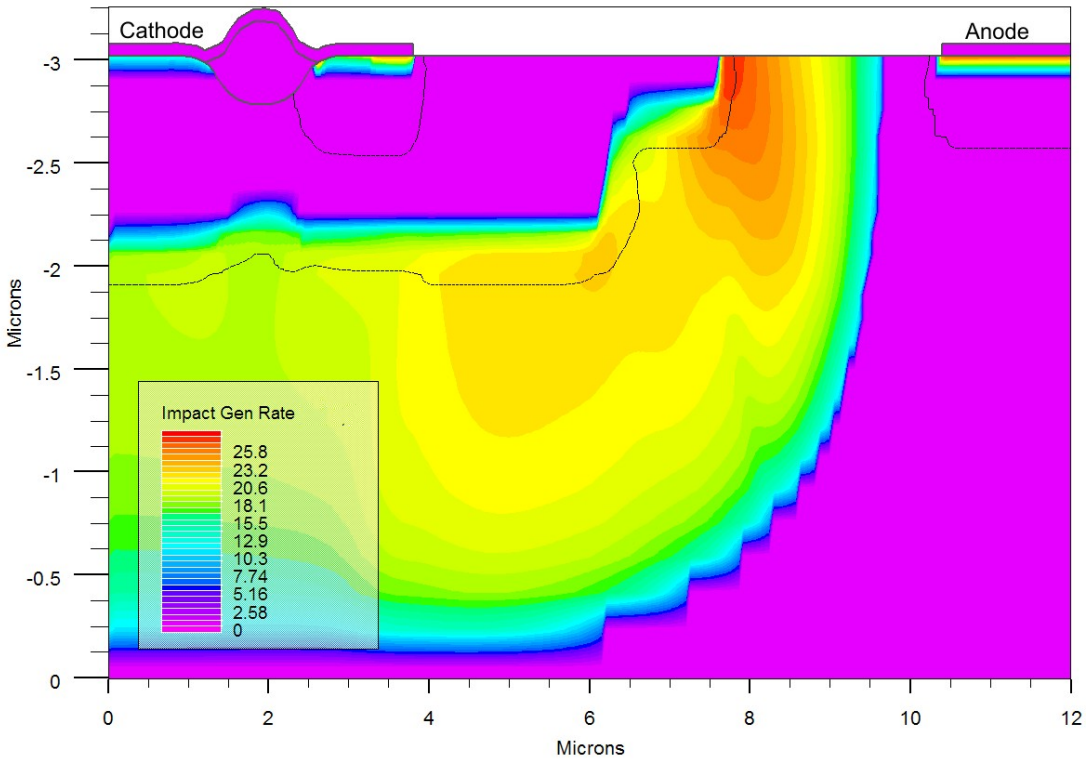
Figure 2.7. (a) General schematic of the device simulation, and (b) example of simulated S-type I-V characteristics and points where contours are taken.



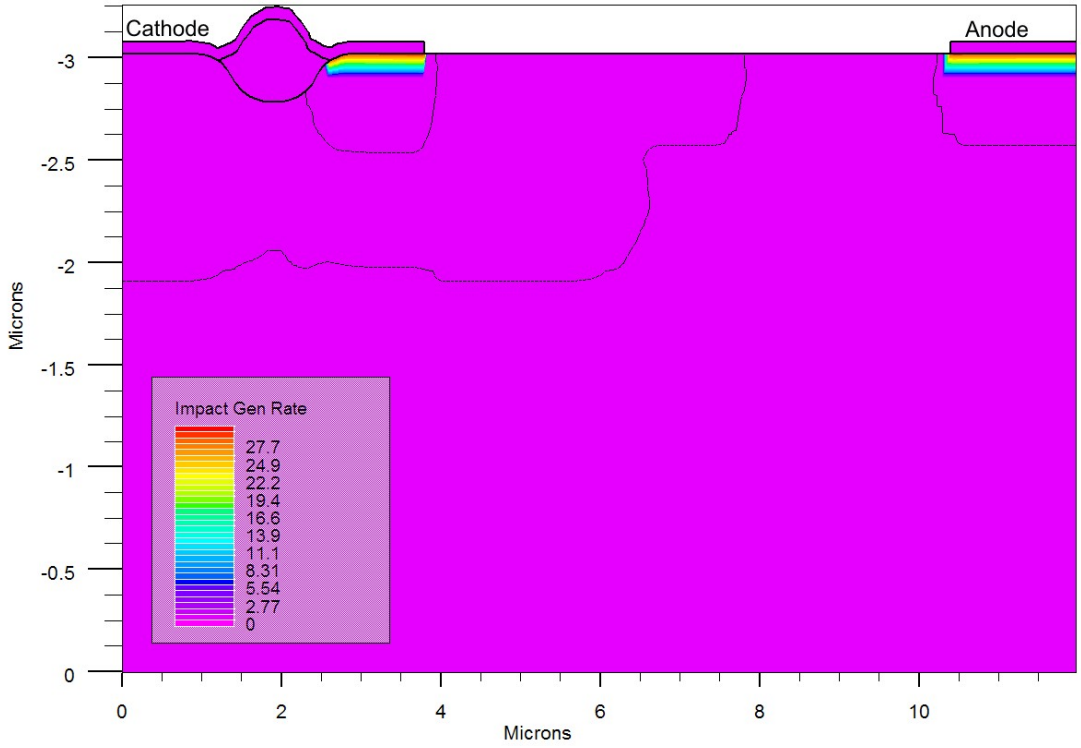
a) Off-state



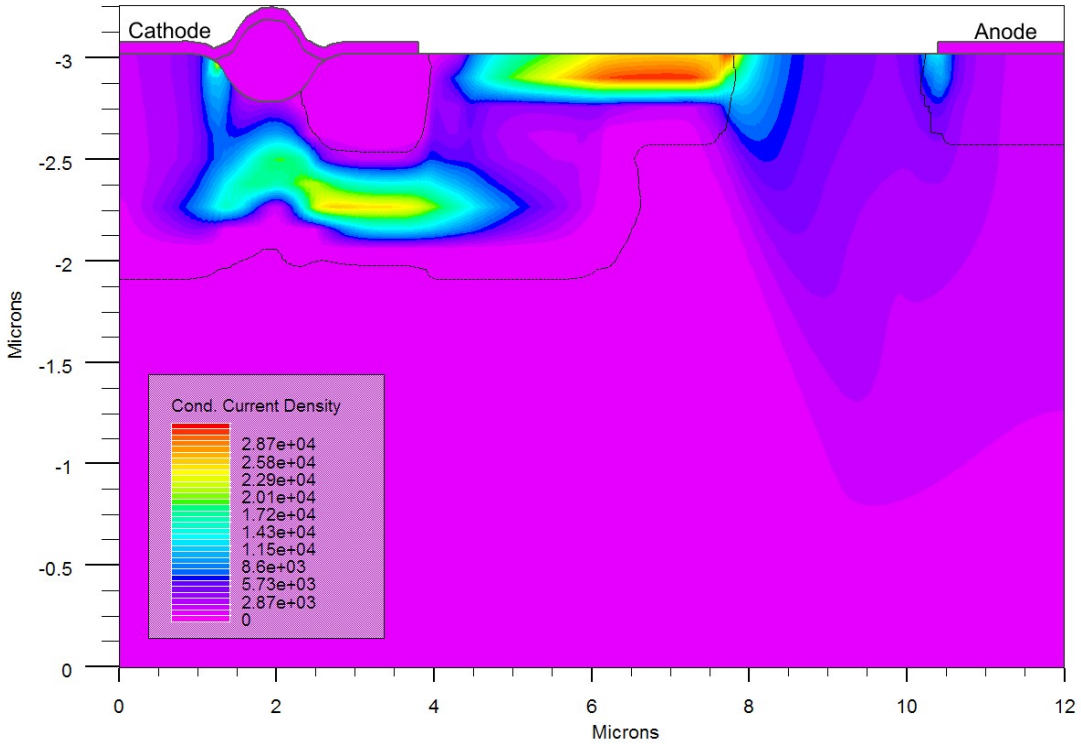
a) On-state



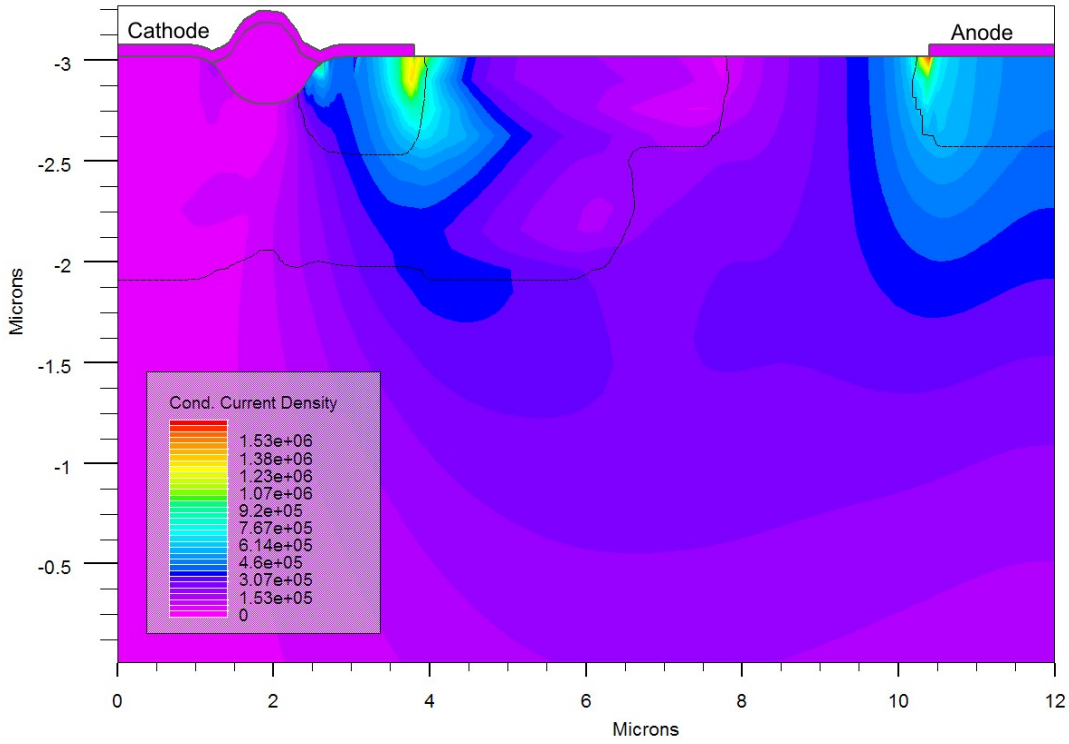
b) Off-state



b) On-state



c) Off-state



c) On-state

Figure 2.8. Comparison of on- and off-state 2D current density contours of (a) lattice temperature in (K), (b) impact generation rate (10 ^ (number in the contour) $s^{-1}cm^{-3}$), and (c) current density (A/cm).

The contours shown in Figure 2.8 give important insights that are used along this study in the implementation of tailored ESD devices. For instance, the lattice temperature contour shows the optimum location for the hot spot deep in the device during the on-state. Likewise, the current density evolves from a narrow conduction area, when the device is operating close to the trigger point, to a well-spread conduction along the device during the on-state. Additionally, the impact generation rate gives results that can be used for calibrating the trigger voltage (chapter 5).

The time required for the transient simulation previously described can be considerably more than that required for the steady state simulations. However, in the transient simulation the device response can be also evaluated and optimized at different rise-times, which can be useful when designing for protection against CDM.

2.2.3. Mixed-Mode Simulation

The TCAD mixed-mode simulation creates the capability of embedding one or more numerically simulated devices in a SPICE-like circuit that may include lumped resistors, capacitors, and inductors as well as voltage sources, current sources, and compact models for diodes, MOSFETs, or BJTs. The total circuit is normally solved in a coupled manner, in which the semiconductor equations previously discussed are still incorporated in the simulation of the 2D devices, as well as the current and voltage Kirchhoff circuit equations given below:

$$\sum_{x=1}^{m} i_x = 0\,,\ m = \text{ number of paths converging in one node,} \qquad 2.17$$

$$\sum_{y=1}^{n} v_y = 0\,,\ n = \text{ number of branches in a close loop.} \qquad 2.18$$

Mixed-mode simulations can be used for transient characterization of ESD tests, such as the ESD standards discussed in chapter 1. This type of simulation can also be used to generate the I-V points of the snapback curve typically obtained in ESD protection devices. Figure 2.9 shows a schematic representation of a mixed-mode simulation incorporating a numerically-described ESD protection device and the simplified equivalent circuit previously shown in Figure 1.2.

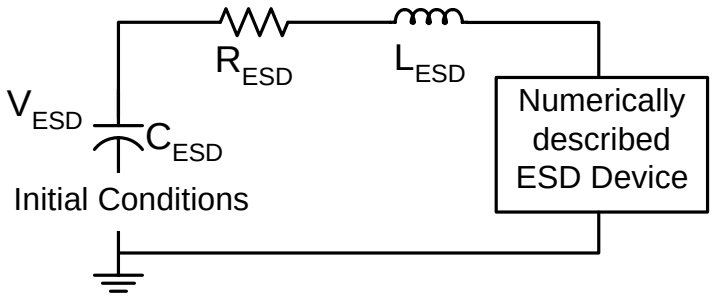


Figure 2.9. Schematic representation of mixed-mode simulation using simplified ESD model lumped circuit and numerically-simulated device.

Applications of the mixed mode simulation have been demonstrated for assessing the I-V characteristics, and device performance, under events closer to those obtained from the actual ESD tester. This type of simulation, however, is time consuming and convergence problems are difficult to solve when the device structure is complex. Thus, even though for some analysis mixed-mode simulation it may be necessary in the assessment of ESD protection designs, there are intrinsic limitations regardless of the approach that is followed. Therefore, reevaluation of the TCAD strategy is also necessary for selecting the most efficient way to obtain the information.

2.3. Chapter Remarks

Two methods to design ESD protection structures have been discussed. The first ESD design method follows an experimental approach, in which design requirements are obtained via fabrication, testing and failure analysis. This design method is time consuming and expensive, but systematic test matrices designs and testing procedures can improve the predictability of the experimental approach. The second method consists of the TCAD-assisted ESD protection design. This method incorporates key numerical simulations in different stages of the ESD design process in order to provide less expensive and even more predictable and systematic ESD development strategies. These methodologies are used as design guidelines and will be applied in the following chapters to develop custom ESD protection components. Physical models incorporated in the device simulation were identified and discussed. These models will be considered in the TCAD simulations accomplished in the subsequent study. Different simulation strategies that can be followed in order to obtain meaningful results were revised, as well as methods to relax the complexity of the device simulations.

CHAPTER 3
DESIGN AND INTEGRATION OF HH-LVTSCR DEVICES FOR ESD PROTECTION IN CMOS/BICMOS TECHNOLOGIES

This chapter presents an approach to the design of ESD protection devices, which can be customized for circuits operating at relatively low voltage range, e.g., digital- or mixed-signal-applications. The quest of optimum design and integration of the ESD protection components for different technologies has led to the introduction of custom thyristor-based structures, such as those discussed in references [9], [18], [23], [49]-[53], [55]-[56], [66], [72]-[73], [75], [87]-[90], [105], [108], [120]. The S-type current-voltage (I-V) characteristics of thyristor- or silicon controlled rectifier (SCR)-based structures allow for the ESD protection device to remain off in the normal IC operation, and switch to a low voltage/high current condition during the ESD stress (on-state). In the on-state, the SCR device can bypass a significant ESD current per unit area, but it can also induce latchup if the IC operating voltage/current sustains the on-state condition in the protection structure after the ESD has passed.

Different SCR-based structures and circuits have been reported in other studies to address the problem of adjusting the trigger and holding voltages and conducting currents for ESD protection without latchup problems, e.g., references [18], [52]-[56], [67], [72]-[73], [108]. Nonetheless, these solutions are only applicable for specific technologies and are insufficiently robust for protecting against a relatively high ESD stress.

The concept of a novel and robust ESD device called the High-Holding Low-Voltage-Trigger Silicon Controlled Rectifier (HH-LVTSCR) developed in this study has been discussed in references [82], [87]-[88], and [90]. In this chapter, a detailed and comprehensive design and

characterization of HH-LVTSCRs is presented. Specifically, experimental n- and p-type HH-LVTSCRs are fabricated and measured, and their ESD performances are compared for different operating conditions. Effective dual-polarity ESD protection solutions for over 2 kV MM (machine model) and over 15 kV, as described by the ESD standard IEC 1000-4-2 [45], are also accomplished by using HH-LVTSCRs with a multifinger layout for optimal ESD scaling.

3.1. Structures and Terminal Connections

Figure 3.1 and Figure 3.2 depict the cross-sectional views of the n- and p-type HH-LVTSCR, respectively. The design of the HH-LVTSCRs is first accomplished in the pre-silicon phase using TCAD simulations of the device's fabrication process and I-V characteristics [7]-[8]. The device simulations allow for the estimation of the junction breakdowns, current distributions, and hot spots during the ESD stress, see chapter 2. Devices are then fabricated and measured to verify the ESD protection requirements with no latchup problems at different operating voltages.

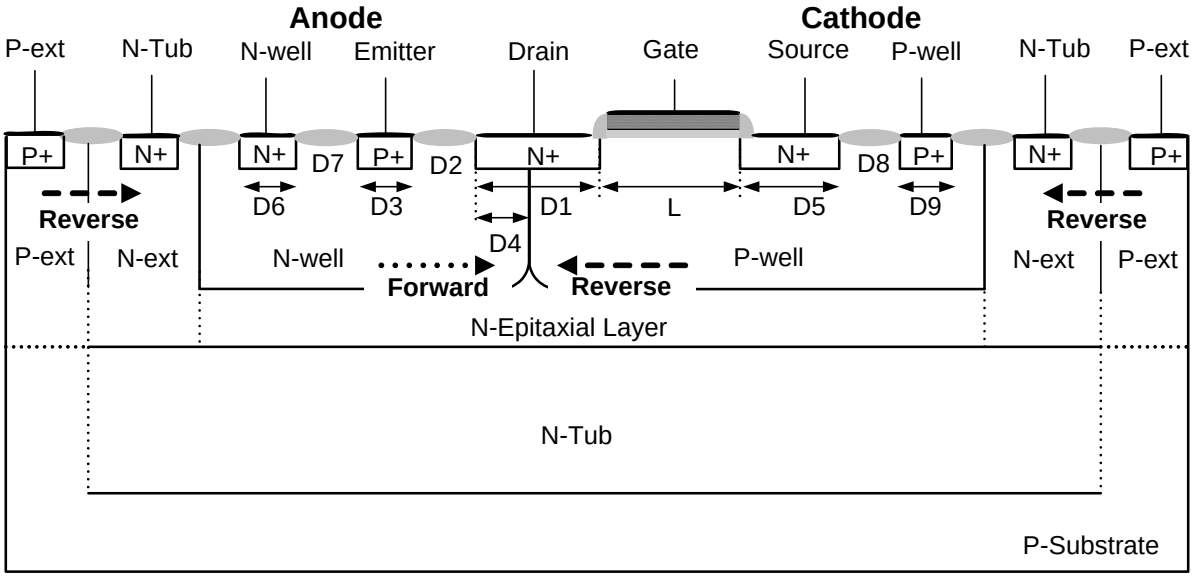


Figure 3.1. Cross-sectional view of the n-type HH-LVTSCR

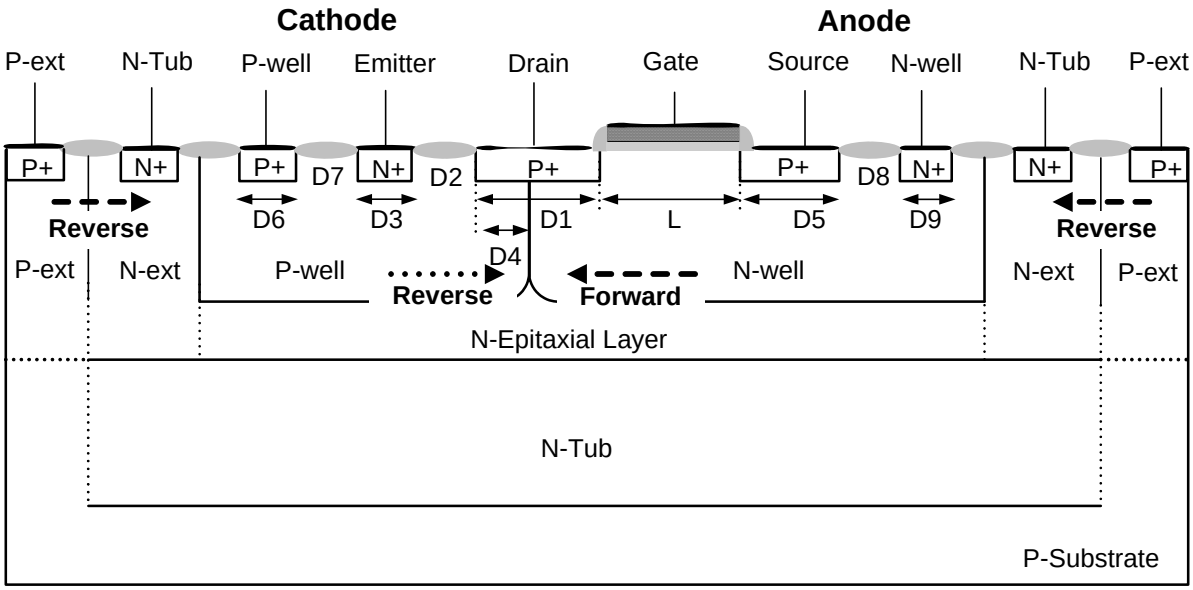


Figure 3.2. Cross-sectional view of the p-type HH-LVTSCR

The HH-LVTSCRs are developed in complementary n- and p-type versions using a silicided submicron triple-well BiCMOS technology. However, implementation of these devices can be extended as well to triple- or twin-well CMOS technologies within the scope of the technology constraints and specific application requirements. Moreover, the following two different terminal connections can be realized: 1) HH-LVTSCR with N-Tub connected, and 2) HH-LVTSCR with N-Tub open. These different connections result in substantially different cathode to anode reverse I-V characteristics of the HH-LVTSCR. The discussion below focuses on the n-type HH-LVTSCR, and the same concept applies to the p-type HH-LVTSCR.

3.1.1. HH-LVTSCR with N-Tub Connected

The N-Tub and N-well on the anode side form a p/n junction which can change the conduction characteristics of the device depending on the external interconnections. When the anode contact connects the emitter (p+ region) and the N-well (n+ region), and the cathode contact connects the gate, the source (n+ region), and the P-well, the structure is referred to as

HH-LVTSCR with N-Tub connected. A similar condition is also obtained for the p-type HH-LVTSCR shown in Figure 3.2, by connecting the gate, source (p+ region), and N-well (n+ region) to the anode, and connecting the cathode contact to the emitter (n+ region) and the P-well (p+ region).

The forward operation results when the anode voltage increases abruptly and reaches the trigger voltage. At the trigger voltage, the parasitic bipolar transistor underneath the gate turns on. High-level injection of electrons and holes takes place in the cathode and anode regions, and the laterally distributed N-well/P-well blocking junction begins to conduct. This gives rise to a condition where 1) the voltage snaps back from the trigger voltage (V_T) to the holding voltage (V_H), and 2) a low impedance current path is created in the device. The anode to cathode voltage is the addition of the voltages along the device, i.e., the voltages underneath the gate, in the N-well/P-well blocking junction, and in the distributed N-well and P-well resistances. During the on-state, the high-level injection of holes and electrons from the anode and cathode, respectively, floods the anode/cathode region with mobile charges, which results in a desirable conductivity modulation and efficient discharge of a large current.

For the reverse operating condition, the voltage at the anode is lower than that at the cathode. This forward biases the P-substrate/N-well junction, and a low-impedance conduction path is formed in the device.

3.1.2. HH-LVTSCR with N-Tub Open

When the electrodes of the N-well and the N-Tub regions are not connected to the anode contact, i.e. the anode is only connected to the emitter (p+ region) in the n-type HH-LVTSCR, or

to the source and the gate in the p-type HH-LVTSCR, the conduction mechanisms for the HH-LVTSCR in the forward and reverse conditions are considerably different.

For the forward operating condition, similar to the physical effect previously described in section 3.1.1, the concentration of holes and electrons injected from the anode (p+ region) and cathode (n+ region), respectively, are several orders of magnitude larger than the concentration of majority carriers in the P-well and N-well regions. The N-well region corresponds to the base of the lateral PNP bipolar junction transistor (BJT), and the P-well region corresponds to the base of the lateral NPN BJT. With the N-well floating and a positive voltage applied to the anode terminal (emitter of the PNP), the leakage is amplified by the current gain of the PNP BJT. This yields a lower breakdown voltage in the open base BJT and consequently reduces the trigger and holding voltages in the HH-LVTSCR. However, since the current gain of the PNP BJT is relatively small, the trigger voltage and the holding voltage do not change drastically from those of the HH-LVTSCR with N-Tub connected.

For the reverse operating condition, the anode voltage is lower than the voltage in the cathode and the P-substrate. With the N-well and the N-Tub floating, the reverse conduction is no longer taking place in the P-substrate/N-well junction, but rather is associated with the emitter-collector breakdown of the open base PNP between the outermost P-ext implantation (p-side of the guard ring) and the anode. This leads to a high-impedance conduction path and a relatively low current discharging capability in the reverse operation of the HH-LVTSCR. Thus it is expected that only destructive snapback can take place in this parasitic BJT, since the silicide junctions would have been damaged by the time the anode to cathode voltage reaches the necessary level for the onset of the snapback condition. As will be experimentally shown later, prior to the destructive snapback, the introduction of the multifinger structure in the design

allows for the HH-LVTSCR to sustain a very high current level (-2 A for 3-finger and -6 A for 5-finger) without being damaged.

3.2. Measurements and Characterization

Figure 3.3 shows the measured transmission line pulse (TLP) current-voltage (I-V) characteristics for 200 μm width, p-type HH-LVTSCRs with N-Tub -connected and -open. Notice that the two connection schemes give rise to significantly different reverse breakdown voltages and reverse conducting currents. The N-Tub open device has a larger reverse breakdown voltage, but its conducting characteristics are not suitable for ESD protection. The I-V characteristics for the forward operation, on the other hand, are less sensitive to the type of N-Tub connection.

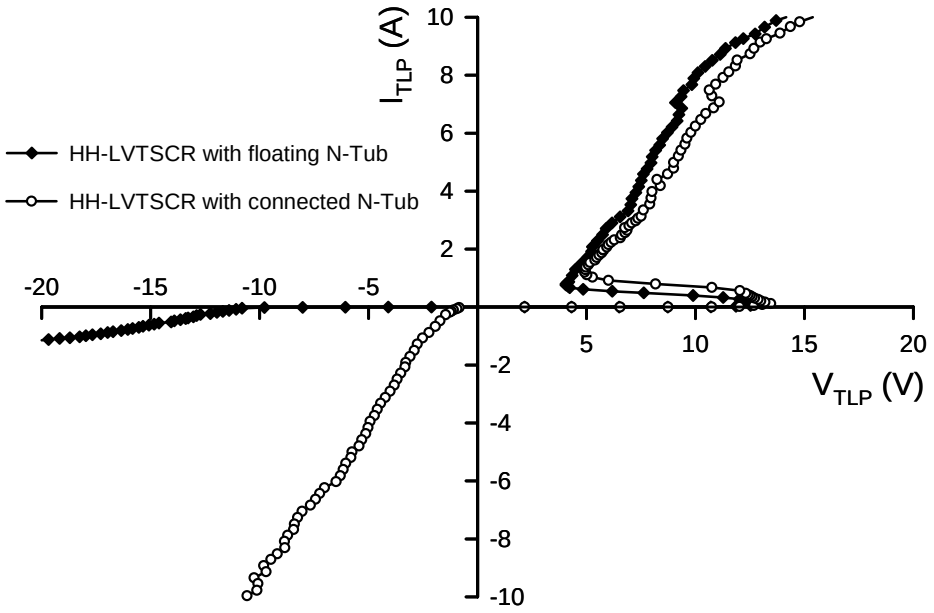


Figure 3.3. Measured TLP I-V characteristics of experimental p-type HH-LVTSCRs with N-Tub connected and floating.

In addition to the different electrode interconnections, changing the lateral dimensions allows for the adjustment of the holding voltage and trigger voltage of the HH-LVTSCR [87]-[88].

Table 3.1 (a) and Table 3.1 (b) depict specific lateral dimensions and the sustainable Human Body Model (HBM) ESD levels for different n- and p-type HH-LVTSCRs with N-Tub connected and a width of 100 μm. The dimensions not listed in the tables are kept constant in this experiment, i.e., D6 and D9 are 1.6 μm, and D2, D7 and D8 are 0.6 μm. For the p-type HH-LVTSCR, D3 and D5 are also kept constant at 1.6 μm. Evaluation using measurements and TCAD simulations showed that the S-shaped I-V characteristics of the HH-LVTSCR are affected by different internal dimensions [90], but are most sensitive to the lateral dimension D1. Notice in Table 3.1 that the ESD level is reduced with increasing anode to cathode distance [73].

Table 3.1. Lateral dimensions (in microns) of a) n-type HH-LVTSCRs, and b) p-type HH-LVTSCRs.

(a)

Name	L	D1	D3	D4	D5	HBM (kV)
N-Cell 1	7	1.6	3.2	1.6	3.2	> 8
N-Cell 2	7	3.2	1.6	1.6	1.6	> 8
N-Cell 3	7	5.1	1.6	3.2	1.6	6.0
N-Cell 4	7	7.3	1.6	3.2	1.6	5.2
N-Cell 5	7	8	1.6	4.8	1.6	4.1

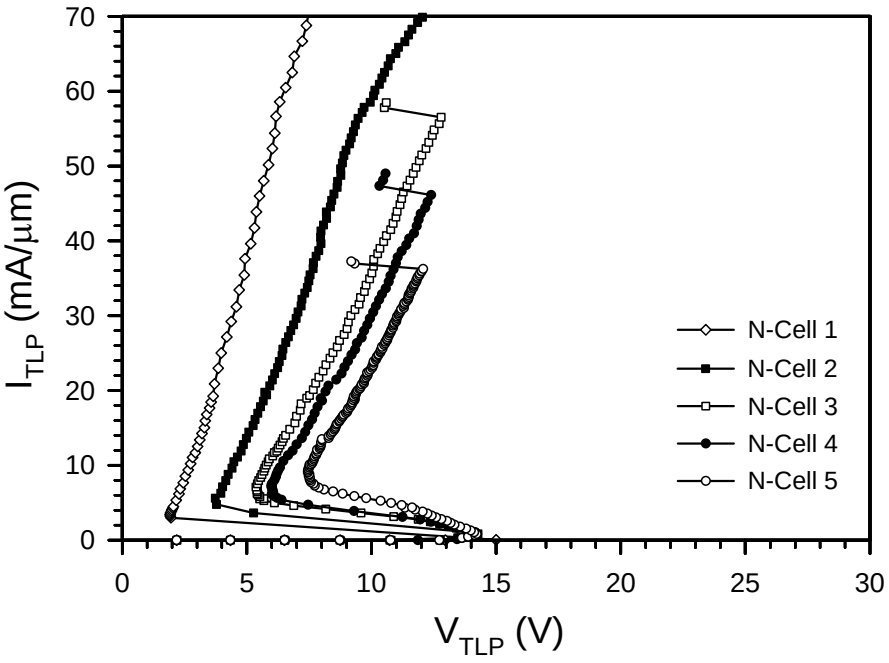
(b)

Name	L	D1	D4	HBM (kV)
P-Cell 1	0.7	3.2	1.6	> 8
P-Cell 2	3.5	3.2	1.6	> 8
P-Cell 3	7	3.2	1.6	6.5
P-Cell 4	7	4.8	3.2	5.7
P-Cell 5	7	8	4.8	5.2

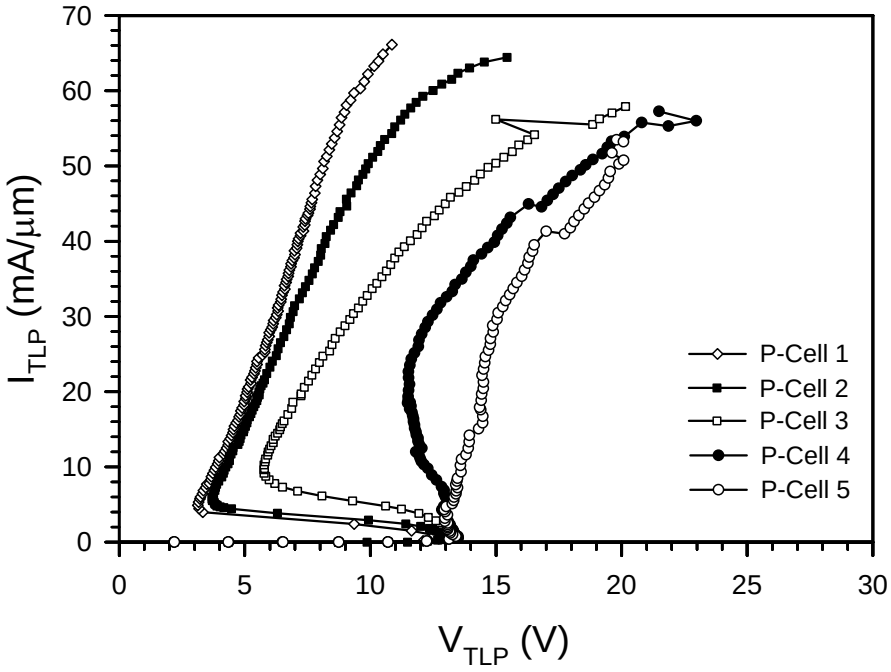
The use of n- or p-type HH-LVTSCR structures also gives flexibility in designing S-shaped I-V characteristics suitable for different ESD protection schemes. Figure 3.4 shows the anode to cathode I-V characteristics for a) the n-type HH-LVTSCR (N-cells), and b) p-type HH-LVTSCR (P-cells) listed in Table 3.1(a) and Table 3.1(b), respectively. Figure 3.4 demonstrates the shifting in the S-shaped I-V characteristics obtained by using the complementary versions of the HH-LVTSCR and adjusting the lateral dimensions. Furthermore, the ESD level versus V_H trade-off can be optimized for a given ESD protection requirement by the proper selection of the dimensions and type of HH-LVTSCR. Failure analysis conducted on these devices showed that the failure mechanism in both types of HH-LVTSCRs was silicide short paths between anode-cathode electrodes. This effect becomes more prominent when the holding voltage is increased. In the next figures, critical parameters in the HH-LVTSCRs devices for ESD design are analyzed and compared in groups of five samples per point, each of them for n- and p-type devices.

Figure 3.5 shows the holding voltage (V_H) versus the dimension D1 for the n- and p-type HH-LVTSCRs. The holding voltage in the p-type device is comparatively higher than that in the n-type device. Additional experimental results have shown that V_H higher than 8 V is hardly obtainable from the n-type HH-LVTSCR. For the case of the p-type HH-LVTSCR, however, the holding voltage can reach 11.5 V, which is close to the trigger voltage of the device. The holding voltage higher in the p-type HH-LVTSCR than in the n-type HH-LVTSCR is due to the fact that the injection efficiency, and thus the current gain, of the coupled bipolar devices in the n-type HH-LVTSCR is higher than that of the p-type HH-LVTSCR for a given D1. This is because D1, which is relatively large, is the length of the intermediate N+ region in the n-type HH-LVTSCR and corresponds to the collector of the embedded NPN. On the other hand, in the p-type HH-

LVTSCR, D1 is the length of the intermediate P+ region, and it corresponds instead to the base of the embedded NPN.



(a)



(b)

Figure 3.4. Measured TLP I-V characteristics of a) five n-type HH-LVTSCRs given in Table 3.1(a), and b) five p-type HH-LVTSCRs given in Table 3.1(b).

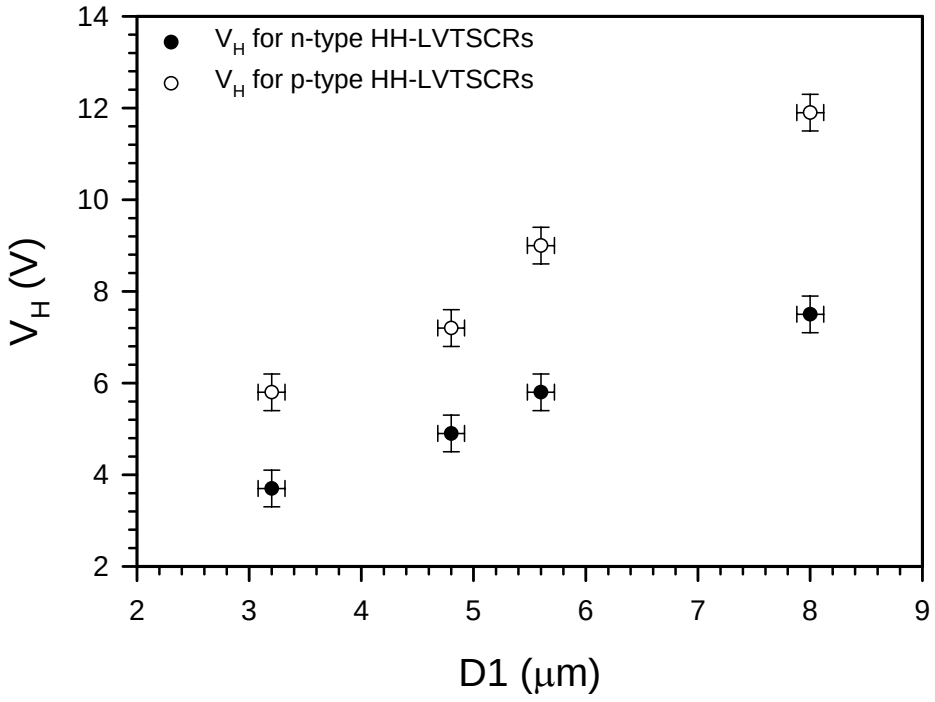


Figure 3.5. Comparison of measured holding voltage (V_H) versus dimension D1 for n- and p-type HH-LVTSCRs.

Figure 3.6 shows the trigger voltage (V_T) versus the lateral dimension D1 for the n- and p-type HH-LVTSCRs. For the n-type HH-LVTSCR, the trigger voltage increases slightly when D1 is increased. For the case of the p-type HH-LVTSCR the trigger voltage was found to be almost constant.

Figure 3.7 compares the on-state resistance (R_{ON}) versus the dimension D1 for the n- and p-type HH-LVTSCRs. This resistance represents the current discharging capability during the ESD event. For a small D1, which yields lower holding voltage, the on-state resistance for the p-type device is higher than that for the n-type device. However, as D1 increases, the R_{ON} difference of the two devices is minimal.

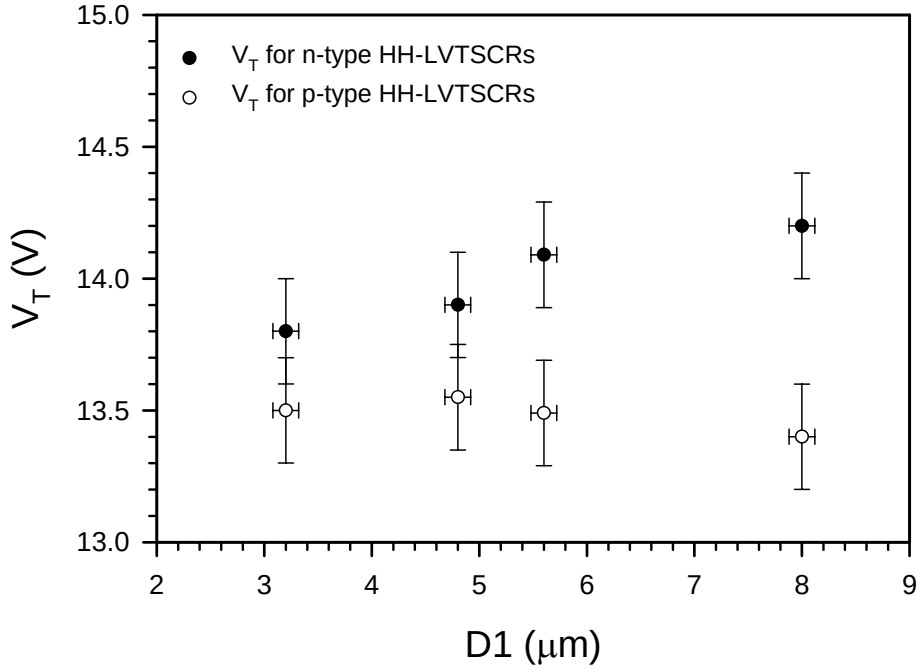


Figure 3.6. Comparison of measured trigger voltage (V_T) versus dimension D1 for n- and p-type HH-LVTSCRs.

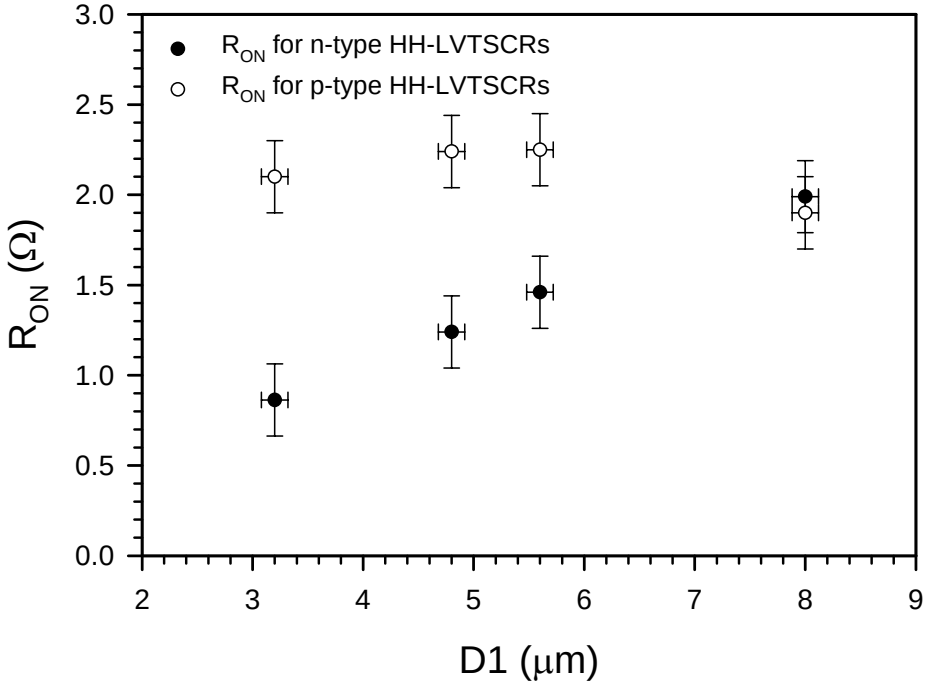


Figure 3.7. Comparison of measured on-state resistance (R_{ON}) versus dimension D1 for n- and p-type HH-LVTSCRs.

Figure 3.8 shows the failure current (I_{MAX}), i.e. the TLP current that causes the hard-failure in the HH-LVTSCR, as a function of the holding voltage (V_H). For the n-type HH-LVTSCR, the failure current decreases more quickly with increasing holding voltage than that for the p-type HH-LVTSCR. This suggests that the p-type HH-LVTSCRs are superior to the n-type HH-LVTSCRs for ESD designs requiring a relatively high holding voltage. But when a low holding voltage is allowed, the n-type HH-LVTSCR is able to discharge a higher level of ESD current per unit area.

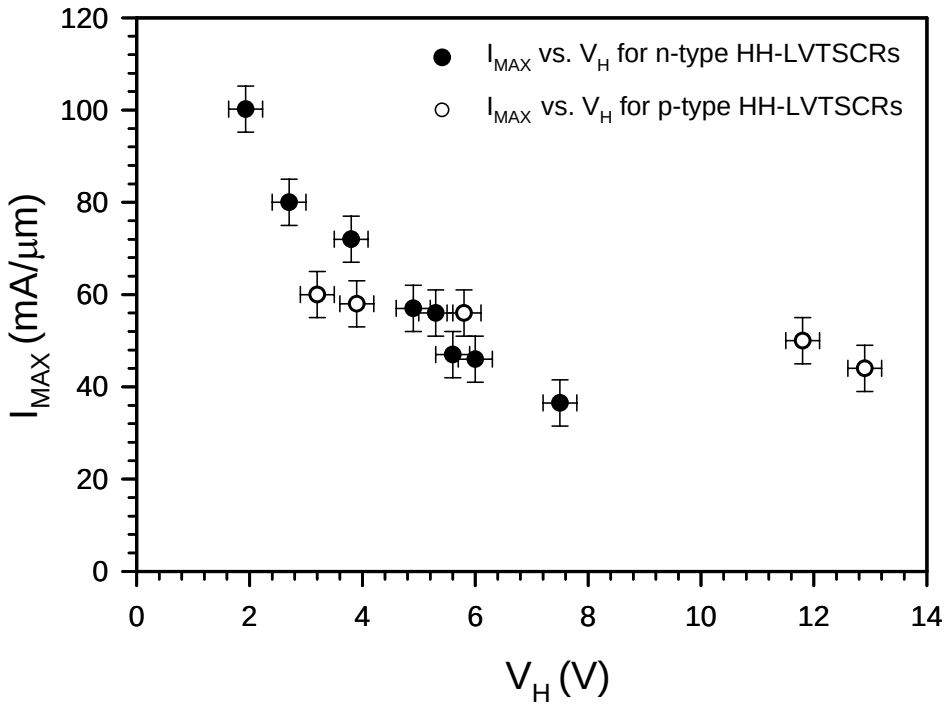


Figure 3.8. Failure current (I_{MAX}) versus V_H in n- and p-type HH-LVTSCRs tested using the TLP technique.

The holding and trigger voltages shown above have been obtained from the TLP measurements. A different method to estimate the holding voltage is sweeping the stress current until the device exits the state of latch-up. The experiments showed, however, that such a method underestimates the holding voltage because of the device self-heating in the on-state.

Furthermore, the devices were damaged during the measurements in the vicinity of the post-snapback region due to the presence of high current stress.

The HH-LVTSCR I-V characteristics are also evaluated for elevated temperatures. Figure 3.9 and Figure 3.10 show the effect of temperature on the holding and trigger voltages, respectively, of a HH-LVTSCR designed for a holding voltage higher than 5 V. The results indicate that the holding voltage decreases and the trigger voltage experiments a subtle increase with increasing temperature. As observed in Figure 3.9, an elevated ambient temperature can also cause latchup problems in the IC if the holding voltage drops below the operating voltage.

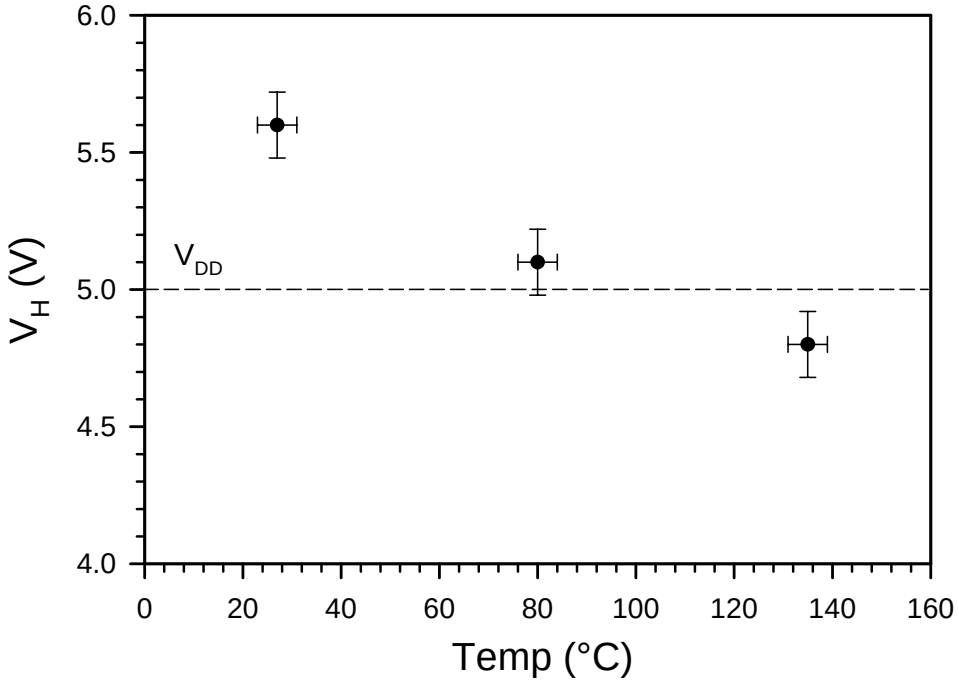


Figure 3.9. Holding voltage (V_H) versus temperature (Temp) for a HH-LVTSCR designed for $V_H > V_{DD} = 5$ V.

The drop in the holding voltage with increasing temperature is in general predictable for SCR-based devices [10]. However, the trigger voltage may behave differently depending on the device design and electrodes' interconnection. At high temperatures, the triggering of the

devices' regenerative feedback is especially influenced by: 1) the increase in the breakdown voltage at the blocking junction due to a decrease in the impact ionization and carrier multiplication associated with the enhanced scattering of free carriers at elevated temperatures, and 2) the thermally-induced leakage current exacerbated by the current gain of the laterally coupled bipolar junction transistors, which in turn tends to reduce the forward blocking voltage at high temperatures. The mechanism in (1) mentioned above is the dominant one on the observed slightly increased trigger voltage with increasing temperature shown in Figure 3.10.

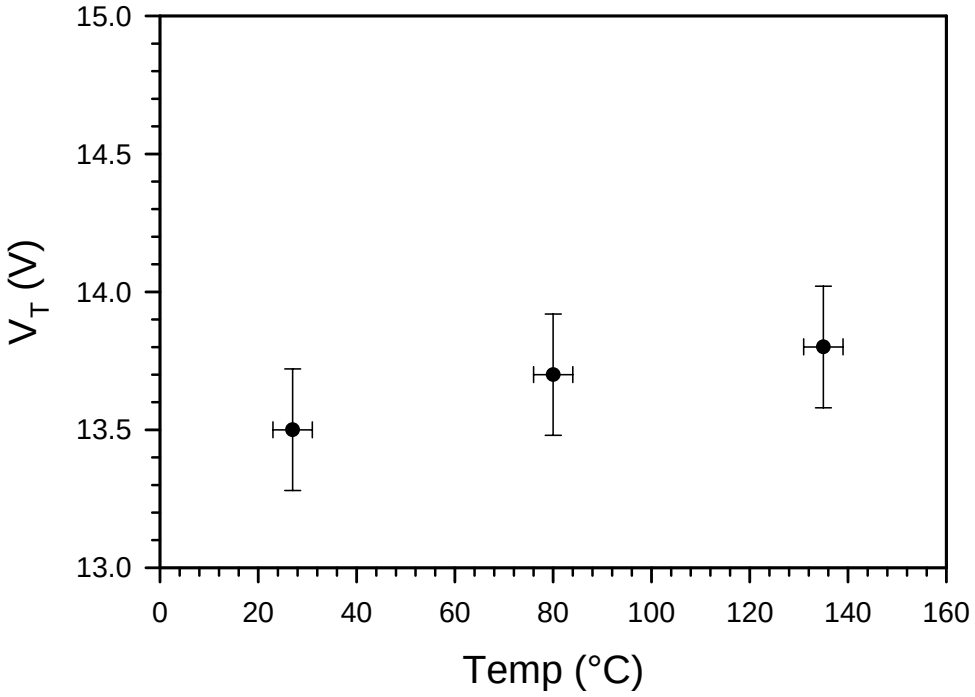


Figure 3.10. Trigger voltage (V_T) versus temperature for HH-LVTSCR designed for the holding voltage shown in Figure 3.9.

3.3. Layout Considerations

High levels of ESD protection are required for different low voltage integrated circuits operated in hazardous conditions or directly exposed to the users' handling. For these kinds of applications, the ICs are required to comply with a very high level of the ESD standard, e.g. 60 A

peak ESD current for 16.5 kV [45]. This, along with the possible large swing of operating voltage at the I/O pads, imposes complications on the integration and development of ESD protection structures. For these stringent ESD requirements, HH-LVTSCRs are attractive and sufficiently robust, as has been demonstrated from the results in Figure 3.3 to Figure 3.10.

Changing the device width has frequently been used to scale the ESD protection level. However, increasing the HH-LVTSCR width does not always guarantee a direct increase in the ESD protection capability. Moreover, such an approach may not fit into the restrictions imposed by the area constraints, circuit layout, and packaging of the microchip. To address this, a multifinger layout for optimal ESD scaling and enhancing ESD protection capability is developed. Figure 3.11 shows the top view of a two-finger HH-LVTSCR with even number of interdigitated metal-3 (M3) stripes and minimum separation for low interconnection resistance. In this layout scheme, the width of the HH-LVTSCR is kept small, e.g., W=200 μm, and all the device interconnections are accomplished in such a way that the contacts and vias between metal levels are aligned and the current is well distributed in the multifinger structure. The number of fingers thus allows for the scaling of the ESD protection capability, which has been known as one of the most difficult issues in the design and implementation of ESD solutions.

Figure 3.12 and Figure 3.13 show the resulting scaling of the S-shaped I-V characteristics with the number of fingers, for a p-type HH-LVTSCR with N-Tub connected and N-Tub open, respectively. The holding voltage for these multifinger structures is designed close to 5 V. These figures show the effect of finger number over the S-shape of the I-V characteristic. The trigger voltage of the HH-LVTSCR structure increases with increasing number of fingers, however this voltage is still considerably below the voltage that causes damage to the core circuit, and can be further customized by gate-induced triggering [52]. The holding current also increases with

increasing finger number, which allows for faster turn-off of the ESD device once the ESD has passed. Higher conductance for increased number of fingers is also observed in the reverse I-V characteristics, which gives rise to a more robust implementation of dual-polarity ESD protection cells.

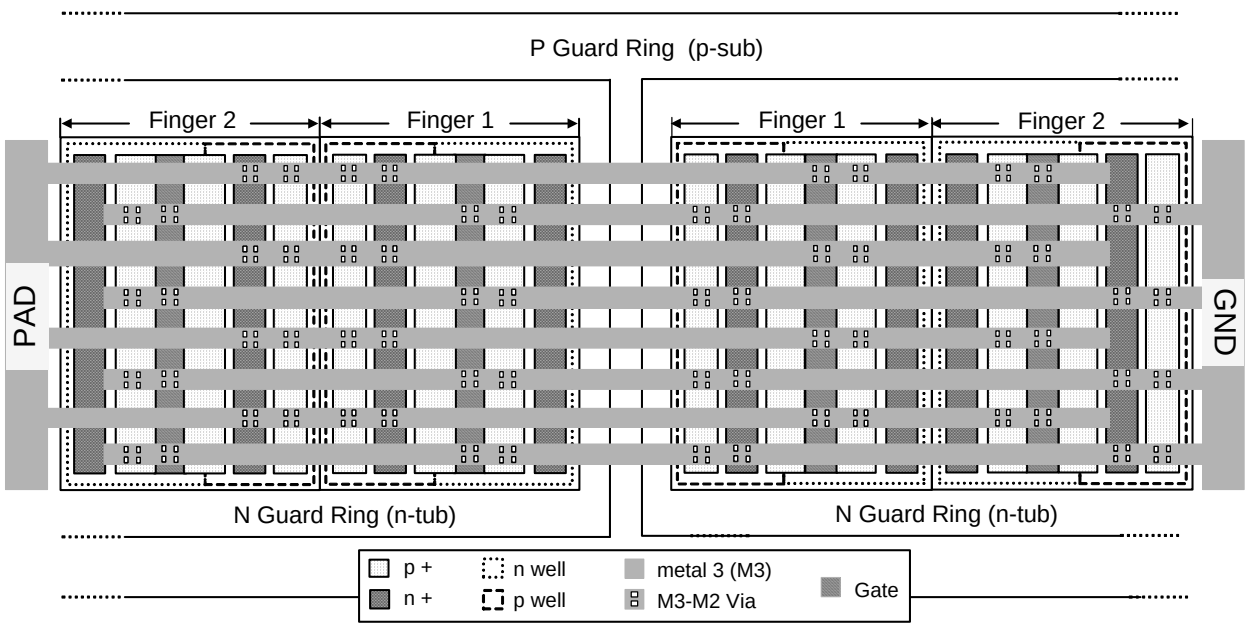


Figure 3.11. Layout top-view of a two-finger p-type HH-LVTSCR cell for bidirectional ESD protection.

3.4. ESD Protection Schemes with HH-LVTSCR

HH-LVTSCRs' applications for the design of effective ESD protections are illustrated by considering the following two cases: 1) ESD protection for ICs with an I/O pad voltage swing within the range of the supply voltage, and 2) ESD protection for ICs with an I/O voltage swing outside the supply voltage range.

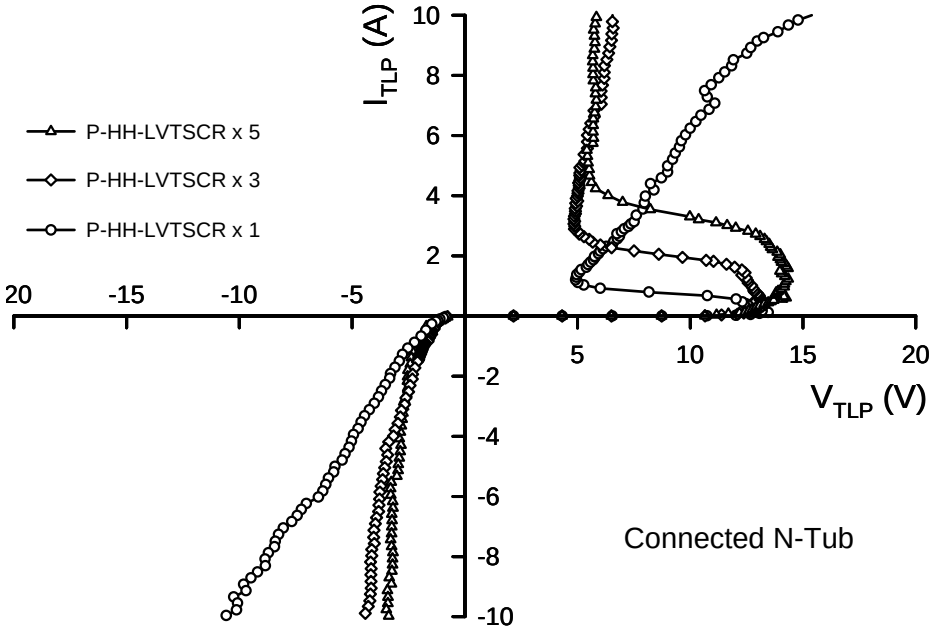


Figure 3.12. Comparison of measured I-V TLP characteristics for p-type HH-LVTSCRs with N-Tub open and having one-, three-, and five-finger.

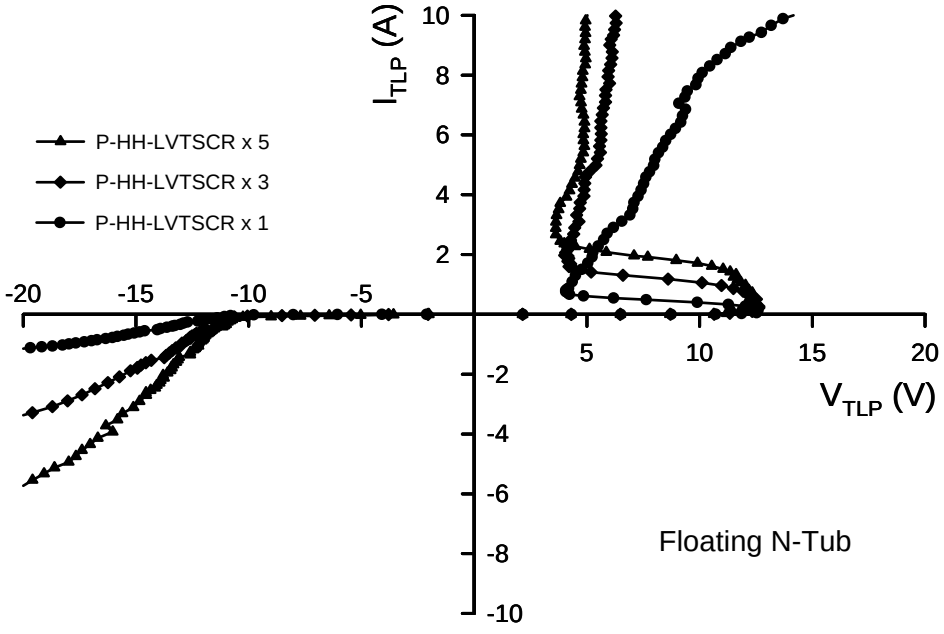


Figure 3.13. Comparison of measured I-V TLP characteristics for p-type HH-LVTSCRs with N-Tub open and having one-, three-, and five-finger.

The first example is the ESD protection of a typical digital circuit in which the swing of the pad voltage is within the range of the supply voltage, i.e. above V_{SS} = 0 and below V_{DD} = 5 V.

For the ESD protection of this IC, the trigger voltage of the pad protection cell should be larger than V_{DD} for the positive ESD and lower than V_{SS} for the negative ESD. For the supply clamp, an additional requirement is that its holding voltage must be equal to or larger than V_{DD} to prevent ESD latchup. Figure 3.14 shows the TLP characteristics of a p-type, five-finger HH-LVTSCR with N-Tub connected, designed for this purpose. The holding voltage is slightly higher than V_{DD} and the reverse conduction is about 0.7 V below V_{SS}. Furthermore, the trigger voltage and the maximum on-state voltage are lower than the critical voltage that may cause damages to the core circuit. The protection cell occupied an area of 200 x 226 μm^2, and sustained a component-level dual-polarity ESD stress of over 16.5 kV [45], and 2 kV MM. In addition, a system-level ESD testing was conducted, showing the protection structure can successfully uphold a stress of 15 kV [45].

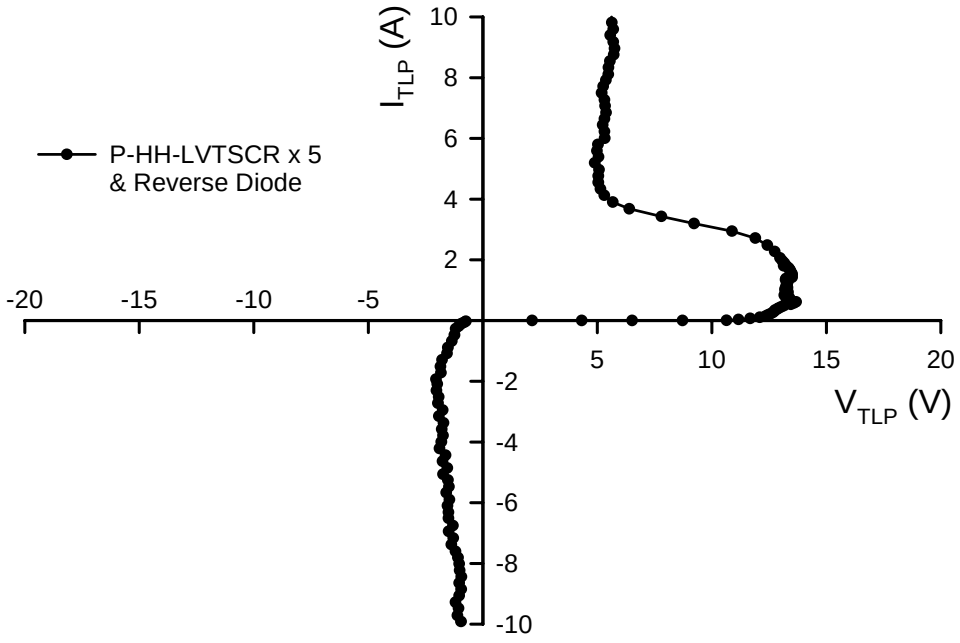


Figure 3.14. TLP I-V characteristics of the I/O pad protection and supply clamp for digital circuits.

The second example is the ESD protection of a mixed-signal application with a pad voltage ranging between -10 and 10 V. This voltage swing is below/above the power supply of V_{SS} = 0 and V_{DD} = 5 V (i.e., outside the range of the power supplies). The implementation of the ESD protection scheme for this circuit is accomplished using two shunt p-type, 5-finger HH-LVTSCRs with N-Tub open for the I/O pad protection cell, and a p-type, 5-finger HH-LVTSCR with N-Tub connected for the supply clamp. The use of two shunt HH-LVTSCRs for the I/O pad cell is required by the very large reverse operating voltage at the pad. Figure 3.15 shows the schematic for this ESD protection structure.

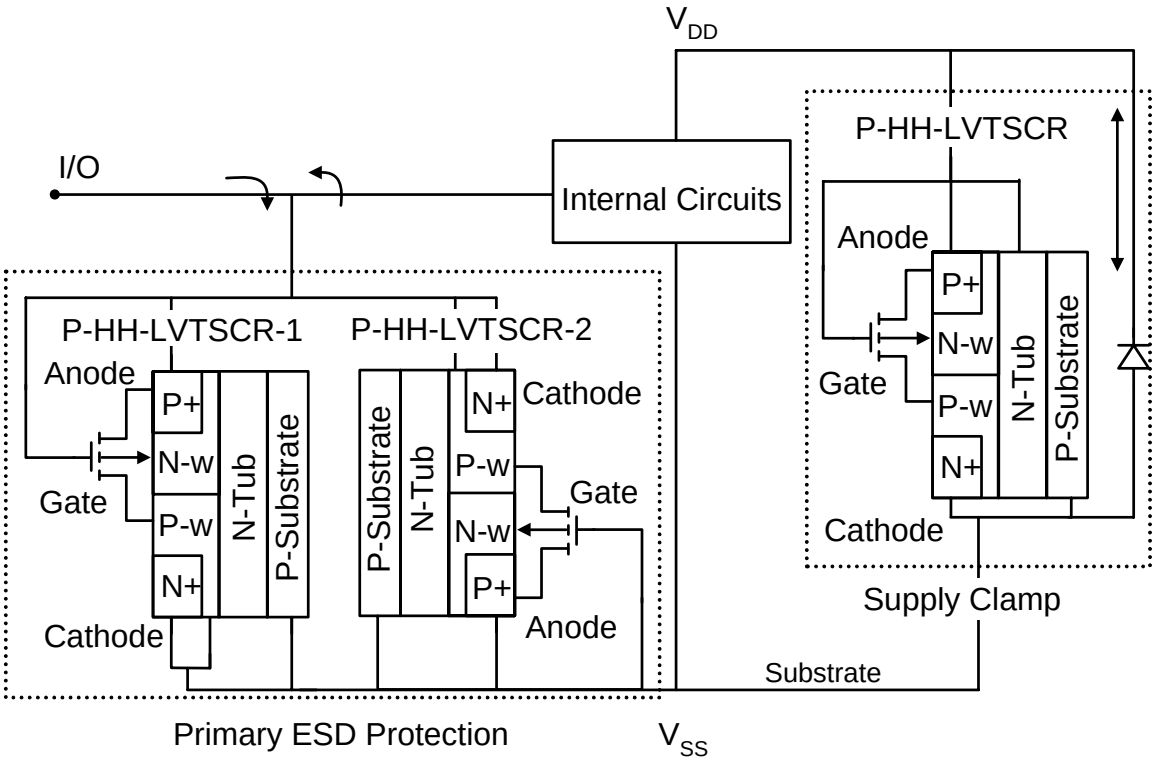


Figure 3.15. Schematic of the ESD protection solution using p-type HH-LVTSCRs for mixed-signal applications.

Figure 3.16 shows the I-V characteristics of the dual-polarity ESD protection cell at the I/O pad. The forward and reverse operating voltages at the I/O pad are within the forward and

reverse ESD trigger voltages, respectively. A holding voltage lower than the operating voltage is allowed in this case because the typical current available at the I/O pad during the normal operation is lower than the holding current of the protection cell and not enough to sustain a latchup condition [53], [121]. The protection cell occupied an area of 200 x 440 μm^2, and similar to the previous example sustained a component-level dual-polarity ESD stress of over 16.5 kV and 2 kV MM and the established system-level ESD stress of 15 kV [31].

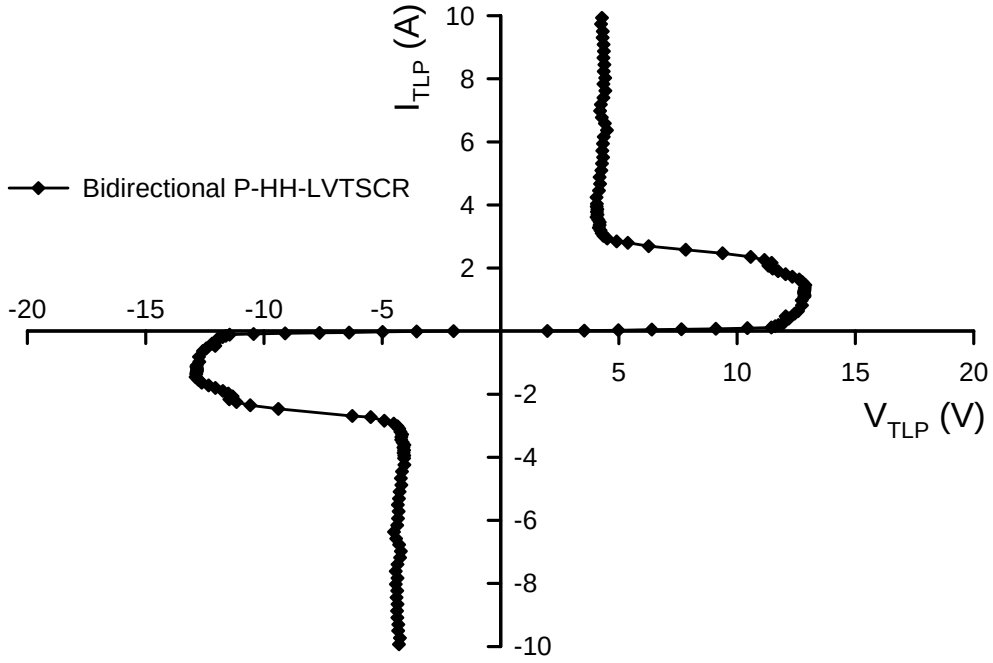


Figure 3.16. Bidirectional TLP I-V characteristics for the I/O pad protection.

3.5. Chapter Remarks

High-holding, low-trigger-voltage SCRs (HH-LVTSCRs) has been designed, fabricated, and characterized. A custom multifinger structure for layout optimization has been also implemented for scaling-up the ESD protection capability. Both n- and p-type HH-LVTSCRs have been assessed and the advantages of their tunable trigger and holding voltages have been presented. Moreover, characterization of the HH-LVTSCR at high temperatures was also discussed. The n-

type device performs better than the p-type device in the low holding voltage regime, but for high holding voltages the p-type device shows superior ESD performance. Two examples have been used to demonstrate that the devices are robust and effective for providing ESD protection of over 16 kV, as defined by the ESD standard IEC-1000-4-2 [31], and 2 kV MM [70], for a wide range of circuit operating conditions and applications.

CHAPTER 4
HH-LVTSCR-CONCEPT FOR ESD PROTECTION IN MULTI-TECHNOLOGY EMBEDDED SENSOR SYSTEM ON A CHIP

The MEMS (MicroElectroMechanical systems) microhotplate-based gas sensor is an emerging CMOS (complementary metal oxide semiconductor)-based technology that has cost and performance advantages over existing commercial gas sensing technologies [2], [99]. The microhotplate gas-sensor platform, heater-power amplifier, signal conditioning, and control circuitry have recently been formulated as a VC (virtual component) conforming to the SoC (system-on-a-chip) block-based design approach [1]. SoC design methodology is necessary due to the complexity of large digital systems and facilitates functional block design reuse. Formulating the gas sensor as a VC enables incorporation into CAD (computer aided design) libraries and facilitates the development of single-chip gas-sensing and classification solutions. Implementation of ES (embedded sensor)-VCs requires the use of a standard digital interface and standard DFT (design for test) functionality.

A major reliability problem in fabrication, assembly, and during handling and routine characterization of CMOS SoC ICs (integrated circuits) is electrostatic discharge (ESD)-induced damage. Because of critical chip area constraints, the presence of the ES (embedded sensor), and the processing steps following standard chip fabrication, the design of ESD protection for the gas sensor SoC is more stringent than that for typical VLSI (very large-scale integration) circuits. These problems have been investigated and reported in references [85], [89] and [91].

The gas sensor SoC requires ESD protection at various components. Figure 4.1 illustrates a generic ESD protection scheme. Bidirectional ground-referenced ESD protection elements are connected to the I/O pads, power supplies, and sensor electrodes. For better illustration of

sensing structure, Figure 4.2 depicts a Scanning Electron Microscope (SEM) micrograph of a microhotplate-based gas sensor. The SEM of the sensor shows the suspended membrane, the heater, and the sensing film electrodes where the ESD protection is included.

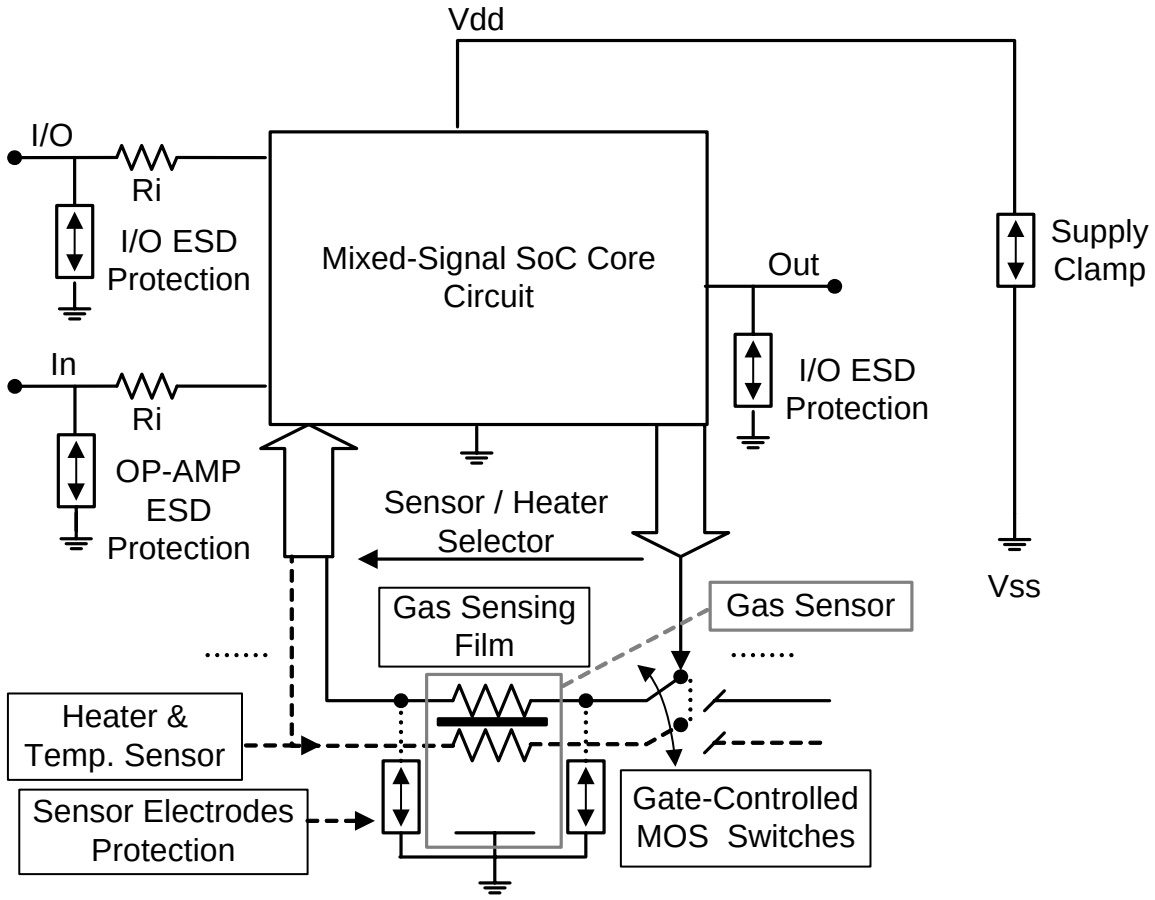


Figure 4.1. ESD protection scheme for the gas sensor SoC (system-on-a-chip).

This chapter presents a comprehensive design methodology and implementation of custom ESD protection devices in gas-sensor SoC applications. The microhotplate gas sensors are fabricated in a standard CMOS process using bulk micromachining post-processing [2] as opposed to the custom processes for microhotplate-type MEMS fabrication [123]. Such a foundry process enables the monolithic integration of a tailored ESD-protection structure with the core circuit and mixed-signal functional blocks on the same chip. The ESD solution will be

designed using the HH-LVTSCR concept presented in chapter 3, extended in this case to the standard CMOS technology used in the SoC development [85], [89].

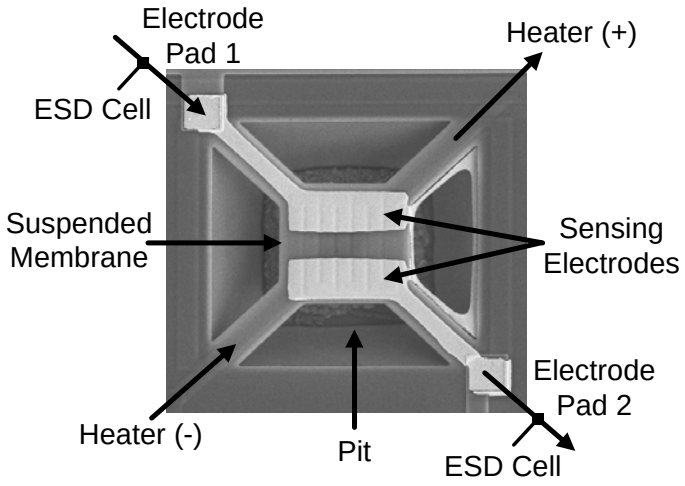


Figure 4.2. An SEM micrograph of microhotplate showing sensor electrodes and ESD protection points.

4.1. Implementation of ESD Protection Device

ESD protection design using conventional devices (e.g., MOSFETs, BJTs, and diodes) is standard practice. However, even though the I-V characteristics of the conventional devices are more predictable and scalable to some extent, other considerations such as area efficiency, clamping voltage, on-state conductivity, and power dissipation during stress can actually reduce the usefulness of conventional devices for implementation in compact ESD protections structures. SCR-type devices such as the discussed in chapter 3, [85], [89], [91] on the other hand, offer better performance for developing compact ESD protections.

4.1.1. SCR-Type ESD Protection Device

In chapter 3, a thyristor- or silicon controlled rectifier (SCR)-type device was applicable for ESD protection because it exhibited snapback behavior, low holding voltage and a high conductance during an ESD event (i.e., on-state). The current density in this device is uniformly

distributed, which permits better heat dispersion and reduces thermal hot-spot generation during the ESD event, see 2D contours in chapter 2. The low-voltage-trigger-silicon-controlled-rectifier (LVTSCR), an offspring of the SCR, offers the further advantage of reducing the trigger voltage to a level acceptable for use in CMOS IC protection [18]. However, as discussed in chapter 3, the low holding voltage and the low holding current [52], [87]-[89], [105] of the LVTSCR often cause latchup problem in ICs with an operating voltage above 1.5 V.

An extension of the HH-LVTSCR concept, shown in Figure 4.3, has been designed and fabricated using the same standard 1.5 μm CMOS process used for the development of the MEMS gas sensor SoC described in this study [85]-[89]. However, the design methodology can be extended under the constraints of the specific CMOS processes. By appropriate adjustment of the diffusions and inter-diffusion dimensions L, D, and D2 in Figure 4.3, the S-shaped I-V characteristics of the protection devices can be customized for each one of the protection elements presented in Figure 4.1, allowing for ESD protection without latchup problem.

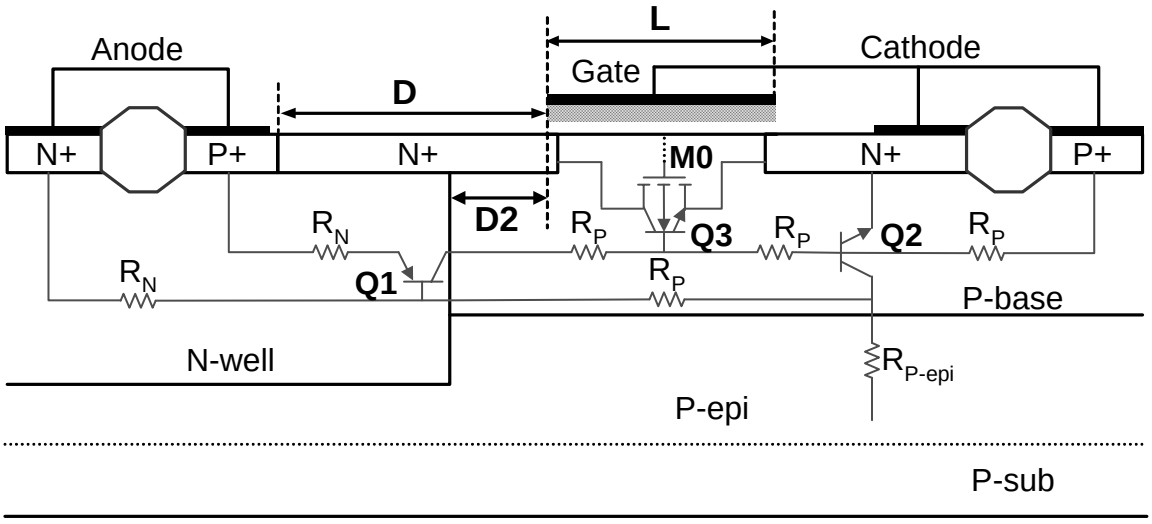


Figure 4.3. Cross-sectional view of SCR-type ESD protection device.

The concept of adjusting the holding voltage (V_H) in the SCR-based ESD protection circuits has been introduced and discussed in the previous chapter. However, the methodology for adjusting the devices' I-V characteristics and the circuit implementation constraints needs to be reassessed for each technology and system application. In the following sections, an ESD protection design and integration approach are discussed and developed in detail for an emerging MEMS-based CMOS gas-sensor SoC technology.

4.1.2. ESD Protection Device Operation

The thyristor-type ESD protection device shown in Figure 4.3 can provide effective ESD protection in both forward and reverse operating conditions. The forward on-state characteristic results when the anode voltage increases abruptly and turns on the NPN bipolar transistor underneath the gate (Q3). High injection of electrons and holes takes place in the cathode and anode regions, respectively, and the laterally distributed N-well to P-base blocking junction becomes conductive. This gives rise to a potential snapback between the anode and cathode from the trigger voltage (V_T) to the holding voltage (V_H) and a low impedance path when the voltage is increased beyond V_H. Note that the base of Q2 and the collector of Q1 form the common node in the P-base/P-epi region, and the collector of Q2 and the base of Q1 form the common node in the N-well region. These embedded BJTs interact with each other to sustain the regenerative feedback during the on-state.

The snapback behavior is consistently attributed to a distributed vertical- and lateral-bipolar effect. In the region formed underneath the gate, the mechanism of operation involves avalanche breakdown and high impact ionization. The minimum potential difference in the N-well to P-base junction is related to the reverse junction barrier, consistent with the gradual junction approximation, and the holding voltage is the sum of this voltage and the voltage underneath the

gate of the embedded MOS (M0), shown in Figure 4.3. Following the approach previously discussed in chapter 3, tuning of the holding and trigger voltages is readily accomplished by adjusting the dimensions D, L, and D2.

For reverse operating condition, the voltage at the anode is lower than that at the cathode, and it forward biases the vertical P-sub to N-well junction and the lateral P-base to N-well junction. The maximum voltage is thus clamped by lateral and vertical forward-biased junctions (see Figure 4.3), and a low impedance path is created for ESD current.

Following the previous discussion and the results presented in chapter 3, the above-mentioned ESD device can be customized to implement efficiently the protection components in the ES-SoC of Figure 4.1, but specific lateral dimensions are required to tailor V_T, V_H, and R_{ON} for the needs of each component. The trigger voltage V_T is designed to be smaller than the transient voltage that causes circuit malfunction. Since V_{DD} = 5 V and V_{SS}= 0 V power rails are directly biasing the core circuit, the trigger voltage can be designed smaller for the supply clamp than for the I/O protection. However, in the ESD design window, V_T cannot be very close to V_{DD}, since the protection device should not be activated without the presence of an ESD event.

The holding voltage (V_H) is adjusted based on the operating voltage and current at the I/O. Although it should be higher than the operating voltage at the protected pad (e.g., higher than V_{DD}), a holding voltage lower than V_{DD} can be used if the I/O pad operating current cannot sustain a latchup condition in the protection device after the ESD has passed. A lower holding voltage improves the ESD performance per unit area of the protection cell. One the other hand, when a high holding voltage is required (for the case of supply clamp), it can be obtained by degrading the injection efficiency and transport factor of the coupled BJTs (Q1 and Q2) in

Figure 4.3. Nonetheless, it has the drawback of lowering the conductivity modulation, which results in a higher on-state resistance.

The required on-state resistance R_{ON} is determined from the maximum voltage allowed at the pad and the maximum current level of ESD. The on-state resistance is then used to determine the width required for the protection cell. The discussed ESD device has a much lower R_{ON} per unit width than conventional ESD protection devices, thus minimizing the chip area needed for ESD protection.

Table 4.1 summarizes the values of V_T, V_H, and R_{ON} obtained from 80-μm width devices with different internal lateral dimensions D, L, and D2. The other dimensions in the device are kept at the minimum feature sizes allowed by the design ground-rules. The measurements are accomplished using the 50 Ω Transmission Line Pulsed (TLP) system, model 4002 from Barth Electronics, Inc., calibrated for 10 ns rise time and 100 ns pulse width.

Two slightly different versions of ESD devices were tested. Devices in Table 4.1 (a) follow the cross-sectional view depicted in Figure 4.3, and devices in Table 4.1 (b) are fabricated without the P-base implantation in the cathode side. Note that devices in Table 4.1 (b) possess a larger trigger voltage, but also provide a lower R_{ON} that allows for higher levels of ESD current. The trigger voltages given in Table 4.1 are close to the trigger voltages previously obtained for a different technology in chapter 3, and are found to be in a desirable range for providing effective ESD protection in the considered CMOS technology.

The information summarized in Table 4.1 for the two versions of the ESD devices also shows the effects of the intermediate p-type region (in Figure 4.3, base of the BJT Q2 and collector of the BJT Q1) on the resulting S-shaped I-V characteristics. By incorporating or removing the P-

base implantation, the superficial doping concentration can be correspondingly increased or reduced. The incorporation of the P-base region leads to a lower trigger voltage due to a more abrupt blocking junction (collector-base of Q1), but also results in a higher R_{ON} and thus a lower conductivity during the regenerative feedback.

Table 4.1. Holding voltage (V_H), trigger voltage (V_T), and on-state resistance (R_{ON}) for dimensions L, D, and D2 (in μm). a) devices as shown in Figure 4.3, and b) devices as shown in Figure 4.3 without P-base.

(a)

Devices	L	D	D2	≈ V_H (V)	≈ V_T (V)	≈ R_{ON} (Ω)
Device A1	5.6	5.6	3.2	4.5	11.4	3.1
Device A2	5.6	8	4	5	11.7	3.8
Device A3	6.4	5.6	3.2	4.8	11.6	3.6
Device A4	6.4	8	4	5.2	12.2	4.4

(b)

Devices	L	D	D2	≈ V_H (V)	≈ V_T (V)	≈ R_{ON} (Ω)
Device B1	4.8	5.6	3.2	3.2	14	2.1
Device B2	4.8	8	4	4.3	14	2.3
Device B3	5.6	5.6	3.2	5.6	14.2	2.4
Device B4	5.6	8	4	6.8	14.3	2.6

4.1.3. Layout of Multifinger Protection Device

The layout is a critical step in the design and integration of the ESD protection structure on the ES-SoC. The ESD protection structure not only needs to be small and reliable, but also is required to fit in the space available and comply with all the design rules imposed by the IC-fabrication technology being used and the ES-SoC development. The maximum ESD level that the ESD protection device can sustain before failure is proportional to the width of the device.

The width of the ESD device is constrained in this design by the pad lateral dimension and the inter-pad distance. Figure 4.4 shows a simplified layout-top view of two adjacent pads, the power rails (V_{DD} and V_{SS}), and the proportional area occupied by the thyristor-type devices. The width (W) extends from the metal connected to the I/O pad (protected node) to the guard ring on the periphery of the protection cells.

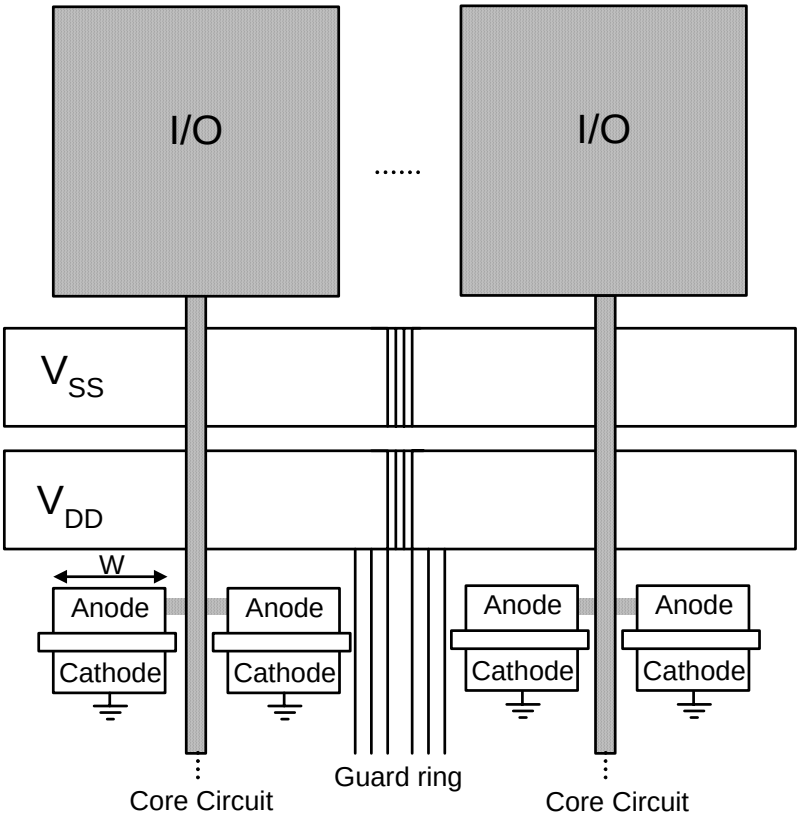
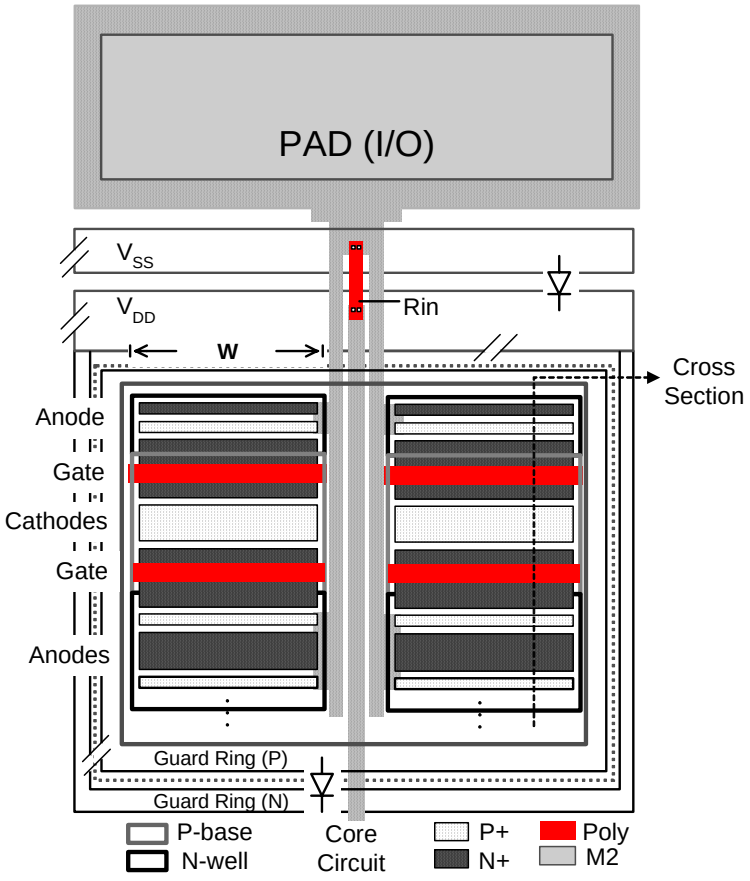


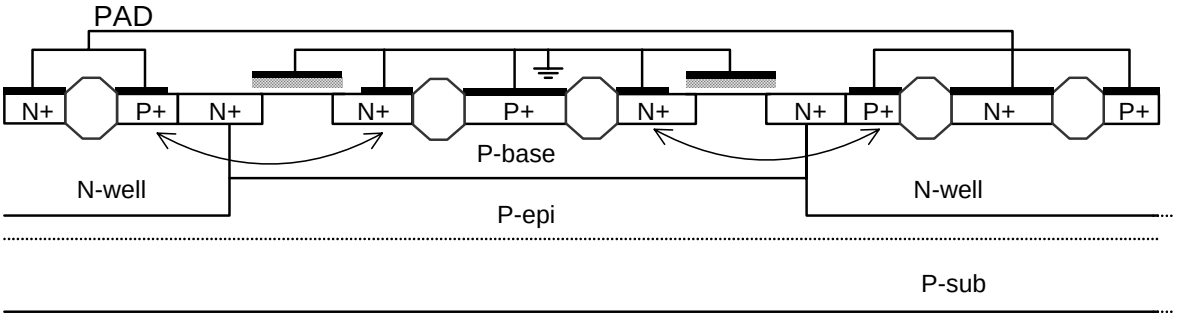
Figure 4.4. Simplified top-view of two consecutive pads and proportional area required for single SCR-type device.

The total length of the device extends in the direction perpendicular to the pad. Since the internal lateral dimensions determine the S-shaped I-V characteristics of the thyristor, these dimensions are fixed by the constraints of the ESD design. ESD scaling is then accomplished by using a multiple finger layout scheme, with the number of fingers determined by the required ESD-protection level.

Figure 4.5 (a) shows a partial top-view of the layout for a multifinger ESD protection cell, and Figure 4.5 (b) shows the corresponding cross-sectional view along the dashed line indicated in Figure 4.5 (a). The conduction paths for the dual-polarity current are also indicated with dashed lines in the cross-sectional view. Note that the ESD current distributed along the fingers flows in both directions; i.e., through the forward p-n junction when the ESD voltage in the pad is below V_{SS} and through the SCR-type structure when the ESD voltage in the pad is above the trigger voltage of the SCR (V_T). In this ES-SoC-tailored layout scheme, adjacent SCR devices can also share properly sized common wells (e.g., P+ inside the P-base) which further reduce the inter-finger distance with no design rules violations.



(a)



(b)

Figure 4.5. (a) Partial layout top-view of a multifinger SCR-type protection cell, and (b) the corresponding cross-sectional view. Anodes are connected to the PAD and cathodes to V_{SS}.

The multifinger ESD protection structure has the advantages of robustness and scalability, is more immune to process variation, and is compatible with the SoC development process. The devices' anodes are connected through metal 1 (M1) to the protected pad, and the cathodes are connected to metal 2 (M2) and grounded. The width of the M1 connected to each anode is properly increased from the top (pad) to the bottom (circuit input) to provide a more uniform input resistance to the fingers of the protection device. Uniform input resistance guarantees similar voltage stress conditions for each finger and better distribution of the ESD current in the multifinger device.

To provide different levels of ESD protection, different number of fingers should be used in the protection cell. The multifinger structure is described using "AxB fingers" (e.g., 2x8 fingers), the nomenclature stands for an ESD protection cell formed by "A" devices connected in parallel each having "B/A" fingers. Table 4.2 summarizes a) the HBM level obtained from device A1 in Table 4.1 having 2x6 and 2x8 fingers, and b) the HBM level obtained from device B2 in Table 4.1 having 2x6 and 2x8 fingers. It shows that with the 2x6-finger protection cell, a HBM-ESD level of higher than 3 kV is obtained, and for the case of the 2x8-finger cell, an even higher HBM level of 5.5 kV is achieved.

Table 4.2. HBM ESD protection level of multifinger SCR-type devices; a) multifinger cell considering device A2 in Table 4.1 (a), and b) multifinger cell considering device B2 in Table 4.1 (b). 5.5 kV is the highest testing voltage applied.

(a)

Device /Fingers Number	+ HBM (kV)	- HBM (kV)	$\approx V_H$ (V)	$\approx V_T$ (V)	$\approx R_{ON}$ (Ω)
(A1) 2x6	3.9	3.3	5.8	12.1	1.9
(A1) 2x8	5.5	4.2	6.1	12.3	1.5

(b)

Device /Fingers Number	+ HBM (kV)	- HBM (kV)	$\approx V_H$ (V)	$\approx V_T$ (V)	$\approx R_{ON}$ (Ω)
(B2) 2x6	4.1	3.5	5.1	14.8	1.2
(B2) 2x8	5.5	4.4	5.6	14.9	1.0

The multifinger layout scheme is very useful in the SoC development, as it can further optimize the trade-off between ESD robustness and chip area. Figure 4.6 and Figure 4.7 depict the TLP I-V characteristics for each group of the multifinger devices in Table 4.2. Notice the reduction in the on-state resistance with increasing number of fingers.

As mentioned earlier, the present design provides enhanced area efficiency. The 2x8-finger protection structure developed occupies 20% less space than the conventional MOSFET-based dual-diode structure discussed in chapter 1. The dual-diode-type protection implemented in the same 1.5-μm CMOS technology occupied an area of 132 x 336 μm^2, to sustain a 2 kV HBM stress level [102]. Furthermore, since the protection structures are all ground-referenced, the present solution also reduces the parasitics between the I/O pad and power rail, and a considerable smaller V_{DD} rail around the periphery of the circuit can be used (see power rails in Figure 4.4), thereby gaining more effective area for the SoC core circuit.

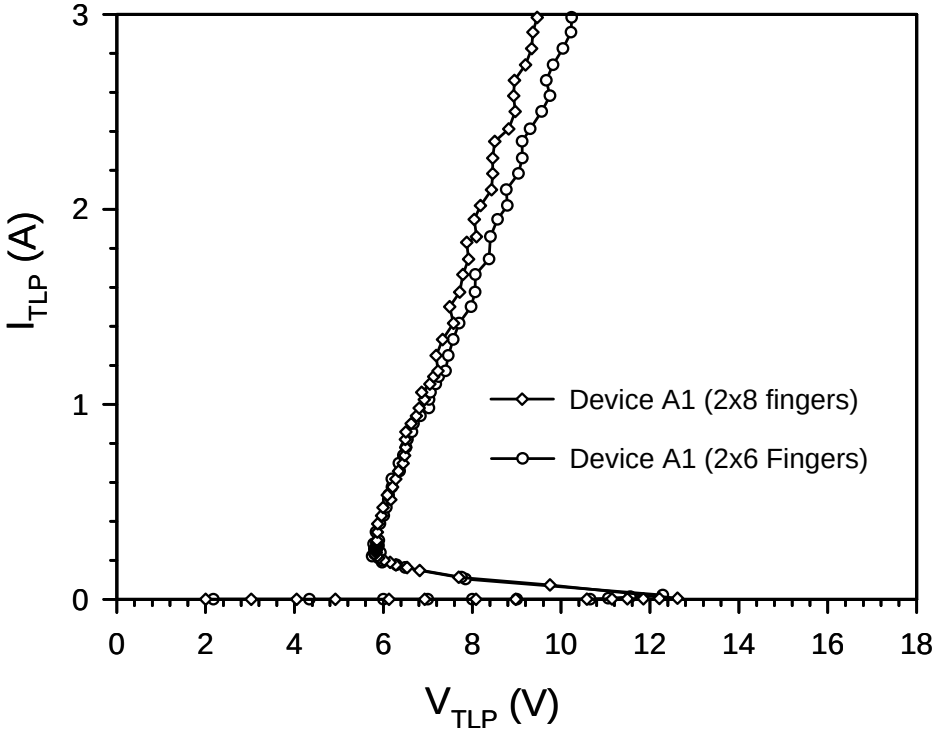


Figure 4.6. TLP I-V characteristics of a multifinger cell using device A1 (Table 4.1 (a)).

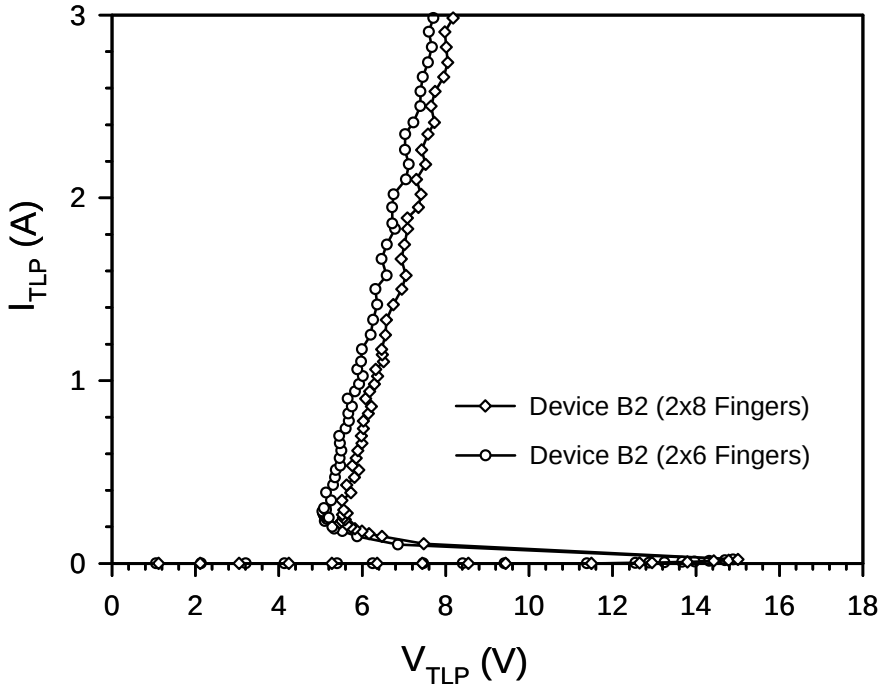


Figure 4.7. TLP I-V characteristics of a multifinger cell using device B2 (Table 4.1(b)).

4.2. Overall SoC ESD Protection Design

Aimed to an optimum implementation of the ES-SoC ESD protection structure, the custom design of the protection elements must consider the operating conditions and constraints associated with each protected node. Based on this premise, the devices discussed in the preceding section are used next for the supply clamp design, the I/O pad protection, and the sensor electrodes protection.

Figure 4.8 shows the schematic ESD protection structure at the SoC periphery. For positive ESD stress at V_{DD} or the I/O pad, the SCR-type cell is triggered at a relatively low V_T and snaps back to V_H. The thyristor S-shaped I-V characteristics provide a low impedance conduction path from V_{DD} or the I/O pad to V_{SS} during the ESD event and bring the necessary protection to the ES-SoC core circuit without latchup problems. For negative ESD stress, the anode-to-cathode p/n junctions embedded in the protection device are forward biased, as shown in Figure 4.5. The negative voltage is then clamped by the forward biased p/n junctions in each finger, which provides a low impedance path from V_{SS} to V_{DD} for the ESD current.

4.2.1. Supply Clamp

Figure 4.9 shows the TLP I-V characteristics for a 2x8 multifinger protection cell integrated on the periphery of the SoC as a supply clamp. The protection device can carry a TLP current of 7 A with no damages. The voltage level at this point is below the maximum ESD voltage (V_M), beyond which the internal CMOS devices can suffer ESD-induced damage. This assures that at this level of stress the supply clamp is effective in providing the required voltage clamp over V_{DD} for reliable operation of the ESD protection structure.

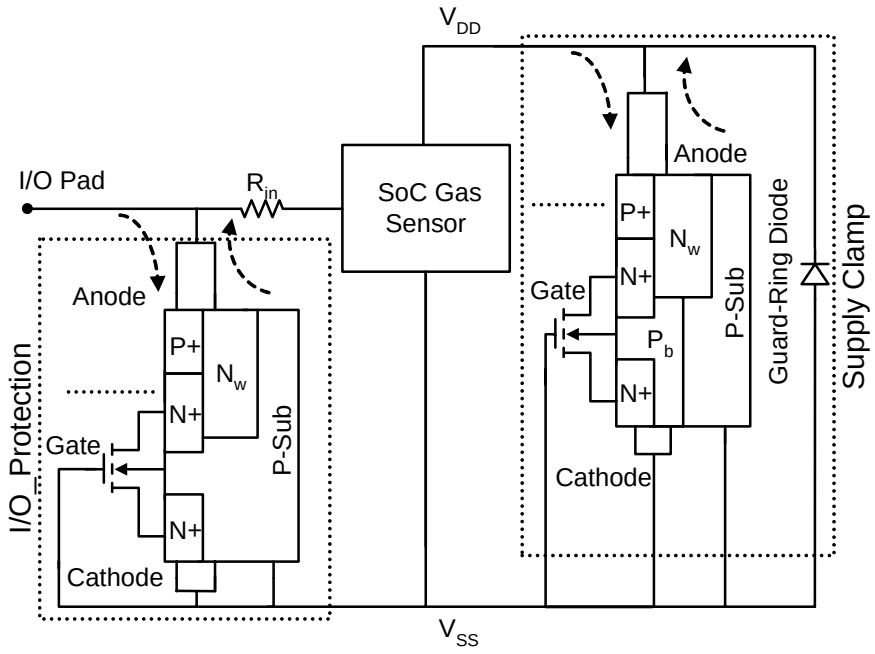


Figure 4.8. Schematic of the on-chip ESD protection structure.

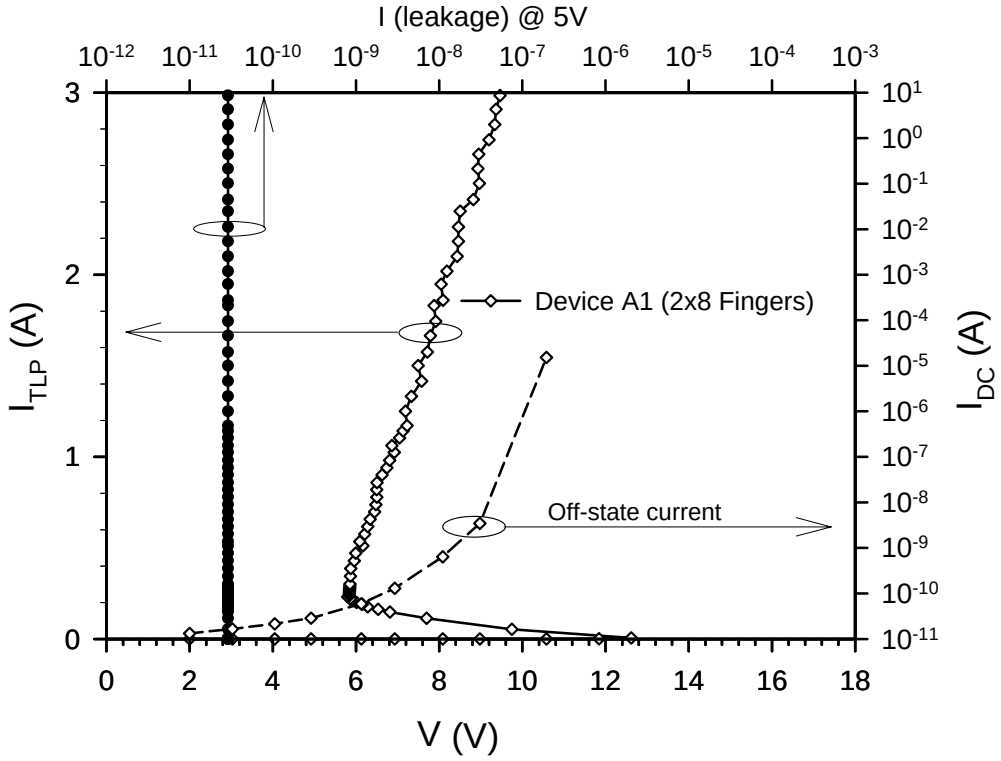


Figure 4.9. TLP I-V characteristics and leakage current in logarithmic scale for the supply clamp multifinger cell using device A1 (Table 4.1).

The leakage currents evaluated at V_{DD} = 5 V after each TLP measurement at off-state and on-state, were found to be lower than 10^{-10} A. The leakage current is depicted on the same graph (Figure 4.9) for better illustration. This leakage current was measured using the TLP system, but it was further verified below the trigger voltage using the HP semiconductor parameter analyzer.

4.2.2. I/O Pad ESD Protection

While a SCR-type device that meets the requirements for the supply clamp can also meet the requirements for I/O protection, a slightly different device can be considered for improved protection. Removing the P-base in the device shown in Figure 4.3 leads to an increased V_T, as shown in Table 4.1. Nevertheless, it also results in smaller forward and reverse conduction resistances and consequently higher ESD current per unit area in the protection device. Furthermore, the I/O protection structure can be designed with a lower V_H because the driving current available in the logic pads during the normal operation is low and cannot sustain a latchup condition. It is important to point out, however, that there are limitations in the minimum current that can be detected in the 50 Ω TLP system and additional latchup verifications were successfully accomplished once the devices were incorporated in the SoC application.

A smaller holding voltage results in lower power dissipation and thus a smaller required device area. Figure 4.10 depicts the TLP I-V characteristics for a 2x8 multifinger protection cell integrated on the periphery of the SoC for the I/O protection, indicating a higher V_T but lower V_H and R_{ON} than that of the supply clamp cell.

Notice in Figure 4.9 and Figure 4.10 that the multi-finger scheme yields a higher holding voltage than its corresponding single-finger data given in Table 4.1. The shift in the holding voltage is due to the mobile charge divergence among the adjacent fingers, which reduces the

overall injection efficiency during the regenerative feedback obtained in the device at stress condition.

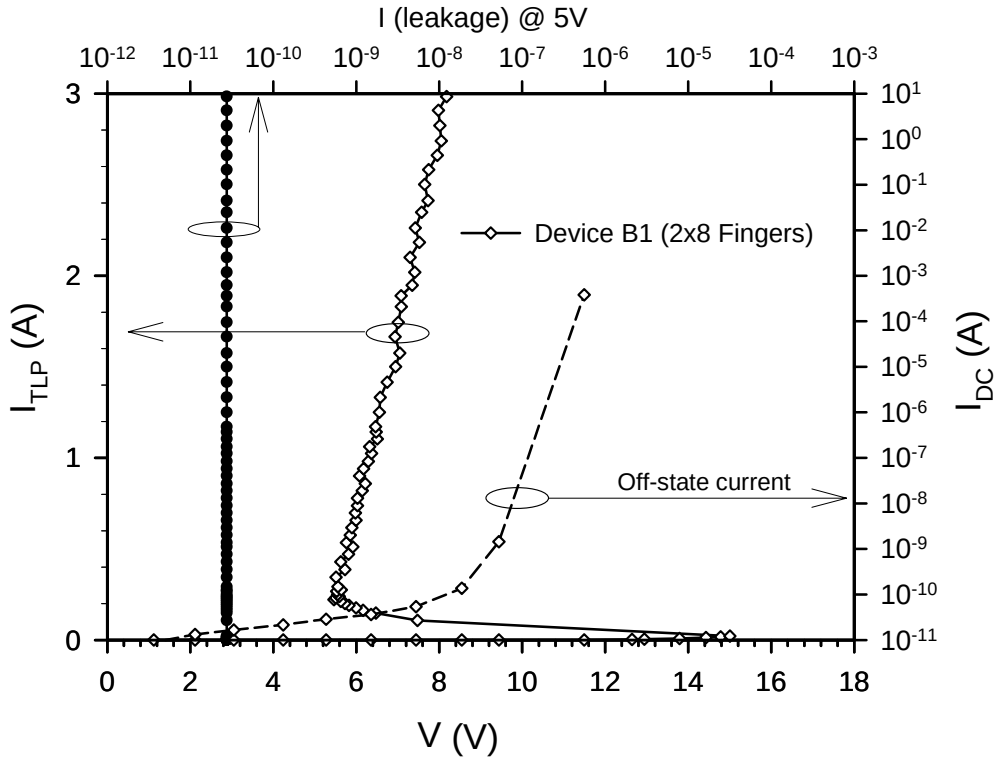


Figure 4.10. TLP I-V characteristics and leakage current in logarithmic scale for the I/O multifinger ESD protection cell using thyristor B2 (Table 4.1).

4.2.3. Sensor Electrodes ESD Protection

Figure 4.11 shows the ESD protection device at the ES electrodes and a cross-sectional view of the gas sensor, illustrating the effective capacitance (C) between the exposed metal oxide sensing film and the substrate. For this particular ESD protection device, an additional contact to the anode region from the drain of the embedded MOS device allows for direct injection of carriers into the base of the PNP (Q1 in Figure 4.3) resulting in a lower V_T. This modification is aimed to create a discharge path at lower voltage/current conditions in the electrodes of the sensors. The protection device included at the sensor electrodes does not receive the same high

ESD stress that can be generated at the pad. As a result, it requires a smaller area than that for the I/O pads and supply clamp.

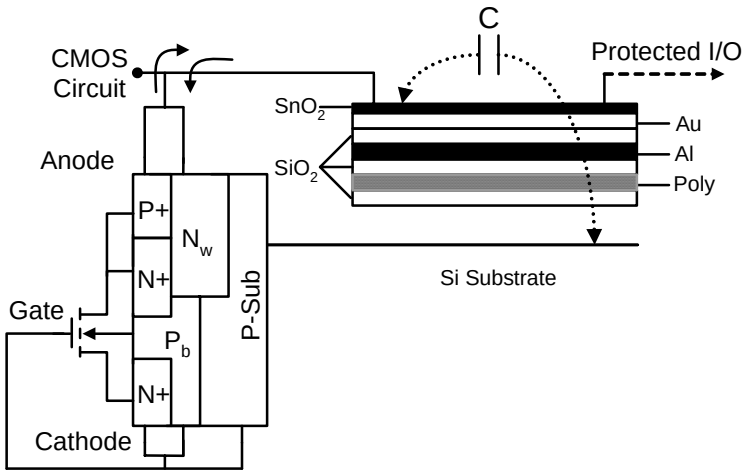


Figure 4.11. Cross-sectional view of microhotplate-based gas sensor with ESD protection at the sensor electrode.

The main objective of the microhotplate electrodes' protection is to avoid possible ESD mechanisms originating from the outside while characterizing the sensor or originating at the sensor itself. Thus, the protection structure can render the necessary low impedance path for current/voltage overshoots at the ending electrodes. Besides, the protection devices avoid the possible damage caused by over stress associated with the micromachining post-fabrication processing of the gas sensor SoC, a reliability problem that is still difficult to predict and characterize.

Figure 4.12 depicts the TLP I-V characteristics of a 2x2 finger ESD protection integrated at the sensor electrodes. Since the protection cell is smaller and the conduction conditions for the device have been slightly modified with the additional connection in the anode, R_{ON} increases but the trigger is kept relatively low and the holding voltage sufficiently above V_{DD}, which further reduces any possible interaction of the sensor protection with sensor operation.

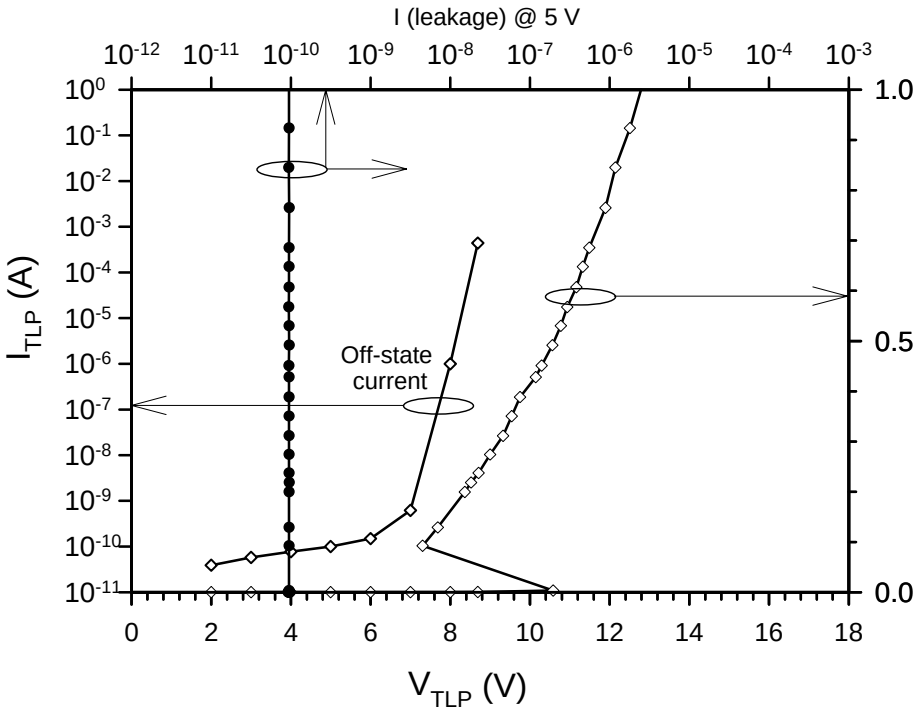


Figure 4.12. TLP I-V characteristics of ESD protection at the sensor electrode.

4.3. SoC ESD Testing Results

The ESD protection cells discussed above are integrated in the ES-SoC and the final performance of the protected circuit is evaluated. The circuit without ESD protection failed right after it was subjected to a TLP of 35 V and less than 100 mA. This very low level of ESD immunity demonstrates the urgent need for an integrated ESD protection.

Table 4.3 summarizes the measured values of V_T, V_H, and R_{ON} for the ES-SoC supply clamp, I/O protection, and sensor electrode protection structures. Both the I/O protection and supply clamp utilize a 2x8 SCR-type cell. Consistent with the explanations presented in Section 4.2, the I/O protection has higher V_T and lower V_H and R_{ON} than the supply clamp. For sensor electrode protection, R_{ON} is higher because a 2x2-finger device is used.

Table 4.3. Measured V_H, V_T, and R_{ON} of multifinger protection devices: 2x8 fingers used for the supply clamp and I/O protection, and 2x2 fingers used for the sensor electrode protection.

Protection Dev.	$\approx V_T$ **(V)**	$\approx V_H$ **(V)**	$\approx Ron$ **(Ω)**
Supply Clamp	12.5	6.1	1.9
I/O protection	14.9	5.1	1.3
Sensor Electrodes	10.4	7.3	3

Table 4.4 summarizes the passing HBM levels between the various pads and power supplies of the ES-SoC with ESD protection designed using the 2x6- and 2x8-finger protection cells. It indicates that for the 2x6 finger SCR cells, HBM ESD protection higher than 3 kV is obtained and still a higher ESD protection of 4 kV is possible for the case of 2x8 finger devices. The lower HBM level for the negative polarity is due to the series resistance associated with the diode for the reverse conduction of the multifinger protection cells. The passing HBM level for the sensor electrode protection designed with the 2x2 finger cell is also found over 1.5 kV.

Table 4.4. Passing HBM levels of the SoC with ESD protection designed using two different multifinger SCR-type devices.

Dev. Fing.	**I/O-V_{SS}**	**V_{SS}-I/O**	**V_{DD}- V_{SS}**	**V_{SS}-V_{DD}**	**I/O-I/O**	**I/O-V_{DD}**
2x6 Fing.	4.3 kV	3.3 kV	4.0 kV	3.4 kV	3.2 kV	3.2 kV
2x8 Fing.	5.5 kV	4.2 kV	5.5 kV	4.1 kV	4.1 kV	4.1 kV

4.4. ESD Protection for Multi-Technology SoC and the Downscaling in the CMOS Technology.

As the technology used in the development of the sensor system-on-a-chip is scaled-down, a narrower ESD design window and even more stringent area constraints are imposed. In CMOS technologies such as 0.5-μm, 0.25-μm and smaller, the design of the ESD protection solution and

optimization of the overall system require to combine ESD schemes such as those presented in Figure 1.9(a). For instance, MOS-based diodes can be incorporated in the inputs, and preferably, optimized SCR-type devices for implementing the supply clamp [94]. Furthermore, ESD protection components are necessary not only at the final stage of integration, but they should also be included at the early stage of sensors design and characterization, since the MEMS devices incorporated in the ES-SoC are also sensitive to stress conditions.

The MOS-based diodes can be readily implemented using the standard MOSFET devices available in the design tools. However, suitable SCR-based supply clamps are not available in standard design libraries and can only be designed by using the restricted information provided by the foundry. Following the discussion in chapter 2, doping profiles and a device simulation setup can be generated to investigate the extension of the HH-LVTSCR concept to the new technology where the gas sensor SoC application is being designed [94]. In this case, general information such as the characteristic sheet resistance may be available for the definition of the different wells used in the device structure. The APPENDIX shows an input deck example of a device simulation where the analytical doping profiles are generated and equivalent sheet resistances and junction depths are extracted within the TCAD environment.

Figure 4.13 shows an example of an analytically-generated 2D HH-LVTSCR type-device for evaluation of the ESD protection performance using approximated doping profiles in the range of those normally used in sub-micron CMOS technology [17], [26]-[27] [35], [49]. Figure 4.14 shows steady-state simulations when the distance D is increased. These results are consistent with those presented in previous discussions, where the holding voltage increased when D is increased.

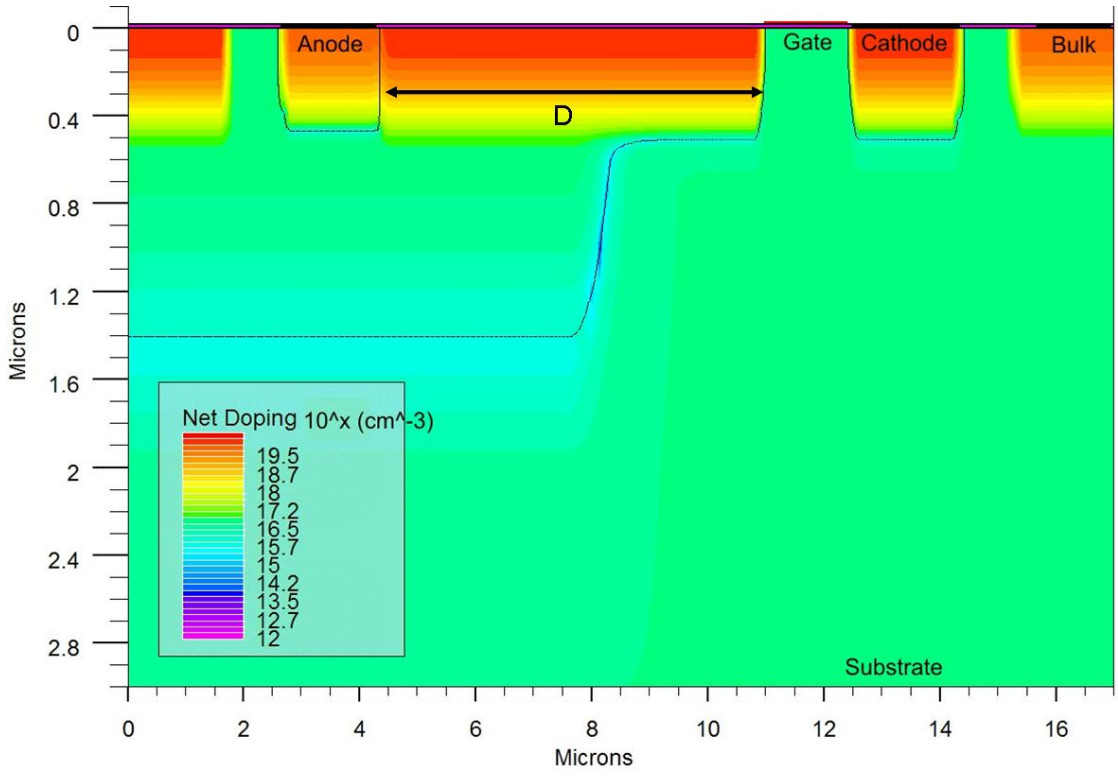


Figure 4.13. Analytically generated 2D cross-sectional view of ESD protection device.

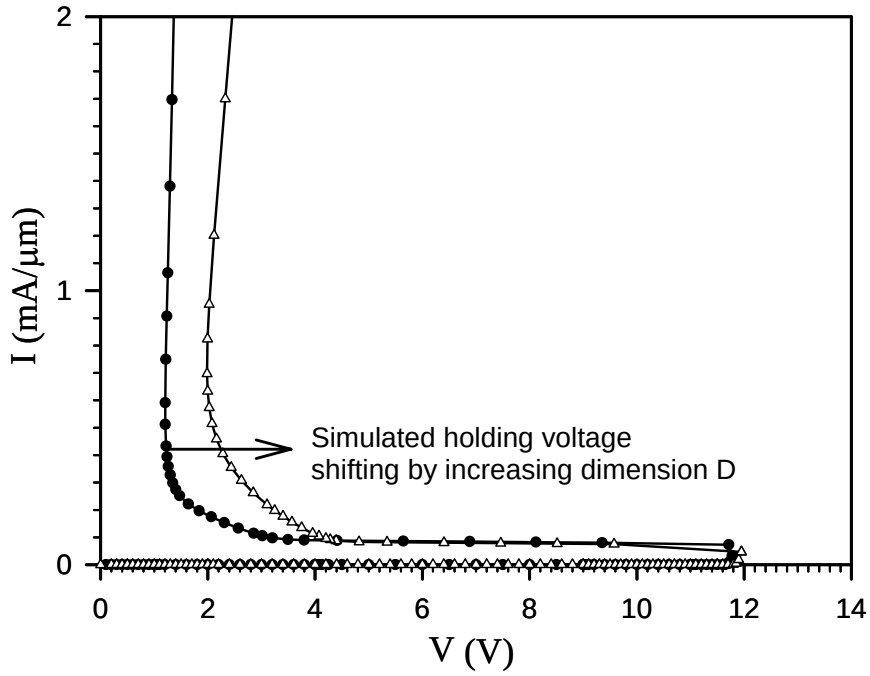
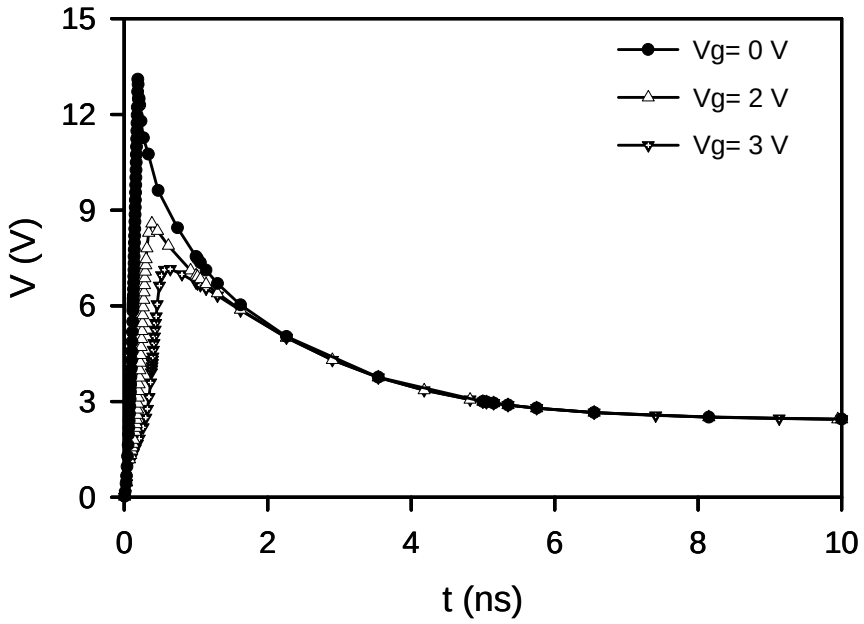
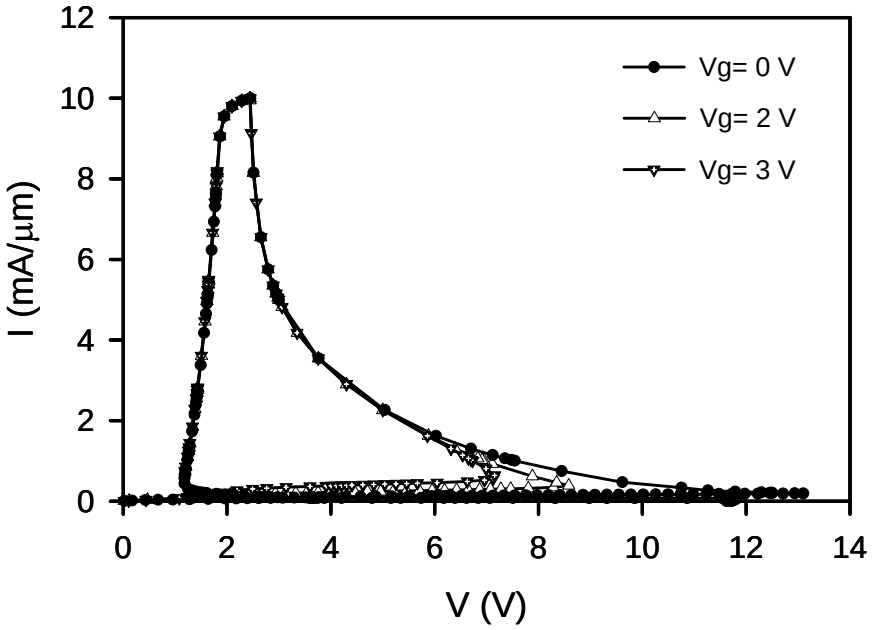


Figure 4.14. Steady-state simulation results and predicted holding voltage shifting for 2D structure in Figure 4.13 when different dimensions D are used.

A second simulation experiment accomplished using the structure in Figure 4.13 illustrates the voltage and current-voltage transient response in the device when the waveform shown in Figure 2.6 is applied to the anode of the 2D structure and the gate voltage is changed. The intention of this transient simulation was to evaluate the change obtained in the trigger voltage by applying different voltage in the gate. Note in Figure 4.15 (a) and (b) the predicted control in the trigger voltage, feature that is more critical for the ESD protection in small dimension CMOS technologies, in which the design windows are very narrow and high trigger voltages can lead to ineffective protection of the thin gate oxide dielectric during an ESD event. The characteristics shown in Figure 4.15 (b) not only provided the tendency of the trigger voltage level under different conditions, but also predicted the evolution of the device, starting from off-state, reaching triggering, turning-off decay and minimum on-state holding condition. This plot provided very relevant information for the design and optimization of SCR-type protection devices required to operate within stringent design windows.



(a)



(b)

Figure 4.15. Transient simulation a) voltage-time and b) current-voltage for the 2D structure in Figure 4.13 when different gate voltage are applied.

Additional research and optimization of the device performance, or even new developments in other CMOS technologies can follow a similar analysis and design methodology. Thereby, information can be gathered to investigate device structures for ESD design, regardless of the constraints imposed by the limited information about the specific process or technology.

4.5. Chapter Remarks

Monolithic integration of an ESD protection scheme for a microhotplate-based gas sensor SoC has been demonstrated as well as simulation methods that can be used to investigate new protection devices in sub-micron CMOS tecnologies. SCR-type devices were developed for custom implementation of ESD protection elements at the I/O pads, power rails, and gas sensor electrodes. A multifinger layout scheme was also developed to integrate the protection devices and obtain the required ESD protection level under the constraint of chip size. The ESD

protection design methodology was tested and verified at both, the device and SoC levels, and its effectiveness and robustness have been illustrated in the CMOS technology being used in the ES-SoC development. Experimental results showed that the SoC passed a 4.1 kV HBM ESD stress with no latchup induced and a very low leakage current of 10^{-10} A.

CHAPTER 5
TCAD METHODOLOGY FOR CUSTOM ELECTROSTATIC DISCHARGE (ESD) PROTECTION DESIGN

Reliability of integrated circuits (ICs) is considered one of the most important benchmarks in the semiconductor industry. Some of the reliability issues are related to the lifetime of the circuit operating under normal conditions, and others are associated with the capability of the IC to safely withstand random stress conditions, such as the electrical overstress/electrostatic discharge (EOS/ESD) events [100], [116].

As the dimensions of the semiconductor devices continue to scale down [19], [103], circuit design considerations are becoming more stringent and so are the on-chip ESD protection structures. Modern ICs are increasingly susceptible to ESD-induced damages, and the existing ESD design approaches must be continuously evolving and improving [109]. The development of ESD protection solutions, however, traditionally relies on a trial-and-error process and thus is time consuming and cost ineffective. Designing ESD devices based on numerical simulations and reduced experiments in silicon, on the other hand, is more desirable and advantageous [33], [35], [79], [81].

Technology CAD (TCAD) simulations of ESD elements have been mainly accomplished to assess the grounded gate MOSFET (ggMOS) in different technologies [13], [34], [37], [75]. This stems from the fact that the ggMOS has traditionally been the most widely used ESD device. However, certain applications require customized and advanced ESD devices with complex structures that not only are difficult to simulate, but also necessitate ample computational resources [87], [91], [106]-[107]. In addition, divergence often is a hindrance for the widespread

use of the TCAD, particularly for ESD designs and evaluations, due to the rapid change of the boundary conditions in the snapback region. Consequently, as the technology evolves toward more stringent requirements and more complex ESD applications, there is a need for the development of a TCAD methodology from which advanced ESD devices can be designed and optimized in a simulation environment [92].

In this chapter, a practical TCAD methodology based on a process/device simulator is developed for the design and implementation of custom silicon controlled rectifier (SCR)-type devices for ESD applications. The background of the ESD protection devices considered in this study and the TCAD fundamentals are first introduced. Key junctions in the protection devices are then targeted to obtain relatively simple 2D structures that require much less simulation time, have less problems of numerical divergence, and provide better insight into the ESD requirements than the full version of the device. Custom design of ESD protection devices based on the TCAD methodology is then carried out and subsequently verified against measurements.

5.1. Custom SCR Devices for ESD Protection

The main goal of ESD protection devices is to provide a low-impedance discharge path during an ESD event, and at the same time, a minimal interaction with the core circuit during the normal operation. Realistically, all ESD devices have their intrinsic limitations and parasitics that not only affect the core circuit integrity, but also degrade the robustness of ESD protection.

In order to attain effective and optimum ESD protections for various applications, it is commonly necessary to depart from the traditional approaches [25] and to explore new structures. From the discussion in previous chapters, one of such structures is an SCR-like device. In this chapter, new devices that do not incorporate the gate and can be extended to high

operating voltage are developed. Figure 5.1 shows a fully customizable ESD protection structure recently proposed [83]. Both the cross-sectional view, including the key regions identified as the FBJ (forward blocking junction) and RBJ (reverse blocking junction), and the equivalent circuit are depicted in the figure. This device will be used as an example to illustrate the development of the TCAD methodology, but the simulation approach described below applies in general to other advanced ESD protection devices.

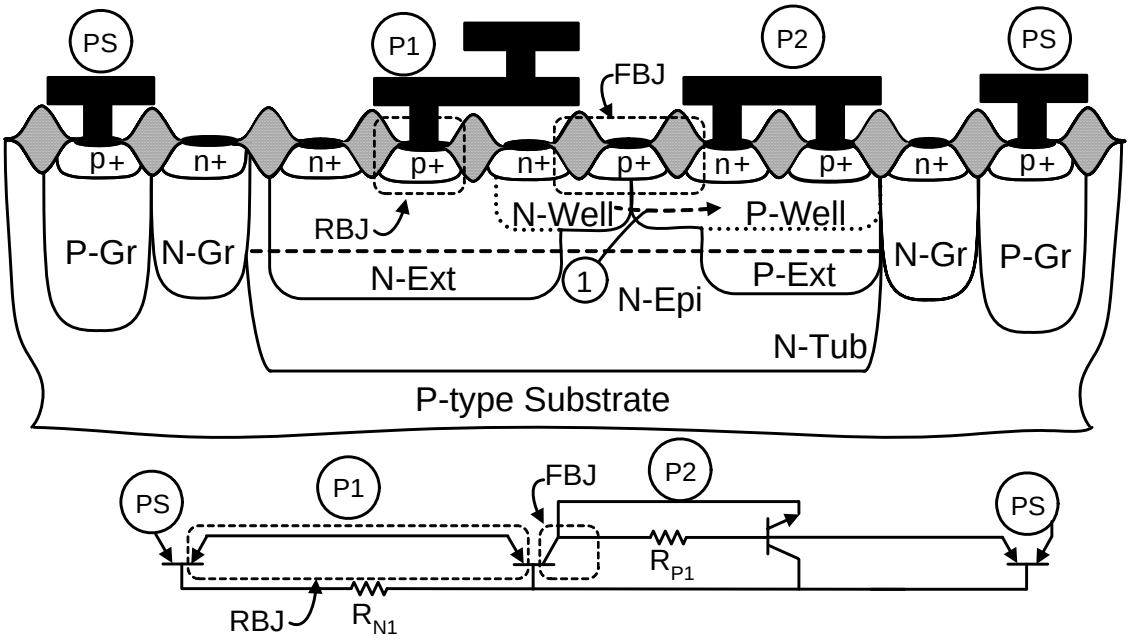


Figure 5.1. Cross-sectional view and equivalent circuit of a P_1N_1-P_2N_2 structure, with the forward and reverse blocking junctions (FBJ and RBJ) indicated.

The device shown in Figure 5.1 is capable of producing single-polarity S-type current-voltage characteristics (i.e., it exhibits snapback behavior in the forward direction, indicated with number 1, and junction breakdown-type behavior in the reverse direction) [80], [83]. It can basically be separated into two subsections; P_1N_1 (P+ and N-well) on the left and P_2N_2 (P-well and N+) on the right. Two types of junction are important in controlling the forward- and reverse- conduction, namely the forward- and reverse- blocking junction (see Figure 5.1). Once

the different configurations of these junctions in the device are identified and simulated, the key performance of this relatively complex device can be predicted. This information is subsequently used for optimizing and implementing the P_1N_1-P_2N_2 structure.

5.1.1. Forward Blocking Junction

The forward blocking junction (FBJ) in the P_1N_1-P_2N_2 structure is formed in the middle region of the device, between the N- and P-well (see Figure 5.1). Figure 5.2 shows three FBJ configurations that could be fabricated in standard CMOS/BiCMOS technologies [80], [83]. The forward blocking voltage can be adjusted by the different combinations of the doping implantations [10], silicide blocking layers and/or isolation layers available in the predetermined fabrication process. The dimensions *dx*, *dxn*, and *dxp* indicated in Figure 5.2 allow for further adjustment of the blocking voltages. In other words, different blocking voltages can be obtained by using different FBJ configurations and/or different *dx*, *dxn*, and *dxp*. Note that such a blocking voltage determines the forward trigger voltage for the snapback of the ESD device.

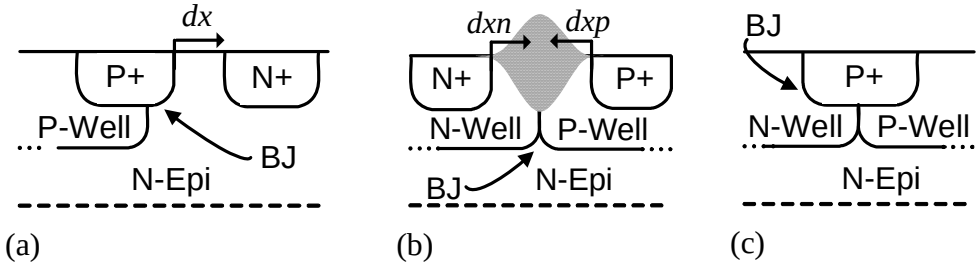


Figure 5.2. Examples of forward blocking junction (FBJ) configurations.

5.1.2. Reverse Blocking Junction

The reverse blocking junction (RBJ) is formed between the outermost p-region (PS) and the electrode (P1), and between the electrodes (P2) and (P1) (see Figure 5.1). Figure 5.3 shows two

reverse blocking junction (RBJ) configurations examples for adjusting the reverse blocking voltage of the structure shown in Figure 5.1. Such a voltage determines the breakdown voltage in the reverse conduction. This voltage is critical on the ESD design because in many IC applications I/O (input/output) voltages are operated below V_{SS} (negative power rail), and the ESD protection device is normally required to block a relatively large reverse voltage.

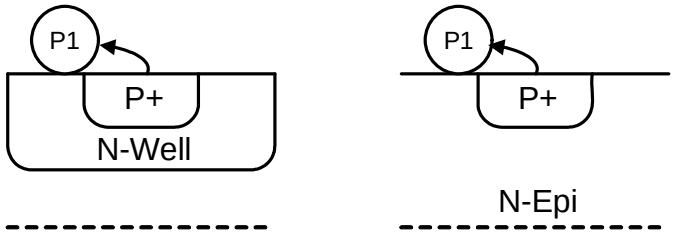


Figure 5.3. Examples of reverse blocking junction (RBJ) configurations.

5.2. Technology CAD Simulation for ESD Design

Following the discussion in chapter 2, the TCAD simulation in this study is conducted using Silvaco software tools. Two different methods can be used for describing the 2D doping profiles of a device needed in a simulation environment. The first uses analytical functions to empirically define the doping distributions [7]. This method is less effective in advanced technologies where the lateral doping densities are critical and complex 2D doping distributions and isolation regions are incorporated. The second method generates the 2D doping profiles directly from the simulation of the actual fabrication process (i.e., process simulation) [8]. The device structures obtained from the process simulation are then imported into a device simulator [7] for the simulation of device electrical characteristics. The second method is chosen for this study.

5.2.1. Device Simulation Models

As was discussed in chapter 2, the TCAD device simulator uses a set of discrete fundamental equations, which correlate the electrostatic potential and carrier density within a finite element grid. These fundamental equations consist of the Poisson's equation, free-carrier continuity equations, and free-carrier transport equations [101]. Beside the fundamental equations, physics pertinent to ESD mechanisms need to be included.

During an ESD event, the protection device is subject to a high electric field and high temperature. To account for these effects, chapter 2 discussed the physical models employed in this study. Once these models are selected, the simulation is then calibrated by adjustment of the models' parameters using the procedures proposed in [34]. Basically, the calibration of the TCAD simulation consists of two steps 1) calibration of the process simulation and 2) calibration of the device simulation. Calibration of the process simulation has been accomplished by comparing data gathered from SIMS (secondary ion mass spectrometry) analysis with doping profiles obtained from the process simulation [21].

This calibration step allows for an accurate estimation of the impurities distribution in different regions generated from the TCAD tool. For the device simulation calibration, one of the most important parameters for estimating the breakdown voltage in the ESD simulation is the impact ionization model, which is discussed in chapter 2. Another important parameter is the free-carrier lifetime model governing by the Auger and Shockley-Read-Hall recombination processes. Parameters associated to these phenomena need to be adjusted so that a good correlation between the simulated and the measured ESD characteristics can be obtained. Finally, the selection of appropriate meshes is also of great importance, since there is a trade-off between the mesh density and simulation time. A denser mesh results in a more accurate simulation and

less likelihood of divergence, but it requires a longer simulation time. As such, it is a common practice to define denser meshes in the critical regions, e.g., the vicinity of the metallurgical junctions, and more relaxed meshes elsewhere.

5.2.2. Blocking Junctions Simulation

As discussed earlier, the FBJ and RBJ junction configurations influence the triggering and reverse conductions, respectively, of the P_1N_1-P_2N_2 structure. Examples of possible FBJ and RBJ configurations have been depicted in Figure 5.2 and Figure 5.3. Calibrated TCAD simulation results and measured data for the breakdown behavior of the FBJ and RBJ are compared in Figure 5.4 and Figure 5.5, respectively. A good agreement between the simulation and measurements is found. For the case of the FBJ (a) configuration in Figure 5.4, a large *dx* is selected such that interaction of the two highly doped regions separated by *dx* can be omitted.

Figure 5.6 shows simulated current-voltage characteristics of FBJ (a) (see Figure 5.2) having different *dx*. It can be seen that different blocking voltages are predicted for different lateral dimensions. This is because changes in the inter-well distance modify the space charge region and electric field in the junction. To illustrate this, Figure 5.7 shows the impact generation rate as a function of *dx* changing from 0 to 1.6 μm. When *dx* is reduced, the space-charge region decreases and the peak of impact generation rate increases. This leads to a lower blocking voltage.

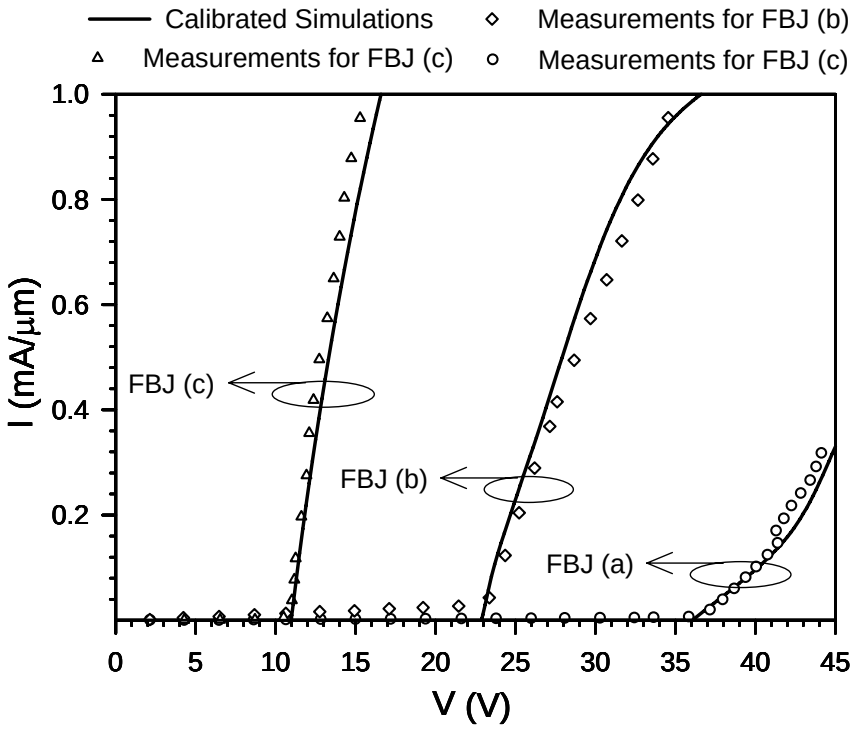


Figure 5.4. TCAD simulation results and TLP measurements of the breakdown behavior for the three different forward blocking junctions in Figure 5.2.

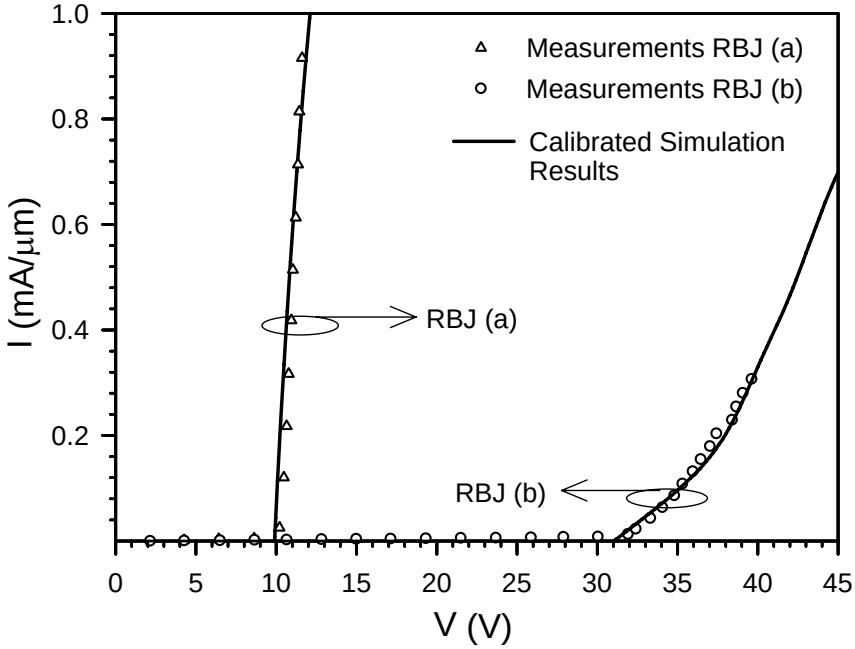


Figure 5.5. TCAD simulation results and TLP measurements of the breakdown behavior for two different reverse blocking junctions in Figure 5.3.

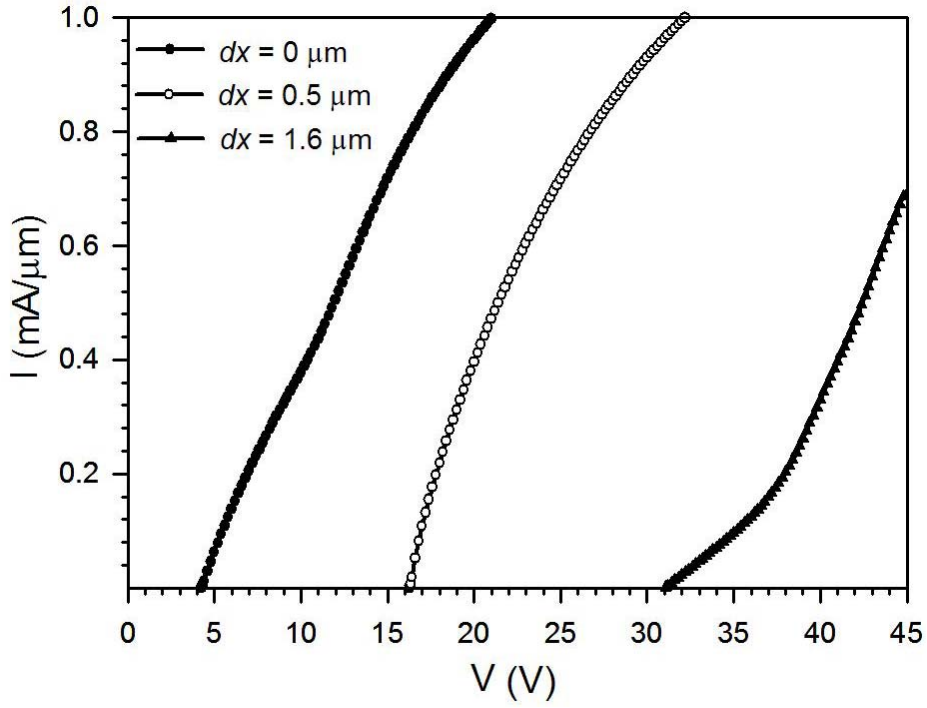


Figure 5.6. TCAD simulation results of the breakdown behavior for the FBJ (a) configuration in Figure 5.2 with three different dimensions *dx*.

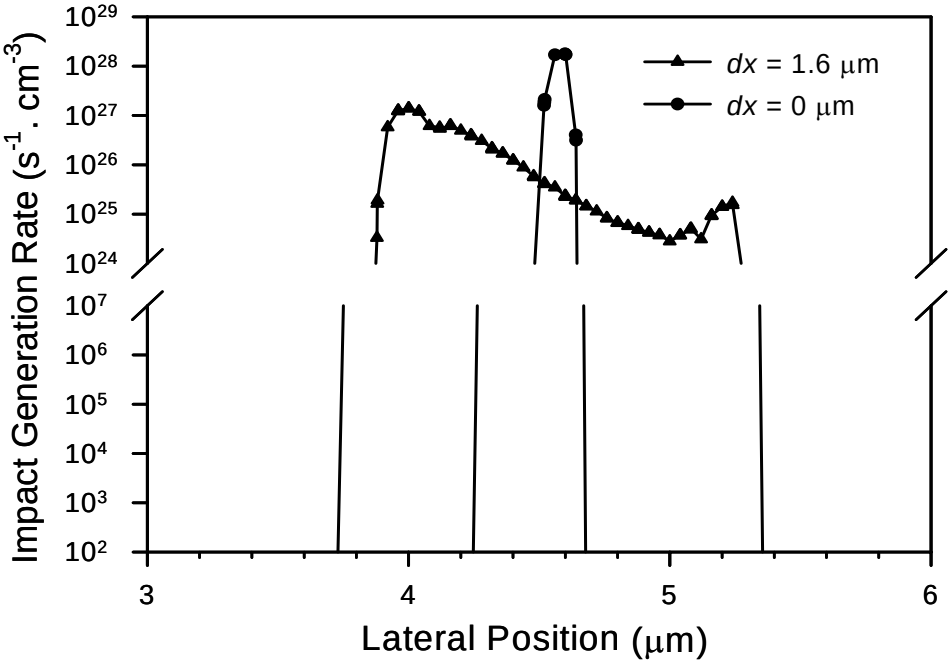


Figure 5.7. Impact generation rate obtained at a vertical position of -2.9 μm (see Figure 5.8) in FBJ(a) having two different dimensions *dx* (see Figure 5.2).

The current density and lattice temperature contours, shown in Figure 5.8 and Figure 5.9, respectively, give further insights into the junction behavior. The results are simulated for the FBJ (a) with dx = 0.5 μm. A maximum current density, and thus a maximum lattice temperature take place near the surface. This is not desirable, as high current density (darker contours) and resulting hot-spot located close to the surface can induce early failure. This condition is one of the main factors limiting the robustness of the ESD device. As will be shown later, this problem can be minimized when the FBJ is implemented into the P_1N_1-P_2N_2 structure.

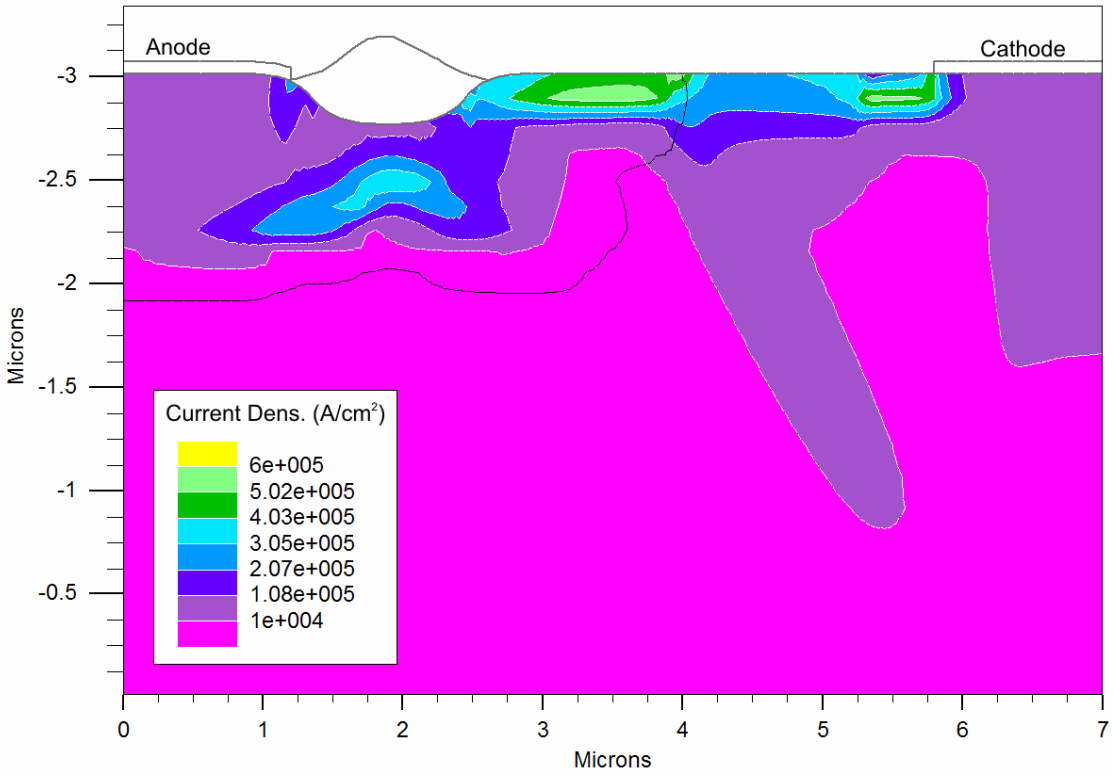


Figure 5.8. 2D current density contours simulated after the breakdown voltage for FBJ (a) in Figure 5.2.

The preceding simulation of the blocking junctions serves as a first step in the TCAD design of more complex and complete ESD protection structures. However, a complete ESD device with the forward and reverse blocking junctions incorporated exhibits snapback behavior (S-type

I-V characteristics), and additional effort is necessary to ensure successful TCAD simulation for such a device. In the next section, an algorithm called the *curvetracer* used in this work to address the divergence problems during the simulation of S-type I-V characteristics is discussed.

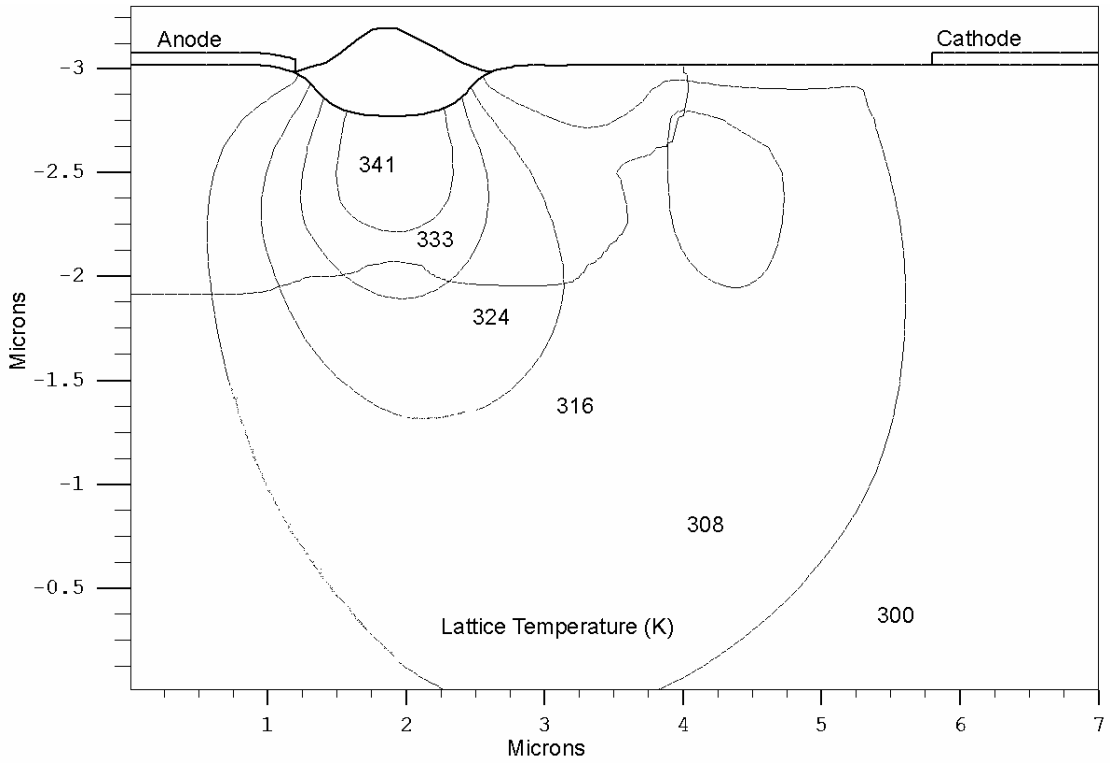


Figure 5.9. 2D lattice temperature contours simulated near the breakdown voltage for FBJ (a) in Figure 5.2.

5.2.3. Curvetracer Algorithm

In a TCAD environment, the S-type I-V characteristics are difficult to simulate in the sense that there are: 1) flat regions where the magnitude of the current experiences small changes with voltage, 2) steep regions where the current rises rapidly with voltage, and 3) snapback regions where the slope of the I-V curve changes sign and multiple current solutions at a particular voltage exist. Simulating these characteristics with traditional methods is computationally difficult because the boundary conditions must be continuously changed to maintain stability and

convergence. From a numerical point of view, the voltage boundary condition (VBC), with the voltage being swept, is stable if the current does not change abruptly with the applied voltage. On the other hand, the current boundary condition (IBC), with the current being swept, is effective if the voltage necessary to sustain a given current does not vary too much with the current. These observations are graphically illustrated in Figure 5.10. The numerical solution using the voltage boundary condition is equivalent to finding the point on the I-V curve with the vertical line defined by the voltage value, whereas the current boundary condition solution is represented by the intersection of the I-V curve with the horizontal line. In general, a solution is stable when the line defined by the boundary condition is perpendicular to the local part of the I-V curve. Thus, the sloped line, which represents a voltage or current source with an internal load (VLBC), gives the ideal boundary condition for the intermediate part of the hypothetical I-V curve shown in Figure 5.10.

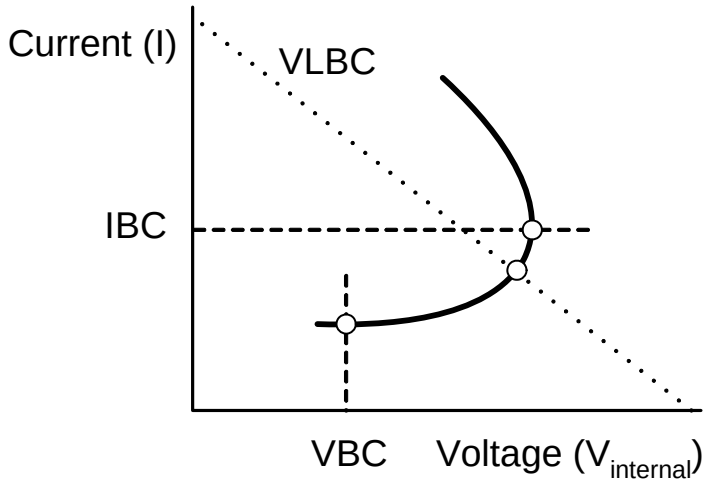
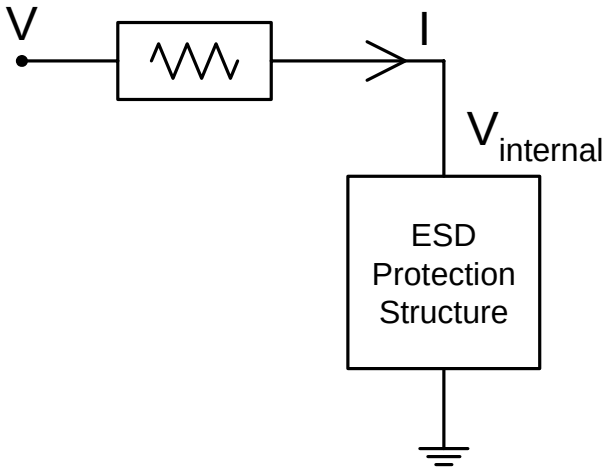


Figure 5.10. Schematic showing the different boundary condition specifications for numerical simulation: current boundary condition (IBC), voltage boundary condition (VBC), and variable load boundary condition (VLBC)

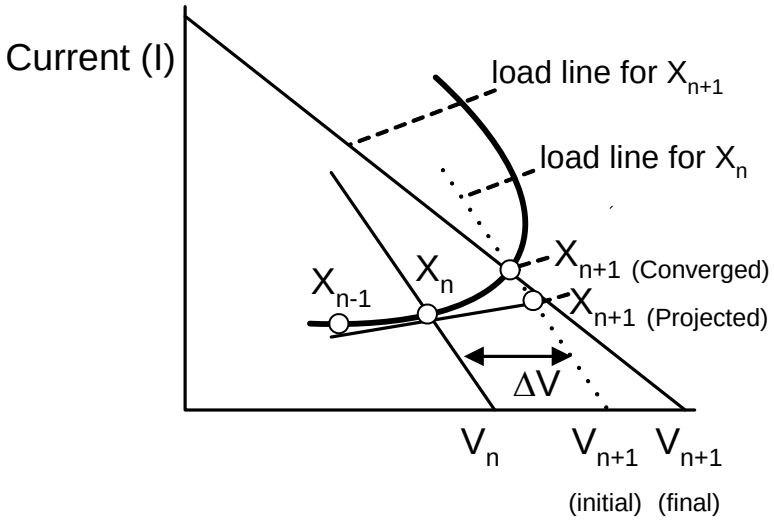
The VBC or IBC approaches do not work for the simulation of the I-V curve in the vicinity of snapback due the issues mentioned in the beginning of this section. To guarantee better convergence throughout the numerical calculations [41], an algorithm called the *curvetracer* is incorporated in the simulation [7]. This algorithm changes from pure voltage or pure current control by using a voltage or current source with an external load which changes at each solution point to keep the load perpendicular to the local section of the curve.

Figure 5.11 (a) shows a schematic representation of the *curvetracer* algorithm, which includes a variable load, variable voltage source, and intrinsic voltage at the device terminals ($V_{internal}$). Once a solution point (X_n) is found using an external voltage source and a load resistance which yield a perpendicular load line, the initial guess of the next point ($X_{n+1\ (Projected)}$) is projected on the I-V curve by increasing the external voltage along the tangent of the known solution point (X_n). Then, based on the initial guess ($X_{n+1\ (Projected)}$) obtained over a parallel load slope (dotted line) the actual solution point is found ($X_{n+1\ (Converged)}$). Once the converged point is known ($X_{n+1\ (Converged)}$), the next point is found by adjusting to a new load resistance and external voltage that yield a load line perpendicular to the actual solution ($X_{n+1\ (Converged)}$), and the algorithm loop repeats the previous steps, see Figure 5.11 (b).

This projection scheme requires input parameters related to the minimum error and voltage steps, so it keeps track of the turning points to ensure that the external voltage is projected in the right direction [41]. Since the *curvetracer* algorithm requires more iteration and computation time, the simulation input deck is defined to initially solve for the flat region (region before the snapback) using the VCB until the trigger voltage is approached. This is followed by the activation of the *curvetracer* algorithm for the simulation of snapback behavior. ICB is then used for the post-snapback region.



(a)



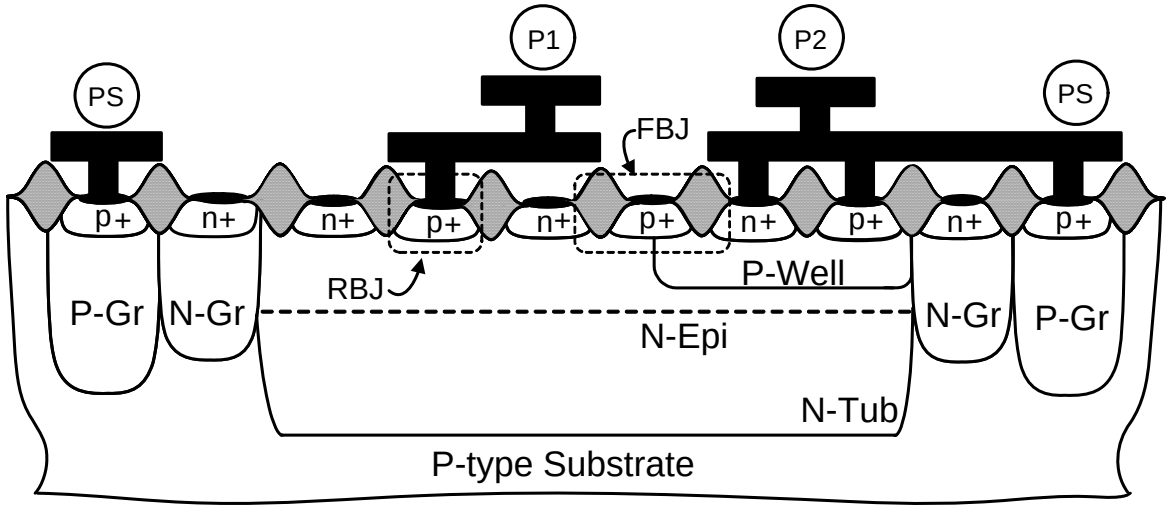
(b)

Figure 5.11. (a) Schematic of the ESD protection device with variable voltage and load conditions, and (b) procedure for adaptation of the load line along the I-V curve to address convergence issues.

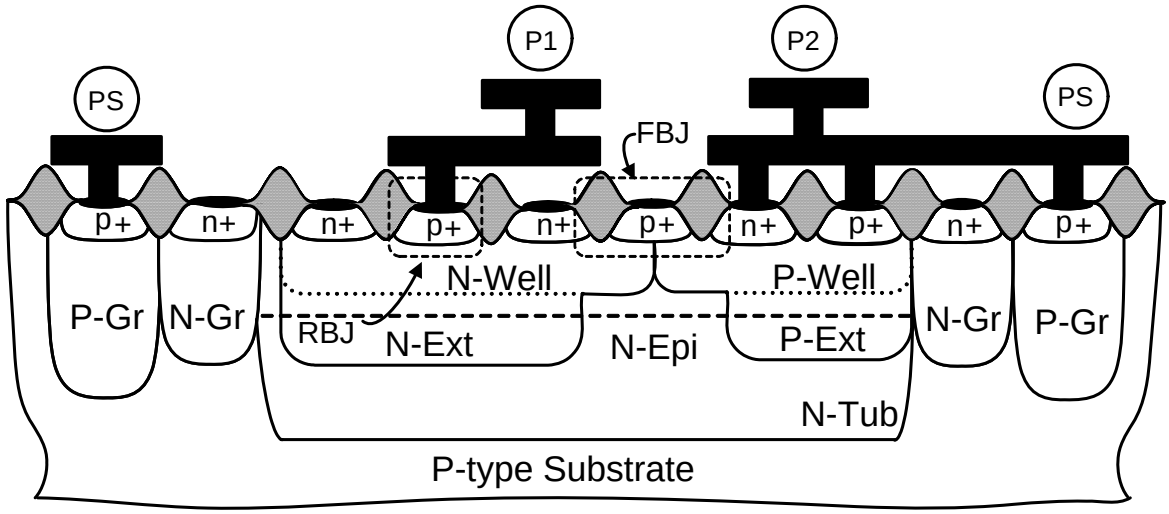
5.2.4. Design and Simulation of Complete ESD Protection Device

The TCAD methodology for the simplified FBJ and RBJ developed above is highly helpful for putting together a complete P_1N_1-P_2N_2 structure (see Figure 5.1) with certain desirable forward trigger and reverse breakdown voltages. In the next discussion is considered the case of designing two ESD structures, one (Device A) with relatively large trigger and breakdown

voltages and the other (Device B) with relatively small trigger and breakdown voltages. These requirements, together with the simulation results obtained from the different FBJ and RBJ configurations, lead to the construction of the two devices that combine different forward- and reverse- blocking junction configurations as shown in Figure 5.12 (a) and Figure 5.12 (b). The device in Figure 5.12 (a), which satisfies the requirement of Device A, incorporates FBJ (a) in Figure 5.2 and RBJ (b) in Figure 5.3, whereas the device in Figure 5.12 (b), which satisfies the requirement of Device B, includes FBJ (c) in Figure 5.2 and RBJ (a) in Figure 5.3. Both structures are fabricated using a submicron silicided CMOS/BiCMOS technology at IBM. The terminals interconnection considered for the characterization and simulation of these devices is also shown in Figure 5.12, where P1 is defined as the forced pad, while P2 and PS are connected to the ground reference.



(a)



(b)

Figure 5.12. Cross-sectional views of two different P_1N_1-P_2N_2 devices incorporating a) FBJ (a) and RBJ (b) configurations for relatively large forward trigger and reverse breakdown voltages and b) FBJ (c) and RBJ (a) configurations for relatively small trigger and reverse breakdown voltages.

Firstly, the forward conduction and the trigger voltage of the device in Figure 5.12(a) are analyzed. Figure 5.13 shows the S-type I-V characteristics simulated from this device and the FBJ (a) configuration alone having different dimensions *dx*. As can be seen, a main difference between the two structures is that the P_1N_1-P_2N_2 array depicts snapback behavior, but the FBJ configuration does not. However, the simulation results show a trend consistent with the earlier statement that the trigger voltage of the P_1N_1-P_2N_2 structure is determined by the blocking junction voltages of the simplified FBJ, an assumption that reduces the simulation complexity and expedites considerably the design process. Figure 5.14 and Figure 5.15 show the on-state current density and lattice temperature contours, respectively, for the device considered in Figure 5.12 (a) having the FBJ (a) configuration and dx = 0.5 μm. Unlike the current density contour in Figure 5.8, the current density in the P_1N_1-P_2N_2 structure is now distributed well below the surface, thus even at a comparatively higher current density the corresponding hot-spot is obtained at relatively lower lattice temperature and it is now located deep in the bulk. This

allows the ESD device to discharge significantly higher current per unit area with less likelihood of being damaged during the stress condition. The enhanced robustness results directly from the dual-injection of carriers [84] on the P_1N_1-P_2N_2 structure, induced by the presence of additional n+ regions next to the FBJ, and the interaction of the forward and reverse blocking junctions embedded in such a device.

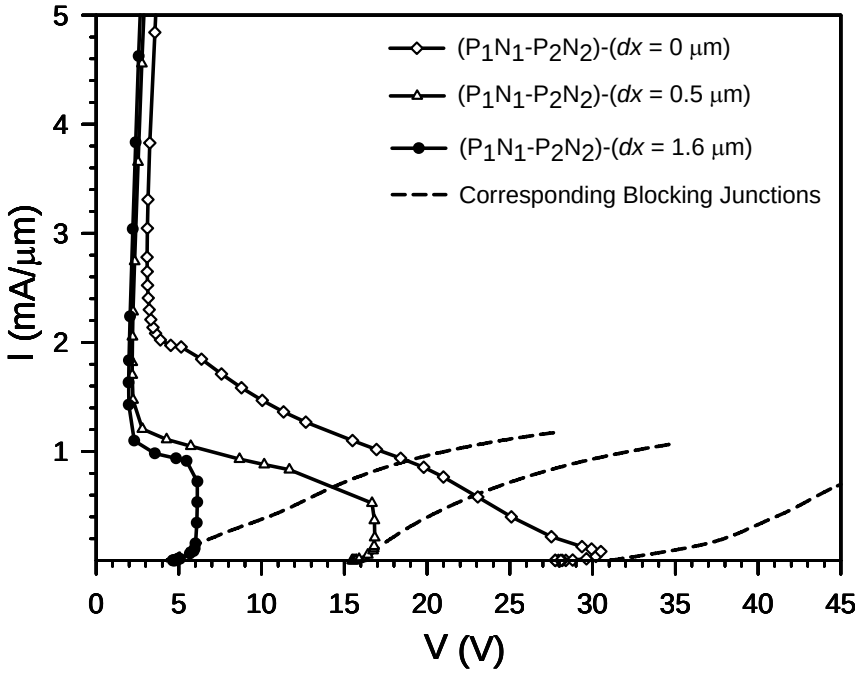


Figure 5.13. Simulated forward I-V characteristics for the complete ESD device in Fig. 12(a) and the simple forward blocking junction (FBJ (a) in Figure 5.2) having different dimensions *dx*.

Secondly, the implementation of the two ESD devices in Figure 5.12 (a) and (b) is examined and verified. Figure 5.16 compares the TCAD simulated and TLP measured I-V curves of these devices operating in both the forward and reverse ESD conductions. The results verify that the two devices meet the trigger and breakdown voltages requirements specified earlier. Moreover, it is demonstrated that the methodology developed in this work yields an accurate prediction of the ESD behavior and thus reduces significantly the development cycle and the amount of iteration in silicon.

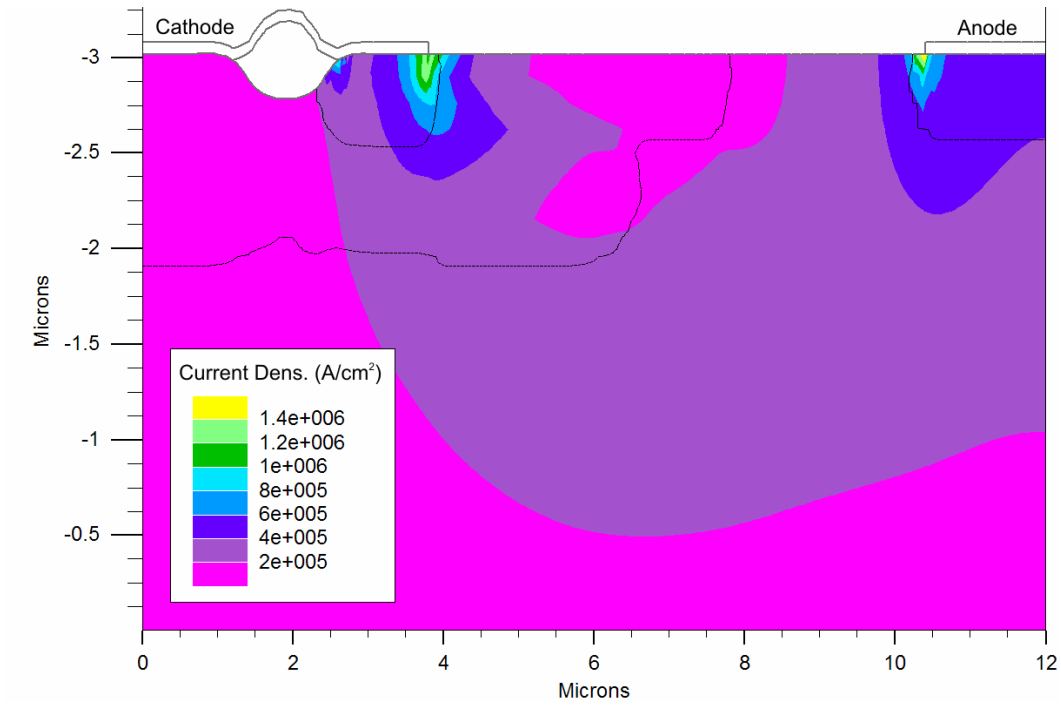


Figure 5.14. 2D on-state current density contours of a P_1N_1-P_2N_2 structure constructed based on the FBJ (a) configuration.

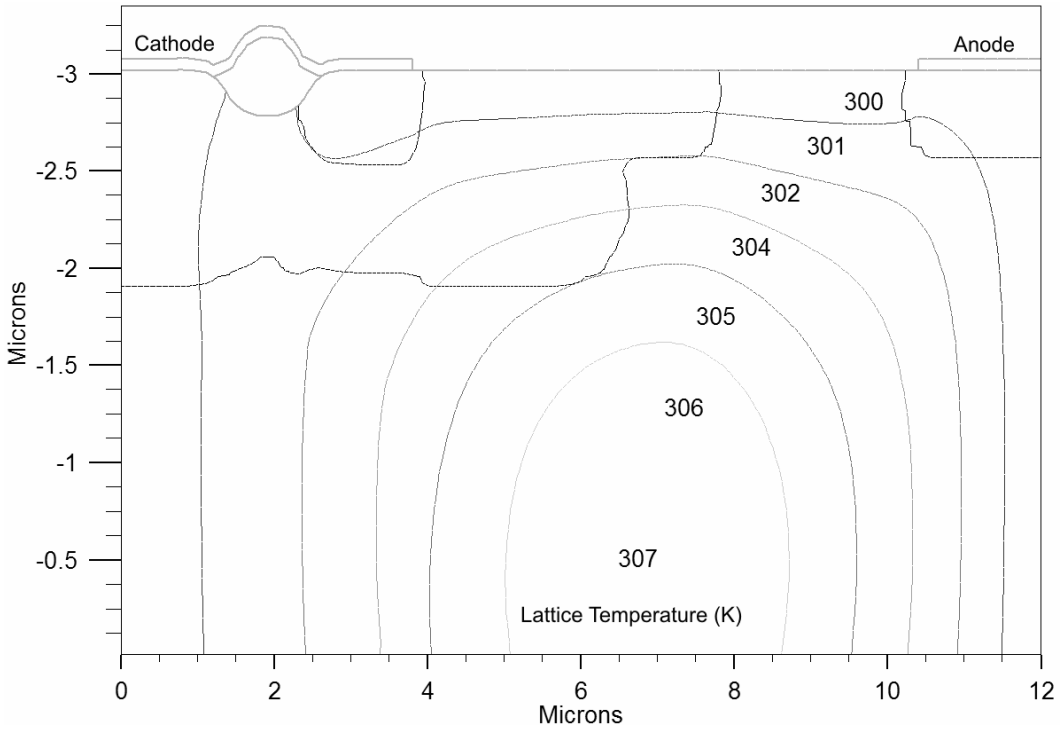


Figure 5.15. 2D lattice temperature contours of a P_1N_1-P_2N_2 structure constructed based on the FBJ(a) configuration.

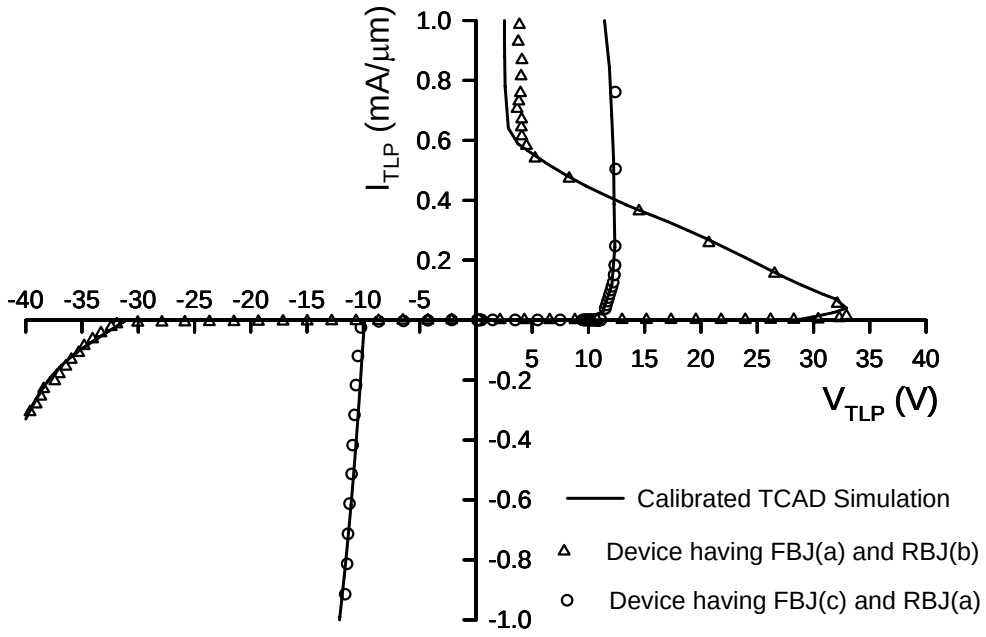
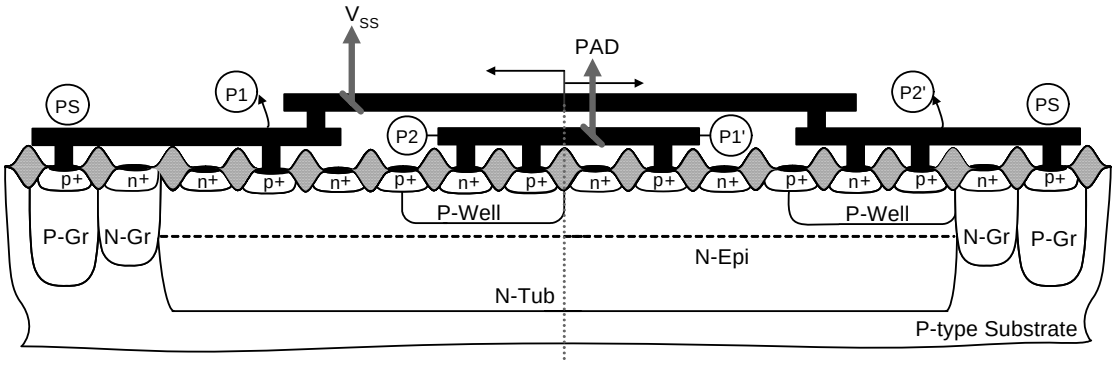


Figure 5.16. Simulated and measured S-Type I-V characteristics for two ESD devices having different combinations of forward and reverse blocking junctions.

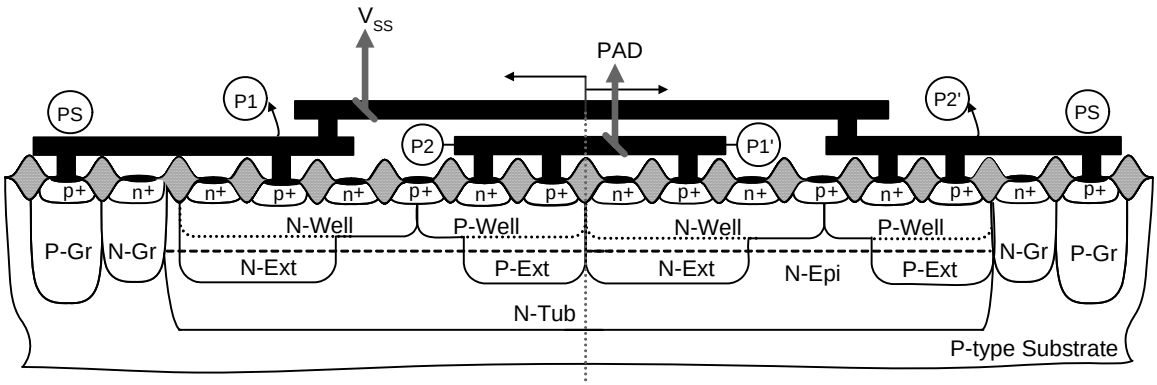
The above approach for the design of the P_1N_1-P_2N_2 structure can be readily extended to the implementation of a dual-polarity ESD device having snapback in both the forward and reverse ESD conductions [80]. Such a device, which possesses the advantage of allowing bi-directional ESD conductions, can be constructed in general by coupling the P_1N_1-P_2N_2 structure with a complimentary N_2P_3-N_3P_1 structure (i.e., P_1N_1-P_2N_2//N_2P_3-N_3P_1 device). The right-hand side P_1N_1-P_2N_2 and left-hand side N_2P_3-N_3P_1 cells produce the forward and reverse snapbacks, respectively. An extension of these results and implementation of devices for actual IC applications is discussed in chapter 6.

The cross-sectional view for two examples of symmetric dual-polarity P_1N_1-P_2N_2//N_2P_2-N_1P_1 devices constructed based on the junction configurations used in the single-polarity device in Figure 5.12 (a) and Figure 5.12 (b) are depicted in Figure 5.17 (a) and Figure 5.17 (b), respectively. Because of the structures size and complexity, TCAD simulation of these devices is even more difficult and time consuming than that of the single-polarity P_1N_1-P_2N_2 structures.

Nevertheless, as will be discussed in the next chapter, the dual-polarity devices are formed by superposition of the characteristics obtained from two single-polarity P_1N_1-P_2N_2 and N_2P_3-N_3P_1 cells. Thus, the TCAD simulation can be carried out for each cell individually, and the simulated results are then defined by addition in current (I_{TLP}) within the limits of the lower conducting voltage (V_{TLP}). It allows for a good estimation of the dual-polarity S-type I-V characteristics. This concept is illustrated in Figure 5.18 and Figure 5.19, where the characteristics of the two individual single-polarity cells obtained from TCAD simulations, having high- and low- trigger voltage, respectively, are illustrated along with the predicted dual-polarity conduction and the dual-polarity characteristics obtained from measurements. The snapbacks in both the forward and reverse conductions are demonstrated. The dual-polarity ESD devices fabricated using a multifinger array [81] occupy an average area of 200 x 230 μm^2 and have been successfully incorporated in different commercial applications that require a system-level ESD immunity of over 15 kV as defined by the IEC-1000-4-2 standard [31]. Thus, the examples given above have indicated that based on the information for the simplified blocking junctions derived from the TCAD methodology, one can directly design and optimize both the single- and dual-polarity structures for various ESD triggering requirements.



(a)



(b)

Figure 5.17. Schematics of dual-polarity ESD devices constructed based on a) the junction configurations used in the single-polarity device in Figure 5.12 (a) and b) the junction configurations used in the single polarity device in Figure 5.12 (b).

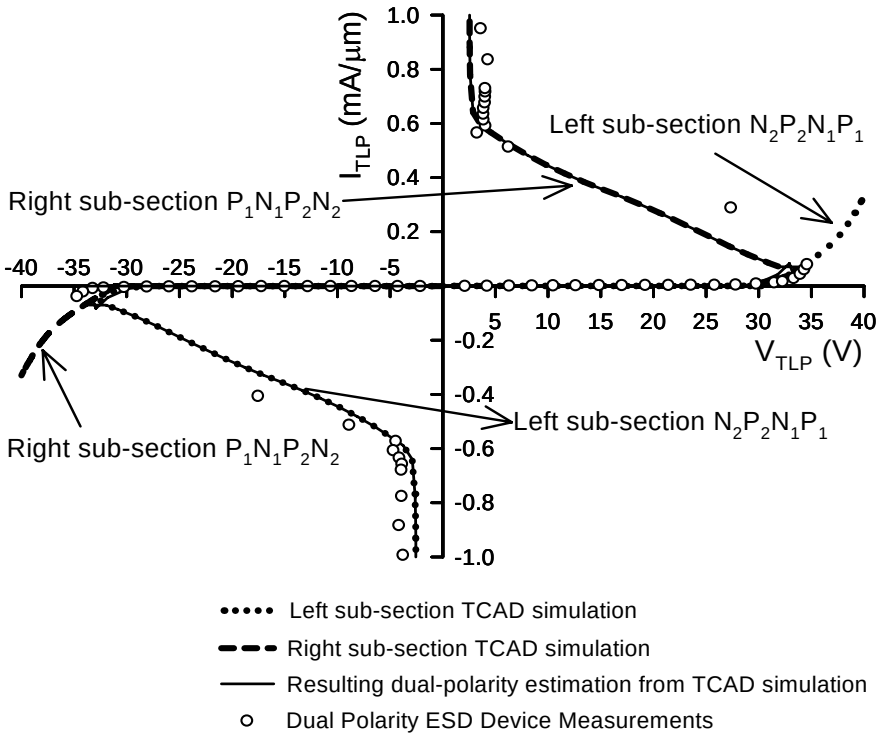


Figure 5.18. 1) TCAD simulations of forward- and reverse- conduction of two individual single-polarity cells, one with forward conduction (snapback) for the negative side (left sub-section), and the other with forward conduction (snapback) for the positive side (right sub-section), 2) the resulting high-trigger dual-polarity characteristics obtained from superposition of the single section characteristics, and 3) normalized measurements of dual-polarity S-type I-V characteristics obtained from the structure in Figure 5.17 (a).

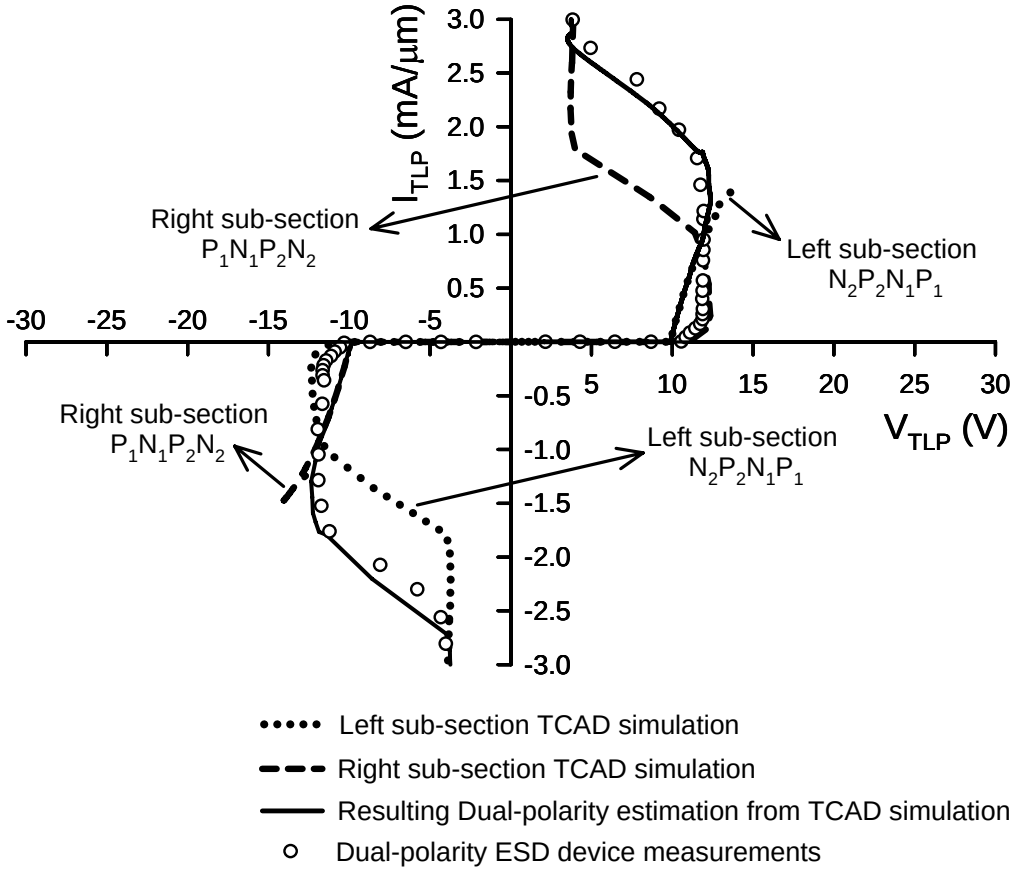


Figure 5.19. 1) TCAD simulations of forward- and reverse- conduction for two individual single-polarity cells, one with forward conduction (snapback) for the negative side (left sub-section), and the other with forward conduction (snapback) for the positive side (right sub-section), 2) the resulting low-trigger dual-polarity characteristics obtained from superposition of the single section characteristics and 3) normalized measurements of dual-polarity S-type I-V characteristics obtained from the structure in Figure 5.17 (b).

5.3. Chapter Remarks

The increasingly stringent requirements for on-chip electrostatic discharge (ESD) protection solutions are often main roadblocks in the successful realization of microchips. This is further compounded by the fact that ESD designs are very complex and demanding. A practical and useful TCAD simulation methodology has been discussed in this chapter to assist in the optimization and implementation of ESD protection devices. Divergence in TCAD simulation associated with the presence of snapback behavior of the ESD device was addressed with the use

of the *curvetracer* algorithm. Key blocking junction configurations were identified to simplify the TCAD simulation and provide insight about the ESD characteristics. The design and implementation of several advanced ESD devices based on TCAD simulations were also carried out and verified with experimental data.

CHAPTER 6
IMPLEMENTATION OF STRUCTURES WITH DUAL-POLARITY SYMMETRICAL/ ASYMMETRICAL S-TYPE I-V CHARACTERISTICS FOR ESD PROTECTION DESIGN

The downscaling of device dimensions and increasing circuit complexity in advance mixed-signal technologies have originated microchips that are highly sensitive and susceptible to ESD (electrostatic discharge) events [83]. To provide the necessary on-chip ESD protection, chapter 1 showed that tailored devices are placed at the input/output pads and between the power rails in order to prevent the core circuit from being damaged by ESD stress. Due to the high current associated with the ESD event, typical protection structures normally occupy a large portion of the chip area in advanced technology. Increasing the dimension of the ESD devices, however, can cause non-uniform conduction [4]. Furthermore, as discussed in previous chapters, such an approach does not always guarantee that a certain level of protection can be achieved.

Custom devices have been reported in the literature to provide smaller and more effective ESD protection solutions, and one of these devices is the unidirectional SCR (silicon controlled rectifier). However, SCR problems discussed in previous chapters and adjustment of the device characteristics to the plethora of mixed-signal applications are still challenges for the use of the SCR-based ESD devices. Wang et al., [120] proposed an improved ESD protection with a custom NPNPN five-layer structure, which allows for symmetrical bidirectional I/O pad ESD protection using a single device. A limitation of this approach is the lack of a methodology for adjusting the forward and reverse I-V characteristics.

In this chapter, the dual-polarity concept introduced in chapter 5 is used to develop devices aimed to provide high-level ESD protection, and relatively high conducting currents in both ESD

polarities (i.e., positive and negative ESD). The devices can be designed to provide symmetrical and asymmetrical S-type I-V characteristics with different trigger voltages, holding voltages, and conducting current capabilities. The performance of the ESD device is verified and evaluated using the transmission line pulse (TLP), human body model (HBM), machine model (MM), and International Electrotechnical Commission (IEC) 1000-4-2 standard at the device-level and once they are integrated in the actual IC application.

6.1. The ESD Protection Concept and Device Characteristics

6.1.1. Blocking Junctions Flexibility and Dual-Polarity Conduction

For reference, Figure 6.1 shows a cross-sectional view of a dual-polarity ESD protection device developed in this study. Extending the concepts previously discussed in chapter 5, the structure consists of the following two sections (indicated with the arrows in Figure 6.1): 1) right section for discharging ESD current from the pad to the power rail, and 2) left section for discharging ESD current from the power rail to the pad. An equivalent circuit of the device is also included in Figure 6.1. While the device allows for the design of each section independently, interaction between the opposite sections can affect the forward and reverse I-V characteristics.

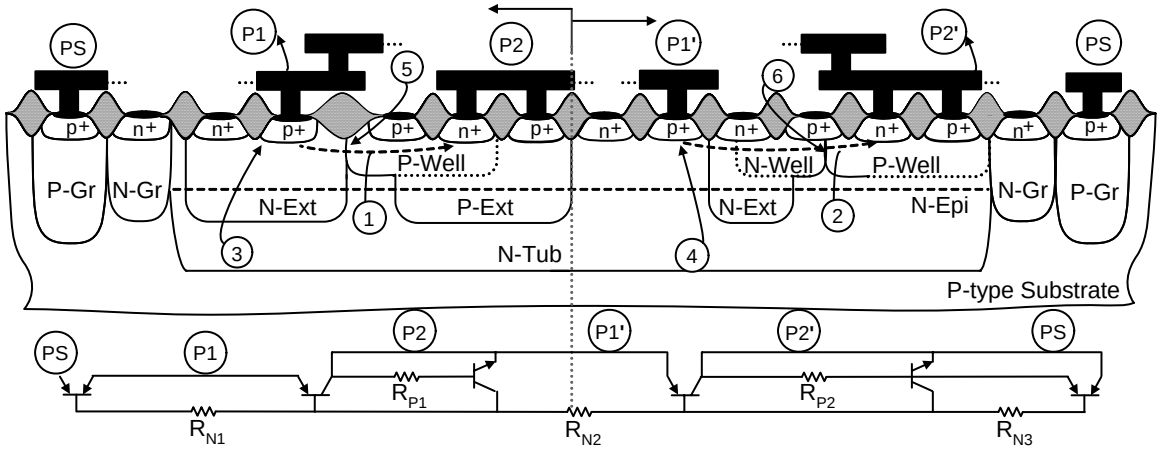


Figure 6.1. Dual-Polarity ESD Protection Device.

The current paths during the ESD conduction are labeled with the numbers 1 and 2, the four key p/n junctions are labeled with numbers 3 through 6, and five key terminals are labeled with P1, P2, P1' P2', and PS (guard ring). Consider the case of ground-referenced I/O pad protection. P1, P2', and PS are interconnected to form the first electrode (ground), and P2 and P1' are interconnected to form the second electrode (pad). Using this connection scheme, symmetrical or asymmetrical I-V characteristics are obtained from pad to ground and vice versa.

Elaborating on the analysis in previous chapters, the first step for the custom design of the symmetrical and asymmetrical S-type I-V characteristics involves the ability of adjusting the forward trigger and reverse breakdown conditions in each section of the device shown in Figure 6.1. Focusing on the left section (the same concept applies to the right section), single-section device can be designed to yield different reverse breakdown voltages BVR and forward trigger voltages V_T, see chapter 5. The junction labeled with number 3 controls the blocking voltage BVCEO, or the reverse breakdown voltage V_R, for the two open-base parasitic BJTs, one formed between the guard ring PS and P1 and the other between P2 and P1. Several junction configurations can be defined for label 3, some of them were also showed in chapter 5. An extended group of reverse blocking junctions is depicted in Figure 6.2 . Configuration (a) in Figure 6.2 yields the smallest V_R, followed by configuration (b), and configuration (c) yields the largest V_R among the three.

The forward trigger voltage V_T is adjusted using different blocking junction configurations. Extending the group of configurations showed in chapter 5, Figure 6.3 (a) through (l) shows twelve alternative forward blocking junction configurations that can be used to control trigger voltage. The breakdown of this junction is the main mechanism that defines the triggering of the regenerative feedback in the device, see junction labeled number 5 in Figure 6.1. These junction

configurations are defined for the particular case of the technology used in the validation and implementation of this concept. The same approach can be extended to different CMOS/BiCMOS technologies, once the characteristics of the doping and isolating regions are identified.

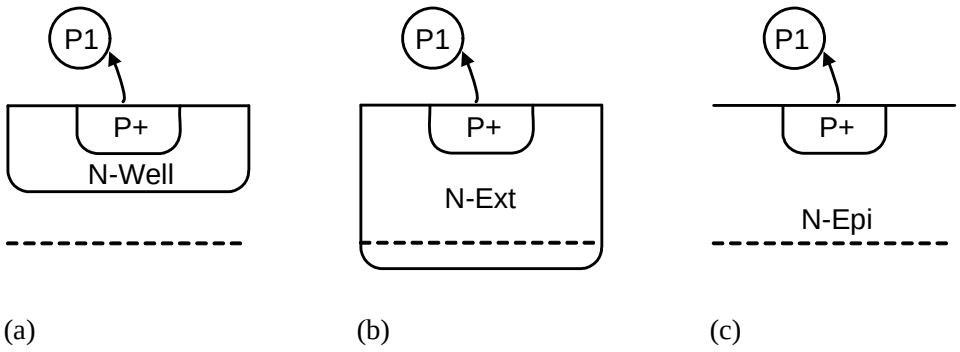


Figure 6.2. Extended schematics of different junction configurations for adjustment of the reverse breakdown voltage.

The forward blocking junctions shown in Figure 6.3 (a) through (l) can comprise a sub-region at a junction between adjacent regions. According to Figure 6.3, the sub-region can be a doped region to either conductivity type (n- or p- type), or an isolation area, such as a LOCOS (local oxidation of silicon), STI (shallow trench isolation), blocking silicide resistor layer, or other isolation areas. On the other hand, the adjacent regions can comprise 1) a portion of a tub layer in which the junction is formed, 2) an extension region (Ext) formed in the tub layer, and/or 3) a well region (Well) formed in the tub layer. At this point, the TCAD methodology presented in chapter 5 allows for a fast simulation and close prediction of the blocking junction voltage that can be used for implementing custom devices such as the one depicted in Figure 6.1.

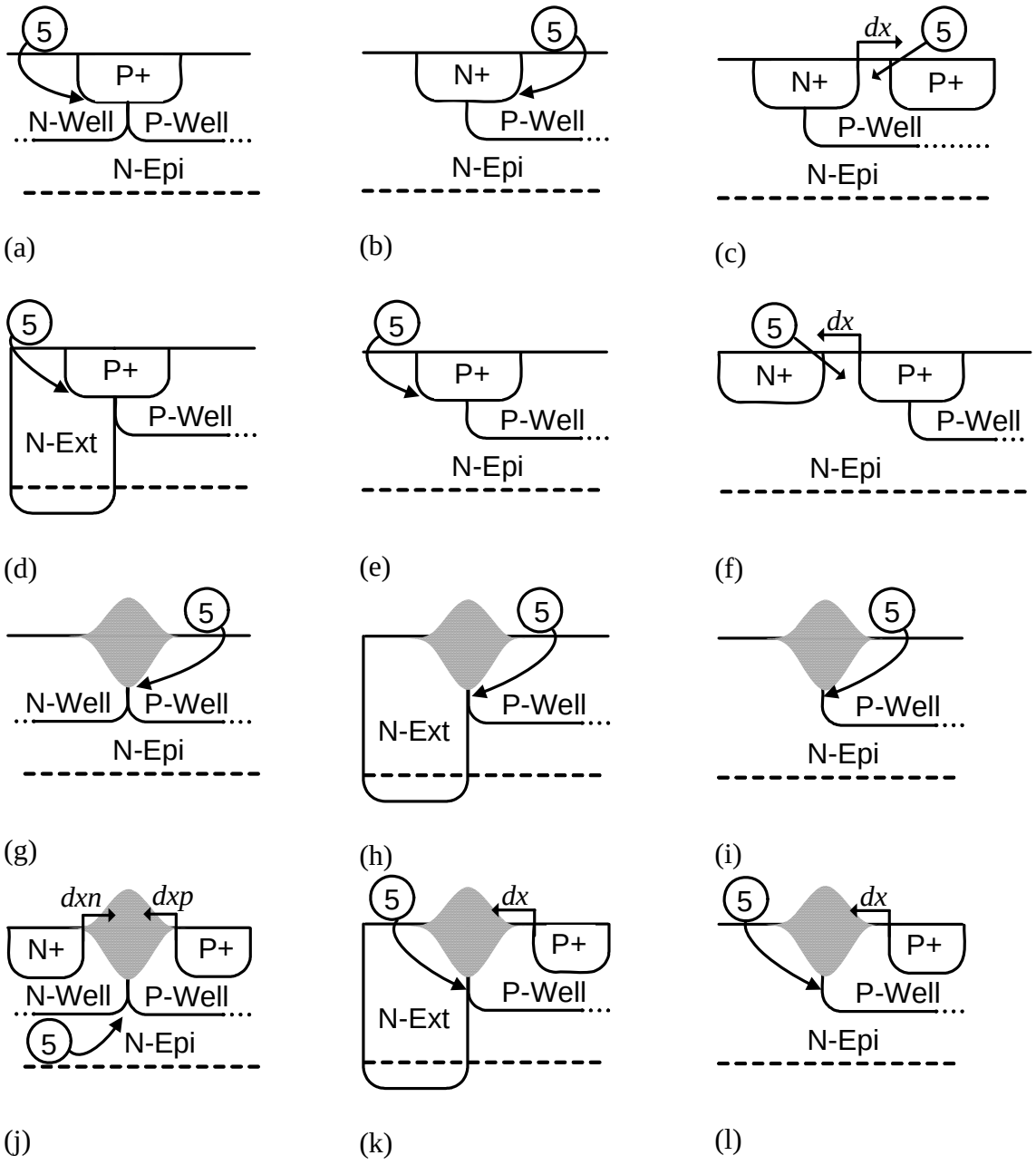


Figure 6.3. Schematics of 12 junction configurations for adjusting the forward trigger voltage V_T.

6.1.2. Doping Profiles and Definition of Conducting Characteristics

Figure 6.4 shows average V_T obtained from devices having selected junction configurations listed in Figure 6.3 for label 5. Note the capability of customizing the blocking voltage for the typical doping density levels listed in Figure 6.4. Furthermore, following the discussion in chapter 5, adjustment of the distance between highly doped regions close to the blocking junction (i.e., distances: *dx*, *dxn*, and *dxp*, for configurations in Figure 6.3 -(c), - (f), - (j), - (k), and - (l)) modifies the device behavior. For instance, V_T is changed from 6.5 V to 12.3 V when configuration in Figure 6.3(c) is used and *dx* is increased from 0.2 μm to 0.7 μm. Similar experiments to those presented in chapter 5 using the 2D device simulations provide the following quantitative insights. For *dx*= 0.2 μm, the peak electric field and Selverherr's impact generation rate in the blocking junction are 7×10^5 V/cm and 1×10^{28} $s^{-1} \cdot cm^{-3}$, respectively. For *dx* = 0.7 μm, the peak electric field and impact generation rate reduce to 6.5×10^5 V/cm and 2.5×10^{27} $s^{-1} \cdot cm^{-3}$, respectively, and hence the larger trigger voltage. In addition to the blocking junction selection, by using the concept previously discussed in chapter 3, the lateral dimensions of the device can be adjusted to further optimize the I-V characteristics during the on-state.

A detailed graphical reference of the ion-implantation doping profiles combinations considered in the TCAD simulation is presented in reference [83]. The graphical illustration of different doping profiles combinations allows for evaluation of the design flexibility in the base-line of the specific CMOS/BiCMOS process. Figure 6.5 to Figure 6.9 show normalized versions of the doping profiles considered in this study. For better illustration, the doping profiles normalization is set such that the magnitude of highest doping level is 10^{10} cm^{-3}/ cm^{-3}.

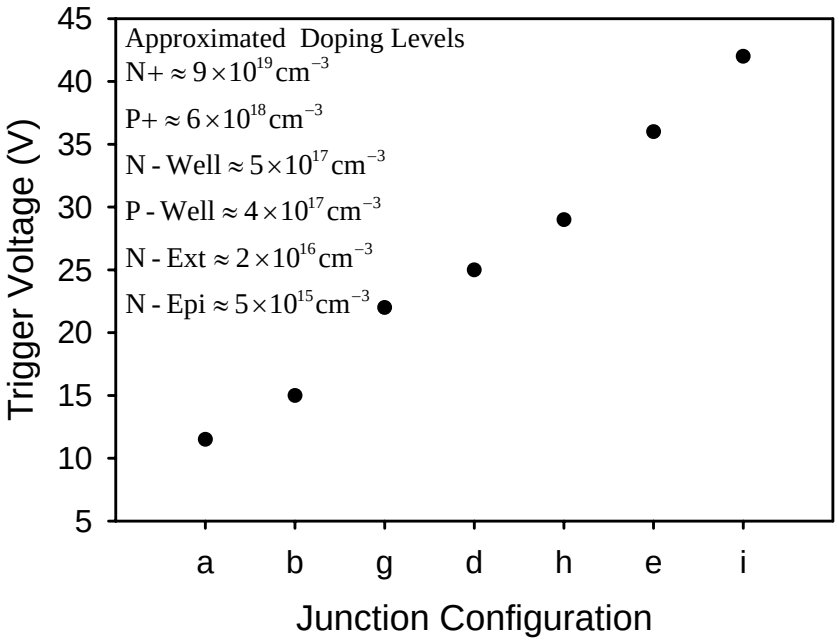


Figure 6.4. Trigger voltage level for some of the junction configurations listed in Figure 6.3.

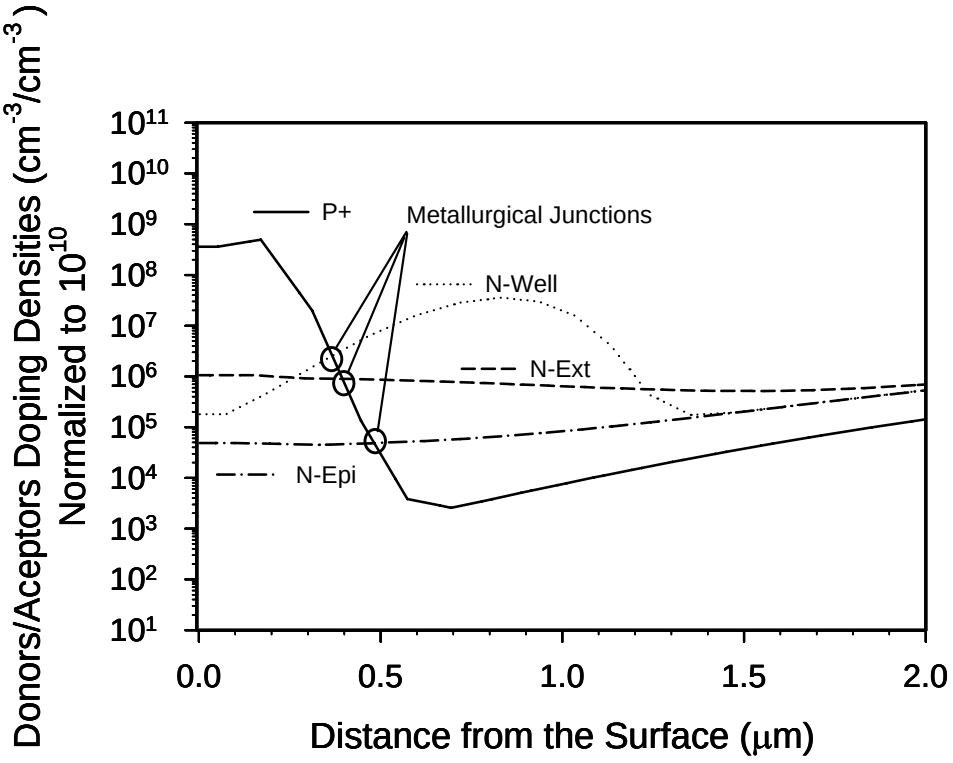


Figure 6.5. Comparison of normalized P+/N-Well, P+/N-Ext, and P+/N-Epi doping profiles indicating the corresponding metallurgical junctions form for each of these doping combinations. Normalization versus peak of maximum doping level obtained at 10^{10} cm^{-3}/cm^{-3}.

Figure 6.5 shows the normalized doping profiles for the P+, and it is depicted in the same plot with the corresponding doping profiles for the N-Epi, N-Ext, and N-Well regions. The different shapes at the metallurgical junctions give rise to changes in the breakdown- or associated trigger- voltages. Figure 6.6 shows the opposite case where the normalized N+ doping profile is combined with the p-type lightly doped regions. In this condition, associate trigger voltages are different to the one that can be obtained with the configurations in Figure 6.5.

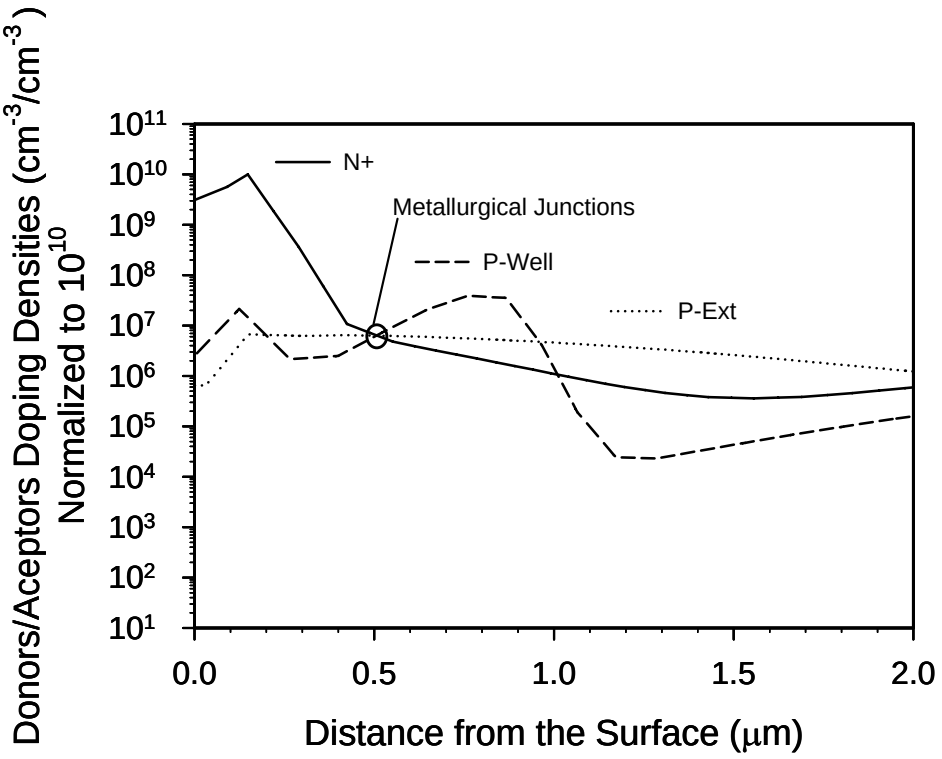


Figure 6.6. Comparison of normalized N+/P-Well and N+/P-Ext doping profiles indicating the corresponding metallurgical junctions. Normalization versus peak of maximum doping level obtained at 10^{10} cm^{-3}/cm^{-3}.

Figure 6.7 and Figure 6.8 compare the P-Well and P-Ext, respectively, with the corresponding lightly doped n-type regions. In this specific case, these configurations can allow for the design of the higher trigger voltages. Note that for the particular example presented in Figure 6.8, the associated junctions are obtained far away from the surface. For this reason, the

P-Ext is not considered in the definition of the blocking junction configurations. Figure 6.9 shows the case where the distance between two highly doped regions of opposite type (P+ and N+) are separated by a predetermined distance *dx*, corresponding to a lightly doped region (N-Well). When the distance *dx* is reduced, the breakdown voltage can be modulated to lower levels than the N-Well to the P+ breakdown. This latest design strategy is followed in Figure 6.3 - (c), - (f), - (j), - (k), and - (l).

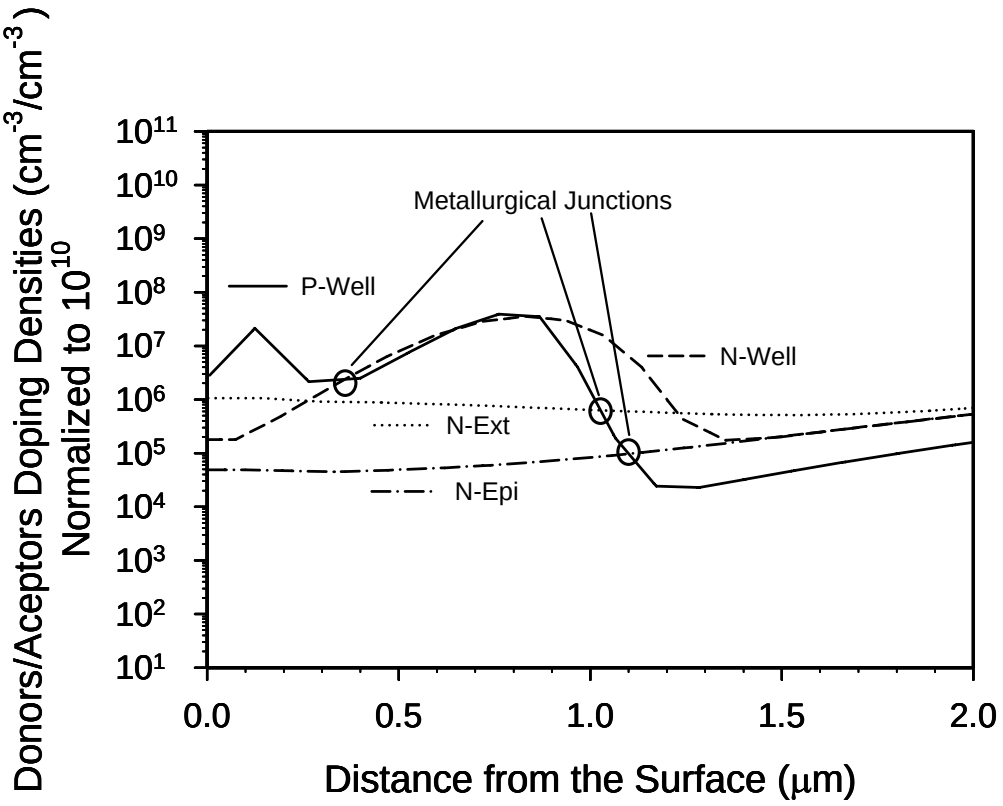


Figure 6.7. Comparison of normalized P-Well/N-Well, P-Well/N-Ext and P-Well/N-Epi doping profiles indicating the corresponding metallurgical junctions. Normalization versus peak of maximum doping level obtained at 10^{10} cm^{-3}/cm^{-3}.

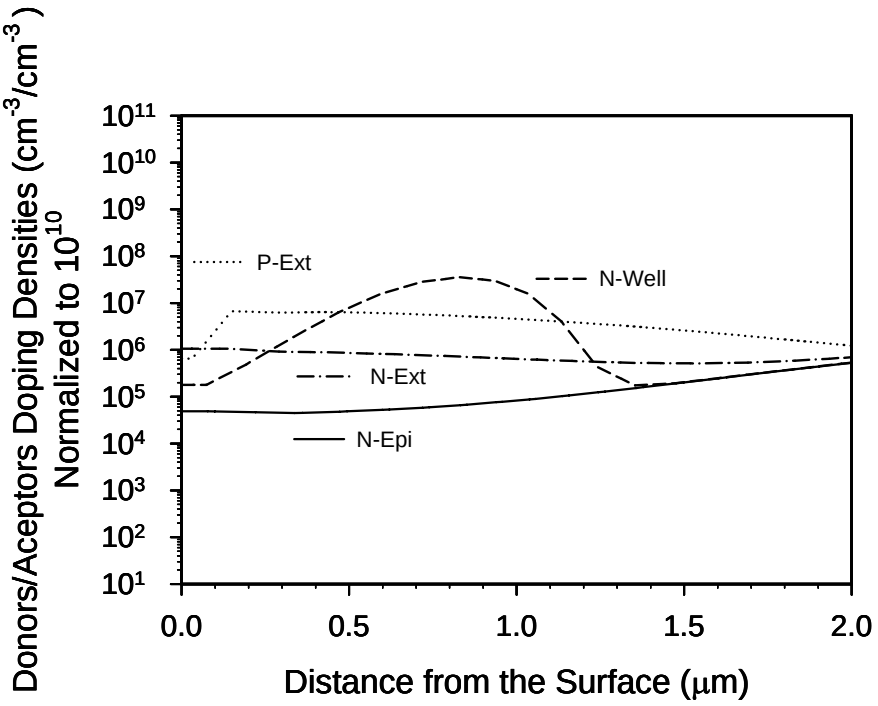


Figure 6.8. Comparison of normalized P-Ext with the normalized N-Well, N-Ext and N-Epi. Normalization versus peak of maximum doping level obtained at 10^{10} cm^{-3}/cm^{-3}.

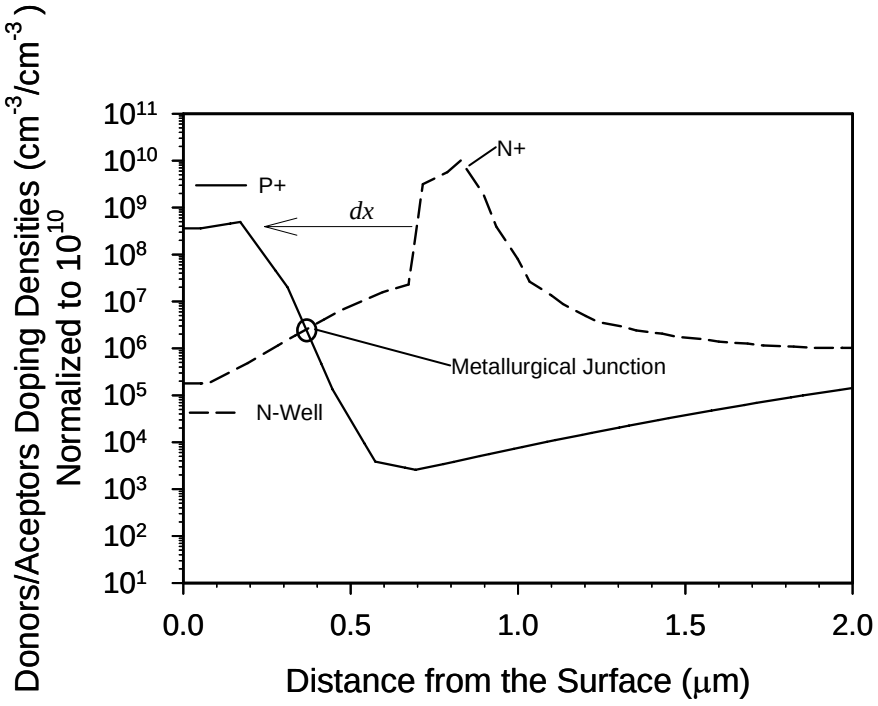


Figure 6.9. Normalized P+/N-Well/N+ example doping profile array used to control the breakdown voltage and associated trigger voltage obtained with the P+/N-Well blocking junction.

6.2. Obtaining Custom S-Type Conducting Characteristics

6.2.1. Fabricated Single Section Devices

Several versions of single sections devices have been simulated and fabricated [83], [86]. These structures follow in general the TCAD-assisted design approach introduced in chapter 5 and discussed in section 6.1. Three S-type I-V characteristics measured using the TLP technique are discussed and compared next. Figure 6.10 shows the Transmission Line Pulsed (TLP) I-V characteristics of different examples of single-section devices (SD-1, SD-2, and SD-3) fabricated in a sub-micron, silicided, triple-well CMOS technology and using the junction combinations summarized in Table 6.1. The inset in Figure 6.10 depicts the I-V characteristics in the low current region.

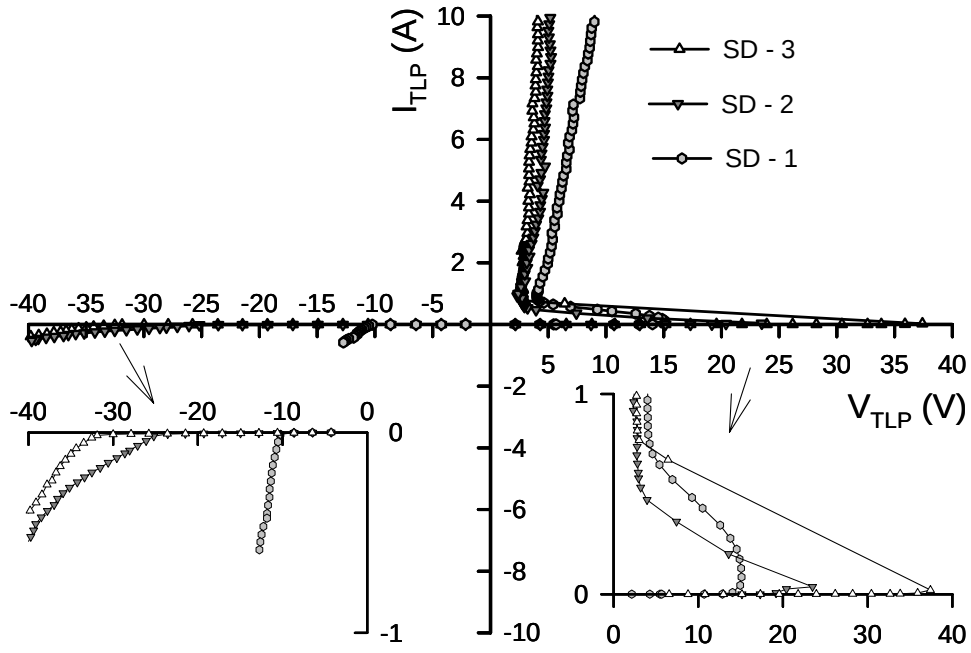


Figure 6.10. Comparison of forward and reverse conducting characteristics for single-section devices, using different combinations of the junction configurations shown in Figure 6.2 and Figure 6.3.

Table 6.1. Junction configurations embedded in devices having the I-V characteristics depicted in Figure 6.10.

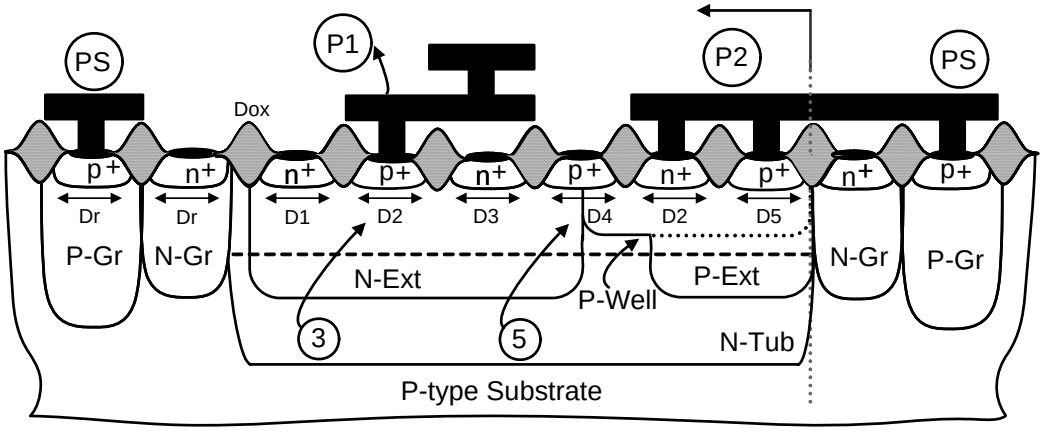
ESD Protection Element	Blocking Junction Configurations	
	Label 3 (RBJ)	Label 5 (FBJ)
SD-1	Figure 6.2(a)	Figure 6.3(b)
SD-2	Figure 6.2(b)	Figure 6.3(d)
SD-3	Figure 6.2(c)	Figure 6.3(e)

Testing on wafer using an industry standard TLP instrument are shown herein. As can be seen in Figure 6.10, three different V_R, V_T, and conduction current capabilities are obtained. The different junction configurations mainly defined the conducting conditions, and in general can be customized to the specific ESD requirements. For illustration, Figure 6.11 shows the cross-sectional view of the stand-alone device SD-2 and corresponding layout dimensions (similar regions can be identified as well, at the right section of the structure in Figure 6.1). More detailed information about the dimensions used in an extended list of devices developed in this study is provided in references [83], [86].

6.2.2. Fabricated Dual-Polarity Devices

In order to realize dual-polarity ESD conductions (triggering and snapback for both the positive and negative ESD), the approach previously discussed in chapter 5 and Figure 6.1 is followed. The key junctions in the right section corresponding to those in the left section are labeled with numbers 4 and 6. Integrating the right and left sections, one for the positive and the other for the negative ESD, will therefore generate different combinations of the four junctions

in the two-section device and therefore alternative I-V characteristics with customized snapback behaviors.



Device	Dimensions (μm)						
	Dr	D1	D2	D3	D4	D5	Dox
SD-2	1.6	1.6	1.6	1.0	3.2	1.6	1.0

Figure 6.11. Cross-sectional view of sub-section structure corresponding to the SD-2 I-V characteristics in Figure 6.10 and approximated layout dimensions.

Figure 6.12 shows the measured TLP results of three different two-section devices (BD-S1, BD-S2, and BD-AS1) fabricated using the same technology and having the junction combinations listed in Table 6.2. The inset in Figure 6.12 depicts the I-V characteristics in the low current region. Both BD-S1 and BD-S2 exhibit symmetrical I-V characteristics (i.e., identical trigger and holding voltages for positive and negative ESD), whereas BD-AS1 yields asymmetrical characteristics. In addition, the three devices exhibit different trigger, holding, and on-state current characteristics. This clearly demonstrates that the originality of this work, in addition to the adjustable triggering voltage, lies on the capability of generating fully customizable bi-directional, symmetrical and asymmetrical S-type I-V characteristics for very

robust ESD solutions. It should be pointed out that the relatively high trigger current (or late snapback) for the reverse ESD of the device BD-AS1 results from the interaction between the highly asymmetrical left and right sections. Such an interaction gives rise to not only asymmetrical trigger voltages (-10.5 V vs. 15 V), but also to asymmetrical snapback behavior (early snapback vs. late snapback).

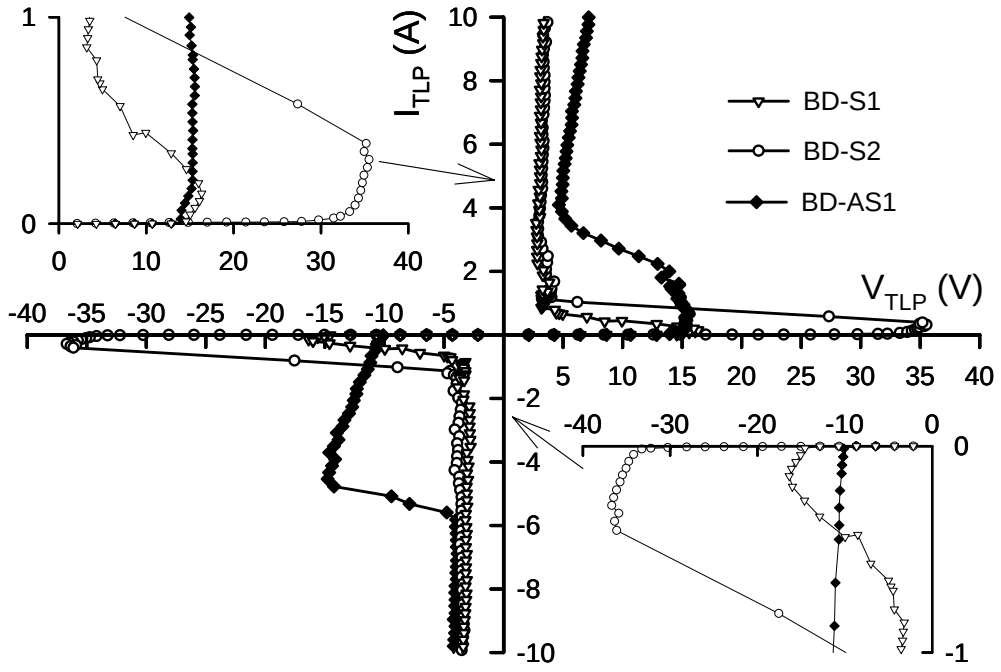


Figure 6.12 Comparison of forward- and reverse- conducting characteristics for dual-polarity devices using different combinations of the junction configurations in Figure 6.2 and Figure 6.3.

The three dual-polarity devices were also tested using device level HBM, and MM, and system level IEC 1000-4-2 ESD standards. With an area as small as 120 μm x 200 μm, several implemented dual-polarity devices passed the ESD stresses of 15 kV HBM, 2 kV MM, and 16.5 kV as defined by the IEC standard. Table 6.3 summarizes the measured ESD DC characteristics of these devices at room temperature. The very low leakage current minimizes the

ESD protection parasitic effect. Applications of the proposed ESD device include the protection of advanced communication interface systems with a power supply of 3 V or 5 V and different I/O operating voltages, e.g., (-10, to 10 V), (-8, to 12 V), and (-25 and 25 V).

Table 6.2. Junction configurations incorporated in devices having the I-V characteristics depicted in Figure 6.12.

ESD Protection Element	Left Section		Right Section	
	Label 3 (RBJ)	Label 5 (FBJ)	Label 4 (RBJ)	Label 6 (FBJ)
BD-S1	Figure 6.2(c)	Figure 6.3(b)	Figure 6.2(c)	Figure 6.3(b)
BD-S2	Figure 6.2(c)	Figure 6.3(e)	Figure 6.2(c)	Figure 6.3(e)
BD-AS1	Figure 6.2(c)	Figure 6.3(b)	Figure 6.2(a)	Figure 6.3(a)

Table 6.3. Summary of DC characteristics obtained for dual-polarity ESD devices

ESD Protection Element	Positive Trigger Voltage	Negative Trigger Voltage	Leakage at DC Operating Voltage (nA)
BD-S1	14 V	- 14 V	0.7 @ $\pm$ 12 V
BD-S2	35 V	- 35 V	3.5 @ $\pm$ 15 V
BD-AS1	15 V	- 10V	< 2 @ (-7 V to12 V)

At a temperature of 140 °C, consistent with explanations in chapter 3, it was verified experimentally that V_T in this case decreases slightly, leakage current increases, and the holding current decreases. Thus, for microchips operating at elevated temperatures, the ESD design needs to be reassessed to make sure that the changes in the leakage, triggering, and holding behavior are within an acceptable range.

6.3. On-Chip ESD Protection Performance

Chapter 2 illustrated the general flow for the different stages of the on-chip ESD design. In chapters 3 and 4 the design flows have been applied for the complete design development for applications operated at relatively low voltage, and within a voltage range according with the technology native voltage. In the next sections, results of two examples that followed the TCAD-measurements ESD design flow, are discussed for applications required to operate at I/O voltage levels considerably higher than the predefined for the CMOS devices in the specific technology.

6.3.1. Case Study 1: ESD Protection for Mixed-Signal Interface Application Operating at High I/O Asymmetric Voltage

In the first sections of this chapter, dual-polarity designs and the general approach to adapt the conducting characteristics to the given requirements have been discussed. To illustrate these guidelines, a specific example where a predetermined design window is defined will be presented, and the different design considerations will be illustrated.

Figure 6.13 shows a predetermined asymmetrical ESD design window. For the conducting characteristics below V_{SS} (negative ESD), the ESD protection structure is required to trigger at a $V(-)_{max}$ voltage range between -10 V and -13 V, while the snapback is allowed below the V_{O1-} operating voltage (-8 V), as long as the I_{hr} holding current is higher than about 100 μA (I/O pad driving current). For the conducting characteristics above V_{DD} (positive ESD), the ESD protection structure should trigger at a $V(+)_{max}$ voltage range between 13 V and 16 V. Likewise, the snapback is allowed below the V_{O2+} operating voltage (12 V), as long as the holding current is higher than the I/O pad driving current defined by the circuit designer. Additionally to the previous requirements, the device must sustain an I/O dual-polarity level of stress of ± 15 kV, as

defined by the system-level IEC 1000-4-2 standard, while clamping the maximum voltage level within the range previously defined in the design window.

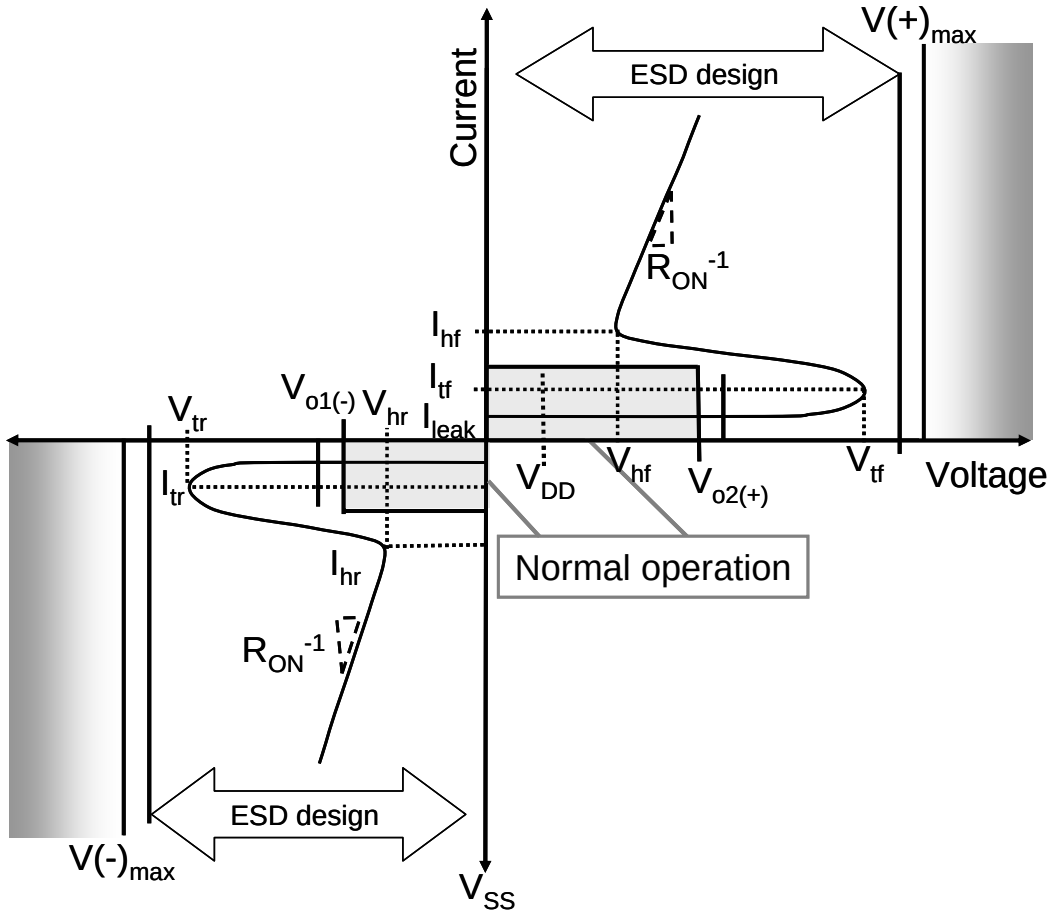


Figure 6.13. Asymmetrical ESD protection design window.

Following the previously discussed design flow in chapters 2 and 5, the first step is the simulation and identification of the forward and reverse junction combination, which allows for the design of the asymmetric dual-polarity trigger voltage. From TCAD simulations and previous characterization, the selected blocking junction configurations are summarized in Table 6.4. By incorporating these blocking junctions in the dual-polarity device, the reverse blocking junctions configurations give a reverse blocking voltage of over 30 V, while the forward blocking

junctions give conducting voltages of about 11.5 V and 15 V, which can be used for the design of the trigger voltages for the negative- and positive- conduction, respectively.

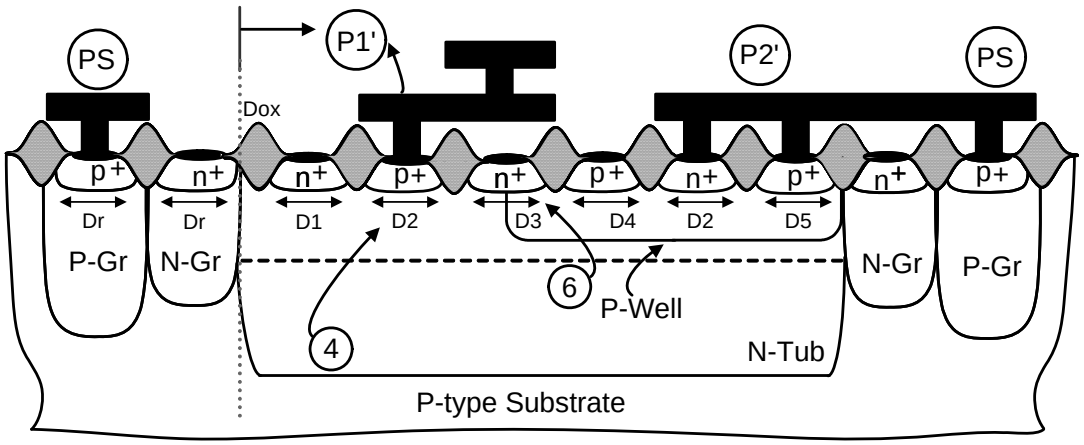
Table 6.4. Blocking junction selection for conduction within the design window defined in Figure 6.13.

ESD Protection Element	Left Section		Right Section	
	Label 3 (RBJ)	Label 5 (FBJ)	Label 4 (RBJ)	Label 6 (FBJ)
BD-AS2	Figure 6.2(c)	Figure 6.3(a)	Figure 6.2(c)	Figure 6.3(b)

Figure 6.14 and Figure 6.15 show the cross-sectional views of the single section devices that include the blocking junctions in Table 6.4. In order to provide the required high level of ESD protection, experimental verification was conducted to estimate an optimum device width and the level of stress that can be sustained using one finger. Results of this experiment showed that up to about 200 μm width, the level of ESD stress sustainable by the device increased well with width. Wider devices can suffer filamentation problems and are more difficult to integrate. For 200 μm width, one finger sustains slightly more than 10 A (maximum limit measured with the available TLP instrument). From this result, it was considered that properly designed five-finger devices can sustain over 50 A (corresponding to the stress voltage of 15 kV divided by the predetermined resistance of 300 Ω defined in the ESD standard), while still clamp the maximum voltage within the ESD design window. This assumption was successfully verified.

Consistent with the simulation predictions as in chapter 5, the TLP characteristics measured from the single section devices are shown in Figure 6.16 and Figure 6.17. These characteristics provide on their own the ESD protection requirements for the positive (Figure 6.16) and negative

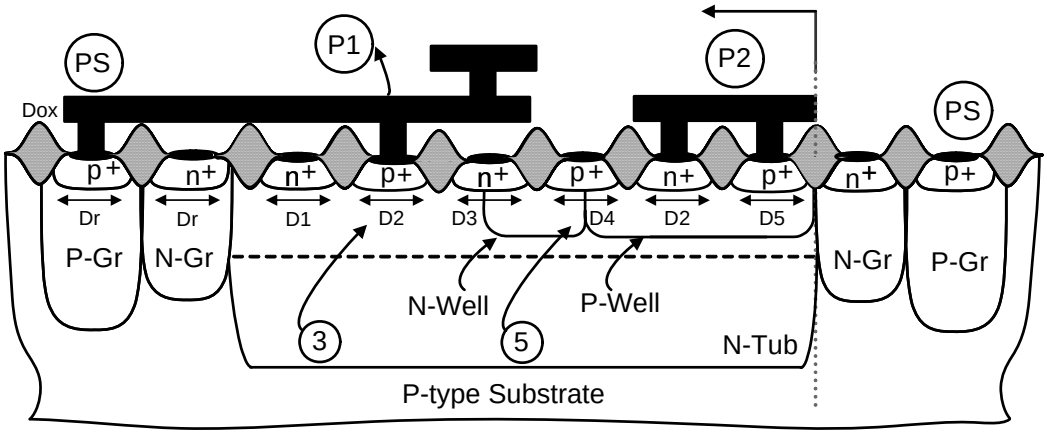
(Figure 6.17) ESD stress. The next step consists in the integration of these structures in a more complex dual-polarity ESD protection while taking the minimum silicon area.



Device	Dimensions (μm)						
	Dr	D1	D2	D3	D4	D5	Dox
SD-2	1.6	1.6	1.6	3.2	1.6	1.6	1.0

Figure 6.14. Single section device for implementing the positive-side of the ESD design window.

Figure 6.18 shows the cross-sectional view of a dual-polarity device, which includes the four previously identified blocking junctions (Table 6.4), which have been incorporated in the two single section devices shown in Figure 6.14 and Figure 6.15. Figure 6.19 shows the resulting dual-polarity I-V characteristics. This device meets the ESD requirements, and it is operating in the design window previously described. Furthermore, it has been integrated and verified in commercial products developed in submicron technologies [45], in which previously existing ESD solutions did not provide the robustness required to pass the system-level test program.



Device	Dimensions (μm)						
	Dr	D1	D2	D3	D4	D5	Dox
SD-2	1.6	1.6	1.6	3.2	3.2	1.6	1.0

Figure 6.15. Single section device for implementing the negative-side of the ESD design window.

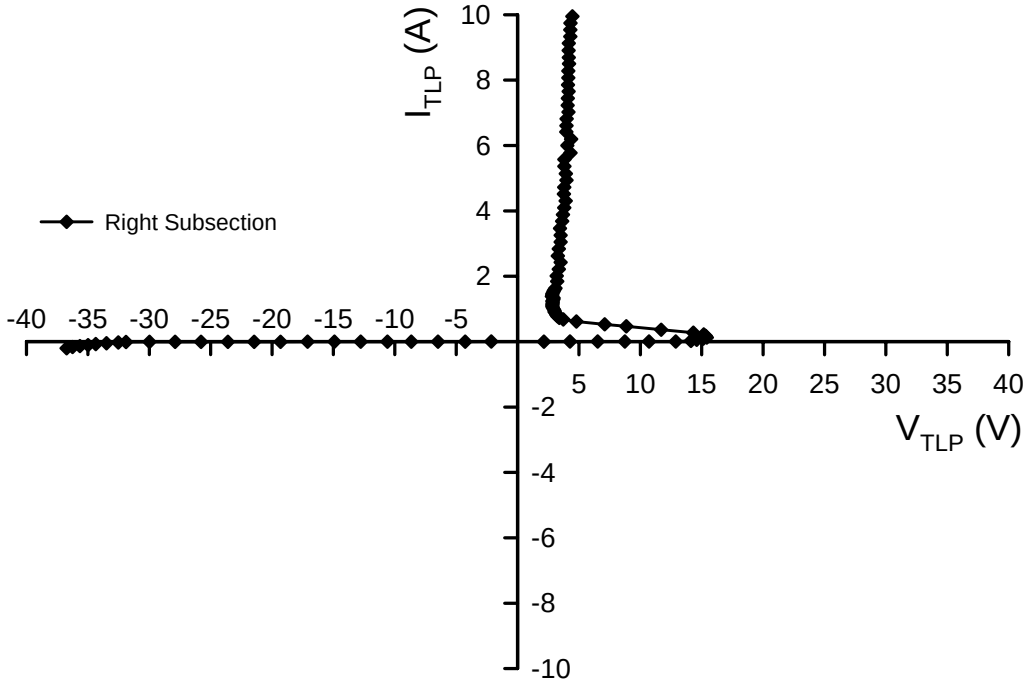


Figure 6.16. TLP I-V characteristics for positive ESD protection design.

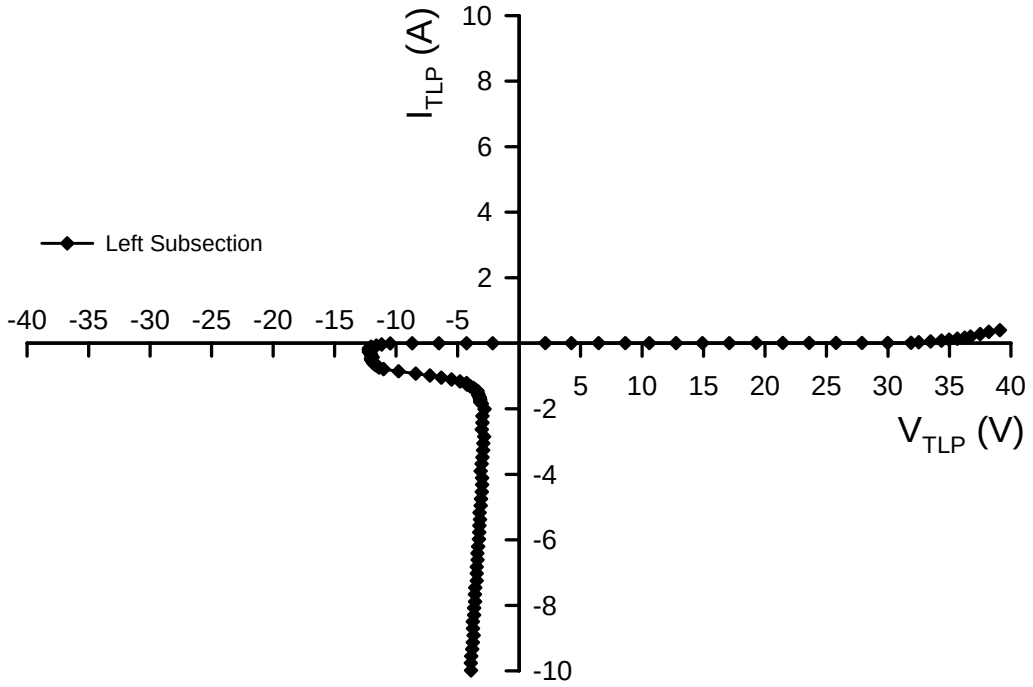


Figure 6.17. TLP I-V characteristics for negative ESD protection design.

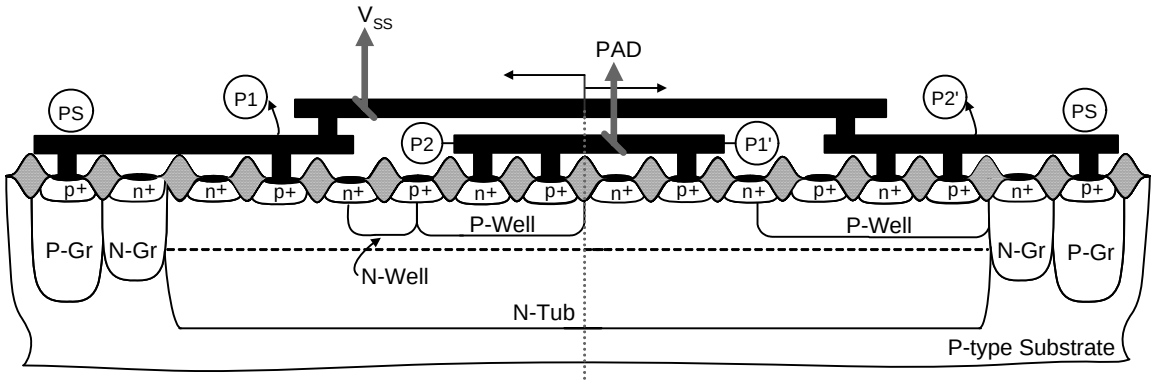


Figure 6.18. Cross-sectional view of dual-polarity device for the asymmetrical ESD design predetermined by the ESD design window in Figure 6.13.

6.3.2. Case Study 2: ESD Protection for Mixed-Signal Interface Application Operated at High I/O Symmetric Voltage

Following a similar approach to the previously described for the case of asymmetrical ESD design, symmetrical ESD designs can be implemented within a wide range of operating voltages covered in Figure 6.4. Combinations of any of those trigger voltages is allowed, given that the appropriate forward- and reverse blocking junctions are selected.

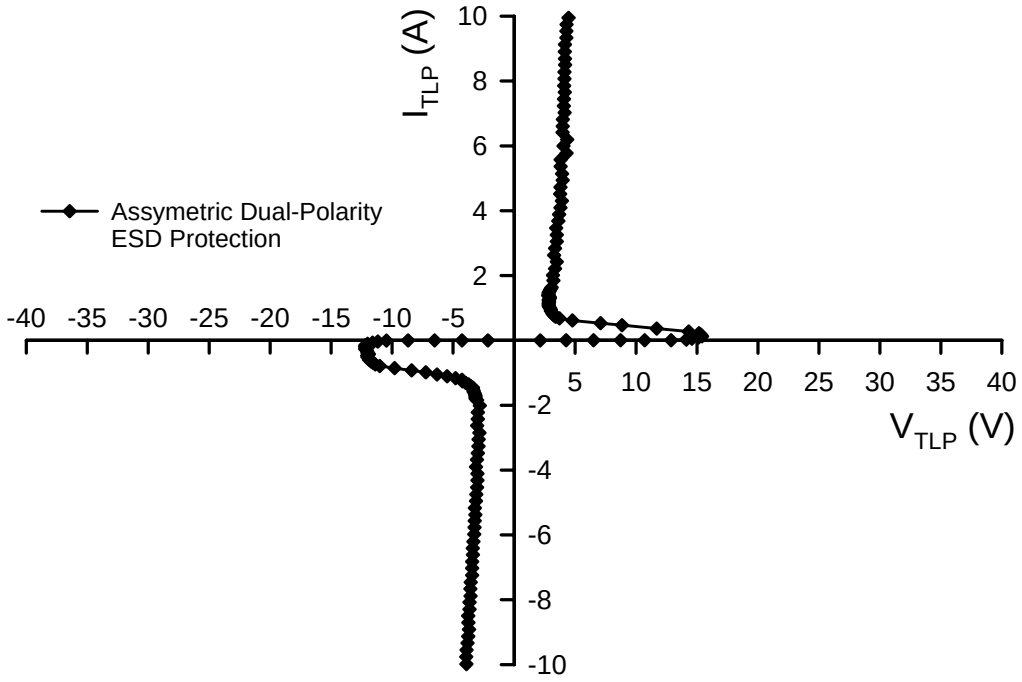


Figure 6.19. Asymmetrical dual-polarity I-V characteristics for the device in Figure 6.18.

Figure 6.20 shows a predetermined symmetrical ESD design window. In this case the conducting characteristics below V_{SS} (negative ESD) and above V_{DD} (positive ESD), can be even higher than in the previous example, e.g., over ± 25 V [93], and even more difficult to visualize without a systematic design approach. Assuming that the ESD protection structure is required to trigger at a voltage range between ± 15 to ± 18 V, the snapback is allowed below the operating voltage (± 12 V), while the holding current is higher than 100 μm (I/O pad driving current).

Similar to the design in section 6.3.1, the device must sustain an I/O dual-polarity level of stress of ± 15 kV, as defined by the system-level IEC 1000-4-2 standard, while clamping the maximum voltage level within the design window range.

Following the design guidelines, the first step is the simulation and identification of the forward- and reverse- junction combinations that allow for the design of the dual-polarity symmetric trigger voltage. In this case, only one forward and one reverse junction configuration need to be identified, since the same pair of junctions is used for each sub-section of the dual-polarity device. The selected reverse and forward blocking junctions are shown in Figure 6.2(c) and Figure 6.3(b), where the predicted blocking voltages are about 33 V and 15 V, respectively.

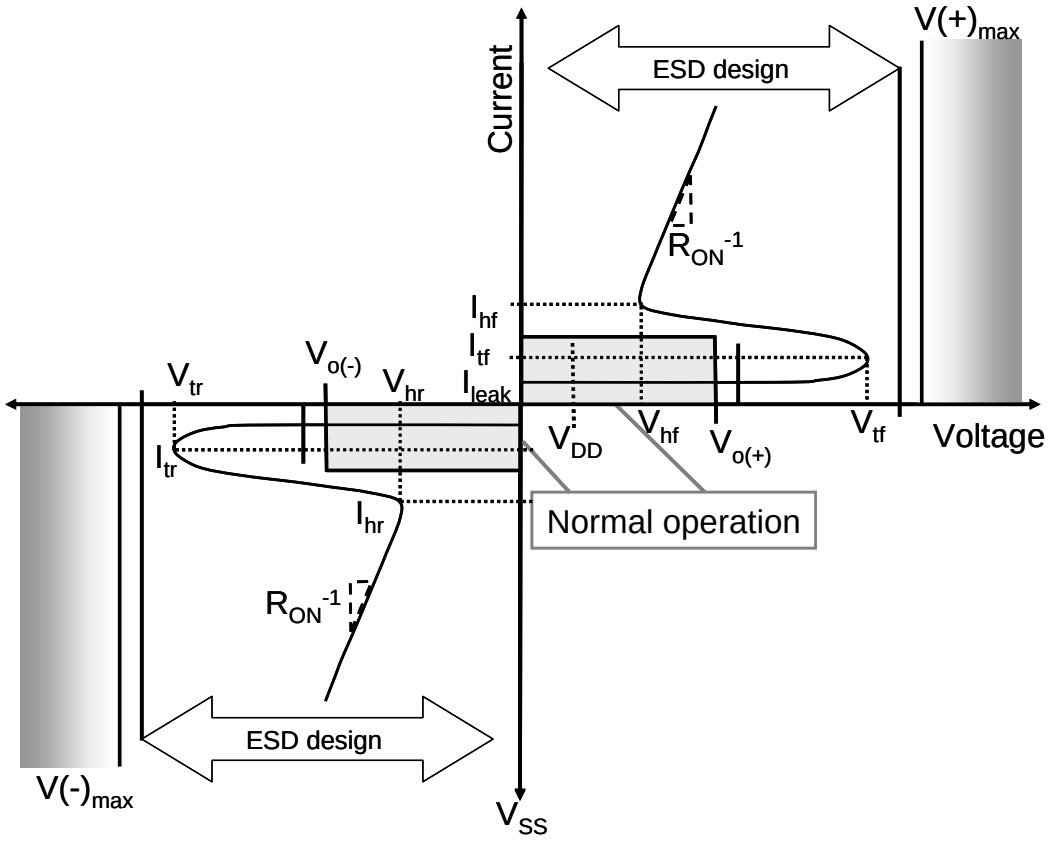


Figure 6.20. Symmetrical ESD design window.

Figure 6.14 previously shown includes the selected forward and reverse blocking junction configurations. By using the same criteria previously discussed for the multifinger device in section 6.3.1, and the TLP characteristics shown in Figure 6.16, both sections of the symmetric dual-polarity ESD protection can be implemented.

Figure 6.21 shows the cross-sectional view of the dual-polarity device, including the single section devices shown in Figure 6.14. Figure 6.22 depicts the resulting dual-polarity I-V characteristics. This device is operating in the established design window and sustains the required ESD level. At this point of the design, it is also important to mention that an additional and useful verification accomplished in the protection devices includes the evaluation of the OBIC via EMMI. For this evaluation setup, a pulse of voltage was applied in the ESD protection structure, while the conduction in the multifinger structure was verified initially on the stand-alone device (Figure 6.23), and subcequently in the actual protected circuit (Figure 6.24).

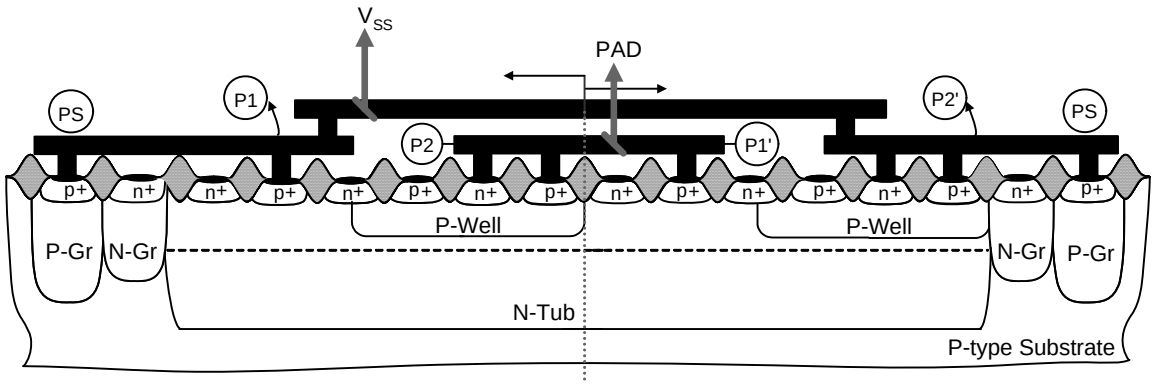


Figure 6.21. Cross-sectional view of symmetric ESD protection device incorporating the device in Figure 6.14.

Figure 6.23 (a) and (b) show the emission microscopy (EMMI) images of the optical beam induced current (OBIC), for the five-finger dual-polarity device. In the corresponding areas where the blue color is detected (conduction-induced light), uniform emission is verified for the

corresponding 5 fingers conducting for each stress polarity. Figure 6.23(a) shows the emission for the positive ESD conduction (pad to V_{SS}), while Figure 6.23(b) shows the emission for the negative ESD conduction (V_{SS} to pad). The uniform emission pattern along the ESD devices' fingers was verified for the implementation of different structures assessed in this study, and indicates that the layout of the ESD structure allows for a predictable scaling of the ESD protection level.

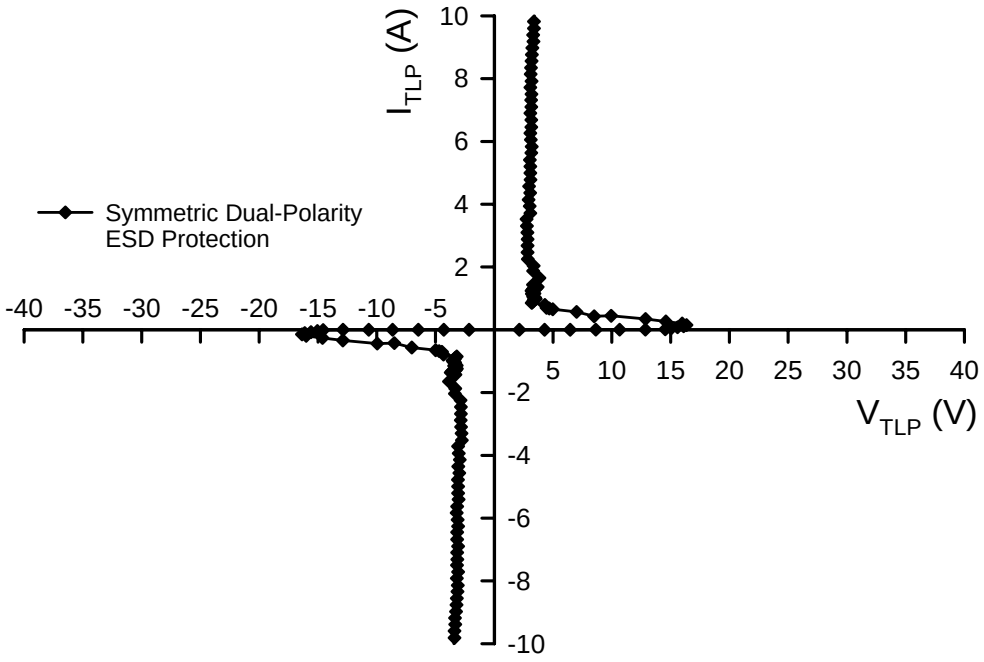
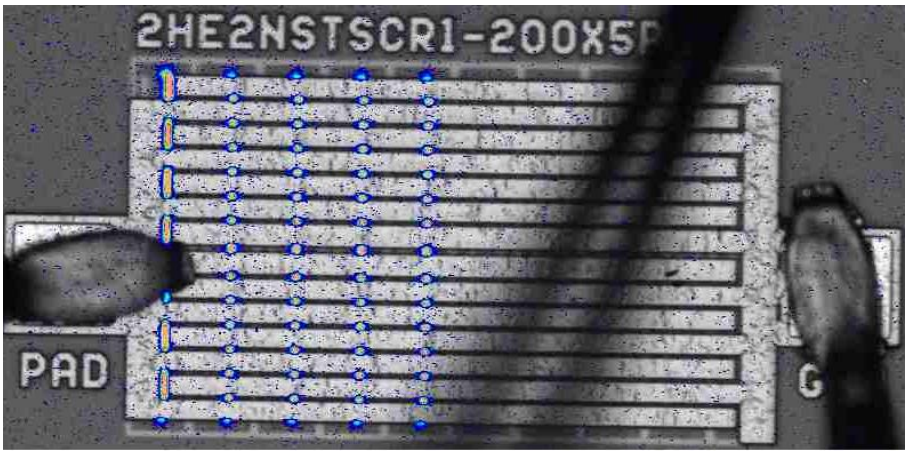


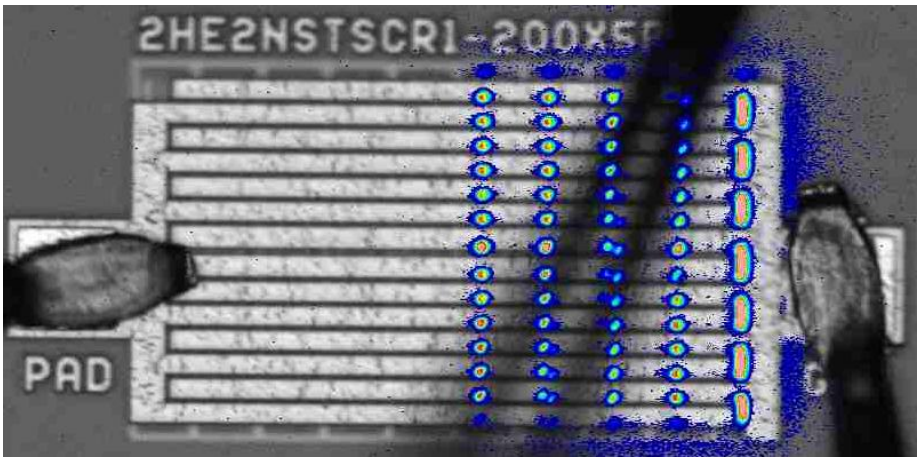
Figure 6.22. Measured dual-polarity symmetric TLP I-V characteristics for structure in Figure 6.21.

The device in Figure 6.23 occupies an area of 200 x 226 μm^2, and successfully sustains over 15 kV system-level ESD stress as described by the IEC-1000-4-2 standard. Once the protection devices are integrated in the circuit, the next verification step also involves detection of the OBIC via EMMI analysis on the circuit. The result depicted in Figure 6.24 corresponds to the EMMI captured while a negative voltage pulse was applied in one of the high ESD I/O pads. Note that for the specific stress applied in the circuit, only the five fingers of the protection

structure are emitting light (conducting), which guarantees the integrity of the protected circuit during the applied stress. This design methodology has been extended to a wide range of mixed-signal circuit applications, and demonstrated at solving complex ESD problems in a unique and effective way. Results of experiments for many other different operating voltages have been successfully verified and are expected to open doors for new future findings. Extended group of results and cross-sectional views of device characterized in this study [93] can be found in references [83] and [86].



(a)



(b)

Figure 6.23. Emission Microscopy (EMMI) images of the optical beam induced current (OBIC), having a) pad to V_{SS}- and b) V_{SS} to pad- conducting current.

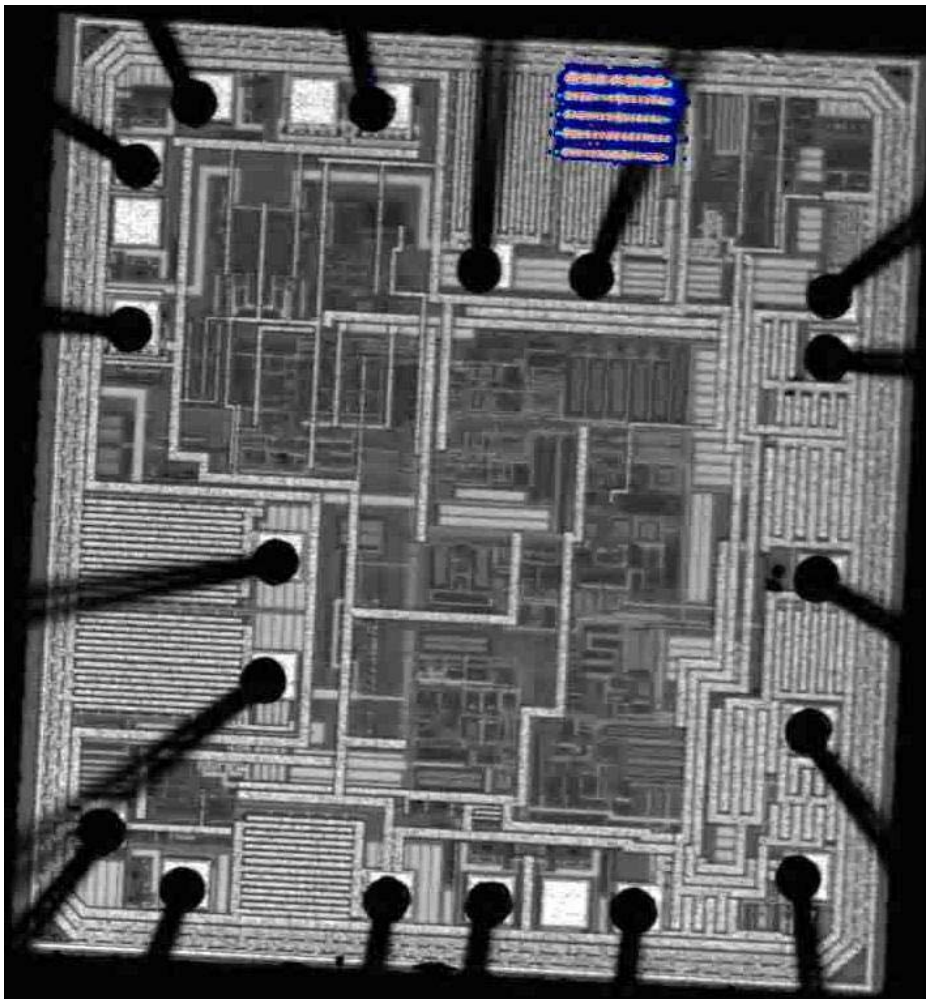


Figure 6.24. Emission microscopy image of the optical beam induced current when a negative voltage pulse is applied in the high ESD I/O. The five fingers of the protection device are the only regions in the chip showing conduction during stress.

6.4. Chapter Remarks

Novel design methodologies using TCAD simulations and reduced measurements for the design of fully customizable single- and dual-polarity S-type I-V characteristics have been demonstrated. Different compact and tailored devices have been developed for robust ESD protection applications. The devices allow for flexible design of symmetrical and asymmetrical S-type I-V characteristics and thus provide versatile solutions to meet demanding ESD protection requirements in advanced CMOS/BiCMOS mixed-signal technologies. ESD performance has

been demonstrated in stand-alone devices, as well as in commercial applications that incorporate different device structures developed in this study using the discussed design approach. The ESD devices and ESD-protected circuit applications have been characterized using TLP measurements, the HBM, MM, and IEC 1000-4-2 ESD standards, and the emission microscopy (EMMI) images of the optical beam induced current (OBIC).

CHAPTER 7
CONCLUSIONS

7.1. Dissertation Summary

As technology evolves, ESD protection techniques and circuit integration design methodologies should also be improved. The trial-and-error approach for the ESD protection design is not longer an effective strategy to generate technology- and application- adapted ESD protection solutions within short time cycles.

Development of new embedded-MOSFET PN-PN, P_1N_1-P_2N_2 and P_1N_1-P_2N_2 //N_1P_3-N_3P_1 structures for implementing custom ESD protection has been demonstrated using existing CMOS/BiCMOS technologies. The assessment of the different device structures was accomplished following a systematic design methodology, which incorporates electro-thermal TCAD simulations, reduced experiments in the design flow, and novel layout strategies for device evaluation and integration on-chip.

ESD protection design for applications operating at relatively low voltage has been demonstrated by introducing the HH-LVTSCR (high-holding-low-voltage-trigger-silicon-controlled-rectifier). In this device, effective ESD protection response is reached by designing relatively low trigger voltage without using external triggering components, while latchup problems are eliminated by providing a high holding voltage during the on-state operation. The high holding voltage is tailored by effective control of the carrier injection efficiency during the regenerative feedback of the protection device. This characteristic of the HH-LVTSCR devices makes them suitable for implementing robust input/output and supply clamp protections in commercial mixed-signal ICs. Even though these families of devices have been incorporated

without external triggering components, they do provide this flexibility and applications required to trigger at an even lower voltage can include detection circuits for gate-induced triggering.

Application of the HH-LVTSCR concept was successfully extended to different CMOS technologies being used for characterization and development of reliable multi-technology embedded sensor SoC applications. In this design, custom ESD protection devices were designed for the first time in the technologies studied, and a complete process of characterization, classification, integration, and ESD testing verification was presented. The developed ESD solution was also demonstrated to be smaller than the existing ESD designs.

Additional complications in the ESD design are encountered when circuit applications are required to interface with external components operating at a voltage considerably above/below the native core circuit power supply. For these applications, devices incorporating gate oxide cannot be used. To address this limitation, design methodologies that include comprehensive TCAD simulations, reduced measurements, and novel layout techniques have been demonstrated for the design of fully customizable single- and dual-polarity S-type I-V characteristics.

Using the discussed design approach, tailored P_1N_1-P_2N_2 and P_1N_1-P_2N_2//N_2P_3-N_3P_1 coupled devices have been developed for robust ESD protection. The devices permit the flexible design of symmetrical and asymmetrical S-type I-V characteristics and thus provide versatile solutions to meet demanding ESD protection requirements in advanced CMOS/BiCMOS technologies. ESD performance has been demonstrated in stand-alone devices, as well as in IC applications that incorporate different device structures developed in this study. The ESD devices and ESD-protected circuit applications have been characterized using TLP measurements, the HBM, MM, and IEC 1000-4-2 ESD standards, and emission microscopy images of optical beam induced current. The presented ESD design methodology and the resulting protection devices have been

successfully demonstrated in commercial products were standard ESD protection strategies were not suitable to meet the demanding requirements.

7.2. Outlook

Progress in the ESD area will continue to expand as new technologies and circuit applications emerge. This tendency and the accelerated IC development cycle demand more sophisticated and advanced methodologies and tools for ESD protection design and integration. These methodologies are vital for the advancement of the semiconductor industry roadmap.

Research is necessary in the establishment of new technologies with an optimum trade-off between performance, power handling capability, and cost. Even though this study has presented devices and design methodologies to extend the ESD protection capability in existing technologies, a major obstacle is the degradation of reliability to gain in the devices' downscaling. Unreliable devices for circuit design can be accepted to some extent for gigascale digital applications, where systems strategies are being researched to create reliable systems using unreliable devices. However, this solution at the architectural level still remains in the early stage of study and cannot be extended generally to mixed signal applications.

The strategy developed in this study for the custom design of ESD protection components is a first step in what is expected to become a standard practice. Development will continue not only by adapting the devices to the constraints of the technology, but also by creating the technology that will allow for the high performance and flexibility to implement robust and fully customizable ESD protection solutions. At this point, design tools for generation of tailored ESD protection devices, as well as research in the area of compact modeling are also fundamental for incorporating the new ESD devices in the standard design libraries.

Advancements in the introduction of numerical simulation tools and application of TCAD to ESD design and assessment have contributed to the physical understanding of the ESD phenomena and the enhancement of effective and more comprehensive strategies to address ESD problems. However, there are intrinsic limitations of accuracy, complexity, and convergence that require further improvements in the tools, which would result in a more reliable interpretation of 2D and 3D effects in ESD devices. In the same order of ideas, the establishment of sophisticated interfaces between circuit design evaluation using compact models and physics-based simulation at the system level would allow for better prediction and identification of several failures that are not well understood. In this approach, the simulation can predict not only physical phenomena inside the ESD protection structure, but also the overall condition in the chip system when the ESD is taking place. Due to the lack of these simulation tools, failures at the system level are traditionally evaluated using failure analysis techniques and trial-and error experimental procedures.

The ESD devices presented in this study provide the possibility of external voltage- or current- control of the turn-on and turn-off. Design of additional control components can be avoided as long as the ESD devices are properly designed to meet the requirements. However, the ESD protection requirements cannot always be fulfilled in this way. Given the current tendency toward narrower design widows and high ESD protection performance, the turn-on and turn-off control of the ESD devices will require more sophisticated solutions. These features can be incorporated in the devices presented in this study via gate- or substrate- triggering and are expected to be a topic of future research, especially for the design of devices that can respond fast enough to protect against ESD signatures such as those obtained during CDM stress.

APPENDIX
EXAMPLES OF TCAD INPUT FILES FOR ESD SIMULATION

In the next sections, examples of the simulation flows using TCAD statements for the analytical generation of doping profiles and input deck for steady-state, transient and mixed-mode simulation are presented. The simulations' setups for ESD assessment realized in this study utilize the scheme established in these inputs decks, followed by the necessary calibration or model adjustments applicable for each specific technology, ESD devices design or device assessment. The set of models proposed in these input decks considers the most critical physical models, important for ESD simulations discussed along this study. For more detailed information about the input deck statements and models, references [7]-[8], and [117], provide detailed description of the equations, parameters and further numerical considerations to address convergence problems. The device structures generated in this study have been obtained using a process simulation, which has been simulated using Athena/SSUPREM3 and analytical doping simulations. For reference, an example of the input deck for the analytical simulations is provided.

Analytical Structure Simulation: Atlas Input Deck

Nowadays, fabrication of ICs is frequently accomplished using outside foundries. The use of external foundries is becoming a common practice, but in this case, designers have access to limited information about the process. Different methods can be used to extract the information of the doping profiles. The obtained data can be subsequently incorporated in the TCAD input to generate custom ESD protection devices. The ESD device structure is then simulated by using analytical approaches to the doping profile, such as the discussed in chapter 2. In the next example is depicted the input deck developed for a 0.5-um CMOS process employed in this study for the assessment of a new generation of ESD devices for the ES-SoC application.

```
#*****************************************#
go atlas

TITLE Structure Simulation: HH-LVTSCR (n-type) Author: JAVIER A. SALCEDO

# (1) ESD DEVICE DEFINITION

# Analytic Device Structure Specification: Atlas's Command Language

# (1.1) Initial Mesh Specification
# Define the command language that establishes a 2D simulation area,
# and the distance between each point in the simulation mesh.
# In this example, the area extends in the lateral direction
# x = [from 0 to 14] and in the vertical direction y = [from -0.014 to 3].

mesh space.mult=1.0

x.mesh loc=0.0    spac=0.2
x.mesh loc=1.6    spac=0.1
x.mesh loc=2.8    spac=0.05
x.mesh loc=7.8    spac=0.02
x.mesh loc=9.6    spac=0.02
x.mesh loc=11.2  spac=0.1
x.mesh loc=14     spac=0.2

y.mesh loc=-0.014   spac=0.005
y.mesh loc=0.0       spac=0.02
y.mesh loc=0.1       spac=0.05
y.mesh loc=0.5       spac=0.05
y.mesh loc=1.6       spac=0.2
y.mesh loc=3.0       spac=1.0

# (1.2) Regions and Materials Specification

region number=1  y.min=0.0 silicon
region number=2  y.max=0.0 oxide

# (1.3) Electrodes Specification

electrode    name=drain     x.min=0.3  x.max=1.3  y.min=0.0  y.max=0.0
```

```
electrode    name=anode     x.min=3.1 x.max=4.1 y.min=0.0  y.max=0.0
electrode    name=gate      x.min=7.8  x.max=9.6  y.min=-0.014  y.max=-0.014
electrode    name=cathode   x.min=9.9 x.max=10.9  y.min=0.0  y.max=0.0
electrode    name=bulk      x.min=12.7  x.max=13.7  y.min=0.0  y.max=0.0

# (1.4) Analytical Doping Specification considering uniform and Gaussian doping distribution

# Substrate (p-), and Substrate ohmic contact (p+)
doping region=1 uniform conc=3.5e16  p.type outfile=lvt1_0.dop
doping region=1 gauss     conc=4e19    peak=0.0 characteristic=0.18 ratio.lateral=0.45 x.left=12.4 x.right=14 p.type

# N_well (n-)
doping region=1 gauss    conc=8e16 peak=0.0 junction=1.4 ratio.lateral=0.55 x.left=0.0 x.right=6.1 n.type

# Drain (n+), anode (p+)
doping region=1 gauss      conc=9e19  peak=0.0  characteristic=0.18  ratio.lateral=0.35  x.left=0.0 x.right=1.6 n.type
doping region=1 gauss      conc=4e19 peak=0.0 characteristic=0.18 ratio.lateral=0.45 x.left=2.8 x.right=4.4 p.type

# (n+) Drain of MOSFET above the blocking junction
doping region=1 gauss      conc=9e19  peak=0.0  characteristic=0.18  ratio.lateral=0.35  x.left=4.4 x.right=7.8 n.type

# Cathode (n+)
doping region=1 gauss      conc=9e19  peak=0.0  characteristic=0.18  ratio.lateral=0.35  x.left=9.6 x.right=11.2 n.type

# Regrid (This statement can be use to optimize previously defined mesh)
# regrid log doping ratio=6 outfile=lvtscr_r.str dopf=lvt.dop smooth.k=4

# Extract sheet resistance and junction depth from analytically simulated doping profiles
extract name="substrate rho" sheet.res silicon mat.occno=1 x.val=11.8 region.occno=1
extract name="p+ xj" xj silicon mat.occno=1 x.val=13.2 junc.occno=1
extract name="p+ rho" sheet.res silicon mat.occno=1 x.val=13.2 region.occno=1
extract name="n-well xj" xj silicon mat.occno=1 x.val=3.0 junc.occno=1
extract name="n-well rho" sheet.res silicon mat.occno=1 x.val=3.0 region.occno=1
extract name="n+ xj" xj silicon mat.occno=1 x.val=0.8 junc.occno=1
extract name="n+ rho" sheet.res silicon mat.occno=1 x.val=0.8 region.occno=1
```

```
# Save Analytical Simulation Output Structure
save outf=n-lvtscr1_nist.str
# Plot Structure
tonyplot n-lvtscr1_nist.str

#*********************************************#
```

Steady-State Simulation: Atlas Input Deck for I-V Characteristics Simulations and 2D Contours Extraction Pre- and Post- Snapback

The input deck presented below allows for the steady-state simulation of S-type I-V characteristics, and the extraction of the 2D doping contours for any selected simulation point. The simulation point where the *curvetracer* algorithm will be activated should be readjusted. The method employed in this study follows an initial assessment of the steady state simulation until the estimated voltage level where the trigger was expected, region in which the simulation gives convergence problems. At this point, the simulation can be stopped after the last stable point is saved. The last solution of the simulation can be loaded as initial condition, and the *curvetracer* algorithm is activated from this point to solve the next part of the simulation as described in chapter 5.

```
#*********************************************#

go atlas
TITLE ESD Simulation: Steady-State Simulation Author: JAVIER A. SALCEDO

# Load previously simulated Structure from Analytical simulation or process simulation
mesh inf=n-lvtscr1_nist.str   master.in

# Denition of Contacts Characterisitics
contact name=gate n.polysilicon
```

```
# This thermcontact define the external temperature border conditions (in this case 300 K)
thermcontac number=1 alpha=1000 temp=300 y.min=3 y.max=3

# PSYSICAL MODELS for electro-thermal simulation (carrier statistics, mobility model, recombination model, impact ionization)

models reg=1 fermi bgn auger cvt consrh lat.temp
#models reg=1 analytic fldmob bgn auger cvt consrh lat.temp (alternative set of models)
impact selb
# material reg=1 taup0=1e-7 taun0=1e-7 (definition of carrier lifetime in the material)

# Solutions
#Save I-V characteristics simulated in the next steps (before the curvetrace algorithm)
log outf=n-lvtscr1_nist_0.log
# Solve initial conditions (the different electrodes are biased to 0V)
solve init

#Steady State Simulation. The 2D contours indicated in the
# output statements are saved at the last point of each simulation set.
output flowlines charge e.field e.lines e.temp h.temp ex.field ey.field impact j.conduc j.total j.electron j.hole recomb

solve vanode=0.0 vstep=0.1 vfinal=1.0 name=anode
save outf= n-lvtscr1_nist_03-07-06_01.str master

solve vanode=1.2 vstep=0.2 vfinal=4.0 name=anode
save outf= n-lvtscr1_nist_03-07-06_03.str master

solve vanode=4.5 vstep=0.5 vfinal=9.0 name=anode
save outf= n-lvtscr1_nist_03-07-06_05.str master

solve vanode=9.2 vstep=0.2 vfinal=11.0 name=anode
save outf= n-lvtscr1_nist_03-07-06_07.str master

solve vanode=11.1 vstep=0.1 vfinal=11.7 name=anode
save outf= n-lvtscr1_nist_03-07-06_09.str master

# The load statement is used to load previous solutions when the simulation is
# interrupted. For instance, when it is stopped due to numerical convergence issues,
# the new simulation can start from the last reliable result, thereby saving simulation time.
```

```
#load infile = n-lvtscr1_nist_03-07-06_08.str master

#This solve statement set the compliance for initiation of the curvetrace algorithm
solve vanode=11.75 vstep=0.05 vfinal=11.95 name=anode compl=1e-6 cname=anode

# Save I-V characteristics simulated during the curvetrace algorithm.
log outf=n-lvtscr1_nist_1.log
# NUMERICAL METHODS
#method newton climit=1e-4 (alternative numerical method constraints)
method newton climit=1e-4 trap atrap=0.3

# Curve Trace algorithm end.val=5e-3
curvetrace  contr.name=anode  step.init=0.05  nextst.ratio=1.05  mincur=1e-9  end.val=5e-3 curr.cont

# Log File Creation (V-I Output File)
log outf=n-lvtscr1_nist_01.log

solve curvetrace
#save contours in on-state condition
save outf= n-lvtscr1_nist_03-07-06_09_on-1.str master
# save contours in other on-state conditions
output flowlines charge e.field e.lines e.temp h.temp ex.field ey.field impact j.conduc j.total j.electron
j.hole recomb
solve previous vanode=13.0 outf= n-lvtscr1_nist_03-07-06_on-2.str master
solve previous vanode=14.0 outf= n-lvtscr1_nist_03-07-06_on-3.str master
#Plot command. It can be used to display any output file “extensions “log” and “str”
tonyplot n-lvtscr1_nist_01.log

quit
#*******************************************#
```

Transient Simulation: Atlas Input Deck for Evaluation of ESD Device Response (including devices having snapback) During: 1) Variable Rise Time, 2) Variable Temperature, and 3) Variable Bias Condition

The transient simulation is a simpler approach than the mixed mode simulation, which can also give a close estimation of the transient performance of the device, and response to different

levels of stress and rise times. In the input deck below, the transient simulation is accomplished by using the transient waveform presented in chapter 2, which approximates the HBM. 2D contours can be also extracted for the different simulation points. This simulation takes more time than the steady-state simulation, but can reproduce the evolution of the I-V characteristics of the device during the transient stress numerical simulation.

```
#*******************************************#
go atlas
TITLE ESD Simulation: Transient Simulation Author: JAVIER A. SALCEDO
# Load Structure from analytical- or process-simulation
# Simulation input current waveform approaching HBM transient characteristics
mesh inf=n-lvtscr1_nist.str master.in

# CONTACTs CHARACTERISTIC
contact name=gate n.poly
contact name=anode current

thermcontac number=1 alpha=1000 temp=300 y.min=3 y.max=3

# PSYSICAL MODELS (carrier statistics, mobility model, recombination model, impact ionization)

#models reg=1 analytic fldmob bgn auger cvt consrh lat.temp

models reg=1 fermi bgn auger cvt consrh lat.temp
impact selb

method newton climit=1e-4 trap atrap=0.3 tauto

#setup quantities to monitor during simulation
#results go into the log file

# The next statements allow for evaluation of critical –electric field and temperature.
# These options can be used to research failures mechanisms
# vertical field across gate oxide
probe x=0.98 y=0.21 field dir=90 name=OxideField
# temperature at anode metal contact
probe x=3.8 y=0.22 lat.temp name=MetalTemp
```

```
# Solutions
log outf= tr_n-lvtscr1_nist_03-25-06_01_vg2.log master
solve init

#output  charge e.field e.lines e.temp h.temp impact j.conduc j.total j.electron j.hole recomb
solve ianode=0.0
solve vgate=2.0
#save outf= n-lvtscr1_nist_03-22-06_00_.str
## In the next statements, 2D contours are saved at different points of the simulation##
#method newton climit=1e-4 trap atrap=0.3 ^tauto
output  charge e.field e.lines e.temp h.temp impact j.conduc j.total j.electron j.hole recomb
solve ianode = 1.0e-3  ramptime = 1.e-9 tstep = 0.50e-11 tstop = 1.e-9
save  outf = n-lvtscr1_nist_03-25-06_01_vg2.str

solve ianode = 5.0e-3  ramptime = 4.e-9 tstep = 2.0e-11 tstop = 5.e-9
save  outf = n-lvtscr1_nist_03-25-06_02_vg2.str

solve ianode=10.0e-3  ramptime=5.e-9 tstep=5.0e-11 tstop=10.e-9
save  outf= n-lvtscr1_nist_03-25-06_03_vg2.str

#load infile= n-lvtscr1_nist_03-22-06_03_.str master

solve    ianode=0.0 decay=150e-9 tstep=1.e-9 tstop=40e-9
save  outf= n-lvtscr1_nist_03-25-06_04_vg2.str

solve    ianode=0.0 decay=150e-9 tstep=1.e-9 tstop=100e-9
save  outf= n-lvtscr1_nist_03-25-06_05_vg2.str

solve    ianode=0.0 decay=150e-9 tstep=1.e-9 tstop=200e-9
save  outf= n-lvtscr1_nist_03-25-06_06_vg2.str

solve    ianode=0.0 decay=150e-9 tstep=1.e-9 tstop=400e-9
save  outf= n-lvtscr1_nist_03-25-06_07_vg2.str

#solve   ianode=0.0  decay=150e-9 tstep=10.e-9 tstop=1000e-9
#save  outf= n-lvtscr1_nist_03-25-06_08_vg2.str

#solve    ianode=0.0 decay=150e-9 tstep=10.e-9 tstop=1500e-9
#save  outf= n-lvtscr1_nist_03-25-06_09_vg2.str
```

```
# The final response is plotted
tonyplot tr_n-lvtscr1_nist_03-22-06_03.log

Quit
#*****************************************#
```

Mixed-Mode Simulation: Atlas Input Deck for Evaluation of Device Response Using Lumped Circuits

In the input deck presented below, the simplified lumped circuit described in chapter 1 is incorporated together with the numerically simulated device that can be generated analytically or through process simulation. This input deck solves first the initial conditions in the device at DC, and in the second step, these initial conditions are loaded to solve the transient simulation of the device during the discharge of the capacitor. The waveform simulated resembles the HBM. By using the *save* statement in the second section of the simulation, the contours of the device can be also saved for different simulated points.

```
#*****************************************#
go atlas
TITLE Mixed-Mode ESD Simulation: Author: JAVIER A. SALCEDO
# Input device name generated from analytical- or process- simulation: pst-scr.str
# Simplified lumped circuit for HBM c=100pF, l=7.5uH, r=1.5 kOhm
# ESD stress: 2 kV; 100um device

# (1) The initial conditions are solved
.begin
c1 1 0 100p
l1 1 2 7.5u
r1 2 3 1.5k
apst-scr 0=cathode  3=anode width=100 infile= pst_scr.str
.nodeset v(1)=2000  v(2)=0  v(3)=0
.ic v(1)=2000  v(2)=0  v(3)=0
.numeric toldc=1.e-5 vchange=0.5 imaxdc=999
```

```
.options m2ln debug print=20
.save outfile=pst-scr-ic
.end
thermcontact num=1 device= apst-scr  ext.temp=300 alpha=1000
models device= apst-scr fermi bgn auger cvt consrh lat.temp
impact device= apst-scr selb
go atlas
# Using initial conditions solved in the previous case, the transient simulation is solved
# Structures after each simulation point are saved by using the save statement,
# while the I-V curve is saved by using the log statement. The load statement load the initial
# conditions.
.begin
c1 1 0 150p
l1 1 2 7.5p
r1 2 3 1.0e6 exp 1.0e6 1500 0. 1ps 10 10
apst-scr 0=cathode 3=anode width=100 infile=pst-scr.str
.numeric toltr=1.e-3 vchange=10. lte=0.1 dtmin=0.01ps

.ic v(1)=2000 v(2)=0
.options  print relpot
.tran 0.2ps   2.e-6

.load  infile=pst-scr-ic
.log outfile=pst-scr-log
.save outfile=pst-scr-tr
.end
thermcontact num=1 device= apst-scr  ext.temp=300 alpha=1000
models device= apst-scr fermi bgn auger cvt consrh lat.temp
impact device= apst-scr selb
#NUMERICAL METHODS
method climit=999
quit
#*****************************************#
```

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