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LATERAL POWER MOSFETS HARDENED AGAINST SINGLE EVENT RADIATION EFFECTS

by

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A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy
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Major Professor: Z. John Shen

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ABSTRACT

The underlying physical mechanisms of destructive single event effects (SEE) from heavy ion radiation have been widely studied in traditional vertical double-diffused power MOSFETs (VDMOS). Recently lateral double-diffused power MOSFETs (LDMOS), which inherently provide lower gate charge than VDMOS, have become an attractive option for MHz-frequency DC-DC converters in terrestrial power electronics applications [1]. There are growing interests in extending the LDMOS concept into radiation-hard space applications. Since the LDMOS has a device structure considerably different from VDMOS, the well studied single event burn-out (SEB) or single event gate rapture (SEGR) response of VDMOS cannot be simply assumed for LDMOS devices without further investigation.

A few recent studies have begun to investigate ionizing radiation effects in LDMOS devices, however, these studies were mainly focused on displacement damage and total ionizing dose (TID) effects, with very limited data reported on the heavy ion SEE response of these devices [2]-[5]. Furthermore, the breakdown voltage of the LDMOS devices in these studies was limited to less than 80 volts (mostly in the range of 20-30 volts), considerably below the voltage requirement for some space power applications.

In this work, we numerically and experimentally investigate the physical insights of SEE in two different fabricated LDMOS devices designed by the author and intended for use in radiation hard applications. The first device is a 24 V Resurf LDMOS fabricated on P-type epitaxial silicon on a P+ silicon substrate. The second device is a

much different 150 V SOI Resurf LDMOS fabricated on a 1.0 micron thick N-type silicon-on-insulator substrate with a 1.0 micron thick buried silicon dioxide layer on an N-type silicon handle wafer. Each device contains internal features, layout techniques, and process methods designed to improve single event and total ionizing dose radiation hardness. Technology computer aided design (TCAD) software was used to develop the transistor design and fabrication process of each device and also to simulate the device response to heavy ion radiation. Using these simulations in conjunction with experimentally gathered heavy ion radiation test data, we explain and illustrate the fundamental physical mechanisms by which destructive single event effects occur in these LDMOS devices. We also explore the design tradeoffs for making an LDMOS device resistant to destructive single event effects, both in terms of electrical performance and impact on other radiation hardness metrics.

Dedicated to my family.

ACKNOWLEDGMENTS

I would like to express my sincere gratitude and appreciation to Professor John Shen, my advisor and director of the Power Semiconductor Research Laboratory (PSRL) at the University of Central Florida. His enthusiastic lectures in an introductory semiconductor physics course first drew me toward the study of microelectronics and helped me realize my calling in this field. Our work together in the field of power semiconductor devices has been an incredibly exciting and rewarding experience.

I would like to acknowledge the support of Sandia National Laboratories in the fabrication and characterization of the 25 V LDMOS device presented in this work. Specifically, I would like to thank Brandon Witcher, Bruce Draper, Ralph Young, Daniel Savignon, and the rest of the Sandia microfabrication team involved in the project. I would also like to thank Paul Dodd for taking the initiative to present this work at the 2009 NSREC conference and later in the IEEE TNS.

I would like to thank Matthew Landowski, formerly of the UCF PSRL and presently at Lockheed Martin, for his continuation of the 25 V LDMOS work after I diverted my attention to development of the 150 V SOI device. Matthew is a good friend. His kind demeanor and enthusiasm for his work make him a pleasure to work with.

I would also like to thank Leif Scheick of NASA JPL for his open advice and informative discussions regarding SEE in vertical power MOSFETs. The sharing of his time and expertise is greatly appreciated.

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LIST OF ACRONYMS AND ABBREVIATIONS

BV_{DSS} ....Drain to Source Breakdown Voltage

BJT.................Bipolar Junction Transistor

DUT ....Device Under Test

EPI..................Silicon Epitaxial Layer

FET ....Field Effect Transistor

FOM...............Figure of Merit

g_m ....MOSFET Transconductance

IC....................Integrated Circuit

L_D ....Drift Length

LDD ....Lightly Doped Drain

LDMOS..........Lateral Double-Diffused MOSFET

MOSFET........Metal-Oxide-Semiconductor Field Effect Transistor

N_D...................N Drift Region Doping Concentration

PCH................P-Channel Region (also called P-Base)

Q_G...................Gate Charge

Q_{GD}.................Gate to Drain Charge

Q_{GS} ....Gate to Source Charge

Q_{RR} ....Body Diode Reverse Recovery Charge

R_B ....Base Resistance

R_D...................Drift Resistance

R_{DSON}.............Drain to Source On-State Resistance

Resurf............Reduced Surface Field Effect

SEB ....Single Event Burnout

SEE ....Single Event Effect(s)

SEL ....Single Event Latchup

SEGR ....Single Event Gate Rupture

SET ....Single Event Transient

SEU ....Single Event Upset

TID.................Total Ionizing Dose

TrenchFET .....Trench Gate Vertical Power MOSFET

T_{RR}..................Body Diode Reverse Recovery Time

VDMOS ....Vertical Double-Diffused MOSFET

V_{DS} ....Drain to Source Voltage

V_{GS} ....Gate to Source Voltage

V_{TH} ....MOSFET Gate to Source Turn-On Voltage (Threshold Voltage)

x_j.....................Junction Depth

CHAPTER ONE: INTRODUCTION

Modern electronics systems are based in most part upon silicon metal oxide semiconductor field effect transistor (MOSFET) technology. This technology is not only found in all types of modern digital electronics but also is the driving force within the power electronics circuits that drive those digital systems. As with all modern MOS technology, the specialized transistors used in power supplies remain vulnerable to all types of damaging and destructive effects caused by ionizing radiation [6][7]. These effects do not represent a significant concern in most environments, however they are of paramount importance for electronics systems designed to operate in ionizing radiation environments such as nuclear power facilities, medical equipment, and especially the most hostile radiation environments – earth orbit and deep space. Because ionizing radiation effects are only found in these and a few other unique environments, most MOS devices are not designed to withstand these effects. Devices and systems that are specially designed to withstand ionizing radiation effects are termed "radiation-hardened", or simply rad-hard.

In the case of power MOSFET technology, the differences between standard commercial devices and rad-hard devices are significant, not only in terms of cost, but also in terms of design and fabrication. The special features and design methods found in today's rad-hard power MOSFETs have arisen from decades of study of ionizing radiation effects in MOS devices, and specifically a wealth of study of one power device in particular – the planar VDMOS. The planar VDMOS has exclusively dominated the

market of rad-hard power MOSFETs, but unfortunately this device offers no further potential in terms of improving electrical performance. This leaves rad-hard power electronics technology at an impasse. Without the development of a replacement power MOSFET technology, the further advancement of power electronics in radiation environments is basically halted. For this reason, there has been a recent drive to develop alternatives to rad-hard VDMOS technology.

One such alternative we are exploring is the power LDMOS. Recently this device has found use in some of the most advanced MHz frequency DC-DC converter systems in the world. The LDMOS therefore offers huge potential for the modernization of radiation hard power systems, but it also presents some unique challenges, not the least of which is a lack of previous scientific study of ionizing radiation effects in lateral power MOSFET structures. A wealth of information is available for deep submicron NMOS devices, which are lateral structures, but these studies cannot take into account the radiation-induced failure mechanisms specific to higher voltage power MOSFET structures, specifically the single event effects such as single event burnout and single event gate rupture.

As part of an investigation into destructive SEE in lateral power MOSFETs, the author has designed and fabricated two types of discrete power LDMOS device with features, layout, and fabrication methods intended to provide hardness against SEE and other ionizing radiation effects. These devices are presented as characteristic representatives of two different power LDMOS technologies, both intended for use in

MHz frequency switching DC-DC converters, similar in terms of electrical performance to state of the art commercial trench VDMOS power MOSFET (TrenchFET) technology.

Evolution of Modern Power Electronics and Power Semiconductor Devices

Advancements in semiconductor device scaling and integration, especially in digital circuits, have largely driven the advancement of all types of modern electronics systems. Across the history of their development, digital components have become smaller and faster, with ever increasing density and complexity. Today's microprocessors operate at ever decreasing voltages and increasing currents, and as the requirements of these systems have changed, the technology of power electronics must become more advanced in order to keep pace. Figure 1 outlines some of the important relationships between advances in digital electronics and the accompanying demands placed on power electronics. Without corresponding advances in power electronics, modern computer systems would be penalized both in terms of computing performance and electrical efficiency.

The power electronics circuit which has the most impact on overall computer system electrical efficiency is the DC-DC converter. Most computing systems run off a 12 V DC bus, which is then stepped down to lower DC voltages throughout the system, depending on the demands of various computer components. The various microprocessors, memories, controllers, fans, drives, and other components each may

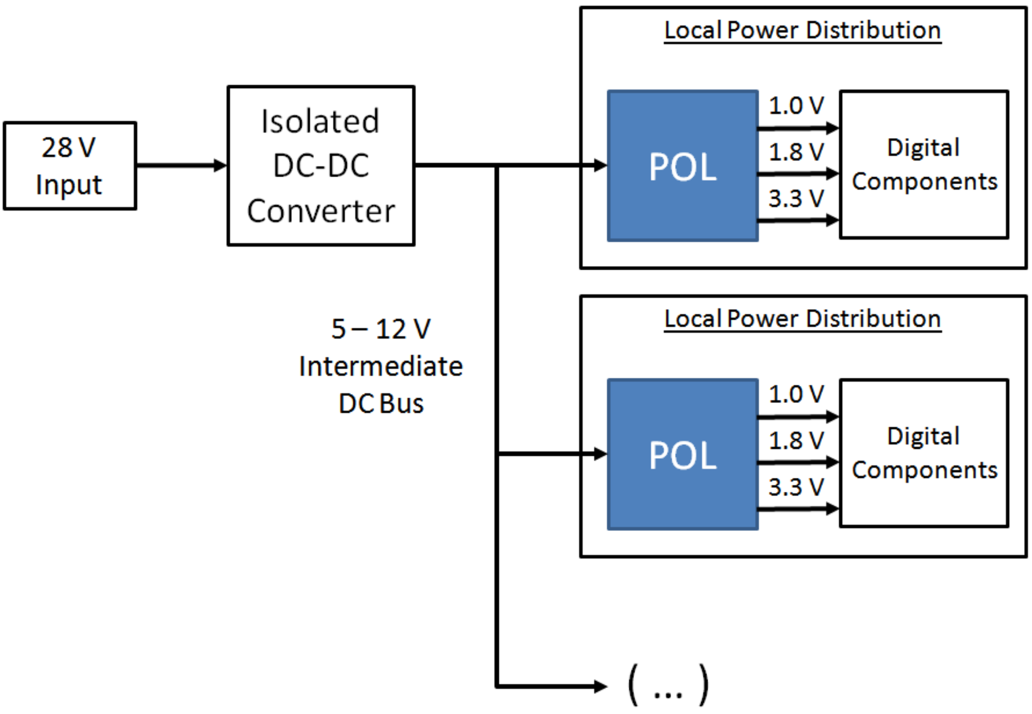
come with different voltage and current requirements. Power dissipation across these different loads may range from milliWatts to tens or even hundreds of Watts. As such, an all-in-one DC-DC converter system does not yield ideal efficiency across such a wide variety of loads, especially when these loads are scattered throughout the computer system, with relatively large distances between components.

The enablement of modern digital electronics systems through recent advances in power electronics technology.

Figure 1: Coupling of Modern Digital Systems and Power Electronics

Modern DC-DC converter technology has therefore evolved to match the distributed nature of these power demands with so-called distributed point-of-load (POL)

power architectures. POL power architecture refers to a method of distributing multiple DC-DC converter circuits throughout a system, with each converter being placed in close proximity to its own specific load [4]. Each converter is designed to meet the voltage and current requirements of its load in the most efficient way possible. An illustration of the distributed POL architecture is provided in Figure 2.



Simplified illustration of a distributed POL power architecture for a battery-powered space satellite system

Figure 2. Point-of-Load DC-DC Converter Architecture

In addition to new types of power distribution architectures, many modern digital systems also demand miniaturization of surrounding power electronics circuits and

components. The requirement for small volume, along with a need for faster transient load response, has driven power electronics circuits to operate at higher and higher switching frequencies, with some modern POL DC-DC converters now operating in the MHz frequency range. By switching at higher frequencies, a smaller inductor can be used in the DC-DC converter circuit. Since the inductor is by far the largest component in the circuit, this results in significant decrease in overall volume for the converter.

This increase in switching frequency brings several challenges. Switching tens of amps at MHz frequencies requires extremely low inductance packaging and routing. At such high dI/dt, even small parasitic inductances can cause transient voltage spikes can easily damage sensitive digital components, not to mention the power semiconductor components themselves. This requirement for low inductance design and packaging has resulted in a trend toward surface mounted "brick" DC-DC converter technology in desktop and server computers and monolithically integrated power system on chip (PSoC) technology for handheld devices, both of which are designed to operate at MHz frequencies with high volumetric power density (hundreds of W/in^3).

Introduction to Power MOSFET Design Considerations

These new demands on power electronics circuits, specifically higher current, lower voltage, and higher switching frequency place new requirements on the power semiconductor devices which drive those circuits. The power semiconductor device at the heart of the modern DC-DC converter is the n-channel power MOSFET. The overall

efficiency of the power switching circuit is influenced primarily by power losses across the power MOSFET. These power losses can be separated into two main types: *conduction* losses and *switching* losses.

Conduction Losses in Power MOSFETs

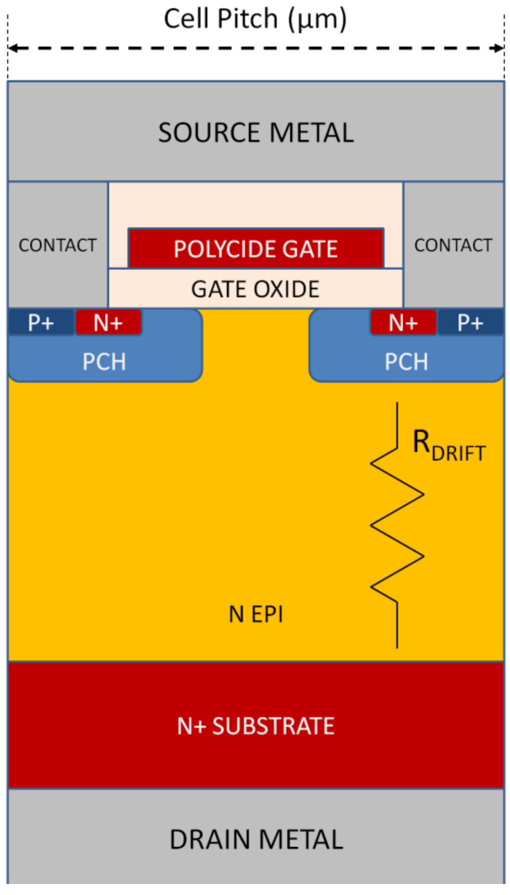
Conduction loss refers to power dissipation across the power MOSFET while it is operating in the "on" state, that is to say a positive V_{GS} potential is applied, and the MOSFET is actively conducting current through the MOS channel. Conduction power losses are determined primarily by the drain to source on-state resistance R_{DSON} of the MOSFET, and the power loss relationship is simply $I_{DS}^2 \cdot R_{DSON}$, where I_{DS} is the total on-state current. In terms of power MOSFET design, R_{DSON} is influenced by many factors. The most direct influence on R_{DSON} is the die size of the MOSFET. A power MOSFET die is actually a plurality of hundreds or even thousands of smaller parallel transistor cells, with the drains and sources of each cell electrically connected together in parallel, and each tied to a common gate terminal. Naturally, a larger die contains more area and therefore more parallel transistor stripes. Thus R_{DSON} has an inverse linear relationship with die size. Die size, however, is more or less independent of device technology and transistor cell design, and comparing the R_{DSON} of devices with two different die sizes tells very little about the merits of the technologies themselves. In order to effectively compare competing technologies, the R_{DSON} must be normalized to die area. This

normalized measurement is known as "area-specific R_{DSON}", or simply "specific R_{DSON}", and is generally given in units of $m\Omega\cdot mm^2$. The lower the specific R_{DSON} of a power MOSFET, the smaller die size will be required to achieve the same R_{DSON}, and therefore the more efficient the technology.

Specific R_{DSON} is influenced by many components, the most important of which for medium to high voltage power MOSFETs are the transistor cell pitch and the transistor drift resistance. Cell pitch is simply the length of the repeatable transistor structure, usually from contact to contact. Specific R_{DSON} has a linear relationship with transistor cell pitch, so the most direct method of reducing specific R_{DSON} is to reduce the cell pitch. Drift resistance refers to the resistance of the n-type lightly doped drain region (the n epitaxial layer in a VDMOS) between the N+ substrate and the P-Channel diffusion. Figure 3 shows a typical planar VDMOS power MOSFET cell, with the cell pitch and drift resistance labeled.

In terms of minimizing R_{DRIFT}, the classic design tradeoff is between R_{DRIFT} and drain to source breakdown voltage (BV_{DSS}). In any power MOSFET structure, BV_{DSS} is primarily determined by two design variables, drift length (L_D) and drift region doping concentration (N_D), both of which directly affect R_{DRIFT}. Higher breakdown voltage requires a longer L_D and a smaller N_D, both of which increase R_{DRIFT}. Very little can be done to reduce L_D for a device with a given BV_{DSS} rating, because of the fundamental limitation of the critical electric field (E_{CRIT}) in silicon, which is somewhat dependent on doping concentration and lies approximately between 2.5×10^5 and 5.0×10^5 V/cm. Once the applied drain to source voltage (V_{DS}) causes E_{CRIT} to form within the silicon, high

levels of impact ionization occur within the device, and the MOSFET is unable to sustain the applied voltage without conducting large amounts of current. In this condition, the MOSFET is said to be under avalanche breakdown, and the voltage at which this occurs is called the “avalanche voltage”. The rated BV_{DSS} which appears on a power MOSFET datasheet is always less than the actual avalanche voltage, generally by 10 – 20%. This difference between the rated BV_{DSS} and the avalanche voltage is called “de-rating”.



Planar VDMOS structure showing cell pitch and drift resistance (R_{DRIFT}) through the n epitaxial layer, which are the two most influential factors in determining area-specific on-resistance (R_{DSON}) of medium to high voltage power MOSFETs.

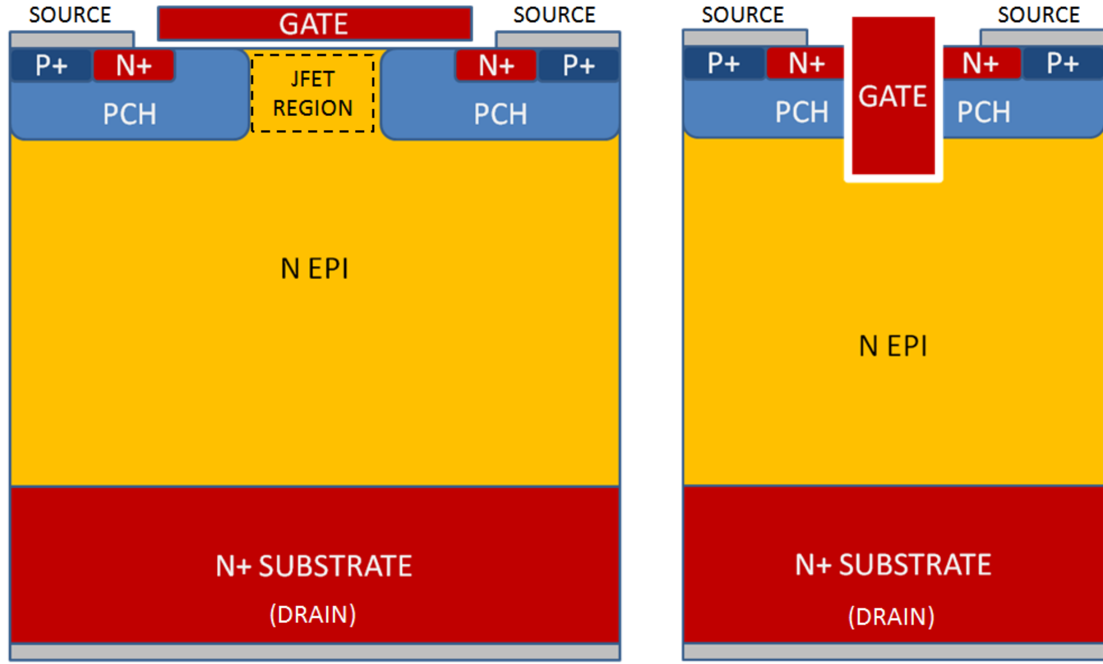
Figure 3: Planar VDMOS Device Structure

Since L_D is more or less fixed for a given avalanche voltage, most methods of reducing R_{DRIFT} focus on increasing N_D for a given BVDSS. Two such methods for increasing N_D both rely upon the so-called reduced surface field effect principle, or "Resurf" principle [8][9]. The Resurf principle is a method of increasing the natural breakdown voltage of a p-n junction by using carefully designed doping distributions, field plates, or other special doping and device geometries to control the spatial distribution of the electric field around the reverse-biased p-n junction. In an ideal Resurf design, the electric field at each point in the depleted semiconductor remains uniform. That is to say, there are no electric field "hot spots" in or around the depletion region which limit the breakdown voltage of the device. In practice, a completely uniform electric field distribution is impossible to achieve, but the spatial electric field distribution in a well designed Resurf structure comes reasonably close and looks very different from a normal p-n diode, in which the peak electric field occurs at the junction and decreases linearly toward the edges of the depletion region. The most popular Resurf design used in modern power devices is a so-called double Resurf or "superjunction" doping profile. A detailed discussion of this design technique is beyond the scope of this work, but a wealth of published literature is available on the subject. Another Resurf technique which applies only to LDMOS power devices is SOI Resurf, which is discussed in detail later in this work. Sufficed to say that implementation of Resurf designs has been the dominant influence on the reduction of R_{DRIFT} in modern power MOSFETs.

As mentioned before, the other important metric which directly affects R_{DSON} for any power MOSFET is the transistor cell pitch. By decreasing the cell pitch, more

parallel transistor stripes can be arranged per unit area on the MOSFET die, resulting in a direct linear relationship between transistor cell pitch and specific R_{DSON}. The cell pitch in a VDMOS device is primarily determined by the design of the source, channel, and junction field effect transistor (JFET) regions, which lie at the surface of the device. The JFET region is the N epi region underneath the poly gate and between the two adjacent P-channel diffusions. This is also sometimes called the "neck" region, which is the preferred terminology in this dissertation, since the term "neck" can also be used in discussion of LDMOS device structure which do not contain a parasitic JFET.

There is little that can be done to reduce the length of the source and channel regions of a power MOSFET, since these feature sizes are constrained by the limits of the available fabrication technology and also the need to prevent punch through or short channel effects between the drain and source. Low R_{DSON} VDMOS structures with reduced cell pitch have therefore resulted from the re-design of the more addressable JFET region, resulting in a new type of VDMOS structure known as the Trench Gate VDMOS or so-called "TrenchFET". A simplified TrenchFET device cross section is shown in figure 4. In a TrenchFET, the JFET and poly gate regions are replaced by a trench, which is surrounded by a thin thermal oxide and then refilled with polysilicon. The MOS channel is then formed vertically along the sidewalls of the trench, rather than laterally across the silicon surface as is the case with the planar VDMOS. By replacing the relatively wide JFET and channel regions with a much narrower trench gate, the TrenchFET results in a much smaller cell pitch than the planar VDMOS, and therefore boasts greatly reduced R_{DSON}.



Simplified device cross sections for two types of vertical double diffused (VDMOS) power MOFETS. The more modern Trench Gate VDMOS (TrenchFET) exhibits greatly reduced area-specific R_{DSON} compared to the planar VDMOS, because of its reduced transistor cell pitch.

Figure 4: Planar VDMOS and Trench Gate VDMOS Device Cross Sections

Switching Losses in Power MOSFETs

Switching losses refers to the power required to turn the MOSFET on and off during operation in the power switching circuit. In terms of the switching efficiency of a DC-DC converter, this term could include power losses related to design of the MOSFET gate driving circuit, however, in a discussion of power semiconductor devices, the term refers only to power losses due to the internal capacitances of the power MOSFET.

The two most critical MOSFET parametrics which determine switching efficiency are gate charge (Q_G) and body diode reverse recovery charge (Q_{RR}). Total gate charge is made up of the sum of gate to drain charge (Q_{GD}) and gate to source charge (Q_{GS}). Q_{GD} is also referred to sometimes as "Miller" capacitance. The ratio between Q_{GS} and Q_{GD} is determined by the power MOSFET device structure, i.e. how much the gate oxide overlaps either the source or drain regions within the transistor cell. Total Q_G for a discrete power MOSFET is determined by the gate oxide thickness and the total gate oxide area on the die. The doping concentrations in the silicon near the gate also have a secondary affect on QG, with lighter doping concentrations resulting in lower gate charge. Equation 1 shows a simple method for calculating QG:

$$Q_G = \frac{V \cdot A \cdot \varepsilon_{ox} \cdot \varepsilon_0}{t_{ox}} \qquad (1)$$

, where V is the applied voltage across the gate oxide, A is the gate oxide area, εox is the dielectric constant of the gate oxide (3.9 for SiO2), ε0 is the permittivity of free space, and tox is the gate oxide thickness.

Figure 5 shows cross sections of the planar and trench VDMOS structures with the internal gate capacitances labeled. As is the case with cell pitch, there are certain unavoidable device structure limitations which affect the magnitude of Q_G, specifically the length of the P-channel and N+ source regions. As such, Q_{GS} for a given technology remains more or less fixed. Most of the flexibility in terms of designing for low Q_G is in the reduction of Q_{GD}, which again is closely related to design of the neck region of the MOSFET. In the planar VDMOS, Q_{GD} can be reduced by removing some portion of the poly gate which lies over the JFET region. In the trench VDMOS, Q_{GD} can be reduced

by offsetting the polysilicon from the bottom of the trench with a thick insulator. One drawback of the TrenchFET is that the increased cell density per unit area, which gives the device its low specific R_{DSON}, also results in higher Q_G per unit area, which makes lowering Q_G the most challenging aspect of TrenchFET design.

Planar VDMOS

Trench Gate VDMOS

Device cross sections showing internal gate capacitances of the planar VDMOS and trench VDMOS power MOSFET structures. Internal gate capacitance is the most important device parametric which influences power MOSFET switching efficiency.

Figure 5: Internal Gate Capacitances in Planar and Trench VDMOS Structures

The other key device parametric for characterizing switching losses is Q_{RR}, which is the reverse recovery charge of the MOSFET's internal body diode (the diode formed by the drain and source). During normal operation in DC-DC converter circuits, the body diode of the power MOSFET is temporarily forward biased during each switching cycle. This results in an injection of electrons from the N+ drain into the drift region. In order for the MOSFET to full turn off, these electrons must first be removed from the semiconductor. The amount of charge which survives recombination and is collected at the device terminals is Q_{RR}, and the time required to collect this charge under a given current slew rate and biasing condition is T_{RR}, the reverse recovery time.

The power losses during reverse recovery are the product of the reverse recovery current multiplied by the junction potential of the body diode, which is usually estimated as 0.7 V. The device designer has very little control over the body diode junction potential, so methods of minimizing reverse recovery power losses focus instead on reducing Q_{RR}. There are two practical ways to minimize Q_{RR}. One way is to control the amount of stored charge in the device, which is done by minimizing the volume of the body diode [10]. The other way is to increase the electron recombination rate in the body diode, which is done by increasing the doping concentration of the P-channel region, or the P-base as it is sometimes called. A heavier p doping concentration results in a lower electron lifetime, meaning more electrons recombine in the P-base before being collected at the source electrode.

As is the case for nearly all power MOSFET design considerations, these two methods do not come without tradeoffs. The depth of the body diode is determined

primarily by the drift length, L_D, and it was explained earlier that L_D cannot be arbitrarily reduced without resulting in a decrease in BV_{DSS}. So for a VDMOS device, the reduction in charge collection volume is primarily a function of area, that is to say die size, and so the same techniques used to reduce specific R_{DSON} and shrink the die size also help to reduce Q_{RR}.

The other method – increasing minority carrier recombination in the P-base – requires either an increase in P-base doping concentration or an increase in channel length. The first, an increase in doping concentration, will result in a corresponding increase in Q_{GS} and gate to source turn on voltage (V_{TH}), if the p doping concentration near the gate oxide is increased. If V_{TH} becomes too high, then the device will not even function in the circuit. So, any design which seeks to decrease P-base minority carrier lifetime must be done in such a way as to not strongly influence the doping concentration in the MOS channel region. The second recombination control method, an increase in channel length, results in a decrease in transconductance (g_m), which is reflected in higher R_{DSON}. Additionally, for a planar VDMOS structure, a longer channel results in a longer cell pitch, which again further increases R_{DSON}. For a TrenchFET, a longer channel requires a deeper gate trench, which in turns requires a thicker epi layer. This results in a corresponding increase in stored reverse recovery charge, albeit an incremental increase for all but very low voltage devices. In any case this method is not desirable, since it probably does not result in any net increase in device efficiency.

Recent Advances in Lateral Power MOSFET Technology

As the demands of modern power electronics circuits have evolved toward lower output voltage, higher output current, and higher switching frequency, new demands have been placed on power MOSFETs which has prompted a re-examination of some of the fundamental design tradeoffs related to power MOSFET conduction losses and switching losses. Table 1 illustrates some of the ways in which these new circuit requirements have influenced power MOSFET design in recent years, particularly power MOSFETs designed for use in POL DC-DC converters.

Table 1. Requirements of Power MOSFETs in Modern POL DC-DC Converters

Demands of Power Electronics in Modern Digital Systems	Impact on Power MOSFET Design
Low Voltage	MOSFET BV_{DSS} < 10 V
High Current	MOSFET R_{DSON} < 1 mΩ
MHz Switching Frequency *(enables miniaturization and faster transient load response)*	Requires Low MOSFET Gate Charge (Q_G) Low Inductance Packaging (DirectFET, Flipchip) Monolithic Integration (SoC)

The power regulation requirements of modern digital electronics drive corresponding advances in power semiconductor device technology.

Older DC-DC converter circuits operated at slower switching frequencies, and most power losses were a result of conduction losses in the MOSFET. As such, the primary design tradeoff for older power MOSFETs was BV_{DSS} vs. R_{DSON}. This is still an important tradeoff, but as power MOSFETs are operated at higher switching frequencies, the switching power losses are now equally if not more significant than the conduction losses. Therefore the primary design tradeoff for modern power MOSFETs is no longer BV_{DSS} vs R_{DSON}, but is now instead R_{DSON} vs Q_G. This is expressed in the modern-day power MOSFET efficiency figure of merit (FOM), $Q_G \times R_{DSON}$. From a first order consideration, the power MOSFET with the lowest FOM offers the best efficiency in a fast switching circuit [11].

Modern POL converters not only operate at higher switching frequencies but also at higher current levels. This results in extremely high current slew rates, dI/dt. Just as these high dI/dt's have prompted a move toward low inductance packaging for DC-DC converter modules, so have they prompted similar advances in low inductance power MOSFET packaging. Such advances include so-called DirectFET™ and flipchip packaging technology, as mentioned in Table 1. Another method of reducing parasitic inductance is to co-package or even monolithically integrate multiple power MOSFET dies. The extreme case of such integration is the power system on chip (PSoC), where the entire DC-DC converter circuit, including magnetic components, is integrated onto a single die. These types of converters might be switched at frequencies in the tens of MHz in order to work with very small integrated inductors.

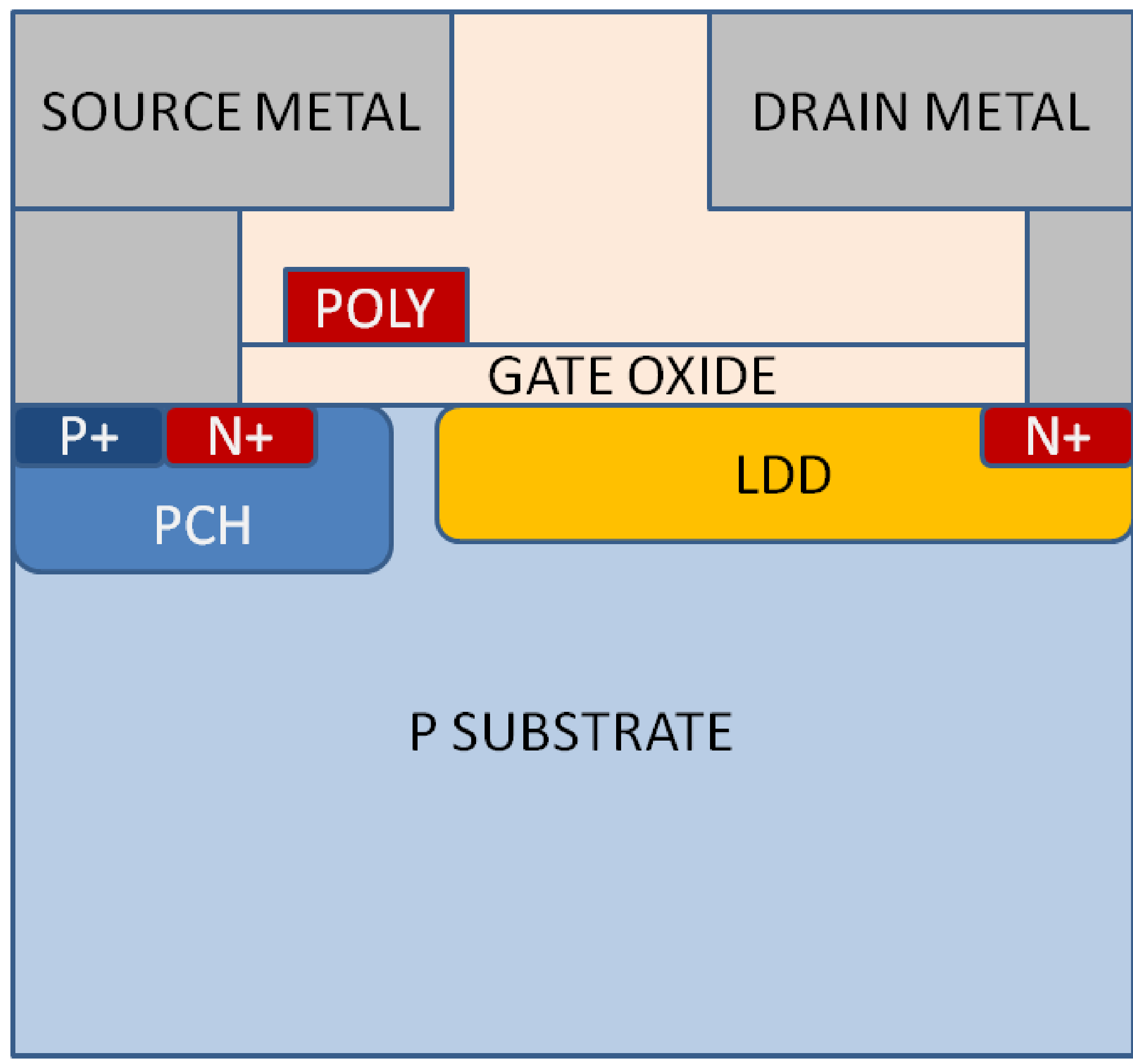
The higher current levels also demand MOSFETs with very low R_{DSON}. Fortunately, this requirement for ultra-low R_{DSON} comes with a corresponding relaxation of the BV_{DSS} requirement. As stated earlier, there are design tradeoffs involved which counterbalance BV_{DSS} and R_{DSON}, and the two generally have an inverse relationship – generally, but not always. Unfortunately, as planar and trench vertical power MOSFETs are scaled to very low BV_{DSS}, there comes a point at which there is no corresponding decrease in R_{DSON}. This occurs somewhere around 20 V, although the exact number of course depends very much on the specific technology. The reasons behind this point of diminishing returns are simple. First, as mentioned before, the cell pitch of a VDMOS transistor (either trench or planar), is more or less fixed for a given fabrication technology. There is no decrease in cell pitch corresponding to a decrease in the BV_{DSS} requirement. This means the only methods for reducing specific R_{DSON} in a VDMOS is in the vertical direction, by reducing the drift length (epi thickness) and reducing the parasitic N+ substrate resistance. Modern low voltage trench MOSFETs employ methods such as using specially doped “red phosphorus” substrates with very low resistivity. Manufacturers also thin down the wafers during processing to reduce the thickness of the N+ substrate down to just a few tens of microns, further reducing the substrate resistance. Finally, the epi layers are kept as thin as possible for the given breakdown voltage and gate trench depth, but care must be taken to avoid placing the bottom of the gate trench too close to the N+ substrate. Given the process tolerances involved with these methods, there are physical limitations to how much the epi and

substrate resistances can be reduced, and somewhere near BV_{DSS} = 20 V, these parasitic resistances make up a large portion of the total device R_{DSON}.

Finally, it was mentioned in the previous section that the low specific R_{DSON} of the TrenchFET comes with a corresponding tradeoff of high Q_G, due to increase in transistor cell density per unit area (high density of transistor gates). When scaling to lower BV_{DSS} with correspondingly lower V_{TH} requirements, Q_G becomes even higher, due to the thinner gate oxide required to meet the lower V_{TH} requirements.

Taking into account all these design tradeoffs, device designers are driven toward the consideration of new device structures specifically for fast switching, low voltage power supplies. One recently developed technology is the discrete lateral power MOSFET based on CMOS fabrication technology. These power MOSFETs are based on LDMOS or NMOS transistor cell structures which are then integrated and arranged in parallel to form a large scale power MOSFET. A basic LDMOS transistor cell structure is shown in figure 6. Prior to the development of flipchip interconnect technology, it was not possible to create a large scale, low resistance lateral power MOSFET. This is because a lateral MOSFET requires that both the source and drain metal interconnects be placed on the surface of the die, which contrasts the very low resistance metal planes on either side of a VDMOS die. The resistance of the interdigitated source and drain metal stripes increase as the transistor is scaled to a larger area. In the case of a low voltage MOSFET, this metal interconnect resistance would far outweigh the actual silicon resistance. With the advent of flipchip technology, Shen et al presented a method by

which a lateral power MOSFET could be formed to an arbitrarily large die size, with no corresponding "lateral scaling penalty" in RDSON [1].



Simplified cross sectional drawing of a Resurf LDMOS transistor cell. There are many types of n-channel LDMOS technologies, including some fabricated on an N substrate. This example is fabricated on a P substrate with an LDD region which is formed adjacent to the poly gate using a self-aligned ion implant process. This type of LDMOS offers very low Q_{GD},which is a key metric of switching power efficiency.

Figure 6: Resurf LDMOS Transistor Cell

Being able to overcome the lateral scaling penalty meant that very low voltage lateral power MOSFETs could be developed using submicron CMOS fabrication technology and then scaled to meet the high current demands of the modern POL converter. The transistor cell pitch of these lateral power devices could be made very small – as small as was possible while still supporting the required BV_{DSS}. At the same time, the metal interconnect resistance of the flipchip design was so low, that there was no practical limit for scaling of R_{DSON} and BV_{DSS}. The result of this work was the world's first power MOSFET with $R_{DSON} < 1$ mΩ with a BV_{DSS} rating of only 7 V and a record setting $Q_G \times R_{DSON}$ FOM.

Later, the development of discrete lateral power MOSFETs branched into higher voltages using LDMOS technologies. It was found that even though the specific R_{DSON} of the LDMOS structure was far greater than the TrenchFET, the FOM of the lateral devices were comparable if not lower than the TrenchFET due to the naturally low Q_G of the LDMOS structure [11]. LDMOS devices have much lower area-specific Q_G than TrenchFETs for two main reasons. The first reason is the larger cell pitch of the LDMOS, which results in fewer parallel gate stripes on the same chip area. The second reason is the fabrication method by which the LDD region is self-aligned with the poly gate, which results in the smallest possible Q_{GD} of any fabrication technology. Having a similar FOM with lower Q_G, along with the ultra-low inductance flipchip packaging, meant that the lateral FETs were especially well suited for use in POL converters operating in the MHz frequency range. Power MOSFET technology had finally broken through into the very low voltage, very high current regime.

Motivation

There is a long-standing disparity between terrestrial electronics and radiation hardened electronics in terms of performance and cost. Although modern sub-micron CMOS technology shows proven radiation tolerance, radiation-hardened power electronics continue to fail to meet the requirements of state-of-the-art digital circuits and therefore limit their use. This results in space craft being equipped with slower computers, less efficient power systems, and electronics of higher mass and volume than would be found on Earth in similar applications. The slow pace of technological evolution in the rad-hard power MOSFET field is due mostly to the unique fabrication and design challenges involved in making a power MOSFET resistant to ionizing radiation, also in part to the rigorous and costly qualification testing required to certify a part as rad-hard, and finally to the natural reluctance of engineers in the high reliability electronics sector to adopt the risks associated with using unproven semiconductor technology in a harsh ionizing radiation environment. Additionally, the cost of special radiation-hardened electronics remains very high due to low sales volume and a long development cycle. The cost of developing hardened components, coupled with the financial risk inherent in competing within a niche market, has resulted in an overall lack of competition among manufacturers of this specialized technology. This lack of driving market forces has resulted in an overall lack of development of new technologies, specifically in the arena of power semiconductor devices.

As described in the previous section, the heart of modern low-voltage power supplies is the power MOSFET. The performance of power electronics systems is most

affected by the technology of these transistors. When compared with older systems, the power MOSFETs required to supply modern digital systems must switch at higher frequencies and exhibit lower conduction losses and internal capacitance. There is presently a lack of rad-hard power transistors with these characteristics. Rad-hard power MOSFET products have not benefited from recent advances in commercial power MOSFET technology, and therefore rad-hard power MOSFETs suffer from significantly higher specific R_{DSON} and higher Q_G than their commercial counterparts. Figure 7 illustrates the differences in FOM between modern day commercial and rad-hard power MOSFETs.

Present day rad-hard power MOSFETs are based on planar VDMOS technology, whereas TrenchFETs and lateral power MOSFETs (LDMOS) are used in today's most advanced commercial power electronics products. Although they lag far behind modern FETs in terms of performance, there are advantages to rad-hard planar VDMOS technology. First is a proven track record after decades of flight time in radiation environments. The second is a wealth of scientific study and understanding of the fundamental physical mechanisms that affect planar VDMOS device reliability in radiation environments. However, without the development of an advanced rad-hard TrenchFET or LDMOS, or some other similarly-performing technology, the state of the art in rad-hard power electronics systems will continue to lag decades behind the commercial world. At some point, it must be decided whether the risks inherent with adopting a new rad-hard technology are outweighed by the potential benefits in terms of being able to efficiently power more advanced digital systems in these environments.

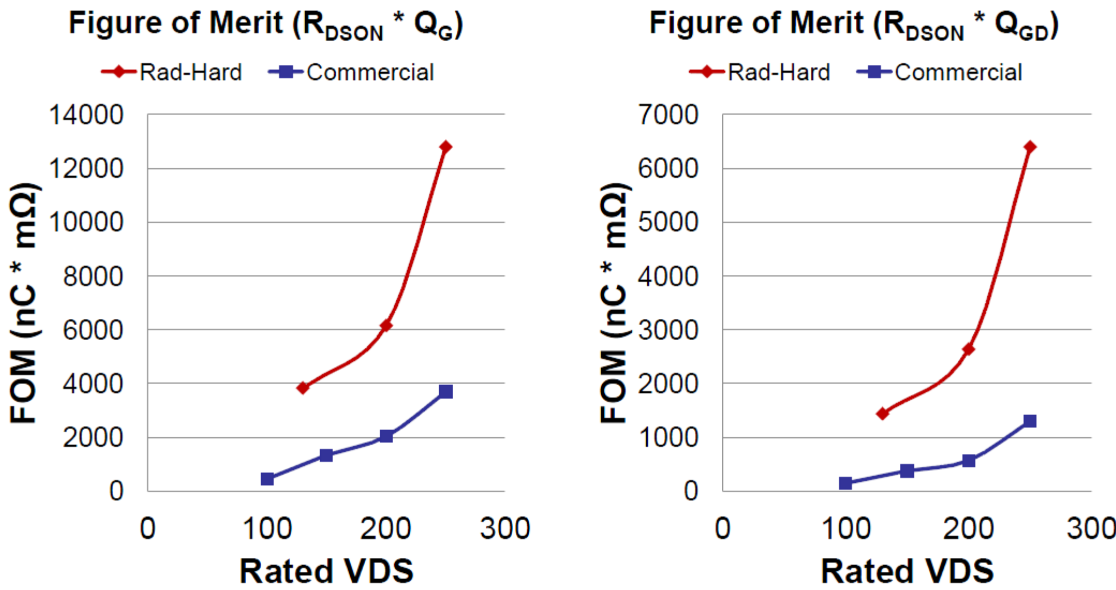


Figure 7: FOM Comparison of Rad-Hard vs Commercial Power MOSFETs

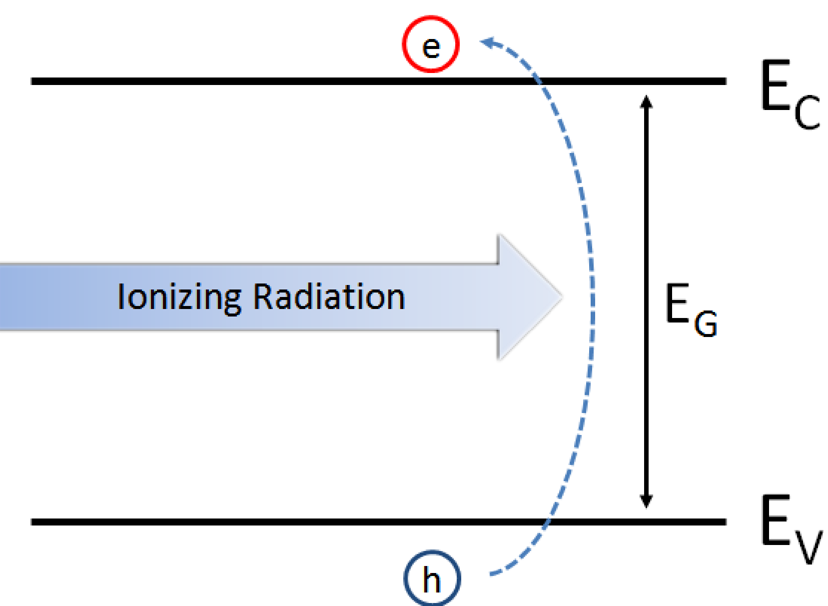
Aside from the significant performance penalty associated with the use of outdated planar VDMOS technology, rad-hard power MOSFET performance is further hindered by the severe electrical de-rating required to safely operate power MOSFETs in a radiation environment which might produce single event radiation effects (SEE) [12]-[14]. SEE refers to a broad array of disruptive, and sometimes catastrophically destructive, transient radiation events affecting semiconductor devices. Power MOSFETs remain especially vulnerable to destructive SEE, because of their high operating voltages and correspondingly high electrical stresses. The mechanisms of why

this is true will be explained in great detail later in this work. Recently published data suggests that modern rad-hard planar VDMOS can experience destructive SEE failure at operating voltages less than 20% of their rated DC voltages [15][16]. This data will be discussed in more detail later in this work during the discussion of the physical mechanisms of destructive SEE. Given the need for such extreme electrical de-rating, it is worthwhile to explore whether other power MOSFET structures exhibit SEE sensitivities similar to the planar VDMOS. If an alternative power MOSFET structure with a lower performance FOM could be developed, which also demonstrates an improved SEE safe operating area, then the electrical performance benefit would be compounded by a relaxation of the de-rating requirement. Furthermore, it is possible that the overall reliability of the rad-hard power electronics circuit could be improved.

Review of Ionizing Radiation Effects in Semiconductor Devices

Carrier Generation

Ionizing radiation generates electron-hole pairs as energy is transferred from a radiation source (photons, subatomic particles, or nuclei) to an absorbing material, such as a semiconductor. A simplified illustration appears in figure 8, which shows a generic diagram of the energy bandgap between the conduction band and the valance band in an arbitrary target material. In the simplest terms, ionization occurs as energy from the incident radiation is absorbed by electrons in the target material, which are then accelerated from the valence band into the conduction band, leaving a hole behind.



Energy from ionizing radiation is absorbed by the target material, accelerating electrons from the valence band to the conduction band, leaving a hole behind.

Figure 8: Electron-Hole Pair Production

Different carrier generation mechanisms are associated with radiation of different types and energies [6][17]-[20]. Particle radiation such as protons, neutrons, and larger nuclei generate carriers via direct ionization mechanisms, either through collisions with or Coulombic interactions with nearby atoms. An example of Coulombic interactions would be a positively charge heavy ion passing through a material, wherein the positive charge of the large nucleus exerts enough Coulombic force to pull negatively charged electrons away from their orbital shells in nearby atoms.

Another possible ionization mechanism associated with nuclear particle collisions is indirect ionization from nuclear decay [21]. In this case, the total energy absorbed by the target material can be more than was present in the original particle, due to the energy release of the nuclear fission reaction. The by-products of nuclear fission, namely the smaller nuclei and any associated EM radiation, can also be ionizing in nature. Furthermore, long term localized ionization may occur as decayed atoms remain trapped within the lattice, causing a displacement defect.

In the case of high energy photons (X-rays, γ-rays), there are three associated carrier generation mechanisms. In order of energy required, these three effects are the photoelectric effect, the Compton effect (Compton scattering), and pair production. In the case of the photoelectric effect, the entire energy of the photon is absorbed by an electron, which is energized into the conduction band, leaving a hole behind. In the case of Compton scattering, the energy and momentum of the photon accelerates an electron into the conduction band, but the electron in turn recoils, giving back some kinetic energy and sending a photon of reduced energy off in a new direction. For a wide spectrum of

photon energies (<0.1 to >10 MeV), Compton scattering is the dominant carrier generation mechanism in silicon [20]. Finally, in the pair production process, a high energy photon is absorbed and ejects both an electron and a positron. The positron is quickly annihilated and releases two 0.51 MeV γ-rays, which may then cause further ionization.

In terms of the spatial distribution of ionization, exposure to most EM radiation sources generally occurs more or less uniformly across the entire semiconductor device or integrated circuit (IC). One notable exception would be an artificially-generated beam, such as a laser. Naturally, ionization from particle radiation is much more localized, and free carriers are generated generally within a submicron radius along the path of the incident particle. This path becomes a highly conductive region, which when caused by heavy ion radiation is sometimes referred to as an "ion shunt".

Linear Energy Transfer (LET) is the metric which quantifies the magnitude of energy deposition as radiation penetrates its target material. Usually LET is used to describe energy transfer from particle radiation, although it can also be applied to EM radiation. LET is expressed in units of deposited energy per unit length, and then normalized to material density, as shown in equation 2:

$$LET = \frac{Energy}{Length} \times \frac{1}{Density} = \frac{MeV \cdot cm^2}{mg} \qquad (2)$$

The LET-dependent rate of electron-hole pair production is shown in equation 3:

$$\frac{\#ehp}{cm^3} = LET \cdot \rho \cdot \phi \cdot \frac{1}{E_p} \qquad (3)$$

, where ρ is the density of the target material, ϕ is the fluence of the incident radiation, and E_p is the material-dependent energy required to generate an electron-hole pair. For reference, $E_p(Si) = 3.6$ eV and $E_p(SiO_2) = 17$ eV.

LET is not constant for a given type of radiation as it passes through a material. As the radiation sheds its energy, its rate of energy transfer also changes. In this way, the instantaneous LET is constantly changing. So, in order to predict the LET of a given particle, both its mass and energy must be known, as well as the properties of the target material. Comparing two particles of the same mass, fast moving particles generally shed less energy than slow moving particles. At least this is the case until a particle slows to a specific energy, at which the linear energy transfer reaches a peak, known as the Bragg peak. A energies below its Bragg peak, the particle will quickly deposit all of its remaining energy within the target material. This behavior becomes very important when conducting radiation testing where the location of the Bragg peak plays a role in determining the response of the semiconductor device, as is later shown to be the case with power MOSFETs.

Generation of electron-hole pairs in and of itself does not describe ionizing radiation effects in semiconductor devices. The effects of interest actually occur during the subsequent transport and recombination of the generated carriers. There are numerous classifications of ionizing radiation effects in semiconductor devices, but most

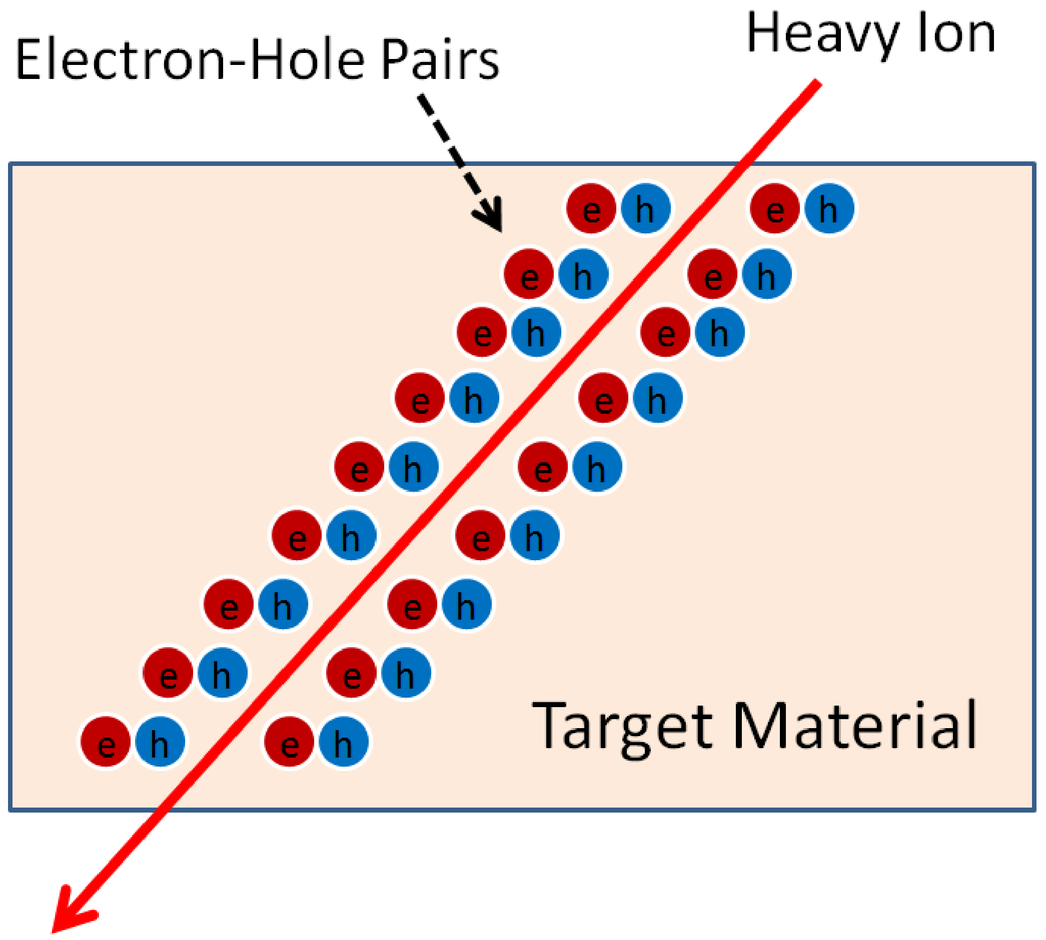
fall under the larger umbrellas of single event effects (SEE) or total ionizing dose (TID) effects. The next sections introduce these two types of effects in more detail.

Single Event Effects

The term "single event effect" describes exactly what the name implies, that is an effect arising from a non-recurring interaction with a single radiation source or event. SEE are the effects of sudden events, not prolonged exposure, and they are normally associated with *high photocurrent density* in the semiconductor device. For example, shining a household light bulb on a photodiode for a long time will produce a sustained photocurrent, but a household bulb is unlikely to produce sufficient current density to result in single event effects. By contrast, exposing the same photodiode to a short high energy laser pulse will produce a sudden large increase in current, the effects of which could be classified as SEE.

Technically, single event effects can occur as a result of sudden exposure to sufficient levels of any type of ionizing radiation, but the term SEE is used most commonly when discussing exposure to particle radiation, usually nuclei. These are the SEE referred to in this work. The "single event" itself will be defined as the highly localized interaction between the semiconductor device and a single particle. The "single event effects" describe the transient response of a semiconductor device to the localized generation of free electrons along the path of the incident particle. The localized electron

generation associated with SEE is frequently referred to as "charge deposition", and the total amount or concentration of generated electrons is called the "deposited charge". A simple illustration of charge deposition is shown in figure 9.



This example shows electron-hole pair generation around the trajectory of a heavy ion passing through an arbitrary target material. Linear energy transfer (LET) describes how radiation sheds its energy per unit length as it passes through a target material. The rate of electron-hole pair generation is proportional to LET. When a heavy ion passes through an electric field in a semiconductor device, the highly conductive trajectory of the ion is sometimes referred to as an "ion shunt".

Figure 9: Heavy Ion Charge Deposition

In a semiconductor device, SEE are caused by the transport and collection of deposited charge at the device terminals. There are many classifications of SEE, most of which do not apply to power MOSFETs.

Single Event Upset and Single Event Latchup

Single event upset (SEU) and single event latchup (SEL) are the most frequently studied SEE in integrated circuits but do not apply to power MOSFETs. SEU refers to a short spike of photocurrent which upsets the input or output of a node within an integrated circuit. In fast switching logic circuits, whose function relies on precise timing and control of current pulses, such SEU frequently generates data errors. Similar photocurrent perturbations in analog circuits must either be filtered out, or they can lead to erroneous operation of the circuit. Device and circuit designers cannot eliminate the photocurrent pulses which SEU. They can only try to minimize and contain the resulting circuit effects through careful design, which among others includes techniques related to circuit layout, fabrication process, and error handling. In cases where the photocurrent does not cause an adverse effect in the operation of the circuit, the photocurrent current pulse is known simply as a single event transient (SET).

SEL by contrast is a destructive effect which occurs in devices with a four-layer structure with three back-to-back p-n junctions. This type of structure is often referred to as a parasitic thyristor, after the power semiconductor device of the same name. Multiple well bipolar and CMOS technology usually contain these parasitic thyristor structures.

The parasitic thyristor can be represented as an NPN and PNP bipolar junction transistor (BJT) connected in a self-amplifying configuration, where the emitter of each transistor is tied to the base of the other. At a given critical charge, under a given bias condition, the BJT pair "latches up". That is to say, it enters a self-sustaining regime of current amplification and positive feedback. Eventually the current density reaches a point at which the power dissipation heats the semiconductor lattice to its melting point.

Due to the small feature sizes of modern deep submicron CMOS devices, a relatively small amount of deposited charge is required to generate SEE in those devices. Consequently, SEE in deep submicron CMOS devices can arise from interaction with alpha particles and even subatomic particles.

Single Event Burnout

Single-event burnout (SEB) is a destructive SEE that occurs primarily in N-channel power transistors [7]. SEB is most often associated with heavy ion radiation, but it can occur as a result of any type of radiation which produces high levels of photocurrent within the device. The basic mechanism is similar to SEL, except SEB occurs in devices where there is no parasitic thyristor structure. Instead, all that is required to cause SEB is a single parasitic bipolar junction transistor. SEB occurs when the parasitic BJT is put into a self-sustaining forward active operating mode as a result of high photocurrent. The forward active operation is initiated and sustained by a complex mechanism, which is described in detail later in this work. Whether or not SEB occurs

for a particular device depends on a combination of factors. Independent of device design, the most influential factors on SEB are the LET and trajectory of the radiation (assumed to be a heavy ion), and the biasing conditions at the device terminals [22]. It should be noted that N-channel devices are more susceptible to SEB, because their parasitic NPN bipolar transistor has higher current gain than the parasitic PNP bipolar transistor of a P-channel MOSFET. Unfortunately, N-channel devices are almost exclusively used in power switching applications, in part because their R_{DSON} is typically half that of a similar P-channel device, and also because power switching circuits generally require a normally "OFF" power MOSFET.

Single Event Gate Rupture

Single Event Gate Rupture (SEGR) is another destructive SEE mostly associated with power MOSFETs and heavy ion radiation. SEGR occurs when a power MOSFET is biased in the OFF state, and a high electric field, on the order of MV/cm is applied across the gate dielectric of a power MOSFET. When a heavy ion passes through the gate oxide under these biasing conditions, it generates electron-hole pairs within the oxide, according to the ion LET and the electric field-dependent generation rate inside the dielectric. At almost the same instant, electron-hole pairs are being generated. both within the polysilicon above the gate oxide, and also in the silicon layers along the ion trajectory underneath the oxide. In this way, an ion shunt is formed through the gate oxide, connecting the gate terminal at ground potential to some portion of the drain

region of the MOSFET, which lies at a higher potential. This potential difference results in high photocurrent density below the gate oxide and high electrical stress across the gate oxide. It is thought that SEGR occurs as a result of interaction between the temporary conductivity of the oxide and the high electric stress across the oxide, resulting in a localized current filament through the oxide [23].

In some cases, SEGR manifests as a small increase in gate-to-source leakage current, suggesting highly localized damage [24]. In other cases, SEGR is catastrophically destructive, resulting in much higher levels of gate leakage current and loss of control over the MOSFET. Another case occurs in which both SEGR and SEB occur more or less simultaneously. Conclusions about the physical mechanisms behind this type of failure can be drawn based on which bias conditions caused the failure. It is likely that in some cases SEGR leads to SEB, whereas in other cases SEB leads to SEGR [7].

Total Dose Effects

The quantitative measure of accumulated energy absorbed from ionizing radiation is called the “dose”. The SI unit for radiation dose is the Gray [Gy], however when discussing ionizing radiation effects in semiconductor devices, the dose is commonly measured in units of rads [rd]. One Gray represents the dose of ionizing radiation required to transfer 1 J of energy per kilogram of target material, and 1 Gy = 100 rads.

Both units are material-specific, because the amount of generated electron-hole pairs corresponding to a given type and energy of radiation varies according to the properties of the target material. These units are therefore a way of normalizing radiation dose measurement across different materials. In the notation of radiation dose units, the material name appears in parentheses after the unit. For example, rads(Si) are units of absorbed radiation dose for silicon, whereas rads(SiO_2) are units for silicon dioxide.

In contrast to SEE, total ionizing dose (TID) effects, refer to the effects of accumulated ionizing radiation exposure and the resulting damage within a semiconductor device. TID effects can be categorized into two major types – charge trapping effects and displacement damage. Charge trapping effects occur in the semiconductor device insulating layers, whereas displacement damage can occur within the semiconductor crystal lattice itself. Displacement damage is caused by exposure to high energy protons, neutrons, and nuclei, where the incident particle deposits sufficient energy to displace atoms either through collision or via a nuclear reaction. Charge trapping effects can be caused by any type of ionizing radiation, and the effects are highly dependent on the characteristics of both the incident radiation and the semiconductor or insulator target material [25]. In most cases, charge trapping effects in MOS devices manifest as a gradual degradation of device performance and functionality due to the buildup of charge in the MOSFET gate oxide. In bipolar devices, charge trapping effects are normally associated with a decrease in transistor gain and cutoff frequency, due to the increase in recombination that occurs in the charge trapping sites. Microdose effects are a very specific type of TID effect that arise due to exposure to heavy ion radiation.

The mechanism of charge trapping in silicon dioxide has to do with the difference in electron and hole mobility in SiO_2, where electron mobility is more than 10,000 times greater than that of holes. This means that as electron-hole pairs are generated within SiO_2, the electrons can be swiftly swept away by any applied electric field, whereas the holes remain more or less fixed within the oxide. For this reason, most of the electrons and holes are not able to recombine within the oxide, and a large number of holes become trapped within the oxide bulk. Meanwhile, electrons remain trapped at the Si/SiO_2 interface. At the interface, dangling bonds are present between the amorphous SiO_2 and the silicon crystal lattice. These interface states act as charge trapping centers by allowing electrons to remain at energy levels that fall within the normally forbidden energy bandgap of silicon.

Because charge transport is the underlying mechanism behind TID charge trapping, the ratio of unrecombined holes as a fraction of generated electron-hole pairs is highly dependent on electric field. A stronger electric field will sweep away the electrons more quickly, resulting in a higher fraction of unrecombined holes. At fields near 5 MV/cm, the fraction of unrecombined holes approaches almost 100% [26]. Trapped charge density is also highly dependent on oxide thickness. From a first order perspective, the magnitude of bulk trapped charge is linearly proportional to oxide thickness, whereas interface trapped charge density is proportional to the square of oxide thickness [27]. Finally, the "quality" of the oxide, which generally describes the density of bulk and interface states prior to radiation, has a severe impact on the susceptibility to TID effects.

The most commonly studied TID effects are threshold voltage shifts and increased leakage current in MOS devices. Threshold voltage shifts are attributed to the accumulation of trapped charge within the gate oxide and along the gate oxide interface. Positive trapped charge lowers the magnitude of the threshold voltage (V_{TH}) of NMOS devices, while negative trapped charge has the same effect for PMOS devices. Threshold voltage shifts over time can become so dramatic that N-channel transistors become normally "ON" devices [28].

Increased leakage current is the other commonly observed effect, particularly in CMOS integrated circuits. Aside from leakage through the MOS channel of a severely affected transistor, parasitic leakage paths also commonly occur along the shallow trench isolation (STI) oxides used in many IC layouts to isolate circuit elements. The deposited STI oxide generally contains more bulk and interface states than a thermally grown gate oxide. Also, the thickness of the STI oxide is several orders of magnitude larger than that of a typical gate oxide. The combination of an extremely thick oxide with a high number of bulk and interface states means that a lower radiation dose is required to generate the same amount of oxide and interface trapped charge.

Leakage around STI oxides occurs when the oxides lie over lightly doped regions which connect otherwise isolated device structures. As charge accumulates in the STI oxide, the lightly doped silicon underneath can become easily inverted, much the same way inversion occurs in the channel of a MOSFET as it is turned ON. These parasitic channels can be eliminated through careful layout techniques and also by avoiding the

placement of STI over lightly doped regions. Methods of hardening ICs using such techniques are referred to as “hardening by design”.

CHAPTER TWO: SINGLE EVENT RADIATION EFFECTS IN POWER MOSFETS

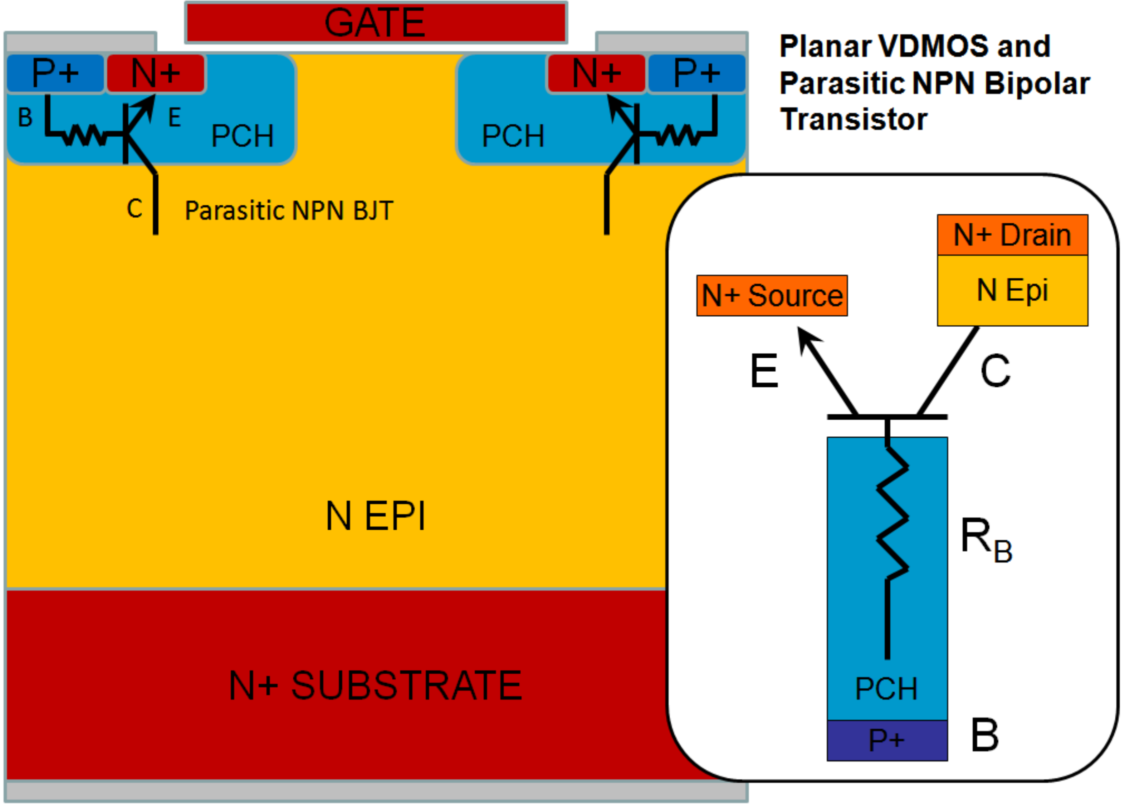
More destructive single event effects occur in power MOSFETs than in low voltage integrated circuits, due to the fact that power MOSFETs operate at higher voltages with large inductive and capacitive loads. From the point of view of a power MOSFET designer, the only two single event effects of any real concern are the destructive effects of SEB and SEGR. These effects occur almost exclusively in power MOSFETs and are not generally observed in low voltage integrated circuits. Conversely, many other SEE are applicable only to integrated circuits and do not apply to power MOSFETs. These include the effects of single event upset and single event latchup. Single event transients can and do occur in power MOSFETs, however whether these SETs cause an upset in the power electronics circuit is more dependent on circuit design than MOSFET design. Therefore, in terms of hardening power MOSFETs against SEE, the focus is on SEB and SEGR.

Furthermore, in practical application, these two effects are almost always associated with heavy ion radiation. The focus of hardening the devices can be further narrowed down to deal with only this particular type of radiation. It is known that SEB can also occur from other types of radiation exposure, but regardless of the type of radiation, the internal physical mechanisms behind SEB remains the same, and so the same hardening methods are assumed to apply regardless of the type of radiation. Except in cases where SEGR occurs as a result of SEB, the author knows of no known radiation source except heavy ions that are associated with SEGR. So the discussion in this work

from this point forward will focus entirely on SEE in power MOSFETs as a result of heavy ion radiation.

Single Event Burnout in Planar VDMOS

As stated previously, single event burnout occurs due to the activation and self-sustained operation of the parasitic NPN bipolar junction transistor inherent in the N-channel power MOSFET device structure. Figure 10 shows a simplified cross section of a planar VDMOS with the parasitic NPN bipolar junction transistor clearly labeled. The figure insert shows another representation of the parasitic BJT, with the base, collector and emitter terminals drawn together with their corresponding device features. Externally, the emitter and base of the parasitic NPN are tied to the same potential at the source contact of the MOSFET. Internally, there is a distributed resistance within the P-Channel diffusion, which makes up the base of the NPN. This so-called base resistance is labeled R_B in the insert.



Each transistor cell of an N-channel power MOSFET contains a parasitic NPN bipolar junction transistor (BJT) structure. The activation and sustained operation of the parasitic NPN can lead to single event burnout.

Figure 10: Planar VDMOS and Parasitic NPN Bipolar Junction Transistor

Figure 11 shows a cross section of a planar VDMOS where the gate and source terminals are tied together at the same potential ($V_{GS} = 0$), and a positive potential is applied between drain and source ($V_{DS} > 0$). These are the biasing conditions normally associated with single event burnout. As a heavy ion traverses the VDMOS device structure, it deposits a wake of electron-hole pairs in its path, known as an “ion shunt”. Because of the externally applied V_{DS} bias, electron current drifts through the N epi

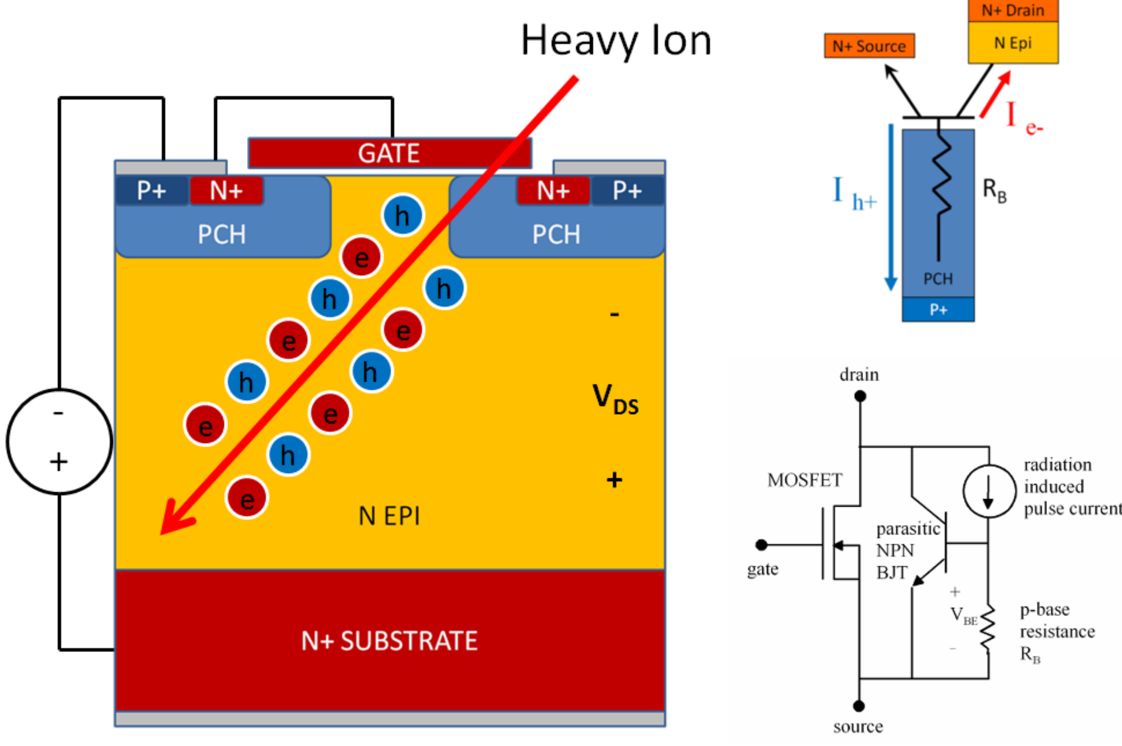
collector to the N+ substrate / drain. Hole current is swept into the P-Base, to be collected at the P+ source contact. Hole current must flow through the distributed resistance of the P-Base, R_B, which causes a voltage drop V_{BE} between the P-Base and the N+ source / emitter. Since the base / collector p-n junction already reverse biased, all that is required to initiate forward active BJT operation is for a sufficient voltage drop across R_B to forward bias the base / emitter p-n junction. But activation of the parasitic NPN is not enough in and of itself to cause SEB. The activation of the parasitic NPN is only the first step which sets off a more complicated series of events in the transient process of SEB. In fact, it is entirely possible that SEB might not occur, even though the NPN is temporarily activated.

Physical Mechanisms of Single Event Burnout

In order to understand the deeper physical mechanisms of SEB, it is first necessary to explain what happens when a reverse biased p-n junction is penetrated by a heavy ion. In the case of a power MOSFET, the reverse biased p-n junction is between the P-Channel (base) and N Epi (collector). Recall the basic one-dimensional case of a one-sided p-n junction. This is a good approximation of the P-Channel / N Epi junction in a power MOSFET. When such a p-n junction is reverse biased, the electric field spreads away from the junction as the charge in the semiconductor around the junction is depleted. As more voltage is applied to the junction, the depletion region spreads further

and further to deplete a correspondingly larger amount of charge. Meanwhile, even though the depletion region is expanding to accommodate the increase in voltage, the magnitude of the peak electric field at the junction does not necessarily remain constant. The field at the junction increases as more voltage is applied. Eventually, if the voltage is fixed at a constant level, the depletion region will cease expanding, and the balanced charge on each side of the junction will sustain the depletion region, thereby preventing the flow of current. If the voltage does not remain fixed, but instead keeps increasing, eventually the electric field at the junction will reach the critical electric field of the semiconductor, resulting in high levels of impact ionization. In this case, the depletion region becomes flooded with charge and the device conducts large amounts of current.

Understanding the mechanisms of how the depletion region forms and can subsequently collapses due to impact ionization is critical in understanding the physical mechanisms of single event burnout. Before SEB occurs, the externally applied V_{DS} bias of the power MOSFET is sustained across the depleted N-Epi region, and the blocking junction occurs between the N Epi and P-Base. In this case, the electric field across the depleted N-Epi is more or less uniform, whereas a slightly higher electric field exists at the blocking junction.



Holes and electrons deposited by the heavy ion are collected at the P+ source and N+ drain of the MOSFET respectively, which make up the base and collector of the parasitic NPN BJT. Hole current flows through the distributed resistance of the P-Base, causing a voltage drop between the base and emitter of the parasitic NPN. Sufficient voltage between the base and emitter cause the parasitic NPN to enter forward active operation, acting as a current amplifier. This is the first step in a domino effect which results in SEB.

Figure 11. Planar VDMOS and Heavy Ion Charge Collection

Figure 12 shows the simplified time evolution of charge transport and generation which leads to single event burnout. When heavy ion traverses a p-n junction in the blocking state, the depletion region along the ion shunt is flooded with deposited charge. The deposited charge is represented by the electron and hole current sources in figure 12a, with a dashed line representing the depletion region. Where deposited charge is

present, current is able to flow, and the ion shunt is highly conductive due to the high density of deposited mobile carriers. The resulting flow of hole and electron current is shown in the blue and red arrows respectively, in both the device cross section and the adjacent NPB BJT diagram.

Where the depletion region in the N epi was one comprised of fixed ions with no mobile charge carriers, that region is now full of mobile electron-hole pairs deposited by the heavy ion. This means that the depletion region which existed around the ion shunt is no longer able to sustain the voltage which continues to be applied externally across the p-n junction.

In order to sustain the externally applied voltage in the presence of the deposited charge, the depletion region must expand. Depending on the concentration of deposited charge and the size of the remaining undepleted N epi, there may or may not be enough lightly doped epi to accommodate the expanding depletion region. In this case, the depletion region will attempt to expand beyond the boundaries of the epi region and into the more highly doped P-Channel and N+ substrate regions. Since these highly doped regions cannot be depleted without exceeding the critical electric field in silicon, high levels of impact ionization begin to occur [29]. This expansion of the depletion region and resulting impact ionization is represented in figure 12b. Note that the current sources in the figure insert in 12b are due to impact ionization, not ion deposited charge.

Whereas the ion's deposited charge was sufficient to overwhelm the depletion region and create impact ionization, the generation rate of electron-hole pairs resulting from the impact ionization itself can be orders of magnitude larger than the generation

rate associated with the deposited charge. It is the high current density associated with impact ionization which leads to a resistive voltage drop across the base of the parasitic NPN which eventually forward biases the base-emitter junction. This is shown in figure 12c, where V_{BE} is now greater than 0.7 V and electrons are being injected from the N+ source / emitter. This is the point at which the fate of the device is decided. If the gain of the NPN is sufficiently low, the device may recover, even after the emitter starts injecting electrons. However, if the gain of the NPN is too high, and the biasing conditions are too stressful, the electron injection from the emitter, through the base, into the collector will cause the collector to enter a high injection regime. This means that the concentration of electrons flowing through the collector is greater than the background doping concentration of the collector. When high injection occurs, the depletion region pushes further into the N+ substrate and the levels of impact ionization there begin to rapidly increase. The hole current generated by this impact ionization is swept through the depleted collector (epi) and into the P-Base, which is now functioning as the base of the forward active BJT. This increase in base current then causes an increase in electron injection from the emitter, which is the well-known amplification effect of a textbook example NPN BJT. As more base current feeds more electron injection, the injected electrons from the emitter pass back into the collector, further feeding the impact ionization at the N+ substrate, and the entire bipolar amplification process repeats itself [7][30]. This is the self-sustaining bipolar operating mode, shown in figure 12d, which results in single event burnout.

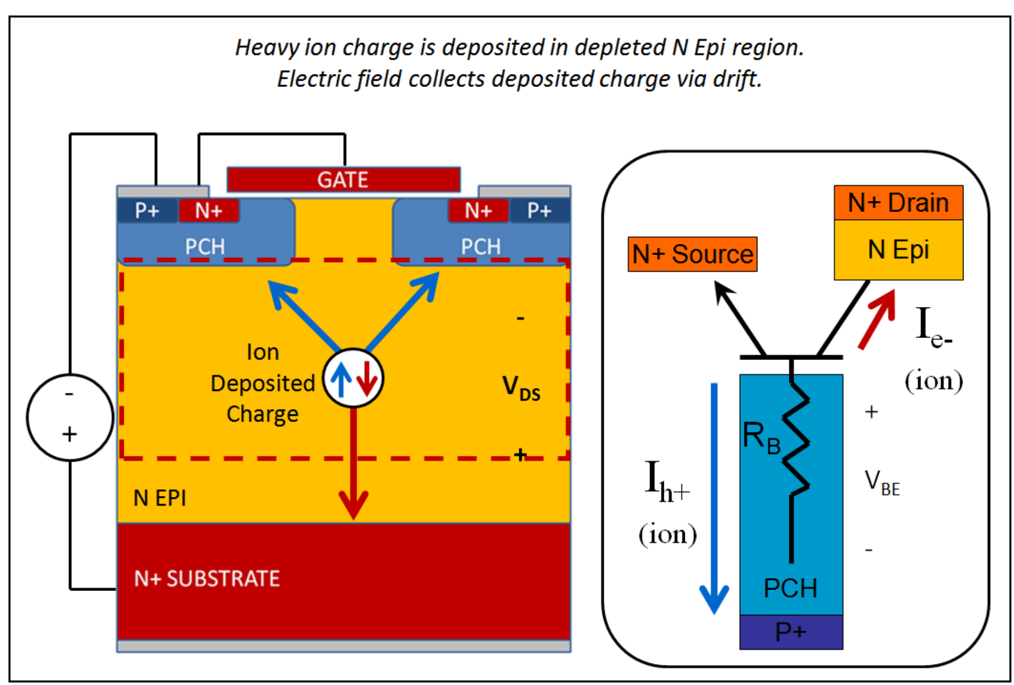


Figure 12a: Heavy Ion Charge Deposition

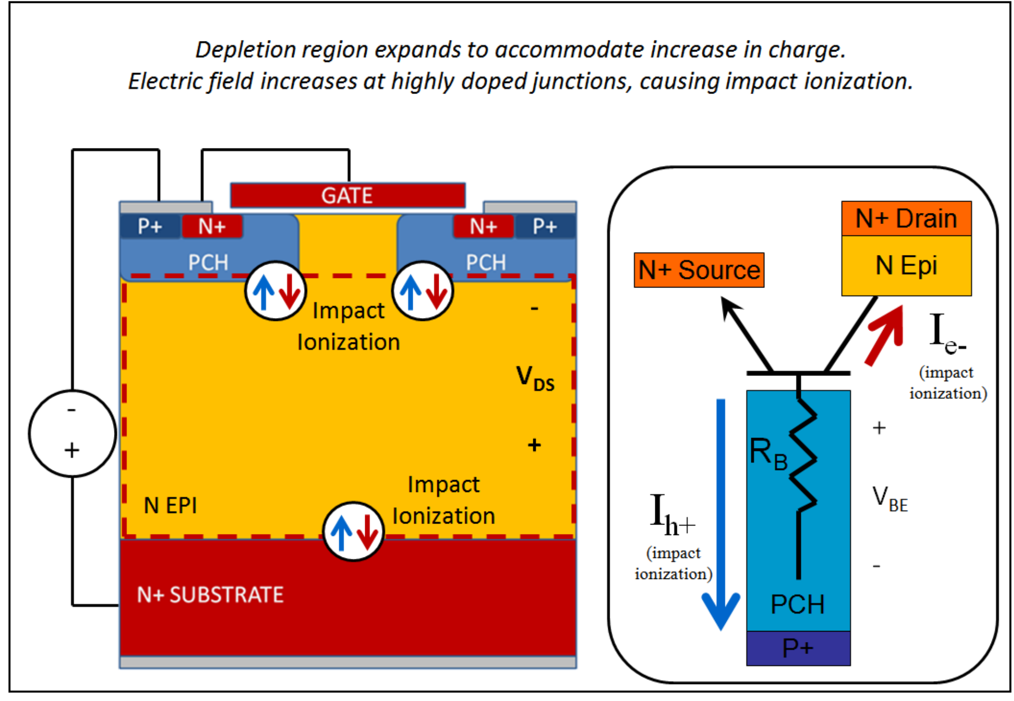


Figure 12b: Impact Ionization Caused by Expansion of Depletion Region

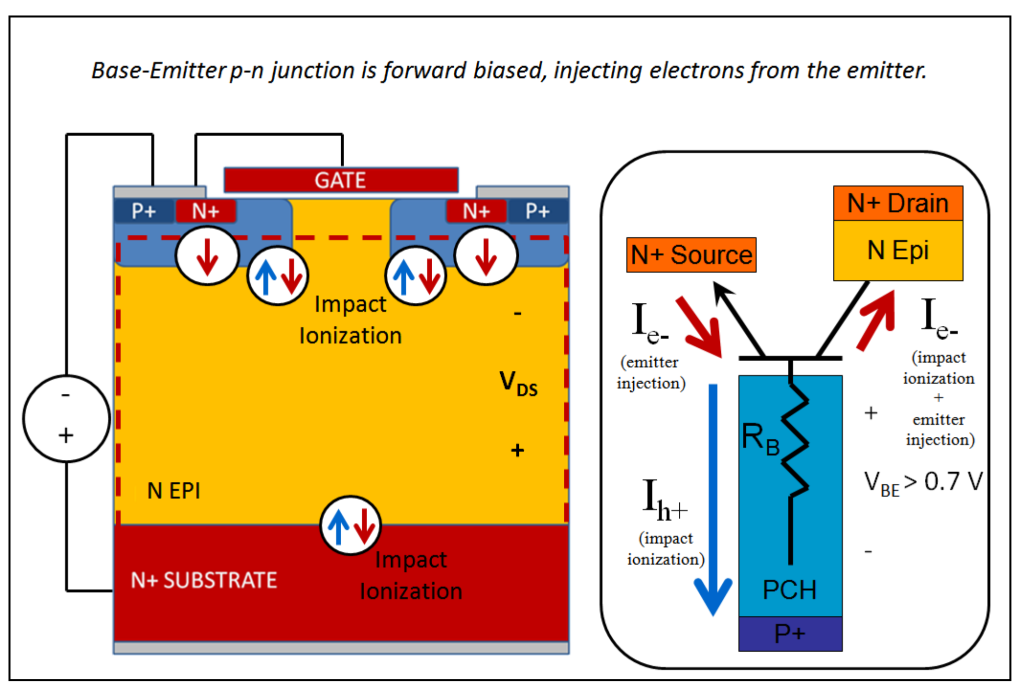


Figure 12c: Activation of Parasitic NPN BJT

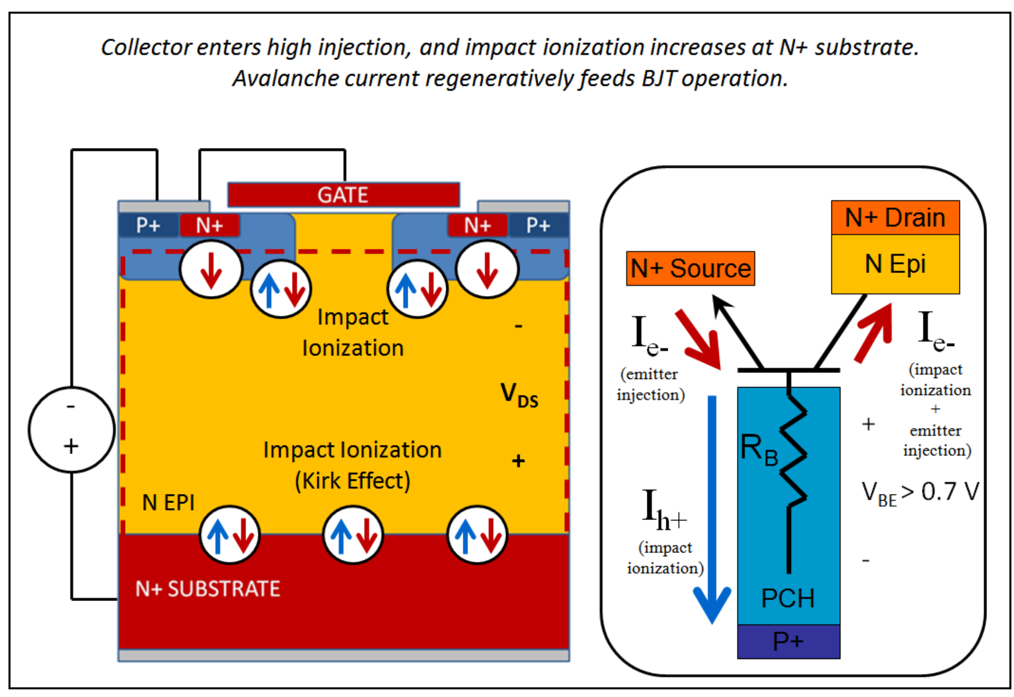


Figure 12d: High Injection and Self-Sustained Bipolar Current Amplification

Figure 12: Time Evolution of Single Event Burnout in Planar VDMOS

Hardening Against SEB in Vertical Power MOSFETs

Table 2 outlines some of the design considerations which most affect the single event burnout safe operating area (SOA) of a power MOSFET. SOA is a term used to describe the upper bounds of the operating voltages or currents under which a device may be operated without causing damaging or destructive effects. The SEB safe operating are of power MOSFETs is generally described in terms of LET vs. V_{DS}. Before such design methods were implemented, SEB was a major limiting factor in the reliability of power MOFSETs. By contrast, the SEB SOA of modern rad-hard power MOSFETs is generally very good, with some devices being theoretically immune to the effect. Today, SEB is not so much of a concern as SEGR, which remains the limiting factor in determining the device's overall SEE safe operating area.

Table 2: Design Considerations for Improving SEB Safe Operating Area

Design Consideration	Impact on SEB Resistance	Potential Impact on Device Performance
Decrease P-Base Resistance	Reduce Bipolar Current Gain	Negligible
Increase P-Base Length	Reduce Emitter Injection Efficiency	Increased $R_{DSON;}$ Decreased g_m
Decrease Base Minority Carrier Lifetime	Reduce Emitter Injection Efficiency	Increased I_{DSS} Leakage Current; Requires Exotic Processing Methods
Decrease N+ Source Doping Concentration	Reduce Emitter Injection Efficiency	Increased R_{DSON}
Increase N Epi Thickness	Increase Avalanche Voltage	Increased $R_{DSON,}$ Q_{RR}
Include Highly Doped N Epi Drain Buffer Layer	Resistance to High Injection	Increased R_{DSON}

Single Event Gate Rupture in Planar VDMOS

Single event gate rupture (SEGR) refers to a destructive single event effect which occurs after a power MOSFET gate oxide has been penetrated by a heavy ion. Today, SEGR is still a major concern when operating power MOSFETs exposed to heavy ion radiation. There are several reasons for this. First, the real-world SEGR safe operating area of a power MOSFET is not easy to determine. The fundamental physical mechanisms which cause SEGR are difficult to simulate in a way which is both reliable and practical for power MOSFET designers. Even more important, the SEGR response of a power MOSFET is very difficult to determine even when performing real-world heavy ion testing. The SEGR SOA is dependent on many factors, which complicates efforts to reliably test or simulate the response. These factors include but are perhaps not limited to V_{DS}, V_{GS}, gate oxide thickness, ion trajectory, ion energy, epi thickness, and device design and doping profiles.

Earlier works in developing mathematical formulae for predicting SEGR were very helpful in providing guidelines for device designers [31]. The first formula describes what is commonly referred to as the capacitor response of a MOS capacitor, and is shown in equation 4.

$$V_{GS} = \frac{(E_{OX_BR})(T_{OX})}{(1+\frac{LET}{53})} \qquad (4)$$

, where T_{OX} is the oxide thickness and E_{OX_BR} is the natural critical electric field of the oxide, usually assumed to be 10 MeV/cm. This equation was found to be a fairly accurate empirical fit of the actual SEGR voltage of simple MOS capacitor structures, but it does not help predict the SEGR sensitivities of more complex devices, such as power MOSFETs, in which biases are applied at three or more terminals. Later, the same authors expanded their work to develop a so-called drain coupling factor, which was then appended to the original equation. The drain coupling factor was also an empirical fit, taken from a wealth of SEGR test data on planar VDMOS power devices. The complete equation, along with the drain coupling factor, is shown in equation 5, which is sometimes called the Titus-Wheatley approximation, after two of the authors who developed the equation.

$$V_{GS} = (0.84)(1 - e^{\frac{-LET}{17}})(V_{DS})\frac{(E_{OX_BR})(T_{OX})}{(1 + \frac{LET}{53})} \qquad (5)$$

The drain coupling coefficients attempt to simulate what is commonly termed the "substrate response" of the MOSFET, which is a way of describing how the electric field in the depleted MOSFET drift region enhances the electrical stress across the gate oxide during the heavy ion event. These terms were all fits to a wealth of empirical data from heavy ions striking normal to the silicon surface of planar VDMOS devices. Later test data consistently found that an ion strike normal to the silicon surface is the worst case

strike angle for planar VDMOS, implying that the vertical direction of the electric field in the depletion region played a strong role in determining the SEGR response [32].

Later work focused on developing a more comprehensive understanding of the substrate response, taking into account not just peak LET and V_{DS}, but also ion energy and the power MOSFET device structure [33][34]. This includes studies of ions with similar peak LET but different penetration depths. It was found that the substrate response was highly dependent on the average amount of energy deposited in the depleted epitaxial layer by the ion, not just the ion's peak LET. This had strong implications towards methods of conducting radiation hardness assurance testing of power MOSFETs. If the SEGR response of the MOSFET depends on the energy deposited in the epitaxial layer, then the safe operating area could no longer be defined simply by V_{GS}, V_{DS}, and LET. For a given LET, deeper penetrating ions would have to be used to test higher voltage MOSFETs with correspondingly deeper epitaxial layers. Similarly, lower energy ions, which deposit their energy in a shallower region, would have to be used for lower voltage MOSFETs. This meant in some cases that different power MOSFETs would have to be tested at different radiation testing facilities, since each facility only offers a limited selection of ion beams.

Recent test results illustrate how the substrate response greatly influences the SEGR threshold of modern power MOSFETs [15][16]. These works presented test data on six different planar VDMOS devices with breakdown voltage ratings spanning the range between 100 V and 600 V. In the typical case, the minimum SEGR threshold voltage was around 20% of the rated V_{DS} for the MOSFET. In [16], each device was

tested using ions of similar LET but different penetration depth, and the results clearly showed that SEGR occurred at much lower V_{DS} for ions whose penetration depth fell between the middle of the epitaxial region and the bottom of the epitaxial region near the N+ substrate. Ions that penetrated the epitaxial region and deposited most of their energy within the N+ substrate caused SEGR at much higher voltages, at or near the rated V_{DS} of the MOSFET. Similarly, ions that deposited the majority of their energy near the surface of the epitaxial region allowed for a much higher V_{DS}.

The strong interaction between the design of the power MOSFET epitaxial structure and the vertical energy deposition profile of the ion demonstrates the inherent weakness of the vertical power MOSFET structure with respect to SEGR. Despite hardening efforts, such as the inclusion of heavily doped source ties extending under the channel, and the elimination of extraneous gate areas in the neck region, modern planar VDMOS devices still demonstrate an unacceptably poor SEGR safe operating area. For a wide range of ion strike trajectories, there is a high likelihood of the heavy ion creating a conductive shunt between the poly gate and a zone of high potential in the epitaxial region – the conditions which lead to SEGR. This is because the poly gate and the epitaxial drain region lie in perpendicular planes with respect to each other. Later in this work, it will be shown how the lateral power MOSFET structure may offer an inherently improved SEGR safe operating area, due to the positioning of the poly gate and the drain region along the same plane.

CHAPTER THREE: MODELING AND DESIGN METHODOLOGY

Device modeling and design was conducted using the Sentaurus TCAD (technology computer aided design) software tools. TCAD tools allow for simulation of microelectronic device fabrication and device operation using a wide variety of physical models. More detailed discussion of critical design and process parameters related to each specific power MOSFET are contained in later chapters.

Overview of Design Methodology

The design process begins with creating rough models of the device, using manually-defined device structures and doping profiles. In this way, several design iterations can be quickly simulated without the time consuming process of performing a full physics-based fabrication simulation. The device boundary is defined using a pre-defined materials database, which includes physical constants for materials relevant to semiconductor device fabrication. Doping profiles in this type of rough model are user-defined analytical distributions, usually a Gaussian distribution, emanating from user-specified spatial coordinates. These doping profiles include variables such as doping species, doping concentration, junction depth, and lateral diffusion coefficient. This type of distribution mimics the thermal diffusion of dopants during a real world fabrication

process and allows for the creation of a reasonably realistic device structure with smooth grading of doping concentration near the p-n junctions.

The Sentaurus Device software was used to simulate the electrical operation of the device structure. These simulations include the extraction of critical DC parametrics including drain to source breakdown voltage (BV_{DSS}), gate to source threshold voltage (V_{TH}), and drain to source specific on-resistance (R_{DSON}). After the desired device structure and DC operation is achieved, transient simulations were performed using the built-in heavy ion radiation model, which is detailed in the next section. Once the transistor cell design is fixed using this rough modeling method, the next stage in the design process is to develop a real world process flow and mask layout in order to fabricate the device.

Fabrication process simulations were conducted with Sentaurus Process, which is a physics-based semiconductor device fabrication process simulator. In these simulations, real world device fabrication conditions are specified, including mask dimensions, photoresist polarity, ion implant conditions, thin film deposition and etching, and thermal processes such as furnace anneals and thermal oxidation. The devices in this work were fabricated at two different 0.35 μm CMOS foundries. Some process conditions, especially those related to thermal oxidation and also furnace ramp-up and ramp-down rates, were pre-defined by the wafer foundry, however the majority of the fabrication processes were heavily modified from the foundries' standard CMOS processes, in order to achieve the desired power MOSFET structure. These structures were then again used an inputs to the Sentaurus Device simulator, for the extraction of

DC parametrics and evaluation of SEE performance. In this way, the physics-based process simulations were used to define a fabrication process design space for each device.

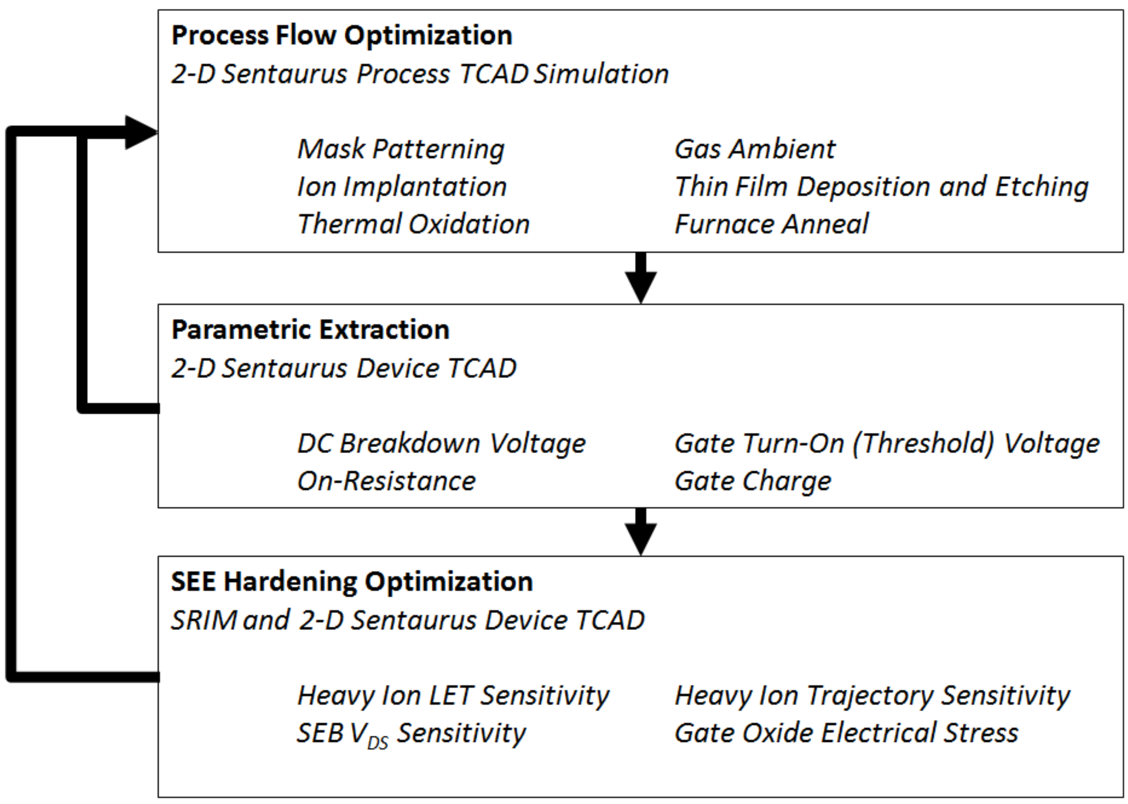


Figure 13: Power MOSFET Modeling Workflow

It is unrealistic to experimentally explore every possible set of fabrication process variables, so a subset of critical process flow variables had to be identified, while the majority of the fabrication process remained fixed. There is a potential for complex interactions between process conditions, so defining the fixed versus variable process

conditions requires careful consideration of the potential secondary effects of each process condition. The task of designing a radiation-hardened power device adds another layer of complexity to this fabrication process development. Often it was found that device features and process conditions which improved electrical performance did so at the expense of radiation hardness. It was also frequently the case that features which improved hardness against one type of radiation often sacrificed hardness against a different type of radiation. So, in terms of power MOSFET design considerations, there are all the tradeoffs normally associated with optimizing electrical performance, but now they interact with an additional set of tradeoffs to preserve radiation hardness.

Once the fabrication process and transistor cell design were fixed, the final design task is mask layout. As with the fabrication process, there are also special mask layout considerations for radiation hardened devices. Most of the layout considerations are related to the avoidance of parasitic leakage current paths that might develop as the device accumulates a high total ionizing dose (TID). Since TID effects are due to charge buildup in the insulating layers of the device, the leakage current paths most often associated with TID effects occur along the boundaries of oxide layers such as the gate oxide and shallow trench isolation (STI). As a general rule, any lightly doped area adjacent to an insulating material has the potential to become inverted as a result of TID effects. Leakage along STI patterns is especially a concern for integrated circuit design, where TID effects can create a parasitic bridge between normally isolated devices. There are similar concerns in the layout of power devices, since a parasitic leakage path or parasitic channel might develop between the drain and source or between a plurality of

transistor stripes. Specific layout concerns for each power MOSFET are discussed in subsequent chapters.

TCAD SEE Modeling

SEE modeling was conducted using the built-in heavy ion radiation model in Sentaurus Device. Input parameters for the heavy ion model were sometimes taken from the Stopping and Range of Ions in Matter (SRIM) computer program. The radial charge distribution along the ion track was modeled as an exponential function with a characteristic radius of 100 nm. In each 2-D simulation, an area scaling factor of 100 nm is used, consistent with the ion track characteristic radius, in order to scale the current and charge values to a reasonable order of magnitude.

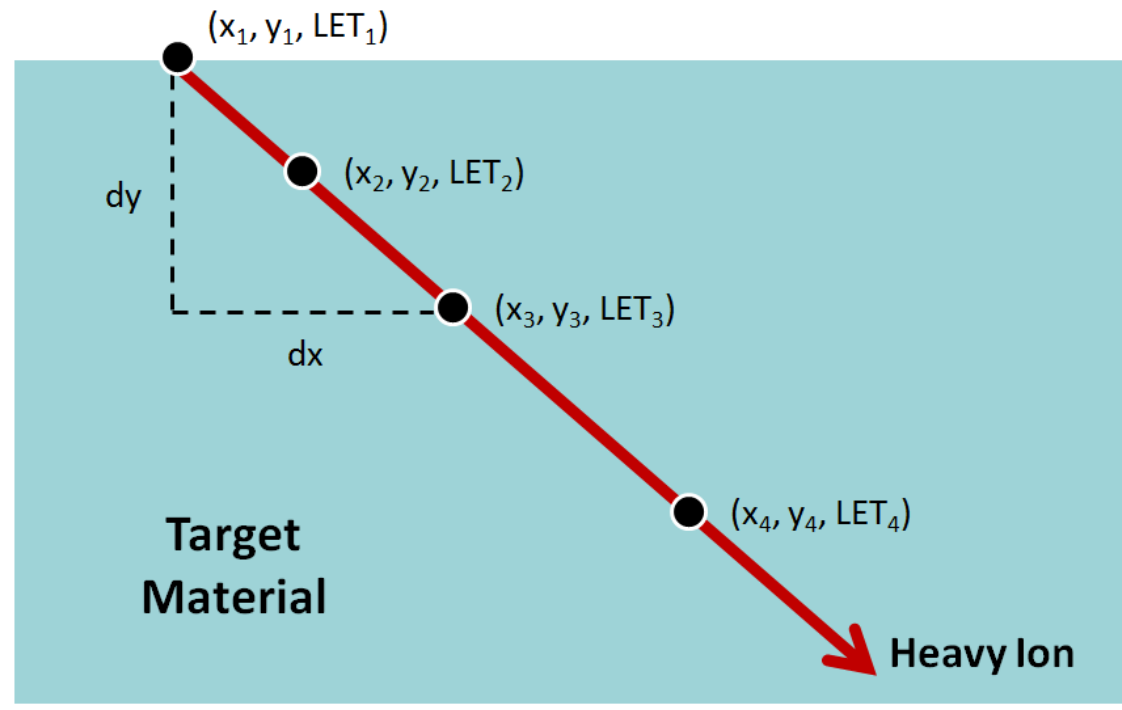


Figure 14: Representation of Heavy Ion LET and Trajectory Input from SRIM

CHAPTER FOUR: 25 V LDMOS ON P-TYPE EPITAXIAL SILICON

In order to efficiently implement a POL DC-DC converter system, low voltage power MOSFETs with low $R_{DSON} \times Q_G$ figure of merit are required. In non radiation hardened commercial applications, these needs are met by trench VDMOS and Resurf LDMOS power MOSFETs. In a rad-hard application, the requirements of low FOM is still required, however there are also the additional requirements of high TID and SEE resistance. Specifically, in the case of low power MOSFETs, a high degree of resistance to SEGR is required. SEGR resistance cannot be accomplished by simply replacing a low voltage device with a severely de-rated higher voltage device, as is commonly done with rad-hard planar VDMOS. As such, unless the low voltage power MOSFET has some inherently improved resistance to SEGR compared to the planar VDMOS, the FOM requirements for an efficient POL converter cannot be met. Since trench VDMOS are based upon a similar vertical structure as planar VDMOS, it is thought that their susceptibility to SEGR might be very similar to that of planar VDMOS. In other words, without empirical data to suggest otherwise, it is thought that trench VDMOS would have to undergo severe de-rating in order to resist SEGR.

The requirement for significant improvement in SEGR safe operating area suggests that radically different power MOSFET structures be considered. The alternative low voltage power MOSFET structure to a trench VDMOS is the lateral double diffused power MOSFET. LDMOS transistors have long been implemented in CMOS-based mixed signal integrated circuits. They are favored for use in ICs, because their lateral structure is naturally compatible with the substrates and fabrication processes

normally used to develop CMOS and BiCMOS integrated circuits. Also, the switching efficiency of LDMOS transistors has historically been much better than VDMOS transistors, due to the lower area-specific gate charge of the lateral transistor structure. One widespread use of LDMOS devices is in so-called "smart power" technology, with on-chip voltage and current regulation. Figure 15 shows a few typical LDMOS structure which might be used in low cost commercial smart power circuits.

Prior Art LDMOS Device Structures

Figure 15a is a simple N-channel LDMOS formed on a P substrate with a self-aligned LDD implant process. This means that the poly gate is patterned prior to the LDD implant, and then the relatively thick poly gate serves as the masking layer for the LDD ion implant. This means that no photolithography process is required to form the LDD region, which helps minimize fabrication costs. It also means that the overlap between the LDD and the poly gate, typically referred to as the "neck" region, is smaller than what is achievable with photolithographic patterning. This very small overlap between the poly gate and the drain results in very low Miller capacitance for this LDMOS structure. This results in very low Q_{GD}, which helps keep the overall Q_G of this device very low.

The N-channel LDMOS structure in figure 15b is similar to that of 15a, except it is formed on an N-type substrate or within an N well. In this case, the N well or N

substrate is electrically tied to the N+ drain of the MOSFET and serves as the lightly doped drain. This forms a more or less one-sided p-n junction between the LDD and the P-Channel, with the LDD region being much more lightly doped than the P-Channel. In this device structure, the P-Channel diffusion may be self-aligned to the poly gate, however the LDD is not self-aligned. The overlap between the poly gate and the LDD region instead depends heavily upon the lithographically-defined length of the poly gate and the depth of the LDD / P-Channel junction (the body diode junction), which is defined by both process and starting material. In this type of process, the factors which influence the location of the body diode junction include the background N substrate or Nwell doping concentration, the P-Channel ion implant dose and energy, the time and temperature of the processing steps following the P-Channel ion implant, the amount of boron segregation from the P-Channel implant into the gate oxide during processing, and finally the density of interface states between the gate oxide and the silicon substrate. Some of the conditions which define the spacing of the neck region can be very precisely controlled, while others such as substrate resistivity should be expected to experience more variation. Additionally, there is a limitation on what P-Channel process conditions can be used while still achieving the desired V_{TH}, g_m, and R_{DSON} specifications of the transistor. In some cases, it may not be possible to develop a reliable process which meets all device performance specifications while still achieving a very small Miller capacitance.

The N-channel LDMOS structure shown in figure 15c can be formed on either an N or P type background (well or substrate). The key feature of this device is the shallow

trench isolation (STI) oxide between the poly gate and the LDD. The purpose of this oxide is to allow the use of a more heavily doped LDD region in order to significantly reduce the drift resistance, R_D, of the MOSFET. Recall that for almost all LDMOS structures, R_D forms the most significant portion of the overall R_{DSON} of the MOSFET. Therefore, reducing R_D is a very effective way of reducing overall R_{DSON}. Normally, as the LDD doping concentration in an LDMOS is increased, the device in the OFF state will exhibit a higher magnitude electric field between the LDD and the gate. If the LDD doping concentration is made too high, the resulting high electric field between the gate and LDD will cause avalanche breakdown in the neck region. This behavior in and of itself is not desirable, because repeated avalanche stress of the device will lead to hot carrier injection (HCI) reliability issues with the gate oxide. Specifically, hot holes will be injected into the gate oxide during avalanche breakdown, and over a long period of time the accumulation of hot holes will degrade the characteristics of the device. If the LDD doping concentration is increased even further, in addition to HCI reliability issues, the avalanche breakdown in the neck region may occur at a voltage which is lower than the desired BV_{DSS} of the MOSFET. So these issues naturally cause some upper limit on the resistivity of the LDD region for a given blocking voltage.

In order to be able to dope the LDD more heavily and reduce R_D, the STI oxide is placed in the vulnerable region between the gate and drain where avalanche breakdown would normally occur in the silicon. The dielectric strength of the STI oxide is approximately 10 times higher than that of silicon, so the STI is able to sustain a very high electric field without undergoing rupture. Now, as the doping concentration of the

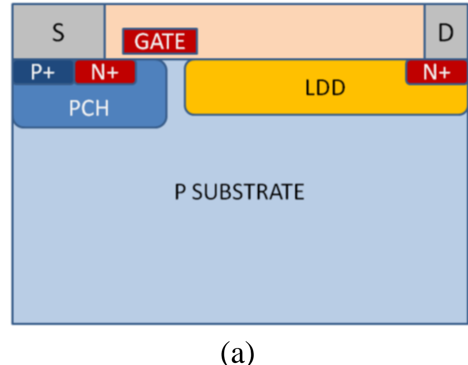
LDD region is increased, the electric field in the STI oxide gets correspondingly stronger at a given V_{DS}, but the magnitude of the electric field in the surrounding silicon remains below the critical value for silicon. This allows the device to simultaneously have a high breakdown voltage and a more heavily doped drift region. Using this design technique, the structure in figure 15c should have the lowest specific R_{DSON} of the three examples.

The drawback of using the STI structure in figure 15c is that the alignment of the poly gate, the STI, and the LDD can severely impact both R_{DSON} and Q_G and therefore imposes significant layout and process constraints on the design of the MOSFET. The first design consideration is R_{DSON}. In this design, when the device is in the ON state, the drain to source electron current must flow through the LDD region, underneath the STI oxide, and then through the neck region back up toward the silicon surface, where the current eventually finds the MOS channel. This makes the LDD regions both underneath the STI and also in the neck region potential regions of high resistance for drain to source current. These so-called "bottleneck" regions must be made sufficiently wide and heavily doped to avoid a significant increase in R_{DSON}.

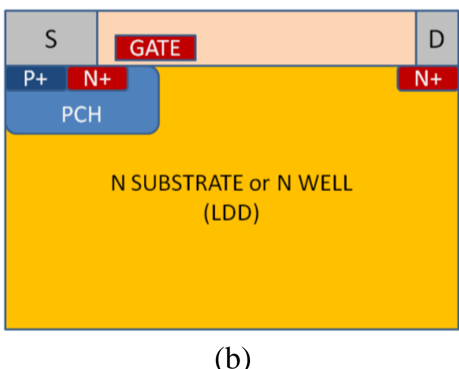
In the vertical direction, this requires balancing the LDD junction depth against the STI depth. The STI depth should be expected to have a significant process variation, so this tradeoff requires a large design margin. In the horizontal direction, the spacing of the neck region is strongly influenced by the alignment between three different mask layers, as well as the diffusion of the P-Channel implant, which can be self-aligned to the poly gate. This means that the design tolerances for defining the neck region are significantly impacted by the resolution of the photolithographic process, and the

expected misalignment between the three mask layers is on the same order of distance as the length of the poly gate itself. The result of these complex design and process dependencies is a transistor which requires a longer gate and a wider neck region than structures 15a and 15b. This means that despite having the lowest RDSON of the three structures, the STI oxide LDMOS also has the highest gate charge. Further, as this device is scaled to very low voltages, the structure of the gate and neck regions remains more or less fixed, and the drift length of the device remains limited by the space required to accommodate the STI oxide. In short, the device reaches a saturation point at which further reduction in cell pitch is not possible, and the $R_{DSON}\times Q_G$ FOM begins to increase disproportionally to the voltage rating. Finally, the other major drawback of this structure is cost. This structure requires the most photolithographic processing of the three examples, and therefore it is the costliest to fabricate.

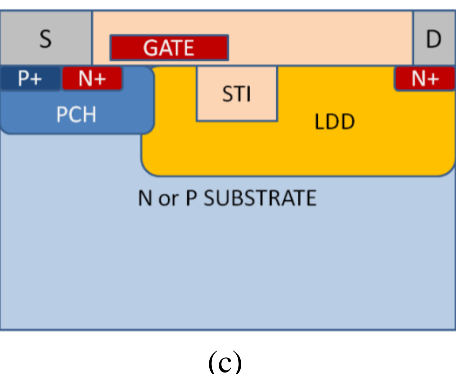
For the development of a 25 V LDMOS for MHz frequency POL converter, it was deemed that the low gate charge, specifically low Q_{GD}, of the self-aligned LDMOS on P substrate would offer the most efficient switching performance. Also, this LDMOS offered the simplest process flow and highest chance of success for engineering a functional device with limited process iterations. Furthermore, published literature suggested that a P substrate is the preferred starting material for rad-hard N-channel devices, due to its lower mobility, which should result in an increased percentage of radiation generated carriers being recombined in the substrate during a heavy ion strike.



(a)



(b)



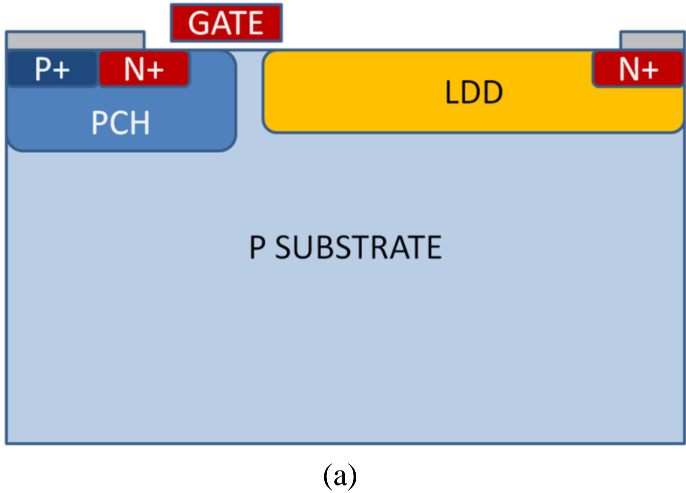
(c)

Three simplified LDMOS device structures commonly used in smart power ICs for on-chip voltage and current regulation. Each device structure is compatible with a typical CMOS or BiCMOS fabrication process flow. LDMOS fabricated on a P substrate using a self-aligned LDD implant process (a);. LDMOS fabricated on an N substrate (or in an N well), where the LDD region is not self-aligned to the poly gate (b); LDMOS fabricated on either an N or P substrate or well, with a thick STI oxide between the gate and LDD region. The LDD region and STI are not self-aligned to the poly gate (c).

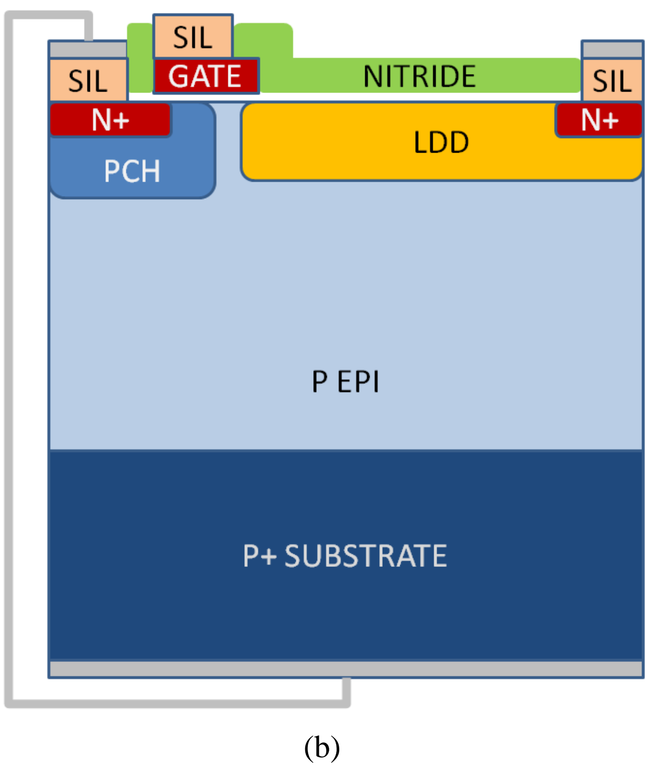
Figure 15: Prior Art LDMOS Device Structures

25 V Rad-Hard LDMOS Device Concept

Figure 16 shows a comparison of the standard LDMOS device structure on P substrate, and the proposed rad-hard LDMOS device structure on a P epitaxial layer grown on a P+ substrate. The use of a thin P epi layer on a P+ substrate is a well known technique for hardening integrated circuits against SEE. This is because the short minority carrier lifetime in the P+ substrate helps to recombine much of the deposited charge during a heavy ion strike or other similar ionizing radiation event. In effect, almost all the electrons which are deposited in the P+ substrate will recombine before reaching the sensitive junction of the device. Therefore, the collection of photocurrent is limited primarily to only the charge deposited in the more lightly doped epitaxial layer, where the minority carrier lifetime is much longer. In this situation , the epi region is often referred to as the *charge collection volume* or *sensitive volume* when discussing SEE sensitivity. By limiting the charge collection volume with a thin epi, less photocurrent is collected, which should lead to lower levels of impact ionization during a heavy ion strike. The use of this substrate is therefore the first method in hardening the device against SEB from heavy ion radiation.



(a)



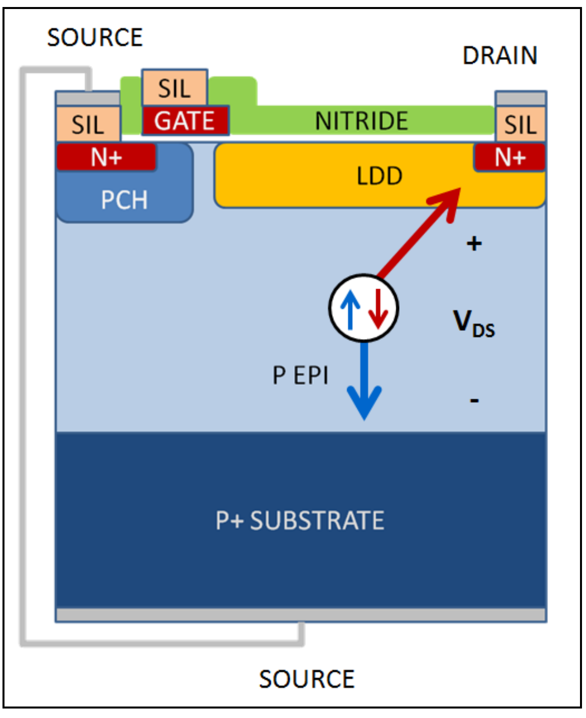
(b)

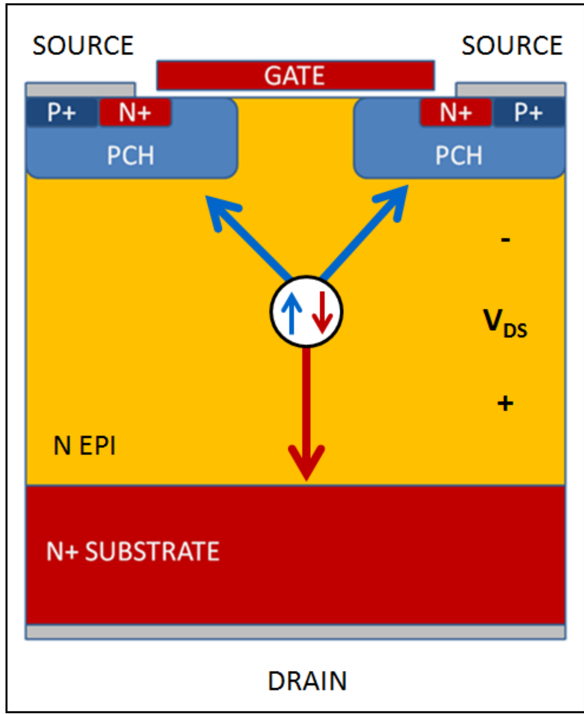
Device cross section drawingss of the standard LDMOS (a) and proposed rad-hard LDMOS (b). The rad-hard LDMOS is fabricated on a P epi silicon on top of a P+ silicon substrate. The P+ source contact is moved to the bottom of the P+ substrate, to divert photocurrent away from the sensitive base-emitter p-n junction, in hopes of avoiding activation of the parasitic NPN bipolar junction transistor.

Figure 16: Standard LDMOS and Proposed Rad-Hard LDMOS

The second method of hardening the device has to do with the suppression of the parasitic NPN bipolar junction transistor. The P+ body tie contact normally found adjacent to the N+ source in the standard LDMOS, Figure 16a, has been eliminated. Instead, a backside metallization is performed, and the P+ substrate is tied externally to the source of the MOSFET. In this way, the P+ substrate forms the base terminal of the parasitic NPN BJT. As the device is biased in the OFF state, the electric field between drain and source will cause holes to drift downward toward the P+ substrate, to be collected at the backside contact.

Because the P+ substrate is very highly doped and many orders of magnitude larger than the volume of the deposited charge, the P+ substrate presents a very low resistance path for the collection of hole current. Since the substrate offers the lowest resistance path for the collection of holes, it is thought that the vast majority of hole current will be immediately drawn into the substrate, and very little hole current will flow through the P-Channel region. This means the vast majority of the hole current will be diverted away from the N+ source p-n junction, which forms the sensitive base-emitter junction of the parasitic NPN BJT. With the hole current diverted safely away from the base-emitter junction, the voltage drop V_{BE} across that junction should remain low, and the parasitic BJT will not be pushed into forward active operating mode. Figure 17 shows an illustration of the supposed flow of photocurrent in the rad-hard LDMOS device, contrasted with the photocurrent flow in a planar VDMOS device.





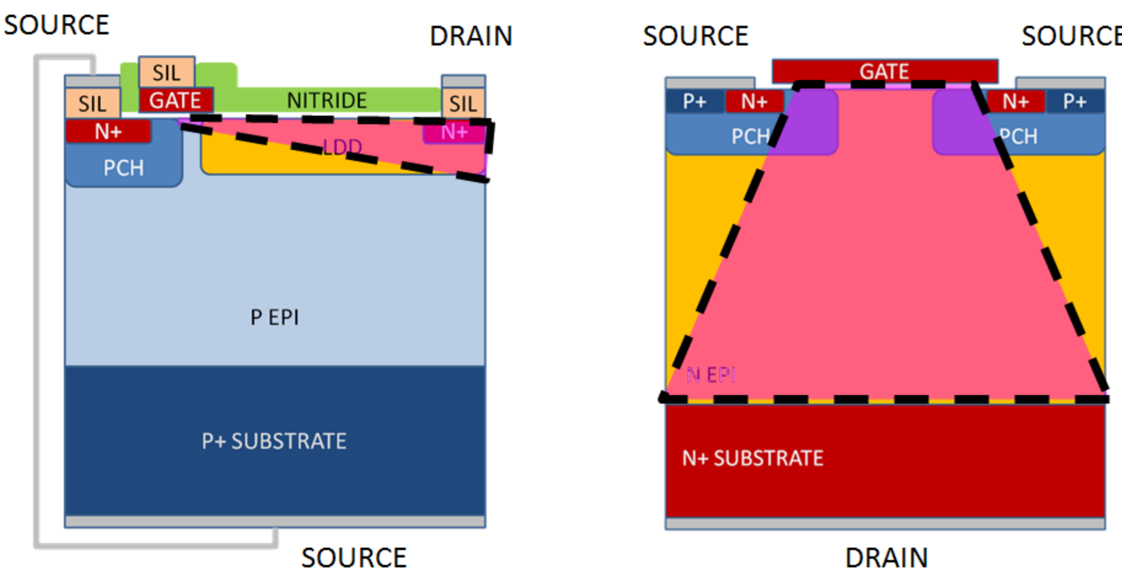
Theorized collection of deposited holes (blue) and electrons (red) in rad-hard LDMOS (top) and planar VDMOS (bottom). LDMOS hole current is diverted away from the sensitive base-emitter junction.

Figure 17: Theorized Charge Collection in Rad-Hard LDMOS and Planar VDMOS

The same diversion of hole current which is thought to provide added hardness against SEB should also improve the SEGR safe operating area of the device. One theoretical cause of SEGR in VDMOS transistors is the high transient electric field caused by accumulation of radiation-generated holes underneath the gate oxide. After being deposited by a heavy ion, holes are driven from the N epi toward the gate oxide by the vertical electric field. This accumulation of holes results in a highly localized increase in the electric field across the gate oxide, which has an additive effect with any externally-applied negative V_{GS} bias [23][35]. In the case of the proposed rad-hard LDMOS, the vertical electric field in the epi layer is pointing in the opposite direction of that in a VDMOS. Because holes are driven downward in an LDMOS, there should be no accumulation of holes near the gate oxide during a heavy ion strike. This should theoretically cause reduced transient electric field stress across the gate oxide in an LDMOS, compared to a VDMOS.

An additional improvement in SEGR SOA is expected to result from the geometry of the electric field distribution between gate, source and drain in the lateral device. As explained previously, vertical power MOSFET SEGR threshold voltages exhibit a strong dependence on the penetration depth and the vertical charge deposition profile of the heavy ion. Deeper penetrating ions which deposit their energy closer to the N Epi / N+ Substrate junction cause SEGR at lower voltages than shallower penetrating ions of the same LET [15][16]. Another way to consider this is that deeper penetrating ions deposit their charge in higher potential zones inside the depletion region. This suggests that the worst case for SEGR is when the heavy ion shunt occurs between the

gate oxide and the point of highest potential in the depletion region near the drain. Figure 18 shows cross-sectional drawings of the approximate heavy ion angles of incidence which would produce such a strong gate to drain shunt in the LDMOS and planar VDMOS devices.



The heavy ion angles of incidence subtended by the pink shaded area within the dashed lines represent trajectories theorized to be most likely to create a strong gate to drain shunt in the LDMOS (left) and planar VDMOS (right) device structures. These are thought to be the trajectories which cause the most sensitivity to SEGR in each power MOSFET. The range of supposed sensitive ion angles is much smaller in the LDMOS than the VDMOS, suggesting the LDMOS may have a statistically lower probability of exhibiting SEGR in a real-world operating environment.

Figure 18: Heavy Ion Trajectories Shunting Gate to Drain

If the shunting effect between gate and drain is indeed the mechanism which most affects the SEGR safe operating area of the device, then the LDMOS should be less

vulnerable to SEGR at most angles of incidence, with the exception being a grazing strike along the surface of the LDMOS device. In contrast, a grazing strike along the surface of the VDMOS is known to cause the *least* SEGR sensitivity, and the worst case strike angle is known to be one perfectly normal to the silicon surface. So in terms of SEGR angular sensitivity, the lateral and vertical devices should be completely opposite of one another. It is also possible, due to the lateral orientation of the electric field between the LDMOS gate and drain, the lateral component of the transient electric field stress across the gate oxide will be stronger than the vertical component. Given the almost wild nature in which the electric field is redistributed during a heavy ion strike, it is unknown if this would actually be the case. However, if this is the case, then the overall magnitude of the transient electric field across the thin vertical dimension of the gate oxide would be further reduced in an LDMOS, even in the case of a direct gate to drain shunt.

In summary, it is theorized that the proposed rad-hard LDMOS structure will provide the required electrical performance for low voltage MHz frequency power switching applications. It is also thought that the lateral device structure on P+ substrate could offer inherently improved SEB and SEGR performance compared to existing rad-hard planar VDMOS device geometries. Such improved SEE hardness would reduce the need for performance-degrading electrical de-rating commonly necessary for VDMOS power transistors. Furthermore, excellent TID hardness is expected to result by basing the LDMOS fabrication process on a slightly modified version of a known TID-hard CMOS fabrication process at Sandia National Laboratories.

Design Considerations

Figure 19 is a cross sectional drawing of the rad-hard LDMOS structure, showing the critical design dimensions for the device.

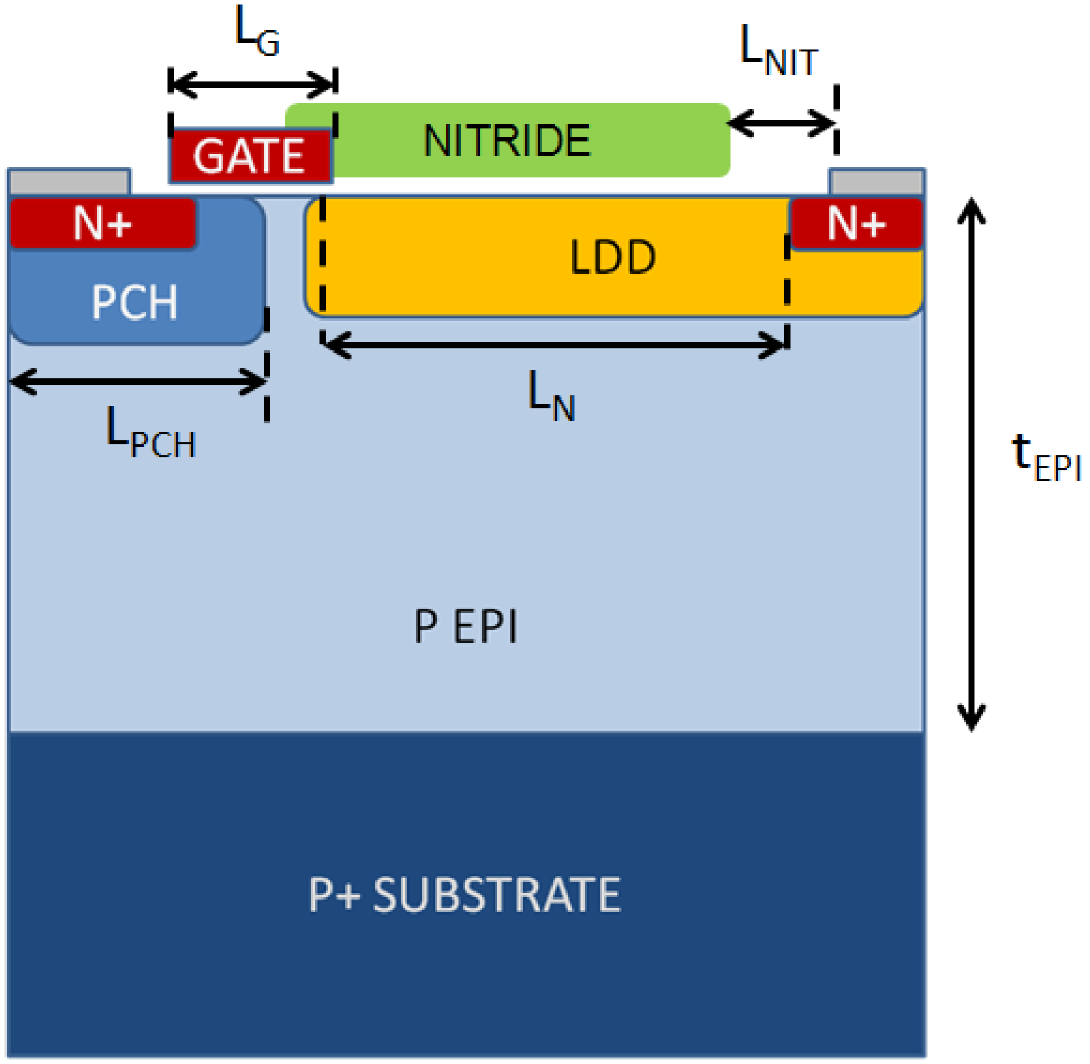


Figure 19: LDMOS Critical Design Dimensions

This device is fabricated using a silicided drain, source and gate, similar to the self-aligned silicide (salicide) process commonly used in CMOS device fabrication. In the case of the LDMOS, a masking layer is necessary to prevent formation of the silicide over the LDD region. Any silicide formed over the LDD region would short that region to the N+ drain, making it incapable of sustaining a depletion region. This would degrade the blocking voltage of the LDMOS. In order to prevent the formation of silicide over the LDD, a patterned nitride masking layer (hard mask) is formed over the LDD prior to silicidation. L_{NIT} represents the spacing between the nitride silicide blocking layer and the drain contact plug. If the nitride layer is too far from the drain contact, the silicide will encroach into the LDD region. If the nitride is placed too close to the drain contact, then it will interfere with the contact etching process, and the contact area in the drain will be smaller than desired. In the best case, this would lead to increased contact resistance, which would impact R_{DSON} and might present a reliability concern. In the worst case, it would result in the complete loss of Ohmic contact to the drain, resulting in a non-functioning device. For the most part, L_{NIT} is dictated by the resolution of the photolithography process.

L_N represents the drift length of the device and is defined as the lateral spacing between the poly gate and the N+ drain diffusion. This is essentially the portion of the LDD region which is capable of being depleted when the device is in the OFF state. It is also the length that defines R_D, or drift resistance, which is the largest component of R_{DSON} in an LDMOS device of this voltage rating. Note that for lower voltage LDMOS, as L_N becomes smaller, the drift resistance and channel resistance eventually become

equal to each other, and at very low voltages, the channel resistance can actually be higher than the drift resistance. So, in terms of its impact on electrical performance, L_N controls the tradeoff between BV_{DSS} and R_{DSON}. Both more or less exhibit a direct linear proportionality to L_N.

L_G is the gate length of the device, the lower bound of which is defined by the limits of the photolithographic process. L_G influences a number of electrical characteristics, including R_{DSON}, Q_G, and g_m. L_G also affects the gain of the parasitic NPN bipolar transistor, which is formed at the device surface between the LDD and the N+ source, however this was not considered during the first design iteration. This effect will be discussed in more detail during the later discussion of experimental results.

L_{PCH} determines the overlap of the P-Channel region and the poly gate. Since this design does not rely on the P-Channel region to conduct avalanche hole current, the primary purposes of the P-Channel are to control V_{TH} and prevent drain to source punch through when the device is in the OFF state. Aside from affecting these parametrics, a longer L_{PCH} will also result in higher channel resistance, which in turn leads to higher overall R_{DSON}.

Finally, t_{epi} refers to the thickness of the lightly doped epi layer. Epi thickness can affect both BV_{DSS} and SEE performance. If the epi is made too thin, then BV_{DSS} will be limited vertically between the N+ drain and the highly doped P+ substrate. However, if the epi is too thick, then SEE hardness will suffer, due to the thicker epi providing a larger charge collection volume.

Table 3 shows a simplified version of the simulated LDMOS process flow, which was used to define the process design space for meeting the required electrical specifications. The design goals for this device are BV_{DSS} > 25 V and 1.5 V < V_{TH} < 3.5 V.

A series of process and device simulations were performed prior to designing a test element group mask set for fabrication. These simulations served to explore the design space of both the transistor geometry and fabrication process conditions. The results of these simulations are presented in figures 20 – 28.

Table 3: Simulated 25 V LDMOS Fabrication Process

Step	Name	Description
1	Initialization	Low resistivity <100> p+ silicon substrate
2	Epitaxy	Lightly doped p- epitaxial layer Thickness must support vertical component of electric field for device in OFF state.
3	P-Body Implant	Low energy boron implant patterned in the source side of the MOSFET Prevents punch through from LDD to N+ source. Strongly influences V_{TH}
4	P-Body Drive	Controls P-Body implant junction depth and lateral diffusion. Strongly influences V_{TH}
5	Gate Oxidation	Thermal oxidation time, temperature and ambient are adjusted to produce desired oxide thickness Strongly influences V_{TH}, g_m, and SEGR
6	Polysilicon Deposition	Polysilicon doping affects work function difference of MOS capacitor
7	Gate Stack Etch	Patterning of poly gate
8	LDD Implant	Low energy phosphorus implant self-aligned to the poly gate Strongly influences BV_{DSS} and R_{DSON}
9	N+ Implant	Patterned low energy arsenic implant to form Ohmic contact regions for source and drain
10	Source-Drain Anneal	Furnace Anneal
11	ILD Deposition and Etch	Deposited oxide and contact window etch
12	Finalization	Write completed structure to compatible file format for device simulation

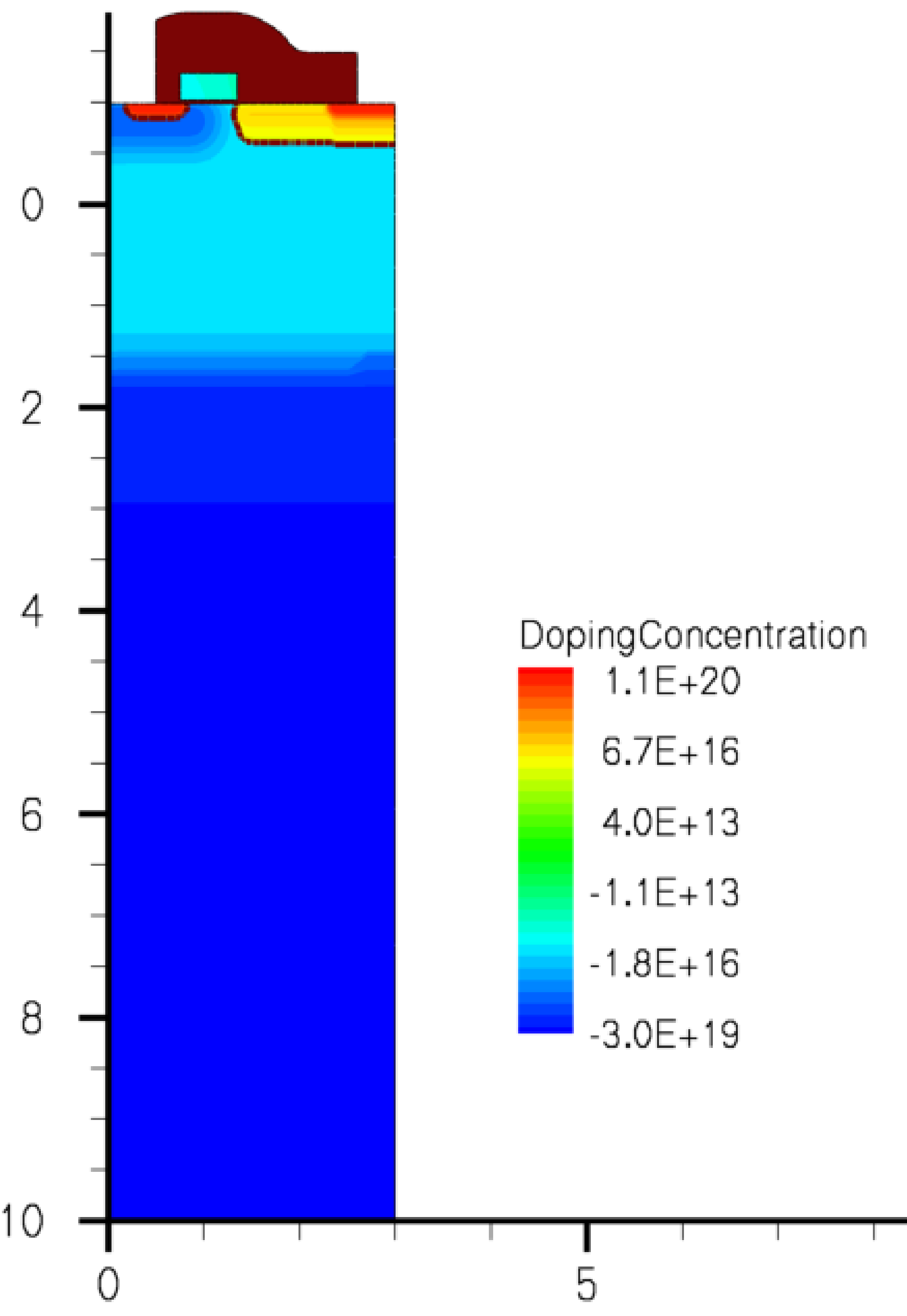


Figure 20: Simulated 25 V LDMOS Structure

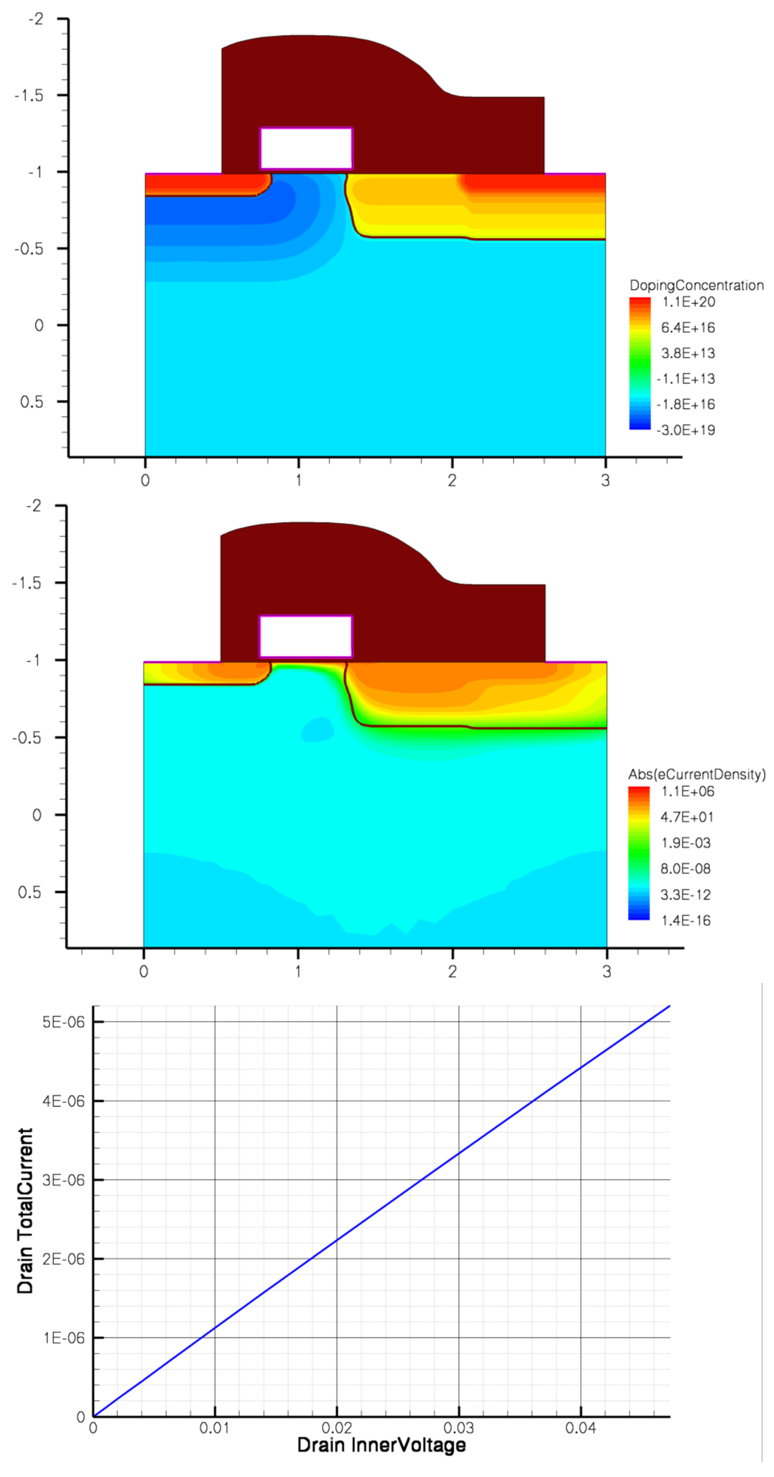
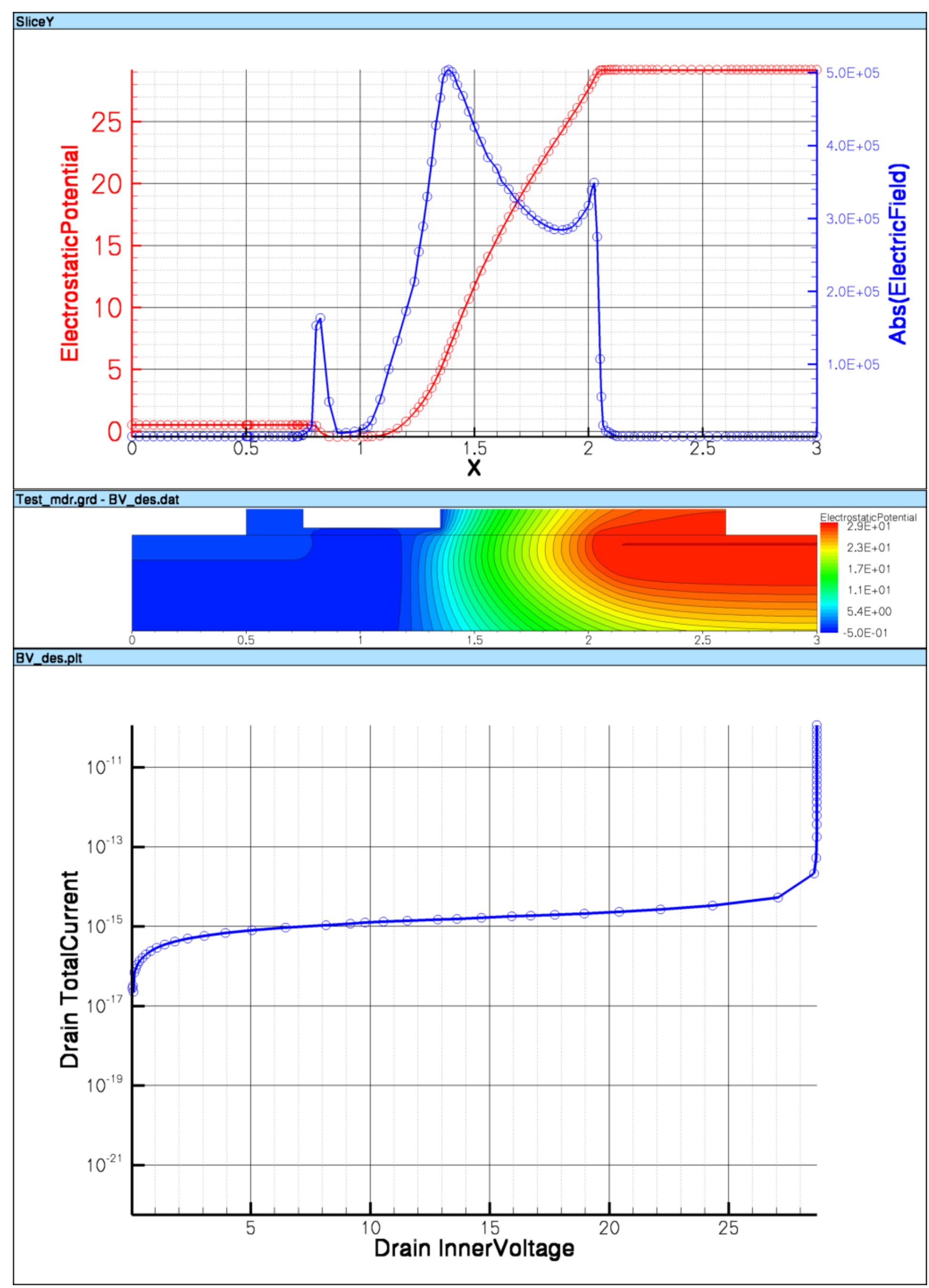


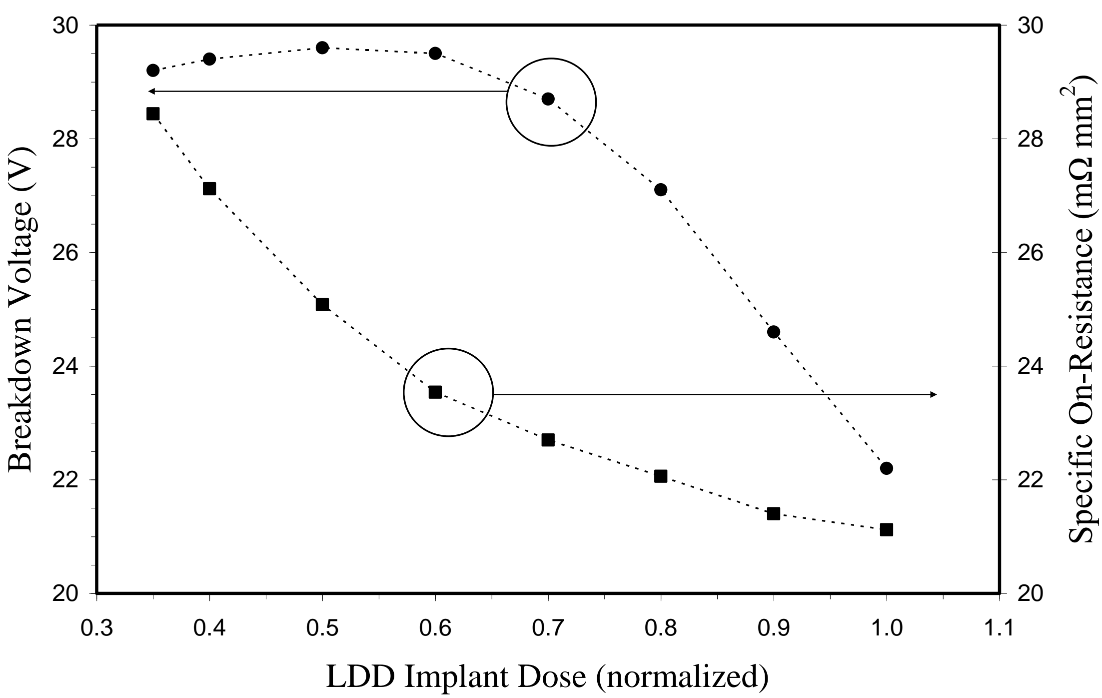
Figure 21: Simulated 25 V LDMOS ON-State Operation



The top plot shows electrostatic potential (red) and electric field (blue) along a slice taken in the lateral direction along the silicon surface. The middle plot shows potential lines in the device cross section near the surface. In this simulation, the device supports a BV_{DSS} of 29 V (bottom plot).

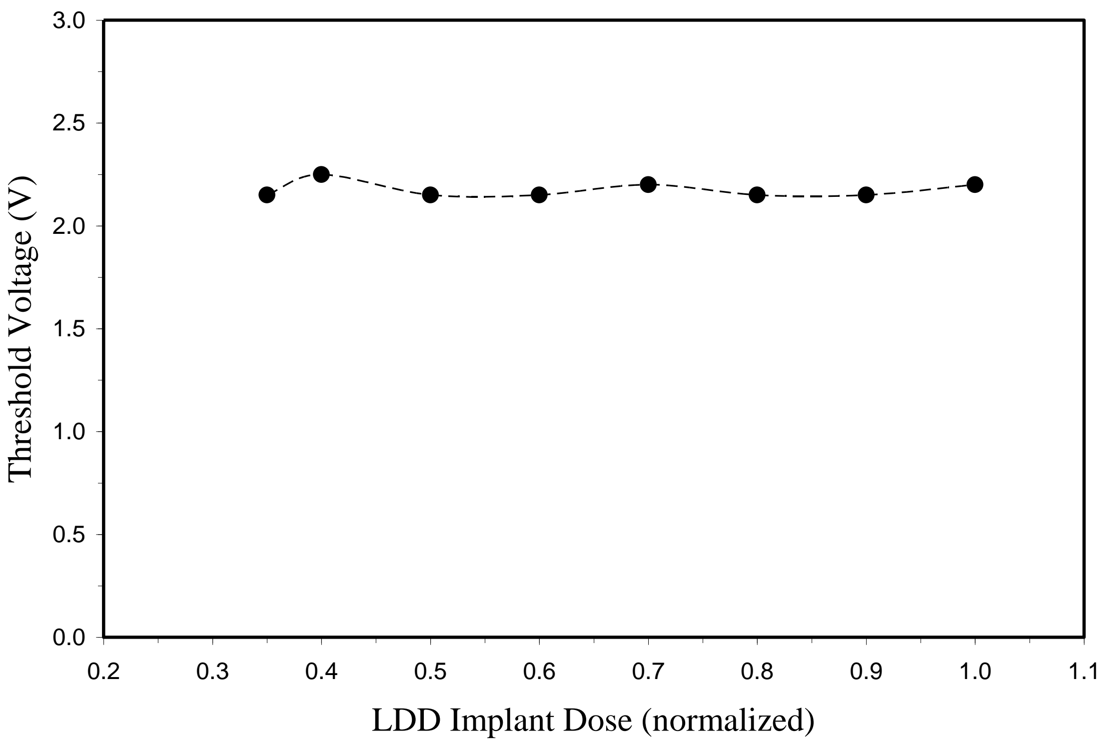
Figure 22: Simulated 25 V LDMOS Surface Potential and Electric Field

The results of the device simulations on the resulting structures are presented in the following set of figures. The first set of simulations varied the LDD Implant dose while other parameters were kept constant. Figure 23 illustrates the primary tradeoff related to LDD implant dose, which is BV_{DSS} vs. R_{DSON}. A heavier LDD implant dose will always reduce R_D, which in turn reduces R_{DSON}. However, beyond an optimal LDD dose, the reduction in R_{DSON} is accompanied by a reduction in BV_{DSS}. Figure 24 shows that V_{TH}, unsurprisingly, is not affected by changes in LDD dose.



The primary design tradeoff related to LDD implant dose is BVDSS vs. RDSON. BV_{DSS} remains high for low implant doses, because the LDD region can be fully depleted without before creating a high electric field. In the cases of low LDD doses, BV_{DSS} is dictated by the drift length (distance between the N+ drain and the poly gate). When the LDD dose is increased beyond a certain point, the electric field builds up at the gate and causes avalanche before the drift region becomes depleted, resulting in decreased BV_{DSS}.

Figure 23: Simulated LDD Implant Dose versus BV_{DSS} and R_{DSON}



Threshold voltage is determined primarily by the P-Channel implant and gate oxide thickness. Variations in LDD implant dose have no effect on V_{TH}.

Figure 24: Simulated LDD Implant Dose versus Threshold Voltage

The next set of simulations varied the p-body implant dose while keeping other design parameters constant. The primary design tradeoff related to the p-body implant dose is R_{DSON} vs V_{TH}, shown in figure 25. The increased on-resistance occurs because a weaker inversion layer forms in a more highly doped p-type region for a given gate bias, meaning that a given gate voltage creates a less conductive channel. The increase in threshold voltage simply shows that a higher gate bias is necessary to invert a more heavily doped channel. The purpose of simulating this effect is to determine what dose is necessary to achieve a threshold voltage closest to 2.5 V, as dictated by the design

specifications. The effect of the p-body implant dose on BV_{DSS} should be negligible, as shown in figure 26, long as the p-body concentration is heavy enough to prevent punch through between the drain and source.

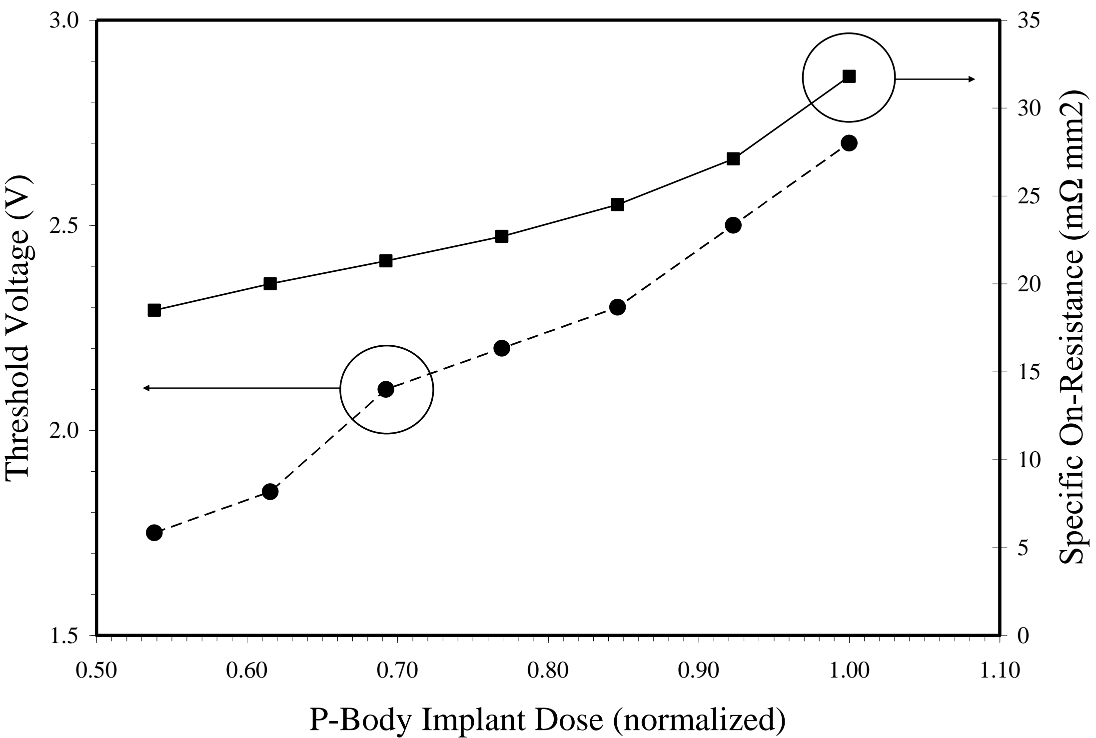


Figure 25: Simulated P-Body Implant Dose versus V_{TH} and R_{DSON}

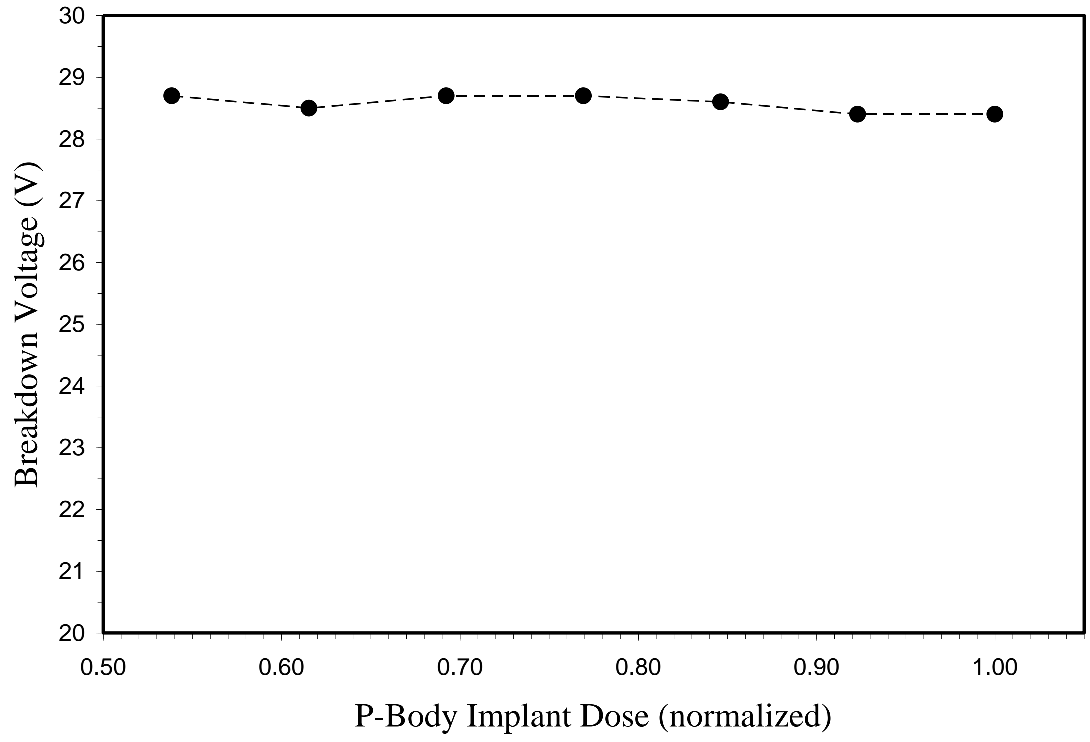


Figure 26: Simulated P-Body Implant Dose versus BV_{DSS}

The final set of simulations show the effect of the lateral diffusion of the P-Channel implant. Figure 27 shows that the overlap between the poly gate and the P-Channel diffusion must remain within a narrow range to prevent an adverse effect on BV_{DSS}. If the P-Channel is formed too close to the LDD, then a high electric field will form between the LDD and P-Channel. This results in a decrease in BV_{DSS}. On the other side of the design space, if the P-Channel implant has too small of an overlap with the poly gate, then the depletion region between the LDD and the P-Channel can extend all the way to the N+ source junction. This type of punch through behavior results in low BV_{DSS} and can also result in high I_{DSS} leakage current.

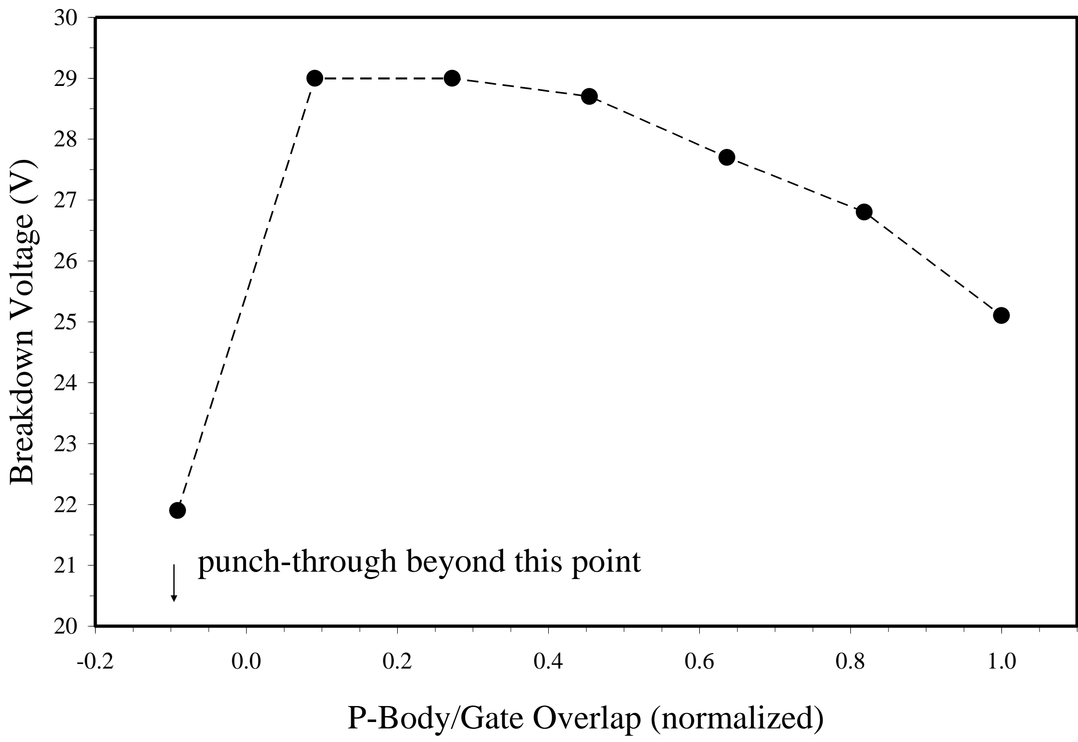


Figure 27: Simulated P-Body/Gate Overlap versus BV_{DSS}

So long as the P-Channel diffuses a sufficient distance underneath the gate to prevent punch-through, the main concern becomes the trade-off between threshold voltage and on-resistance. Figure 28 shows how increases in channel resistance can significantly increase the total specific R_{DSON} of the transistor cell.

Once a suitable design space was simulated, a test element group (TEG) mask was created. The primary variables among the TEG designs are shown in Figure 19 at the beginning of this section. The exact design values for each transistor are not authorized for public release at the time of this dissertation.

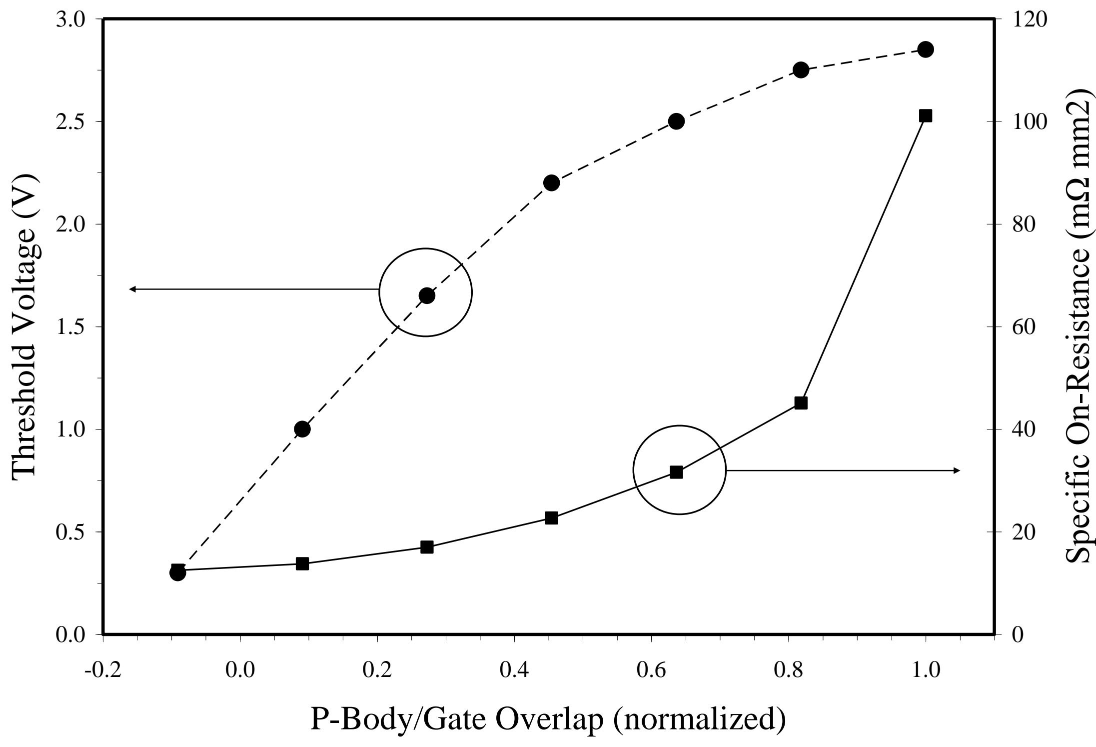


Figure 28: Simulated P-Body/Gate Overlap versus V_{TH} and R_{DSON}

First Iteration Experimental Results

Functional devices were obtained from the first TEG fabrication lot with BVDSS ranging from approximately 20 V to 34 V. The most critical design dimension proved to be the overlap between the P-Channel and the poly gate (L_{PCH}). Typical measurements for functional devices are shown in Figures 29 – 32. For functional devices with sharp BV_{DSS} and forward IV characteristics, V_{TH} was about 2 V higher than predicted by the TCAD modeling.

Figure 32 shows the measured V_{TH} versus L_{PCH} for different designs on the same wafer. Devices with small LPCH were not functional ($V_{TH} < 0.5$ V) and exhibited low BV_{DSS}. Devices with nominal LPCH exhibited a high variability in V_{TH} with no discernible influence from other layout variables. Only devices with the largest L_{PCH} showed any consistency in parametric yield.

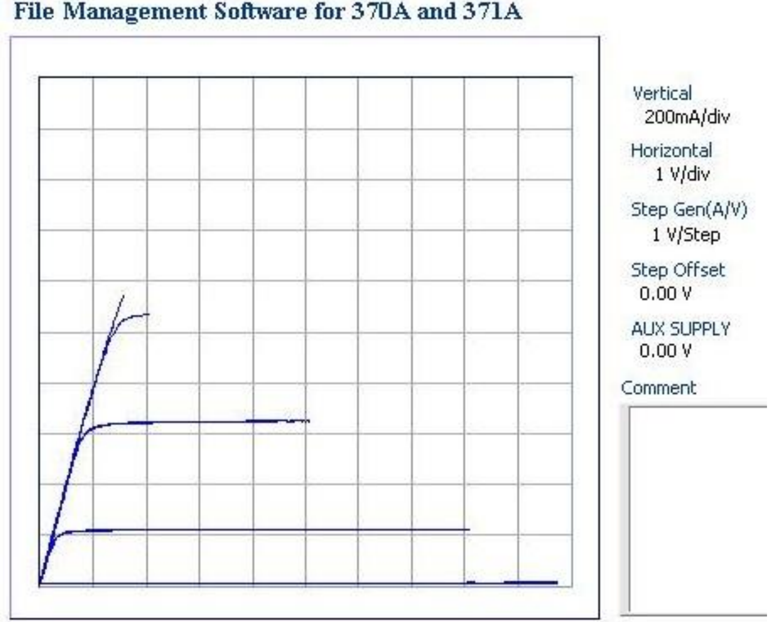


Figure 29: Measured Forward IV Characteristic of PCM Test Transistor

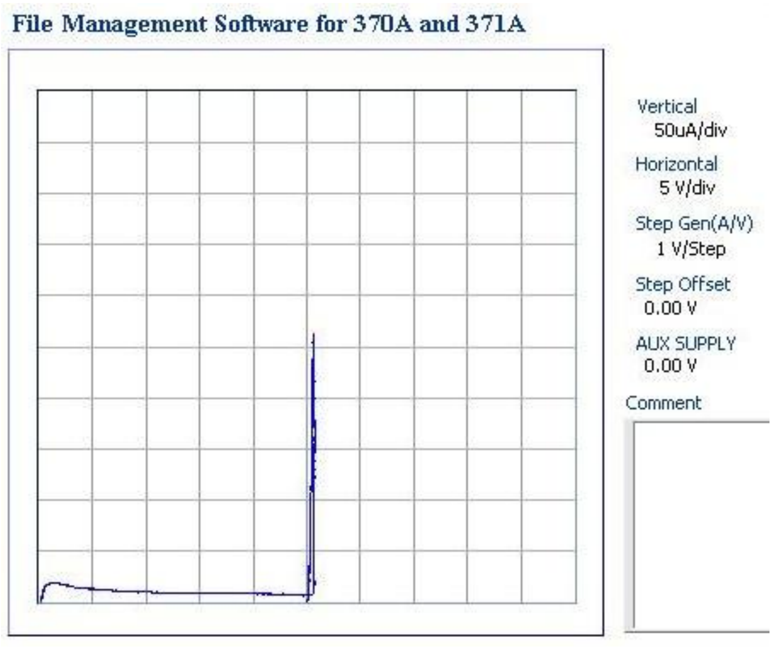


Figure 30: Measured BVDSS of PCM Test Transistor

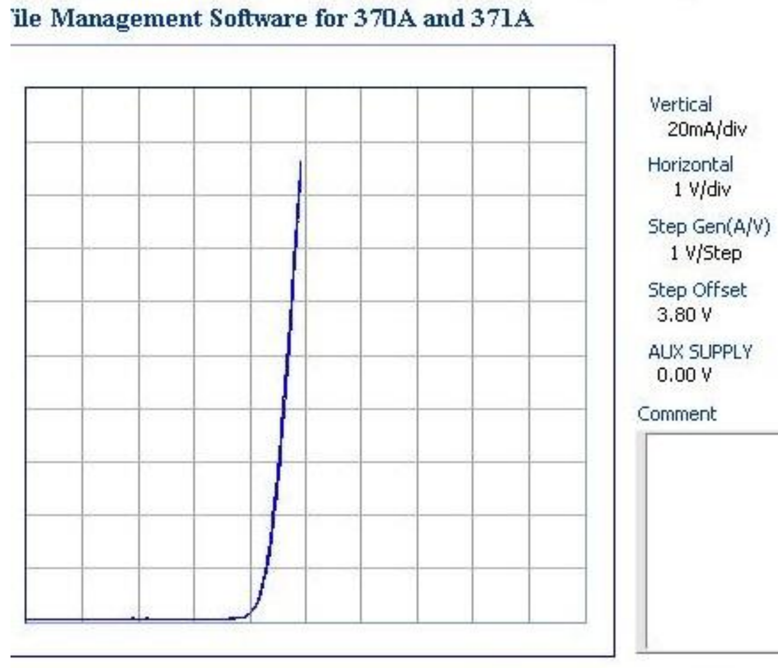


Figure 31: Measured VTH of PCM Test Transistor

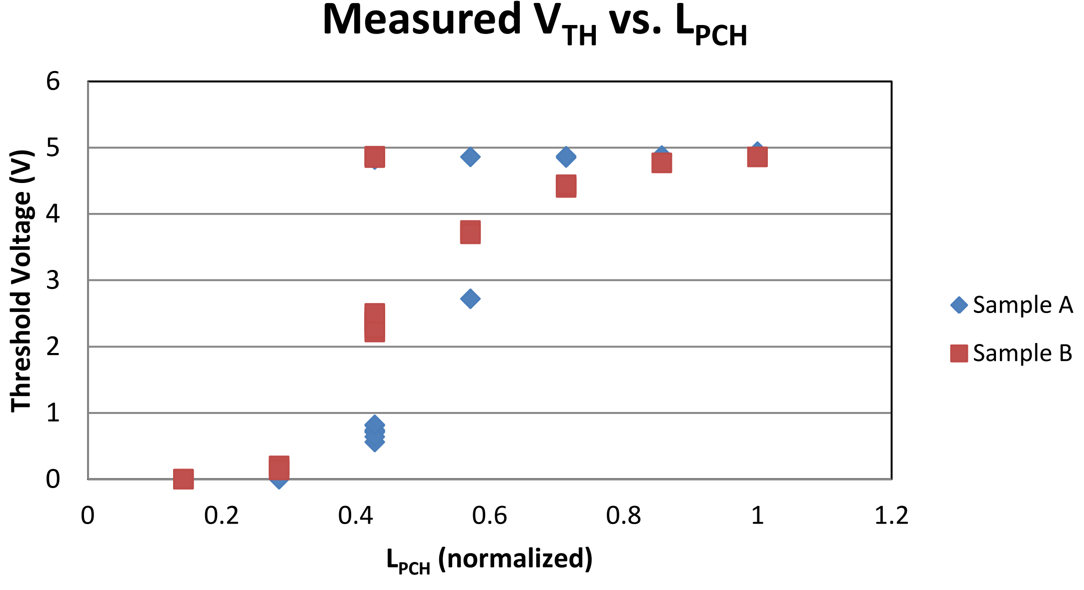


Figure 32: Measured Threshold Voltage vs. P-Channel Length

First Iteration SEE Test Results

Devices with BV_{DSS} of approximately 28 V and gate oxide thickness of 350 Å were tested for both SEB and SEGR by engineers from Sandia National Laboratories. The capacitor-response SEGR voltage was found to be approximately 14 V, which is consistent with predictions from the Titus-Wheatley formula. This suggests that lateral and vertical power MOSFETs exhibit similar capacitor response SEGR threshold voltages. Based on the structure of the devices and the nature of the capacitor response bias conditions ($V_{GS} < 0$, $V_{DS} = 0$), there was no prior expectation of any difference between the capacitor response of the two device types.

The SEB response of the device was found to be much worse than expected. Figure 33 shows measured SEB threshold voltages for different LET ions. At LETs at and above 42 $MeV \cdot cm^2 \cdot mg^{-1}$, devices failed due to SEB near $V_{DS} = 7$ V, or about 25% of the device's avalanche voltage.

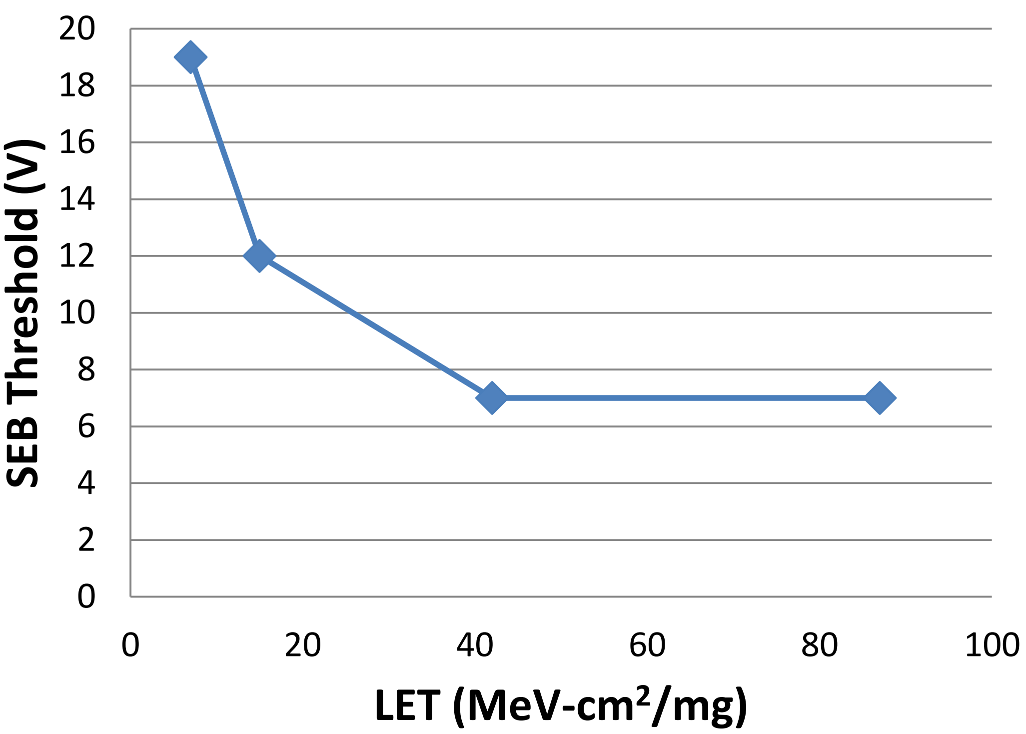


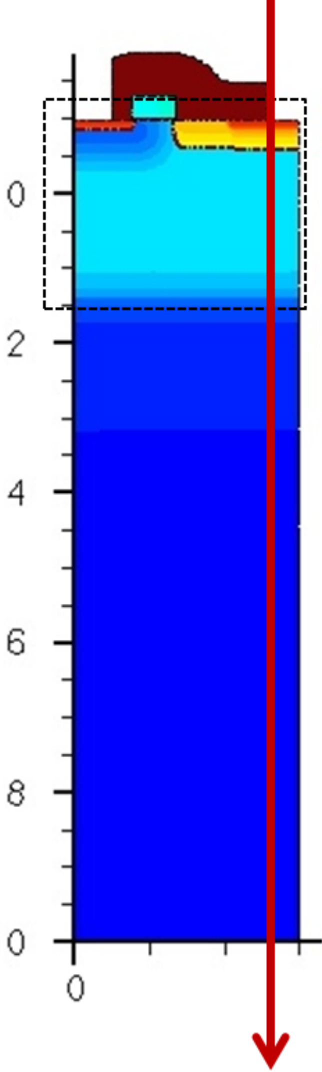
Figure 33: Measured SEB Threshold Voltage vs. LET

Second Iteration Modeling and Design

In order to explain the worse than expected SEB safe operating area, a series of two-dimensional heavy ion simulations were conducted using TCAD. No such SEE simulations had been performed prior to the original device design and fabrication. The results of these simulations provided insight into the fundamental physical mechanisms of single event burnout in the 25 V LDMOS structure.

The first set of SEE simulations were performed on the original design, which features a grounded P+ substrate and no P+ source body tie contact. The ion trajectory was a vertical strike through the N+ drain. Bias conditions are V_{DS} = 25 V, V_{GS} = 0 V. The bottom of the P+ substrate is tied to the same circuit ground as the N+ source, however different electrode names for the substrate and source are used in the simulation. This allows the substrate current to be plotted separately. Figure 34 shows a 2-D cross section of the simulated transistor half-cell, with the location and trajectory of the simulated heavy ion indicated by the red arrow.

In each transient simulation, the heavy ion charge generation peaks at 10 picoseconds. One goal of the simulations was to observe the transient response of voltage and current within the 2-D device cross section during the heavy ion strike. The first step was to perform a transient simulation to determine at which times critical changes in current were likely to occur. Then, 2-D device snapshots at those times were programmed into future simulations. The results are a series of time snapshots on a roughly logarithmic scale, which illustrate the physical mechanisms of SEB.

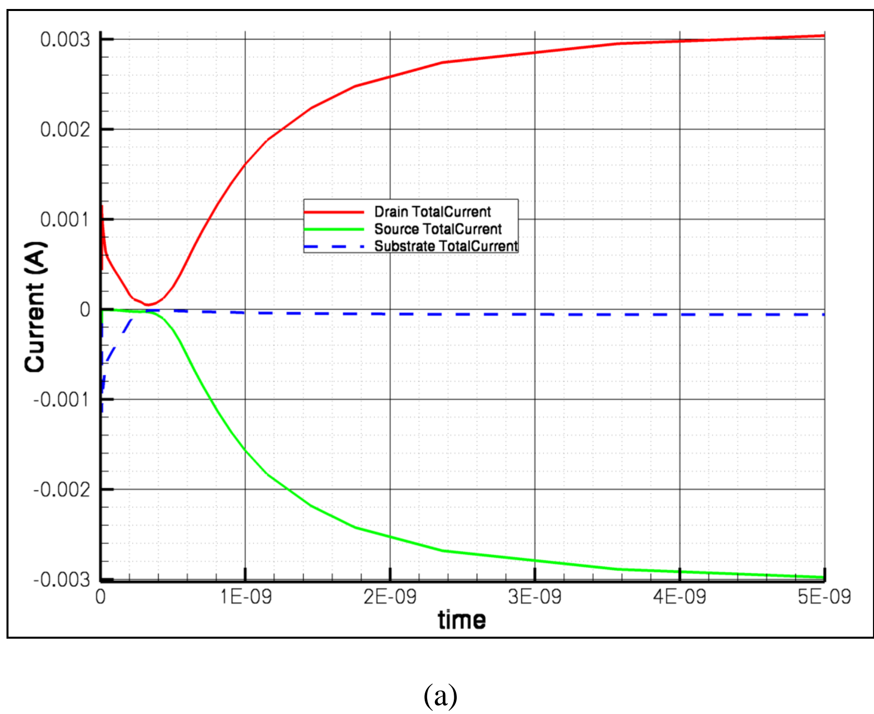


The red arrow illustrates the simulated trajectory of the heavy ion. Biasing conditions for SEE simulations with this structure are VDS = 25 V, VGS = 0 V. The substrate and N+ source are tied to a common ground node, but use different electrode names, so the current in the substrate can be plotted separately from N+ source current. The dashed line encloses the area shown in many subsequent figures, which illustrate the transient response of the device.

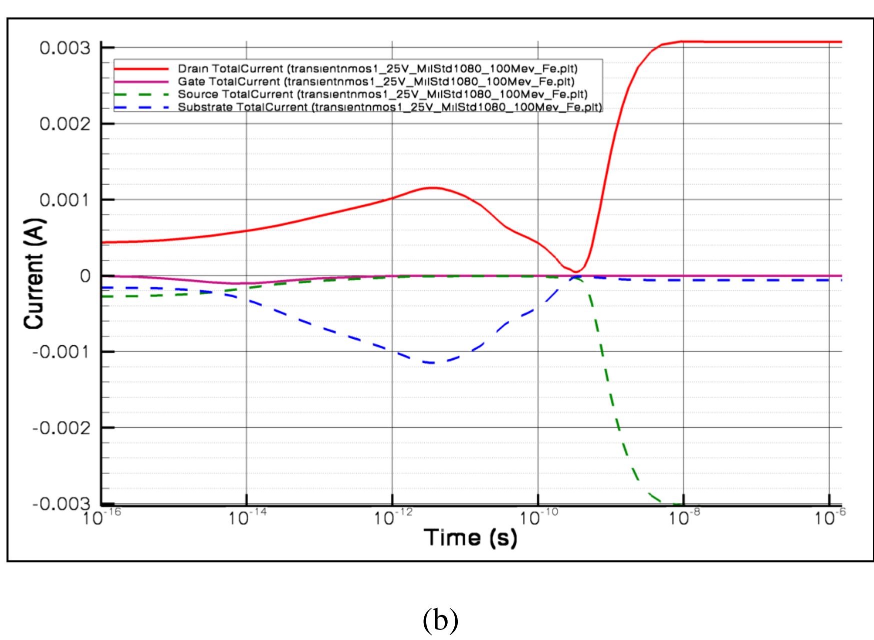
Figure 34: LDMOS Structure for SEE Simulations (Design 1)

Figure 35 shows the transient single event burnout waveform in both linear and logarithmic time scales. At time = 10 ps, the heavy ion charge generation reaches its transient peak. This corresponds to the first peak in current in Figure 35b. Between time = 100 ns and 200 ns, it appears that most of the heavy ion charge has been collected, and the total current decreases Until this time, the vast majority of current flow has been between the drain and substrate. After this time, the current suddenly increases again, and this time the vast majority of current is flowing from the N+ drain to the N+ source. At the end of the simulation, time = 1.5 μs, the device has been experiencing a self-sustained high level of current for over 1 μs, indicating that single event burnout has occurred.

Figures 36 – 41 show the 2-D transient snapshots of electrostatic potential, electric field magnitude, impact ionization, total current density, electron current density, and hole current density for the same simulation. It can be noted that around time = 100 ns, high levels of impact ionization are observed in three distinct regions – the N+ drain, the neck region, and the P+ substrate junction below the drain. At this time, it can also be seen that the entire surface of the device has floated up to a slightly higher voltage than in the previous time frame at time = 50 ps. Hole and electron current begins to flow through the source region at the surface of the device, indicating that the source-body p-n junction has become forward biased. From that point forward, the current flow is almost exclusive at the device surface. The MOSFET features at the device surface are operating together as an open-base NPN BJT.



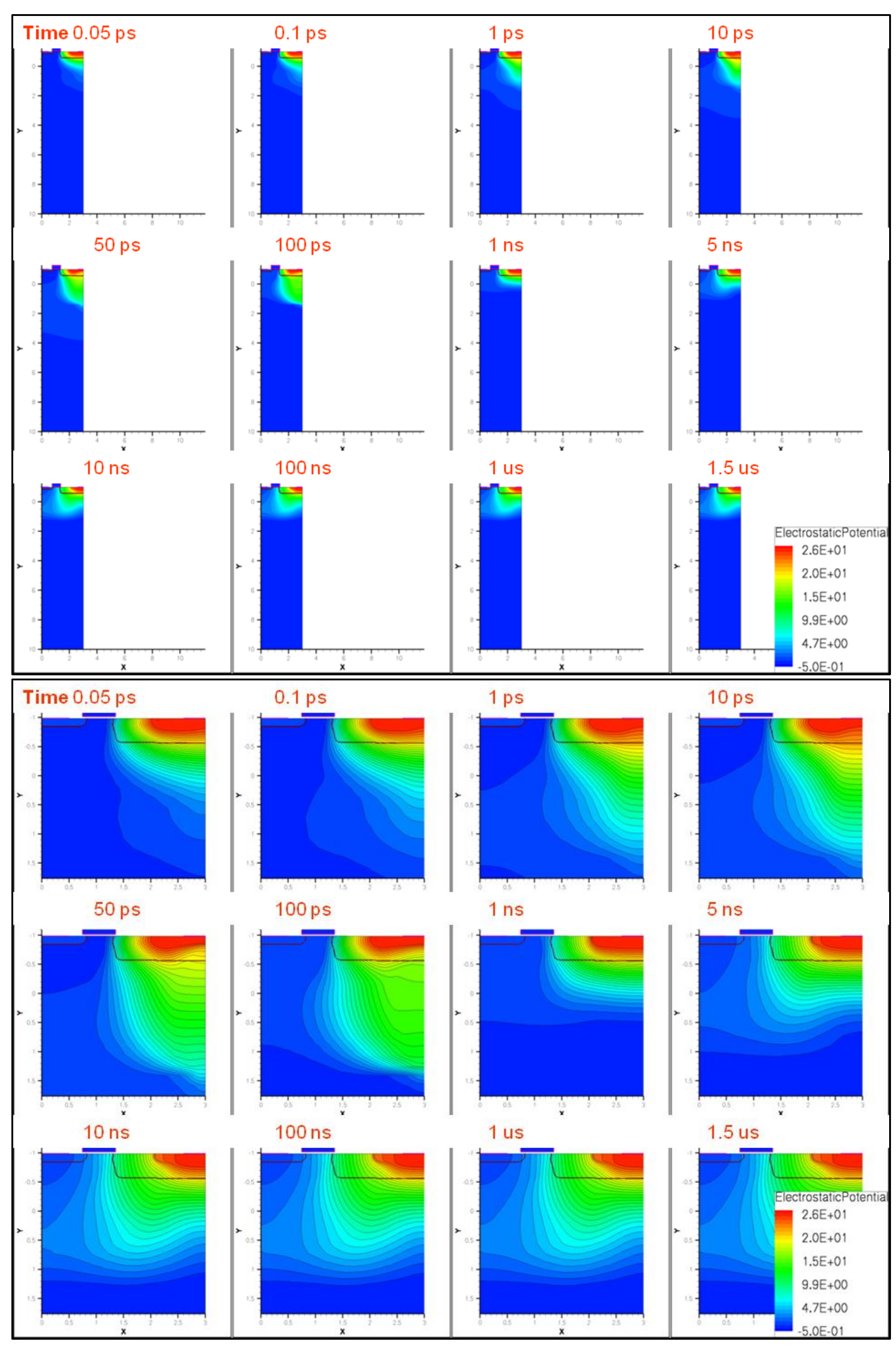
(a)



(b)

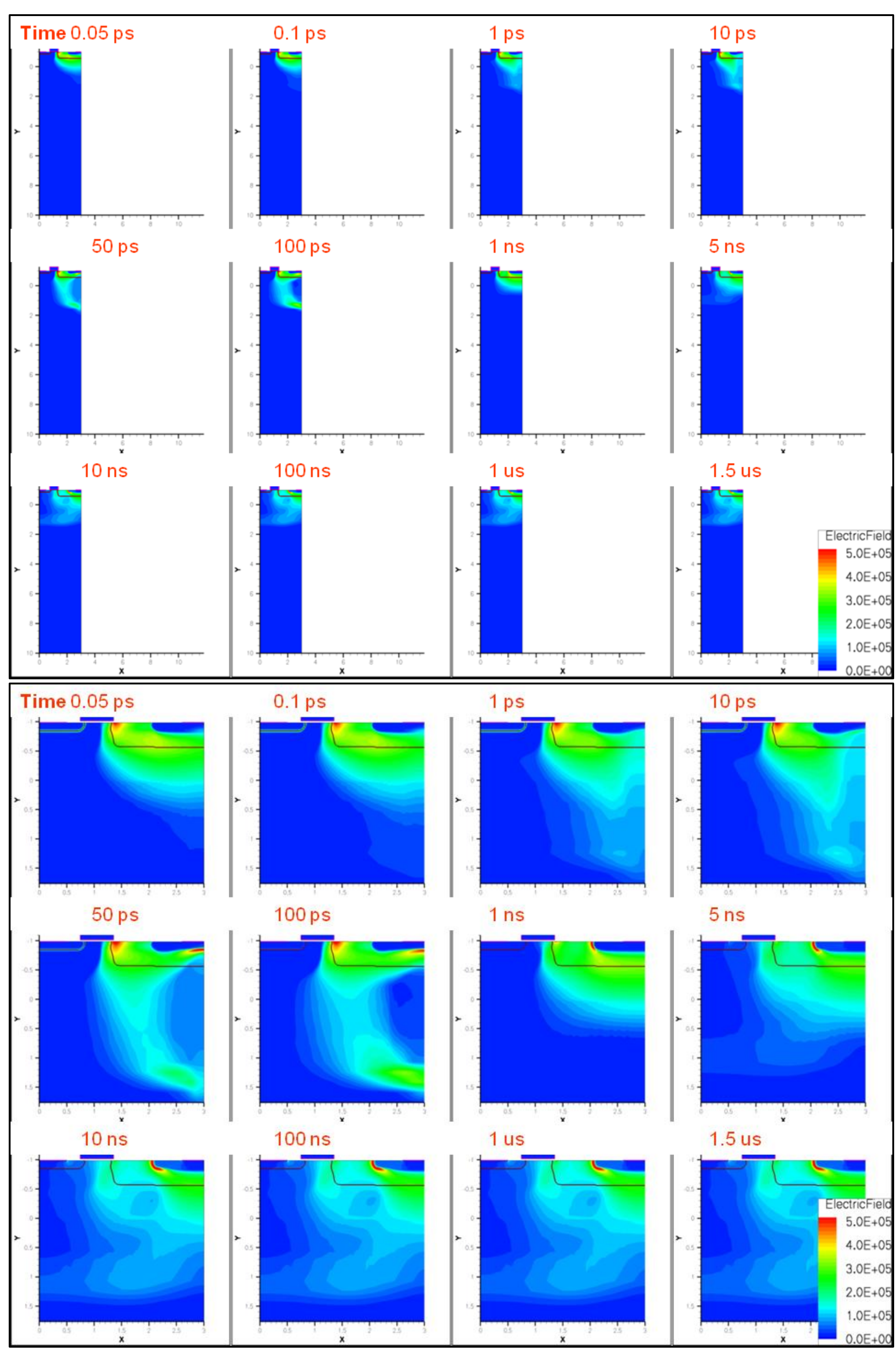
Linear time scale (a) and logarithmic time scale (b) of terminal currents during single event burnout simulation. Just before time = 1 ns, the parasitic NPN bipolar transistor is activated, and the majority of the drain to source current stops flowing through the substrate and instead flows through the N+ source.

Figure 35: Simulated Single Event Burnout Waveforms (Design 1)



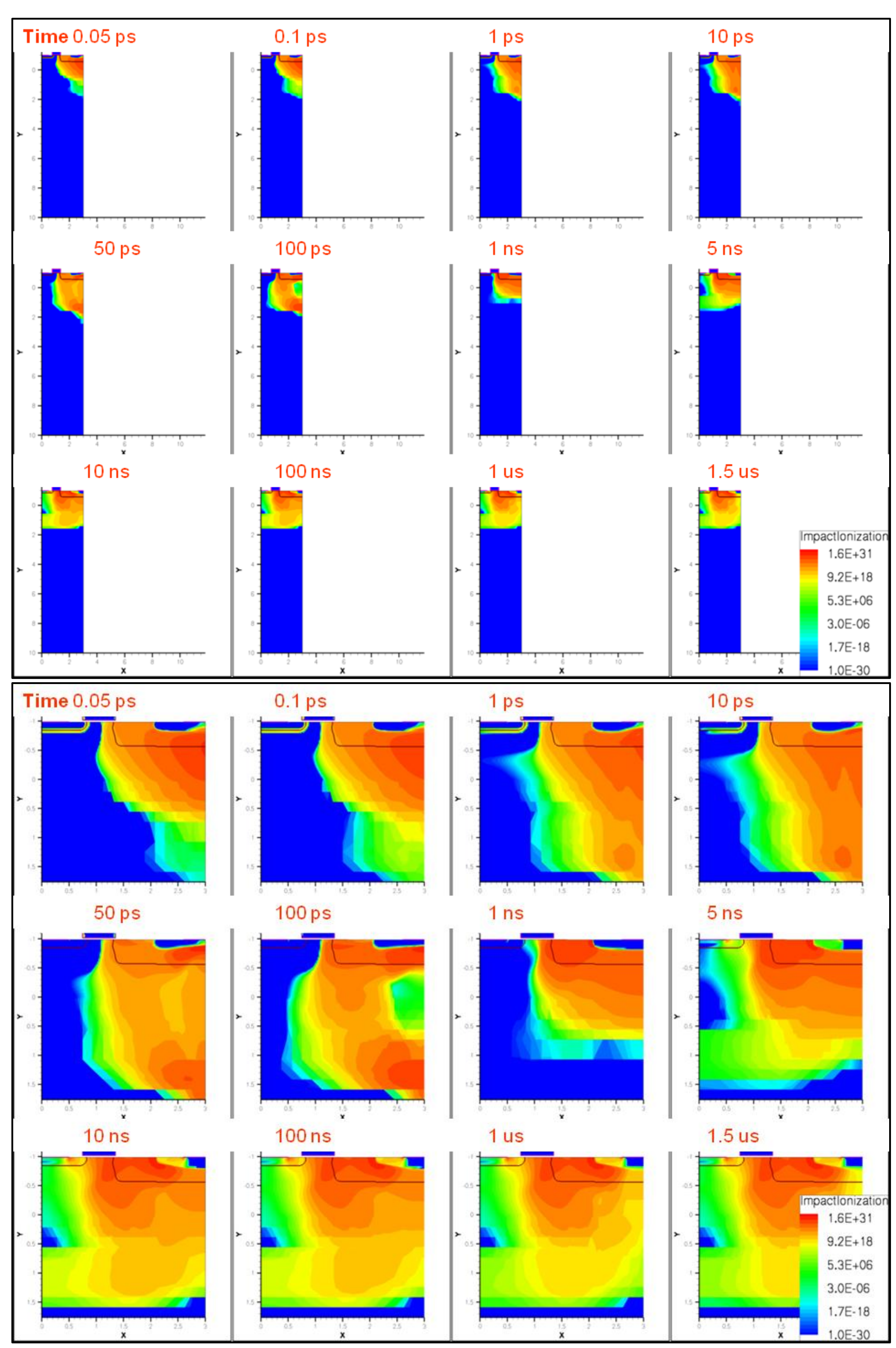
Wide view (top) and zoomed-in view (bottom) of transient electrostatic potential during heavy ion strike through the N+ drain. VDS = 25 V, VGS = 0 V, LET = 86 MeV·cm^2·mg^{-1}.

Figure 36: Simulated Electrostatic Potential During Heavy Ion Strike (Design 1)



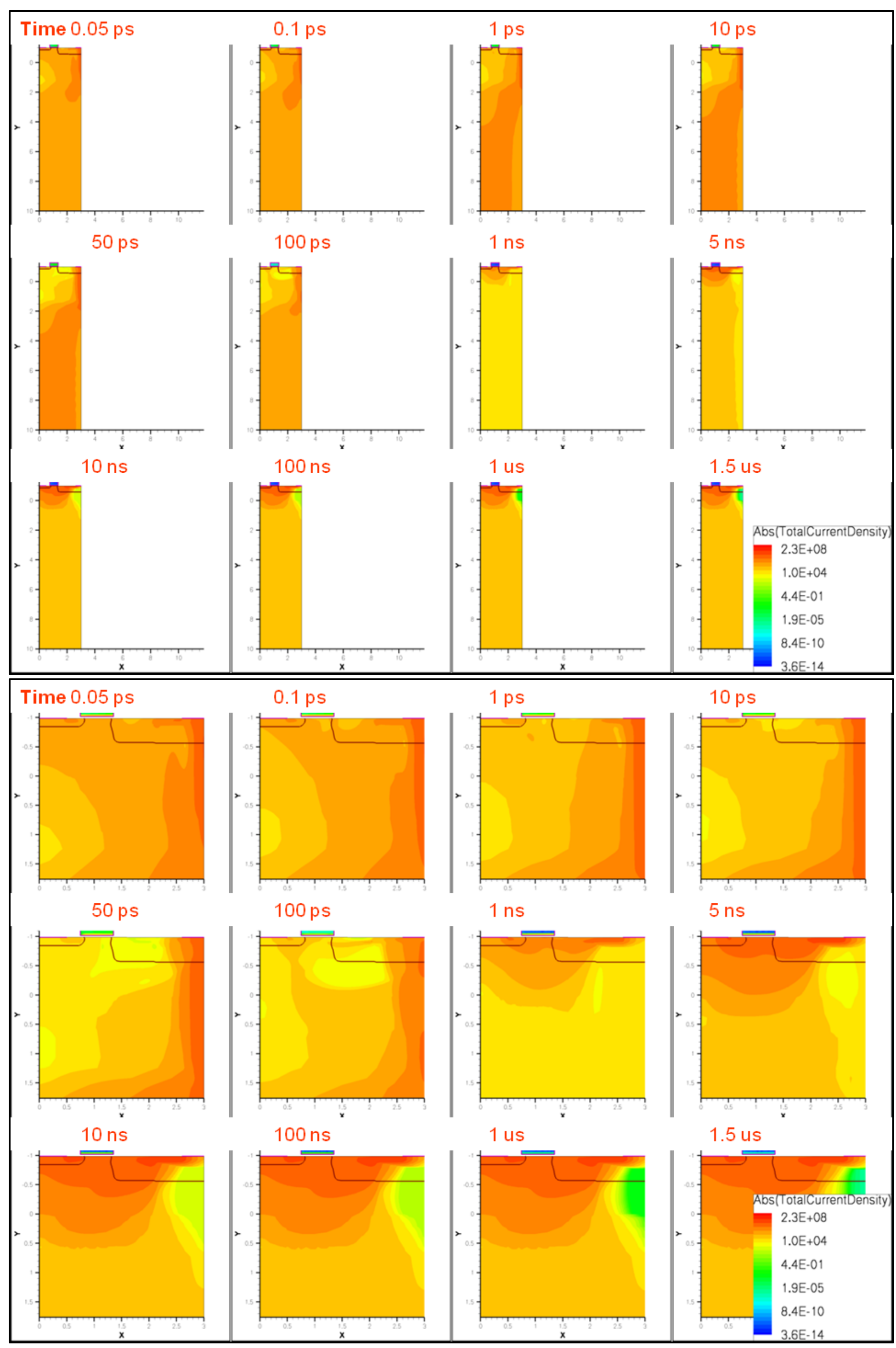
Wide view (top) and zoomed-in view (bottom) of transient electric field magnitude during heavy ion strike through the N+ drain. VDS = 25 V, VGS = 0 V, LET = 86 MeV·cm^2·mg^{-1}.

Figure 37: Simulated Electric Field During Heavy Ion Strike (Design 1)



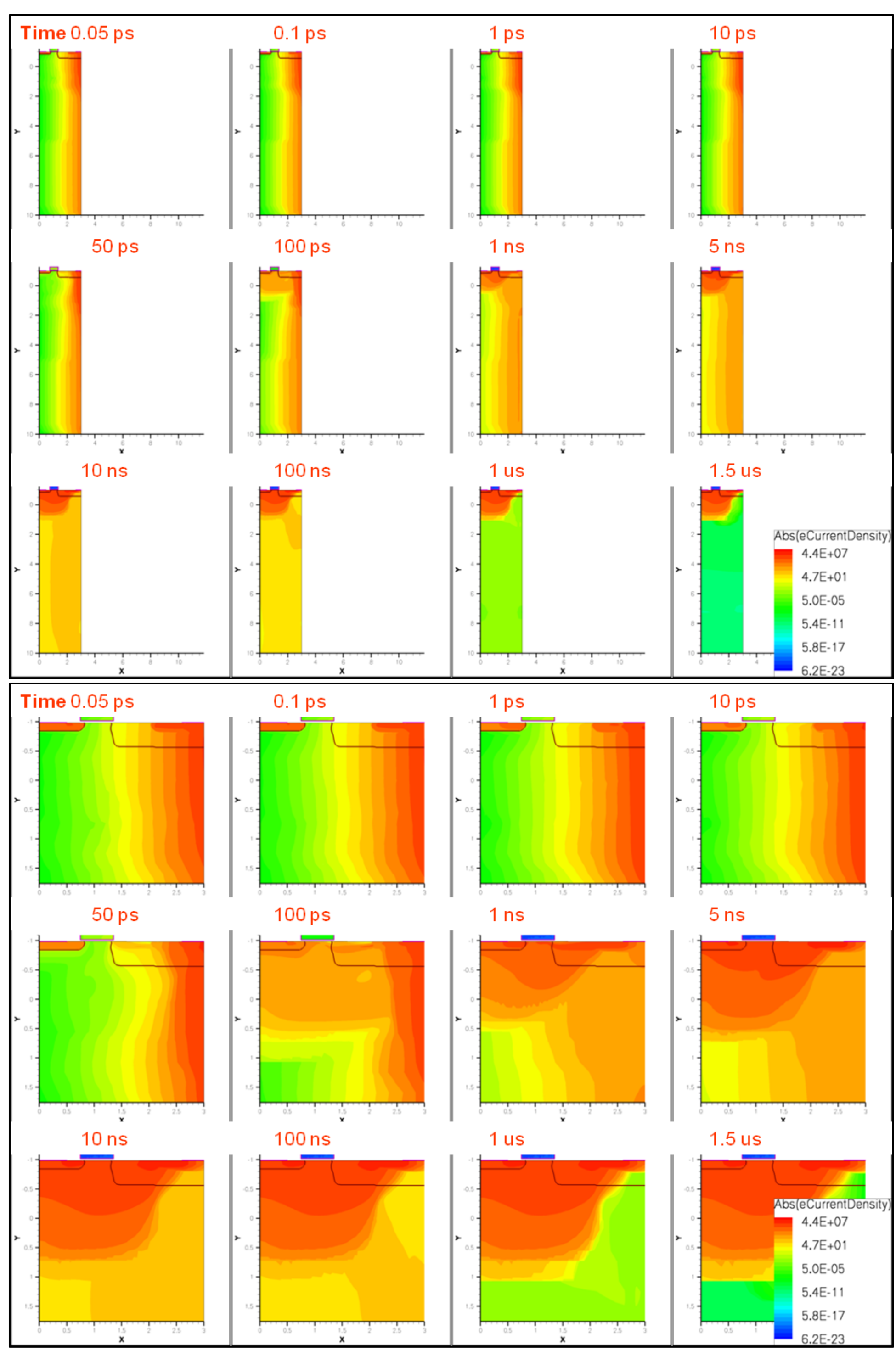
Wide view (top) and zoomed-in view (bottom) of transient impact ionization during heavy ion strike through the N+ drain. VDS = 25 V, VGS = 0 V, LET = 86 MeV·cm^2·mg^{-1}.

Figure 38: Simulated Impact Ionization During Heavy Ion Strike (Design 1)



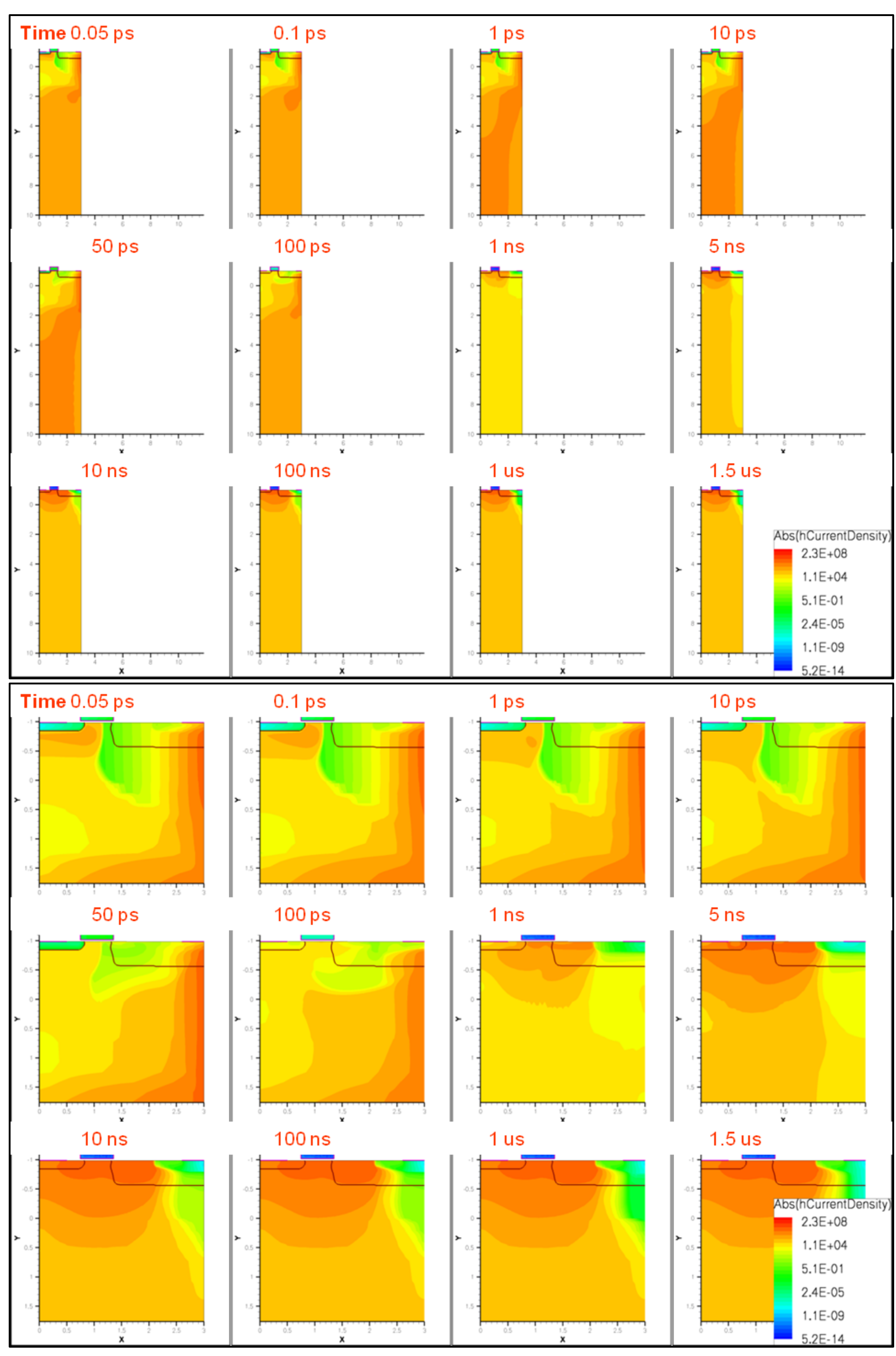
Wide view (top) and zoomed-in view (bottom) of transient total current density during heavy ion strike through the N+ drain. VDS = 25 V, VGS = 0 V, LET = 86 MeV·cm^2·mg^{-1}.

Figure 39: Simulated Total Current Density During Heavy Ion Strike (Design 1)



Wide view (top) and zoomed-in view (bottom) of transient electron current density during heavy ion strike through the N+ drain. VDS = 25 V, VGS = 0 V, LET = 86 MeV·cm^2·mg^{-1}.

Figure 40: Simulated Electron Current Density During Heavy Ion Strike (Design 1)

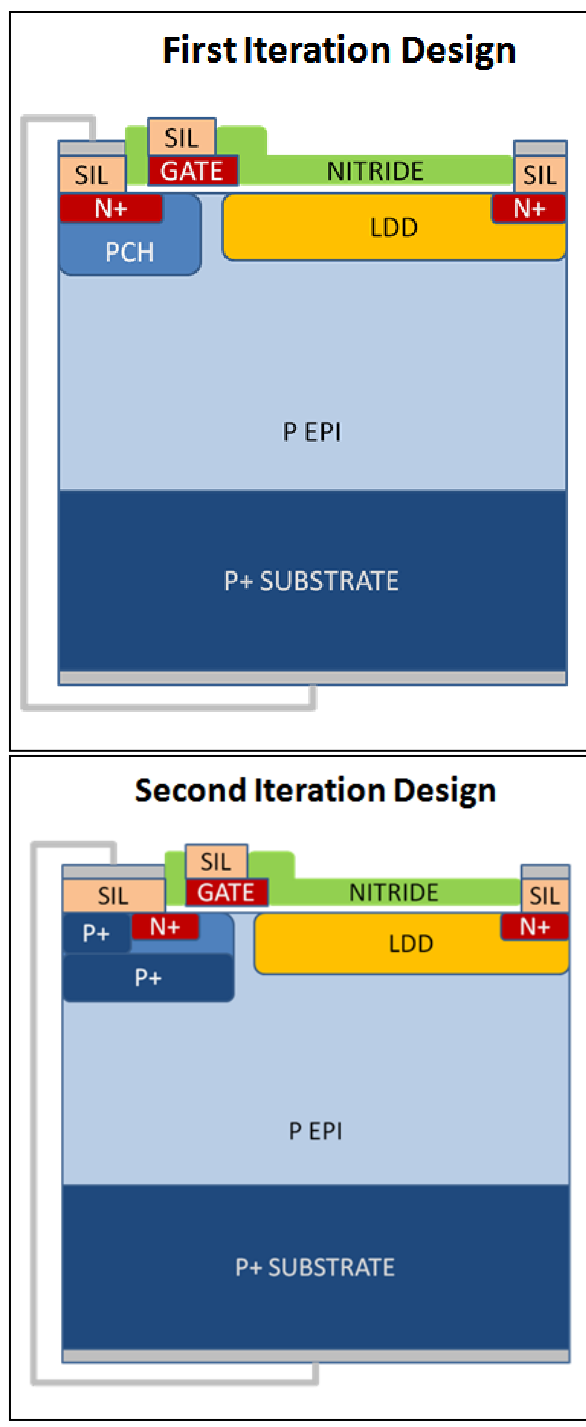


Wide view (top) and zoomed-in view (bottom) of transient hole current density during heavy ion strike through the N+ drain. VDS = 25 V, VGS = 0 V, LET = 86 MeV·cm^2·mg^{-1}.

Figure 41: Simulated Hole Current Density During Heavy Ion Strike (Design 1)

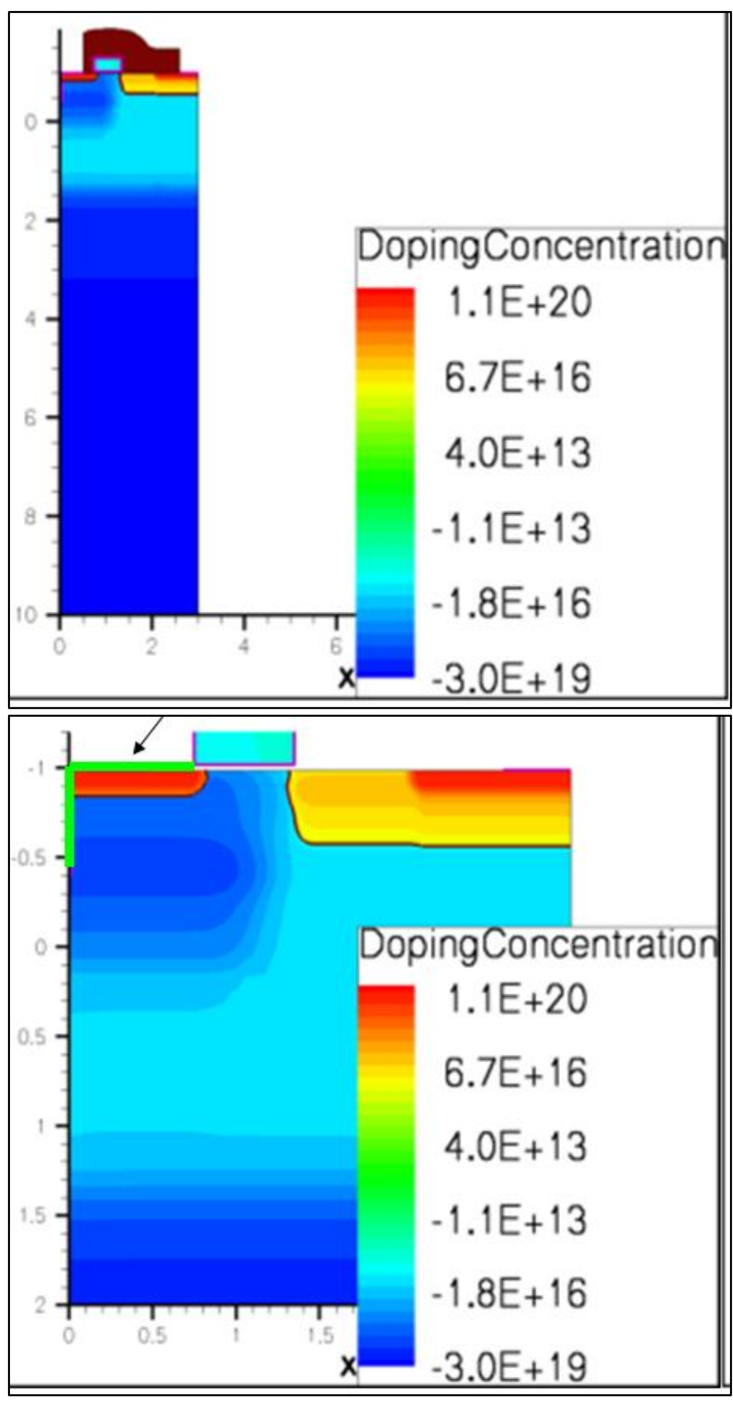
It was determined from these simulations, that despite the P+ substrate providing a very low resistance path for the collection of hole current during the heavy ion strike, the parasitic NPN bipolar transistor at the surface of the device was still being activated. Therefore, it was concluded that a low resistance P+ source body tie should be added to the top surface of the device, to eliminate the open-base NPN BJT. We developed a new structure, shown in Figures 42 and 43, which incorporates the P+ body tie as well as a highly doped P+ buried layer, which runs underneath the P-Channel region. The P+ buried layer is degenerately doped for very low resistance. This type of structure was thought to provide a very low base resistance at the surface. Also, any electrons being injected from the N+ source would have to travel across the wide P+ buried layer, which would recombine many of the electrons and reduce the gain of the parasitic NPN. The P+ buried layer was placed approximately 0.5 μm deep, in order to prevent incursion into the channel region, so that it would not significantly increase VTH of the MOSFET.

We theorized that the P+ source body tie and P+ substrate would work in parallel to share the hole current during the ion strike, but we still expected most of the hole current to flow through the large P+ substrate. We also recognized, however, that the grounded P+ substrate was a source of impact ionization during the simulated ion strike. By fixing the potential at the P+ substrate junction, that junction formed an electrostatic potential barrier at which a high electric field would form during the transient, as had also been reported for N-channel devices [29]. We therefore decided to explore the option of leaving the P+ substrate floating, to observe how the electric field might be reshaped and whether we could eliminate or suppress that source of impact ionization.



Cross sectional drawings of original (top) and redesigned (bottom) 25 V LDMOS with P+ buried layer source body tie. The P+ body tie and N+ source are silicided and tied to a common contact.

Figure 42: First and Second Iteration 25 V LDMOS Designs

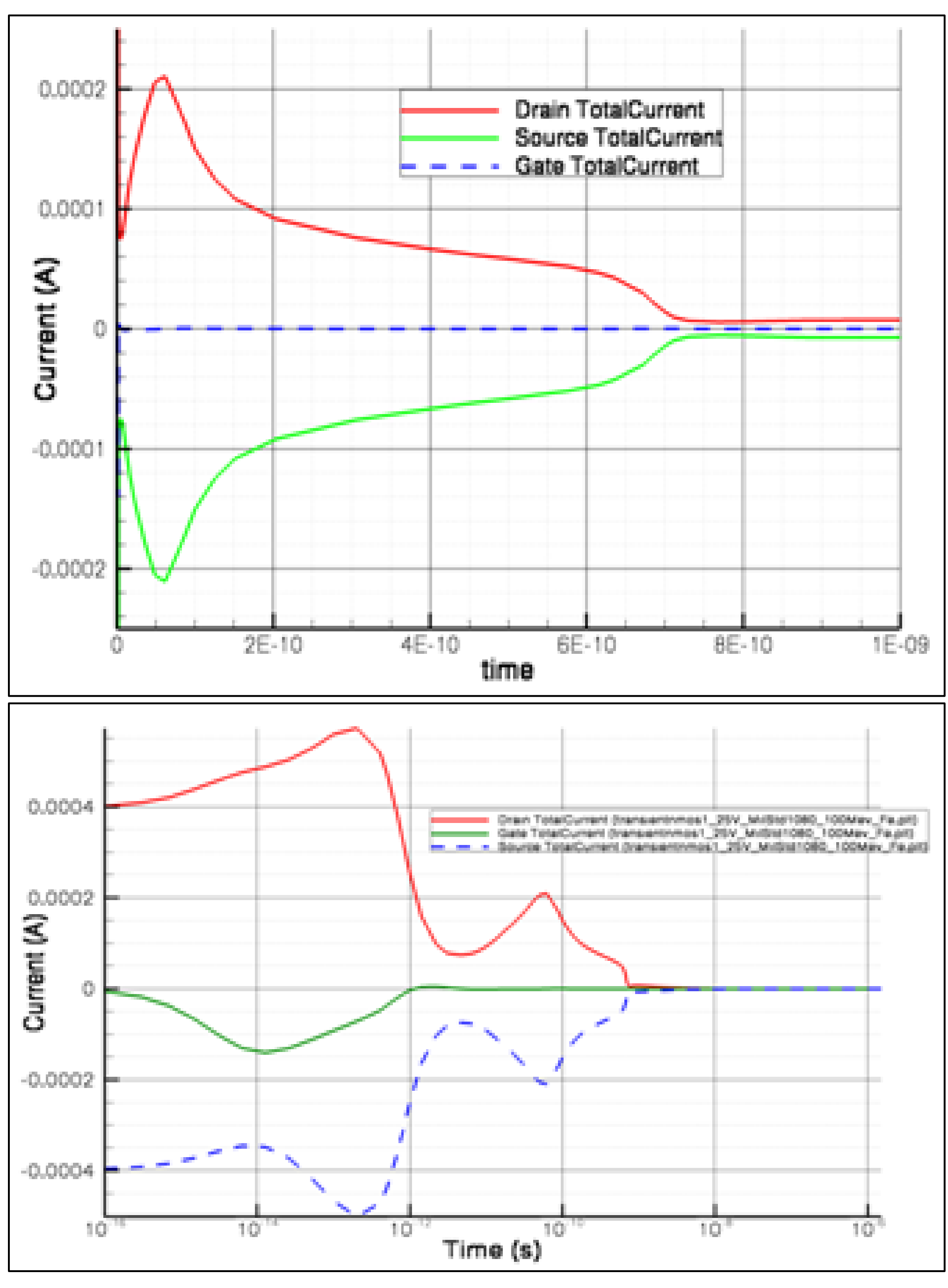


Wide view (top) and zoom-in view (bottom) of redesigned 25 V LDMOS with P+ buried layer source body tie. The P+ body tie and N+ source are tied to a common contact, indicated by the green shaded area at the top left corner of the device.

Figure 43: Redesigned 25 V LDMOS with P+ Buried Layer Source Tie

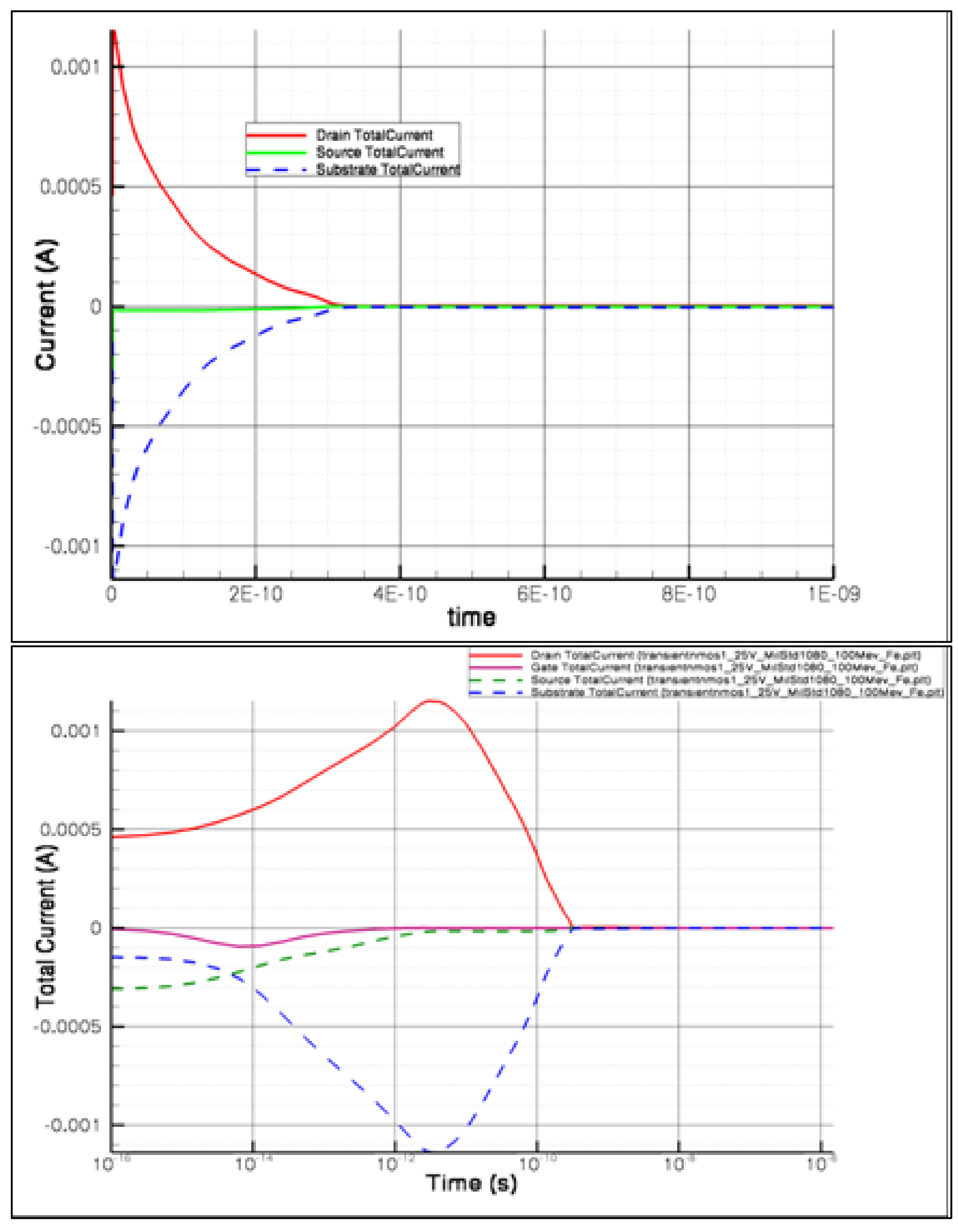
The results of the two sets of simulations on the improved device structure, one set with a grounded substrate and one set with a floating substrate, are presented in Figures 44 – 50. These simulations used the same heavy ion model and same V_{DS} and V_{GS} biasing conditions as the previous set of simulations for the original device structure without P+ buried layer. In both cases, grounded or floating substrate, no SEB was predicted for the new design with P+ buried layer. Additionally, no activation of the parasitic NPN bipolar transistor could be observed in the simulations. In the waveform shown in figure 45, for the device with the grounded substrate, it can be seen that almost all the current is carried between the drain and substrate, with very little current flowing through the topside source contact.

The option of floating the P+ substrate did not result in reduced levels of impact ionization. The floating substrate instead became electrically coupled to the drain by the highly conductive ion shunt, and the substrate floated up almost to the rail voltage. At that point, almost the entire V_{DS} voltage had to be sustained between the P+ substrate and the P+ buried layer. The electric field hotspot and associated impact ionization simply moved from the P+ substrate junction, in the case of the grounded substrate, to the P+ buried layer, in the case of the floating substrate. The floating substrate was thought to be a worse case than the grounded substrate, because of the close proximity of the impact ionization to the base-emitter p-n junction, and the increased current flow through the P+ buried layer, which made it more likely to induce a resistive voltage drop across the base. The grounded P+ substrate seemed to distribute the current and electrical stress much more evenly throughout the device, which should translate to improved SEB SOA.



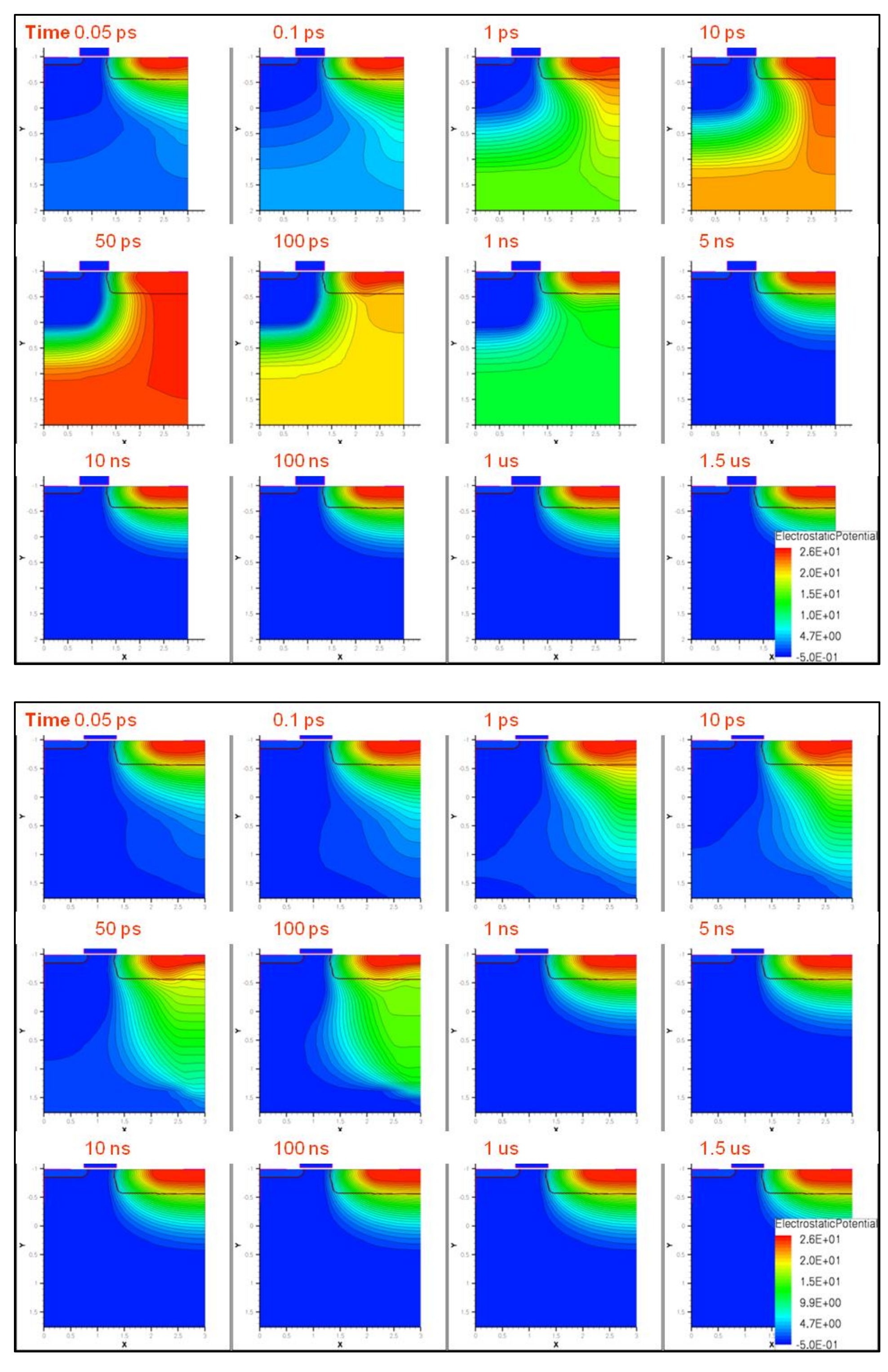
Linear scale (top) and log scale (bottom) single event transient waveforms for the redesigned structure with P+ buried layer and a floating P+ substrate. No activation of the parasitic NPN bipolar transistor was observed. This simulation uses the same biasing and LET conditions (VDS = 25 V, VGS = 0 V, LET = 86 MeV cm^2 mg^{-1}) that resulted in SEB during simulation of the original MOSFET design.

Figure 44: Simulated Single Event Transient Waveforms
(Design 2 Floating Substrate)



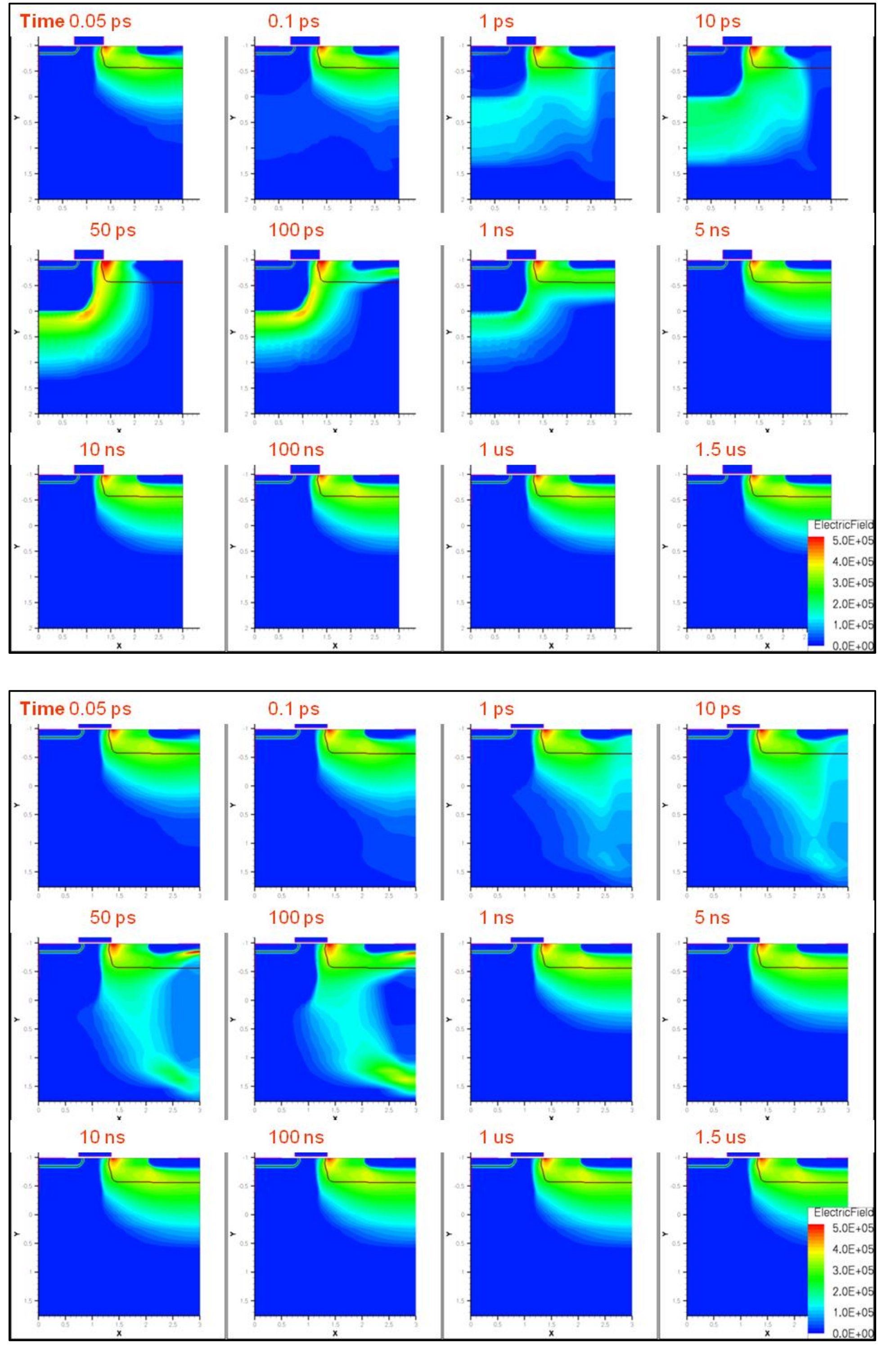
Linear scale (top) and log scale (bottom) single event transient waveforms for the redesigned structure with P+ buried layer and a grounded P+ substrate. No activation of the parasitic NPN bipolar transistor was observed. This simulation uses the same biasing and LET conditions (VDS = 25 V, VGS = 0 V, LET = 86 MeV cm^2 mg^{-1}) that resulted in SEB during simulation of the original MOSFET design.

Figure 45: Simulated Single Event Transient Waveforms
(Design 2 Grounded Substrate)



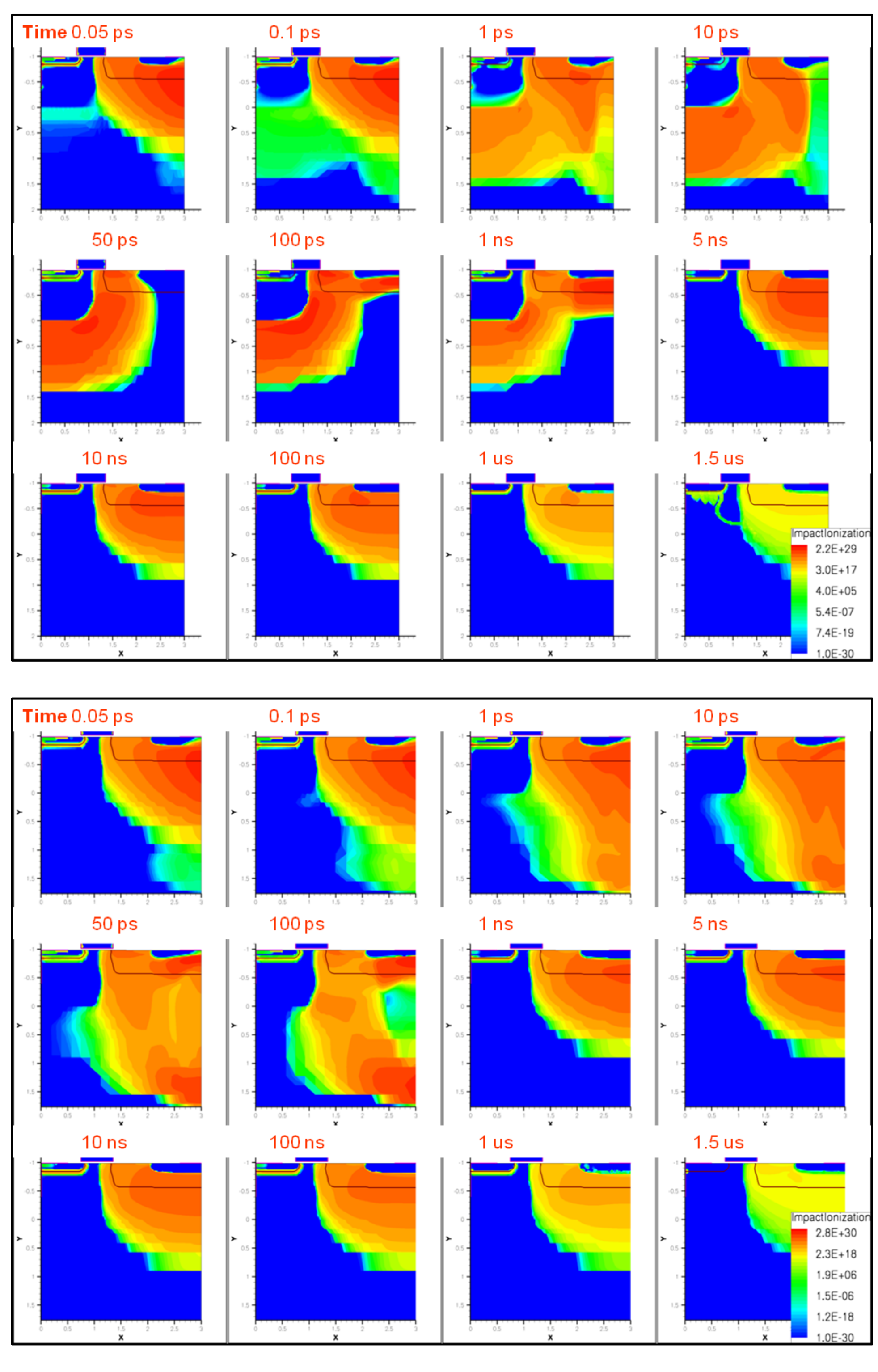
Potential contours during heavy ion strike for floating substrate (top) and grounded substrate (bottom).

Figure 46: Simulated Electrostatic Potential During Heavy Ion Strike (Design 2)



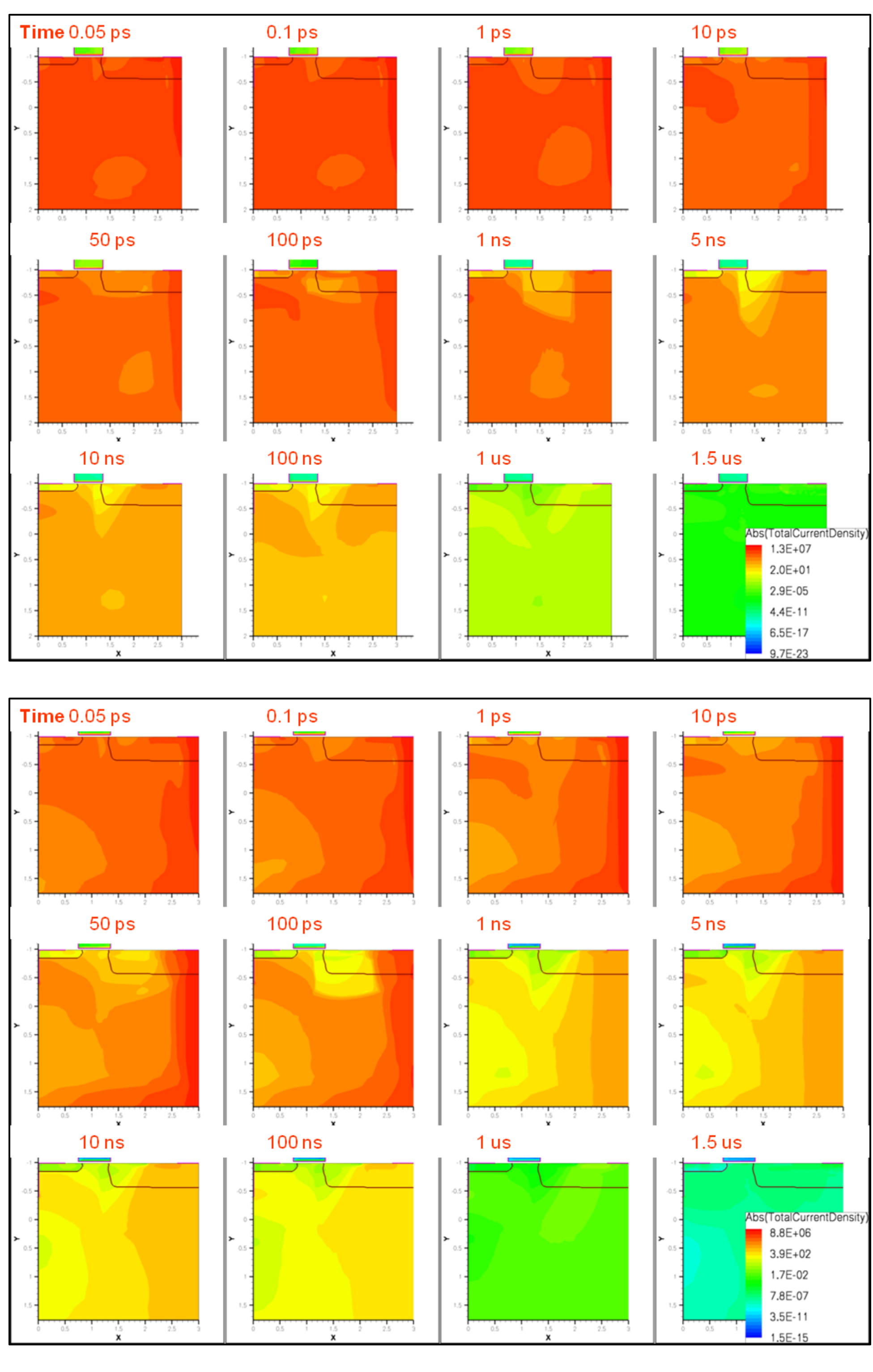
Electric field during heavy ion strike for floating substrate (top) and grounded substrate (bottom).

Figure 47: Simulated Electric Field During Heavy Ion Strike (Design 2)



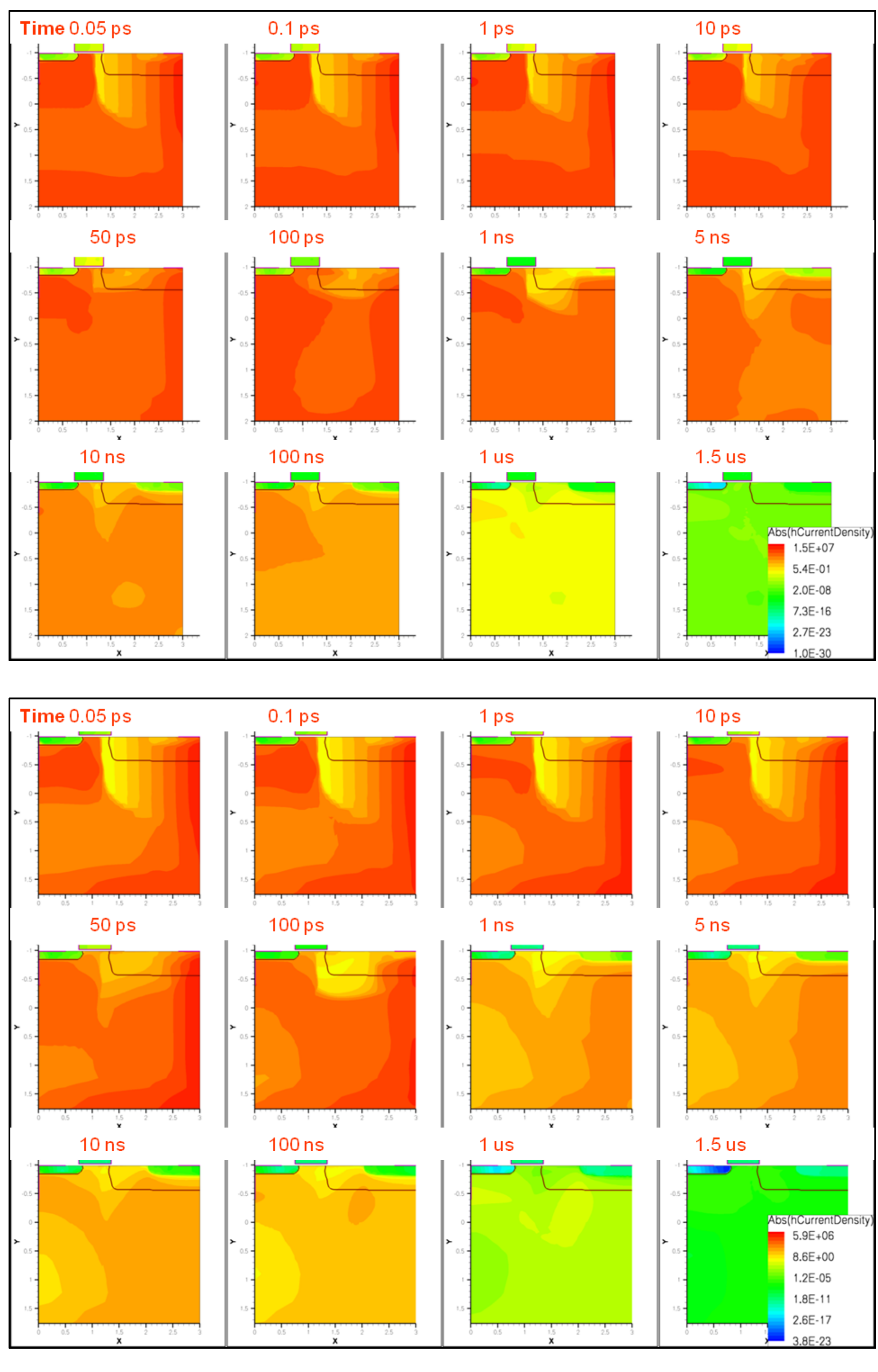
Impact ionization during heavy ion strike for floating substrate (top) and grounded substrate (bottom).

Figure 48: Simulated Impact Ionization During Heavy Ion Strike (Design 2)



Total current density during heavy ion strike for floating substrate (top) and grounded substrate (bottom).

Figure 49: Simulated Total Current Density During Heavy Ion Strike (Design 2)



Hole current density during heavy ion strike for floating substrate (top) and grounded substrate (bottom).

Figure 50: Simulated Hole Current Density During Heavy Ion Strike (Design 2)

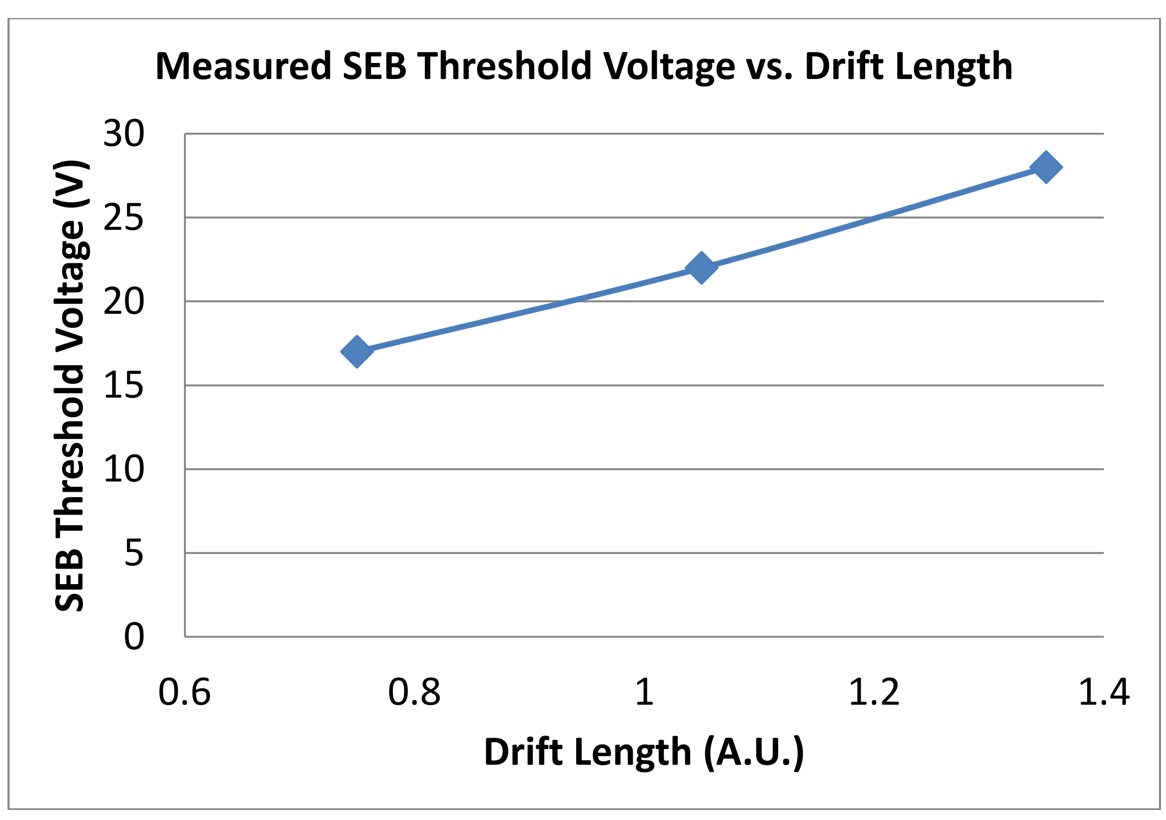
Second Iteration Experimental Results

A second design matrix containing transistors with varied drift length was used to generate a new TEG mask, and a second wafer lot was run using wafers with varied epi layer thicknesses. Also, the nominal gate oxide thickness for the device was increased from 350 Å to 600 Å, to increase SEGR hardness. As mentioned previously, drift resistance R_D makes up a large portion of the total R_{DSON} of the LDMOS. Increasing drift length L_N increases both BV_{DSS} and R_{DSON} of the MOSFET. Similarly, increasing the gate oxide thickness leads to an increase in V_{TH} and a decrease in g_m, which leads to an increase in channel resistance. Channel resistance accounts for another large portion of the total R_{DSON} of the transistor. The increase in drift length, compounded by the increase in gate oxide thickness, produced significantly higher R_{DSON} for the second iteration devices. Additionally, to compensate for the higher V_{TH} due to the thicker oxide, the P-Channel implant dose had to be reduced, which increases the base resistance of the parasitic NPN bipolar transistor near the surface of the MOSFET. Similarly, the P+ buried layer implant dose and energy had to be tuned to avoid up-diffusion of the P+ buried layer implant into the MOS channel region, which would have resulted in high R_{DSON}.

The result of the second iteration design was an improvement in SEB safe operating area, as shown in Figure 51. At LET = 14 MeV cm2 mg-1, first iteration devices with normalized L_N = 0.75 had an SEB threshold voltage of only 12 V. The SEB threshold voltage was improved to 17 V in the second iteration design with the same drift

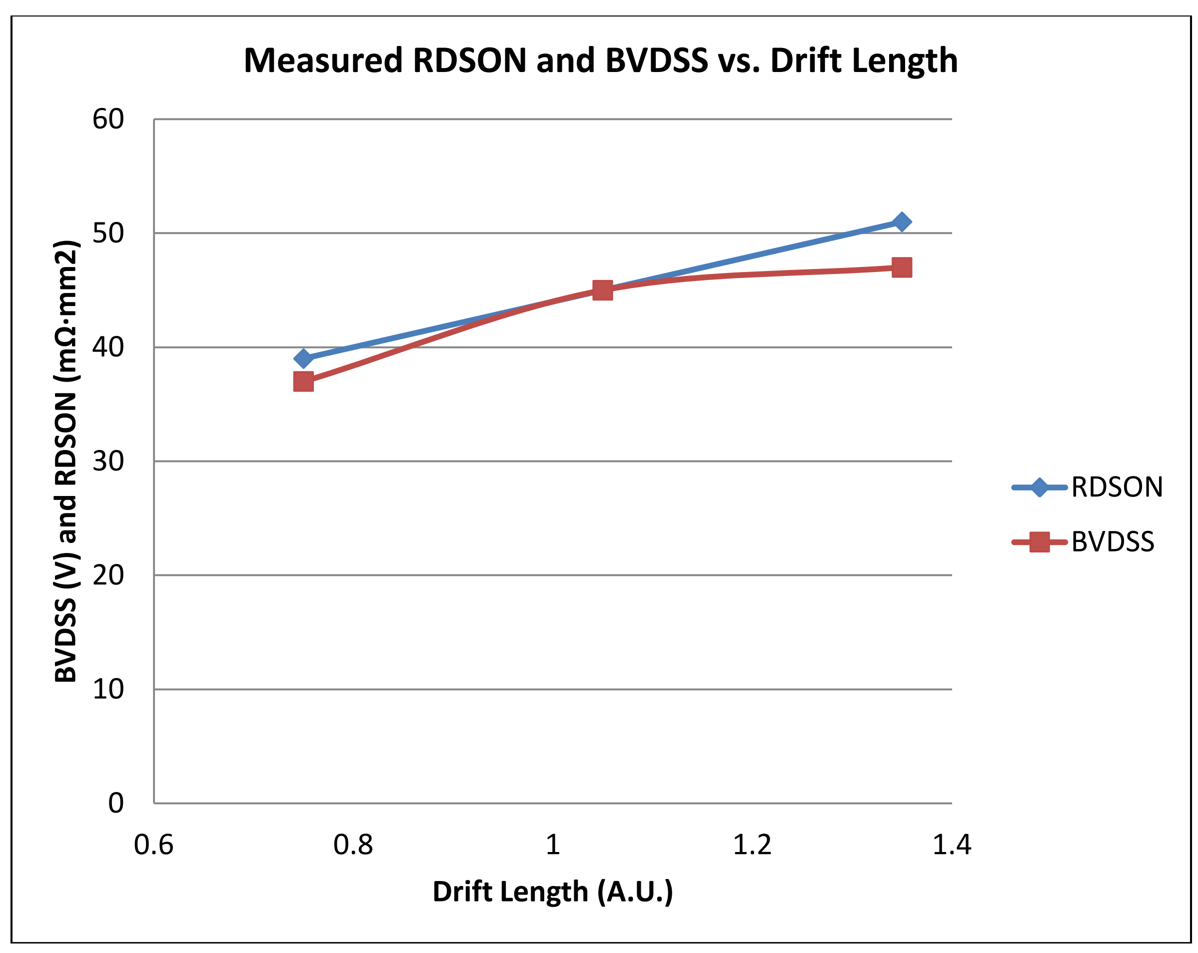
length. Devices with longer drift lengths from the same wafer were able to achieve SEB threshold voltages up to 28 V, however those devices had 30% higher R_{DSON}.

Further SEB safe operating area improvements were accomplished by using thinner epi layers to reduce the charge collection volume of the MOSFET, as well as varying the P+ buried layer implant conditions, as shown in Figure 53. SEB threshold voltages increased from approximately 28 V to 38 V with further optimization of these design metrics.



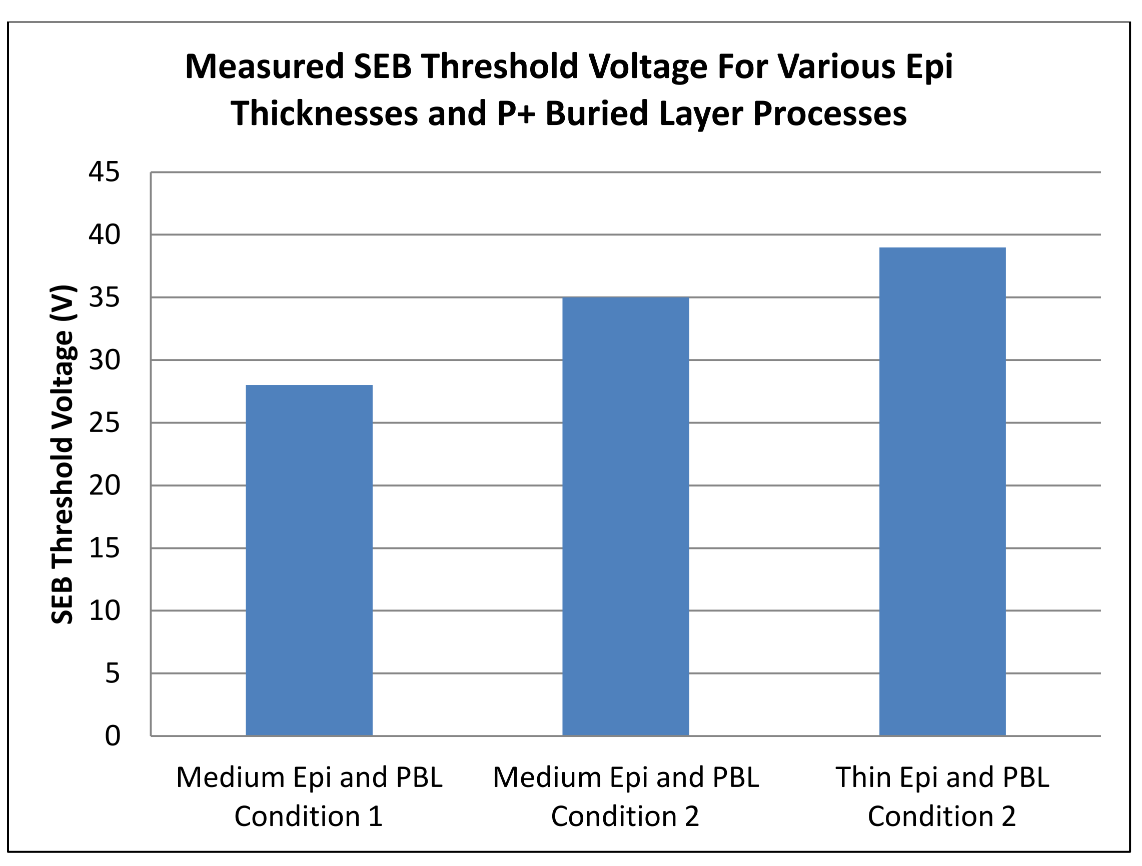
Measured SEB threshold voltage vs. drift length for second iteration designs with P+ buried layer. Longer drift length improve SEB safe operating area but also increases R_{DSON}. LET = 14 $MeV \cdot cm^2 \cdot mg^{-1}$

Figure 51: Measured SEB Threshold vs. Drift Length (Second Iteration)



Measured R_{DSON} and BV_{DSS} vs. Drift Length for second iteration designs with P+ buried layer.

Figure 52: Measured BV_{DSS} and R_{DSON} vs. Drift Length (Second Iteration)



Improvements in SEB safe operating area due to variation in epi layer thickness and P+ buried layer process conditions. LET = 14 $MeV \cdot cm^2 \cdot mg^{-1}$

Figure 53: SEB Threshold Voltage vs. Epi Thickness and P+ Buried Layer Implant

CHAPTER FIVE: 150 V SOI RESURF THIN FILM LDMOS

This chapter described the development of a medium voltage LDMOS power MOSFET, which is designed with resistance to single event radiation effects. Compared to bulk silicon, thin layer SOI substrates render LDMOS devices a considerably improved breakdown voltage vs. on-resistance trade-off due to the more ideal electric field distribution – the so called SOI Resurf principle [36]-[39]. This is especially true in the voltage range over 100 volts. In addition, the thin SOI layer significantly reduces the reverse recovery charge of the inherent body diode of the LDMOS device, further lowering the total switching power loss [10]. Furthermore, we hypothesize that the silicon volume affected by the heavy ion irradiation is limited to the thin SOI layer, resulting in a much reduced photo current and subsequently improved single event radiation hardness. Previous reports on the radiation response of SOI MOSFETs were primarily focused on TID effects, particularly on the buildup of radiation-induced trapped charge in the buried oxide (BOX) layer [40]-[44]. Most such literature focused on the response of SOI logic devices such as NMOS and PMOS, rather than higher voltage power devices such as LDMOS. No published studies specifically explored the heavy ion radiation response of SOI lateral power devices.

In this work, we focus on developing rugged LDMOS transistors on SOI substrate with very low gate charge which are optimized for MHz frequency switching applications and hardness against single event radiation effects. The concept behind this device is to improve the tradeoff between BV_{DSS} and R_{DSON} using the SOI Resurf effect, to minimize the charge collection volume during a heavy ion strike by using a thin SOI device layer,

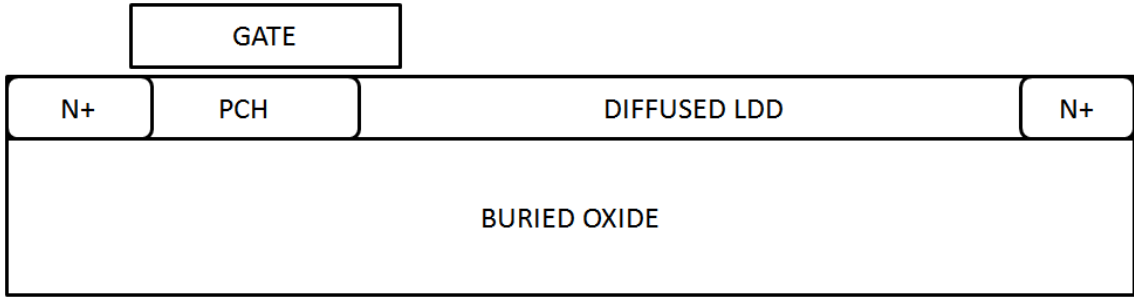
and to incorporate device features to enhance avalanche ruggedness and minimize gate charge.

Prior Art of SOI Resurf LDMOS

Figures 54 and 55 show two different prior art SOI LDMOS structures. The structure in Figure 54 is a classic ultra-thin film SOI Resurf LDMOS. Previous work on this type of SOI LDMOS was mainly focused on optimizing the tradeoff between BV_{DSS} and R_{DSON} based on the SOI Resurf principle [36]-[39]. Those works analytically defined the optimization of the lateral doping profile of the LDD region of the power MOSFET, where the heaviest LDD doping concentration occurs near the N+ drain, and the doping concentration is linearly decreased toward the source/drain p-n junction. This gives the theoretically optimal tradeoff between BV_{DSS} and R_{DSON} for an SOI LDMOS. Those structures were fabricated on thin SOI device layers, generally on the order of 100-200 nm thick. This allows the N+ drain to diffuse all the way to the buried oxide layer, thereby reducing the optimization of the LDD doping profile to a 1-D problem in the lateral direction. While this linearly-graded thin SOI LDMOS structure provides for the lowest possible R_{DSON}, the issues of gate charge, switching losses, and SOA were not discussed. It is thought that this type of device would not be very rugged, because the thin SOI device layer does not allow for a low resistance P+ body contact, thereby making the parasitic NPN bipolar transistor more susceptible to activation during avalanche.

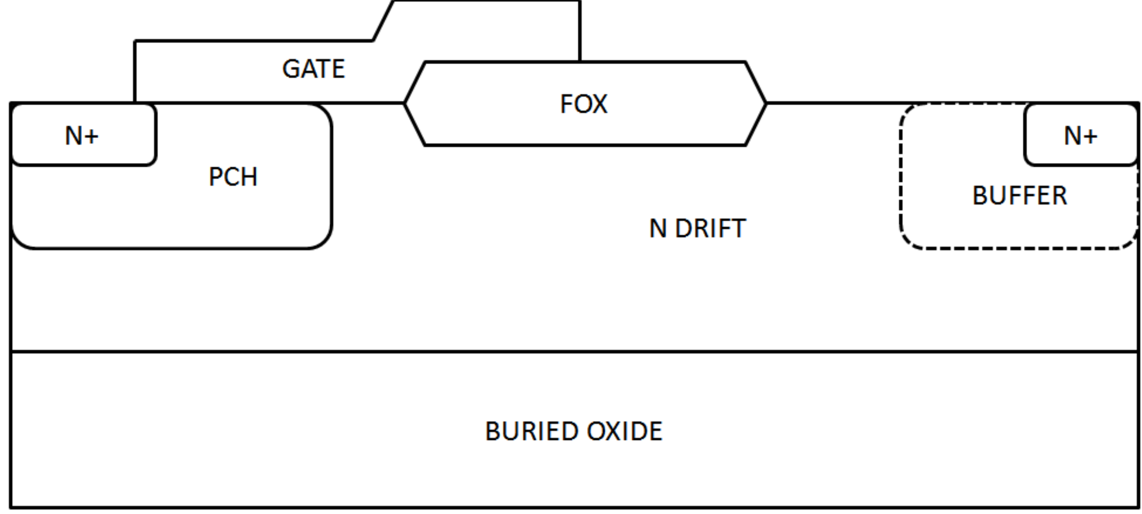
Some designs were also reported which focused on using “adaptive Resurf” and other techniques in order to form a rugged LDMOS, however those works also did not include gate charge or switching efficiency as part of the design optimization equations [45]-[48]. In fact, the switching efficiency of many of these LDMOS structures is assumed to be quite low, due to high Miller capacitance. This is because the popular LDMOS design requires the poly gate to double as a field plate, overlapping the drain region and thereby reducing the peak electric field between the drain and the gate oxide. Normally a thick field oxide is present between the poly gate and the drain, which helps limit the Miller capacitance to some degree but does not eliminate the penalty entirely. An example of such a structure is shown in Figure 55.

Note that the structure in Figure 55 uses a thicker SOI device layer than the ultra-thin film SOI LDMOS in Figure 54. This allows for the inclusion of two features which enhance avalanche ruggedness. Once is the deeper PCH region, which contains more charge and can be more heavily doped than the thin PCH region in the ultra-thin film transistor. This allows for a lower base resistance to suppress the parasitic NPN transistor. The second major feature to improve avalanche ruggedness is the N buffer around the N+ drain. This region is doped approximately one order of magnitude higher than the surrounding N Drift region. Its purpose is to prevent punch through into the N+ drain when the N drift region enters high injection during avalanche or bipolar activation.



Ultra-thin film LDMOS transistor. This device structure uses the SOI Resurf effect to produce a superior tradeoff between RDSON and BVDSS. The SOI Resurf effect allows the vertical component of the electric field to be sustained across the buried oxide layer. This design technique requires that the handle wafer underneath the buried oxide is fixed at a low voltage, usually the source voltage.

Figure 54: Ultra-Thin Film SOI Resurf LDMOS



This type of SOI device can be made very rugged against avalanche current, but it is thought that the gate charge is too high for efficient MHz frequency power switching applications. This device would suffer from high Q_{GD}, because of the large overlap between poly gate and the lightly doped N drift region. The inclusion of the drain buffer helps to improve avalanche ruggedness. This is the so-called “adaptive Resurf” design.

Figure 55: SOI LDMOS on N-Type SOI with Field Oxide and Gate Field Plate

Device Concept

Unlike previously reported ultra-thin film SOI Resurf devices, we use a relatively thick 1.0 μm p-type SOI device layer on top of a 1.0 μm buried oxide. The device features a P+ buried layer tied to the source and an N-buffer region surrounding the N+ drain, both of which are features intended to increase avalanche ruggedness. The STI oxide runs along a portion of LDD, and a source metal extension over the drift region acts a field plate to reduce the electric field between drain and gate. A cross-sectional drawing and SEM micrograph of the new SOI LDMOS are shown in figures 56 and 57 respectively.

The P+ buried layer is implanted at a depth near the buried oxide interface and tied to the P+ source using contacts spaced every 1 μm along the width of the transistor. This provides a very low resistance path to divert hole current away from the sensitive base-emitter junction of the parasitic NPN bipolar transistor. The SOI layer is sufficiently thick so that the vertical diffusion of the heavily doped P+ buried layer does not significantly affect the P-channel doping concentration near the surface. This allows for a "body-under-source" design [41] to eliminate back channel leakage, a TID effect commonly associated with SOI LDMOS. This also allows the design of the P+ buried region to be decoupled from the MOSFET threshold voltage to such a degree that the P+ buried layer can be degenerately doped.

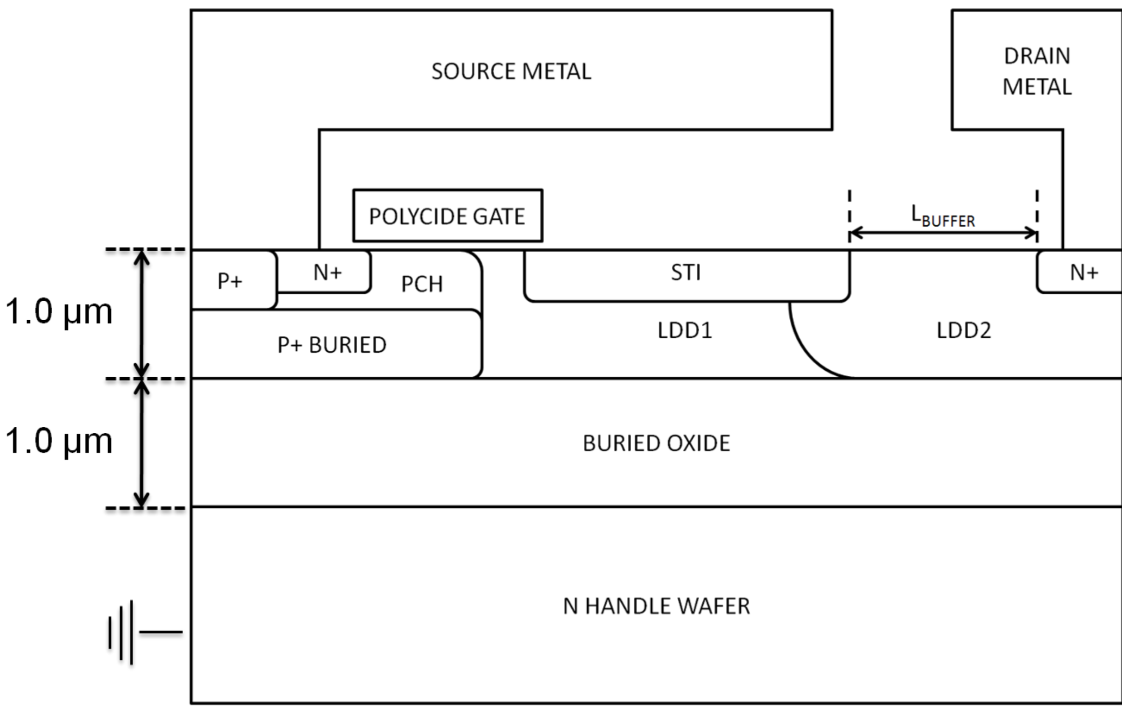
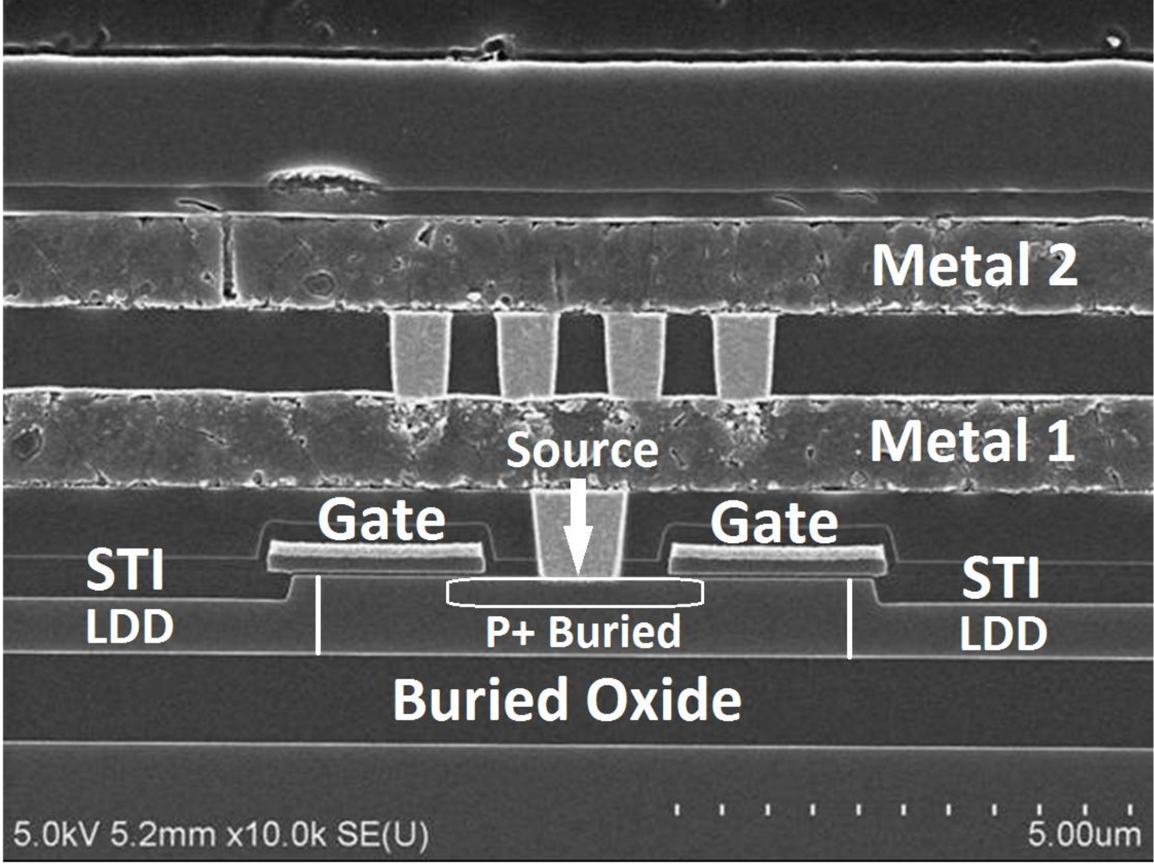


Figure 56: Cross Section Drawing of SEE-Hardened 150 V SOI Resurf LDMOS

The LDD region is formed differently from previously reported SOI LDMOS. In previous works, the lateral grading of the LDD doping concentration was achieved by patterning successively larger LDD implant windows from source to drain. In this device, two discrete LDD regions are patterned and then formed using different phosphorus implant doses. The LDD1 implant covers the entire drift region, while the LDD2 implant is patterned only in the portion of the drift region near the drain side. The doping concentration of the LDD2 region is defined by the sum of the LDD1 and LDD2 implant doses. After implant, the two LDD implants are driven together by a high temperature furnace anneal. The balance of LDD implant doses and patterning, in conjunction with the LDD drive, allows the lateral diffusion of the LDD implants to form

a near ideal linear grading of doping concentration in the lateral direction in accordance with the SOI Resurf principle.



This SEM cross section shows the source region and a portion of the drift region of the 150 V SOI Resurf LDMOS. The approximate locations of the N+ source and body diode p-n junctions are shown by thin white lines.

Figure 57: 150 V SOI LDMOS SEM Cross Section

A 0.35 μm thick TEOS-based shallow trench isolation (STI) runs underneath the drain edge of the polysilicon gate and along a portion of the lightly doped drain (LDD). Effectively, this creates a thin gate oxide between the gate and source but a very thick

oxide between the gate and drain. The primary purpose of the STI is to protect the device from SEGR by shielding the thin gate oxide from the high electric field between the gate and drain in the event of heavy ion irradiation. Taking into account the geometric relationship between the SOI device layer thickness and the LDD drift length, the STI is patterned in such a way as to prevent a heavy ion strike from directly shunting the gate oxide to the N+ drain. In the case of heavy ion trajectory passing across the STI region, the induced electric field across the gate oxide caused by the drain-gate shunt will be considerably reduced with the STI region sustaining a large portion of the drain-to-gate voltage.

As mentioned previously, STI is typically associated with TID effects such as parasitic drain to source leakage in MOS devices and integrated circuits. Since the STI region in our LDMOS has a race track layout pattern and is entirely contained within the LDD region of each transistor cell, it does not provide a leakage path directly linking the drain to the source of the LDMOS. No special processing techniques were used in this work to minimize charge trapping effects in the BOX or STI, although such processing techniques have been previously reported [49]-[51].

The shallow trench isolation (STI) is formed after the LDD drive, so a portion of both LDD implants are consumed by the STI process. In each design, the drift length and transistor cell pitch remain fixed, while the spacing between the STI and the N+ drain was varied. Increasing this spacing causes a greater amount of the LDD1 and LDD2 implant doses to be preserved in the silicon near the N+ drain, compared to the rest of the drift region. This more heavily doped LDD region acts as a buffer to suppress the so-

called Kirk effect and improve avalanche ruggedness. Prior work in LDMOS has established the effectiveness of such a buffer technique [45][46][48]. Studies involving heavy ion radiation in VDMOS have also established that such a buffer translates to improved SEB safe operating area [52].

In order to minimize Miller capacitance, we try to minimize both the gate-drain overlap and also the LDD doping concentration near the gate. Instead of being self-aligned, the LDD1 implant is patterned some distance away from the poly gate and then diffused laterally during the aforementioned drive. Extensive process simulations were performed to determine the proper spacing between the LDD1 implant and the poly gate to ensure that the drain-source p-n junction is formed on the source side of the STI but with minimal overlap of the poly gate. The location of this junction is also dependent on lateral diffusion of the P+ buried layer during the source-drain anneal. This process results in a very low LDD doping concentration underneath the poly, according to simulation.

To further minimize Q_{GD}, we avoid the use of the poly gate as a field plate over the drain, and instead we extend the source metal across a wide portion of the LDD. The source metal field plate affects BVdss differently depending on the ILD thickness and the length of the metal extension over the drift region, the mechanics of which are well described in previous literature. One effect of this design is that the STI is not necessary at all to achieve a high breakdown voltage, provided the LDD doses are tuned accordingly; however this precludes the formation of the N buffer and was shown to sacrifice ruggedness.

TCAD simulation was used extensively in the optimization of the design and process. A variety of designs were incorporated into a test mask array to explore design and process tradeoffs. Figure 58 shows some of the critical design dimensions associated with the 150 V SOI LDMOS Structure.

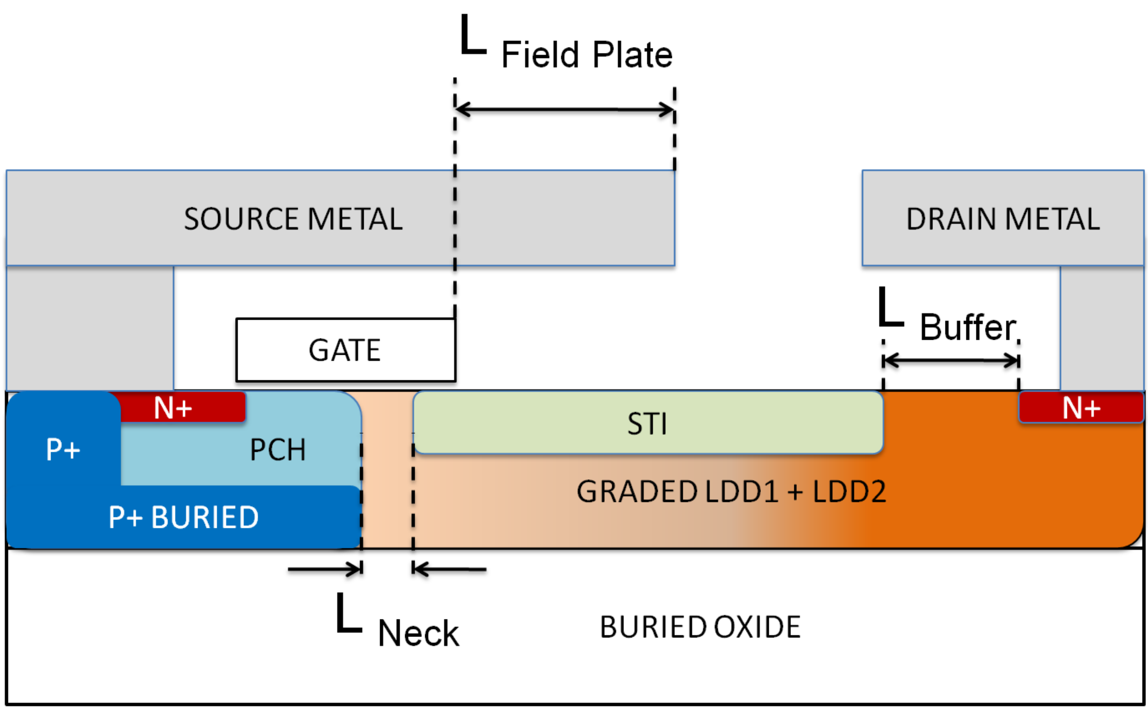


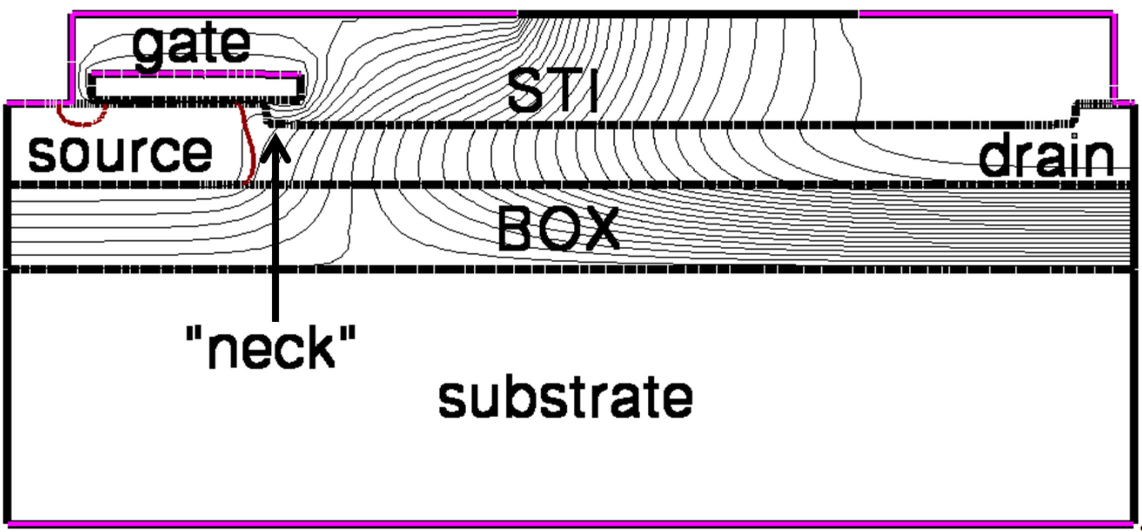
Figure 58: Critical Layout Dimensions of 150 V SOI Resurf LDMOS

Whereas the major tradeoff in designing the 25 V epi LDMOS was BV_{DSS} vs. R_{DSON}, the major electrical performance tradeoff for the 150 V SOI Resurf LDMOS is R_{DSON} vs. Q_G. The majority of this tradeoff occurs around the neck region of the MOSFET. L_{NECK}, denoted in Figure 58, is controlled by the combined patterning of the PCH, Gate, STI, and LDD masks, along with the time and temperature of the LDD drive. If L_{NECK} is made too small, then the conduction of electron current from the drain to the MOS channel will be inhibited, resulting in high R_{DSON}. If the neck is made too large, then Q_{GD} of the MOSFET will be unnecessarily high. The other critical dimension in determining Q_{GD} is the overlap of the source metal field plate over the drift region. The field plate length has a secondary effect on R_{DSON}, due to the change in metal interconnect resistance along the first layers of drain and source metal, but the primary impacts of the field plate are on BV_{DSS} and Q_{GD}. There is an optimal field plate length corresponding to the device geometry and LDD doping profile. BV_{DSS} is strongly influenced by not only the length of the field plate, but also the vertical distance between the field plate and the silicon surface. In this experiment, we did not vary the thickness of this interlayer dielectric, but prior literature has documented the effect [53].

L_{BUFFER} has a primary effect on both BV_{DSS} and avalanche ruggedness and a secondary effect on R_{DSON}. The buffer length must be tuned together with the two LDD doses and LDD drive conditions, as well as the field plate length, to achieve the desired combination of BV_{DSS} and avalanche ruggedness.

Figure 59 shows the simulated potential contours of a typical design at 150 V. The substrate is grounded to the source, and the vertical electric field component between

drain and source is is sustained across the buried oxide layer. For a device rated at 150 V, the peak electric field across the 1 μm buried oxide is 1.5 mV/cm. This is well below the expected critical electric field of the buried oxide, which is estimated to be between 5 – 10 MV/cm.



Simulated equipotential contours of the SOI LDMOS biased at V_{DS} = 145 V and V_{GS} = -16 V. The spacing between potential lines indicates the strength of the electric field. Closely spaced lines indicate a stronger field. The inclusion of the source metal field plate overhanging the drift region, along with the STI field oxide, helps to prevent the high electric field in the neck region from limiting the avalanche voltage of the MOSFET.

Figure 59: Simulated Equipotential Contours of SOI LDMOS at V_{DS} = 150 V

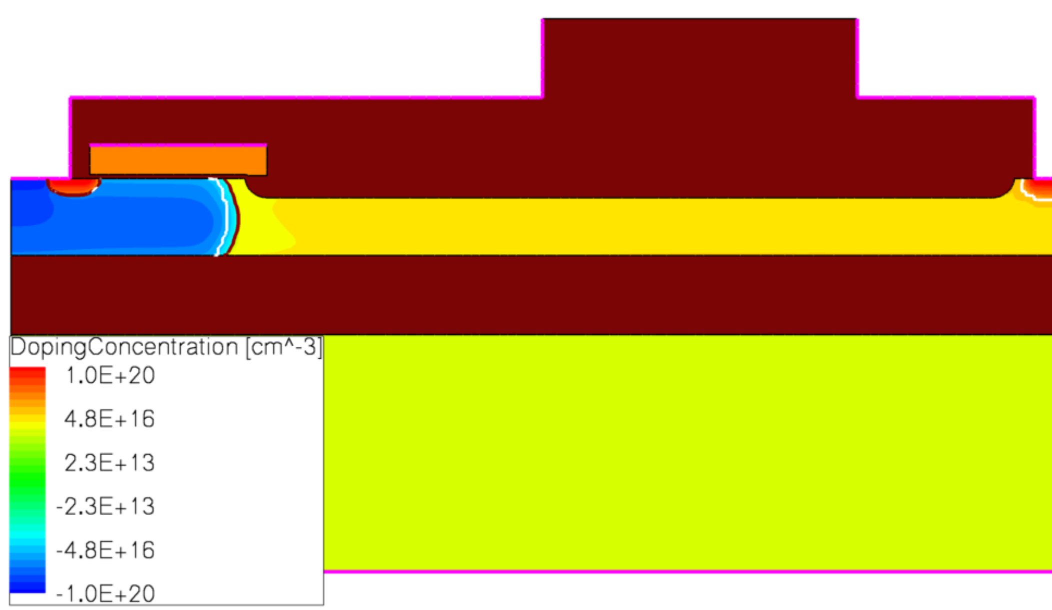


Figure 60: Simulated Doping Concentration
of 150 V SOI Resurf LDMOS Without Buffer

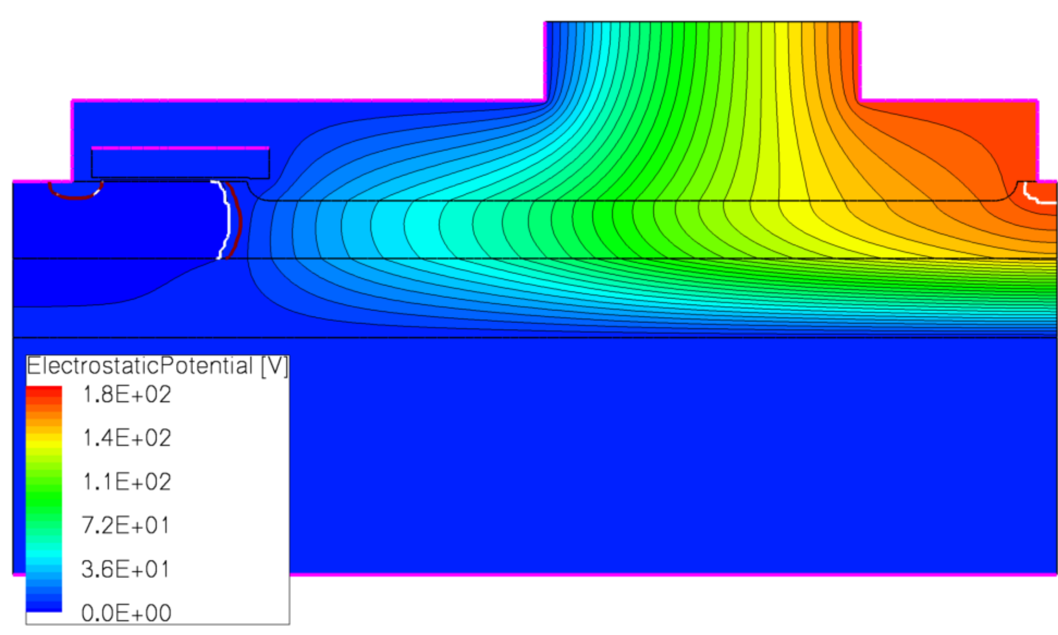


Figure 61: Simulated Electrostatic Potential Lines at Avalanche Breakdown
for SOI LDMOS Without Buffer

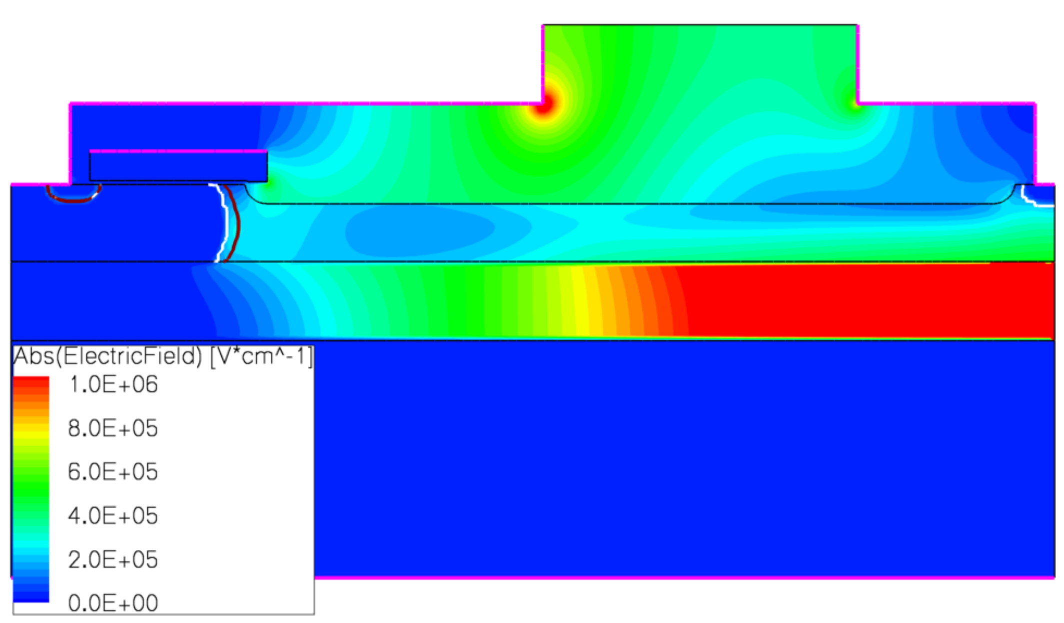
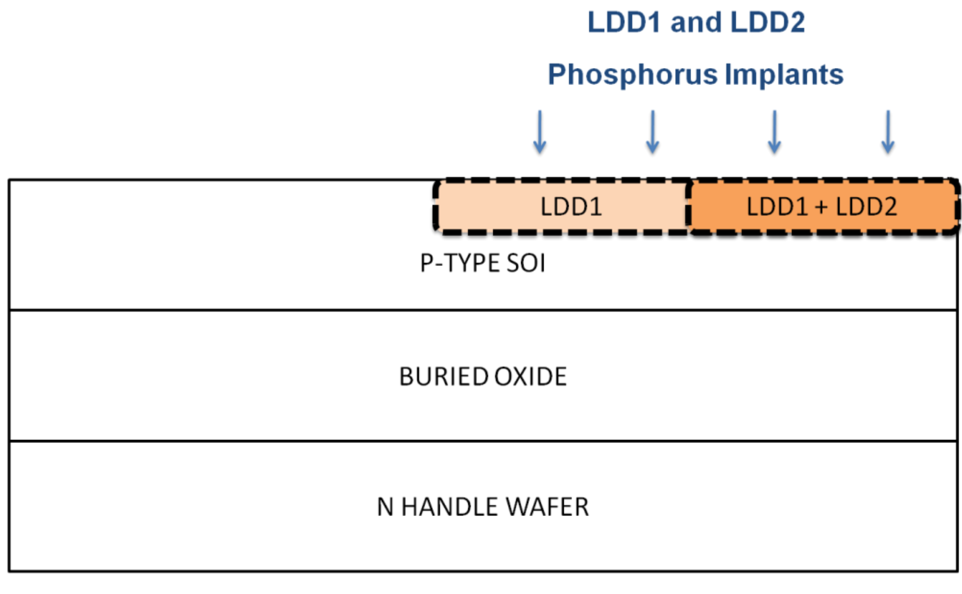
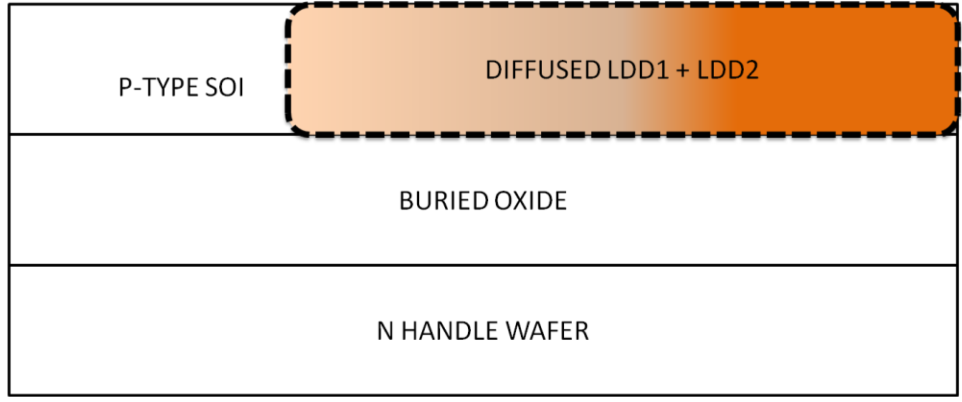


Figure 62: Simulated Electric Field Magnitude During Avalanche Breakdown for SOI LDMOS Without Buffer

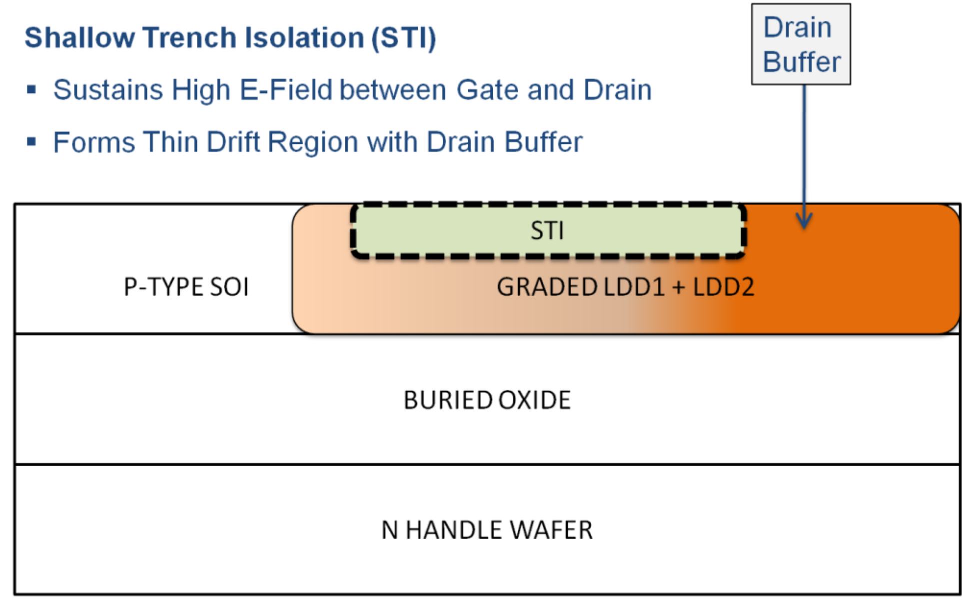
Fabrication Process



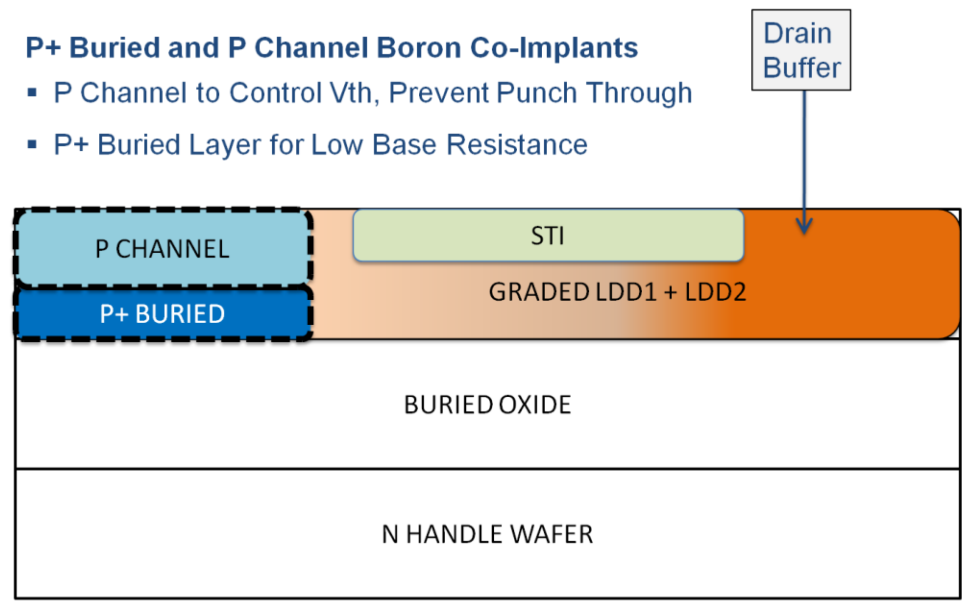
(a)



(b)



(c)



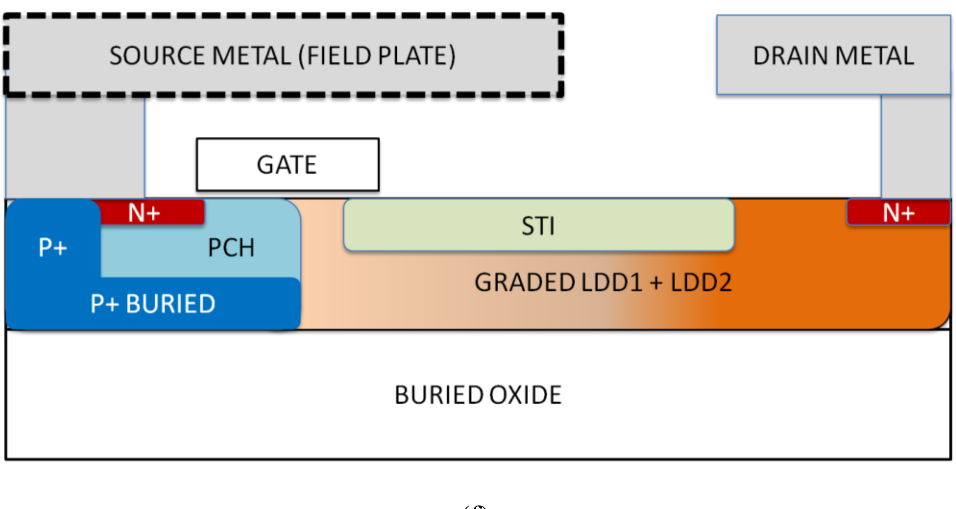
(d)

- Thermal Oxidation (Gate Oxide)
- Polycide Gate Patterning
- N+ Source and Drain Implants
- P+ Source Implants
- Furnace Anneal

Drain Buffer
GATE
N+
P+
PCH
STI
N+
GRADED LDD1 + LDD2
P+ BURIED
BURIED OXIDE

(e)

- Contacts and First Metal



(f)

Figure 63: 150 V SOI Resurf LDMOS Fabrication Process Flow

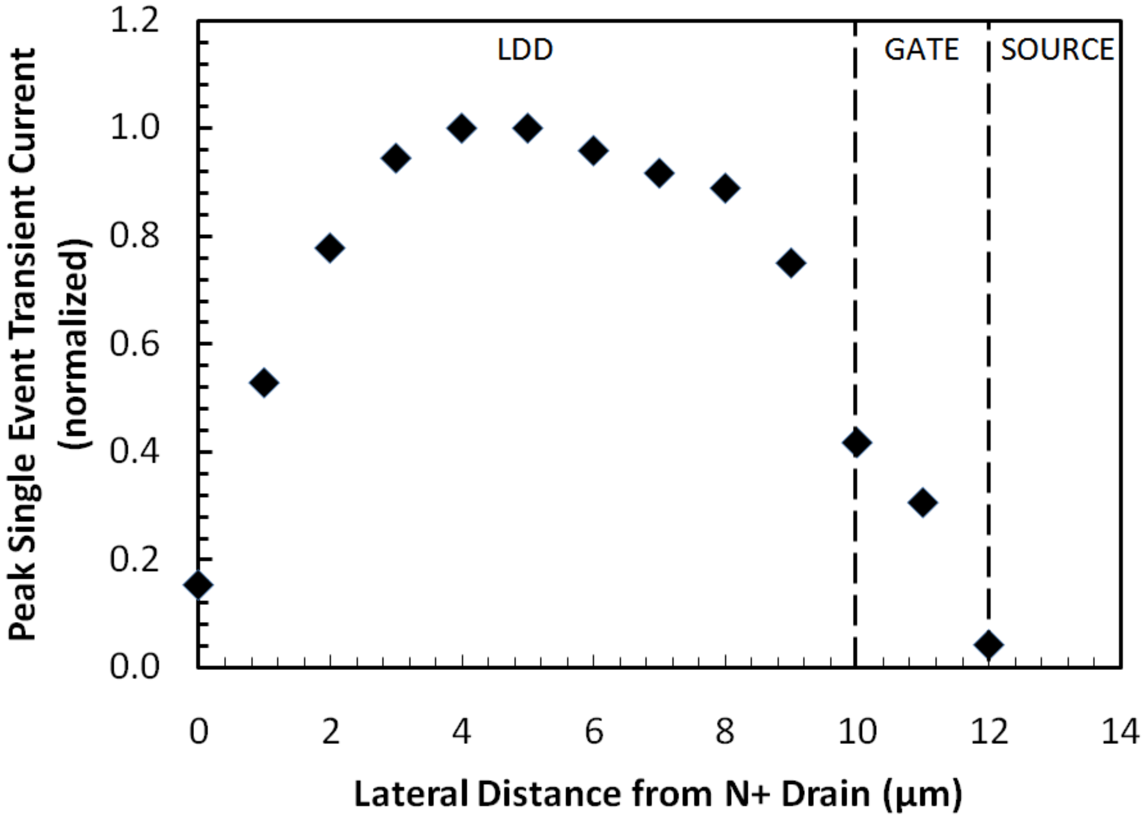
SEE Modeling

2D device simulations were conducted with Sentaurus TCAD using the built-in heavy ion radiation model. The goals of these simulations are to gain a fundamental understanding of the mechanisms which might cause SEB within the device and to predict whether the SEE hardening features offered the intended capability. In order to accomplish these goals, the time evolution of the heavy ion event was observed in a method similar to the 25 V LDMOS.

Because the SOI device layer is only 1.0 μm thick, accurate modeling of the exact location of the Bragg Peak was not deemed necessary, and the simulations instead assume a constant LET along the length of the ion track. The ion track penetrated the entire simulated device structure, through the top silicon device layer, into the buried oxide, and completely through the substrate. The LDMOS source terminal and the bottom of the N-type substrate each have their own electrodes in the simulation, with both being set to ground potential, so that displacement current within the substrate could be independently monitored. It was quickly determined that the magnitude of the displacement current was insignificant compared to the total drain to source current during the single event transient.

The initial series of simulations focused on characterizing the sensitivity of the device to strikes at different locations along the lateral device structure. The goal was to determine at which location a strike would produce the largest single event transient or was most likely to induce SEB. This location would then be used as a worst-case

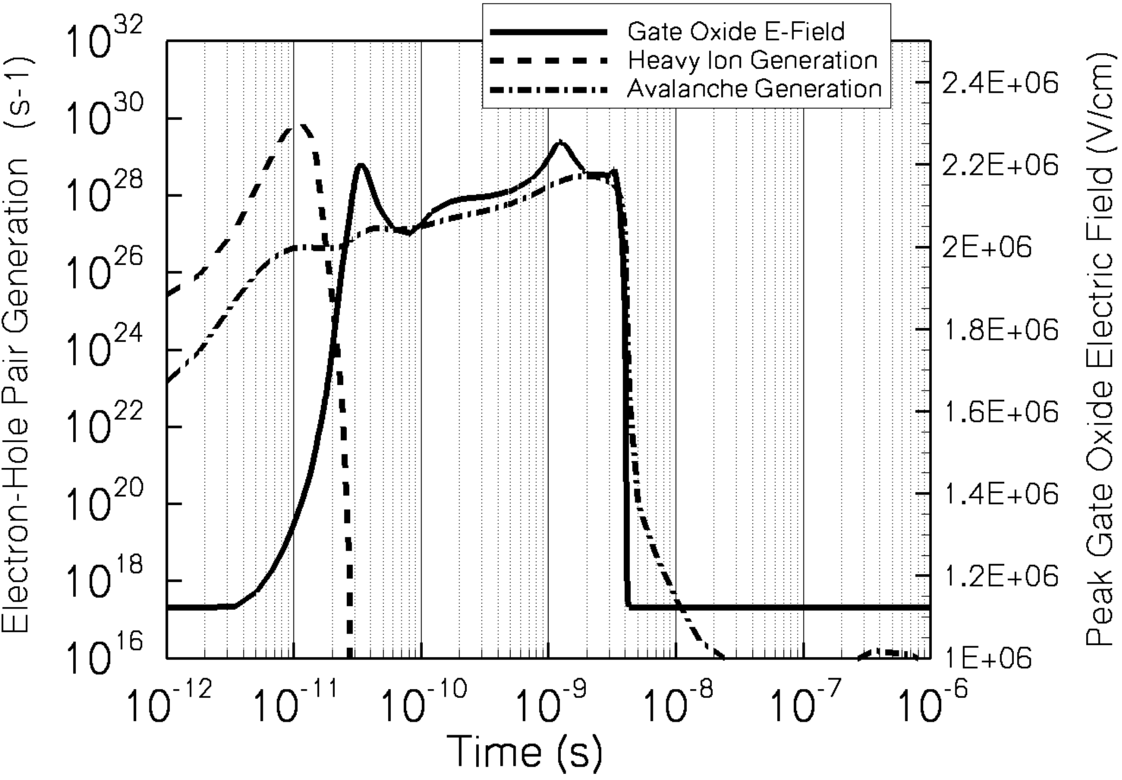
coordinate for subsequent simulations, as a control, in order to explore the effects of other variables such as LET and various bias conditions. The results shown in Figure 64 illustrate, in the case of a strike normal to the silicon surface, that the device is most vulnerable near the center of the LDD region. It should be noted that the peak current shown in Figure 64 follows the same trend as the total collected charge for each simulated event.



Initial series of simulated single event transients for heavy ion of LET = 87 MeV·cm2/mg striking different locations along the lateral device structure. This laid the groundwork for subsequent series of simulations, which investigated the sensitivity of the LDMOS to more complex heavy ion trajectories.

Figure 64: Simulated SOI LDMOS Sensitivity to Ion Strike Location

In order to determine the spatial distribution of the electrical stress during the single event transient (SET), we first observed the SET waveform to determine the time at which the peak stress occurred. During each solve iteration, the simulator calculated and recorded the magnitude of the peak electric field in four distinct insulating regions of the device – the gate oxide, the STI, the BOX, and the interlayer dielectric. An example of a commonly observed transient response is shown in Figure 65. This plot includes heavy ion charge generation, avalanche charge generation, and peak gate oxide electric field. The charge terms are integrated throughout the entire device structure.



Peak electric field across the gate oxide was calculated automatically by the simulation. The Heavy Ion Generation and Avalanche Generation are integrated throughout the silicon device layer.

Figure 65: Simulated Single Event Transient Waveform

In each simulated case, the total collected charge was several orders of magnitude higher than the charge deposited by the ion. Avalanche generation accounted for nearly all of the collected drain to source current. The peak electric field in the gate oxide has two distinct peaks, each corresponding to different influences. The first peak occurs around 50 picoseconds, shortly after the initial deposition of heavy ion charge. The second peak occurs near 1 ns and coincides with the peak generation of avalanche charge. This "twin peaks" waveform of the gate oxide electric field was characteristic of all simulations where the ion trajectory passed through the middle of the LDD region.

Once the magnitude and time of the peak transient electrical stress was known, we observed the 2-D device cross section that had been generated during the solve iteration corresponding to the time of interest. This allowed us to determine the exact spatial distribution of electrical stress within the device. The peak electric field in the gate oxide occurs in the "neck" region, where the poly gate overlaps the STI and the LDD. This is a region normally associated with high electric fields in LDMOS devices, where the gate and drain are strongly coupled. As the depletion region is perturbed by the deposition and collection of heavy ion charge, the fixed potential at the gate creates a boundary at which no further depletion of the LDD can occur, resulting in high transient electric field stress during the heavy ion event.

The final series of simulations explores the effects of angled ion strikes to investigate whether device stress is dependent on total deposited charge, ion angle of incidence, or some combination of both. In each of the simulated conditions, the ion trajectory is oriented around the center point of the LDD region, as shown in Figure 66.

Effective LET provides a measure of total deposited charge and is calculated as LET / cos(θ), where theta represents the angular difference (in degrees) between the ion trajectory and a line normal to the silicon surface.

TCAD includes the necessary charge transport models to simulate the SEB failure mechanism. TCAD is not so well suited toward the prediction of SEGR or microdose effects, since more fundamental atomic-scale physics are involved in those failure mechanisms. Therefore only a relative comparison of gate oxide electrical stress for various heavy ion conditions is presented as an indicator of possible susceptibility to damaging effects in the oxide.

Figure 67 shows the simulated peak current density during ion strikes at various angles of incidence. SEB appears primarily dependent on the total deposited charge (LET_{EFF}), independent of the normal ion LET. It should be noted that the simulator predicted a worse SEB safe operating area (SOA) than was demonstrated in the experimental data. These simulations should not be taken as an accurate prediction of expected real-world SOA, but instead serve only to illustrate a general trend in the relationship between SEB, deposited charge, and ion angle of incidence. Further experimental investigation would be required to calibrate the TCAD model to predict a real world safe operating area with any degree of confidence.

Figure 68 shows the simulated peak electric field in the gate oxide during the same set of simulations shown in Figure 67. The plotted electric field is the first peak of the characteristic transient electrical stress waveform described previously and shown in the example waveform in Figure 65. This peak is strongly associated with the initial

distribution of heavy ion generated charge and initial collapse of the depletion region, occurring prior to the majority of avalanche generation and before the activation of the parasitic NPN bipolar transistor.

The simulations show that the magnitude of the gate oxide electric field is closely associated with the heavy ion angle of incidence. For simulated strikes with the same deposited charge but different angles of incidence, the simulator predicts that a steeper angle of incidence will produce a higher electric field in the gate oxide. Gate oxide electrical stress is consistently higher during ion strikes that occur at shallower angles. One possible explanation of this is due to the positioning of the deposited charge relative to the gate oxide. More charge is deposited near the gate during an angled strike. However, no significant change in electric field is observed for ions of different LETs at the same angle of incidence, until the strike actually intersects the gate, which is only the case in a simulated 76 degree angle. This trend indicates that there may be a stronger coupling of the gate and drain, as the ion angle becomes steeper and penetrates into zones of higher potential in the drift region.

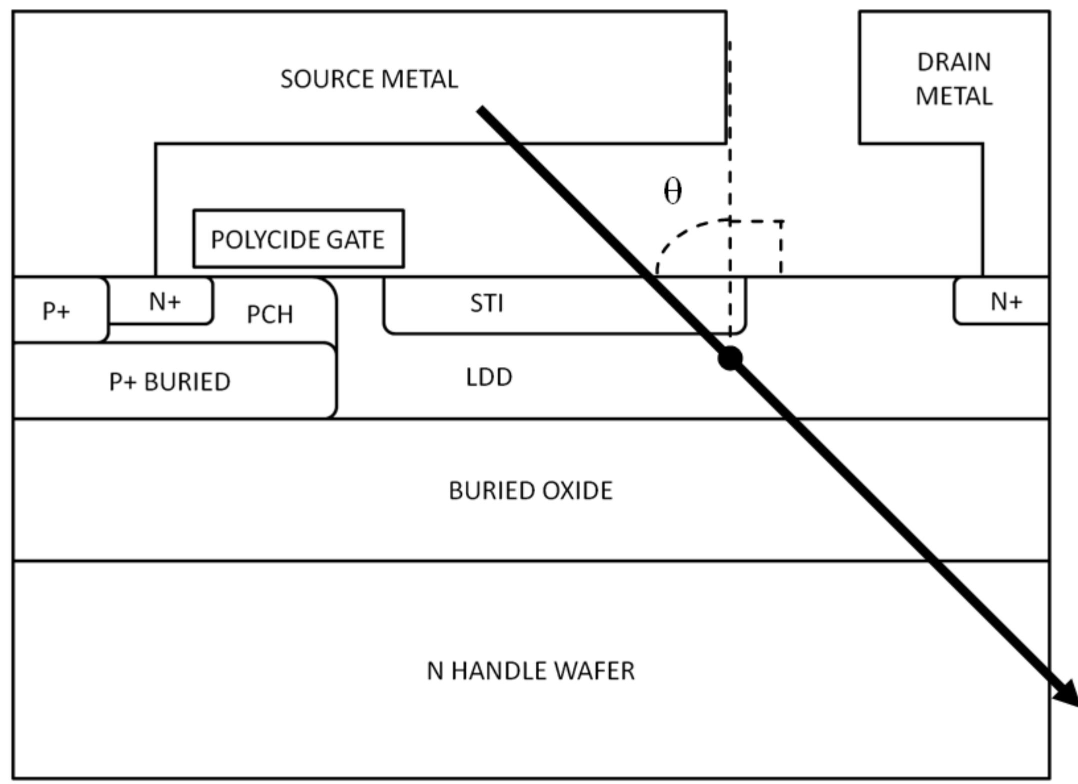
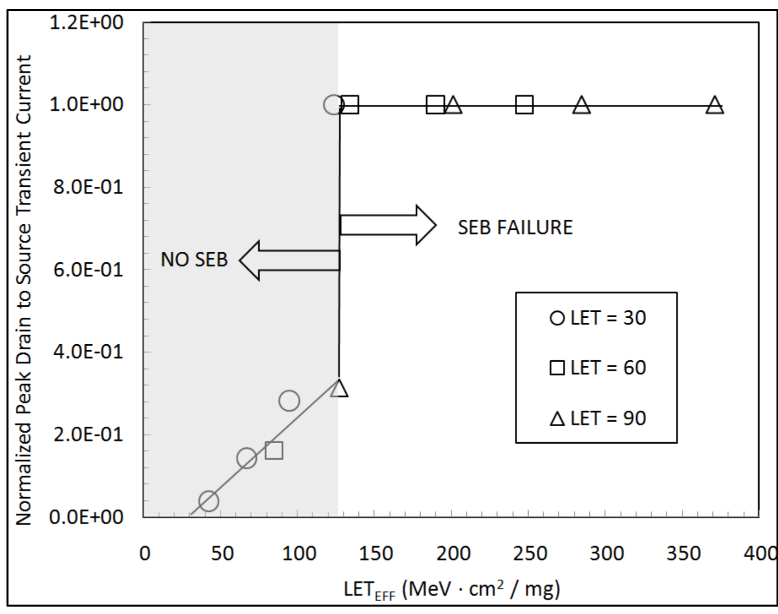


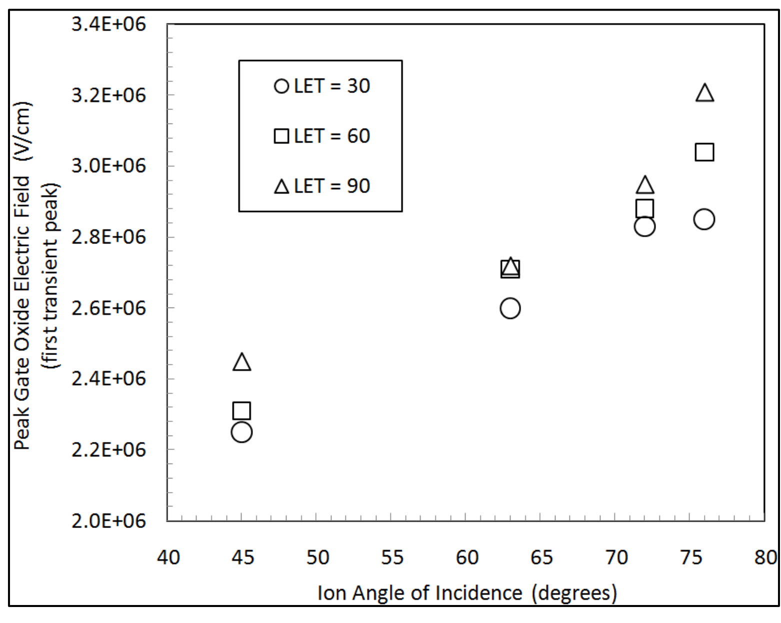
Diagram illustrating the modeled heavy ion trajectory for strikes at varied angles of incidence passing through the center point of the LDD region.

Figure 66: Diagram of Heavy Ion Angled Trajectory



Simulated magnitude of peak current density vs Effective LET for different LET ions. VDS = 120 V, VGS = 0 V.

Figure 67: Simulated 150 V SOI LDMOS SEB Safe Operating Area



Simulated magnitude of gate oxide electric field vs. ion angle of incidence for different LET ions. VDS = 120 V, VGS = 0 V. Steady state gate oxide electric field = 1.1×10^{6} V/cm.

Figure 68: Simulated Gate Oxide Electrical Stress vs. Ion Angle of Incidence

Analysis of SEB Failure Mechanism

Figure 69 shows the simulated transient current waveforms of the LDMOS device during heavy ion irradiation with a passing case observed at VDS of 120V but a failing case at VDS of 150V. In the passing case, the transient drain to source current recovers to zero quickly after the ion strike, whereas the transient current becomes self-sustaining in the failing case. Snapshots of internal physical quantities are plotted in Figure 70 to better illustrate the time evolution of the electric field and avalanche generation during a heavy ion strike. These simulations are for strikes within the LDD, which the simulator predicts is the most sensitive region of the SOI LDMOS structure in terms of inducing SEB.

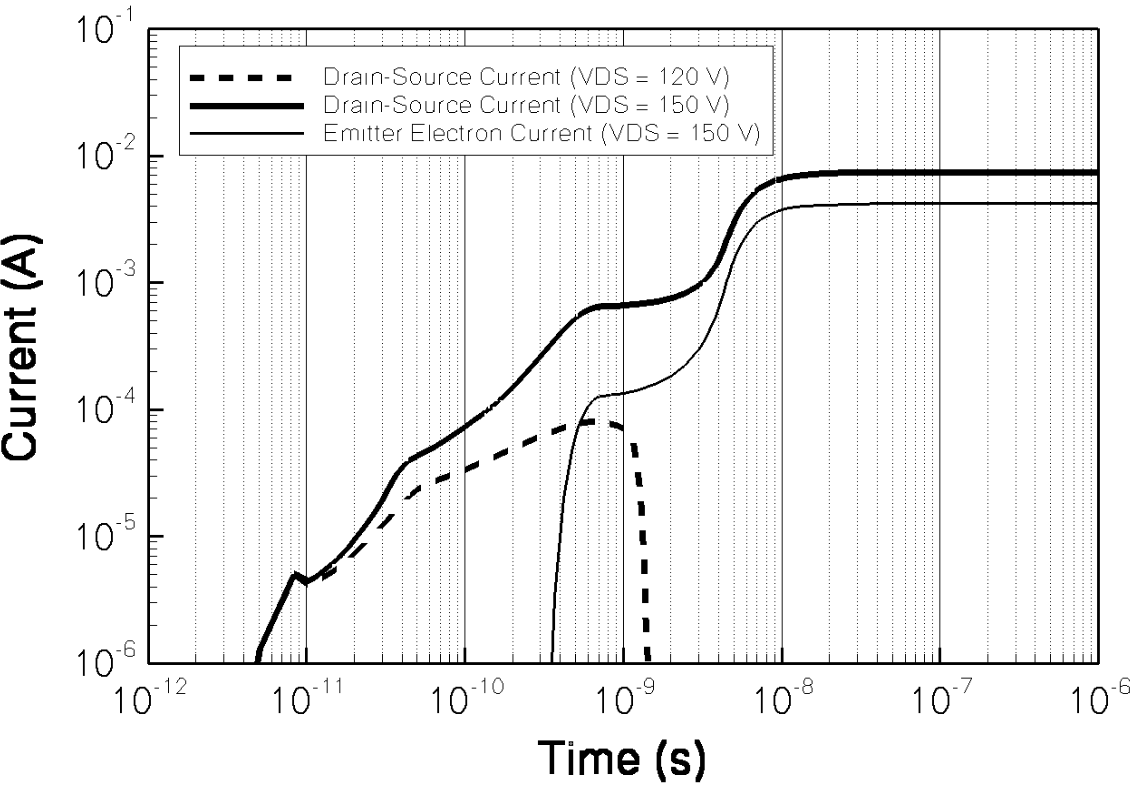
Heavy ion charge generation peaks at 10 picoseconds. Shortly afterwards, a wide portion of the space charge region collapses near the strike location due to the large number of mobile carriers generated by the incident ion. These generated electrons and holes are swept laterally toward the drain and source terminals respectively. Because the depletion region in the center of the LDD has collapsed, the electric field is redistributed to either edge of the drift region, near areas of fixed potential, including the highly doped N+ drain, the P+ buried source layer, and the LDD region immediately adjacent to the poly gate. The resulting high electric fields at both lateral ends of the LDD generate high levels of impact ionization near the N+ drain diffusion and near the source/drain p-n junction, that is, the base/collector junction of the parasitic bipolar transistor, underneath the poly gate. This spatial distribution of electric field and avalanche generation is shown

at time = 100 ps in Figure 70. This corresponds to the first characteristic transient peak in the gate oxide electric field, shown in Figure 65.

Avalanche generation typically reaches a peak near time = 1 ns. This peak in avalanche generation corresponds in time to the second peak in the characteristic gate oxide electric field waveform. At this time, the activation of the parasitic bipolar transistor is observed in most simulated cases, passing or failing. Forward-active NPN conduction is indicated by a sharp increase in the electron current flowing through the N+ source/emitter electrode. The temporary activation of the parasitic BJT by itself does not necessarily lead to SEB failure. Nevertheless, it is advantageous to suppress the NPN BJT by including a P+ buried layer to assist in recombining the electrons injected from the N+ source, reducing the gain of the NPN BJT, and allowing the device more time to collect the avalanche-generated charge as the depletion region is re-established.

Near 5 ns is the most critical time for the device, in which sufficient levels of avalanche generation can drive the device into a sustained bipolar operating mode, resulting in SEB. Near this time, the BJT operation of the passing case in Figure 8 starts to diminish, and the depletion region begins to be re-established to support the V_{DS} voltage without creating a high electric field in the device. However, for the failing case shown in Figure 8, its BJT operation is not only sustained but also enters into a second breakdown mode. This is because the very high BJT collector current causes a redistribution of the electric field in the depletion region, creating a new peak electric field region ("hot spot") near the N+ drain. The new "hot spot" induces more avalanche generation, which in turn reinforces the BJT operation. This is the so-called Kirk effect,

wherein the collector is operating in a high injection regime, and the depletion region extends all the way to the N+ drain diffusion. The inclusion of a drain buffer helps to suppress this effect, by preventing the depletion region from punching through to the N+ drain and thereby reducing avalanche generation in the collector. In cases where stresses are sufficient to extend the depletion region into the N+ drain, the device is unlikely to survive.



Simulated SEE transient current waveforms for passing and failing cases. These cases are for the same ion LET and trajectory, simulated at two different drain to source voltages. Strong activation of the parasitic NPN bipolar in the failing case (VDS = 150 V) is indicated by a sharp rise in emitter electron current.

Figure 69: Simulated Single Event Transient and Single Event Burnout Waveforms

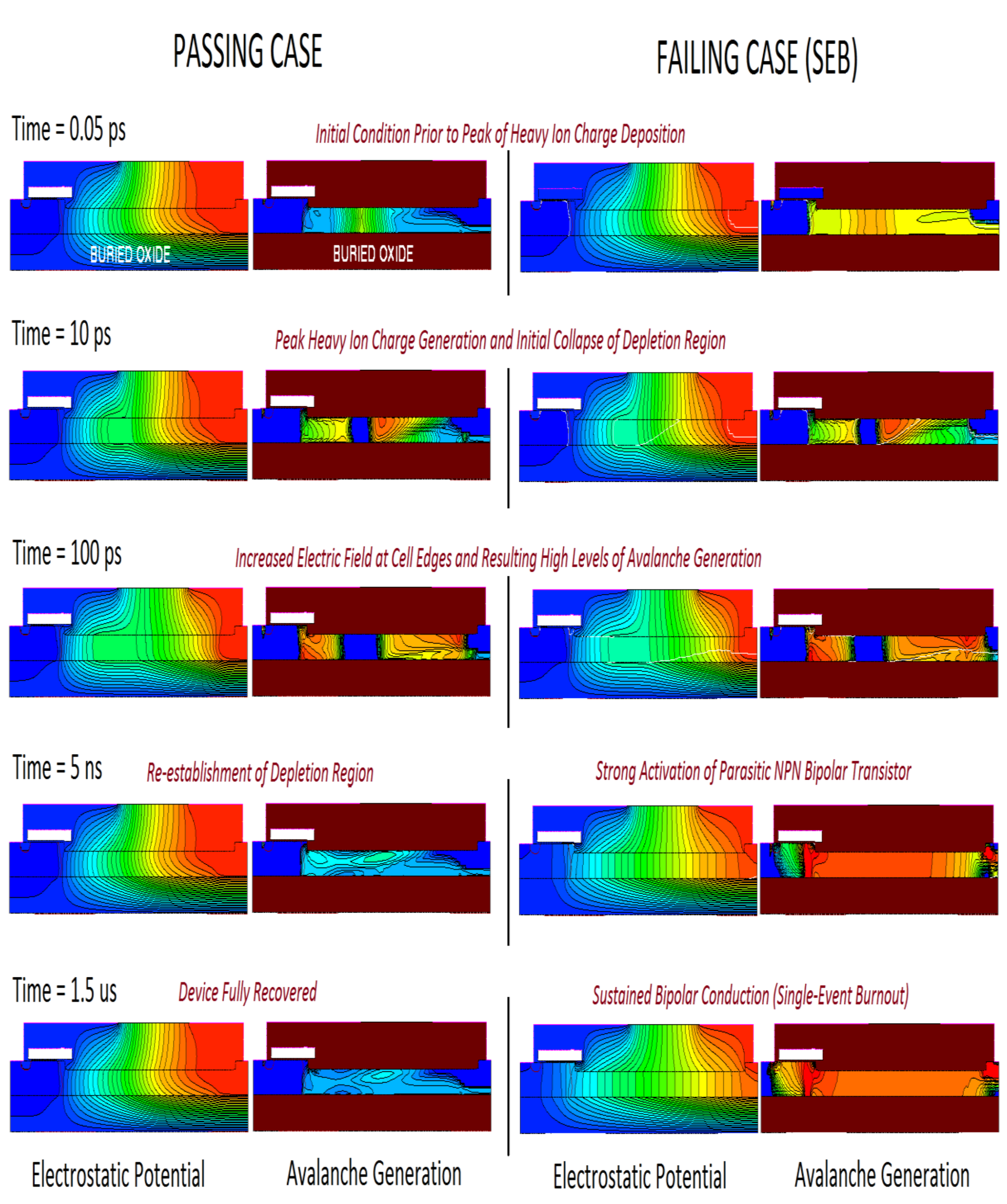


Figure 70: 150 V SOI LDMOS Time Evolution of Heavy Ion Strike and Single Event Burnout

Experimental Results

Devices were fabricated in a 0.35 μm CMOS foundry on a SmartCut® SOI substrate. Device performance varied across a wide range of designs and process conditions using a test element group mask of 34 different designs, and a wafer lot containing 25 process splits. DC electrical characterization was performed on-wafer using a FET tester, and the probe data was analyzed to select candidate samples for UIS testing and AC characterization. SEE Testing was conducted on pre-screened samples which were wirebonded and mounted on evaluation boards with the top of the surface exposed to the air.

DC and AC Electrical Characterization

Figure 71 shows the BV_{DSS} curve for a design without drain buffer, with a measured BVdss = 180 V. BV_{DSS} of a design which included the drain buffer was 165 V. Figure 72 shows the measured forward I-V characteristics of the same device. R_{DSON} values measured at Ids = 4 A and Vgs = 8V, 10V, and 12V were 115 mΩ, 109 mΩ, and 102 mΩ respectively.

The device is designed with very low gate-to-drain charge and reverse recovery charge in order to improve switching efficiency at MHz switching frequencies. Figure 73 shows the typical gate charge waveforms. Q_{GD} for this design is only 0.8 nC measured at

Ids = 4 A, Vds = 72 V and Vgs = 8 V. Figure 74 shows the reverse recovery current waveform.

Even with the inclusion of the P+ buried layer and drain buffer, ruggedness varied across a wide array of designs and processes. A strong relationship was noted between the LDD dose and UIS capability, as shown in Figure 75. Self-driven UIS current was limited to 45 A, using the JEDEC UIS test method with a 25 Ω gate to source resistor. Separate UIS testing without the gate resistor displayed an avalanche current capability of 73 A without failure, at a peak voltage of 230 V.

Table 4 summarizes basic device performance of the SOI LDMOS as compared to a state of the art 150 V commercial trench power MOSFET [54] and a 150 V rad-hard VDMOS [55]. The SOI LDMOS device demonstrates a specific on-resistance of 918 $m\Omega \cdot mm^2$. Although modern power trench MOSFETs typically offer a higher cell density and a lower area-specific on-resistance, the significantly smaller gate charge of the LDMOS more than compensates for this disadvantage and results in an electrical performance figure of merit (FOM) $Q_{GD} \times R_{DSON}$ of 37% better than the trench MOSFET and 20x better than the rad-hard VDMOS. This FOM directly indicates the total MOSFET power loss including conduction, switching, and gate drive power losses. Additionally, the smaller reverse recovery charge (Q_{RR}) of the SOI LDMOS offers a further advantage in reducing switching losses, which is not accounted for in the figure of merit.

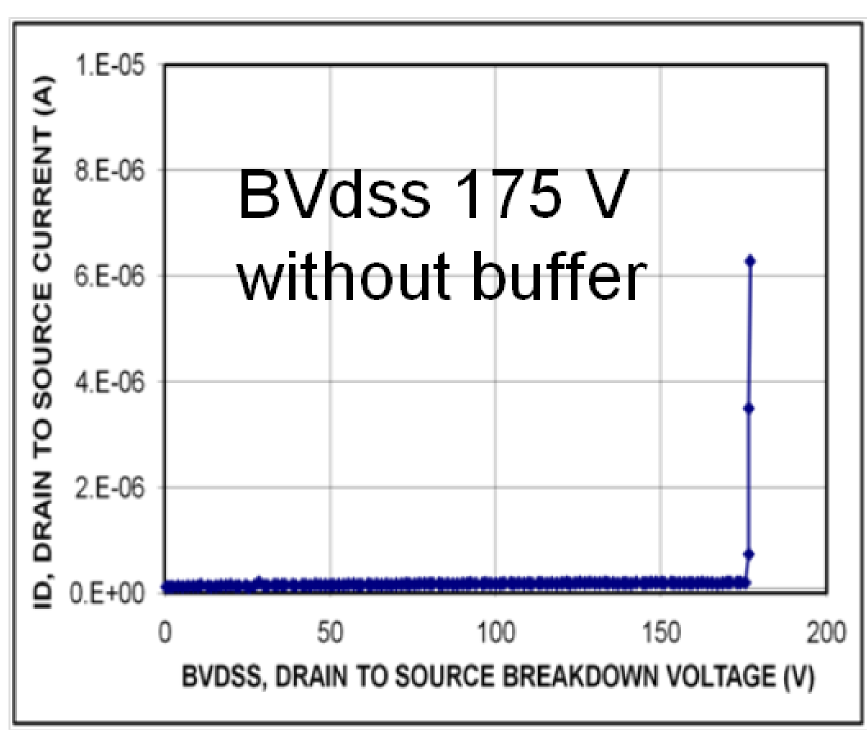


Figure 71: Measured BV_{DSS} of SOI Resurf LDMOS

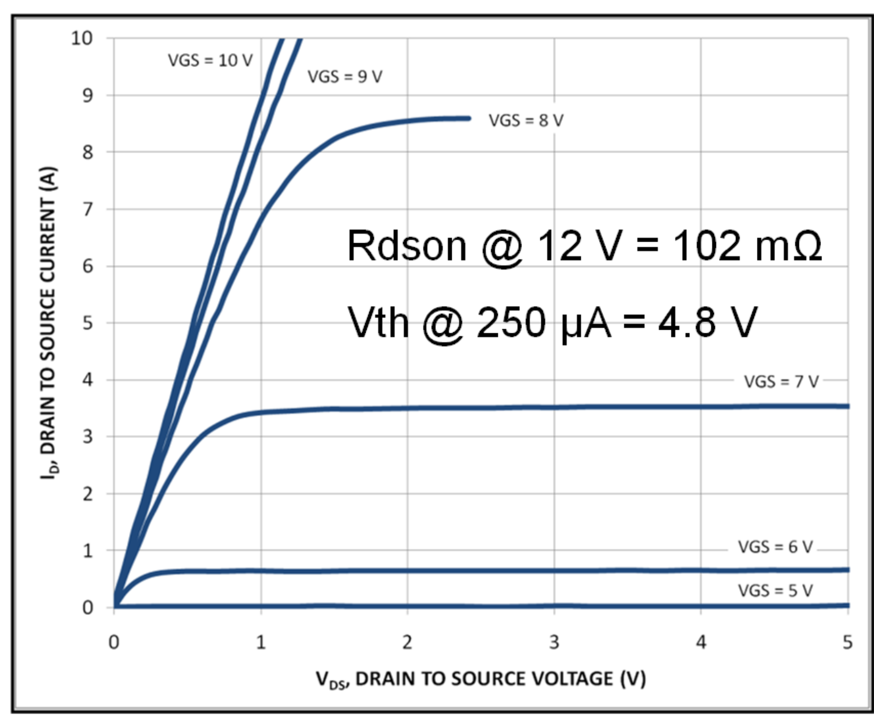


Figure 72: Measured Forward IV Characteristic of SOI Resurf LDMOS

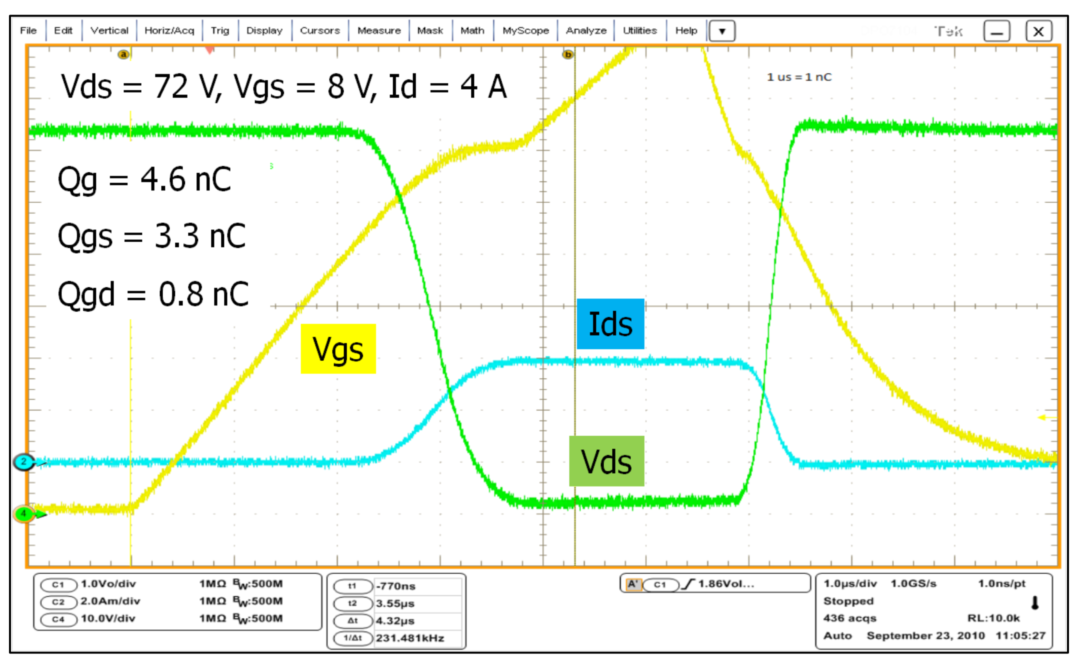


Figure 73: Measured Gate Charge Waveform of SOI Resurf LDMOS

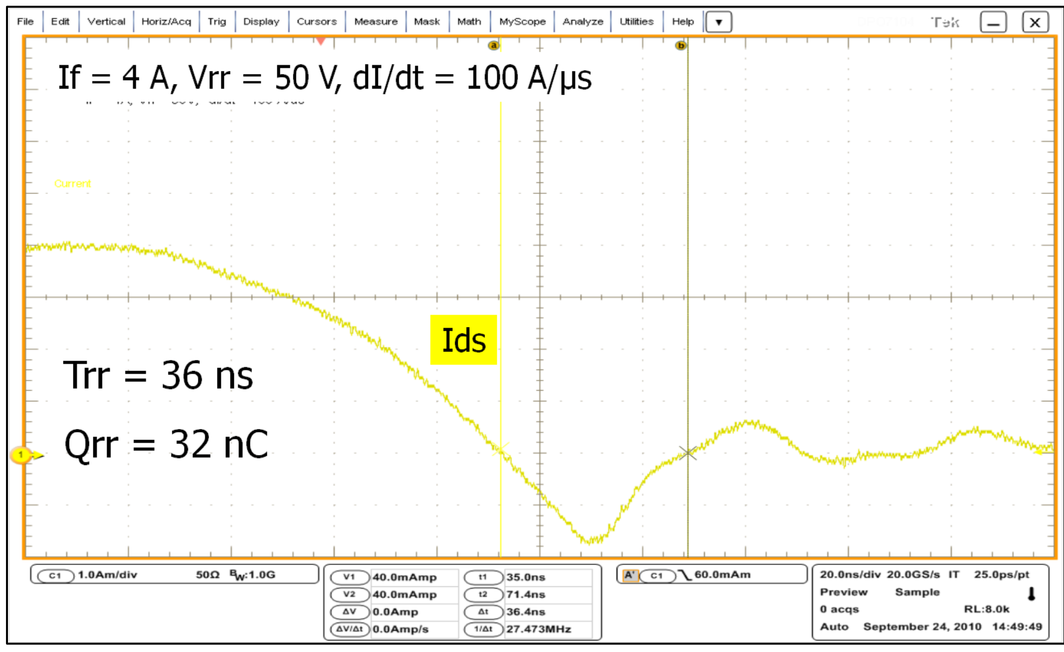


Figure 74: Measured Body Diode Reverse Recovery Waveform of SOI Resurf LDMOS

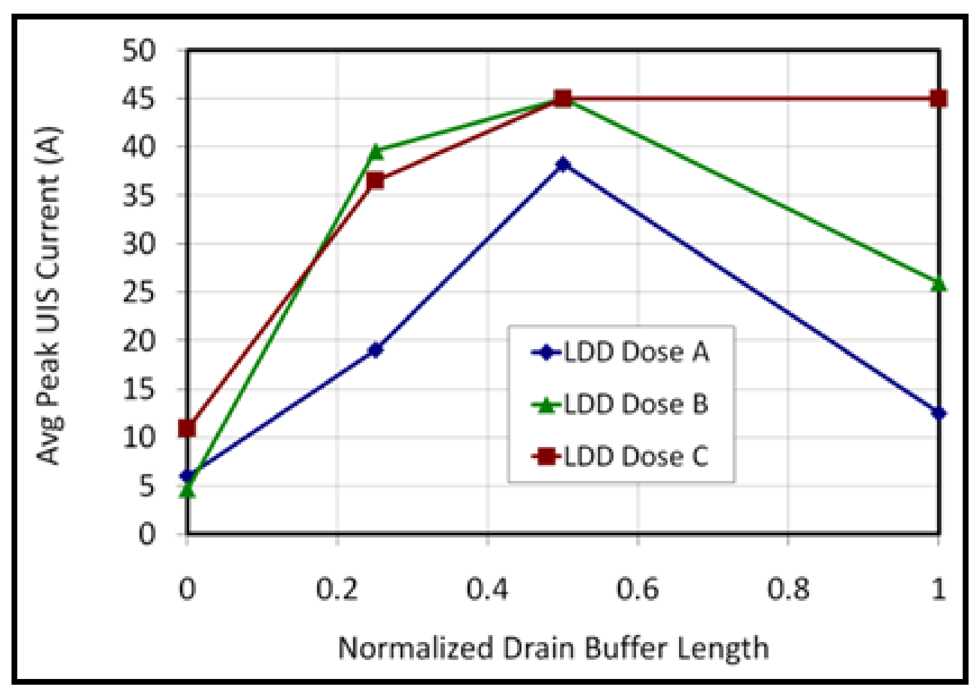


Figure 75: Measured UIS Current vs Drain Buffer Length for Various Process Splits

Table 4: Key Electrical Parametrics: Comparison Against Modern 150 V Power MOSFETs

Parametric	**This Work**	**150 V Commercial Trench VDMOS [54]**	**150 V Rad-Hard VDMOS [55]**
On-State Resistance R_{DSON} *(mΩ)*	102	56	90
Total Gate Charge Q_G *(nC)*	4.6	8.9	50
Gate-to-Drain Charge Q_{GD} *(nC)*	0.8	2.0	18
Body Diode Reverse Recovery Time T_{RR} *(ns)*	36	61	300
Body Diode Reverse Recovery Charge Q_{RR} *(nC)*	32	71	2600
Figure of Merit $R_{DSON} \times Q_G$	469	498	4500
Figure of Merit $R_{DSON} \times Q_{GD}$	82	112	1620

SEE Testing Results

Heavy ion radiation testing was conducted using the Texas A&M University Cyclotron Institute K500 cyclotron. All runs were performed at room temperature using the 15 MeV/amu Au beam to a fluence of 1.0×107 ions/cm2. Linear energy transfer (LET) within the 1.0 µm thick SOI device layer was calculated at 87 MeV cm2 / mg, based on overlayer thickness of the device. A summary of SEB and SEGR test data is summarized in Table 5.

Testing was conducted in accordance with MIL-STD 750E Method 1080 – test method for SEB and SEGR testing of power MOSFETs. In accordance with the test standard, the ion beam was oriented normal to the device surface during all runs. The device samples were wirebonded to a small PCB evaluation board with the top surface of the die exposed. A low inductance test fixture was used which supplied ample gate-to-source and drain-to-source capacitance, using high speed capacitors mounted in close proximity to the DUT. Drain-to-source and gate-to-source DC leakage currents were monitored using Keithley precision multimeters. Voltage and current waveforms were monitored on a 2.5 GS/s digital oscilloscope. Each sample was electrically tested for both BVdss and Vth prior to placement in the test chamber and again upon removal.

Due to the limited number of available beam runs, it was necessary to forego characterization of the capacitor response of the gate oxide and instead proceed directly to testing the SEB and SEGR safe operating areas (SOA) of the device. SEB tests were conducted with the gate and source power terminals connected to a common ground. The DC drain-to-source breakdown voltage of each sample was similar – approximately 164

V. During SEB tests, the devices were biased up to 160 V with no destructive failures observed.

SEGR testing was done by simultaneously applying gate-to-source and drain-to-source voltages, with the understanding that this represented the worst-case test condition for SEGR. Devices were biased with V_{GS} = -16 V and V_{DS} = 160 V (within 4 V of the DC breakdown voltage) simultaneously with no destructive SEGR failures observed. Unfortunately these devices were not further tested to failure at even more stressful biasing conditions due to the limited beam time, however the measured data demonstrated a rectangular SEE safe operating area matching the VGS and VDS maximum ratings for this class of power MOSFETs. This represents a significant improvement over conventional power VDMOS devices that typically have a SEB and SEGR SOA considerably below their maximum V_{GS} and V_{DS} DC ratings [52]. Gate oxide thickness for each sample is 55 nm, which should support a capacitor SEGR voltage of approximately 21 V, according to the Titus-Wheatley estimation for a gold ion strike at normal incidence.

Table 5: Heavy Ion SEB / SEGR Experimental Results

V_{DS} (V)	V_{GS} (V)	V_{GS} / tox (V/cm)	Ion Species	LET (MeV·cm^2/mg)	Flux (ions/cm^2/s)	Fluence (ions/cm^2)	Deposited Dose (rads(Si))	SEB (Y/N)	SEGR (Y/N)
145	0	N/A	Au	87	2.6E+4	1.0E+7	13.9k	N	N
160	0	N/A	Au	87	3.4E+4	1.0E+7	13.9k	N	N
145	-12.8	2.3E+6	Au	87	2.7E+4	1.0E+7	13.9k	N	N
145	-16.0	2.9E+6	Au	87	3.4E+4	1.0E+7	13.9k	N	N
160	-16.0	2.9E+6	Au	87	3.6E+4	1.0E+7	13.9k	N	N
160	-16.0	2.9E+6	Au	87	3.8E+4	1.0E+7	13.9k	N	N

Heavy ion test data of six device samples (one sample per test condition) using designs from the same wafer. BV_{DSS} of these samples is approximately 164 V with a gate oxide thickness of 55 nm. The ion beam is oriented normal to the silicon surface for all runs. Gate-to-source leakage current pre- and post-irradiation remained unchanged at levels below 1 nA. Devices began showing increased drain-to-source leakage current (I_{DSS}) at fluences between 2E+6 and 8E+6 ions/cm^2. The leakage current was reduced substantially after a short room temperature anneal, during which each sample remained biased at the same V_{DS} and V_{GS} conditions as during irradiation.

CHAPTER SIX: CONCLUSIONS AND FUTURE WORK

Summary

This work reports on two new classes of SEE hardened lateral power MOSFETs intended for MHz frequency power switching applications. Both lateral devices were fabricated in a CMOS foundry and offer the possibility of monolithic integration into power integrated circuits. The first reported device is a low voltage 25 V Resurf LDMOS fabricated on P-type epitaxial silicon on a P+ silicon substrate. The second reported device is a 150 V SOI Resurf Thin Film LDMOS fabricated on a SmartCut™ SOI wafer, with a 1.0 µm thick P-type silicon device layer with a 1.0 µm thick buried SiO_2 layer on top of an N handle wafer. Both devices incorporates features to improve avalanche ruggedness and switching efficiency, both of which are primary concerns for high frequency power switching. The improvement in avalanche ruggedness also provides additional hardness against single event burnout.

The 25 V Epi LDMOS was originally designed with no top-side P+ source body tie, with a strategy of providing the P+ body tie at the bottom of the P+ substrate. This design did not produce the expected avalanche ruggedness, since the parasitic NPN transistor structure at the surface of the device could still be activated. Later, the device was redesigned to provide a top-side P+ source body tie which connected to a P+ buried layer extending underneath the poly gate. The purpose of this device feature is to provide very low resistance path for the diversion of hole photocurrent and avalanche hole current away from the sensitive base-emitter junction of the parasitic NPN BJT. This device

demonstrated a significant improvement in SEB threshold voltage. Optimization of the epitaxial layer thickness and P+ buried layer process were shown to have a significant impact on single event burnout threshold voltage.

The length of the drift region had a similar impact on SEB threshold voltage, which scaled with BV_{DSS}. This leads to a significant tradeoff between single event radiation hardness and R_{DSON}. The 25V LDMOS demonstrated lower specific R_{DSON} than state of the art radiation hardened power MOSFETs, because it was designed with a much lower BV_{DSS}.

The 150 V SOI LDMOS demonstrate improved electrical performance over state of the art commercially available 150 V power MOSFETs while at the same time demonstrating single event radiation hardness improved over state of the art radiation hardened planar VDMOS. This device exhibited very low Q_{GD} and a correspondingly low $R_{DSON} \times Q_G$ figure of merit. The device also exhibited approximately 50% lower Q_{RR} than state of the art 150 V commercial TrenchFET, which suggests an additional improvement in switching efficiency not accounted for in the figure of merit. The SOI LDMOS device also exhibited extreme avalanche ruggedness due to the incorporation of both a P+ source buried layer and an N drain buffer region. Unclamped inductive switching tests demonstrated a peak avalanche power capability of over 1.85×10^5 W/cm^2.

Testing was performed at the Texas A&M University Cyclotron Institute, using the most highest available LET ion beam. Testing with the 15 MeV/amu Au ion beam shows that SEB did not occur, even when the LDMOS is biased within a few volts of its DC drain-to-source breakdown voltage. No SEGR failures were observed when the

maximum possible V_{DS} and -16 V V_{GS} were applied simultaneously, demonstrating a SEGR safe operating area much improved from the traditional VDMOS devices. These tests were all performed using ion strikes at an angle of incidence normal to the silicon surface, per MIL-STD 750E Method 1080. SEB performance against a normal incidence strike is enhanced by the small collection volume afforded by the thin SOI device structure. Further SEB resistance was accomplished through implementation of customized doping profiles and device features to enhance avalanche ruggedness.

Measured data shows that the SOI LDMOS offers a high degree of resistance to SEGR, when the ion strike is normal to the silicon surface. This may be because a normal incidence strike naturally prevents a direct shunt between the gate oxide and the high potential zones of the depletion region in the lateral structure. Prior work [16[33][56] in evaluating worst case test conditions for VDMOS structures indicates that penetration into high potential zones of the depletion region has a strong effect on the SEGR response, and so we suspect the same might be the case for LDMOS. In that case, an angled strike may be a worse case for inducing SEGR and other damaging effects in the oxide, however this theory must be tested in future work.

Future Work

Further heavy ion testing of the 25 V LDMOS should be conducted using ions of higher LET. The SEB and SEGR safe operating area of the device should be characterized with respect to LET and ion angle of incidence. If the device fails to

demonstrate an acceptable SEB safe operating area for typical applications, then additional design optimizations should focus on the P+ buried layer process conditions. If the device fails to exhibit an acceptable SEGR safe operating area, then more radical design changes should be considered, which might help to further reduce the electrical coupling between the gate and drain.

Regarding the 150 V SOI LDMOS, simulations suggest that the small collection volume afforded by a 1.0 μm thin SOI device layer would not guarantee SEB immunity. In simulation, the SOI LDMOS remains susceptible to SEB, however an accurate real world safe operating area could not be predicted, due to no failures being observed experimentally. In terms of experimentally inducing SEB in this device using today's SEE test facilities, an angled ion strike would be necessary. Future heavy ion testing on both devices should be conducted to test the response to ion angle of incidence.

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