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Analysis And Design Optimization Of Multiphase Converter

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ANALYSIS AND DESIGN OPTIMIZATION OF MULTIPHASE CONVERTER

by

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Major Professor: Thomas Xinzhang Wu (Chair)
Issa Batarseh (Co-Chair)

TO MY PARENTS

WUSHAN ZHANG AND WENXIU DUAN

TO MY WIFE

SIQI GUO

ABSTRACT

Future microprocessors pose many challenges to the power conversion techniques. Multiphase synchronous buck converters have been widely used in high current low voltage microprocessor application. Design optimization needs to be carefully carried out with pushing the envelope specification and ever increasing concentration towards power saving features. In this work, attention has been focused on dynamic aspects of multiphase synchronous buck design. The power related issues and optimizations have been comprehensively investigated in this paper.

In the first chapter, multiphase DC-DC conversion is presented with background application. Adaptive voltage positioning and various nonlinear control schemes are evaluated.

Design optimization are presented to achieve best static efficiency over the entire load range. Power loss analysis from various operation modes and driver IC definition are studied thoroughly to better understand the loss terms and minimize the power loss. Load adaptive control is then proposed together with parametric optimization to achieve optimum efficiency figure.

New nonlinear control schemes are proposed to improve the transient response, i.e. load engage and load release responses, of the multiphase VR in low frequency repetitive transient. Drop phase optimization and PWM transition from long tri-state phase are presented to improve the smoothness and robustness of the VR in mode transition. During high frequency repetitive transient, the control loop should be optimized and nonlinear loop should be turned off. Dynamic current sharing are thoroughly studied in chapter 4. The output impedance of the multiphase

synchronous buck are derived to assist the analysis. Beat frequency is studied and mitigated by proposing load frequency detection scheme by turning OFF the nonlinear loop and introducing current protection in the control loop.

Dynamic voltage scaling (DVS) is now used in modern Multi-Core processor (MCP) and multiprocessor System-on-Chip (MPSoC) to reduce operational voltage under light load condition. With the aggressive motivation to boost dynamic power efficiency, the design specification of voltage transition (dv/dt) for the DVS is pushing the physical limitation of the multiphase converter design and the component stress as well. In this paper, the operation modes and modes transition during dynamic voltage transition are illustrated. Critical dead-times of driver IC design and system dynamics are first studied and then optimized. The excessive stress on the control MOSFET which increases the reliability concern is captured in boost mode operation. Feasible solutions are also proposed and verified by both simulation and experiment results. CdV/dt compensation for removing the AVP effect and novel nonlinear control scheme for smooth transition are proposed for dealing with fast voltage positioning. Optimum phase number control during dynamic voltage transition is also proposed and triggered by voltage identification (VID) delta to further reduce the dynamic loss. The proposed schemes are experimentally verified in a 200 W six phase synchronous buck converter.

Finally, the work is concluded. The references are listed.

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AVP   Adaptive voltage positioning

PFM   Pulse frequency modulation

CCM   Continues conduction mode

DPWM   Digital pulse width modulation

LL   Load line

IIR   Infinite impulse response

Q_g MOSFET gate charge

R_G MOSFET gate resistance

Q_{RR} Reverse recovery charge

FOM   figure of merit

f_{SW} Switching frequency

C_{OSS} Output capacitance

C_{DS} Drain-source capacitance

C_{GD} Gate-drain capacitance

C_{GS} Gate-source capacitance

C_{DFP} Drain-field plate capacitance

V_{SD} Diode forward voltage drop

$V_{GS(th)}$ Gate-source threshold voltage

BV_{DSS} Drain-Source Breakdown Voltage

R_{fp} Snubber resister in MOSFET cell

V_{BUS} Input voltage of the converter

V_O Output voltage of the converter

V_{FET_DRV} MOSFET driving voltage

DCR   Direct current resistance

LSB   Least significant bit

GPIB   General purpose interface bus

ZCS   Zero current switching

ZVS   Zero voltage switching

CHAPTER ONE: INTRODUCTION

Power conversion techniques have been continuing to be the focus in the power management industry. With ever increasing the emphasis on power efficiency, switch mode power supplies and power management ICs are extensively used in automotive, smart phones, TVs, desktop PCs, servers, notebooks and etc. According to IMS research [1] power management & driver IC reaches $13.9567 billion in revenue in the fiscal year 2011.

The current and forecast worldwide market for power management ICs shipment (units in million) are shown in Figure 1. 1. [1] .

Power Management & Driver ICs by Application (Shippment in MU)
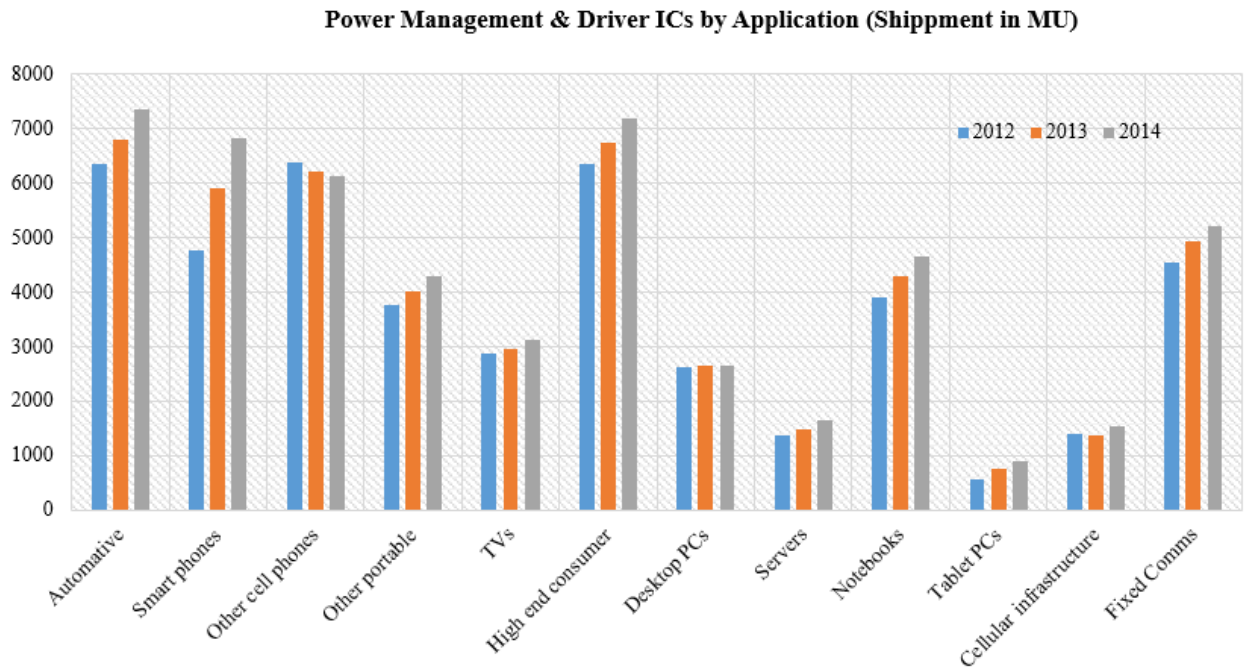
Figure 1. 1. The world market for power management IC by application.
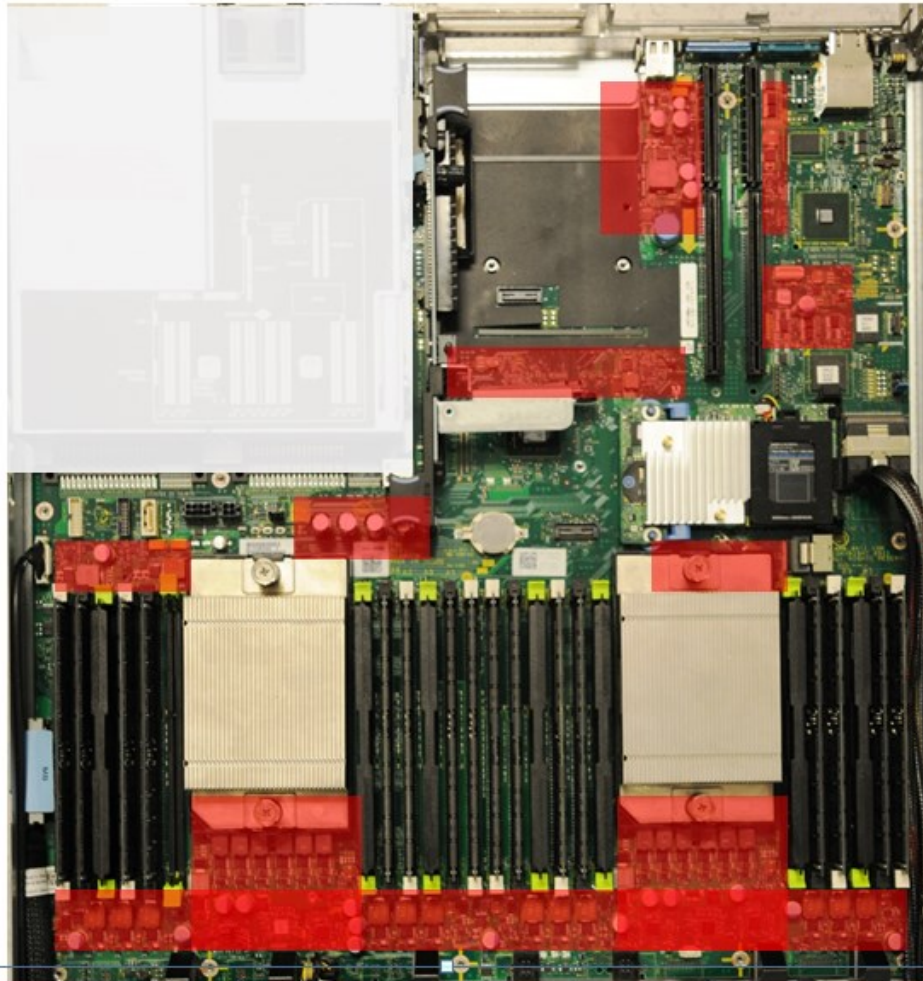
Figure 1. 2. Voltage regulator real estate in server motherboard.

This is the newly released Dell PowerEdge R620 Server motherboard. It can support two 150 W high end CPUs and 4 memory channels up to 768GB of memory (32GBx24dimms). The multiphase voltage regulators, 2 for CPU, 4 for MEM and the rest point of load (POL) VRs are highlighted in red. The VRs convert 12V DC from the PSU output to various voltage levels to power up the CPUs, memories, hard drives, ASICs on board and peripheral cards. It occupies more than 10% area of the motherboard.
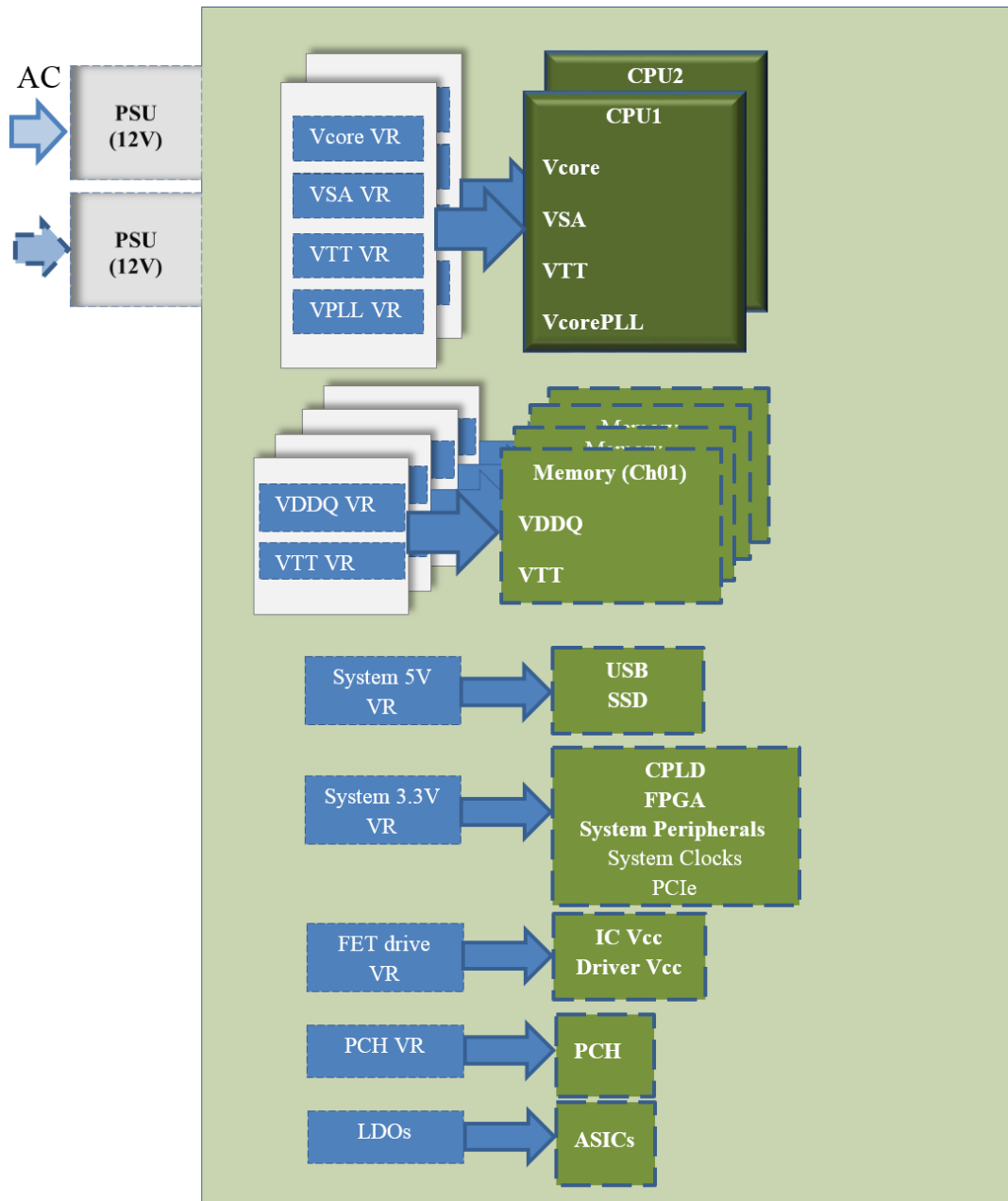
Figure 1. 3. A typical power management map for server system.

Figure 1. 3 shows a simplified power management map for a typical 2S (socket) server system. System interaction is eliminated in the illustration and the focus is only on the power conversion.

1.1 Introduction to Multiphase Buck Converter

As the complexity and number of transistors exponentially rise in the modern high end processors, the supply current specification is common to be above 100A. Paralleling the regulators is the only way to alleviate the thermal stress on the power components (power MOSFETs, power inductor). Therefore, multiphase buck converter has been employed in the power conversion field. Although the initial concept has been adopted in power management industry for quite a while, there are still a lot of areas worth investigating due to the increasing complexity of the power architecture and growing focus on the green energy. Green energy here refers to less power conversion loss and less output capacitors.
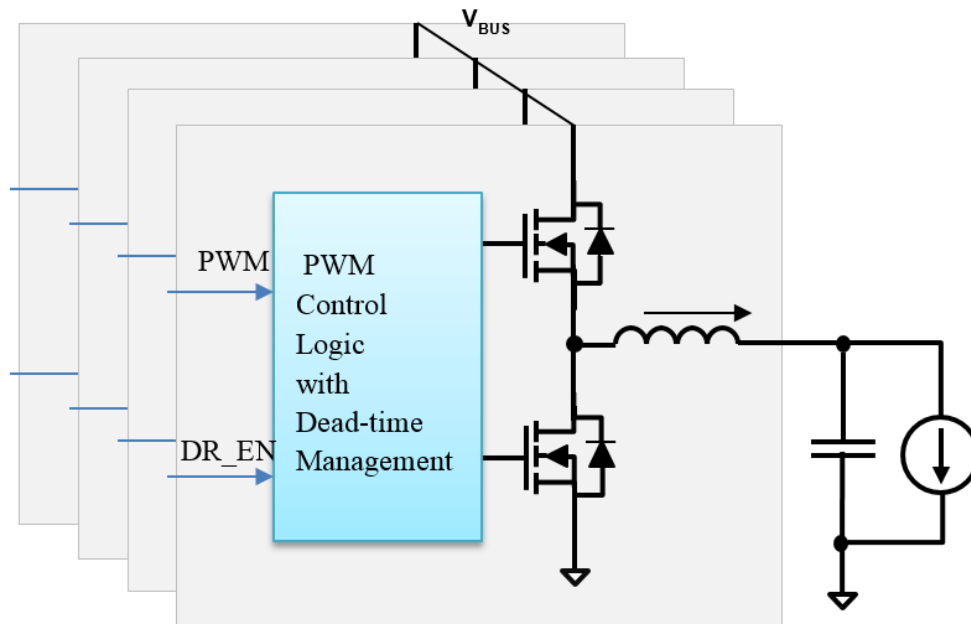
Figure 1. 4. A multiphase synchronous buck converter for CPU application.

Figure 1. 5 shows the relationship of normalized ripple current between duty cycle and phase number.
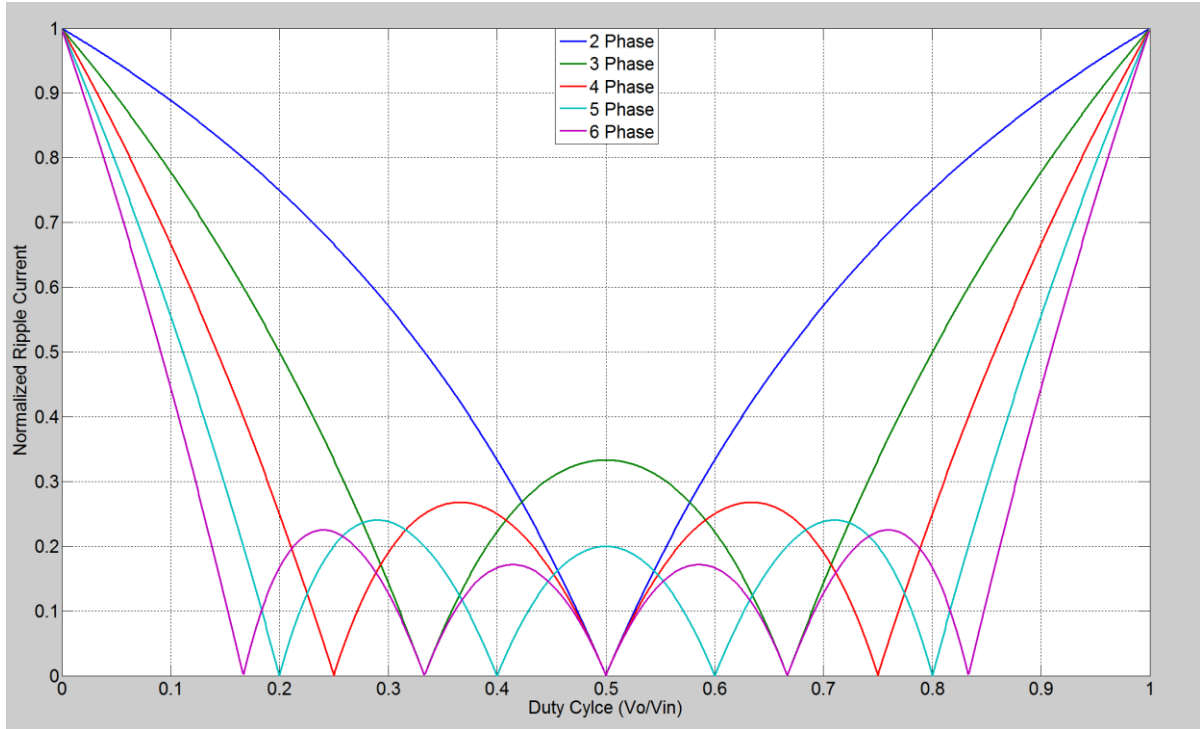
Figure 1. 5. Normalized ripple current as a function of phase number and duty cycle.

The benefits of adopting multiphase buck converter in the design are bulleted as follows:

- Decreased I_{RMS} and reduced power loss;

- Increased inductor current slew rate: $L_{effective} = \dfrac{L}{N_{phase}}$;

- Output inductor current cancellation and voltage ripple reduction;

- Optimized efficiency over the whole load range, especially, in light load

    o Load adaptive control(LAC)

    o Pulse skipping control(PFM)

- Better dynamic voltage regulation capability

However, with those advantages, there are challenges that the multiphase converter have brought in as well. The challenges are the major focus of this dissertation.

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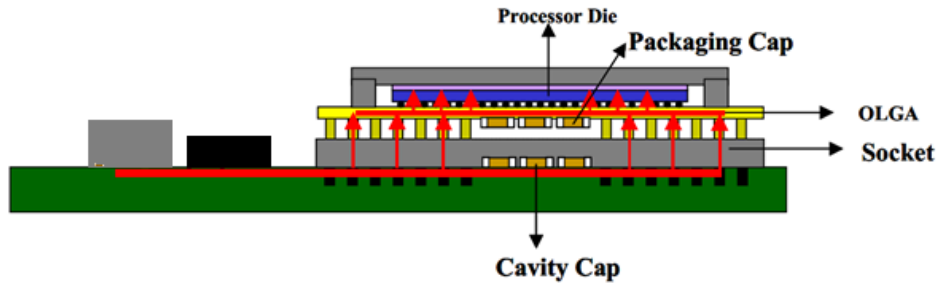
Figure 1. 6. A typical power delivery path for today's microprocessors.

Figure 1. *6* shows a typical power delivery path for today's microprocessors. With all the mechanical restriction, the power inductors and output capacitors need to be placed close to the processors in order to reduce the power distribution loss.
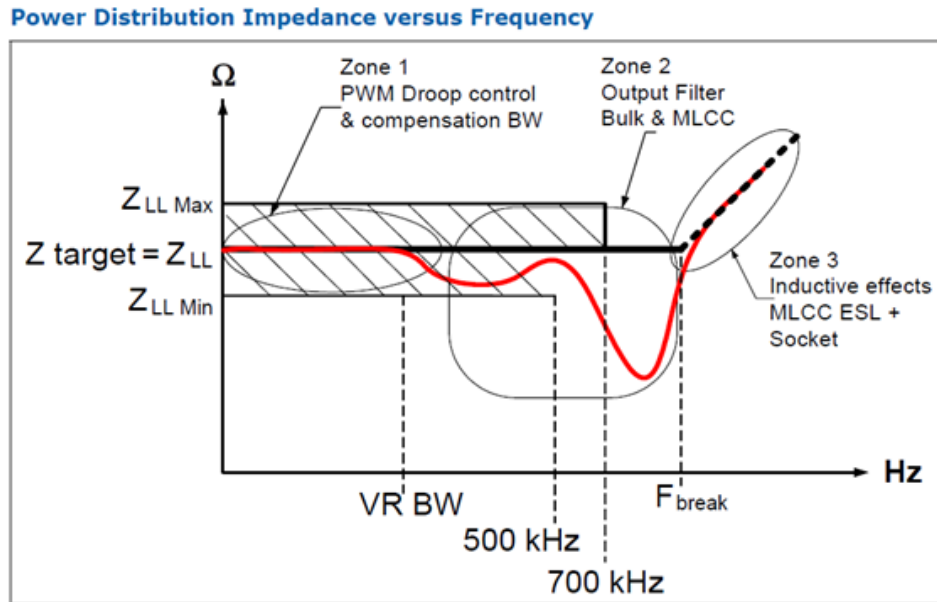
Figure 1. 7 Power distribution impedance versus frequency.

Closed-loop output impedance of voltage regulator is an important specification in the frequency domain. Figure 1. 7 [2] shows the output impedance plot of a power supply for CPU application with AVP. The output impedance, as shown by the red curve, is determined by the

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power supply's AVP design value within the loop bandwidth of the VR. At higher frequency, the output impedance will be dominated by the ESL of MLCC and the socket.

Figure 1. 8 shows the pyramid of server power design. Robustness is of the top priority in the power design since the system are running with various kinds of customer's data, some of which are very critical. The power related failures can stop the transaction or communication and would create substantial loss. The power conversion efficiency is the foundation of the power design. Design parametric optimization and latest silicon technology adoption should be rigorously studied. Functionality, such as, phase shedding control and load transient enhancements, shows the advancement of the design and can improve the system reliability, efficiency and reduce the cost. Cost reduction is the final step to optimize the design and give environment less burden.
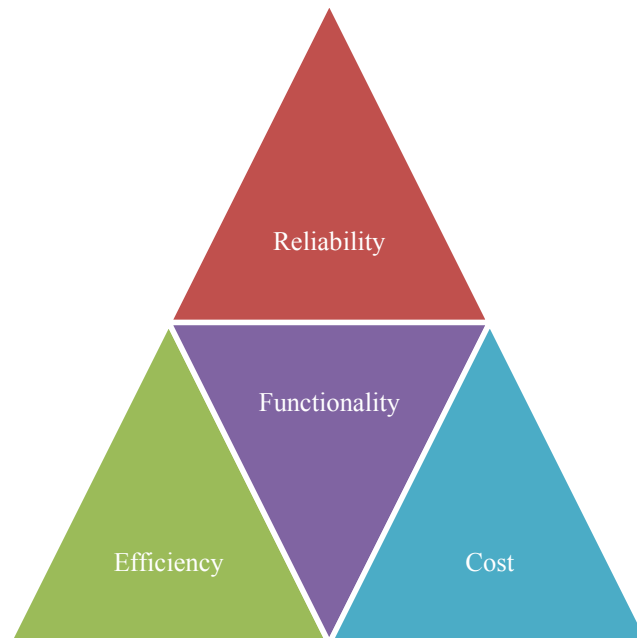
Figure 1. 8. Robustness, efficiency and cost pyramid in server power design.

<u>1.2 Adaptive Voltage Positioning</u>

Due to the working mode of the processors, load transient is an important design requirement for multiphase synchronous buck converter. Adaptive voltage positioning (AVP) has been adopted to lower the power dissipation, especially at heavy load [3] - [5] . The introduced constant output impedance reduces the value of output capacitance.

Figure 1. 9 illustrates the comparison results of AVP implementation when load transient events occur. The introduced AVP window can be fully utilized to optimize the load transient.
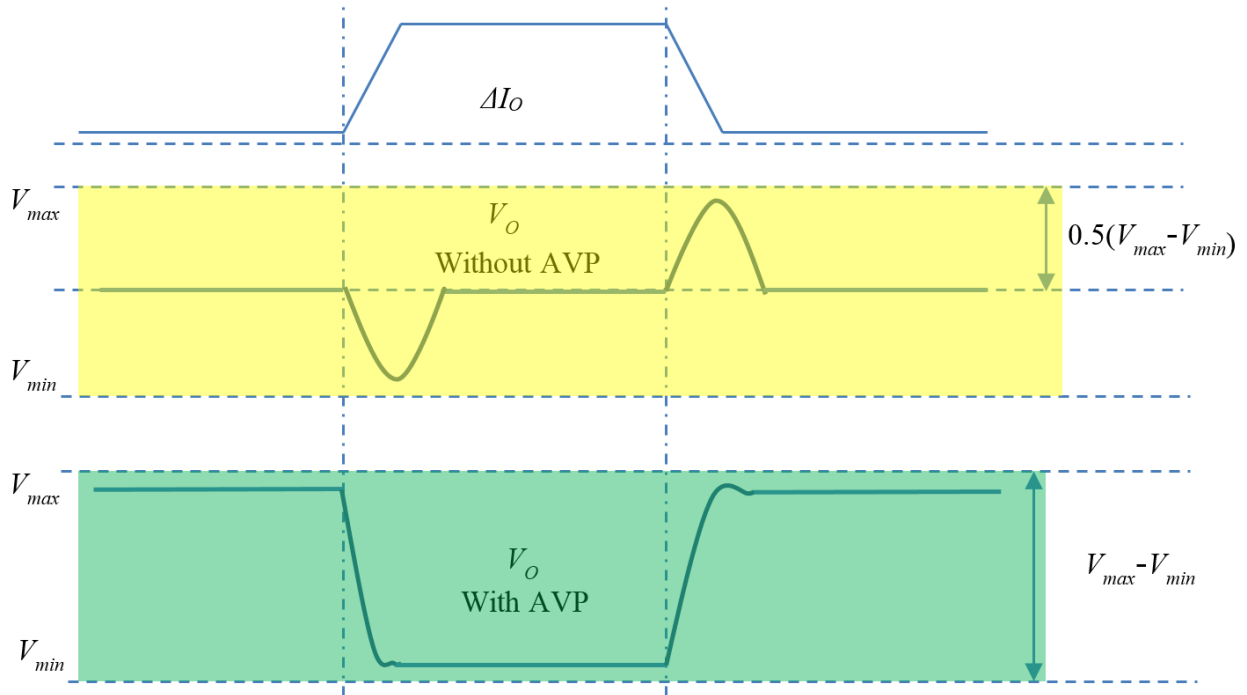
Figure 1. 9. Load transient without and with AVP implementation.
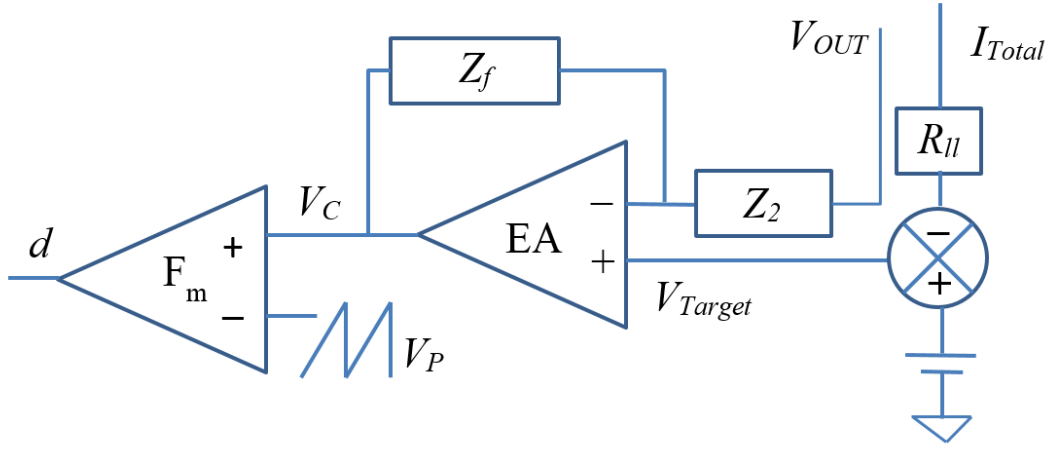
Figure 1. 10. AVP design in analog realization.

Figure 1. 10 illustrates the block diagram of AVP design in an analog realization [6]
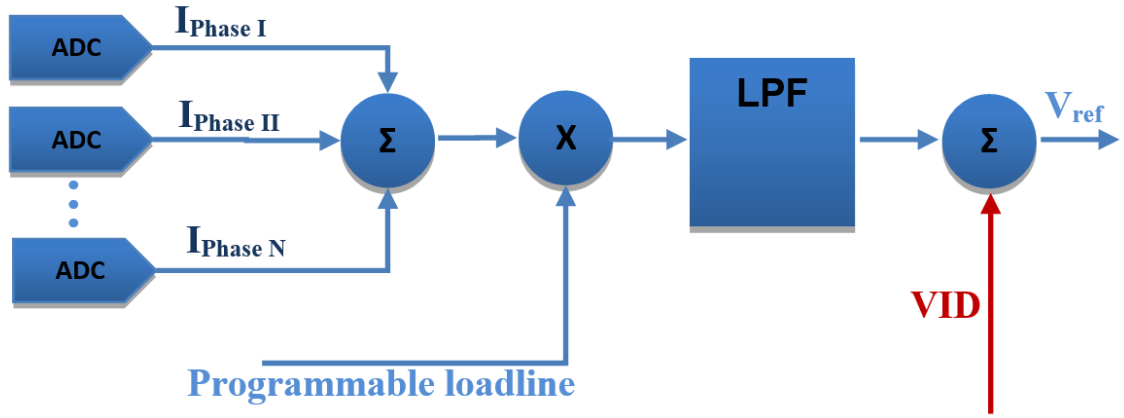
Figure 1. 11. AVP design in digital realization.

To make it simple, the adaptive voltage position (AVP) design is to use the entire AVP window for voltage excursions during the transient event. As depicted in Figure 1. 12, another design benefit of adopting AVP scheme is that the output power of the multiphase VR at full load, thus, less thermal burden compared to the implementation without AVP.

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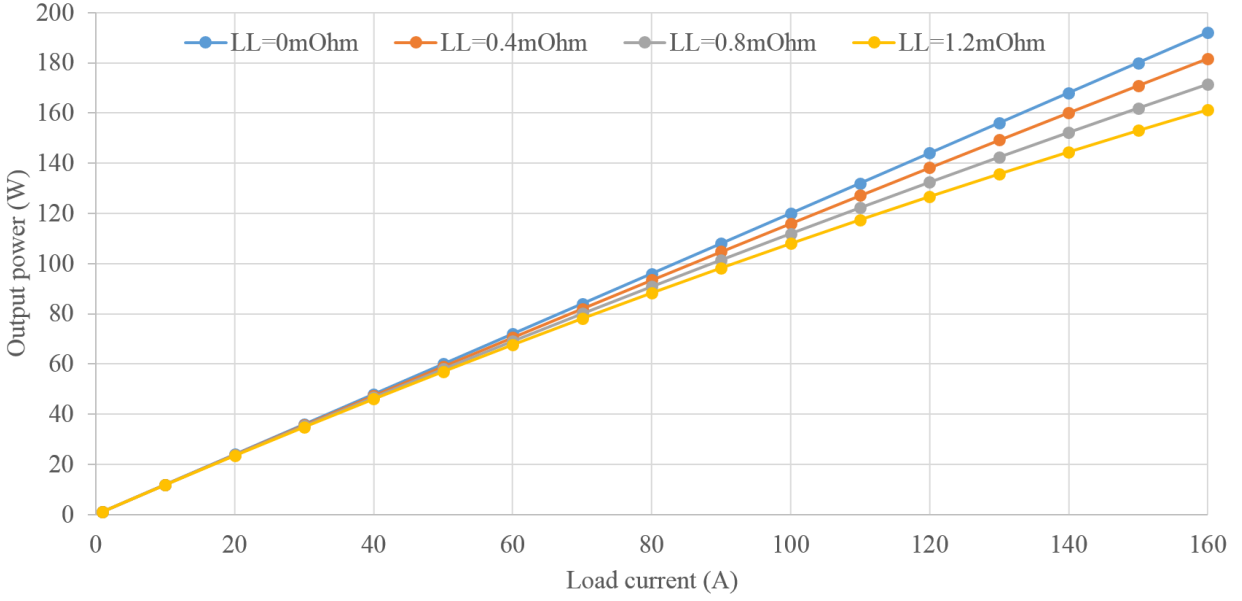
Figure 1. 12. Output power comparison with different LL.

The differential output of the sensed inductor current feeds into the dedicated ADC and digitized values are summed together for the total load current. The V_{REF} is generated by the current VID minus the filtered (averaged) output of summation of phase current multiplied by the load line.

$$V_{Target} = VID - I_{LOAD} \cdot R_{LL} \qquad (1.1)$$

1.3 Review of Prior Arts

In order to meet the stringent transient requirement, novel control schemes [12] -[15] should be adopted to meet the specification and minimize the output capacitance. Traditional voltage mode based buck converter is the most popular thus widely adopted topology in the power management industry. It is a clock based converter and the VR needs to wait the entire switching cycle to issue the next PWM on pulse no matter when the transient event occurs. Constant ON-time (COT) is a popular scheme. Traditional COT uses ESR of output capacitor as

output current feedforward term to initial the pulse. Current mode hysteretic control [17] [18] is a very popular topology to achieve fast transient response. It uses sensed/synthetic inductor current to compare against the hysteresis band. In [18] authors propose current mode hysteretic control that can accomplish the AVP by the natural hysteresis band, however, the fairly constant hysteretic window cannot pull in the pulse fast enough when the transient event occurs.

1.3.1 Constant ON-time (COT)

Constant ON-time (COT) is a popular frequency modulation scheme which is capable of achieving fast transient response.
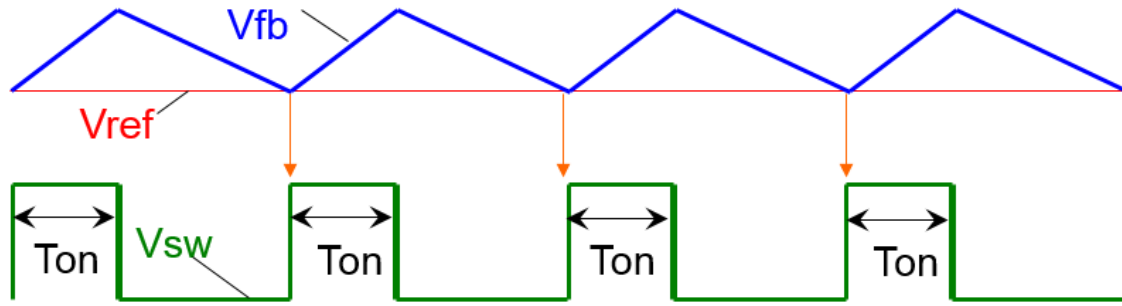
Figure 1. 13. Constant ON time.

The core of the modulator is the one-shot that sets the HS ON-time. The T_{ON}, as shown in (1.2), is inversely proportional to V_{IN} and proportional to the V_{OUT}:

$$T_{ON} = T_{SW} \frac{V_{OUT}}{V_{IN}} \tag{1. 2}$$

As shown in Figure 1. 13, when V_{FB} becomes lower than V_{REF}, the next ON period is initiated. On pulse period stays for a predetermined period as equation (1.2) indicates. The clock-less architecture shows the advantage that the HS pulse can be initiated sooner when transient

event occurs. There will be a minimum OFF-time between the HS pulses to guarantee the current sensing purpose. The minimum OFF-time also decides the maximum duty cycle that the VR can support.
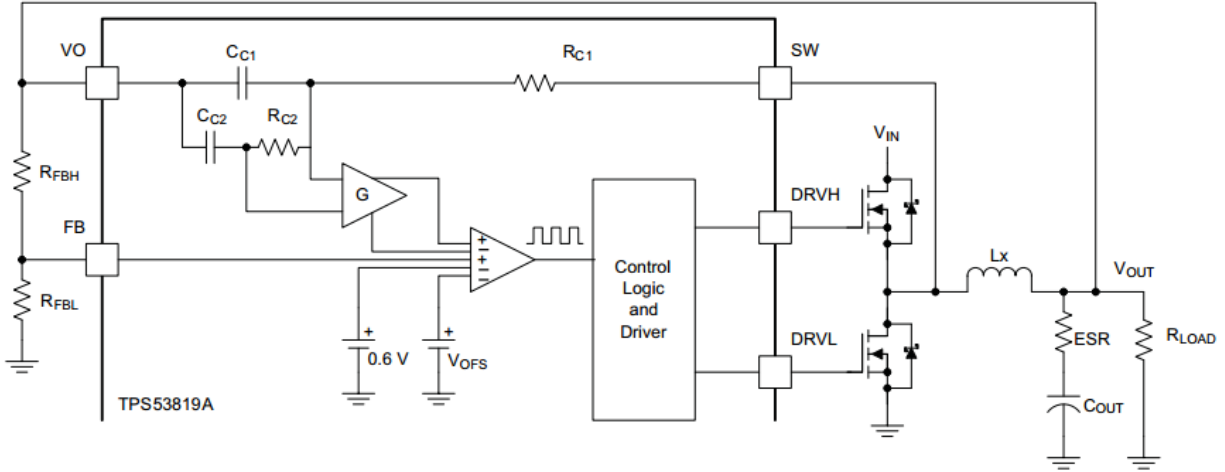
Figure 1. 14. Simplified voltage mode COT architecture with ripple injection.

The D-CAP2 control scheme [19] , introduced by Texas instruments, includes an internal ripple generation circuitry, RCC, as the red block in Figure 1. 14. Compared with first generation of D-CAP, multi-layer ceramic capacitors (MLCC) solution with very low ESR can be used due to the ripple injection. The hybrid control mode is to employ the emulated inductor current ripple and then combine it with the voltage feedback signal.

To meet small-signal stability, the output capacitance value should be governed by (1.3)

$$5 \times f_{C2} \leq = \frac{R_{C1} \times C_{C1} \times 0.6 \times (0.67+D)}{2\pi \times G \times L \times C_{OUT} \times V_{OUT}} \leq \frac{f_{SW}}{3} \tag{1.3}$$

where G =0.25. $R_{C1} \times C_{C1}$ time constant can be referred to TPS53819 datasheet. D is the duty cycle.

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1.3.2 Current Mode Hysteresis

Hysteretic control is a very popular topology for fast transient required application. A drawback of traditional hysteretic control from the static point of view is the switching frequency is variable (clock-less), which is defined by parasitic elements, primarily the ESR of the output capacitor. Advanced hysteretic control incorporates the frequency control (phase-locked loop) to stabilize the switching frequency.

Intersil refers to the R4 (Robust Ripple Regulator as described with R3) Modulator as a "Current-Mode Hysteretic" modulator (CMH). It is a variable frequency switching architecture which operates without a clock and uses a hysteretic band against which a "current" signal is compared. However, true inductor current is not used for the modulation, unlike a true current-mode controller. A synthesized (synthetic) current ripple is generated and compared against the hysteretic window that is created relative to the voltage loop feedback to determine power switch on and off times. Also there is no compensating ramp utilized. The architecture does not make use of any voltage feedback compensation and no integrator. Therefore it has the capacity for fast transient response and easier deployment of a design.
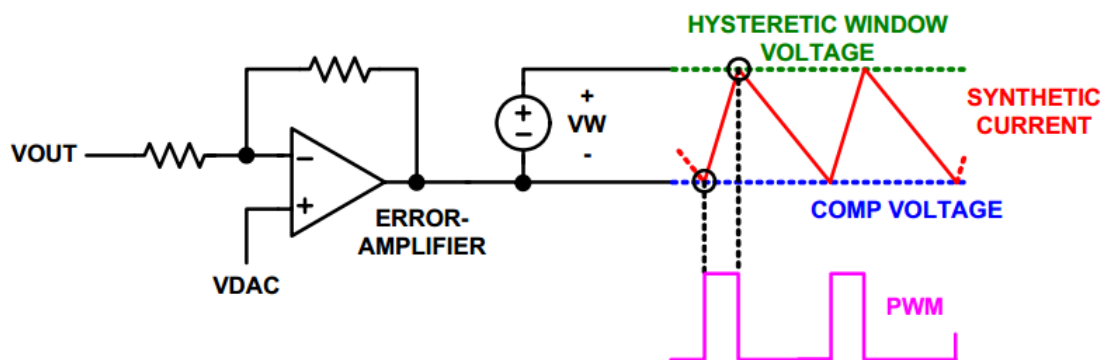
Figure 1. 15. Simplified R4™ modules for PWM generation.

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Figure 1. 15 [22] shows the modulator core of the R4 controller, the error-amplifier, synthetic current generator and the hysteretic window comparator. The error voltage, generated by the VDAC minus feedback, compares against monitors the synthetic current signal against and corresponding window voltage to determine the PWM switching events.
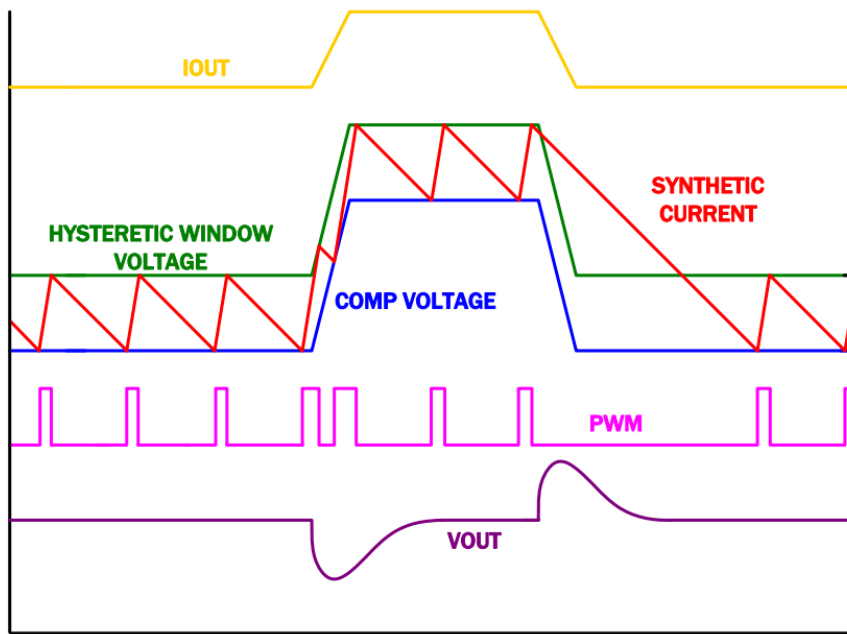
Figure 1. 16. Simplified operation waveform during load transient.

Figure 1. 16 [22] shows the operational waveform during load assertion and load release. Switching frequency, as the magenta curve indicates, speeds up during load assertion and slows down during load release. Both PWM edges are modulated since the synthetic current compares against Hysteric upper window and V_{COMP} voltage.

1.3.3 EAPP

Minimizing the delay in control loop is critical during transient event. Based on the advantages of trailing/leading edge modulation during turning OFF/ON, the enhanced active pulse positioning (EAPP) is able to minimize both ON/OFF delays by combining the schemes as discussed in [24] .
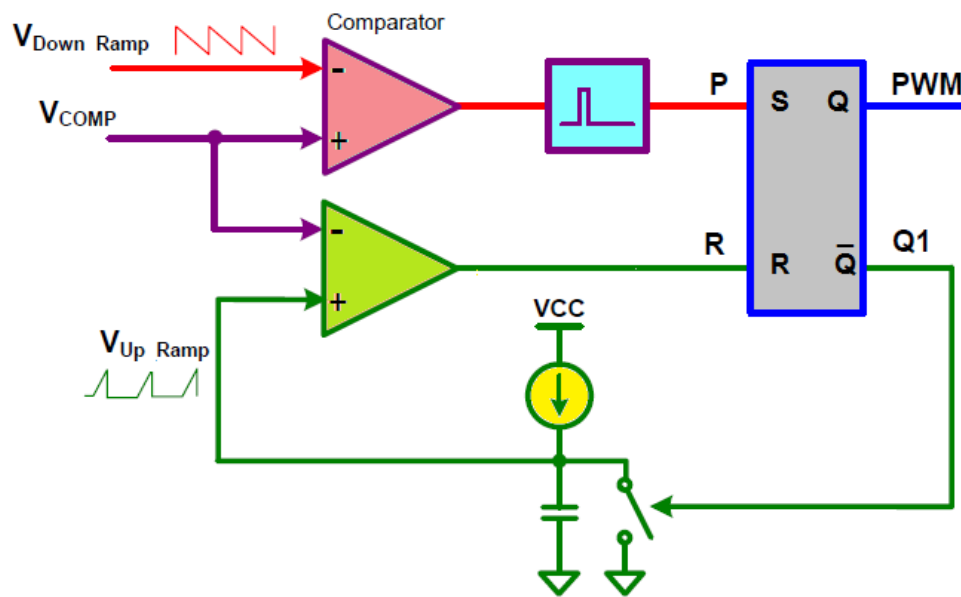
Figure 1. 17. Schematic diagram of EAPP circuitry.

The simplified block diagram and the corresponding operational waveforms are illustrated in Figure 1. 17. During transient event, EAPP will turn on PWM early (from t3 to t2) and move the next PWM ahead (from t8 to t7) to reduce the blanking time. Figure 5 shows transient load engage response of 3-phase VR with EAPP [24] , [25] .

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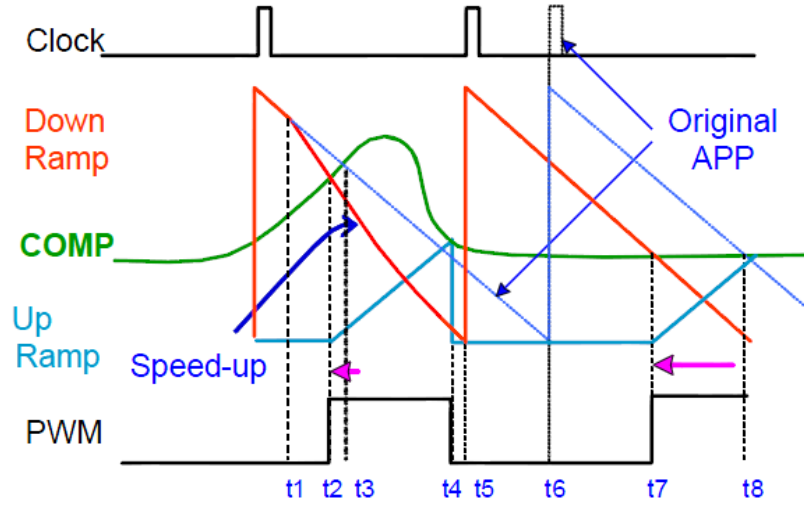
Figure 1. 18. Dual-Edge and Variable-Frequency Operational Waveforms.

1.4 Dissertation Outlines

The primary focus and objective of the dissertation is to comprehensively investigate the current and voltage dynamics of the multiphase synchronous buck converter. We focus on optimizing the topology to achieve best efficiency and highest possible reliability based on the real system running condition and corner case scenarios.

In chapter 1, we introduce the background information of the importance of power management IC in different business sectors, then the scenario multiphase synchronous buck converter and briefly talk about the AVP design that can reduce output capacitors and power dissipation. The ongoing research and advanced control topologies are reviewed and several nonlinear control schemes are studied

In chapter 2, we start the efficiency optimization from static operation. First, we design the compensation of the voltage mode controller with digitized format. We meticulously study

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the power loss in several modes of operation, i.e. buck, PFM and boost modes, which cover all the operation scenarios of CPU VR. Driver interface is thoroughly investigated here for operation and efficiency purposes. Switching waveforms are understood better with all the parasitics. An efficiency optimization routine is generated by parametric variation.

In chapter 3, we propose the load transient enhancement schemes to minimize the output voltage excursion during low repetitive load transient. We first study the DCR current sense impact for the AVP loop, which can effectively shape the output voltage excursion. During load engage, the pulse should be pulled in fast enough to compensate the voltage deviation. During load release, adaptive body braking schemes are proposed to adaptively suppress the voltage overshoot during load release. Special design consideration needs to be carried out during slow phase shedding that the inductor current in the shedded phase needs to be ramped down to zero before turn OFF the phase. A corner case operation with potential power MOSFETs shoot-through is captured and new dead-time management scheme is proposed to maintain the high efficiency, eliminate the shoot-through and hence ensure the system reliability.

In chapter 4, we first study the sampling nature of PWM converter. The closed loop system output impedance is derived and the compensation network are optimized in the high frequency range to attenuate the high frequency system noise. Beat frequency is studied and load frequency detection scheme and current protection in the control loop are proposed to mitigate the issue and bound the phase current.

Multiphase converter design capable of dynamic voltage scaling (DVS) is presented in chapter 5. Modes of operation are thoroughly studied first. Optimized driver dead-time in boost

mode operation are illustrated and DVID downward transition can be achieved with shared phase current. The excessive stress on the control MOSFET which increases the reliability concern is captured in boost mode operation. Feasible solutions are also proposed and verified by both simulation and experiment results. CdV/dt compensation for removing the AVP effect and novel nonlinear control scheme for smooth transition are proposed for dealing with fast voltage positioning. Optimum phase number control during dynamic voltage transition is also proposed and triggered by voltage identification (VID) delta to further reduce the dynamic loss.

Chapter 6 presents the conclusions and the future work is outlined.

CHAPTER TWO: OPTIMIZATION ON STATIC OPERATION
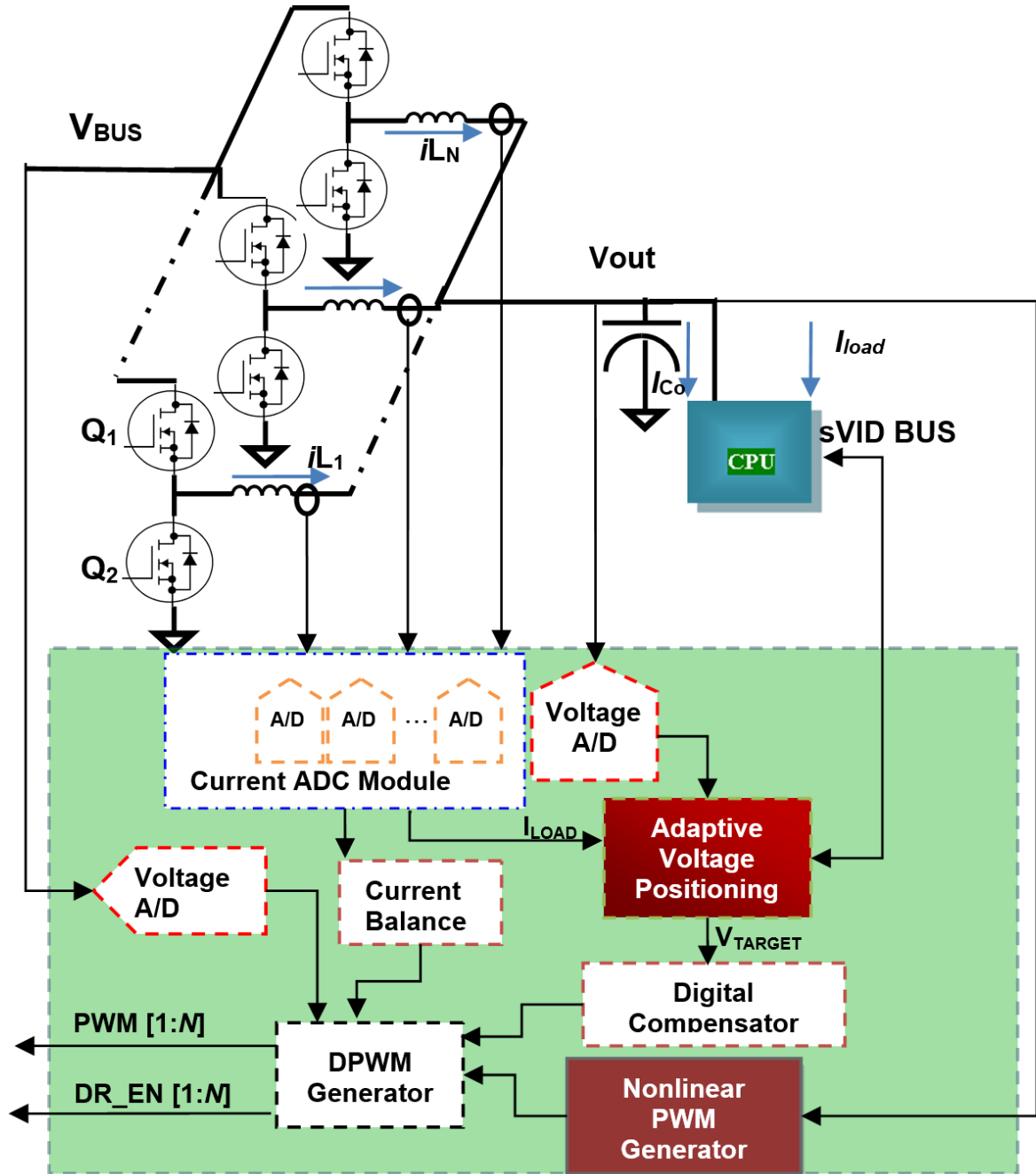
Figure 2. 1. The architecture of the bidirectional multiphase synchronous controller.

Figure 2. 1 shows the architecture of the multiphase synchronous buck converter which can be working in the bidirectional fashion. Each phase is interleaved by $360/N_{PHASE}$ to achieve optimal ripple cancellation. In the controller section, the main sub-circuit modules are illustrated. Current ADC module samples and digitizes each phase current, which is the voltage across the cap of inductor DCR the sense network, in the real time manner. Voltage ADCs sense and digitize both the V_{OUT} and V_{BUS}, and the digitized V_{BUS} acts as feed-forward term in the control loop. Adaptive voltage positioning (AVP) module decodes the VID command and generates the reference based the digitized total phase current information with DVID compensation. Digital compensator filters the error voltage generated by ADC output and AVP blocks and feeds into the DPWM generator block. Current balance module, which is designed as 1/5 of the voltage loop, and Nonlinear PWM generator both modifies DPWM patterns in different fashions. The control outputs of DPWM generators are the PWM and driver enable (DR_EN) signals.

2.1 Compensation Design

Compensator design is the core of VR design [7] [8] . As shown in Figure 2. 2, a small signal ac model is presented. $V_{out}(s)$ is the function of the reference voltage $V_{target}(s)$, line input voltage $V_{in}(s)$ and the output load current $I_{out}(s)$. The design objective is the VR capable of rejecting the disturbances of the line input voltage and output load current, good transient response and stability.

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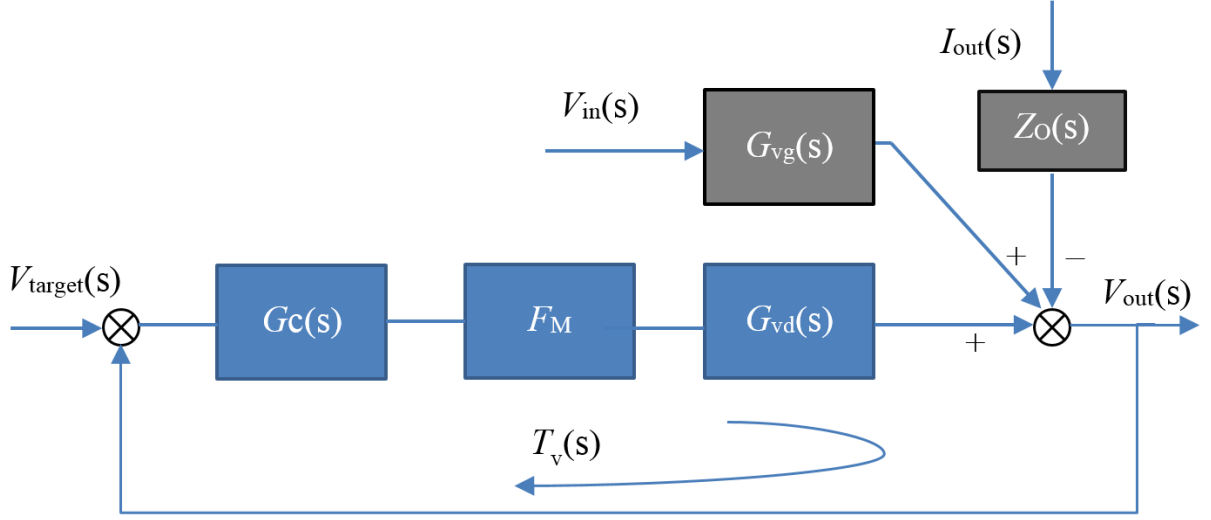
Figure 2. 2. Small signal model of voltage mode buck converter.

$$\hat{v}_{out}(s) = G_{vd}(s)\hat{d}(s) + G_{vg}(s)\hat{v}_{in}(s) - Z_o(s)\hat{i}_{out}(s) \tag{2.1}$$

$$G_{vd}(s) = \frac{\hat{v}_{out}(s)}{\hat{d}(s)}\Big|_{\substack{\hat{v}_{in}(s)=0 \\ \hat{i}_{out}(s)=0}} = \frac{V_{in}(1+sR_{ESR}C_{OUT})\frac{R_{Load}}{(R_{Load}+R_{DCR})}}{s^2LC_{OUT}\left(\frac{R_{Load}+R_{ESR}}{R_{Load}+R_{DCR}}\right)+s\left(\frac{L}{R_{Load}+R_{DCR}}+C_{OUT}R_{ESR}+R_{Load}//R_{DCR}\right)+1} \tag{2.2}$$

$$Z_o(s) = \frac{\hat{v}_{out}(s)}{\hat{i}_{out}(s)}\Big|_{\substack{\hat{d}(s)=0 \\ \hat{i}_{out}(s)=0}} = \frac{\left(1+\frac{sL}{R_{DCR}}\right)(1+sR_{ESR}C_{OUT})\frac{R_{Load}R_{DCR}}{(R_{Load}+R_{DCR})}}{s^2LC_{OUT}\left(\frac{R_{Load}+R_{ESR}}{R_{Load}+R_{DCR}}\right)+s\left(\frac{L+R_{Load}R_{DCR}+C_{OUT}R_{ESR}(R_{Load}+R_{DCR})}{R_{Load}+R_{DCR}}\right)+1} \tag{2.3}$$

$$G_{vg}(s) = \frac{\hat{v}_{out}(s)}{\hat{v}_{in}(s)}\Big|_{\substack{\hat{d}(s)=0 \\ \hat{i}_{out}(s)=0}} = D\frac{\frac{R_{DCR}(1+sR_{ESR}C_{OUT})}{R_{Load}+R_{DCR}}}{\frac{s^2LC_{OUT}(R_{Load}+R_{ESR})}{R_{Load}+R_{DCR}}+s\frac{(L+C_{OUT}(R_{ESR}(R_{Load}+R_{DCR})+R_{Load}R_{DCR})}{R_{Load}+R_{DCR}}+1} \tag{2.4}$$

$$T_v(s) = G_C(s)F_MG_{vd}(s) \tag{2.5}$$

The derivation is based on the state-space averaging model.

Gvd(s) is a state-space averaging model for the plant, which represents open loop control-to-output voltage transfer function.

Zo(s) is the output current-to-output voltage transfer function.

Gvg(s) is the open loop input-to-output voltage transfer function.

2.1.1 Direct Digital Design

Due to the double pole of output filter in the voltage mode control, as shown in Figure 2. 3, two zeros from the type III compensation network are needed so that the phase can be boosted by 180 degrees. There are two methods to design the digital compensation network:

(1) Emulation method, design the analog compensation first in Laplace domain and transfer to digital domain.

(2) Direct digital design, design the compensation network in digital domain by first digitizing the plant.
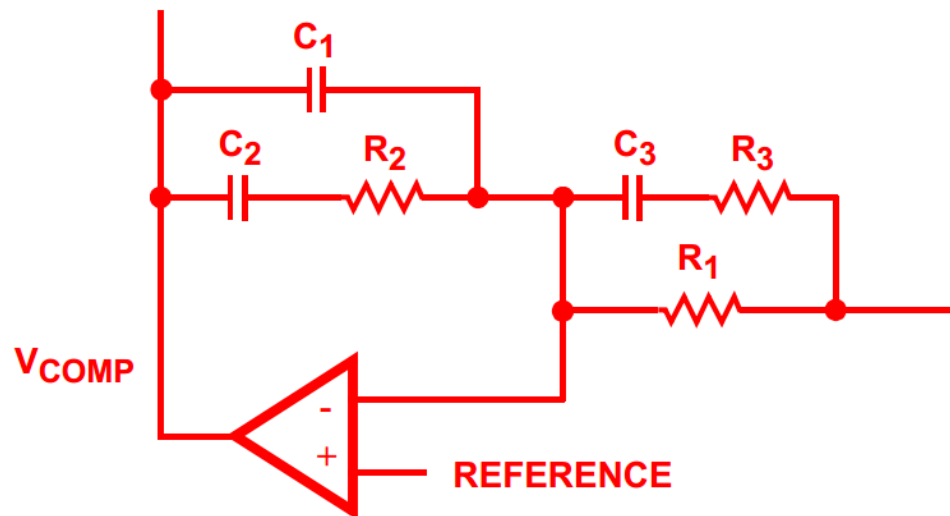
Figure 2. 3. Generic type III compensation network.
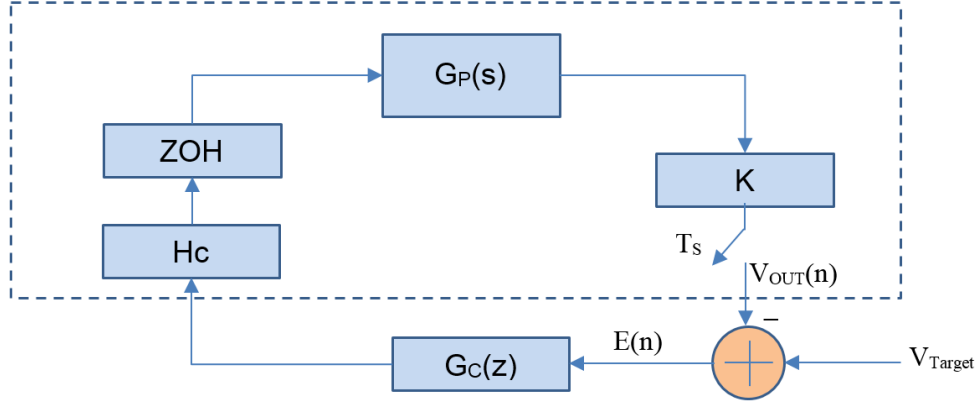
Figure 2. 4. Digital control loop block diagram

To digitize the plant, there are several methods can be used, for example Zero-Pole matching (ZPM), Impulse Invariant Mapping, as well as, Tustin approximation. We use ZPM as the method of conversion. The matched DC gains is necessary for analog and discretized systems. The zeros and poles are transformed by the following equation:

$$z_i = e^{s_i/F_S} \tag{2. 6}$$

where, s_i is the ith pole or zero of the continuous-time system. z_i is the ith zero or pole of the discretized system accordingly. F_S is the sampling frequency.

2.1.2 Root Locus and Bode Plot

Root locus is a graphical technique of studying the roots (poles and zeros) of the characteristic equation of a linear system [9] . Matlab SISO design tool [10] can be utilized to move the poles and zeros location so that the desired system bandwidth and phase margin can be guaranteed.

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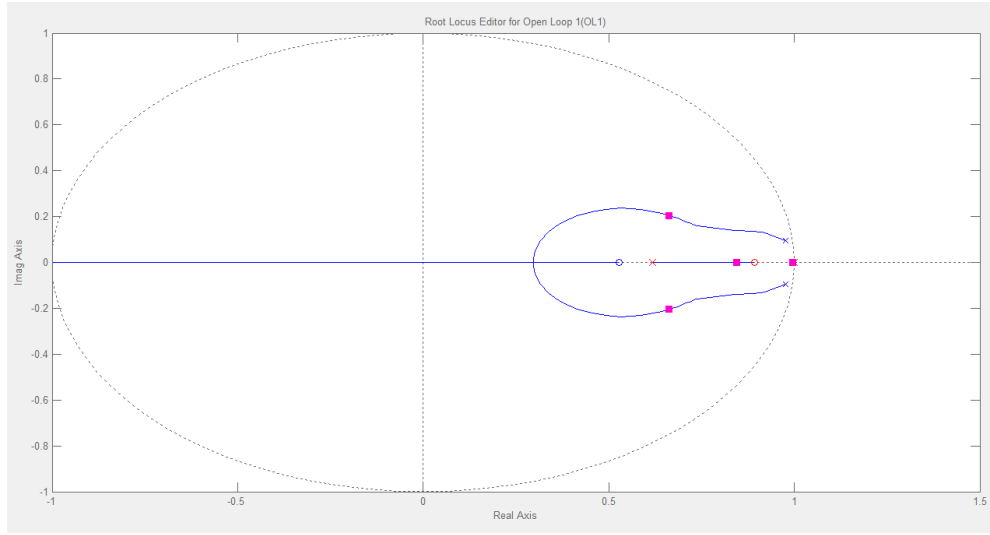
Figure 2. 5. Root Locus.

Figure 2. 5 shows the system root locus plot using Matlab.
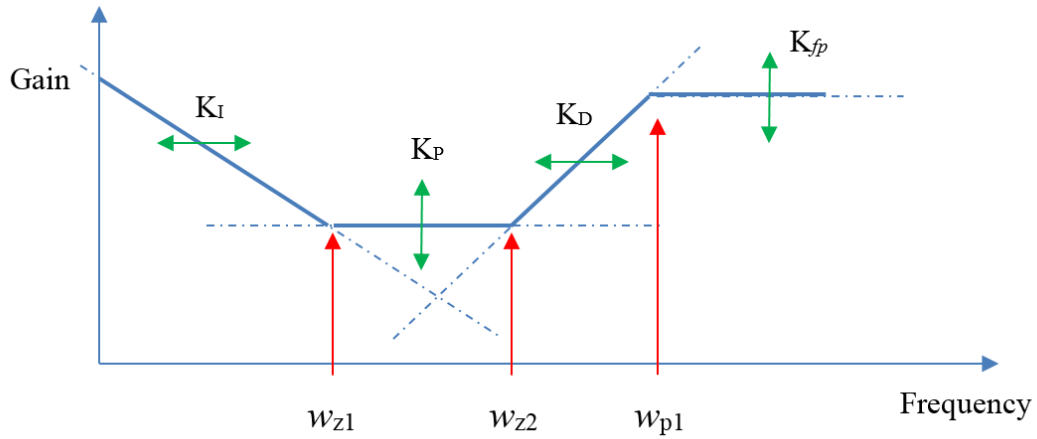
Figure 2. 6. Bode plot.

Figure 2. 6 shows the compensator gain in frequency domain. K_I and K_D are dominating in both low frequency and high frequency ranges. K_P maintains compensator gain in middle frequency range, which affects loop BW. K_{fp} is essential for high frequency noise reduction which rolls off loop gain at high frequency.

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2.2 Power Loss Analysis

In order to support various system running configuration, the VR design (multiphase + single phase) in server application need to cover the entire loading condition and then budget wisely. Figure 2. 7 shows a typical power budget in percentage scale.
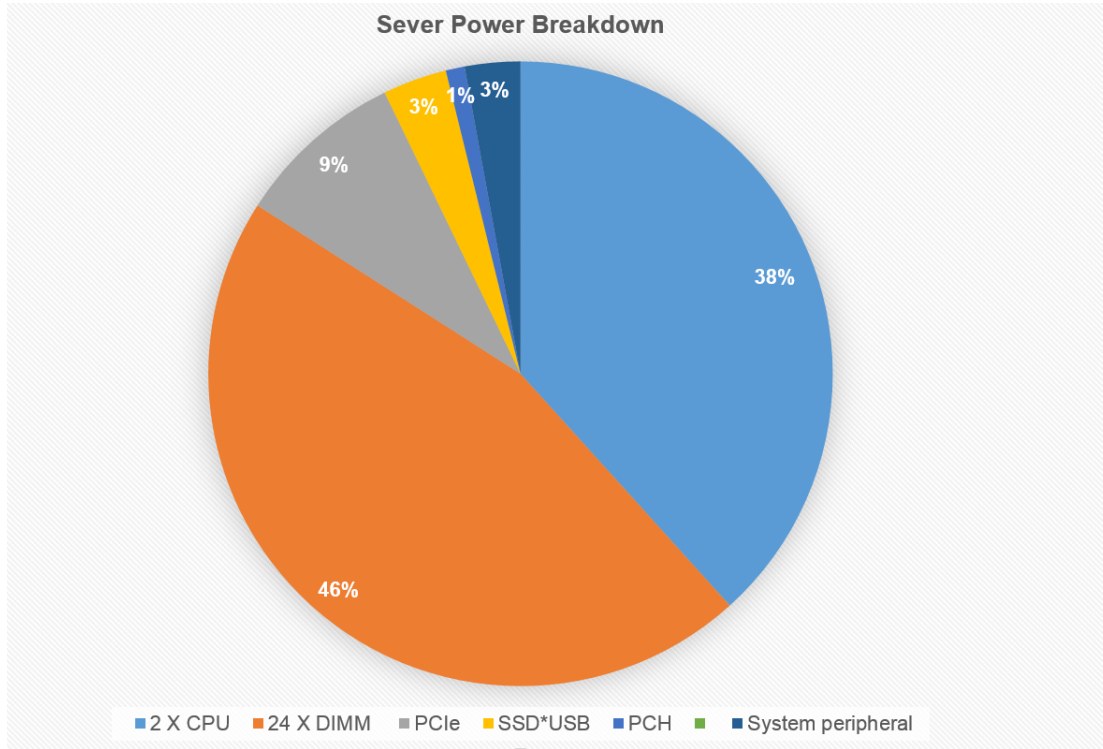
Figure 2. 7. A power design breakdown in server application.

The power conversion loss [26] - [29] should be understood well first then optimized accordingly. Due to the different operation modes of buck converter, the loss model is divided in three cases, CCM buck, CCM boost and PFM buck, respectively. The corresponding power loss representations with inductor current profiles are shown in Figure 2. 8, Figure 2. 10 and Figure 2. 19, respectively.
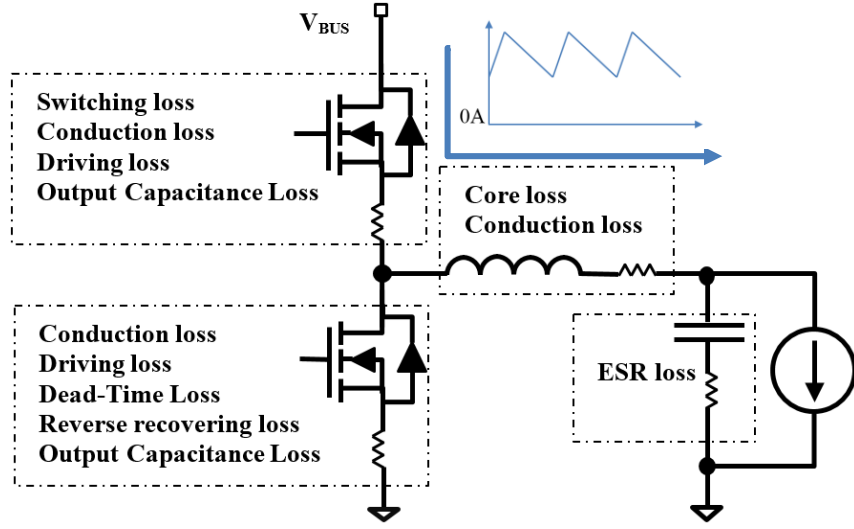
Figure 2. 8. Power loss distribution of a synchronous buck in buck mode.

Power loss simulation and experimental verification should be both carried out with varying switching frequency and PVCC(MOSFET drive voltage). The following equations shows power loss portion when the VR is operating in synchronous buck mode.

The recent development of power MOSFETs has been focusing on the ultra-low channel resistance and ultra-fast switching speed. FOM is a fast measure to gauge the MOSFET under the same breakdown voltage. Infineon's OptiMOS^{TM} and Fairchild Semi's PowerTrench$^{®}$ are considered industry leading technologies of low voltage power MOSFETs.

$$\text{FOM} = R_{ds\_ON} \cdot Q_g \tag{2.7}$$

The conduction loss is the resistive loss due to current conducted through the channel resistance R_{ds_ON}.

$$P_{COND} = I_{RMS}{}^2 \cdot R_{ds\_ON} \tag{2.8}$$

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$$I_{RMS(LS)} = \sqrt{\left(\frac{I_{out}^2}{N^2} - \frac{I_{ripple}^2}{12}\right)(1-D)} \qquad (2.9)$$

$$I_{RMS(HS)} = \sqrt{\left(\frac{I_{out}^2}{N^2} + \frac{I_{ripple}^2}{12}\right)D} \qquad (2.10)$$

P_{COSS} is the power loss caused by the output capacitance of MOSFET

$$P_{COSS} = 0.5 \cdot Q_{OSS} \cdot V_{BUS} \cdot f_{SW} \qquad (2.11)$$

$P_{deadtime}$ represents the body diode conduction loss during $t_{deadtime}$.

$$P_{deadtime} = V_{SD} \cdot f_{SW} \cdot \left[\left(I_{OUT} - \frac{I_{ripple}}{2}\right)t_{deadtime(r)} + \left(I_{OUT} + \frac{I_{ripple}}{2}\right)t_{deadtime(f)}\right] \qquad (2.12)$$

where V_{SD} is diode forward voltage drop; $t_{deadtime(r)}$ represents rising edge dead-time between LS turn off and HS turn on; $t_{deadtime(f)}$ represents rising edge dead-time between HS turn off and LS turn on.

P_{QRR}, the LS body diode reverse-recovery loss, is induced during the phase of turning off of the LS body diode.

$$P_{QRR} = Q_{RR(LS)} \cdot V_{BUS} \cdot f_{SW} \qquad (2.13)$$

where Q_{RR} is the excess minority carrier charge in the reverse recovery transient.
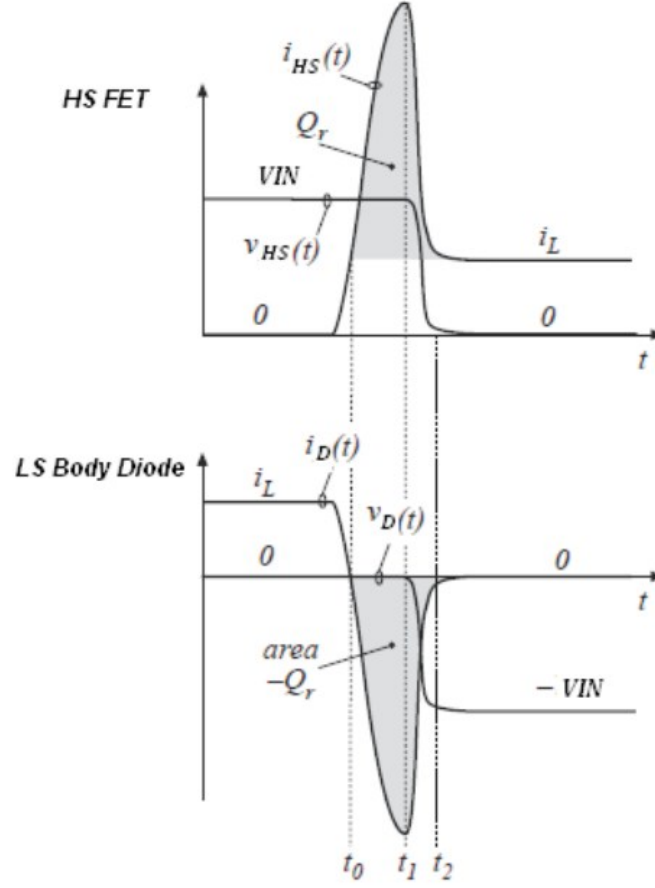
Figure 2. 9. Diode reverse-recovery waveforms

In the buck mode operation, the LS MOSFET is considered as soft switching. The HS MOSFET turn on/off loss incorporating common source inductance due to device package can be accurately calculated by:

$$P_{SW(ON)} = V_{BUS} \cdot f_{SW} \cdot \left(I_{OUT} - \frac{I_{ripple}}{2}\right) \cdot \left(\frac{\frac{0.5 \cdot Q_{gs2(HS)}}{V_{FET_{DR}} - V_{PL(HS)}}}{R_{g(HS)} + R_{driver} + L_{csi} \cdot \frac{I_{OUT} - \frac{I_{ripple}}{2}}{Q_{gs2(HS)}}} + \frac{\frac{0.5 \cdot Q_{gd(HS)}}{-(R_{g(HS)} + R_{driver}) + \sqrt{(R_{g(HS)} + R_{driver})^2 + 4\frac{L_{csi} \cdot Q_{OSS(LS)}}{Q_{gd(HS)}^2}(V_{FET_{DR}} - V_{PL(HS)})}}}{2\frac{L_{csi} \cdot Q_{OSS(LS)}}{Q_{gd(HS)}^2}} \right) \quad (2.14)$$

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$$P_{SW(ON)} = V_{BUS} \cdot f_{SW} \cdot \left(I_{OUT} + \frac{I_{ripple}}{2}\right) \cdot \left(\frac{\frac{0.5 \cdot Q_{gs2(HS)}}{V_{PL(HS)}}}{R_{g(HS)} + R_{driver} + L_{csi} \cdot \frac{I_{OUT} + \frac{I_{ripple}}{2}}{Q_{gs2(HS)}}} + \frac{0.5 \cdot Q_{gd(HS)}}{\frac{-(R_{g(HS)} + R_{driver}) + \sqrt{(R_{g(HS)} + R_{driver})^2 + 4 \frac{L_{csi} \cdot Q_{OSS(LS)}}{Q_{gd(HS)}^2}(V_{PL(HS)})}}{2 \frac{L_{csi} \cdot Q_{OSS(LS)}}{Q_{gd(HS)}^2}}} \right) \quad (2.15)$$

where I_{OUT}, V_{BUS}, V_{FET_DR}, R_g, V_{PL}, R_{driver}, Lcis, Q_{ds} and Q_{gd} are the output current, Bus voltage, gate drive voltage, gate drive resistance, HS MOSFET plateau voltage, HS MOSFET source inductance, current, HS MOSFET Q_{ds} and HS MOSFET Q_{gd}, respectively.

The gate charge induced loss:

$$P_{gate} = (Q_{g(HS)} + Q_{g(LS)}) \cdot V_{FET\_DR} \cdot f_{SW} \quad (2.16)$$

The switching frequency and V_{FET_DR} should be optimally selected based on the minimum power loss.
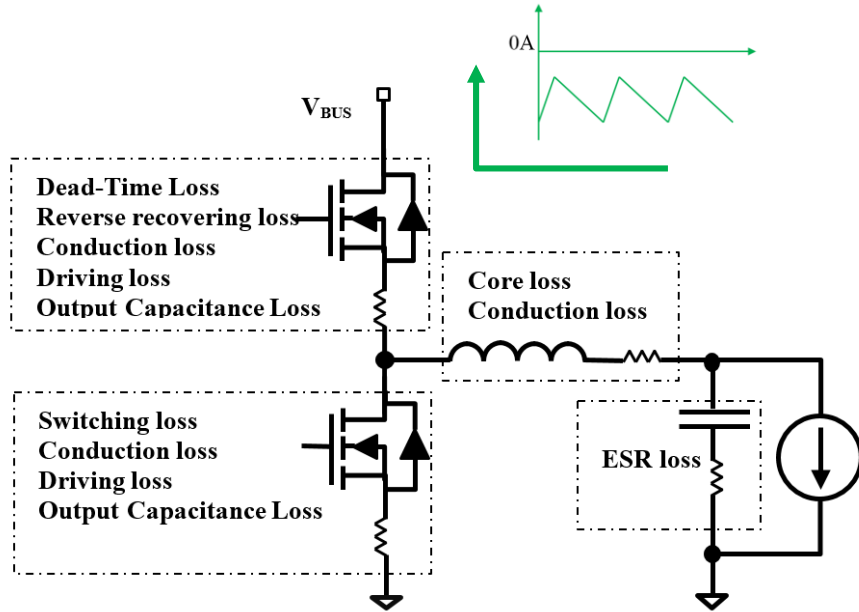
Figure 2. 10. Power loss distribution of a synchronous buck in boost mode.

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When the inductor current flow reversely, as shown in Figure 2. 10, the converter is enforced working in sink mode, or boost mode. The loss formulas change accordingly. HS power MOSFETs are soft switching.

$$P_{QRR} = Q_{RR(HS)} \cdot V_{BUS} \cdot f_{SW} \tag{2.17}$$

LS power MOSFETs are consequently hard switching in the boost mode. The simplified turn ON/OFF losses are:

$$P_{SW(ON)} = (V_{BUS} + V_{SD}) \cdot f_{SW} \cdot \left(I_{OUT} + \frac{I_{ripple}}{2}\right) \cdot \left(\frac{Q_{SW}}{\frac{V_{FET\_DR} - V_{PL}}{R_g + R_{driver}}}\right) \tag{2.18}$$

$$P_{SW(OFF)} = (V_{BUS} + V_{SD}) \cdot f_{SW} \cdot \left(I_{OUT} - \frac{I_{ripple}}{2}\right) \cdot \left(\frac{Q_{SW}}{\frac{V_{FET\_DR} - V_{PL}}{R_g + R_{driver}}}\right) \tag{2.19}$$

2.3 Driver Interface

One phase of the multiphase synchronous buck converter with the dead-times management is shown in Figure 2. 11. Dead time $t_{dead-time}$ [30] during which both power MOSFETs (Q_1 and Q_2) are off, is inserted between the gate signal cycle to avoid cross-conduction and guarantee safe operation of the circuitry. There is another dead time which is very critical in the driver IC design for the DVID downward operation, i.e. watch-dog timer $t_{watch-dog}$, which is defined as from HS gate signal is low and switch node is still high, after this defined time length, the LS MOSFET is turning on. The detailed analysis of system impact by $t_{watch-dog}$ is in chapter V.
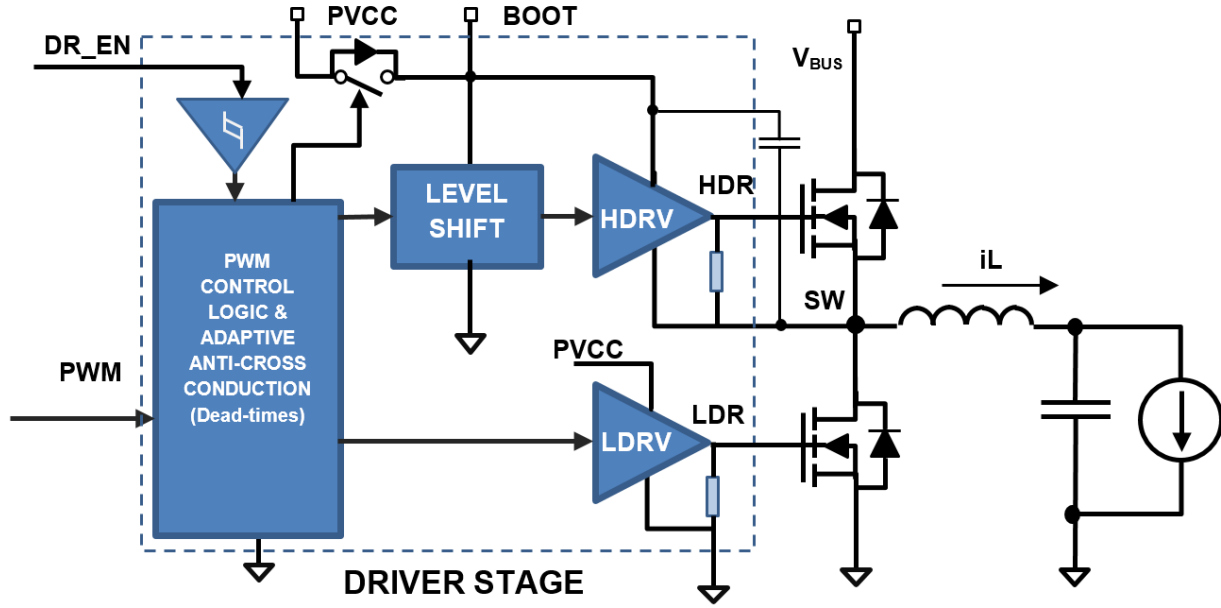
Figure 2. 11. Driver IC block diagram with proposed dead-time management.

Dead-time must be sufficient enough to guarantee no cross conduction between high & low side MOSFETs. However, a longer dead-time will bring in more switching power loss to a VR since the body diode but not channel of low-side MOSFET turn on during dead-time. On the other hand, a shorter dead-time may increase risk of cross-conduction. Therefore, Dead-time management is critical in a MOSFET driver, which will directly impact VR efficiency and reliability.

The discrete driver dead-time design should consider MOSFET parameter variation (R_G, C_{ISS}, $V_{GS(TH)}$) and the dead-time should be adaptive to the MOSFETs. The adaptive dead-time scheme measures the actual voltage on the gate and only when the voltage on the gate is below a proper value (1V, since this is a good value for 90% of the MOSFET), the transition is allowed to turn on the other gate. Adaptive dead-time control has been used in a general MOSFET driver

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circuitry that can drive discrete MOSFETs. Adaptive dead time is the improvement of the long fixed dead-time (fixed delay block). As a result, actual dead-time is usually pretty long (12ns is the best from industrial leading suppliers).Dead-time impacts the system efficiency as discussed in (2.12). To reduce the dead-time and Q_{RR} loss, LS Schottky barrier diode (V_{SD} = 0.56V, Infineon BSC014NE2LSI) should be incorporated in the design. By calculation, adding extra 5 ns dead-times will result in 0.2% of efficiency penalty.

Integrated power stage containing MOSFETs and driver has been increasingly used in recent years especially for high density design such as blade server. In order to boost the power conversion efficiency, the fixed driver dead-time with simpler logics can be used in a power stage since parasitic MOSFET parameters inside power stage package is predictable and in a relatively small variation range. However, the fixed driver dead-time may create a shoot-through scenario in a multiphase VR when the shedded phases are in tri-state for a long period, then recovered to operation mode. Both MOSFETS are kept in the OFF state when the driver receives a PWM tri-state signal.

PWM and DR_EN are both control input signals for driver IC which are generated by the state machine of PWM controller. Figure 2. 12 shows the timing diagram of driver interface with HiZ management. HiZ here refers to the high-impedance stage by keeping all MOSFETs in off state. HiZ window is defined as voltage range of the PWM between 1.2 V and 2.2 V for a 3.3 V application. t_1 and t_3 represent propagation delay of LS Gate and HS Gate, respectively. t_2 and t_4 represent dead times from LS falling and HS falling, respectively. t_5 and t_8 both represent hold-off times. t_6 and t_7 represent propagation delay of DR_EN rising and falling.
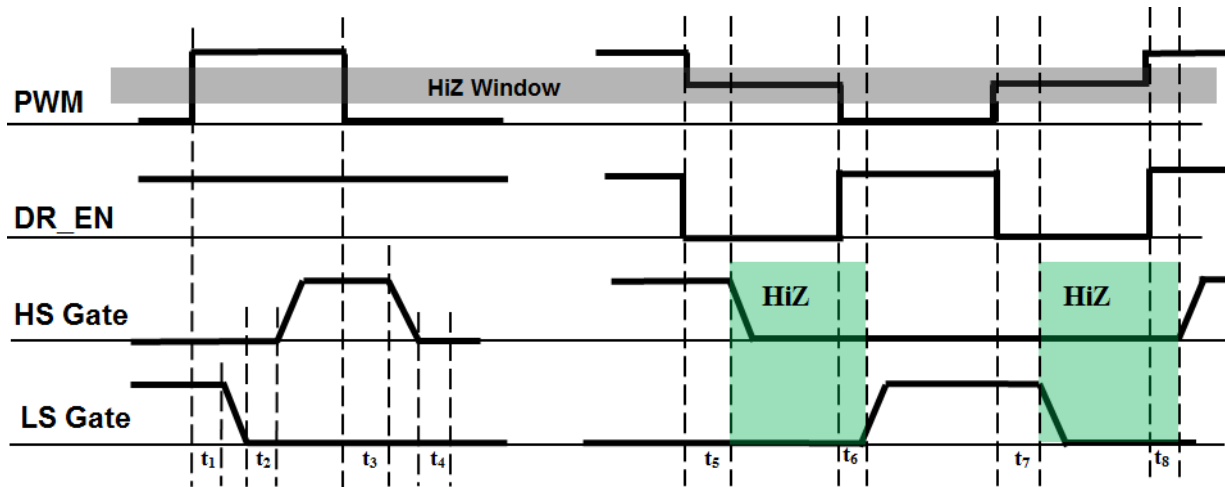
(a) (b)

Figure 2. 12. Timing diagram of driver interface: (a) DR_EN is asserted; (b) DR_EN is toggling during operation.

Figure 2. 13 shows timing diagram of the boot switch which is embedded inside of driver. The boot switch is ON when the LS is ON to charge the bootstrap capacitor. The boot switch is OFF when the HS is ON. During PWM HiZ, the switch must remain OFF since the negative current can discharge the boot cap if the switch is ON.
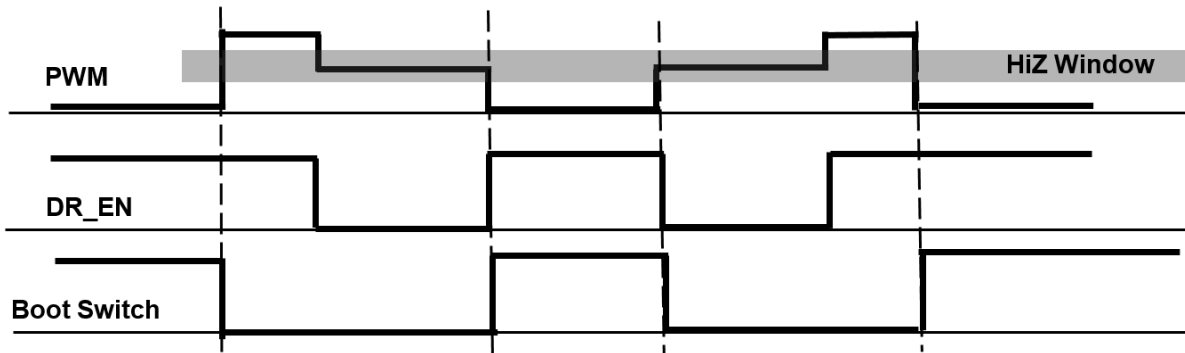
Figure 2. 13. Timing diagram of driver interface: PWM vs. Boot switch.

To obtain the optimum static efficiency for the whole load range, not only the lower FOM of power MOSFETs should be employed, the driver capability and the parameters associated with the power loss should be carefully studied and optimally defined. Finally, phase shedding control needs to be implemented to improve the efficiency in mid-light load, and the control thresholds are the intersection points of adjacent phases in efficiency plot.

Table 2. 1 DIVER DEFINTION

Upper driver source/sink current	2A / 2A
Upper driver source/sink impedance	0.8 Ohm / 0.6 Ohm
Lower driver source/sink current	2A / 4A
Lower driver source/sink impedance	0.8 Ohm / 0.35 Ohm
$t_{deadtime(f)}$	8 ns
$t_{deadtime(r)}$	15 ns

It's very important to correctly define and strengthen the driving capability of the power MOSFETs driver to minimize the HS switching loss during commutation (the overlapped area). TABLE I shows the definition of driving capability and dead times. The low sink impedance is extremely important to avoid Cdv/dt induced turn on phenomenon (shoot-through) [32] in the LS MOSFET during the fast turn on of HS MOSFET.
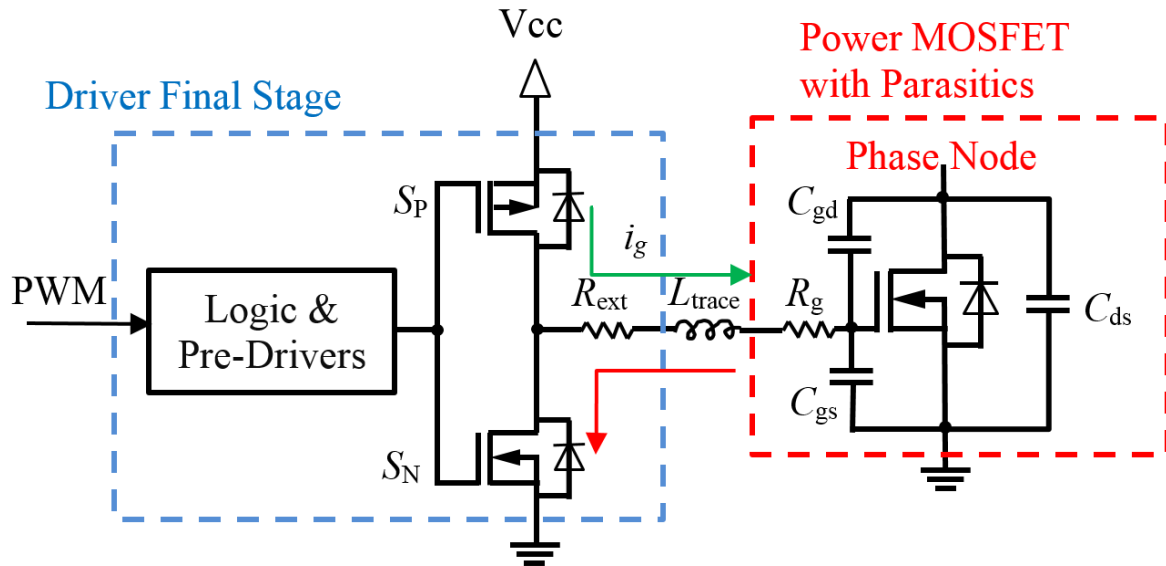
Figure 2. 14. LS turning ON/OFF.

Figure 2. 14 shows color coded procedures of LS MOSFET turning ON/OFF. The speed of turning ON and OFF is limited by the parasitic RLC as illustrated in the loop. The red arrows in Figure 2. 15 represents the peak source and sink current, respectively. Sink current needs to be bigger to avoid the shoot-through. There is also a need of minimum OFF time latch in the driver design to ensure the energy on the gate are fully discharged when turn OFF.
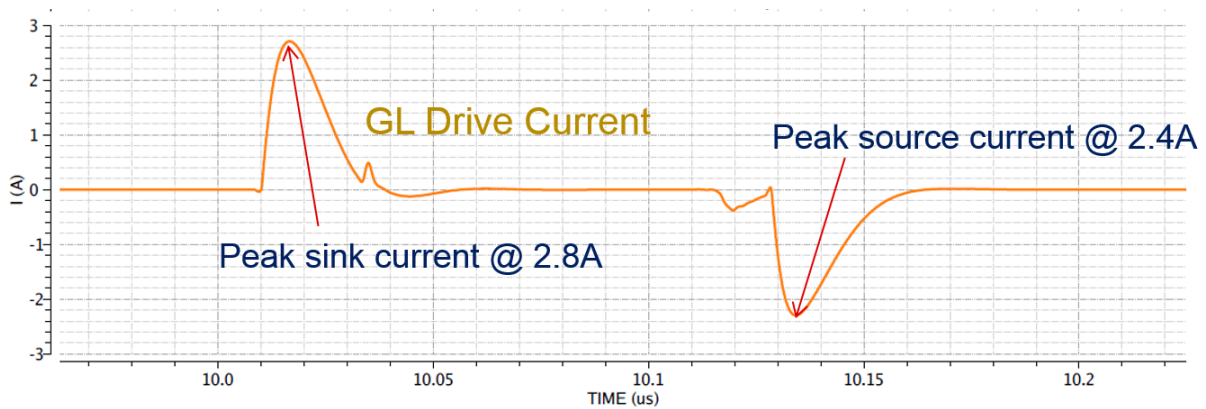
Figure 2. 15. Simulation result of LS turning ON/OFF.
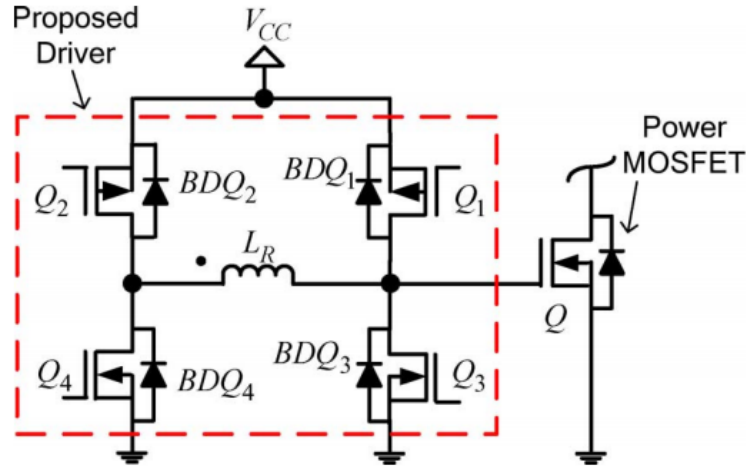
Figure 2. 16. An example of resonant gate-drive circuit.

Figure 2. 16 [33] shows a resonant gate driver structure. It is an interesting idea that the energy on the gate can be recovered by the resonance [33] - [35] . However, it is not applicable for the hard switching design. The loss analysis from the previous section reveals that the gate drive loss is only the smallest portion in a typical design. Moreover, a resonant gate driver puts timing constraints on the switching transitions (MOSFETs are not driven hard) and the switching goes from inductively limited to MOSFET limited. That means that the dynamic losses will increase substantially. The only way to resolve this is to have an entirely resonant buck topology. With the larger phase currents, this offsets the benefits by additional conduction loss.

2.4 Light Load Operation

Reducing power conversion loss during light load is one of the major focus in computing industry [36] [37] The power saving features should be implemented in VR. In this dissertation,

we treat the terms, diode emulation (DE), discontinuous conduction mode (DCM), pulse skipping, and pulse frequency modulation (PFM) the same.

The voltage gain during PFM can be found:

$$M = \frac{2}{1 + \sqrt{1 + \frac{8 I_{OUT} L}{T_{ON}^2 f_{SW}}}} \tag{2. 20}$$

where $M = {V_o}/{V_{in}}$, T_{ON} is the ON time of the control MOSFET. L is the per phase inductance. I_{OUT} is the load current.
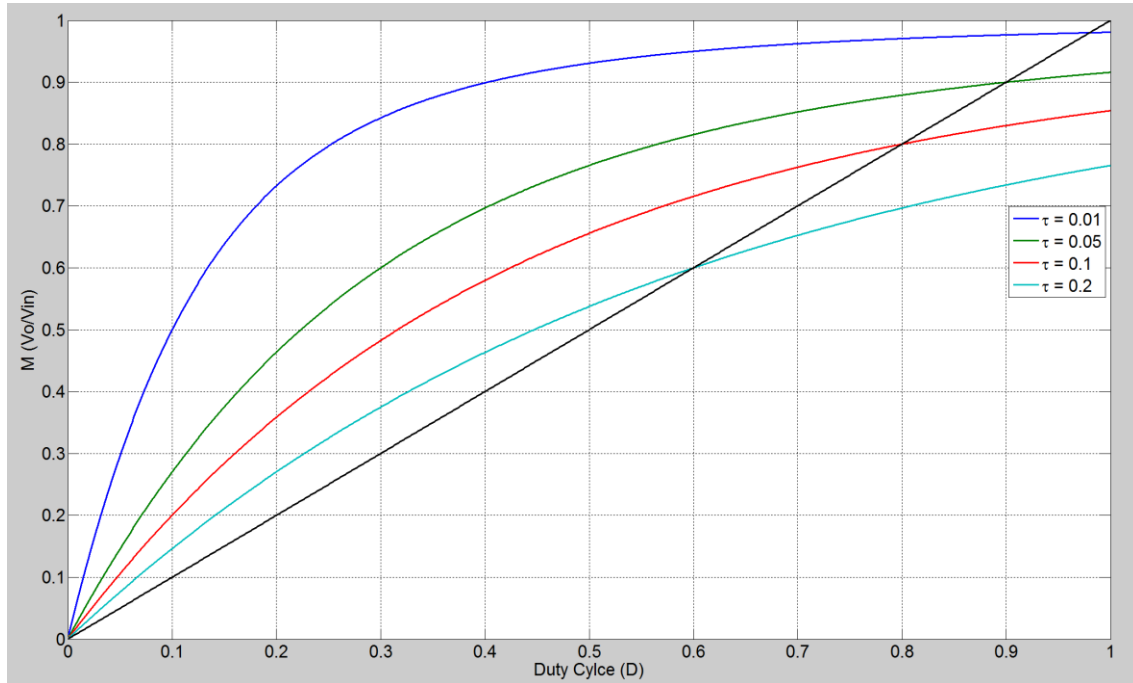
Figure 2. 17. Transfer ratio M vs. duty cycle D.

Assume T_{ON} is constant during PFM, the f_{SW} is linearly proportional to the load current to achieve the same regulation of the output voltage. Therefore, the light load efficiency can be improved since the switching frequency can be decreased based on the load condition.

From Figure 2. 12, we can easily find

$$\tau = I_{OUT} L f_{SW} \qquad (2.21)$$

τ is the normalized inductor time constant.

When CPU is in idle state, it is normally the condition of load current less than half of the inductor current ripple. The VR should be operating in PFM to reduce power loss [36] [37] However, once the VR receives the dynamic VID transition command, the VR should be able to immediately transition from PFM to CCM operation. It is noted that the VR is not able to sink current in PFM, which means downward transition cannot be accomplished in this mode.
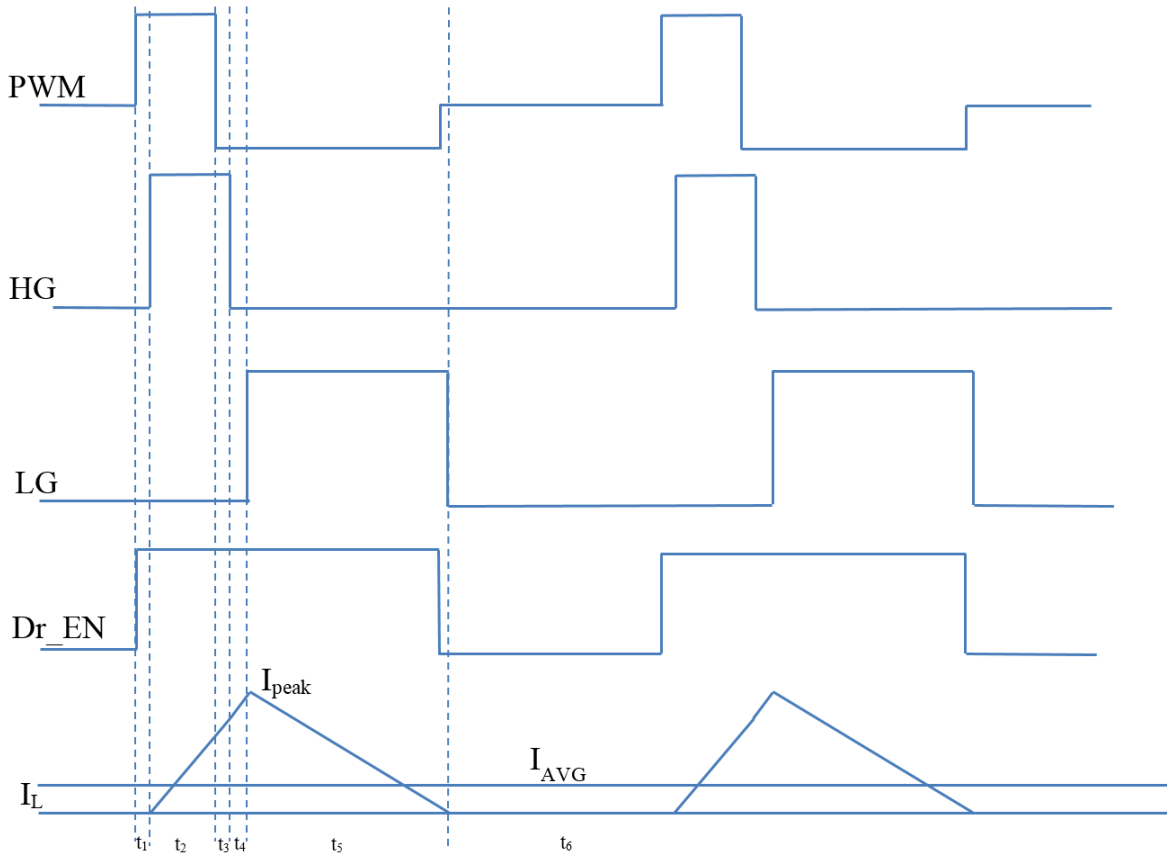
Figure 2. 18. Operational waveforms of PFM operation.

In PFM, as shown in Figure 2. 18, PWM transitions from HiZ to high. Phase node moves from output voltage level to V_{BUS}. To achieve fast HiZ operation as depicted in Figure 2. 12(b), EN toggle should be utilized in PFM operation. When the inductor current reaches zero, the LS is turning off. The output voltage then decays as a function of load. Power MOSFETs remain HiZ until the output voltage drop below the regulation target to trigger a PWM on pulse. If the turn off LS operation is through PWM entering tri-state (slow HiZ operation), the hold-off time would create a delay and then negative inductor current.
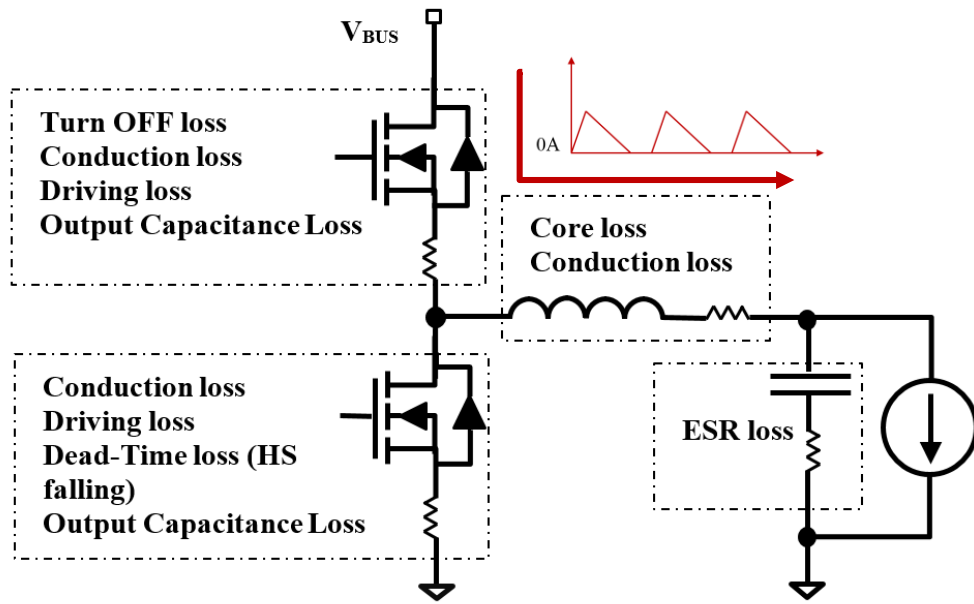
Figure 2. 19. Power loss distribution of a synchronous buck in PFM.

Other than the reduced loss caused by reduced switching frequency, there are several other loss items eliminated in PFM as well. There is no turn ON loss in HS due to ZCS. LS body diode reverse recovery loss is gone since there is no current freewheeling during HiZ time period.

Similarly, there is no HS rising dead-time loss if accurate zero current detection scheme can be implemented. The power loss in PFM is summarized in Figure 2. 19.
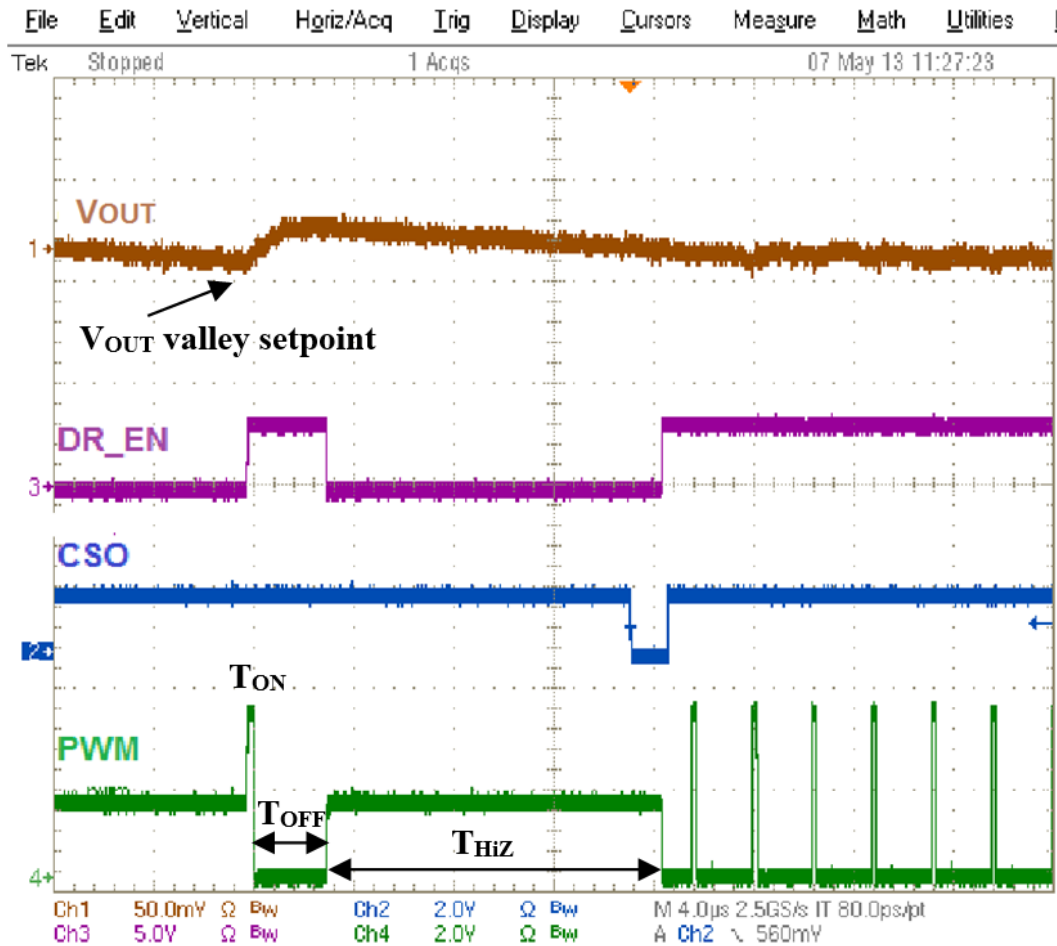
Figure 2. 20. PFM to CCM transition (load: 1 A).

Figure 2. 20 shows the mode transition from PFM to CCM initiated by power stage change. PWM ON time pulse is triggered by the V_{OUT} below the setpoint. The T_{ON} pulse is calculated by incorporating the converter parameters and V_{OUT} ripple requirement. T_{OFF} pulse is estimated by zero current crossing. T_{HiZ} is depending upon the load condition. The bigger

voltage ripple in PFM is expected due to the excessive charge of inductor ripple current (minus load) built upon the output capacitor compare to CCM operation.

2.5 Switching Waveforms

Switching waveforms, LS V_{DS}, LS V_{GS}, HS V_{DS} and HS V_{GS}, are critical parts of evaluating the robustness of the VR design. The waveforms should be within the defined range so that the MOSFETs are not stressed and thus the reliability is not a concern. Since the measurements can be only taken at the pins of the package, not the silicon die, it is needed to study the delta between the measured waveforms at the pin and at the die. Having a good understanding of the above waveforms are essential to optimize the overall VR design.
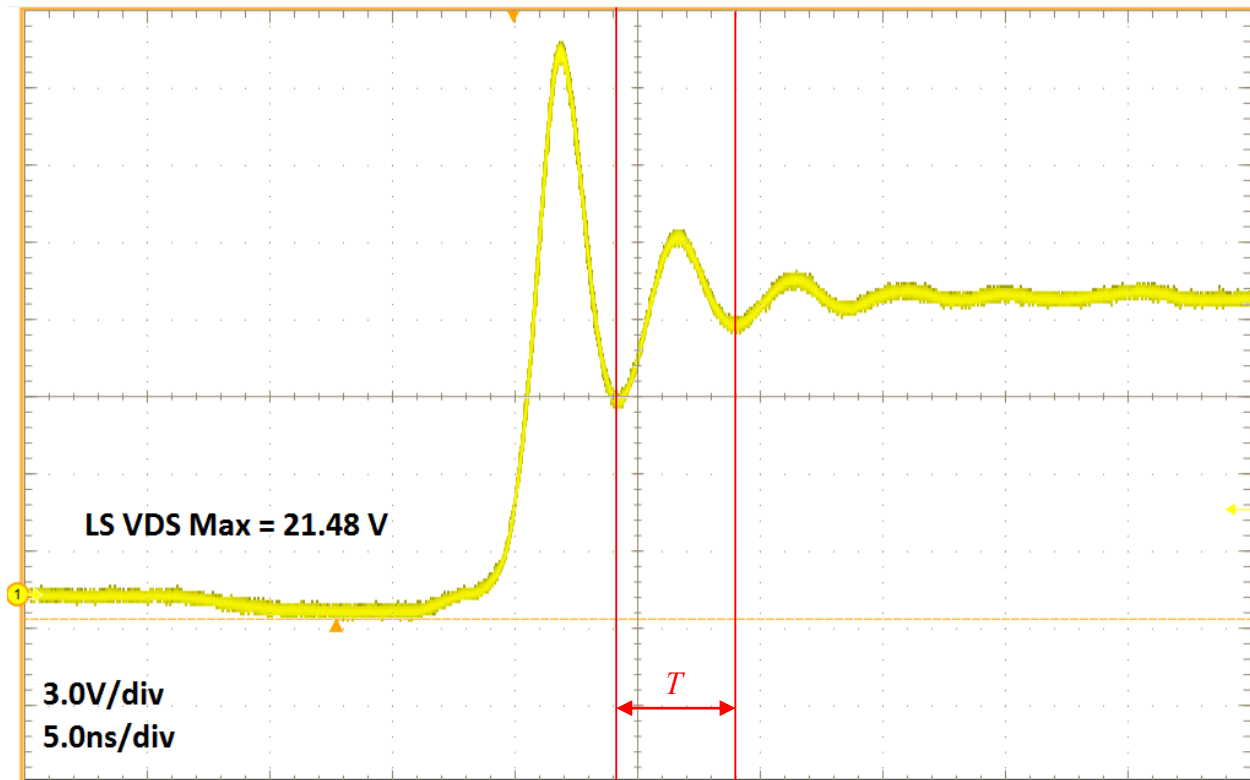
Figure 2. 21. LS V_{DS} rising waveform due to diode reverse recovery.

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$$L_{para} = \frac{T^2}{(2\pi)^2 C_{OSS}}$$

(2. 22)

Since the C_{OSS} can be looked up from the curve in the datasheet, therefore, L_{para} can be calculated by using (2.22).
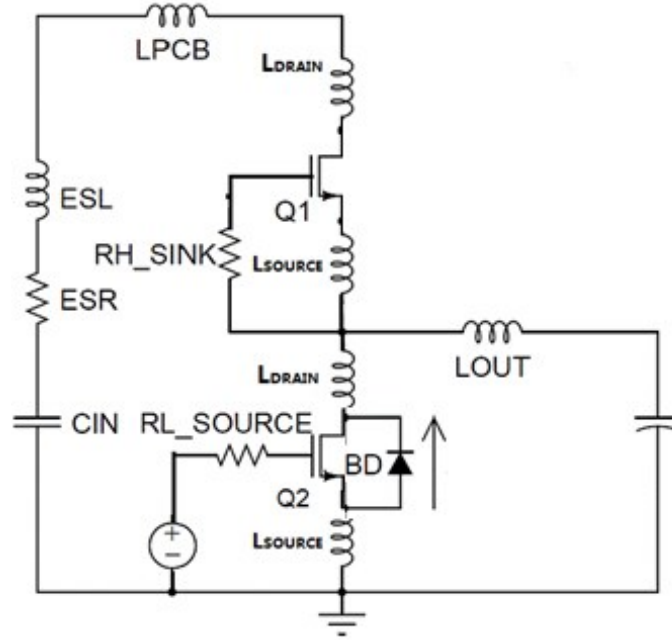
Figure 2. 22. Discrete solution of the converter considering circuitry parasitics in the buck mode.
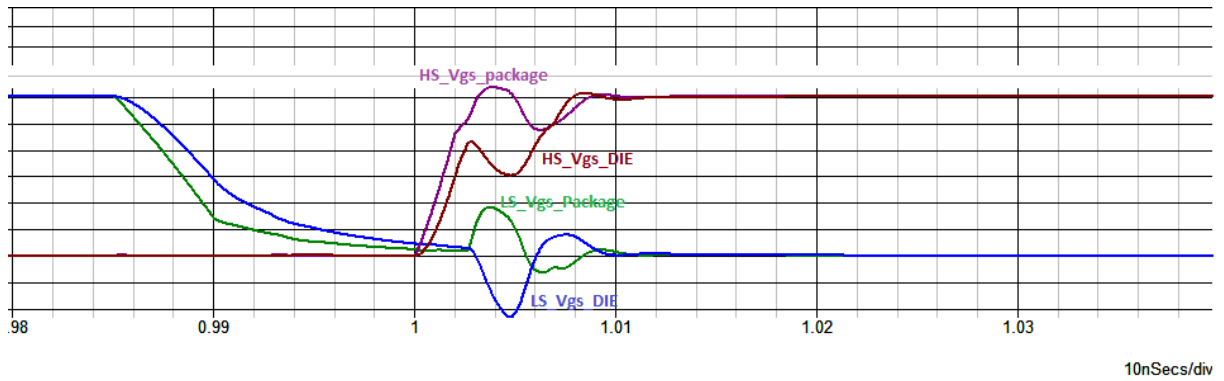
Figure 2. 23. Simetrix simulation of Gate waveforms.

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Figure 2. 23 shows the simetrix simulation of gate drive waveforms comparison. There is a quite big delta between the actual waveform on the silicon die and the waveform on the package. There is a shoot-through concern of LS bump back, as depicts in green curve, however, the measurement result is misleading since it includes the parasitics and the real waveform on the silicon die is very low, as depicts in blue curve, the peak of which is lower than the $V_{GS(th)}$ of LS MOSFET.
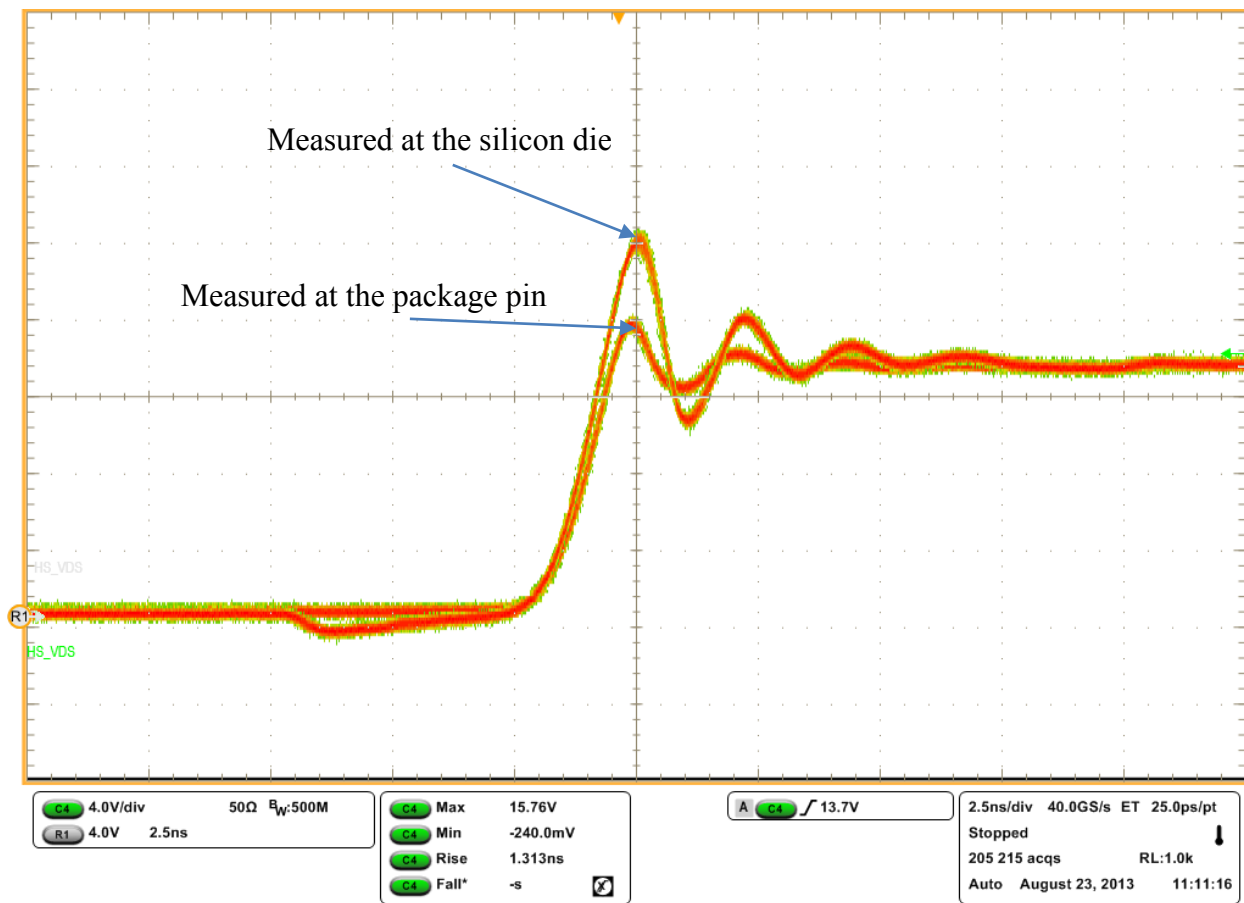
Figure 2. 24. HS V_{DS} waveforms comparison.

Figure 2. 24 shows the HS V_{DS} waveform measured at the power pin (source) on the package and at the silicon die as the arrows indicate. As depicted clearly in the fast acquisition

scope shot, the true V_{DS} is around 4V more than the result usually taken at the package. The voltage delta is caused by the combination effect of fast di/dt and source clip inductance.

<p style="text-align:center">2.6 Efficiency Optimization</p>

It is critical to optimize the static efficiency of power stage first since it is one of the key performance metrics of the VR design. Load adaptive control (LAC) is proposed and experimentally verified. The multiphase VR operation mode and phase number is the function of the load current. FET drive voltage should also be adaptively adjusted to achieve the optimal efficiency. Switch frequency, f_{SW}, should be optimally chosen with nonlinear control loop enabled so that the relatively low switching frequency would not impact the load transient behavior.
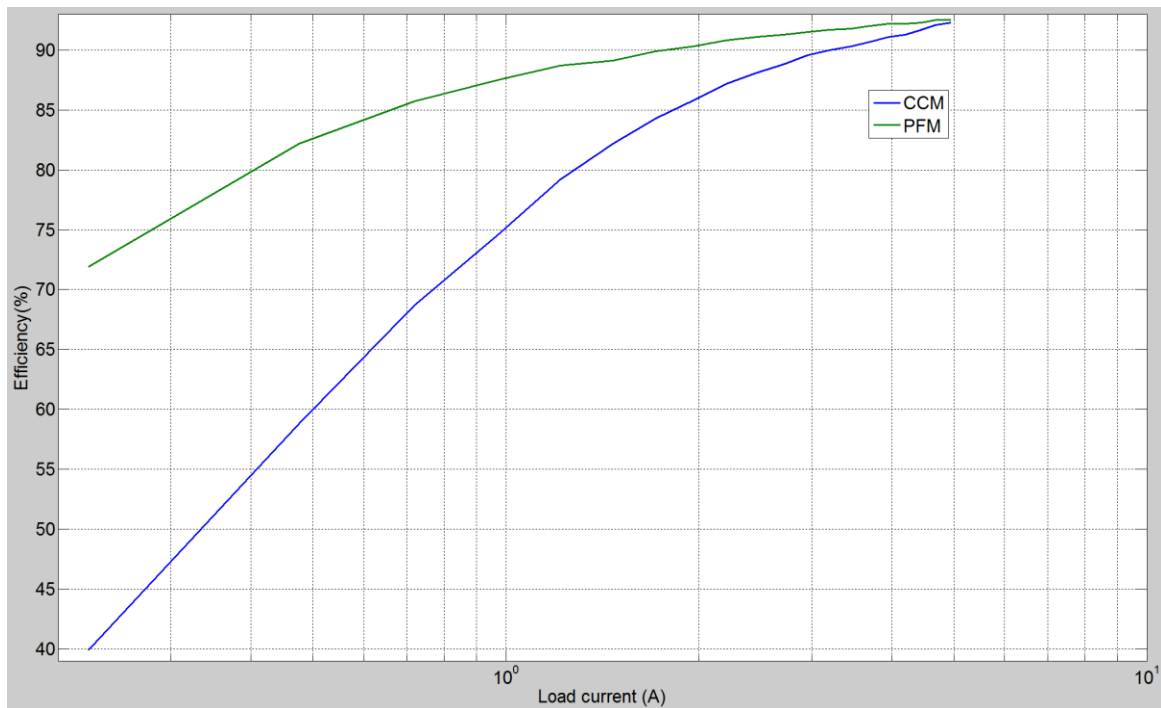
Figure 2. 25. Light load CCM vs. PFM.

Figure 2. 25 shows the efficiency comparison at light load. PFM operation shows a big advantage over CCM operation as expected and two curves are eventually converged at the load which is around half of the inductor current ripple.
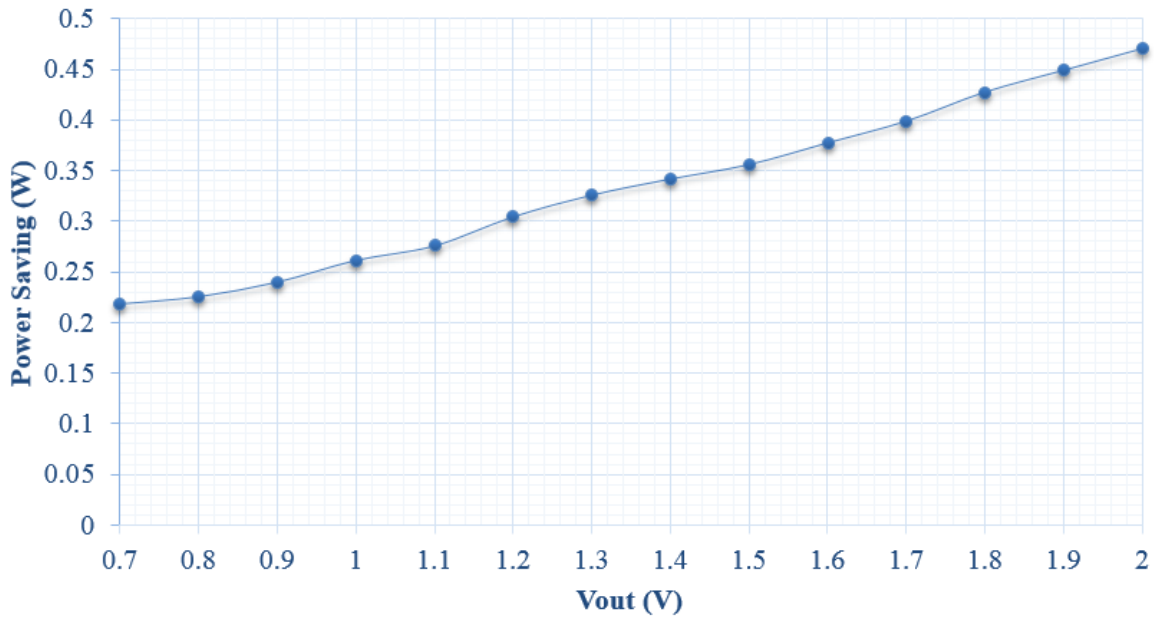
Figure 2. 26. Power loss reduction (PFM minus CCM) vs. VID.

Figure 2. 26 shows the power saving plot with increasing V_{OUT} with 10mA of load current. As the V_{OUT} increases, it becomes more important to enable the VR working in the PFM when the load current is small.

Converter parameters are in TABLE I, except for the disabled LL. V_{OUT} is regulating at 1.05 V and measured at the output inductor. A GPIB based automated efficiency program, which communicates to the data acquisition unit (Agilent 3497A) and electric load (Sorensen).is written to record, V_{IN}, I_{IN}, V_{OUT}, I_{OUT}, V_{FET_DR}, I_{FET_DR} and plot the efficiency curve.
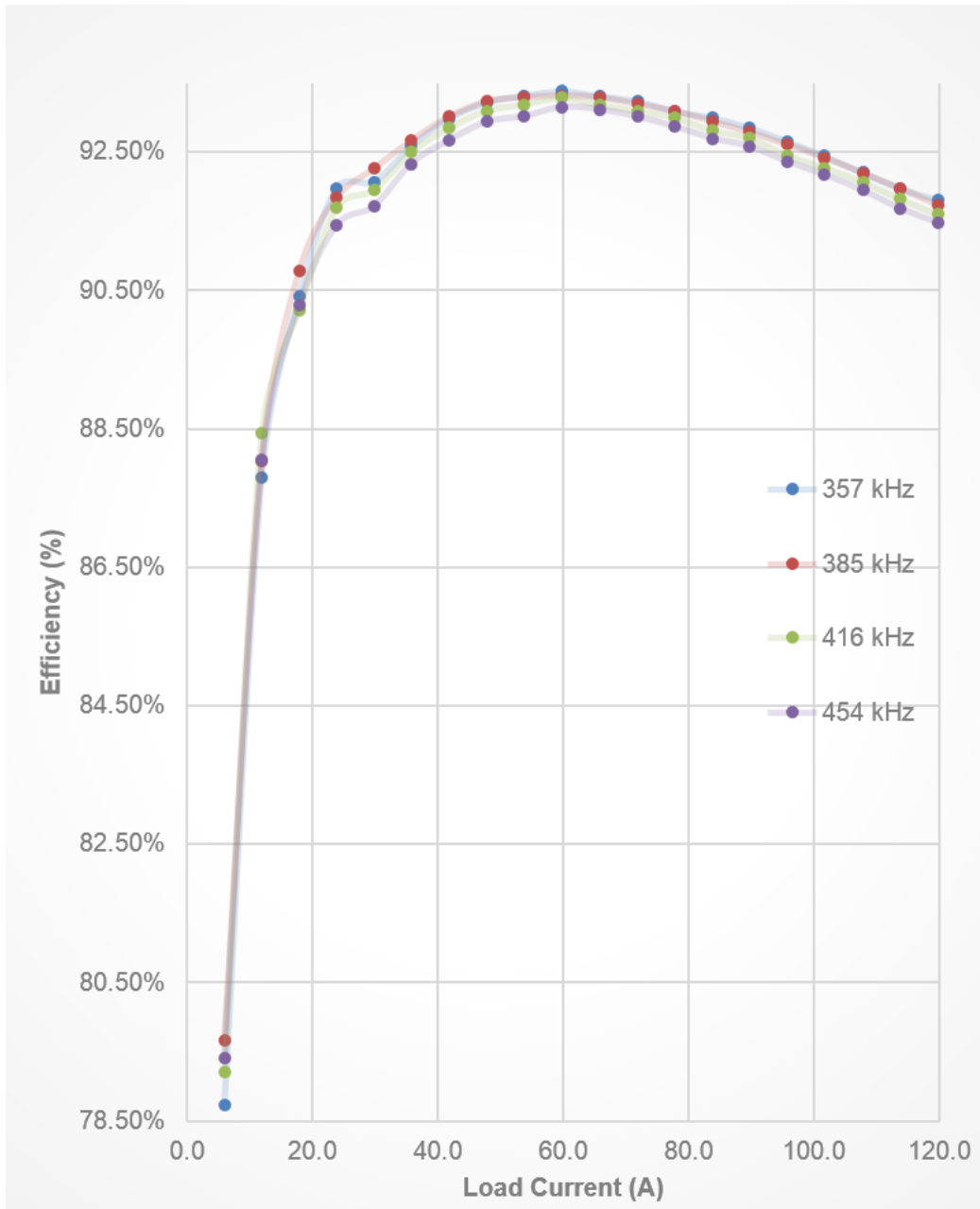
Figure 2. 27. Efficiency vs. switching frequency.

Switching frequency, f_{SW}, is the key parameter that needs to be optimized for achieving optimum efficiency. Figure 2. 27 shows the efficiency comparison between different f_{SW} cases.
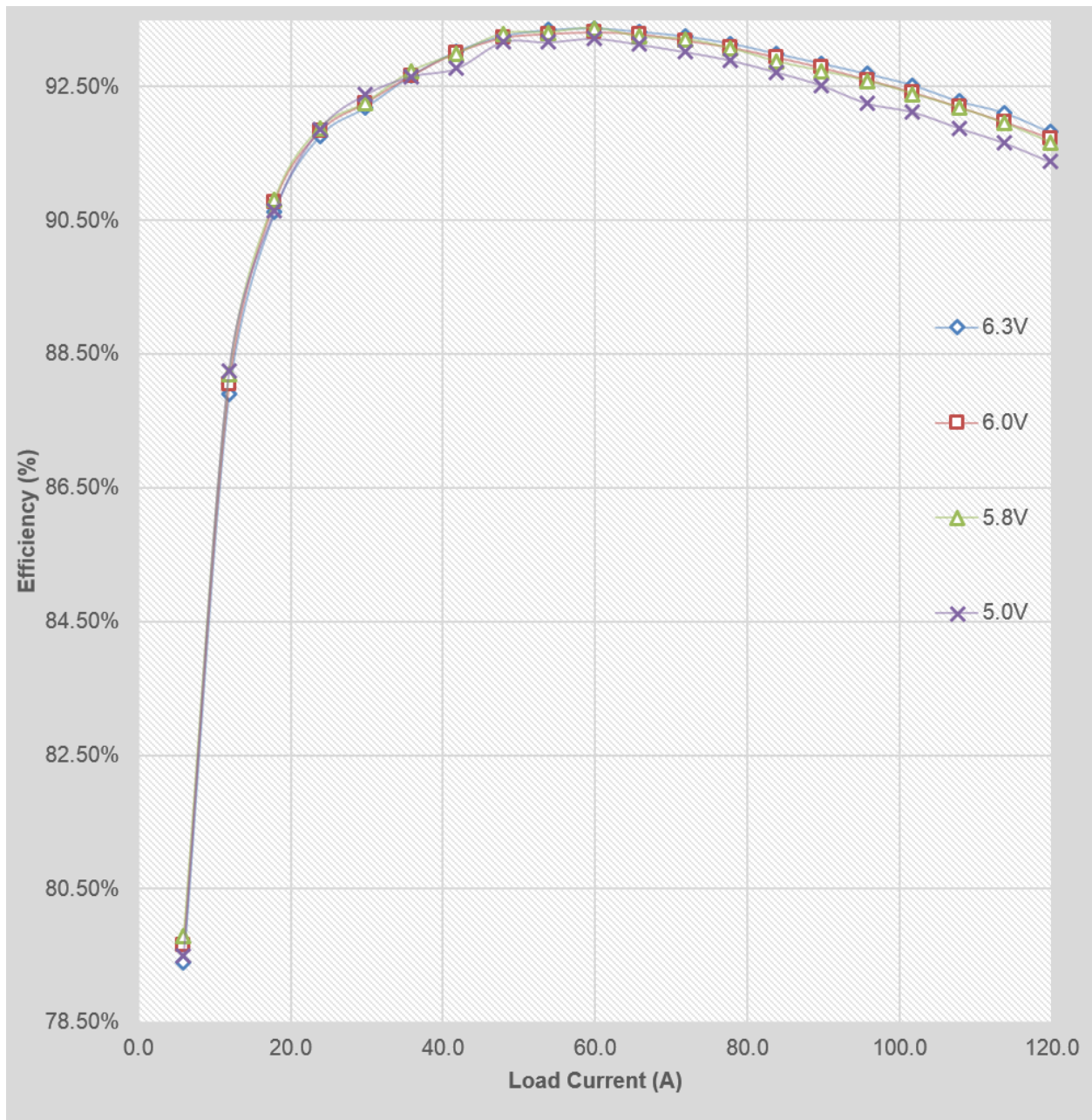
Figure 2. 28. Efficiency vs. FET drive voltage.

The driver voltage of power MOSFETs is also an important parameter to be optimized. In the total power loss formula, it affects the Rdson of (2.6) and (2.14).

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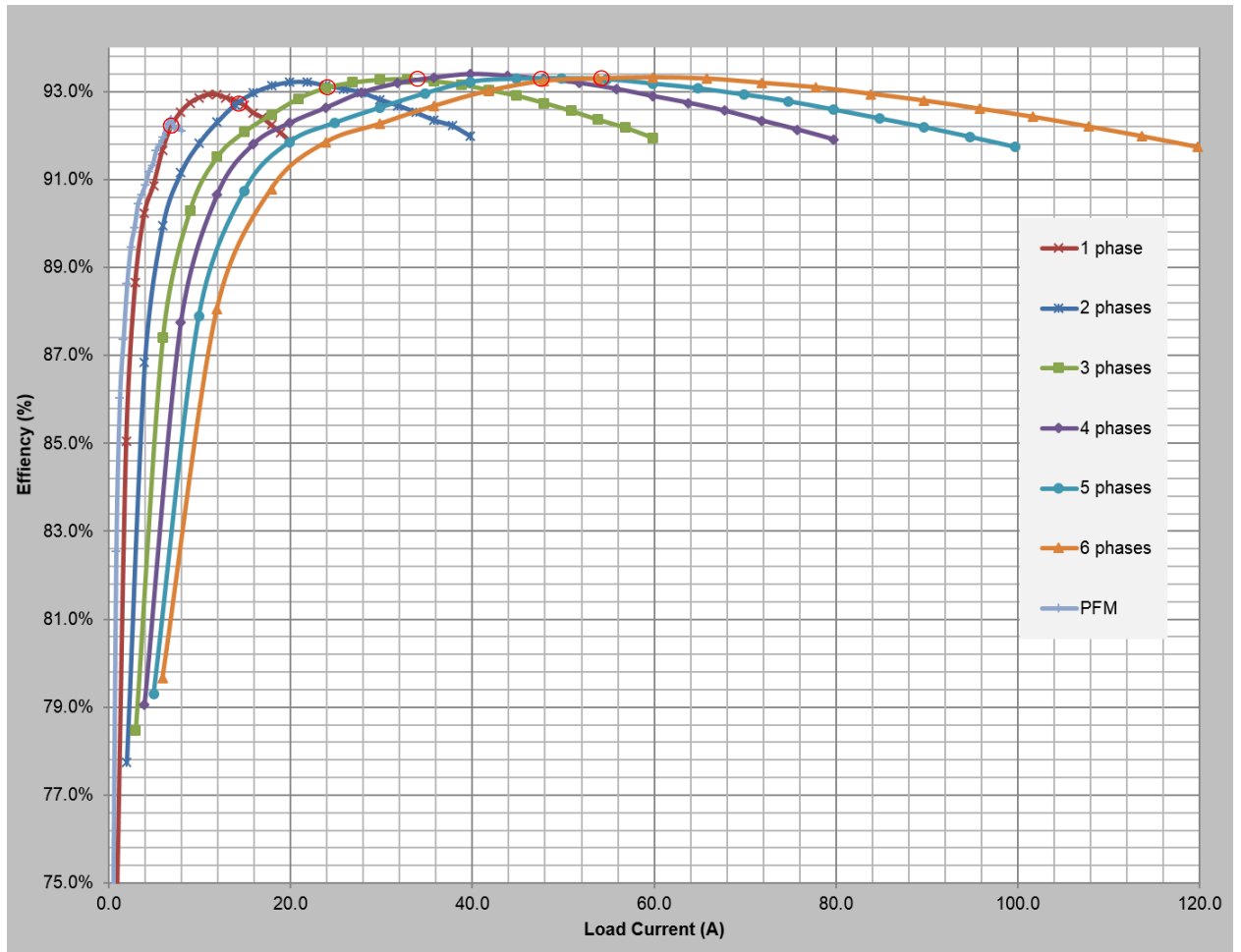
Figure 2. 29. Measured efficiency of multiphase buck converter with operating different number of phases.

Figure 2. 29 shows the measured efficiency plot of multiphase buck converter with statically configured operation modes and different number of phases. There are in total seven cases in this plot: one phase PFM and one to six phase CCM. The cross points between adjacent phases operation can be programmed into the non-volatile memory (NVM) for this specific power stage for auto phasing shedding purpose to flatten the efficiency curve over the entire load range.
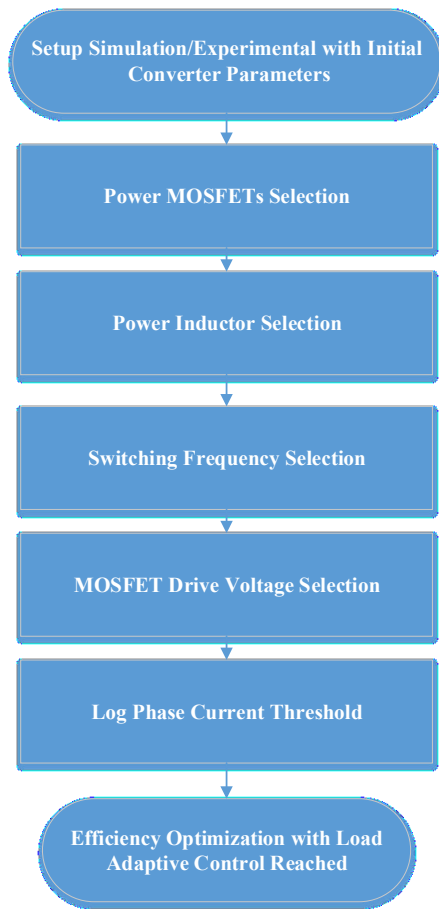
Figure 2. 30. Power efficiency optimization flow chart.

Table 2. 2 THE CONVERTER PARAMETERS

V_{BUS}	12 V
V_O	0.7 V~1.2 V
V_{FET_DRV}	6.0 V
f_{sw}	385 kHz
Loadline slope	0.8 $m\Omega$
Output inductor per phase	L = 230 nH
Output capacitor	6×470 μF Panasonic SP-Caps EEFSX0D471XE
	44×22 μF MLCC
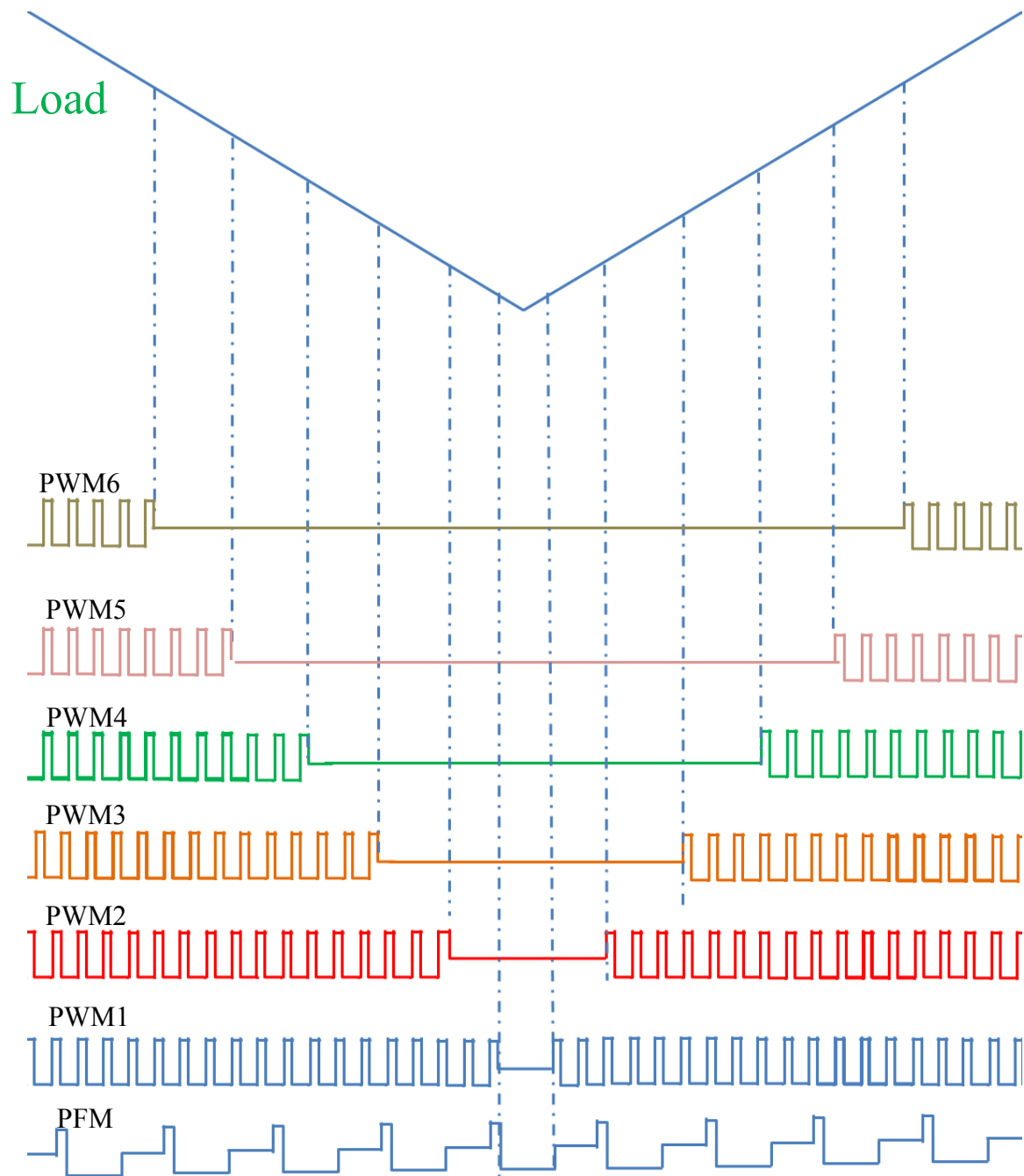
Figure 2. 31. Diagram of Load adaptive control.

Figure 2. 31 shows the diagram of load adaptive control based on previous optimization

results.

CHAPTER THREE: LOW FREQUENCY TRANSIENT AND SYSTEM DYNAMIC

In this chapter, load transient enhancement schemes are introduced for low frequency transient operation. Adaptive body braking control is proposed to actively suppress the load release. There is a consideration for dynamically adding and dropping phases so that the V_{OUT} excursion can be minimized. Load adaptive control has provided the benefit in power saving perspective, however, it also creates a corner case scenario that shoot-through can be induced. Hence, we propose a new dead-time management scheme incorporating both fixed and adaptive dead-times so that the system reliability is secured and the power conversion efficiency during normal operation is improved.

3.1 DCR Sense Network Impact

Accurate load current monitoring is an important feature and requirement in multiphase converter design. The RC network across the definition points of the inductor can be implemented to monitor the total phase current. The first design tuning in transient operation to make the DCR sense match.

$$\frac{L}{DCR} = RC \tag{3.1}$$

L/DCR < RC   L/DCR = RC   L/DCR > RC
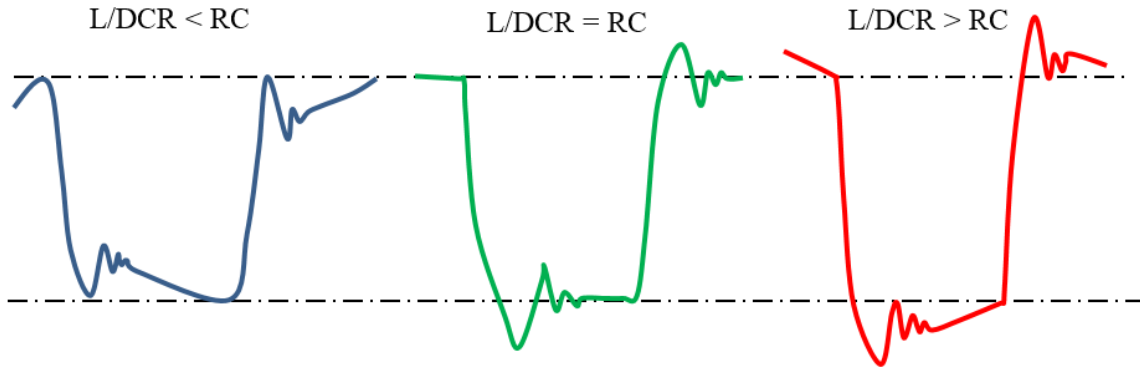
Figure 3. 1. DCR sense network RC time constant.

In a pure voltage mode control with correct compensation as an optimization starting point, Figure 3. 1 illustrates the V_{OUT} impacted by the DCR sense network and the V_{OUT} excursions are color coded as blue, green and red. Green curve represents the ideal RC time constant without nonlinear control enabled. If RC time constant is too large, as blue curve indicates, V_{OUT} is sluggish due to the delay in AVP loop and the overshoot can hurt the reliability of CPU; if RC time constant is too small, as depicted in red curve, there will be a V_{OUT} sag during load insertion and the excessive undershoot can create a system hang in the computing systems.

3.2 Nonlinear Control Scheme

In this section, control schemes are proposed and implemented to improve the system dynamics during load transient operation.

Output voltage deviations or excursions that exceed the pre-defined window thresholds are treated as load transient event [41] and a fast correction signal must be applied accordingly. Without losing the benefit (high DC gain) of the voltage mode control during static operation,

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the fast nonlinear loop includes a programmable multi-threshold window comparator, pulse generation circuitry and interfacing circuitry to the normal PWM. When the sensed voltage is out of the programmable window, the ATR asynchronously signals the modified PWM patterns for compensating the output voltage. There are basically two types of asynchronous responses, i.e. Active Load Release Response (ALRR) and Active Load Engage Response (ALER). The nonlinear response essentially extends effective regulation bandwidth while maintain constant output impedance over frequency. The red rectangles represent the time slot in each phase that ALRR event can initiate. The orange and blue rectangles represent ALER event can be triggered and they are threshold 1 and threshold 2, respectively. The internal counter module in each phase is synchronous with switching frequency and points where the nonlinear events should be added. For example in load engage event, the asynchronous pulses in each phase boost the switching frequency to MHz range in the transient event, which effectively pumping the inductor current energy to the output capacitance bank. The extra voltage generated by the nonlinear loop:

$$V_{EX} = \frac{\sum_{K=1}^{N} \int iL_K(t+\theta_K)dt}{C_{OUT}} \qquad (3.2)$$

where $iL_K(t)$ represent the inductor ripple generated by the asynchronous pulse in phase K. θ_K represents the phase angle difference between phase one. N presents the number of the active phases. For simplicity C_{OUT} represent the total capacitance of bulk and ceramic caps.
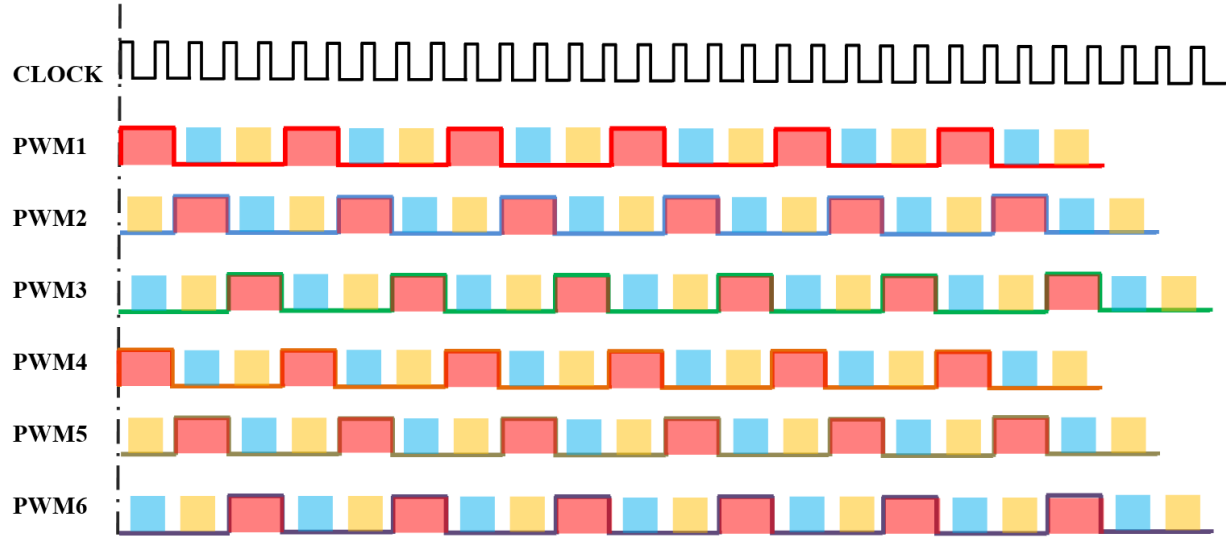
Figure 3. 2. The ATR timing architecture of the multiphase controller.

AVP scheme is to maintain constant output impedance so that less output capacitors can be populated and the output power of VR at full load can be reduced [1] -[5] . The nominal loadline equation is mathematically expressed in (3.3) given system impedance (R_{LL}):

$$V_{Target} = VID - I_{LOAD} \cdot R_{LL} \tag{3. 3}$$

3.2.1 Load Engage Enhancement

Nonlinear control scheme is a very critical technology and should be adopted in the slow transient application (below 50 kHz). In VR application, nonlinear control schemes during load engage transient event represent pulling-in PWM pulses or asserting PWM pulses faster than the response from the linear loop. It reduces the voltage excursion and saves output capacitors.

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Figure 3. 3 shows load engage response. The load current step is 131 A and the associated slew rate is 524A/μs. The 6 digital channels represent 6 PWMs and the lighter blue is the load current and darker blue is the voltage output.

Figure 3. 3. Load engage response with pure voltage mode control.

This is purely the voltage mode response and the 80 kHz control bandwidth can never respond fast enough (fire the phases sooner rather than waiting the internal clock cycle) to compensate the unwanted extra 60 mV undershoot. The ESR and ESL of the output caps are causing the first sharp dip. Because the inductor current slew rate is far less than the slew rate of output load current, due to the physics of the charge balance, the undershoot when load engage can never be removed, but the undershoot can be improved if nonlinear control scheme can be used.
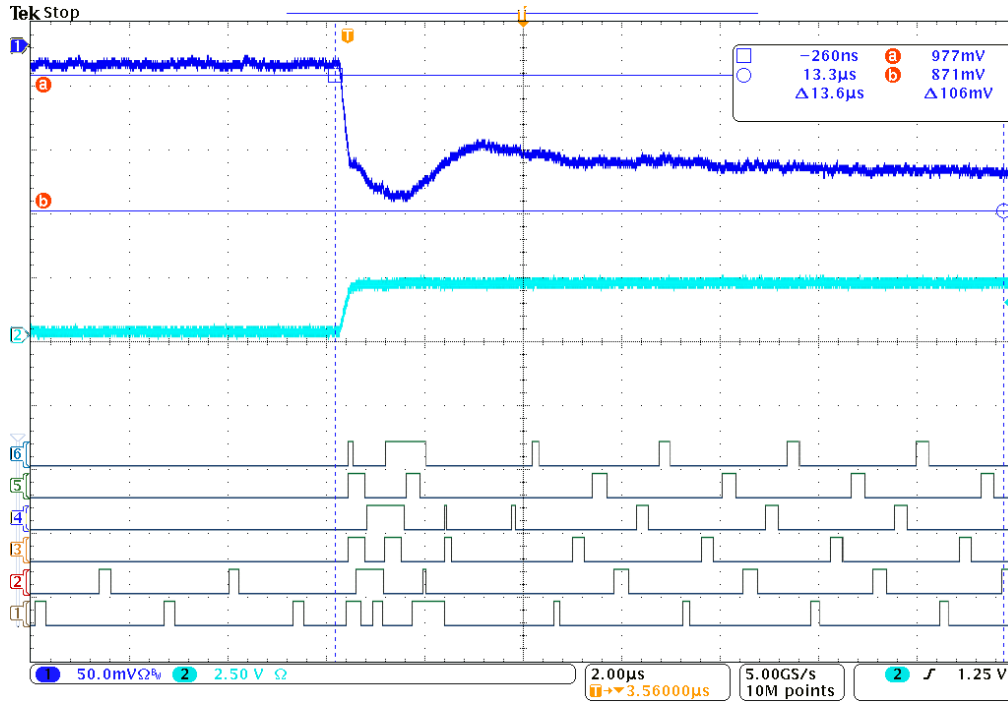
Figure 3. 4. Load engage response w/ auto-phasing.

Figure 3. 4 depicts the load engage response of the multiphase buck converter with ALER enabled. The same step and slew rate are adopted which are 131A and 524A/μs, respectively. The 6 digital channels represent 6 PWMs and the cyan blue represents the load current while darker blue represents the voltage output. Before the load is applied, it's running with 2 phase.

3.2.2 Load Release Enhancement

Existing methods for dealing with the overshoot voltage include increasing the output capacitance of the VR to suppress the overshoot voltage, or "body braking" by using the body diode of the power MOSFET in the VR to dissipate the excess current. Both options are problematic, however, as large capacitors increase the cost and size of the VR and "body braking"

generates additional power loss and excess heat. Therefore, we propose a method to pulse the LS gate ON and OFF to achieve the compromised result.

The equation set in (3.4) represents all operation scenarios or inductor current slopes in the converter. Equation (a) represents the charging slope when converter is operating is the boost (sink) mode with body diode of HS conducting. Equation (b) represents the charging slope when converter is working is the buck mode. Equation (c) represents the discharging (freewheeling) slope when LS is in asynchronous operation and body diode conducts (body braking). Equation (d) represents the discharging slope when LS is turned on.

$$iL_{slew} = \begin{cases} \dfrac{V_{BUS} - V_{OUT}(t) + V_{SD}}{L} & (a) \\[2ex] \dfrac{V_{BUS} - V_{OUT}(t)}{L} & (b) \\[2ex] -\dfrac{V_{OUT}(t) + V_{SD}}{L} & (c) \\[2ex] -\dfrac{V_{OUT}(t)}{L} & (d) \end{cases}$$

$$(3.4)$$
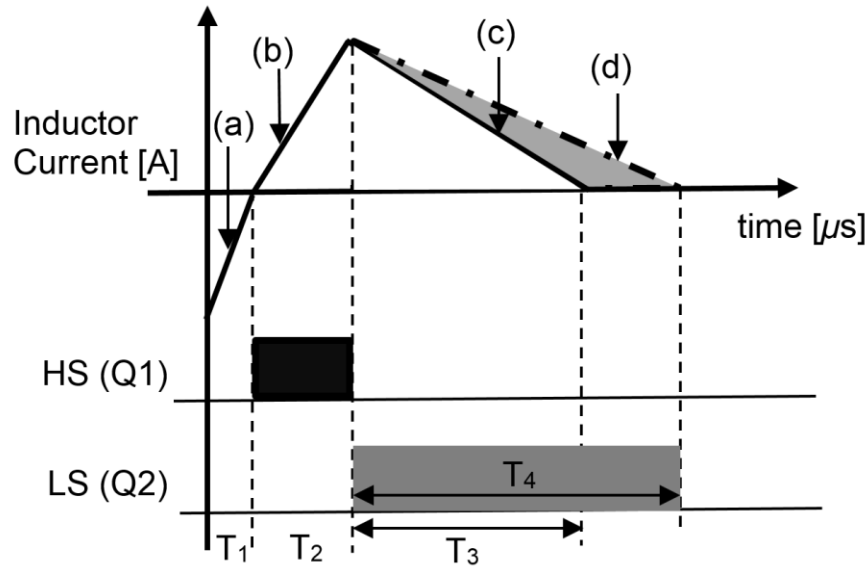
Figure 3. 5. Inductor current profile and gate-drive signals for the corresponding operations.

Figure 3. 5 depicts the all possible inductor current slopes or buck/boost mode from equation (1) and corresponding gate-drive signals of synchronous and asynchronous operations. Interval T_1 and interval T_2 represents HS body diode conducting and HS channel conducting, respectively. Interval T_3 and interval T_4 represent asynchronous and synchronous rectifier control, respectively.
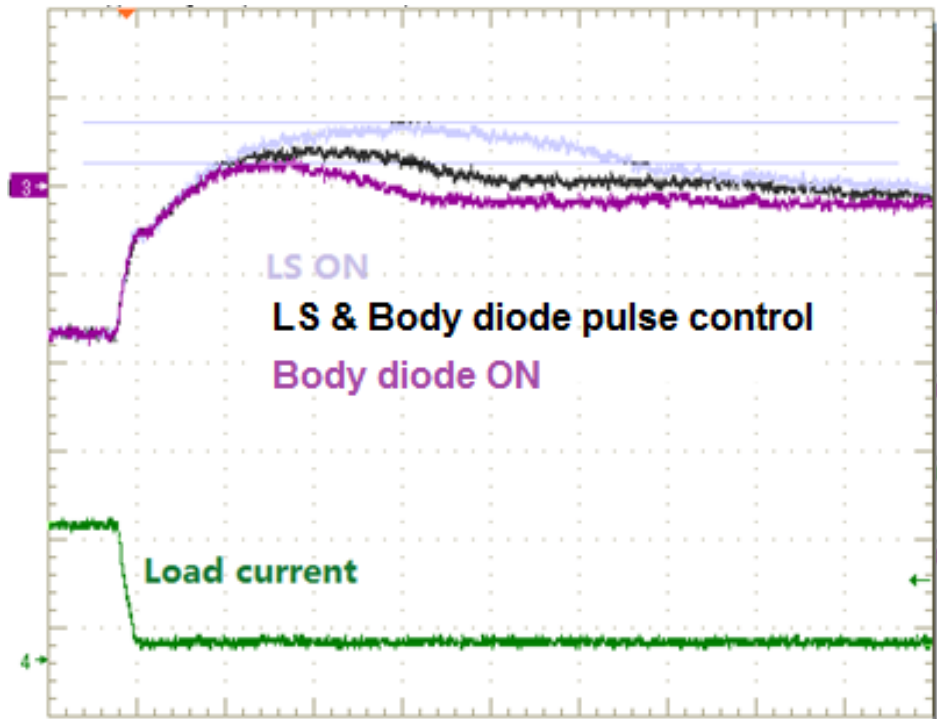
Figure 3. 6. Load release response comparison.

As depicted in Figure 3. 6, the scope shot shows comparison effects of suppressing the load release, which are the LS MOSFET ON, LS MOSFET OFF, and LS MOSFET Pulse control. The colors of the waveforms are light blue, black and magenta, respectively. Overshoot = 58 mV (Body diode ON). Overshoot = 68 mV (LS & Body diode ON).

Inductor current profile with during load release

$$iL_{slew} = \frac{Vout(t)}{L}$$

$$iL_{slew} = \frac{Vout(t) + V_D}{L}$$
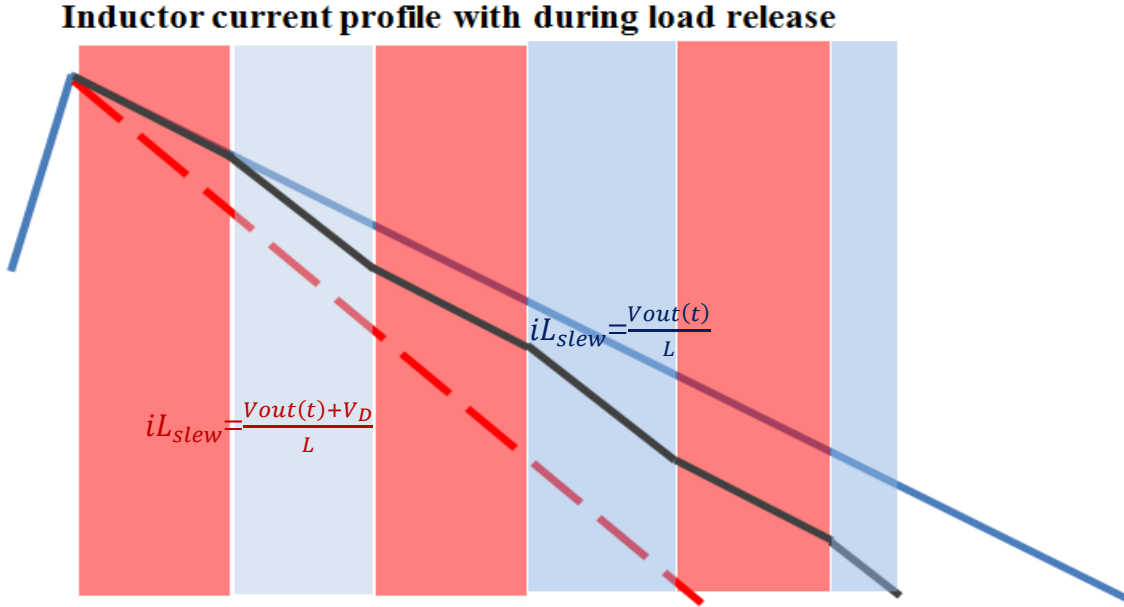
Figure 3. 7. Inductor current slew rate difference during load release

Figure 3. 7 shows the resultant inductor current profiles during load release.

By using the pulse control of the LS during load release, the temperature is 7 degrees lower than turning off the LS to freewheel the load current. Figure 3. 8 shows the inductor current slopes difference when body diode ON, pulsing the LS and LS ON, respectively.

When a transient load such as a CPU operates in a large voltage range, the worst case overshoot usually occurs at the lowest VID. Conventional body braking methods include turning off the LS FET for either a whole cycle or a period of time targeting the lowest VID only. Unfortunately, this braking method is typically too aggressive for higher VID levels. As a result, power will be unnecessarily dissipated in body diode, which may also cause a thermal issue.
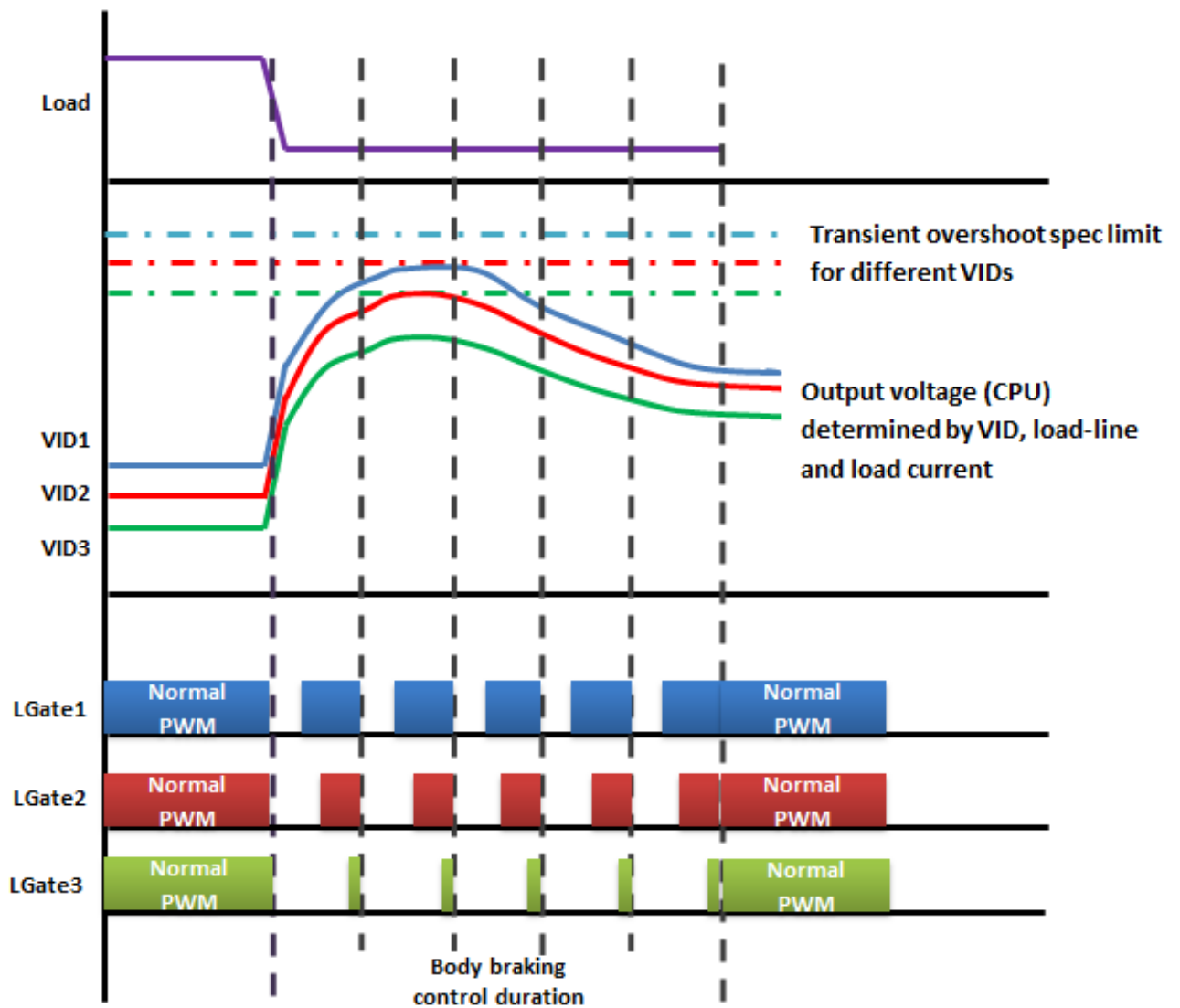
Figure 3. 8. Adaptive body-braking control (pulsing control).
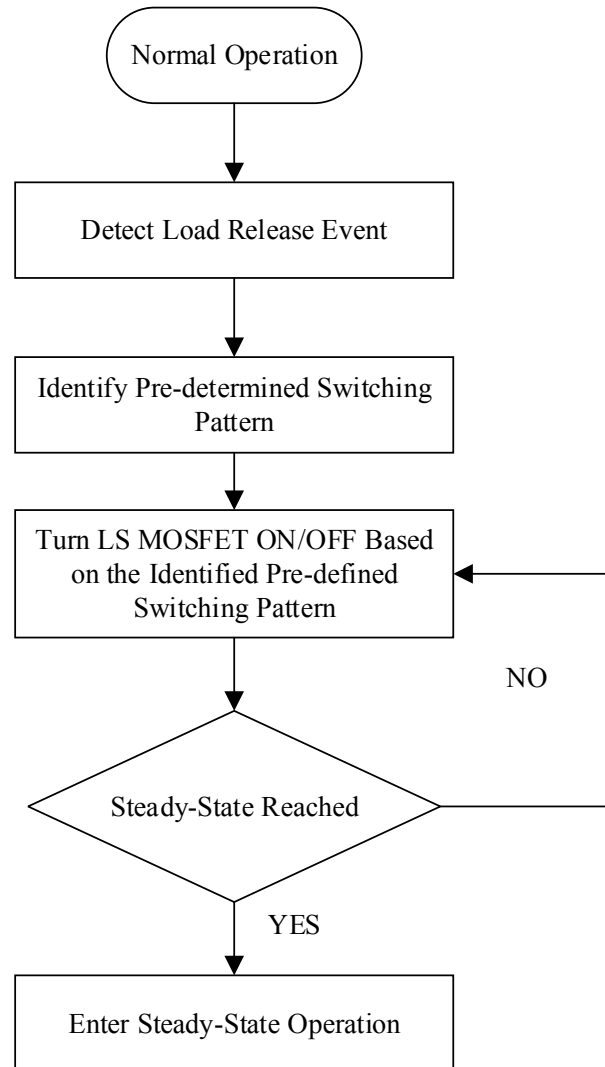
Figure 3. 9. Flow chart of adaptive body-braking control (pulse control).

The flow chart of adaptive body-braking control in pulse control mode is shown in Figure

3. 9.
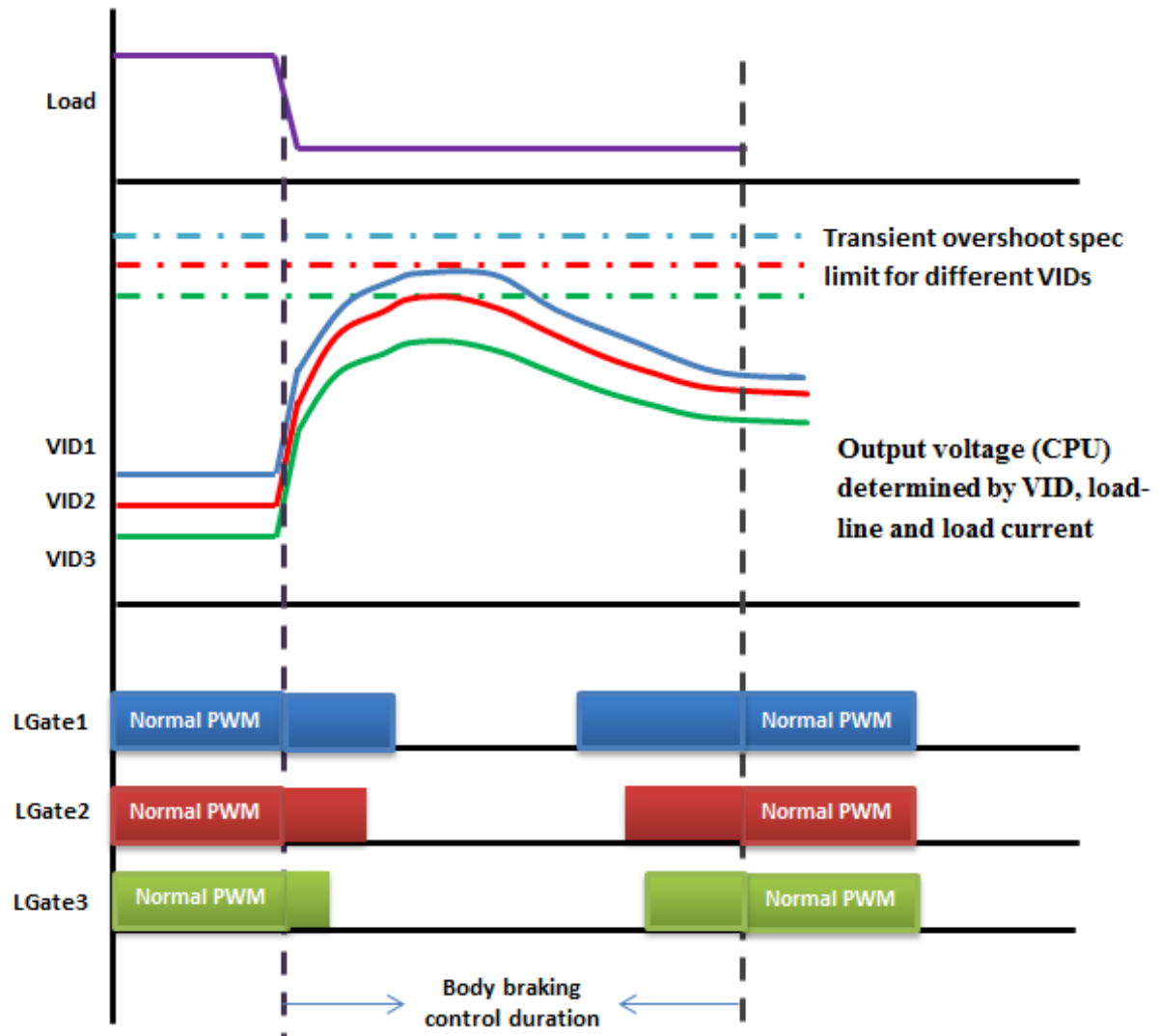
Figure 3. 10. Adaptive body-braking control (Body diode ON).

In Figure 3. 10, in body braking control duration, the pulse pattern is pulsing the LS gate, but the duration of the OFF time is still adaptively changing according to the current VID, which still based on the worst case overshoot in the lowest VID. Figure 3. 11 shows the related flow chart.

```
                    ┌─────────────────┐
                    │ Normal Operation │
                    └─────────────────┘
                            │
                            ▼
            ┌───────────────────────────────┐
            │   Detect Load Release Event    │
            └───────────────────────────────┘
                            │
                            ▼
            ┌───────────────────────────────┐
            │      Turn OFF HS MOSFET        │
            │      Turn ON LS MOSFET         │
            └───────────────────────────────┘
                            │
                            ▼
            ┌───────────────────────────────┐
            │   Adaptive Turn OFF LS MOSFET  │◄──────┐
            └───────────────────────────────┘       │
                            │                        │
                            ▼                    NO  │
                         ╱──────╲                    │
                        ╱  Output ╲                  │
                  ╱ Voltage Exceed Identified ╲──────┘
                  ╲  Pre-determined Threshold  ╱
                        ╲        ╱
                         ╲──────╱
                            │  YES
                            ▼
            ┌───────────────────────────────┐
            │  Re-enter Steady State Operation │
            └───────────────────────────────┘
```
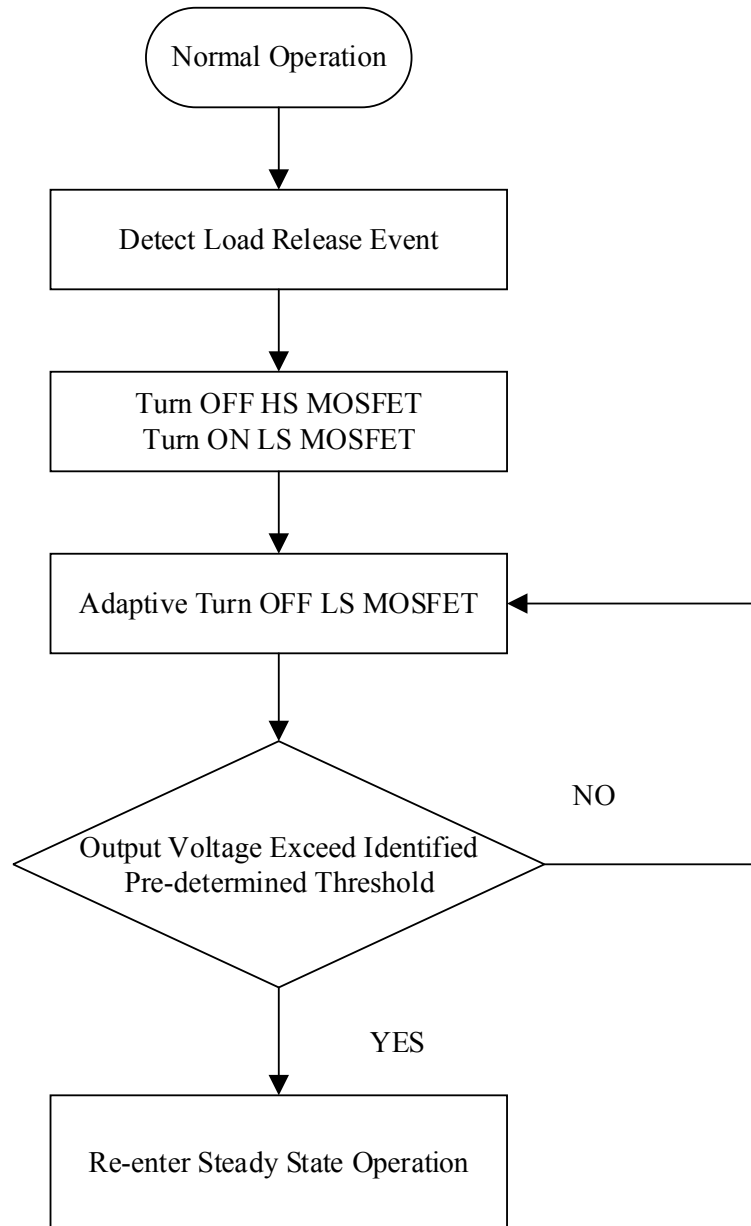
Figure 3. 11. Flow chart of adaptive body-braking control (Body diode ON).

3.3 Drop Phase Optimization

As analyzed in chapter 2, the phase number of the multiphase converter is the function of load current and should follow adaptively with the load change from the static operation perspective. However, there is extra care needs to be taken when shutting off the phase, which is ramping down the inductor current before the drop operation.
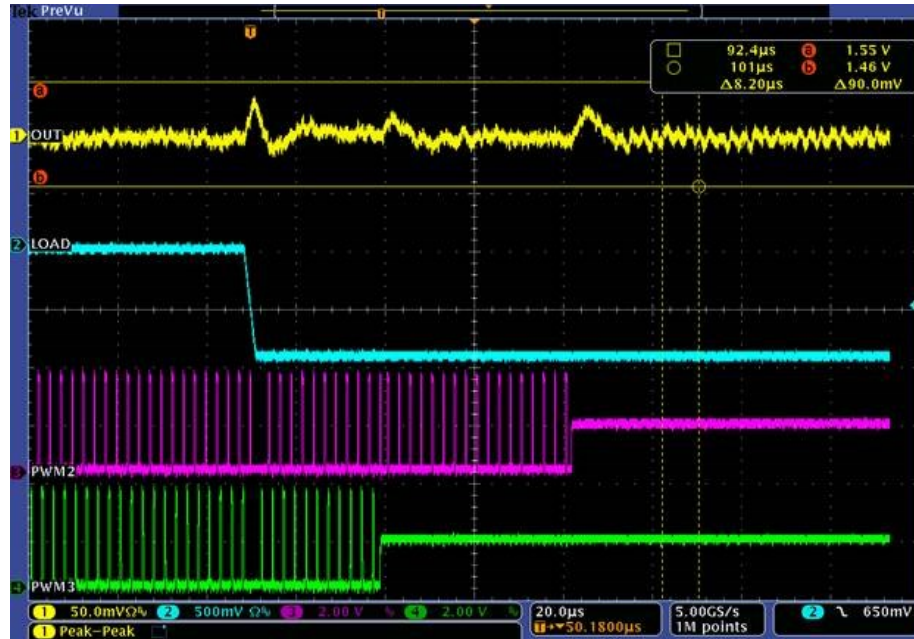
Figure 3. 12. Overshoot during phase shedding.

Figure 3. 12 shows the phase shedding during load release. The yellow channel is V_{OUT}. The blue channel is load current. PWM2 and PWM3 are green and magenta channels respectively. The load current step is 30A and slew rate is 10A/μs. There are three overshoots in this scope shots circled in red. The first one is normal and is caused by the load step. The rest overshoots are the result of dropping phase 2 and 3. When the two phases are turning off, the corresponding phase still carries some current in the inductor. The turning OFF slew rate is

increased when the phase is off state because the current is freewheeling through the LS body diode.

Once the phase dropping command is initiated, the state-machine of the current balance module starts to modify the modulated ON time generated by PID and ramping down the inductor current in the phase that is going to be turned off, meanwhile also increase the current in other phase to take over the total load current. The overshoot caused by phase dropping can be eliminated.
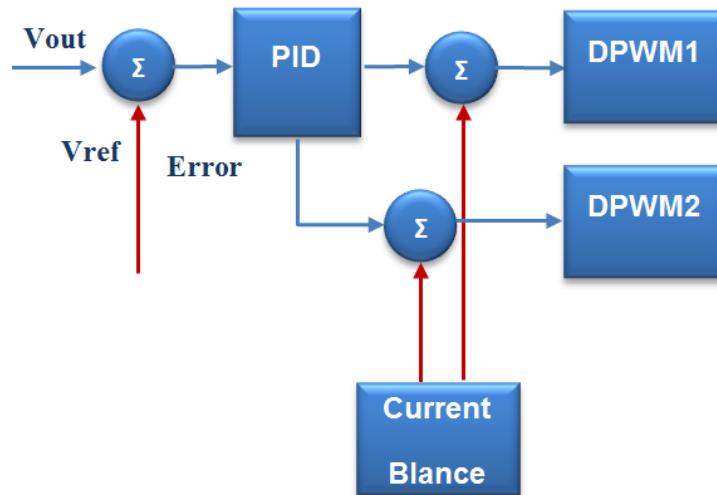
Figure 3. 13. Current balance block diagram.

The simulation shows the inductor current is ramping down 5 consecutive switching cycles before the controller issue a drop commend.
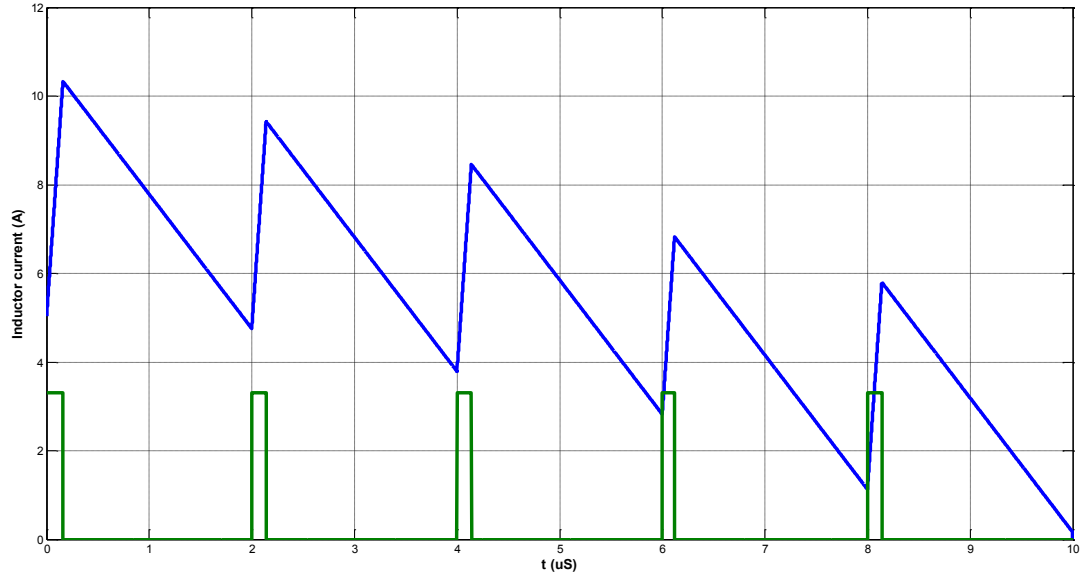
Figure 3. 14. Simulated inductor current with smooth gain.

3.4 PWM HiZ to High Transition in Shedded Phase

In the event of power state transition or load transient, the shedded phase need to be active instantaneously to conduct current, therefore, there can be a scenario that PWM signal transits from HiZ to high.

Figure 3. 15 shows the simulation results of VR existing tri-state. PWM signal transitions from HiZ to high directly. Voltage across the bootstrap capacitor is around 3V due to the gate drive leakage. In Figure 3. 15, Vboot_SW decays linearly due to the leakage (extra leakage current is artificially incorporated in the simulation to shorten the running time) and finally clamped according to equation (1). Around 13 ns of shoot-through is captured in Figure 3. 16 (a) and no shoot-through captured in Figure 3. 16 (b) due to the different dead-time schemes.
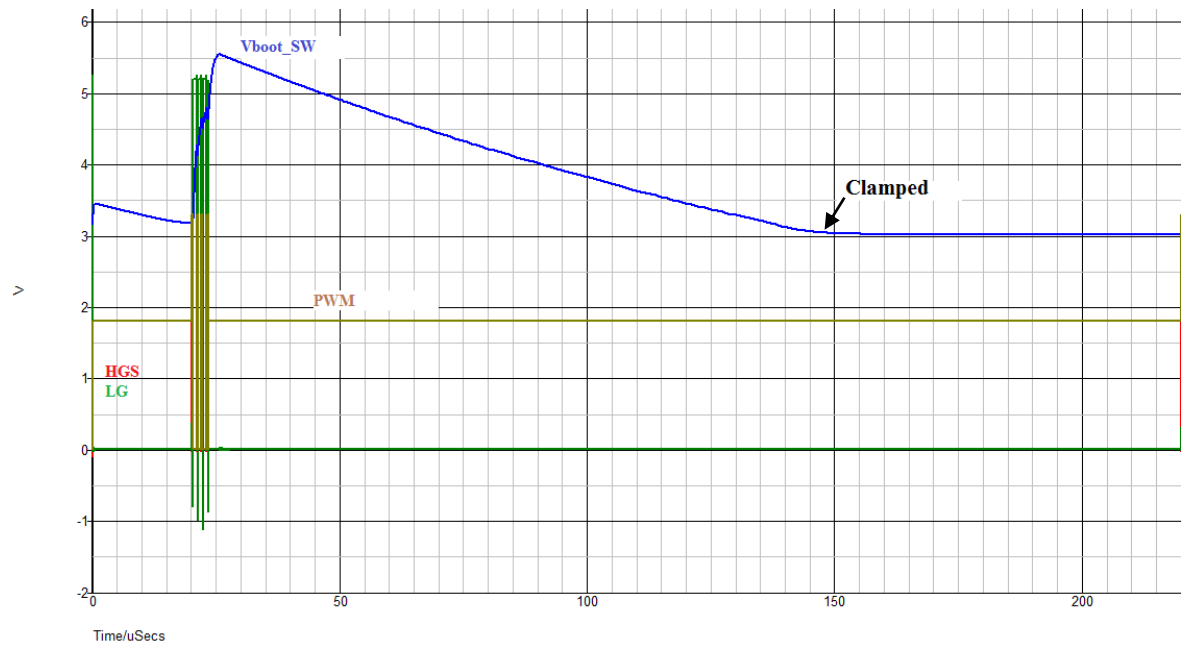
Figure 3. 15. Simulation results of VR entering tri-state.
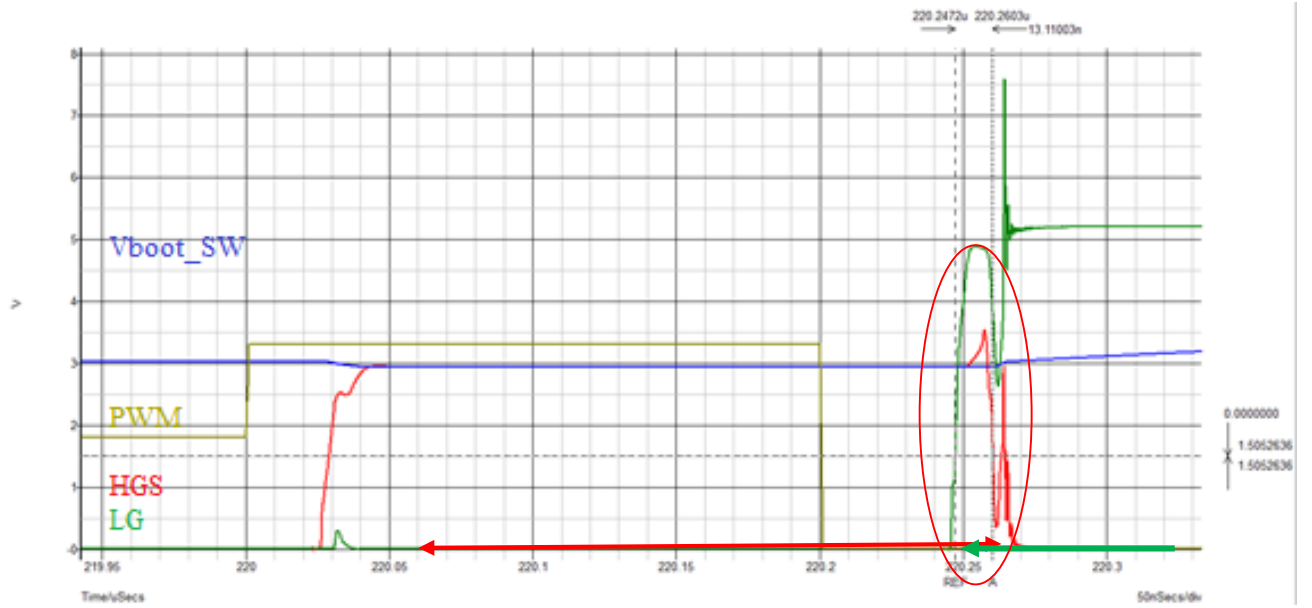
(a)
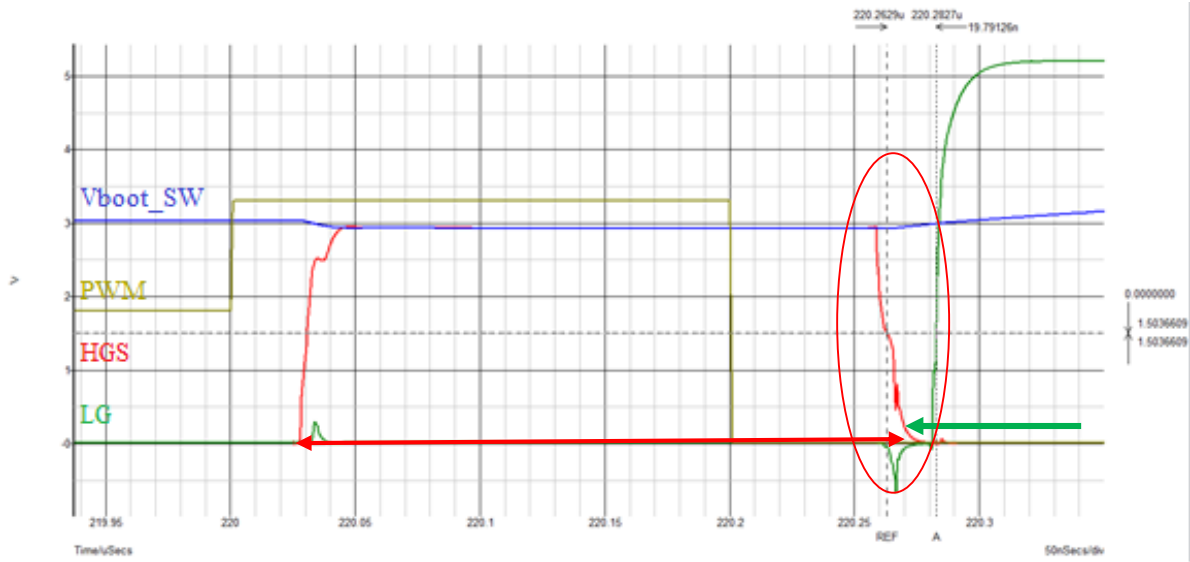
(b)

Figure 3. 16. Simulation waveforms of existing long tri-state: (a) fixed dead-time: around 13 ns of shoot-through (b) adaptive dead-time: No shoot-through captured.

There is no issue when VBOOT-SW is above 3.8 V, which presents the most operating conditions. With lowering down PVCC and increased VOUT (around 1.8 V), there is a case that driver can create a GH/GL overlap (shoot-through) scenario if the driver dead-time design is fairly aggressive. When the dropped phase stays in tri-state in long period of time, the boot capacitor is discharged by the gate driver leakage current (leakage rate: 1 nA/s), and eventually VBOOT-SW is clamped depending on equation (1):

$$V_{BOOT-SW} = PVCC - V_{SD} - V_{OUT} \qquad (3.5)$$

Where PVCC is the power MOSFET drive voltage. V_{SD} is the diode voltage drop for the internal switch.

As shown in Figure 2. 11, the level shift circuit takes the GND referenced signals and level shift them to the HDRV "isolated" circuitry (level shift output) which is referenced to SW

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node and powered from BOOT-SW capacitor voltage. The HS gate falling edge propagation delay gets larger relative to LS rising edge delay. This BOOT-SW bleed depends on variables such as VOUT and length on time in tri-state among other variables. The HS falling preparation delay increase occurs regardless of PVCC voltage and can create a GH/GL overlap until BOOT capacitor charges back up from the 2nd LS pulse.

As shown in Figure 3. 17(a), the red circle highlights the gates overlap when existing long PWM tri-state. .The overlap is around 10 ns. As shown in Figure 3. 17(b) and (c). There are several methods to eliminate the overlap. In Figure 3. 17(b), the PWM generate by the controller should go to LOW first, which can charge up the voltage on BOOT capacitor, thus can shorten the propagation delay and eliminate the shoot-through. In Figure 3. 17(c), the anti-shoot protection unit directly monitors HG and LG, which can adaptively prevent the gate overlap phenomenon in this specific scenario.

The avalanche breakdown energy of the power stage devices, from the worst case aspect, is 50 mJ by Cadence Virtuoso Analog Design Environment simulation. The energy during the gate overlap event is under 100 μJ, 1/500th the energy necessary for breakdown. However, from the system robustness point of view, the gate overlap should be prohibited.

(a)

(b)

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C2	2.0V/div	1MΩ BʷW:250M
C3	2.0V/div	50Ω BʷW:500M
C4	2.0V/div	50Ω BʷW:1.0G

V1	202.8mV	t1	262ns
V2	3.536V	t2	272.5ns
ΔV	3.334V	Δt	10.5ns
ΔV/Δt	317.486MV/s	1/Δt	95.238MHz

| A' C4 ∫ 1.92V |

| 50.0ns/div 5.0GS/s IT 250fs/pt |
| Stopped Single Seq |
| 1 acqs RL:2.0M |
| Auto April 19, 2013 15:28:43 |
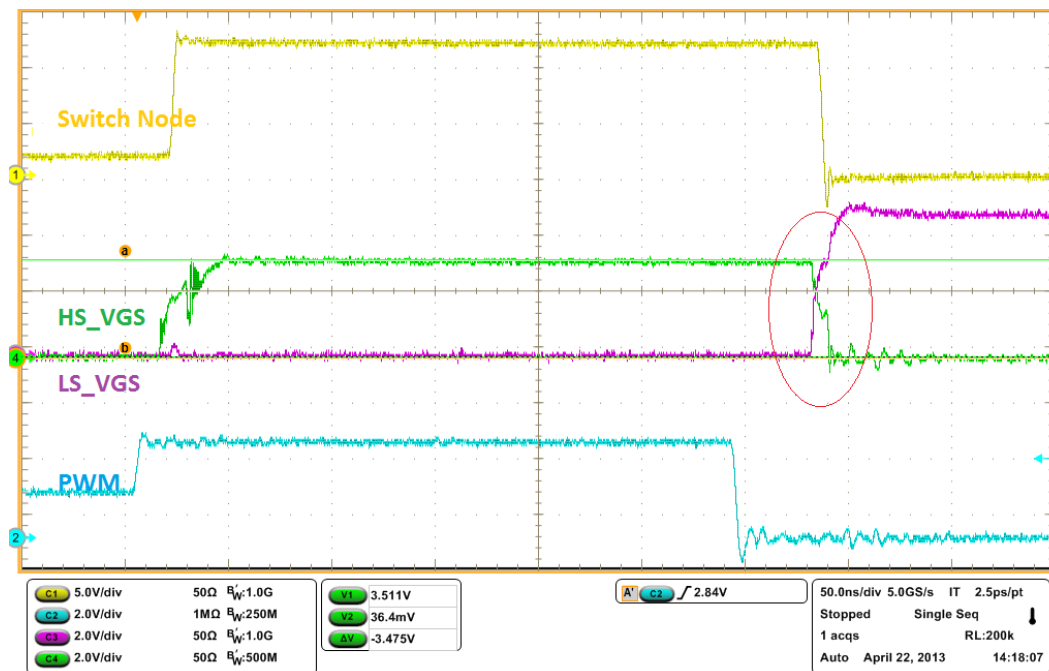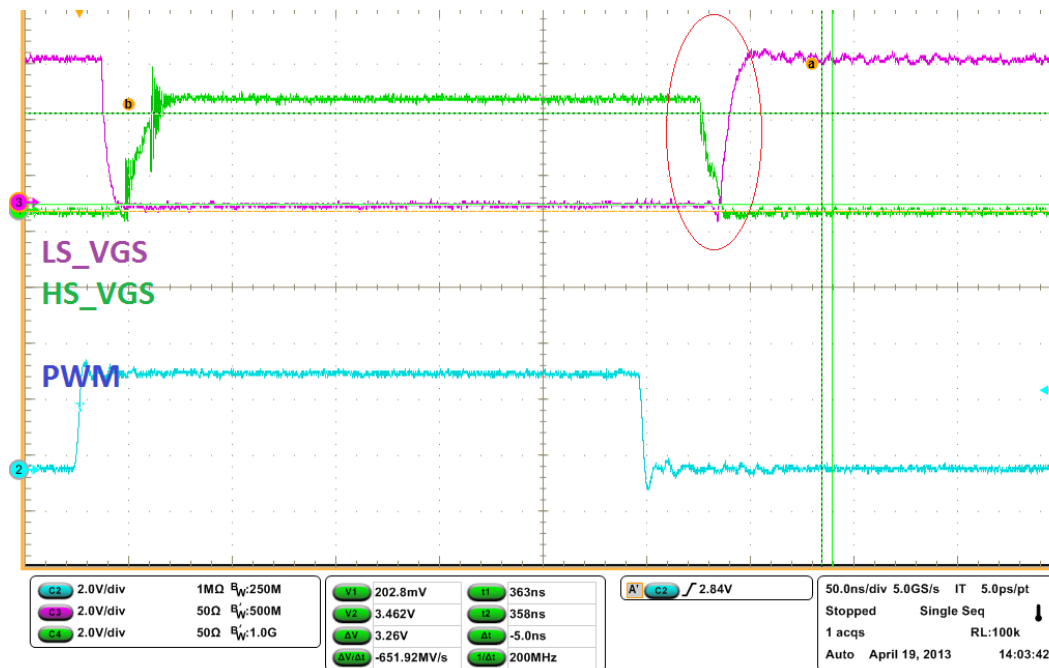
(c)

Figure 3. 17. Operational waveforms of existing long tri-state: (a) around 10 ns of shoot-through; (b) No shoot-through captured by PWM going low first when exiting tri-state. (c) No shoot-through captured with "adaptive" shoot-though protection.

This proposed method is to eliminate the shoot-through issue described above while still maintaining efficient VR operation during steady-state operation mode. The proposed approach combines advantages of both fixed dead-time and adaptive dead-time control methods.

The proposed dead-times management contains two sets of dead-times circuitries, i.e. fixed dead-time and adaptive dead-time. Power conversion efficiency can be maximized due to the shorter dead-times that can be implemented in steady-state mode. The adaptive dead-time can be switched in when necessary to ensure the robustness of the power converter operation.

The adaptive dead-time control, which is adaptive to the manufacturing variation of Q_g and R_G of the discrete MOSFETs, monitors the driver outputs, HDR and LDR. When the PWM

transitions to high, the LS gate voltage begins to fall after a propagation delay. At the same time, LDR voltage is sensed, and high-side driving voltage starts to increase after LDR voltage is lower than a proper threshold (1 V).

The fixed dead-time monitors the gate signals before level shift circuitry. Since the MOSFET parameter variation is known and can be controlled, therefore a shorter (more aggressive) delay can be asserted to achieve the fixed dead-time.

The efficiency improvement can be calculated based on the buck loss model. Reducing 5 ns more of both LS rising/falling dead-times translates to about 0.30% efficiency gain. For example in mainstream application, there are totally 20 phases of multiphase VR in operation and 1.23 W (12 phases of 2 Vcores: 0.66W, 8 phases of 4 MEM VRs: 0.57W) can be saved if the dead-time can be shrunk by 5 ns given a general MOSFET usage.

$$P_{deadtime} = V_{SD} \cdot f_{SW} \cdot \left[\left(I_{OUT} - \frac{I_{ripple}}{2} \right) t_{deadtime(r)} + \left(I_{OUT} + \frac{I_{ripple}}{2} \right) t_{deadtime(f)} \right] N_{phase} \quad (3.\ 6)$$

where $t_{deadtime(r)}$ represents rising edge dead-time between LS turn off and HS turn on; $t_{deadtime(f)}$ represents rising edge dead-time between HS turn off and LS turn on; N_{phase} represents number of active phases.
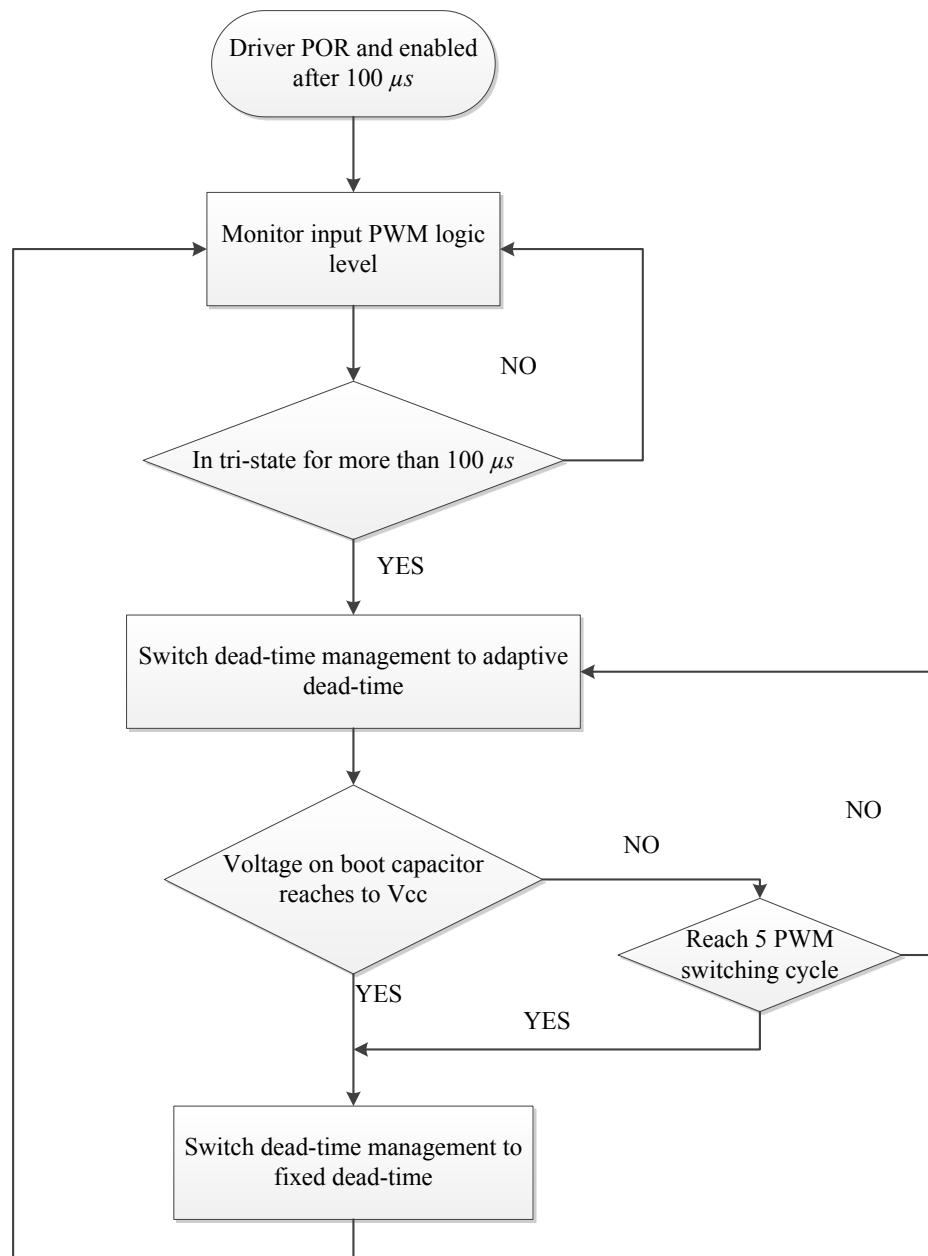
Figure 3. 18. Dead-time management diagram when VR exist tri-state

Figure 3. 18 shows the proposed dead-time management scheme that can enhance the system reliability and also maintain high power conversion efficiency.

CHAPTER FOUR: HIGH FREQUENCY TRANSIENT

High repetitive rate of load transient, especially the transient frequency at around switching frequency, has been a challenge in power management industry [39] -[45] . Multiphase buck converter suffers from the dynamic current sharing at this range of operation.

Voltage excursion generated by high frequency transient should be regulated within the specification window. In voltage mode control, dynamic phase current imbalance is an expected behavior and can be an issue, however, if it results in extra dynamic power loss, electrical or thermal stress beyond the capability of the power component since the phase currents can sink and source among phases. In this chapter, the high repetitive rate of load transient is explored. We propose several methods to mitigate the issue so that the phase current can share better, dynamic loss is therefore reduced and the system reliability in this operation mode is fully enhanced.

4.1 Sampling Effects of PWM Converters

In voltage mode control, V_{COMP}, as illustrated in Figure 4. 1 (a), is the error amplifier output and it compares with saw-tooth carrier signal to generate the PWM. As an illustration of trailing-edge modulation in Figure 4. 1 (b), the perturbed V_{COMP} is introduced and PWM signal is generated by the comparison between V_{COMP} and the saw-tooth carrier signal.
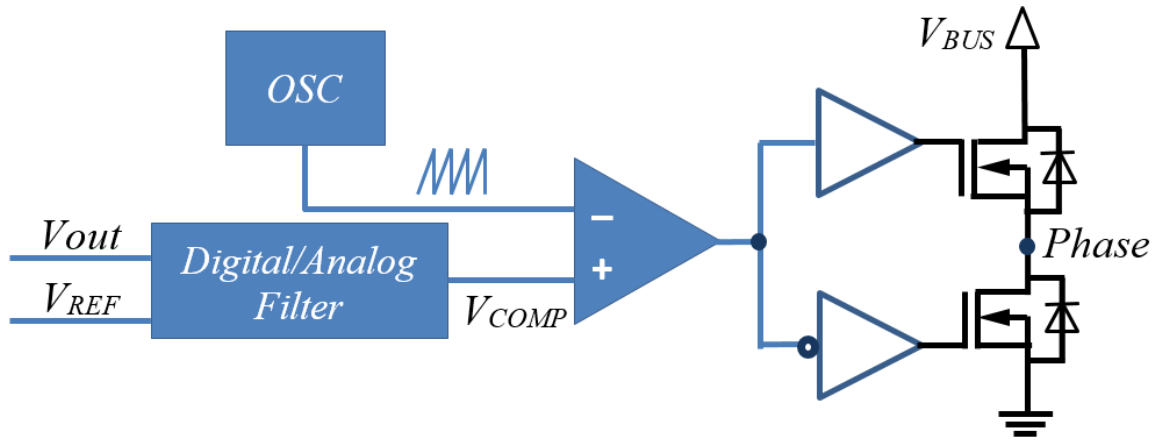
(a)
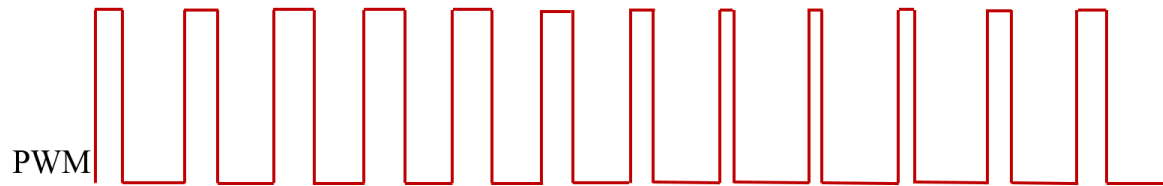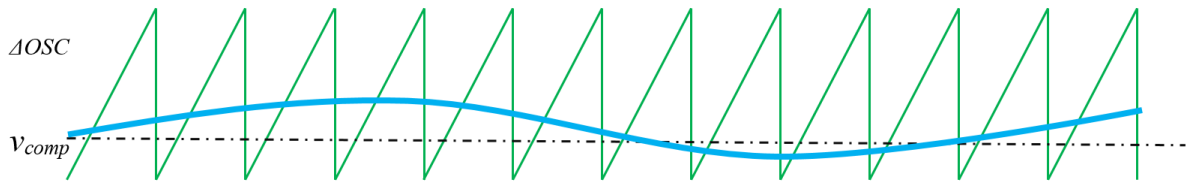
(b)

Figure 4. 1. PWM modulator diagram and V$_{COMP}$ perturbation waveform: (a) PWM Modulator; (b) modulation waveform with V$_{COMP}$ perturbations.

Pulse width modulation (PWM) is a sampling hold system and it samples periodically at the switching frequency where V$_{COMP}$ and ΔOSC encounters.

The transfer function of zero-order hold is:

$$H_{ZOH}(s) = \frac{1-e^{-ST}}{s} \qquad (4.1)$$
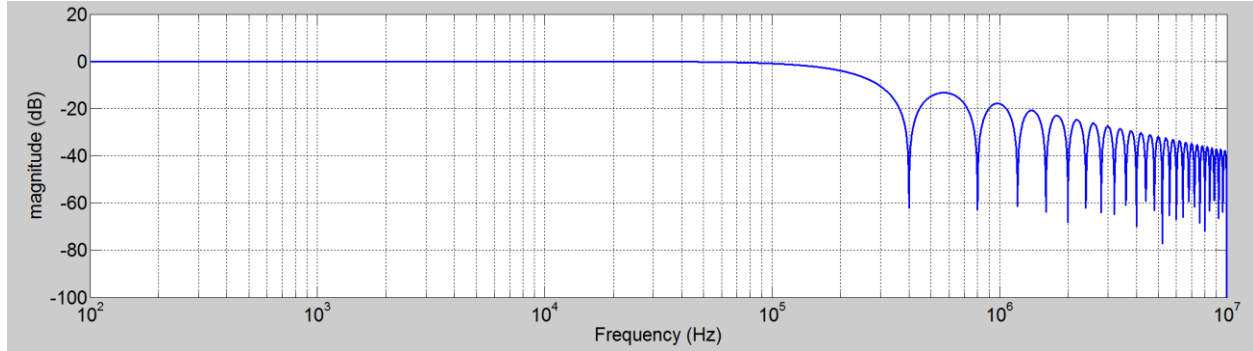
(a)
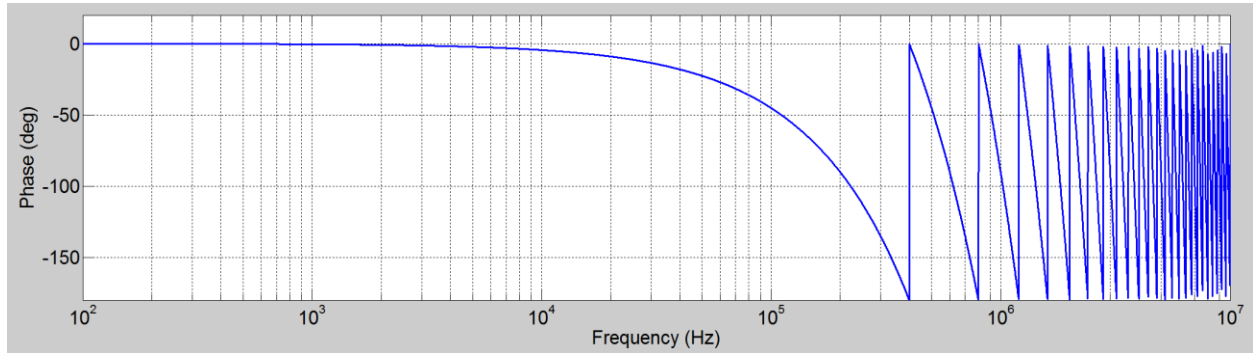
(b)

Figure 4. 2. Frequency response of zero-order hold: (a) Gain; (b) Phase.

The transfer function of sample data system can be found as:

$$H_{ZOH}(s) = \frac{1-e^{-ST}}{sT} \qquad (4.2)$$

Figure 4. 2 shows the frequency response of PWM sample data system. The sampling frequency is 400 kHz as the simulation indicates.

4.2 Output Impedance Optimization

The output impedance design is a good measure of feedback loop characteristic. According to CPU vendors' requirements, a desired close loop Z_{OUT} of the multiphase converter should be constant across the full frequency range.
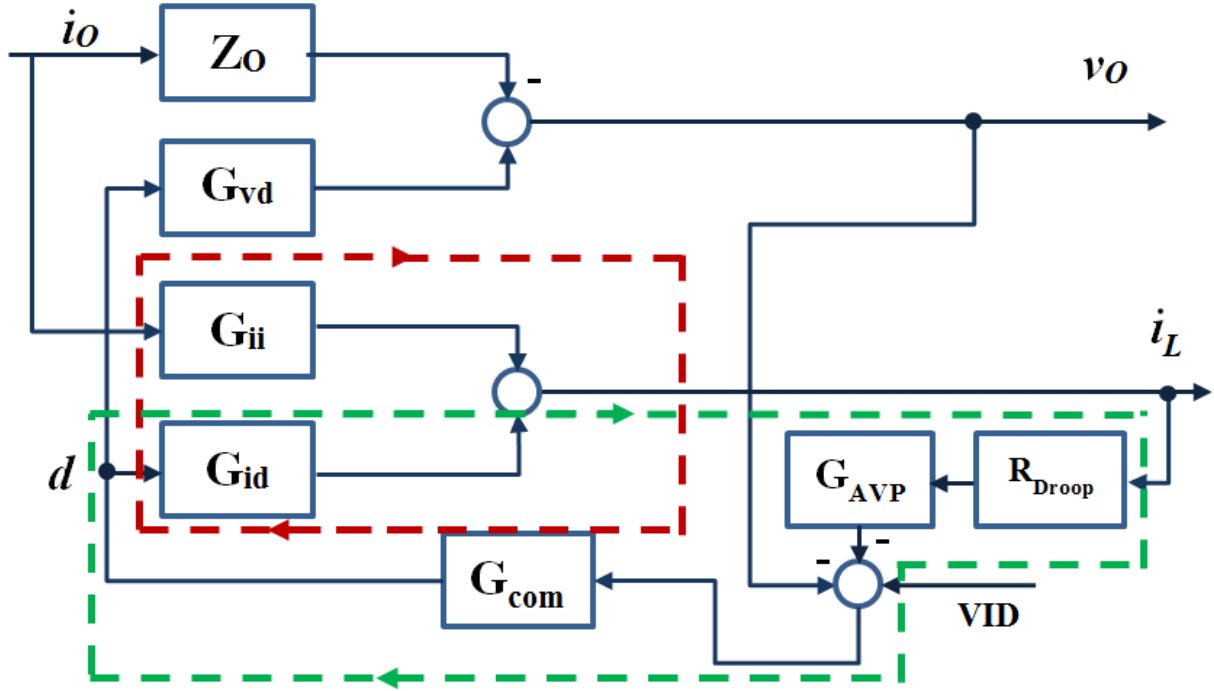
Figure 4. 3. Small-signal control block diagram of the closed loop output impedance.

$$G_{id}(s) = \frac{\hat{\imath}_L(s)}{\hat{d}(s)}\Big|_{\substack{\hat{\imath}_o(s)=0 \\ \hat{v}_{in}(s)=0}} = \frac{V_{in}}{sL + R_{DCR} + R_{OUT}//(R_{ESR} + \frac{1}{sC_{OUT}})} \tag{4.3}$$

$$Z_O(s) = \frac{\hat{v}_O(s)}{\hat{\imath}_O(s)}\Big|_{\substack{\hat{d}(s)=0 \\ \hat{v}_{in}(s)=0}} = \frac{R_{DCR}(1+sR_{ESR}C_{OUT})\left(1+\frac{sL}{R_{DCR}}\right)}{s^2 L C_{OUT}\left(\frac{R_{Load}+R_{ESR}}{R_{Load}+R_{DCR}}\right)+s\left(\frac{L}{R_{Load}+R_{DCR}}+C_{OUT}R_{ESR}+R_{Load}//R_{DCR}\right)+1} \tag{4.4}$$

$$G_{ii}(s) = \frac{\hat{\imath}_L(s)}{\hat{\imath}_O(s)}\Big|_{\substack{\hat{d}(s)=0 \\ \hat{v}_{in}(s)=0}} = \frac{1+sR_{ESR}C_{OUT}}{s^2 L C_{OUT}\left(\frac{R_{Load}+R_{ESR}}{R_{Load}+R_{DCR}}\right)+s\left(\frac{L}{R_{Load}+R_{DCR}}+C_{OUT}R_{ESR}+R_{Load}//R_{DCR}\right)+1} \tag{4.5}$$

G_{id} is the transfer function of open loop duty cycle to inductor current.

Z_O is the open loop output impedance.

G_{ii} is the transfer function of open loop output current to inductor current.

G_{AVP} is the AVP LPF transfer function.

G_{COM} is the total compensator gain.

As illustrated in Figure 4. 3, two transfer functions representing the loop gains, Ti(s) and Tv(s) are defined as:

$$T_v(s) = G_{vd}(s) \cdot G_{com}(s) \tag{4.6}$$

$$T_i(s) = G_{id}(s) \cdot G_{com}(s) \cdot R_{droop} \cdot G_{AVP}(s) \tag{4.7}$$

By adopting Mason's gain formula, the overall output impedance of voltage mode control with AVP loop can be mathematically expressed as:

$$Z_{OC}(s) = \frac{Z_O(s)(1+T_i(s)) + G_{ii}(s)G_{com}(s)R_{droop}G_{AVP}(s)T_v(s)}{1+T_i(s)+T_v(s)} \tag{4.8}$$

The output impedance and the compensation gain in high frequency region should be low enough to attenuate high frequency noise.
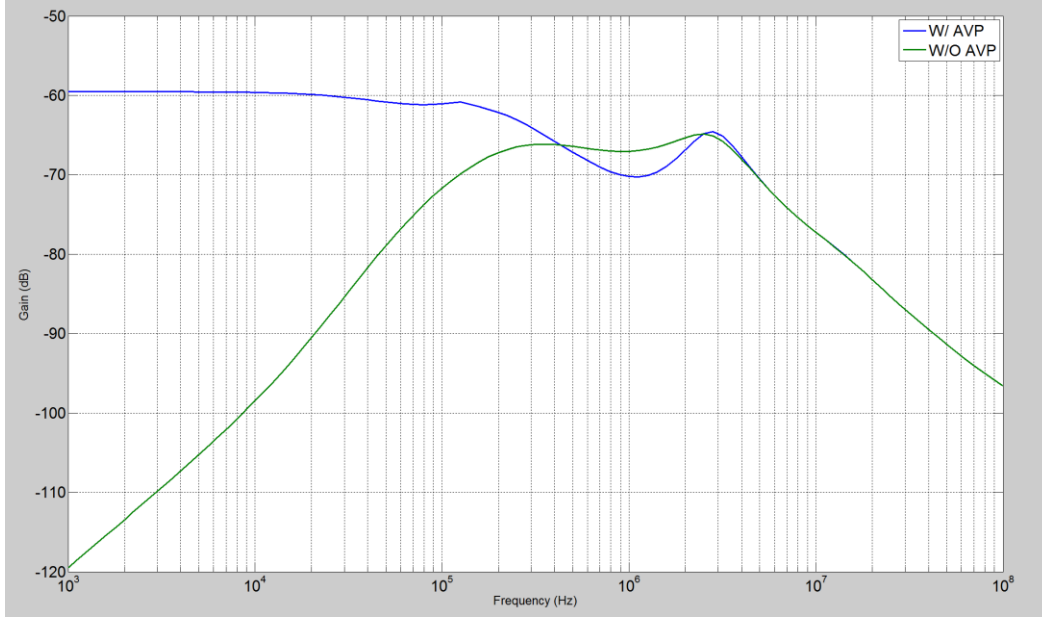
Figure 4. 4. *Plots of* $|Z_v|$ *and* $|Z_{OC}|$

4.3 Beat Frequency Mitigation

As repetitive load frequency is approaching switching frequency, the control loop cannot respond fast enough to the load transient, as well as the current sharing loop. The dynamic current between phases can sink and source and the dynamic loss increases due the extra circulating energy. The extra phase imbalance current can also introduce extra stress on the power devices. Therefore, there is a design mitigation need to be carried out.

The voltage loop BW is optimized to be 75 kHz, which is 1/5 of f_{SW} as shown in this work. Within the loop BW, feedback loop can maintain the stability of system. However, beyond the loop BW, the compensator may not have good response to high frequency transient since the loop gain is much damped. Moreover, it is prune to aliasing problem. So beyond the loop BW, it is better to lower the impact of compensator and let the C_{OUT} handle the transient response.

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In the event of low frequency load current transient, the control loop is optimized to suppress load current changes so that the output impedance is controlled by the system's closed loop response. In the presence of high frequency, large load current change, the closed loop response is optimized to minimize the peaking of the output impedance.
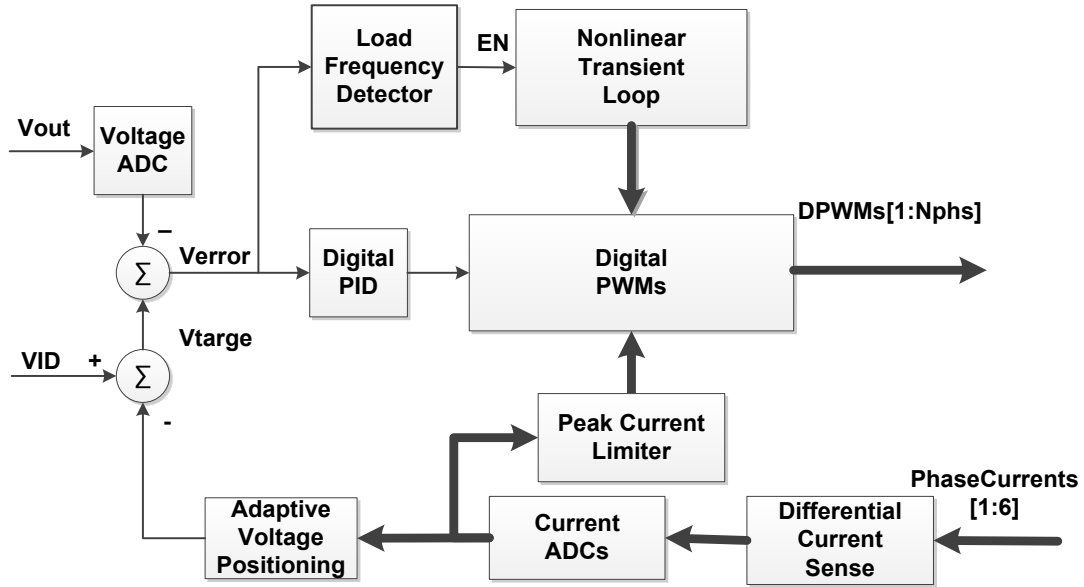
Figure 4. 5. Block diagram of load frequency detection (LFD).

Figure 4. 5 illustrates the simplified block diagram of the LFD scheme during high frequency repetitive load transient. The programmable threshold should be bigger than the ripple voltage. The polarity change rate in the voltage error indicates the load transient events: load engage and load release. Once the detected load frequency surpassed the defined high frequency range, the EN of nonlinear transient loop will be de-asserted. The current ADCs monitors the phase current in the real time manner. The peak current limiter acts as a double layer protection in the control loop that can truncate the PWM pulse once the sensed current is greater than the threshold value. The inductor saturation can be eliminated and system reliability is enhanced. In

order to improve the reliability of the VR, the instantaneous phase current should be bounded. The current protection in the control loop is proposed as a two layer function to mitigate the beat frequency issue.

4.4 Dynamic Current Sharing

As shown in Figure 4. 6 (a), two cursors mark the total AC window for both overshoot and undershoot excursions in low frequency transient. The extra undershoot caused by the beat frequency oscillation in Figure 4. 6 (a), is not desirable and may cause blue screen in computing systems. The beat frequency oscillation is eliminated by disabling the nonlinear loop. The V_{OUT} is regulated well within the AC window as illustrated in Figure 4. 6 (b).

(a)

81
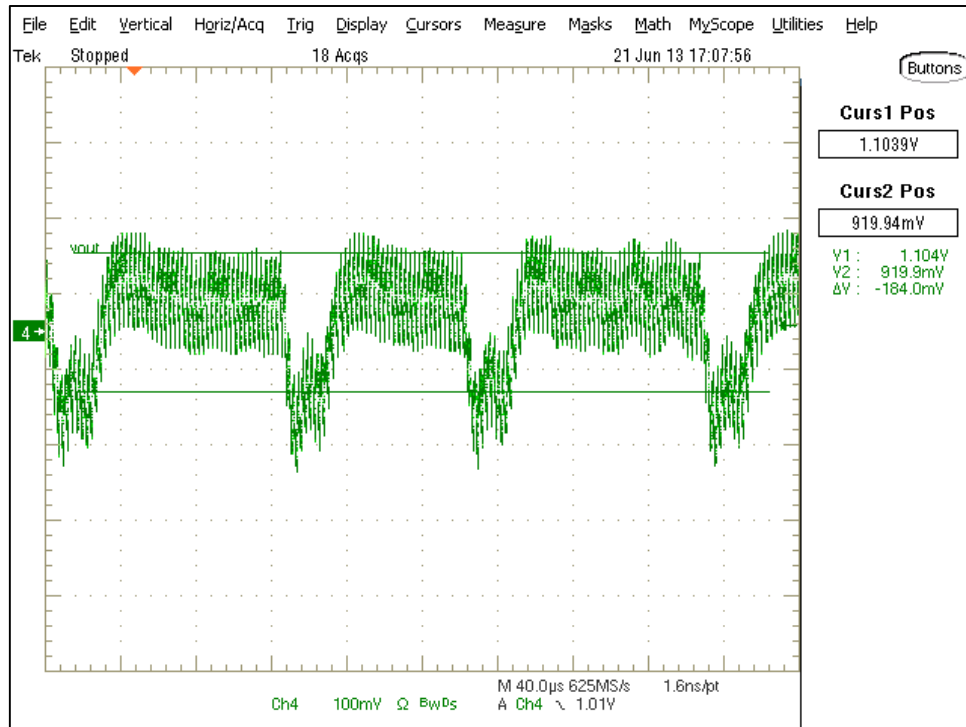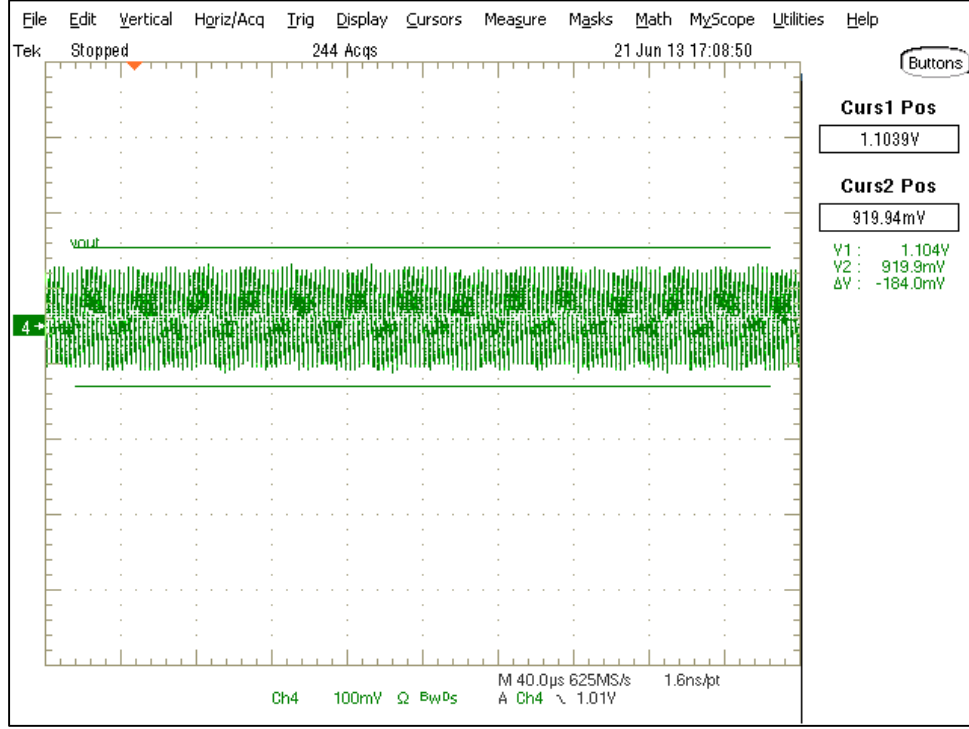
(b)

Figure 4. 6. A load transient response. Load step: 10A-141A, slew rate: 450 A/μS. Rep rate: 400 kHz. (a) Nonlinear loop enabled. (b) Nonlinear loop disabled.

Frequency domain analysis using Matlab is carried out and the effectiveness of the proposed scheme is verified.

$$Vout_k = \sum_{n=0}^{N-1} vout_n e^{-i2\pi kn/N}$$

(4. 9)

Load rep rate is around 400 kHz, which is generated by Intel VRTT. The V_{OUT} data are the same as depicted in fig. 6 and are exported in DAT file from the scope. The spectral characteristics of V_{OUT} are informative. The low frequency peaking is around 9 kHz in Figure 4. 7 (a) with the nonlinear loop enabled. After disabling the nonlinear loop, as shown in Figure 4. 7 (b), the low frequency oscillation is removed and the only high magnitude in the spectrum represents the load frequency.

82
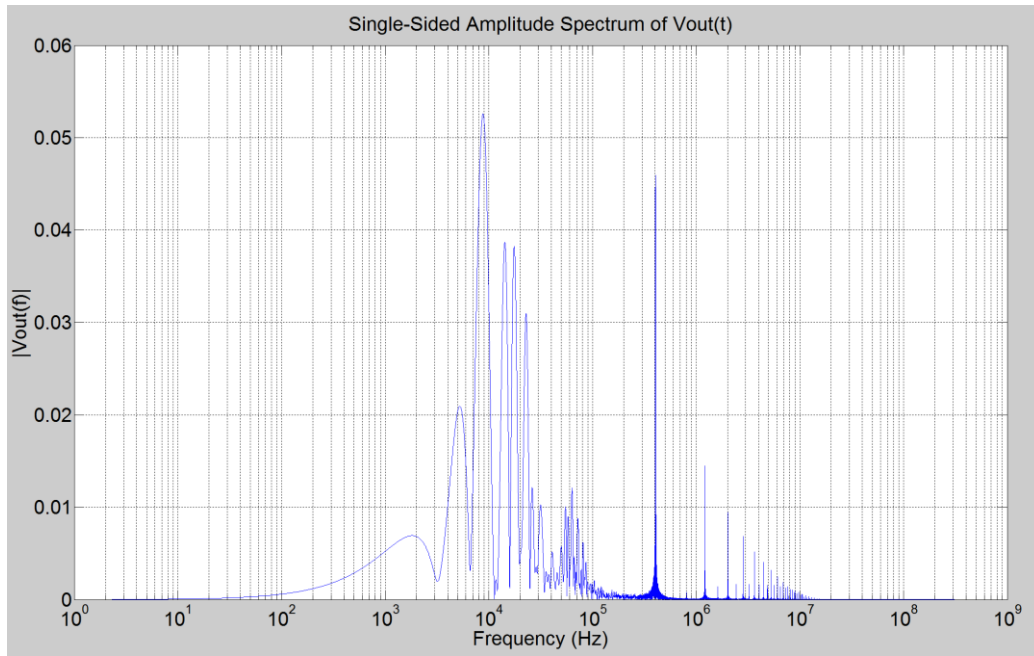
(a)
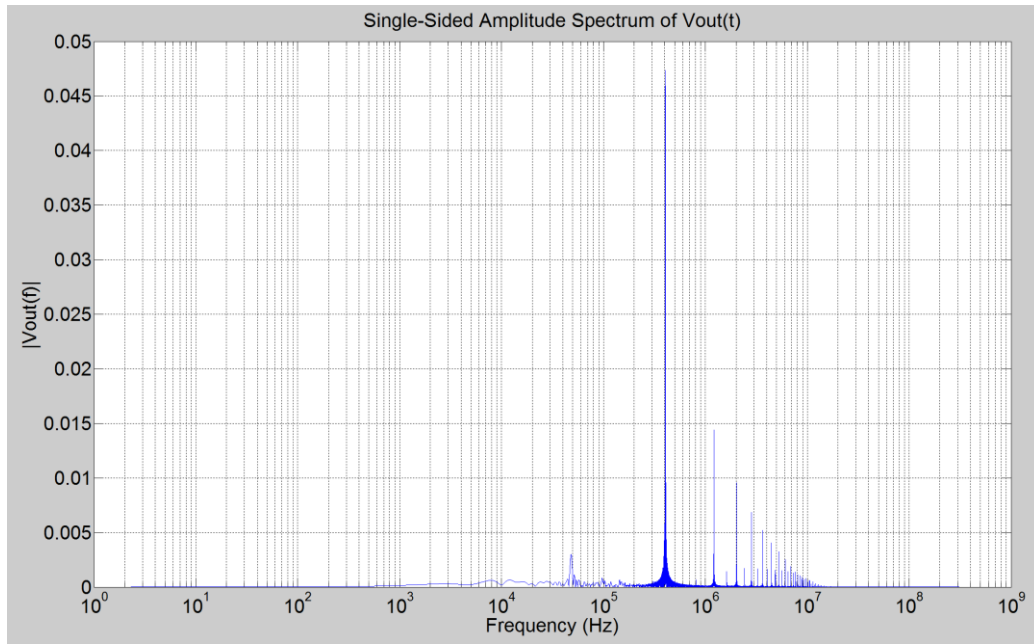
(b)

Figure 4. 7. Magnitude of an N-point DFT on V_{OUT} (high frequency rep rate transient). (a) Nonlinear loop enabled. (b) Nonlinear loop disabled.
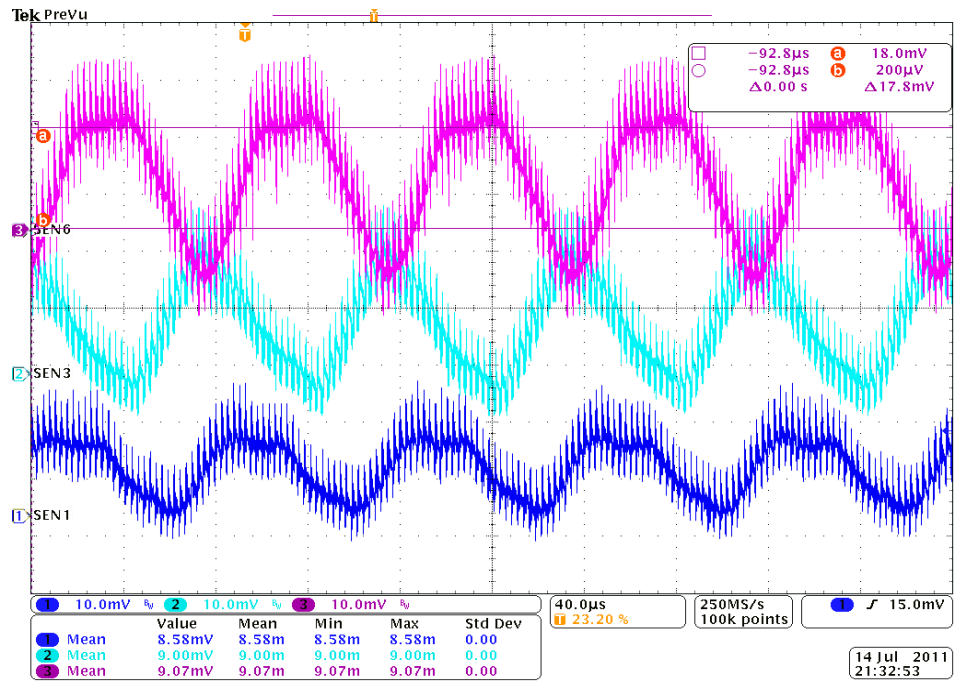
(a)
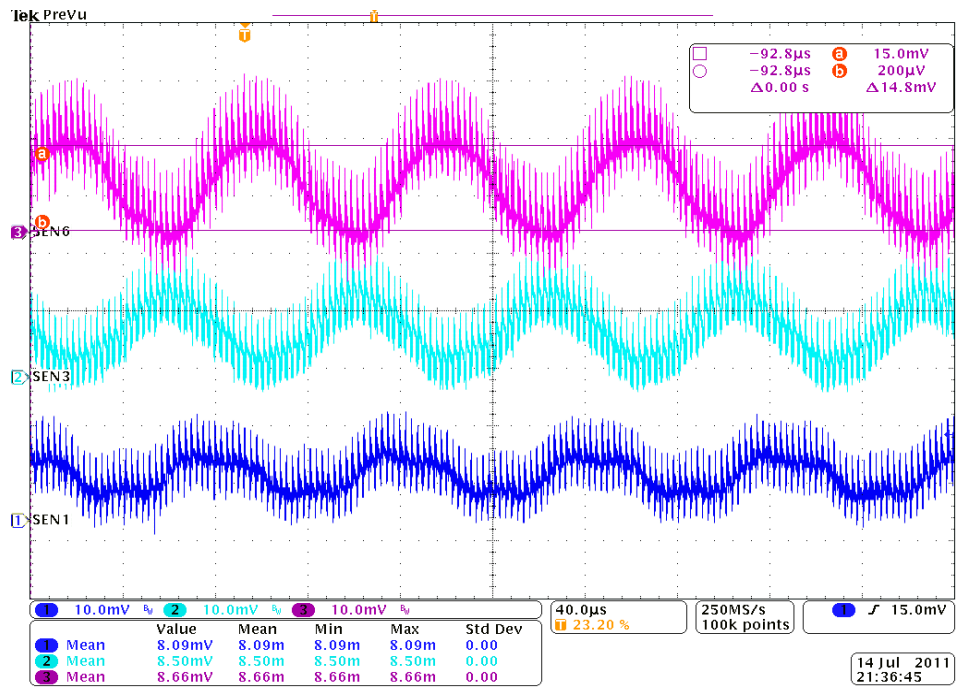
(b)

Figure 4. 8. Phase currents oscillation: transient step: 132A-165A, load frequency 385 kHz. (a) LFD disabled. (b) LFD enabled.

Figure 4. 8 shows the improved phase currents screen captures by implementing the proposed schemes. Magenta, cyan-blue and blue channels represent the 3 phase currents when load frequency is 385 kHz, which is around switching frequency. Figure 4. 8 (a) shows the circulating phase current among phases, the maximum sourcing and sinking current is 62A and -24A, respectively. Phase currents were measured using proprietary fixture with BNC cables.

CHAPTER FIVE: DYNAMIC VOLTAGE SCALING

Dynamic voltage scaling is an energy saving feature in modern processors. The multiphase VR design should have to facilitate CPUs to transit to the newer voltage level within the specification with minimum power conversion.

(a) Peak Power Reduction (b) Energy Saving
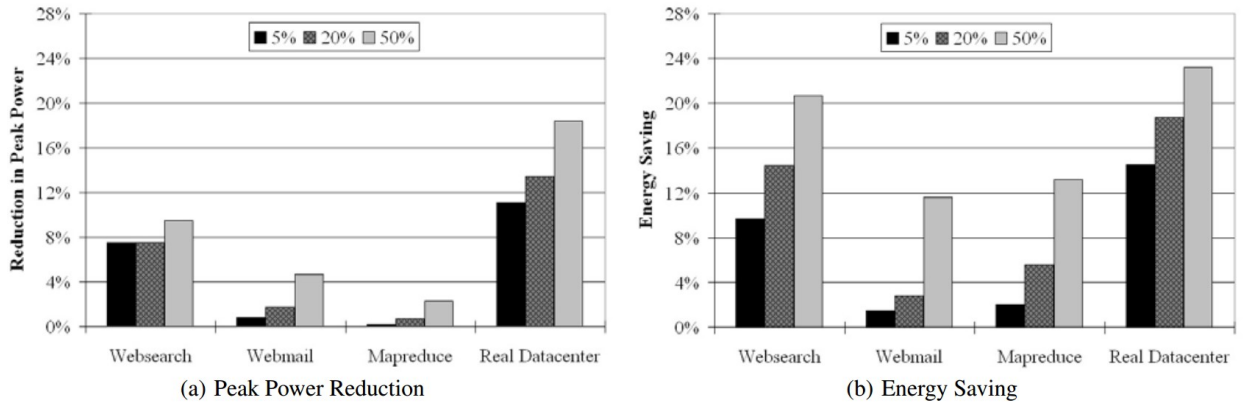
Figure 5. 1. The impact of DVS operation at datacenter level.

Figure 5. 1 [46] shows the impact of DVS operation at datacenter level and shows the significance of this operations.

5.1 Modes of Operation

In PFM, as shown in Figure 5. 2(b), PWM transitions from HiZ to high. Phase node moves from output voltage level to V_{BUS}. To achieve fast HiZ operation as depicted in Figure 5. 2 (b), EN toggle should be utilized in PFM operation. As the inductor current is reaching to zero, the LS turns OFF. The output voltage then decays as a function of load. Power MOSFETs remain HiZ until the output voltage drop below the regulation target to trigger a PWM on pulse.
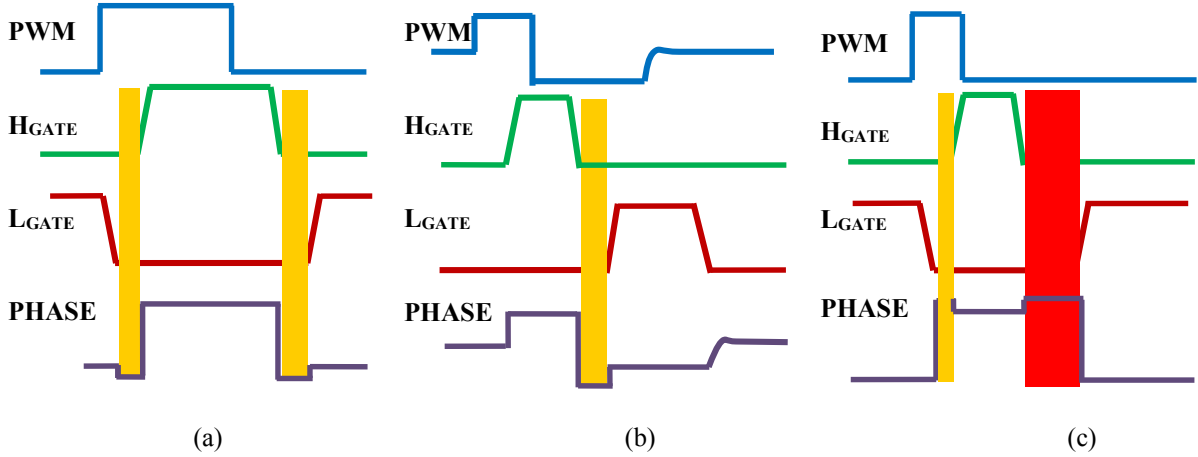
Figure 5. 2. Operational waveforms with the critical dead times: (a) Buck (Source) CCM; (b) Buck (Source) PFM; (c) Boost (Sink) Mode.

Under the boost mode, as shown in Figure 5. 2 (c), the phase node voltage is clamped to V_{BUS} plus a diode forward voltage drop after the HS MOSFET is OFF. The red rectangle represents $t_{watch-dog}$. LS MOSFET is hard switching after $t_{watch-dog}$. After LS MOSFET turns on, the current in the HS body diode commutates to the LS, going through the reverse recovery phase.

Inductor current in one phase and the corresponding LS V_{DS} waveform during mode transition are shown in Figure 5. 3 LS V_{DS} is starting negative because of the body diode voltage drop during $t_{dead-time}$. The edges in first V_{DS} pulse are sharp due to C_{OSS} charges and discharges very fast. After the $t_{dead-time}$, LS is turning on the voltage drop on the V_{DS} is $R_{DS}(on)$ multiplies the inductor current. The falling edge of middle V_{DS} pulse representing inductor equals to zero and C_{OSS} discharges very slowly. In the last pulse, V_{DS} is clamped to VIN plus diode forward drop V_{SD} during $t_{dead-time}$ and $t_{watch-dog}$, respectively.
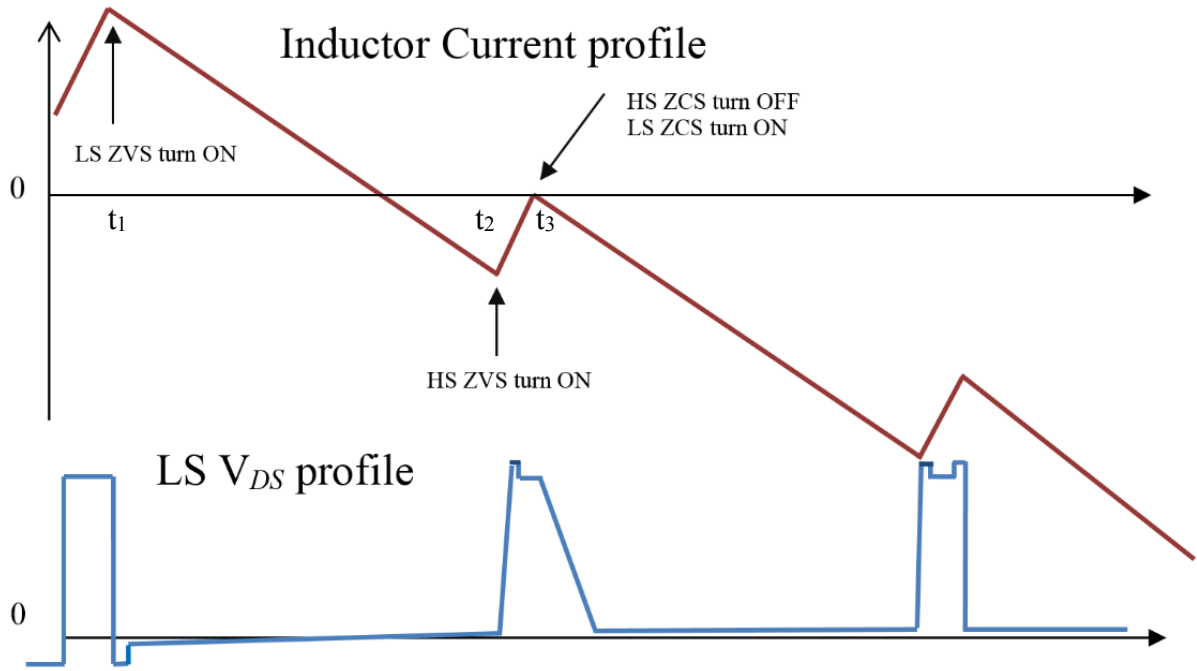
Figure 5. 3. Operational waveforms during mode transition.

In the buck mode operation at t_1, LS is ZVS turning on. During transition at t_2, the inductor is flowing through the HS body diode and HS is ZVS turning on. At t_3 when inductor current reaches zero, HS is ZCS turning OFF and LS is ZCS turning ON.

5.2 Driver Dead-time in Sink Mode

Given the switching frequency 385 kHz which is optimized by the system static efficiency, the efficiency result is shown in section V. The on time pulse of PWM ranges from 280 ns to 80 ns during the voltage transition from 1.2 V to 0.7 V. Figure 5. 4 illustrates impact caused by the driver $t_{watch\text{-}dog}$ in two consecutive switching cycles during DVID down. Discharging slope being the same (5.1):

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$$\Delta i_L = \frac{V_{OUT}(\tau) - V_{OUT}(\tau + \Delta t)}{2L} \Delta t \qquad (5.1)$$

where Δt represent the modulated OFF time or LS ON time between two switching cycles. Inductor current 2 sank more when $t_{watch\text{-}dog}$(red bar) is narrower, which effectively turns on the LS2 sooner, therefore, the V_{OUT} can be easily regulated and slewed down with respect to the internal reference DAC.
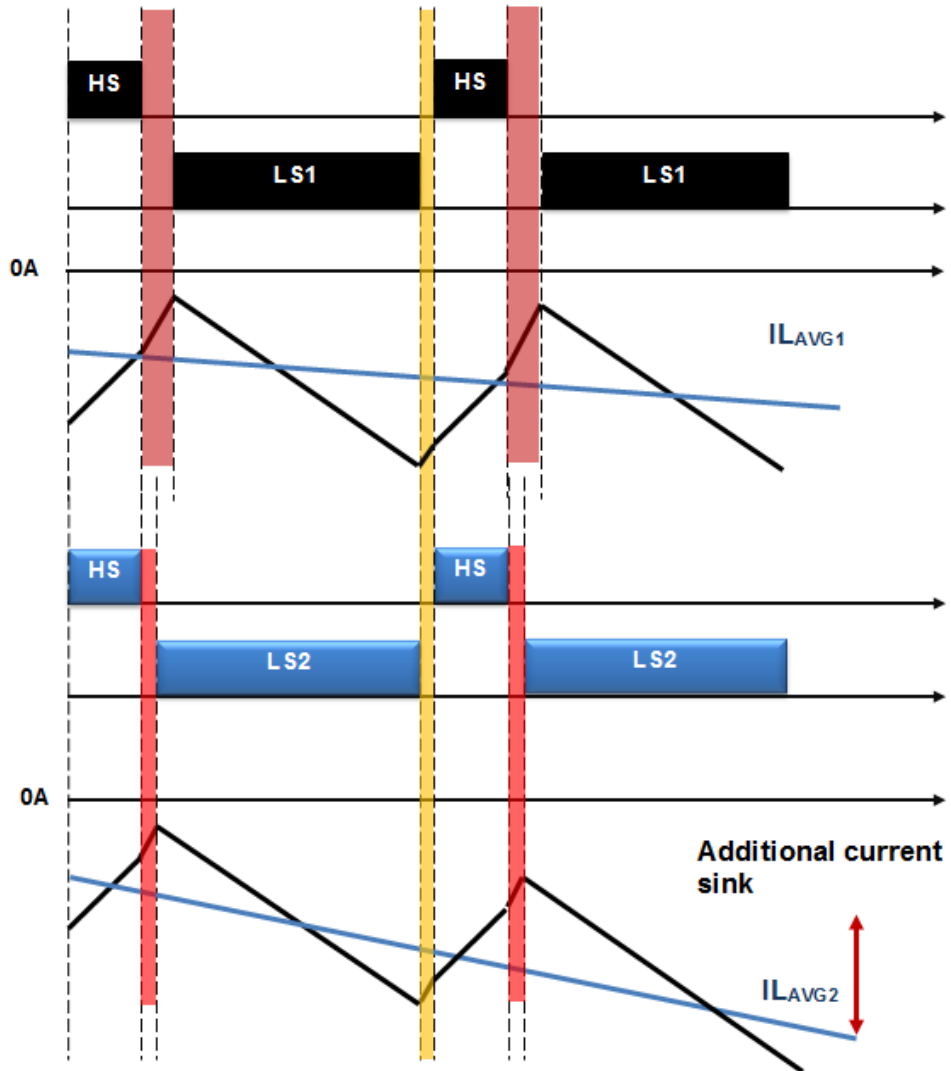
Figure 5. 4. System dynamic comparison of different driver $t_{watch\text{-}dog}$.
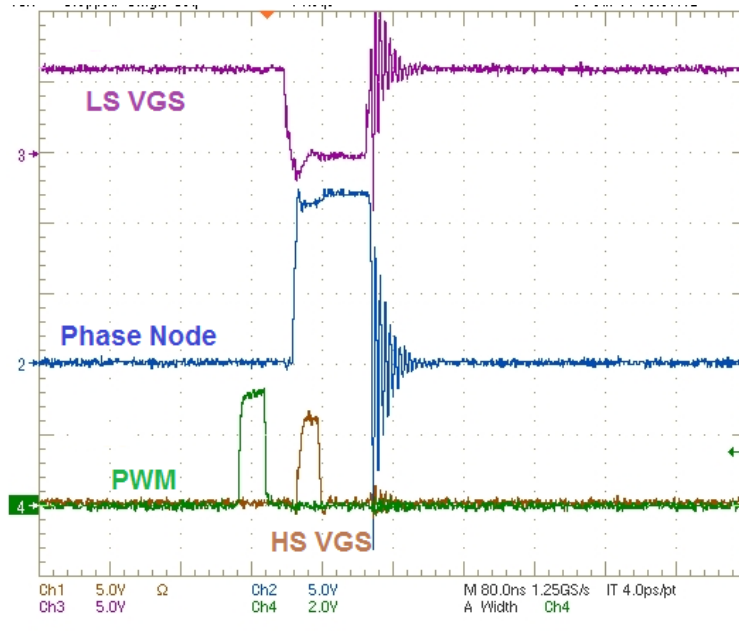
(a)
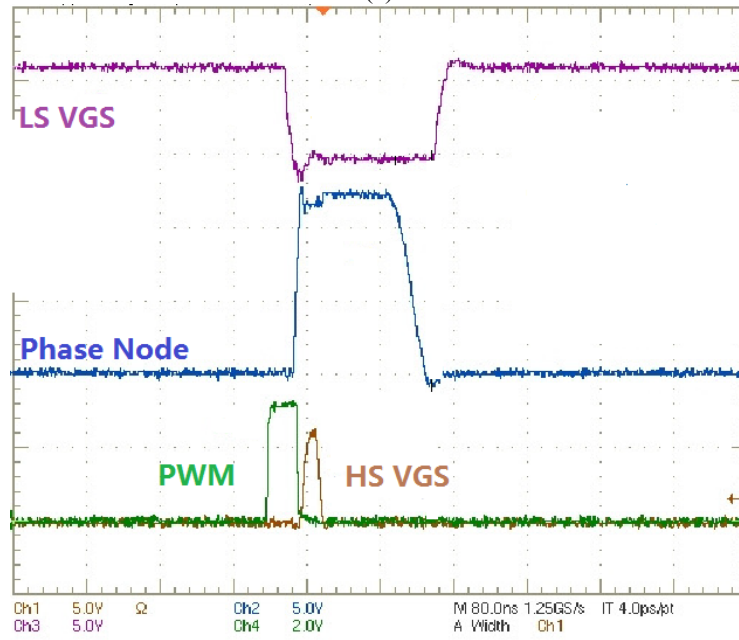
(b)

Figure 5. 5. Experimental waveforms with different design of $t_{watch-dog}$: (a) Boost (Sink) mode: $t_{watch-dog} = 60$ ns; (b) Boost (Sink) mode: $t_{watch-dog} = 120$ ns.

Because the designed voltage mode controller will skip the PWM high pulse once the sensed output is far beyond the reference DAC in the DVID downward operation. The prolonged $t_{watch\text{-}dog}$ would cause essentially turning on the LS MOSFET of one phase asymmetrically, therefore generate the unbalanced negative inductor current between phases. The MOSFETs and VR long term reliability would degrade.

Figure 5. 5(a) illustrates the scenario of $t_{watch\text{-}dog}$ equals to 60 ns when the converter is working in the boost mode (the output inductor current is negative). The driver actively sinks current by "hard" turning on the LS MOSFET. Figure 5. 5(b) illustrates the scenario of $t_{watch\text{-}dog}$ equals to 120 ns when the converter is in the DVID operation. The output inductor current reaches zero, C_{OSS} of the LS MOSFET discharges and the driver waits for the phase node goes low then turns on the LS MOSFET. The inductor energy is being discharged entirely back into input capacitors. The extra 60 ns in $t_{watch\text{-}dog}$ introduce a delay in regulation which makes DVID downward regulation very difficult.

5.3 Control MOSFET Stress Suppression

Repetitive avalanche can occur in the power MOSFETs in buck converters when the voltage across the MOSFET exceeds the BVDSS voltage specified in the datasheet of the Power MOSFET.
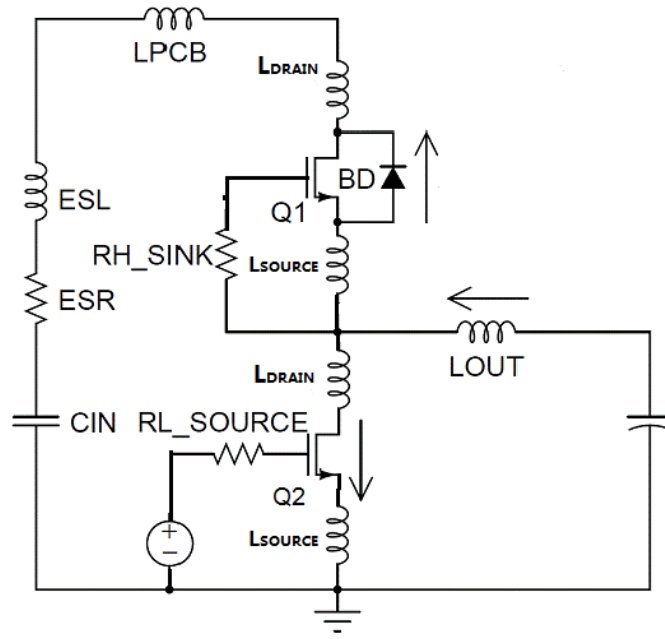
(a)
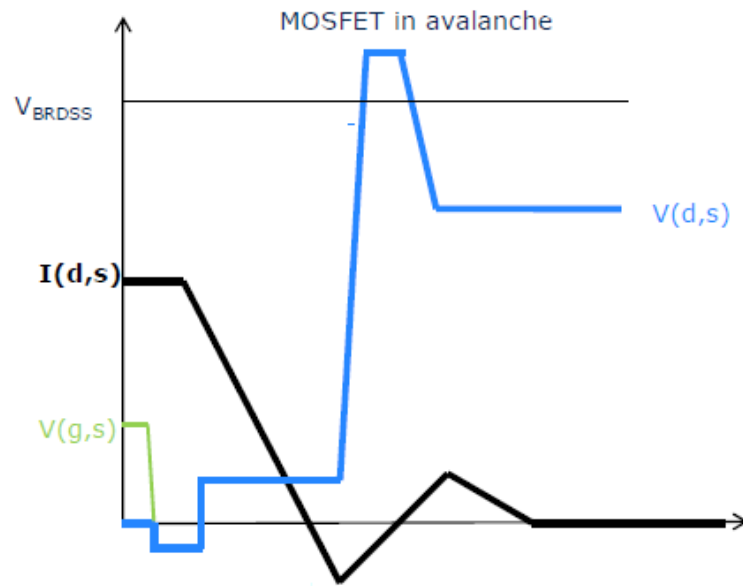
(b)

Figure 5. 6. (a) Discrete solution of the converter considering circuitry parasitics in the boost mode; (b) HS MOSFET enters avalanche due to high di/dt and parasitic inductance.

The schematics of the discrete type of solution with circuitry parasitics are shown in Fig. 9 (a) when the converter is in the boost mode. The HS V_{DS} can be mathematically expressed as:

$$V_{DS}(t) = V_{BUS} + L_{STRAY}\frac{di_D(t)}{dt} \qquad (5.2)$$

where L_{STRAY} is loop parasitic inductance including L_{PCB}, L_{DRAIN} and L_{SOURCE}. i_D is the diode reverse recovery current. A MOSFET spike approaching breakdown voltage level can inflict high current transients on the MOSFET. While the body diode of HS MOSFET is conducting current during the $t_{watch\text{-}dog}$ time slot, the diode PN junction are stored with minority carriers.
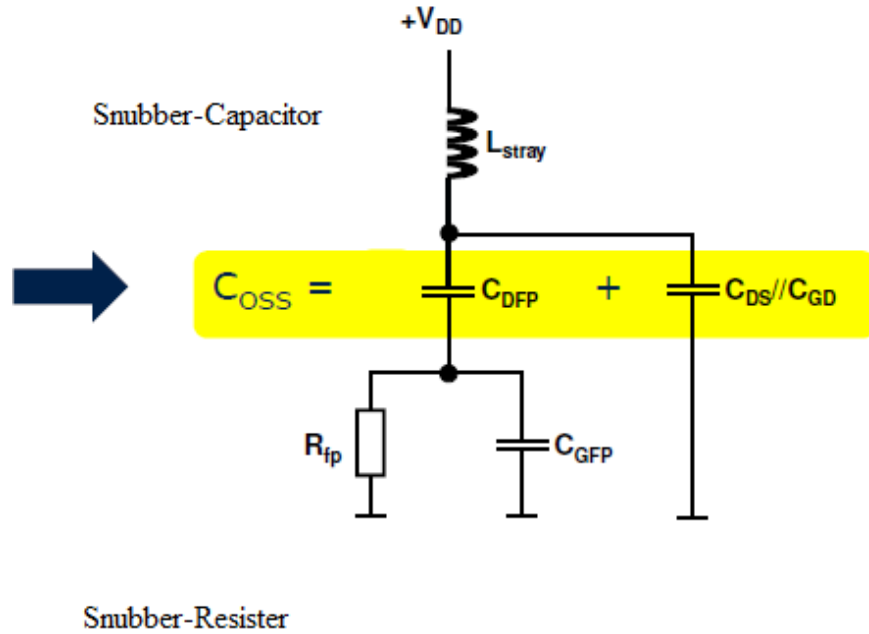
Figure 5. 7. Equavelent circuitry with snubber when MOSFET is in off state.

Figure 5. 7 shows the equivalent circuitry with snubber circuit when MOSFET is in off state. C_{GFP} is formed by gate electrode, interelectrode and field electrode. R_{fp} is the field-

electrode resistance between source terminal and field electrode. Fine tune the snubber resister, R_{fp}, is very critical in the MOSFET design to surpress the V_{DS} ringing.
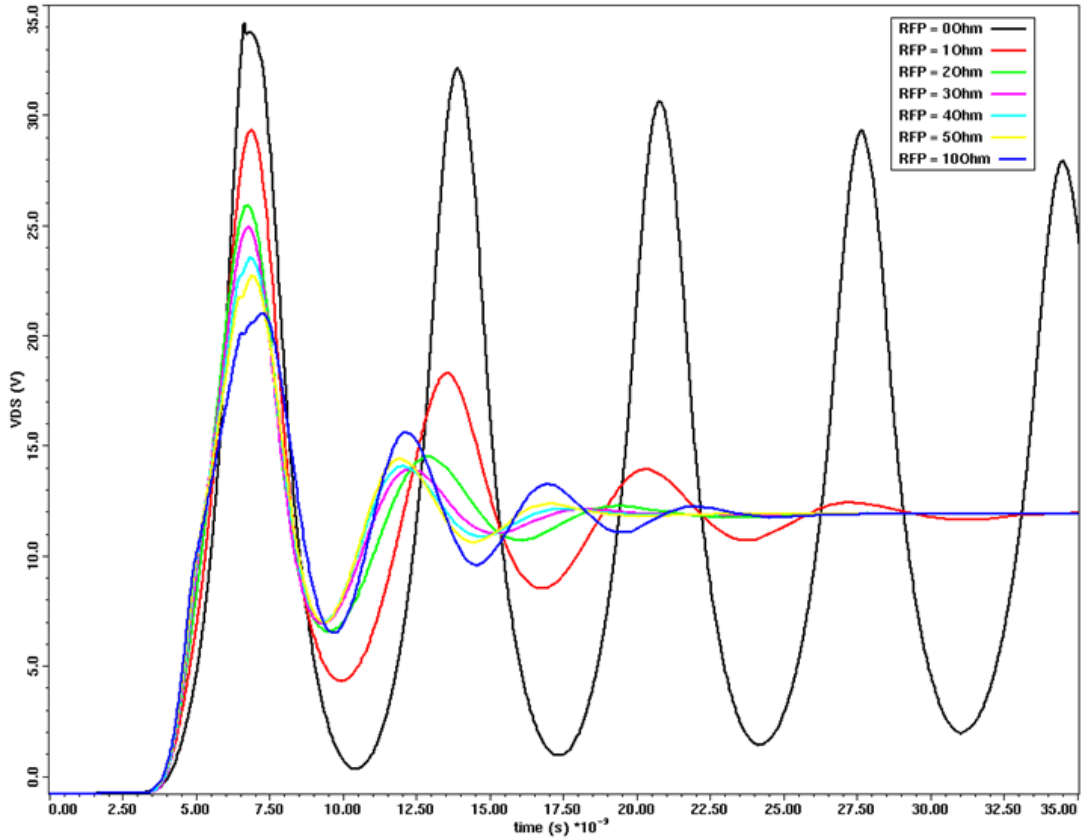
Figure 5. 8. Simulation result of HS V_{DS} waveforms with different snuber resister R_{fp}.

Figure 5. 8 shows the Simetrix simulation result of the damping effect of HS V_{DS} waveforms by varying R_{FP} resistance. The snubber resister cannot be too large, as the blue curve indicates, which produces a shoot-through condition and degrades the system reliability and efficiency. Likewise, the resistance cannot be too small, which indicates the avalanche syptom. 3 Ohm can be chosen as a optimal value for the snubber circuitry.

In Figure 5. 9, the screen capture shows the HS VDS during the fast DVID (a) 20 mV/μs and (b) 40 mV/μs down in the fast acquisition mode. The maximum amplitude of VDS in Figure

5. 9(b) is 20.6 V which is reduced by 4.4 V compared with the result in Figure 5. 9(a) or [41] because HS with smaller QRR are implemented and also damped by intrinsic internal snubber structure in MOSFET.
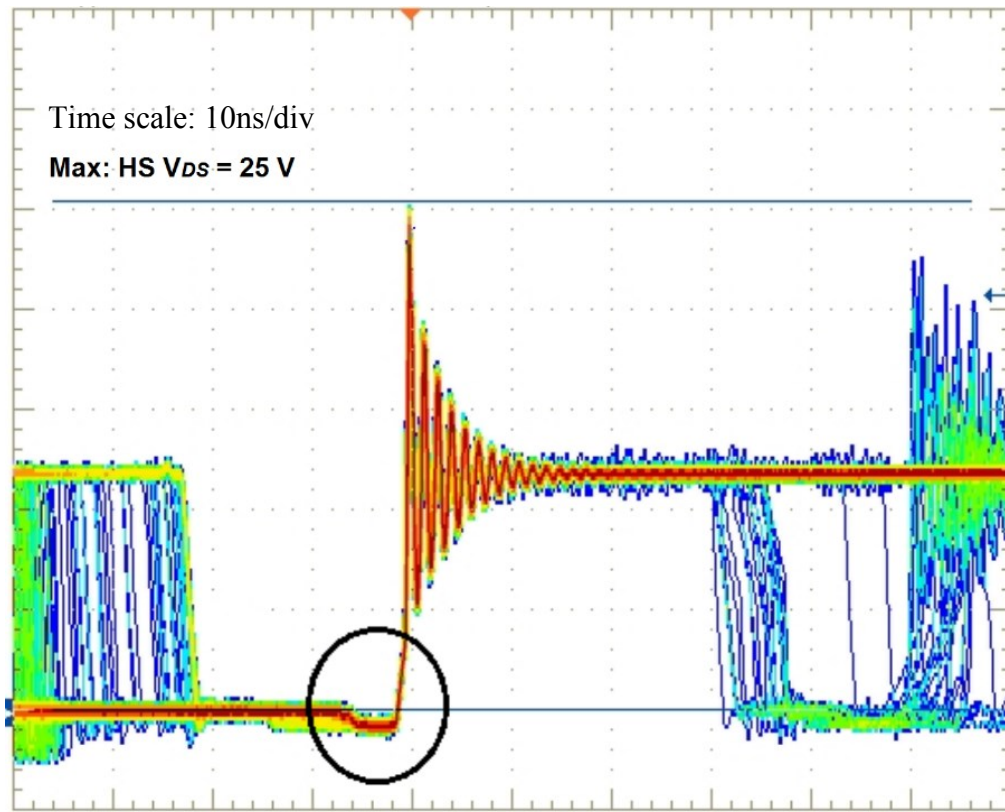
(a)
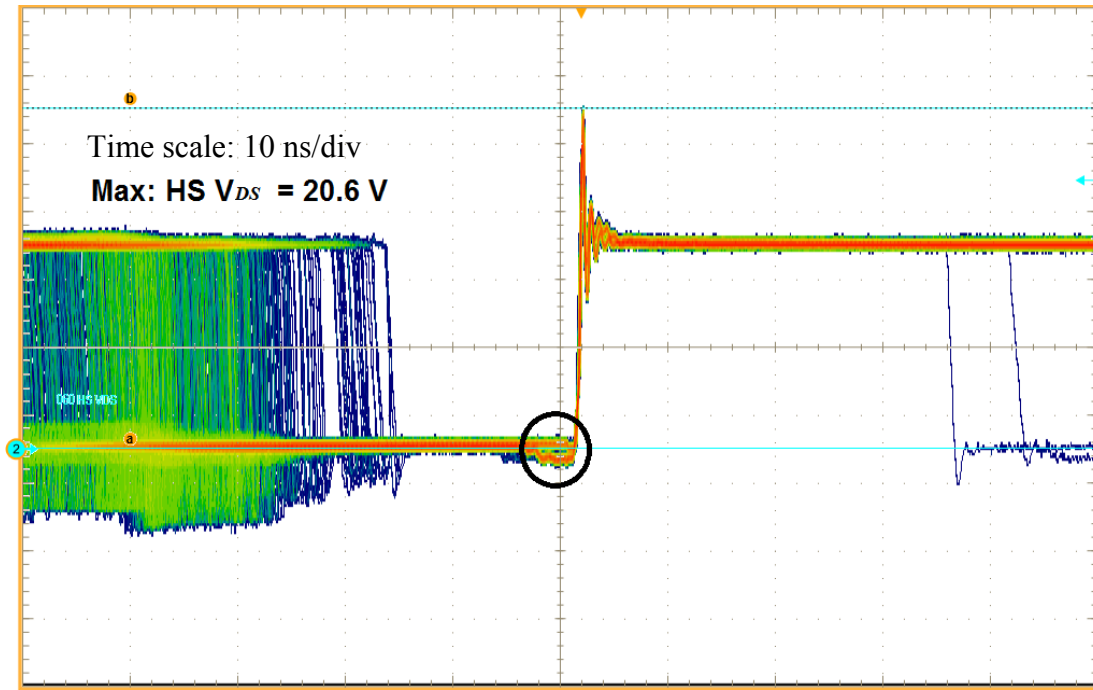
(b)

Figure 5. 9. High side V_{DS} during repetitive DVID operation: (a) Q_{RR} = 20 nC and without snubber circuitry; (b) Q_{RR}= 10 nC with snubber circuitry. Channel 2: HS drain-source voltage, 5V/div.

During DVID downward transition, the inductor current is flowing reversely because the energy stored in the cap banks dumps back to the input side. The circled area shows when HS turned off and body diode of HS is conducting. The excessive spike on V_{DS} may lead to impact ionization and avalanche of the MOSFET. According to simulation and experimental verification, there are three ways to reduce the ringing on V_{DS}:

- Embed and fine tune the internal snubber structure;

- Embed one more layer of Schottky barrier diode in the HS MOSFET design, which essentially reduces Q_{RR};

- Use integrated power stage, such as stacked-die package, which reduces the parasitic inductance.

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5.4 DVS Responsiveness Optimization

The voltage transition during dynamic voltage scaling should meet the timing and voltage excursion requirements of the specific CPU application. Nonlinear control scheme and Cdv/dt compensation are introduced to fulfill the smoothness of this dynamic transition.

5.4.1 Nonlinear Control Scheme
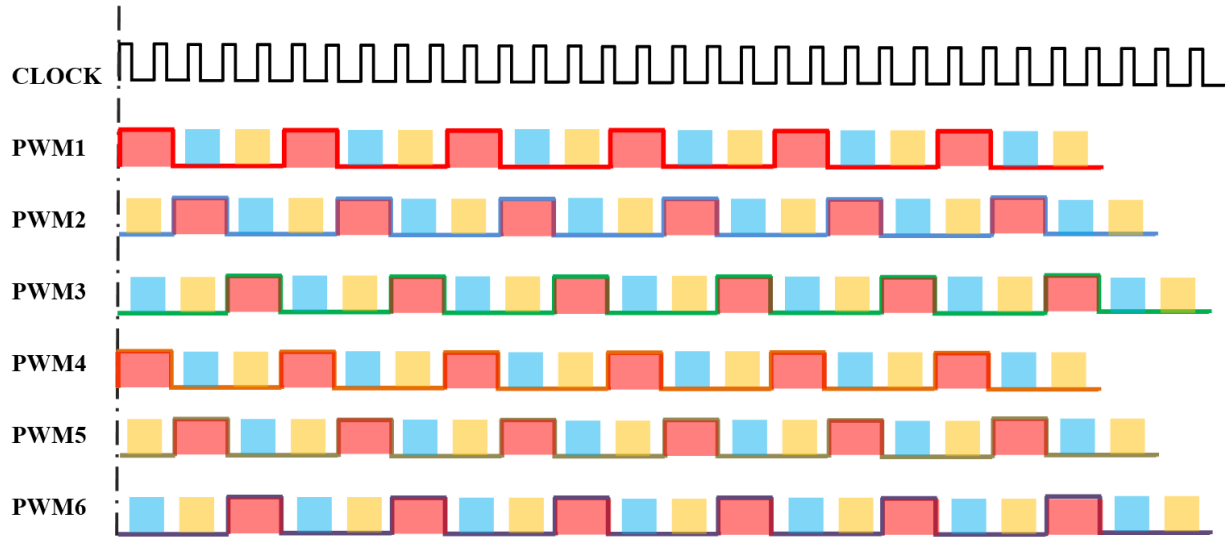
Figure 5. 10. The timing architecture of the multiphase controller.

Figure 5. 10 shows the timing architecture of the multiphase VR. It is not only useful for dealing with low frequency load transient, it can help smooth the voltage output during DVID operation, especially during DVID downward transition.

5.4.2 CdV/dt Compensation

AVP is an advantageous technique for load transient events. The AVP loop, however, should be carefully examined in the DVID design. It uses the total inductor current to represent the load current, however, during VID changes, even though the load current stays constant, there is amount of phase current, CdV/dt current to charge or discharge the output capacitors. The extra amount of total inductor current is in the closed loop that can affect the V_{OUT} regulation target according to (4). The AVP loop creates a lag and slows the V_{OUT} settling in DVID upward transition. The slow settling generates the issue for Alert timing in the sVID bus if the stringent timing is required in the processor application.
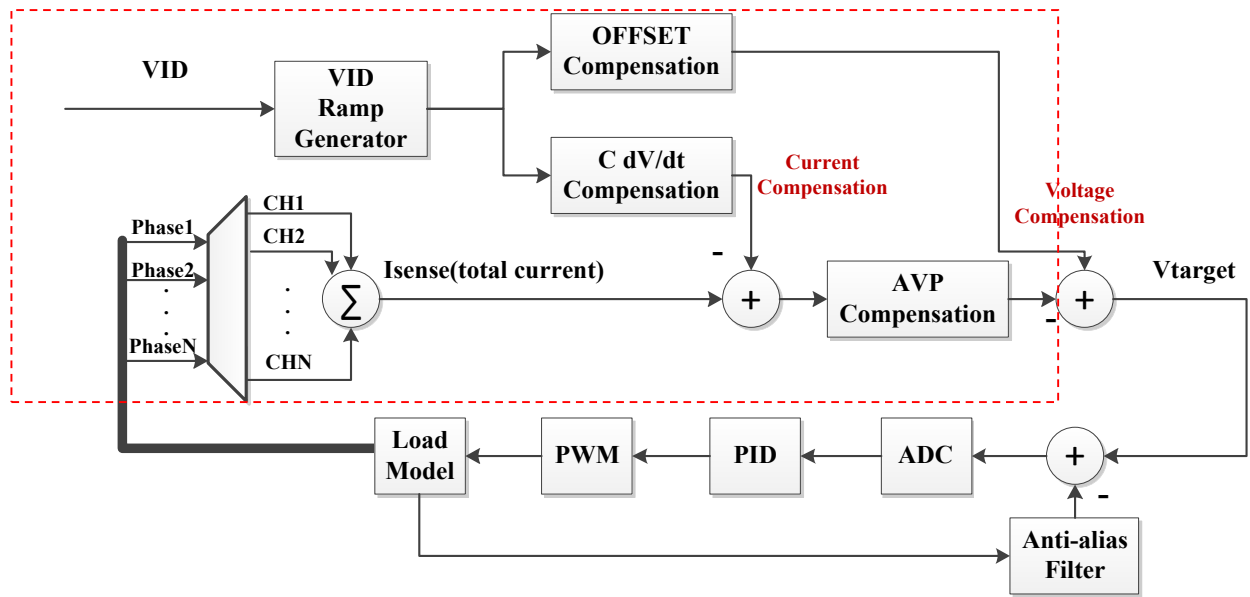
Figure 5. 11. Architecture of DVID module with compensations.

Figure 5. 11 illustrated the architecture of DVID compensation in both current and voltage aspects. It is very critical for compensating the droop current, the current for charging the output capacitors during dynamic operation and thus catching the timing of DVID upward

transition. It is very critical for the VR to drive the Alert line to low, by which the Processor acknowledge the readiness for the voltage transition. The current compensation digitally subtracts the absolute value of the sensed total current, therefore, the AVP effect is removed in the current loop during DVID. The voltage compensation adds a programmable offset, which reshapes the ramp DAC during the initial and final transitions for speeding up and smoothness purposes. During DVID upward transition, the sensed output voltage is actually the voltage across the capacitor plus the ESR voltage generated by Cdv/dt current. There need to be an offset voltage to compensate the sag of the ESR drop at the end of the transition.

(a)

99
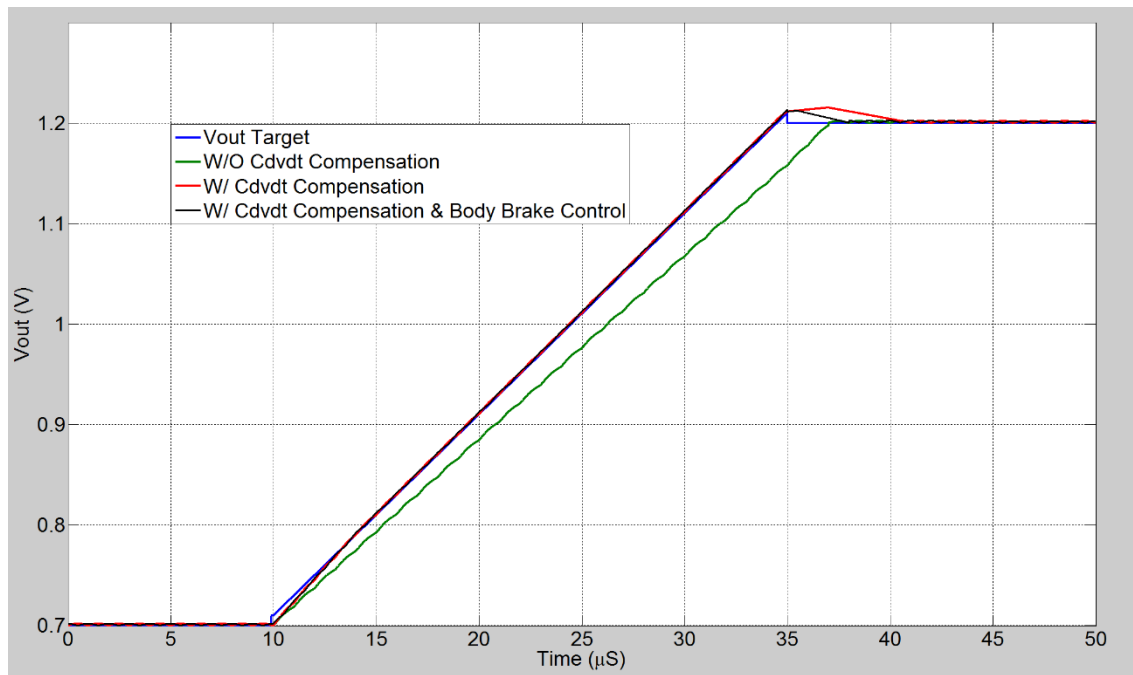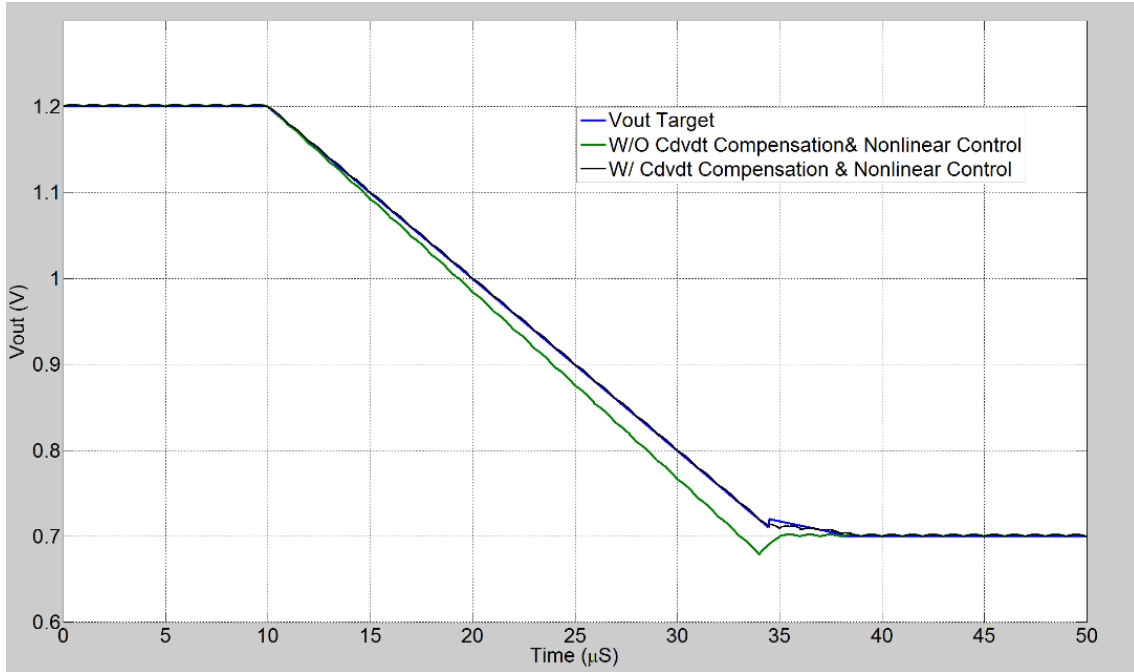
(b)

Figure 5. 12. Matlab simulation result of DVID transition with and without droop compensation and nonlinear control: (a) DVID upward transition; (b) DVID downward transition.

DVID transitions are simulated using Matlab and presented in Figure 5. 12. The V_{OUT} with CdV/dt compensation (red and black curves), in Figure 5. 12 (a) was regulated tightly to the V_{Target}. Body brake control can further reduce the overshoot during DVID upward transition as indicated in the black curve. As shown in Figure 5. 12 (b), the reshaped V_{Target} with Cdv/dt compensation can bring in extra asynchronous pulses at the end of the transition to ensure no undershoot occurs.

Figure 5. 13(a) and (b) show experimental waveforms of fast DVID transition with CdV/dt compensation (Cyan) and without the compensation (Black). Six digital channels in the scope shots represent the six PWM signals of the VR.

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The excessive undershoot of output voltage during DVID transition should be prohibited since it can cause the system hang or blue screen in the server systems. As indicated by the asynchronous pulses (digital channels) in the red rectangles, the reshaped ramp pattern adds an voltage offset at both beginning DVID upward and the end of the DVID downward transaction, which ensures to speed up the DVID upward transition and eliminate the undershoot in the downward transition.
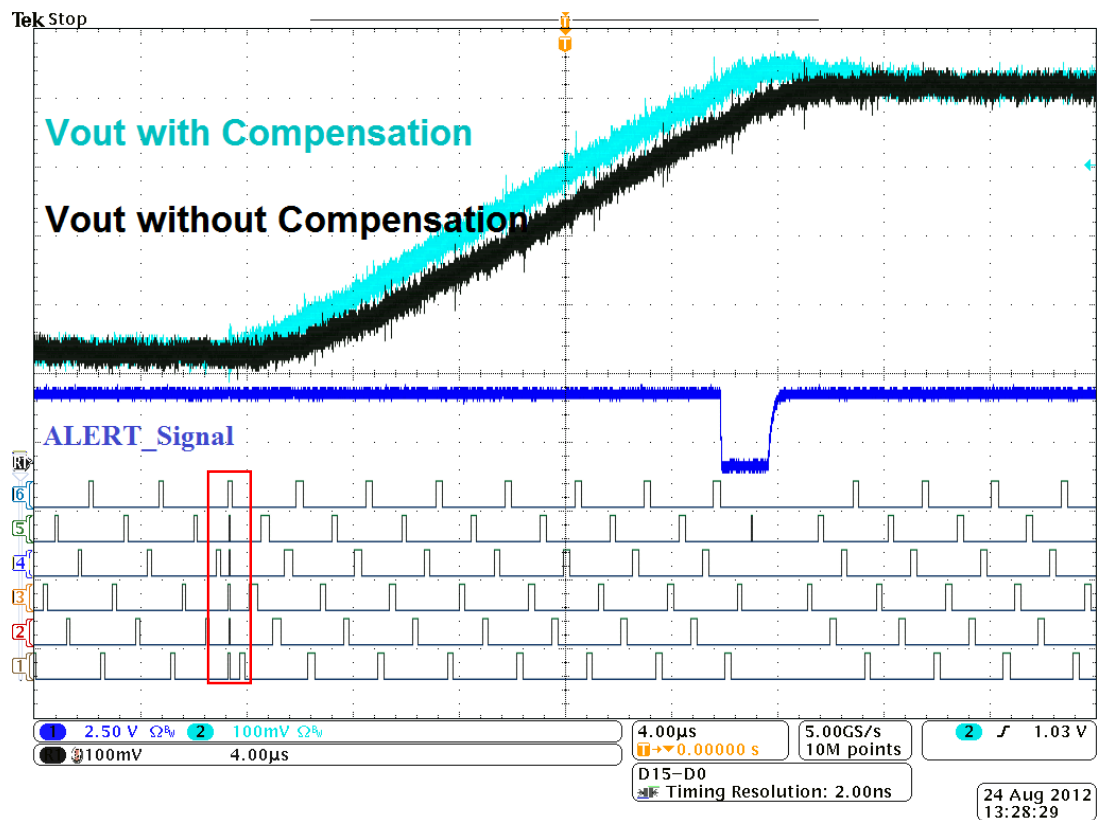
(a)
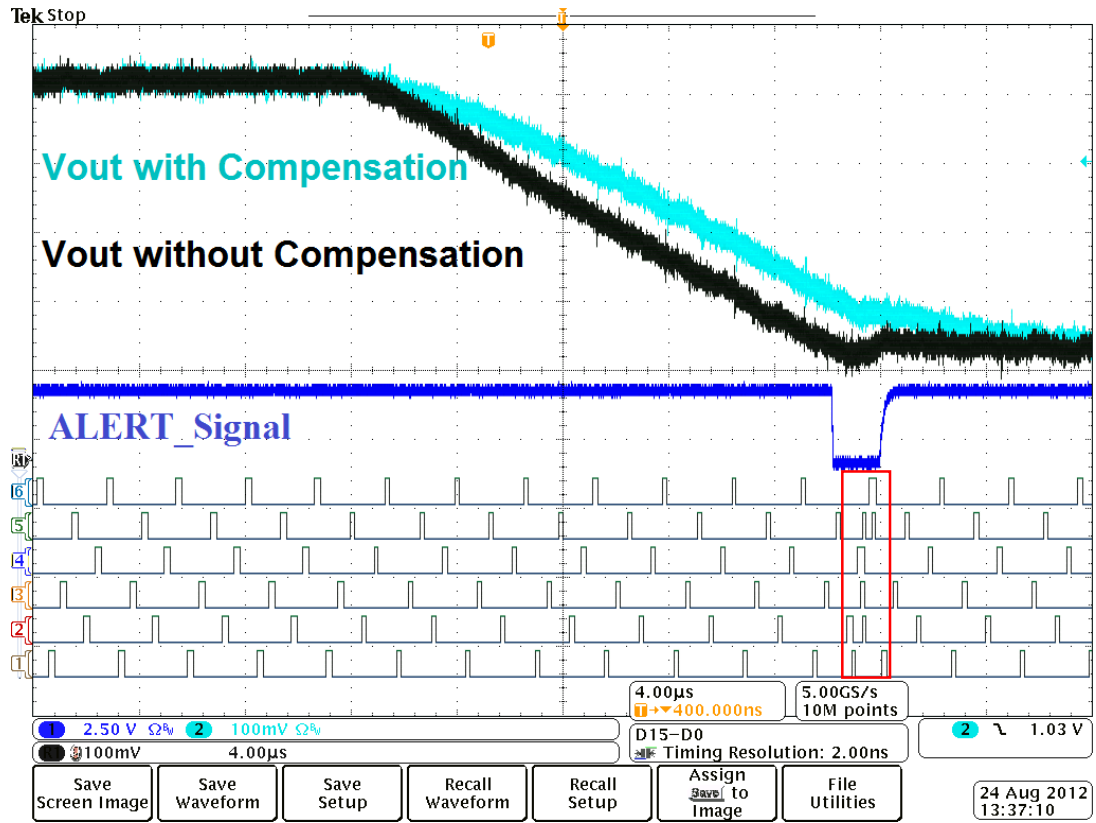
(b)

Figure 5. 13. Experimental waveforms of fast DVID transitions with/without $C \cdot dV/dt$ compensation: (a) Fast DVID upward transition; (b) Fast DVID downward transition.

Given the total output capacitance C_O, the relationship between the sinking/sourcing current and DVID slew rate can be expressed by:

$$I_{sink/source} = C_O \frac{dV}{dt}$$ (5. 3)

Server processors roughly have about 4000 μF of C_O in each VR. At 20mV/μs DVID rate: 80 Amps of source or sink current during DVID.

5.4 Current Sharing during DVS

In order to ramp up or down the voltage on the output capacitor according to the sVID transactions, an extra amount of phase currents need to charge or discharge the output capacitors. The phase current during transitions, especially DVID downward operation, should be shared evenly among the active phases.
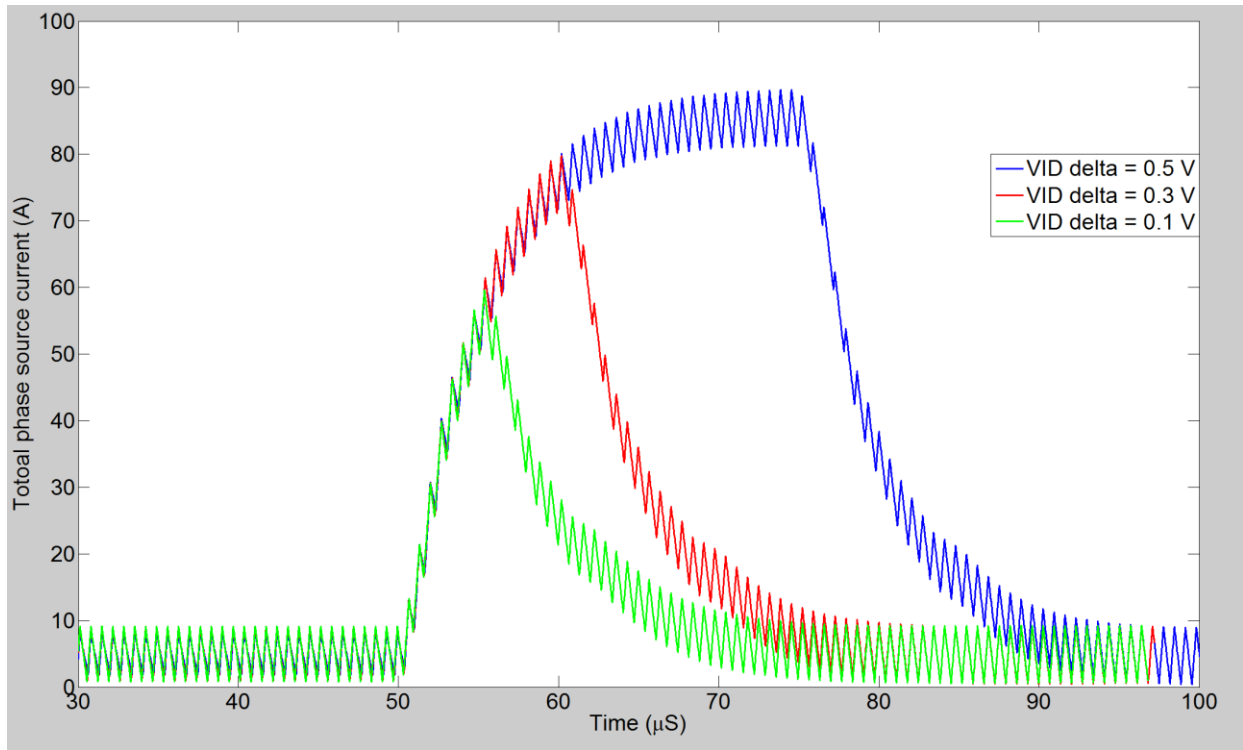
(a)
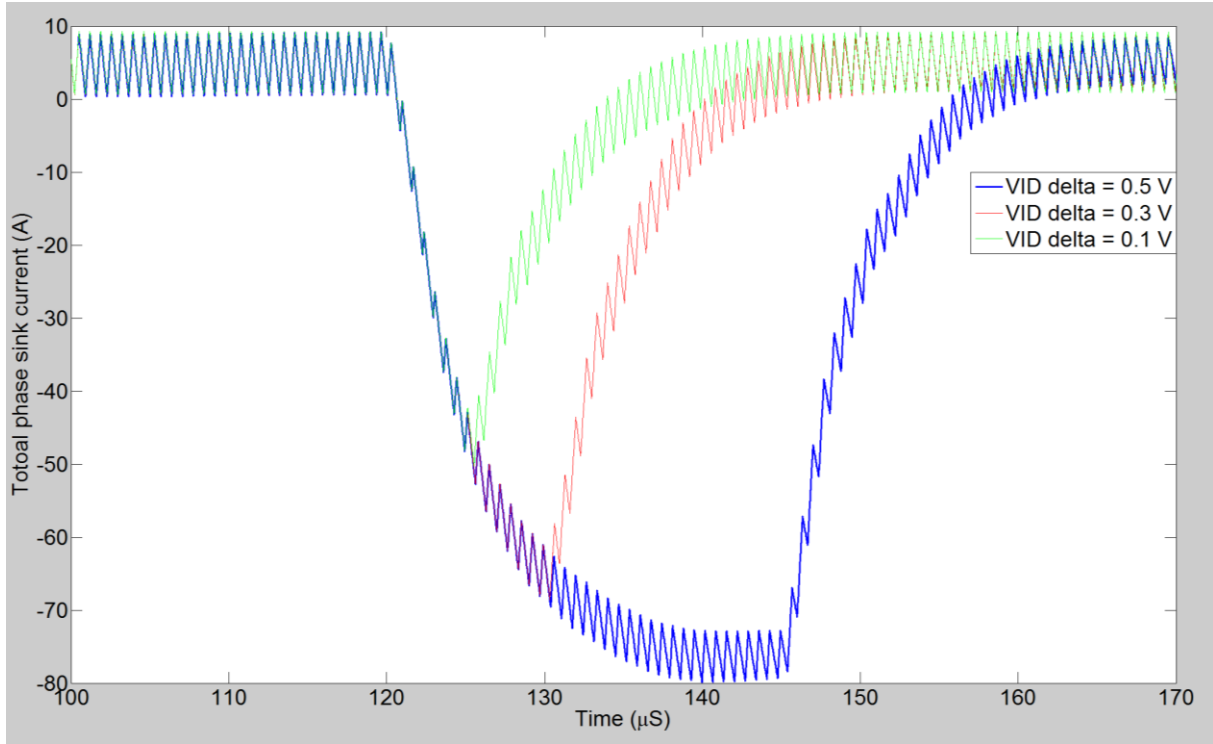
(b)

Figure 5. 14. Simulation result of total phase current. (a) Source current at different VID transition. (b) Sink current at different VID transition.

Figure 5. 14 shows the simulation results of total charge and discharge phase current during 3 different VID transition, which are 1.2V-0.7V (in blue), 1.2V-0.9V(in red) and 1.2V-1.1V(in green), respectively. As the equation (5.3) indicates, the VID delta represents different sink/source energy. Figure 5. 14 (b) can enforce the VR in sink (boost) mode, so the inductor current flows reversely and the negative current need to be shared during this operation. As it has been discussed in the previous section that $t_{watch-dog}$ is an important IC parameter that need to be optimized. If the value is too big, the controller can turn on the LS asymmetrically and the phase current cannot be shared evenly among phases since during this operation, the priority operation of the controller is to ramp down the V_{OUT} in a controlled fashion.
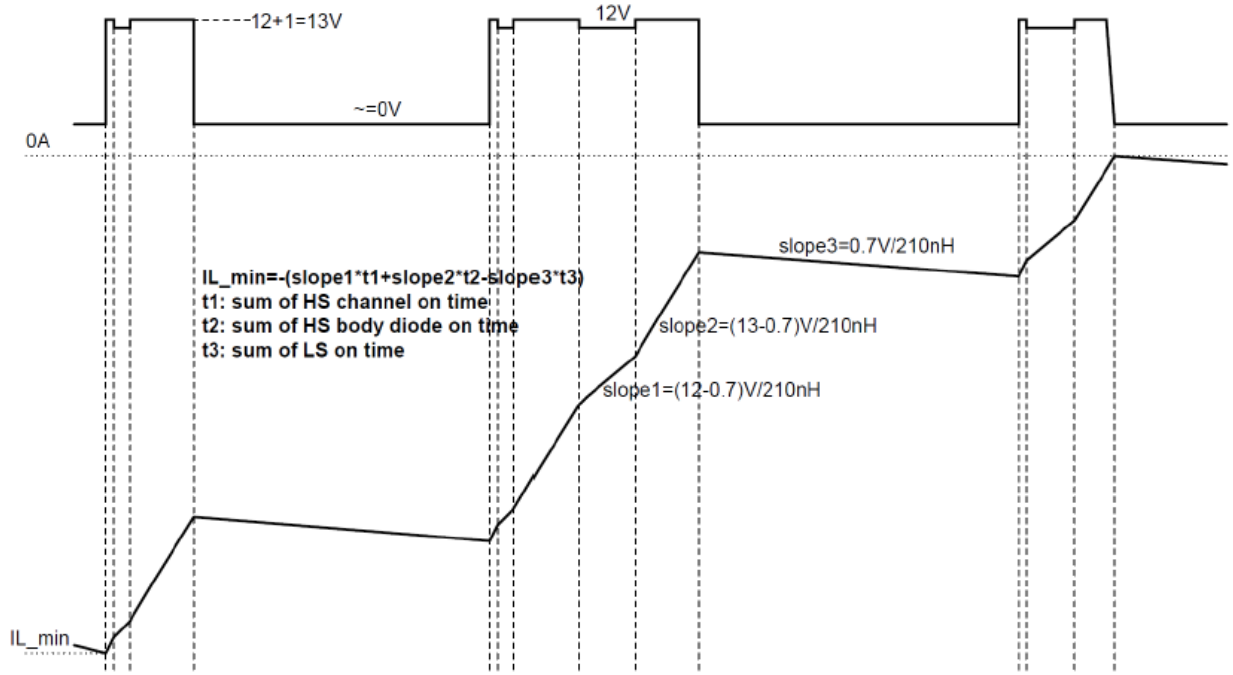
Figure 5. 15. Negative current calculation in DVID downward transition.

The worst case negative current in one phase can be calculated by measuring the time and applies to the corresponding slope section in this illustration. There are totally three inductor current slopes, which are HS ON slope1, HS body diode ON slope 2 and LS ON slope3. And we know this happens at the end the very end of downward transition, so we assume the V_{OUT} equals to 0.7V. . And the inductance we assume not varied with load

$$P_{induced\_loss} = (E_{conduction} + E_{Avalanche}{}^{*}) \times f_{rep\_rate} \qquad (5.4)$$

*: if there is avalanche.

105
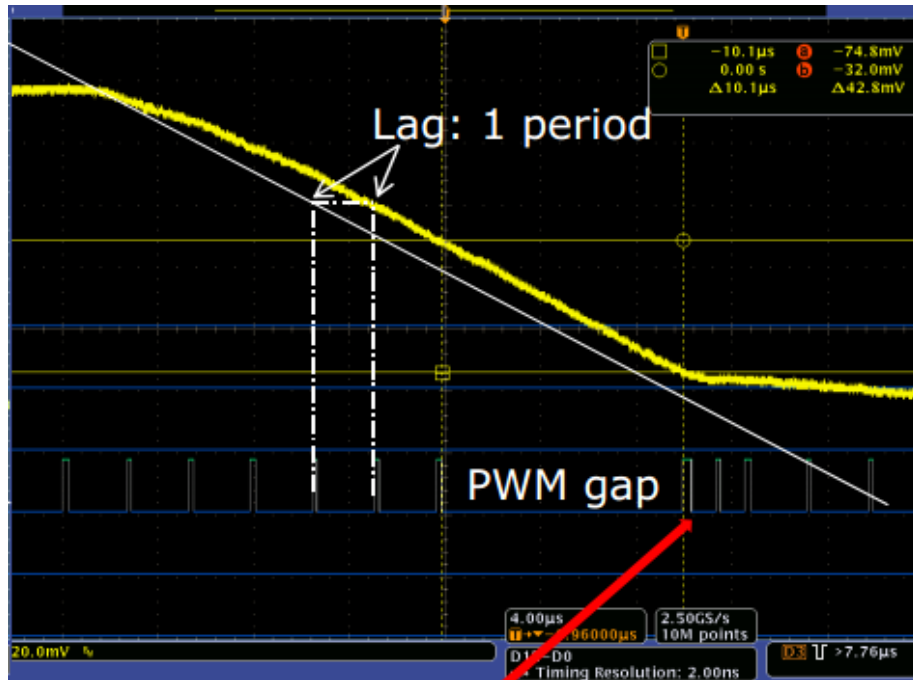
(a)

(b)

Figure 5. 16. Vout regulation comparison of different driver $t_{watch-dog}$ during DVID down.

(a) Sink mode: $t_{watch-dog}$ =120 ns; (b) Sink mode: $t_{watch-dog}$ = 60. ns.

In order to accomplish the DVID downward operation in the controlled fashion, the energy stored in the output capacitor must be discharged. The phase current must sink fast enough to regulate down the voltage.

5.5 Phase Number Control during DVS Operation

In dynamic voltage operation, the phase number should also be optimized when VID transits, but as the function of VID delta. As discussed in previous section, there are two operation modes, i.e. buck and boost, respectively. The switching characteristics are shown in Table 5. 1.

TABLE 5. 1 SWITCHING CHARACTERISTICS

	HS	**LS**
Buck mode	"Hard" switching	"Soft" switching
Boost mode	"Soft" switching	"Hard" switching

TABLE 5. 2 MOSFET CHARACTERISTICS

	HS (BSZ036NE2LS)	LS (BSC014NE2LSI)
R_{ds_on} (mΩ)	3.6	1.4
R_g (Ω)	0.9	0.6
Q_{gs} (nC)	3.1	7
Q_{gd} (nC)	1.9	7
Q_g (nC)	7.7	19
Q_{RR} (nC)	10	5
Q_{OSS} (nC)	9.4	25

Table 5. 2 shows the MOSFETs employed in the experiment, including static, gate charge and reverse recovery characteristics.

A six phase synchronous buck converter is designed and built to support 145 W high-end EP CPU as shown in Figure 5. 17 Intel VRTT (Voltage regulator testing tool) is used to emulate the behavior of CPU to generate and acknowledge all the sVID commands for DVID transactions. The operating voltage of the CPU is controlled by the internal PCU (power control unit), and the step of change can be varied from 5 mV (LSB) to 0.6 V for a 1.05 V (nominal output) CPU application.
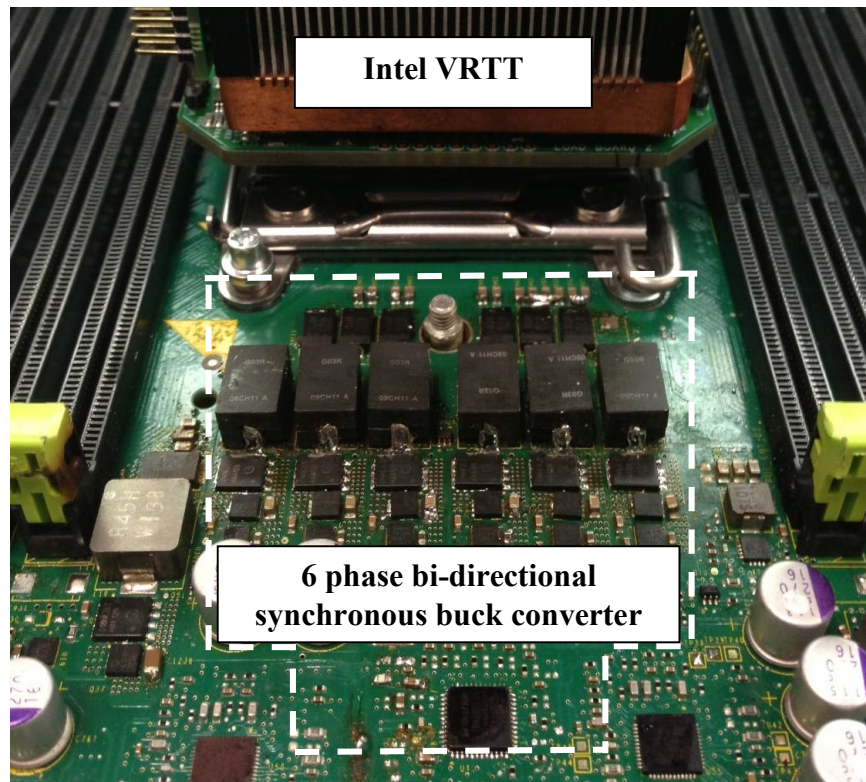
Figure 5. 17. A six phase synchronous buck converter with Intel VRTT.

A multiphase buck converter prototype was setup to verify the optimization for the proposed control strategy. The experiment is done by using Intel VRTT which can set repetitive dynamic transition from two different VIDs. Input power matrix is captured and presented in

Figure 5. 18. Each data point, P_{IN_DVID}(phase_count, VID_delta, frequency), represents one scenario of the matrix.
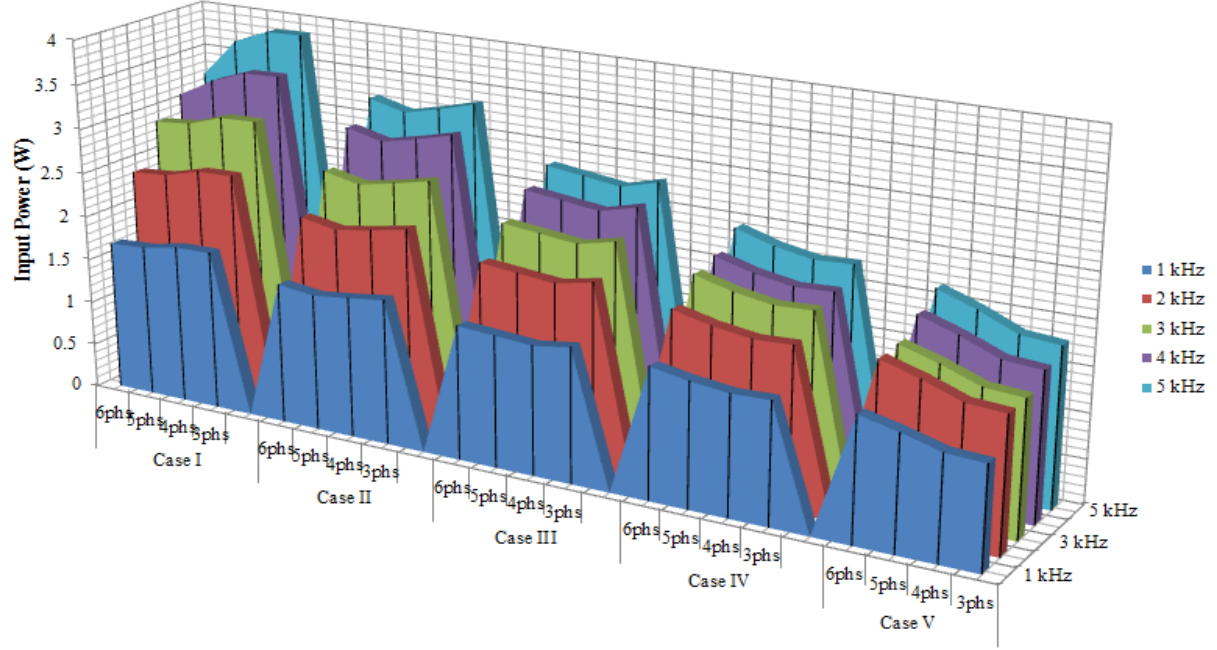
Figure 5. 18. Input power consumption matrix(4×5×5): number of active phases in 5 VID thresholds and repetative DVID operation.

Case I, II, III, IV, V represent VID change from 1.2 V to 0.7 V, 1.2 V to 0.8 V, 1.2 V to 0.9 V, 1.2 V to 1.0 V, 1.2 V to 1.1 V, respectively. Each VID delta represents a certain amount of energy been transferred back and forth during the repetitive operation. The controller can fire up to six phases to do the transition at different VID delta, however, energy can be further saved if the right number of phases are activated. The test result is obtained by using Intel VRTT tool by varying the VID delta and repetitive rate. We statically configure the phase number (3/4/5/6) and run the test. There are totally 100 data points (4×5×5) that need to be collected eventually. The system is fully isolated and only the VR under test is locally powered up. Input RMS current

is obtained using data acquisition unit to compare the different power consumption. Repetitive DVID frequency is color coded and ranges from 1 kHz to 5 kHz, as shown in Figure 5. 19. Active phase count is labeled in each test case. From the experiment results, case 1 and case 2 we can program 6 phases to run, even 4 phases may save certain power, but the stress (especially, HS V$_{DS}$) on the device is much higher. From the power saving standpoint, case 3 and case 4 can be using 5 phases, and 4 phases, respectively. Case 5 represents lowest VID delta in this experiment, 3 phases will be sufficient and 300 mW can be saved compared to firing 6 phases.
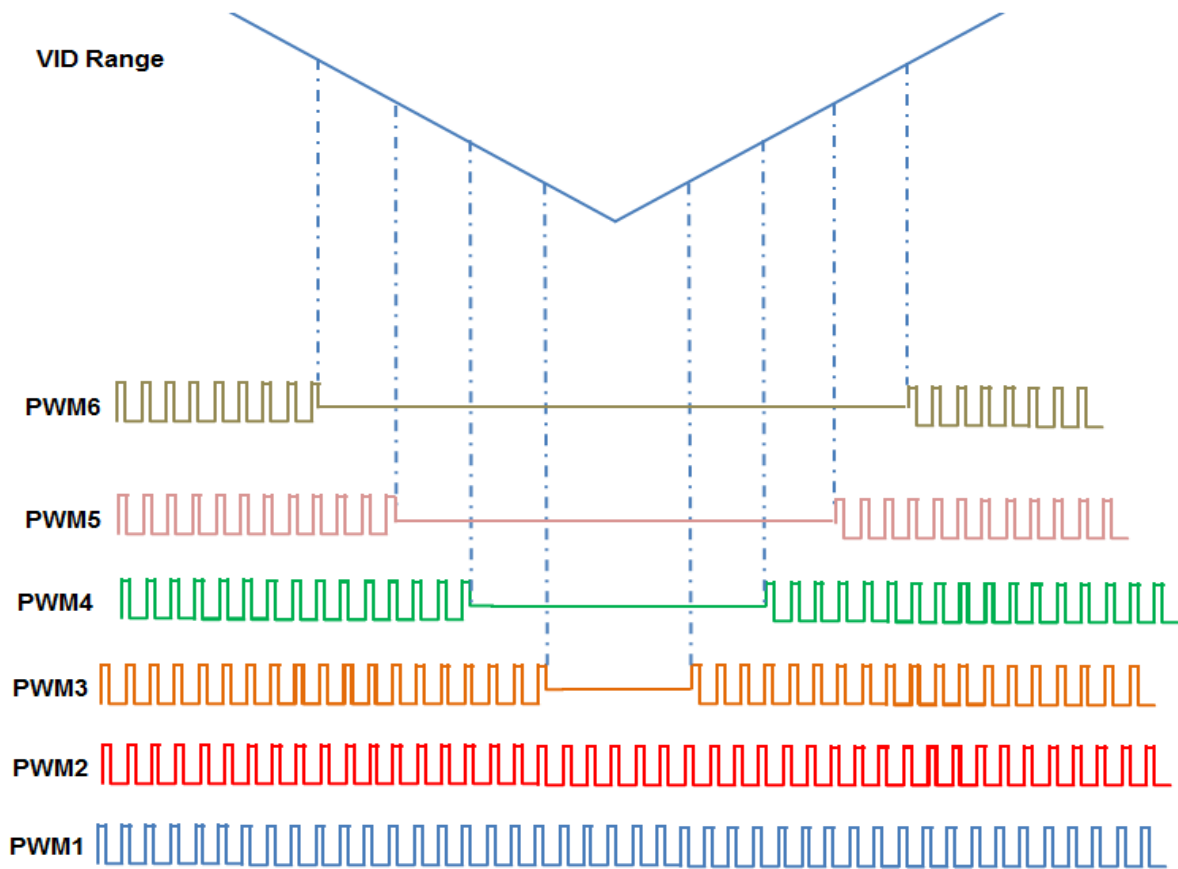
Figure 5. 19. Phase number control based on VID delta.

When the output voltage transits from one VID to another VID, number of active phases should be added or shedded to minimize the power loss based on VID delta, as shown in Figure 5. 19.

CHAPTER SIX: CONCLUSIONS AND FUTURE WORK

In this dissertation, comprehensive investigations and optimizations on multiphase synchronous buck converter are presented. The optimization is focused on the real system running condition and corner case scenarios.

6.1 Major Contributions

The major contributions of this work are listed in below.

We investigate the power conversion loss in all CPU VR operating conditions, carry out the efficiency optimization by parametric variation and propose load adaptive control scheme. Driver interface is thoroughly investigated for operation and efficiency purposes. Switching waveforms are understood better with incorporating all the parasitics.

We propose the load transient enhancement schemes to minimize the output voltage excursion during low frequency load transient. During load engage, the pulse should be pulled in fast enough to compensate the voltage deviation. During load release, adaptive body braking schemes are proposed to adaptively suppress the voltage overshoot. A true system operation scenario that can create power MOSFETs shoot-through is captured and new dead-time management scheme is proposed to maintain the high efficiency and ensure the system reliability.

In the presence of large, high frequency load current change, the closed loop response is optimized to minimize the peaking of the output impedance. The small signal closed loop system output impedance is derived and the PID values are optimized in the high frequency range to attenuate the high frequency system noise. Beat frequency is studied and mitigated by the

proposed load frequency detection scheme by turning OFF the nonlinear loop and introducing current protection in the control loop.

We present the detailed design considerations for multiphase converter running in dynamic voltage scaling (DVS). Optimized driver dead-time in boost mode operation are illustrated and DVID downward transition can be achieved with negative current shared among phases. The excessive stress on the control MOSFET which increases the reliability concern is captured in boost mode operation. Feasible solutions are also proposed and verified by both simulation and experiment results. CdV/dt compensation for removing the AVP effect and novel nonlinear control scheme for smooth transition are proposed for dealing with fast voltage positioning. Optimum phase number control during dynamic voltage transition is also proposed and triggered by voltage identification (VID) delta to further reduce the dynamic loss.

6.2 Future Works

System integration is the trend of power related design. Discrete power MOSFETs and drivers can be designed and manufactured into the same package to minimize the footprint and ringing. Driver dead-time can be further optimized since the MOSFET parameters and parasitics are known in a defined range.

Efficiency optimization can be further carried out by using inductor with ultra-low DCR. Since the SNR is too low that controller cannot handle. The current sense architecture, therefore, needs to be redesigned. MOSFET current sense, with built-in current mirror, can be adopted and characterized to solve the above issue.

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