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LOW POWER CMOS CIRCUIT DESIGN AND RELIABILITY ANALYSIS FOR WIRELESS MEMS SENSORS

by

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A dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in the Department of Electrical and Computer Engineering in the College of Engineering and Computer Science at the University of Central Florida Orlando, Florida

Fall Term 2004

Major Professor: Jiann S. Yuan

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ABSTRACT

A sensor node 'AccuMicroMotion' is proposed that has the ability to detect motion in 6 degrees of freedom for the application of physiological activity monitoring. It is expected to be light weight, low power, small and cheap. The sensor node may collect and transmit 3 axes of acceleration and 3 axes of angular rotation signals from MEMS transducers wirelessly to a nearby base station while attached to or implanted in human body. This dissertation proposes a wireless electronic system-on-a-single-chip to implement the sensor in a traditional CMOS process. The system is low power and may operate 50 hours from a single coin cell battery. A CMOS readout circuit, an analog to digital converter and a wireless transmitter is designed to implement the proposed system.

In the architecture of the 'AccuMicroMotion' system, the readout circuit uses chopper stabilization technique and can resolve DC to 1 KHz and 200 nV signals from MEMS transducers. The base band signal is digitized using a 10-bit successive approximation register analog to digital converter. Digitized outputs from up to nine transducers can be combined in a parallel to serial converter for transmission by a 900 MHz RF transmitter that operates in amplitude shift keying modulation technique. The transmitter delivers a 2.2 mW power to a 50 Ω antenna. The system consumes an average current of 4.8 mA from a 3V supply when 6 sensors are in operation and provides an overall 60 dB dynamic range.

Furthermore, in this dissertation, a methodology is developed that applies accelerated electrical stress on MOS devices to extract BSIM3 models and RF parameters through measurements to perform comprehensive study, analysis and modeling of several analog and RF circuits under hot carrier and breakdown degradation.

To my father who always inspires me to be someone different And my mother who always loves me to be someone caring

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LIST OF ACRONYMS/ABBREVIATIONS

A/D	Analog to Digital (Converter)
ADC	Analog to Digital Converter
AM	Amplitude Modulation
ASK	Amplitude Shift Keying
BD	Breakdown
BPF	Band Pass Filter
CDS	Correlated Double Sampling
CMFB	Common Mode Feedback
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
СР	Charge Pump
D/A	Digital to Analog (Converter)
DAC	Digital to Analog Converter
DC	Direct Current
DFF	D-type Flip Flop
DFT	Discrete Fourier Transform
DR	Dynamic Range
DRIE	Deep Reactive Ion Etching
FDMA	Frequency Division Multiple Access
HBD	Hard Breakdown
НС	Hot Carrier

HPF	High Pass Filter
ISM	Industrial, Scientific and Medical (Frequency Band)
LCO	LC oscillator
LO	Local Oscillator
LPF	Low Pass Filter
LSB	Least Significant Bit
MEMS	Micro Electro-mechanical Systems
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
NMOSFET	N-type Metal Oxide Semiconductor Field Effect Transistor
OOK	On-Off-Keying
PA	Power Amplifier
PCA	Programmable Capacitor Array
PD	Phase Detector
PFD	Phase Frequency Detector
PLL	Phase Lock Loop
PMOSFET	P-type Metal Oxide Semiconductor Field Effect Transistor
PSRR	Power Supply Rejection Ratio
PSS	Periodic Steady State
РТАТ	Proportional to Absolute Temperature
RF	Radio Frequency
SAR	Successive Approximation Register
SBD	Soft Breakdown

SCL	Source Coupled Logic
SEM	Scanning Electron Microscopy
SNR	Signal to Noise Ratio
VCO	Voltage Controlled Oscillator
XF	Transfer Function

CHAPTER 1: INTRODUCTION

1.1 Motivation

In the last half a century the world is blessed by thousands of electronic products. Electrical engineers relentlessly pushed the design limits to develop the products. These innovations and developments prompted an unmatched peak in the human civilization. Distributed wireless networks with smart, low cost, low power and tiny sensors all around us will lead the human civilization to a new era. The sensors will collect vast amount of data to help us run factories, maintain buildings, treat patients, watch for earthquakes, monitor wildlife, forecast weather, and fight terrorism. Within a decade sensor networks are expected to show their presence everywhere: homes, offices, factories, automobiles, shopping centers, super-markets, farms, forests, rivers, lakes and in space. While sensors are already used for many applications, however, most sensors being used today are large and expensive. Micro electro mechanical system (MEMS) and nanotechnology have the potential to yield tiny, low cost, low power sensors.

The integrated circuits to implement the interface and the wireless transmitter for sensors are usually power hungry. In some applications, sensor nodes may require to operate several years before a battery replacement is possible. These sensors may operate in a burst mode, where they operate and go to a sleep mode periodically. However, a sensor may need to operate continuously and real time. The sensor node may operate from a coin cell battery or a tiny solar cell or even it may acquire microwave energy from a remote location. It is challenging to design electronic circuits that consume very low power and provide a good resolution with an acceptable form factor. Low power consumption may be achieved at the cost of low resolution.

Complementary metal oxide semiconductor (CMOS) has emerged as the dominant technology for its low cost, low power, and scalability. Therefore, electronic circuits for sensor nodes in a mainstream CMOS technology are highly desirable. The CMOS processes provide the opportunity to design MEMS transducers, interface, signal conditioning, and wireless circuits on a single chip.

On-chip signal processing is very critical to design miniature sensor nodes. This dissertation presents a system with multiple MEMS transducers, interface circuits, analog to digital converters and a wireless transmitter integrated together in a single chip to implement a miniature sensor node for continuous real time data collection. The sensor node, as named 'AccuMicroMotion', has the ability to detect motion in 6 degrees of freedom for an application in physiological activity monitoring. The sensor node may collect and transmit 3 axes of acceleration and 3 axes of angular rotation signals from MEMS transducers wirelessly to a nearby base station while attached to or implanted in human body. Such a system has to be light weight, ultra low power, and small for an un-tethered monitoring of a subject. While designing the MEMS transducers for the proposed sensor is not the focus of this work, the design issues and analysis of the CMOS circuits to be integrated on a single chip using a traditional CMOS process are presented in this dissertation in detail. The integrated node is expected to be light weight and reliable, consumes very low power, and has reasonably good resolution.

Some probable applications for the 'AccuMicroMotion' sensor may include but not limited to medical diagnosis, physical therapy, sports, and fitness. The sensor node can be used in activity monitoring in biomedical applications that already plays a very important role in diagnosing many diseases and finding answers for many physiological questions. The proposed sensor may also help physical therapists to find a way to eliminate or reduce someone's disability. Coaches may use this devices to be able to know how the athletes are performing and improving. Exercise and fitness equipment manufacturers may want to know how their products are affecting human bodies. Multiple of these devices can form a network to provide a larger picture on the physiological movements. To the best of our knowledge this is the first effort [1] to provide a solution to detect vibratory signals in 6-degrees of freedom for the physiological activity monitoring application.

1.2 Related Works

Capacitance sensing is a widely used method to sense the signal from MEMS vibration microstructures [2-14]. It is low power, low noise, and compatible to fabricate in standard CMOS. This is the most commercially used technique. Other methods for motion sensing include piezo-resistive [15], piezo-electric, and tunneling current sensing [16].

The process in which the MEMS structures are realized has significant effect on the type of interface circuit needs to be designed. Although the most successful commercial devices by Analog Devices [9] use dedicated BiCMOS process with poly-silicon thin film microstructures, the MEMS processes based on standard CMOS offer many advantages. CMOS provides scalability, multi vendor accessibility, short design cycles and cheaper MEMS devices. Post-CMOS processing is an option widely used to release microstructures. While surface micromachining [17] provides low cost and easy integration, bulk micromachining [18] has some distinct advantages. Bulk micromachining offers larger mass that results in lower thermalmechanical Brownian noise for the microstructures. It also provides larger sensing capacitances that lead to better sensitivity.

To implement the capacitive sensing interface circuits, two major trends are observed: continuous time sensing [2-8] and switched capacitor discrete time sensing [9-14]. Being the dominant approach in design arena, the switched capacitor interface circuit offers few distinct advantages. It provides virtual ground and robust dc biasing at the sensing nodes so that the sensed signal is insensitive to parasitic capacitances and undesirable charging. Also, it offers a wide range of techniques to suppress offset and low-frequency noises, including correlated double sampling (CDS) and programmable capacitor array (PCA) [10, 14]. On the other hand, it suffers from inferior noise performance due to two reasons. First, the on-resistances of the MOS switches at the sensing node give rise to an additional thermal noise. Second, it is a sampled-data system and the noise folding causes the output noise power to multiply. Due to its superior noise performance continuous time sensing is being used recently.

Very few wireless vibration sensors are reported so far. Microstrain developed a wireless accelerometer [19] that uses analog devices' ADXL2XXJE accelerometer with few other chips on a board. This accelerometer uses 916 MHz for RF transceiver. It has a size of 25 mm by 75 mm by 7.25 mm excluding batteries, an RF range of 30 meter line of sight and power consumption of 72 mW when transmitter is active. A wireless accelerometer is reported in [20], where MEMS and surface acoustic devices are integrated. It does not require any on board power supply at sensor location. In [21], a multi-functional input devices system (MIDS) is reported where Analog Devices' accelerometers are used to sense the multi axis motion in the finger rings, and a MIDS wrist watch communicates with the rings and transmits data wirelessly to

interface with a PC. ADXL MEMS accelerometers are used to design a wireless motion sensing system for the sports science applications in [22].

Existing solutions for motion sensor systems require multiple chips that make them bulky and power inefficient. However some applications such as activity monitoring and implantable devices require that the wireless sensors be light weight and ultra low power. Therefore, low power single system-on-a-wireless-chip is highly desirable. This work propose a system which is a single chip solution and suitable for such applications.

1.3 System Overview

A block diagram of the proposed 'AccuMicroMotion' sensor node is shown in Figure 1.1. Main building blocks of the system include four transducers (an XYZ accelerometer and three gyroscopes), CMOS interface circuits, analog to digital converters, parallel to serial converter, and a radio frequency (RF) transmitter. The XYZ accelerometer requires three sensing circuits for three axis acceleration detection.

System level selections include the choice of interface circuit, the type of baseband signal processing, and the modulation scheme for wireless transmission. The requirements for low power and low cost manifest the use of CMOS technology. There are two choices for interface circuits: switch capacitor or continuous time. Continuous time circuits are used in this work for their low noise performance. The interface circuits sense and amplify very low frequency weak signals from MEMS transducers using capacitive sensing principle. Human body motions have the characteristics of relatively low intensity and low frequency acceleration or angular movement. Therefore, direct amplification and signal processing provides very low signal to

noise ratio because of the high 1/f or flicker noise of the input MOS transistors. To avoid the flicker noise chopper stabilization technique is used for the interface circuit, where the signal is first up-converted to a higher frequency using a carrier and then down-converted to original frequency band after amplification and signal processing. Higher the modulation frequency lower the overall noise level, however it increases the power consumption. Baseband readout signal is first digitized before wireless transmission, since an all analog signal path will not provide sufficient dynamic range. Although a commercial product for the physiological activity monitoring has to be interactive, and an RF receiver will be needed, to keep the scope of this research limited, only a wireless transmitter is considered.



Figure 1.1: Proposed single chip wireless 'AccuMicroMotion' sensor node

The signals are digitized using successive approximation register (SAR) analog to digital converters (ADC) and up-converted to RF signal for transmission using Amplitude shift keying (ASK) or on-off-keying (OOK) modulation scheme. Frequency division multiple access (FDMA) scheme can be used for multiple sensor nodes in a network. The designed phase lock loop (PLL) circuit can provide carriers in the instrumentation scientific and medical (ISM) frequency band of 902-928 MHz with 1 MHz channel spacing. The power amplifier (PA), which also works as a RF modulator, delivers 2.2 mW power to a 50 Ω antenna. The required radiated power from the antenna is much lower for a short distance of 20 meters. However, provision for extra power is kept so that very low efficiency on-chip or on board patch antenna can be used. Usually these antennas have much lower resistance than a standard 50 Ω antenna. The proposed electronic system has a dynamic range (DR) of 60 dB and it consumes 14 mW power to operate more than 50 hours from a 230 mAh single coin cell battery.

The OOK or ASK modulation scheme is selected for its low power operation and ease of implementation. In the ASK modulation scheme, the transmitter can be designed such that it only transmits when the digital information bit is logic 'one' and nothing is transmitted for a logic 'zero'. Therefore, the most power hungry component in a transmitter, the PA, can be turned off when digital bit is 'zero'. If any of the transducers do not produce any signal, then PA can be turned off to save power. In the proposed system, up to nine transducers can use the single transmitter. If an application does not require that many sensing readout channels, for example the proposed 'AccuMicroMotion' sensor node for physiological activity monitoring requires six readout interfaces, the transmitter power can be saved proportionately.

Since power consumption is a major issue for a sensor node, it is a very attractive practice to keep the sensor in a periodic on off (to sleep mode) schedule [23]. Transducers within

a sensor node can also be put under time multiplexing using a selection switch before the interface circuit [23]. However, for the type of application this system is designed for it is required that the sensor provides continuous data. As a result, multiple CMOS interface circuits and ADCs are required, and the transmitter should be able to transmit data from all transducers (with six channels) simultaneously.

Despite several efforts [5, 10] sensor DC offset remains challenging. In [10], a solution is proposed that trims the sensor DC offset in digital domain after A/D conversion. However, often the sensor offset is so large that it may saturate the interface circuit, where digital trimming does not help. In [4], an electronic calibration technique is proposed to cancel this offset. But, this scheme requires off-chip signal with precise frequency, phase and amplitude. It is hard to get precise matching in frequency unless it comes from the same source. An on-chip solution is very desirable to calibrate or trim the sensor offset before it saturates the electronic readout circuits. This work proposes a sensor offset cancellation technique using off chip resistance tuning. Furthermore, DC offsets created by sensing amplifiers also need to be corrected.

A study to characterize the human activity during rowing has been reported in [24]. This report reveals that the range of acceleration that the rowers produced is ± 1 g. Therefore, a range of ± 2 g for the proposed wireless sensor will suffice the targeted application of physiological activity monitoring. Although the CMOS interface circuits for the system is optimized for an accelerometer, since the gyroscope devise the signals from acceleration using Coriolis force analysis, the same circuits can be used for gyroscope interface as well.

An off the shelf RF receiver attached to a laptop or PC can serve as the base station. For the 'AccuMicroMotion' sensor, the base station can be located nearby to the subject in the same room. The overall specifications for the accelerometer can be summarized in Table 1.1.

Table 1.1. Overall Specifications of the Accumicionionion whereas Sensor	
Specifications	Value/Comments
Technology	TSMC 0.35 μm
Full Scale Acceleration Range	±2 g
Resolution	100 µg
Power consumption	15 mW
Wireless distance	20 meter line of sight
Dynamic range	60 dB
Frequency band for transmission	900 MHz ISM band (902-928 MHz)
Power supply	Single 3 V coin-cell battery
Transmitting antenna	On chip or on board patch antenna
Integration	Fully integrated except few off-chip passive components.

Table 1.1: Overall Specifications of the 'AccuMicroMotion' Wireless Sensor

1.4 Organization of the Dissertation

Chapter 2 introduces inertial sensors and their commercial applications. Some important accelerometer design issues such as spring design, curl matching, Brownian noise, sensor offset, electrostatic spring softening etc. are briefly introduced. Also, principles of acceleration and capacitive sensing and how they relate to interface circuit design are presented.

Chapter 3 identifies the sources of electronic noises and analyzes the overall noise of the readout circuit referred to the input acceleration. A noise optimization technique by capacitance matching is then evaluated. Chopper stabilized continuous time circuit architecture is discussed. This chapter introduces the details of the proposed readout circuit for the sensor. Individual circuit blocks are discussed in detail and Spectre simulation results are given. ADC design details are also presented in this chapter.

In chapter 4, wireless transmitter architecture for the 'AccuMicroMotion' is introduced. Design details and simulation results are provided for the PLL and the ASK transmitter. Chapter 5 discusses the reliability issues especially hot carrier and gate oxide breakdown. The tests results from MOS device measurements are presented. The models for design and analysis of RF and analog circuits such as LC oscillator, passive mixer, and interface circuit are proposed. Degradation due to HC and BD discussed and analyzed.

Finally, summary and future research directions are given in Chapter 6.

CHAPTER 2: CMOS MEMS SENSORS

MEMS sensors find a wide variety of commercial and military applications in recent years. It is expected that this industry will grow exponentially in the foreseeable future. Ranging from inertial, pressure, temperature, particle sensing and detection, MEMS sensors may be used to detect and identify biological agents as well. These tiny sensors are expected to change every perspective of human life significantly.

Inertial sensors can be divided into two categories: acceleration and angular rate sensors. In recent years, micro-machined inertial sensors are produced in large quantity for commercial use. While accelerometers are the current leaders in commercially successful MEMS technology, other inertial devices such as rate gyroscopes are poised to have similar success. In addition to high-volume markets for automotive crash sensors, there are markets for high-resolution seismic sensing and high-g sensors.

Accelerometers are bought in millions each year by the automotive industry. They are used to activate safety system of the modern automobiles such as crash sensing for airbag control, vehicle dynamic control, rollover detection, and antitheft systems. Inertial sensors can also be used in numerous present and potential new applications such as physiological monitoring, automotive occupant safety, vibration monitoring, sports diagnostics, appliance balance, earthquake detection, game pads, inclinometer, pedometer etc.

MEMS pressure sensors made a revolution with millions of popular bubble jet printer being sold world wide. Pressure sensors may find many more applications such as tire pressure monitoring, blood pressure, barometer/altimeter, engine control, respiratory applications, process control, drug delivery for inhalers, industrial control, water level monitoring etc. Most inertial and many pressure sensors work on a principle of capacitive sensing, where a small capacitive change is sensed by an interface electronics.

2.1 Accelerometer

An acceleration sensor or simply accelerometer has a proof mass, which is suspended to a reference frame by a set of spring elements. Acceleration causes a displacement of the proof mass proportional to the acceleration. This displacement can be measured by a change in capacitance between the proof mass and some additional electrodes. For better sensitivity, the proof mass needs to be larger which can be achieved by implementing the accelerometer in bulk CMOS micromachining. For less demanding applications, surface micromachining is often adequate.



Figure 2.1: SEM of a DRIE z-axis accelerometer [6]; (a) full view, and (b) close-up

Figure 2.1 and 2.2 show two examples of CMOS MEMS accelerometers [4, 6]. First one is vertical axis and second one is a lateral axis accelerometer. The proof mass, spring and capacitive comb fingers are marked.

Interdigitated multi-layer parallel plate capacitors are used in CMOS MEMS devices for both capacitive sensing and electrostatic actuation. Common-centroid layout style compensates cross axis manufacturing gradients and help to achieve better cross-axis rejection.



Figure 2.2: SEM of a thin film CMOS MEMS accelerometer [4]

2.1.1 Three-axis Accelerometer

The topology of a 3-axis accelerometer reported in [6] is shown in Figure 2.3. The comb fingers for x-axis sensing form eight capacitors, i.e., four C_{i1} 's, and four C_{i2} 's, where i = 1, 2, 3,

4. Let, $C_i = C_{i1} + C_{i2}$. Because of the symmetry, the C_i 's are insensitive to y-axis acceleration to first order. C_1 and C_2 form a differential capacitive divider, and so do C_3 and C_4 . Thus, a full differential capacitive bridge is obtained using the four C_i 's. As there is silicon underneath the spring beams, the springs are much stiffer (about two orders of magnitude) in the z-direction than in the x- or y-direction, which significantly reduces the z-axis cross-sensitivity. The same rationale applies to the y-axis acceleration sensing.



Figure 2.3: Topology of a 3-axis accelerometer [6]

The z-axis acceleration sensing is obtained by embedding a z-axis accelerometer in the center of the whole structure. The suspension of the z-axis accelerometer is flexible in the z-direction. Again, the cross-axis acceleration contributions are rejected by the differential capacitive topology. It should be noted that the differential capacitors in the z-axis accelerometer are stacked vertically and separated into groups.

2.2 Gyroscope

Most micromechanical gyroscopes are vibratory gyroscopes. A gyroscope can be modeled by a two-dimensional vibratory system with two orthogonal vibration modes as shown in Figure 2.4. If the proof mass is driven in the x-direction with a driving frequency of ω_d , a Coriolis force appears in the y direction that can be sensed by a y-axis accelerometer. An x-axis drive and y-axis sensing measure the angular rate Ω in the z-axis as indicated in Figure 2.4.

A z-axis gyroscope has an x-axis comb drive to excite the vibration, and a y-axis accelerometer to sense the induced Coriolis acceleration. The only difference in the topology of the lateral axis gyroscope is that the embedded accelerometer in the lateral-axis gyroscope senses the z-axis instead of y-axis acceleration. Therefore the sense mode must have a z-axis compliant spring. A lateral axis gyroscope [6] is shown in Figure 2.5. The structure is a two-fold, orthogonal spring-mass system where the inner frame (together with the proof mass) is driven to vibrate in the z-direction by the comb drive while the induced Coriolis acceleration is sensed by the accelerometer. Thus, the rotation sense axis of this device is along the x-axis.



Figure 2.4: Simplified model for vibratory gyroscope



Figure 2.5: SEM of a lateral axis gyroscope [7]

2.3 Pressure Sensor

The pressure sensors are based on the deflecting micro-machined thin silicon diaphragm anchored to the glass substrate, forming a variable capacitor with the applied pressure as shown in Figure 2.6. Capacitive pressure sensors [9] are more sensitive, low power, easy to integrate and less temperature dependent than piezoresistive sensors.

Another sensor that works in principles of capacitive sensing is humidity sensor. Miniaturized humidity sensors play an important role in a wide range of humidity measurement applications. Capacitive humidity sensors are the most preferred type of humidity sensors, satisfying the requirements of high sensitivity, short response time, small hysteresis, low cost, and low power consumption. Polyimide is the most frequently used humidity sensitive material because of its varying dielectric constant against relative humidity, which is almost linear. The CMOS circuits for vibration sensing can be easily used with humidity sensor as well.



Figure 2.6: Schematic view of a basic capacitive pressure transducer

2.4 Design Issues of an Accelerometer

A CMOS MEMS accelerometer micromechanical system can be modeled by a proof mass, spring and damping system all realized by micromechanical structures. A lumped model for such an accelerometer is shown in Figure 2.7.



Figure 2.7: Mechanical lumped parameter model of an accelerometer

When the substrate of an accelerometer chip experiences an external acceleration, the proof mass experiences a force equal to the external force that causes the acceleration. This force causes an immediate displacement of the proof mass. A portion of the force creates acceleration to the proof mass; other portion is absorbed by the viscous damping force and spring elastic force. As a result the differential equation in the sensing axis that governs the force-displacement relation is given by:

$$F_{in}(t) = ma_{in}(t) = m \frac{d^2 x(t)}{dt^2} + b \frac{dx(t)}{dt} + kx(t)$$
(2.1)

$$\Rightarrow \frac{d^2 x(t)}{dt^2} + \frac{\omega_n}{Q} \frac{dx(t)}{dt} + \omega_n^2 x(t) = a_{in}(t), \qquad (2.2)$$

where, ω_n (natural frequency) $=\sqrt{\frac{k}{m}}$, and Q (mechanical quality factor) $=\frac{\sqrt{km}}{b}$. Now in *s* domain,

 $s^{2}X(s) + \frac{\omega_{n}}{Q}sX(s) + \omega_{n}^{2}X(s) = A_{in}(s)$

$$\Rightarrow H(s) = \frac{X(s)}{A_{in}(s)} = \frac{1}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2}.$$
(2.4)

(2.3)

A device is underdamped if Q > 0.5, critically damped when Q = 0.5 and overdamped with Q < 0.5. At frequencies much smaller than resonance frequency,

$$H(s) = \frac{X(s)}{A_{in}(s)} = \frac{1}{\omega_n^2}.$$
 (2.5)

Consequently, the sensitivity of the accelerometer is given by:
$$\frac{x}{a_{in}} = \frac{1}{\omega_n^2} = \frac{m}{k}.$$
(2.6)

While, underdamped devices show ringing behavior and have slow settling under shock, overdamped structures result high thermal-mechanical noise, known as Brownian noise. Most accelerometers sense acceleration at a frequency much smaller than natural frequency. Human motion is limited to few tens of Hz in the proposed wireless accelerometer.

Brownian noise: There are two sources of mechanical damping: the structural damping and the viscous damping. The CMOS MEMS structures are made of the metal, oxide and silicon substrate layers, all of them are high Q materials with low structural damping. Proof mass and other microstructures experience viscous damping by flow of gas that surrounds the structures. The dominant damping mechanism in lateral axis accelerometer is squeeze-film damping between the parallel plate capacitor fingers. Such air damping creates the Brownian noise whose power spectral density is given by:

$$\overline{a_n^2(f)} = \frac{4k_b T b}{9.8^2 m^2} = \frac{4k_b T k^{\frac{1}{2}}}{9.8^2 O m^{\frac{3}{2}}},$$
(2.7)

where, k_b is the Boltzman constant, k is the spring constant, T is the temperature in degree Kelvin, m is the mass and Q is the quality of the sensor structure, and b is the damping coefficient which is given by:

$$b \propto \mu_{eff} h \left(\frac{l}{d}\right)^3,$$
 (2.8)

where, l and h are the length and height of the fingers, d is the gap between the fingers, and μ_{eff} is the effective viscosity of the gas and depends on the pressure. The viscous damping can be reduced by decreasing the air pressure. Therefore, the Brownian noise can be reduced by packaging the device in vacuum.

Spring design: The proof mass is floated to the anchor of the structure by serpentine springs. The spring can be designed to have sensitivity in lateral or vertical direction by carefully choosing the dimensions of the spring. If a spring dimensions are length l, width w and height h then the spring constant in x-direction is given by [4]:

$$k_x = \frac{1}{N} Eh\left(\frac{w}{l}\right)^3,\tag{2.9}$$

where, N is number of turns and E is the Young's modulus of elasticity. The spring constant in z-direction is given by:

$$k_z = \frac{1}{N} E w \left(\frac{h}{l}\right)^3.$$
(2.10)

Therefore, lateral axis sensitivity can be ensured with narrower and higher beams.

Electrostatic Actuation: Similar capacitive comb fingers usually provide the electrostatic actuation which is necessary to cancel the sensor offset and to realize force-balanced feedback. While, an external acceleration generates corresponding electrical signal through sense comb fingers, an external electrical voltage creates a force through actuation drive fingers to generate a mechanical motion and acceleration to floating proof mass structure. To find the expression for the electrostatic force in the drive combs let us assume that a voltage of V is applied and a

displacement of dx and a capacitive change of dC result. As a result the incremental energy is given by:

$$F_{x}dx = \frac{1}{2}dC(x)V^{2}.$$
 (2.11)

Thus, the force in the comb drive is given by:

$$F_{x} = \frac{1}{2} \frac{dC(x)}{dx} V^{2} .$$
 (2.12)

Structural curling: The radius of the curvature of a CMOS MEMS structure can be as small as few millimeters. The difference in curling of stator and rotor fingers causes mismatch between them, and results in loss of capacitance. A compensation technique to cancel the structural curling is proposed in [6]. Both the suspension springs and the stator fingers are anchored to a rigid curl matching frame instead of the substrate. The springs, the proof-mass, the rotor and the stator finger are made to have same composition of structural layers. As a result, by using curl matching frame, the stator and rotor fingers are expected to curl in similar fashion therefore, the mismatch is minimized.

Sensor offset: Lateral manufacturing mismatch creates an unbalance in the sensing capacitances in the capacitance bridge. As a result, even when there is no acceleration applied to the accelerometer, this capacitance offset appears as an electrical signal at the sensing nodes. It appears as constant (DC) acceleration. Modulated by the high frequency modulation signal this signal can not be eliminated by ac coupling or filtering. For our specific application the

acceleration signal is either DC or very low frequency, as a result, electronically the sensor offset can only be removed by trimming or calibration.

The sensor offset cancellation can be done in mechanical domain by using electrostatic actuators to pull the proof-mass back to the center position. However, in case the sensor offset is very large, large actuator area and high voltage are needed. Thus, it is therefore very desirable to have electronic cancellation of sensor offset.

Electrostatic spring softening: Modulation voltage across the comb fingers generates an electrostatic force on the proof mass. The electrostatic spring force in the sensing axis has a positive sign, hence, having a destabilizing effect on the proofmass. As the proofmass moves in one direction, this force tends to push the proofmass further into that direction, thus, acting as a negative spring. This effect is called electrostatic spring softening. The total spring constant must remain positive in order for the device to be stable. The largest modulation signal amplitude allowable is found to be [4]:

$$V_{m,\max} = \sqrt{\frac{kx_0^2}{2C_{s0}}} .$$
 (2.13)

In reality, when the capacitive divider is not perfectly balanced, the electrostatic spring softening effect increases with the position offset. Therefore, design headroom is needed for adequate stability margin.

2.5 Principles of Capacitive Sensing

CMOS MEMS accelerometers are designed such that hey have two sets of capacitive comb fingers. Rotor fingers are mechanically attached to the proof mass and hence float with it. On the other hand, stator fingers are rigidly attached to an anchor. While an external acceleration causes the proof mass to move along with rotor fingers, as sown in Figure 2.8, the gaps between the rotor and stator fingers change, creating a change in inter finger capacitances. As in Figure 2.3, the capacitance C_{s1} increases as the gap decreases and C_{s2} decreases as the gap increases, and these changes are proportional to the acceleration. The principal design objective of the CMOS accelerometer is to convert the mechanical displacements and hence capacitive change into electrical signal efficiently. To perform this objective an electrical modulation signal (v_m) is applied in the stator fingers as shown in the Figure 2.8 that creates an electrical sensing signal v_s . Again, v_s is proportional to the external acceleration.



Figure 2.8: Principle of accelerometer

The capacitive sensing principles can be represented in term of electrical components and signals as in Figure 2.5, where C_p represents the total parasitic capacitance present in the sensing node. When the sensor is in its rest (center) position and if the gap between fingers is x_0 then the capacitance between the stator and the rotor is given by:

$$C_{s0} = \frac{\varepsilon A}{x_0} \implies \varepsilon A = x_0 C_{s0} .$$
(2.14)



Figure 2.9: Capacitive sensing by capacitance divider

With a displacement of x, the sensor capacitances become:

$$C_{s1} = \frac{\varepsilon A}{x_0 - x} = \frac{x_0 C_{s0}}{x_0 - x}$$
, and $C_{s2} = \frac{x_0 C_{s0}}{x_0 + x}$ (2.15)

Applying KCL in the sensing node,

$$sC_{s1}(V_m - V_s) = sC_p V_s + sC_{s2}(V_s + V_m)$$
(2.16)

$$\Rightarrow V_{s} (C_{s1} + C_{s2} + C_{p}) = V_{m} (C_{s1} - C_{s2})$$
(2.17)

$$\Rightarrow V_{s} = V_{m} \cdot \frac{\frac{C_{s}x_{0}}{x_{0} - x} - \frac{C_{s}x_{0}}{x_{0} + x}}{\frac{C_{s}x_{0}}{x_{0} - x} + \frac{C_{s}x_{0}}{x_{0} + x} + C_{p}} = V_{m} \cdot \frac{2xx_{0}C_{s}}{(2C_{s} + C_{p})x_{0}^{2} - C_{p}x^{2}} = V_{m} \cdot \frac{2C_{s}}{2C_{s} + C_{p}} \cdot \frac{\frac{x}{x_{0}}}{1 - \frac{C_{p}}{2C_{s} + C_{p}}} (2.18)$$

Expanding using Taylor's series:

$$V_{s} = V_{m} \cdot \frac{2C_{s}}{2C_{s} + C_{p}} \cdot \frac{x}{x_{0}} \left[1 + \frac{C_{p}}{2C_{s} + C_{p}} \left(\frac{x}{x_{0}} \right)^{2} + \left(\frac{C_{p}}{2C_{s} + C_{p}} \right)^{2} \left(\frac{x}{x_{0}} \right)^{4} + \dots \right]$$
(2.19)

Since *x* is very small compared to x_0 , neglecting the higher order of $\frac{x}{x_0}$:

$$V_s = \frac{2C_s}{2C_s + C_p} \cdot \frac{x}{x_0} \cdot V_m \,. \tag{2.20}$$

The sensor structures are usually designed to be fully differential which provides fully differential signals to the following readout circuits with very good common mode rejection ratio (CMRR) and eliminates the need for common mode feedback (CMFB) circuits at the front end. Figure 2.10 shows the electrical equivalent circuit.



Figure 2.10: Fully differential capacitive sensing

With a fully differential capacitive sensing,

$$V_{s} = V_{s}^{+} - V_{s}^{-} = \frac{4C_{s0}}{2C_{s0} + C_{p}} \cdot \frac{x}{x_{0}} \cdot V_{m}.$$
(2.21)

Using (2.4) for very low frequency acceleration,

$$V_{s} = \frac{4C_{s0}}{2C_{s0} + C_{p}} \cdot \frac{a_{in}}{\omega_{n}^{2}} \cdot \frac{1}{x_{0}} \cdot V_{m}.$$
(2.22)

As a result, the sensitivity is given by

$$\frac{V_s}{a_{in}} = \frac{4C_{s0}}{2C_{s0} + C_p} \cdot \frac{V_m}{x_0} \cdot \frac{1}{\omega_n^2},$$
(2.23)

where, $\omega_n = \sqrt{\frac{k}{m}}$

As it is evident from (2.23), the sensitivity of an accelerometer can be improved by better capacitive matching, using high amplitude modulation signal, decreasing the gap between the capacitive fingers, or decreasing the natural frequency of the mechanical structure. The amplitude of the modulation signal can not be increased arbitrarily due to sensor offset and electrostatic spring softening effect. The aspect ratio of the DRIE process limits the minimum gap between the fingers that can be allowed. The lower bound of the natural frequency is limited by the achievable lowest spring constant and highest possible effective mass of the structure, mechanical shock resistance, manufacturability and desired bandwidth.

CHAPTER 3: INTERFACE CIRCUIT

3.1 Sources of Electronic Noises

There are two kinds of noises in CMOS MEMS accelerometers or gyroscopes: thermal mechanical Brownian noise from the mechanical transducers and electronic noises from the readout circuits. The Brownian noise has been discussed briefly in the previous chapter. Figure 3.1 shows the sources of the electronic noises in the readout circuit.



Figure 3.1: Sources of electronic noises

Thermal noise: Thermal noise generated in the channel can be modeled by a current source connected between the drain and source terminal for a long-channel MOS transistor operating in saturation with a spectral density:

$$i_{n,thermal}^2 = 4\gamma kTg_m , \qquad (3.1)$$

where, for long channel devices, $\gamma = \frac{2}{3}$. Thus, input referred thermal noise is given by:

$$\overline{v_{n,thermal}^{2}} = \frac{i_{n,thermal}^{2}}{g_{m}^{2}} = \frac{8kT}{3g_{m}}.$$
(3.2)

Flicker noise: While the reason and an accurate model for flicker noise in MOS devices are still obscure, this noise is very large in CMOS technology especially in low frequencies. In literature [25-27] the models for this noise often do not agree with each other. Depending on the oxide interface state, flicker noise may assume considerably different values and may vary from one CMOS technology to other. From measurements it has been observed that the spectral density of this noise is inversely proportional to the frequency. However, the frequency up to which this noise is significant also widely varies from process to process. The flicker noise is often modeled as a current source from drain to source terminal with a spectral density:

$$\overline{i_{n,flic\,ker}^2} = \frac{K_f I_D}{C_{ox} L^2 f}.$$
(3.3)

Thus, input referred flicker noise is given by:

$$\overline{v_{n,flic\,ker}^{2}} = \frac{i_{n,flic\,ker}^{2}}{g_{m}^{2}} = \frac{K_{f}I_{D}}{C_{ox}L^{2}f \cdot 2\mu C_{ox}\frac{W}{L}I_{D}} = \frac{K_{f}}{2\mu C_{ox}^{2}WLf}.$$
(3.4)

Shot noise from input biasing devices: Leakage current through reverse biased PN junction at the input nodes cause the shot noise, which is given by:

$$\overline{i_{n,leak}^2} = 2qI_{leak} \,. \tag{3.5}$$

Input referred shot noise now can be expressed as:

$$\overline{v_{n,leak}^{2}} = \frac{i_{n,leak}^{2}}{(2\pi f C_{total})^{2}} = \frac{q I_{leak}}{2\pi^{2} C_{total} f^{2}}, \qquad (3.6)$$

where, C_{total} is the total capacitance at the sensing node.

Noise from modulating signal: The modulating signals are often generated using on-chip digital circuits. The signal waveforms generated from such digital circuits can be noisy, and may contribute to the overall noise floor at the sensing nodes. If the noise from the modulating signal is modeled as $\overline{v_{mod}^2}$, then noise contribution to sensing node is given by:

$$\overline{v_{\text{mod},input}^2} = \left(\frac{2C_s}{2C_s + C_p}\right)^2 \cdot \left(\frac{x}{x_0}\right)^2 \cdot \overline{v_{\text{mod}}^2} .$$
(3.7)

Other noise: The interface circuits include digital circuits as well. The mechanical vibration and switching of the digital circuits make the substrate of the chip very noisy. Despite layout techniques, a significant noise is very likely to be present at the substrate of the preamplifier. The substrate noise modulates the body effect of the amplifier that elevates the overall noise floor.

Again the digital circuits may produce a significant power and ground bounce that may appear in the amplifier as a noise. The amplifier needs to be designed with high power supply rejection ratio (PSRR).

Overall noise floor: In the frequencies up to 100 KHz - 1 MHz the flicker noises normally dominate. The shot noise is often in the order of pA and can be ignored. The overall input referred noise for the thermal and flicker noise is given by:

$$\overline{v_n^2} = \frac{8kT}{3g_m} + \frac{K_f}{2\mu C_{ox}^2 WLf}.$$
(3.8)

The overall noise floor in terms of acceleration can be obtained. Using (2.10) the input referred noise can be given by:

$$\overline{a_n^2(f)} = \frac{\left(2C_s + C_p\right)^2 x_0^2 \omega_n^4}{4C_s^2 V_m^2} \cdot \overline{v_n^2(f)}.$$
(3.9)

Using (3.8) we can write:

$$\overline{a_n^2(f)} = \frac{\left(2C_s + C_p\right)^2 x_0^2 \omega_n^4}{4C_s^2 V_m^2} \cdot \left[\frac{8kT}{3g_m} + \frac{K_f}{2\mu C_{ox}^2 WLf}\right].$$
(3.10)

Again, the parasitic capacitance at the input node can be given by:

$$C_{p} = C_{int} + C_{gs} + A_{l}C_{gd}, \qquad (3.11)$$

where, C_{int} is the parasitic capacitance associated with interconnection between the sensor and CMOS readout circuits, and the gate to drain capacitance is multiplied by the gain of the first stage of the preamplifier to include Miller's effect. Thus, the overall noise floor is given by:

$$\sqrt{\overline{a_n^2}} = \sqrt{\frac{\left(2C_s + C_{\text{int}} + C_{gs} + A_1C_{gd}\right)^2 x_0^2 \omega_n^4}{4C_s^2 V_m^2}} \cdot \left[\frac{8kT}{3\sqrt{2\mu C_{ox}} I_D \frac{W}{L}} + \frac{K_f}{2\mu C_{ox}^2 WLf}}\right] \quad (g/\sqrt{Hz})(3.12)$$

The above expression suggests that increasing the current through the input transistor reduces the noise floor. However, this improvement is costly, since a 2X reduction in noise requires a 16X increase in the drain current and consequently the power consumption.

3.2 Noise Optimization with Capacitance Matching

While a large transistor at the input stage of the preamplifier results in a large gain, it also increases the gate area and therefore increases the input capacitance. It can be seen in the expression for the overall noise floor of the accelerometer in (3.12) that the transistor width appears in the denominator and the gate capacitances appear in the numerator. As a result, while increasing the width decreases the noise, increased input capacitance reduces the sensitivity and consequently increases the noise floor. Thus, there is an optimum width of the input transistor for which the noise floor is minimum. Matching the input transistor to minimize the noise floor is known as capacitance matching and is given in detail in [4]. The optimum width for minimum noise floor can be found by:

$$\frac{\partial}{\partial W}\overline{a_n^2(f)} = 0.$$
(3.13)

Thus, the expression for optimum width is found to be:

$$W_{opt} = \eta \cdot \frac{2C_s + C_{int}}{\frac{2}{3}C_{ox}L + 2AC_{ox}L_{ov}},$$
(3.14)

where, $\frac{1}{3} < \eta < 1$ is a coefficient dependant on W_{opt} . The relation for the capacitance matching for

optimum width and the minimum noise floor is given by:

$$C_{gs} + AC_{gd} = \eta \left(2C_s + C_{int} \right) \tag{3.15}$$

3.3 Chopper Stabilized Continuous Time Circuit Architecture

Since an external acceleration or rotation produces a very small capacitive change that results a very small electrical signal at the sensing node, the electrical noise from the readout circuit is very critical for a better sensitivity of a transducer. Again, to keep the input capacitance small the input stage of the preamplifier is often designed with relatively smaller transistors. As a result, the flicker noise at low frequencies is very large. Since, for our application we are dealing with very low frequency acceleration, due to flicker noise, we will not get any meaningful signal at those frequencies unless something is done. Chopper stabilization technique [28] is very useful to avoid such a severe situation.

Chopper stabilization technique applies a high frequency modulation signal to transpose the sensor signal to a higher frequency where there is no or significantly low flicker noise. Then using the same frequency the signal is demodulated back to the base band. The chopper stabilization principle is illustrated in Figure 3.2. Usually this technique is applied along with band pass filtering. While, high pass filtering eliminates the DC offset and low frequency noises, low pass filtering eliminates the higher order odd harmonics resulted from the chopper modulation.

The frequency for chopper modulation should be chosen such that, it is at least more than twice of the signal bandwidth and the flicker noise at that frequency becomes insignificant or in the order of thermal noise. Higher the modulation frequency, better the noise performance will be. However, it is expensive to design an amplifier that has higher bandwidth for a given gain in terms of power consumption. Through simulation it has been found that with input capacitive matching and reasonable power the flicker noise becomes somewhat of same order at few MHz. A modulation frequency of 500 KHz is chosen for this design.



Figure 3.2: Chopper stabilized circuit architecture

Both an accelerometer and a gyroscope provide a capacitive change at its output. Therefore, the same readout circuit architecture can be used for an accelerometer and a gyroscope since both of them operate on the same capacitive sensing principle. In the designed systems, the front-end preamplifier, demodulator and analog to digital converter are followed by a wireless transmitter. The elements of the wireless transmitter will be discussed in the next chapter. This chapter presents the front end interface circuits.

3.4 Readout Circuit

The structure of the front end interface circuit for the 'AccuMicroMotion' is given in Figure 3.3. With a differential design, a mechanical transducer can be represented by a capacitance bridge with four capacitances. In case of an acceleration signal, there will be an unbalance between the capacitances; with an application of electrical voltage across the bridge, there will be a differential electrical signal at the output. To implement the chopper stabilization technique, the signal needs to be up-converted to a higher frequency in the mechanical domain.



Figure 3.3: The readout circuit architecture

A wideband amplifier performs the readout operation. The amplifier has two auxiliary input stages. One is used to feedback the amplifier output to implement the DC offset cancellation and another is used for sensor offset cancellation. A passive demodulator follows the preamplifier circuits. Clock signals to generate modulation and demodulation signals, and bias rest signal are generated using digital circuits. Since many components of the proposed 'AccuMicroMotion' system is mixed signal (both digital and analog circuits) in nature, a fully differential architecture is highly desirable. Differential architecture provides better CMRR and PSRR.

3.4.1 Preamplifier

The choice of the preamplifier architecture is a critical decision for number of reasons. Since the preamplifier has to be wideband, the power consumption could be large if a good choice is not made. A smaller number of legs in the architecture provide the least power consumption. Therefore, telescopic architecture may seem attractive. However, the preamplifier needs to have at least two stages to implement the DC offset and sensor offset cancellation. Also, the device size at first stage of the amplifier is limited by the capacitive matching issue to have the best sensitivity at the transducer inputs. Considering these issues, the folded cascode amplifier architecture is chosen. Folded cascode architecture has better gain bandwidth product for a given power. This amplifier also provides better CMRR and PSRR. One downside of this architecture is its relatively lower output voltage swing. However, with a modest DR specification of 60 dB, this is particularly not a problem. The overall gain of the interface circuit can be obtained by the gain of the preamplifier and an active low pass filter (LPF). The schematic of the preamplifier is shown in Figure 3.4.

The PMOS first stage of the preamplifier provides better noise performance since PMOS provides lower flicker noise than NMOS devices. The sizes of the input transistors are optimized for optimum input noise floor for best capacitance matching as discussed in the previous section using (3.13). Minimum device length is not used to reduce the flicker noise. Therefore, for a 1

 μ m long transistor the optimum width is 100 μ m. To calculate this channel width η is assumed to be 2/3, C_s to be 200 fF, C_{int} to be 100 fF, and C_{ox} is found by the following relation:

$$C_{ox} = \frac{\mathcal{E}_r \mathcal{E}_0}{t_{ox}} \tag{3.16}$$

where, ε_r is 3.9 for SiO2 and ε_0 is the permittivity in free space which is $8.854 \times 10^{-12} F/m$ and t_{ax} is around $7.3 \times 10^{-9} m$ for the TSMC 0.35 µm technology.

In the amplifier, two auxiliary input pairs are included for DC and sensor offset cancellation arrangements [5, 28]. The auxiliary amplifier for sensor offset cancellation steals current at the carrier frequency. On the other hand, the auxiliary amplifier for the DC offset cancellation is a slow amplifier that steals current at lower frequencies from the main amplifier. The first stage of the preamplifier carries a 10X bias current, where 1X is 100 μ A current, the second stage carries another 10X current in two limbs. However, the tail current biases of the main amplifier add up to 14X current. Remaining currents are supplied by the auxiliary amplifiers.

Common mode input and output levels are set at analog reference potential which is ¹/₂ rail to rail voltage (1.5 V for the 3 V supply). The output common mode level is set through a common mode feedback (CMFB) network as shown in Figure 3.5. CMFB network has two high impedance nodes in its loop. As a result, it requires compensation for stability. A capacitance along with a resistance in series is connected in parallel to the feedback control node. Both the resistor and the capacitor can be implemented on chip. The loop gain and phase after compensation is shown in Figure 3.6. It can be seen that the phase margin of this loop is 61°.



Figure 3.4: Preamplifier schematic

The preamplifier provides an overall gain of about 45 dB as shown in Figure 3.7. The bandwidth is chosen to be at the vicinity of signal bandwidth (500 KHz) such that higher harmonics from the square wave modulation signal are attenuated as much as possible. PSRR is better than 200 dB at the frequency of interest.



Figure 3.5: Common mode feedback circuit





Figure 3.6: Magnitude and phase of the loop gain for CMFB circuit



Figure 3.7: Frequency response of the preamplifier

As discussed in a previous section, higher the bias current, lower the noise is. However, this comes at the expense of high power consumption. A 200 μ A bias current produces input equivalent noise of 200 nV/\sqrt{Hz} at 500 KHz as in Figure 3.8. According to (2.23) with sensing capacitance C_s of 200 fF, transistor width of 100 μ m, interconnect capacitance C_{int} of 100 fF, V_m of 0.5 V, capacitance sensing finger gap x_0 of 1 μ m and mechanical resonance frequency ω_n of 5 KHz, this noise corresponds to an input noise floor of less than 100 $\mu g/\sqrt{Hz}$ which meets the specification.

Transient simulation results for the preamplifier are shown in Figure 3.9. A 500 KHz, 1 mV input signal amplitude modulated (AM) by 1 KHz with a modulation index of 1 is applied to the preamplifier. The plots 1 and 2 show the input and output signal respectively versus time. The plots 3 and 4 show the discrete Fourier transform (DFT) of the signals.



Figure 3.8: Input referred equivalent noise



Figure 3.9: Transient waveform at the preamplifier input and output and their DFT

3.4.2 DC Offset Cancellation

The DC offset cancellation is implemented by an auxiliary amplifier as shown in Figure 3.10. The basic idea of the DC offset cancellation architecture can be understood in the frequency domain. If a LPF is applied in the feedback path, a high pass filtering is achieved in the signal path. Low pass filtering in the feedback path is achieved through a simple differential amplifier with a capacitance connected at its outputs. The value of the capacitance determines the -3-dB frequency of the high pass filter (HPF) corner. A parametric analysis of XF simulation is performed to see the effect of different offset capacitances and the results are shown in Figure 3.11. A capacitance of 100 pF is chosen which provides a high pass filtering with a -3-dB frequency at around 200 KHz as it appears in Figure 3.7 and 3.11. Higher capacitance provides lower -3-dB frequency.

An intentional DC offset is created through transistor mismatch for simulation purpose. With no DC offset cancellation circuit in place, the DC offset is 55 mV (plots 1 & 3 of Figure 3.12). With the DC offset cancellation circuit included in the simulation, DC offset reduces to 1.2 mV (plots 2 & 4 of Figure 4.12). Thus, a 33 dB attenuation to the DC offset is achieved.

Since the DC offset cancellation is a feedback network, it is necessary to check the stability of the loop. It is found that without any compensation the phase margin of the loop gain is 83 as shown in Figure 3.14.



Figure 3.10: DC offset cancellation circuit



Figure 3.11: Parametric analysis: offset capacitance versus frequency response



Figure 3.12: DC offset cancellation. Notice gradual cancellation of the offset.



Figure 3.13: Loop gain magnitude and the phase of the DC offset cancellation loop

3.4.3 Sensor Offset Cancellation

Similar to DC offset cancellation, an auxiliary amplifier provides a correction signal necessary to cancel the sensor offset which appears as a 500 KHz carrier. Figure 3.14 shows a proposed circuit where a 500 KHz signal is applied to a resistive divider. One of the resistors, R2, is off chip and can be tuned to generate exact voltage necessary to cancel the offset. The polarity of the voltage applied to the resistive divider can be set by a switch network.

A signal of 5M Hz, 1mV sine wave with AM modulation frequency of 1 MHz and modulation index of 1 is applied at the input of the preamplifier for simulation purpose. Such input is applied to mimic the presence of a sensor offset (5MHz) along with acceleration signal (4 MHz and 6 MHz in this case). Without an offset cancellation the 5 MHz carrier is found to be 202 mV at output of the preamplifier. A 20 mV signal at the auxiliary arm reduces the sensor offset (which is 5 MHz carrier) to 9.77 mV. Thus, an attenuation of 26 dB is achieved in this simulation.



Figure 3.14: Sensor offset cancellation circuit



Figure 3.15: Sensor offset cancellation.

3.4.4 Biasing Circuits

High swing cascode current sources are used for the preamplifier to boost the output resistances of the tail current sources which improve the CMRR and PSRR. The biasing for such current mirrors is shown in Figure 3.16. To implement the high swing cascode mirrors, the transistor M1 and M2 are sized such that M1 is one fourth of M2. M3 is a cascode device and minimum length (actually little bit larger device is used for reliability concern) is used. The main advantage of high swing cascode current mirror structure is that the drain voltage of the transistor M5 can go as low as $V_{th} + 2V_{DSAT}$, whereas for regular cascode mirrors this voltage is $2V_{th} + 2V_{DSAT}$. The 20 µA proportional to absolute temperature (PTAT) reference current [25] can be generated on chip using a bandgap [25] reference circuit or generated externally.



Figure 3.16: Biasing circuit

An input bias reset circuit (Figure 3.3) is included in the preamplifier to set the input DC bias voltage. This topology is robust against charging and leakage activity at the input nodes. Digital clock generation circuits generate the necessary input bias reset signal. This reset signal turns on the bias MOS switches once in every 16 clock cycles of the modulation carrier and connects the input nodes to the analog reference (common mode input level of ½ supply voltage). This reset scheme re-establishes the input DC level periodically. Other possible input bias schemes are reverse bias diode [2] and sub threshold MOSFET [3].

The reset of every 16 cycles produces signal at 1/16th of the modulation frequency (31.2 KHz) which is attenuated by the bandpass filtering of the preamplifier. Thus, the distortion produced at this frequency does not corrupt the desired signal.

3.5 Clock Generation Circuits

Clock signals are needed to generate the modulation and demodulation signals, and the input bias reset signal. The 900 MHz signal from the PLL can be divided by a divide-by-2 and divide-by-3 circuit-chain to produce a 1 MHz signal to generate the various clock signals as shown in Figure 3.17 using a counter and D-type flip-flops (DFF) and digital logic gates. If the frequency of the crystal oscillator is a multiple of 1 MHz, it can be used to generate the modulation signal. Avoiding the divider chain will reduce power consumption significantly. The counter implementation is shown in Figure 3.18. The clock waveforms are shown in Figure 3.19. The signals ϕ and ϕb are required for modulator and demodulator. The modulator is turned off when the input nodes are reset. The signals ϕ_{rst} and $\phi_{rst}b$ are required to reset the modulator. Bias reset signal ϕ_{pitas} is needed in the bias resetting circuit to set the input DC level.



Figure 3.17: Clock generation circuit



Figure 3.18: Counter circuit





3.6 Demodulator

n CMOS technology the MOS switch based double balanced passive mixer [30-31] is an excellent choice as a demodulator for a number of reasons. Although the conversion gain of a passive mixer is always less than unity, it does not consume any power. Another advantage is the inherent linearity of the switching mixer due to the good linearity of MOS devices operated in the linear region. In passive mixer the bias current through the transistors is zero leading to a low flicker noise. The main source of error in this mixer is the non-symmetry in the devices or in the driving voltages.



Figure 3.20: A passive mixer as a demodulator

A switch based CMOS passive mixer is shown in Figure 3.20. It consists of four transistors, M1 through M4. These four transistors are grouped together into two pairs of two transistors each. Transistor M1 and M3 work together and controlled by positive carrier signal at their gates while M2 and M4 form another unit and controlled by negative carrier signal. Each pair serves the function of connecting the input terminals to the output terminals of the

demodulator. When positive carrier signal is high the pair M1-M3 is on and the input is directly connected to the output. On the other hand, when negative carrier signal is high the other transistor pair connects the input to the output with opposite polarity.

The design parameters for the switching mixers are the transistor size, the DC bias voltage of the carrier and input signals, and the amplitude and type of the carrier signal. A square wave carrier signal provides the best possible conversion gain of $2/\pi$ while output contains many mixing products that result from the odd-harmonic Fourier components of the square wave, which can be easily filtered out. A general expression for the output of a passive mixer is given by the following equation in [30]:

$$v_{rf}(t) = v_{BB}(t) \cdot \left[\frac{g_T(t)}{g_{T\max}} \cdot m(t) \right] \cdot \frac{g_{T\max}}{\overline{g_T}}, \qquad (3.17)$$

where, the function $g_T(t)$ is the time varying Thevenin equivalent conductance as viewed from the output terminals, $g_{T_{\text{max}}}$ and $\overline{g_T}$ are the maximum and average, respectively, of $g_T(t)$. The mixing function m(t) is defined by:

$$m(t) = \frac{g(t) - g(t - T_{car}/2)}{g(t) + g(t - T_{car}/2)},$$
(3.18)

where, g(t) is the conductance of each switch and T_{car} is the period of the carrier signal.

The bias voltages of input and carrier signals determine the switching instant of the transistors. If the gate source bias voltage is exactly equal to the threshold voltage V_T , the switching take place precisely when the carrier signal reaches the bias voltage. If the gate source voltage is less than V_T , the switching will be break-before-make and there will be finite amount of time when no transistor is on. If the gate source bias voltage is greater than V_T then the

switching will be called make-before-break and all transistors will be on for a certain amount of time. Besides the amplitude of the carrier signal, this also plays a significant role in design. The amplitude of the carrier signal has to be large enough so that it can turn on the switches when the input signal at its maximum and turn off when input signal at its minimum.

The dominant source of noise in this mixer is from the switches. In general, it is desirable that the switching transistors will be very wide to increase the conversion gain and to reduce their on resistances and associated thermal noise.



Figure 3.21: Transient response of the demodulator circuit

The size of the transistors in the demodulator circuit is 100 μ m and a square wave carrier is used. The transient simulation results are given in Figure 3.21. While plots 1 and 2 show the input and the output signals, plots 3 and 4 show their DFTs. DFT of the preamplifier output (plot

3) shows the frequency components at 499, 500 and 501 KHz. The DFT of the demodulator output (plot 4) has signal components at DC and 1 KHz as expected after demodulation. Conversion gain for the demodulator is about 0.6 which is very close to the ideal value of $2/\pi$.

3.7 Low Pass Filter

After demodulation, the down-converted baseband signals need to be low pass filtered to eliminate the higher harmonics created by the square wave carrier of the demodulator. The output of the preamplifier is shaped by its band pass characteristics leaving the frequencies at the carrier and its vicinity. The LPF provides further attenuation to the out of band signals. The LPF provides some gain to compensate for the mixer loss and provide best possible output swing at the input of the ADC. This LPF also performs anti-aliasing filtering for the ADC as well.

The schematic for the LPF is shown in Figure 3.22. It is a second order filter; the first pole is provided by the resistance R1 and the capacitance C1 at 3K and the second pole is provided by the output resistance of an analog buffer and an off chip capacitor C2 at around 10K. The LPF filter is followed by a level shifter. The source follower helps to present the output signal at a level such that the full dynamic range of the ADC can be utilized. Analog buffers at the input of the filter provide very high input impedance to the preceding demodulator circuit. This ensures a good conversion gain from the demodulator. The schematic of the analog buffer is given in Figure 3.23.



Figure 3.22: Lowpass filter



Figure 3.23: Analog buffer

Magnitude response of the LPF transfer function from XF simulation results is shown in Figure 3.24. It can be seen from the plot that the magnitude response of the LPF rolls-off by
about -20 dB/dec from 2K to 10K, and by about -40 db/dec from 10K to 100K. Figure 3.25 shows the transient simulation results. Plots 1 and 2 show the transient input and output signals and Plots 3 and 4 show their DFTs. It is clear from these plots that the LPF eliminates the 3rd and 5th harmonic from the demodulator carrier. Plots 5 and 6 are close up of the plots 3 and 4 at the vicinity of output signal at 1 KHz. It can be noticed that although the input has a significant DC component, the output does not have. This is due to the level shifting. The LPF is designed to provide a gain of 10; however due to loading and very low bias current at the level shifter circuit, effective gain is about 5 or 14 dB.



Figure 3.24: Frequency response of the lowpass filter



Figure 3.25: Transient response of the filter: input and its DFT and output and its DFT.

3.8 Analog to Digital Converter

The choice of ADC architecture plays an important and critical role in designing a low power electronic system. A poor architectural choice can jeopardize the low power goal irrespective of how well the individual ADC building blocks are designed. While low power consumption is vital in wireless sensor applications, many other factors such as ease of design, architectural flexibility, and technology portability play a significant role in choosing the ADC architecture as well. Since the proposed sensor node may have multiple sensors, for continuous real time data capability multiple ADCs are required. A design with higher performance than necessary would require an increase in power consumption. The power consumption of the ADC must be as small as possible. Moreover, the architecture should be able to incorporate outputs of multiple ADCs to form a digital bit-stream for transmission using a single RF transmitter. The interface circuit is designed to provide a 60 dB DR, and the signals from the sensor nodes are band-limited to 1 KHz. With these considerations and keeping the application in mind, the specifications for the ADC are set as following:

- 1. Resolution: 10-bits,
- 2. Dynamic range: 60 dB,
- 3. Sampling rate: 5 KHz, and
- 4. Power consumption: $<100 \mu$ W.

A comparison matrix [32] for common ADC architectures is given in Table 3.1. The comparison reveals that some types of ADCs are suitable for low power applications, while some others are poor choices. Flash and pipeline ADCs are not good choices due to their high power consumption. Dual slope (analog integration) architecture requires high precision off-chip components. Since the speed requirement of the ADC for the proposed system is moderate to low, sigma delta architecture could be a good choice for its low power and high resolution. However, this ADC is relatively complex to implement. Successive approximation register ADC architecture suits very well for the specifications of the proposed sensor node system. While analog components consume large bias currents even at standby, the SAR ADC requires a single analog component, a comparator. Remaining circuits in this architecture are digital, which run at a moderate frequency requiring very low power. The specifications for the comparator is not

stringent. The digital circuits along with the comparator are readily portable to a different technology. The ADC is simple in architecture and easy to implement. The outputs from multiple ADCs can easily be combined in this architecture to form a digital bit-stream for transmission using a single RF transmitter.

1	Flash	SAR	Dual Slope	Pineline	Sigma-Delta
Cood nick	Illtro Uigh	Madium to high	Monitoring DC	Ligh speeds	Ligh resolution
when:	Speed when	resolution (8 to	signals high	for Mana to	low to modium
when.	speed when	16bit) 5Mens and	resolution low	$100\pm$ Maps 8	speed no precision
	power	under low nower	nesolution, low	hits to 16 bits	speed, no precision
	not primary	amall size	power	lower nower	camponente digital
	not primary	sinali size.	consumption,	iower power	filter reduces onti
	concern		good noise	then flesh	aliaging
			performance	ulali fiasii.	raquiromonto
Comming	NIL:40 DAN	Dinom, accush	I Inless on insert	Small manallal	Ouerrormalia a
Mathad	IN DILS - 2° IN -	algorithm	Unknown input	sinali parallel	ADC
Method	1 Commonstant	algorithm,	voltage is	structure, each	ADC,
	Comparators	internal circultry	integrated and	stage works on	programmable data
	Caps increase	runs nigher speed.	value compared	bite	output.
	Dy a factor of			ons.	
Encoding	2 for each bit.	Cupananius	A male a	Disital	Orven Commilia o
Encoding	Thermometer	Successive	Analog	Digital	Over-Sampling
Method	Code	Approximation	Integration	Correction	Modulator, Digital
D: 1 /	Encoding	0 11: : 14	<u> </u>	Logic	Decimation Filter
Disadvantages	Sparkle codes	Speed limited to	Slow Conversion	Parallelism	Higher order (4th
	/	~5Msps. May	rate. High	increases	order or higher) –
	metastability,	require anti-	precision	throughput at	multi-bit ADC and
	high power	aliasing filter.	external	the expense of	multi-bit feedback
	consumption,		components	power and	DAC.
	large size,		required for	latency.	
	expensive.		accuracy.	-	
Conversion	Conversion	Increases linearly	Conversion time	Increases	Tradeoff between
Time	Time does not	with increased	doubles with	linearly with	data output rate and
	change with	resolution.	every bit	increased	noise free
	increased		increase in	resolution.	resolution.
	resolution.		resolution.	<u> </u>	<u> </u>
Resolution	Component	Component	Component	Component	Component
	matching	matching	matching does	matching	matching
	typically	requirements	not increase with	requirements	requirements
	limits	double with every	increase in	double with	double with every
	resolution to 8	bit increase in	resolution.	every bit	bit increase in
	bits.	resolution.		increase in	resolution.
				resolution.	

Table 3.1: An ADC Comparison Matrix

3.8.1 Successive Approximation Register ADC

One of the most popular types of successive approximation ADCs uses a binary-weighted capacitor array as its DAC and it is called charge redistribution SAR ADC. The schematic diagram of the designed 10-bit ADC, similar to a design in [33], is shown in Figure 3.26.



Figure 3.26: 10-bit successive approximation analog to digital converter

The successive approximation register block presents an N-bit digital code to the switching network, which is converted to an analog voltage V_{comp} by the binary-weighted capacitor array. The analog output V_{comp} is continuously updated by the DAC (formed by the SAR, the switching network and the capacitor array) using the comparator outputs until it reaches (within an LSB of the desired output resolution) a reference voltage V_{ref} , when the digital code at the input of the DAC is the N-bit representation of the sampled input voltage.

For the operation of the ADC, the input voltage signal is sampled into the capacitor array, while the V_{comp} node is charged to the reference voltage of the comparator. During this sampling phase a CLR signal keeps the reference and the CMOS switches at the input closed while the switches that connect the capacitor array to the SAR are open. The total charge stored in the capacitor array during the sample phase is then

$$Q = C_{tot}(V_{ref} - V_{in}) = 2^{N} C(V_{ref} - V_{in}).$$
(3.19)

This charge remains fixed (although it is redistributed) throughout an N-bit standard binary search, with the final digital output code available at the end. During the N-bit serial bitcycling the top plates of the capacitors are left to float at V_{comp} , while the bottom plates are cycled between V_{ref} and V_{ss} depending on the SAR codes. For a 10-bit ADC, the bit-cycling starts with the SAR guessing an initial value for the output as 1000000002 = 51210 equivalent to the mid point of the available input range, which is $0-V_{ref}$ V. Since the floating V_{comp} node voltage changes during the bit cycling while the total charge on the array remains constant at Qgiven by Equation (3.19). The voltage on the V_{comp} node for this approximation (51210) is

$$V_{comp} = \frac{3}{2} V_{ref} - V_{in} \,. \tag{3.20}$$

From Equation (3.20) it is seen that if V_{in} is greater than $0.5V_{ref}$ then the comparator produces a high output; and the SAR presents the next approximation, which in this case would be 1100000002 = 76810. For V_{in} less than $0.5V_{ref}$, the comparator produces a low output and the next SAR approximation would be 0100000002 = 12810. This process continues for N cycles when the inputs of the ADC are digital representation of the analog input signal.

3.8.2 Capacitor Array and Switching Network

As shown in Figure 3.26, the switching network, the SAR, and the capacitor array together act as a DAC. The switches for the input voltage must be able to pass signals with large swing; therefore CMOS switches are used. Single NMOS or PMOS transistors are used to implement other switches. The unit capacitor C in the capacitor array is chosen to be 100 fF.

Capacitance matching and the linearity of the switches determine the linearity of the ADC. Careful layout and a large unit capacitor size help good capacitance matching. The capacitor array layout must be made insensitive to parasitic capacitance. The switches may suffer from the charge injection and the clock feed-through inaccuracies. The reference and the CMOS input switches may contribute to charge injection error since they are turned off at the end of the sample phase. A dummy switch is used to compensate for the potential error caused by the reference switch. NMOS and PMOS transistors in the input pass gates compensate errors produced by each other when the input signal is somewhat close to the mid-value. The top plates of the capacitors are isolated; therefore, no charge error is contributed on the V_{comp} node. The

charging and discharging time of the capacitor array restricts the speed of the ADC. Therefore, the unit capacitance size and the 'on' resistance of the switches decide the maximum sampling rate.

If the input analog voltage is zero, according to (3.20) the voltage at the V_{comp} node can swing as high as $1.5V_{ref}$. On the other hand, the linearity of the ADC depends on the charge at the V_{comp} node remaining fixed throughout the bit- cycling. Therefore, the reference switch must remain strongly off for all possible V_{comp} values. Assuming a worst case V_{comp} voltage of $1.5V_{ref}$, the resulting constraint on V_{ref} and V_{tp} is

$$V_{ref} < V_{DD} - \left| V_{tp} \right|. \tag{3.21}$$

The value of V_{ref} is chosen $0.66V_{dd}$.

3.8.3 Comparator

The comparison time of the comparator must be such that N comparisons can be made during a single bit-cycling phase. The comparator should be fast enough so that the capacitor array charge-discharge time limits the sampling rate, not the comparator. On the other hand, if care is not taken, the resolution of the comparator may also limit the overall resolution of the ADC. A simple "track-and-latch" comparator, adopted from [34], as shown in Figure 3.27 suffices the moderate requirements of the ADC. The NMOS differential pair (transistors M1 and M2) in the comparator tracks and amplifies the differential input signal when a positive feedback is activated by a cross-coupled PMOS load formed by M3 and M4 resulting a tremendous amplification forcing the outputs of the comparator to latch to the rails. The latching comparator requires a reset phase (RST low) when the internal output nodes $V_o + \text{ and } V_o - \text{ in Figure 3.27}$ are clamped to V_{dd} by the transistors M5 and M6. When the RST signal goes high the nodes $V_o + \text{ and } V_o - \text{ slew towards ground at unequal rates determined by the differential input voltage. Inverters placed at the internal outputs provide CMOS rail to rail outputs.$

A good matching between two input transistors is required for low DC offset. The noise and circuit non-idealities are important during the track phase only. As the comparator latches, the positive feedback overwhelms any noise or disturbance in the circuit. However, during the track phase the input referred noise of the comparator must be kept substantially lower than one LSB in order to make sure that the ADC resolution is not limited by the comparator.

The comparator offset is dominated by the V_t mismatch between M1 and M2. The mismatch can be kept minimal by layout techniques. The large input devices also reduce the mismatch. Figure 3.28 shows transient simulation results of the comparator. During simulation, a 1 mV differential input signal is applied at time t = 10 µs. Differential output nodes V_o + and V_o - show that a small voltage difference is developed within 100 ns, which is very quickly pulled apart by the regeneration circuits. Output of the comparator is available after 300 ns at t = 10.3 µs.



Figure 3.27: Comparator



Figure 3.28: Transient simulation results of the comparator with a 1 mV differential input

3.8.4 Successive Approximation Register

The SAR implements the binary search algorithm for the ADC. The SAR is implemented using a design presented in [35]. The schematic of the circuit is shown in Figure 3.29. The different DFFs are designed to provide minimum signal activity to keep the power consumption low. Since the SAR is completely realized in the digital domain, it consumes lower power than the other circuits in the ADC.



Figure 3.29: Successive approximation register (SAR)

3.8.5 Parallel to Serial Converter

When the binary search algorithm finishes with the ADC output within 1 LSB of , the input to the ADC is the digital representation of the input signal. The available digital output needs to be serialized to make digital bit-stream for a convenient wireless transmission. A parallel to serial converter, as shown Figure 3.30, is designed to perform this function. Since, in the proposed 'AccuMicroMotion' wireless sensor system, there are multiple transducers and multiple interface and ADC blocks, the serial to parallel converter should be able to take inputs from multiple ADCs and provide serial outputs to the wireless transmitter. The designed parallel to serial converter can take input from up to 9 ADCs with 10-bit each. The input buffer used for this circuit is designed to provide a bit 'zero' input to the circuit, when input to the buffer is low. The buffer circuit is presented in Figure 3.31.

A four bit header and a four fit footer is included in the digital message to be transmitted wirelessly. Since these overhead bits are predefined and known to the wireless receiver, they help to identify the beginning and the end of a message. They also help the receiver to extract the clock signal from the message itself.

Transient simulations are performed for the ADC with different input voltages. The simulation results are shown in Figure 3.31. For a 1 KHz band limited signal, Nyquist rate is one sample in each 500 μ s. If each ADC has 10 bit data output, for data from 9 transducers, a message contains 98 bits including a 4 bit header and a 4 bit footer. Therefore, the message length becomes 196 μ s. As a result, theoretically up to 2.5 KHz input signal can be sampled.



Figure 3.30: Parallel to serial converter



Figure 3.31: Digital buffer



Figure 3.32: Digital output for different analog input

CHAPTER 4: WIRELESS TRANSMITTER

The design of the wireless transmitter for the 'AccuMicroMotion' sensor starts with the appropriate carrier frequency selection. There are three issues to consider for frequency selection: available frequency band allowed by the regulatory commission, best suitability in terms of circuit implementation and finally but not least importantly the effect on human tissues.

Since the application for the 'AccuMicroMotion' sensor require that the device will be worn on human skin or be implanted inside human body, the absorption of energy by the human body needs to be considered. The energy absorption needs to be minimal, first due to health reason, and second if the device is implanted then to keep the transmitted energy loss low. Human tissue can be considered as a non ideal dielectric material and can be modeled by a capacitor and a resistor in parallel [23]. Thus, the absorption of energy depends on the conductivity and the relative permittivity of the tissue. The models and experimental results [23, 36] show that energy absorption increases as the frequency of operation increases. Therefore, a smaller carrier frequency is desirable.

The nature of the signal that the sensor will transmit is a continuous data signal and not the burst codes. Thus, the options for transmission frequencies in USA due to federal regulations are limited to the frequencies as given in Table 4.1.

Frequency range	Approx max. power	Restrictions
902-928MHz	1mW	None
902-928MHz	1W	Only frequency hopping systems allowed
2.40-2.483GHz	200mW	virtually none
5GHz	-	-

 Table 4.1: Spectrum Restrictions

Low frequency RF circuits are easier to design. However, the transmission antenna for a low frequency carrier gets bigger for a same performance. Since the wireless signal for the proposed 'AccuMicroMotion' system needs to travel only 20 meters, the required output radiated power will be well below 1 mW. The transmitter of the proposed system is designed using 900 MHz ISM band. Using a standard ISM band will also give the flexibility to improve the designed system for various other amenities.

4.1 Wireless Architecture

To keep the implementation of the wireless sensor node simple, only a transmitter is designed at this stage. A receiver may be required for an actual product implementation of the 'AccuMicroMotion' sensor to accommodate interactions with other wireless sensors in a network and also with the base station that receives and acquires the physiological activity signals. To keep the power consumption minimum the strategy of this design is to use the simple circuits unless other options do not provide compelling advantages. The analog modulations such as amplitude modulation (AM) or frequency modulation (FM) are simpler. But, due to a DR requirement of 60 dB, it is difficult to design the circuits for AM. Especially the output stage can not provide such a large DR without introducing significant nonlinearity. FM requires very large bandwidth for the given DR. Therefore, a digital modulation is preferred.

With the proposed architecture, the digital bit-stream from the sensors' interface circuits turn on or off depending on the bits, consequently, the PA either transmit or don't transmit a 900 MHz RF signal. The modulation scheme is essentially Amplitude Shift Keying (ASK) or on-offKeying (OOK). OOK is considered because, it is simple to implement, does not require extra circuits and low power.

The PA provides the necessary power to a 50 Ω off-chip antenna through output impedance matching. For a commercial 'AccuMicroMotion' sensor product, the antenna will most likely be an on chip or on board loop or patch antenna. The efficiency of such an antenna is very inferior and their characteristics impedance is also very small. Since transmit signal is a constant envelop signal and it only needs to travel 20 meters, the specifications for the PA are very relaxed and it can be either linear or non linear.

Block diagram for the proposed ASK transmitter is shown in Figure 4.1. The phase lock loop generates the RF carrier signal synthesized from an off chip crystal oscillator. The PA circuit is turned on when the input digital information signal is logic 'one' and off when the input is logic 'zero'. This is implemented by two MOS switches.



Figure 4.1: ASK transmitter

4.2 Phase Lock Loop

A simplified block diagram for the phase lock loop (PLL) is shown in Figure 4.2. A PLL generates an output signal whose frequency is dependent on the phase relationship between two input signals. The phases of a reference signal, f_{ref} and a feedback signal, f_{comp} re compared in a phase-frequency detector (PFD). PFD generates 'up' or 'down' signal depending on the phase difference between its input signals. The phase difference is then converted to a current signal, I_{pump} by a charge pump (CP) circuit. A LPF known as the loop filter transforms this current signal into a control voltage v_{ctr} . This voltage tunes a voltage controlled oscillator (VCO) to change its resonance frequency to generate a signal with the desired frequency.

An external crystal oscillator provides the reference signal f_{ref} at the PFD input. A feedback divider divides the output signal f_{out} by a programmable divider with a divide ratio of N to generate the feedback comparison signal f_{comp} for the PFD. The feedback divider can be programmed to divide the f_{out} by 1 to 1024 with 1 MHz steps. Therefore, to implement FDMA for multiple sensors in a wireless network the channel spacing can be 1 MHz. The feedback divide divide is designed using the modular programmable divider given in [37]. The designed divide by 2/3 cell is similar, but uses regular logic gates and DFFs instead of source coupled logic (SCL) implementation.



Figure 4.2: Block diagram for the PLL circuit

4.2.1 Voltage Controlled Oscillator

Voltage controlled oscillator (VCO) is the key and most critical block of the PLL. An ideal VCO generates a periodic output whose frequency is a linear function of a control voltage v_{ctr} :

$$\omega_{out} = \omega_{fr} + K_{vco} v_{ctr}, \qquad (4.1)$$

where ω_{fr} is the free running frequency and K_{vco} is the gain of the VCO. Since phase is the time integral of frequency, the output of a sinusoidal VCO can be expressed as

$$y(t) = A\cos\left(\omega_{fr}t + K_{vco}\int v_{ctr}dt\right).$$
(4.2)

If the VCO is considered linear time-invariant system, with the control voltage as the system's input and the excess phase of the output signal as the system output. Since the excess phase is

$$\Phi_o(t) = K_{vco} \int v_{ctr} dt , \qquad (4.3)$$

the input/output transfer function is:

$$\frac{\Phi_o(s)}{V_{ctr}(s)} = \frac{K_{vco}}{s}.$$
(4.4)

The schematic of the designed VCO circuit is shown in Figure 4.3. It is an LC oscillator (LCO) whose resonance frequency is set by a varactor. A complementary LCO architecture is used for its better reliability, $1/f^3$ corner, higher transconductance for a given tail current, and fast settling time [38] compared to an NMOS only LCO. The output of the LCO is buffered and converted to a CMOS level signal by the CMOS inverters.

Since an LCO circuit usually consumes a large amount of power, the main design objective is to reduce the power consumption. The amplitude of oscillation is proportional to the tail current and the quality of the LC tank. Quality of the active transistors in the differential pairs and the input devices of the buffer is usually not a design parameter. The quality of the varactor can be set high by choosing correct DC bias and LCO architecture. An LCO architecture that does not suffer from gate oxide breakdown effects provides better varactor quality. A complementary architecture is better compared to NMOS only structure. Detail analysis of LC oscillator design and reliability issues are presented in the next chapter. The choice of the inductor is the only design issue here. A high quality inductor will provide higher amplitude of oscillation for a given tail current. On chip inductors are reported to have very low quality factor in the order of 5-10. Although it is expensive in terms of system implantation, off chip inductor is apparently better choice for the sensor application for low power consumption by the LCO.



Figure 4.3: VCO circuit and output buffer

Varactor: A varactor (variable reactor) is a capacitor used in a VCO whose capacitance value can be changed or set by a control voltage. In CMOS technology, the varactor can be realized with a reverse biased PN junction or a MOS transistor. There are three choices for the varactor implementation in a CMOS technology using MOS transistors. These three varactors are shown in Figure 4.4.

The gate capacitance of a MOS transistor varies nonlinearly as the DC gate bias varies among accumulation, depletion and inversion. Depending on the terminal connections, DC tuning characteristics of a MOS varactor can be different. PMOS transistor provides two options. First, the drain (D), source (S) and the bulk (B) terminals are connected to form a capacitance between the gate (G) and the D=S=B terminal as shown by the inset in Fig. 4.4 (b). However tuning characteristic for this varactor is non-monotonic and a stable PLL can not be implemented. Second, the bulk terminal is connected to VDD and the gate and source are tied to form the control terminal. This varactor is monotonic, but it suffers from the supply noise. On the other hand, NMOS transistor provides only one choice, where the drain (D) and source (S) terminals are connected to form a capacitance between the gate (G) and the D=S terminal as shown in Figure 4.4 (a); and the bulk (B) terminal is connected to ground. Simulated capacitance versus control voltage curves are shown in Figure 5.5 for the three types of varactors.



Figure 4.4: Three different varactor options



Figure 4.5: Capacitance versus control voltage for three different varactors

The varactor in Figure 4.4 (a) is used to design the VCO of the designed PLL. The tuning curve of the VCO is shown in Figure 4.6, which is monotonic. The VCO has 600 MHz tuning range in room temperature and nominal process corner. Required tuning range for the transmitter is only about 30 MHz. A much higher tuning range is necessary to cover a wide range of temperature and process variation. Figure 4.7 shows the peak to peak voltage of differential output (*vout* + and *vout* – in Figure 4.3) of the VCO versus control voltage, v_{cur} . The amplitude of the VCO output is fairly constant for a wide range of control voltages. The phase noise of the VCO is shown in Figure 4.8. The phase noise at a 1 MHz offset frequency of the carrier or at an adjacent channel is -120 dBc/Hz.



Figure 4.6: VCO tuning curve



Figure 4.7: Peak to peak output voltage at the output on the VCO (before the buffer)



Figure 4.8: Phase noise of the oscillator dBc/Hz versus offset frequency from the carrier

4.2.2 Phase Frequency Detector

The phase frequency detector (PFD) generates the error signal required in the feedback loop of the PLL. The PFD can resolve phase differences in the $\pm 2\pi$ range or more. The PFD compares the reference signal f_{ref} with that of the divided down VCO signal $f_{comp} = f_{out}/N$ and activates the charge pumps based on the difference in phase between these two signals.

Phase detector can operate at frequency detect, phase detect, or phase locked mode. When the phase difference is greater than $\pm 2\pi$, the device is considered to be in frequency detect mode. In frequency detect mode the output of the charge pump will be a constant current (sink or source, depending on which signal is higher in frequency). The loop filter integrates this current and results a continuously changing control voltage applied to the VCO. The PFD will continue to operate in this mode until the phase error between the two input signals drops below 2π . When the phase difference between the two signals is less than 2π , the PFD begins to operate in the phase detect mode. In phase detect mode the charge pump is only active for a portion of each phase detector cycle that is proportional to the phase difference between the two signals. Once the phase difference between the two signals reaches zero, the device enters the phase locked state. In the phase locked state, the PFD output will be narrow "spikes" that occur at a frequency equal to f_{ref} .

A simple PFD circuit is used in this design which is shown in Figure 4.9. The output of the NAND gate is delayed by approximately 1 nS to avoid the so called 'dead zone' details of which can be found in [25].

4.2.3 Charge Pump

The charge pump (CP) circuit used in this design is a single ended circuit. Its operation principle is very simple. Based on input signals (*up* and *down*) the CP circuit either push or pull

a 6 μ A current to or from the loop filter. The symmetry of the current sources and the device matching is extremely important in the CP.



Figure 4.9: Phase frequency detector circuit



Figure 4.10: Charge pump circuit

Transient simulation results for the PFD and CP circuits connected together are given in Figures 4.11 and 4.12. Figure 4.11 shows the transient waveforms of the PFD and CP outputs,

when reference and comparison signals have same frequency and phase. The PFD generates narrow spikes of about 1 nS. The CP circuit does not push or pull any average current to or from the filter. Figure 4.12 shows the same outputs with reference and comparison signals have different frequency. Due to a constant difference in the frequencies of the PFD inputs, the phase difference between them increases (since it is not inside a loop). Consequently, the time the CP pushes I_{out} current increases.



Figure 4.11: Transient waveforms of the PFD and CP circuit outputs, when reference and comparison signals have same frequency and phase



Figure 4.12: Transient waveforms of the PFD and CP circuit outputs, when reference and comparison signals have different frequency

4.2.4 Loop Filter

A second order RC filter as shown in Figure 4.13 is used as the loop filter for the PLL. Therefore, the PLL is third order. To select the component values for the loop filter, it is important to understand the behavior of the loop and its stability. A linear model for the PLL in terms of excess phase is given in Figure 4.14.



Figure 4.13: Loop filter circuit

Trans-impedance function of the loop filter is:

$$Z(s) = \frac{V_{out}}{I_{in}} = \frac{1 + sR_2C_2}{s^2R_2C_1C_2 + s\left(C_1 + C_2\right)} = \frac{1 + sT_2}{sC_1\left(1 + sT_1\right)} \cdot \frac{T_1}{T_2},$$
(4.5)

where, Time constants T_1 and T_2 correspond to pole and zero of the filter and as defined:

$$T_1 = R_2 \frac{C_1 C_2}{C_1 + C_2}$$
, and $T_1 = R_2 C_2$. (4.6)



Figure 4.14: PLL linear model

The open loop gain of the third order PLL is

$$G(s)H(s) = K_{\Phi}Z(s)\frac{K_{VCO}}{s}\frac{1}{N}$$
(4.7)

where, phase detector/charge pump constant is $K_{\Phi} = \frac{ICP}{2\pi}$ in A/rad and K_{VCO} is the VCO tuning constant in Hz/V. *ICP* is the charge pump current. In this design the value of this current is 6 μ A. Now, the open loop gain in the frequency domain:

$$G(\omega)H(\omega) = \frac{-K_{\Phi}K_{VCO}(1+j\omega T_2)}{\omega^2 C_1 N(1+j\omega T_1)} \frac{T_1}{T_2}$$
(4.8)

The available phase margin of the loop:

$$G(\omega)H(\omega) = \frac{-K_{\Phi}K_{VCO}(1+j\omega T_2)}{\omega^2 C_1 N(1+j\omega T_1)} \frac{T_1}{T_2}$$
(4.9)

To ensure loop stability, the phase margin is expected to be maximum, when the magnitude of the loop gain is unity. If the loop bandwidth is ω_p and the phase margin is ϕ_p , these conditions mandate to [39]:

$$\frac{d\phi(\omega)}{d\omega} = \frac{T_2}{1 + (\omega T_2)^2} - \frac{T_1}{1 + (\omega T_1)^2} = 0$$
(4.10)

$$\Rightarrow \omega_p = \frac{1}{\sqrt{T_1 T_2}},\tag{4.11}$$

and,
$$|G(\omega)H(\omega)| = \frac{K_{\Phi}K_{VCO}\sqrt{1+(\omega T_2)^2}}{\omega^2 C_1 N \sqrt{1+(\omega T_1)^2}} \frac{T_1}{T_2} = 1.$$
 (4.12)

Formulas for T_1 and T_2 can be found using (4.6)-(4.12):

$$T_1 = \frac{\sec \phi_p - \tan \phi_p}{\omega_p}, \qquad (4.13)$$

and,
$$T_2 = \frac{1}{\omega_p^2 T_1}$$
. (4.14)

The component values for the loop filter can be determined using following expressions:

$$C_{1} = \frac{K_{\Phi}K_{VCO}}{\omega_{p}^{2}N} \sqrt{\frac{1 + (\omega_{p}T_{2})^{2}}{1 + (\omega_{p}T_{1})^{2}}},$$
(4.15)

$$C_2 = C_1 \left(\frac{T_2}{T_1} - 1\right), \tag{4.16}$$

and,
$$R_2 = \frac{T_2}{C_2}$$
. (4.17)

For an output frequency of the PLL (f_{out}) of 910 MHz, and the feedback comparison frequency f_{comp} of 1 MHz the feedback divider ratio N is 910. The charge pump current is 6 μ A, therefore the PFD/PD constant K_{ϕ} is 955 nA/rad. The VCO tuning constant K_{VCO} is 1 GHz/V. Loop bandwidth ω_p and the phase margin ϕ_p are 100 KHz and 60⁰ respectively. Using (4.15)-(4.17), the component values of the loop filter can be calculated. The values are: C_1 =1.73 pF, C_2 =22.43 pF and R_2 =265 KΩ.

The PLL is simulated using HSim simulator in the Cadence environment. The simulated results are shown in Figure 4.15.

4.3 Power Amplifier

The design of the power amplifier (PA) is critical to achieve low power objective of the system. Since at the input of the PA we have constant envelop carrier signal, non linearity of the PA is not a problem. Most of the PA designs found in the literature focus on high efficiency and high power transmit capability. However, the efficiency of a PA goes very low when the required transmitted power is about or below 1 mW [40].



Figure 4.15: Transient simulation results of the PLL circuit

To implement the PA for the ASK transmitter, we searched for a low power architecture. Class E amplifiers (usually have very high efficiency) do not promise good efficiency for a power around 1 mW. A simple class AB amplifier is chosen for this design which is based on the design in [40] and modified to make the PA capable of ASK modulation by using switches. The PA circuit schematic is given in Figure 4.16. The preamplifier stage is stacked on top of the output stage to use a single bias current for both stages. Because of the low power requirement, the output voltage swing is not large; therefore a stacked structure does not create any problem.



Figure 4.16: Power amplifier circuit

The preamplifier stage takes the 900 MHz carrier from the PLL circuit and provides the output at the drain of the transistor M3. This output is fed to the second stage through a coupling capacitance C_{c1} . The second stage is biased by a current mirror that sets the gate voltage of the output driver transistor M2. The capacitor C and the inductor L form a resonance circuit at 900 MHz at the drain of the transistor M2. The coupling capacitance C_{c2} and the inductor L_m provide the matching for a 50 Ω antenna. The digital data bit-stream from the interface circuits are used to turn on or off the PA to implement the ASK modulation. The switches realized by transistors M4 and M5. The PA circuit is simulated to fine tune the circuit components and the

simulated results are given in Figures 4.17 to 4.18. The PA performance matrix is summarized in Table 4.2.

Parameter	Simulated Value					
Output	With logic '1' input	2.282 mW				
power	With logic '0' input	230 nW				
Power	With logic '1' input	14.22 mW				
Dissipation	With logic '0' input	10 μW				
Efficiency	With logic '1' input	16 %				
Total Harmo	-40.3 dB					
Noise Figure	11.8 dB					
Output noise	4nV/√Hz					

Table 4.2: Performance of the PA



Figure 4.17: Transient voltage and current waveforms of the PA



Figure 4.18: Transient output voltage and its DFT


Figure 4.19: Output signal through PSS analysis



Figure 4.20: Conversion gain of the PA



Figure 4.21: S22 parameters of the PA

Figure 4.17 shows the transient voltage waveforms at the gate and drain of the second stage amplifier transistor. It also shows drain current and the output voltage. Notice when the drain current is at its maximum the drain voltage is its minimum. Figure 4.18 show the transient output voltage when the input of the PA is a digital bit-stream (in this case a 1010.. sequence). Figure 4.19 shows the output signal through PSS analysis. The simulation results show that the 2nd harmonic is 42 dB and 3rd harmonic is 50 dB lower then the carrier signal. Total harmonic distortion is calculated to be -40.3 dB. Figure 4.20 shows the conversion gain of the PA. At 900 MHz it is about 0 dB. Figure 4.21 shows the S22 parameters of the PA on a smith chart. S22 is

used to find the output matching. The overall performance especially the SNR, power consumption of the different blocks of the transmitter and overall power efficiency of the transmitter is summarized in Table 4.3. The SNR of the transmitter is calculated by the ratio of the output power when the PA is transmitting and when it is not transmitting.

Parameters	Simulated value
SNR (Mark to space ratio)	40dB
Average Power dissipation	8 mW
Oscillator	1.95 mW
Oscillator bias	0.15 mW
Loop filter	0.00 mW
Charge pump	0.24 mW
Phase Frequency Detector	0.06 mW
Feedback divider	0.9 mW
Power amplifier (ON 33% time)	4.75 mW
Power amplifier bias	0.30 mW
Transmitter power efficiency	27 %

Table 4.3: Transmitter

CHAPTER 5: MODELING AND RELIABILITY OF CMOS RF CIRCUITS

As CMOS technology advances, it is becoming more and more attractive for system-ona-chip implementation. Due to continued scaling, deep sub-micrometer CMOS transistors can result in a cutoff frequency (f_T) over 100 GHz and noise figure lower than 0.5 dB [41-42]. On the other hand, when the oxide is scaled down to less than 3 nm, hot carrier (HC) and soft breakdown (SBD) or even hard breakdown are more likely to take place [43-45]. As a result, oxide trapping and interface generation cause long-term performance drift and related reliability problems in CMOS devices and circuits. Nowadays, the oxide has already been scaled down to 1.2 nm [46], so it is essential to study the HC and breakdown (BD) oxide breakdown effect on deep sub-micrometer RF MOS transistors and circuits. Combined hot carrier and soft breakdown effect on RF MOSFETs has been reported [47-48], and effect of soft and hard breakdown on RF devices and circuit performance has also been published [49-53].

HC and SBD are two critical issues of deep sub-micrometer CMOS device and circuit reliability. HC are usually believed to be caused by damage of Si/Si interface state and charge trapping in the oxide due to the high channel electric field between drain and source. Some carriers may gain enough kinetic energy from the lateral electric field so that they overcome the Si/SiO barrier and trapped in the oxide. Interface state generation may result due to recombination with trapped carriers or breakage of Si–H bonds by high energy carriers. Interface states lead to mobility degradation by scattering interaction with channel carriers. Mobility degradation leads to the drain current degradation. Charge trapping and interface state change the charge distribution above the channel, and cause the threshold voltage to change. The increased random thermal motion of the carriers in the channel after HC stress increases the channel thermal noise, which is a critical factor in most RF circuit design. Breakdown is another important issue for device and circuit reliability. Compared to hard breakdown, SBD is more prevalent for ultra-thin oxides. In addition, HC also triggers more SBD. Similar to HC, the BD also causes the mobility, threshold voltage shift and transconductance shift. BD also changes the gate capacitance and introduces a finite gate to drain and gate to source conductance that change the RF parameters.

The HC induced device degradations are correlated to the substrate current and the gate current for nMOSFETs and pMOSFETs, respectively. For nMOSFETs, the correlation exists because hot carriers and I_{sub} are driven by the maximum channel electric field, which occurs at the drain end of the channel. For pMOSFETs, the charge trapping in the gate oxide is the dominant driving force for degradation, so the degradation is correlated with the gate current.

5.1 Device Modeling and Reliability

A small-signal equivalent circuit of the MOSFET after breakdown is employed for accurate parameter extraction using *Y*-parameters converted from measured *S*-parameters. Data measured on the MOS transistor biased in the linear region before and after breakdown is used to extract the breakdown spot resistance and total gate capacitance. This methodology provides critical information about the impact brought by gate oxide breakdown.

When a device is stressed by an applied voltage, an oxide film could lose its insulating properties and traps are generated within the oxide that increase the leakage current through the film. Eventually, these traps complete some conducting paths that bridge the two electrodes across the oxide [54-57]. At a given time, assume the number of conducting paths inside the gate

oxide is n, and each conducting path is associated with a conductance gi,i=1,2,...,n, these conducting paths divide the resistance between drain and source into many parts. This situation is illustrated in Figure 1. As stress time increases, more conducting paths are formed, and the gate leakage current increases.



Figure 5.1: Distribution of breakdown conductance inside oxide

Y parameters of a device can be extracted from the S parameters. Y parameters can be used to extract the gate capacitance and the gate to drain and gate to source resistances. S parameters can be measured directly from the device. The shift of S-parameters due to BD can be utilized to estimate RF device parameters degradation. The procedures to extract device parameters from the Y-parameters are discussed below.



Figure 5.2 Equivalent circuit after breakdown for calculation of Y_{11} ($V_{DS} = 0$ V)

Small-signal equivalent circuit used for the calculation of Y_{11} is given in Figure 5.2. The breakdown equivalent resistance R_0 is added to the equivalent circuit, and also the external components such as R_g , R_d , and R_s are considered so that an accurate parameter extraction can be implemented. By using assumptions in [58]: the relevant operation frequency is considered up to roughly to 10 GHz, resulting in the following simplifications:

$$\omega^{2}C_{gd}C_{gs}R_{d}R_{s} \ll 1$$

$$\omega^{2}C_{gd}C_{gs}(R_{d} + R_{s})R_{g} \ll 1 , \qquad (5.1)$$

$$\frac{1}{1 + j\omega C_{gg}R_{g}} \cong 1 - j\omega C_{gg}R_{g}$$

where C_{gg} is the total gate capacitance $C_{gg} \cong C_{gs} + C_{gd}$. The input admittance Y_{11} can be expressed as

$$Y_{11} = \left(R_g + \left(\frac{1}{R_0} + \left(\frac{1}{R_s} + \frac{1}{j\omega C_{gs}} + \frac{1}{R_d} + \frac{1}{j\omega C_{gd}} \right)^{-1} \right)^{-1},$$
(5.2)

where $R_0 = 1/g_0$.

Neglecting higher order terms, (5.2) is simplified to

$$Y_{11} \cong \frac{1}{R_0} + \omega^2 (C_{gg}^2 R_g + C_{gs}^2 R_s + C_{gd}^2 R_d) + j\omega C_{gg}, \qquad (5.3)$$

$$R_{0} = \left| \frac{1}{\operatorname{Re} al(Y_{11}) - \omega^{2} (C_{gg}^{2} R_{g} + C_{gs}^{2} R_{s} + C_{gd}^{2} R_{d})} \right|_{(BD)}, \text{ and}$$
(5.4)

$$C_{gg} = \left| \frac{\operatorname{Im} ag(Y_{11})}{\omega} \right|_{(BD)}.$$
(5.5)

Note that (5.3) is the expression of Y_{11} after breakdown. The equation of Y_{11} before breakdown is given as [58]

$$Y_{11} = j\omega C_{gg} + \omega^2 (C_{gg}^2 R_g + C_{gs}^2 R_s + C_{gd}^2 R_d).$$
(5.6)

 C_{gg} before and after breakdown depends on the imaginary part of Y_{11} . Because R_g, R_s , and R_d are dominated by the resistive poly-silicon and diffusion layers and treated as bias-, stress- and frequency-independent. They can be extracted from the Y-parameters before breakdown [58].

$$R_g = \left| \frac{\operatorname{Re} al(Y_{12})}{\operatorname{Im} ag(Y_{12}).\operatorname{Im} ag(Y_{11})} \right|_{(FRESH)}$$
(5.7)

Due to the symmetry reasons,

$$R_{d} = R_{s} = \left| \frac{\operatorname{Re} al(Y_{21}) - \operatorname{Re} al(Y_{12})}{\operatorname{Im} ag(Y_{12})^{2}} \right|_{(FRESH)}$$
(5.8)

After breakdown, since the transistor is operating in the linear region with $V_{DS} = 0$ V, C_{gd} is approximately equal to C_{gs} , from equation (5.5)

$$C_{gd} = C_{gs} \cong \frac{C_{gg}}{2} \tag{5.9}$$

Using (5.4) and (5.5), R_0 and C_{gg} can be obtained from the Y-parameters converted from S-parameters.

5.1.1 Experiments and Measurements

The devices used in this work are 0.16 μ m CMOS transistors. The oxide thickness is 2.4 nm and total channel width is 50 μ m. Many transistors are tested to verify the physical effect. The wafer is tested with a Cascade 12000 Probe Station and an Agilent 4156B Semiconductor Parametric Analyzer for dc measurements, while the RF experiments up to 10 GHz are carried out using an Agilent 8510C Network Analyzer. It is found that the breakdown voltage is about 3 V. For the gate oxide breakdown, an accelerated stress is carefully set at VG = 2.6 V, and VD = 0 V. The stress was interrupted every 1800 s to measure various transistor parameters. The source and bulk are grounded. S-parameters are measured in the common source-bulk configuration. On-wafer dummy structures are used to calibrate the pad parasites. A photograph for the experimental and measurement set up is shown in Figure 5.3.



Figure 5.3: Device measurement setup in the lab

A time-dependent dielectric breakdown is shown in Figure 5.4. The gate current increases drastically after the device is stressed between 80 and 120 s, which indicates the occurrences of gate oxide breakdown. S-parameters of the devices are measured. The current gain h_{21} and cutoff frequency are extracted before and after stress. h_{21} decreases with an increase of frequency at very high frequencies. After breakdown, there is a large drop in h_{21} , as shown in Figure 5.5. The normalized cutoff frequency degradation is displayed in Figure 6. The percentage of degradation of f_T due to oxide breakdown increases with stress. It is interesting to note that the degradation saturates after 2 hours of stress when it reaches 25 % degradation.



Figure 5.4: Gate current versus time

The comparison of the real part and imaginary part of Y_{11} before and after breakdown is given in Figure 5.6 and Figure 5.7. It is seen that stress affects Y-parameters, especially the real parts [59]. The change of real part of Y_{11} represents the breakdown effect on the gate oxide resistance. The change of imaginary part of Y_{11} demonstrates the effect of breakdown on the gate oxide capacitance.



Figure 5.5: Current gain h_{21} as a function of frequency

Using (5.7), (5.8), in the range of 5GHz to 10GHz, R_g , R_s , and R_d are extracted from the Y-parameters converted from S-parameters before breakdown: $R_g = 8.12 \Omega$, $R_d = R_s = 1.24 \Omega$, they are bias-, stress- and frequency-independent. C_{gg} , C_{gd} and C_{gs} can be extracted from (5.5) and (5.9). R_0 is thus available from (5.4). From Figure 5.8, it can be seen that the breakdown spot resistance decreases to 11 k Ω . C_{gg} versus stress time is shown in Figure 5.9. The gate oxide capacitance decreases with stress time due to formation of conducting paths caused by traps which degrades the integrity of gate oxide. In [60] it is found that the area of an oxide defective region around the BD spot is much larger than the BD conductive path. It is explained that the neighboring region around the BD spot also loses the capability to hold charges. Figure 5.9 shows that in every half of an hour the gate capacitance reduces about 2 %, which corresponds to an effective gate oxide area reduction in the order of 10⁻⁹ cm². This is consistent with [60], where

the area of the damaged region of each BD spot is around 10^{-10} cm² and multiple breakdowns give the effective damage area greater than 10^{-10} cm². Note that the degradation of R_0 and C_{gg} slows down after 2 hours of stress. This observation is consistent with the saturation of cutoff frequency degradation after 2 hours of stress.



Figure 5.6: Real part of Y_{11} as a function of frequency



Figure 5.7: Imaginary part of Y_{11} as a function of frequency



Figure 5.8: R_0 versus stress time



Figure 5.9: C_{gg} versus stress time

5.1.2 HC and SBD Combined Effect

For HC and SBD combined effects on transistors, the devices are stressed at $V_G = V_D = 2.6$ V. The transistor models are extracted from device measurements under the HC and SBD combined stress using BSIMPro software. While model parameters for the transistors degrade across the board, an increase of threshold voltage and decrease in mobility are most noticeable and are given in Figs. 5.10 (a) and (b) respectively. Experimental data show that the transconductance of the transistor degrades significantly subject to stress. Figure 5.10 (c) shows the transconductance versus stress time due to the HC effects. The transconductance was measured at a bias current of 7 mA.



Figure 5.10: Threshold voltage, mobility and transconductance versus stress time.

5.2 Finite Input Impedance and Reliability of Interface Circuits

The CMOS MEMS capacitive sensors have ultra small sensing capacitance (in the order of 10-100 fF), hence, have very high impedances, according to the following relationship:

$$Z = \frac{1}{2\pi fC}.\tag{5.10}$$

With most systems operating at modulation frequency between 100 KHz and 10 MHz, the impedance of CMOS MEMS capacitive sensor is in the range of 10⁶-10⁸. To avoid substantial attenuation of the signal, the interface circuit must have comparably high input impedance. Field effect transistors (FET), such as MOSFETs, are usually very suitable in capacitive sensing for MEMS devices for their high input impedance. However, deep sub micron devices have very thin gate oxide. Sustained high electric field for prolonged period may lead to BD in the gate oxide region. The degree of degradation depends on the electrical stress in the gate terminal. Nonetheless, the input resistance of the deep sub-micron devices tends to decrease from its ideal infinite value. As a result, the effects of finite input resistance need to be included for sensitivity calculation in deep sub-micron CMOS processes.

An equivalent transistor model that accommodates the finite input resistance can be found in [50, 61]. Using that model the simplified input sensing circuit can be drawn as in Figure 5.11.



Figure 5.11: MEMS capacitance sensing to include finite input impedance.

To find the expression for sensitivity, let us apply KCL in the sensing node,

$$j\omega C_{s1}(V_{m}-V_{s}) = (g_{0}+j\omega C_{p})V_{s}+j\omega C_{s2}(V_{s}+V_{m})$$
(5.15)

$$\Rightarrow V_{s} = V_{m} \cdot \frac{j\omega (C_{s1}-C_{s2})}{j\omega (C_{s}+C_{s2}+C_{p})+g_{0}}$$

$$= V_{m} \cdot \frac{j\omega \left[\frac{C_{s}x_{0}}{x_{0}-x}-\frac{C_{s}x_{0}}{x_{0}+x}\right]}{j\omega \left[\frac{C_{s}x_{0}}{x_{0}-x}+\frac{C_{s}x_{0}}{x_{0}+x}+C_{p}\right]+g_{0}}$$

$$= V_{m} \cdot \frac{2xx_{0}C_{s}}{2x_{0}^{2}C_{s}+(x_{0}^{2}-x^{2})\left(C_{p}+\frac{g_{0}}{j\omega}\right)}$$

$$= V_{m} \cdot \frac{2C_{s}}{2C_{s}+C_{p}+\frac{g_{0}}{j\omega}} \cdot \frac{1}{1-\frac{C_{p}+\frac{g_{0}}{j\omega}}{2C_{s}+C_{p}+\frac{g_{0}}{j\omega}}}$$
(5.16)

Expanding using Taylor's series and assuming x is very small compared to x_0 we get,

$$V_{s} = \frac{j\omega 2C_{s}}{g_{0} + j\omega \left(2C_{s} + C_{p}\right)} \cdot \frac{x}{x_{0}} \cdot V_{m}.$$
(5.17)

For very low frequency acceleration, using (2.23) the sensitivity is given by:

$$\frac{V_s}{a_{in}} = \frac{j\omega 2C_s}{g_0 + j\omega \left(2C_s + C_p\right)} \cdot \frac{V_m}{x_0} \cdot \frac{1}{\omega_n^2}.$$
(5.18)

When the input impedance of the transistor is assumed to be infinity, the expression for sensitivity becomes:

$$\frac{V_s}{a_{in}} = \frac{2C_s}{2C_s + C_p} \cdot \frac{V_m}{x_0} \cdot \frac{1}{\omega_n^2}.$$
(5.19)

As an example to illustrate the effects of finite input resistance of MOS transistor, let us consider a surface micromachining accelerometer in [3] where the amplitude of the modulation signal is 1 V. The modulation frequency is 2 MHz. The Sensing capacitances (C_s) are 64 fF. Transistor input capacitance and sensor to electronic circuit interconnect capacitance are about 110 fF and 10 fF respectively. As a result, C_p is 120 fF. The displacement of the sensor for 1 g acceleration is 3.1 nm which corresponds to capacitance change, ΔC of 0.13 fF Resonance frequency of the sensor is 56 krad/s and finally the gap between the fingers is 1.5 µm.

Now, without considering the finite input impedance the sensitivity of the accelerometer according to (6.4) is 219.4 μ V/g. A typical value for a deep submicron NMOS transistor has been found to be in the order of 10⁶-10⁷ [52]. Let us pick a value of 1 M Ω for illustration. The sensitivity of the accelerometer with finite input resistance can be calculated using (6.3) and it is 184.6 μ V/g.

5.3 Modeling of LC Oscillator for Reliability

The differential LC oscillator became attractive in recent years [38, 62-65] because of the implementation of cheap and reliable monolithic voltage controlled oscillator (VCO) for the integrated system-on-a-chip RF CMOS transceivers. It is found that the LC oscillator offers better phase noise performance. However, the secondary effects of the deep submicron devices make the design of this circuit challenging. As the CMOS device size shrinks, the horizontal electric field becomes increasingly higher and generates hot carriers (HC) in the channel. These high energy carriers, when traveling from the source to the drain, create interface-traps and oxide-trapped-charges and, thereby alter the device characteristics. Experimental results show

that the HC effect reduces the mobility of the carrier, increases the threshold voltage, and degrades the transconductance. On the other hand, when a high gate voltage sustains across the thin gate oxide of a transistor for a prolonged time, the breakdown (BD) phenomenon is more likely to take place. While the BD causes damages to a device, it still can be operational. The BD effect develops conducting paths through the gate oxide and reduces the gate capacitance. Both HC and BD effects have serious consequences on the LC Oscillator. The HC and soft-breakdown (SBD) effects on a ring oscillator based VCO have been reported in [66]. Some interesting and useful observations are presented in [67]. However, it does not provide a complete picture because it does not address the combined effects of HC and BD degradations on the active transistors in the differential (diff) pair of the LC VCO and the BD degradations on the varactor performance.

In this work, to characterize the effects of HC and BD on the LC oscillator on-wafer 0.16 μ m NMOS transistors with oxide thickness of 2.4 nm and a channel width of 50 μ m are stressed to obtain transistor models before and after stress. The tank amplitude of the oscillator is derived analytically. A closed-form expression for the average capacitance of a varactor that accounts for large signal effect is presented. HC and BD effects on the NMOS LC oscillator are analyzed and corresponding reliability models are developed. HC and BD effects on the oscillator are also demonstrated through Cadence SpectreRF simulation.

5.3.1 LC Oscillator

A capacitor and an inductor in parallel form an LC tank that resonates at a frequency of

$$\omega_o = \frac{1}{\sqrt{LC}} \,. \tag{5.20}$$

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If both the inductor and the capacitor are lossless and some energy is trapped in the resonator tank, there will be an oscillation. However, since it is impractical to fabricate any lossless passive components, as a result, the oscillation dies. Now if a negative resistance is connected to the tank, the loss in the parasitic resistances of the passive components is recovered by the energy supplied by the negative resistance, therefore, the circuit oscillates. A negative resistance is usually synthesized by the active transistors. A popular version of the negative resistance LC oscillator and its equivalent one port representation is shown in Figure 5.12 (a) and Figure 5.12 (b) respectively. In the LC oscillator structure, back to back transistors in positive feedback yield an equivalent resistance of $R_{in} = -(2/g_m) + (2/g_{ds})$, where, g_m is the transconductance and g_{ds} is the output conductance of the NMOS transistors.



Figure 5.12: (a) LC Oscillator and (b) its equivalent circuit.

The equivalent resistance of the tank is $R_{eq} = R_{LC} || (2/g_{ds})$, where, R_{LC} represents the parasitic resistance for the inductor and capacitor. The condition for sustained oscillation is $|-2/g_m| \le R_{eq}$. In other words, the amount of energy supplied by the negative resistance has to be bigger than the amount of energy lost in the tank. Therefore, there is a minimum value of the transconductance $g_{m0} = 2/R_{eq}$ that ensures the oscillation.

When the oscillation of the tank grows, the differential pair of the oscillator in Figure 5.12 (a) switches the tail current I_{tail} completely from one arm to another in every half cycle. However, the current through the tank is not a standard rectangular current waveform; rather it has a waveform as shown in Figure 5.13 (a). The fundamental component of the current is

$$I_0 = \frac{1}{\pi} \int_0^{2\pi} i(t) \sin\left(\omega t\right) d\left(\omega t\right) = \frac{4}{\pi} \int_0^{\frac{\pi}{2}} i(t) \sin\left(\omega t\right) d\left(\omega t\right)$$
(5.21)

The current follows a sine waveform until it reaches its maximum value of $I_{tail}/2$ at an offset angle of θ . Thus,

$$I_{0} = \frac{4}{\pi} \int_{0}^{\theta} A \sin(\omega t) d(\omega t) + \frac{4}{\pi} \int_{\theta}^{\frac{\pi}{2}} I_{tail} \sin(\omega t) d(\omega t)$$

$$= \frac{4}{\pi} \Big[A \Big(\frac{\theta}{2} - \sin(2\theta) / 4 \Big) + I_{tail} \cos \theta \Big]$$
(5.22)

where $\theta = \omega \cdot \Delta T$ and A can be evaluated from $I_{tail} / 2 = A \sin \theta$. Therefore,

$$I_0 = \frac{4}{\pi} I_{tail} \cdot \left(\frac{\theta}{4\sin\theta} + \frac{3\cos\theta}{4}\right).$$
(5.24)

As a result, the resonator tank amplitude can be approximated as

$$V_m = \alpha \frac{4}{\pi} I_{tail} R_{eq} , \qquad (5.25)$$

where $\alpha = \frac{\theta}{4\sin\theta} + \frac{3\cos\theta}{4}$ is a fitting parameter. The parameter α for different offset angle θ is plotted in Figure 5.13 (b). The parameter θ is obtained from the relation $\theta + 1.5\sin 2\theta = \pi / g_m R_{eq}$.



Figure 5.13: (a) Differential drain current and (b) evaluated fitting factor, α .

This mode of operation is the current limited operation. On the other hand, the power supply limits the largest possible amplitude to V_{DD} , when the tail current source transistor shuts off at each negative peak of the oscillation. The optimum tail current that achieves this maximum amplitude in the voltage limited operation is

$$I_{opt} = \frac{\pi V_{DD}}{4\alpha R_{eq}}.$$
(5.26)

A 2.4 GHz LC oscillator using the structure shown in Figure 5.12 (a) has been designed using two ideal inductors and an ideal capacitor. The amplitude of oscillation is simulated for varying tail currents for different supply voltages using SpectreRF circuit simulator. Corresponding values are calculated using the analytical expression given in (5.25). The simulated and calculated tank voltage amplitude versus tail current is shown in Figure 5.14. Obviously, a nonlinear relationship between the tail current and the tank voltage amplitude exists. Simulated results (lines) agree with analytical values very well.

The DC drain to source voltage across the differential MOS transistors in the LC oscillator shown in Figure 5.12(a) is

$$V_{DS} = V_{DD} - \frac{I_{tail}}{2} R_s - V_{DSAT, tail}$$
(5.27)

where R_s is the series resistance to the inductor due to its finite quality.

The parasitic series resistance of a reasonable quality inductor is very small (order of few ohms), therefore the voltage drop across it is negligible. Also, the overdrive voltage at the tail current source $V_{DSAT,tail}$ is usually kept low to allow a higher output swing. Thus, the transistors at the differential pair experience a DC bias voltage of $V_{DS} = V_{GS} \approx V_{DD}$. Moreover, the transient

voltage across the transistors can reach as high as $2V_{DD}$. As a result, if the oscillator is in operation for a prolonged time the transistors experience HC and BD simultaneously.



Figure 5.14: Simulated voltage amplitude versus tail current

The transconductance of a transistor is approximated as

$$g_{m} = \mu_{n} C_{ox} \frac{W}{L} (V_{GS} - V_{th}) = \sqrt{\mu_{n} C_{ox} \frac{W}{L} I_{tail}} .$$
 (5.28)

As HC and oxide BD decrease the mobility of the carrier and increase the threshold voltage; it is clear from (5.28) that the transconductance decreases with stress. Degraded g_m may cause the oscillation to cease if $g_m \le (2/R_{eq})$.

5.3.2 MOS Varactor

A varactor (variable reactor) is a capacitor used in a VCO whose capacitance value can be changed or set by a control voltage. In CMOS technology, the varactor can be realized with a reverse biased PN junction or a MOS transistor. The MOS varactors became popular in recent years [68-70]. The gate capacitance of a MOS transistor varies nonlinearly as the DC gate bias varies among accumulation, depletion and inversion. Depending on the terminal connections, DC tuning characteristics of a MOS varactor can be different. In the first option, the drain (D), source (S) and the bulk (B) terminals are connected to form a capacitance between the gate (G) and the D=S=B terminal as shown by the inset in Figure 5.15 (a). This varactor has a nonmonotonic tuning characteristic that is difficult to handle by a frequency synthesizer. Figure 5.15 (a) shows the simulated capacitance versus gate voltage C-V curve for an NMOS varactor of this type. In the second MOS varactor option as shown in Figure 5.15 (b), the bulk terminal is connected to one of the supplies and the gate and source are tied to form the control terminal to realize a phase lock loop frequency synthesizer. This structure is known as the inversion mode varactor and its simulated C-V curve is shown in Figure 5.15 (b) using an NMOS transistor. The last option is to operate the MOS varactor in the accumulation region [69]. Typical CMOS processes and design tools do not provide sufficient models for this kind of varactor. This paper uses the inversion mode varactor for analysis and simulation.

The parasitic resistance associated with the channel of the transistor that mainly determines the quality of a MOS varactor in the inversion mode is [71]

$$R_{mos} = \frac{L}{12\mu_n CoxW(V_{gs} - V_t)}$$
 (5.29)

In this analysis, the capacitor of the LC tank is formed by two varactors connected in series in the inversion mode operation as shown in Figure 5.15 (b). The layout of the varactor transistor has n number of multi-fingers in our design. Since the number of conducting paths due to the soft breakdown is a statistical phenomenon, we consider the following conditions: some m fingers out of total n are broken over time. And R is the resistance parallel to a breakdown finger, R_{mos} is the channel resistance, and R_s is the resistance in series with the inductor L due to its finite quality factor. The frequency of oscillation is determined by the inductance in the tank and the total equivalent capacitance in the tank that includes the capacitance $C_{gg,N}$ from the active transistors of the diff pair. Therefore, the LC tank can be modeled by Figure 5.16 (a). Through the impedance transformation, the equivalent tank is obtained in Figure 5.16 (b).



(a)



(b)



Figure 5.15: (a) Simulated C-V curve for NMOS varactor @ D=S=B, (b) Simulated C-V curve for the inversion NMOS varactor, and (c) the capacitance versus V_g for different V_{ctr} for an inversion NMOS varactor.



Figure 5.16: (a) LC tank and (b) its equivalent circuit

The equivalent parallel resistance of the LC tank including the parasitics from the active transistors is

$$R_{eq} = R_C \left\| R_L \right\| \left(2/g_{ds} \right) \tag{5.30}$$

where R_C is the equivalent parallel resistance of the varactor and is equal to

$$R_{C} = \frac{\left[R_{mos}\left(m^{2} + \omega^{2}R^{2}C_{gg}^{2}\right) + mR\right]^{2} + \omega^{2}R^{4}C_{gg}^{2}}{\omega^{2}R^{2}C_{gg}\left[R_{mos}\left(m^{2} + \omega^{2}R^{2}C_{gg}^{2}\right) + mR\right]}$$

$$\cdot \frac{2\omega^{2}R^{2}C_{gg}}{m^{2} + \omega^{2}R^{2}C_{gg}^{2}}$$
(5.31)

and R_L is the parallel resistance for the inductor given by

$$R_{L} = R_{S} + \frac{\omega^{2} L^{2}}{R_{S}} \,. \tag{5.32}$$

As the number of breakdown fingers increases, the oscillator operates in the current limited region, the equivalent tank resistance decreases reducing the amplitude of oscillation according to (5.25).

5.3.3 Large-signal Analysis

An oscillator requires its amplitude to be as large as possible to keep the phase noise low and provide a good local oscillator (LO) signal to a subsequent mixer stage. Therefore, in an LC oscillator, the signal swing across the varactor is large. As a result, the instantaneous value of the varactor capacitance changes throughout the signal swing across it. The effective capacitance seen by the large-signal LC tank is the weighted average of the instantaneous capacitance for a complete cycle of the signal. The average large signal capacitance is derived as [69]:

$$C_{AVG} = \frac{\omega_0}{\pi} \int_0^{\frac{2\pi}{\omega_0}} C[v(t)] \cos^2(\omega_0 t) dt$$
(5.33)

where $v(t) = V_m sin(\omega_0 t) + V_{GS} + V_{ctr}$ is the oscillation signal and C[v(t)] is the small-signal capacitance according to the *C-V* characteristics in Figure 5.15. The value of C_{AVG} is solved numerically [69]. In this work, the average capacitance is obtained for an inversion mode varactor. As shown in Figure 5.15 (c), the instantaneous capacitance C[v(t)] swings between

 C_{max} when $V_g > (V_{th} + V_{ctr})$ and C_{min} when $V_g < (V_{th} + V_{ctr})$. Therefore, the tuning characteristic can be assumed a stair case and the expression for C_{AVG} is obtained

$$C_{AVG} = \frac{2}{T} \int_{t_1}^{T+t_1} C_{\max} \cos^2\left(\frac{2\pi}{T}t\right) dt -\frac{2}{T} \int_{\frac{T}{2}-t_1}^{T+t_1} \left(C_{\max} - C_{\min}\right) \cos^2\left(\frac{2\pi}{T}t\right) dt$$
(5.34)

where, $t_1 = \frac{T}{2\pi} \sin^{-1} \left[\frac{V_{th} - V_g + V_{ctr}}{V_m} \right].$

The large-signal *C*-*V* curves of an inversion mode varactor for different amplitudes of oscillation are given in Figure 5.17 using (5.34) with T = 0.42 ns, $V_{th} = 0.5 \text{ V}$, $V_{ctr} = 0.5 \text{ V}$, $C_{max} = 50 \text{ fF}$, and $C_{min} = 20 \text{ fF}$ for an inversion mode varactor with the transistor channel width of 50 µm and the channel length of 0.16 µm.



Figure 5.17: C-V curves for an inversion mode varactor for different signal amplitudes



Figure 5.18: Simulated capacitance versus gate-source voltage

As seen in Figure 5.18 the average gate capacitance is fairly constant over a wide range of gate-source voltages. Therefore, the total capacitance of the LC tank is $C = C_{AVG} \left\| \left(C_{gg,N} / 2 \right) \right\|$. Now, the frequency of oscillation is calculated analytically using (5.21).

The frequency drift for an LC oscillator is caused by two mechanisms. First, the degradation of amplitude due to the gate oxide BD of the varactor transistors cause the effective average capacitance to change; whether the capacitance will increase or decrease depends on the gate bias voltage V_G and V_{ctr} according to Figure 5.17. Second, the small-signal capacitance of the varactor is reduced for some internal mechanisms as observed in measurements shown in Figure 5.8.

As the hardness of breakdown increases, the breakdown spot resistance is reduced to few $k\Omega$, as a result, the amplitude decreases. A 2.4 GHz LC oscillator has been designed and simulated using an inversion type varactor. The varactor transistors have five fingers with 50 µm in width and 0.16 µm in length (the size of the measured devices) each. For SpectreRF

simulation in Cadence, a 10 k Ω breakdown spot resistance is assumed for each broken finger. BSIM3 model parameters extracted from the measured data are used in the simulation. The amplitude of the oscillator has been evaluated with the different numbers of fingers experiencing hard BD using the analytical models in (5.25) and (5.30)-(5.32) and by computer simulation. The simulation and analytical results for the amplitude of oscillation are shown in Figure 5.19. Good agreement between the model predictions and SpectreRF simulation is obtained.



Figure 5.19: Amplitude of oscillation versus number of finger breakdown in varactor. Shaded: SpectreRF simulation, black: analytical.

5.3.4 Oscillator Phase Noise

The mechanisms for phase noise have been analyzed in [71-72]. The phase noise of an LC oscillator at an offset frequency of ω_m from the frequency of oscillation ω_0 normalized with respect to the carrier is given by

$$\Im(\omega_m) = 10 \log\left[\frac{4kTFR_{LC}}{V_m^2} \cdot \left(\frac{\omega_0}{2Q\omega_m}\right)^2\right]$$
(5.35)

where $F = 2 + \frac{8\gamma R_{eq}I_{tail}}{\pi V_m} + \gamma \frac{8}{9}g_{mbias}R_{eq}$. The three terms in F account for thermal noise for the

tank resistance, the differential pair, and the tail current source, respectively. $R_{LC} = R_C ||R_L|$ is the equivalent resistance of the resonator tank. The loaded quality factor Q depends on the inductors and the capacitors. In CMOS technology on-chip inductors have low quality factor and usually dominates in overall quality factor. However, as we have seen the quality of the varactor can degrade significantly as the transistors experience BD. Also, as the amplitude of oscillation degrades as the gate oxide BD progresses, the phase noise of the oscillator increases. Figure 5.20 shows the phase noise of the oscillator for different numbers of varactor transistor finger experiencing breakdown, where solid lines show SpectreRF simulation results and discrete points are calculated using (5.35). Since we have used ideal current source during the simulation of the oscillator, we ignored the noise coming from the tail current source in our calculation. There is a good agreement between the simulation results and the model prediction. At a given offset frequency, the higher the number of finger breakdown, the higher the phase noise of the oscillator.

5.3.5 Design of LC Oscillator in Reliability

As discussed in the previous sections, the performance degradation of an LC oscillator occurs mainly through two mechanisms. First, the combined HC and BD cause the transistors in the differential pair to degrade. Second, due to the BD, the varactor quality factor degrades resulting in a reduced amplitude of oscillation at the output. The reduction in amplitude increases the phase noise and drifts the frequency of oscillation. The root cause for HC and BD is high drain and gate voltages.



Figure 5.20: Normalized phase noise of the oscillator versus offset frequency.

While designing an LC oscillator, one can select a small g_m to provide the required negative resistance for a sustained oscillation and to keep the power consumption low. When the transistors degrade due to combined HC and BD effects, g_m could be below the critical value of g_{m0} , the circuit will stop oscillating. To avoid such a disaster, therefore, circuit designers need to select a design margin such that $g_m = g_{m,margin} + g_{m0}$. For a given gate bias, the gate oxide breakdown in a varactor may be prevented or reduced by keeping the control voltage V_{ctr} comparatively high with a reduced tuning range of the VCO inside a phase locked loop.

To reduce or eliminate the HC and gate oxide BD effects, a different LC oscillator structure with a cascoded structure is proposed as shown in Figure 5.21. In this structure, both NMOS and PMOS transistors are used to synthesize the negative resistance required for a sustained oscillation. It offers high transconductance for a given tail current, fast settling time, and small $1/f^3$ noise corner [38].



Figure 5.21: Complementary LC oscillator

The output common mode voltage of the complementary oscillator can be set by changing relative sizes of NMOS and PMOS transistors. This is especially helpful to set the common mode voltage at the LO input of a mixer. Circuit designers can utilize the freedom to set
the DC bias point of the output at a given voltage that optimizes between circuit performance and reliability. Obviously, a lower output DC bias voltage provides less probability of HC and BD at the expense of smaller output voltage swing and higher phase noise. For example, if the output DC bias voltage is set at $V_{DD}/2$, the varactor experiences a maximum DC voltage of $V_{DD}/2$ across its gate to source (with $V_{crr} = 0$) and the maximum instantaneous voltage swing of V_{DD} . Therefore, a much smaller electric stress appears on a varactor compared to that of an NMOS only the oscillator and the transistors at the differential pair experience the DC drain to source voltage of $V_{DD}/2$. Although the DC voltage is reduced 50 % in this example compared to that in the NMOS oscillator, the likelihood of HC or BD events is reduced significantly. In the complementary oscillator, the highest achievable amplitude is 50 % lower and the phase noise is 6 dB inferior to that of the NMOS oscillator. In the current limited region, these two structures are comparable in performance, but the complementary structure provides great immunity against the HC and BD degradation.

The expression for the tank amplitude of this oscillator is same as that of the NMOS only structure in the current limited region. The maximum voltage swing in the positive direction is limited by the supply voltage and in the negative direction by the voltage when the tail current source turns off. For a complementary oscillator, the equivalent tank resistance is $R_{LC} \| (2/g_{ds,N}) \| (2/g_{ds,P}) \|$ and the total capacitance seen at the tank is $C = C_{AVG} \| (C_{gg,N}/2) \| (C_{gg,P}/2)$. R_{LC} and C_{AVG} have the same expressions as that of the NMOS only model. By selecting the gate voltage bias equal to $V_{th} + V_{ctr}$, the average capacitance can be made independent of the signal amplitude.

5.4 Reliability Analysis of a Passive Mixer

On wafer 0.16 µm NMOS transistors are stressed and measured. Soft breakdown effects on MOS switch and passive mixer are evaluated. Time constant for the switch increases. Conversion gain and LO feed-through of the mixer degraded.

MOS switch is widely used in switch capacitor circuits. It also has applications in multiplexing, modulation and mixing circuits. While circuit designers tend to use larger gate voltage for better performance of the switch, associated vertical electric field increases the probability of soft gate oxide breakdown in deep sub-micrometer transistors. It is our understanding that this is the first reporting of the effects of soft breakdown on MOS switch and switch based passive mixer. This effort will help the circuit designers to prepare for potential performance degradation of the switch based circuits.

5.1 MOS Switch

A step pulse at the gate of a MOS switch [74] is applied for simulation as in Figure 5.24. A model for the switch is proposed in Figure 5.25 that accounts for the finite gate oxide resistance of the transistor.

Channel on-resistance of a switch is given by (5.29). If the channel resistance is R_{ON} , then time constant is given by:

$$\tau = R_{ON}C_L \,. \tag{5.36}$$

The increase in V_{th} and decrease in μ for soft breakdown stress cause the on-resistance of the switch to increase according to (5.29). Therefore, time required to charge the load capacitance also increases according to (5.36) and can be verified by transient simulation results

in Figure 5.26. Time constant with a fresh device is 87.2 ps and with a stressed device it is 95.8 ps (increase of 10%).



Figure 5.24: Simulation setup for MOS switch



Figure 5.25: Model for MOS switch

5.2 Passive Mixer

A MOS switch based balanced passive mixer [30-31] similar to Figure 3.23 has been used for simulation for reliability analysis. The simulation results of the designed mixer are

given in Figures 5.27-29. The curves with marking 'x' are with fresh transistor model and ' Δ ' with soft gate oxide stressed model. After soft breakdown, conversion gain of the mixer has degraded by 4%, LO feed-through by 4 dB. However, noise figure remains almost unchanged



Figure 5.26: Voltage across load capacitance versus time



Figure 5.27: Conversion gain versus frequency







Figure 5.29: Noise figure versus frequency

CHAPTER 6: SUMMARY

6.1 Achievements

In this dissertation a sensor node 'AccuMicroMotion' is proposed for detecting micro motion with high resolution for physiological activity monitoring application. The proposed system is outlined and the interface and transmitter circuits are designed in a 0.35 µm CMOS process and simulated in Cadence environment using Spectre simulator. Also, CMOS RF circuit reliability issues are discussed and analyzed through device measurements and circuit simulations. Achievements of this research can be summarized as following:

- A sensor node 'AccuMicroMotion' is proposed that has the ability to detect motion in 6 degrees of freedom for the application of physiological activity monitoring which is expected to be light weight, low power, small and cheap. The 'AccuMicroMotion' sensor node may collect and transmit the movement and vibration signals wirelessly to a nearby base station while attached to or implanted inside human body. The device may have useful applications in medical diagnosis, physical therapy, sports or fitness.
- A system to implement the 'AccuMicroMotion' sensor node is proposed. This dissertation provides detail design and analysis of relevant electronic circuits for a system on a single chip implementation using traditional CMOS process.
- A Study of MEMS vibration sensors in terms of mechanical-electrical interface is presented. Although the design of MEMS transducers is not the focus of this research, the circuit design and transducer design needs to be corroborated.

4. The CMOS circuits for the 'AccuMicroMotion' interface and transmitter are designed. The CMOS circuit architecture provides a dynamic range of 60 dB and can operate for more than 50 hours from a single coin cell battery. The designed interface circuit can resolve a DC to 1 KHz and as low as 200 nV signal from a sensor. After low pass filtering, the base band signal is digitized using a 10-bit successive approximation register analog to digital converter. Digitized outputs from up to nine sensors can be combined in a parallel to serial converter to be transmitted by a 900 MHz RF transmitter that operates in amplitude shift keying (ASK) modulation technique. The transmitter delivers 2.2 mW power to a 50 Ω antenna. Transmitting signals from 6 sensors will keep the PA turned off for 1/3 of the time. If the digital bit-stream has equal probability of being logic '1' or '0', The system consumes an average current of 4.8 mA (Table 6.1) from a 3V supply when 6 sensors are in operation. Therefore, total power consumption is 15 mW.

Circuit	Comment	Current (mA)
Interface circuit	$@250 \ \mu A$ for each, total 6	1.5
ADC	$@$ 100 μ A for each, total 6	0.6
Transmitter	PA is on for 33% time	2.7
Total		4.8

Table 6.1: Summary of Average Current Consumption

5. As the CMOS technology is scaling, the probability and extent of hot carrier and gate oxide breakdown increases. A methodology is developed that applies accelerated electrical stress on MOS devices to extract BSIM3 models and RF parameters through measurements to perform comprehensive study and analysis of several analog and RF circuits under hot carrier and breakdown degradation.

6.2 Future Work

- Due to resource constraints the 'AccuMicroMotion' sensor is not implemented on silicon. As a result, it should be exciting to verify the simulated results with experimental results. A detail design and analysis is provided in this dissertation that will guide the implementation.
- Sensor offset cancellation through auto-calibration can be investigated. Each sensor can be under calibration mode each time it is turned on; the sensor offset can be calculated and a correction signal can be stored to apply for auto-calibration.
- Adding a receiver to the system for interactive communication between the 'AccuMicroMotion' sensor and the base station. The interactive communications can also set up for multiple sensors in a wireless network.

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