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## Intrinsic Modulation Response Modeling and Analysis for Lithographic Vertical-Cavity Surface-Emitting Lasers

Mingxin Li  
*University of Central Florida*

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INTRINSIC MODULATION RESPONSE MODELING  
AND ANALYSIS FOR LITHOGRAPHIC VERTICAL-  
CAVITY SURFACE-EMITTING LASERS

by

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A dissertation submitted in partial fulfillment of the requirements  
for the degree of Doctor of Philosophy  
in the College of Optics and Photonics  
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Orlando, Florida

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## ABSTRACT

Vertical-cavity surface-emitting lasers (VCSELs) have been greatly improved and successfully commercialized over the past few decades owing to their ability to provide both mode and current confinement that enables low energy consumption, high efficiency and high modulation speed. However, further improvement of oxide VCSELs is limited by the nature of the oxide aperture because of self-heating, internal strain and difficulties in precise size control.

In this dissertation, VCSELs using lithographic approach are demonstrated to overcome the limitations of oxide VCSELs, in which an intra-cavity phase shifting mesa is applied to define the device size and provide optical mode and electrical current confinement instead of an oxide aperture. A newly developed model of intrinsic modulation response is proposed and analyzed to focus on the thermal limit of the modulation speed of VCSELs. The results show that both the temperature dependent differential gain and stimulated emission rate impact laser speed and the stimulated emission rate dominates the speed limit. Thermal limits of modulation response are compared for oxide and lithographic VCSELs for various sizes. The results predict that the intrinsic modulation response can be significantly increased by using lithographic VCSELs due to low thermal resistance and reduced mode volume while maintaining high efficiency. The intrinsic bandwidth could exceed 100 GHz for a 2- $\mu\text{m}$ -diameter lithographic VCSEL. Combined with low electrical parasitics, it is expected to produce over 100 Gb/s data rate from a single directly modulated laser. VCSELs designed for high speed are discussed and their characteristics are demonstrated.

To my parents, Jingbo Li and Junmin Xu

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## **LIST OF ACRONYMS/ABBREVIATIONS**

CW	Continuous-Wave
DBR	Distributed Bragg Reflector
EEL	Edge-Emitting Laser
MBE	Molecular Beam Epitaxy
MOCVD	Metalorganic Chemical Vapor Deposition
PCE	Power Conversion Efficiency
QW	Quantum Well
RHEED	Reflection High-Energy Electron Diffraction
RT	Room Temperature
VCSEL	Vertical-Cavity Surface-Emitting Laser

## **CHAPTER 1: INTRODUCTION AND OUTLINE**

Vertical-cavity surface-emitting lasers (VCSELs) have been intensely studied and greatly improved since 1980s due to low energy consumption, circular output beam profile and ease of 2D array formation. Ion implanted VCSELs were the first commercialized ones because of improved reliability. Yet they were quickly surpassed by VCSELs using selective oxidation technologies owing to better mode and current confinement provided by the oxide aperture. Until today, oxide VCSELs still dominate the market. However, as the drastically development of information technologies, superior performance is demanded for VCSELs, especially in high speed communications. However, the oxide aperture introducing self-heating, internal strain and difficulties in precise size control limits VCSELs for achieving even higher performance.

To overcome the limitations of oxide VCSELs, we present a new VCSEL, the lithographic VCSEL, using a lithographically defined intra-cavity phase shifting mesa instead of the oxide aperture. The mesa defines the device aperture and provides optical mode and electrical current confinement. By removing the oxide aperture, lithographic VCSELs inherently enable enhanced heat flow in the junction and eliminate internal strain around the active region. The lithographically defined mesa allows us to achieve good size uniformity and reduce VCSEL size to 1  $\mu\text{m}$ , and it is highly expected to scale the devices down to sub-micron range. Owing to these advantages, lithographic VCSELs have shown significant improvement in L-I-V characteristics and realized highly uniform single mode operation. Lithographic VCSELs are also promising to surpass the oxide VCSELs for higher modulation speed.

The advantages of lithographic VCSELs also promises a higher modulation speed, which leads to the research on designing and modeling for high speed VCSELs. In Chapter 2, an overview of VCSELs is presented. The discovery and development of VCSELs are firstly reviewed and several VCSEL structures using different technologies are introduced. The limitations of oxide VCSELs is then discussed. The basic structure and mode confinement of lithographic VCSELs is presented to overcome the limitations of oxide VCSELs. The growth and fabrication steps are shown at last.

In Chapter 3, a mathematical model of intrinsic modulation response is developed to focus on the thermal limits of VCSEL modulation speed. The intrinsic modulation response can be represented as a transfer function of the changing of the photon density over electron density in frequency domain. The transfer function is derived from a set of two laser rate equations using small signal analysis. The most challenging part is to establish the analytical expression for the differential gain, which is found by calculating the gain and the numbers of electrons and holes in the active region.

The thermal analysis in Chapter 4 shows that both the temperature dependent differential gain and stimulated emission rate impact the laser speed, and the stimulated emission rate plays the limiting role. Thermal limits are presented and compared for oxide and lithographic VCSELs of various sizes. The results predict that the VCSEL's intrinsic bandwidth can be dramatically increased by using device structures with low thermal resistance and reduced mode volume. An over 150 GHz intrinsic bandwidth is predicted for a 1  $\mu\text{m}$  lithographic VCSEL.

Chapter 5 talks about the design of VCSELs for high speed, which basically includes the design of reflecting mirrors, resonant cavity and active region. The key features for increasing

intrinsic and parasitic modulation bandwidth are discussed and demonstrated to show the great potential of lithographic VCSELs for achieving high speed.

Chapter 6 talks about the summary and future work on the lithographic VCSELs.

## CHAPTER 2: OVERVIEW OF VCSELS

### 2.1. Brief review of VCSELS

The vertical-cavity surface-emitting laser (VCSEL) is a type of laser diode which emits laser beam perpendicular to the chip surface. The cavity is formed by two distributed Bragg reflectors (DBRs) and incorporates with multiple quantum wells (QWs) in the active region as the gain medium. The DBRs consist of multiple layers of materials with alternating refractive index with each layer having a quarter wavelength optical length.

In contrast to conventional edge-emitting lasers (EELs) with light emission in a direction parallel with the wafer surface and cavity realized by cleaving individual device out of the wafer, VCSELS have many inherent advantages over EELs such as on-wafer test, easy array formation and circular output beam with small divergence. Figure 2-1 shows a typical VCSEL and EEL structure.

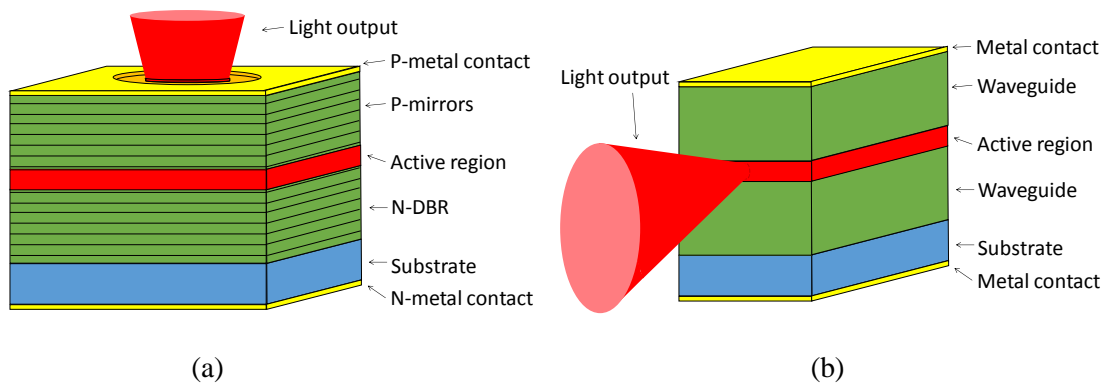


Figure 2-1: Schematic diagrams of (a) a typical VCSEL structure and (b) a typical EEL structure

The idea of VCSEL was firstly proposed by Prof. Kenichi Iga in 1977 and then published in 1979 [1], which incorporated undoped GaInAsP bulk material as active layer with p- and n-



type InP on the sides. The grown surface and the polished n-side substrate served as the resonant mirrors. Metal contacts were deposited on both sides to increase the mirror reflectivity. The device was mounted p-side down and tested under pulse operation at 77 K. Light output came out from the n-side window and the lasing wavelength was 1.18  $\mu\text{m}$  with a threshold current density of 11  $\text{kA/cm}^2$ . Despite of the high threshold current density and low efficiency due to the poor optical and electrical confinement, this innovated design had shown promising characteristics such as two-dimensional (2-D) packaging for arrays. However, Prof. Iga's work did not attracted too much attention until almost ten years later when researchers in Bell Laboratories started to work on optical computing using 2-D arrays of light modulators. Soon the distributed Bragg reflector grown by molecular beam epitaxy (MBE) [2] and quantum-well structures [3] were introduced in VCSELs, which significantly reduced the threshold current. At the same time, Prof. Iga's group continued working in parallel and demonstrated the first VCSEL working under continuous-wave (CW) operation at room temperature in 1989 [4].

VCSEL had been greatly improved by these technologies, but was still not satisfactory. Therefore, better overlap between the optical mode and the gain region are required for further improvement of VCSEL performance. Different designs had been proposed focusing on electrical current and optical mode confinement in the cavity. As shown in Figure 2-2 (a), an air-post VCSEL is formed by a deeply etched mesa [5]. Optical mode is confined through index guiding, i.e., the large refractive index difference between the air and the mesa. However, the current confinement is still weak and the carriers move laterally in the active layer. Another disadvantage of this structure is the roughness of the mesa-air interface, which causes scattering losses of the optical field [6] and may lead to reliability problem.

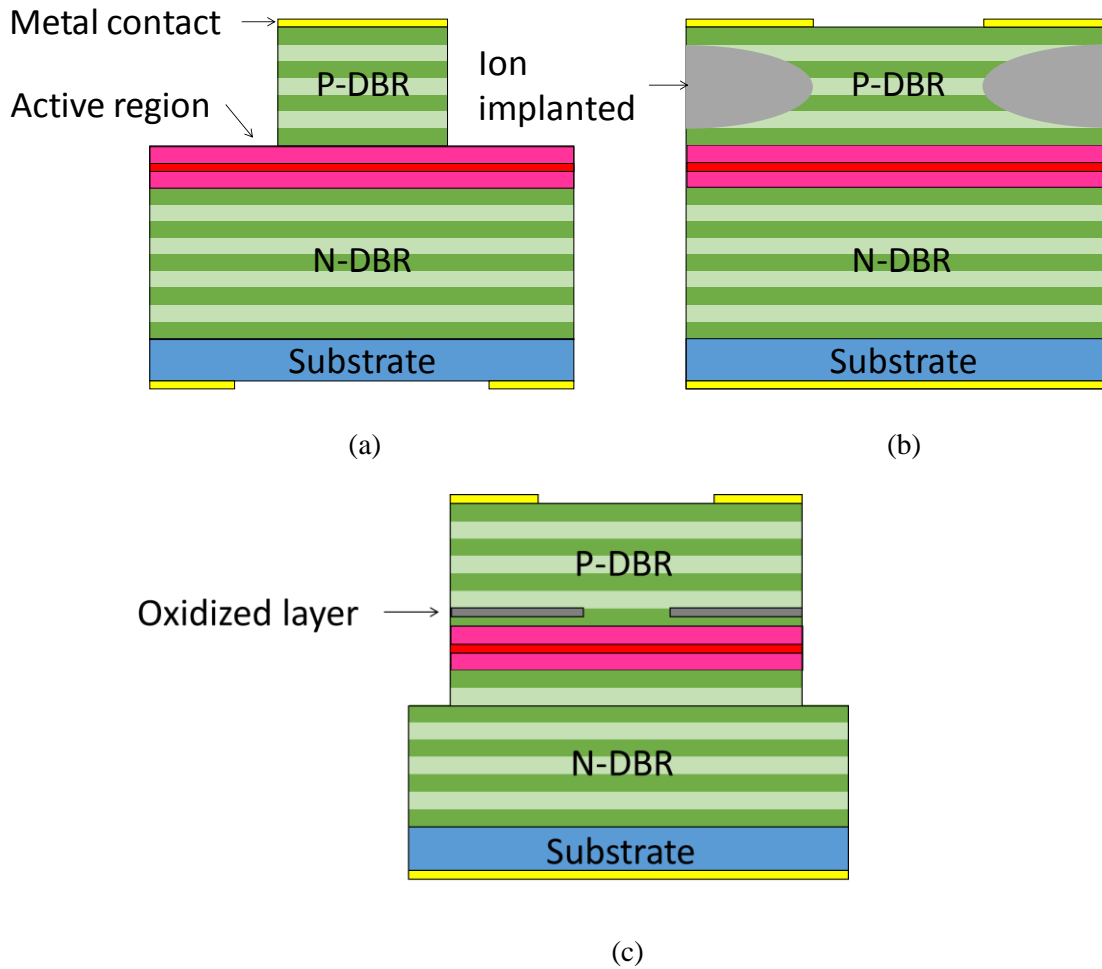


Figure 2-2: Different VCSEL structures: (a) Air-post VCSEL, (b) Ion implanted VCSEL and (c) Oxide-confined VCSEL

Figure 2-2 (b) shows the structure of ion implanted VCSELs. The ion implantation (primarily proton implantation) creates highly resistive regions under the metal contact and forces current flow through the aperture, thus providing current confinement [7, 8]. The optical confinement is provided by thermal lensing effect coming from the variation of refractive index in lateral direction due to temperature distribution. Owing to its easy manufacturability and high reliability, the proton implanted VCSEL has been the first commercialized structure in mid-

1990s. However, the insufficient mode confinement by thermal lensing effect causes low efficiency and high threshold current. Besides, the difficulties in size control leads to variation of device performance.

The discovery of selective oxidation for high Al-content III-V semiconductors by Prof. Nick Holonyak's group [9] has made a major impact on most of today's VCSELs. The implementation of selective oxidation into VCSELs was firstly presented in 1994 by Prof. Deppe's group [10] and makes oxide confined VCSELs shown in Figure 2-2 (c) the most successful and widely commercialized structure since late 1990s due to their extremely low threshold current [11, 12], high power conversion efficiency [13, 14] and high modulation speed [15, 16]. The high performance comes from better confinement of current and optical mode because the oxide layer is an insulator so that current has to flow through the aperture and the refractive index difference of the oxide ( $\sim 1.7$ ) and III-V semiconductor ( $\sim 3.0$ ) is large enough for sufficient index guiding.

## 2.2. Limitations of oxide VCSELs

Oxide VCSELs have been intensely studied and drastically improved ever since the first demonstration and thus become the primary optical sources in many applications especially for high speed communication. However, the nature of the oxide layer is becoming the limitation of the VCSELs for achieving smaller sizes, superior reliability and higher speed.

The oxidation is a diffusion process in which the high Al content AlGaAs layer is oxidized laterally from outer rim of the mesa to inner aperture termination in hot water vapor ambient. The geometry and size of the oxide aperture is strongly dependent on many conditions

such as the furnace temperature, water vapor flux, and oxidation rate of the material, which make it difficult for precise control of the aperture size since any variation in the process results in the size deviation throughout a single wafer. It has been shown that there is at least 1  $\mu\text{m}$  size variation even in well-developed manufacture process [17]. VCSEL performance is strongly dependent on its aperture size and this size variation greatly limits the reproducibility of small devices, making it almost impossible for uniform production of one micron or sub-micron size VCSELs.

Another drawback is the point defect and dislocations generated at the termination of oxide aperture during oxidation process that causes internal strain between the oxide and the semiconductor. The strain becomes more severe at elevated internal temperature due to different thermal expansion of the oxide and III-V material. Thus defect propagation is produced into active region and degrades VCSEL reliability, eventually causes device failure.

Additionally, the low thermal conductivity of oxide layer makes it a thermal block that prevents efficient heat spreading from the device. As the bias current increases, heat is accumulated around the active region and leads to a rapid rise of the junction temperature. As a result, the stimulated emission rate and the output power are easily saturated at high bias current. We will show in the following chapters that the early saturation of stimulated emission rate notably limits the maximum modulation bandwidth of oxide VCSELs.

### 2.3. Lithographic VCSELs

Due the fact that oxide VCSELs have severe limitations in reliability and manufacturability, especially for small size devices, a novel VCSEL technology is highly

desirable for easy size scaling while maintaining high efficiency and reliability. The idea of all-epitaxial lithographically-defined VCSEL was proposed through eliminating the oxide layer and was firstly demonstrated in 2004 [18]. After over a decade of study and development, the lithographic VCSELs have shown comparable or even better static characteristics and huge potential to produce better dynamic performance comparing to oxide VCSELs.

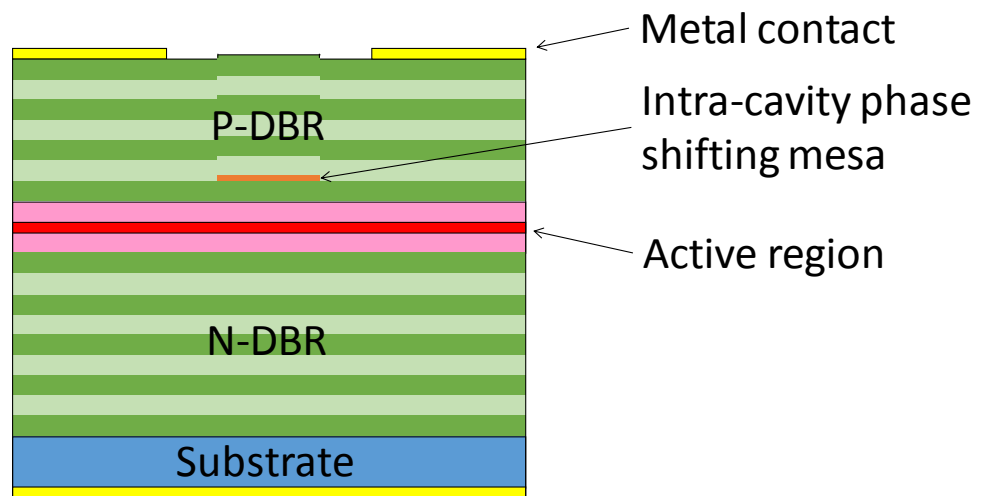


Figure 2-3: Schematic diagram of a lithographic VCSEL.

As shown in Figure 2-3, the basic structure of a lithographic VCSEL is similar to an oxide VCSEL. The major difference is the lithographically defined intra-cavity phase shifting mesa above the active region instead of an oxide aperture. The phase shifting mesa defines the device size and provides both optical mode and electrical current confinement at the same time.

The lithographically defined phase shift mesa is independent from the way how it is processed and thus allows for easy and precise size control of the device. Good device uniformity can be realized across large wafers, especially for small size devices [19, 20]. The internal strain caused by point defects and dislocations is simply eliminated without the oxide layer, which greatly reduces the reliability problems. The heat spreading is significantly

improved due to the removal of the heat barrier and thus a smaller thermal resistance is achieved [21].

#### 2.4. Mode confinement

Figure 2-4 shows schematically how the intra-cavity phase shifting mesa confines mode in the cavity. The resonance cavity is divided into two regions which are “on mesa” region defined by the phase shifting mesa where  $r \leq \frac{W}{2}$  and “off mesa” region where  $r > \frac{W}{2}$ . The cavity lengths of the two regions are  $L_0$  and  $L_1$ , respectively and  $L_0 > L_1$ . When electrically biased, the device will have both lasing mode and waveguide mode resonating in on mesa and off mesa region. Note that the lasing mode size  $W_0$  can be different from the mesa size  $W$ . The placement of the mesa and mesa height has to be carefully designed to provide mode confinement and scattering loss control.

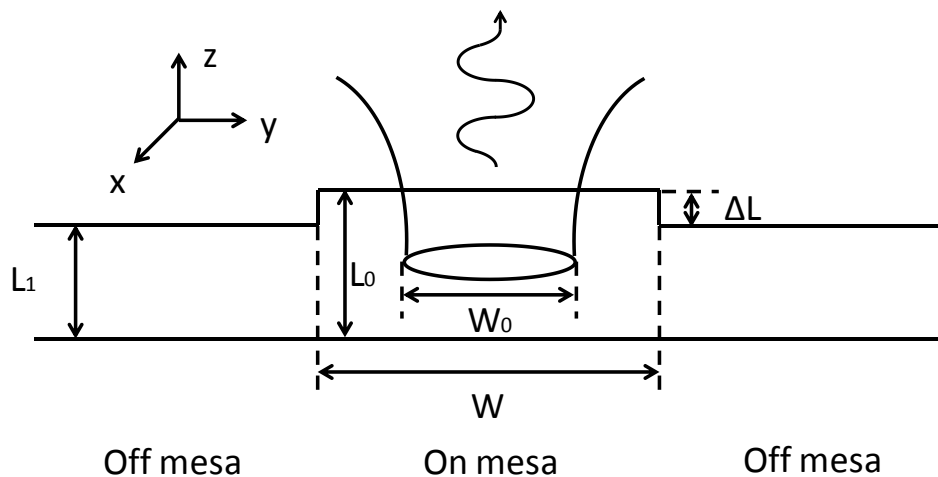


Figure 2-4: Schematic diagram of an optical cavity with intra-cavity phase shifting mesa

The standing waves existing in the cavity must be normal to the reflectors and satisfy the conditions given below

$$k_{z,0} = \frac{\pi}{L_0 \sqrt{\varepsilon}} m_z, \quad (2.1)$$

$$k_{z,1} = \frac{\pi}{L_1 \sqrt{\varepsilon}} m_z, \quad (2.2)$$

where  $k_{z,0}$  and  $k_{z,1}$  are the wave vectors of the modes in on and off mesa regions perpendicular to the reflectors, respectively.  $m_z$  is a positive integer and  $\varepsilon$  is the permittivity of the cavity.

In cylindrical coordinates, the wave vector can be written as

$$k_0 = \frac{\omega_0}{c} = \sqrt{k_\rho^2 + k_z^2}, \quad (2.3)$$

where  $k_\rho$  is the wave vector component in lateral direction (x-y plane),  $\omega$  is the angular frequency and  $c$  is the speed of light in free space. Considering that the solution to the field profile of the fundamental mode in a cylindrical region can take the form of Bessel function of the first kind, the lateral component of the wave vector in on mesa region can be written approximately as

$$k_{\rho,0} = \frac{4.81^2}{\varepsilon W_0^2}. \quad (2.4)$$

Therefore, the relation between the modes in on and off mesa regions can be found by

$$\frac{\omega_o}{c} = \sqrt{\frac{4.81^2}{\varepsilon W_0^2} + k_{z,0}^2} = \sqrt{k_{\rho,1}^2 + k_{z,1}^2}. \quad (2.5)$$

According to Equation (2.1), (2.2) and  $L_0 > L_1$ , the normal wave vector in on mesa region is smaller than that in off mesa region for the same mode number, i.e.  $k_{z,0} < k_{z,1}$ . If the

mode size  $W_0$  is large enough, the wave vector  $k_{\rho 10}$  has to be imaginary to make Equation (2.5) valid, which indicates that the mode in off mesa region becomes evanescent wave and the optical mode is thus confined in on mesa region [22], given as

$$W_0 \geq \frac{4.81}{\pi} \sqrt{\left(\frac{1}{L_1^2} - \frac{1}{L_0^2}\right)^{-1}}. \quad (2.6)$$

It can be shown that the mode confinement is enhancing with the increase of the mesa height  $\Delta L$ .

The introduction of the phase shifting mesa can eliminate the diffraction loss but causes scattering loss due to non-orthogonality of the longitudinal modes between the on and off mesa regions. However, the scattering loss can be minimized by carefully designing the phase shifting mesa. The scattering loss is set by the normalized overlap of the electrical field  $E_0$  in on mesa region and the electrical field  $E_1$  in the off mesa region [23]:

$$|C|^2 = \frac{\left| \int E_0(z) E_1^*(z) dz \right|^2}{\int E_0(z) E_0^*(z) dz \int E_1(z) E_1^*(z) dz}. \quad (2.7)$$

The scattering loss is a minimum if the mesa height  $\Delta L$  is zero with  $|C|^2 = 1$ , but there is no mode confinement. Non-zero mesa height  $\Delta L > 0$  gives  $|C|^2 < 1$ , which means the scattering loss is increasing with the mesa height. Therefore, a trade-off between the mode confinement and the scattering loss has to be considered for the design of the phase shifting mesa.



## 2.5. Growth and fabrication

The lithographic VCSELs are grown by solid state molecular beam epitaxy on n-type GaAs substrates and require two growths. Figure 2-5 shows a microscopic image of a lithographic VCSEL with p-metal. As shown in Figure 2-6 (a), the first growth starts with 30 pairs of n-type GaAs/AlAs bottom DBR mirrors, followed by a one-wavelength cavity with three 60 Å thick In<sub>0.2</sub>Ga<sub>0.8</sub>As and four 100 Å thick GaAs barriers at the center of it, and ends with the first quarter wavelength of the p-type top mirrors. After pulling out the wafer, the phase shifting mesas are formed by wet etching as shown in Figure 2-6 (b). The mesa diameters vary from 1 μm to 20 μm with good uniformity across the whole wafer. The wafer is then loaded back into the MBE system and outgassed before the regrowth. During the regrowth, shown in Figure 2-6 (c), 14 pairs of p-type GaAs/AlAs top DBR mirrors are grown on the wafer. When the growth is finished, metal contacts are deposited on both sides of the wafer, as shown in Figure 2-6 (d). Finally, isolation is done by a deep wet etching down to the n-type mirrors to separate each individual device on wafer.

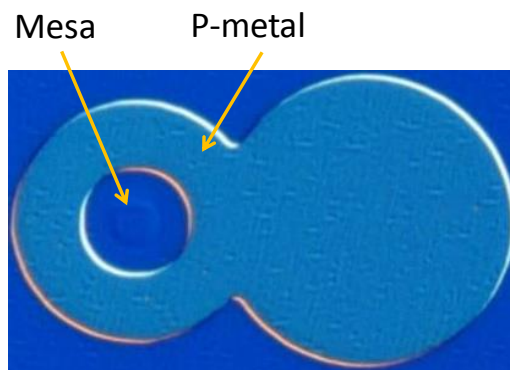


Figure 2-5: Microscopic image of a lithographic VCSEL with p-metal.

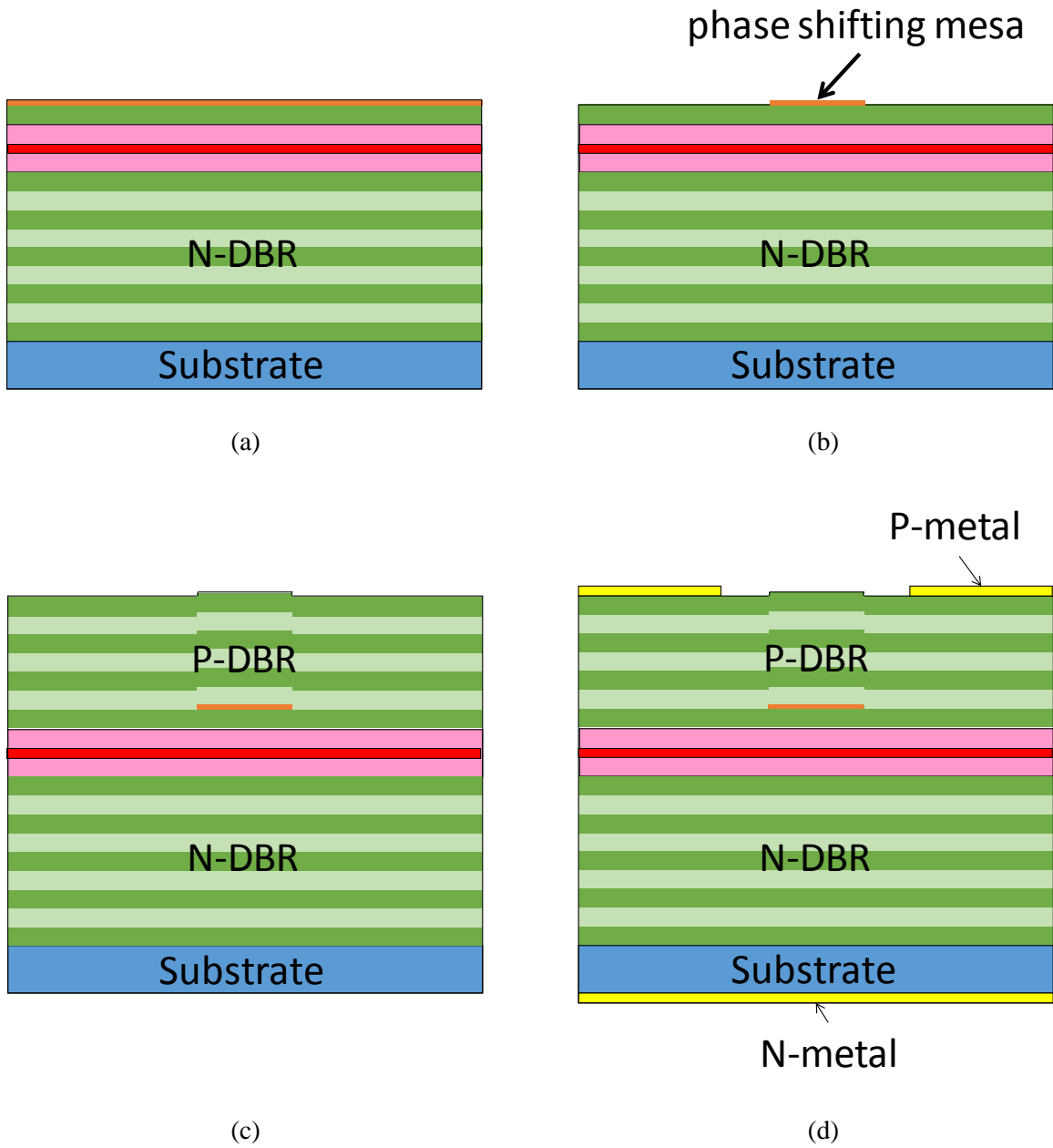


Figure 2-6: Growth and fabrication flow of lithographic VCSELs. (a) First growth; (b) Mesa formation; (c) Regrowth; (d) Metal deposition.

## 2.6. Summary

In this chapter, we have briefly reviewed the development of VCSEL technologies. The most conventional VCSEL structure to date is oxide-confined VCSELs. However, the introduction of the oxide aperture limits VCSELs for higher performance. Here we present a new VCSEL technology using lithographic approach to overcome the limitations of oxide VCSELs. In lithographic VCSELs, an intra-cavity phase-shifting mesa is applied to replace the oxide aperture for both mode and current confinement. The mechanism of optical mode confinement using phase-shifting mesa is addressed. However, the technology for achieving current confinement is proprietary and should not be discussed in this dissertation. We have also shown how the lithographic VCSELs are grown and fabricated. In the next chapter, we will talk about our newly developed model addressing on the thermal limits of intrinsic modulation response of VCSELs for high speed.

### CHAPTER 3: INTRINSIC MODULATION MODEL

The rapid growth of information technologies such as big data and cloud storage demands the next generation photonics electronics technologies to provide huge data transmission rate. Among all kinds of network devices, high speed modulated lasers are highly desirable as the sources of optical signal. To generate intensity modulated optical signals, many approaches have been exploited and the simplest way is direct modulation, which is to modulate the driving current of a laser. As shown in Figure 3-1, the input electrical signal is converted to output optical signal through a laser. The modulated driving current is centered at  $I_0$  and the perturbation of current  $\Delta I$  is very small compared to  $I_0$ . This type of signal modulation is called small signal modulation.

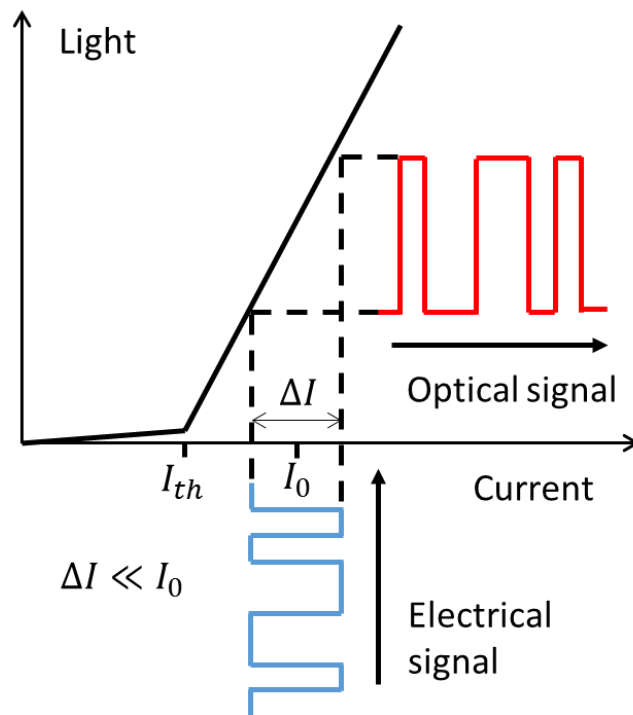


Figure 3-1: Small signal modulation of a directly modulated semiconductor laser.

For electrically pumped semiconductor lasers, the modulation response consists of intrinsic modulation response and parasitic modulation response. Intrinsic modulation response characterizes photon and carrier interactions and is set by the structure of the active region and resonant cavity. Parasitic modulation response is determined by the resistance and capacitance from the epi-layers and metal contacts. In frequency domain, both intrinsic and parasitic modulation response can be represented by a transfer function, respectively, and the total response is the product of both. In this chapter, we will focus on developing a mathematical model to characterize the intrinsic modulation response of VCSELs and then compare the simulation results with experimental results of an oxide VCSEL designed for high speed from published literatures.

### 3.1. Rate equations

A good start point for modeling the intrinsic dynamic behavior of semiconductor lasers is to form a set of two rate equations, one for the number of photons in the cavity and the other one for the number of carriers (electron or hole) in the active region.

For semiconductor lasers, the rate equations can be written as:

$$\frac{dn_m(t, T_J)}{dt} = -\frac{\omega_{c,m}}{Q_m}(T_J)n_m(t, T_J) + g_{st,m}(N_e, T_J)n_m(t, T_J) + g_{sp,m}(N_e, T_J), \quad (3.1)$$

$$\frac{dN_e(t, T_J)}{dt} = \frac{I(t)}{q} - \sum_m [g_{st,m}(N_e, T_J)n_m(t, T_J) + g_{sp,m}(N_e, T_J)], \quad (3.2)$$

where  $n_m$  is the photon number of the m-th mode in the cavity,  $N_e$  is the number of electrons in the active region.  $\omega_{c,m}/Q_m$  is the photon loss rate of the cavity where  $\omega_{c,m}$  is the lasing

frequency in the cavity and  $Q_m$  is the quality factor which is set by the photon lifetime.  $g_{st,m}$  is the gain coefficient corresponding to stimulated emission and  $g_{sp,m}$  is the spontaneous emission coefficient. Note that all these terms are related to the junction temperature  $T_j$ .  $I$  is the injected current into the active region and  $q$  is the charge of an electron. The change of the number of holes is the same as electrons according to charge neutrality, given as

$$N_e(t, T_j) = N_h(t, T_j), \quad (3.3)$$

where  $N_h$  is the number of holes in the active region.

We will show how junction temperature limits laser's intrinsic modulation response and how lithographic VCSELs benefit from low junction temperature due to the removal of the oxide aperture.

### 3.2. Small signal modulation response

The small signal response analysis involves finding the linear frequency response of the rate equations (3.1) and (3.2). Since the coupling between the photons and the carriers is nonlinear, we have to assume that the variation of the injected current is sufficiently small so that the higher order nonlinear terms are negligible.

We assume that the current injected in the active region with small perturbation can be expressed as

$$I(t) = I_0 + \Delta I(t), \quad (3.4)$$

where  $I_0$  is the direct current drive level and  $\Delta I(t)$  is the small perturbation and then we have  $|\Delta I(t)| \ll I_0$ . The resulting numbers of photons and electrons are given by

$$n_m(t) = n_{m,0} + \Delta n_m(t), \quad (3.5)$$

$$N_e(t) = N_{e,0} + \Delta N_e(t). \quad (3.6)$$

Under the assumption of charge neutrality within the active region, the modulation of the holes is the same as the modulation of the electrons.

The material gain  $g_{st,m}$  and  $g_{sp,m}$  are set by the electron and hole quasi-Fermi levels through the number of electrons and  $N_e$  is time dependent, so they are also time dependent and can be written as

$$g_{st,m}(t) = g_{st,m,0} + \frac{dg_{st,m}}{dN_e} \Delta N_e(t), \quad (3.7)$$

$$g_{sp,m}(t) = g_{sp,m,0} + \frac{dg_{sp,m}}{dN_e} \Delta N_e(t), \quad (3.8)$$

where  $\frac{\partial g_{st,m}}{\partial N_e}$  is the differential gain coefficient and  $\frac{\partial g_{sp,m}}{\partial N_e}$  is the differential spontaneous coefficient. Then we can apply equations (3.4) through (3.8) into (3.1) and (3.2) and after neglecting the higher order terms we have

$$\frac{d\Delta n_m(t)}{dt} = -\frac{\omega_{c,m}}{Q_m} \Delta n_m(t) + \frac{dg_{st,m}(N_e)}{dN_e} \Delta N_e n_{m,0}(t) + g_{st,m,0} \Delta n_m(t) + \frac{dg_{sp,m}(N_e)}{dN_e} \Delta N_e, \quad (3.9)$$

$$\frac{dN_e(t)}{dt} = \frac{\Delta I(t)}{q} - \sum_m \left[ \frac{dg_{st,m}(N_e)}{dN_e} \Delta N_e n_{m,0}(t) + g_{st,m,0} \Delta n_m(t) + \frac{dg_{sp,m}(N_e)}{dN_e} \Delta N_e \right]. \quad (3.10)$$

Note that from the steady-state solutions to the rate equations, the time independent terms sum to zero. By applying Fourier transform to equations (3.9) and (3.10) and eliminating the term  $\Delta N_e(\omega)$  we should obtain the expression for the frequency response

$$\left. \frac{\frac{\omega_{c,m}}{Q_m} \Delta n_m(\omega)}{\frac{\Delta I(\omega)}{q}} \right|_{\frac{dg_{st,m}}{dN_e} n_{m,0} \gg \frac{dg_{sp,m}}{dN_e}} \approx \frac{\frac{\omega_{c,m}}{Q_m} \frac{dg_{st,m}}{dN_e} n_{m,0}}{-\omega^2 - i\omega \frac{dg_{st,m}}{dN_e} n_{m,0} + \frac{\omega_{c,m}}{Q_m} \frac{dg_{st,m}}{dN_e} n_{m,0}}. \quad (3.11)$$

Note that we are considering the above threshold situation where the stimulated emission dominates and the spontaneous emission coefficient is negligible and we have used the threshold condition of  $g_{st,m} \cong \omega_{c,m}/Q_m$ . Equation (3.11) illustrates that the frequency response above threshold is set by cavity bandwidth, differential gain and photon number in the active region. The cavity bandwidth is determined by the loss rate  $\omega_c/Q$ , also known as the inverse of photon lifetime, i.e.,  $1/\tau_p$ .

The photon number  $n_{m,0}$  is directly related to the L-I characteristics of VCSELs and can be found by

$$P_{out} = \frac{1}{\tau_p} \eta_{diff} \hbar \omega_c \sum n_{m,0}, \quad (3.12)$$

where  $P_{out}$  is the output power and  $\tau_p$  is the photon lifetime, set by cavity mirror reflectivities.  $\eta_{diff}$  is the differential quantum efficiency corresponding to slope efficiency. For a 985 nm VCSEL with 0.8 W/A slope efficiency, the differential quantum efficiency is 63.5%.



### 3.3. Differential gain

#### 3.3.1 Electronic structure

In order to calculate the differential gain  $\frac{\partial g_{st,m}}{\partial N_e}$  of a VCSEL, we need to find out the electronic structure in the quantum well, which is illustrated in Figure 3-2.

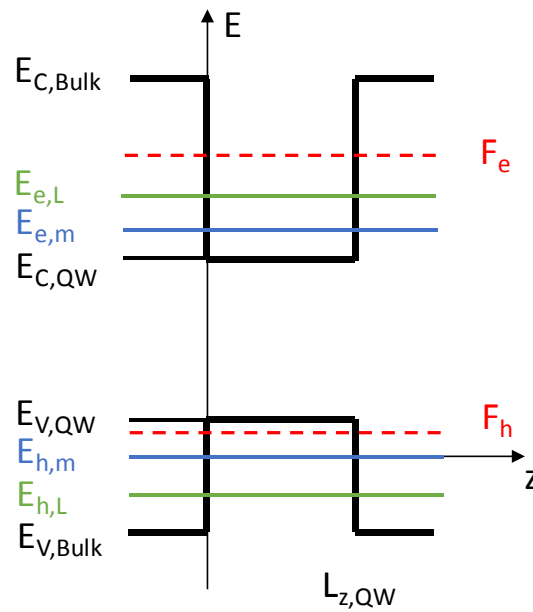


Figure 3-2: Schematic electronic structure of a finite quantum well.

When an atom absorbs or emits a photon, the transition acquires momentum and thus momentum conservation as well as energy conservation should be satisfied, from which we have

$$E_{e,L} = E_{e,m} + \frac{\hbar^2 k_{e,m}^2}{2m_e}, \quad (3.13)$$

$$E_{h,L} = E_{h,m} + \frac{\hbar^2 k_{h,m}^2}{2m_{h,m}}, \quad (3.14)$$

$$k_{e,m} - k_{h,m} = k_{photon,m}, \quad (3.15)$$

where  $E_{e,L}$  and  $E_{h,L}$  are cavity lasing transition energies,  $E_{e,m}$  and  $E_{h,m}$  are the m-th sub-band energies.  $k_{e,m}$ ,  $k_{h,m}$  and  $k_{photon,m}$  are the momentums of the electron, hole and photon, respectively. On a relative scale, the photon momentum is so small relative to the electron and hole momentums being summed over, so we can assume that  $k_{photon,m} \cong 0$  or  $k_{e,m} \cong k_{h,m}$ .  $E_{C,QW}$  and  $E_{V,QW}$  in Figure 3-2 are the energy levels of the conduction and valence band edge of the quantum wells.  $E_{C,Bulk}$  and  $E_{V,Bulk}$  are the energy levels of the conduction and valence band edge of the bulk material for confining the quantum wells.  $m_e$  and  $m_{h,m}$  are the effective masses of electrons and holes in the quantum wells. It is known that the heavy- and light-hole valence bands can be split in strained quantum wells. Different hole valence bands have different band edges with a different effective mass. For light-hole sub-bands, they are spaced further apart because of the lighter effective mass and thus have fewer holes occupied. Therefore in our model we will focus on heavy-holes since they are dominant in the optical transitions.

The effective electron mass and energy levels of the conduction band and valence band edge of the bulk material can be found in literature [24-26]. The effective hole masses and energy separation of heavy-holes sub-bands can be found by using the spherical approximation in strained-layer quantum wells [27]. Then the values of  $E_{e,L}$  and  $E_{h,L}$  can be calculated by

$$E_{e,L} = E_{e,m} + \frac{m_{r,m}}{m_e} (E_L - E_{QW}), \quad (3.16)$$

$$E_{h,L} = E_{h,m} + \frac{m_{r,m}}{m_{h,m}} (E_L - E_{QW}), \quad (3.17)$$

where  $m_{r,m}$  is the reduced effective mass of an electron and hole pair and is calculated as  $\frac{1}{m_{r,m}} = \frac{1}{m_e} + \frac{1}{m_{h,m}}$ .  $E_L$  and  $E_{QW}$  are temperature dependent lasing transition energy  $E_{e,L} - E_{h,L}$  and quantum well sub-band energy gap  $E_{e,m} - E_{h,m}$ , respectively, which can be calculated by the following empirical formulas

$$\lambda_L(T_J) = \lambda_{L,0} + \frac{d\lambda_L}{dT_J}(T_J - T_{J,0}), \quad (3.18)$$

$$\lambda_{QW}(T_J) = \lambda_{QW,0} + \frac{d\lambda_{QW}}{dT_J}(T_J - T_{J,0}), \quad (3.19)$$

where  $\lambda_L$  and  $\lambda_{QW}$  are the wavelengths corresponding to lasing transition energy  $E_L$  and quantum well sub-band energy gap  $E_{QW}$ , respectively.  $\lambda_{L,0}$  is 985 nm, the resonance wavelength of our designed cavity, and  $\lambda_{QW,0}$  is 965 nm, corresponding to the bandgap of the quantum well material.  $\frac{d\lambda_L}{dT_J}$  and  $\frac{d\lambda_{QW}}{dT_J}$  are 0.07 nm/K and 0.28 nm/K, respectively [28].  $T_{J,0}$  is 293 K.

### 3.3.2 Junction temperature

As the drive current is increasing, the junction temperature rises due to the self-heating in the device. Self-heating can be attributed to a range of sources, such as the dissipated power in the resistive elements, leakage current and non-radiative recombination. For well-designed VCSELs, the dissipated power is the main cause for the elevated junction temperature and can be written as

$$\Delta P_D = P_{in} - P_{out}. \quad (3.20)$$

The relation between the dissipated power and the increased temperature in the junction can be characterized by thermal resistance, which is defined as

$$R_{th} = \frac{\Delta T}{\Delta P_D} = \frac{\Delta \lambda / \Delta P_D}{\Delta \lambda / \Delta T}, \quad (3.21)$$

where  $\Delta T$  is the temperature rise in the junction and  $\Delta \lambda$  is the lasing wavelength shift corresponding to the temperature change. For GaAs/AlGaAs materials, the wavelength shift with temperature  $\Delta \lambda / \Delta T$  is 0.07 nm/K.  $\Delta \lambda / \Delta P_D$  can be found by plotting lasing wavelength vs. dissipated power shown in Figure 3-3. Thus the thermal resistance when given can be used to determine the bias current dependence on junction temperature. For a 4  $\mu\text{m}$  diameter lithographic VCSEL, the thermal resistance is found to be 1.81 K/mW.

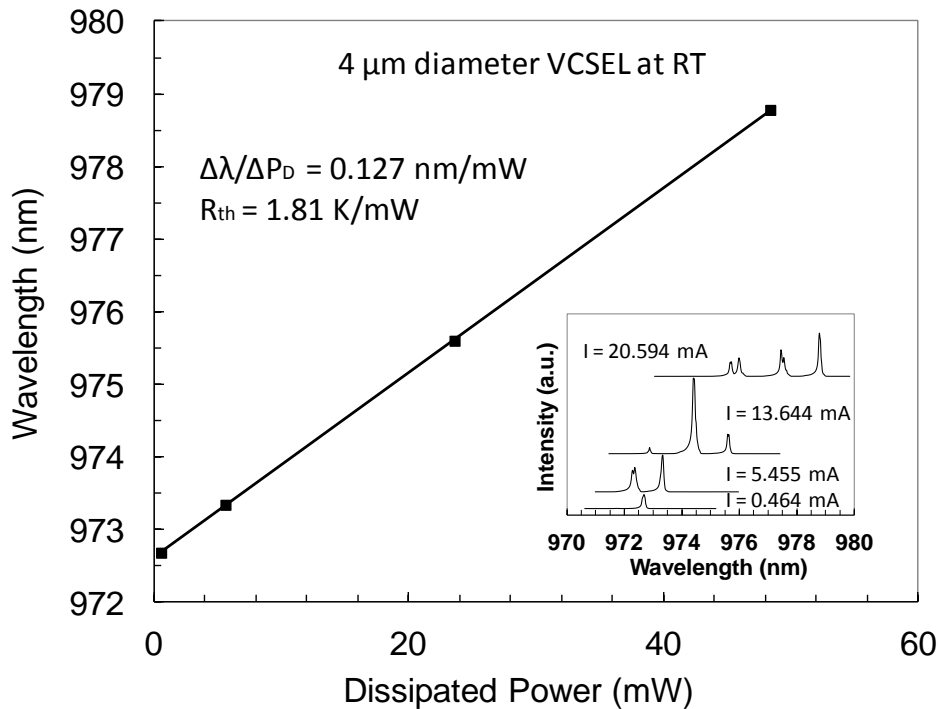


Figure 3-3: Lasing wavelength shifts vs. dissipated power for a 4  $\mu\text{m}$  diameter lithographic VCSEL. Inset:

Red shift of lasing wavelength with increasing current.

Using Equation (3.21), the temperature rise of a device can be calculated from its L-I-V characteristics, and the junction temperature can be found by

$$T_j = T_{stage} + \Delta T. \quad (3.22)$$

Figure 3-4 shows the thermal resistance for various sizes of lithographic VCSELs, compared with oxide VCSELs designed for achieving high speed modulation with low thermal resistance [15, 29]. The measurements of the lithographic VCSELs were performed without any heatsinking and demonstrate a significant reduction of thermal resistance due to better heat spreading in the active region and p-type structure, which makes lithographic VCSELs good candidate for achieving higher output power and faster modulation speed.

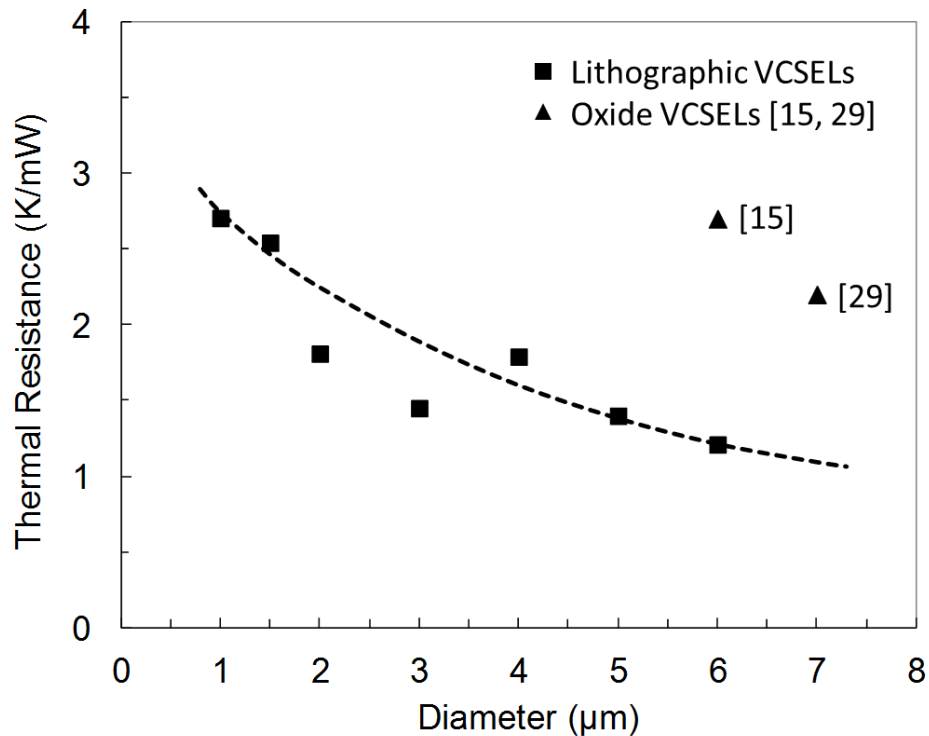


Figure 3-4: Comparison of the thermal resistance of lithographic and oxide VCSELs designed for high speed for various sizes.

### 3.3.3 Gain coefficient

Considering the device biased above lasing threshold, the gain coefficient  $g_{st,m}$  is determined by the electron and hole quasi-Fermi levels  $F_e$  and  $F_h$  and electron and hole energy levels  $E_{e,L}$  and  $E_{h,L}$  at lasing, which can be written as

$$g_{st,m} = \Gamma_{QW} N_{QW} g_{QW,m} \left[ \frac{1}{e^{(E_{e,L}-F_e)/(k_B T_J)} + 1} - \frac{1}{e^{(E_{h,L}-F_h)/(k_B T_J)} + 1} \right], \quad (3.23)$$

where  $k_B$  is the Boltzmann constant and  $g_{QW,m}$  is a coefficient independent of the electron and hole concentrations and can be derived from the dipole moment, lasing mode normalization and density of optical transitions.  $N_{QW}$  is the number of quantum wells in the active region.  $\Gamma_{QW}$  is the normalized confinement factor. The gain coefficient does not increase linearly with the number of the quantum wells and more quantum wells only bring marginal further improvement to the gain, because the confinement factors in the side quantum wells are smaller than that of the center quantum well.  $\Gamma_{QW}$  is used to model this effect and is defined as

$$\Gamma_{QW} = \frac{\sum_{i=1}^{N_{QW}} \int_{L_{z,QW,i}} |E(z)|^2 dz}{N_{QW} \int_{L_{z,QW,center}} |E(z)|^2 dz}, \quad (3.24)$$

where  $E(z) = E_0 \cos(2\pi n_r z / \lambda)$ ,  $n_r$  is refractive index in the active region and  $z = 0$  is at the center of the cavity.  $L_{z,QW,i}$  is the thickness of each quantum well and  $L_{z,QW,center}$  is the thickness of the quantum well at the center.  $\lambda$  is the wavelength of the cavity. For lasers designed for 985 nm with three 60 Å thick quantum wells separated by 100 Å barriers, the normalized confinement factor is 0.923. Here we assume that the quantum wells are separated far enough that the coupling effect is negligible.

For planar quantum wells, the coefficient  $g_{QW}$  in (3.23) is related to interaction of electric field of the  $m$ -th mode and dipole moment and can be written as

$$g_{QW} = 4\pi L_x L_y q^2 \frac{|d_{c,v} \cdot E^*(z_{QW})|^2}{3\hbar} \frac{m_r}{\pi\hbar^2}, \quad (3.25)$$

where  $L_x L_y$  is the mode size and  $q\mathbf{d}_{c,v}$  is the dipole moment between the electron and hole in conduction and valence band.  $\mathbf{E}$  is the normalized electric field strength in the quantum wells and is found by

$$\mathbf{E} = \mathbf{a} \sqrt{\frac{\hbar\omega_c}{2\varepsilon L_x L_y L_{z,eff}}}, \quad (3.26)$$

where  $\mathbf{a}$  is a unit vector and  $L_{z,eff}$  is the effective length of the mode in  $z$  direction and can be found by

$$\frac{\omega_c}{Q} = \frac{c}{n_r L_{z,eff}} \ln \sqrt{\frac{1}{R_F R_B}}, \quad (3.27)$$

where  $R_F$  and  $R_B$  are the reflectivities of the front and back mirrors. We know that the spontaneous emission rate from a 2-level system is

$$A_{2,1} = \frac{1}{\tau_{sp}} = \frac{n_r^3 q^2 |d_{c,v}|^2 (\omega_2 - \omega_1)^3}{3\pi c^3 \varepsilon \hbar} = \frac{n_r q^2 |d_{c,v}|^2 \omega_c^3}{3\pi \varepsilon_0 \hbar c^3}, \quad (3.28)$$

where  $\tau_{sp}$  is the spontaneous photon life time.  $\varepsilon$  and  $\varepsilon_0$  are permittivity and vacuum permittivity respectively with the relation of  $\varepsilon = \varepsilon_0 n_r^2$ . Plugging (3.26) and (3.28) into (3.25) we have

$$g_{QW} = \frac{2\pi c^3 m_r}{\tau_{sp} \hbar \omega_c^2 n_r^3 L_{z,eff}}. \quad (3.29)$$

### 3.3.4 Numbers of electrons and holes

Considering a finite quantum well shown in Figure 3-2, for a semiconductor laser with  $N_{QW}$  quantum wells, the numbers of electrons and holes in the quantum wells are given by

$$\begin{aligned}
 N_{e,QW} &= N_{QW} A_{QW} \frac{m_e}{\pi \hbar^2} \sum_{m=1}^{\infty} \int_{E_{C,QW} + \pi^2 \hbar^2 m^2 / (2m_e L_z^2, QW)}^{E_{C,Bulk}} dE \frac{1}{e^{(E-F_e)/(k_B T_J)} + 1} \\
 &= N_{QW} A_{QW} \frac{m_e k_B T_J}{\pi \hbar^2} \sum_{m=1}^{\infty} \ln \left[ \frac{e^{-(E_{C,QW} + \pi^2 \hbar^2 m^2 / (2m_e L_z^2, QW) - F_e)/(k_B T_J)} + 1}{e^{-(E_{C,Bulk} - F_e)/(k_B T_J)} + 1} \right], \tag{3.30}
 \end{aligned}$$

$$\begin{aligned}
 N_{h,QW} &= N_{QW} A_{QW} \frac{1}{\pi \hbar^2} \sum_{m=1}^{\infty} \int_{E_{V,Bulk}}^{E_{V,m,QW} - \pi^2 \hbar^2 m^2 / (2m_{h,m} L_z^2, QW)} dE \frac{m_{h,m}}{e^{-(E-F_h)/(k_B T_J)} + 1} \\
 &= N_{QW} A_{QW} \frac{k_B T_J}{\pi \hbar^2} \sum_{m=1}^{\infty} m_{h,m} \ln \left[ \frac{e^{(E_{V,m,QW} - \pi^2 \hbar^2 m^2 / (2m_{h,m} L_z^2, QW) - F_h)/(k_B T_J)} + 1}{e^{(E_{V,Bulk} - F_h)/(k_B T_J)} + 1} \right], \tag{3.31}
 \end{aligned}$$

where  $A_{QW}$  is the area of the quantum wells in the x-y plane perpendicular to the direction of the quantum well thickness.

To simplify our model and calculations, we have to find out how the different sub-bands of the conduction and valence band are occupied. As shown in Figure 3-5, the density of states in a planar quantum well (solid lines) is like a staircase, which is much different than that for a bulk material (dashed line). The planar quantum well density of states consists of sub-bands for each mode number  $m$ , with each sub-band having a density of states that is independent of energy. The electrons in conduction band comply with Fermi distribution and tend to occupy the lowest sub-band but can be smeared into higher sub-band due to thermal broadening.



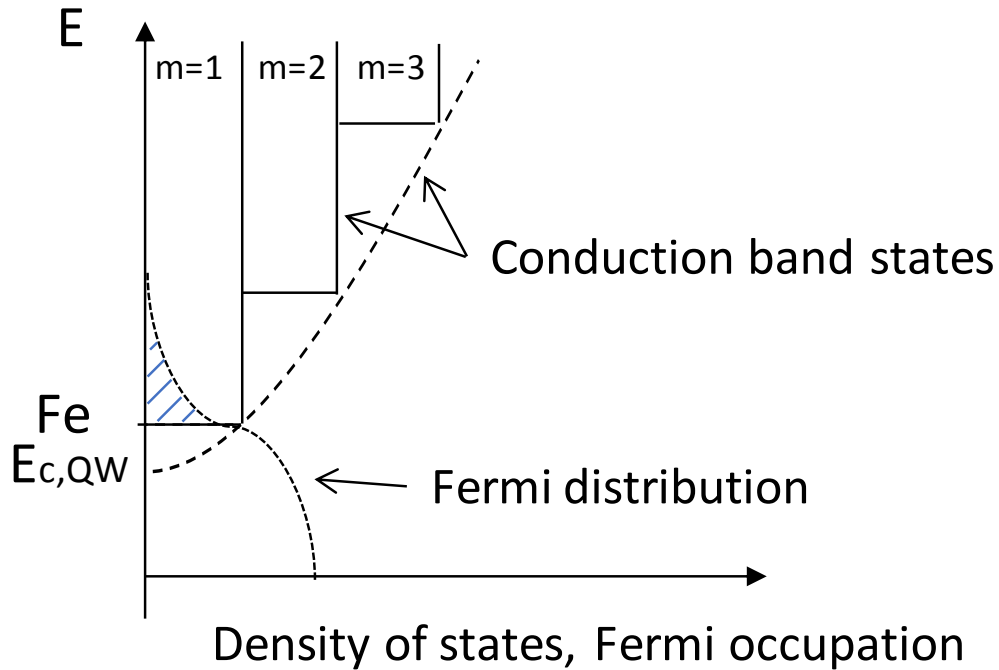


Figure 3-5: Density of conduction band states in a planar quantum well.

For a finite quantum well, the confined energy levels of electrons and holes are found by choosing the boundary conditions to match the barrier height. At room temperature, given a typical GaAs quantum well with thickness  $L_z = 100\text{\AA}$  and effective electron mass of  $0.063m_0$ , where  $m_0$  is electron rest mass, the ratio of the electron concentrations in the first lowest two sub-bands is  $\frac{N_{e,QW,m=2}}{N_{e,QW,m=1}} = 1.2 \times 10^{-3}$ . Obviously the quantum well is forcing electrons into the lowest sub-band through its confinement of electrons. For holes, however, the confinement is weaker, since the effective mass is much larger, which is  $0.51m_0$  for GaAs. The ratios of the hole concentrations in the lowest three sub-bands are  $\frac{N_{h,QW,m=2}}{N_{h,QW,m=1}} = 0.5$  and  $\frac{N_{h,QW,m=3}}{N_{h,QW,m=1}} = 0.13$ . For thinner quantum wells and other material (such as InGaAs) with smaller effective electron and hole masses, the confinement is more effective.

Therefore for simplicity, we assume that electrons are mostly confined in the lowest sub-band and holes are mainly confined in the first two lowest sub-bands in the quantum well and the lasing transition happens only between the first sub-bands in conduction and valence band, as shown in Figure 3-6.

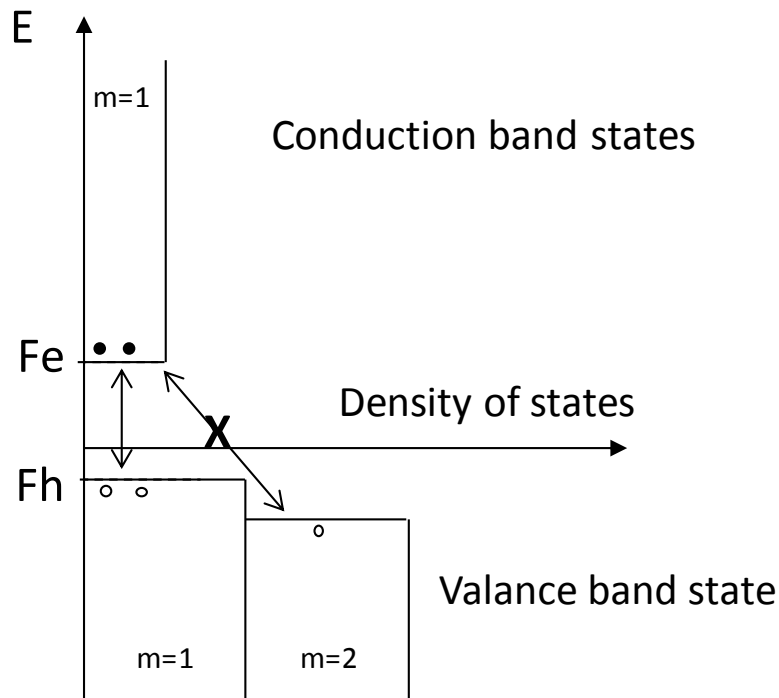


Figure 3-6: Simplified density of states in a planar quantum well.

It is well known that Fermi distribution of carriers broadens as the junction temperature increases with bias current. The detuning between the cavity and quantum well gain peak becomes sufficient at elevated temperature, causing quasi-Fermi levels moving closer to the barrier state. Consequently, carriers in the quantum wells could be thermally ejected out and go into a bulk density of states above the highest energy level of the quantum wells. Figure 3-7 illustrates the carrier distribution at high junction temperature.

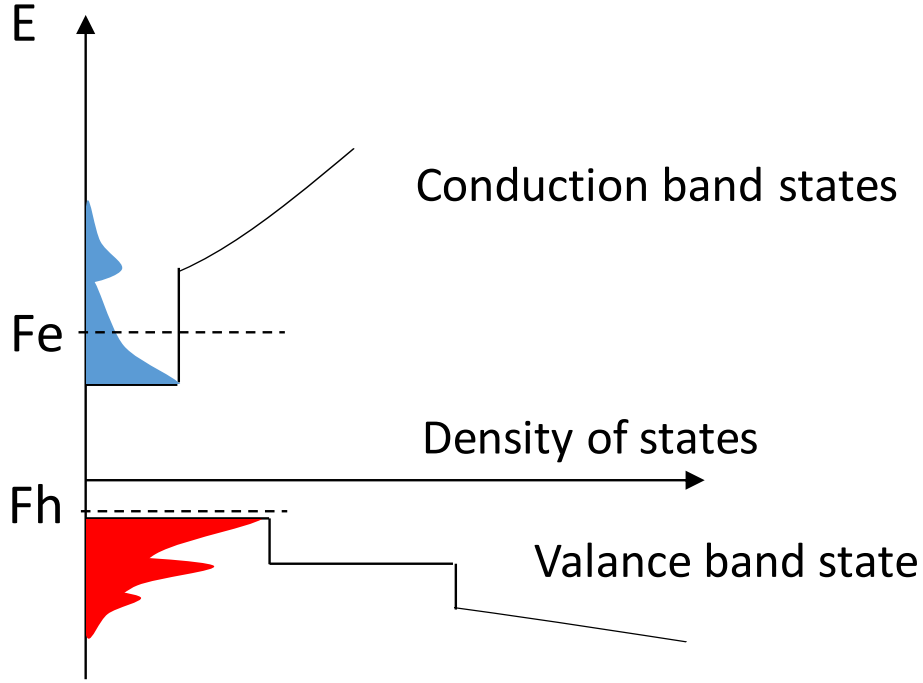


Figure 3-7: Broadening of carriers distribution at high junction temperature.

The electron and hole concentrations above the barrier energy can be found by

$$\begin{aligned}
 N_{e,Bulk} &= N_{QW} A_{QW} L_{z,QW} \frac{\sqrt{2}}{\pi^2} \left( \frac{m_e}{\hbar^2} \right)^{3/2} \int_{E_{C,Bulk}}^{+\infty} dE \sqrt{E - E_{C,Bulk}} \frac{1}{e^{(E-F_e)/(k_B T_J)} + 1} \\
 &\quad + A_{Bulk} L_{z,Bulk} \frac{\sqrt{2}}{\pi^2} \left( \frac{m_{e,Bulk}}{\hbar^2} \right)^{3/2} \int_{E_{C,Bulk}}^{+\infty} dE \sqrt{E - E_{C,Bulk}} \frac{1}{e^{(E-F_e)/(k_B T_J)} + 1} \\
 &\approx \frac{(N_{QW} L_{z,QW} m_e^{3/2} + L_{z,Bulk} m_{e,Bulk}^{3/2})}{\sqrt{2}} A_{QW} \left( \frac{k_B T_J}{\pi \hbar^2} \right)^{3/2} e^{-(E_{C,Bulk} - F_e)/(k_B T_J)}, \tag{3.32}
 \end{aligned}$$

$$\begin{aligned}
 N_{h,Bulk} &= N_{QW} A_{QW} L_{z,QW} \frac{\sqrt{2}}{\pi^2} \left( \frac{m_h}{\hbar^2} \right)^{3/2} \int_{-\infty}^{E_{V,Bulk}} dE \sqrt{E_{V,Bulk} - E} \frac{1}{e^{-(E-F_h)/(k_B T_J)} + 1} \\
 &\quad + A_{Bulk} L_{z,Bulk} \frac{\sqrt{2}}{\pi^2} \left( \frac{m_{h,Bulk}}{\hbar^2} \right)^{3/2} \int_{-\infty}^{E_{V,Bulk}} dE \sqrt{E_{V,Bulk} - E} \frac{1}{e^{-(E-F_h)/(k_B T_J)} + 1} \\
 &\approx \frac{(N_{QW} L_{z,QW} m_h^{3/2} + L_{z,Bulk} m_{h,Bulk}^{3/2})}{\sqrt{2}} A_{QW} \left( \frac{k_B T_J}{\pi \hbar^2} \right)^{3/2} e^{(E_{V,Bulk} - F_h)/(k_B T_J)}, \tag{3.33}
 \end{aligned}$$

where  $A_{Bulk}$  is the area of the bulk material in the x-y plane and  $A_{QW} = A_{Bulk} \cdot L_{z,Bulk}$  is the thickness of the bulk material.  $m_h$  is the effective mass of holes in bulk quantum well material.  $m_{e,Bulk}$  and  $m_{h,Bulk}$  are the effective masses of electrons and holes of the bulk material. Note that Boltzmann approximation is applied in equations (3.32) and (3.33) because the energy difference between the energy levels in the bulk material and their corresponding quasi-Fermi levels is much larger than  $k_B T_J$ . Therefore the total numbers of electrons and holes in the active region are

$$N_e = \frac{A_{QW} k_B T_J}{\pi \hbar^2} \left\{ N_{QW} m_e \ln \left[ \frac{e^{-(E_{e,1} - F_e)/(k_B T_J)} + 1}{e^{-(E_{C,Bulk} - F_e)/(k_B T_J)} + 1} \right] \right. \\ \left. + (N_{QW} L_{z,QW} m_e^{3/2} + L_{z,Bulk} m_{e,Bulk}^{3/2}) \left( \frac{k_B T_J}{2\pi \hbar^2} \right)^{1/2} e^{-(E_{C,Bulk} - F_e)/(k_B T_J)} \right\}, \quad (3.34)$$

$$N_h = \frac{A_{QW} k_B T_J}{\pi \hbar^2} \left\{ N_{QW} \sum_{m=1}^2 m_{h,m} \ln \left[ \frac{e^{(E_{h,m} - F_h)/(k_B T_J)} + 1}{e^{(E_{V,Bulk} - F_h)/(k_B T_J)} + 1} \right] \right. \\ \left. + (N_{QW} L_{z,QW} m_h^{3/2} + L_{z,Bulk} m_{h,Bulk}^{3/2}) \left( \frac{k_B T_J}{2\pi \hbar^2} \right)^{1/2} e^{(E_{V,Bulk} - F_h)/(k_B T_J)} \right\}, \quad (3.35)$$

where  $E_{e,1}$  and  $E_{h,m}$  ( $m=1, 2$ ) are the sub-band energy levels of electrons and holes.

To find out the quasi-Fermi levels in the quantum wells, we need to solve a set of two equations, which are the charge neutrality equation (3.3) and the threshold condition:

$$g_{st}(F_e, F_h) = \frac{\omega_c}{Q}. \quad (3.36)$$

### 3.3.5 Differential gain

Since the electron and hole concentrations are set by the quasi-Fermi levels as well as the conduction and valence band edge energy levels, the gain coefficient is connected to the electron

and hole densities through quasi-Fermi levels. Therefore we can find the expression for the differential gain coefficient from quasi-Fermi levels and electronic structure. We have

$$\frac{dg_{st}}{dN_e} = \frac{dg_{st}}{dF_e} \frac{dF_e}{dN_e} = \frac{\Gamma_{QW} N_{QW} g_{QW}}{k_B T_J} \left\{ \frac{e^{(E_{e,L}-F_e)/(k_B T_J)}}{[e^{(E_{e,L}-F_e)/(k_B T_J)} + 1]^2} - \frac{e^{(E_{h,L}-F_h)/(k_B T_J)}}{[e^{(E_{h,L}-F_h)/(k_B T_J)} + 1]^2} \frac{dF_h}{dF_e} \right\} \frac{dF_e}{dN_e}. \quad (3.37)$$

From (3.34) and (3.35), we get

$$\begin{aligned} \frac{dN_e}{dF_e} = & \frac{A_{QW}}{\pi \hbar^2} \left\{ N_{QW} m_e \left[ \frac{1}{e^{-(E_{C,Bulk}-F_e)/(k_B T_J)} + 1} - \frac{1}{e^{-(E_{e,L}-F_e)/(k_B T_J)} + 1} \right] \right. \\ & \left. + (N_{QW} L_{z,QW} m_e^{3/2} + L_{z,Bulk} m_{e,Bulk}^{3/2}) \left( \frac{k_B T_J}{2\pi \hbar^2} \right)^{1/2} e^{-(E_{C,Bulk}-F_e)/(k_B T_J)} \right\}, \end{aligned} \quad (3.38)$$

$$\begin{aligned} \frac{dN_h}{dF_h} = & -\frac{A_{QW}}{\pi \hbar^2} \left\{ N_{QW} \sum_{m=1}^2 m_{h,m} \left[ \frac{1}{e^{(E_{V,Bulk}-F_h)/(k_B T_J)} + 1} - \frac{1}{e^{(E_{h,m}-F_h)/(k_B T_J)} + 1} \right] \right. \\ & \left. + (N_{QW} L_{z,QW} m_h^{3/2} + L_{z,Bulk} m_{h,Bulk}^{3/2}) \left( \frac{k_B T_J}{2\pi \hbar^2} \right)^{1/2} e^{(E_{V,Bulk}-F_h)/(k_B T_J)} \right\}. \end{aligned} \quad (3.39)$$

Inserting (3.38) and (3.39) into (3.37), we find the expression of differential gain in terms of electronic structure, quasi-Fermi energies and junction temperature, which is

$$\begin{aligned} G_{Diff}(T_J) = \frac{dg_{st}}{dN_e}(T_J) = & \frac{\Gamma_{QW} N_{QW} g_{QW} \pi \hbar^2}{A_{QW} k_B T_J} \\ & \left\{ \frac{e^{(E_{e,L}-F_e)/(k_B T_J)}}{[e^{(E_{e,L}-F_e)/(k_B T_J)} + 1]^2} \right. \\ & N_{QW} m_e \left[ \frac{1}{e^{-(E_{C,Bulk}-F_e)/(k_B T_J)} + 1} - \frac{1}{e^{-(E_{e,L}-F_e)/(k_B T_J)} + 1} \right] + (N_{QW} L_{z,QW} m_e^{3/2} + L_{z,Bulk} m_{e,Bulk}^{3/2}) \left( \frac{k_B T_J}{2\pi \hbar^2} \right)^{1/2} e^{-(E_{C,Bulk}-F_e)/(k_B T_J)} \\ & \left. + \frac{e^{(E_{h,L}-F_h)/(k_B T_J)}}{[e^{(E_{h,L}-F_h)/(k_B T_J)} + 1]^2} \right. \\ & \left. N_{QW} \sum_{m=1}^2 m_{h,m} \left[ \frac{1}{e^{(E_{V,Bulk}-F_h)/(k_B T_J)} + 1} - \frac{1}{e^{(E_{h,m}-F_h)/(k_B T_J)} + 1} \right] + (N_{QW} L_{z,QW} m_h^{3/2} + L_{z,Bulk} m_{h,Bulk}^{3/2}) \left( \frac{k_B T_J}{2\pi \hbar^2} \right)^{1/2} e^{(E_{V,Bulk}-F_h)/(k_B T_J)} \right\}. \end{aligned} \quad (3.40)$$

And the expression of the intrinsic modulation response above threshold becomes

$$H_I(\omega) = \frac{\frac{\omega_c(T_J)\Delta n(\omega, T_J)}{Q}}{\frac{\Delta I(\omega)}{q}} \approx \frac{\frac{\omega_c(T_J)G_{Diff}(T_J)n_0(T_J)}{Q}}{-\omega^2 - i\omega G_{Diff}(T_J)n_0(T_J) + \frac{\omega_c(T_J)G_{Diff}(T_J)n_0(T_J)}{Q}}. \quad (3.41)$$

Note that (3.41) is derived from semiconductor rate equations. The expression of differential gain (3.40) is found from a general quantum well electronic structure, and the expressions for bulk material and quantum dot lasers can also be found in a similar way while the only difference is the density of states in the active region for calculating electron and hole concentrations. Therefore this model of intrinsic modulation response can be applied to other types of semiconductor lasers, such as distributed feedback (DFB) lasers. We can clearly see that the intrinsic modulation speed tracks not only active volume and junction temperature, but differential gain and stimulated emission rate (i.e. photon number in the active region). Cavity lasing transition (between  $E_{e,L}$  and  $E_{h,L}$ ) detuning from quantum well gain peak ( $E_{e,m}$  and  $E_{h,m}$ ) is also taken account in the gain and differential gain.

### 3.4. Calculation results

To verify the validity of our model, it is supposed to compare the calculated results with experimental data. Since the measured data is the total modulation response, the model of parasitic modulation response should be included in the calculation.

Here we present the comparison our calculation with the results of a 7  $\mu\text{m}$  oxide VCSEL from published literatures [29, 30]. The equivalent RC circuit model of the oxide VCSEL is shown in Figure 3-8, where  $C_p$  is the pad capacitance including the capacitances due to the metal contact pads,  $C_m$  is the capacitance associated with the oxide and the depleted region near the

active region,  $R_m$  is the resistance from both p- and n- mirrors, and  $R_j$  is the junction resistance from the intrinsic region below the oxide aperture. The benzocyclobutene (BCB) under the p-metal contacts is a dielectric material used for reducing the pad capacitance.

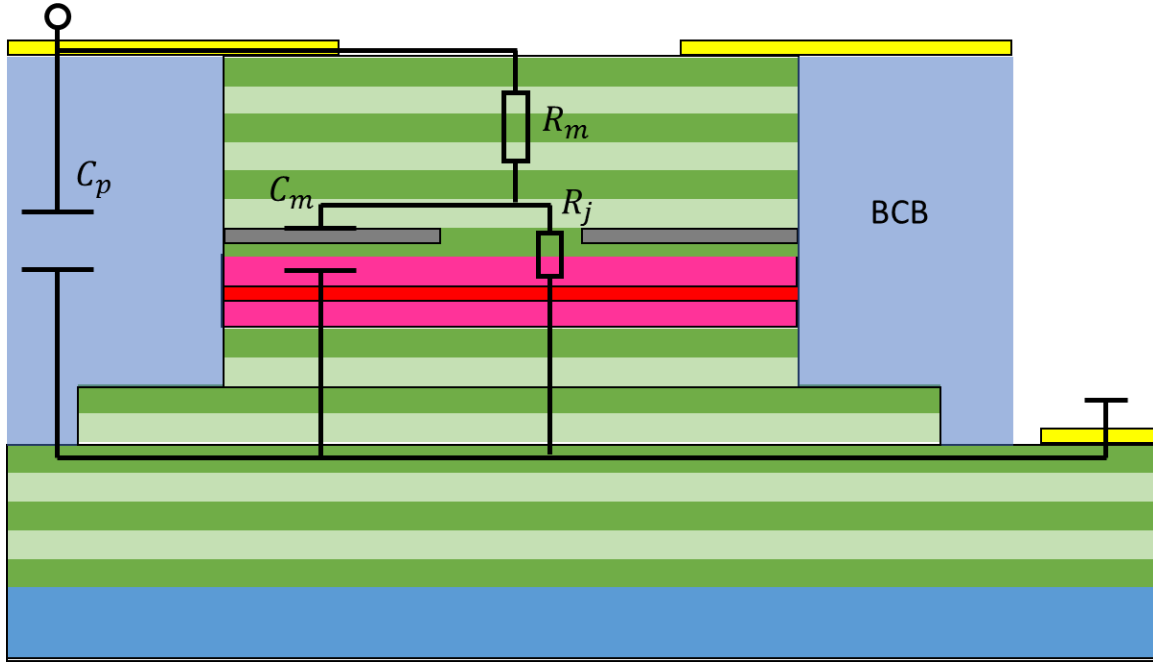


Figure 3-8: Schematic diagram of an oxide VCSEL superimposed with equivalent RC parasitics.

Finding the transfer function of the parasitic modulation response is relatively straightforward and the expression is given as

$$H_p(\omega) = \frac{I_L(\omega)}{I_{input}(\omega)} = \frac{1}{-\omega^2 - i\omega \frac{C_m R_j + C_p R_m + C_p R_j}{C_p C_m R_m R_j} + \frac{1}{C_p C_m R_m R_j}}. \quad (3.42)$$

The total modulation response is

$$H(\omega) = H_l(\omega)H_p(\omega). \quad (3.43)$$

Figure 3-9 shows the comparison between the calculated 3dB bandwidth from our model and the experimental data of a 7  $\mu\text{m}$  oxide VCSEL at stage temperatures of room temperature (RT) and 85  $^{\circ}\text{C}$ .

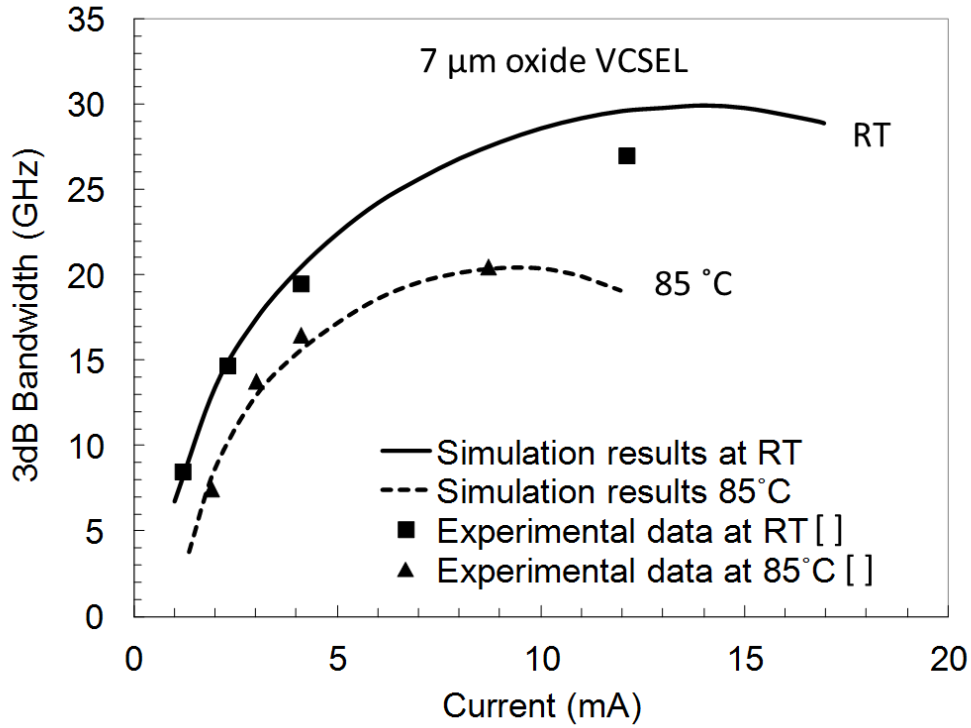


Figure 3-9: Comparison of 3dB bandwidth between simulation results and experimental data of a 7  $\mu\text{m}$  oxide VCSEL.

For stage temperature at 85  $^{\circ}\text{C}$ , our simulation results match with the data points very well, whereas at RT, our calculations fit the experimental data at low bias current but become about 10% higher than the measured data. Our interpretation of the mismatch is that it comes from the rise of the thermal resistance at high junction temperature as the VCSEL is being driven harder. The thermal resistance of a VCSEL increases with junction temperature as the injected current density goes up. The elevated thermal resistance in turn causes a faster increase of the



junction temperature, leading to the saturation of stimulated emission rate and hence thermal rollover of the output power. For the solid curve at RT, our calculations are based on a given thermal resistance measured at RT. Thus at high bias current, the thermal resistance is increased due to the rapid rise of temperature and the actual temperature in the junction is higher than what we calculated. As a result, the calculated 3dB bandwidth is higher than that from measurement. For stage temperature of 85 °C, the thermal resistance of the VCSEL does not increase so much since it is already started at a pretty high temperature.

### 3.5. Summary

In this chapter, we have proposed a new model of intrinsic modulation response of VCSELs by being able to calculate the differential gain from the electronic structure of quantum wells in the active region. It is shown that the intrinsic modulation response above threshold is set by the cavity loss rate, the differential gain and the stimulated photon density in the cavity. It is worth noting that the differential gain and the photon density are temperature dependent and both of them decrease at high junction temperature, thus limiting the modulation speed of a laser. Therefore, it is expected to increase the intrinsic modulation response of a VCSEL by reducing the junction temperature through better heat spreading. In the next chapter, we will discuss the thermal limits of a VCSEL and how the differential gain and the stimulated photon density affect the speed of a laser.

We have also shown the comparison between our simulation results and reported data of an oxide VCSEL in terms of the 3dB bandwidth. The calculations include both intrinsic modulation response and parasitic modulation response. As for the parasitic modulation

response, it is mainly set by the resistance and capacitance between the intrinsic active region and the driving circuit. The results have shown good conformity within a reasonable range.

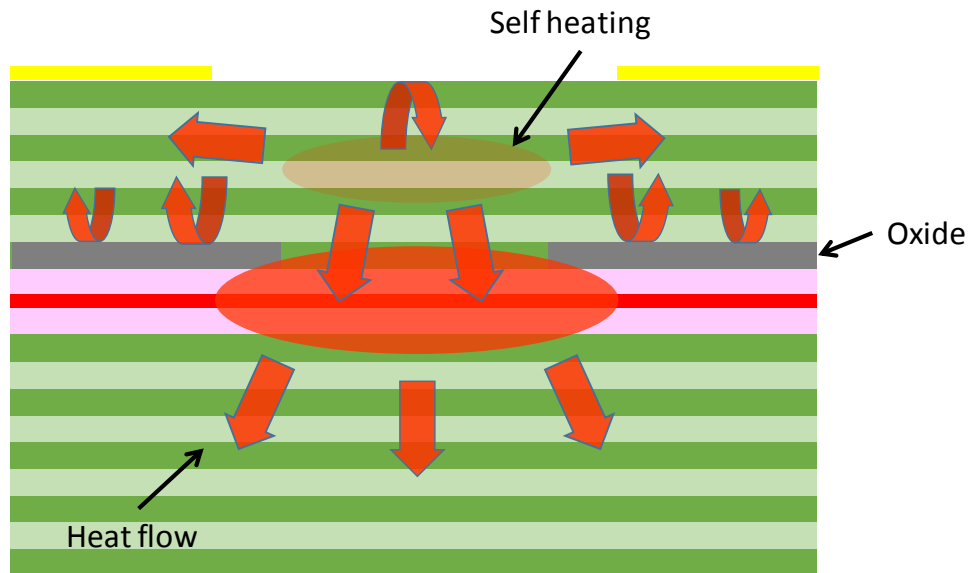
## CHAPTER 4: THERMAL EFFECT AND ANALYSIS

According to the discussion from the previous chapter, junction temperature has great impact on the differential gain and stimulated photon density, hence the intrinsic modulation response. It is believed that reducing the junction temperature leads to the improvement of intrinsic modulation speed. In this chapter, we will show how lithographic VCSELs reduce the thermal resistance through eliminating the oxide aperture and how the low thermal resistance improve the intrinsic modulation response combining with reduced mode volume.

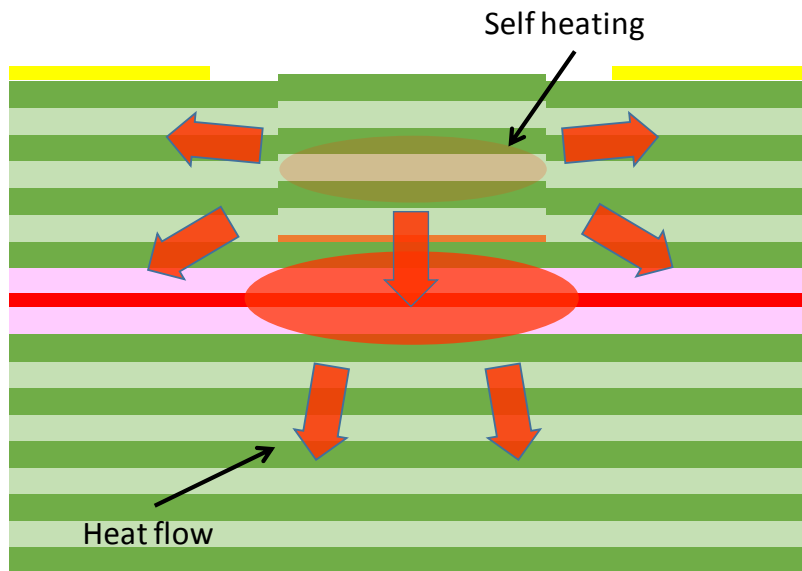
### 4.1. Heat spreading in the cavity

Oxide-confined VCSELs have been intensely studied and greatly improved to achieve low power consumption and high efficiency, and become the dominant optical sources in various applications including optical sensing, data centers and high speed optical interconnects. However, the oxide aperture creates a heat barrier between the p-mirror and the active region because of the different thermal conductivities, 0.7 W/mK for  $\text{Al}_x\text{O}_y$  and  $\sim 50$  W/mK for GaAs/AlAs mirrors [31]. As shown in Figure 4-1 (a), this heat barrier prevents the heat generated in the p-mirror due to resistive heating and free carrier absorption from spreading downward freely and forces the heat to flow through the oxide aperture into the active region. The temperature in the active region can be  $\sim 50^\circ\text{C}$  higher than that of the surrounding cavity at high bias level [32]. The elevated temperature causes more internal strain around the oxide aperture and in turn leads to defect propagation [33]. In contrast, as shown in Figure 4-1 (b), the lithographic VCSELs have a more three-dimensional heat spreading scheme by removing the

oxide layer. With much heat bypassing the active region, the junction temperature can be greatly reduced and therefore higher reliability and longer device lifetime are expected.



(a)



(b)

Figure 4-1: Comparison of heat flow in (a) an oxide VCSEL, and (b) a lithographic VCSELs.

#### 4.2. Low thermal resistance

Removing the high Al content AlGaAs layer used to form oxide aperture in the p-side gives us more material choices for the p-mirror stack, which can further enhance the thermal conductivity of the p-mirrors. According to the thermal resistivity (inverse of thermal conductivity) of  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  alloys, shown in Figure 4-2 [34], it is the best to use GaAs for the high refractive index layers and AlAs for the low refractive index layers in the mirrors to get the maximum thermal conductivity. However, oxide VCSELs cannot have very high Al content AlGaAs materials in the p-mirrors because they will be oxidized in the formation of oxide aperture and cause high resistance in the p-mirrors. For most conventional oxide VCSELs, ~90% AlGaAs is often used in p-mirrors, of which the thermal resistivity is approximately five time higher than AlAs.

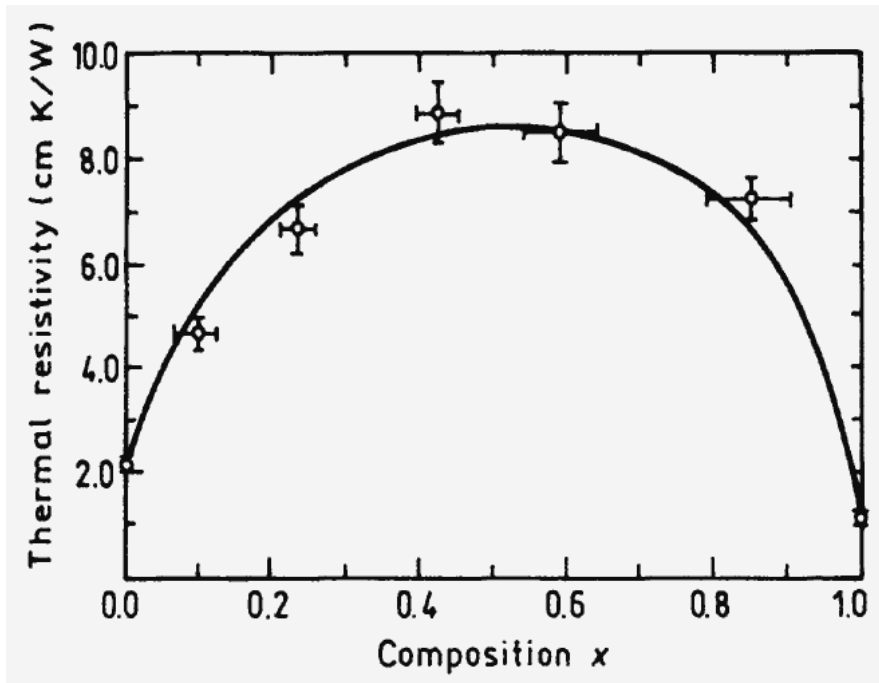


Figure 4-2: Thermal resistivity of  $\text{Al}_x\text{Ga}_{1-x}\text{As}$  alloys.

In contrast, lithographic VCSELs can have AIAs in the p-mirrors to further increase the thermal conductivity because the oxidization is no longer necessary. In order to show how effectively the thermal resistance can be reduced by incorporating AIAs in the p-mirrors, we have grown three different 850 nm VCSEL structures and compare their thermal resistances for various sizes [35]. As shown in Figure 4-3, the three structures have the same active region and n-mirrors, but different AlGaAs compositions in p-mirrors and the first quarter wavelength layer on the n-side. The n-mirrors of all structures are using 22% AlGaAs/AIAs pairs, while the p-mirrors are 15% AlGaAs/75% AlGaAs for Structure A, and 20% AlGaAs/AIAs for both Structure B and C. For the first quarter wavelength layer on the n-side, AIAs, 30% AlGaAs, AIAs are used in the three structures, respectively.

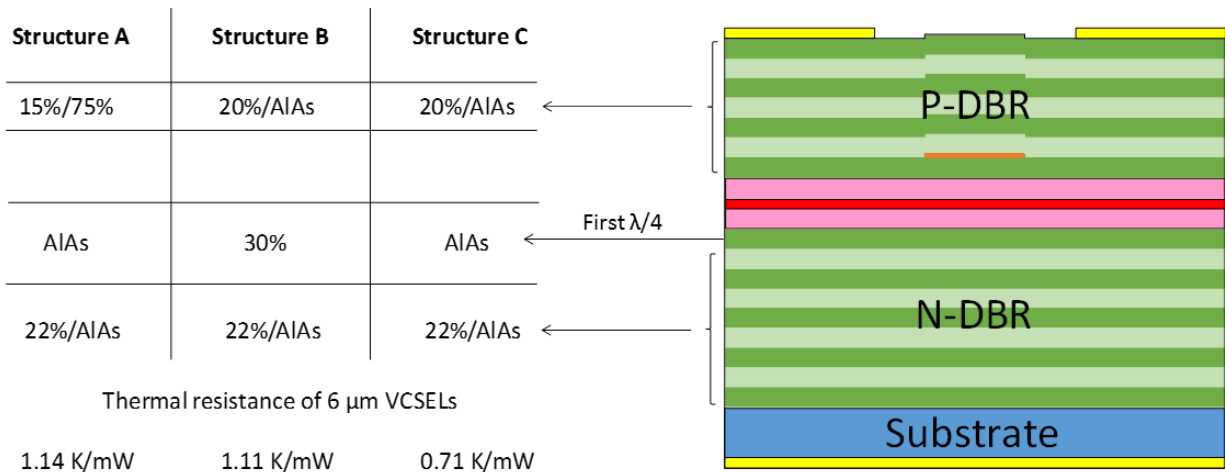


Figure 4-3: Schematic diagram of three different lithographic VCSEL structures using different amount of AIAs in the mirrors.

The thermal resistance of the three structures for different sizes are shown in Figure 4-4. Comparing Structure A and B, thermal resistances of Structure B for all sizes are lower than those of Structure A due to the utilization of AIAs in the p-mirrors. The thermal resistance can be

further reduced in Structure C by replacing the 30% AlGaAs with AlAs. The measured thermal resistance of a commercial available 6  $\mu\text{m}$  oxide VCSEL is also shown in Figure 4-4 [35], which is approximately three times higher than that of a lithographic VCSEL using Structure C.

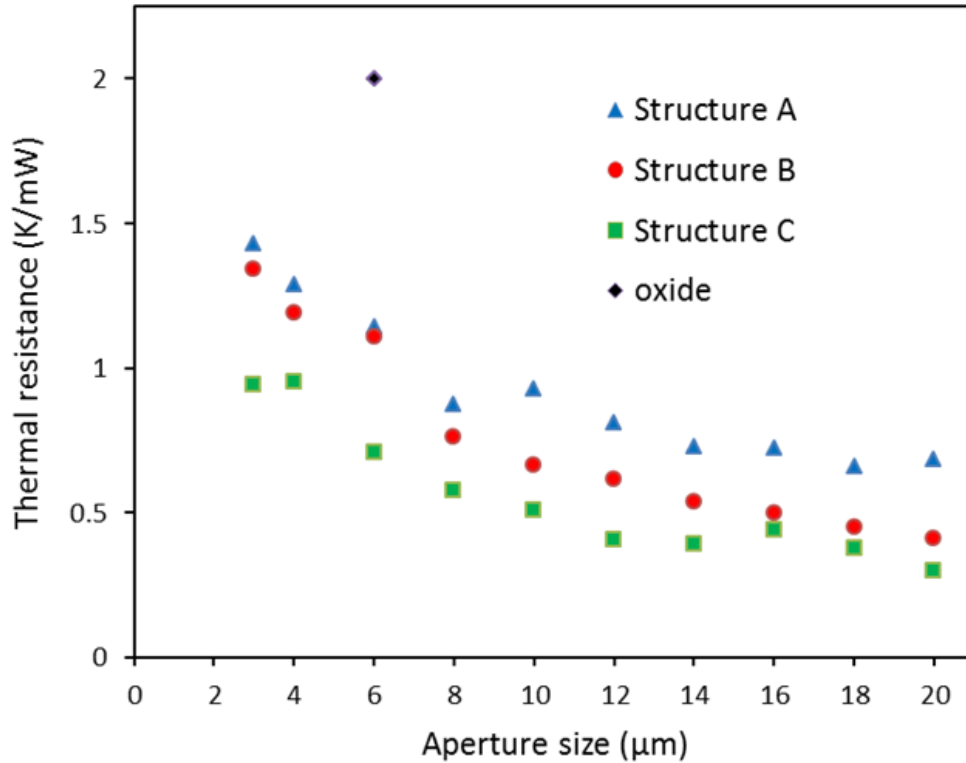


Figure 4-4: Comparison of thermal resistance of three lithographic VCSEL structures for various sizes with a 6  $\mu\text{m}$  diameter oxide VCSEL.

#### 4.3. Thermal limits of intrinsic modulation response

In this section, we will show how the low thermal resistance contributes to the enhancement of intrinsic modulation speed according to our new model.

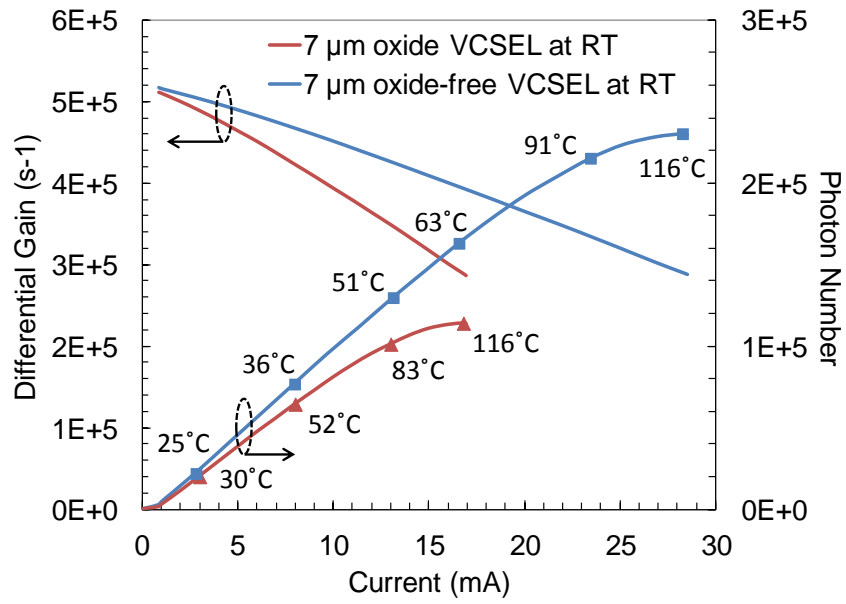
The intrinsic modulation response given in Equation (3.41) is set by cavity bandwidth, differential gain and stimulated emission rate. The cavity bandwidth is determined by the loss rate  $\omega_c/Q$ , or the inverse of photon lifetime,  $1/\tau_p$ . For photon lifetime as short as 1.5 ps, the cavity bandwidth could exceed 180 GHz, which is extremely high and thereby not limiting the maximum speed.

According to Equation (3.40), the differential gain is determined by a number of factors, such as quantum well structure, electronic structure in the quantum wells, mode volume and most importantly the junction temperature. Considering the spectral detuning between the lasing transition energy and the quantum well sub-band energy, analysis indicates that the differential gain decreases with the increase of the bias current, but remains moderately high at the thermal roll-over.

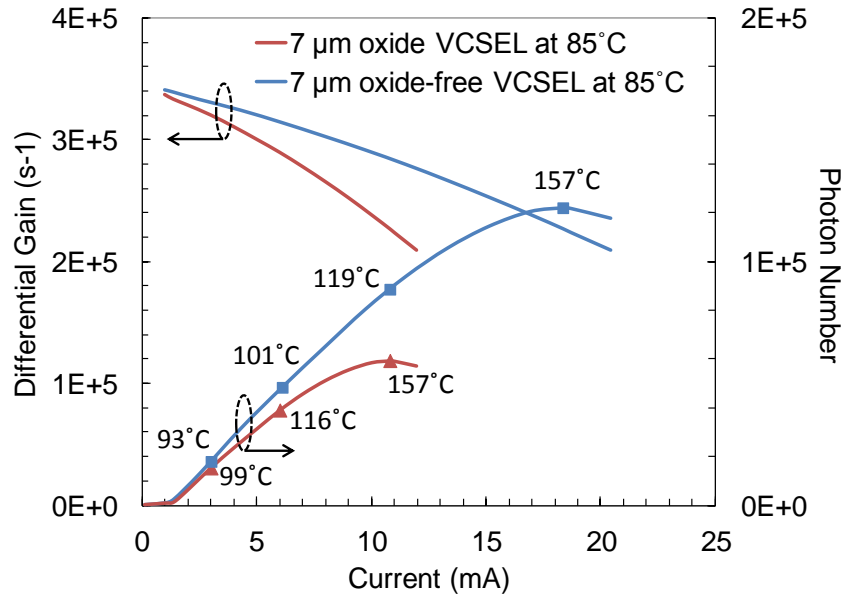
The stimulated emission rate is set by the photon density and the differential gain and thus sensitive to the junction temperature, which changes with bias current. As being driven harder by the bias current, the junction temperature could be sufficiently high, which results in the saturation of photon density, eventually limiting the maximum modulation speed.

We have shown that eliminating the oxide layer in VCSELs and incorporating AIAs in the low index mirror layers can greatly reduce the thermal resistance of VCSELs. To illustrate how the reduced thermal resistance improves the differential gain and stimulated emission rate, we present the dependence of calculated differential gain, photon number and junction temperature over bias current for two 7  $\mu\text{m}$  VCSELs with different thermal resistance, as shown in Figure 4-5.





(a)



(b)

Figure 4-5: Comparison of differential gain, photon number and junction temperature over bias current between 7 μm diameter oxide and oxide-free VCSELs at stage temperature of (a) RT and (b) 85°C.

The parameters of the 7  $\mu\text{m}$  diameter oxide VCSEL are provided in a published literature [29] and then are applied to our intrinsic modulation model to calculate the differential gain, photon number and junction temperature at stage temperature of both RT and 85 °C. The calculation results of the 7  $\mu\text{m}$  oxide-free VCSEL are calculated by simply decreasing the thermal resistance from 2.2 K/mW [29] to 1.1 K/mW while keeping other parameters fixed.

For both stage temperatures, the differential gain decreases with the increasing bias current due to thermal broadening and spectral detuning. The decrease in differential gain, however, is not significant compared with the saturation of the stimulated emission rate, which comes from the rapidly rise of the threshold current density after reaching the critical junction temperature. Above this temperature, any further increase in the bias current has to compensate the increase of the threshold current density due to self heating and spectral detuning. Therefore, the photon number and the stimulated emission rate saturate, resulting in a ceased growth in output power, hence limiting the maximum modulation speed. Comparing the junction temperature in two VCSELs at same bias currents, it is apparent that the oxide-free VCSEL is much cooler, which leads to higher differential gain and photon number. This is because that the saturation of the stimulated emission is delayed due to relative low junction temperature, thus a higher modulation speed is expected.

Figure 4-6 shows the impact of the low thermal resistance on the modulation response in terms of the two VCSELs mentioned above. The lower thermal resistance enables a higher bias current for getting the same thermal rollover temperature and thereby a higher stimulated emission rate. The maximum intrinsic modulation bandwidth of the oxide-free VCSEL for both stage temperatures increases significantly by 40% over the oxide VCSEL.

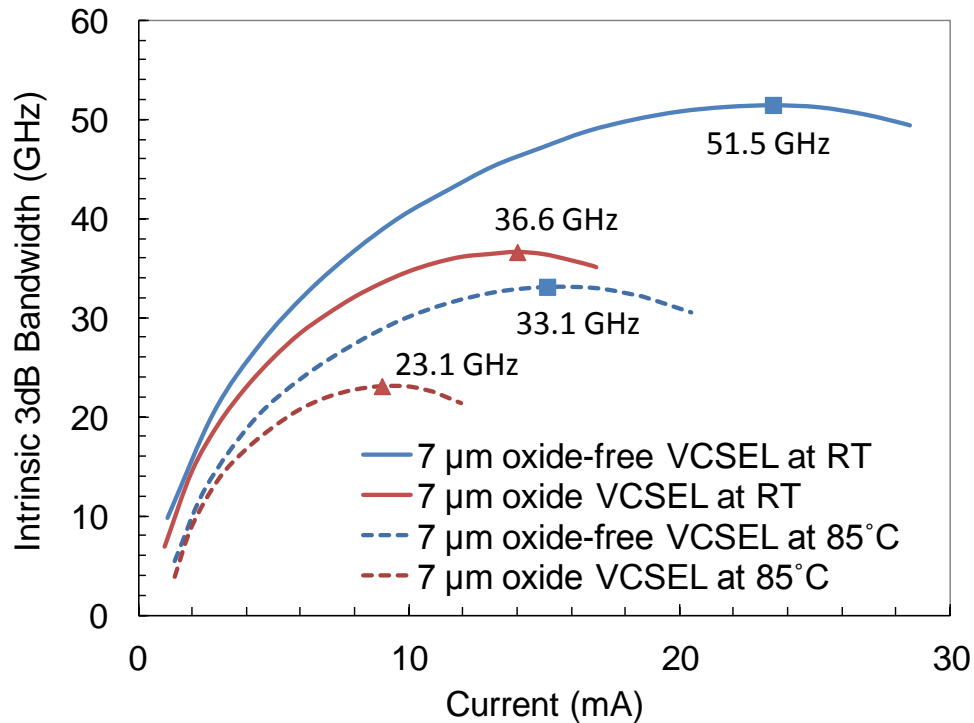


Figure 4-6: Comparison of intrinsic modulation 3dB bandwidth on bias current for 7 μm oxide and oxide-free VCSELs at stage temperature of RT and 85°C. Red triangles and blue squares indicate the calculated maximum intrinsic modulation bandwidth for the oxide and oxide-free VCSELs, respectively.

#### 4.4. Impact of reducing mode volume

Scaling down the size has always been a challenge for oxide-confined VCSELs because of the difficulties in the lateral geometry and size control of the oxide aperture. The oxide aperture is formed by a means of selective lateral oxidation, which is to convert buried high Al content (typically 98% or higher) AlGaAs layers to  $Al_xO_y$  [10, 11] in hot water vapor ambient. This process strongly depends on conditions such as Al content in AlGaAs and the temperature of the furnace and water vapor flow, causing poor uniformity and size control for small aperture

size. By eliminating the oxide, lithographic VCSELs, in which the aperture is defined only by lithography and epitaxial growth, enable uniformity and scalability for very small size VCSELs. This is essential for producing very high speed VCSELs.

According to Equation (3.21), the rise of junction temperature  $\Delta T$  can be expressed as the product of thermal resistance and dissipated power, i.e.,  $\Delta T = P_D \cdot R_{th}$ . The dissipated power causes temperature rise mainly through resistive heating and can be written in terms of bias current and electrical resistance, which is  $P_D = I^2 R \propto J^2 \cdot d^2$ , where  $d$  is the diameter of the device,  $I$  and  $J$  are the injected current and current density,  $R$  is the electrical resistance and has the relationship with device diameter as  $R \propto 1/d^2$ . For a VCSEL with a cylindrical shape on a thick substrate, the approximate relation between the thermal resistance and VCSEL size can be written as  $R_{th} = 1/(2\xi d)$  [28], where  $\xi$  is the effective thermal conductivity of the VCSEL. Therefore, the temperature change can be given as  $\Delta T \propto J^2 \cdot d$ . Under these simple assumptions, we can infer that small size VCSELs have lower junction temperature at a certain current density, or higher current density can be injected into smaller size VCSELs before thermal rollover. Measurements have been performed to verify this effect, as shown in Figure 4-7 and Figure 4-8 [36].

Figure 4-7 demonstrates the measured junction temperatures of both oxide and lithographic VCSELs for various sizes at the same current density of 50 kA/cm<sup>2</sup>, at which high intrinsic modulation response can be produced. All measurements were under continuous-wave (CW) operation at stage temperature of RT without any heat sink. The junction temperature was obtained in terms of measured lasing spectral shift with different bias current. Obviously, the junction temperature is lower for small size lithographic VCSELs. The junction temperature of a

3  $\mu\text{m}$  oxide VCSEL is plotted for comparison. A 7.5  $\mu\text{m}$  VCSEL was also measured but could not show stable L-I characteristics at this current density due to high internal temperature. The oxide VCSELs are commercially available and are designed for 850 nm while the lithographic VCSELs are for 975 nm applications. The comparison is not direct but still intuitive because it has been shown that the 8xx nm lithographic VCSELs also produce low thermal resistance approximately half of those of oxide VCSELs [35].

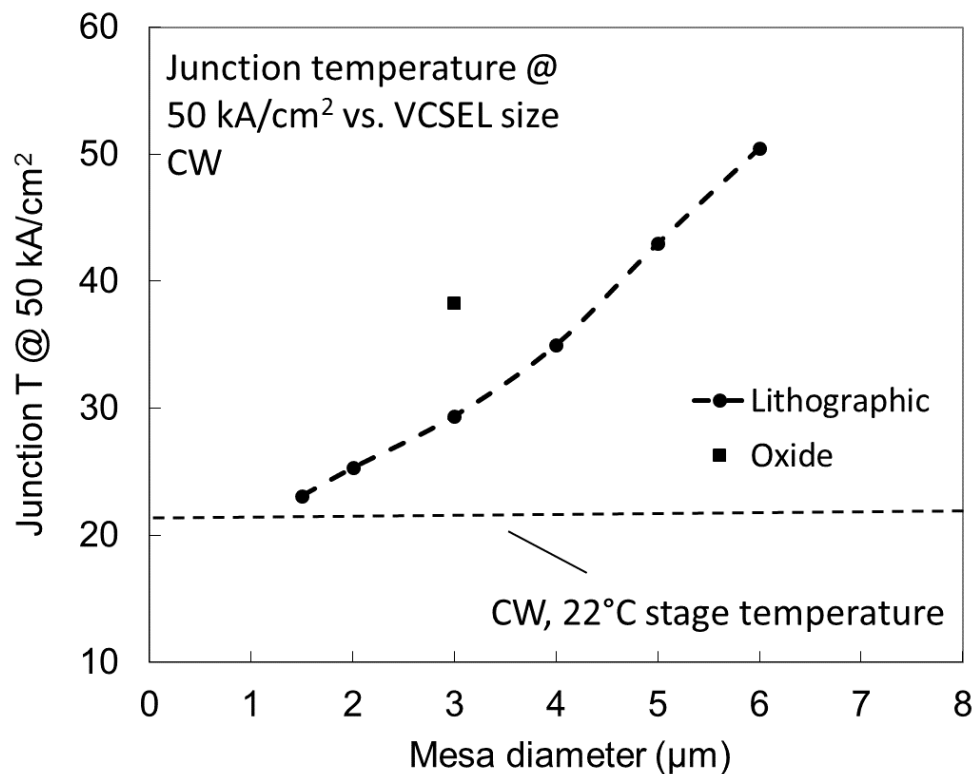


Figure 4-7: Internal junction temperature vs. VCSEL size at a given current density of 50 kA/cm<sup>2</sup>.

The low internal junction temperature indicates possibilities of improving reliability by reducing the VCSEL size at a given bias current density. This is different from oxide VCSELs, because small oxide aperture introduces more strain which causes rapid failure for the devices

[33, 37]. Therefore, the lithographic approach is promising for improving the reliability of small VCSELs.

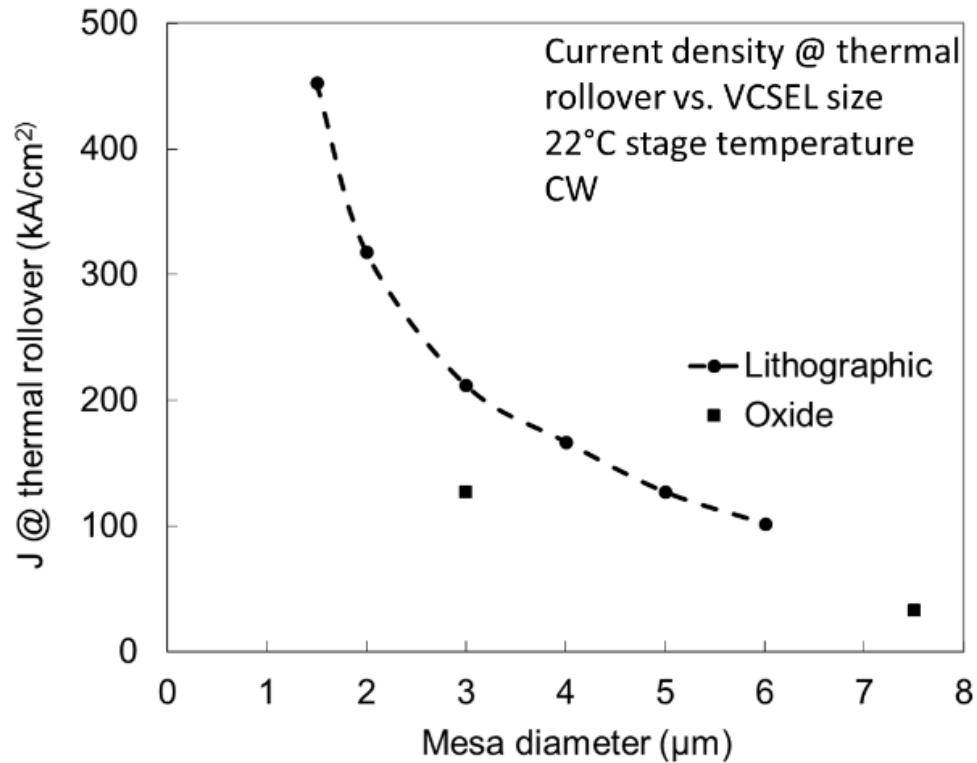


Figure 4-8: Measured current density at thermal rollover for various sizes of lithographic and oxide VCSELs.

Figure 4-8 demonstrates the measured current density at thermal rollover for various sizes lithographic and oxide VCSELs. The 6 µm diameter lithographic VCSEL shows a current density of 102 kA/cm<sup>2</sup> at thermal rollover and the 2 µm device has a current density of 318 kA/cm<sup>2</sup>. For 3 µm VCSELs, the lithographic one can operate at 213 kA/cm<sup>2</sup> whereas the oxide one can only work at 127 kA/cm<sup>2</sup> at thermal rollover. The delay in thermal rollover for the small size lithographic VCSELs indicates the ability of being able to operate at high current density,

enabling high photon density. As a result, higher intrinsic modulation bandwidth can be achieved for smaller size VCSELs.

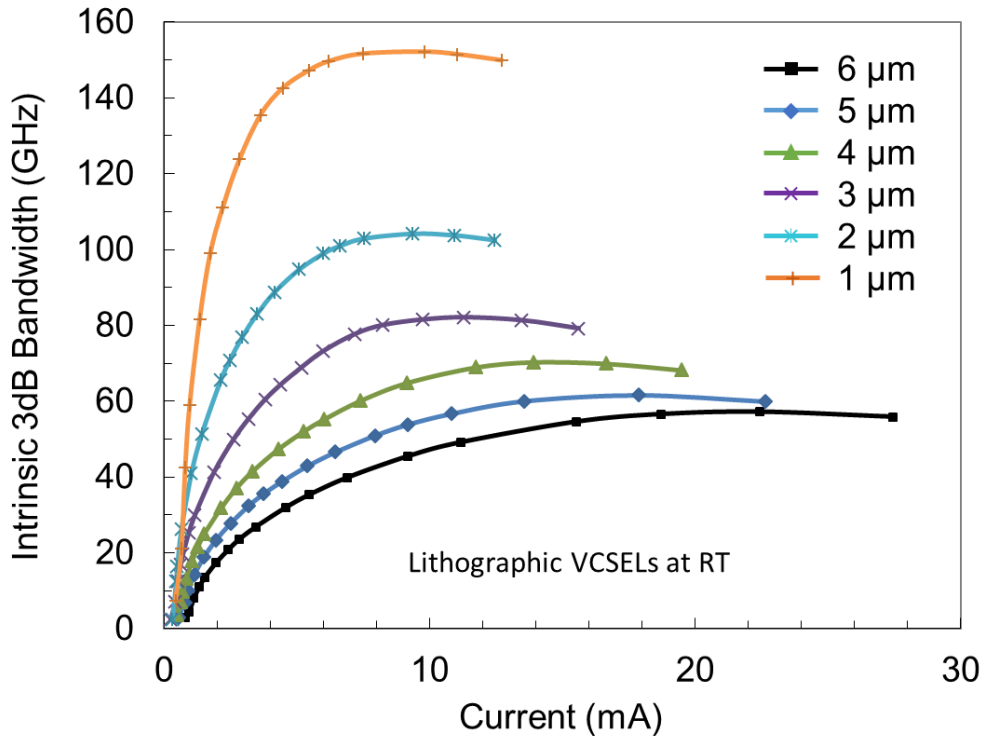


Figure 4-9: Calculated intrinsic 3dB bandwidth vs. bias current for 1 μm – 6 μm diameter lithographic VCSELs at stage temperature of RT.

To find out how the intrinsic modulation bandwidth can be improved with reduced mode volume, calculations have been done by using our intrinsic modulation response model. As shown in Figure 4-9, intrinsic modulation bandwidth of lithographic VCSELs ranging from 1 μm to 6 μm was calculated based on measured L-I characteristics and thermal resistance along with the differential gain found from the active region and cavity detuning. As the device size is scaling down, the intrinsic modulation speed is increasing rapidly. The calculated maximum intrinsic 3dB bandwidth exceeds 150 GHz for a 1 μm diameter lithographic VCSEL at RT. This

large bandwidth is the result of very high photon density ( $1E13 \text{ cm}^{-2}$ ) and relative low junction temperature ( $66 \text{ }^\circ\text{C}$ ) at high current density ( $1250 \text{ kA/cm}^2$ ).

#### 4.5. Summary

In this chapter, we have discussed the improvement of heat spreading in VCSELs by using lithographic approach and reducing the mode volume. Analysis on thermal limits of VCSELs shows that both temperature dependent differential gain and stimulated emission rate set the maximum intrinsic modulation speed, but the stimulated emission rate plays the limiting role. Our intrinsic modulation model predicts that extremely high bandwidth can be achieved by small size lithographic VCSELs due to high photon density and low thermal resistance.



## CHAPTER 5: VCSELS DESIGNED FOR HIGH SPEED

In this chapter, we will discuss about high speed VCSELS from a structure design perspective and present the characteristics of our lithographic VCSELS for high speed. As mentioned in Chapter 3, the total modulation response of a VCSEL includes intrinsic modulation response and parasitic modulation response. Analysis from Chapter 4 shows that high intrinsic modulation bandwidth requires designing differential gain and photon density as large as possible. For the parasitic modulation response, it is essential to have capacitance and resistance as small as possible.

### 5.1. Basic structure design

VCSEL structure design consists of three major parts, Bragg reflectors, cavity and active region. Since the light in a VCSEL is propagating perpendicular to the chip surface, the gain medium is much shorter compared with an edge emitting laser. In order to obtain enough gain to compensate the loss for lasing, high feedback from the mirrors is necessary, which requires high reflectivity from the reflectors, normally >99.9% reflectivity for the back mirror and >99% reflectivity for the front mirror. The introduction of distributed Bragg reflectors (DBR) into VCSELS solved this problem and significantly boosted VCSEL performance with ability to grow good quality mirrors by metalorganic chemical vapor deposition (MOCVD) or MBE [38]. The spectral dependent reflectivity of a DBR can be found by transfer matrix method. Figure 5-1 demonstrates the calculated reflection spectral of the p- and n-mirrors of a top-emitting 985 nm VCSEL.

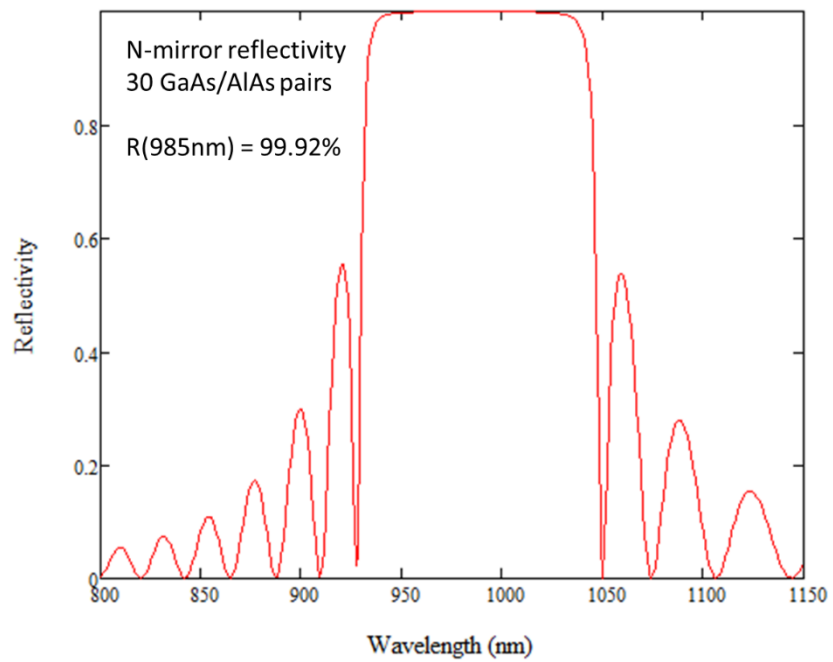
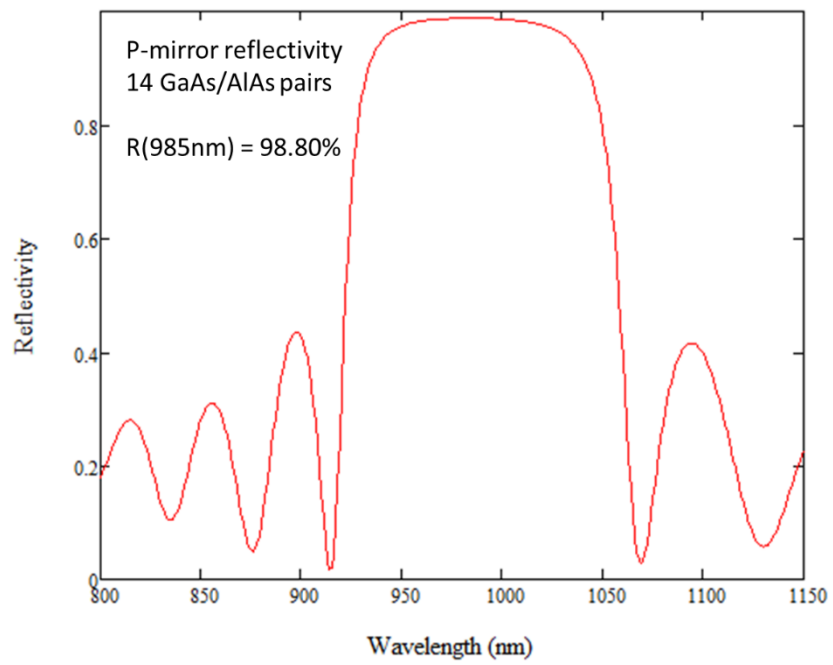


Figure 5-1: Calculated wavelength dependent reflection spectral of the p- and n-mirror of a 985 nm VCSEL, with reflectivity of 98.80% and 99.92%, respectively.

For the cavity design, one needs to decide the cavity length, choose the material for cavity spacer, and carefully place the quantum wells in the cavity to get maximum overlap with the electric field, as illustrated in Figure 5-2. The VCSEL has a  $1-\lambda$  cavity with 3 InGaAs quantum wells in the center, overlapped with an anti-node of the standing-wave in the cavity.

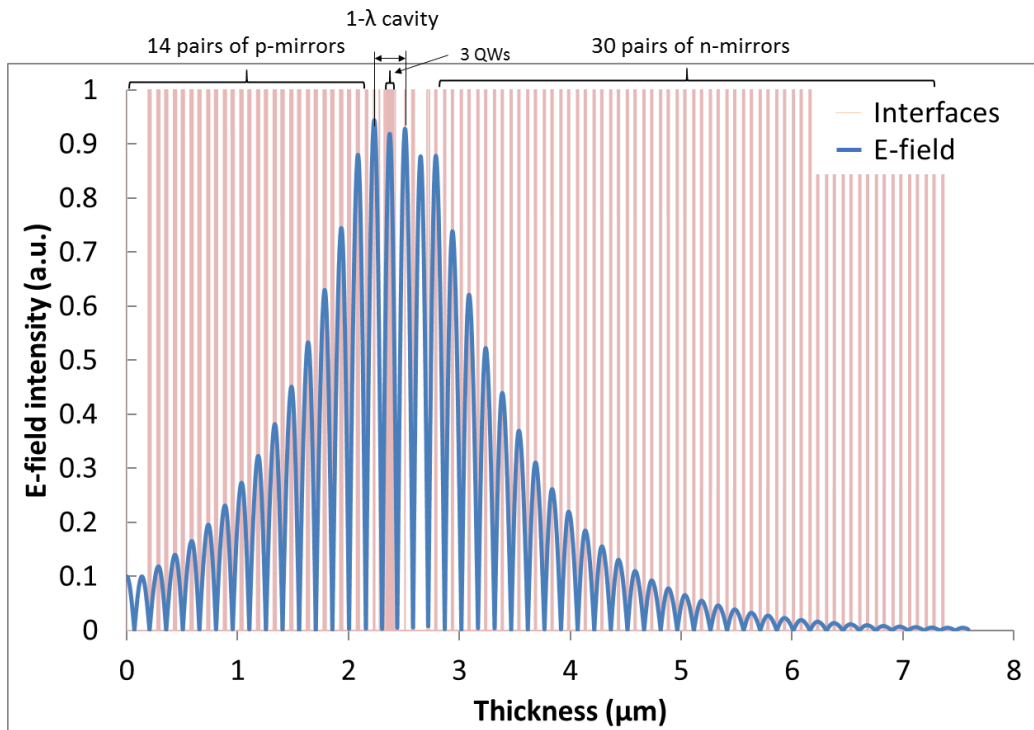


Figure 5-2: Calculated electric field intensity distribution of a standing-wave in a VCSEL by transfer matrix method.

Putting the cavity between two well-designed DBRs, one can find the resonant wavelength of a VCSEL by measuring the reflection spectrum. Figure 5-3 demonstrates the resonance showing up in the center of the reflectivity band for a 985 nm VCSEL from both simulation (top) and measurement (bottom). This dip indicates the lasing wavelength which is set by the two DBRs and will shift to longer wavelength at junction temperature due the refractive index change and thermal expansion.

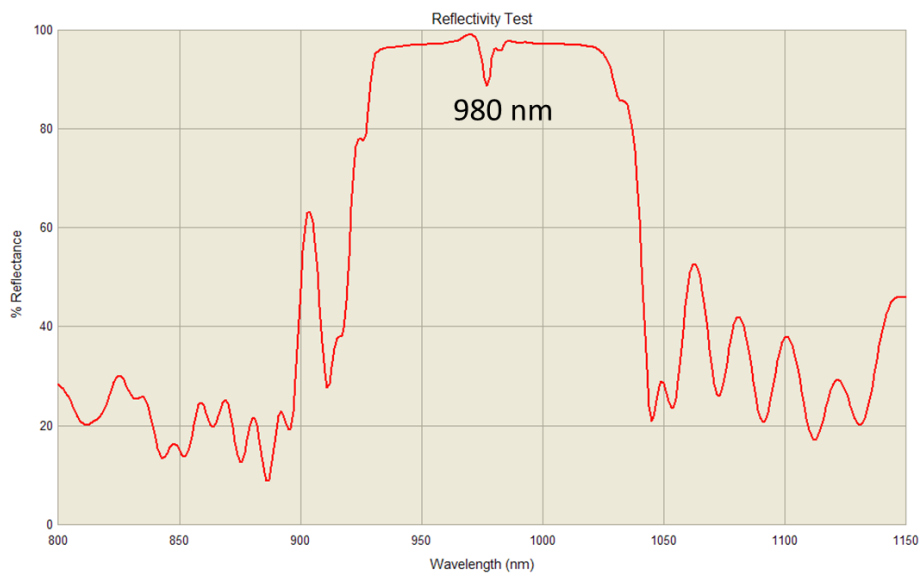
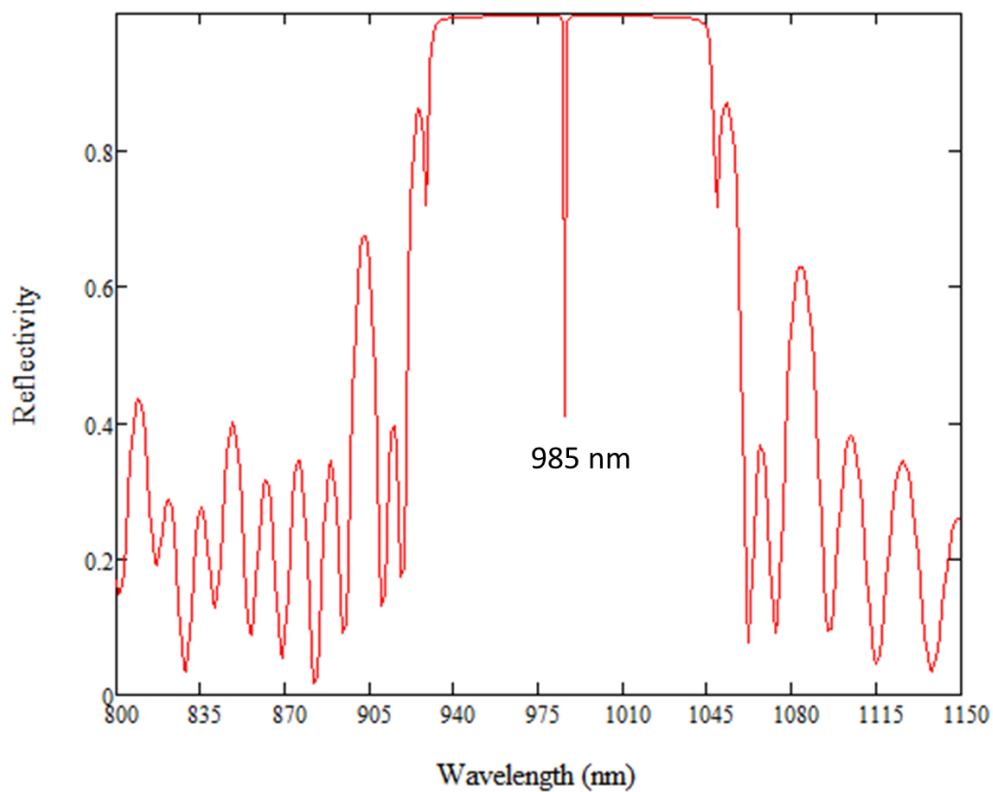


Figure 5-3: Resonant wavelength .of a 985 nm VCSEL from simulation (top) and measurement (bottom).

The measurement of the resonant wavelength is very helpful because it tells us the lasing wavelength immediately after the epitaxial growth and the quality of the grown DBRs. The offset of the resonant wavelength between the simulation and measurement comes from the error during growth rate calibration, which can be reduced by growing a calibration mirror or using *in situ* real time monitoring reflection high-energy electron diffraction (RHEED) during the epi-growth.

Active region design requires considerations of the material, thickness and number of quantum wells and barriers to get low threshold gain and desired gain peak. The gain peak is usually designed at a wavelength shorter than lasing wavelength for wide temperature range operation due to detuning. This can be verified by a photoluminescence measurement, as shown in Figure 5-4.

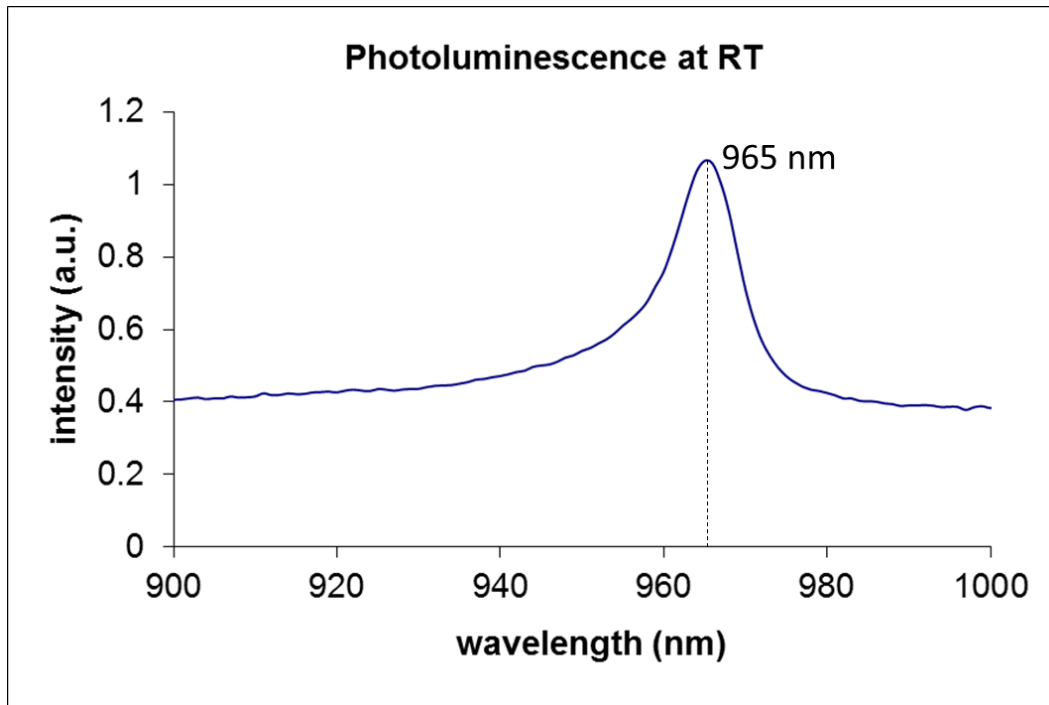


Figure 5-4: Photoluminescence measurement of the quantum wells of a VCSEL.

## 5.2. Intrinsic modulation response

### 5.2.1 Differential gain

As discussed above, large intrinsic modulation bandwidth requires large differential gain and photon density. To obtain large differential gain, one can try to reduce the cavity length to improve the carrier transport [39, 40]. Reducing the threshold current also helps increasing the differential gain. Figure 5-5 illustrates how the gain tracks with the injected carrier density or current. The gain increases approximately linearly with injected carrier density until a certain point after the threshold and eventually saturates at high carrier density. As a result, the slope, i.e. the differential gain decreases with the increase of the injected carrier density. The carrier density making zero gain is called transparency carrier density  $N_{trans}$ . Keep increasing carrier density, the gain will balance the loss at the threshold carrier density  $N_{th}$  or threshold current density  $J_{th}$ . The closer the threshold carrier density to the transparency, the larger differential gain can be produced.

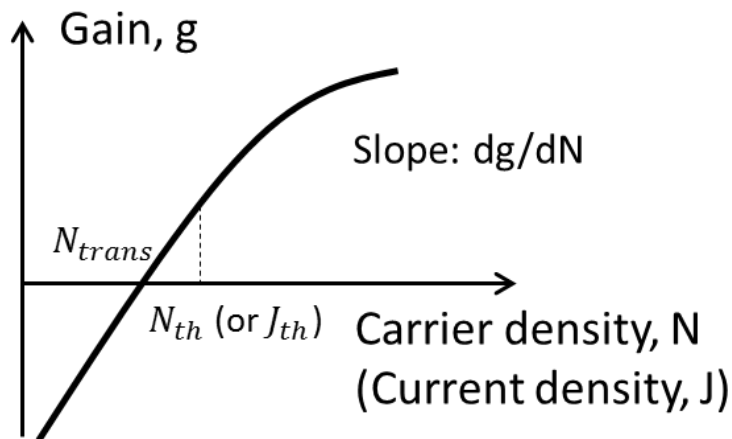


Figure 5-5: Photoluminescence measurement of the quantum wells of a VCSEL.

Several techniques have been employed to reduce the threshold current density. One of them is to use multiple quantum wells in the active region, so that each quantum well can produce less gain to compensate the loss, thus less carrier density is needed. However, putting too many quantum wells will decrease the gain enhancement factor [28] of a VCSEL. For our current structure, three quantum wells are found to be an optimized option.

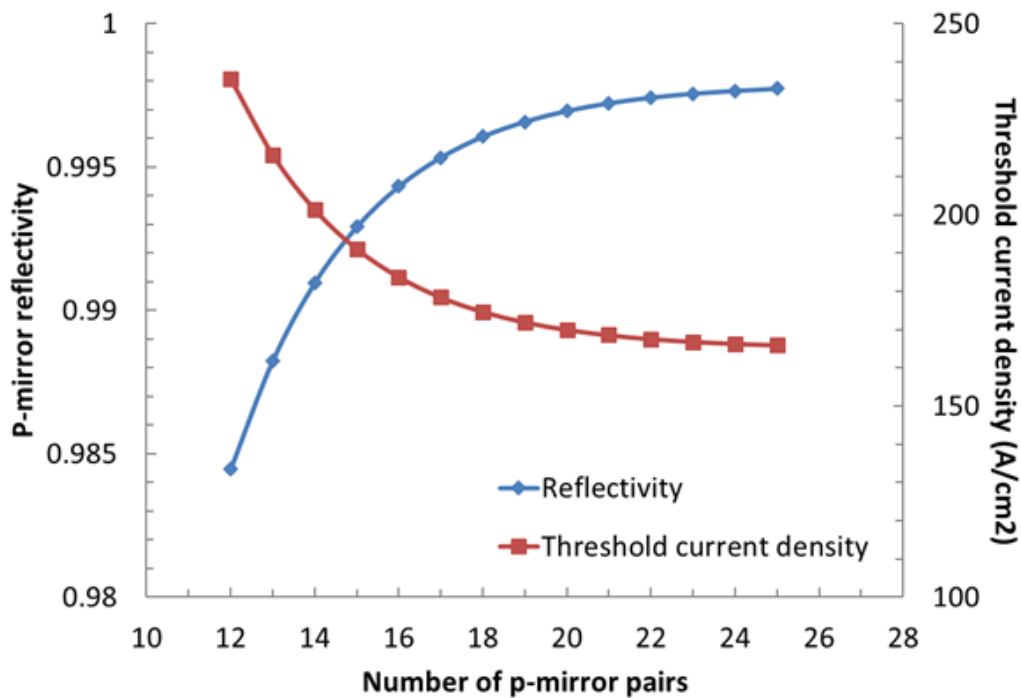


Figure 5-6: P-mirror reflectivity and threshold current density vs. number of p-mirror pairs.

Another way is to design high reflectivity mirror for producing low threshold current density because of the large feedback from the reflector. Figure 5-6 shows the simulated p-mirror reflectivity and threshold current density as functions of number of p-mirror pairs while the n-mirror reflectivity is fixed. The mirror reflectivity increases with the number of mirror pairs, thus reducing the threshold current density.

Normally the threshold of a laser diode rises at high ambient temperature, degrading device efficiency and output power. Carefully setting the detuning between the gain peak and the lasing wavelength, i.e.  $\Delta\lambda = \lambda_{gain} - \lambda_{laser}$  can widen the temperature range of operation. As depicted in Figure 5-7, the gain spectrum red shifts faster than lasing wavelength as the temperature rises. If the gain peak wavelength is set shorter than the lasing wavelength at low temperature, the lasing mode will have large gain over a wide temperature range, enabling low threshold within this temperature range.

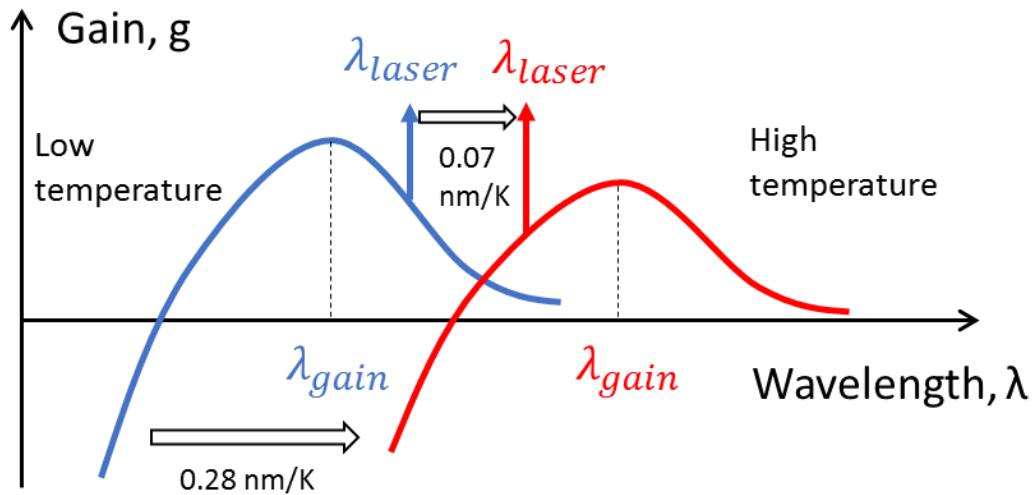


Figure 5-7: Detuning between the gain spectrum and lasing wavelength.

Figure 5-8 shows the comparison between two VCSEL structures with different detuning wavelength  $\Delta\lambda$ . Both lasers are lasing at 980 nm at RT. Structure B with smaller detuning wavelength shows a rapid rise of threshold current density while Structure A remains working at low threshold current density until the temperature is above 100 °C. At 85 °C, a typical high operating temperature for optical data links, the threshold current density of Structure B is five times higher than that of Structure A.



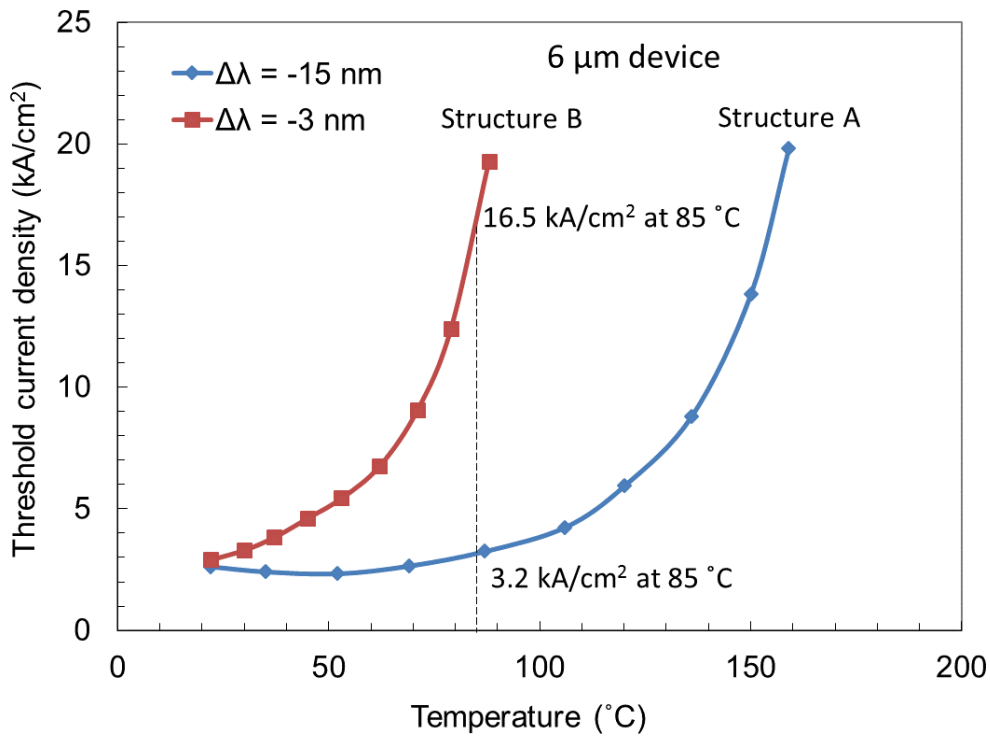


Figure 5-8: Threshold current density as a function stage temperature for two VCSEL structures with different detuning settings.

### 5.2.2 Photon density

To achieve high photon density, the simplest method is to reduce the device size. The smallest commercial available oxide VCSEL is about 3  $\mu\text{m}$  due to the difficulties in precise oxidation control. In contrast, lithographic VCSELs can be reduced as small as 1  $\mu\text{m}$  with good uniformity. Sub-micron size lithographic VCSELs are predictable using high resolution photo mask and aligner.

Another way is to increase the output power. According to Equation (3.12), the output power is proportional to the differential quantum efficiency, i.e. slope efficiency in percentage,

which can be designed by varying the reflectivity of the mirrors. Figure 5-9 shows the calculated p-mirror reflectivity and slope efficiency in terms of the number of p-mirror pairs for a top-emitting VCSEL. The reflectivity of n-mirrors remains unchanged. Apparently, low reflectivity gives high slope efficiency, hence high output power. However, reducing mirror reflectivity increases threshold current density, leading to a low differential gain. A trade-off has to be made between the threshold current density and slope efficiency when designing the mirror reflectivity.

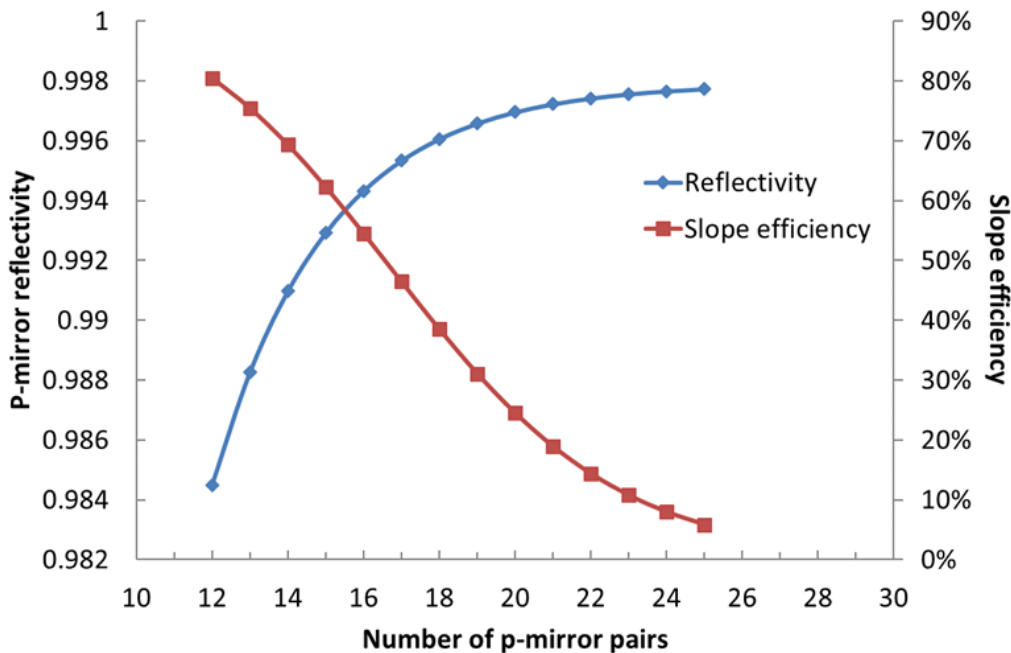
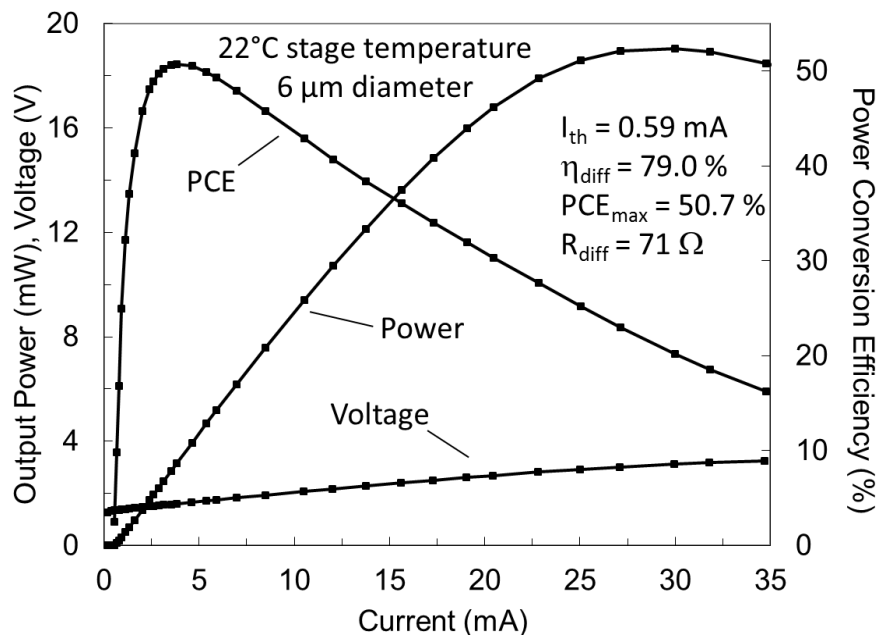
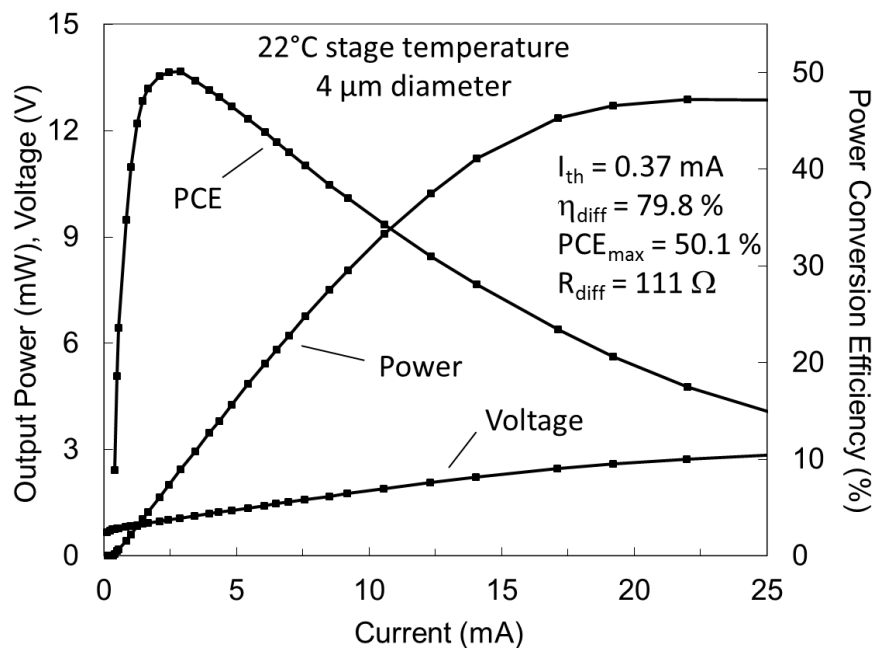


Figure 5-9: P-mirror reflectivity and slope efficiency vs. number of p-mirror pairs.

Besides, high photon density can be achieved by being able to obtain high injected current density due to low thermal resistance, as discussed in Section 4.4. Taking all these into considerations, we have designed and demonstrated lithographic VCSELs with high power conversion efficiency, high output power and relatively low threshold current.



(a)



(b)

Figure 5-10: L-I-V characteristics for (a) 6 μm and (b) 4 μm diameter lithographic VCSELs operating in CW mode at room temperature.

Figure 5-10 shows the L-I-V characteristics of the 6  $\mu\text{m}$  and 4  $\mu\text{m}$  diameter VCSELs lasing as 975 nm [36]. The measurements are for continuous-wave (CW) operation at room temperature without applying any heat sink. The 6  $\mu\text{m}$  device can produce over 19 mW output power which, to our best knowledge, is the highest reported for this size VCSEL operating at CW mode at room temperature. The 4  $\mu\text{m}$  device demonstrates high output power as well, which is over 13 mW. Maximum power conversion efficiency of both devices are over 50 % with differential quantum efficiency close to 80%, which are comparable or even better than most of the commercial and laboratory demonstrated oxide VCSELs. Measured threshold current and differential resistance are 0.59 mA and 71  $\Omega$  for the 6  $\mu\text{m}$  diameter VCSEL and 0.37 mA and 111  $\Omega$  for the 4  $\mu\text{m}$  diameter device, respectively.

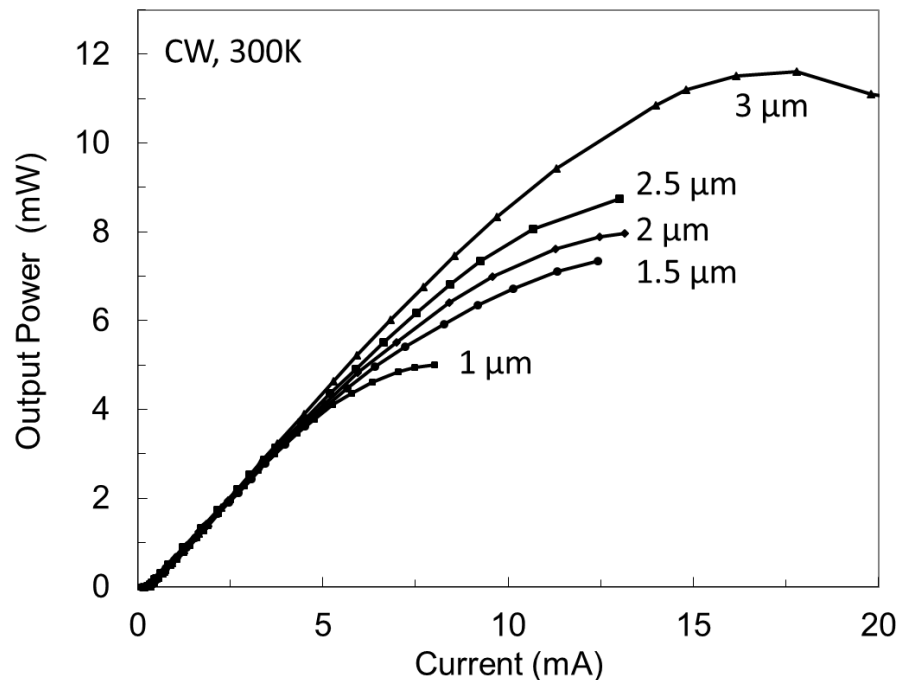


Figure 5-11: Output power vs. current for the 1 - 3  $\mu\text{m}$  diameter lithographic VCSELs measured in CW mode at room temperature.

Owing to better overlapping between the gain and optical mode as well as low thermal resistance, the small size lithographic VCSELs also show high performance under CW mode at room temperature. As shown in Figure 5-11, the maximum output powers for 1, 1.5, 2, 2.5 and 3  $\mu\text{m}$  diameter VCSELs are 5, 7.34, 7.97, 8.74 and 11.61 mW, respectively, which are also, to our best knowledge, the highest output powers demonstrated for the similar size VCSELs [41].

### 5.3. Parasitic modulation response

According to analysis of parasitic modulation response, the capacitance and resistance in VCSELs should be designed as small as possible. The electrical parasitics of a lithographic VCSEL can be attributed to for elements, pad capacitance  $C_p$ , current blocking capacitance  $C_m$ , junction resistance  $R_j$  and mirror resistance  $R_m$ , as shown in Figure 5-12.

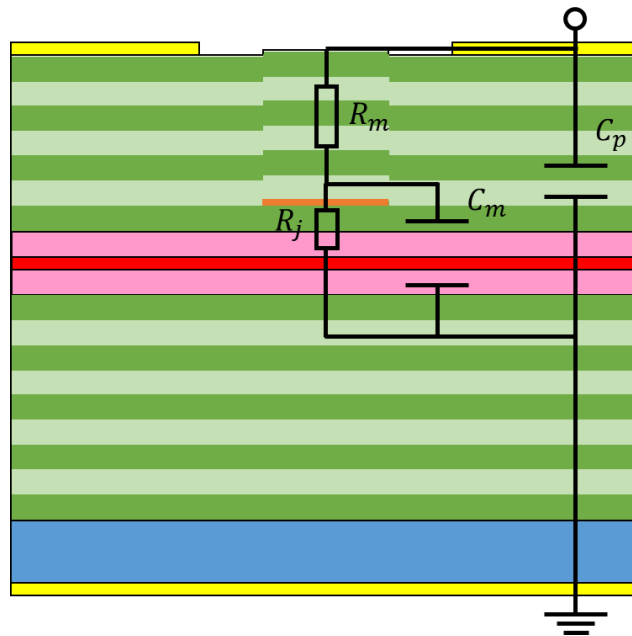


Figure 5-12: Schematic diagram of a top emitting lithographic VCSEL superimposed with equivalent RC parasitics.

The pad capacitance  $C_p$  can be reduced by using small contact pad combined with proton implantation underneath the metal. To obtain small current blocking capacitance  $C_m$  for top emitters, one should design the ring metal contact around the mesa as small as possible but not affecting the current injection efficiency. Applying thick current blocking layer in the structure also helps reducing the capacitance.

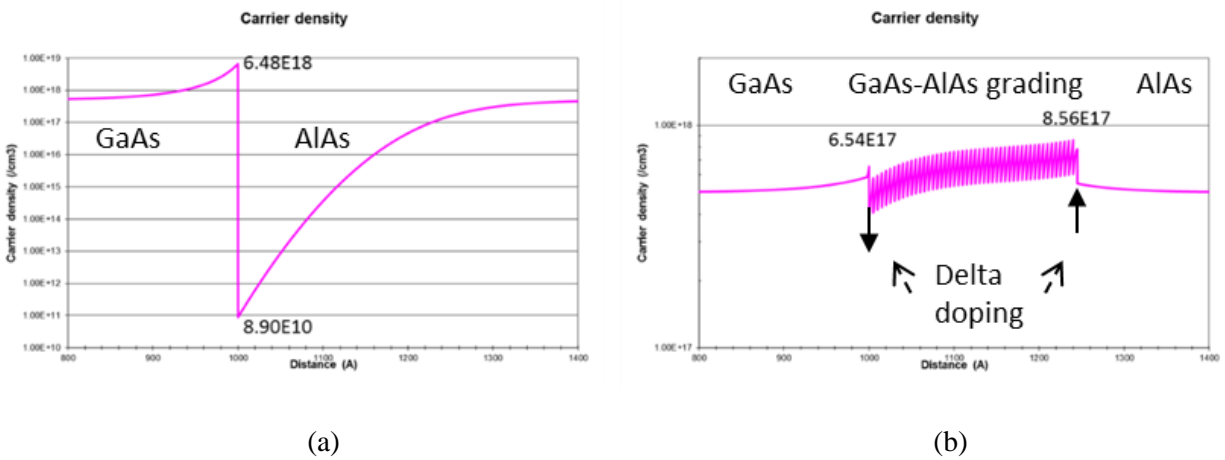


Figure 5-13: Calculated hole density at the hetero-structure interface between GaAs and AlAs without (a) and with (b) grading and delta dopings.

Engineering the resistance in mirrors  $R_m$  is one of the most important parts in VCSEL design. The DBRs of VCSELs consist of a certain number of pairs of two quarter wavelength layers with high and low refractive indices. Simply putting those two layers together will cause carrier depletion at the hetero-structure interface due to discontinuity of the band gap, as illustrated in Figure 5-13 (a). Both layers are supposed to be doped p-type at  $7.5E17 \text{ cm}^{-3}$  while the hole density drops down to  $8.9E10 \text{ cm}^{-3}$  at the AlAs side close to the interface, causing large heterojunction resistance. The band discontinuity can be smoothed by adding gradually changed Al composition AlGaAs layers between GaAs and AlAs. Linear and parabolic grade or

combining of the two have been exploited and applied in those hetero-structure interfaces [42-44]. Figure 5-13 (b) shows a linear grading with a 2% AlGaAs step. However, carrier density peak and valley still exist at the GaAs and AlAs sides, respectively. Delta doping is then applied to those places where the peak is cut down by introducing a thin layer of a few angstroms with n-type doping and the valley is filled up by doping p-type more heavily. Finally, the carrier density is smoothed around the expected doping level.

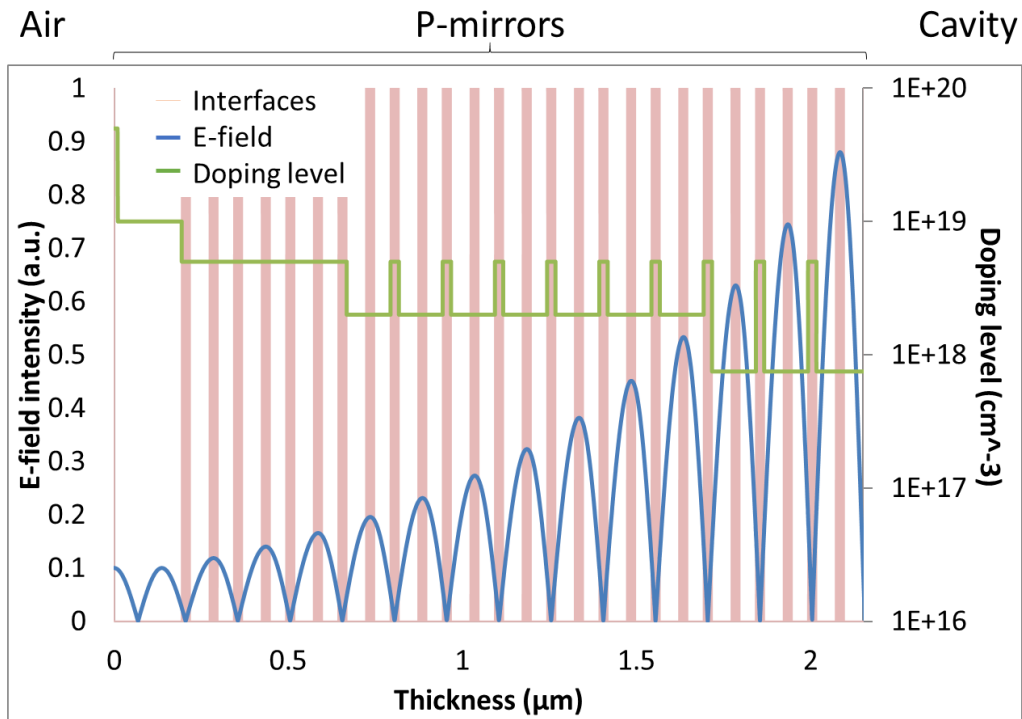


Figure 5-14: Doping profile and normalized e-field intensity in p-mirrors.

For the whole mirrors, the overall doping profile is like a staircase with multiple spikes at the nodes of the standing wave, as illustrated in Figure 5-14. This doping scheme comes from the consideration of the balance between the resistance and free carrier absorption loss for maximum power conversion efficiency. High doping increases conductivity hence reducing the resistance but at the same time introduces more loss especially at places where the electric field intensity is

high. Therefore, we have relatively low doping level in the most of the first three pairs of mirrors close to the cavity but high doping level in the standing wave nodes, because it won't introduce loss at those places due to very low electric field intensity. The doping level is increased in the following seven pairs of mirrors with high doping at the nodes. The last few pairs of mirrors are doped heavily for low resistance and little loss is introduced. The very top layer of the mirror is doped more heavily for reducing the resistance from metal contact.

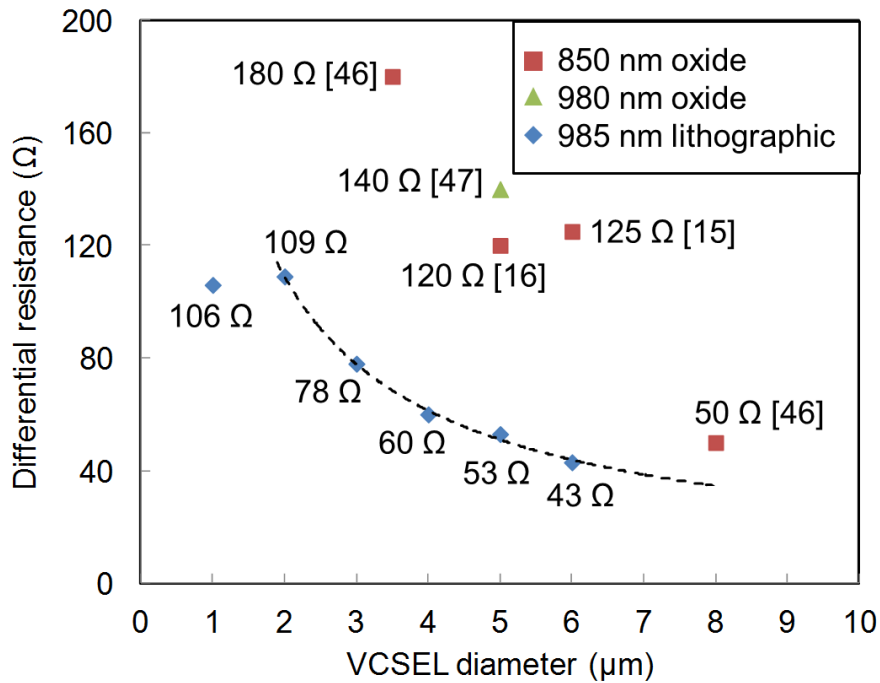


Figure 5-15: Differential resistance as a function of VCSEL size. Squares and triangle: oxide VCSELs with the lowest values of differential resistance found from the published literature. Diamonds: lithographic VCSELs.

An inherent advantage of lithographic VCSELs is the small junction resistance due the removal of the oxide aperture. The junction resistance of an oxide VCSEL mostly comes from the hetero interface between the high Al content AlGaAs layer and the low Al content AlGaAs



layer after it. The techniques used in mirrors for reducing heterojunction resistance do not apply in this situation. Firstly, if a grading is used after the aperture, the high Al content AlGaAs layer in the grading will also be oxidized during aperture formation, which increases optical loss and degrades the device reliability. On the other hand, the doping the layers underneath the aperture makes carrier spreading laterally, resulting in a weak carrier confinement and contradicting the purpose of oxidation. In contrast, lithographic VCSELs eliminates the high Al content AlGaAs layer for oxidation and thus reduces the heterojunction resistance.

By carefully engineering and optimizing the mirrors and cavity, we have demonstrated lithographic VCSELs with record low differential resistance (combination of mirror resistance and junction resistance) for various sizes from 1  $\mu\text{m}$  to 6  $\mu\text{m}$ , as shown in Figure 5-15 [45]. Differential resistance of oxide VCSELs designed for high speed [15, 16, 46, 47] are also plotted as comparison. The differential resistances of the lithographic VCSELs are obtained from measured L-I-V characteristics for CW operation at room temperature. Obviously the lithographic VCSELs can reach differential resistance well below those of previously reported oxide VCSELs for similar sizes.

Compared with the oxide VCSELs in literatures, lithographic VCSELs can maintain higher differential quantum efficiency with lower differential resistance. As shown in Figure 5-16 [45], the values are corresponding to the differential resistance in Figure 5-15. The abrupt drop in differential resistance and differential quantum efficiency of the 1  $\mu\text{m}$  diameter lithographic VCSEL is due to leakage current caused by electrical contacts. Once this issue is resolved, it is expected to produce high power conversion efficiency and high differential quantum efficiency.

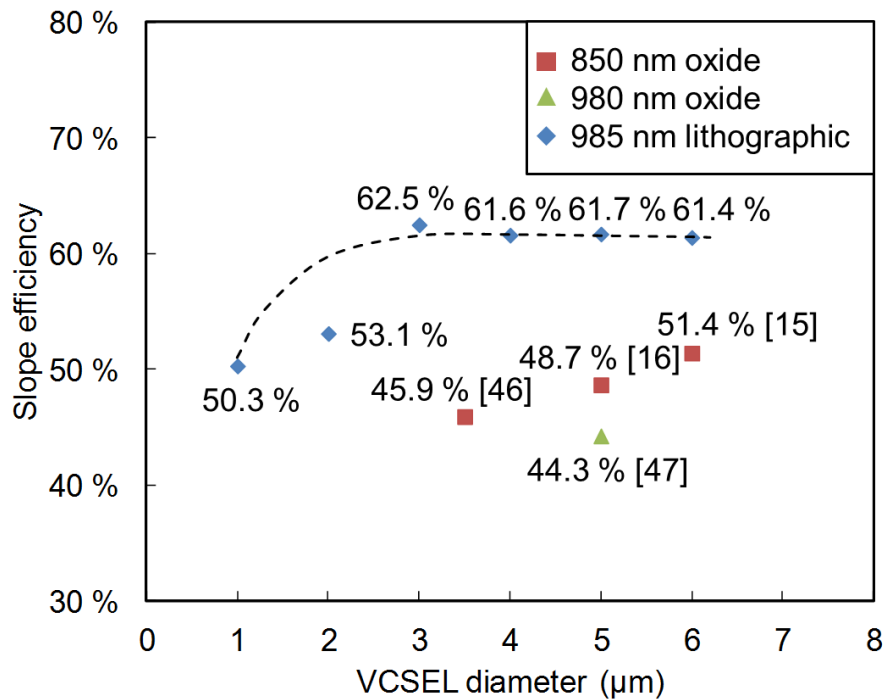
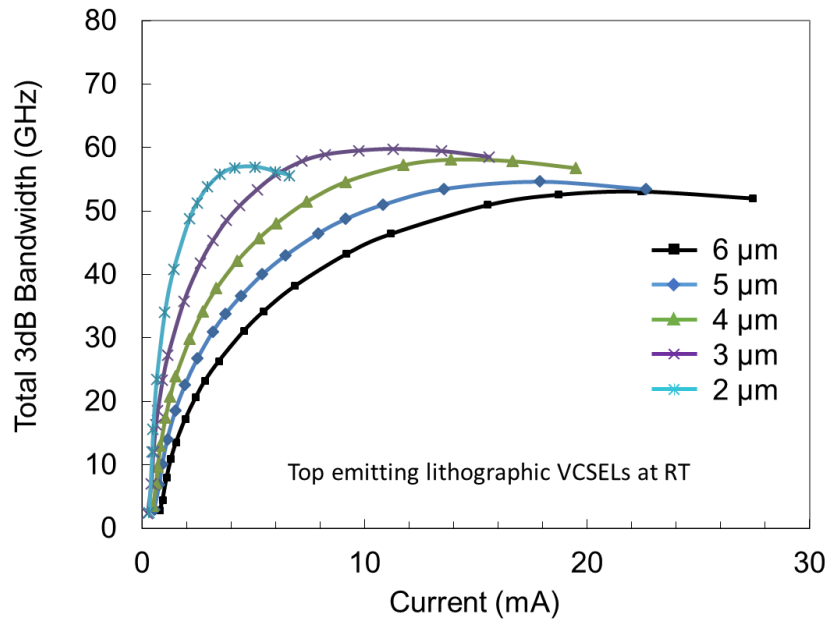


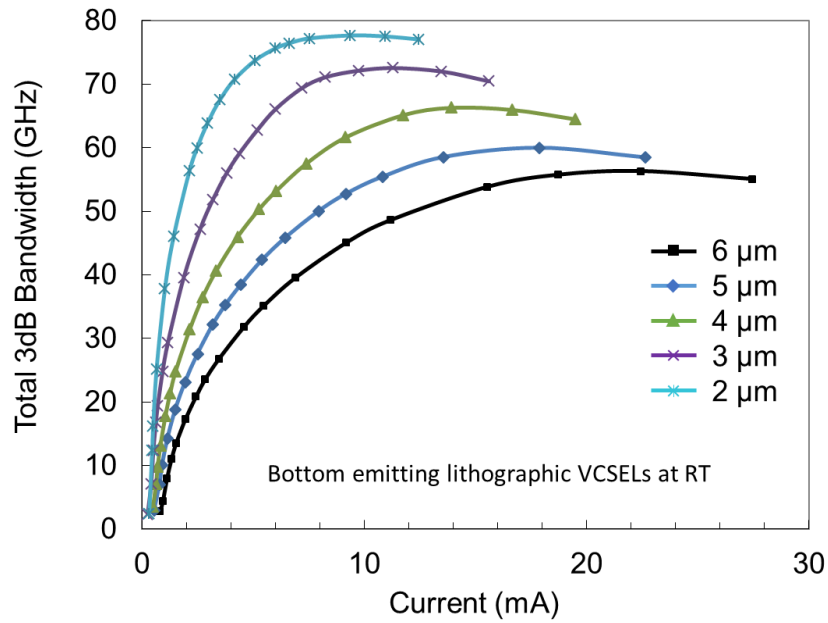
Figure 5-16: Differential quantum efficiency as a function of VCSEL size. Squares and triangle: values corresponding to the differential resistances shown in Figure 5-15. Diamonds: lithographic VCSELs.

#### 5.4. Total modulation response calculations

The transfer function of the total modulation response is the product of the transfer functions of intrinsic and parasitic modulation response in frequency domain, as expressed in Equation (3.43). Applying our intrinsic modulation response model and the parasitic modulation response analysis from Xu Yang's work [48], we are able to calculate the total modulation bandwidth as a function of bias current for our top-emitting lithographic VCSELs, as shown in Figure 5-17 (a).



(a)



(b)

Figure 5-17: Total modulation 3dB bandwidth calculations for (a) top-emitting and (b) bottom-emitting lithographic VCSELs.

The maximum modulation speed is higher for smaller VCSELs except for the 2  $\mu\text{m}$  device. This is because of the rapid rise of differential resistance for small size VCSELs that is proportional to the inverse of the mesa area. The speed of devices smaller than 3  $\mu\text{m}$  is mainly limited by the parasitics. To improve the modulation speed of the small VCSELs by reducing the parasitics, we have designed a bottom-emitting VCSEL structure, as illustrated in Figure 5-18.

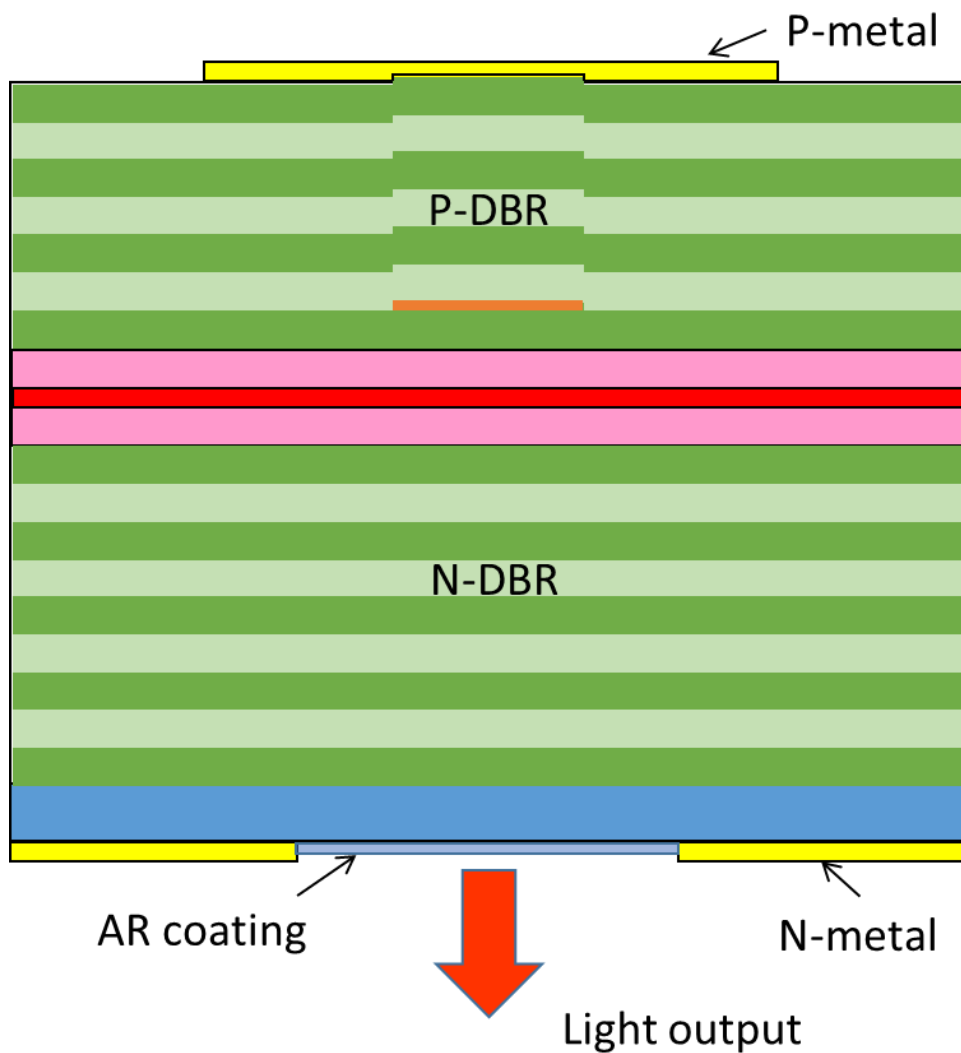


Figure 5-18: Schematic diagram of a bottom-emitting lithographic VCSEL.

The main advantage of the bottom-emitting VCSELs is the low resistance and low free carrier absorption loss due to the reduced number of p-mirror pairs. The p-metal is coated to cover the whole mesa area as part of the DBR and provides high reflectivity due to the large refractive index difference [49]. Therefore, less mirror pairs are needed to reach ~99% reflectivity. For our case, the number of p-mirror pairs are reduced from 13 pairs to 9 pairs. Additionally, the current can flow through the mesa more uniformly compared with a ring metal contact, thus further reducing the mirror resistance. The anti-reflection (AR) layer is deposited on the bottom for better light transmission. Proton implantation is used for reducing the pad capacitance.

According to the parasitics analysis [48], the mirror resistance of the bottom-emitting VCSELs can be reduced by over 50% for the optimal situation. The total modulation bandwidth of various size bottom-emitting VCSELs is calculated and plotted in Figure 5-17 (b). Obviously, the maximum modulation bandwidth of each size is increased and the parasitic limiting effect is reduced for small size VCSELs. The 2  $\mu\text{m}$  bottom-emitting VCSEL can produce over 70 GHz bandwidth, at which over 100 Gb/s data rate can be achieved based on conservative estimation.

## 5.5. Other characteristics

### 5.5.1 Reliability

High speed VCSELs are required to show high reliability for long term operation. The technology of selective oxidation has been intensely studied to improve VCSELs reliability over the years. However, the reliability is limited by defect propagation, which results from increased internal strain around the oxide aperture termination at elevated junction temperature under high

bias current [33]. This defect propagation can be greatly developed by exposing to moisture [37]. The degradation of VCSEL reliability is primarily caused by high junction temperature and injected current density.

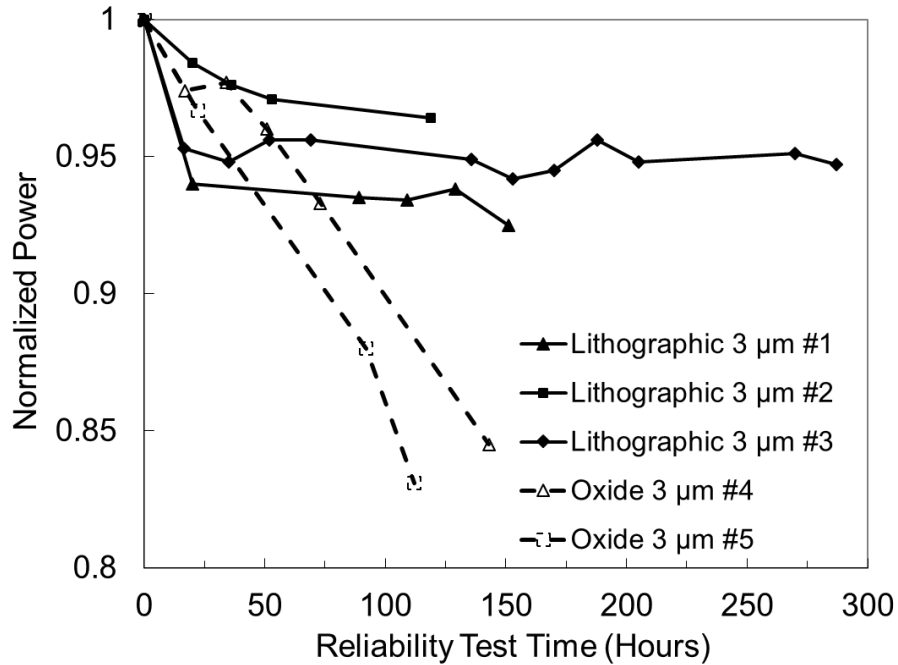


Figure 5-19: Stress test under extreme operation conditions of 140 kA/cm<sup>2</sup> and 150°C for both lithographic and oxide 3 μm diameter VCSELs.

As shown in Figure 5-19, a stress test under extreme operation conditions is performed on both lithographic and oxide VCSELs to show the advantage of lithographic approach over selective oxidation due to low junction temperature [50]. The 3 μm diameter oxide VCSELs are commercial available and are operated at the wavelength of 850 nm, while the 3 μm lithographic VCSELs are lasing at ~960 nm. The VCSELs are tested at a stage temperature of 150 °C with injected current density at 140 kA/cm<sup>2</sup> to accelerate the degradation. After a certain time of operation, the devices are cooled down to room temperature for L-I-V characteristics

measurements. Then the normalized powers versus test time are plotted in Figure 5-19. The output power of the oxide VCSELs continuously drops over the operating time while the output power of the lithographic VCSELs remains stable for longer time after an initial drop at the beginning of the test. The high reliability of lithographic VCSELs under these extreme stress conditions indicates low junction temperature inside the devices and is confirmed by experimental measurements, which is  $\sim 185$  °C while the junction temperature of the oxide VCSELs is  $\sim 225$  °C. These results show that this lithographic and all-epitaxial method is promising to provide superior reliability for applications in harsh environments.

#### 5.5.2 Single mode and single-lobed beam pattern

Single mode operation is favorable for high speed VCSELs due to the low power consumption. Various techniques have been exploited on monolithic and electrically driven VCSELs to achieve single-mode emission by introducing mode-selective gain or loss to suppress higher order modes [51-53] or narrowing the size of waveguide to support the fundamental mode only [54, 55]. Most of these techniques are achieved by forming an oxide aperture, leading to high thermal resistance and difficulties of size control for small VCSELs. In contrast, the lithographic approach can realize much lower thermal resistance and most importantly provide precise size control and easy manufacturability over large area wafers. In this section, lasing spectral and far field beam profiles of a 2  $\mu\text{m}$  901 nm lithographic VCSEL are demonstrated to show the capability of producing single transverse mode with stable beam [56].

In Figure 5-20, the spectra of the 2  $\mu\text{m}$  VCSEL as a function of bias current is plotted on a semi-logarithmic scale. The laser initially emits at a wavelength around 901 nm and then shows

a red shift as driven harder. The VCSEL keeps operating in single transverse mode until 5.3 mA, at which the current density is as high as 169 kA/cm<sup>2</sup> and the output power is 4.1 mW.

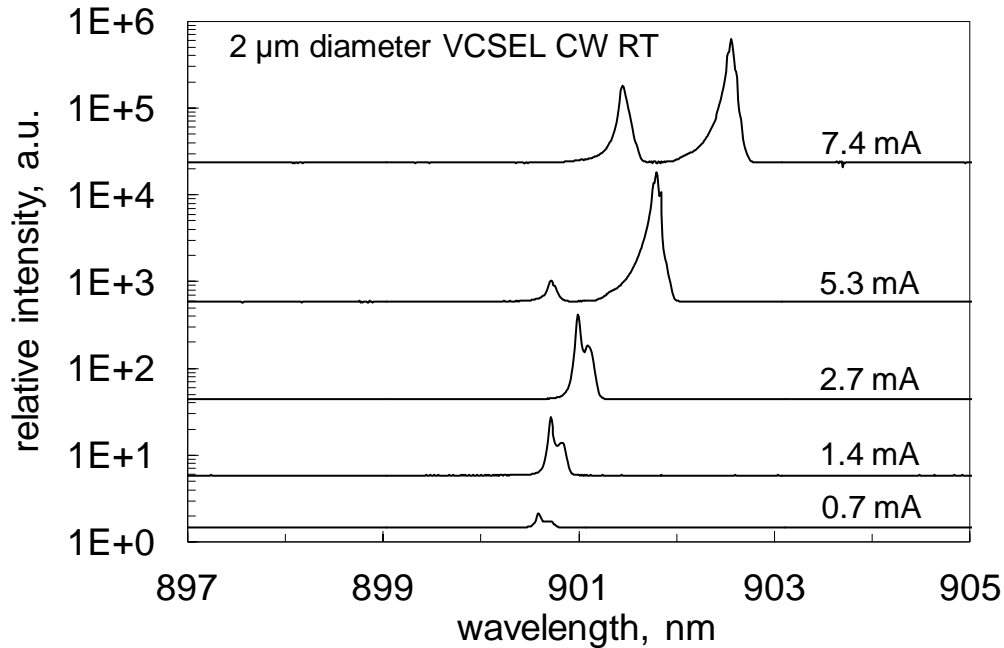


Figure 5-20: Lasing spectra of a 2 μm diameter VCSEL under different bias currents.

The far-field profile of the 2 μm VCSEL is shown in Figure 5-21. The measurable divergence angle is limited by the size of the aperture of the CCD used to capture the beam profiles. Stable beam profile is obtained up to 5 mA and then the broadening starts to show up due to thermal lensing. The full divergence angle is calculated by using Gaussian fit for the measure beam profile. At 5 mA, the full divergence angle is ~12° and then increases to ~25° near thermal rollover. The far-field radiation pattern remains single-lobed over the full range of operation, while for other VCSELs at such high drive level, a typical donut shape will show up. The show up of the second mode at 7.4 mA in Figure 4-7 is consistence with onset of the thermal



lensing in Figure 4-8. This thermal lensing can be avoided by pulsed operation and thus an increase in the maximum power and beam quality can be expected.

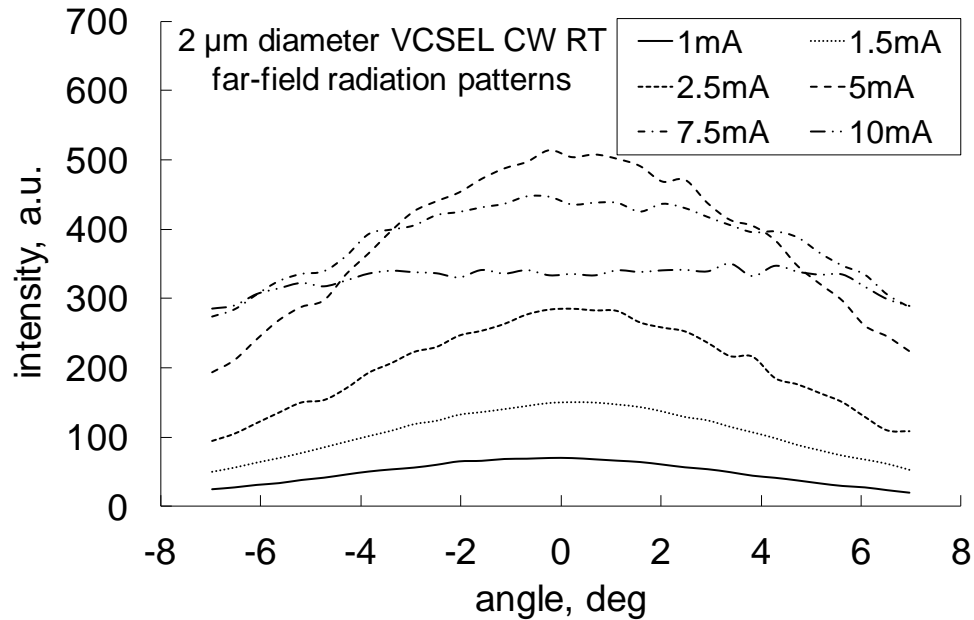


Figure 5-21: Measured far-field radiation patterns of a 2  $\mu\text{m}$  diameter VCSEL under different bias current.

## 5.6. Summary

In this chapter, we have introduced the basic ideas of VCSEL design. To design VCSELs for high speed, it is essential to increase intrinsic modulation bandwidth by improving differential gain and photon density and enhance parasitic modulation bandwidth through reducing the capacitance and resistance. The total modulation bandwidth can be significantly boosted by lithographic VCSELs with small size and low parasitics.

## CHAPTER 6: CONCLUSIONS

In this dissertation, the focus of the work is to develop a mathematical model of intrinsic modulation response and analyze the thermal properties of VCSELs to demonstrate how thermal limits impact on the laser speed. Simulation results show that the intrinsic modulation bandwidth is largely limited by stimulated emission rate as well as the differential gain. Analysis also predicts that small size lithographic VCSELs are highly expected to produce high intrinsic modulation bandwidth due to low thermal resistance and high photon density. The 2  $\mu\text{m}$  diameter lithographic VCSEL is promising to produce over 100 GHz intrinsic modulation bandwidth. The parasitic modulation response is also briefly discussed. The results predict an over 70 GHz total modulation bandwidth produced by a 2  $\mu\text{m}$  lithographic VCSEL, enabling over 100 Gb/s data rate by estimation.

For high speed VCSELs, the intrinsic modulation bandwidth can be increased by designing large the differential gain and high photon density and the parasitic modulation bandwidth can be improved by reducing the capacitance and resistance and using a bottom-emitting scheme.

The characteristics of lithographic VCSELs has demonstrated comparable or even better performance over oxide-confined VCSELs. The intra-cavity phase shifting mesa provides better scalability and uniformity for device diameters ranging from 1  $\mu\text{m}$  to 6  $\mu\text{m}$ . The removal of the oxide aperture eliminates the internal strain caused by point defect and dislocation around the termination of the aperture, leading to a significant improvement in reliability. The thermal resistance of lithographic VCSELs is greatly reduced due to better heat spreading in the junction,

which allows wider operation temperature range, higher injected current density and stronger stimulated emission rate, resulting in higher output power and faster intrinsic modulation speed.

Future works will be developing process flow for high speed VCSELs as well as refining the intrinsic modulation response model for better design guidance. Densely packed high power single mode 2-D VCSEL arrays using lithographic approach are also attractive for future research.

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