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Transient Safe Operating Area (tsoa) For Esd Applications

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TRANSIENT SAFE OPERATING AREA (TSOA) FOR ESD APPLICATIONS

by

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ABSTRACT

A methodology to obtain design guidelines for gate oxide input pin protection and high voltage output pin protection in Electrostatic Discharge (ESD) time frame is developed through measurements and Technology Computer Aided Design (TCAD). A set of parameters based on transient measurements are used to define Transient Safe Operating Area (TSOA). The parameters are then used to assess effectiveness of protection devices for output and input pins. The methodology for input pins includes establishing ESD design targets under Charged Device Model (CDM) type stress in low voltage MOS inputs. The methodology for output pins includes defining ESD design targets under Human Metal Model (HMM) type stress in high voltage Laterally Diffused MOS (LDMOS) outputs. First, the assessment of standalone LDMOS robustness is performed, followed by establishment of protection design guidelines. Secondly, standalone clamp HMM robustness is evaluated and a prediction methodology for HMM type stress is developed based on standardized testing. Finally, LDMOS and protection clamp parallel protection conditions are identified.

To my parents Milos and Zdenka

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LIST OF ACRONYMS

BiCMOS	Bipolar Complementary Metal-Oxide-Semiconductor
CAD	Computer Aided Design
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide-Semiconductor
DUT	Device Under Test
ESD	Electrostatic Discharge
ESDA	Electrostatic Discharge Association
FA	Failure Analysis
GGMOS	Grounded Gate MOSFET
HBM	Human Body Model
HMM	Human metal Model
LVTSCR	Low-Voltage-Trigger SCR
IC	Integrated Circuit
IEC	International Electrotechnical Commission
IEC-61000-4-2	International Electrotechnical Commission ESD standard

LOCOS	Local Oxidation of Silicon
MM	Machine Model
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
SCR	Silicon Controlled Rectifier
SoC	System-on-a-Chip
STI	Shallow Trench Isolation
TDDB	Time Dependent Dielectric Breakdown
TCAD	Technology Computer Aided Design
TLP	Transmission Line Pulse

CHAPTER 1
INTRODUCTION

In order for Integrated Circuit (ICs) containing products such as cell phones, laptops, medical appliances, cars to be on the market, they need to pass certain reliability tests [1,2]. One set of reliability tests required pertains to Electrostatic Discharge (ESD) [3] group. These tests are summarized in different standards or given to the manufacturer by the IC customer. The ESD test standards required for an IC to pass differ based on where the IC is: standalone or integrated into a system. ESD induced failures account for about 35 % of IC manufacturers customer returns [4] and therefore, significant effort is put to minimize this number.

In ESD protected areas (EPA) the integrated circuits (ICs) need to pass a certain level of standard stress types such as Charged Device Model [5], Human Body Model [6], and Machine Model [7]. The EPAs are: fabrication environment, IC Assembly and Test environment, and Assembly and Repair environment [8]. In a fabrication environment, ionizers are installed to prevent discharge to ground. In the latter two environments, proper grounding and ionizers are also installed to lower the ESD threat. A detailed reference about reliability standards including ESD standards, their evolution and the entities that issue them is by Bisschop [1]. Once the ICs are mounted on the board they need to be

able to pass certain levels of system level tests depending on the final application. Each stress model previously mentioned emulates a specific kind of event in which a discharge of a particular kind occurs.

1.1 Electrostatic Discharge Models and Characterization

Each electrostatic discharge event has its representation as an equivalent RLC circuit [9, 10], with a capacitor charged to a certain voltage level, usually represented in kilo Volts (kV). Different stress types are typically described by: rise time, duration(typically given as 3RC constants) and peak or multiple characteristic current peak values.

1.1.1 Human Body Model

Human Body Model (HBM) emulates a human discharging into an IC. The standard HBM required pass level is about 2kV [8], although 1kV is in discussion for component level ESD because the operators do not charge more than 100 V and the risk of damage is low [11]. The equivalent RLC circuit model and its values are shown in Figure 1.1. HBM typical rise time is about 10 ns and the duration of approximately 3RC constants is about 450 ns. The peak current is 0.67A/kV [6].

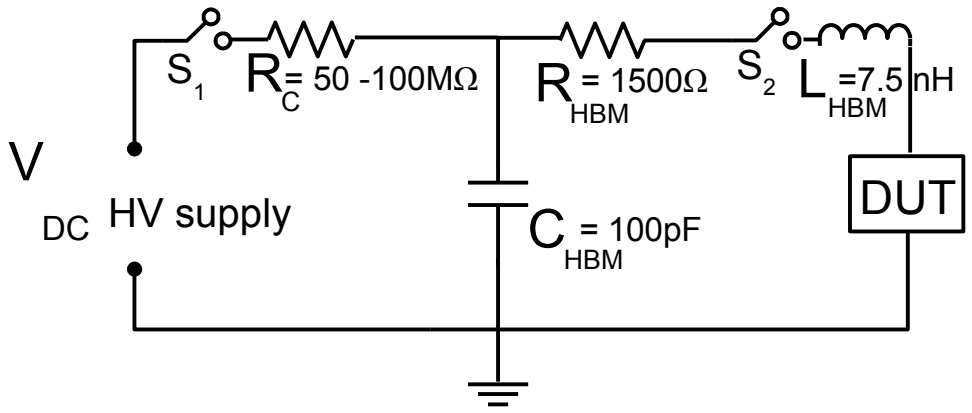

Figure 1.1: Equivalent HBM circuit

Transmission Line pulsing (TLP) technique is commonly used to evaluate and estimate HBM robustness. Simplified equivalent circuit schematic of TLP technique is shown in Figure 1.2. The simplified schematic consists of high voltage source that charges a capacitor which in turn discharges through a 50 ohm transmission line. The capacitor is charged in increasing voltage steps and discharged through the DUT until failure is detected either by the change in leakage current or DC parameter degradation [12]. The TLP system used in this study is Barth 4002 [13]. The capacitor is charged to 2Vpulse value, as Vpulse is defined as voltage on 50ohm load.

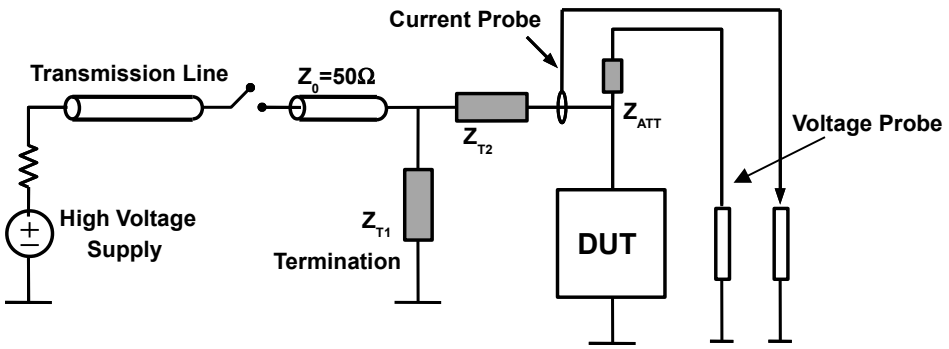

Figure 1.2: Schematic view of the TLP tester

The commonly used duration of the Transmission Line Pulse (TLP) stress is 100 ns. Other pulse widths are implemented [14], too. TLP stress of 100 ns duration and 10 ns rise time has been correlated to HBM pass levels [12], hence the use of TLP to estimate HBM pass levels on wafer with the following ratio: 1.3A TLP current correlates to 2kV HBM pass level. The correlation is based on the peak current of HBM pulse being the same as the peak current of TLP pulse [12].

1.1.2 Machine Model

Machine Model (MM) represents the interaction of a charged machine and a component or IC. The typical required pass level is 200V [8]. Equivalent circuit is the same as in Figure 1.1 with different circuit element values R= 15 ohm, C=200pF and L=1.5 μH [10]. Due to the very low resistance in the path the current peaks for MM are much higher then HBM. A correlation between HBM and MM stress was previously achieved [15].

1.1.3 Charged Device Model

Charged Device Model (CDM) emulates the event in which the pin of a pre-charged integrated circuit (IC) comes in contact with a grounded metallic surface. CDM is a high current ESD event with a rise time about 100 to 200 ps. This event is either produced by direct charging or through field induced charging modeled respectively as Charged Device Model (CDM) or Field Induced CDM (FICDM) [16, 17]. During this ESD event, a high voltage overshoot is obtained in the initial picoseconds, which requires the ESD protection device to be designed to turn-on fast enough to dissipate the charge [18]. These failures are frequently found in the gate oxide [16,19–21] and shallow junctions of core-circuit transistors [22]. The typical CDM required pass level is about 1kV [8]. Correlation between HBM, MM and CDM was studied with the result that CDM does not correlate to HBM and MM, while HBM and MM correlate [23].

One of CDM failure modes is gate oxide damage at the input receiver, where the voltage across the gate oxide reaches a critical value thus damaging the gate [16, 21, 24, 25]. Another failure mode under positive stress is between gate and drain overlap region in a protection device such as grounded gate MOSFET [26].

Equivalent circuit model for CDM is more involved as it depends on the tester used and has been reported in [27] , [28]. CDM emulates the fastest ESD event, depicting a rise time and a total stress duration in the picoseconds and nanoseconds regime, respectively. This ESD event simulates the positive or negative charge build-up in the integrated circuit

(IC) die and package through direct contact charging or through field induced charging [9]. The electrostatic discharge is generated via direct ground contact of one of the ICs input/output (IO) pins. This ESD event is very common in automated IC handling and assembly. Consequently, it is nowadays widely considered to be the leading cause of ESD induced IC failure.

The CDM waveform is difficult to reproduce because it is highly dependent on the testing method, the die and the size of the IC package, among others [29]. To use a more controllable measurement strategy and be able to gain insight in the phenomena taking place in the CDM-time domain, Very-/Ultra- Fast Transmission Line Pulsing (VFTLP/UFTLP) [30], with a pulse rise time in the hundreds of picoseconds and pulse width less than ten nanoseconds, is currently being used to assess CDM-like device response and CDM-induced failure. The standard TLP stress, on the other hand, provides a minimum of 200 ps rise time and 100 ns pulse width. The one used in this study is Barth VFTLP system [31] which produces pulses of 1,2,5 and 10 ns duration with rise time of 0.1, 0.2 and 0.4 ns.

VFTLP system has been used for CDM robustness evaluation [32–35] and in general to evaluate fast transient response of different structures [36,37]. The direct correlation with VFTLP as in the case of HBM type of stress is not performed due to the difference in stress dynamic: during VFTLP stress is applied between two pins and response between those two pins is measured. On the other hand, in CDM event the source of the charge is the whole package that discharges through one pin to the ground. A correlation for a variation of VFTLP test called Capacitively Coupled TLP (CC-TLP) [38] has been studied based on

peak current values. An introductory tutorial describing TLP and VFTLP testing can be found in [39].

1.1.4 System Level Stress and Component Level Stress

Once an IC is mounted on a board and a system is built, a system level test is required called IEC 61000-4-2 [40]. For some applications, communication lines such as Controller Area Network (CAN), Local Interconnect Network (LIN) and Flexray [41] are externally connected at the system level and are directly exposed to system level stress [14, 42]. Moreover, in some automotive cases there is a requirement of no additional external ESD solutions [42]. Therefore, an IC in some cases needs to withstand system level IEC stress, and a new standard practice called Human Metal Model (HMM) has been established to address the need for system level stress on the component level. It is at this point a standard practice used to evaluate components of the system and even device level ESD robustness to IEC type of ESD [43]. The equivalent circuit is the same as for the IEC standard shown in Figure 1.3.

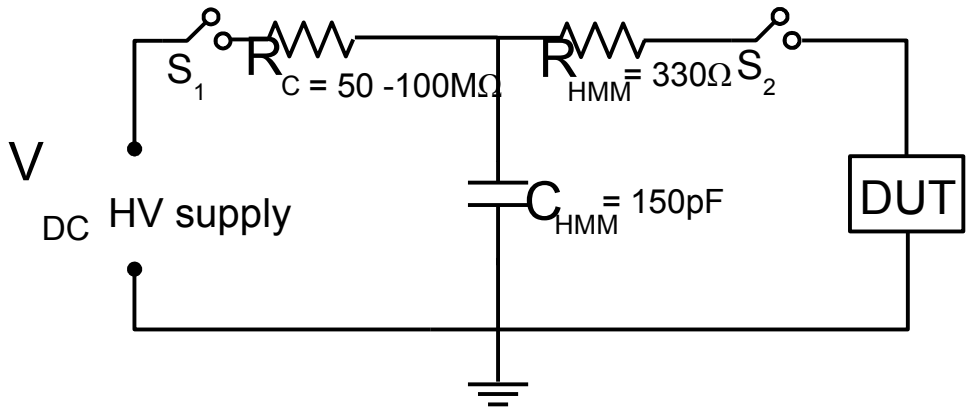

Figure 1.3: HMM and IEC equivalent circuit

The main difference between the IEC and HMM is the location where the stress is applied as illustrated in Figure 1.4. While IEC is applied at the system level in which case some external system level protection element may be used, the HMM is applied at the component level. As was stated earlier in some applications the external element cannot be used, making HMM and IEC test the same.

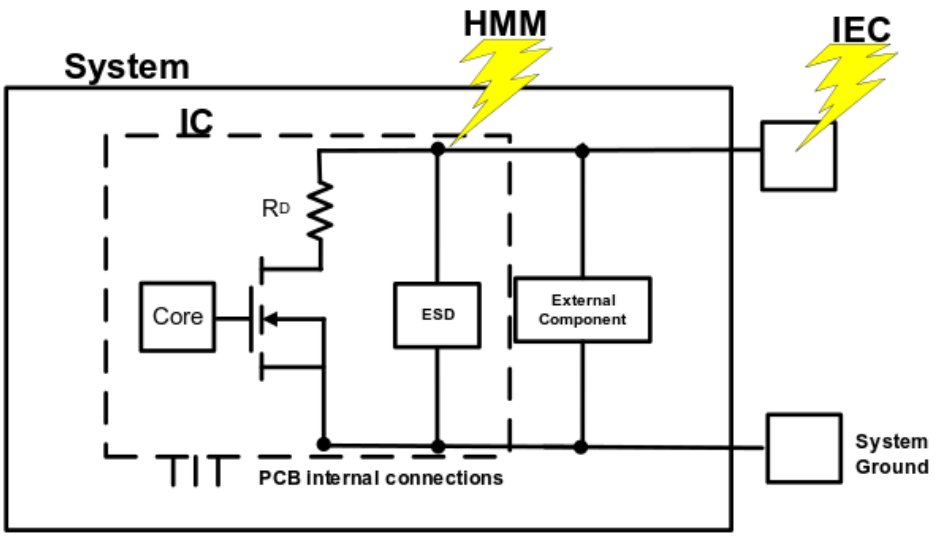

Figure 1.4: Illustration of the difference between HMM and IEC

The HMM/IEC tester used in this study is Hanwa W5000M system for wafer-level HMM [44]. The experimental setup used is shown in Figure 1.5. It uses current probe CT1 [45] to capture the waveform. The scope used is 500MHz scope model TDS3054 by Tektronix with the corresponding voltage probe. Additional 20dB attenuator is needed at the input of the scope for current probe input.

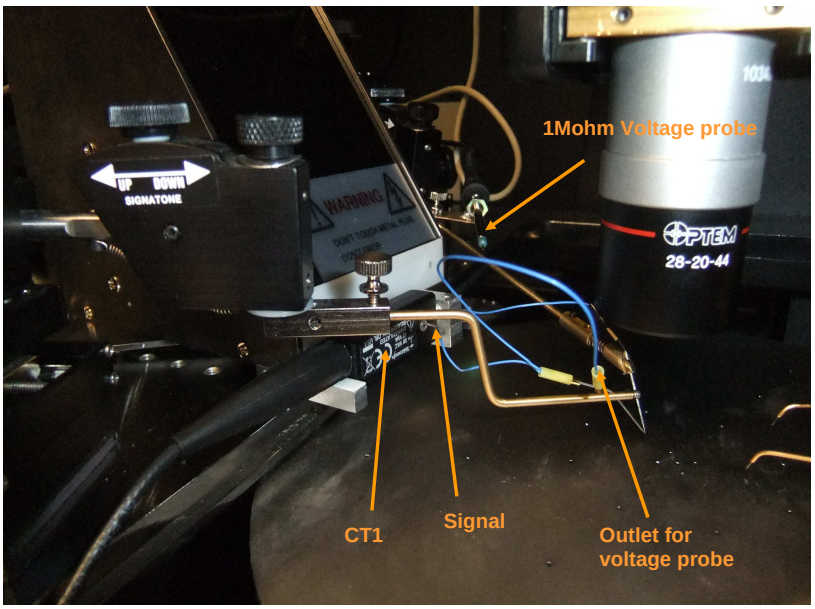

Figure 1.5: Experimental HMM setup description

The HMM standard defines the characteristics of the waveform [43] in terms of rise time, 3RC constants duration of 150 ns and characteristic current peaks listed in table 1.1.

Table 1.1: HMM standard description

Human Metal Model Pulse	Value	Unit
Pulse Rise-time 10 to 90 %	0.8 ± 25 %	ns
First peak current of the discharge (Ip)	3.75 ± 15 %	A/kV
Current at 30 ns from initial 10 % point	2 ± 30 %	A/kV
Current at 60 ns from initial 10 % point	1 ± 30 %	A/kV

Due to the variations in the standard, the tester used in this study was evaluated in terms of peak current values as defined in table1.1. The characteristic peak values are shown in figure 1.6. Notice that the first peak current is on the lowest end of the specification due to the longer cables that were used for ease of testing. On the other hand, the 30 and 60 ns peak current values are about 10 % above the main value given in the table 1.1, thus within 30 % variation allowed.

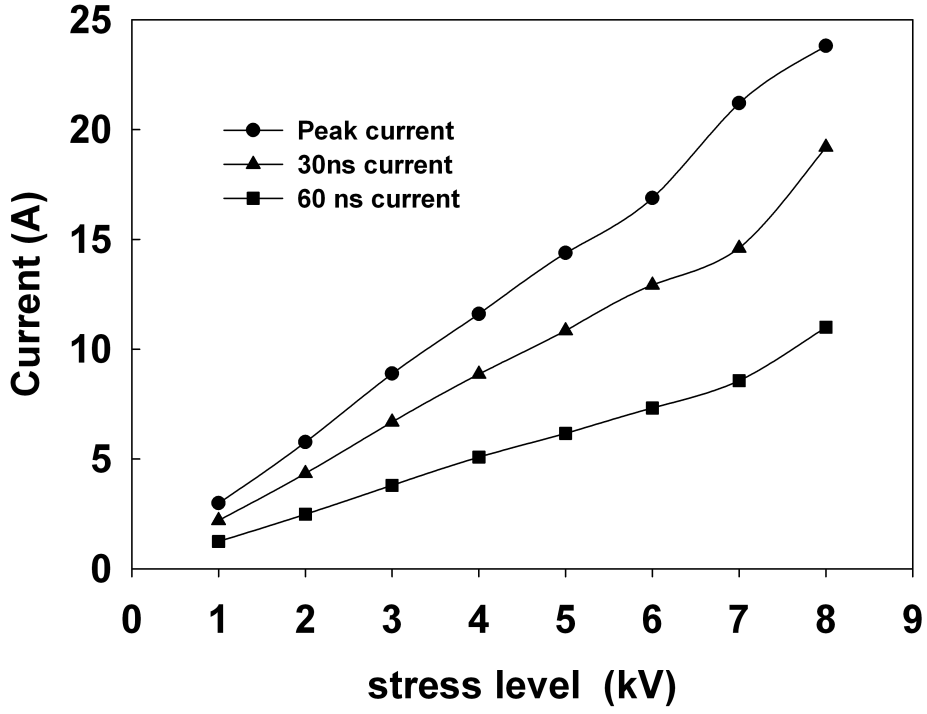

Figure 1.6: HMM characteristic peak current values for the setup used vs. stress level(kV)

In order to measure the impact of different loads on the tester and the impact of probes and the connection cables on the current waveform, the probes were removed and discrete resistors of different values were placed directly in between the terminals. Additionally, for

comparison the probes with all of the connections were placed and the current waveform on a silver short pad was captured at the same 1kV HMM stress level.

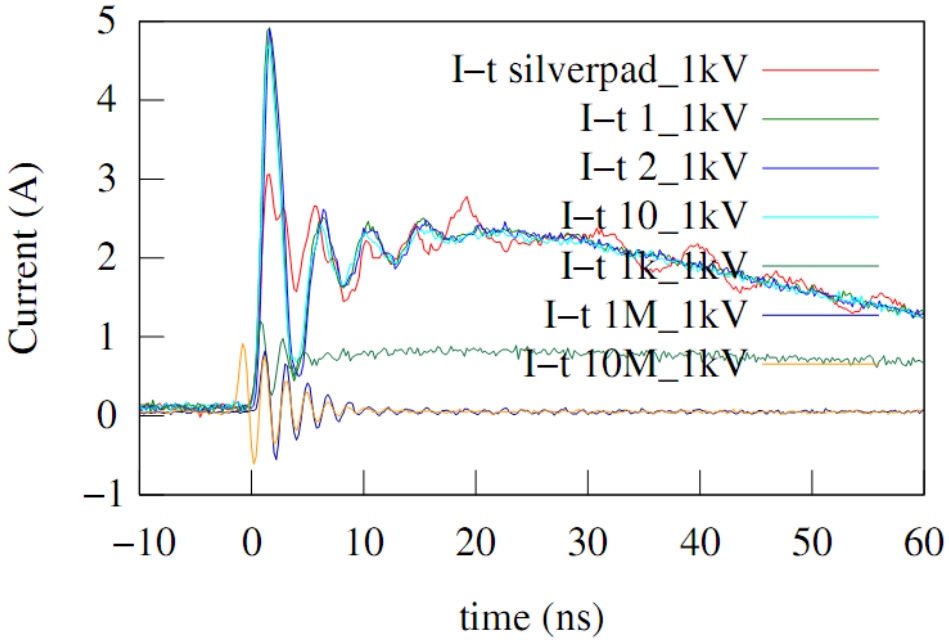

Figure 1.7: Different resistance values and setup influence on HMM current waveform

The current levels scale proportionally to the resistor values, with no major difference seen for 1, 2, and 10 ohm loads as they are well below the 330ohm which implies that a DUT that has reached low ohmic state will see the full peak of the waveform. The current peak without the extra cabling is well above 3.75A/kV. For 1kohm load the first proportional lowering of the current peak occurs, followed by other higher resistor values. Once the cabling and the probe are added the waveform meets the specification given in table 1.1. Shortening the cables to the probe will produce higher first peak and can be targeted at exact 3.75A/kV.

1.2 Safe Operating Area and Design Window

Out of all of the stress types described previously, the two fastest are CDM and HMM/IEC. The most common damage due to the CDM stress is gate oxide breakdown of N type or P type Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) and shallow junction burnout [25, 46, 47] which usually occurs in the input pins as shown in simplified diagram in Figure 1.8. The protection scheme depicted consists of up and down protection devices at the input pin and a power supply clamp between power supply and ground. When the ESD stress is applied the protection devices should shunt the current and keep the core devices NMOS and PMOS protected during an ESD event. The ESD protection scheme should not interfere with circuit operation during normal operating conditions. To keep core devices protected, protection devices need to be designed keeping in mind the Safe Operating Area (SOA) of the protected core devices. The SOA information needed is: the highest voltage the gates can sustain prior to failure and the highest voltage and current condition prior to drain source junction failure.

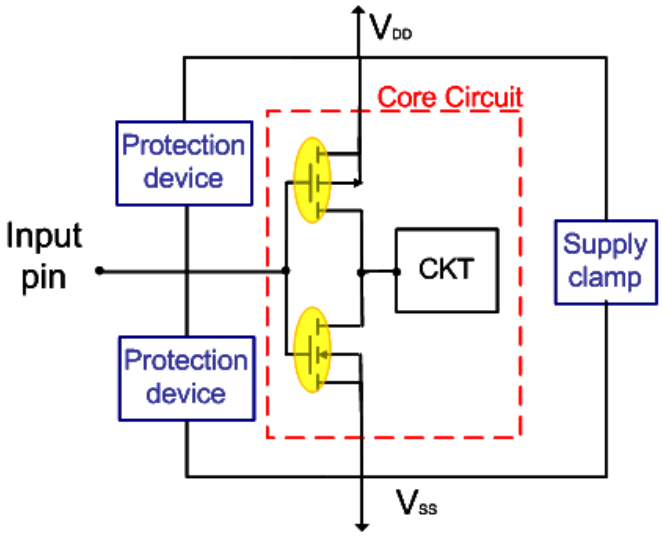

Figure 1.8: Simplified input pads protection scheme and failure mode under transient stress

Safe Operating Area information is needed to define the protection device design window depicted in Figure 1.9.

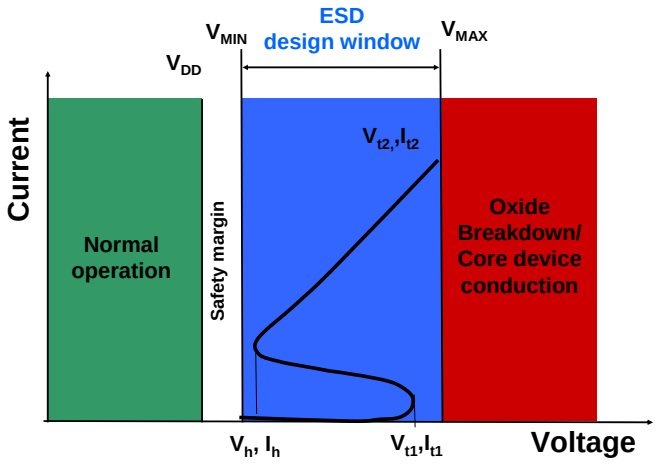

Figure 1.9: ESD protection design window

The ESD protection design window is defined by the circuit operating voltage, latch-up conditions given by the safety margin, gate oxide breakdown and junction failure condition. The design window boundaries are usually based on the DC conditions or on quasi-static TLP conditions. The protection device design requirements are described through trigger voltage and trigger current (Vt1, It1), holding voltage and holding current (Vh, Ih) and finally the failure levels of voltage and current called Vt2 and It2. A typical TLP plot [12] for a protection device containing VDUT, IDUT and leakage current (measured at 25V) information is shown in Figure 1.10. VDUT and IDUT are quasi static values obtained by averaging voltage and current waveforms averaged between 70 and 90 % of time duration for each voltage step. The failure is detected at about 2.5 A of current when the leakage current increased one order of magnitude.

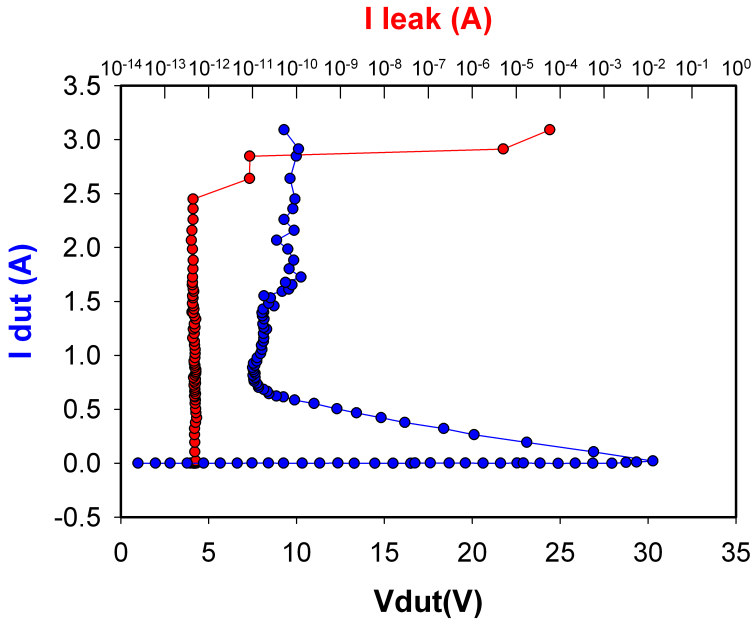

Figure 1.10: Protection device quasi static VDUT vs IDUT TLP response with leakage current

Gate oxide breakdown in the input pins, usually in the low voltage domain, is the most common CDM failure mode and thus gate oxide breakdown needs to be studied in the CDM time frame to better define the gate conditions under transient stress. Secondly, the response of different ESD protection devices needs to be investigated in greater detail using the same fast transient measurements to see if they can protect the gate oxide or they need to be further optimized or used with additional protection elements. The condition definition for reliable input protection clamps during fast transients is still a very challenging problem due to the statistic nature of gate oxide breakdown and typical data availability obtained only at DC conditions.

For some automotive, power management, and display driver circuit products, semiconductor companies use a mature process extended to include high voltage options typically from 20 to 100V operating voltage [8, 48]. The high voltage option is added by introducing thick oxides and low doped drain and source implants to increase the breakdown voltage [48]. Laterally diffused MOS (LDMOS) devices are frequently used in mixed-signal applications, in output circuits pins.The desirable characteristics of such devices include high-current/voltage handling capability and superior reliability qualification [49]. Designing an effective electrostatic discharge (ESD) protection solution for LDMOS in high-voltage mixed-mode technologies is challenging because of the shrinking design window and the lack of information on LDMOS behavior under very fast transient ESD stresses [49–51].

At the output pins, a common HMM/IEC failure mode occurs in high voltage LDMOS transistors [8,52,53] and it is thermal in nature [54–56]. A simplified diagram of output pins is depicted in Figure 1.11 with the same protection scheme as in the case of input pin. The same information about the core devices as in the case of the input pins is needed for the appropriate design of the protection structures. Additionally, CDM damage has recently been reported for Laterally Diffused N type MOS(NLDMOS) Silicon Controlled Rectifier (SCR) which are used as protection device [57] for high voltage applications in low voltage Complementary MOS (CMOS) technology.

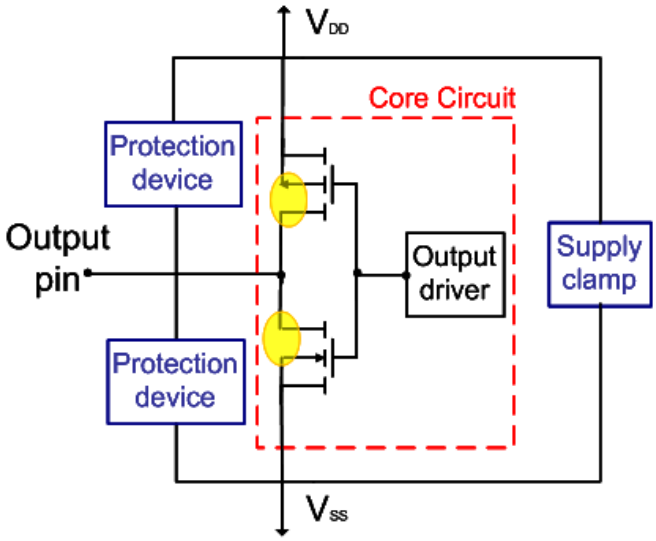

Figure 1.11: Simplified output pads protection and failure mode under transient stress

During very fast transient stresses, large overshoots were reported for protection structures [17, 18, 32, 58–60], while the protected core structures have not been studied in detail under very fast transient stress in order to establish the design window more accurately. In the case of output devices, as it will be shown, protection design based on DC breakdown data is not an adequate metric to assess the ESD protection robustness of stand-alone output devices or output devices combined with protection clamps during transient stress.

Quasi static 10 ns VFTLP stress results with 100 ps rise time of a high voltage protection clamp used to protect an output LDMOS device are depicted in Figure 1.12. The standard averaging window to generate the quasi-static-like I-V curve lies between the 25 to 75 % marks through each applied pulse. Also plotted in Figure 1.12 are the maximum voltage during the pulse versus the current at the corresponding point in time (Vmax,I(t(Vmax)),

and the maximum current during the pulse versus the voltage at that point during the pulse (V(t(Imax), Imax)).

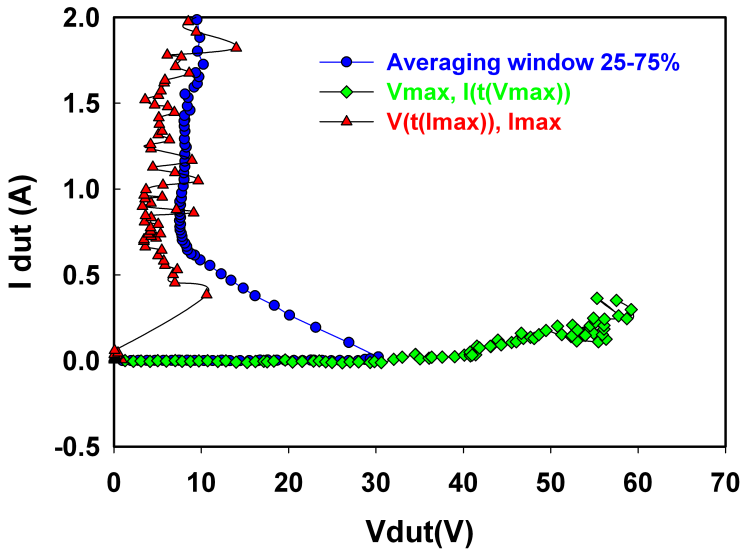

Figure 1.12: Clamp response for 10 ns pulse width and 100 ps rise time: Quasistationary response with averaging window 25 to 75 % , maximum overshoot voltage and maximum current

Comparing the standard VFTLP I-V curve with the one based on Vmax, notice that for higher VFTLP stress the triggering voltage of this high voltage clamp increases. The quasistatic I-V characteristics snapback voltage does not actually provide the maximum voltage that can be obtained across any device protected by this high voltage clamp. Figure 1.13 shows the voltage and current transient response versus time for a 10 ns Vpulse. The averaging window for a 1 ns pulse is located at a different point in time, resulting in a holding voltage of approximately 48V and 14 V for 1 ns and 10 ns, respectively. While the 1

ns averaging window gives us a better insight into the peak voltage, it still does not provide information about the true peak voltage.

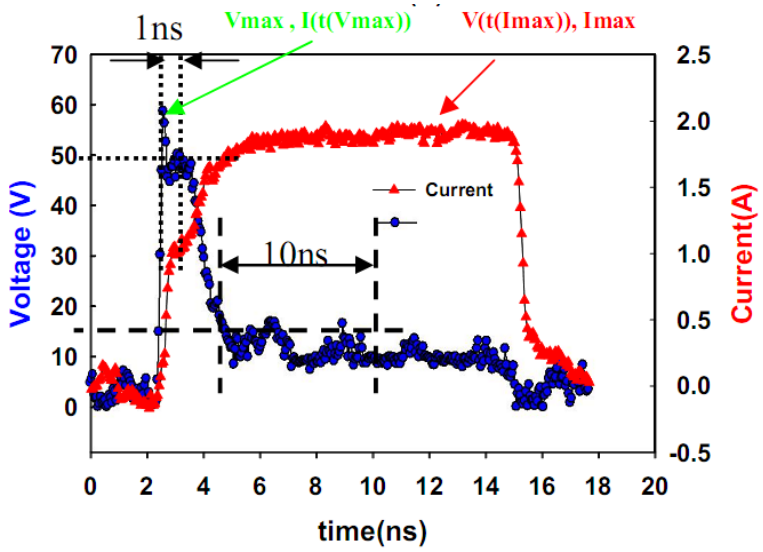

Figure 1.13: Clamp response for 10 ns pulse width and 100 ps rise time: Voltage and current waveform for Vpulse=60V with 25 to 75 % averaging window for 10 ns stress and the same averaging window for 1 ns stress

Figure1.14 depicts current (time) vs. voltage (time) for the pulse in Figure 1.14 . This alternative way to plot the data provides an I-V curve from just a single pulse and shows additional information on the voltage overshot not available from the quasistatic I-V characteristics. Additionally, the current (time) vs. voltage (time) plot covers the on state (constant current) and turn off conditions.

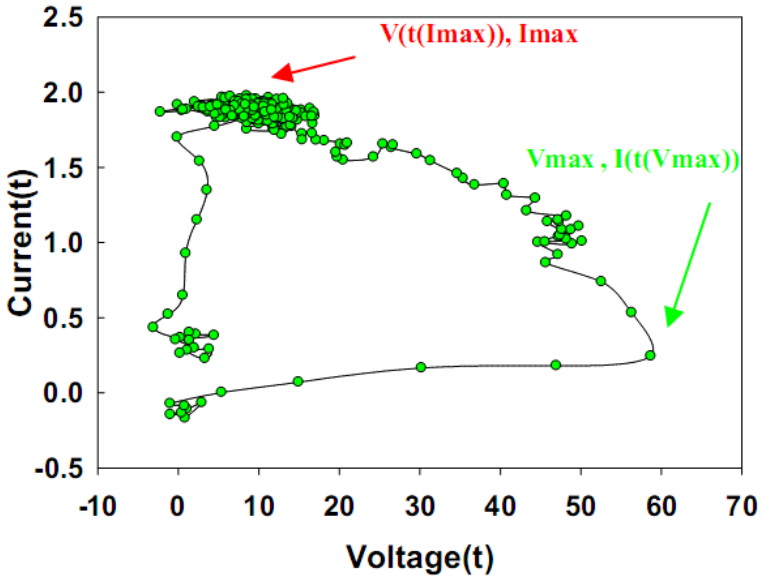

Figure 1.14: Clamp response for 10 ns pulse width and 100 ps rise time: Voltage vs. current from plot form 1.13

1.3 Organization of the Dissertation and Contributions

A methodology to obtain design guidelines for gate oxide input pin protection and high voltage output pin protection in Electrostatic Discharge (ESD) time frame is developed through measurements and Technology Computer Aided Design (TCAD).

In Chapter 2 transient behavior of core circuit elements and protection elements is studied under transient conditions. A set of parameters based on transient measurements are used to define Transient Safe Operating Area (TSOA). The parameters are then used to assess effectiveness of protection devices for input and output pins.

As ESD events are transient in nature, an appropriate TCAD methodology needs to be developed in the same way that the protection requirements need to be redefined. In Chapter 3 TCAD methodology is developed and later used to explain device behavior under very fast transient stresses. First, appropriate structures are chosen for calibration in order to extract the key technology parameters. Secondly, a methodology to correlate the transient measurements and simulations is established. This is followed by optimization and evaluation of low, medium and high voltage protection elements in terms of their TSOA.

In Chapter 4 TCAD methodology is applied to high voltage laterally diffused MOS used in output pins. Device behavior under transient stresses for both p and n type devices is evaluated. Secondly, TCAD failure conditions are discussed. Further study on transmission line pulsed robustness under transient stress for different widths is undertaken. Finally, interaction with the protection clamps is evaluated.

In chapter 5 standalone clamp HMM robustness is evaluated and a prediction methodology for HMM type stress is developed based on standardized transmission line pulsed testing. Secondly, standalone NLDMOS HMM robustness is evaluated as a function of width under both HMM and transmission line pulsed conditions. Finally, LDMOS and protection clamp parallel protection conditions are identified.

In chapter 6 future work recommendations are briefly discussed.

CHAPTER 2
TRANSIENT DEVICE BEHAVIOUR

The traditional ESD protection design window does not include a time component and it is defined by the circuit operating voltage, latch-up conditions and typically gate oxide breakdown (GOB) under DC conditions [51, 61, 62]. In this chapter gate oxide is evaluated under transient pulsed stresses and its safe operating area is defined. This is followed by evaluation of both protection and protected device behavior under pulsed stress with time component included. Finally, transient safe operating parameters are defined and the methodology for input and output pins is discussed.

2.1 Gate Oxide transient behavior

Sub-nanosecond time-dependent characterization of gate oxide degradation and oxide breakdown mechanism are central to predicting and modeling oxide failure when a fast voltage transient is applied to a thin CMOS gate-oxide. Understanding this phenomenon, on the other hand, is critical to developing guidelines and a systematic circuit design strategy that avoids common oxide damage resulting from Charged Device Model (CDM)-type electrostatic discharge (ESD) events [21], [16].

For a fast transient stress, such as CDM, the protection device may not respond fast enough to protect sensitive gate oxides and the time-dependent gate oxide breakdown voltage increases compared with the traditional DC voltage stress for long-term gate reliability evaluation. As a result, a different methodology is required to evaluate the gate reliability under CDM-type stress as well as ESD device transient response in the sub-nanosecond time domain. The shortest time pulse width for CDM characterization reported in the literature is sub-50 ps [24] with a rise time in the picoseconds. Such pulses can also be generated during CDM stress by the inductive coupling between long metal lines. Transmission line pulsed characterization of gate oxide has been widely published in the literature, [21], [63–70].

Standard TLP pulse is significantly wider in duration than a CDM-type ESD event and this measurement provides limited information on gate failure during a faster CDM event. Preliminary studies using VFTLP/UFTLP measurements to characterize gate degradation have been recently reported, [24, 66]. Notwithstanding, defining a predictive failure condition for circuit simulation or effective CDM ESD device protection remains elusive.

Two models have been proposed in the literature for the gate-oxide breakdown for thick oxide and under TLP stress conditions. The first is the power law model [63], [68, 69], [71–77], and the second is the 1/E model [9], [64], [66], [78]. Recently the Hydrogen Release Model, [72,73], [79–82], linked to the power law model, has also been reported as the physical breakdown mechanism. Nonetheless it was refuted by several authors [74, 83–85]. A major endorsement of the power law model, however, came from the experimental work performed

by Nicollian et al. [86]. The latter showed that the time to breakdown did not reduce after decreasing the doping in the poly silicon gate.

Each stress pulse applied to the oxide induces damage proportional to the voltage the gate oxide sustains. This relationship is not a linear one, it is given by the power law. It implies that as the pulse applied approaches the failure pulse its contribution to the failure is greater, making the pulse prior to failure and the failure pulse portion the most significant. In constant voltage stress (CVS) tests, empirical TDDB models have been proposed to easily estimate the breakdown performance of a characterized oxide. Two of these models are well known, the exponential law and the power law [71], [73]. The TDDB power law is defined in 2.2 as, [71] and [9]:

$$T_{BD} = A \cdot V_G^{-n}. \tag{2.1}$$

The TDDB exponential law is defined as [73]:

$$T_{BD} = t_0 \cdot e^{-\gamma \cdot V_G}, \tag{2.2}$$

where γ is the voltage acceleration factor.

It was recently demonstrated that the power law more accurately predicts TDDB than the exponential law [71], [73], [76]]. The power laws exponent, n, is independent of oxide thickness and the value for both n- an p- MOSFET is 44 in DC regime [71], hence it is more predictive. Recently it has been reported that in ESD regime n is about 30 [20].

In this study, the experimental setup for the VFTLP measurements is reviewed. Next, the VFTLP waveforms close to the oxide breakdown condition are depicted and discussed. The power law model is then used to analyze the time dependent dielectric breakdown (TDDB) through the voltage the gate oxide can sustain prior to failure under fixed stress duration of 1 and 10 ns.

2.1.1 Characterization Methodology

A criterion to define the total stress time has been proposed by Wu et al. [66]. The total stress time was equated to the pulse width multiplied by the pulse count applied prior to the oxide damage, plus the time elapsed from the beginning of the pulse that damaged the oxide until the actual damage detected by an increase in leakage current. This methodology has the advantage of being straightforward to implement. However, as will be shown later in this study, this method does not allow for benchmarking of measurement results with other studies following different test procedures. Often the testing methodology leads to different interpretations and definitions of time to breakdown, further complicating comparison and interpretation of published experimental data.

There are five oxide testing methodologies considered in this study. The first is Constant Voltage Stress (CVS), for which TDDB was initially defined, and is the time it takes from the instant the voltage is initially applied to an oxide until the time when the oxide

is damaged (i.e. current flows through it). For this testing method, extensive experimental data is available.

A second closely related testing method is Repetitive Constant Voltage Stress (RCVS), in which Time Dependent Dielectric Breakdown (TDDB) is defined as the number of pulses applied, multiplied by the pulse width, plus the time to breakdown in the final pulse. It has been shown that this method reports longer time to breakdown. The time to breakdown under repetitive stress is a function of pulse width, frequency and stress voltage, showing the cumulative nature of the breakdown [63].

The third stressing methodology uses the previously discussed TLP- or VFTLP-type stress, commonly referred to as Ramped Voltage Stress (RVS), where the voltage increases for each pulse [68]. In this method, it is difficult to define the time to breakdown as low voltage pulses do not have the same effect as the subsequent higher voltage pulses. As a result, if the time to breakdown is interpreted as the sum of all of the pulses [66], following the concept of repetitive CVS, it is dependent on the initial stress voltage and voltage step during stressing. In this study, based on power law more importance is given the later/higher pulses [20].

The fourth testing methodology is Ramped Voltage Stress, which is done through Constant Current Stress (CCS) [87]. The influence of dV/dt can be studied in this way, and a model which can reproduce both CVS and CCS would likely be capable of predicting failure induced by arbitrary waveforms.

The measurements in this study follow the third testing procedure. They are performed with two different waveforms, one at 1 ns pulse width and 100 ps rise time, corresponding to CDM-like stresses, and the other at 10 ns pulse width and 200 ps rise time, a pulse type that is about an order of magnitude wider than the previous one and in between the CDM type VFTLP and the HBM like TLP stress. The devices tested are thin oxide N and P type MOSFETs in inversion mode. The gate oxide is formed via thermal oxidation, and the sample structures were tested at room temperature.

Testing setup includes the charging of a transmission line by a high voltage source, which is discharged down the calibrated transmission line to stress the device under test, while voltage and current probes measure the device response. The measurements consist of recording the voltage versus time and current versus time waveforms for a variety of pulses, which are increased in energy for each pulse, and after each pulse a DC leakage current stress at low voltage of 0.5V is performed. The applied voltage step between the pulses is fixed, with the voltage stress increasing in steps of 0.5V per pulse starting at 0.5V until reaching failure. The leakage current measurement is performed after each pulse. To generate the classic TLP I-V characteristics, the voltage and current versus time pulse waveforms in the DUT are averaged between the 25 and 75 percent of the pulse durations to generate a single current-voltage (I-V) data point.

In the following discussion, GOB is detected by looking first at the point where the DC leakage current increases by orders of magnitude and later looking closer to the waveform

where the hard failure occurred. The safe region is the pulse prior to the pulse that damages the oxide.

2.1.2 Gate Oxide under pulsed stress

Figures 2.1, 2.2, 2.3 show three examples of fast-pulsed I-V characteristics where hard failure is detected at different levels for NMOS device. The oxide thickness affects the breakdown point in the I-V curve, making the breakdown voltage approximately 34.95V for the 70 A thickness for 3.3V operation (Figure 2.1) and 37.2 V for 130A for 5V operation (Figure 2.2) for 1 ns duration pulses. In case of the longer pulses of 10 ns, the oxide breakdown occurs earlier (at 26.5V, see Figure 2.3) due to the cumulative damage of longer pulses.

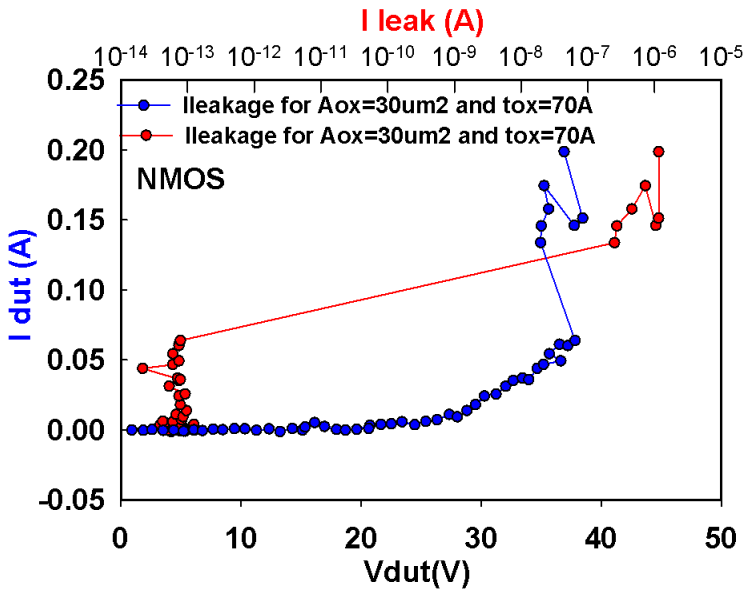

Figure 2.1: I-V characteristics for an NMOS tox=70A, pulse width=1ns, rise time=100ps

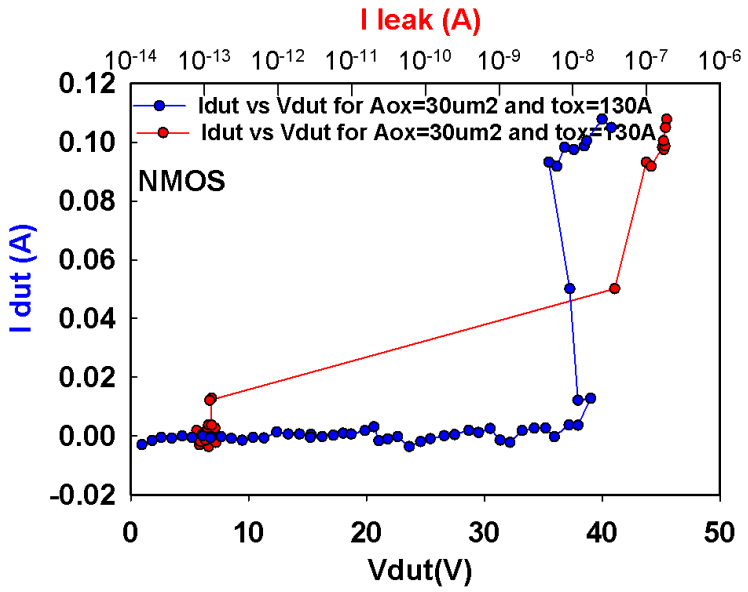

Figure 2.2: I-V characteristics for an tox=130A, pulse width=1ns, rise time=100ps

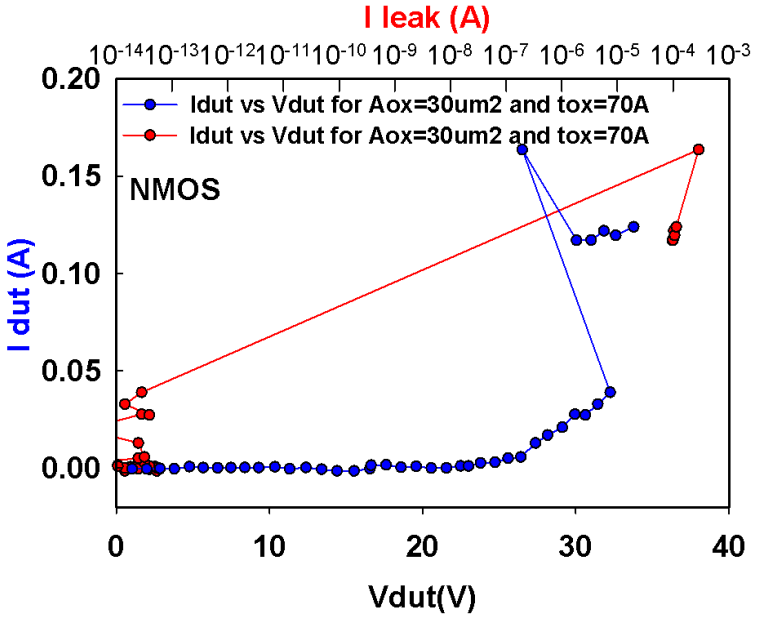

Figure 2.3: I-V characteristics for an tox=70A, pulse width=10ns, rise time=200ps

The statistical nature of the oxide breakdown needs to be taken into account when interpreting individual measurement results. The TLP I-V characteristics shown in Fig.2.1, 2.2, 2.3 depict example I-V characteristics for which failure is close to the average failure voltage obtained in different samples under the same measurement conditions, that is, (Fig. 2.1 - 37.5 V, Fig. 2.2 - 39.5 V, Fig 2.3 - 32.2 V). The actual failure voltage is different from the average voltage where the DC leakage current increases abruptly in the Idut-Vdut characteristics in Fig. 2.1, 2.2, 2.3, where Idut-Vdut are calculated as the average of the current-voltage between 25 and 75 of the pulse duration. Once failure occurs and the voltage across the oxide drops as current flows through it, this average is no longer a valid measurement of the voltage that caused oxide failure. Notice that due to the statistical nature of trap generation, individual measurements may lead to seemingly contradictory results, as voltage distributions of reaching the critical trap density may overlap.

To illustrate the transient waveforms during different stress conditions, Fig. 2.4 shows the voltage and current versus time of the DUT at the breakdown point for two case study oxide thicknesses of 70 A and 130 A using a pulse of 100 ps rise time and 1 ns width. Additionally, the 70 A gate oxide is also stressed using a 200 ps rise time and 10 ns pulse width signal. Figure 2.4a shows how the transient current waveform behaves when the oxide hard-failure takes place. In this case, the current sharply increases to 0.14A, approximately 2 ns after the initial part of the pulse. Figure 2.4b shows the current increase to 0.1 A, and in Fig. 2.4c the current increases first to 0.1 A, while voltages reach approximately 37.5V, 39.5V, and 32.2V, respectively.

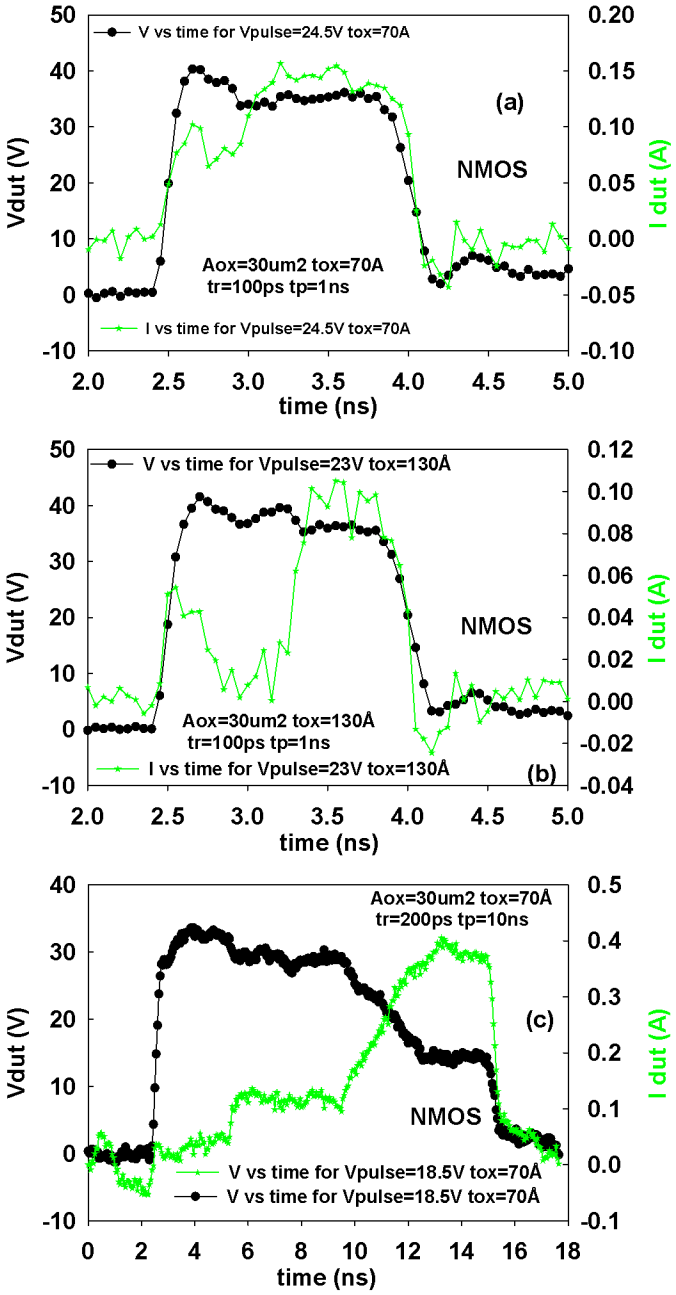

Figure 2.4: Detection of the breakdown within the VFTLP pulse with I(t) and V(t) curves a) tox=70A, pulse width=1 ns, rise time=100 ps b) tox=130A, pulse width=1ns, rise time=100 ps c) tox=70A, pulse width=10 ns, rise time=200 ps.

Figures 2.5, 2.6, 2.7 compare the pre-breakdown, breakdown, and post-breakdown waveforms for the three cases in Figs.2.1, 2.2, 2.3 and 2.4. The breakdown time within this recorded waveform is defined as the point in time when the current begins to rise above its previous average value, rather than when it reaches its new average value.

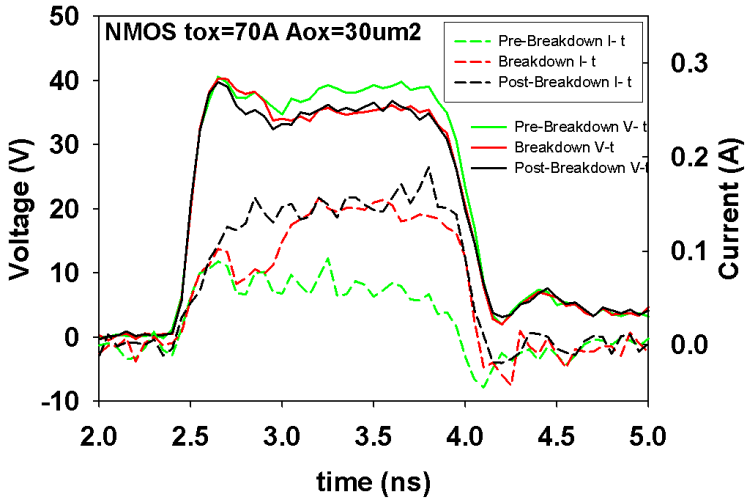

Figure 2.5: I-V characteristics for an NMOS tox=70A, pulse width=1 ns, rise time=100ps

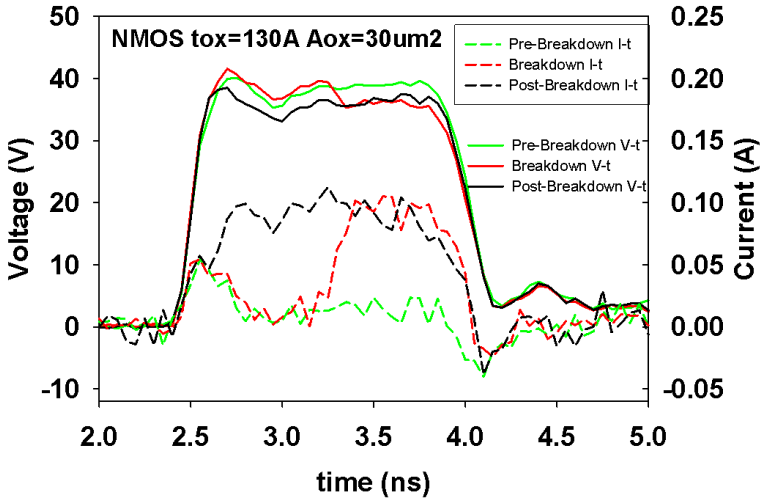

Figure 2.6: I-V characteristics for an tox=130A, pulse width=1 ns, rise time=100ps

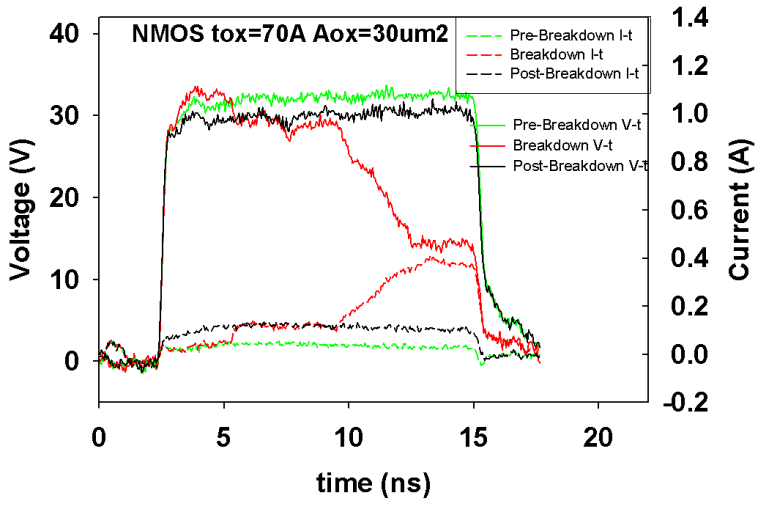

Figure 2.7: I-V characteristics for an tox=70A, pulse width=10 ns, rise time=200ps

The breakdown point appears to be a transition point for the oxide from a reliable- to a damaged- insulator, as can be seen by how closely the breakdown waveform tracks the pre-

breakdown and post-breakdown waveforms before and after this point, respectively. Notice in Fig. 2.7 that the breakdown current rises a second time far above the level it originally reached, but then returns to the lower average current level in the next pulse. This behavior has been observed before and its exact cause is not well understood, but different hypotheses have been discussed in reference [88]. The same methodology was applied to PMOS devices that were stressed with negative pulse values at the gate.

Figure 2.8 depicts the histogram plots of the highest voltage condition the oxide can sustain for both n and p MOSFET. The stress condition is 100 ps rise time and 1 ns pulse duration for oxide area (Aox)=30 $\mu m2$ and oxide thickness (tox)=70 A. The voltage condition is given by the value of Vpulse which represents the voltage seen at 50 ohm load, which means that the charge line in the TLP system was charged to 2Vpulse. The NMOS gate oxide can sustain Vpulse=18V while PMOS can sustain Vpulse=12V. Based on [20] we can calculate the voltage the device can sustain under 1 ns stress.

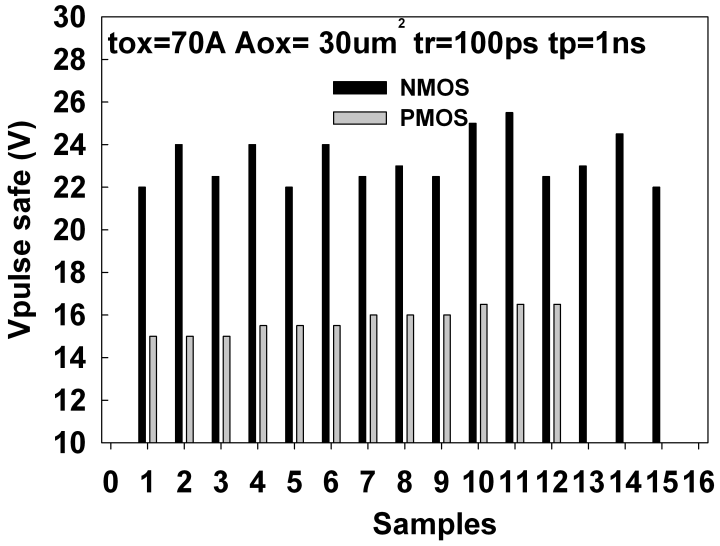

Figure 2.8: 30 $\mu m2$ oxide area and 70A oxide thickness n and p type MOSFETs stressed using a 100 ps rise time and 1 ns train of VFTLP pulses

Figure 2.9 shows a histogram for the case of 200 ps rise time and 10 ns pulse duration. The time to breakdown increases and the voltage to breakdown decreases due to the longer pulse times.

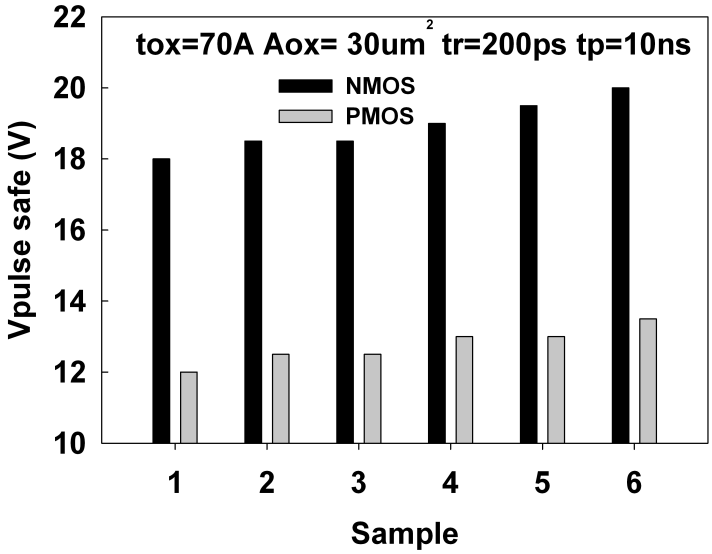

Figure 2.9: 30 $\mu m2$ oxide area and 70A oxide thickness n and p type MOSFETs stressed using a 200 ps rise time and 10 ns train of VFTLP pulses

For a thicker oxide tox=130 A and the same area, it is observed that the oxide lifetime seen through the value of Vpulse increases compared to the thinner oxide [89], as depicted in Figure 2.10.

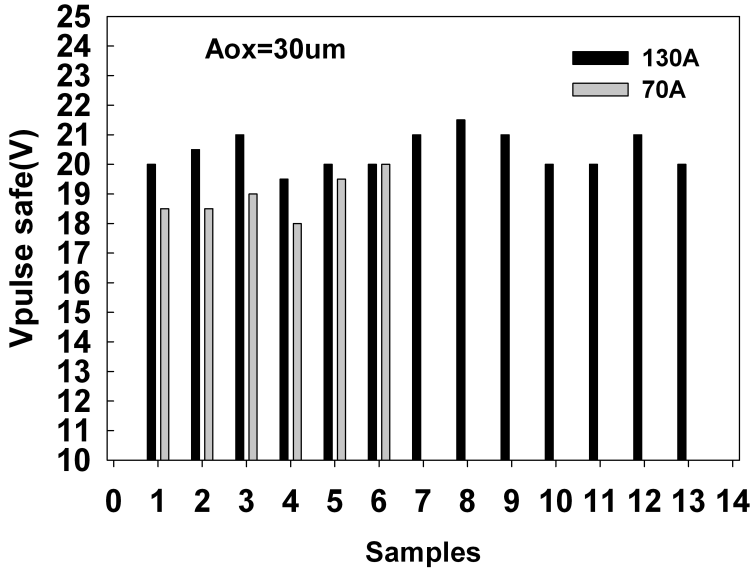

Figure 2.10: NMOS for 200 ps rise time and 10 ns pulse duration for Aox=30 $\mu m2$ and tox=130 A and tox=70 A

Figure 2.11 shows the plot for NMOS devices with different areas, where one is twice the area the other under 1 ns stress. Notice the area dependence in terms of the Vpulse. It is lower for the larger area device consistent with lower TDDB for larger area oxides.

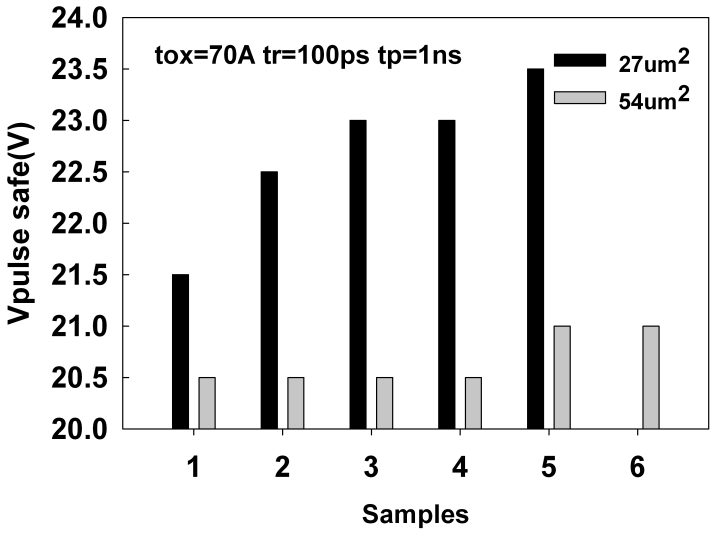

Figure 2.11: NMOS for 100 ps rise time and 1 ns pulse duration for tox=70 A and Aox= 27 $\mu m2$ and 54 $\mu m2$

In table 2.1 the average highest pulse before failure Vsafe, the average highest gate oxide voltage prior to failure Vdut are shown for different gate oxide thickness, area and device type. The lowest voltage can be sustained by PMOS device.

Table 2.1: Gate Oxide Safe Operating Area summary

Device type	Area($\mu m2$)	tox(A)	pulse width (ns)	average Vpulse safe(V)	average Vdut safe(V)
NMOS	30	70	1	21.4	38.52
PMOS	30	70	1	15.73	28.32
NMOS	30	130	10	20.43	36.77
NMOS	30	70	10	18.92	34.05
PMOS	30	70	10	12.75	22.95
NMOS	27	70	1	22.63	40.73
NMOS	27	70	10	18.78	33.80
NMOS	54	70	1	22.27	40.09
NMOS	54	70	10	18	32.40

2.2 Device transient behavior

2.2.1 Protection device

A high voltage clamp from section 1 is further analyzed in details under transient stress for rise time of 200 ps and pulse duration of 10ns. The quasi static IV curve with different color labels for different TLP pre charge voltages is shown in Figure 2.12. The final depicted Vpulse=90V label is the pulse that damages the the clamp.

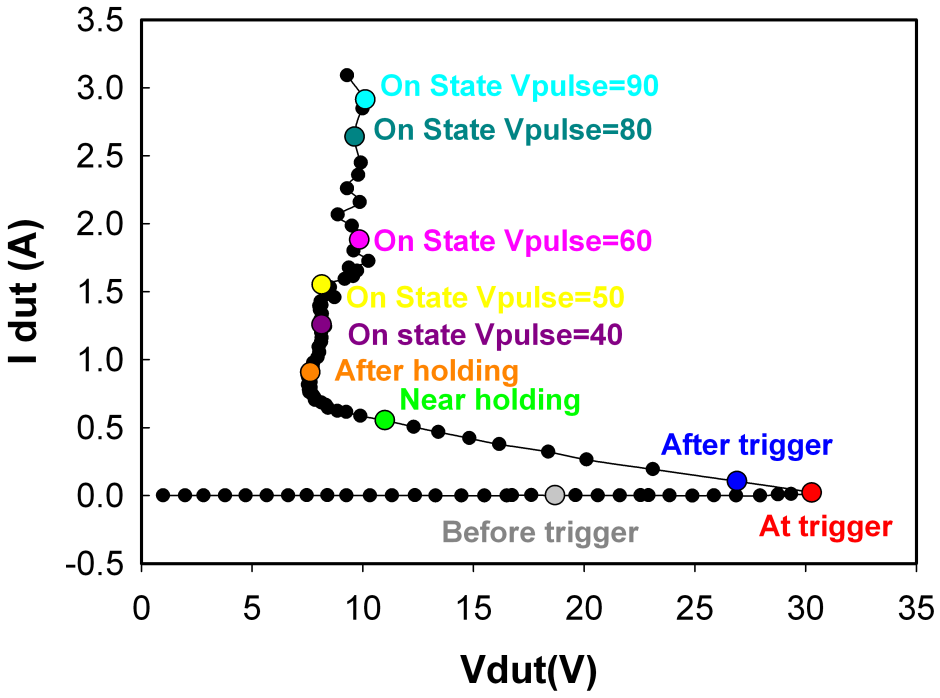

Figure 2.12: Quasistatic 10ns high voltage clamp response with different color coded Vpulse stress values depicted

For each increasing Vpulse shown in Figure 2.12 the detailed voltage vs. time is shown in Figure 2.13 up to right after holding voltage. Figure 2.14 shows transient voltage responses for high current conducting state from Vpulse=40V up to the final pulse stress that damages the clamp. Before trigger point the voltage represents an open circuit voltage. At trigger point the voltage decreases. After the trigger point for each higher stress level the peak voltage increases and the time to reach the transient holding voltage (25 to 75 % average voltage value) decreases.

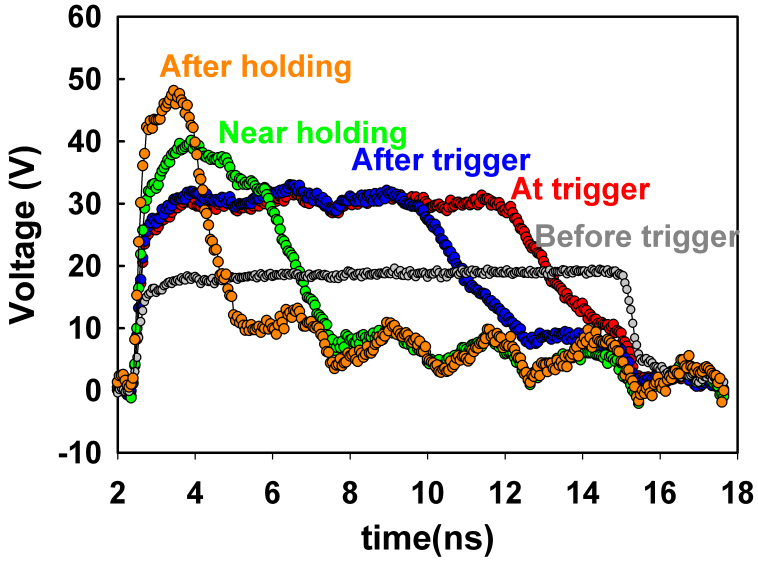

Figure 2.13: Transient voltage response for high voltage clamp under 10 ns pulse width and 200 ps rise time stress from before trigger to after the holding voltage state

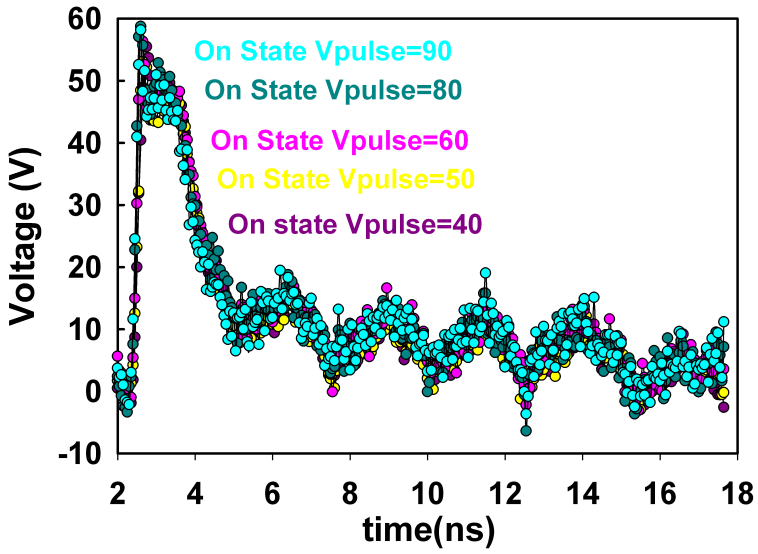

Figure 2.14: Transient voltage response for high voltage clamp 10 ns pulse width and 200 ps rise time stress in high current conduction state up to the failure point

For even higher stress the peak voltage seems to vary much less and the time to reach the transient holding voltage remains almost consonant as shown in Figure 2.15 where the zoom into the initial part of both current and voltage waveform is depicted.

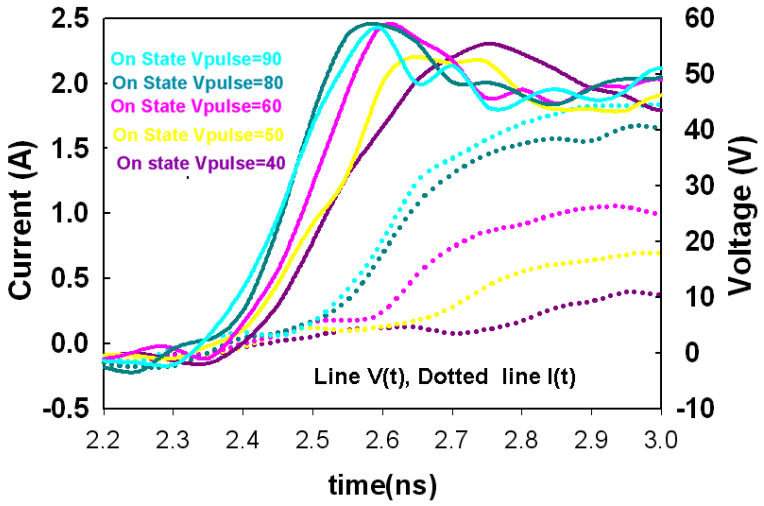

Figure 2.15: Zoom into the transient voltage and current response for high voltage clamp under 10 ns pulse width and 200 ps rise time stress

The corresponding transient current waveforms for all stress levels are depicted in Figure 2.16. Very low current is observed below the trigger point, some current at the trigger point and increasing current levels after the trigger point.

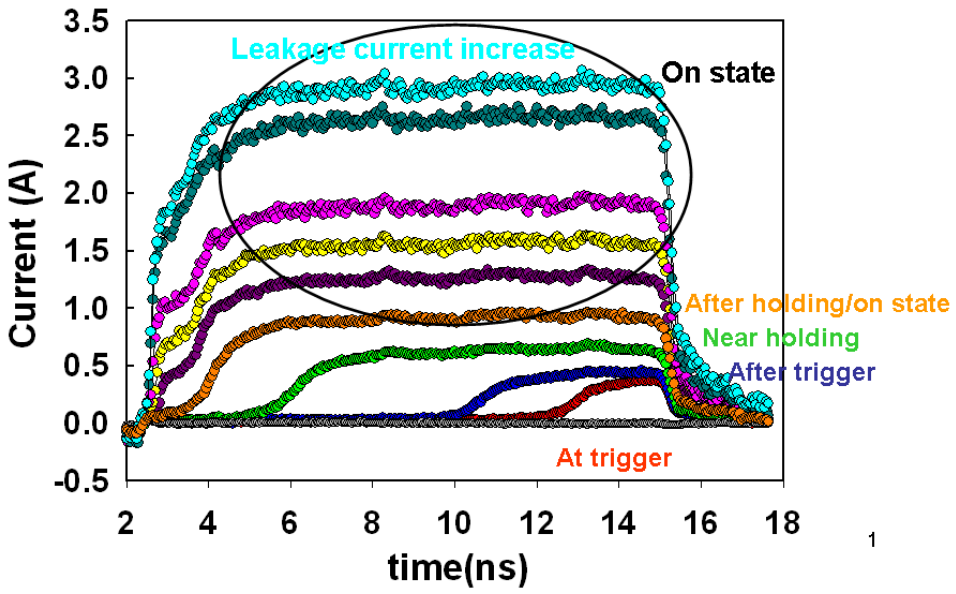

Figure 2.16: Transient current response for high voltage clamp under 10 ns stress up to the failure point

An alternative way to represent each transient voltage and current curve is depicted in Figure 2.15 for different pulse values. Similar behavior as in Figure 2.14 is observed with the exception that both voltage and current information is present. This curve contains a more accurate protection device behavior than the one shown in quasi static design window in Figure 2.12. In order to fully describe the design window we need to obtain the same information for the protected devices.

2.2.2 Protected device transient behavior

For the output pins, the device that typically needs to be protected is a 4 finger 200 μm N type Laterally Diffused MOS (LDMOS) device for 20 V applications. Due to its size it cannot be used as self protected device with the gate biased during ESD stress as the channel current of such a small structure is not high enough to sustain the stress. A dedicated protection clamp needs to be designed in order to protect it. The DC drain to source breakdown voltage is 32 V. The device in gate grounded (GG) condition is desired during the ESD stress to avoid competitive triggering between the LDMOS and the clamp designed to protect it [50], [90]. That may not be the case due to drain to gate coupling and the gate can be in a floating (GF) state [50], [91].

Standalone VFTLP measurements on the LDMOS to be protected with pre and post DC measurements are used to detect damage. The pre and post DC measurement performed is done with the gate grounded. In order to be able to perform pre and post DC measurements on this device a special setup and layout is implemented as depicted in Figure 2.17. The source and body of the NLDMOS are shorted and another pad for the ground of the parameter analyzer is shorted through metal line to body and source pad. Parameter analyzer is used either as a parameter analyzer or as a voltage source when the gate bias is needed.

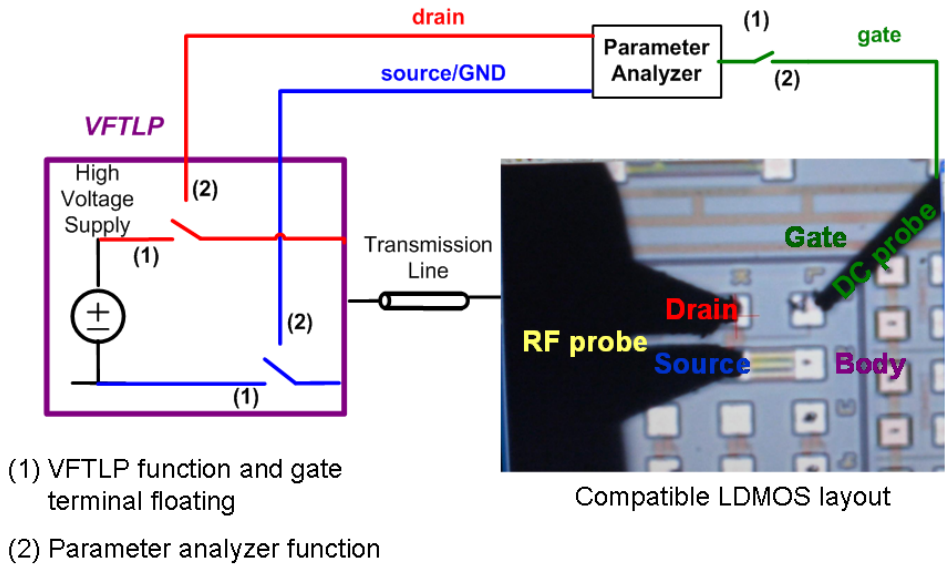

Figure 2.17: Experimental setup diagram for VFTLP stress with pre and post DC testing capability

The pre failure conditions under VFTLP for 1 ns pulse width stress and 100 ps rise time in grounded gate (GG) is Vpulse=100 V, Idut=3.34 A and floating gate (GF) configuration Vpulse=170 V and Idut= 5.96 A. The current of the DUT Idut is obtained from the 25-75 % averaging window. Figure 2.18 shows the LDMOS voltage and current vs. time waveforms. The current waveforms show that the LDMOS conducts a significant amount of current which is very similar to a short current before it is damaged. The voltage waveforms show that LDMOS overshoots significantly above the DC source to drain breakdown voltage, but it is not damaged which impacts the SOA information based on DC or quasi static TLP measurements.

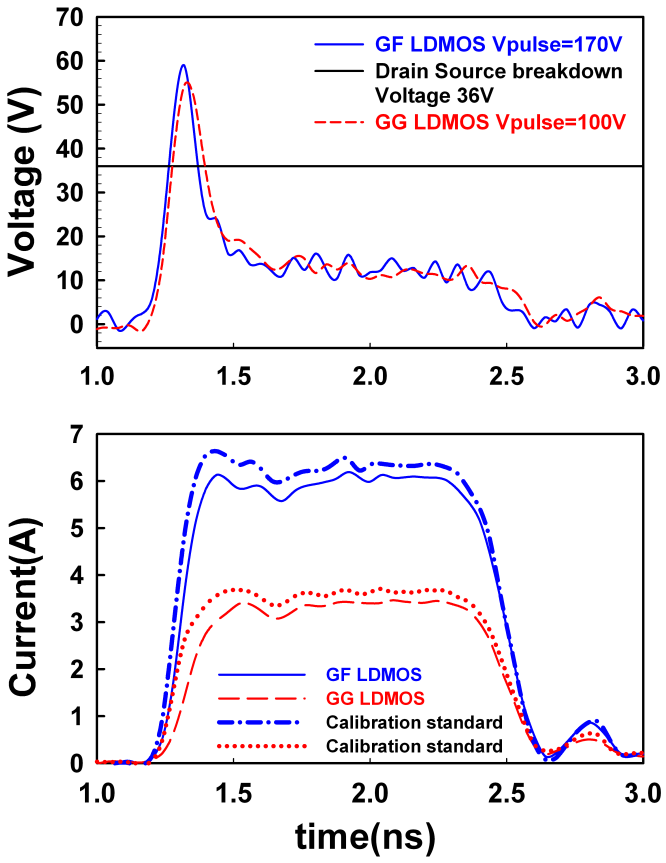

Figure 2.18: Voltage and current for 1 ns pulse width and 100 ps rise time, voltage lines, current dashed lines, open and short standards dotted

2.3 Transient SOA (TSOA) definition

For fast transient stresses, transient behavior plays a significant role in ESD susceptibility, and including the time factor is essential in developing the transient definition of the point prior to failure, the transient safe operating area (TSOA) for ESD applications.

The purpose of this work is to study both protection and protected devices subject to fast transient stresses and develop a more accurate design window definition and a criteria by which the protection device is deemed suitable during transient stress. A set of parameters to describe the device transient behavior is defined which will subsequently be used to define TSOA of either protection or protected device.

In Figure 2.19, the highest 1 ns stress response prior to failure of 200 μm NLD-MOS and the corresponding TSOA parameters are shown. These TSOA parameters can be extracted for any type of stress and for any desired structure.

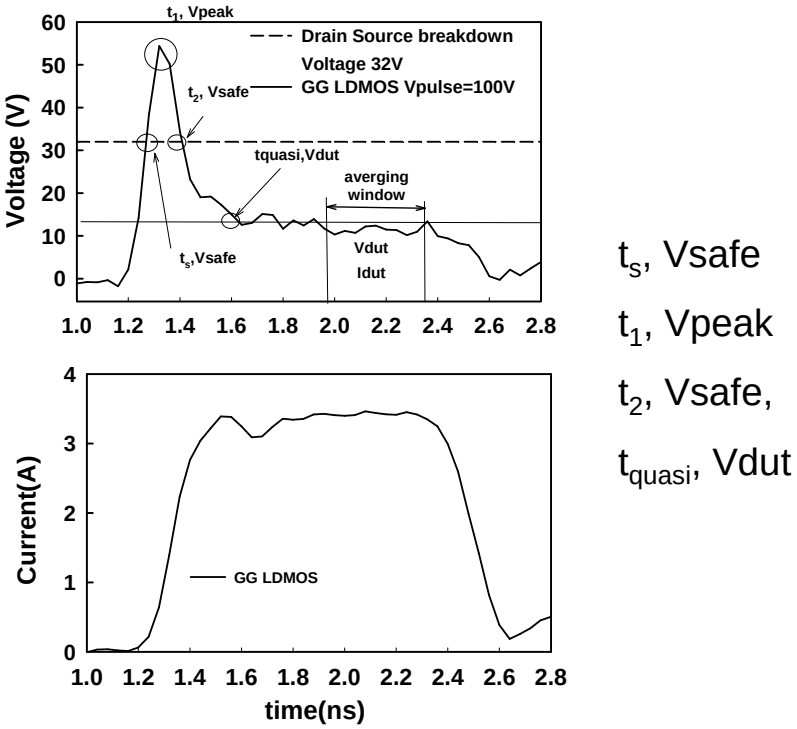

Figure 2.19: Transient device response and the transient parameters

The TSOA 1) provides information for ESD design of output circuits incorporating high voltage NLDMOS devices that are required to be robust for device or system level ESD stress conditions and 2) helps assess if the devices can be designed to be self-protecting or if they must be combined with a dedicated ESD protection component to reach the required level of ESD robustness. In describing the NLDMOS transient response, the first point of interest (ts, Vsafe) is where the drain voltage reaches the DC breakdown voltage of the NLDMOS as shown in Figure 2.19. The current at the same time point is called Its. The second point of interest is (t1, Vpeak), at which the device reaches the peak voltage and the current Ipeak. After this point, the device impedance starts to decrease significantly. The third point is the time it takes for the device to snapback to the voltage Vsafe (t2, Vsafe). After this point, the device reaches the quasi-static point labeled (tquasi, VDUT), where the voltage is essentially flat and similar and the current IDUT behaves similarly. For this case the NLDMOS device sustains a voltage higher than the DC breakdown (32 V) for about 200 ps without exhibiting damage. The five parameters ts, t2, Vsafe, Vpeak and Its together provide the dynamic information for a clamp cell design protecting the NLDMOS during an ESD-type transient stress condition.

To follow the evolution of each parameter across different stress levels in figure 2.20 the peak voltage and quasi static voltage Vdut for every stress level is shown. For reference both the safe DC breakdown voltage and the highest stress level the device can sustain of 100V are shown. The peak voltage is well above the DC breakdown voltage and it saturates after a value of about 55V. Initially at the low stress level, the peak value and

the quasistatic value are the same. In this region device is turned off and it is showing an open circuit characteristics. After Vpulse=25V the device triggers and the Vpeak and Vdut values separate.

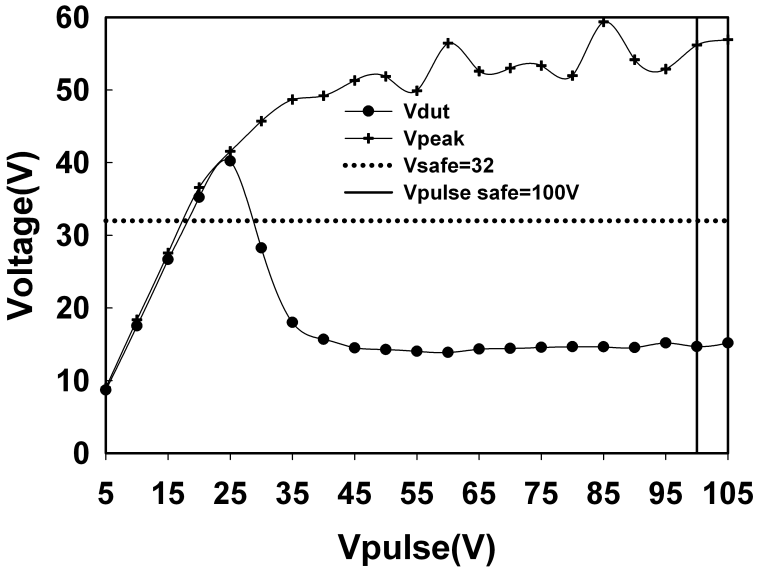

Figure 2.20: Peak voltage and quasistatic voltage for NLDMOS vs stress level for 1 ns pulsed stress

In order to evaluate how long the structure stays above the DC voltage for each stress level shown in figure 2.20, the time the device reaches the DC breakdown voltage (ts) , tpeak and t2 values are depicted in Figure 2.21.The device sustains above DC voltage for about 200 ps for most of the stress values.

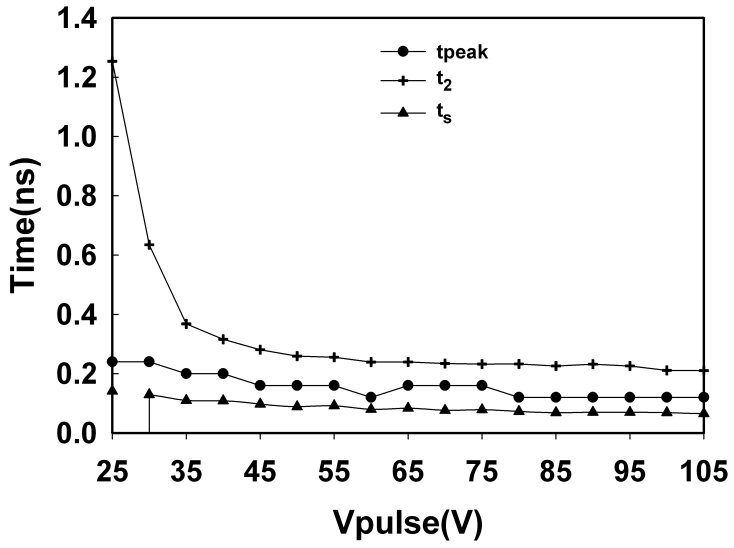

Figure 2.21: Peak voltage and quasistatic voltage for 200 μm NLDMOS vs stress level for 1 ns pulsed stress

The current values for quasistatic part Idut, the short standard, the value of the current during the peak voltage (Ipeak), when the device reaches DC voltage (Its) are shown in Figure 2.22. As expected the short standard and the Idut are close in values. The current at the peak voltage (Ipeak) is a faction of the Idut and so is the current upon reaching the DC voltage (Its) as the device has not reached a fully conducting state.

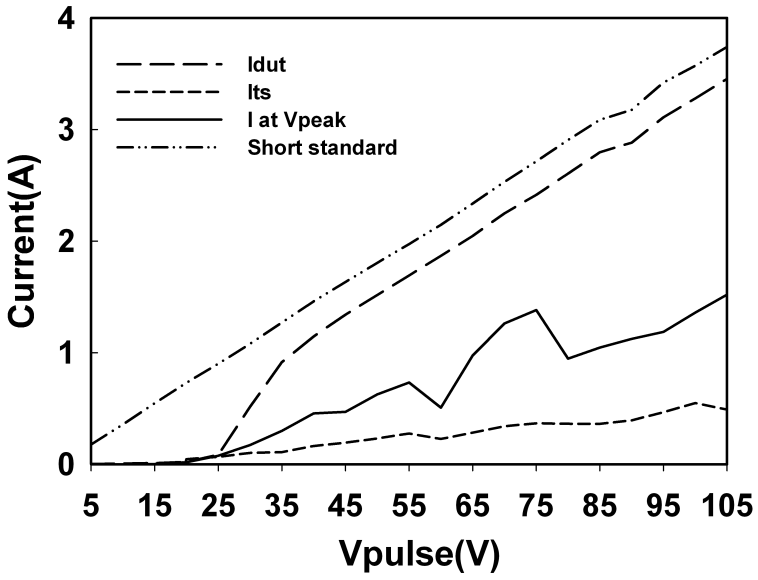

Figure 2.22: Characteristic current values for 200 μm NLDMOS under 1 ns pulse stress

The corresponding resistance values obtained by dividing the voltage and current values at specific characteristic times is given in Figure 2.23. Prior to Vpulse=25V, as was seen in Figure 2.20, the device is is in high ohmic state. Upon triggering, the resistance values decrease with increasing stress values. Rdut is the smallest resistance of all as it is calculated by dividing Vdut by Idut.

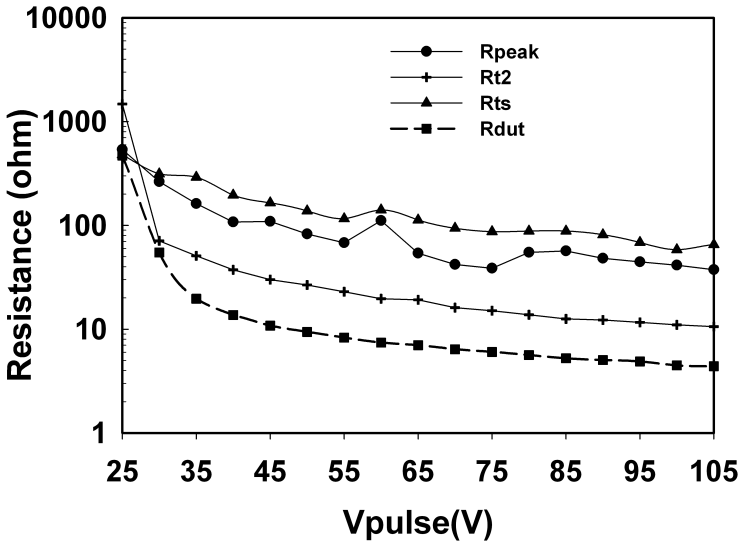

Figure 2.23: Characteristic dynamic resistance values for 200 μm NLDMOS under 1 ns pulse stress

The design window for this structure is defined by the TSOA voltage and current waveforms, which are described through TSOA parameters as shown in Figure 2.19.

2.4 TSOA and protection window

For the output pins, the TSOA definition is centered on the changing impedance of the output devices to be protected, and identifying ESD devices that would switch on fast enough to prevent the output pin from channeling the majority of the current and burning itself out. Input pins, which are usually gate oxides, reach their failure condition the moment

their impedance has changed. They do not fail from overheating, but through the formation of a percolation path [74] induced cumulatively over time.

2.4.1 Input pins - Gate Oxide

The transient response under a VFTLP of 1ns pulse width and 100ps rise time for two protection devices :grounded gate MOS GGMOS (60 μm wide) and a modified lateral SCR with n+ trigger NT-SCR (60 μm wide) are evaluated [17]. Figure 2.24 shows the voltage and current waveforms of the two protection devices under the same TSOA Vpulse of 60V. The NT-SCR demonstrates a voltage overshoot in the first few hundred picoseconds not seen in the GGMOS.

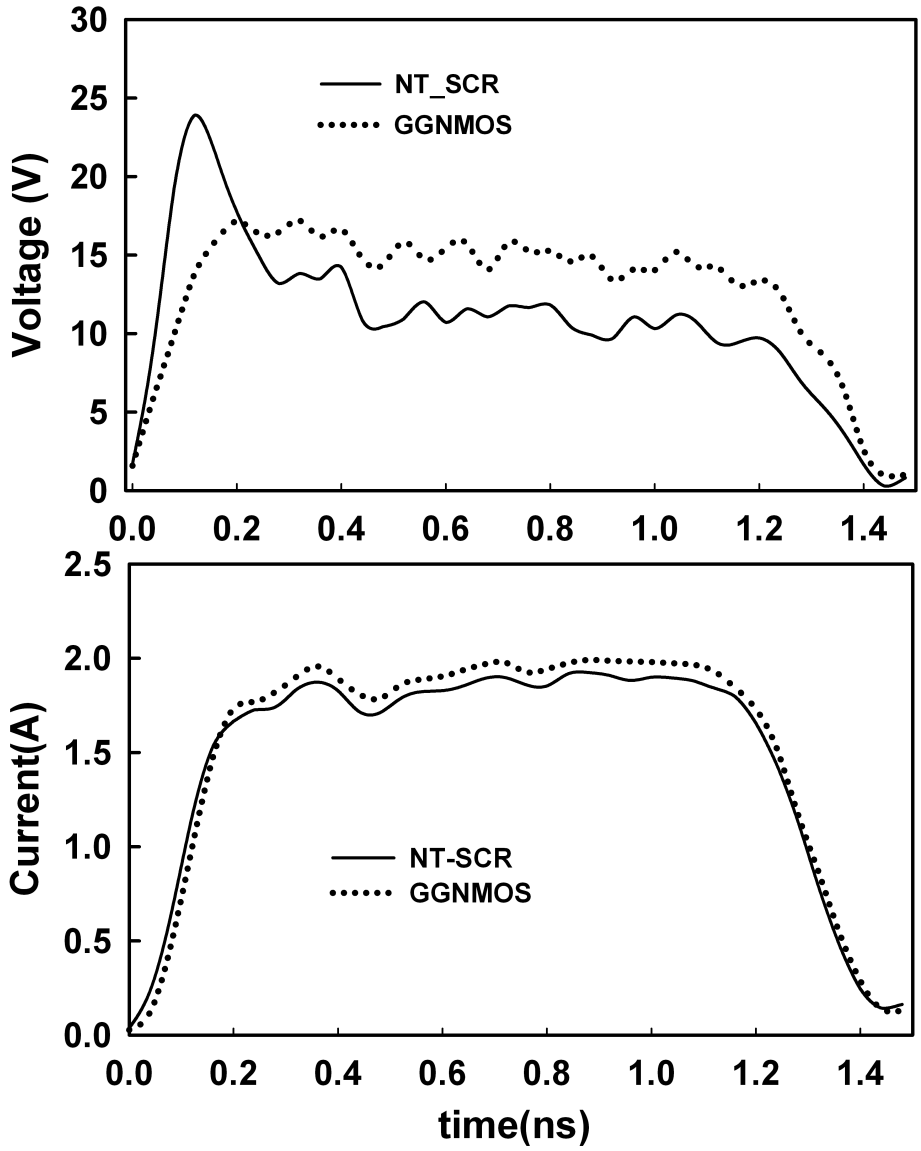

Figure 2.24: NT-SCR and GGMOS transient response for Vpulse = 60V

In order to evaluate these two clamps in terms of the threat to a gate oxide, the idea is to compare the voltage response of the protection devices with that of a pulse that induces oxide breakdown (Vsafe). Figure 2.25 shows the V-t and I-t transient response of an oxide

that fails during the first applied pulse. For comparison purposes, a duplicate oxide was stressed at a slightly lower voltage to demonstrate the differences in the voltage and current waveforms between the oxide failing and that one that does not fail. The failure can be observed by the simultaneous increase in current and decrease in voltage, uncharacteristic of a capacitor.

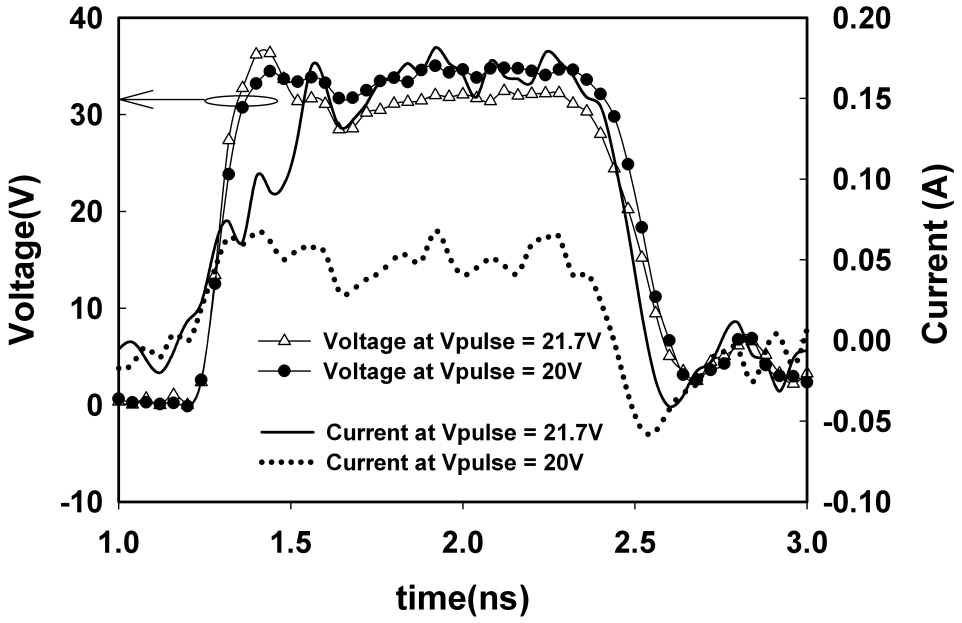

Figure 2.25: Constant Voltage Pulse Stress (CVPS) to induce breakdown in an oxide and a voltage pulse just below this failure level

This can be made more apparent by looking into the resistance versus time curve used in the previous section and comparing the oxide breakdown pulse with the slightly lower stress that avoids breakdown, shown in Figure 2.25. Both oxides show an early low resistance due to the dV/dt current effect. For the oxide that does not fail, it rises to a large

resistance (dictated by the leakage current), and when the voltage falls at the end of the pulse, the dV/dt effect induces an increased resistance (until the current goes negative and it becomes a negative resistance).

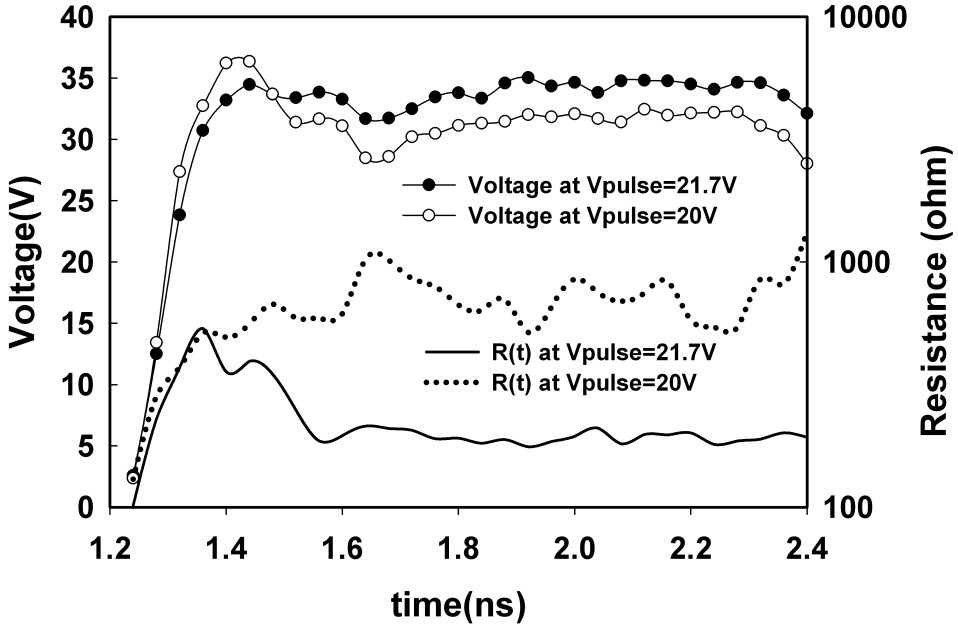

Figure 2.26: The V-t and R-t curves for an oxide that failed and a slightly lesser stress that avoided breakdown

Figure 2.27 shows several measurements of the oxide performed using the pulse that induces breakdown [20], which indeed consistently resulted in the oxide breakdown.These voltage curves are Vsafe for the gate oxide. As long as the TSOA voltage clamp response is below Vsafe the oxide is protected.

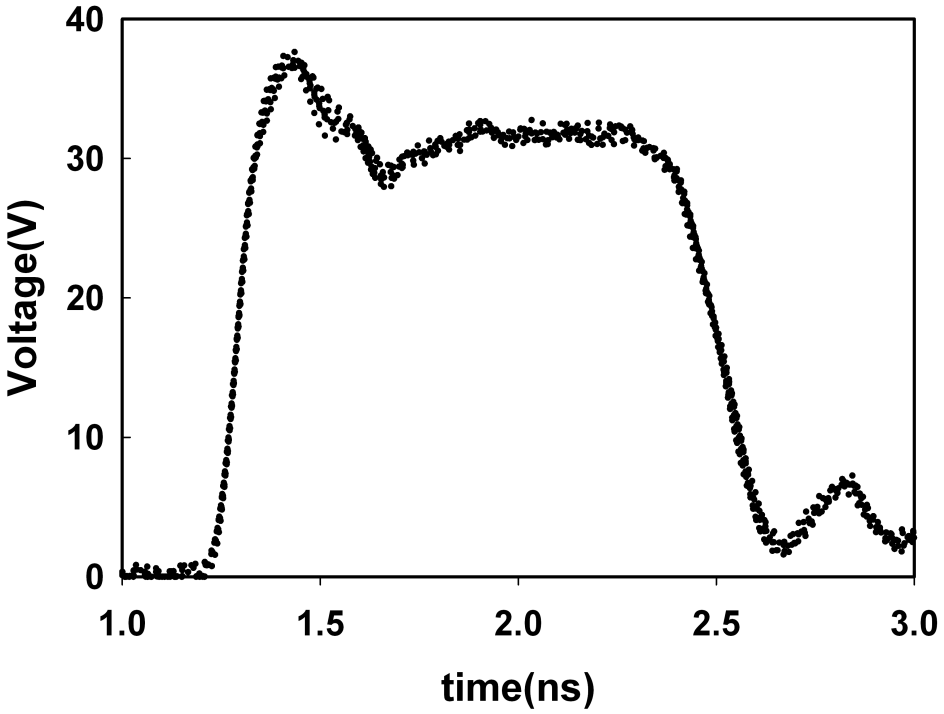

Figure 2.27: V-t curves of several oxides breakdown measurements

Having obtained the condition at which the oxide fails, the voltage response of a GGMOS and NT-SCR are compared to one of the Constant Voltage Pulsed Stress (CVPS) measurements that induce oxide breakdown called Vsafe. Figure 2.24 shows that both of these devices protect the gate oxide effectively because their voltage values are lower than the one required to damage the oxide (Vsafe), and well below even the statistical margin of error.

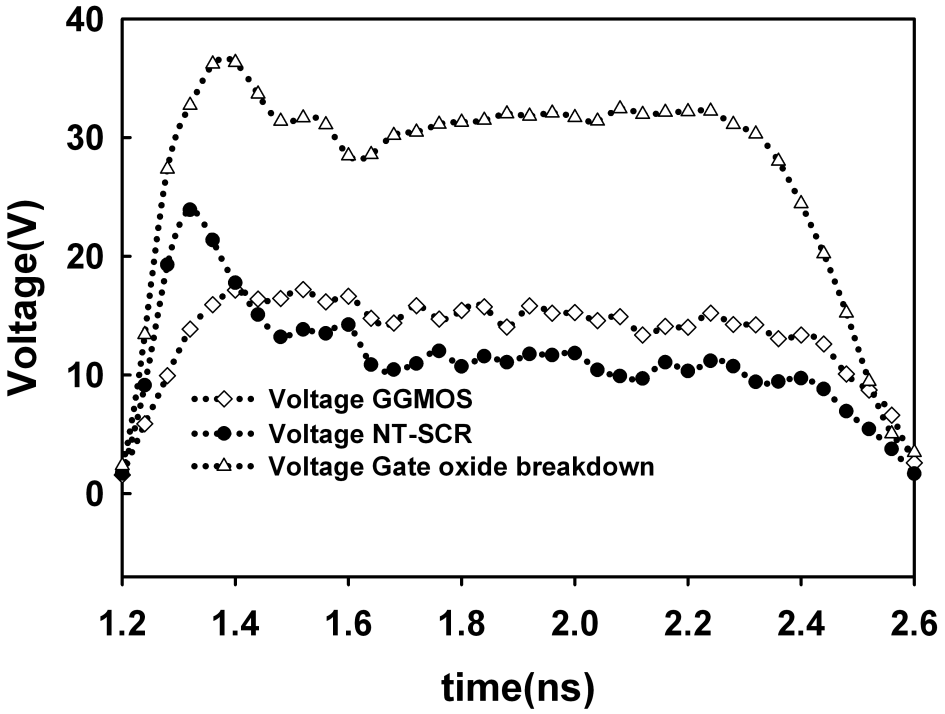

Figure 2.28: ggMOS, NT-SCR, and gate oxide breakdown voltage (Vsafe)

For input pins, the lowest pulse that damages the oxide can be used to extract TSOA parameters. These are then compared to the protection clamp TSOA parameters extracted at the highest pulse that does not damage the clamp. Then, the following criteria is used to evaluate suitability 2.3:

$$t_1, Vpeak_{CLAMP} < t_1, Vpeak_{GateOxide}, \tag{2.3}$$

$$t_{quasi}, Vdut_{CLAMP} < t_{quasi}, Vdut_{GateOxide}, \tag{2.4}$$

where MOS represents the gate oxide to be protected by the clamp.

In this evaluation there is no need for Vsafe as in the case of LDMOS device. For a greater safety margin, a pre failure pulse can also be used. The equations 2.3 can be replaced with a graphical representation by plotting V(t) and I(t) shown in Figure2.29 to more accurately represent the design window. The voltage reached by the clamp needs to be lower than that of the gate oxide. Notice that gate oxide conducts almost no current while the clamp conducts about 2A during the constant current region.

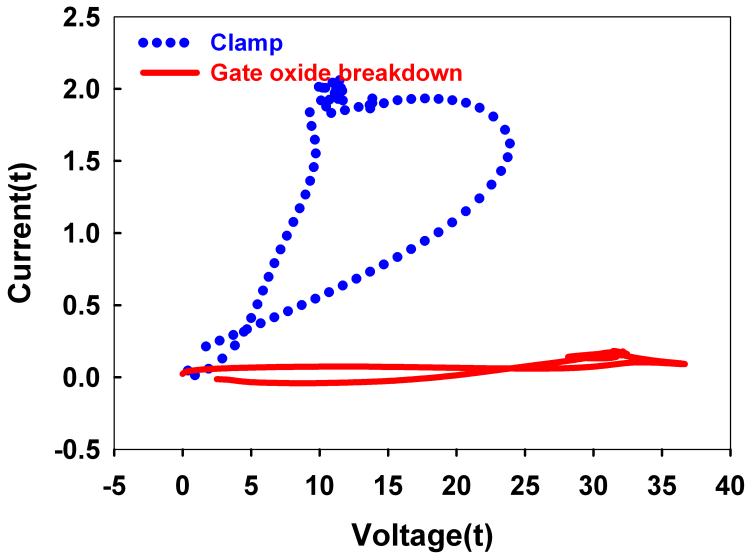

Figure 2.29: Graphical representation of TSOA usage on gate oxide for input pins

2.4.2 Output pins - High Voltage MOS

In order to evaluate if the clamp is adequate the clamp TSOA parameters need to be extracted on the highest stress value that does not damage the clamp. Then the following criteria 2.5 is used:

$$ts_{CLAMP}, Vsafe_{CLAMP} < ts_{LDMOS}, Vsafe_{LDMOS}, \tag{2.5}$$

$$t_1, Vpeak_{CLAMP} < t_1, Vpeak_{LDMOS}, \tag{2.6}$$

$$t2_{CLAMP}, Vsafe_{CLAMP} < t2_{LDMOS}, Vsafe_{LDMOS}, \tag{2.7}$$

where LDMOS is the device to be protected by the clamp and Vsafe is its breakdown voltage.

If this does not apply, the clamp is not suitable. To evaluate if the clamp will partially protect the device the SOA parameters should be extracted at the lower stress levels for the clamp and comparison can be done again. Another approach is to plot parameters against each stress level and compare. This will be discussed in more details in Chapter 4. The equations 2.5 can be replaced with a graphical representation by plotting V(t) and I(t) to more accurately represent the design window shown in Figure2.30. The clamp response needs to be within the NLMDOS response in the bast case. Other cases will be discussed in more details in Chapter 4.

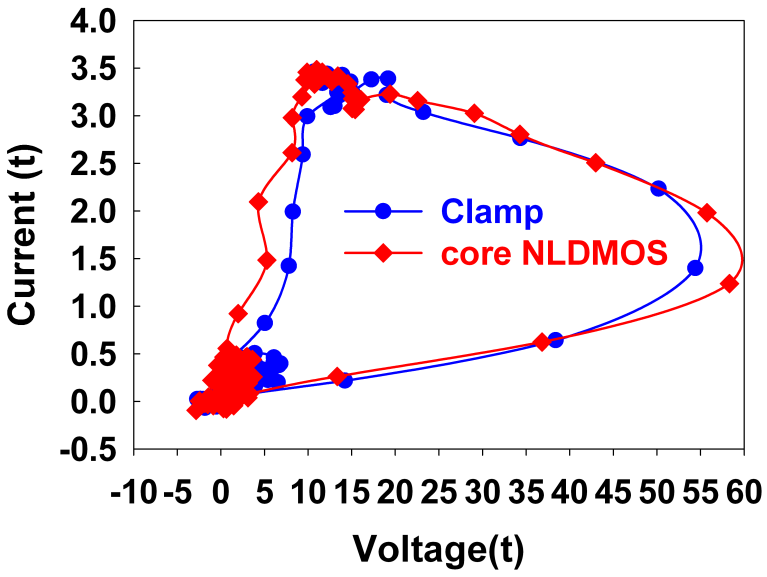

Figure 2.30: Graphical representation of TSOA usage for output pins

2.5 Chapter Remarks

Gate oxide breakdown is analyzed under very fast transmission line pulsed (VFTLP) stress, using different pulse -rise times and -widths. The switching of oxide behavior pre- and post- breakdown occurs in tenths of a nanosecond and it shows reproducible voltage and current characteristics. A high voltage protection clamp is analyzed in details under 10ns pulse width stress. The device behavior information that can be obtained by using quasistatic values is contrasted with the device behavior information that can be obtained by looking into the voltage and current waveform vs time. Based on transient behavior,

Transient Safe Operating Area (TSOA) and its parameters are defined to better describe both protection and protected devices under very fast stress conditions.

Finally,the conditions for protecting the input gate oxide are identified.

CHAPTER 3
TCAD FOR TRANSIENT SIMULATIONS

In the ESD field Technology Computer-Aided Design (TCAD) has been used as a tool to: decrease the number of design cycles, investigate new ESD structures [37, 58, 92–100], strengthen the process with respect to ESD, and also to study the unintended turn on of parasitic npn structures [101]. The design of the ESD structures via TCAD assumes that the design targets are clearly established and that the iterations in test chips are in order to fine tune the ESD protection devices.

During very fast transient ESD events, the response of different ESD protection devices needs to be investigated in greater detail using fast transient measurements and numerical device simulations.

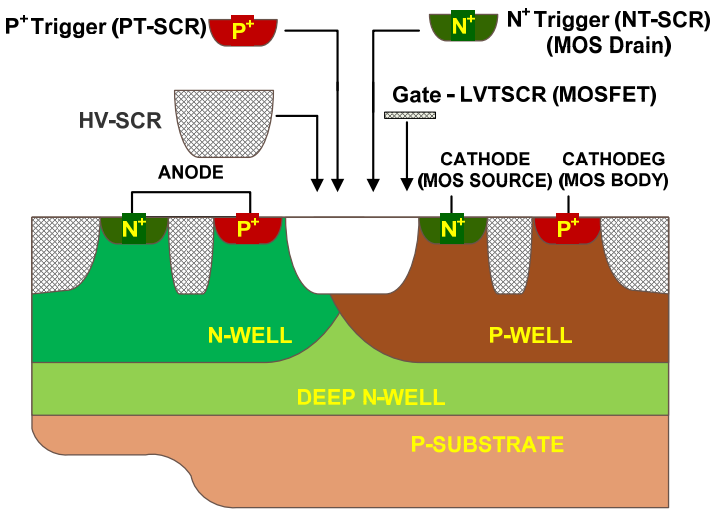

Figure 3.1: Structures whose transient device response is studied

In this section, the transient responses of low-(5V operation), medium-(12-15V operation) and high-trigger voltage (25-40V operation) ESD clamps developed in a mixed-signal high voltage 0.35 μm CMOS process technology are investigated through TCAD. The focus is on the protection devices turn-on time and effectiveness in providing protection within the core circuit ESD TSOA. TSOA includes the highest voltage vs time and corresponding current vs time the device can sustain prior to damage. A set of device structures with different geometries and topographies are characterized through numerical simulations and measurement to optimize their transient behavior.

Figure 3.1 shows the cross-sectional view of different ESD protection device topologies evaluated in this study. It includes the MOSFET with optimized ESD drain contact to Poly-gate spacing, with and without the lightly doped drain (LDD) implant, low voltage triggered

SCR devices (LVTSCRs) with and without LDD, SCR devices with p- and n- type triggering control implants (PT-SCR and NT-SCR), and for higher voltage operation, high voltage SCR devices (HV-SCRs) with P-WELL implant variation. Additionally, Laterally Diffused MOS (LDMOS) devices of both p and n type will be studied.

A simulation environment to assess the turn-on mechanisms in the topologies under study during very fast transients is implemented using Synopsys Sentaurus technology computer aided design (TCAD) numerical simulation tools [102–105]. Process simulation is performed in TSUPREM-IV (TS4). The fast transient measurements are obtained using a Barth model 4012 very fast transmission line pulse (VFTLP) system capable of generating pulse widths in the range of 1 to 10 ns and rise times in the range of 100 to 400 ps. A Keithley 4200 Semiconductor Characterization System with a pulsed I-V bias/measurement feature is also employed for pulsed-trigger measurements. Figure 3.2 shows the simulation framework flow.

Starting from the layout variables, the structure is built in TS4, then imported into Device Simulation Environment where it is simplified and meshed accordingly prior to the device simulation. A detailed explanation of the tool flow and setup used is given in Appendix A.

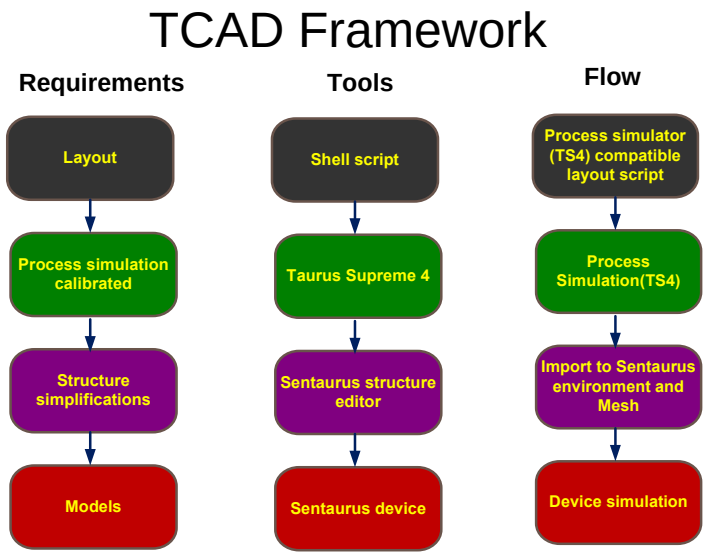

Figure 3.2: TCAD framework

The complete numerical simulation models are selected as follows: Poisson and continuity equations with drift-diffusion for the transport equation in conjunction with Fermi statistics.

3.1 TCAD Environment Calibration

3.1.1 Generation and recombination parameters

The TCAD device simulation environment is calibrated using specific "blocking junction" (i.e., p/n junction) configurations [92], MOS structures, and SCR structures [92, 93]. The cross section of the Blocking Junctions is given in Figure 3.3. The simulated and mea-

sured DC breakdown voltages for Blocking Junctions are given in Table 3.1 and a sample reverse bias simulation setup for a blocking junction voltage breakdown calibration is given in Appendix B.

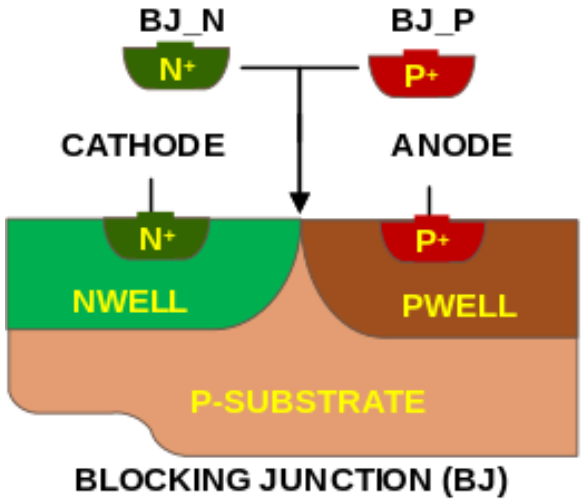

Figure 3.3: Blocking Junctions Cross Section

The Slotboom bandgap narrowing model [105] as well as the Shockley-Read-Hall carrier recombination model are enabled. Auger recombination is included to account for high electric field effects. The impact ionization model developed by Van Overstraeten de Man is also included and valid for temperatures of up to 700K [106]. This impact ionization model assumes the impact coefficient to be a function of the local field. The coefficient b in reference [106] for electrons and holes in the said impact ionization model was changed to 85 percent of their default value in order to match different junction breakdown voltages.

Table 3.1: Blocking Junction Breakdown Voltages

BJ type	Measured Breakdown Voltage(V)	Simulated Breakdown Voltage (V)
nwell-pwell (BJ)	34	35
nwell-p+ (BJ_P)	11	10.5
pwell-n+ (BJ_N)	8.5	8.5

The impact ionization parameter was calibrated during the Blocking junctions simulation.The figure 3.4 describes the available impact ionization models based on their physical or empirical origin and on the temperature range they cover.

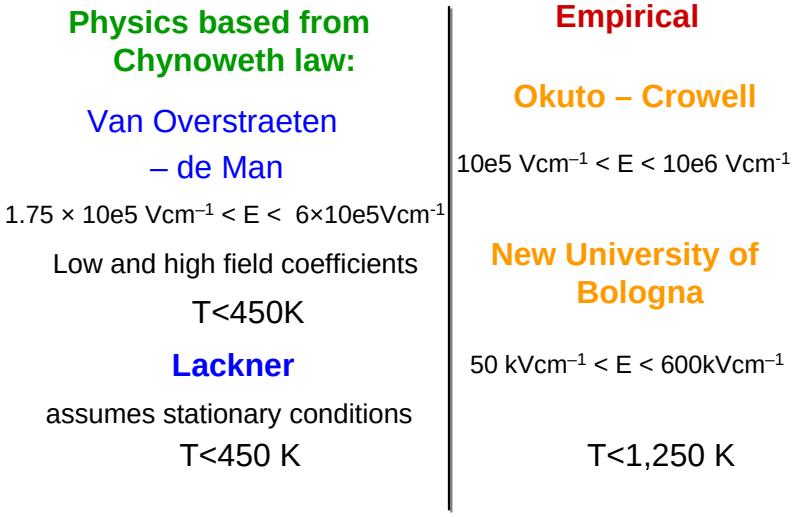

Figure 3.4: Impact Ionization Models Description

The chosen impact ionization model is the Van Overstraeten de Man, because it is a physical model with the highest temperature validity range available. The accuracy of temperature during the simulation is not the primary purpose of this work, but the information on the location and physical interpretation of the failure locations.

The generation and recombination calibrated parameters and the key words used in the simulation environment are listed in Table 3.2.

Table 3.2: Generation Recombination Parameters Calibration Values

Mobility components	Models Used	Default Parameter Value	Calibrated Parameter Value
Recombination	Shockley Read Hall and Auger	default	default
Impact Ionization	Van Overstraeten the Man	$electronsb(low) = b(high) = 1.231 \cdot 10^6, holesb(low) = 2.036 \cdot 10^6 b(high) = 1.693 \cdot 10^6$	$electronsb(low) = b(high) = 1.046 \cdot 10^6, holesb(low) = 1.731 \cdot 10^6 b(high) = 1.439 \cdot 10^6$
Band Gap Narrowing	Slotboom	default	default

3.1.2 Mobility parameters

The low field mobility is calculated by the Mathiessens rule and it incorporates the bulk- and surface- mobility [105]. The bulk mobility model is the Phillips unified mobility model [107], which is composed of lattice scattering and carrier-carrier scattering in the bulk. For the surface mobility degradation due to the normal electric field, the Lombardi model, which accounts for both the phonon and surface roughness scattering is used [105].

Simulated vs measured drain source current (Ids) vs. gate voltage (Vgs) for drain source voltage (Vds) of 50mV is given in Figure 3.5. The sample simulation setup for a DMOS device from import, meshing and device simulation is given in Appendix C.

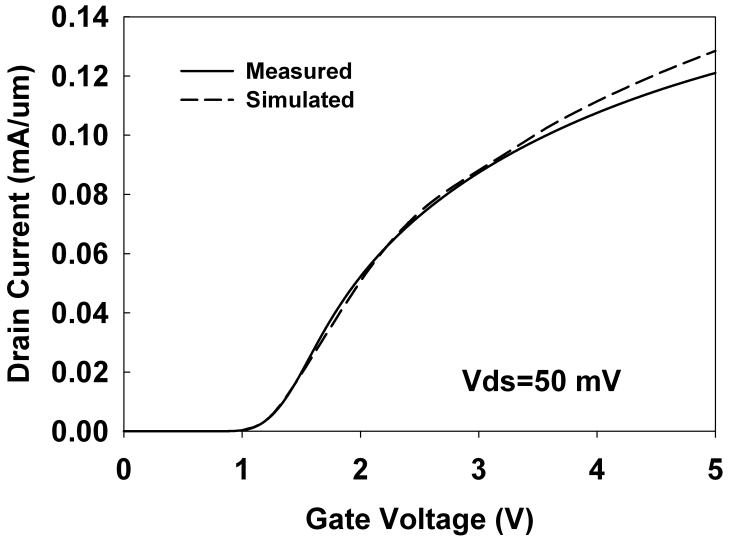

Figure 3.5: Simulated and measured Ids vs Vgs for Vds= 50mV

For high field mobility, the effect of high field saturation is accounted for by the Canali model [108]. High Field saturation parameters were calibrated by using the NLDMOS structure drain source current (Ids) vs drain to source voltage (Vds) for gate voltage Vgs of 5V. As NLDMOS exhibits self heating during the DC Keithey 4200 was used to obtain pulsed instead of DC version of Ids vs Vds for this calibration. The calibrated Ids vs Vds vs. measured one is shown in figure 3.6. Self heating effects were added in the next level of calibration.

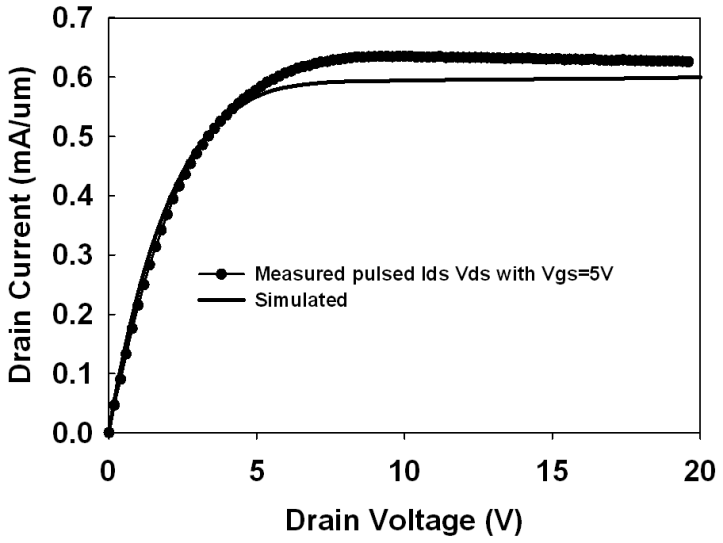

Figure 3.6: Simulated and measured Ids vs Vds for Vgs= 5V

The mobility calibrated parameters and the key words used in the simulation environment are listed in Table 3.3.

Table 3.3: Mobility Parameters Calibration Values

Mobility components	Models Used	Keyword in Sentaurus	Default Parameter Value	Calibrated Parameter Value
Bulk Mobility	Philips Unified Mobility	PhuMob	default	default
Surface Mobility Degradation	Lombardi	Enormal	$\lambda_n = 0.125$ $\lambda_p = 0.0317$	$\lambda_n = 0.1125$ $\lambda_p = 0.0317$
High Filed Saturation	Canali	HighFieldSaturation	$\beta_n = 1.109$ $\beta_p = 1.213$	$\beta_n = 1.5$ $\beta_p = 1.43$

3.1.3 The thermo-dynamic model

The thermo-dynamic model is enabled to account for self-heating. The thermal boundary condition is placed at the bottom of the structure at the substrate electrode which is kept at 300 Kelvin. In order to speed up simulations keyword AnalyticTEP which employs analytical equations for the power instead of the look up table of experimental values [105].

During the initial voltage overshoot the temperature effects are not dominant [37], but temperature effects are important to define the quasi-stationary characteristics [106]. The model assumes that the free-carriers temperature is the same as the lattice temperature,

which permits the use of drift-diffusion as the transport mechanism making the simulations time shorter.

As mentioned in figure 3.6 NLDMOS device was first calibrated in pulsed regime without the self heating effects. In this stage the DC response which exhibits the self heating was used to verify the thermal model. Figure 3.7 shows the simulated and measured DC response. The thermo dynamic model did not require any parameter adjusting.

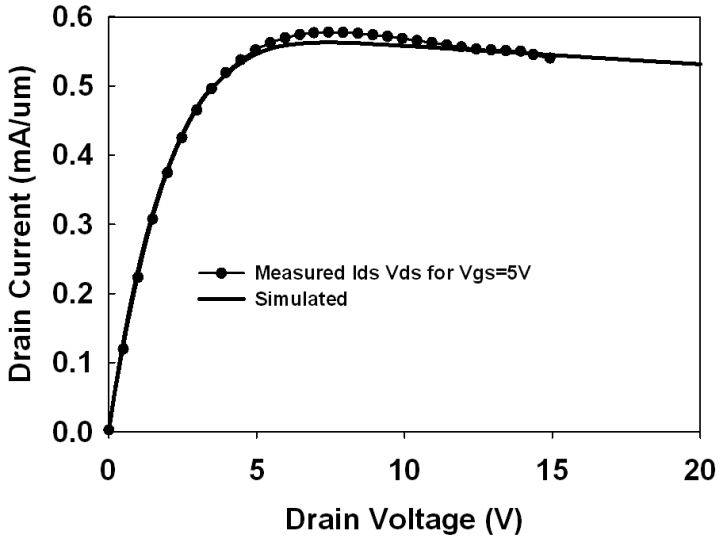

Figure 3.7: Simulated and measured Ids vs Vds for Vgs= 5V

3.1.4 Transient simulation

After calibrating the TCAD simulation tool using DC measurements,the VFTLP measurements are performed for correlation purposes. Figure 3.8 describes the flow for the

VFTLP measurement vs.simulation correlation. From the VFTLP measurement voltage and current vs. time are obtained.

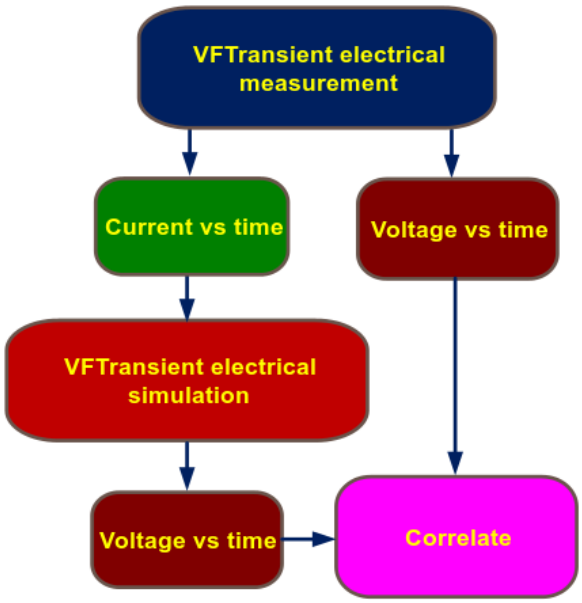

Figure 3.8: Transient calibration flow

The device is stressed in the simulation environment with the current obtained from the measurement and a simulated voltage time curve is obtained. Then, the simulated vs. measured voltage is compared in order to correlate.

Finally, an arbitrary transient stress is used to investigate the device response in the simulation environment. Figure 3.9 shows a first order RLC mixed-mode circuit used to emulate the input stimulus. The following values are used for the elements of the circuit to emulate CDM/VFTLP type stress: $R = 20\Omega$, $L = 80nH$, and $C = 2pF$. The capacitor is pre-charged to different voltage levels, thereby changing the peak current values discharged throughout the DUT.

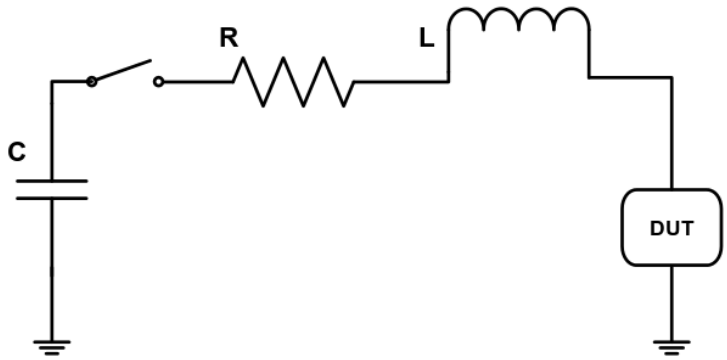

Figure 3.9: RLC circuit used to emulate an arbitrary input waveform

In the following sections the above mentioned TCAD strategy is applied to low and medium holding voltage devices to correlate RLC type stress with the VFTLP one. Afterwards, it is used to explain the high voltage DMOS device transient behavior and to optimize a high voltage clamp.

3.2 Low and Medium Voltage Domain Simulations

Figure 3.10 shows measured quasi-static response under a VFTLP of 1ns pulse width and 100ps rise time for GGMOSFET (60 μm wide), LVTSCR (90 μm wide) and NT-SCR (60 μm). Figure 3.10 is obtained by averaging the voltage and current in time between 25 and 75 percent of the duration of the pulse, thus omitting the critical values of the voltage and current at the beginning of each pulse.

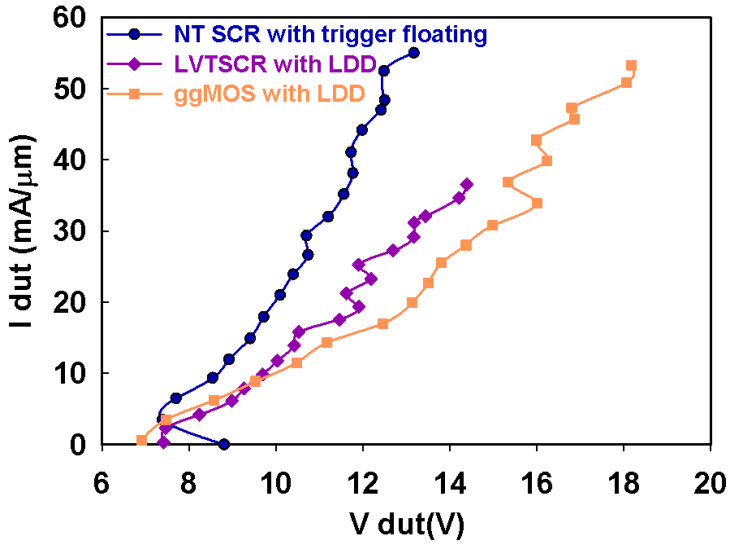

Figure 3.10: VFTLP measurement with 100ps rise time and 1ns pulse width for GGMOSFET, LVTSCR and NT-SCR

Figure 3.11 shows measured transient responses under a VFTLP Vpulse stress of 90V for GGMOSFET, LVTSCR and NT-SCR. Silicon Controlled Rectifier structures exhibit voltage overshoot and are slower to turn-on when compared to grounded-gate MOSFETs (GGMOSFET), which exhibit little or no overshoot. This makes GGMOSFET a good candidate for CDM protection. Furthermore, grounded gate MOSFET exhibits even lower overshoot when LDD implants are blocked. This is because the overlap capacitance of the LDD region is smaller than when LDD region is not present for grounded-gate devices [109]. For the two types of SCR the overshoot is comparable while the one obtained for the GGMOSFET is considerably lower. The low voltage triggered SCR, on the other hand, shows a lower voltage overshoot when the lightly doped drain is used, but adding

the LDD measurements show that it also increases the leakage current. The LDD regions enhance MOS conduction, resulting in extra base current in the embedded SCR PNP and consequently triggering the SCR regenerative feedback faster.

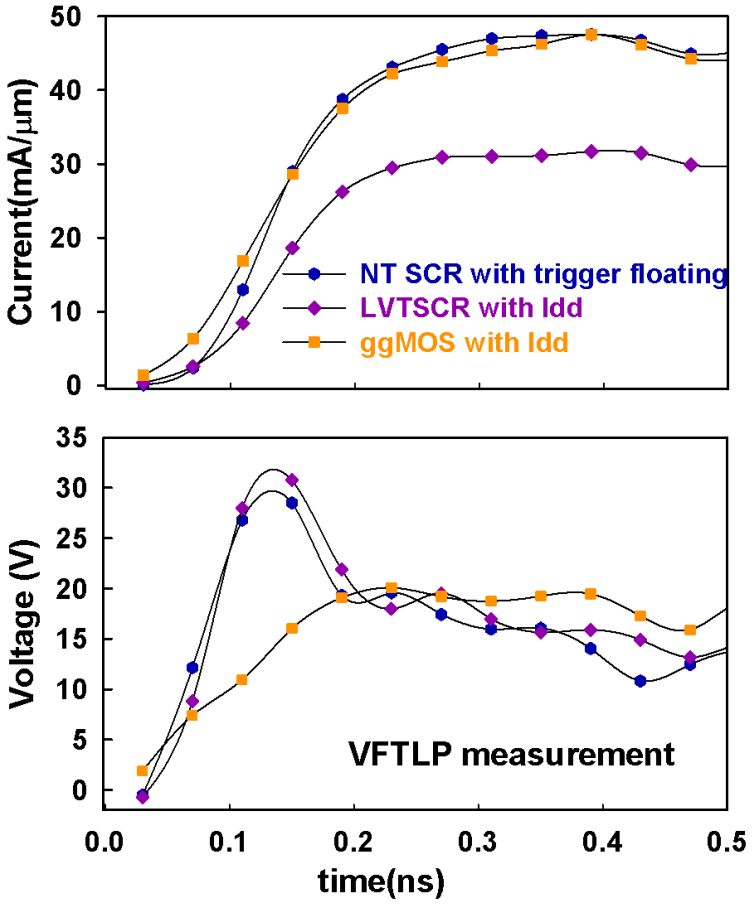

Figure 3.11: VFTLP testing comparing the transient response of GGMOS, LVTSCR, NT-SCR under Vpulse=90V

Consistent with the previous argument, Figure 3.12 compares the simulated transient responses in the devices with and without LDD during an arbitrary input stimulus generated by the RLC network in Fig. 3.9. Notice that the structure with LDD has a lower overshoot

and it responds faster, while the collector current of the PNP is consistently higher for the structure with LDD.

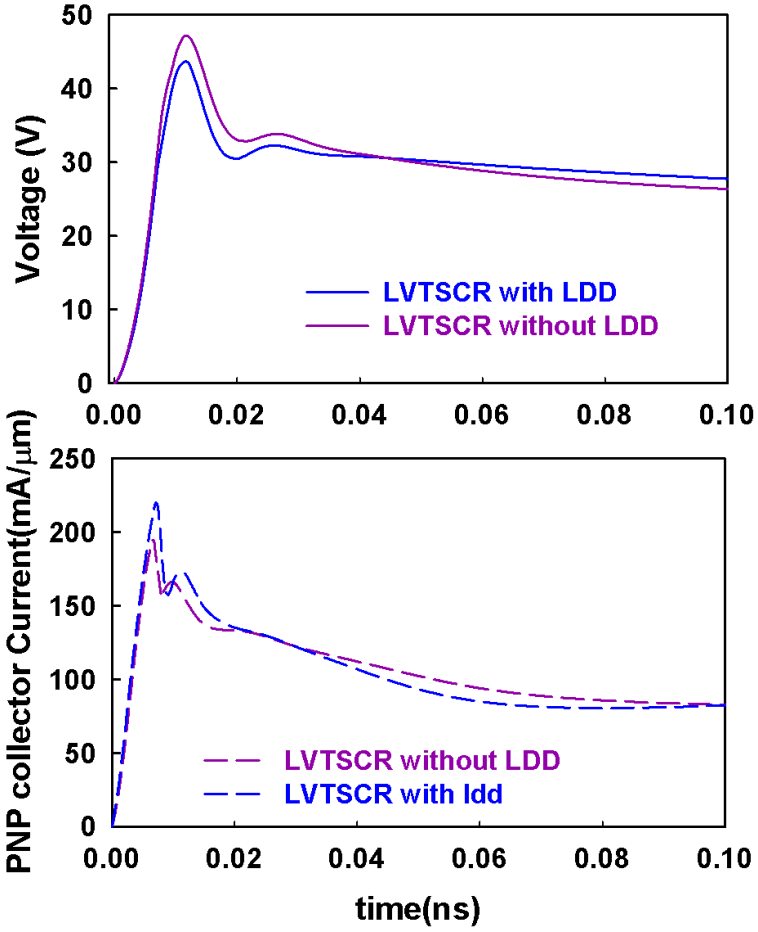

Figure 3.12: Simulation comparing the transient response of LVTSCR with and without LDD regions

Figure 3.13 shows simulated transient responses using the RLC simulation environment with the capacitor pre-charged to 30V. As compared with measurements in Fig. 3.11, it emulates in the simulation a similar current slope to the one obtained via measurements.

Notice that the current transient slope is slightly different between the VFTLP measurement and the TCAD simulation. Since the current stress is produced by the dynamic RLC interaction with the device and there are as well secondary effects in the measurements, the waveforms are expected to have different characteristics. As a result, the voltage waveform is not expected to match, but instead be used as a reference. Nonetheless, the TCAD simulation predicts accurately the tendency and critical turn-on behavior of the different device topologies. This information is to be used early in the design process and for device optimization.

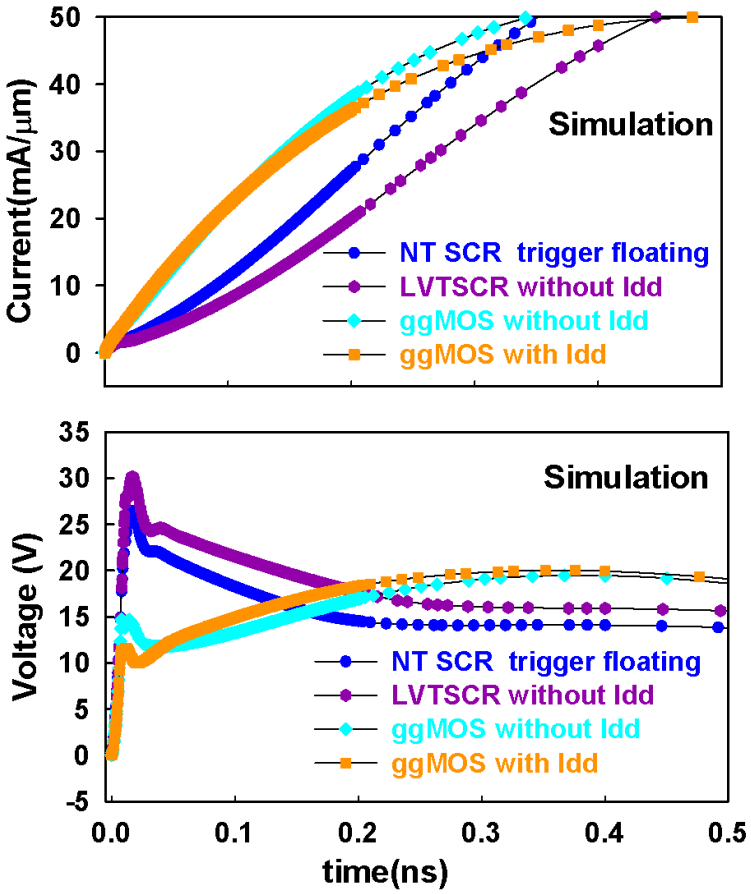

Figure 3.13: Numerical Simulation Comparing the transient response of GGMOS, LVTSCR, NT-SCR

The device characteristics in Fig. 3.10 and Fig. 3.11 are further analyzed by adding the level at which the protected devices are safe. Figure 3.14 shows the comparison of the different protection devices under the same highest pulse value they can sustain Vpulse = 60V, with the TSOA target added.

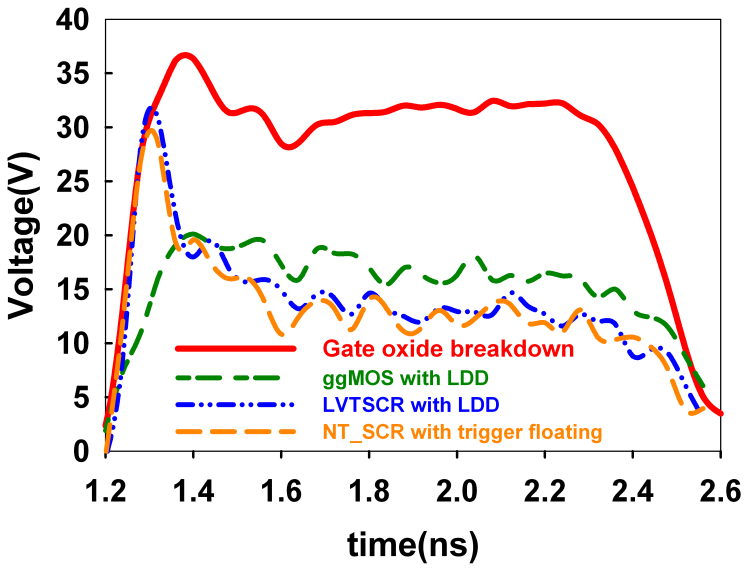

Figure 3.14: GGMOS, LVTSCR, NT-SCR and TSOA targets

Note on the current plot that the GGMOSFET starts conducting faster than the other two clamp devices. Under this condition, the GGMOSFET is the most effective protection component, while the other two devices require an extra series resistance to limit the maximum overshoot that the protected device is expected to see during a fast transient event. Occasionally, the overshoot can be safe for very large output drivers, in which case the protected device needs to be characterized to have a minimum self-protection capability to take some stress while the protection clamp is fully clamping the stress voltage to a safe level.

To investigate the transient response of the devices in the simulation environment, the measured VFTLP current was used as the input stress current for simulating an NT-SCR with n-trigger region floating and benchmark measurement versus TCAD simulations.

Figure 3.15 shows close agreement between the measured transient voltage waveform and the waveform obtained from numerical simulation. This was necessary for comparison purposes and calibration, since due to the very fast transient and the imperfections mentioned earlier in the applied/measured VFTLP waveform, the simulation results from an ideal pulse stress cannot be directly compared with the VFTLP measurements.

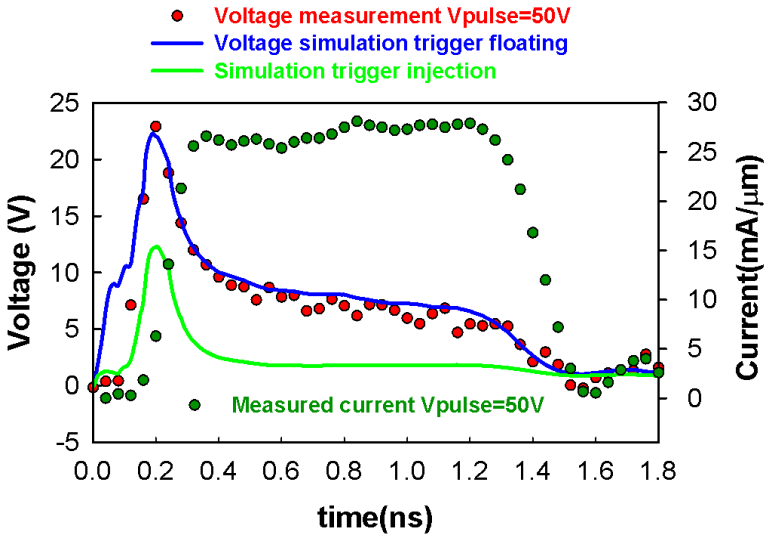

Figure 3.15: Correlation of an NT-SCR measurement and simulation under VFTLP, and simulation by injecting trigger current

To further evaluate the effect of externally injecting different level of majority carriers in similar SCR topologies, differing only by a p- and n-type trigger region (refer to Fig.3.1), the trigger effect was simulated and a similar effect was also measured under a quasi-stationary (500-ns pulse) conditions, varying the levels of DC current injected in the trigger implant.

The expected effect of injecting electrons (holes) in the n- (p) -region triggered SCR is a lower trigger and resulting voltage overshoot. Figure 3.16 shows the quasi-static triggering voltage change as a function of injected current for both PT- and NT- SCRs with and without deep NWELL. In the NT-SCR, the effect of the different injection levels on the trigger voltage is similar regardless of the deep NWELL. For the PT-SCRs without deep NWELL, a portion of the injected holes go to the substrate resulting in less efficiency of the injection to turn the device into the on-state. It explains the higher level of current injection required in PT-SCR without deep NWELL to create the necessary condition to modify the trigger voltage in the device.

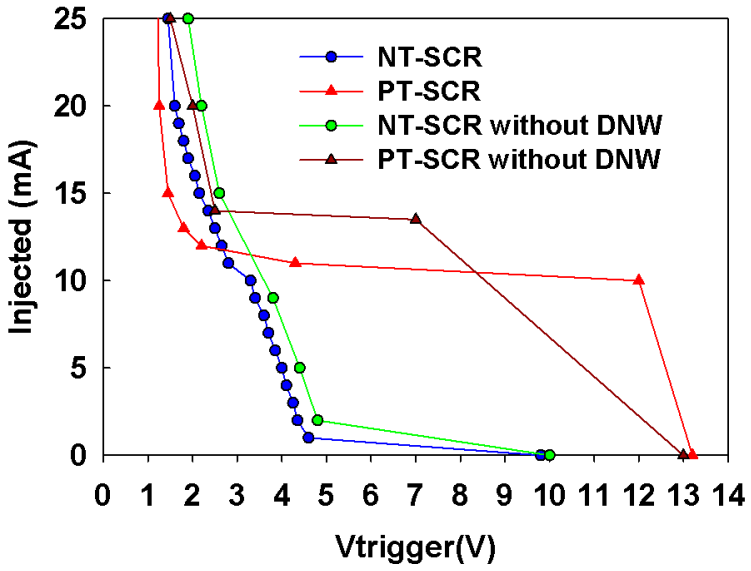

Figure 3.16: Comparison of the triggering voltage of NT- and PT-SCRs with and without the deep n-well

Comparing the change in the trigger voltage for the NT- versus the PT-SCRs, the NT-SCR shows in general a lower trigger voltage, but it also requires lower levels of current injection to substantially reduce the trigger voltage, which is desirable from a circuit design point of view. This makes this type of device topology more controllable and recommendable for conditions where the natural trigger voltage (close to 10 V in this example) is high enough for the required input/output operating conditions.

3.3 High Voltage ESD Protection Structure Optimization

For high voltage operating circuitry, the very fast transient simulation framework was also used to investigate and optimize a high voltage triggering SCR. This high voltage clamp was initially characterized by standard 100 ns pulse stress current. In this initial testing, the device was able to sustain over 5A of TLP current without failing. However, an unexpectedly much lower failure current of 2A was observed under very fast transient measurements and faster than HBM (Human Body Model) - type ESD events.

To evaluate the structure, TCAD was used to emulate the condition of stressing the device with the current from the VFTLP measurement of 5-ns pulse width and 100-ps rise time and Vpulse=60V. Figure 3.17 depicts the overlaid current waveforms for the device and the reference current on a short during the same VFTLP pulse voltage as well as the maximum lattice temperature evolution over time. Figure 3.18 depicts the overlaid voltage

waveform obtained from the simulation, the VFTLP voltage measurement, and the reference voltage on an open during the same VFTLP pulse voltage.

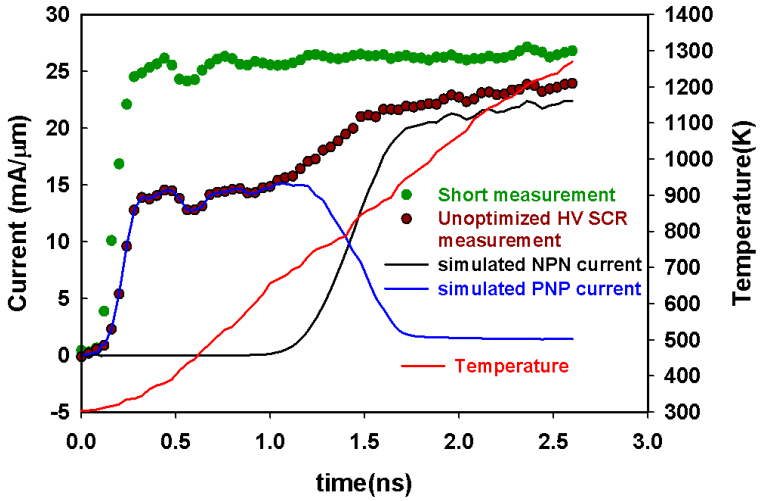

Figure 3.17: Terminal currents of the HV-SCR, short-current measurement reference, and temperature evolution over time

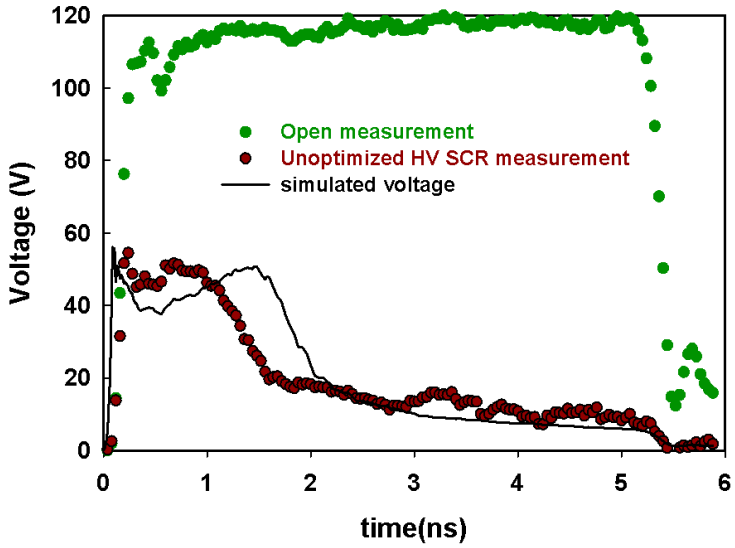

Figure 3.18: Voltage in time for HV-SCR and reference open voltage for the specific VFTLP pulse

By analyzing the current and voltage transient response, notice that during the large time the PNP section of the SCR is conducting a large amount of current, the temperature increases rapidly to levels where failure in the device can occur. This is corroborated in Figure 3.19, which depicts a micro-graph of the failure location and the 2D temperature simulation contours at the failure stress condition.

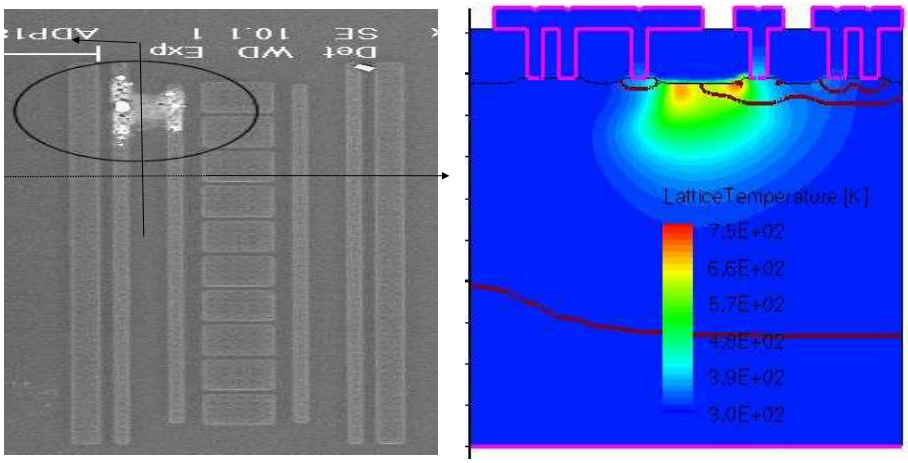

Figure 3.19: Micro graph from failure analysis of damaged obtained during the fast transient, (left) 2D VF simulation contour at the failure location at t=1ns (right)

The 2D simulation contour depicts a substantial over-heating in a relatively superficial path of the device during the fast transients and before full turn-on of the clamp regenerative feedback. By investigating this device via fast transient numerical simulations, the simulated hot-spot matches the damage location identified during the failure analysis. Consistently with observation from the transient response waveforms, it is attributed to the strong conduction of a parasitic lateral pnp bipolar during the first dV/dt, which at relatively low current level prevents the full turn-on in the clamp and leads to a localized failure. From this information, optimization in the device structure and interconnectivity is pursued to eliminate unintended parasitic triggering in the protection clamp. Modifications

in the structure commonly include variation in the terminals interconnects, 2-dimensional well spacing to increase unintended path breakdown and adjustment of the implant combinations used to define the pnp base doping. As discussed below, this optimization not only eliminates conduction in the path which produces the hot spot, but it also allows to reduce the time the device takes to clamp which was around 1.6 ns to around 0.5ns.

Figure 3.20 shows the simulation transient response comparing the terminal currents and temperature evolution over time for the optimized high voltage clamp device under the same current stress as in Figures 3.17,3.18 (VFTLP Vpulse of 50 V). Figure 3.21 shows the corresponding transient simulation voltage waveforms closely matching the VFTLP measurements.

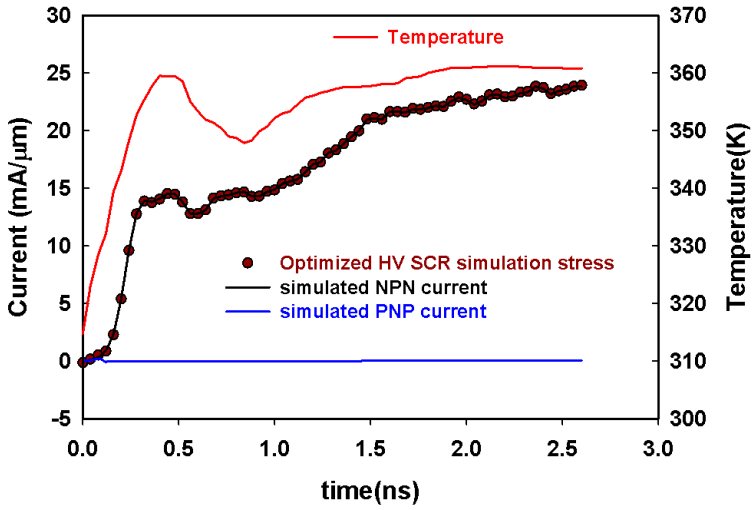

Figure 3.20: Terminal currents and temperature evolution of optimized HV-SCR

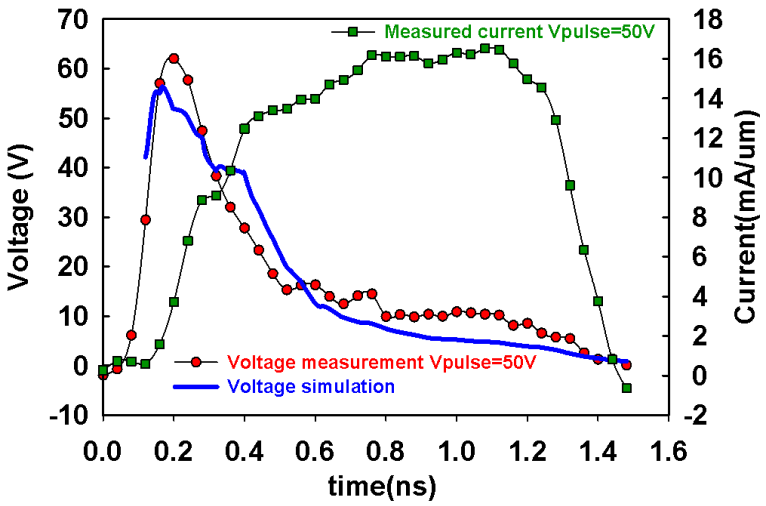

Figure 3.21: Transient voltage measurement and simulation of optimized HV-SCR

The conduction through the pnp parasitic bipolar has been greatly reduced by increasing the base width and substantially increasing the resistance in the pnp collector. As a result, the conduction is no longer throughout the surface pnp path and the maximum temperature is substantially reduced to a safe level. More importantly, the predicted and measured turn-on time of the device is reduced as compared with the previous clamp topology, improving the ability of the clamp to provide reliable protection to sensitive high voltage core devices.

To further compare the clamping characteristics during very fast transient between the initial high voltage clamp and the optimized one, Figure 3.22 shows the VFTLP quasi-static I-V characteristics obtained using a pulse with 100ps rise time and 1ns pulse width. For the initial structure, the clamping voltage stays at a relatively high level for most of

the pulse width and reaches a hard failure close to the 20 mA/μm level. Consistent with previous discussion, the surface conduction characteristic is impeding the device to reach the full clamping condition during the fast transient, which in cases can be as well a desirable effect to optimize holding voltage/ESD requirements trade-offs. On the other hand, the optimized device does reach the full clamping condition during the fast transient, adequate conductivity modulation, and it is able to sustain a substantially higher level of stress without failure. In general, however, important information is missed just by looking at the quasi-static I-V characteristics during fast pulses. For this reason, a detailed analysis of the voltage and current transient response of the device provides more accurate information to define the TSOA of the core device as well the design targets than the quasi-static I-V measurements, which only show the average voltage and current in a predefined section of the pulse.

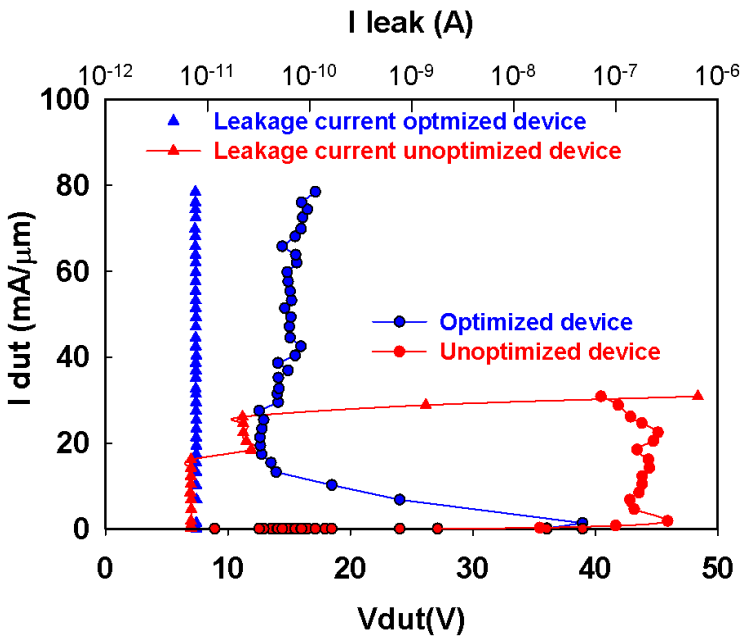

Figure 3.22: Quasi-static response under VFTLP testing with pulse width of 1ns, rise time of 100ps for a 90 μm wide optimized and unoptimized clamp devices. The leakage current is measured at 25V

3.4 Chapter Remarks

The ESD protection clamp response were investigated via very fast transient measurement and simulations to obtain optimized device performance for different mixed-signal high voltage applications. Turn-on behavior and voltage overshoot of ESD protection topologies subjected to CDM-like very fast transient pulses affect the capability of these devices to provide effective ESD protection of sensitive input gates or high voltage core devices. Strategies were investigated in this study via very fast transient numerical simulations and VFTLP

measurements. Solutions that combine device structure optimization and external majority carrier injection were proposed to optimize the ESD device performance and achieve a faster clamping response.

CHAPTER 4
TSOA FOR HIGH VOLTAGE DMOS UNDER PULSED CONDITIONS

Integrated Circuit (IC) specifications for emerging mixed-signal high voltage automotive, medical and ever expanding portable applications require a large combination of one time/multiple time programmable (OTP/MTP) memory, DSP interfaces, MEMS sensors, high voltage drivers, power signal conditioning circuits, among other functional blocks into the same die. These are traditionally defined in the industry as separate IC solutions. To enable this new level of SoC (system-on-a-chip) integration of solutions on high voltage fabrication processes, ESD (electrostatic discharge) design methodologies must be integrated as part of the high voltage interface. This is particularly necessary when it comes with the extra requirement of sustaining system-level ESD robustness at the IC-level. In light of the ESD susceptibility of high voltage N type Laterally Diffused MOS (NLDMOS) devices, previous studies have discussed the NLDMOS device failure mechanisms and design strategies to protect the high voltage devices by avoiding the destructive breakdown in the device [49–51, 110].

A new method to synthesize ESD robustness in high voltage functional blocks including NLDMOS devices is presented in this paper. This method shows that time plays a major role in the definition of the high voltage NLDMOS Safe Operating Area (SOA) and

the device ESD protection design window. The SOA under transient stress considered in this work is referred to as the Transient Safe Operating Area (TSOA). High voltage NLDMOS devices, clamps and clamps in parallel with NLDMOS in a mixed-signal technology are assessed under ESD-type pulsed stress conditions of 1, 2, 5, 10, 100 ns duration and Human Metal Model (HMM) pulses. This provides TSOA information used to define the energy constraint and practical conditions that enable the robust ESD design for advanced high-voltage mixed-signal applications.

4.1 Devices and Measurement Techniques

4.1.1 Devices

The NLDMOS devices in this study are designed and optimized for mixed-signal applications operating at 12 and 20V. The drain-source DC breakdown voltages of these devices are on the order of 21 and 32V for 12 and 20V NLDMOS, respectively. Their sizes vary from 200 μm to 20,000 μm. The main difference between 20 and 12 V versions are: 1) the Nwell implant-gate distance and 2) for the 12V NLDMOS, besides the deep-Nwell isolation implant around the device, there is an extra Nwell implant in the drain, which is not present in the 20 V devices. Dedicated protection clamps must be designed for NLDMOS devices that are not self protecting. ESD protection clamps are also evaluated in addition to the NLDMOS devices. In this study three clamps are evaluated: a low holding voltage

clamp (LHVC) and two high holding voltage clamps (HHVC1 and HHVC2). The clamps are characterized in standalone configurations and the LHVC and HHVC2 are also evaluated in parallel with the $200\mu m$ NLDMOS device to test the clamp protection effectiveness [50].

4.1.2 Measurement Techniques

The measurements and parametric extraction are obtained using an ESD characterization system that includes transmission line pulsed (TLP) and very-fast TLP (VFTLP) systems, Barth models 4002 TLP and 4012 VFTLP, a Keithley 4200 semiconductor characterization analyzer, a TESEQ NSD 438 ESD discharge gun and a Hanwa W5000M-WFC system for wafer-level HMM testing. To identify failure during the TLP/VFTLP measurements, the test procedure is streamlined to obtain pre and post DC parametric measurements during the VFTLP testing. The NLDMOS is tested using a two terminal RF probe with the drain pulsed positive versus the source, and the reference gate voltage is applied independently. The device under test (DUT) is laid out in a 4-pad configuration for this testing, with the body and the source shorted on-wafer and each of them connected as well to a separate pad to define the common ground reference of the different instruments. HMM packaged device measurement is performed by using the TESEQ NSD 438 ESD discharge gun with the IEC model RC discharge network ($R_{HMM} = 330\ \Omega$, $C_{HMM} = 150pF$). The testing on the NLDMOS devices performed according to the HMM standard, 10 positive zaps at the drain for each level, and gate was biased to evaluate accordingly the performance during on-

and off- state conditions. In addition, for the protection clamps 10 positive zaps are applied at the high side terminal for HMM robustness evaluation.

Figure 4.1 shows the flow chart used for packaged NLDMOS device HMM measurement. Prior to HMM stressing, a DC test for drain current versus gate voltage (Id-Vg) at Vd=0.1V is obtained. Subsequently, TLP measurements are obtained between drain and source with gate voltage Vgs=5V to verify functionality and compare it with on-wafer TLP measurements. The leakage current is then verified between drain and source for Vgs=0V. After the device has passed functional pre-test the gate voltage is set either for on-state testing (Vgs=5V) or off-state testing (Vgs=0V). In products, the on state condition is provided by an internal ESD detection circuit. For the testing in this work, a DC gate voltage of 5V was directly applied. For on-wafer HMM testing, the leakage current was measured to detect device degradation after 10 zaps at the same level.

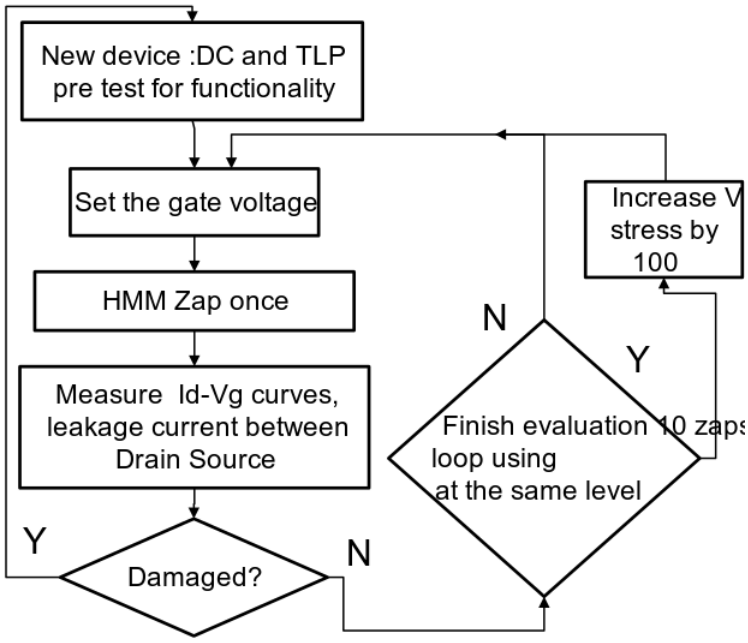

Figure 4.1: Packaged NLDMOS HMM measurements flow chart

The NLDMOS failure is identified either by an off-state leakage current change of an order of magnitude increase, or by a change in the threshold voltage (Vth). For 20V NLDMOS devices, the leakage current change correlates well with changes in the Ids-Vgs curve, while for 12V devices the Ids-Vgs curve degradation precedes drain-source off-state leakage current increase. Initial performance degradation in the normal operating region of the device is used as a failure condition in this work, but the actual failure criteria can be selectively defined as well based on the degradation tolerance of the circuit design of concern. For the case of two-terminal protection clamp device evaluation, the leakage current is monitored for damage detection, as initial measurements show no change in the

I-V curve prior to leakage current change. Each new clamp is pre-tested until snapback to confirm functionality prior to HMM testing.

Different sets of test patterns were packaged in a 28 pin ceramic-type package. The patterns included: 1) standalone NLDMOS devices, 2) standalone clamps, and 3) parallel clamp plus NLDMOS devices [50]. TLP/ VFTLP measurements were taken in 5V step increments with one single pulse (no pulse averaging) for all devices in order to compare them under the same stress conditions. The initial evaluation was done by using TLP measurements, followed by VFTLP measurements and finally ESD gun and on-wafer HMM measurements to assess the HMM robustness.

4.2 Laterally Diffused MOS (LDMOS) TCAD

Laterally Diffused MOS (LDMOS) devices are used frequently in mixed signal applications, and the desirable characteristics of such devices include high current/voltage handling capability and superior reliability qualification [49]. Designing an effective electrostatic discharge (ESD) protection solution for LDMOS in high-voltage mixed mode technologies is challenging because of the shrinking design window and the lack of information on LDMOS behavior under very fast transient ESD stresses [49–51].

The traditional ESD protection design window does not include time component and is defined solely by the circuit operating voltage and latch-up conditions [51]. For fast transient stresses, however, transient behavior plays a significant role in the ESD susceptibility,

and including the time factor is essential in developing the transient definition of the point prior to failure, or the transient safe operating area (TSOA) for ESD applications.TSOA includes the highest voltage vs time and corresponding current vs time the device can sustain prior to damage. The purpose of this work is to study the LDMOS subject to fast transient stresses and subsequently develop the LDMOS TSOA by using both measurements and TCAD environment. Specifically, the TSOA undertaken examines the failure conditions under the stresses of 1, 2, 5, 10 and 100 ns duration pulses generated by the transmission line pulsing (TLP) tester. A pulse duration of 100 ns was the only stress condition used in the previous studies [54, 110, 111], and this is the first time such a comprehensive TSOA is investigated and developed in the literature.

The technology used is a mixed-signal high voltage 0.35 μm CMOS, and the LDMOS devices studied are 20 and 12V laterally diffused PMOS (PLDMOS) and NMOS (NLDMOS). The cross sections of one half of the 200 μm total width, 4-finger NLDMOS and PLDMOS are shown in Figure 4.2 and 4.3, respectively. The finger lengths are 5.3 μm for both the 20 and 12V NLDMOS devices and 5.1 μm and 4.5 μm for the 20 and 12V PLDMOS devices, respectively. The DC source-drain breakdown voltages are approximately 32 and 21 V for the 20 and 12V NLDMOS, respectively and 31 and 16 V for the 20 and 12V PLDMOS, respectively.

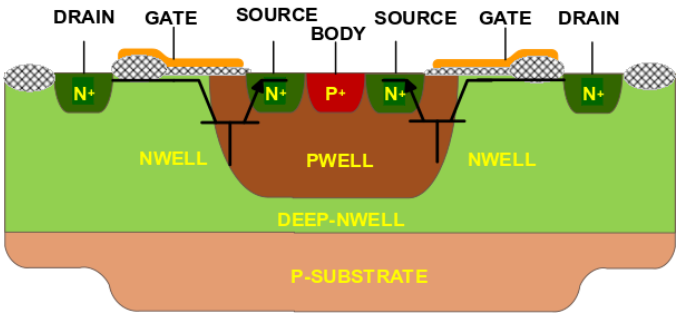

Figure 4.2: Cross section of NLDMOS under study with parasitic bipolar transistors depicted

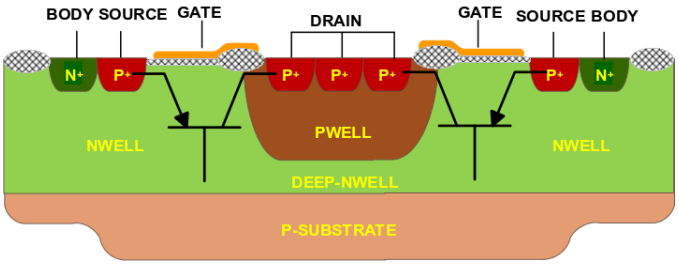

Figure 4.3: Cross section of PLDMOS under study with parasitic bipolar transistors depicted

Transmission Line Pulse (TLP) system, Barth model 4002, was used for generating 100 ns duration and 0.2 ns rise time pulses. The fast transient measurements were conducted using a Barth model 4012 very fast transmission line pulse (VFTLP) system capable of generating pulse durations in the range of 1 to 10 ns and rise times in the range of 100 to 400 ps. The experimental data and parametric extraction were obtained using a system that integrates a TLP/VFTLP, a controlled Cascade wafer probing system, and a Keithley 4200 semiconductor characterization analyzer. The schematic of the experimental setup is given

in Figure 4.4. The devices were laid out in a 4-pad configuration where the body and source were shorted, but each had a separate pad to ensure that the ground of the TLP/VFTLP is connected to the ground of DC parameter analyzer used for gate biasing. In the case of NLDMOS, the drain was pulsed with positive voltage pulses, while the gate was grounded or biased with a positive voltage. In the case of PLDMOS, the drain was pulsed with negative voltage pulses, while the gate was grounded or biased with a negative voltage. The devices were stressed with increasing TLP/VFTLP pulsing voltages until they failed, a condition detected at the point where the leakage current is suddenly increased by at least an order of magnitude [12].

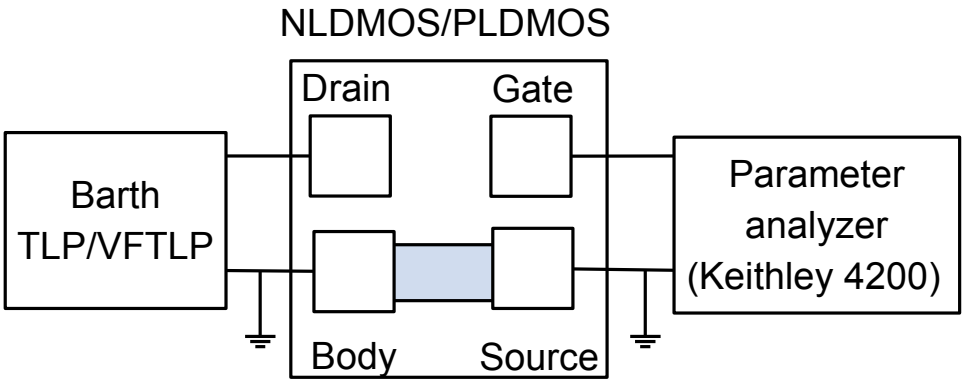

Figure 4.4: Schematic of experimental setup for stressing the NLDMOS and PLDMOS using TLP/VFTLP/HMM testers and parameter analyzer

TCAD simulations were carried out on 200 μm structures to provide physical insights into the TSOA analysis. PLDMOS and NLDMOS structures as shown in Fig. 4.2, 4.3 and were first obtained from the Taurus Supreme 4 (TS4) process simulator and then imported into Sentaurus device simulator.

In the first section we focus on the simulation of NLDMOS. The naming of the contacts is as follows: drain1 denotes the left hand side drain contact, and drain2 denotes the right hand side drain contact. The same applies to the naming of the source contacts. There is only one body contact. The calibration process consists of calibrating the velocity saturation for holes and electrons based on the measured drain current vs. drain voltage characteristics at different gate voltages, calibrating the surface mobility degradation based on the measured drain current vs. gate voltage characteristics, and calibrating the avalanche breakdown based on the measured drain current vs. drain voltage characteristics at zero gate voltage. In the TCAD environment, the NLDMOS and PLDMOS are considered failed when the maximum temperatures in the devices exceed 1100 K and 1500 K, respectively. These two threshold temperatures were obtained by first measuring the currents prior to device failure and then simulating the maximum temperatures in the NLDMOS and PLDMOS at these current levels.

4.2.1 N type LDMOS

Figure 4.5 depicts the measured quasistatic I-V curve of the grounded-gate, 20V NLDMOS stressed with 1ns duration and 100 ps rise time pulses. The two points of interest subject to pulse voltages of Vpulse = 28 (the snapback point) and 100 V (the TSOA point) are also marked. TCAD simulations were performed by applying the measured currents at these two points to the drain contact in the simulation environment.

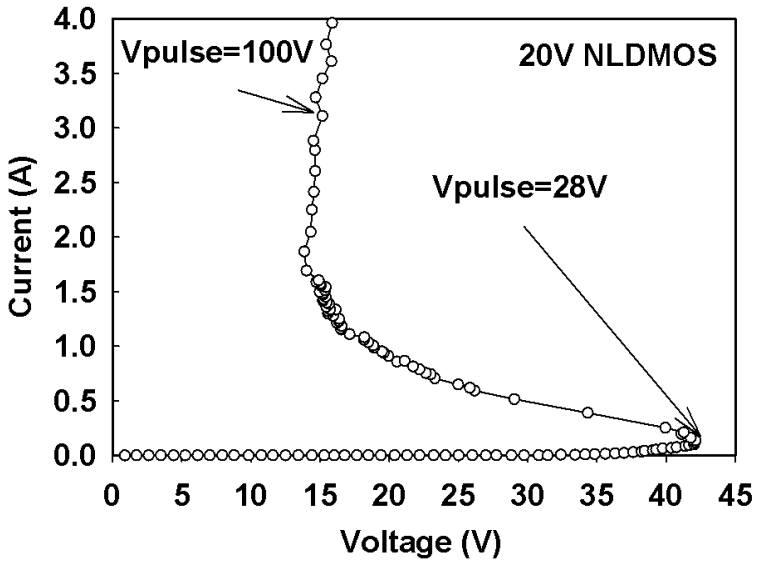

Figure 4.5: Measured quasistatic I-V curve of grounded-gate 20V NLDMOS under 1 ns duration pulsed stress

The two fingers in the NLDMOS are not simultaneously turned on at the snapback point, as demonstrated in Figures 4.6 , 4.7 showing the simulated drain/source currents at drain1 and source1 are much larger than those at drain2 and source2. Moreover, the relatively small pulse voltage does not trigger drain1/source1 finger until about 1 ns after the pulse applied to the device. The process simulator TS4 used emulates the implant angles and dosages in the fabrication process, so the processing-related nonuniform turn-on could be replicated in the device simulation. Figure 4.7 shows that the simulated drain voltage is in good agreement with the measured counterpart. The simulated maximum temperature, located near the drain junction, is also included in Figure 4.7. It indicates that while the

temperature in the NLDMOS goes up rapidly when the device is turning on, the temperature level is still quite low (less than 360 K) due to the limited current conduction at this point.

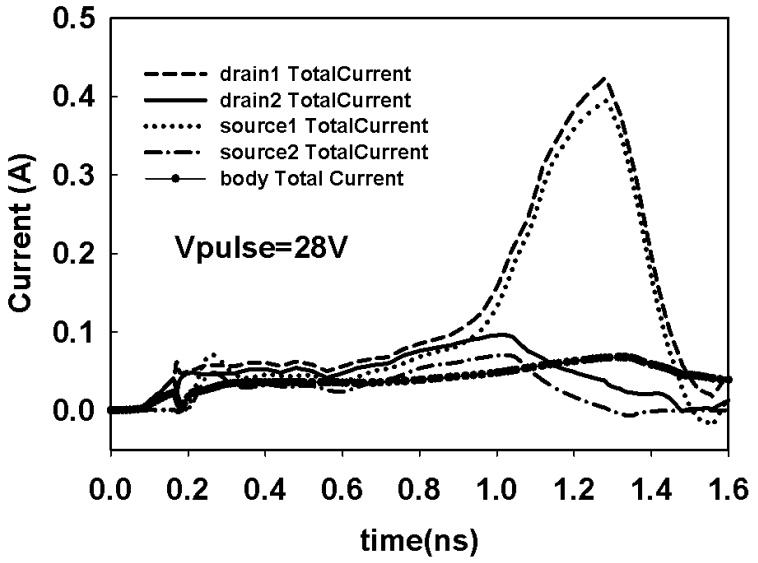

Figure 4.6: Simulated currents for 20V NLDMOS at Vpulse = 28 V

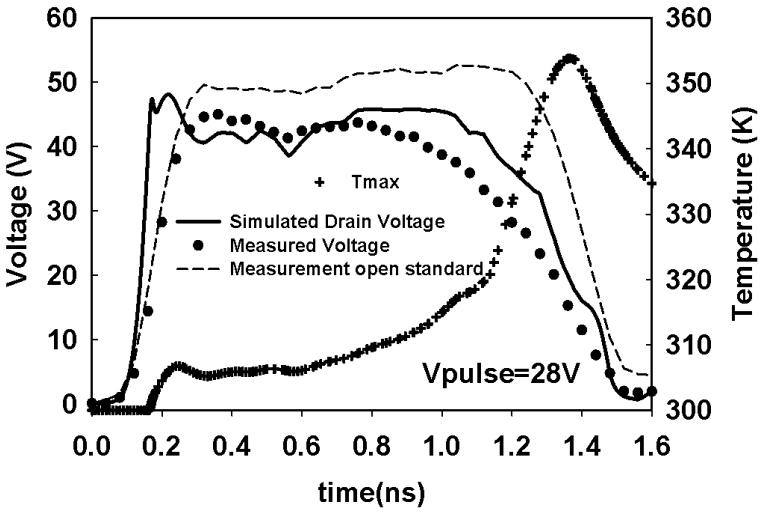

Figure 4.7: Simulated and measured drain voltages and simulated maximum temperature for 20-V NLDMOS at Vpulse = 28 V

Similar trend for the case of gate biased at 5 V is found, as shown in Figure 4.8. Consistent with previous results, nonuniform finger turn-on is found, but the current level at the beginning of the conduction is higher than that of the grounded-gate case owning to the presence of channel conduction in the NLDMOS. The same characteristics can be observed through the body current comparison.

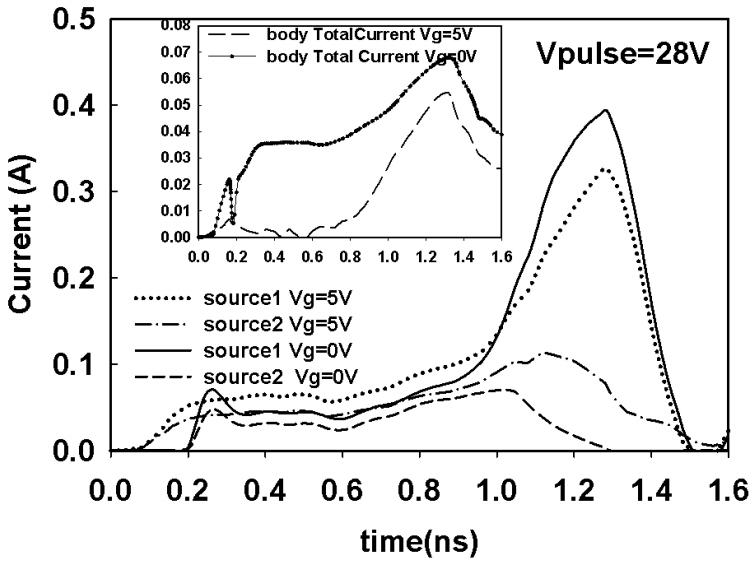

Figure 4.8: Simulated source currents for two different gate voltages of 0 and 5 V at Vpulse = 28 V

Unlike those at the trigger point, both fingers are turned on at the TSOA point (i.e., Vpulse = 100 V), as illustrated by the large drain1 and drain2 currents in Figure 4.9. The 100 V pulse voltage used is sufficiently large to force both fingers to conduct the current not only simultaneously but also instantaneously (see Figure 4.9).

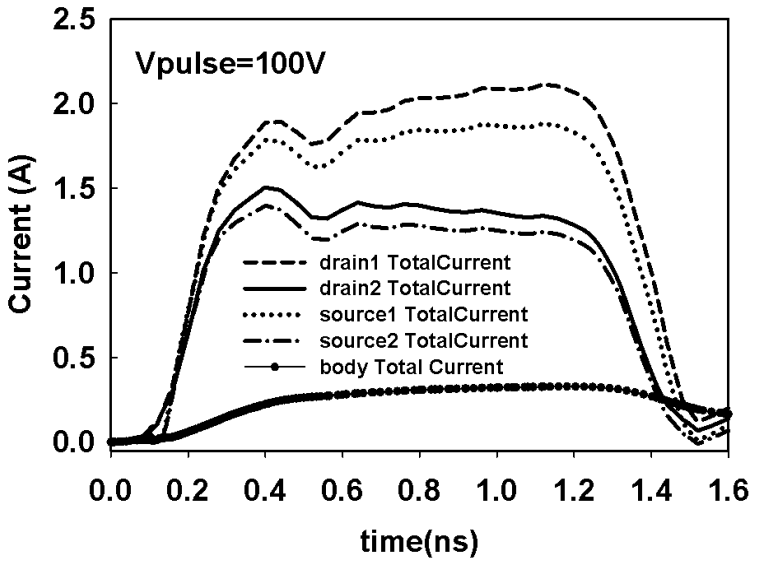

Figure 4.9: Simulated currents for 20V NLDMOS at Vpulse = 100 V

Figure 4.10 shows that the simulated and measured drain voltages agree well with each other. The maximum temperature now exceeds 1100 K due to the high current conduction at the TSOA point. Here, the device enters the reverse breakdown mode, the parasitic n/p/n bipolar junction transistor (BJT) turns on, the base push-out prevails, and the conductivity modulation occurs due to significant free carriers created by impact ionization [112].

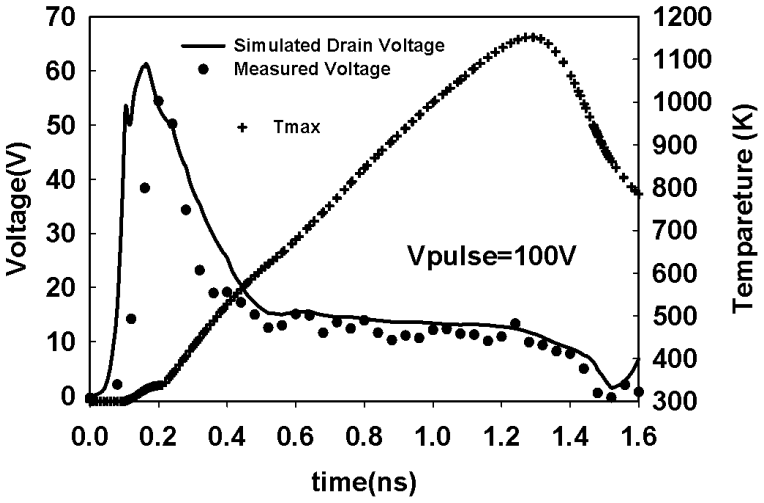

Figure 4.10: Simulated and measured drain voltages and simulated maximum temperature for 20V NLDMOS at Vpulse = 100 V

The evidence of base push-out can be seen in the simulated electric field contours given in Figure 4.11. Four focus points (Points a, b, c, and d) are considered, as indicated in Fig. 4.11(a), and the electric field contours at these points are given in Figs. 4.11(b)-(e). Clearly, the electric field in Nwell/Pwell junction (base-collector junction of the parasitic n/p/n BJT) starts to expand from Point a to Point b. Base pushout takes place from Points b to c and to d, as the maximum field is gradually pushed toward the N+ drain region (i.e., the end of the collector region).

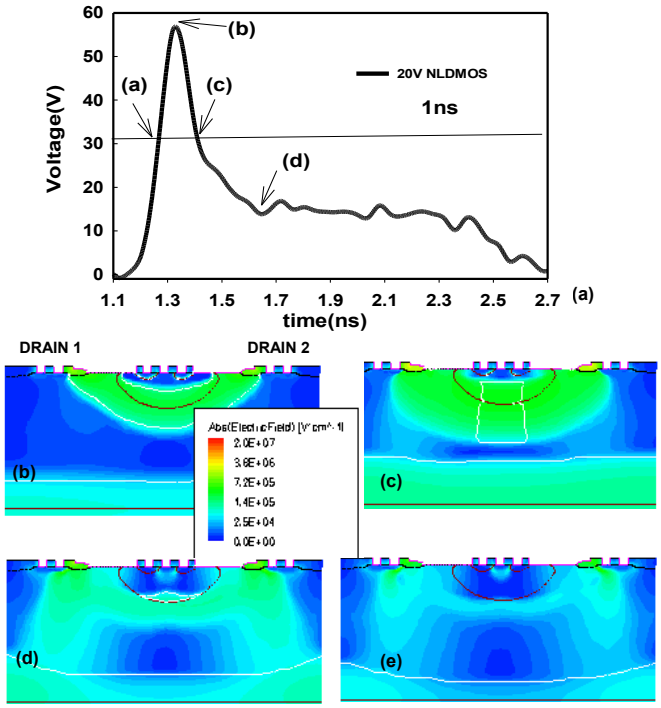

Figure 4.11: (a) drain voltage vs. time waveform of NLDMOS subject to Vpulse = 100 V stress with four focus points (Points a, b, c, and d) indicated, and simulated electric field contours at (b) Point a, (c) Point b, (d) Point c, and (e) Point d.

Figure 4.12 shows the effect of gate voltage on the drain voltage and maximum temperature in the NLDMOS at the TSOA point. Increasing the gate voltage only decreases and shifts in time the peak voltage and slightly increases the temperature, respectively.

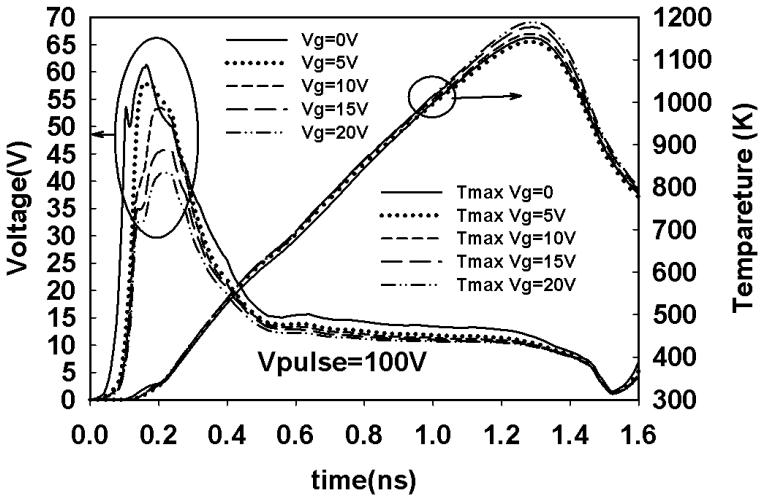

Figure 4.12: Simulated drain voltages and maximum temperatures of the NLDMOS at Vpulse = 100 V for different gate voltages of 0, 5, 10, 15 and 20

4.2.2 P type LDMOS

Next, we simulate the PLDMOS (see Fig. 4.3 under the transient stresses. The naming of the contacts is the following: source1 denotes the left hand side source contact and source2 denotes the right hand side source contact. The same applies to the body contacts. There is only one common drain contact.

Figure 4.13 depicts the measured quasistatic I-V curve of the grounded-gate, 20V PLDMOS subject to pulses having a 1 ns duration and 100 ps rise time. The two points of interest (i.e., trigger and TSOA points) stressed with 25 and 150 V pulse voltages are also marked. Notice that the PLDMOS does not exhibit snapback behavior due to the absence

of significant conductivity modulation in the parasitic p/n/p BJT owning to the relatively low hole mobility [112, 113].

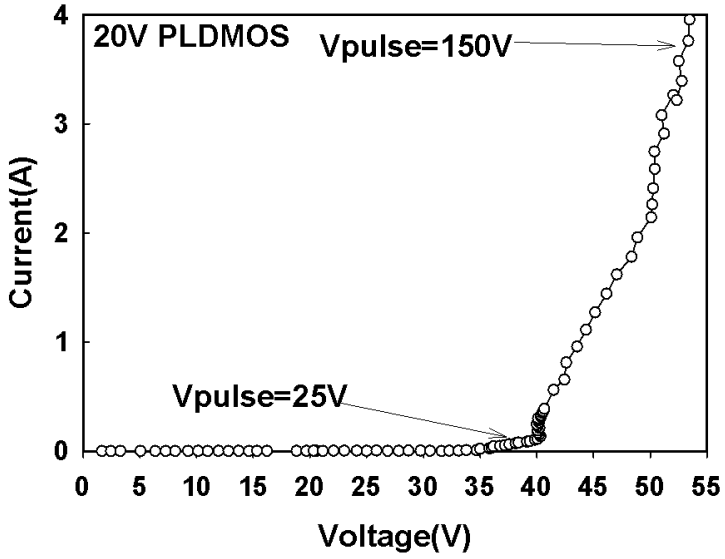

Figure 4.13: Measured quasistatic I-V curve of grounded-gate 20-V PLDMOS under the 1 ns pulse duration stress

Like the NLDMOS, only one finger in the PLDMOS is turned on and conducting the current at the trigger point, as evidenced by the fact that source2 current is much higher than source1 current (Fig.4.14). The body current is relatively high, suggesting that the reverse junction (P+ drain/Nwell) is also conducting. The maximum temperature at this point can reach 318 K (Fig.4.15).

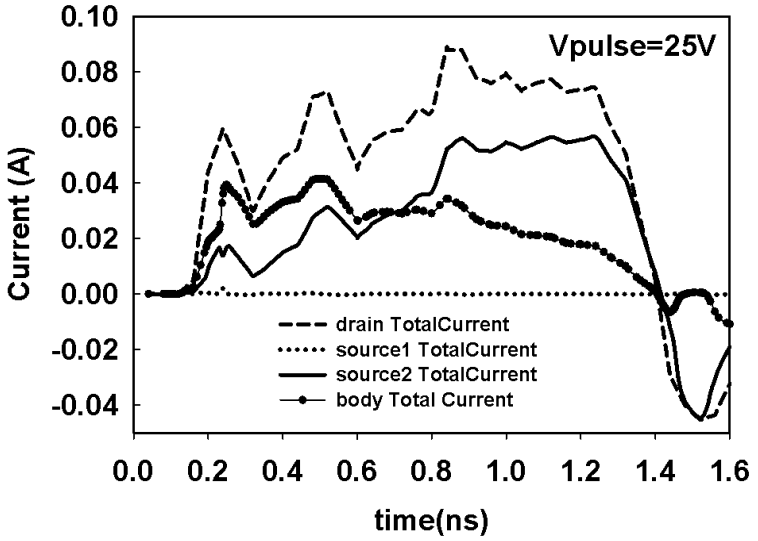

Figure 4.14: Simulated currents of grounded-gate PLDMOS at Vpulse = 25

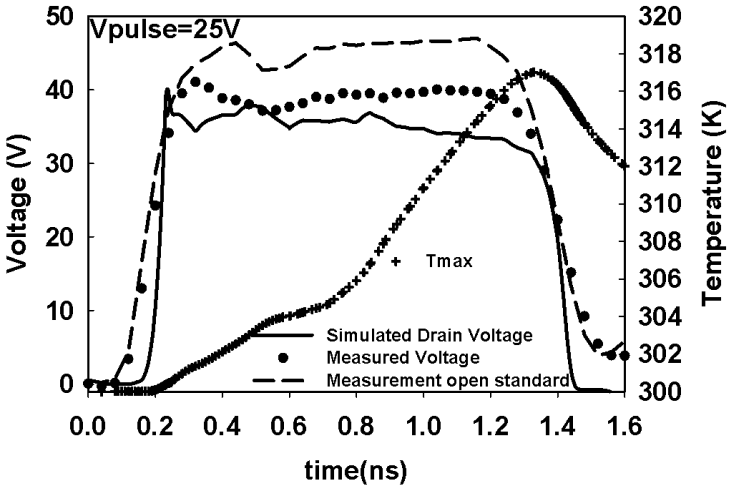

Figure 4.15: Simulated and measured drain voltages and simulated maximum temperature of grounded-gate PLDMOS at Vpulse = 25

As can be seen from the simulated currents for $V_{pulse} = 150V$ given in Fig. 4.16, both fingers in the PLDMOS conduct under such a stress condition. The maximum temperature exceeds 1500 K at this TSOA point (Fig. 4.17). The failure appears to be thermal-related and is located near the drain locos region. Figure 4.18 depicts the evolution of electric field contours in the PLDMOS at four different times. Unlike the NLDMOS, the electric field in the PLDMOS is generally confined in the Nwell/Pwell junction and no notable base pushout is observed from Points a to d. This gives rise to a larger voltage drop in the parasitic p/n/p BJT, and thus a larger voltage drop in the PLDMOS, than that in the base pushout prominent NLDMOS at a comparable current level [113], as evidenced by comparing the I-V characteristics at the two TSOA points in Figs. 4.5 and 4.13 (i.e., Vpulse = 100 V point in Fig.4.5 and Vpulse = 150 V point in Fig.4.13).

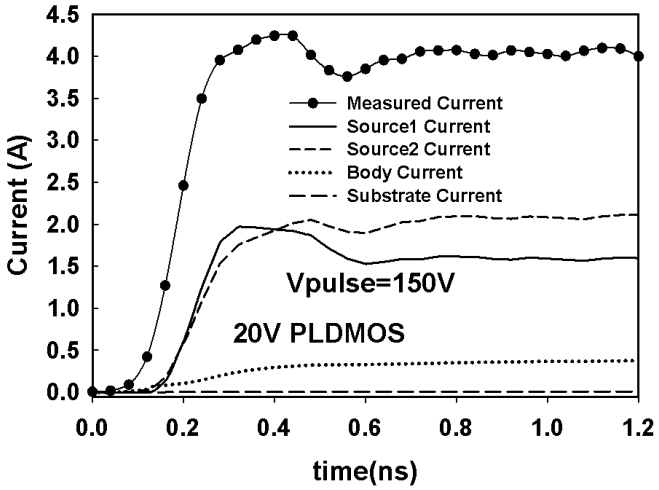

Figure 4.16: Simulated currents of grounded-gate PLDMOS at Vpulse = 150

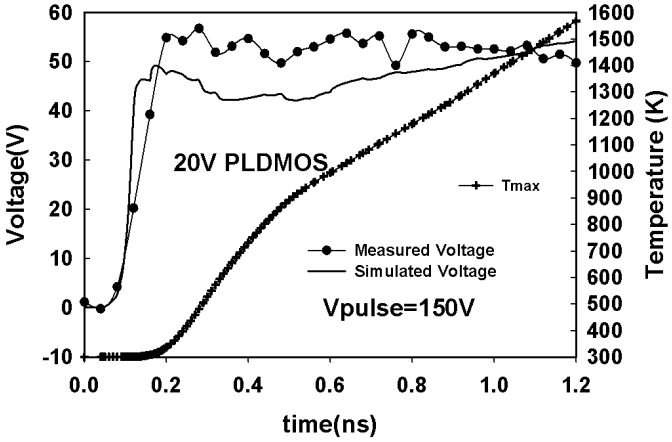

Figure 4.17: Simulated and measured drain voltages and simulated maximum temperature of grounded-gate PLDMOS at Vpulse = 150

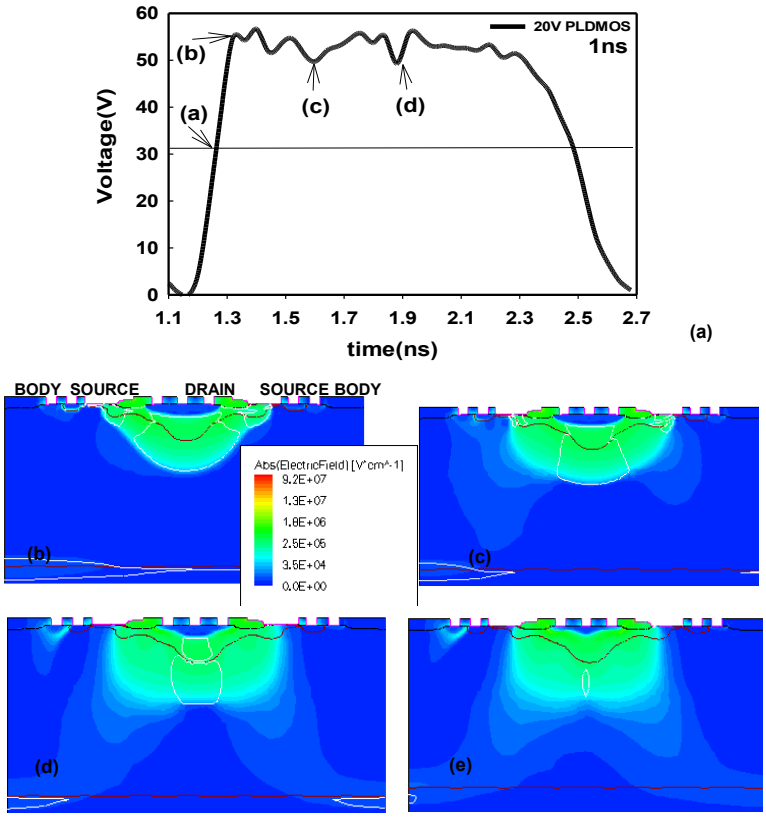

Figure 4.18: (a) Drain voltage vs. time waveform of PLDMOS subject to Vpulse = 150 V stress with four focus points (Points a, b, c, and d) indicated, and simulated electric field contours at (b) Point a, (c) Point b, (d) Point c, and (e) Point d

Figure 4.19 shows the effect of different gate voltages on the drain voltage and maximum temperature in the PLDMOS. The increasing gate voltage alters the voltage and temperature vs. time characteristics only slightly.

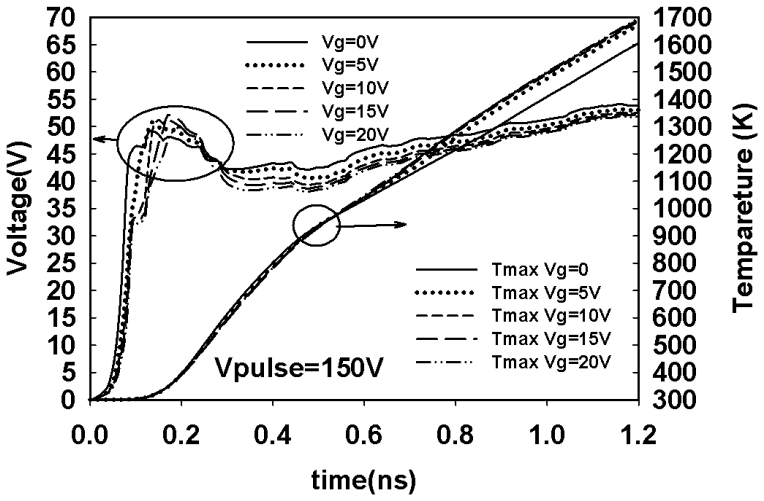

Figure 4.19: Simulated drain voltages and maximum temperatures of the PLDMOS at Vpulse = 150 V for different gate voltages of 0, 5, 10, 15 and 20

4.2.3 TCAD failure considerations for LDMOS

Transient safe operating area (TSOA), or the transient operating condition prior to failure, for NLDMOS and PLDMOS subject to transient stresses was analyzed and studied. Pulses with different durations and rise times generated from the transmission pulsing line (TLP) and very-fast TLP (VFTLP) testers were used to stress the devices under study. Technology computer-aided design (TCAD) simulations were also carried out to provide useful physical insights into the transient behavior of the devices operating at both the triggering and TSOA points.

The current and voltage TSOA waveforms mentioned earlier can be used to formulate the averaged power TSOA, PTSOA, as follows:

$$P_{TSOA} = \frac{1}{t_p + 2t_r} \int_0^{t_p+2t_r} V(t) \cdot I(t) dt, \tag{4.1}$$

where $V(t)$ and $I(t)$ are the transient voltage and current, respectively, tp is pulse duration, and tr is pulse rise time. Figure 4.20 compares PTSOA of all the LDMOS devices considered in the study. Clearly, the PLDMOS can sustain a higher power than the NLDMOS before they are damaged by the transient stresses. This may result from the lower free-carrier mobility and thus a smaller current density in the PLDMOS than the NLDMOS under the same stress condition, hence a higher PTSOA for the PLDMOS. In addition, the finding suggests that a longer pulse duration would result in the failure of both NLDMOS and PLDMOS at a smaller power dissipation.

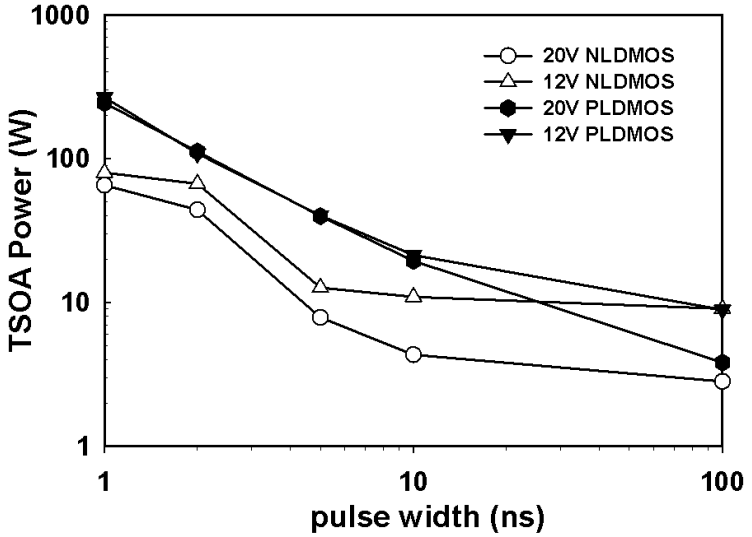

Figure 4.20: Comparison of averaged power TSOA vs. pulse duration for the 4 different LDMOS devices

The study suggested that the PLDMOS can sustain a higher power than the NLDMOS before they are damaged by the transient stresses. In addition, it was found that both NLDMOS and PLDMOS would fail at a smaller power dissipation when they are stressed with pulses having a longer duration.

We will proceed to evaluate the power within TSOA. Therefore, the critical temperature in power to failure calculations (Tc) [114] is to be lower then the melting temperature of silicon and needs to be determined. We will name this temperature Teffective as it will include: the effects of the temperature in silicon, the silicon and aluminum interface (for the contacts) and carrier injection into the locos which may lead to drain gate oxide breakdown. Drain gate oxide breakdown occurs in the case of very short stress where the drain

potential is very high [115]. As an example, Figure 4.21 shows both the TSOA waveform of the NLDMOS in grounded gate configuration and the drain gate TSOA in under 100ps rise time and 1 ns stress. To obtain drain gate TSOA pulses of the same kind were applied between drain and gate while other terminals were left floating. Observe that the pre breakdown voltage level of drain gate is similar to the voltage that the drain reaches in grounded gate configuration, but the high voltage lasts about 0.2 ns compared to 1.2 ns for the oxide pre breakdown. We do have to take into consideration the statistics into this problem in which case some oxides may be damaged faster [20] and the damage is not purely thermal. Therefore, Teffective of the NLDMOS may be much lower then the melting temperature.

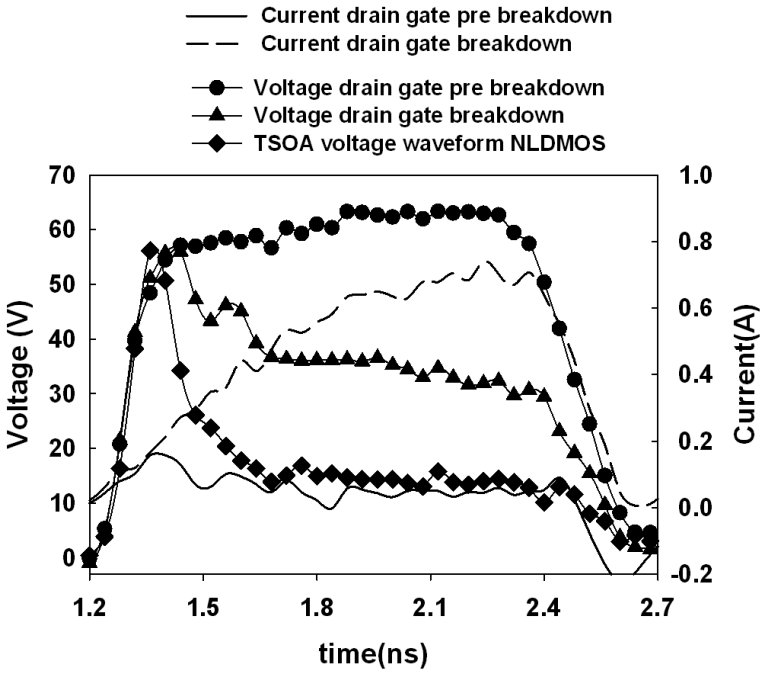

Figure 4.21: 20V NLDMOS TSOA for drain gate and for grounded gate configuration under 100ps rise time and 1 ns pulsed stress

Figure 4.22 shows both the TSOA waveform of the PLDMOS in grounded gate configuration and the drain gate TSOA in under 100ps rise time and 1 ns stress. In case of PLDMOS the TSOA voltage waveform for grounded gate configuration is much higher then the voltage waveform that describes TSOA for drain gate stress. Therefore, the damage is likely to be thermal only.

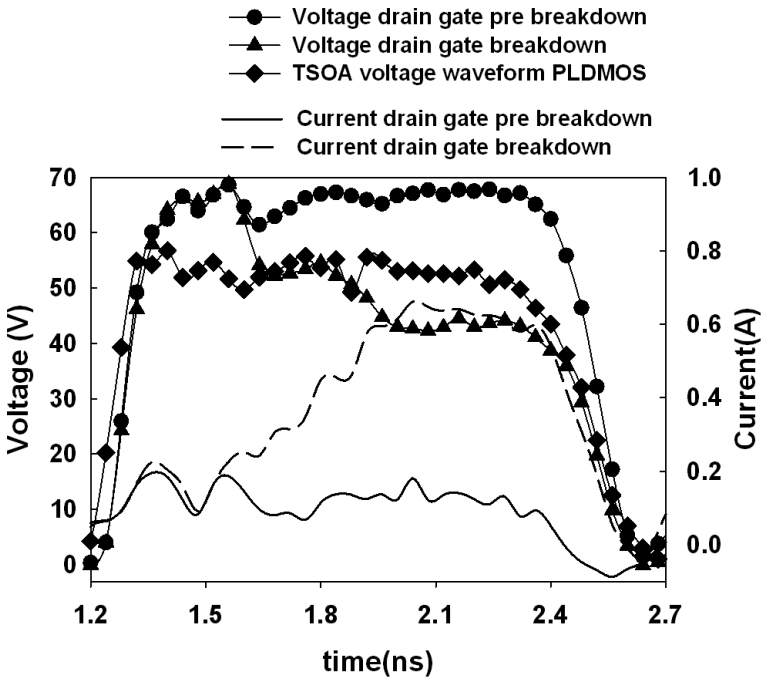

Figure 4.22: 20V PLDMOS TSOA for drain gate and for grounded gate configuration under 100ps rise time and 1 ns pulsed stress

By using the thermal failure model developed by Dwayer, Frankilin and Campbell [54] and TCAD results we can extract Teffective.The model is a solution of heat transfer equation, assuming that the rate of heating is constant inside and zero outside of the volume. The model has 4 major time divisions depending on the time to reach thermal equilibrium in each

direction (diffusion times) which are based on the 3 dimensions in increasing values c ,b and a. Dimension c corresponds to lateral depletion region width (in the direction of diffusion depth), b corresponds to vertical current flow depth (in the direction of the channel length) and a corresponds to the width of drain junction (direction of channel width). For the calculations we ignore the temperature dependence of thermal conductivity (W/cmK) and thermal diffusivity (cm2/s) [116, 117]. From TCAD TSOA level simulation results for 20V version devices we obtain the values of b and c: for NLDMOS b=3.7μm, c=1.2μm, while for PLDMOS and b=2.6μm and c=1.1μm. The finger width for both is a=50μm. This gives us the diffusion times for NLDMOS ta=2.3μs, tb=12ns and tc=1.3ns and PLDMOS ta=2.3μs, tb=6.25ns and tc=1.1ns. From Figure 4.20 we can extract by fitting the Teffective required for TSOA Power for both NLDMOS and PLDMOS which are respectively 500 and 1200 K. Figure 4.23 depicts the predicted TSOA Power vs. the measured power for 20V PLDMOS and NLDMOS.

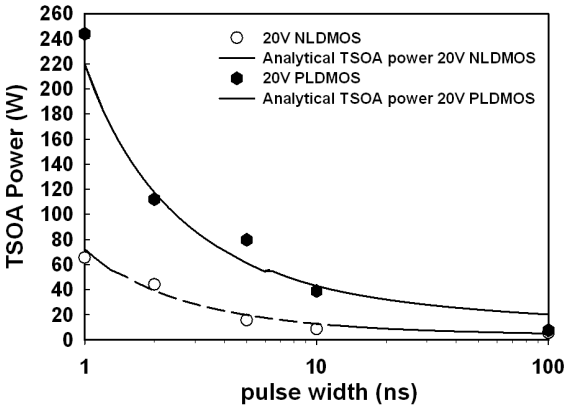

Figure 4.23: Grounded gate LDMOS 20V TSOA measured and predicted power vs. pulse width

4.3 NLDMOS TSOA and protection window

A. Grounded Gate 200 μm

We first consider the NLDMOS with gate grounded. Figure 4.24 depicts the measured drain current and drain voltage waveforms corresponding to the pre-failure pulses (i.e., the maximum pulses the devices can tolerate prior to failure) for the 12 and 20V NLDMOS devices subject to pulses with a 100 ps rise time and 1, 2, 5 and 10 ns durations. These waveforms are called the voltage and current TSOA. The instantaneous power TSOA is depicted in Figure 4.25. It can be seen that a large peak voltage, but with a very short high-voltage regime, appears on the devices before they are damaged for the cases of 1 and 2 ns durations. The magnitude of the peak voltage decreases and regime of the peak voltage expands as the pulse duration is increased toward 5 and 10 ns. Similar trends are found in the current TSOA and instantaneous power TSOA. Notice that the peak TSOA voltage is about 55 V for 1 and 2 ns stresses, a figure much higher than that of the NLDMOSs DC breakdown voltage.

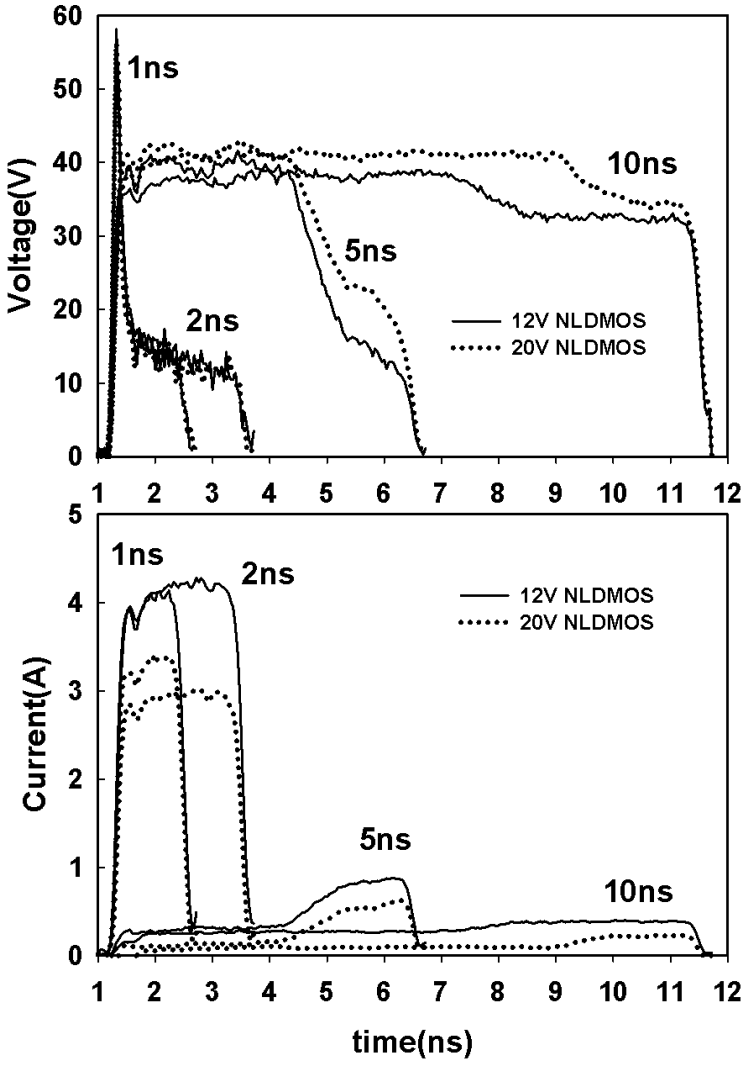

Figure 4.24: TSOA drain voltage and drain current transient waveforms for grounded-gate NLDMOS subject to pulses with different durations

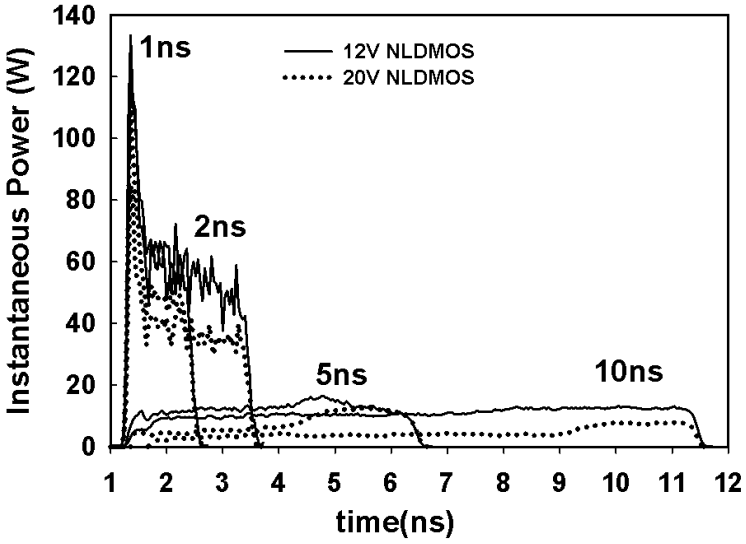

Figure 4.25: TSOA instantaneous power waveforms for grounded-gate NLDMOS subject to pulses with different durations

Figure 4.26 shows the quasistatic current-voltage curves obtained from the transient waveforms for the 1 and 100 ns pulses. These are the averaged current and voltage values taken from the transient waveforms in Fig. 4.24 between 25 to 75 percent timeframe for the 1ns stress and between 70 to 90 percent timeframe for the 100ns stress [12, 18]. All LDMOS start conducting right after the quasistatic trigger voltage (i.e., this voltage is the same as the DC breakdown voltage), and the difference between the 100 and 1ns I-V curves is very small.

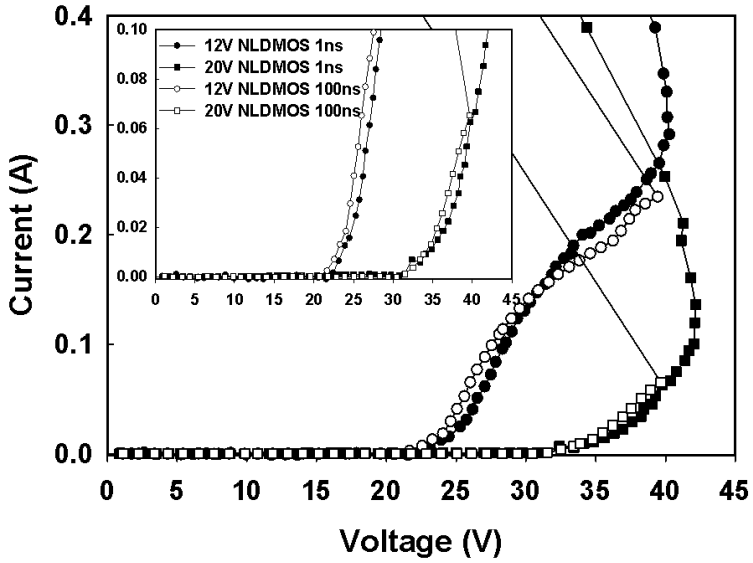

Figure 4.26: Measured quasistatic drain current vs. drain voltage curves of grounded-gate 12V and 20V NLDMOS under 1 ns and 100 ns pulsed stresses

Having the TSOA waveforms and knowing the devices start conducting immediately upon reaching the quasistatic trigger voltage independent of the pulse duration help the engineers to determine how big the devices need to be in order to be self- protected. The information also provides the guidance for designing the ESD protection devices when these devices need to be added to enhance the ESD tolerance of the NLDMOS.

B. Gate Voltage Dependence

Figure 4.27 shows the measured quasistatic I-V curves of the 12-V NLDMOS with a 5 V gate voltage and under the stresses of 1, 10 and 100 ns pulses as well as DC condition. For the MOS operation (i.e., prior to snapback), the results suggest that under the pulsed

conditions of 1, 10, and 100 ns durations, the device can sustain a current of 1.7, 1.4 and 1.1 times higher, respectively, than under the DC condition. This information can provide a guideline for estimating the device size for ESD self protecting purposes. The failure level for the NLDMOS is independent of the gate voltage, as after the snapback the device operation is governed by avalanche current generation irrespective of the gate bias condition.

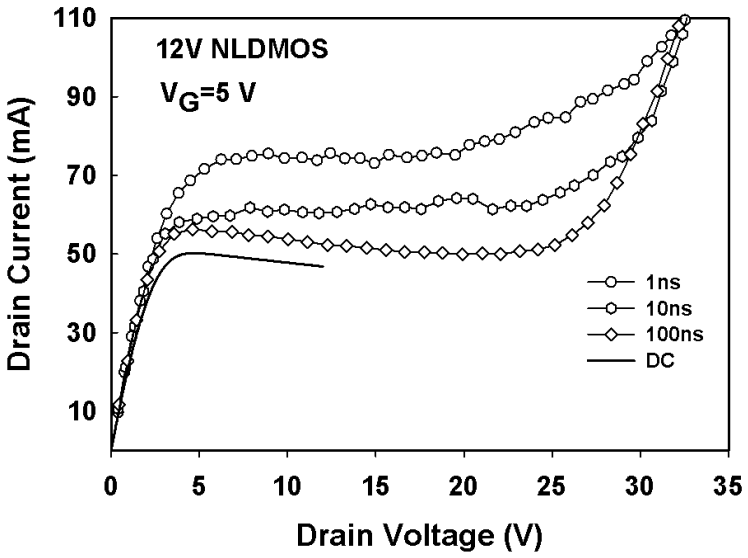

Figure 4.27: Measured quasistatic I-V curves of 12V NLDMOS biased with Vgs = 5 V and subject to DC and 1, 10 and 100 ns pulsed stresses

C. TLP Study for 200 μm to 20,000 μm NLDMOS devices

The standalone clamps and NLDMOS devices are initially tested using the TLP to assess: 1) overall TLP robustness, 2) conduction non-uniformity, 3) 12 and 20V NLDMOS devices characteristics in on-state (Vgs=5V) and off-state (Vgs=0V), and 4) differences between packaged and on-wafer TLP measurements.

Figure 4.28 shows on-wafer and packaged off-state measurements comparison for 20,000 μm width 20 and 12V NLDMOS devices. For simplification, only the leakage current of the 12-V device is shown as it shows an interesting decrease as the stress increases. This behavior is indicative of a walk-out effect and carrier injection into the LOCOS [118]. For the 12V devices, the incremental degradation is more clearly identified by monitoring the threshold voltage (Vth) changes during testing. The 20V device did not show significant degradation before failure, but the common condition in which the leakage current remains constant until it drastically increases right at the failure point. Packaged vs. on-wafer TLP measurements are similar, only showing relatively minor difference in the failure point.

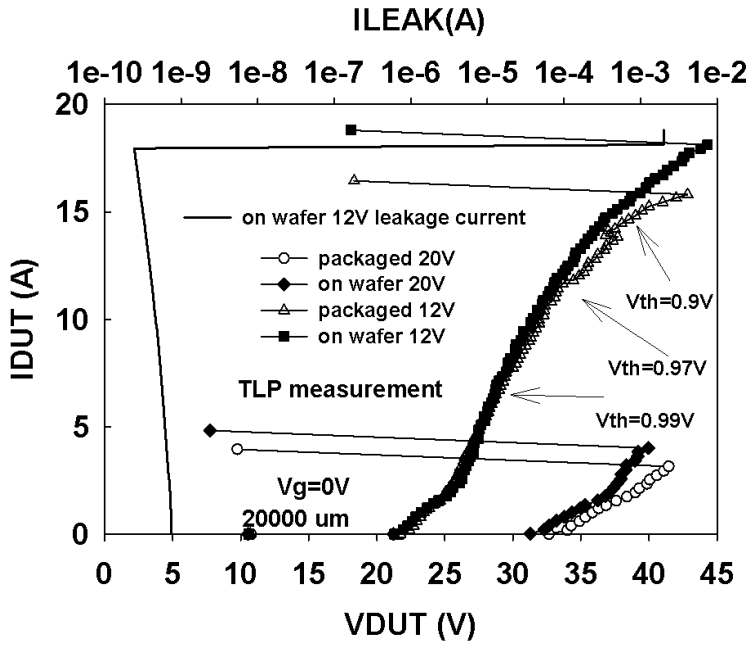

Figure 4.28: On-wafer and packaged measurements for 20 and 12V devices under 10ns rise time and 100ns pulse width for Vgs=0V

NLDMOS structures with different layout options (finger width / number) were evaluated under TLP conditions, with 10ns rise time, 100ns pulse width until the point where one order of magnitude change in the leakage current is detected. At high currents, TLP failure levels for Vgs=5V and Vgs=0V are similar for each given width, indicating that the device failing condition was similar. Figure 4.29 and Figure 4.30 show the distribution and comparison of the maximum TLP current before failure (Imax) and corresponding maximum voltage before failure (Vmax) for different layout / NLDMOS device width options. In this

measurement, these are quasi-static values (averaged between 70 and 90 percent of the time scale) of the pulse.

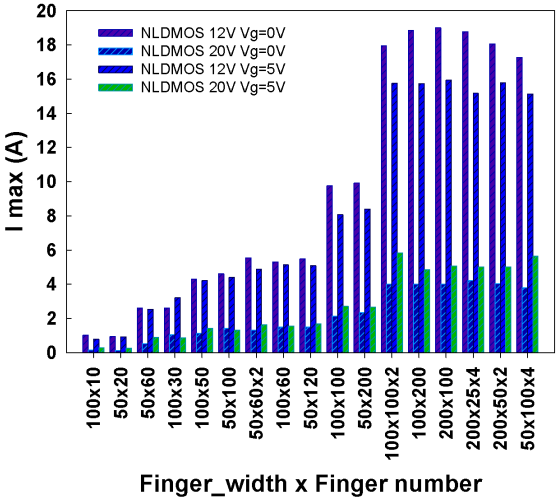

Figure 4.29: NLDMOS maximum TLP current before failure as a function of finger width and finger number

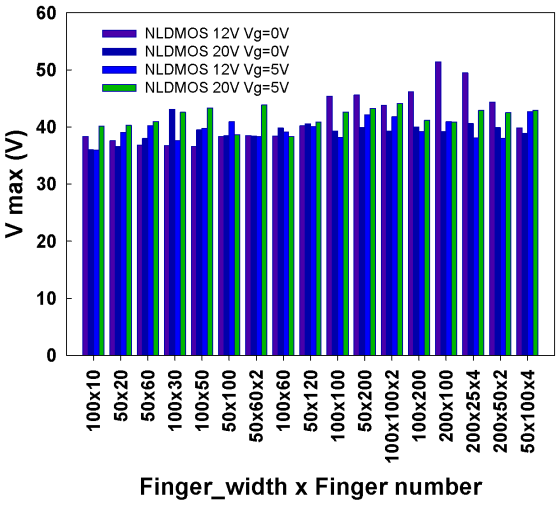

Figure 4.30: NLDMOS maximum TLP voltage before failure as a function of finger width and finger number

The voltage Vmax varies between 36 and 44V for all NLDMOS devices widths prior to the failure for the two Vgs bias conditions. The 12V version of the NLDMOS sustains a significantly higher Imax current and results indicate that it has a better conduction uniformity than the 20V device. The on-state failure level is similar to the off-state failure level for both, 20 and 12V NLDMOS. To better understand the difference in the 12 and 20V NLDMOS devices characteristics, i.e., maximum current to hard-failure, walk-out effect and Vth degradation, TCAD simulation was performed under TLP conditions at Vgs=0V and following the methodology discussed in Chapter 3. Figure 4.31 shows a zoom into the impact ionization profiles, which are linked as well to the carrier injection locations and temperature peaks [54].

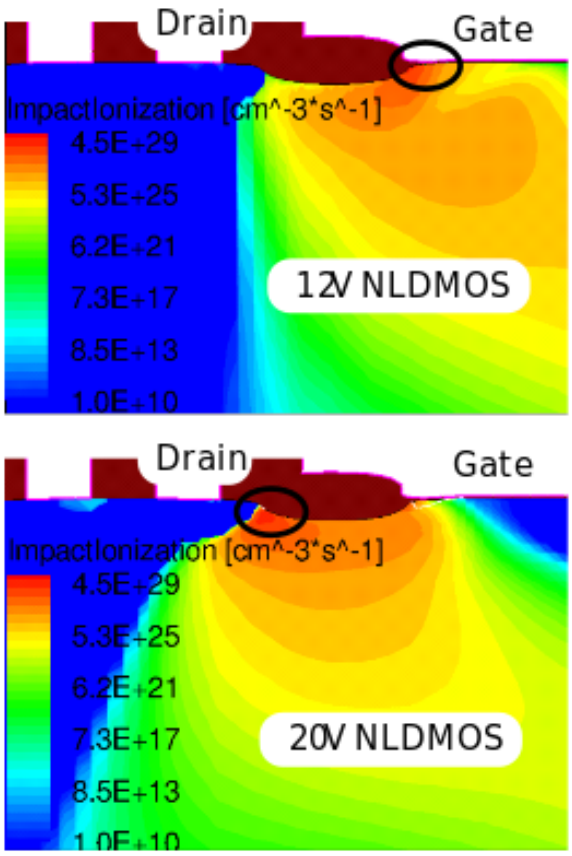

Figure 4.31: Difference in impact ionization for 12 and 20 V NLDMOS during the same TLP-like stress for Vgs=0V

For the 20V NLDMOS the highest impact ionization is located near the drain contact soon after the breakdown voltage level is reached, leading to hard failure at relatively low TLP current. In the case of the 12V NLDMOS, the additional Nwell implant in the drain enhances the TLP performance by sustaining more stress before reaching the hard failure condition at higher TLP current. The hard failure in the NLDMOS devices typically occurs after the hot-spot near the LOCOS moves toward the edge of the drain contact [54]. This

condition is reached in the 20V NLDMOS at relatively low current, close to the TLP stress condition used in the TCAD simulation, while the extra Nwell implant in the drain of the 12V NLDMOS changes the impact ionization profile during the stress condition, resulting in the initial shifting in the Vth, but higher current levels before reaching hard failure.

C. VFTLP Study for 200 μm to 20,000 μm NLDMOS devices

Figure 4.33 shows the voltage and the current parameters of interest versus the respective VFTLP- generated Vpulse stress level for a standard 20V GGNLDMOS. As the Vpulse increases, the transient voltage parameters decrease and the transient current parameters increase. It results in a drastic drop on the dynamic resistance of the device for larger Vpulse, critical for the assessment of the protection design.

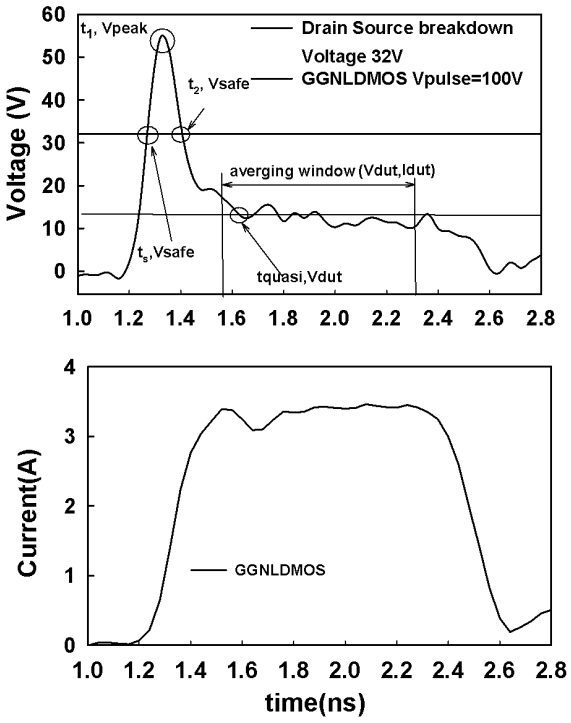

Figure 4.32: GGNLDMOS TSOA waveforms for 100ps rise time and 1ns pulse width

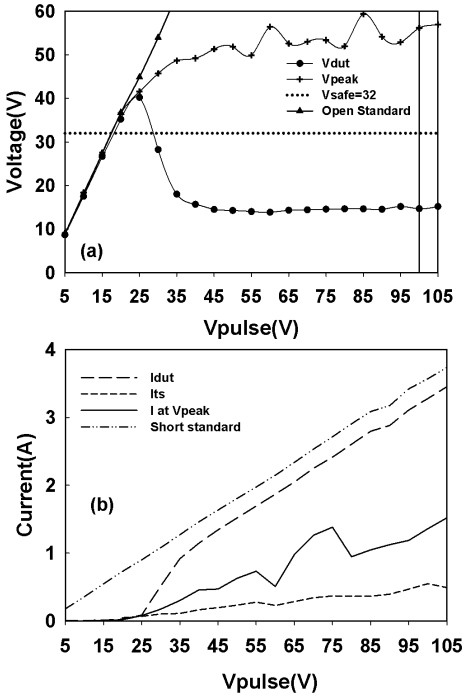

Figure 4.33: GGNLDMOS transient (a) voltage parameters, (b) current parameters for 100ps rise time and 1ns pulse width

Figures 4.33 a and 4.33 b also show the plot of voltage vs. Vpulse and current vs. Vpulse for reference open DUT and a short DUT, describing a very high resistance and very low resistance response, respectively. It is noted that the voltage in the NLDMOS device under test (Vdut) and the voltage in the open DUT are similar until the snapback of the NLDMOS occurs at Vpulse = 25V. After that pulse, the peak voltage (Vpeak) value settles close to 54V. The plot of the current vs. time in Fig. 4.33 b shows the current that flows through the device once it reaches Vsafe (Its), Vpeak (Ipeak) and Vdut (Idut).

Figure 4.34 shows the current and voltage waveforms corresponding to the TSOA pulses (pre-failure pulses) for standard 20V devices of 200 and 20,000 μm total device width. The devices VFTLP transient response was obtained for 100 ps rise time and 1, 2, 5 and 10 ns pulse widths. For 1 and 2 ns pulse widths, significantly more current can be handled through the devices before damage onset. For 5 and 10 ns, a relatively small increase in current and decrease in voltage was observed prior to damage for much lower VFTLP current levels. This current / voltage precursor was also observed for the 100 ns TLP stress. It was noted that no overshoot exists for 2, 5 and 10 ns stresses and that the voltage increases in time.

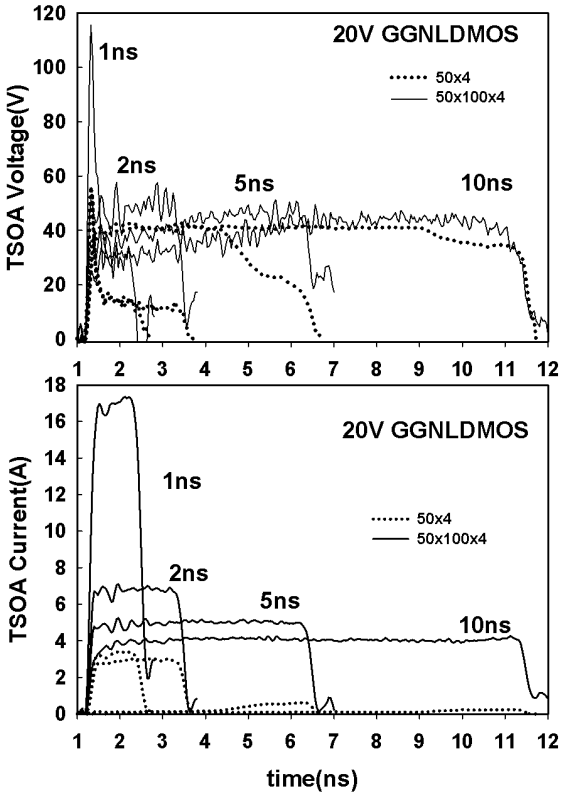

Figure 4.34: 20V GGNLDMOS transient voltage and transient current TSOA waveforms for 200 and 20,000 μm wide devices

The overshoot exists only for 1 ns stress due to the very high Vpulse applied. The TSOA current (ITSOA) levels are only 2.5 - 50 times higher for 1,000 times increase in area, indicating lack of conduction uniformity and proportional scaling of current with device width for the 20V device. In the 1,000 μm device, as in 20,000m device, the 1ns pulse width stress condition did not damage the structure up to the maximum VFTLP stress provided by the instrument. For the 12V devices, the failure current levels were higher, but the failure mode was the similar to the 20V device. Table 4.1 and Table 4.2 summarize the TSOA

maximum VFTLP Vpulse obtained before failure for the different pulse widths for (a) the 20V and (b) the 12V NLDMOS tested in Fig. 4.34.

Table 4.1: Maximum VFTLP V_{pulse} in the 20V NLDMOS for different pulse widths

Device	vfTLP TSOA V_{pulse} (V)			
20V NLDMOS (μm)	1ns	2ns	5ns	10ns
200	100	85	25	23
20,000	> 500	205	150	125

Table 4.2: Maximum VFTLP V_{pulse} in the 12V NLDMOS for different pulse widths

Device	vfTLP TSOA V_{pulse} (V)			
20V NLDMOS (μm)	1ns	2ns	5ns	10ns
200	120	120	29	26
20,000	> 500	> 500	> 500	> 500

For the larger devices a stronger gate coupling was obtained. It resulted in the initial overshoot to be clamped by the gate coupling at the beginning of the stress where the device operates in MOS conduction. Figure 4.35 shows the quasi-static I-V characteristics for the 20,000 μm 20V NLDMOS structure stressed by VFTLPs of 100 ps rise time and 1, 2, 5 and 10 ns as well as TLPs stresses of both, 0.2 and 10 ns rise times, and 100 ns pulse width. Notice that the TLP rise time did not affect the failure point significantly since the quasi-static measurement was taken significantly later in the pulse. Except for the 1ns response,

each response was plotted until the point the leakage current changed at least an order of magnitude. In the case of the 1 ns stress condition, this structure was not damaged. It snapped back and conducted up to the highest possible Vpulse of 500V and 18A instrument limit. It is noted that the TSOA conditions identified under 10ns stress were very similar to those under TLP stress for 20V NLDMOS device. The current and voltage TSOA levels for TLP stress were: ITSOA=3.8A and VTSOA=39V at Vpulse= 110V. For 10 ns stress, the TSOA levels were: ITSOA=3.64A, VTSOA=41.1V at Vpulse=115V. When using 400 ps rise time and 10 ns pulse width stress duration, the 20V NLDMOS TSOA maximum voltage Vpulse increased to 120 V, showing that the failure current and voltage were similar independent of the rise times. The voltage overshoot was lowered by the gate coupling initially, after which point the drain-source voltage increases up to nearly 40V damaging the device.

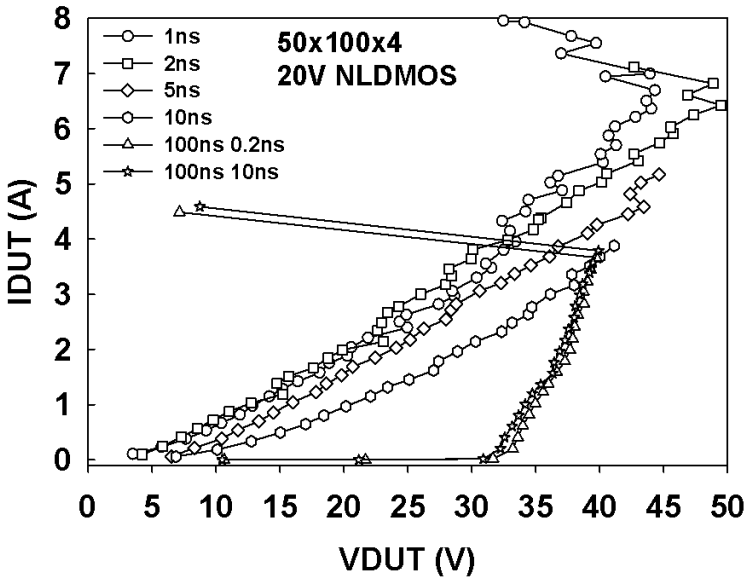

Figure 4.35: 20,000 μm width 20V GGNLDMOS quasi-static curves for VFTLP with 100 ps rise time/different pulse widths and TLP stress with 200 ps and 10 ns rise time and 100 ns pulse width

4.4 Clamp interaction with NLDMOS

For those cases in which the design of the NLDMOS output circuit stage does not allow it to be a TSOA self-protecting device, an additional protection device is incorporated in parallel with the NLDMOS to achieve the required robustness. In order to design this device accordingly, the TSOA parameters can be used. For a given NLDMOS TSOA, the clamp response measured under the same Vpulse should ideally have: a lower Vpeak overshoot as well as a smaller (or none) time above DC voltage given by (t2-ts).The current at the DC break-

down voltage for protection (Its) should be larger than the same current for the protected device (Its), which would guarantee that the dynamic resistances $Rts_{clamp} < Rts_{NLDMOS}$. This ensures that the clamp takes the majority of the current at the point where the NLDMOS starts conducting.

Figure 4.36 shows the voltage and current waveforms for two clamps, LHVC and HHVC 2, together with NLDMOS waveforms under the same Vpulse =100V (TSOA pulse for NLDMOS). The voltage waveform of the HHVC 2 has lower overshoot, less time above the 32V and the $Rts_{clamp} < Rts_{NLDMOS}$. This clamp is adequate for NLDMOS protection until the voltage in the device under test Vdut reaches a value above 32V. This result has been corroborated as well in different qualified and released integrated circuit products where this clamp is currently being used.

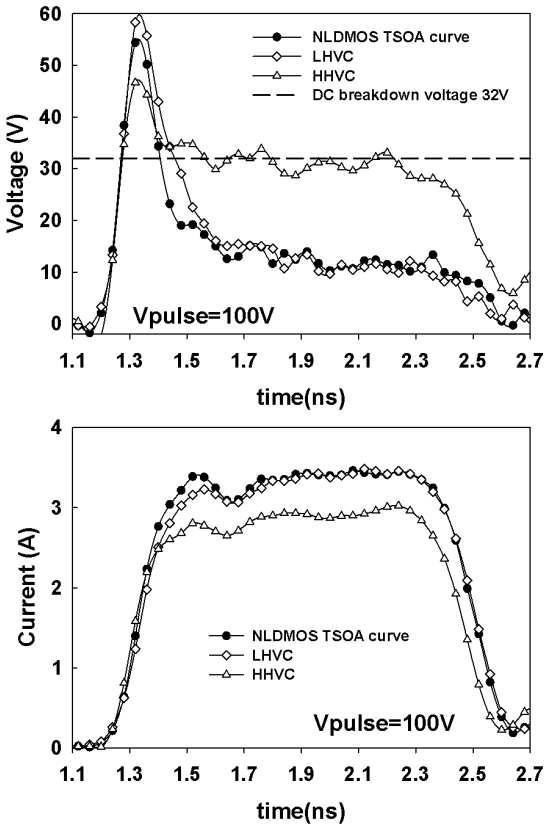

Figure 4.36: GGNLDMOS TSOA curves and corresponding curves for LHVC and HHVC 2

Figure 4.37 shows the parallel response of the HHVC 2 and the NLDMOS to Vpulse=105V and the Vpulse =170 V. Vpulse=105V was the last value that only the HHVC 2 conducts and Vpulse =170 V was the value where the parallel combination fails due to NLDMOS failure. For HHVC 2 to always conduct the majority of the current, the Vdut needs to stay below the 32V for any given Vpulse. It is difficult to achieve this $< 32V$ during the full dynamic response of the protection clamps, thus a failure was identified before reaching

the clamp failure current, which was beyond the maximum Vpulse that the VF-TLP can provide.

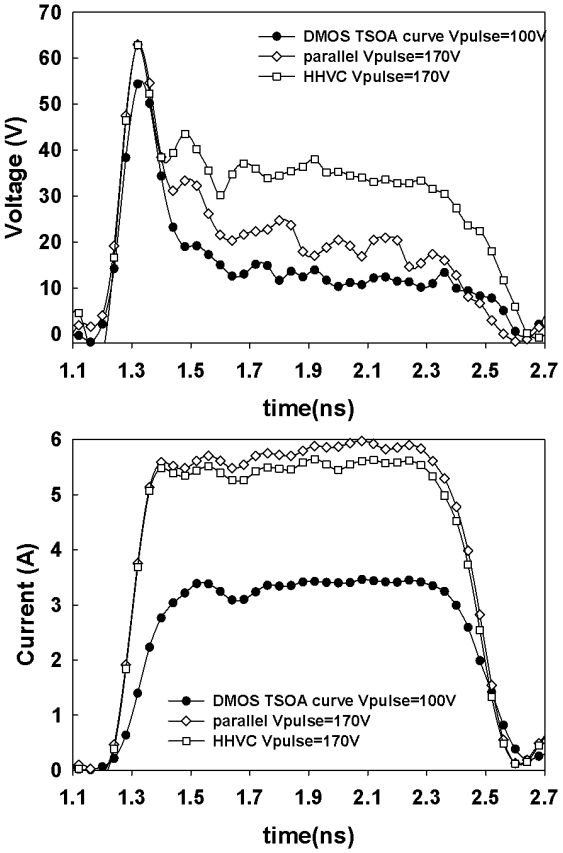

Figure 4.37: GGNLDMOS TSOA curve and parallel combinations with HHVC 2 clamp

For the LHVC, the voltage response was similar to the NLDMOS response, except that the voltage overshoot of the LHVC above 32V was larger than the NLDMOS and more time is needed for this device to clamp the voltage below the said NLDMOS DC breakdown voltage level. This limited this clamp to conduct only part of the current in parallel with the NLDMOS, which resulted in a competitive triggering between the two devices. Consequently,

the LHVC was able to protect the NLDMOS only as long as the current conduction through the NLDMOS remained below the TSOA current level.

To investigate further the interaction of the clamp and NLDMOS devices during the dynamic response, Figure 4.38 shows the TCAD simulated voltage and current response of a 200 μm NLDMOS in parallel with LHVC for a Vpulse=100V and two rise times, 100 and 400 ps. According with the plot of the source current (indicating NLDMOS conduction), the clamp was able to respond fast enough to take over the majority of the current under the slower rise time, e.g., 400 ps. For the fastest rise time, at about 100 ps, the clamp did not respond as fast as the NLDMOS and it was not as effective in protecting the NLDMOS. Even though it can be considered an extreme case in the sense that most of the effective ESD events, e.g., typical CDM-, HBM- and HMM- rise times, that are going to be obtained on-die are closer to or slower than 400ps, it is important to evaluate (via the TSOA definition) the boundary conditions that limits the effectiveness of a protection clamp design and verify that those conditions are outside the area of interest for effective protection.

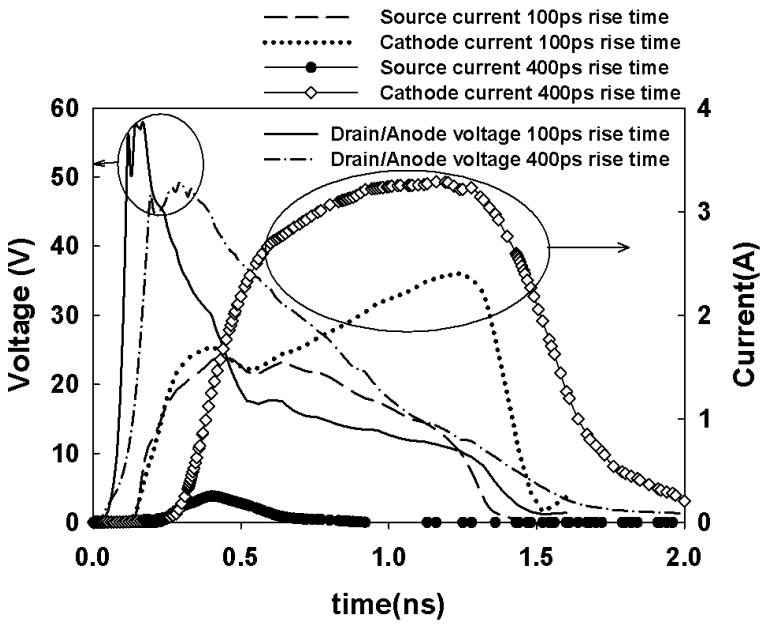

Figure 4.38: TCAD simulated GGNLDMOS and LHVC in parallel under 1 ns stress with 100- and 400-ps rise time for Vpulse=100V

The pulse rise time is one of the variables that change the complex device interaction. Device interaction can also be affected by intrinsic parasitic inductance coming from the leads and the package itself, plus the inductance related to the source providing the actual ESD stress. The higher the parasitic inductance, the larger the expected parallel pass level using LHVC, since the higher inductance tends to increase the overshoot of the stress and to slow down the rise time.

4.5 Chapter Remarks

Transient safe operating area (TSOA), or the point prior to failure, for NLDMOS and PLDMOS subject to transient stresses was analyzed and studied. Pulses with different durations and rise times generated from the transmission pulsing line (TLP) and very-fast TLP (VFTLP) testers were used to stress the devices under study. Technology computer-aided design (TCAD) simulations were also carried out to provide useful physical insights into the transient behavior of the devices operating at both the triggering and TSOA points. The study suggested that the PLDMOS can sustain a higher power than the NLDMOS before they are damaged by the transient stresses. In addition, it was found that both NLDMOS and PLDMOS would fail at a smaller power dissipation when they are stressed with pulses having a longer duration.

Transient Safe Operating Area (TSOA) analysis was practiced on core devices and used to evaluate synthesized output/input ESD robustness. In the case of output pins, the TSOA assessment allows for an optimized ESD solution to maximize performance of either self-protected devices or small output devices along with the protection clamp.

CHAPTER 5
HMM TLP RELATION

Laterally Diffused MOS (LDMOS) device is a key component in todays advanced mixed-signal high voltage applications [51], [50]. It is commonly used as a core device in the low side LDMOS switches in self-protecting scheme with low voltage gate bias, or as a non-self protected structure with dedicated ESD clamp, in which case gate bias is desirable to be 0V (off-state condition). It is also used as a part of active clamps in which case the driver design should provide the on state gate bias.

One of the challenges in designing electrostatic discharge (ESD) protection scheme for LDMOS devices includes finger non-uniformity as the ESD robustness in off-state does not scale well with device width [119]. Secondly, gate-drain coupling [119], [91] due to which the gate voltage can be higher than the 5V can affect the oxide of the LDMOS. The gate-drain coupling during ESD stressing presents a challenge, as the gate bias is determined, not only by the internal drain-gate, gate- source and gate-body capacitances of the LDMOS, but also by the load provided by the gate driver circuit which can also lower the gate voltage below the desired level.

Aside from all of the above-mentioned, the system-level test standard defined by the IEC 61000-4-2 [40] is typically required to assess final application robustness. In some

applications, such as automotive system-level ESD protection solutions with or without any off-chip protection components can be required [14]. In other cases, communication lines are externally connected at the system level and thus directly exposed to system level stress [14], [42]. To this end, integrated circuits (ICs) need to be able to pass system level test. This system-level robustness when tested at the component-level is commonly being assessed nowadays using a new related standard practice emulating the system level IEC 61000-4-2 stress, Human Metal Model (HMM) [43].

Because of its simple setup and easy data interpretation, the transmission line pulsing (TLP) technique has been widely used to characterize ESD protection devices [14]. When using the TLP for predicting accurate ESD passing levels, however, it is necessary to correlate the TLP data with results measured from the ESD zapping tester. Thijs et al. linked the Human Body Model (HBM) and HMM pass levels using a correlation factor [120]. Studies to establish preliminary IEC/HMM vs. TLP relationship were reported in [42], [90], but an extensive correlation between the HMM and TLP is not yet available in the ESD community.

In this section,first the correlation results of 20, 40 and 60V standalone clamps are revised. A comprehensive study is performed with the goal to correlate the HMM passing voltage and the TLP failure current based on data obtained from a large number of different ESD clamps with different holding voltages and on-state resistances. It will be shown that the formula reported in [42, 90] is in fact a subset of the correlation developed in this work.

In the second part standalone LDMOS devices HMM TLP relationship is reviewed. Results are reported on the HMM and TLP performance of 20 and 40V NLDMOS devices.

The LDMOS devices are evaluated under different bias conditions: off-state (Vgs=0V), on-state (Vgs=5V), and in some cases with the gate floating (Vgf). The device robustness improvement with the the device width is also investigated.

5.1 Standalone Clamps

The devices considered were fabricated in 0.35 and 0.18 μm CDMOS and BiCMOS technologies, including SCRs, stacked SCRs, diodes, grounded-gate PMOSs, and stacked grounded-gate PMOSs. They can be categorized into high holding current clamps (HHCC), high holding voltage clamps (HHVC), and low holding voltage clamps (LHVC).

TLP measurements were obtained using the Barth model 4002 TLP tester generating pulses with a 100 ns width and 10 ns rise time. HMM measurements were performed using the Hanwa W5000M system for wafer-level HMM testing up to 8 kV. The onset of leakage current increasing by an order of magnitude was defined as the failure point during the TLP/HMM testing. Figure 5.1 shows the current and energy waveforms of an HHVC measured from the TLP at a pulsing voltage of 155 V (the highest pulsing voltage before the clamp failure) and HMM at a zapping voltage of 0.9 kV (the highest zapping voltage before the clamp failure). The HMM and TLP accumulative energies are very similar (16.4 and 15.8 J, respectively). The great majority of the HMM and TLP currents and energies reside in the time frames of 150 and 100 ns, respectively.

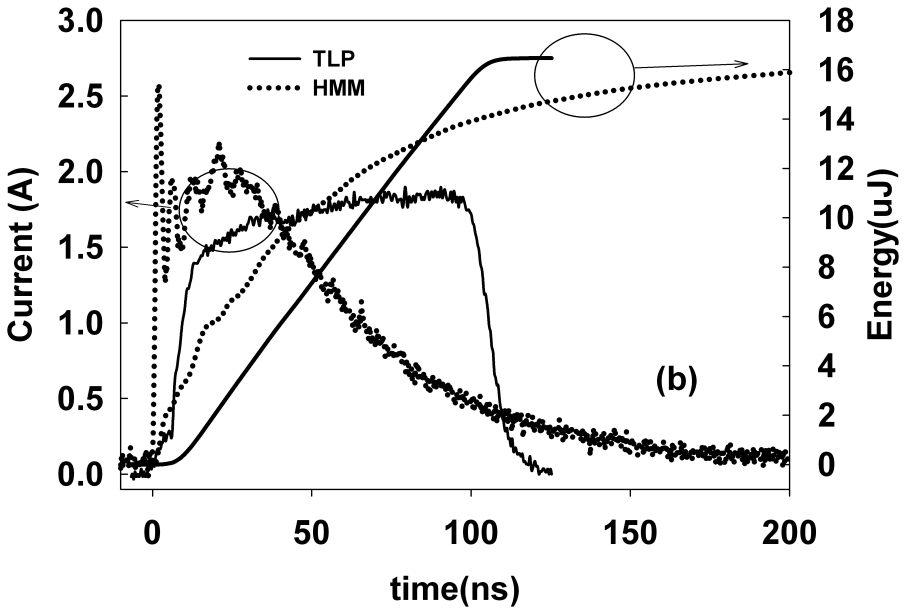

Figure 5.1: Sample TLP and HMM: Current waveforms of a high voltage clamp. Included is the energy over time for both stresses

The energy under any stress provided to the device is:

$$E = \int_0^\infty V(t)I(t)dt, \tag{5.1}$$

where V is the voltage and I is the current of the DUT. Voltage can be written as a sum of holding voltage and the on resistance term and these two terms respectively E_{Vh} and E_{Ron} represent the total energy given in 5.2.

$$
\begin{aligned}
E &= E_{Vh} + E_{Ron} \\
&= Vh \cdot \int_0^\infty I(t)dt, \\
&+ Ron \cdot \int_0^\infty I^2(t)dt
\end{aligned}
\tag{5.2}
$$

In the case of low holding voltage clamps $E_{Ron} >> E_{Vh}$, while the opposite is true for high holding voltage clamps.

As HMM and TLP stress are similar in duration we can use the same energy approach to correlate pass levels. We assume that the energy delivered to device under test (DUT) during HMM stress is similar to the energy delivered during TLP stress. Each stress type will have its own two terms given in the equation 5.2. The integral value for HMM stress is up to 150 ns, while for TLP it will be around 100 ns depending on the rise time used, but the majority of the energy content is within 100 ns.

To simplify the formulation of the current integrals in 5.2 , we assume that the DUT under the HMM stress reaches a full conducting state prior to failure. As such, an HMM current IHMM under the short condition was first measured, and its waveform exhibited a similar characteristic as the HMM current waveform shown in 5.1.

As the current integral showed linear behavior with respect to HMM stress value and the square showed quadratic behavior, they are described through least squares fitting in the following analytical equations:

$$\int_0^{150ns} I_{HMM}(t)dt = 1.77 \cdot 10^{-7} \cdot kV(HMM), \tag{5.3}$$

$$\int_0^{150ns} I^2_{HMM}(t)dt = 3.3 \cdot 10^{-7} \cdot kV(HMM)^2 - 4.2 \cdot 10^{-7} \cdot kV(HMM) + 6 \cdot 10^{-7}, \tag{5.4}$$

Figure 5.2 compares the values calculated from the integrals and from the empirical equations in (4) and (5) vs. HMM passing voltage. Good agreement between the two is demonstrated.

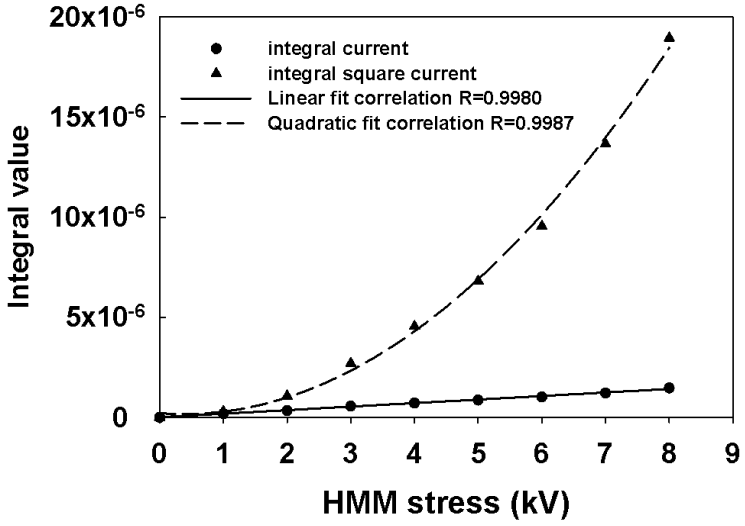

Figure 5.2: Values calculated from integrals (symbols) and calculated from the empirical expressions in 5.3 and 5.4 (lines) versus the HMM voltage using the fitting coefficients

Rewriting equation 5.2 to incorporate the information of the fitting of the integral value vs. the HMM level given by 5.3 and 5.4, we obtain:

$$
\begin{aligned}
E_{HMM} &= E_{Vh\_HMM} + E_{Ron\_HMM} \\
&= Vh \cdot (1.77 \cdot 10^{-7} \cdot kV(HMM)), \\
&+ Ron \cdot (3.3 \cdot 10^{-7} \cdot kV(HMM)^2 \\
&\quad -4.2 \cdot 10^{-7} \cdot kV(HMM) + 6 \cdot 10^{-7}).
\end{aligned} \tag{5.5}
$$

Following a similar approach, for the TLP testing we can also define a similar set of equations resulting in :

$$
\begin{aligned}
E_{TLP} &= E_{Vh\_TLP} + E_{Ron\_TLP} \\
&= Vh \cdot I_{TLP} \cdot 100ns \\
&+ R_{on} \cdot I_{TLP}^2 \cdot 100ns
\end{aligned} \tag{5.6}
$$

Equating the total energies in 5.5 and 5.6 and writing the kV(HMM) as a function of the quasistatic I_{TLP} current, we obtain the solution. Assuming a specific case for which the maximum I_{TLP} current to failure in a device is known and choosing a 10 percent margin (by multiplying the quadratic solution with 0.9) in the predicted kV (HMM) corresponding to this failure, the resulting prediction equation is:

$$kV(HMM) = 0.9 \cdot \frac{-b + \sqrt{b^2 - 4 \cdot a \cdot c}}{2 \cdot a}, \tag{5.7}$$

$$a = R_{on} \cdot 3.3 \cdot 10^{-7}, \tag{5.8}$$

$$b = V_h \cdot 1.77 \cdot 10^{-7} - R_{on} \cdot 4.2 \cdot 10^{-7}, \tag{5.9}$$

$$c = R_{on} \cdot 6 \cdot 10^{-7} - E_{TLP}, \tag{5.10}$$

The equation 5.7 was applied on 55 devices previously mentioned. Table 5.1 contains detailed subset information about the clamps.

Table 5.1: Detailed information on the subset of the evaluated clamps

device type	Vt(V)	Vh(V)	Ron (ohm)	Idut(A)	HMM pass (kV)
diode stack	1.6	1.4	1.2	11.2	6.8
plvtscr	11.4	2.4	1.3	9.4	5.9
lhvc	32	2.6	0.2	6.3	3.9
lhvc	17.6	4.3	4.2	5.8	3.6
pmos	7.1	7.1	1.8	4.6	2.8
pmos Stack	14.2	14.2	1.4	5.8	2.7
pmos lhv Stack	23.4	16.6	4	5.9	3.2
hhvc	27	20	1.3	9	5.2
hhcc	43	25	9.8	5.4	3.5
hhcc	46	28	6	5.7	3.4
hhcc	59	30	3.6	5.7	3.5
hhvc	49	45	3.6	3.6	2.4
hhvc	48	48	2.9	3.6	2.4
hhvc	48	54	2.6	3.8	2.2
hhvc	71	55	0.9	2.8	1
hhvc	65	60	0.5	2	0.9

Figure 5.3 shows that the relative errors of the prediction.

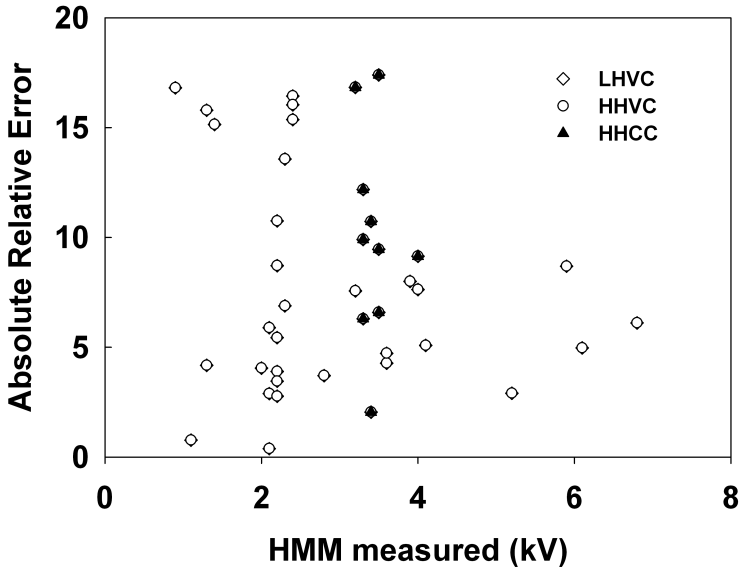

Figure 5.3: Relative errors of predicted HMM passing voltages

The lower and medium holding voltage clamps realized in 0.35 μm technology with holding voltages from 1.4 V to 20 V fit the whole range of kV levels. For those clamps the term E_{Ron} is the dominant one. Only for the PMOS stacks of 14 V and 16 V holding voltage and the clamp with 20V holding voltage the terms are similar in magnitude. Notice also that high holding voltage clamps (HHVC) fit the prediction with less variance then the high holding current clamps (HHVC). In case of HHVC the term E_{Vh} dominates, while for HHCC they are similar in contribution to the total energy and neither can be neglected. From the results in this study, for holding voltage of about 15V and higher both energy terms become equally important.

Previously in [42, 90] the ratio of HMM pass level and the TLP current of about 0.6 was observed. This ratio is not only the function of the the holding voltage, but also of the on resistance and that is why some clamps follow the 0.6 ratio approximation while others can go to 0.35 ratio for the higher holding voltage devices. The equivalent can be observed in the voltage ratio ($HMM(V)/V_{TLP\_PULSE}(V)$) shown in Figure 5.4 when the resistance decreases significantly which goes from about 24 to 12 as a function of increasing holding voltage.

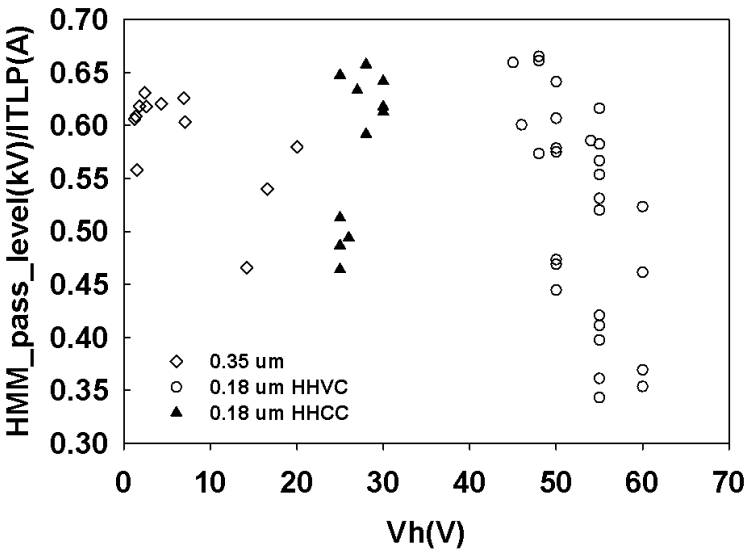

Figure 5.4: Ratio of the HMM pass level and TLP current

Figure 5.5 shows a figure of merit for ESD devices defined as the HMM pass level per area vs holding voltage. Figure 5.5 shows that the lower the holding voltage the higher the ratio. Notice that High Holding Current Clamps (HHCC) provide better high voltage protection options in terms of area then the high holding voltage clamps (HHVC). This is

on one hand due to the way they are implemented. Most of the HHVC are implemented as stacks of devices whose failure is limited by single device failure level. The HHCC can be implemented as a single device with layout and spacings modified for higher holding current. On the other hand, the HHCC require more current conduction compared to HHVC before they switch from low conduction to high conduction mode.

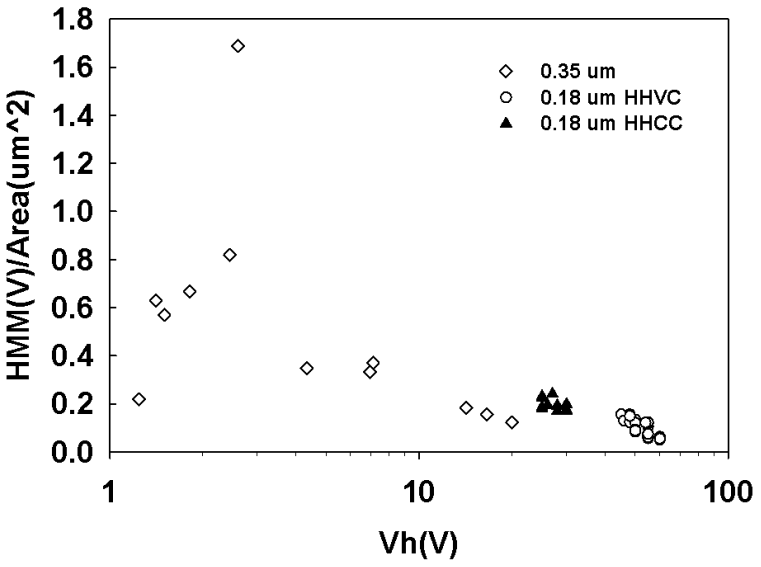

Figure 5.5: Ratio of the HMM pass level and device area

5.2 Standalone NLDMOS

For NLDMOS devices the TLP energy integral approach shown in previous section does not provide the prediction for HMM levels, as it greatly overestimates the HMM pass levels.

5.2.1 20V NLDMOS

From the discussion in chapter 4, a minor dependency of the 20V NLDMOS device TSOA with the rise time (in the range of 100 ps-10 ns) was observed.Also, 10 ns pulse width induced a failure at a Vpulse condition close to that obtained with a 100 ns pulse width at the same Vpulse. This implies that the failure condition is obtained within this initial time and that a Vpulse that causes failure in this device under a 10 ns pulse width would be similar to the Vpulse level that causes failure for wider pulses and within the 100 ns time frame. Assuming that the characteristic of the initial voltage overshoot does not damage the NLDMOS device, an HMM pass level can be initially extrapolated for this NLDMOS by considering that most of the energy of an HMM event is dissipated in the first 30 ns. This implies that the failure is driven by a specific current level.

By using the TSOA obtained from the Vpulse pass levels at 10 ns pulse width as a criterion, the HMM passing level can be identified for this device in both gate biased or gate-grounded conditions. The HMM current waveform into a short specification is: 1kV maximum peak current of about 3.75 A, 2 A at 30 ns and about 1A at 60 ns [43]. For example, for the 20 mm wide 20V NLDMOS, the 10 ns IDUT before failure is around 3.5 A, which would correspond to around 1.75 kV HMM. This is described in equation 5.11 where 90 percent margin is assumed.

$$V_{HMMPASS}(kV) = 0.9 \cdot (TSOA_{current}@10ns(A))/2 \tag{5.11}$$

Table 5.2 depicts the VFTLP maximum current and predicted HMM pass levels by using 5.11 in the case study NLDMOS devices.

Table 5.2: VFTLP predicted HMM pass levels for NLDMOS devices

NLDMOS width (mm)	20/ 12V 10ns VFTLP ITSOA (A)	20/12V HMM predicted pass level (kV)
1	0.2/1	0.1/0.5
3	0.6/3.2	0.3/1.6
5	0.9/5.5	0.45/2.75
20	3.5/11	1.75/5.5

Table 5.3 depicts the NLDMOS measured HMM pass levels in the off and on state using the TESEQ ESD gun. For 12V devices, the 10 ns VFTLP predictions were higher than the pass levels measured by the gun. For HMM gun robustness evaluation of 12V NLDMOS, the first change of threshold voltage greater than 5 percent of the original value was taken as fail criteria. For example, threshold voltage Vth of a 5 mm 12V device showed minor change after 0.6kV HMM stress. The unstressed device initial Vth=1.03V and after a tenth 0.6kV HMM pulse there was a change to Vth=1V. During the 0.7kV HMM zapping, Vth decreased with each zap until after the tenth 0.7kV HMM zap Vth=0.92V. Upon zapping 3 times with 0.8kV HMM, a hard failure was obtained. The pass level identified for this structure was therefore 0.6kV HMM. In cases where a higher Vth drift tolerance is allowed, 0.7kV HMM

can be used as the pass level. For 20V devices, on the other hand, leakage current was a better failure indicator as there was no Vth shift prior to hard failure.

Table 5.3: HMM pass levels for NLDMOS devices

NLDMOS width (mm)	20V HMM gun measured (kV) on state/off state	12V HMM gun measured (kV) on state/off state
1	$< 0.2/< 0.2$	$< 0.2/< 0.2$
3	0.3/0.3	0.5/0.6
5	0.4/0.3	0.4/0.6
20	1.7/1.5	2.3/3

The 3 and 20 mm structures were also measured on-wafer and the results for the 20V NLDMOS are shown in Table 5.4.

Table 5.4: HMM pass levels on-wafer vs. packaged for 20V NLDMOS devices

NLDMOS width (mm)	HMM gun test (kV) on- /off- state	HMM on- wafer test (kV) on /off state	10 ns VFTLP prediction (kV)
3	0.3/0.3	0.4/0.3	0.3
20	1.7/1.5	1.6/1.4	1.75

In the case of 12V NLDMOS, the on-wafer and packaged HMM the failure condition was monitored differently, as the on-wafer measurements monitored the hard-failure only and the packaged testing the Vth shift. Table 6 compares the HMM pass levels on-wafer vs. packaged. The on-wafer measurements closely match the prediction based on 10 ns on-wafer VFTLP measurements. It was noted as well that multiple zaps and the starting zap level can affect the 12V device TSOA. The results in Table 5.5 are reported for 1 zap per level starting at 2kV. For 20V device, the number of zaps did not show an appreciable effect in the pass levels.

Table 5.5: HMM pass levels on-wafer vs. packaged for 12V NLDMOS devices

NLDMOS width (mm)	HMM gun test (kV) on /off state	HMM on- wafer test (kV) on /off state	10 ns VFTLP prediction (kV)
3	0.5/0.6	1.5/1.4	1.6
2	2.3/3	5.4/5.4	5.5

The convenient usage of 10ns VFTLP to identify/extrapolate the failure condition and the TSOA levels of the device for HMM pass-level is based on the assumption that the initial overshoot does not damage the device. Figure 5.6 shows the on-wafer HMM TSOA maximum transient voltage and current response versus time for 20 mm 20V NLDMOS for gate bias of Vgs=0V. It also includes the voltage and current for the same stress for gate-biased (Vgs=5V). The initial overshoot is identified to be at about 150V for a 3.5A of

current. Even though the overshoot is relatively large in voltage, it is for a relatively short time to cause appreciable damage.

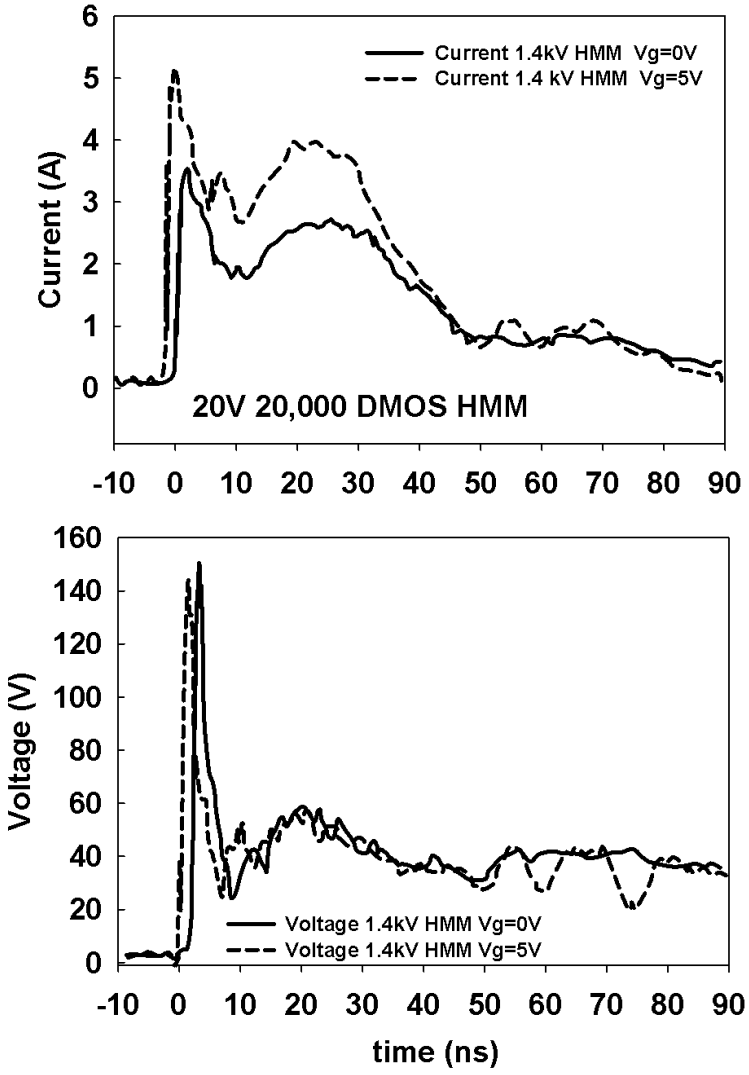

Figure 5.6: On-wafer 1.4kV HMM waveforms measurement when applied to a 20 mm 20V NLDMOS at Vgs=0V and Vgs=5

The voltage immediately dropped and started increasing back above the 40V voltage level in which region the device is close to getting damaged. As the largest portion of energy is delivered in the first 30 ns, 10 ns VFTLP pass levels were extrapolated to 30 ns 2A stress condition. Notice that Vgs=5V shows more current for the same stress condition coming from the NLDMOS channel conduction current, but the voltage is essentially the same with slightly less overshoot.

A set of simulations for 0.2 mm device under HMM stress with gate biased was performed with a simulator DECIMM [121].Prior to that the calibration parameters obtained in Chapter 3 were adjusted and the same calibration procedure was followed. The HMM circuit model is a two stage network as described in [8]. In Figure 5.7 simulated voltage and current waveforms are shown for the gate conditions of 0, 3 and 5V under 100V HMM stress.As the gate bias is applied with the ideal voltage source the gate bias condition is kept constant. The higher voltage drop and increased current conduction can be observed for gate biased conditions due to channel current conduction.

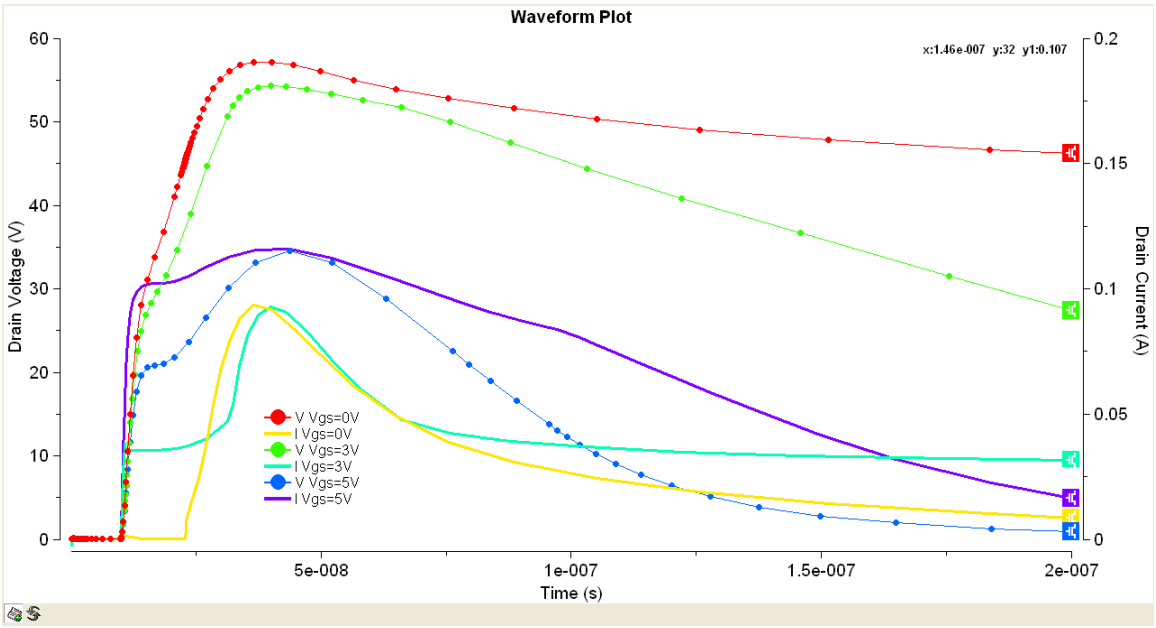

Figure 5.7: Voltage and current waveforms for 0.2 mm structure under different gate bias (Vgs) and 100V HMM stress

During the ESD stress the gate may be grounded, therefore the impact of the resistance between the gate and source (Rgs) is studied under the same 100V HMM stress. In Figure 5.8, the drain and gate voltage and drain current for Rgs values of 0.1Kohm, 1Kohm and 10Kohm are shown. The higher the value of Rgs the higher the gate voltage is during the initial nanoseconds of the HMM stress because the higher voltage is induced at the gate for the same current. In Figure 5.9 zoom into the gate voltage is shown. For Rgs=10Kohm the gate voltage reaches almost 3V.

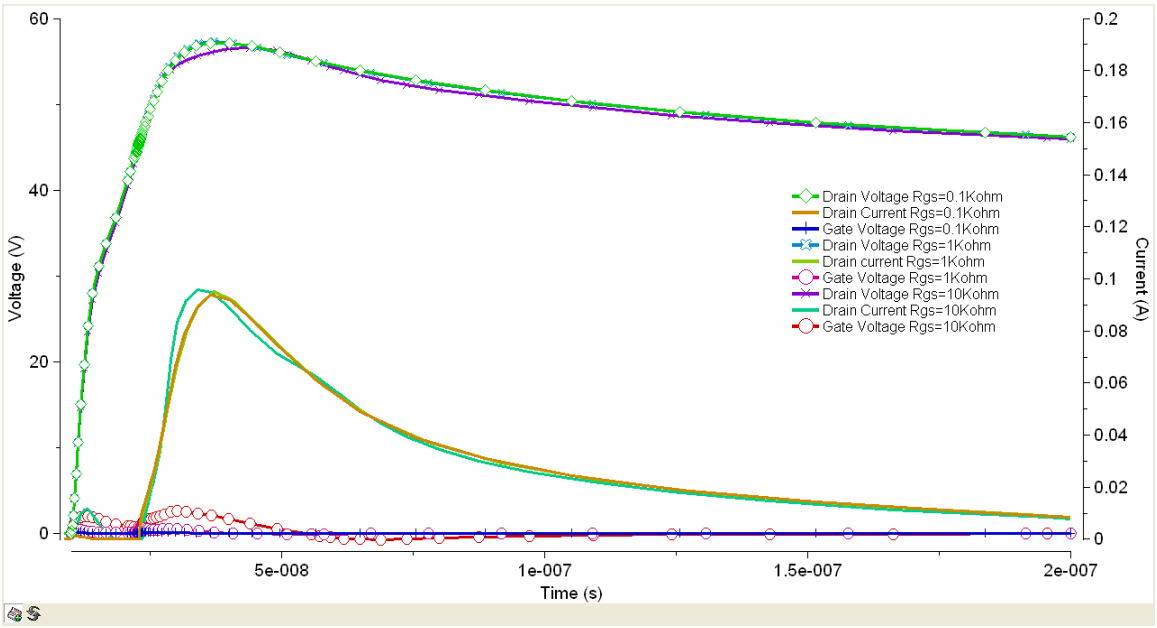

Figure 5.8: Voltage and current waveforms under 100V HMM stress for 0.2 mm structure with different gate to source resistance

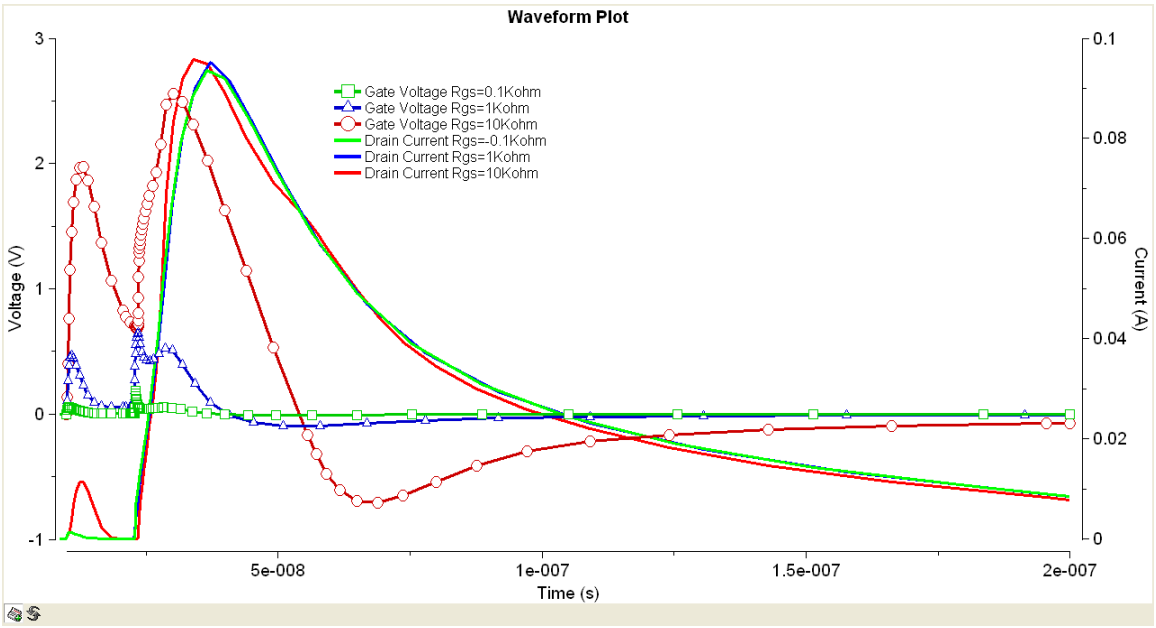

Figure 5.9: Zoom into the gate voltage and current waveforms under 100V HMM stress for 0.2 mm structure with different gate to source resistance

In some applications, the output pins allow for use of the capacitor at the output [122] and this scheme can be used without the protection element if the value of the capacitor is adequate. Different values of the capacitor were simulated placed at the drain of the 0.2 mm NLDMOS to evaluate which one will have the main current path through the capacitor instead of the drain of the NLDMOS. In Figure 5.10 the voltage and current waveform values at the drain for 1pF and 1nF are shown. For 1nF capacitor value the current conduction is mainly through the capacitor and the voltage seen by the drain of the LDMOS is about 10V. On the other hand, the configuration with a 1pF capacitor will still have a very high voltage of about 60V while the main current path is through the LDMOS.

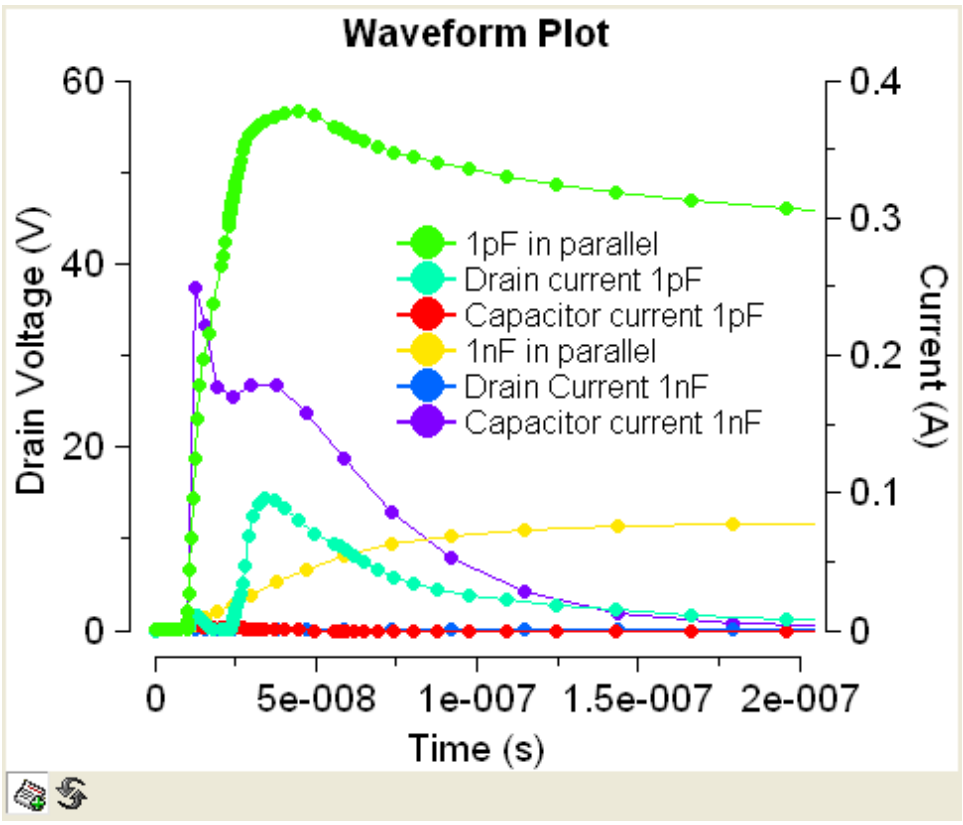

Figure 5.10: Voltage and current waveforms under 100V HMM stress for 0.2 mm structure with different capacitor values at the drain

5.2.2 40V NLDMOS

The reference devices considered in this study are fabricated in 40V 0.18-micron BCD technology with a breakdown voltage ranging from 54 to 56 V and the widths of 0.2 mm (4 stripes of 50 μm each, 4x50 μm), 0.4 mm (4x100 μm), 2 mm (20x100 μm), 3.75 mm (20x187.5 μm), and 15 mm (4x3.75 mm). All devices have butted drain and source.

Figure 5.11 shows the cross section of the devices studied. Equivalent schematic of parasitic devices and the main current conduction paths are also annotated in the cross-section. The current conduction paths take place at different DC breakdown voltages (DC BV) prior to snapback: Drain (NWELL) to Body/Bulk implant on the source side (DC BD of 54 V, Collector Base junction of the NPN), the NWELL to PWELL (DC BV of 58V, D1), NWELL to bulk contact (DC BV of 62 V, D2). Additionally, the current path in the channel (dashed lines) is formed by the gate-drain coupling and/or when a gate bias is applied. Finally, the parasitic NPN bipolar transistor (N+ source/P body/N+ drain) is responsible for creating the snapback condition.

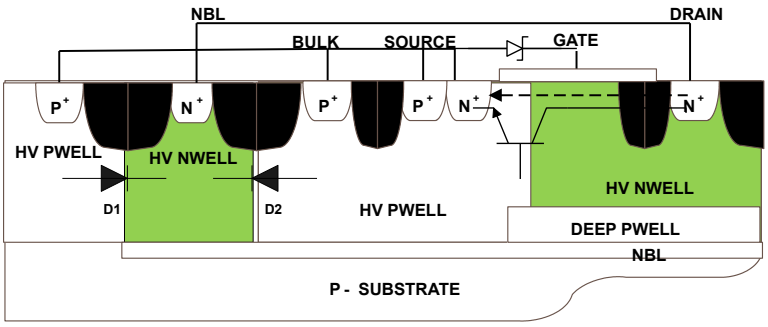

Figure 5.11: Annotated NLDMOS device cross-section showing parasitic components D1, D2 and NPN.

Pulsed testing with both 10 and 100 ns widths and a 0.2 ns rise time was performed using the Barth transmission line pulsing tester. For the HMM testing, the Hanwa HED W-5000M- SP0 manual wafer ESD tester was used. The relatively small LDMOS devices (0.2, 0.4, and 2 mm) ESD robustness was first measured for different widths and gate biasing

states. Figure 5.12 shows the TLP I-V characteristics for devices with: 1) different widths and 2) different bias: off, on, and floating-state gate conditions. They are tested up to the highest voltage and current the devices can sustain prior to failure.

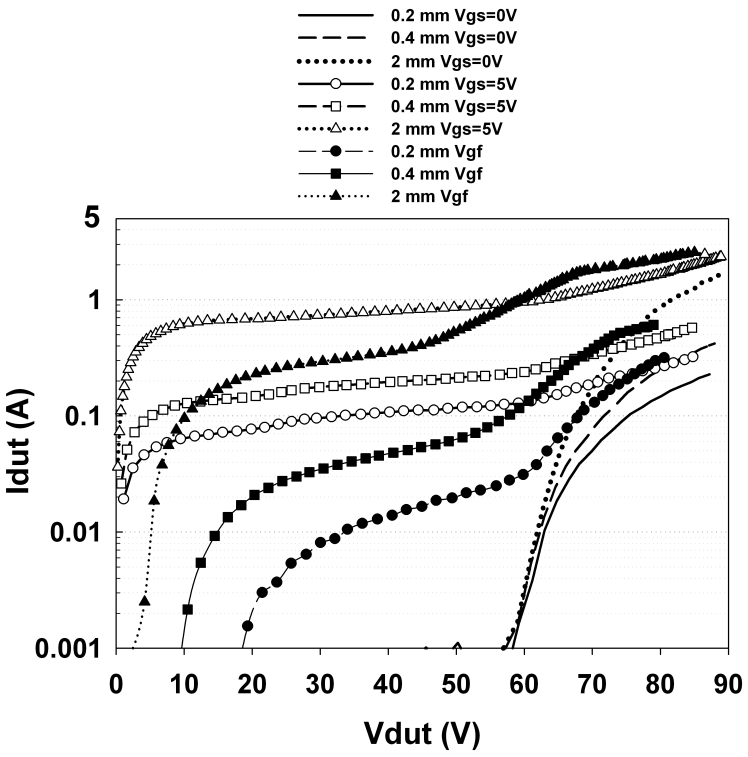

Figure 5.12: 100 ns pulsed stress results on log scale in: on (Vgs=5V), off (Vgs=0V) and gate floating (Vgf) state for 0.2, 0.4 and 2 mm wide devices with zener at the gate

Relatively large LDMOS devices (3.75 and 15 mm) were also tested under TLP conditions. Figure 5.13 shows their I-V characteristics. The largest device from the previous group, the 2 mm one, is added for comparison.

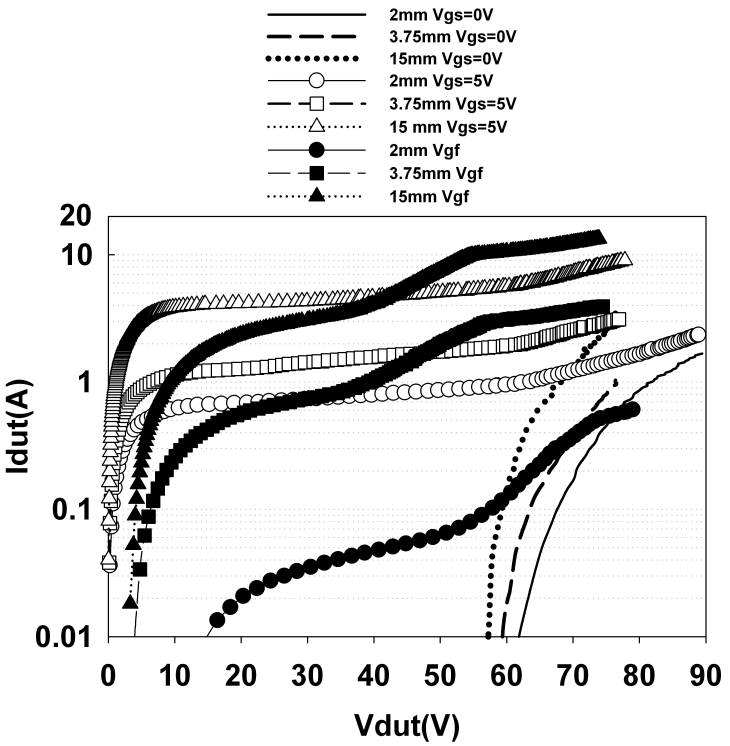

Figure 5.13: 100 ns pulsed stress results on log scale in: on (Vgs=5V), off (Vgs=0V) and gate floating (Vgf) state for 2, 3.75 and 15 mm wide devices with zener at the gate

The average critical voltage prior to failure when snapback is observed is about 85 V. The devices show initial current conduction under gate grounded condition around the drain-source DC breakdown voltage. Prior to snapback, at a voltage around 60 V, the slopes of the I-V curves change, showing an increasing current conduction formed by other parasitic paths in the device and impact ionization due to high drain voltage. For the testing with the gate floating, the gate voltage increases with increasing TLP stress, but for the highest voltage the gate coupling is limited by the zener voltage which implies that the current is

generated by impact ionization rather than through gate coupling. For 10 ns stress the currents are about 15 % higher.

Structures without the zener at the gate were biased at greater than 5V gate bias to achieve the same current conduction level above 60V as the ones with the zener in gate floating condition. The results are shown in Figure 5.14. For 3.75 mm structure this requires Vgs=7V at the gate, while 15 mm structure requires Vgs=8V at the gate equivalent. Observe that for higher gate voltage condition the additional current generation starts earlier around 25V.

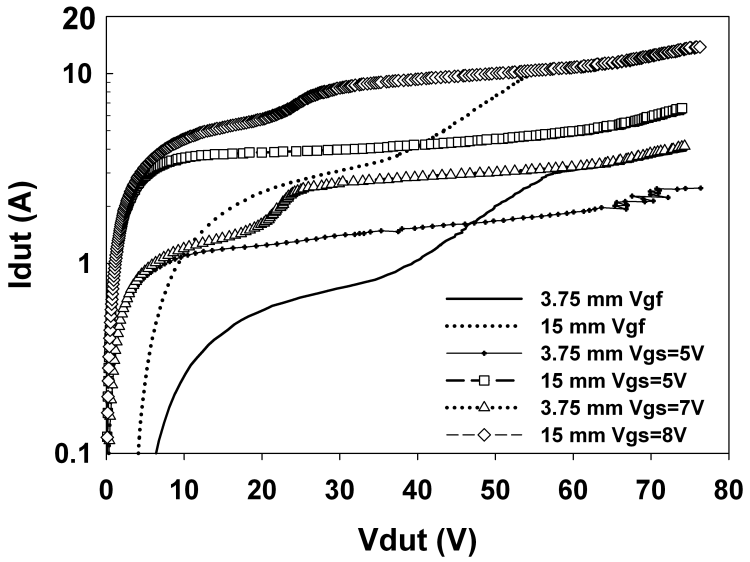

Figure 5.14: 100 ns pulsed stress results on log scale for 3.75 and 15 mm with the zener at the gate with Vgs=5 and gate floating and without zener 3.75 (Vgs=7V) and 15 mm (Vgs=8V)

The HMM pass voltage levels are defined as the highest level the devices can pass. The change in the leakage under both TLP and HMM stress is typically coupled with the snapback (drastic voltage drop) and current increase. HMM pre fail and fail waveforms are shown in Figure 5.15 for the 0.2 mm NLDMOS structure with Vgs=0V, where the structures failed as a short after snapback.

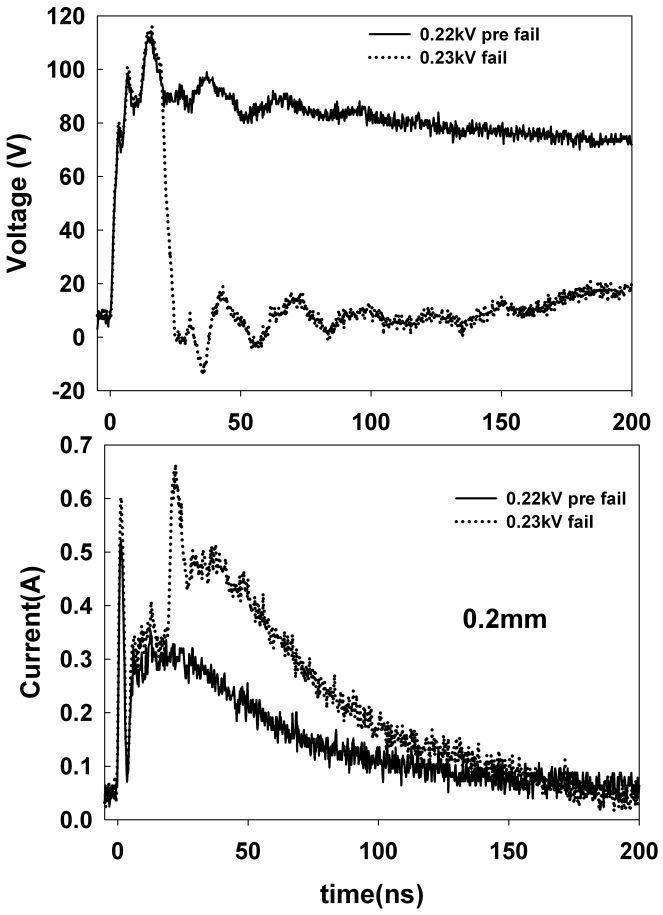

Figure 5.15: HMM pre fail and failure waveforms for 0.2 mm structure in off state Vgs=0V.

To investigate the gate bias effect during HMM, the transient responses of the 0.2 mm LDMOS under different gate voltage conditions and HMM voltage of 40 (operating voltage) and 90 V (around TLP snapback voltage) is shown in Figure 5.16 and Figure 5.17 respectively. The current levels for the cases of small gate voltages (less than 2 V) and gate floating are relatively small, hence the higher voltages observed. This indicates that there is no strong gate coupling effect and the current conduction via the channel is negligible in these gate bias conditions. As the gate voltage increases, the peak drain-source voltage is clamped to a lower voltage and the conduction current is consequently higher.

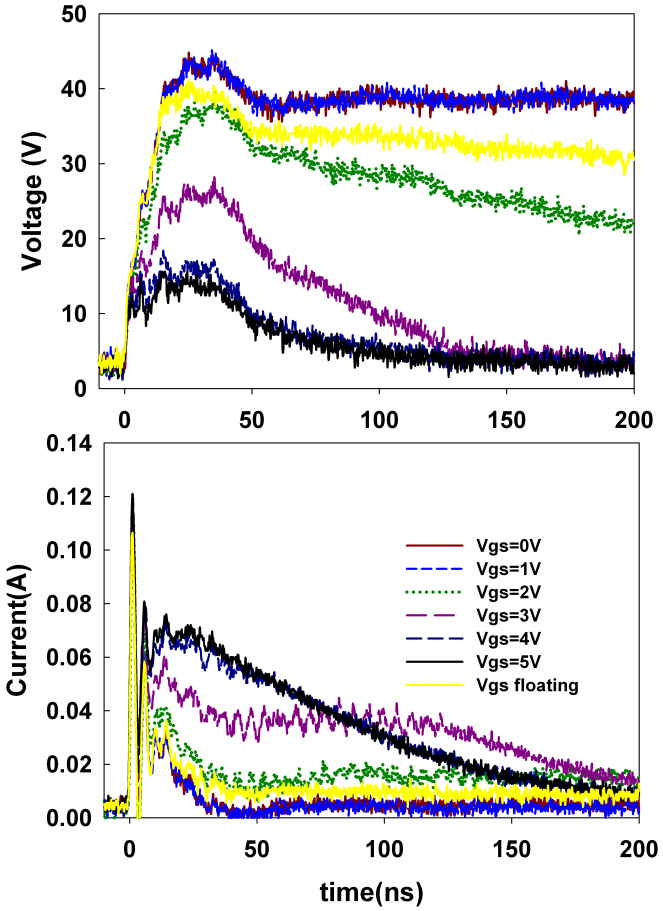

Figure 5.16: 40V HMM waveforms for 0.2 mm device under different gate voltage conditions.

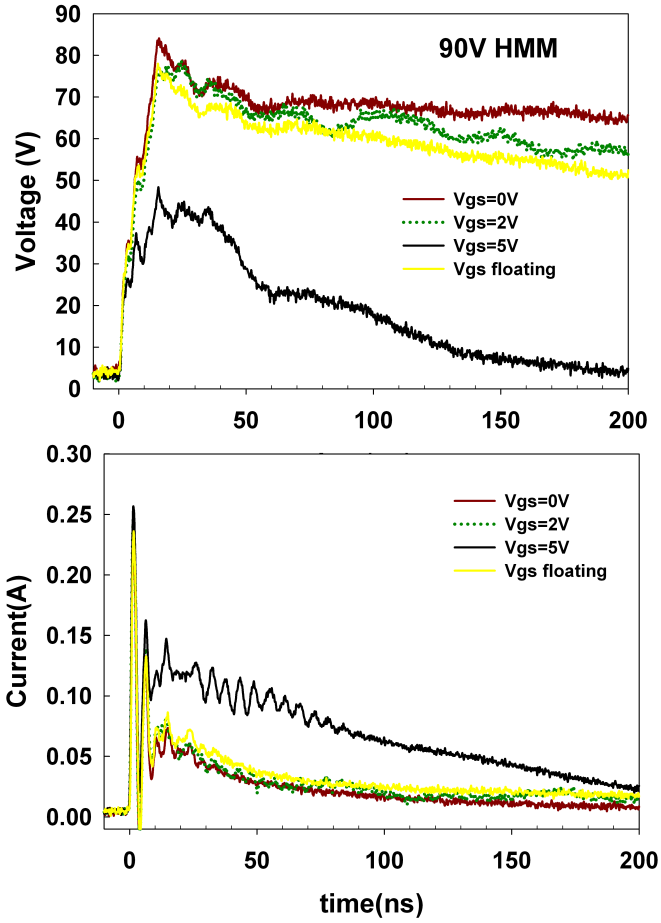

Figure 5.17: 90V HMM waveforms for 0.2 mm device under different gate voltage conditions.

To understand in more detail the effect of gate biasing on the NLDMOS performance under the HMM stress, transient voltage waveforms for the 2 mm NLDMOS subject to the mid range of 0.5 kV of the passing voltage (0.9 kV) for different gate bias conditions are shown in Figure 5.18.

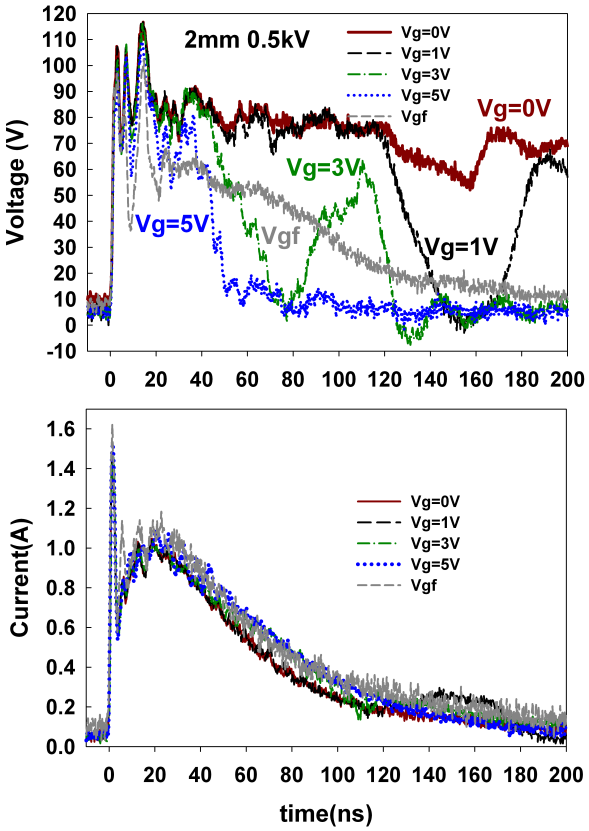

Figure 5.18: 0.5kV HMM waveforms for 0.2 mm structure with Vgs=0, Vgs=3, Vgf and Vgs=5V.

When the NLDMOS gate is in off state, after the initial overshoot the voltage behavior is similar to TLP stressing, and shows a flat voltage of about 85V after the first 20 ns. When the NLDMOS gate is biased, the HMM conduction depends on the stress levels. For lower level HMM stress the current conduction is mostly through channel conduction. For higher HMM stress of 0.9kV shown on Figure 5.19 the first portion of the transient voltage waveform shows a lower voltage due to the channel conduction, parasitic paths conduction and impact

ionization generated current. The second part of the voltage waveform around 60 ns shows an increase in the voltage, implying that the device is conducting mainly channel current. For even higher HMM stress, the NPN creates snapback condition.

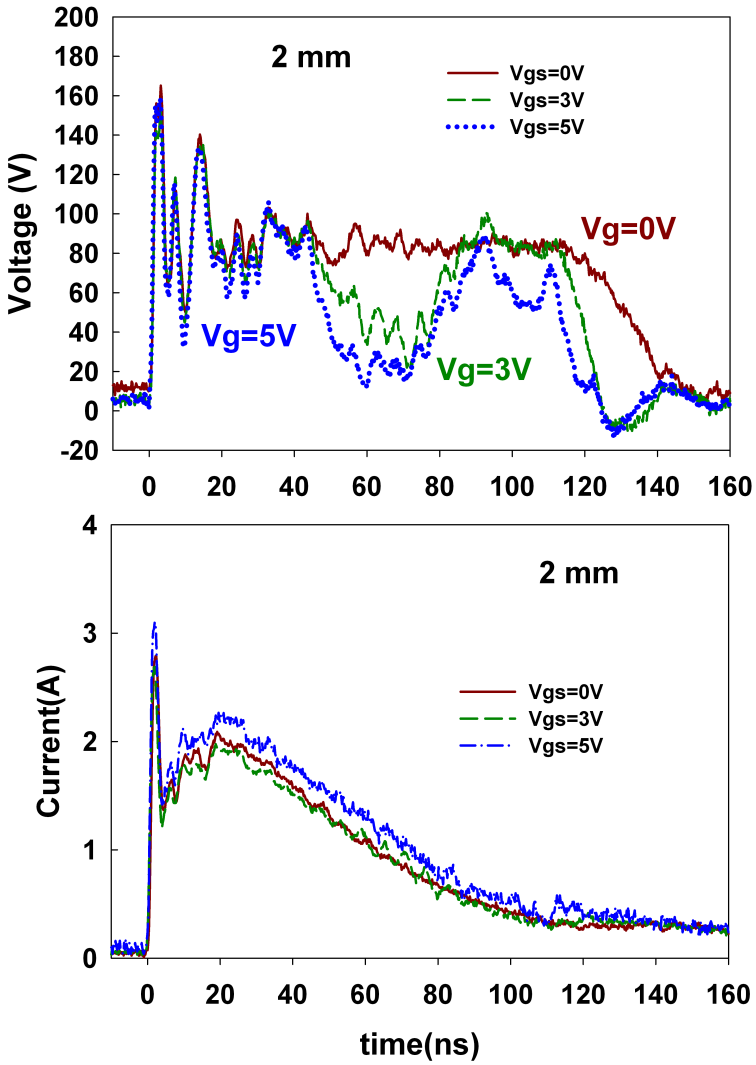

Figure 5.19: Waveforms for 2 mm device under pre failure HMM voltage of 0.9kV and gate voltages of Vgs=0 and Vgs=5 V

Previously, from Figure 5.14 we observed that the higher the gate voltage, the larger the conducting current. Thus, a larger gate voltage should result in a more robust LDMOS. The impact on HMM pass level, however, is not significant: the HMM level for 3.75 mm with Vgs =7 V is 1.3 kV, while for Vgs=5 V it is 1.2 kV and 0.9kV for Vgs=0V. For the largest LDMOS structure of 15 mm under study, it passes 1.4 kV for Vgs= 0, 2.5 kV for Vgs=5 V, and only 2.4 kV for Vgs=8 V which is within the testing step size. The tests for Vgs greater than 5V were performed on structures without the zener at the gate. This implies that the failure is based on the avalanche current generated, rather then the pure saturation current for a given gate voltage.

The pre-failure current levels (in A/mm) for all the NLDMOS devices and their corresponding HMM pass levels (in kV/mm) are listed in Table 5.6. It suggests that there is an important limitation on the capability of these NLDMOS devices to be self-protected during the IEC-61000-4-2 ESD stress conditions, regardless the NLDMOS device width.

Table 5.6: Summary of TLP Pre-Failure Current Levels and HMM Pass Levels for NLDMOS Devices With Different Widths.

Width (mm)	Gate bias (Vgs(V))	Idut(A)/mm	HMM pass level (kV)	HMM(kV)/mm
0.2	0	1.15	0.22	1.10
	5	1.6	0.25	1.25
	floating	1.7	0.29	1.45
0.4	0	1.05	0.31	0.78
	5	1.43	0.36	0.90
	floating	1.53	0.45	1.13
2	0	0.84	0.9	0.45
	5	1.23	1	0.50
	floating	1.28	1.6	0.80
3.75	0	0.27	1	0.27
	5	0.83	1.2	0.32
	floating	1.04	1.6	0.43
15	0	0.23	1.4	0.09
	5	0.6	2	0.13
	floating	0.89	2.5	0.17

Referring to the TLP performance summarized in Table 5.6, an NLDMOS device with a relatively small width under gate biased or floating condition provides the highest failure current per mm of width when subjected to pulsed stresses. The small width devices conduct more uniformly before failure, while the larger width devices do not [90].

Figure 5.20 shows the normalized TLP current prior to failure (normalized to the smallest 0.2 mm structure) and normalized HMM pass voltage levels (normalized to 0.2 mm pass level) for different device widths as a function of the gate bias conditions. The TLP passing levels increase linearly with the device total width. These passing levels are also gate bias dependent; gate grounded condition is the least robust, while gate floating is the most robust. The HMM pass levels, however, do not follow the same trends. The most outstanding case is that of a 75 times wider structure having an HMM pass level only 6.3 times higher for Vgs=0 and 8 times for Vgs=5V. For this same device, the TLP shows corresponding scaling substantially higher at 15 times for Vgs=0 and 28 times for Vgs=5 V. This shows in relative terms the limitation of very large output drivers to be self-protected under HMM stress conditions. It also shows that TLP characterization can be misleading if used as a criterion for designing an HMM self-protected LDMOS output stage. From these results we can conclude that the current non uniformity is more severe for HMM type of stress. Additionally, unlike the 20V device, for 40V device no correlation factor was found between pulsed stress and HMM pass levels due to the very high current non uniformity under HMM for 40V device.

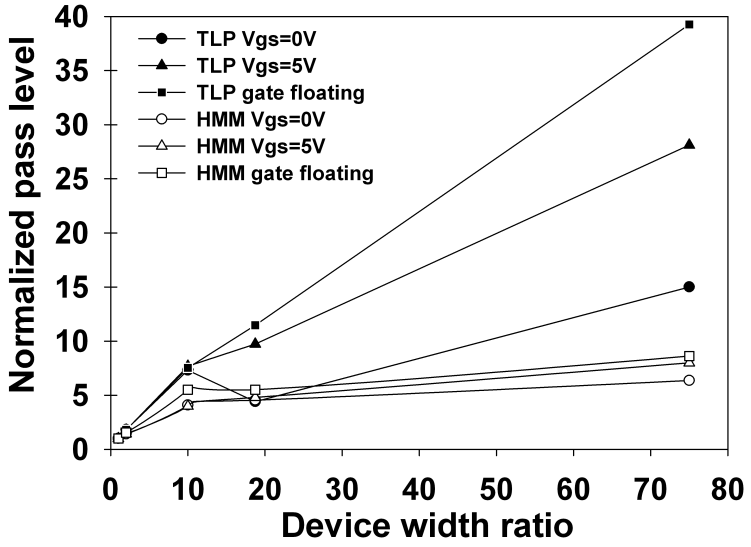

Figure 5.20: Normalized TLP passing levels and normalized HMM passing levels vs. device width ratio

5.3 Interaction between Clamp and NLDMOS

5.3.1 20V NLDMOS

Table 5.7 depicts the maximum VFTLP and TLP current levels before failure and the respective on-wafer HMM pass levels for standalone and parallel devices combinations. Predicting the HMM pass levels of parallel combinations based on the HMM standalone pass levels, however, poses complications due to the mutual interaction between the devices. This mutual interaction changes the equivalent circuit and loading characteristics. As discussed by Maloney for VFTLP stress conditions in [60], the standalone device capacitance, inductance

and resistance of the DUT are current dependent. When a protection element and the NLDMOS device are connected in parallel each device equivalent circuit and the net load of the parallel combination change as a function of time and current conduction during the ESD stress.

Table 5.7: HMM pass levels for standalone devices and parallel combinations.

Pulse Width	1ns (A)	10ns (A)	100ns (A)	Pass HMM on-wafer test (kV)
Rise Time (ns)	0.1	0.1	0.2/10	
LHVC	15	10	5.9/6	3.9
HHVC2	> 16	> 18	8.9/8.9	5.2
20V NLDMOS	3.28	0.1	0.065/0.066	< 0.3
20V NLDMOS + LHVC	10.6	1.18	1.2/6	< 0.3
20V NLDMOS + HHVC2	5.7	3.9	8.9/8.9	3.2

Notice that the parallel combinations of both LHVC and HHVC 2 under 1- and 10- ns passed lower level than the clamp standalone. For 100-ns TLP testing, the LHVC in parallel with NLDMOS was more sensitive to rise time of the TLP test (consistent with observation in Fig. 4.38), while the HHVC 2 exhibits similar failure levels as the parallel combination under TLP. The 100 ps rise time VFTLP result indicated that the clamps would no protect the NLDMOS until the failure, but only part way through, noticeable by comparing the HMM pass level of 3.2 kV instead of 5.7 kV (corresponding to the HHVC 2 clamp).

From the measurement results in the parallel devices, direct correlation was not identified between TLP measurement and the HMM parallel pass levels. More accurate pass protection level prediction based on TLP measurements for parallel devices requires device-specific effective resistance and capacitance loading variability considerations as a function of time in the core NLDMOS and protection device. This is needed to identify the net loading change versus current stress conditions and estimate how this loading condition interacts with the specific discharge characteristics and the stress level that the combined devices can sustain.

In some cases a resistor can be added at the drain of the core LDMOS device in order to use a specific clamp which would not fully protect the device without the resistor. The resistor value added should be the minimum possible in order not to interfere with the circuit design.

5.3.2 40V NLDMOS

From the ESD design perspective of special interest is the case of non self protecting High Voltage (HV) MOS in open drain protection scheme. For this case only a dedicated usually a high holding voltage clamp in parallel with the HV MOS is allowed. In open drain cases, the competitive triggering of the clamp and HV NMOS device increases the number of cycles the design takes. One way to alleviate this problem is to adjust the resistance at the drain [1] to assure the suppression of NLDMOS triggering and encourage the clamp

triggering. Another approach is to include a detection circuit which also includes an isolation resistance at the drain greater than 50 ohm [123]. In general, when adding the resistor the drawback is that the resistor value is empirical, and thus not the optimum/minimum. As a consequence, it may not provide the protection level required. On the other hand, the value of the resistor may be unacceptable for the circuit in normal operation. For this purpose, a version of 40V NLDMOS was studied standalone and in parallel with protection clamps, with and without a resistor at the drain. The competitive triggering of NLDMOS and High Voltage clamps as a function of NLDMOS size under very fast transient stress of Transmission Line Pulsing type (TLP) of 10, and 100 ns duration and their HMM performance is studied. The competitive triggering balance is changed by adding different values of the resistor in the drain in order for the clamp to be able to conduct only, instead of sharing the current with the NLDMOS.

The NLDMOS devices considered were fabricated in 40 V operation BCD technology and the widths of 0.2 mm (4 stripes of 50 μm each, 4x50 μm) and 2 mm (20x2x50 μm) which are typical widths that require protection. The DC breakdown voltage is 58V. The devices are laid out in grounded gate configuration. The structures were tested under Very Fast TLP (VFTLP) of 10 ns, with 100 ps rise time, TLP of 100 ns with 0.2 rise time and Human metal Model (HMM) with different resistances at the drain (named Rd) of the NLDMOS in standalone configuration, and in parallel configurations.

Figure 5.21 shows standalone NLDMOS and standalone clamp used under 100 ns TLP stress with 0.2 ns rise time. Each device is shown with the snapback part. The clamp

pass level is about 3.5A, the small devices has very small TLP current level, while the 2 mm device sustains about 2A of TLP current.

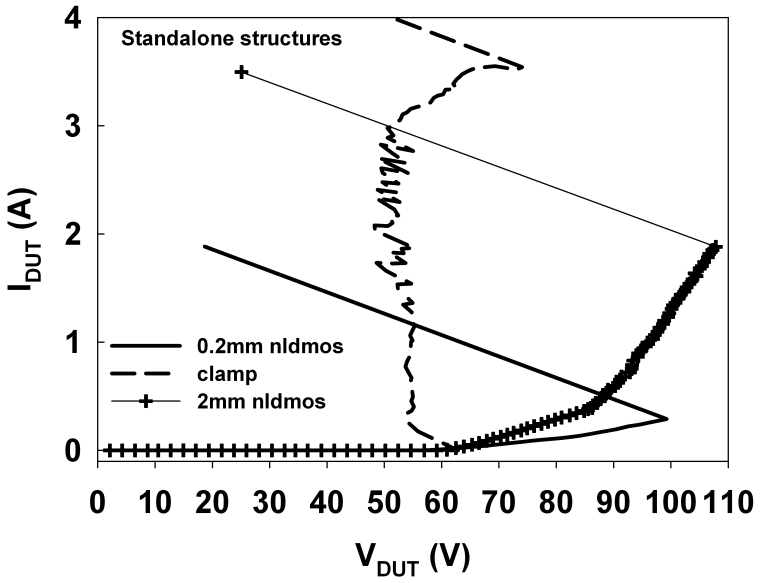

Figure 5.21: Standalone NLDMOS and protection devices under 100 ns TLP with 0.2 ns rise time

Table 5.8 shows results for 0.2 mm device in 40V where standalone pass levels under pulsed conditions for NLDMOS with and without the resistor at the drain (Rd) are described. Included in the table are and the highest Vpulse, the charge line voltage (at 50 ohm load), voltage (VDUT) and current (IDUT) prior to failure. The failure is detected by one order of magnitude leakage current change. In Table 5.9 the parallel combinations with and without (w/wo) the resistor at the drain under pulsed conditions are described. Finally, in table 5.10 the HMM pass levels for standalone and parallel combinations are described.

Table 5.8: Pre Failure Vpulse, VDUT AND IDUT pass levels for pulsed testing for 0.2 mm 40V standalone NLDMOS and standalone clamp

device	Rd(ohm)	duration(ns)	V pulse(V)	VDUT (V)	IDUT (A)
dmos	0	10	60	98.70	0.38
dmos	25	10	66	110.86	0.38
dmos	50	10	72	122.32	0.38
dmos	100	10	84	146.66	0.36
clamp	0	10	226	93.82	7.05
dmos	0	100	53	99.25	0.29
dmos	25	100	55	105.09	0.26
dmos	50	100	60	115.01	0.28
dmos	100	100	66	129.61	0.25
clamp	0	100	112	63.58	3.48

Table 5.9: Pre Failure Vpulse, VDUT AND IDUT pass levels for pulsed testing for 0.2 mm parallel NLDMOS and clmap w/wo drain resistor in 40V

device	Rd(ohm)	duration(ns)	V pulse(V)	VDUT (V)	IDUT (A)
dmos+ clamp	0	10	98	90.25	2.02
dmos+ clamp	10	10	206	79.51	6.59
dmos+ clamp	25	10	216	87.73	6.79
dmos+ clamp	50	10	203	81.13	6.43
dmos+ clamp	100	10	220	93.15	6.89
dmos+ clamp	0	100	99	53.73	3.13
dmos+ clamp	10	100	116	67.09	3.60
dmos+ clamp	25	100	116	64.15	3.64
dmos+ clamp	50	100	118	65.04	3.72
dmos+ clamp	100	100	120	76.79	3.58

Table 5.10: HMM pass levels for 0.2 mm parallel NLDMOS and clmap w/wo drain resistor in 40V

device	Rd(ohm)	V charge pass(kV)
dmos	0	0.27
dmos	25	0.29
dmos	50	0.30
dmos	100	0.32
clamp	0	1.31
dmos+ clamp	0	0.67
dmos+ clamp	10	1.3
dmos+ clamp	25	1.38
dmos+ clamp	50	1.29
dmos+ clamp	100	1.27

For the smaller 0.2 mm device 10 ohms suffices for full HMM protection (standalone clamp level), and the pulsed testing in table 5.9 shows the same results. For this case, the clamp in parallel with the NLDMOS already provided some level of protection.

For 2 mm NLDMOS devices standalone HMM pass level with the Vgs=0V is 1kV. No combination available from 0 to 50 ohms at the drain ensured that the clamp can protect the NLDMOS device. The same outcome can be seen in the pulsed testing as shown in Figure

5.22. This result points that the wider NLDMOS has much higher gate coupling effect then the smaller one and that further optimization of the gate connection is required.

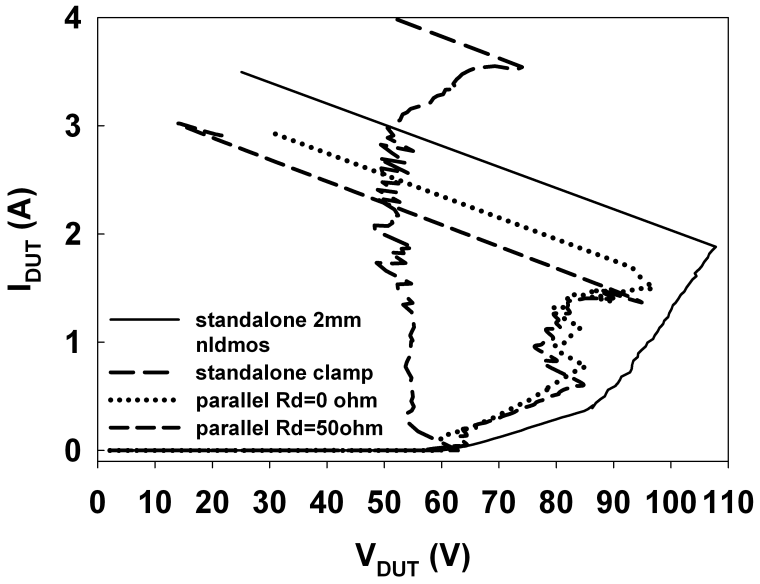

Figure 5.22: Standalone 2mm nldmos , standalone clamp and parallel combinations under 100ns TLP with 0.2ns rise time

5.4 Chapter Remarks

An improved correlation between the HMM and transmission line pulsing (TLP) testing was developed in this work based on the energies associated with the HMM and TLP stresses. It is superior to those reported in the literature because of the inclusion of important TLP parameters like the holding voltage, on-state resistance and failure current. For 20V NLDMOS the correlation between HMM pass levels and 10 ns pulsed stress was obtained.

On the other had, for 40V NLDMOS no such correlation was achieved due to severe current non uniformity under HMM. The maximum TLP failure currents and HMM passing voltage levels for NLDMOS fabricated in a 0.18-micron 40V BCD process with different widths and different gate bias conditions were introduced. Performance scaling with device width is much higher for the TLP than for the HMM stress conditions, indicating that TLP testing is not suitable to design HMM self-protected LDMOS output circuits. Independent of the size of NLDMOS, a low HMM robustness was consistently obtained even under gate biased conditions. This limits the capability of the device to be self-protected and eliminates the option of relying on the device size to achieve target IEC-61000-4-2 robustness at the pin level.

CHAPTER 6
CONCLUSIONS AND FUTURE WORK

A methodology to more precisely define the targets for ESD protection devices under very fast transient stress was presented. The focus of this work is on output pins in high voltage and input pins in low voltage domain as those are the pins with the most common failures. Human Metal Model (HMM) related failures for output pins and Charged Device Model (CDM) type related failures in input pins were the stress conditions of interest.

The CDM type gate oxide failure was studied through very fast pulsed transient measurements as a function of gate oxide thickness and area. Both oxide thickness dependence and area scaling dependence were observed. Further work can be done to extend this methodology to CDM waveforms. Additional effort can also be placed in developing a gate oxide breakdown model under arbitrary transient stress. Furthermore,this effort could be extend to study drain to gate oxide failure as laterally diffused devices have been reported to fail due to drain to gate oxide failure rather than the typical junction failure.

ESD design targets under Human Metal Model (HMM) contact type stress in high voltage Laterally Diffused N type MOS (NLDMOS) outputs were studied as a function of device width and gate bias conditions. NLDMOS devices were first studied in standalone configuration, and in the second stage with the clamp in parallel.

Standalone clamp HMM robustness is evaluated both on wafer and in packaged option by the contact test. A prediction methodology for HMM type stress is developed based on standardized testing. The HMM stress applied was contact test, and the study can be extended to address air gap test and possible correlation with standardized testing on: standalone clamp or LDMOS structures, their parallel combinations and even parts of the output circuits.

APPENDIX A
IMPORTING THE STRUCTURE FROM TS4 TO SENTAURUS ENVIROMENT

In figure A.1 the file/simulation flow used in this study starting from the process simulation, format conversion and preprocessing, followed by device simulation and finally visualization of the device simulation output is presented. The file extensions are included for clarity in the samples given below.

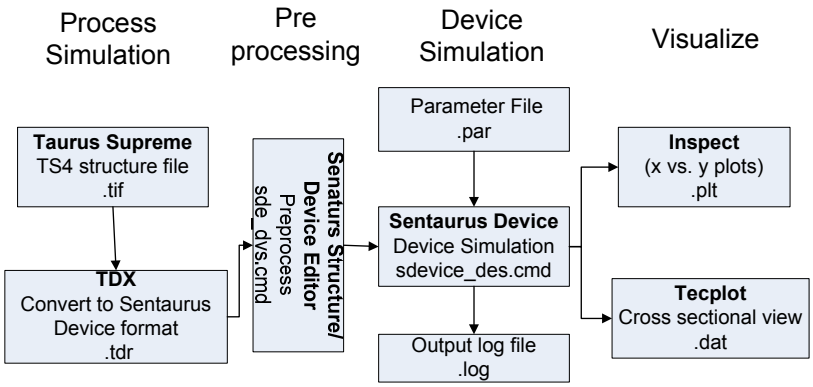

Figure A.1: Tool and file flow during the device simulation

First the process simulation in Taurus (TS4) is performed after which TIF format is obtained. Sentaurus Device uses the TDR format which is a binary format developed by Synopsys. In order to convert between different formats from TIF to TDR a utility called TDX in Sentaurus Data Explorer [102] is used. It converts, views, and edits TDR files.

After the structure format is converted to a Sentaurus Device readable format, Sentaurus Structure Editor (SSE) tool is used for pre processing: usually contacts are re created

(optional), bottom of the substrate is cut off to desired depth, and finally re-meshing of the structure for device simulation is performed as the process simulation mesh is very dense.

Below is the Sample Code For Importing and Meshing a Structure from Taurus Process (TS4) to Sentaurus Device.

```
; This file gets  TS4 structure ready for device simulation
;Slavica Malobabic July 2011
; Symbol ; is used  for comments
;Sentaurus Structure Editor Version D-2010.03, March 2010


; @name@ is a variable in the SWB , it is the name of the structure used
; n@node@ keeps track of which node inside of the execution tree the variable
;is in.
;*****************************************************************************
;First load GEO_lib.scm for additional features

(load "GEO_lib.scm")
(define MinAngle 0.4)

;Name of the TS4 structure is name_elec.tif
;(this file comes out of TS4. The structure is simulated and the contacts are
;placed)

(define TIFstem "@name@_elec")

;Name of the TDR structure
; it will be n followed by a node number it was excetuted then name_tif
(define TDRstem "n@node@_@name@_tif")

;Now convert tif to tdr

(sdemp:read-tif-bnd TIFstem TDRstem MinAngle)

;*****************************************************************************
; Boundary simplification

;- Remove all vertices along a straight line

(define eList (ise:window-select-2d -100 -100 100 100 "all" "edge") )
```

```
(isegeo:delete-collinear-edges eList)

;*****************************************************************************
;- Electrode information
;Only define the missing electrodes or if structure was modified re-define
;contacts again

;*****************************************************************************
;Place sub meshes

;The information about the doping profiles is incorporated from .tdr file

(sdedr:define-submesh "SubMesh" "n@node@_@name@_tif.tdr" 'w)
(sdedr:define-refinement-window "Win.RightHalf" "Rectangle"
(position -100 -100 0.0)
(position  100  100 0.0) )
(sdedr:define-submesh-placement "SubMesh_R" "SubMesh"
"Win.RightHalf" )

; Meshing is done by defining refinement windows of different kind

; Defining a refinement window for the whole device

(isedr:define-refinement-window "RefWin.all"
  "Rectangle" (position -100 -100 0.0) (position 100 100 0.0))

; Defining mesh spacing in each refinement window

;The format is size wise is xmin xmax ymin ymax
(isedr:define-refinement-size "RefDef.all" 0.25 0.1 0.05 0.005)

;The placement is done by using the criteria

(isedr:define-refinement-function "RefDef.all" "DopingConcentration"
 "MaxTransDiff" 0.5)

; Placement - put together refinement window and meshing spacing

(isedr:define-refinement-placement "PlaceRF.all" "RefDef.all" "RefWin.all")

;*****************************************************************************
; Boundary file is saved file _bnd.tdr. It contains the materials, but not the
;doping information.
```

```
(ise:save-model "n@node@_@name@_msh")

;*****************************************************************************
;- Build Mesh and get the final file called *_msh.tdr

;That is the file used in the device simulation
;Name is name_msh.tdr

(ise:build-mesh "mesh" "-s -F tdr" "@name@_msh")
```

APPENDIX B
BLOCKING JUNCTION DC SIMULATION SETUP

This appendix contains the DC simulation setup for Blocking Junction with two terminals Anode and Cathode.

After using steps from the previous appendix, use the following *.cmd* and *.par* files for the simulation. File *sdevice.par* is used primarily to modify the Impact Ionization parameters in order to match the DC breakdown voltage. Other parameters are also changed and the flags are used to include/ exclude models.

```
;Contents for sdevice_des.cmd

* This file simulates a Blocking Junction in reverse in Sentaurus Workbench(SWB)
*Slavica Malobabic July 2011
* The symbol * is used for comments
* Sentaurus Device Version D-2010.03, March 2010

*****************************FLAGS*********************************************

* Flags are used to include/exclude the model options

*LT flag is used to include =1 or exclude=0 temperature simulation
#if @LT@ == 1
#define _optLT_ TempDependence
#define _eqLT_ Temperature
#else
#define _optLT_
#define _eqLT_
#endif

*Enormal flag is used to include =1 or exclude=0 degradation in mobility due to
*normal electric field

#if @Enormal@ == 1
#define _optEnormal_ Enormal
#else
#define _optEnormal_

#endif

*********************************FILES*****************************************
```

```
File {
*Input structure file (the one converted from TS4)

   Grid=   "@name@_msh.tdr"

*Which parameter files to use (by default it finds sdevice.par or any .par file
*in which case the full file name is required)

Parameter="@parameter@"

* Output files:
*Naming scheme is flexible except for n@node@_ part. One can use any combination
*of variables in SWB or fixed values.

   Plot=   "n@node@_@name@_Vcathode_@iimodel@_BGN_@BGN@_@bulk_mobility@_Enormal
@Enormal@_Temperature@LT@_taun@taun@_taup@taup@_blowe@blowe@_bhighe@bhighe@
_blowh@blowh@_bhighh@bhighh@.dat"
   Current="n@node@_@name@_Vcathode_@iimodel@_BGN_@BGN@_@bulk_mobility@_Enormal
@Enormal@_Temperature@LT@_taun@taun@_taup@taup@_blowe@blowe@_bhighe@bhighe@
_blowh@blowh@_bhighh@bhighh@.plt"
   Output= "n@node@_@name@_Vcathode_@iimodel@_BGN_@BGN@_@bulk_mobility@_Enormal
@Enormal@_Temperature@LT@_taun@taun@_taup@taup@_blowe@blowe@_bhighe@bhighe@
_blowh@blowh@_bhighh@bhighh@.log"
}

*****************************ELECTRODES*************************************
* Electrodes are named and their initial conditions are stated
* In this case we have starnadrd anode and cathode. The substrate is across the
bottom of the structure.
* In this part different  types of contacts can be defined. A MOS gate
workfunction value can be defined
* Or a resistor can be placed at a contact by using resistance=Resvalue
* The assumed width of the structure is 1micron , unless othrewise specified by
*writing Area= Areavalue


Electrode {
   { Name="anode"    Voltage=0.0  }
   { Name="cathode"      Voltage=0 }
   { Name="substrate" Voltage=0.0 }

}
```

```
* Use the LT flag

#if @LT@ == 1
Thermode {
{ name="substrate" Temperature=300

}
}
#endif

*****************************PHYSICS*********************************************
*Here _optLT_ is the temperature being included/excluded
*Variable iimodel is in the SWB, so one can change the Impact Ionization Model
*used
*Same applies to variable bulk_mobility
*optEnormal is variable used for the inclusion/exclusion of Enormal
*BGN is a variable used for chosing Band Gap Narrowing

Physics {
    Recombination(
     SRH(DopingDep _optLT_ )
     Avalanche ( @iimodel@ )
     Auger)

    Mobility(
     @bulk_mobility@
     HighFieldSaturation
     _optEnormal_ )

    EffectiveIntrinsicDensity(@BGN@)

  #if @LT@ == 1

  Thermodynamic
  AnalyticTEP

#endif

}
*****************************PLOTS***********************************************
*These physical variables will be calculated and can be plotted after the
*simulation

Plot{
```

```
*--Density and Currents, etc
   eDensity hDensity
   TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
   eMobility hMobility
   eVelocity hVelocity
   eQuasiFermi hQuasiFermi

*--Temperature
   *eTemperature Temperature hTemperature

*--Fields and charges
   ElectricField/Vector Potential SpaceCharge

*--Doping Profiles
   Doping DonorConcentration AcceptorConcentration

*--Generation/Recombination
   SRH Band2Band Auger
    AvalancheGeneration eAvalancheGeneration hAvalancheGeneration
   AvalancheGeneration AugerRecombination TotalRecombination
   eIonIntegral  hIonIntegral  meanIonIntegral

*--Lifetime
     eLifeTime   hLifeTime

*--Driving forces
   eGradQuasiFermi/Vector hGradQuasiFermi/Vector
   eEparallel hEparallel eENormal hENormal

*--Band structure/Composition
   BandGap
   BandGapNarrowing
   Affinity
   ConductionBand ValenceBand
   eQuantumPotential hQuantumPotential

*--Gate Tunneling
   * eBarrierTunneling hBarrierTunneling  BarrierTunneling
   * eDirectTunnel hDirectTunnel
}


*What will be used to do the simulation and when to stop it
*For more details vist the mannual
```

```
Math {
*For parallel thredas processing use the keyword:
   Number_of_Threads=maximum

   Extrapolate
   RelErrControl
   ErReff(electron)=1e5
   ErReff(hole)=1e5
   Notdamped=50
   Iterations=100
  * CNormPrint is used to see in which part of the structure the simulation is
*not converging.
  *If used it slows the simulation
   Transient=BE
 *Stop simulation when the cathode current reches 1e-9A
 *This is good enough in the simulation enviroment as  it does not simulate
*leakage current
   BreakCriteria{
   Current( Contact="cathode" maxval=1e-9)
   }
*Stop at Si melting temperature
   BreakCriteria {
    LatticeTemperature (maxval = 1693)

}
}

*Solve part where the equations to solve are solved gradually for initial
*solution
*Then the quasisitaionary command is used

Solve {

    Coupled(Iterations=1000) {Poisson}
  Coupled(Iterations=100) {Poisson Electron Hole }
  Coupled(Iterations=100) {Poisson Electron Hole _eqLT_ }

    Quasistationary (
*The inital step size, increments in steps and the minimum step the simulator
*will use

InitialStep=1e-6
                Increment=1.35     MaxStep=0.1 MinStep=10e-50
```

```
* Ramping the cathode up to voltage Vfinal defined as a variable in the SWB
               Goal{name=cathode Voltage=@Vfinal@}
       *20 crosss ections will be saved during this simulation

       Plot {Range = (0 1) Intervals=20 })
               { Coupled  { Poisson Electron Hole _eqLT_  }   }
      }



;Contents for sdevice.par

*****************************************************************************
*                              Model Parameters:                            *
*****************************************************************************

Material = "Silicon" {

*************************  Recombination Models: ****************************
* Variable = electron value ,   hole value      # [units]                    *
*****************************************************************************

Scharfetter * relation and trap level for SRH recombination:
{ * tau = taumin + ( taumax - taumin ) / ( 1 + ( N/Nref )^gamma
  * tau(T) = tau * ( (T/300)^Talpha )          (TempDep)
  * tau(T) = tau * exp( Tcoeff * ((T/300)-1) ) (ExpTempDep)
taumin = 0.0000e+00 ,0.0000e+00 # [s]
# taumax = 1.0000e-05 ,3.0000e-06 # [s]
taumax = @taun@ ,@taup@ # [s]
Nref = 1.0000e+16 ,1.0000e+16 # [cm^(-3)]
gamma = 1 ,1 # [1]
Talpha = -1.5000e+00 ,-1.5000e+00 # [1]
Tcoeff = 2.55 ,2.55 # [1]
Etrap = 0.0000e+00 # [eV]
}

}

****************************  Impact Ionization ******************************
* Van Overstraten de Man        *
* Variable = electron value ,   hole value      # [units]                    *
*****************************************************************************
vanOverstraetendeMan:

*default parameters are:
```

```
*electrons
* a(low)=a(high)=7.03*10e5
*b(low)=b(high)=1.231*10e6

*holes
* a(low)= 1.582*10e6
*a(high)=6.71*10e5
*b(low)=2.036*10e6
*b(high)=1.693*10e6

*field E0=4*10e5
*85% from original value of b
*b(low) = 1.046e+06 ,1.731e+06
*b(high)= 1.046e+06,1.439e+06

{
b(low) = @blowe@ ,@blowh@   # [V/cm]
b(high) = @bhighe@,@bhighh@ # [V/cm]
}

**************************  High Field Dependance ***************************
* beta0      *
* Variable = electron value ,   hole value      # [units]                    *
*****************************************************************************

HighFieldDependence:
{ * Caughey-Thomas model:
  * mu_highfield = ( (alpha+1)*mu_lowfield ) /
  *        ( alpha + ( 1 + ( (alpha+1)*mu_lowfield*E/vsat)^beta )^(1/beta) )
  * beta = beta0 (T/T0)^betaexp.

beta0 = @betan@ ,@betap@ # [1]

}
```

APPENDIX C
NMOS DC SIMULATION SETUP

The following is the sample code to import and mesh a two finger NLDMOS structure. There are two drain contacts named drain1 and drain2 and there are two source contacts named source1 and source2. There is one body contact and the bottom of the structure is the substrate contact. The cross section after TS4 process simulation is given in Figure C.1

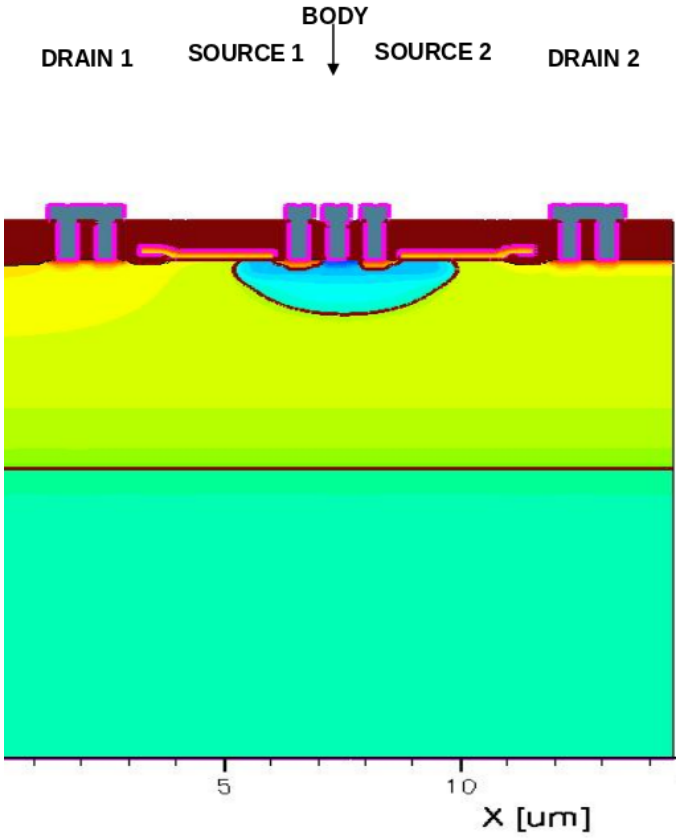

Figure C.1: Cross section of NLDMOS structure after process simulation

The layout variables used for the meshing are:

- Drain1Edge1- Left edge position of drain1
- DrainEdge2 - Left edge position of drain2

- BodyEdge - Left edge position of body
- GateEdge1 - Left edge position of gate1
- GateEdge2 - Left edge position of gate2
- SourceEdge1 - Left edge position of source1
- SourceEdge2 - Left edge position of source2
- SourcePNEdge1 - Left edge position of the deep n well and pwell
- SourcePNEdge2- Left edge position of the deep n well and pwell
- GateWidth - Gate Width
- WellDepth - Depth of the vertical PN junction formed by pwell and deep n well
- ContactWidth - Width of the contacts
- tox - Gate oxide thickness
- LocosDepth - Bottom Locos Position
- LocosLength - Locos Length
- PolyLine - Cut line position to cut off the top part of the structure

Figure C.2 shows the NLDMOS cross section after the import process and meshing based on layout variables.

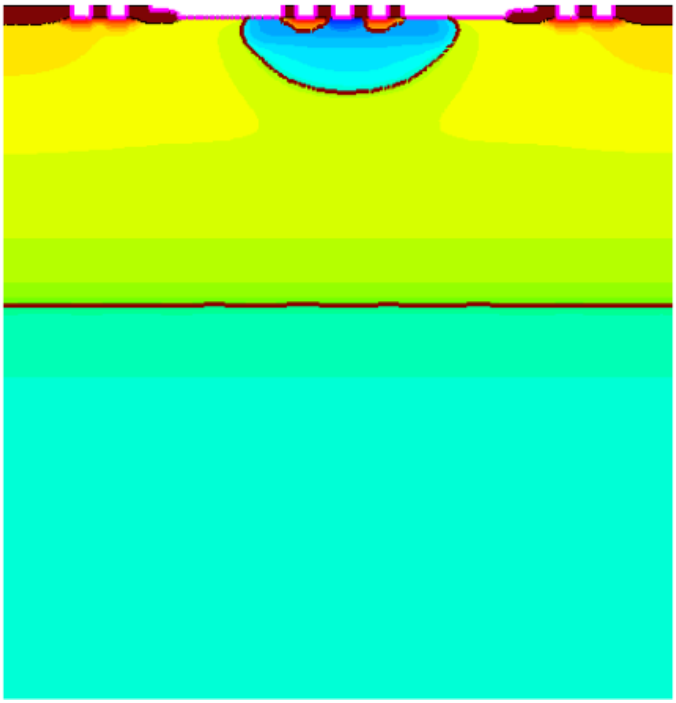

Figure C.2: Cross section of NLDMOS structure after the import from TS4 to Senataurus Device

The following code in Sentaurus Structure Editor imports and meshes the NLDMOS based on its layout variables.

```
; This file gets  TS4 form ready for device simulation
;Slavica Malobabic, July 2011
;The variables used are defined in the SWB
; Include picture and the layout variables

;Now load GEO_lib.scm for additional features

(load "GEO_lib.scm")
(define MinAngle 0.4)
(define epsilon   (* 50 nm))
(define Ycut @PolyLine@)
(define TIFstem "@name@_elec")
```

```
(define TDRstem "n@node@_@name@_tif")
;Now convert tif to tdr
(sdemp:read-tif-bnd TIFstem TDRstem MinAngle)


;Analyse geometry

(display "Global bounding box:")   (newline)

(define Xmin (sdemp:GetGlobalXmin))
(define Xmax (sdemp:GetGlobalXmax))
(define Ymin (sdemp:GetGlobalYmin))
(define Ymax (sdemp:GetGlobalYmax))

(display   "(Xmin = ") (display Xmin) (display Unit)
(display " ; Ymin = ") (display Ymin) (display Unit)
(display ") (Xmax = ") (display Xmax) (display Unit)
(display " ; Ymax = ") (display Ymax) (display Unit) (display ")") (newline)

(define SiID (find-material-id "Silicon"))
(define YminSi (sdemp:GetRegionYmin SiID))
(display "Silicon top coordinate (min Y):   YminSi = ") (display YminSi)
 (display Unit) (newline)

(define OxID (find-material-id "Oxide"))
(define YmaxOx (sdemp:GetRegionYmax OxID))
(display "Oxide bottom coordinate (max Y):   YmaxOx = ") (display YmaxOx)
 (display Unit) (newline)

;-----------------------------------------------------------------------
; Boundary simplification

;- Cut off all upper layers that play very minor role in electrical results

(sdegeo:set-default-boolean "ABA")
(sdegeo:create-rectangle (position Xmin Ymin 0)
 (position Xmax Ycut 0) "Gas" "tmp_top")
(sdegeo:delete-region (find-material-id "Gas"))

(define Ymin Ycut)

;- Remove all vertices along a straight line

(define eList (ise:window-select-2d -100 -100 100 100 "all" "edge") )
```

```
(isegeo:delete-collinear-edges eList)


 ;-----------------------------------------------------------------------#
;- Electrode information
; Redefine the contacts as the top part was removed

(sdegeo:define-contact-set "substrate")
(sdegeo:set-current-contact-set "substrate")
(sdegeo:set-contact-edges (find-edge-id (position (/ (+ Xmin Xmax) 2) Ymax 0)))

(sdegeo:define-contact-set "body")
(sdegeo:set-current-contact-set "body")
(define BodyMetal
 (find-body-id (position (+ @BodyEdge@ epsilon) (- YminSi epsilon) 0 )))
(sdegeo:set-contact-boundary-edges BodyMetal)
(sdegeo:delete-region BodyMetal)


(sdegeo:define-contact-set "source1")
(sdegeo:set-current-contact-set "source1")
(define SourceMetal
 (find-body-id (position (+ @SourceEdge1@ epsilon) (- YminSi epsilon) 0 )))
(sdegeo:set-contact-boundary-edges SourceMetal)
(sdegeo:delete-region SourceMetal)

(sdegeo:define-contact-set "source2")
(sdegeo:set-current-contact-set "source2")
(define SourceMetal
 (find-body-id (position (+ @SourceEdge2@ epsilon) (- YminSi epsilon) 0 )))
(sdegeo:set-contact-boundary-edges SourceMetal)
(sdegeo:delete-region SourceMetal)

(sdegeo:define-contact-set "gate")
(sdegeo:set-current-contact-set "gate")
(define GatePoly (find-material-id "PolySilicon"))
(sdegeo:set-contact-boundary-edges GatePoly)
(sdegeo:delete-region GatePoly)

(sdegeo:define-contact-set "drain1")
(sdegeo:set-current-contact-set "drain1")
(define DrainMetal
 (find-body-id (position (+ @DrainEdge1@ epsilon) (- YminSi epsilon ) 0 )))
(sdegeo:set-contact-boundary-edges DrainMetal)
```

```
(sdegeo:delete-region DrainMetal)



(sdegeo:define-contact-set "drain2")
(sdegeo:set-current-contact-set "drain2")
(define DrainMetal
 (find-body-id (position (+ @DrainEdge2@ epsilon) (- YminSi epsilon) 0 )))
(sdegeo:set-contact-boundary-edges DrainMetal)
(sdegeo:delete-region DrainMetal)




;--- Place sub meshes -------------------------------------------------
;The information about the doping profiles is incorporated from .tdr file

(sdedr:define-submesh "SubMesh" "n@node@_@name@_tif.tdr" )
(sdedr:define-refinement-window "Win.Global" "Rectangle"
(position -100 -100 0.0)
(position  100  100 0.0) )
(sdedr:define-submesh-placement "SubMesh_R" "SubMesh" "Win.Global" )


;-------------------------------------------------------------------------
;- Meshing is done by defining refinement windows of different kind
;-------------------------------------------------------------------------
;All of the structure

;- Meshing criteria substrate
(sdedr:define-refinement-window "RWin.Substrate"
 "Rectangle"
 (position Xmin 6 0)
 (position Xmax  Ymax 0))
(sdedr:define-refinement-size "RSize.Substrate"
  (/ (- Xmax Xmin) 8.0)  (/ (- Ymax Ymin) 16.0)
                   0.5                     0.5)
(sdedr:define-refinement-region "RPlace.Substrate"
 "RSize.Substrate" "RWin.Substrate" )
;-------------------------------------------------------------
; PN junction between substrate and deep nwell
(sdedr:define-refinement-size "RSize.BodyPN"
  (/ (- Xmax Xmin) 8.0)          0.4
                   0.5           0.2)
```

```
(sdedr:define-refinement-function "RSize.BodyPN"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-window "RWin.BodyPN"
 "Rectangle"
 (position Xmin 4 0)
 (position Xmax  10 0))
(sdedr:define-refinement-placement "RPlace.BodyPN"
 "RSize.BodyPN" "RWin.BodyPN" )
;-----------------------------------------------------------
; Top area
(sdedr:define-refinement-size "RSize.TopArea"
  (/ (- Xmax Xmin) 16.0)  (/ 4.0 10.0)
                    0.1           0.1)
(sdedr:define-refinement-window "RWin.TopArea"
 "Rectangle"
 (position Xmin YminSi 0)
 (position Xmax (+ YminSi 4.0) 0))
(sdedr:define-refinement-placement "RPlace.TopArea"
 "RSize.TopArea" "RWin.TopArea" )

;-----------------------------------------------------------------
;Drain 1  mesh
(sdedr:define-refinement-size "RSize.DrainDiff1"
  0.2   0.1
  0.04  0.04)
(sdedr:define-refinement-window "RWin.DrainDiff1"
 "Rectangle"
 (position  Xmin    YmaxOx 0)
 (position @SourcePNEdge1@ (+ YmaxOx @WellDepth@) 0))
(sdedr:define-refinement-function "RSize.DrainDiff1"
 "DopingConcentration" "MaxTransDiff" 0.5)
(sdedr:define-refinement-placement "RPlace.DrainDiff1"
 "RSize.DrainDiff1" "RWin.DrainDiff1" )
;-----------------------------------------------------------------
;Drain 2  mesh
(sdedr:define-refinement-size "RSize.DrainDiff2"
  0.2   0.1
  0.04  0.04)
(sdedr:define-refinement-window "RWin.DrainDiff2"
 "Rectangle"
 (position  @SourcePNEdge2@    YmaxOx 0)
 (position Xmax (+ YmaxOx @WellDepth@) 0))
(sdedr:define-refinement-function "RSize.DrainDiff2"
 "DopingConcentration" "MaxTransDiff" 0.5)
```

```
(sdedr:define-refinement-placement "RPlace.DrainDiff2"
 "RSize.DrainDiff2" "RWin.DrainDiff2" )
;-----------------------------------------------------------------
;LOCOS 1 meshing
(sdedr:define-refinement-size "RSize.DrainLOCOS1"
  0.3   0.045
  0.04  0.04)
(sdedr:define-refinement-window "RWin.DrainLOCOS1"
 "Rectangle"
 (position (+ @DrainEdge1@ 1.2)  0 0)
 (position ( + @GateEdge1@ @LocosLength@ ) @LocosDepth@ 0))
(sdedr:define-refinement-placement "RPlace.DrainLOCOS1"
 "RSize.DrainLOCOS1" "RWin.DrainLOCOS1" )
 ; only cover locos area not the channel itself
;-----------------------------------------------------------------
;LOCOS 2 meshing
(sdedr:define-refinement-size "RSize.DrainLOCOS2"
  0.3   0.045
  0.04  0.04)
(sdedr:define-refinement-window "RWin.DrainLOCOS2"
 "Rectangle"
 (position ( + @GateEdge2@ 2.1)  0 0)
 (position @DrainEdge2@  @LocosDepth@ 0))
(sdedr:define-refinement-placement "RPlace.DrainLOCOS2"
 "RSize.DrainLOCOS2" "RWin.DrainLOCOS2" )

;-----------------------------------------------------------------
;Part of the channel under source
(sdedr:define-refinement-size "RSize.SourceChannel"
  0.2   0.2
  0.04  0.04)
(sdedr:define-refinement-window "RWin.SourceChannel"
 "Rectangle"
 (position @SourcePNEdge1@     YminSi 0)
 (position @SourcePNEdge2@   (+ YminSi @WellDepth@) 0))
(sdedr:define-refinement-function "RSize.SourceChannel"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RPlace.SourceChannel"
 "RSize.SourceChannel" "RWin.SourceChannel" )
;-----------------------------------------------------------------
;Drain gate meshing 1
(sdedr:define-refinement-size "RSize.DrainGate1"
  0.1   0.1
  0.04  0.04)
```

```
(sedr:define-refinement-window "RWin.DrainGate1"
 "Rectangle"
 (position ( + @GateEdge1@ @LocosLength@ )      YminSi 0)
 (position @SourcePNEdge1@   (+ YminSi @WellDepth@) 0))
(sedr:define-refinement-function "RSize.DrainGate1"
 "DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-placement "RPlace.DrainGate1"
 "RSize.DrainGate1" "RWin.DrainGate1" )

;-------------------------------------------------------------------------
;Drain gate meshing 2
(sedr:define-refinement-size "RSize.DrainGate2"
  0.1   0.1
  0.04  0.04)
(sedr:define-refinement-window "RWin.DrainGate2"
 "Rectangle"
 (position @SourcePNEdge2@      YminSi 0)
 (position ( + @GateEdge2@ 2.1)   (+ YminSi @WellDepth@) 0))
(sedr:define-refinement-function "RSize.DrainGate2"
 "DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-placement "RPlace.DrainGate2"
 "RSize.DrainGate2" "RWin.DrainGate2" )
;-------------------------------------------------------------------------------
;DrainContact 1 meshing
(sedr:define-refinement-size "RSize.DrainCont1"
  0.25  0.05
  0.04  0.04)
(sedr:define-refinement-window "RWin.DrainCont1"
 "Rectangle"
 (position @DrainEdge1@  0 0)
 (position (+ @DrainEdge1@ 1.2)  0.3 0))
(sedr:define-refinement-function "RSize.DrainCont1"
 "DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-placement "RPlace.DrainCont1"
 "RSize.DrainCont1" "RWin.DrainCont1" )
; assumed 0.3 is the depth of n plus implant
; 1.2 is becuse I have the edge and there are two contacts
;-------------------------------------------------------------------------------
;DrainContact 2 meshing
(sedr:define-refinement-size "RSize.DrainCont2"
  0.25  0.05
  0.04  0.04)
(sedr:define-refinement-window "RWin.DrainCont2"
 "Rectangle"
```

```
 (position @DrainEdge2@  0 0)
 (position (+ @DrainEdge2@ 1.2)  0.3 0))
(sdedr:define-refinement-function "RSize.DrainCont2"
 "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "RPlace.DrainCont2"
 "RSize.DrainCont2" "RWin.DrainCont2" )
; assumed 0.3 is the depth of n plus implant
;-----------------------------------------------------------------------
;Channel

; Channel Multibox 1
(sdedr:define-refinement-window "MBWindow.Channel1"
 "Rectangle"
 (position ( + @GateEdge1@ @LocosLength@ )      YminSi 0)
 (position @SourcePNEdge1@   (+ YminSi @WellDepth@) 0) )
(sdedr:define-multibox-size "MBSize.Channel1"
  0.2   0.2
  0.005 0.005
  0.0   1.35 )
(sdedr:define-multibox-placement "MBPlace.Channel1"
 "MBSize.Channel1" "MBWindow.Channel1" )

 ; Channel Multibox 2
(sdedr:define-refinement-window "MBWindow.Channel2"
 "Rectangle"
 (position @SourcePNEdge2@      YminSi 0)
 (position ( + @GateEdge2@ 2.1)   (+ YminSi @WellDepth@) 0))
(sdedr:define-multibox-size "MBSize.Channel2"
  0.2   0.2
  0.005 0.005
  0.0   1.35 )
(sdedr:define-multibox-placement "MBPlace.Channel2"
 "MBSize.Channel2" "MBWindow.Channel2" )


 ; Gate Channel Multibox1
(sdedr:define-refinement-window "MBWindow.Gateox1"
 "Rectangle"
 (position ( + @GateEdge1@ @LocosLength@ )     YminSi      0.0)
 (position @SourcePNEdge1@ (- YminSi @tox@) 0.0) )
(sdedr:define-multibox-size "MBSize.Gateox1"
  0.2   0.2
  0.005 0.005
  0.0   -1.35 )
```

```
(sdedr:define-multibox-placement "MBPlace.Gateox1"
 "MBSize.Channel1" "MBWindow.Channel1" )

; Gate Channel Multibox2
(sdedr:define-refinement-window "MBWindow.Gateox2"
 "Rectangle"
 (position @SourcePNEdge2@    YminSi      0.0)
 (position ( + @GateEdge2@ 2.1) (- YminSi @tox@) 0.0) )
(sdedr:define-multibox-size "MBSize.Gateox2"
  0.2   0.2
  0.005 0.005
  0.0   -1.35 )
(sdedr:define-multibox-placement "MBPlace.Gateox2"
 "MBSize.Channel2" "MBWindow.Channel2" )

; Interface refinement
(sdedr:define-refinement-window "InterfaceWindow" "Rectangle"
(position 2.2 -0.2  0.0) (position 3 0.3  0.0))
(sdedr:define-refinement-size "InterfaceSize" 0.01 0.01 0.002 0.002)
(sdedr:define-refinement-function "InterfaceSize" "MaxLenInt" "Silicon"
"Oxide" 0.1)
(sdedr:define-refinement-placement "InterfacePlace" "InterfaceSize"
"InterfaceWindow" )

;-----------------------------------------------------------------------#
;- Save model. It saves the boundary file _bnd.tdr
(ise:save-model "n@node@_@name@_msh")

;-----------------------------------------------------------------------#
;- Build Mesh and get the final file called *****_msh.tdr
;That is the file used in the device simulation
(ise:build-mesh "mesh" "-s -F tdr" "@name@_2finger_separateScontacts_msh")
```

For DC simulation the drain and source contacts do not have to be separated in which case we call drain1 and drain2 drain and the same applies to source contact. The DC simulation of drain source current (Ids) vs. gate source voltage (Vgs) for a given drain voltage Vd.

```
*This file simulates Ids vs Vgs for a given drain voltage Vd
*Slavica Malobabic July 2011

#if @Enormal@ == 1
#define _optEnormal_ Enormal
#else
#define _optEnormal_

#endif


File {
   * input files:
   Grid=   "@name@_msh.tdr"
   Parameter="@parameter@"
   * output files:
   Plot=   "n@node@_@mobility@_@BGN@_Enormal@Enormal@_thetae@thetae@
_thetah@thetah@_IdVd_Vg@Vg@_Vd@Vd@_BN@betan@_BP@betap@_CP@CP@_CN@CN@
_lambdan@lambdan@_lambdap@lambdap@_QF@QF@_taun@taun@_taup@taup@.dat"
   Current="n@node@_@mobility@_@BGN@_Enormal@Enormal@_thetae@thetae@
_thetah@thetah@_IdVd_Vg@Vg@_Vd@Vd@_BN@betan@_BP@betap@_CP@CP@_CN@CN@
_lambdan@lambdan@_lambdap@lambdap@_QF@QF@_taun@taun@_taup@taup@.plt"
   Output= "n@node@_@mobility@_@BGN@_Enormal@Enormal@_thetae@thetae@
_thetah@thetah@_IdVd_Vg@Vg@_Vd@Vd@_BN@betan@_BP@betap@_CP@CP@_CN@CN@
_lambdan@lambdan@_lambdap@lambdap@_QF@QF@_taun@taun@_taup@taup@.log"
}

Electrode {
   { Name="source"    Voltage=0.0  }
   { Name="drain"     Voltage=@Vd@  }
    { Name="gate"      Voltage=0 Workfunction=@WORKFUNCTION@ }
   { Name="substrate" Voltage=0.0 }
   { Name="body" Voltage=0.0 }


}



Physics (MaterialInteface="Oxide/Silicon"){charge(surfconc=@QF@)}

Physics{
```

```
    EffectiveIntrinsicDensity( @BGN@)
   Mobility(
      PhuMob(Phosphorus)
      HighFieldSaturation
      _optEnormal_
   )
   Recombination(
      SRH( DopingDep )
   )
}


Plot{
*--Density and Currents, etc
   eDensity hDensity
   TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
   eMobility hMobility
   eVelocity hVelocity
   eQuasiFermi hQuasiFermi

*--Temperature
   *eTemperature Temperature hTemperature

*--Fields and charges
   ElectricField/Vector Potential SpaceCharge

*--Doping Profiles
   Doping DonorConcentration AcceptorConcentration

*--Generation/Recombination
   SRH Band2Band * Auger
   * AvalancheGeneration eAvalancheGeneration hAvalancheGeneration
   AvalancheGeneration AugerRecombination TotalRecombination

*--Driving forces
   eGradQuasiFermi/Vector hGradQuasiFermi/Vector
   eEparallel hEparallel eENormal hENormal

*--Band structure/Composition
   BandGap
   BandGapNarrowing
   Affinity
   ConductionBand ValenceBand
   eQuantumPotential hQuantumPotential
```

```
*--Gate Tunneling
   * eBarrierTunneling hBarrierTunneling  BarrierTunneling
   * eDirectTunnel hDirectTunnel
}

Math {
   Extrapolate
   Notdamped=50
   Iterations=30
   *RelErrControl
}

Solve {
*- Creating initial guess:
   Coupled(Iterations=100 LineSearchDamping=1e-4){ Poisson }
   Coupled { Poisson Electron}
   Coupled { Poisson Electron Hole }


# Load saved structures and ramp drain to create family of curves:

Quasistationary
(InitialStep=0.01 Maxstep=0.1 MinStep=1e-15
Goal{ name="gate" voltage=@Vg@ }
)
{ Coupled  {Poisson Electron Hole}
CurrentPlot (time=
(range = (0 0.2) intervals=20;
range = (0.2 1.0)))}


}
```

The parameter file is listed below:

```
*******************************************************************************
*                              Model Parameters:                              *
*******************************************************************************
```

```
Material = "Silicon" {

************************  Recombination Models: ****************************
* Variable = electron value ,   hole value      # [units]                    *
*****************************************************************************

Scharfetter * relation and trap level for SRH recombination:
{ * tau = taumin + ( taumax - taumin ) / ( 1 + ( N/Nref )^gamma
  * tau(T) = tau * ( (T/300)^Talpha )          (TempDep)
  * tau(T) = tau * exp( Tcoeff * ((T/300)-1) ) (ExpTempDep)
taumin = 0.0000e+00 ,0.0000e+00 # [s]
*taumax = 1.0000e-05 ,3.0000e-06 # [s]
taumax = @taun@ ,@taup@ # [s]
Nref = 1.0000e+16 ,1.0000e+16 # [cm^(-3)]
gamma = 1 ,1 # [1]
Talpha = -1.5000e+00 ,-1.5000e+00 # [1]
Tcoeff = 2.55 ,2.55 # [1]
Etrap = 0.0000e+00 # [eV]
}

}


****************************  Impact Ionization ******************************
* Van Overstraten de Man        *
* Variable = electron value ,   hole value      # [units]                    *
*****************************************************************************

vanOverstraetendeMan:

*default parameters are:
*electrons
* a(low)=a(high)=7.03*10e5
*b(low)=b(high)=1.231*10e6

*holes
* a(low)= 1.582*10e6
*a(high)=6.71*10e5
*b(low)=2.036*10e6
*b(high)=1.693*10e6

*field E0=4*10e5
*85% from original value of b
*b(low) = 1.046e+06 ,1.731e+06
```

```
*b(high)= 1.046e+06,1.439e+06

{

b(low) = 1.046e+06 ,1.731e+06   # [V/cm]
b(high) = 1.046e+06,1.439e+06 # [V/cm]


}

*****************************  Mobility ***************************************
* PhuMob        *
* Variable = electron value ,   hole value      # [units]                      *
********************************************************************************

PhuMob:

*default parameters are:
*electrons thetae=2.285
*holes thetah=2.247


{

theta_P=@thetae@  # [1]

theta_B= @thetah@ # [1]
}

*****************************  High Field Dependance **************************
* beta0      *
* Variable = electron value ,   hole value      # [units]                      *
********************************************************************************

HighFieldDependence:
{ * Caughey-Thomas model:
  * mu_highfield = ( (alpha+1)*mu_lowfield ) /
  *        ( alpha + ( 1 + ( (alpha+1)*mu_lowfield*E/vsat)^beta )^(1/beta) )
  * beta = beta0 (T/T0)^betaexp.
beta0 = @betan@ ,@betap@ # [1]

}

EnormalDependence:
```

```
{ * mu_Enorm^(-1) = mu_ac^(-1) + mu_sr^(-1)  with:
  * mu_ac = B / Enorm + C (T/T0)^(-k) (N/N0)^lambda / Enorm^(1/3)
  * mu_sr^-1 = Enorm^(A+alpha*n/(N+N1)^nu) / delta + Enorm^3 / eta
  * EnormalDependence is added with factor exp(-l/l_crit), where l is
  * the distance to the nearest point of semiconductor/insulator interface.
  * Factor is equal to 1 if l_crit > 100.
B = 4.7500e+07 ,9.9250e+06 # [cm/s]
C = @CN@ ,@CP@ # [cm^(5/3)/(V^(2/3)s)]
N0 = 1 ,1 # [cm^(-3)]
*lambda = 0.125 ,0.0317 # [1]
lambda = @lambdan@ ,@lambdap@ # [1]
k = 1 ,1 # [1]
delta = 5.8200e+14 ,2.0546e+14 # [V/s]
A = 2 ,2 # [1]
alpha = 0.0000e+00 ,0.0000e+00 # [1]
N1 = 1 ,1 # [cm^(-3)]
nu = 1 ,1 # [1]
eta = 5.8200e+30 ,2.0546e+30 # [V^2/cm*s]
l_crit = 1.0000e-06 ,1.0000e-06 # [cm]
}
```

APPENDIX D
TRANSIENT CODE SETUP FOR 2 GATE NLDMOS VFTLP SIMULATION

This sample code performs a VFTLP stress simulation. The VFTLP current stress is taken from the measurement and converted into .st format. More about the format can be read in Appendix E.

```
*VFTLP simulation
*Slavica Malobabic July,2011


#if @LT@ == 1
#define _optLT_ TempDependence
#define _eqLT_ Temperature
#else
#define _optLT_
#define _eqLT_
#endif




#if @Enormal@ == 1
#define _optEnormal_ Enormal
#else
#define _optEnormal_
#endif
```

```
Device NLDMOS20s


{
File {
   * input files:
   Grid=   "@name@_msh.tdr"
   Parameter="@parameter@"
   * output files:
   Plot=   "n@node@_@name@_D@D@_S@S@_G@G@_B@B@_SUB@SUB@.dat"
   Current = "n@node@_@name@_D@D@_S@S@_G@G@_B@B@_SUB@SUB@.plt"


}


Electrode {
   { Name="source1"    Voltage=0.0  }
   { Name="source2"   Voltage=0.0  }
   { Name="gate"     Voltage= @G@ Workfunction=@WORKFUNCTION@ }
   { Name="substrate" Voltage=0.0 }
   { Name="drain1"   Voltage=0.0 }
    { Name="drain2"   Voltage=0.0 }
```

```
   { Name="body"   Voltage=0.0 }



}


#if @LT@==1

Thermode {

{name="substrate" Temperature=300 }

}

#endif


Physics (MaterialInteface="Oxide/Silicon"){charge(surfconc=@QF@)}


Physics{


    EffectiveIntrinsicDensity( BandGapNarrowing (@BGN@))

   Mobility(

      PhuMob

      HighFieldSaturation

      _optEnormal_

   )

   Recombination(
```

```
      SRH( DopingDep _optLT_) Avalanche Auger

   )

#if @LT@==1

Thermodynamic

AnalyticTEP

#endif


}

}


File {


 Output= "n@node@_@name@_D@D@_S@S@_G@G@_B@B@_SUB@SUB@.log"


}




Plot{

*--Density and Currents, etc

   eDensity hDensity

   TotalCurrent/Vector eCurrent/Vector hCurrent/Vector

   eMobility hMobility
```

```
   eVelocity hVelocity

   eQuasiFermi hQuasiFermi


*--Temperature

   *eTemperature Temperature hTemperature


*--Fields and charges

   ElectricField/Vector Potential SpaceCharge


*--Doping Profiles

   Doping DonorConcentration AcceptorConcentration


*--Generation/Recombination

   SRH Band2Band * Auger

   * AvalancheGeneration eAvalancheGeneration hAvalancheGeneration

   AvalancheGeneration AugerRecombination TotalRecombination


*--Driving forces

   eGradQuasiFermi/Vector hGradQuasiFermi/Vector

   eEparallel hEparallel eENormal hENormal


*--Band structure/Composition
```

```
   BandGap

   BandGapNarrowing

   Affinity

   ConductionBand ValenceBand

   eQuantumPotential hQuantumPotential


*--Gate Tunneling

   * eBarrierTunneling hBarrierTunneling  BarrierTunneling

   * eDirectTunnel hDirectTunnel

}


Math {

   Extrapolate

   Derivatives

   Avalderivative

   NoCheckTransientError

   RelErrControl

   Notdamped=50

   Iterations=100

   Transient=BE

 *Stop at Si melting temperature

   BreakCriteria {
```

```
    LatticeTemperature (maxval = 1693)


}
}


System{


  NLDMOS20s trans ( "drain1"=@D1@ "drain2"=@D2@ "body"=@B@ "gate"= @G@
"source1"=@S@ "source2"=@S@ "substrate"=@SUB@)


*Node named in is where the sterss is applied
*Some resistance is placed at the drain contact


Resistor_pset rd1 (@D1@ in) {resistance=11}
Resistor_pset rd2 (@D2@ in) {resistance=11}


*The width normalized stress values are is in .st file
*Node named in is where the sterss is applied
   Isource_pset vd ( 0 in) {
   pwl=(
#include "ggLDMOS20s_TC3_I100V_1.12e-9_W85_pwli.st"
   )}
```

```
*width of the device is 1 micron
 Plot "n@node@_@name@_BN@betan@_BP@betap@_CP@CP@_CN@CN@_lambdan@lambdan@_lambdap
@lambdap@_WF_@WORKFUNCTION@_D@D@_S@S@_G@G@_B@B@_SUB@SUB@.plt" ( time()  v(in) )

}



Solve {
     Poisson
     Coupled { Poisson Electron Hole }

     Coupled { Poisson Electron Hole  Contact Circuit _eqLT_ }

     Transient ( InitialStep=1e-13
                 InitialTime=0     MaxStep=0.1e-9 MinStep=10e-25 FinalTime=@tp@

                 plot { range=(0, 0.5e-9) intervals=50}
  plot { range=(0.5e-9, @tp@) intervals=50}

)
               { Coupled (Iterations=12) { Poisson Electron Hole Contact Circuit
```

```
_eqLT_ }   }

     }
```

APPENDIX E
TRANSINET CODE SETUP FOR SCR VFTLP SIMULATION

This appendix contains Pearl routine for converting comma separated value (csv) format to .st format for Transient Simulation where the transient stress is given in .st file. Special thanks to David Ellis for implementing this script.

Tool name: csv2st.sh

csv2st tlpi —tlpv—pwlv—pwli name.csv If you want to use mixed mode the pwli for current stress and it produces .st file If you want to define stress at the electrode directly then use tlpi for current stress it produces .tlpi file

The options tlpv and pwlv are for the identical processing for voltage waveforms. Read more about different formats in [105].

```
********************************************************************************
#!/usr/bin/perl
#The line above indicates to BASH what interpretter
#to use when "running" a text file.

#       $ARGV[0]  $ARGV[1]
#csv2st [OPTIONS] [CSVFILE]

use strict;
use Text::CSV;

my $user = getlogin();
my $pid = $$;
my $pwd;
my $outfile;
#Regular Expression below matches (checks for) the existance
#of a \ or a / (to see if a full path is provided)
if($ARGV[1] =~ /[\/\\]/) {
$pwd = $ARGV[1];
#Regular Expression below substitutes (replaces)
#the full path and filename with just the full path.
$pwd =~ s/(.*)[\/\\]([^\/\\]*)$/\1/;
$outfile = $2;
} else {
```

```
$pwd = `pwd`;
#Regular Expression below substitutes
#(replaces) <ENTER> with nothing.
$pwd =~ s/[\n\r\f]//g;
$outfile = $ARGV[1];
}
$outfile =~ s/.csv$//;
$outfile .= "_" . lc($ARGV[0]) . ".st";
my $csv = Text::CSV->new();
open(CSV, $ARGV[1]) or die "Cannot open CSV File: $!";
# ">" means write/overwrite. ">>" means append to this file.
#"<" (default) means read from this file.
open(ST, ">$pwd/$outfile") or die "Cannot open ST File for Writing: $!";
my $firstline = 1;
my $valCol;
my $timeCol;
while(<CSV>) {
if($csv->parse($_)) {
my @columns = $csv->fields();
if($firstline == 1) {
$firstline = 0;
for(my $i = 0; $i < @columns; $i++) {
if((lc($ARGV[0]) =~ /v/ && lc($columns[$i])
eq "voltage") || (lc($ARGV[0]) =~ /i/ && lc($columns[$i]) eq "current")) {
$valCol = $i;
}
if(lc($columns[$i]) eq "time") {
$timeCol = $i;
}
}
} elsif($firstline == 0) {
$firstline = -1;
if(lc($ARGV[0]) =~ /pwl/) {
print ST $columns[$timeCol] .
" " . $columns[$valCol] . " ";
} elsif(lc($ARGV[0]) =~ /tlp/) {
print ST $columns[$valCol] .
      " at " . $columns[$timeCol];
}
} else {
if(lc($ARGV[0]) =~ /pwl/) {
print ST $columns[$timeCol] . " " . $columns[$valCol] . " ";
} elsif(lc($ARGV[0]) =~ /tlp/) {
print ST ", " . $columns[$valCol] . " at " . $columns[$timeCol];
```

```
}
}
}
}
close(CSV);
close(ST);
```

APPENDIX F
TRANSINET CODE SETUP FOR SCR RLC SIMULATION

This sample code simulates RLC stress, with pre charged capacitor into the drain of the grounded gated NMOS.

```
*Slavica Malobabic, July 2011

*Calulating some internal variables, that will make the simulation easier
*Total simulation time
#set tp @<20*Ccdm*Rcdm>@
*Some specific vlues calculated internally
#set tp1 @<1.25*Ccdm*Rcdm>@
#set tp2 @<2.5*Ccdm*Rcdm>@
#set tp3 @<3.75*Ccdm*Rcdm>@
#set tp4 @<5*Ccdm*Rcdm>@


Device SCR

{
Electrode {
   { name="body"    voltage=0.0 }
   { name="source"     voltage=0.0 }
    { name="gate"     voltage=0.0 Workfunction=4.35}
    { name="drain" voltage=0.0}
   { name="substrate" voltage=0.0 }
}

Thermode {{ name="substrate" temperature=300 }}
Physics (MaterialInteface="Oxide/Silicon"){charge(surfconc=3e10)}

File {
    Grid    = "@name@_msh.tdr"
    *Doping  = "@doping@"
    Parameters   ="sdevice.par"
    Plot    = "n@node@_@name@_@stresstype@_@stressvalue@_@Lcdm@_@Rcdm@_@Ccdm@
_@method@_@models@_D@D@_G@G@_S@S@_B@B@_SUB@SUB@.dat"
    Current = "n@node@_@name@_@stresstype@_@stressvalue@_@Lcdm@_@Rcdm@_@Ccdm@
_@method@_@models@_D@D@_G@G@_S@S@_B@B@_SUB@SUB@.plt"

}

Physics {
```

```
    Recombination(SRH(DopingDep TempDependence) Avalanche Auger )
    Mobility(DopingDep HighFieldSaturation Enormal )
    EffectiveIntrinsicDensity(OldSlotboom)
   Thermodynamic
   AnalyticTEP
}

}

File{
   Output = "n@node@_@name@_@stresstype@_@stressvalue@_@Lcdm@_@Rcdm@_@Ccdm@
_@method@_@models@_D@D@_G@G@_S@S@_B@B@_SUB@SUB@.log"
}


Plot {
    *--Density and Currents, etc
   eDensity hDensity
   TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
   eMobility hMobility
   eVelocity hVelocity
   eQuasiFermi hQuasiFermi
   ConductionCurrentDensity
   eCurrentDensity
   hCurrentDensity

*--Temperature
   *eTemperature hTemperature
   Temperature

*--Fields and charges
   ElectricField/Vector Potential SpaceCharge ElectricField

*--Doping Profiles
   Doping DonorConcentration AcceptorConcentration

*--Generation/Recombination
   SRH Band2Band  Auger
   * AvalancheGeneration eAvalancheGeneration hAvalancheGeneration
   AvalancheGeneration AugerRecombination TotalRecombination SRH

*--Driving forces
   eGradQuasiFermi/Vector hGradQuasiFermi/Vector
   eEparallel hEparallel eENormal hENormal
```

```
*--Band structure/Composition
   BandGap
   BandGapNarrowing
   Affinity
   ConductionBand ValenceBand
   eQuantumPotential hQuantumPotential

*--Gate Tunneling
   * eBarrierTunneling hBarrierTunneling  BarrierTunneling
   * eDirectTunnel hDirectTunnel

*-- Power
   eThermoElectricPower
   hThermoElectricPower

*-- Heat
    TotalHeat
    eJouleHeat
    hJouleHeat
    RecombinationHeat
    lHeatFlux
    hHeatflux
    eHeatFlux

    DisplacementCurrentDensity

}


Math {
   Extrapolate
   Derivatives
   Avalderivative
   NoCheckTransientError
   NewDiscretization
   RelErrControl
   Notdamped=50
   Iterations=100
   CNormPrint
   Transient=BE
 *Stop at Si melting temperature
   BreakCriteria {
    LatticeTemperature (maxval = 1693)
```

```
}
}

System{

  SCR trans ("drain"=@D@  "gate"=@G@ "body"=@B@ "source"=@S@ "substrate"=@SUB@)

  *Pre charge capacitor
  Capacitor_pset Ccdm (g 0) { capacitance=@Ccdm@}
*Define the inductor
        Inductor_pset Lcdm (g r) {inductance=@Lcdm@}
*Define the resistor
Resistor_pset resd (r in) {resistance=@Rcdm@}
*Initialize value of the capacitor pre charge
Initialize ( g=@stressvalue@ )
*Set the initial condition for the inductor
Initialize ( Lcdm.branch=0 )

*width of the device is 1 micron
 Plot "n@node@_@name@_@stresstype@_@stressvalue@_@Lcdm@_@Rcdm@_@Ccdm@_@method@
_@models@_D@D@_G@G@_S@S@_B@B@_SUB@SUB@.plt" ( time()  v(g) v(r) v(d) i(resd,in)
 i(rdut,0) i(Ccdm,g ) i(Lcdm,r) )

}


Solve {
     Poisson
     Coupled { Poisson Electron Hole }

     Coupled { Poisson Electron Hole  Contact Circuit Temperature }

     Transient ( InitialStep=1e-13
                 InitialTime=0     MaxStep=0.1e-9 MinStep=10e-18 FinalTime=@tp@

  *The variables used below were calulated at the beginning of the file:

                  plot { range=(0, @tp1@) intervals=49}
 plot { range=(@tp1@, @tp2@) intervals=49}
 plot { range=(@tp2@, @tp3@) intervals=49}
 plot { range=(@tp3@, @tp4@) intervals=49}
                plot { range=(@tp4@, @tp@) intervals=9}
)
```

```
              { Coupled (Iterations=12) { Poisson Electron Hole Contact Circuit
Temperature }   }
     }
```

APPENDIX G
TRANSINET CODE SETUP FOR SCR NLDMOS PARALLEL VFTLP SIMULATION

This sample code performs a VFTLP stress simulation on a parallel combination of an SCR and NLDMOS.

```
*This code simulates NLDMOS and SCR in parallel under VFTLP stress
*Slavica Malobabic , July 2011.

*Each device is defined seperately, first SCR
*Each device needs to have the area defined

Device SCR28
{

Electrode {

   { name="cathode"     Area=90 voltage=0.0 }
   { name="cathodeg"    Area=90  voltage=0.0 }
  { name="anodeg"  Area=90 voltage=0.0 }
   { name="anode"  Area=90 voltage=0.0 }

   { name="substrate"  Area=90 voltage=0.0 }
}

Thermode {{ name="substrate" temperature=300 }}

File {
    Grid    = "@protection_name@_msh.tdr"
  Parameter="SCR.par"

    Plot    = "n@node@_@protection_name@_@stresstype@_@stressvalue@_@tr@_@ton@
_@method@_@models@_A@A@_AG@AG@_C@C@_CG@CG@_SUB2@SUB2@.dat"
    Current = "n@node@_@protection_name@_@stresstype@_@stressvalue@_@tr@_@ton@
_@method@_@models@_A@A@_AG@AG@_C@C@_CG@CG@_SUB2@SUB2@.plt"

}

Physics {
    Recombination(SRH(DopingDep TempDependence) Avalanche Auger )
    Mobility(PhuMob HighFieldSaturation Enormal)
    EffectiveIntrinsicDensity(Slotboom)
   Thermodynamic
   AnalyticTEP
}
```

```
}

*Second device is the NLDMOS

Device NLDMOS20s

{
File {
   * input files:
   Grid=   "@protected_name@_msh.tdr"
   Parameter="LDMOS20s.par"
   * output files:
   Plot=   "n@node@_@protected_name@_@stresstype@_@stressvalue@_@tr@_@ton@_D@D@
_S@S@_G@G@_B@B@_SUB1@SUB1@.dat"
   Current="n@node@_@protected_name@_@stresstype@_@stressvalue@_@tr@_@ton@_D@D@
_S@S@_G@G@_B@B@_SUB1@SUB1@.plt"

}

Electrode {
   { Name="source"     Area=100 Voltage=0.0  }
   { Name="gate"     Area=100  Voltage= 0 Workfunction=4.25 }
   { Name="substrate" Area=100  Voltage=0.0 }
   { Name="drain" Area=100  Voltage=0.0 }
   { Name="body" Area=100  Voltage=0.0 }


}

Thermode {
{name="substrate" Temperature=300 }
}

Physics (MaterialInteface="Oxide/Silicon"){charge(surfconc=3e10)}

Physics{

    EffectiveIntrinsicDensity( BandGapNarrowing (Slotboom))
   Mobility(
      PhuMob
      HighFieldSaturation
      Enormal
   )
```

```
   Recombination(
      SRH( DopingDep TempDependence) Avalanche Auger
   )

Thermodynamic
AnalyticTEP

}
}

System{

 Isource_pset vd ( 0 in) {

*The .st file defines  the VFTLP stress
   pwl=(
#include "ggLDMOS20s_TC3_I100V_1.12e-9_pwli.st"
   )}

  NLDMOS20s nldmos20s ("drain"=@D@ "body"=@B@ gate= "@G@" "source"=@S@
"substrate"=@SUB1@)

  SCR28 scr28 ("anode"=@A@ "anodeg"=@AG@ "cathode"=@C@  "cathodeg"=@CG@
 "substrate"=@SUB2@)

*width of the device is 1 micron
 Plot "n@node@_@protected_name@_@protection_name@_@stresstype@_@stressvalue@
_@tr@_@ton@_@method@_@models@_A@A@_AG@AG@_C@C@_CG@CG@_SUB2@SUB2@_D@D@_S@S@_G@G@
_B@B@_SUB1@SUB1@.plt" ( time()  v(in) )

}

File {

   * output files:
   Plot=   "n@node@_@protected_name@_@protection_name@_@stresstype@_
@stressvalue@_@tr@_@ton@_@method@_@models@_A@A@_AG@AG@_C@C@_CG@CG@_SUB2@SUB2@
_D@D@_S@S@_G@G@_B@B@_SUB1@SUB1@.dat"
   Current="n@node@_@protected_name@_@protection_name@_@stresstype@
_@stressvalue@_@tr@_@ton@_@method@_@models@_A@A@_AG@AG@_C@C@_CG@CG@_SUB2@SUB2@
_D@D@_S@S@_G@G@_B@B@_SUB1@SUB1@.plt"

}
```

```
Plot{
*--Density and Currents, etc
   eDensity hDensity
   TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
   eMobility hMobility
   eVelocity hVelocity
   eQuasiFermi hQuasiFermi

*--Temperature
   *eTemperature Temperature hTemperature

*--Fields and charges
   ElectricField/Vector Potential SpaceCharge

*--Doping Profiles
   Doping DonorConcentration AcceptorConcentration

*--Generation/Recombination
   SRH Band2Band * Augersdevice
   * AvalancheGeneration eAvalancheGeneration hAvalancheGeneration
   AvalancheGeneration AugerRecombination TotalRecombination

*--Driving forces
   eGradQuasiFermi/Vector hGradQuasiFermi/Vector
   eEparallel hEparallel eENormal hENormal

*--Band structure/Composition
   BandGap
   BandGapNarrowing
   Affinity
   ConductionBand ValenceBand
   eQuantumPotential hQuantumPotential

*--Gate Tunneling
   * eBarrierTunneling hBarrierTunneling  BarrierTunneling
   * eDirectTunnel hDirectTunnel
}

Math {
   Extrapolate
   Derivatives
   Avalderivative
   NoCheckTransientError
   NewDiscretization
```

```
   RelErrControl
   Notdamped=50
   Iterations=100
   CNormPrint
   Transient=BE
 *Stop at Si melting temperature
   BreakCriteria {
    LatticeTemperature (maxval = 1693)

}
}

Solve {
     Poisson
     Coupled { scr28.Poisson scr28.Electron scr28.Hole scr28.Contact nldmos20s.
Poisson nldmos20s.Electron nldmos20s.Hole }

     Coupled { scr28.Poisson scr28.Electron scr28.Hole scr28.Contact nldmos20s.
Poisson nldmos20s.Electron nldmos20s.Hole nldmos20s.Contact Circuit Temperature}

     Transient ( InitialStep=1e-15
                 InitialTime=0    Increment=1.35 MaxStep=0.1e-9 MinStep=10e-50
FinalTime=@tp@
                 plot { range=(0, 0.5e-9) intervals=50}
                 plot { range=(0.5e-9, @tp@) intervals=50}

)
               { Coupled (Iterations=12) { scr28.Poisson scr28.Electron
scr28.Hole scr28.Contact nldmos20s.Poisson nldmos20s.Electron nldmos20s.Hole
nldmos20s.Contact Circuit Temperature }   }
      }
```

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