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Investigation And Trade Study On Hot Carrier Reliability Of The Phemt For Dc And Rf Performance

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INVESTIGATION AND TRADE STUDY ON HOT CARRIER RELIABILITY OF THE PHEMT FOR DC AND RF PERFORMANCE

by

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ABSTRACT

A unified study on the hot carrier reliability of the Pseudomorphic High Electron Mobility Transistor (PHEMT) is carried out through Sentaurus Device Simulation, measurement, and physical analyses. A trade study of devices with four various geometries are evaluated for DC and RF performance. The trade-off of DC I-V characteristics, transconductance, and RF parameters versus hot carrier induced gate current is assessed for each device. Ambient temperature variation is also evaluated to observe its impact on hot carrier effects.

A commercial grade PHEMT is then evaluated and measured to demonstrate the performance degradation that occurs after a period of operation in an accelerated stress regime—one hour of high drain voltage, low drain current stress. This stress regime and normal operation regime are then modeled through Sentaurus. Output characteristics are shown along with stress mechanisms within the device.

Lastly, a means of simulating a PHEMT post-stress is introduced. The approach taken accounts for the activation of dopants near the channel. Post-stress simulation results of DC and RF performance are then investigated.

To my family

ACKNOWLEDGMENTS

First and foremost, I would like to express my sincerest gratitude to my advisor, Dr. Jiann-Shiun Yuan for his unswerving support and guidance throughout my undergraduate and graduate career. Since, 2008, Dr. Yuan's intuition, knowledge, and friendship to me has helped foster my talent and passion as an engineer and researcher. I will bring my experiences with him everyday into my professional and academic endeavors, and throughout life.

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LIST OF ACRONYMS

PHEMT	Pseudomorphic High Electron Mobility Transistor
RF	Radio Frequency
MESFET	Metal Semiconductor Field Effect Transistor
2DEG	Two-Dimensional Electron Gas
TCAD	Technology Computer Aided Design
MSG	Maximum Stable Gain
MAG	Maximum Available Gain
MMIC	Monolithic Microwave Integrated Circuit

CHAPTER 1: INTRODUCTION

The Pseudomorphic High Electron Mobility Transistor (PHEMT) has established itself as a high performance transistor for today's wireless handsets and military RF (Radio Frequency) communication systems. The inherent structure of the PHEMT permits low noise, low on-resistance, high power, and high frequency operation [1].

The reliability of the PHEMT is a subject matter that has been studied by several authors, [2-9] and continues to be important due to the high demands of military and commercial applications for low power consumption, high efficiency and superb performance, for the duration of the use of these devices. It is therefore important to understand the physical mechanisms involved behind the reliability of PHEMT devices.

It is within the scope of this work to cover reliability from various stand points. Two popular methods of evaluating reliability include high temperature and high electrical stress, including temperatures up to 150 degrees Celsius as well as large DC biases and large RF signals. The purpose of this work is to expose the physical behavior and output characteristics of stress, through device modeling of arbitrarily designed PHEMT devices, and observe the behavior from a reliability point of view.

The stresses that will be analyzed will correlate to various DC bias points. Output characteristics will be observed in terms of DC voltages and currents. In order to investigate the physical behavior, cross sections of the PHEMT at corresponding DC bias points and temperatures will be observed, through Sentaurus TCAD (Technology Computer Aided Design). Furthermore, RF parameters, including small signal parameters (S-parameters), will be measured against reliability. Mechanisms for reliability will be analyzed and assessed throughout.

Motivation

To reiterate, the goal of this work is to analyze and evaluate the PHEMT for DC and RF performance and for reliability. Using an understanding of reliability from several sources [1-9], a unified study on the reliability of the PHEMT is put forth. Specifically, reliability will be assessed in terms of DC stress only, not large signal RF stress. More so, it is highly important to observe the physical stress mechanisms within the PHEMT to help one assess its true reliability.

Method of Analysis

TCAD device simulation, mixed-mode simulation, and measurements are carried out in this study. Simulations and measurements separately provide quantitative, definitive results. Correlating measurements to simulation are done on a relative scale (without exact matching).

The following methodology is takes place throughout this work: Chapter 2 introduces the PHEMT and its basics; Chapter 3 addresses the reliability concerns of the PHEMT; Chapter 4 describes the simulation of the PHEMT through Sentaurus TCAD, and showcases the physical mechanisms involved in hot carrier reliability, including ambient temperature effects, as well; Chapter 5 introduces a trade-study of several devices to show how geometry changes can affect DC and RF performance and reliability; Chapter 6 describes and analyzes an experiment used to show the effects of DC stress on a PHEMT's DC characteristics and RF characteristics. A simulation is then performed to exhibit what a stressed device may observe versus and device operating in so-called "normal" mode; In Chapter 7, a simulation of post-stress is introduced. This is based on the physical outputs observed from a stressed PHEMT, consistent with the measurements found in Chapter 6 as well as other groups' findings. Chapter 8 summarizes the work and suggests future work for this topic.

CHAPTER 2: PHEMT BASICS

In order to gain an understanding, a brief review of PHEMT device physics and operation is presented here. The strength of a PHEMT is its "high electron mobility." While high doping provides high amounts of carriers, it also causes plenty of scattering/friction forces, thus offsetting the increase of mobility. The PHEMT solves the problem of MESFETS (Metal Semiconductor Field Effect Transistor) (plagued by high doping effects) by introducing a high electron concentration in the channel without high dopants. The result is little scattering/friction along with high mobility.

Gate control is achieved through a shottky barrier, interfacing with the epitaxial structure of the PHEMT (similar to a MESFET). This metal-semiconductor contact produces a depletion region which extends deep into the device to a point that is determined by the doping, the depth between the shottky interface and the channel, and the gate bias. Designing accordingly produces a desired threshold voltage.

Drain and source contacts are made through high doping of silicon or other dopants. Note, that in the TCAD simulations used in this study the metal contacts extend deep into the channel, only to permit ohmic contact (see Chapter 4).

Other characteristics include a passivation layer using an oxide such as Si_3N_4, and a substrate and spacer material. In the case of this study, GaAs is the substrate material and AlGaAs is the spacer material.

Device Structure

Figure 1 shows a basic PHEMT structure. It is comprised of a GaAs susbtrate, an InGaAs channel, AlGaAs setback (undoped) and spacer (doped) layer, and GaAs cap/access region layer. It is passivated with Si3N4. The doping of each layer, shown is consistent with the TCAD simulations introduced in Chapter 4.

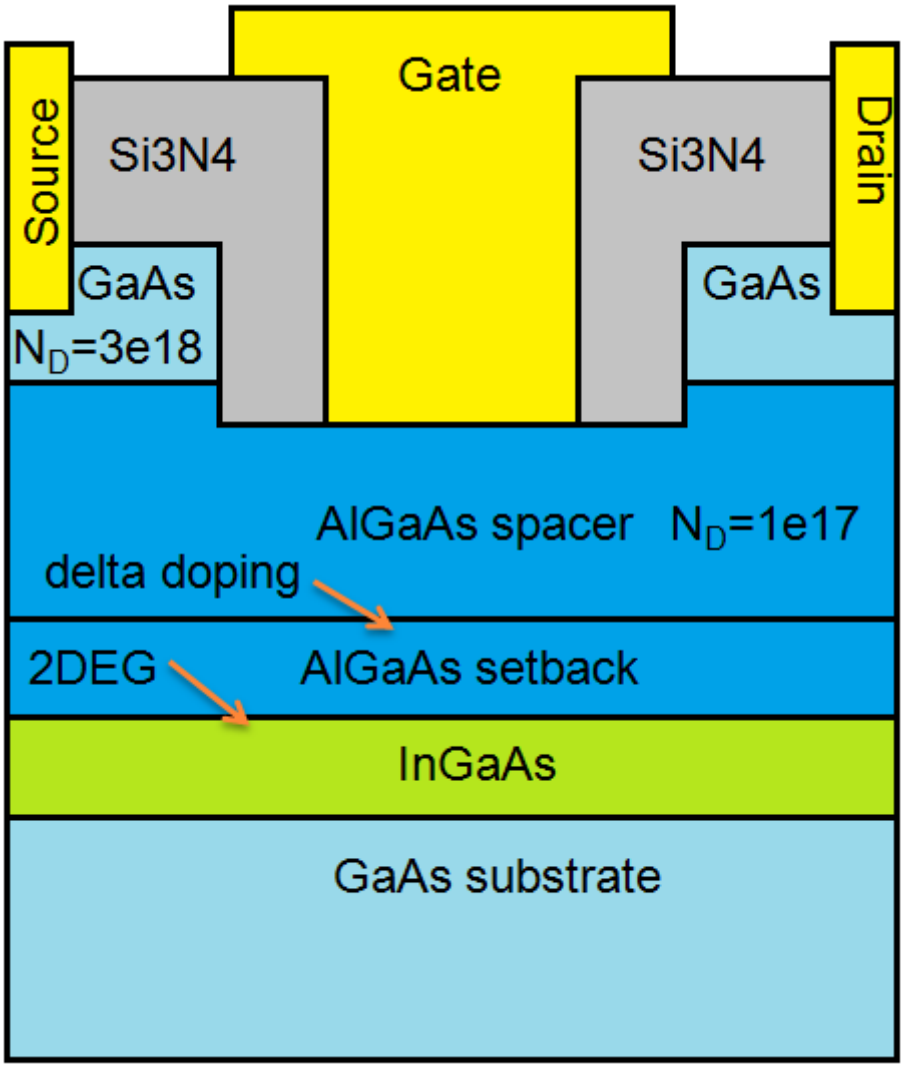


Figure 1: Basic PHEMT structure

Notice that the structure of Figure 1 is symmetrical. This is not always the case, but throughout this study will be evaluated in such a manner. Particularly, during the trade-study of devices (Chapter 5), each geometry change will be a symmetrical one.

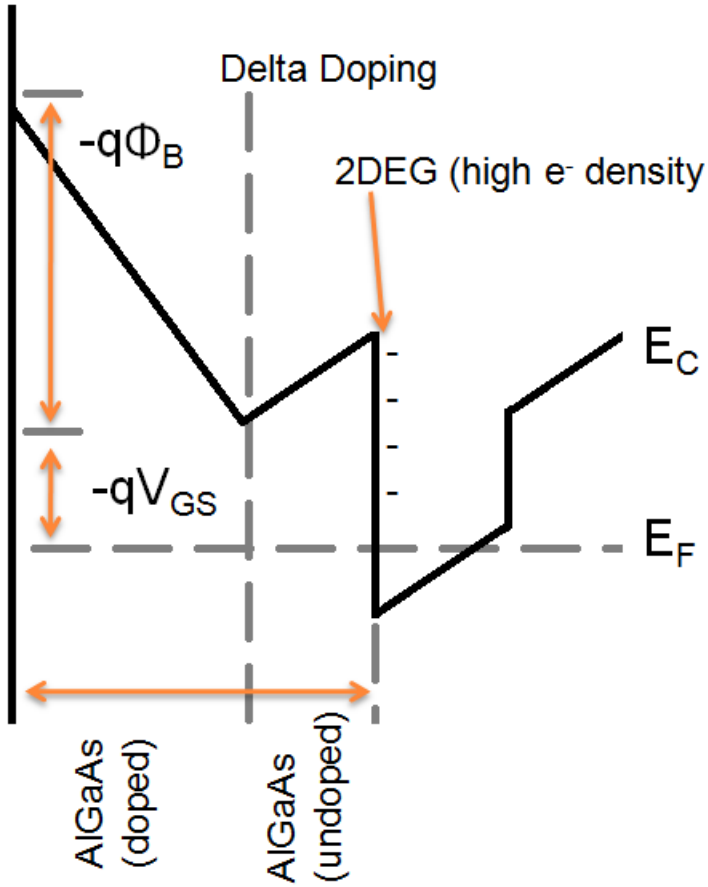


Figure 2: Bandgap diagram of PHEMT

Figure 2 above shows the bandgap diagram associated with the materials implemented in a PHEMT, from the metal gate (leftmost side) to the GaAs substrate (rightmost side). Based on this structure, a heterojunction is formed between the AlGaAs (undoped) layer and the InGaAs layer, which forms a two-dimensional electron gas (2DEG). This 2DEG is a layer of high electron concentration and no doping (ideally). The lattice mismatch between InGaAs and AlGaAs, in fact creates a higher density of electrons for a given space [1].

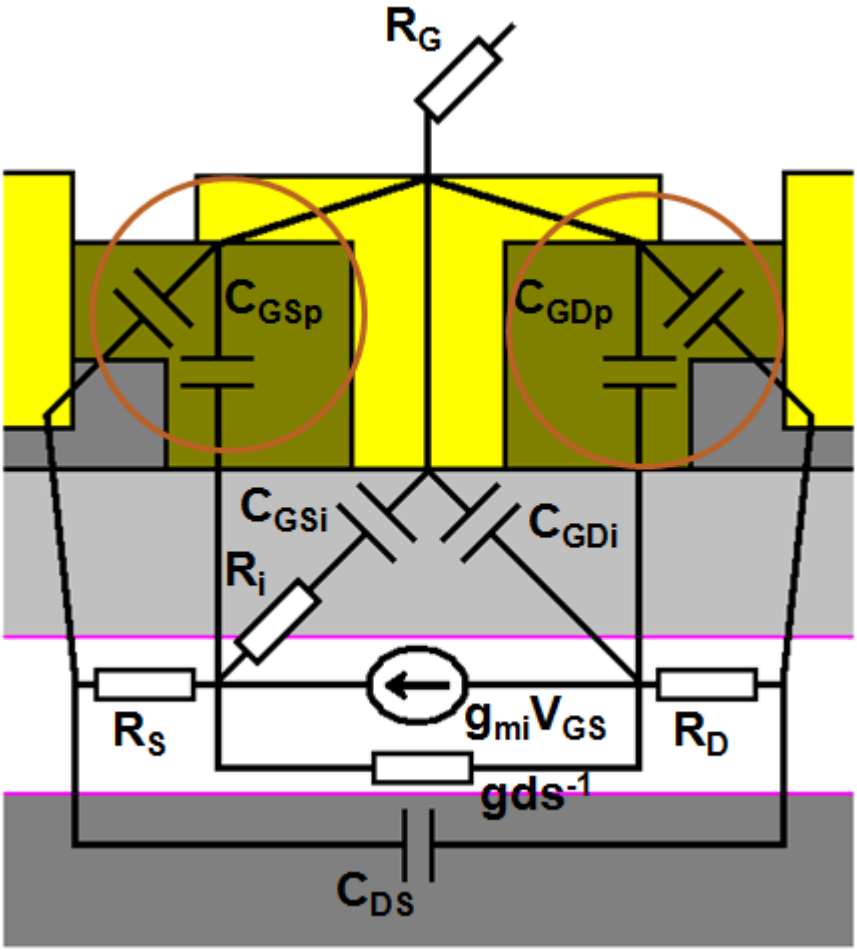


Figure 3: Large signal equivalent circuit

The PHEMT is not a perfect transistor, however. Figure 3 above shows the large signal equivalent circuit of the PHEMT. Parasitics exist that may degrade DC and high frequency performance. From [1], the effect of the parasitics are shown in Equations (2.1)-(2.5).

$$C_{GS} = C_{GSi} + C_{GSp} \tag{2.1}$$

$$C_{GD} = C_{GDi} + C_{GDp} \tag{2.2}$$

$$f_T = g_{mi}/[2\pi(C_{GS} + C_{GD})] \tag{2.3}$$

$$f_{max} = f_T[4g_{ds}(R_S + R_i + R_G) + 2(C_{GD}/C_{GS})((C_{GD}/C_{GS}) + g_{mi}(R_S + R_i))]^{1/2} \quad (2.4)$$

$$g_m = g_{mi}/(1 + R_S g_{mi}) \quad (2.5)$$

Through a device trade study in the following sections, one will observe the effect of geometry changes, as well as biasing conditions of the PHEMT. For example, as oxide/passivation size changes, capacitance *could* increase, resulting in a decrease of f_T. In general, to achieve high universal performance, each of the aforementioned parasitics should be reduced (except for g_{mi}—the intrinsic transconductance of the device).

CHAPTER 3: RELIABILITY CONCERNS OF THE PHEMT

Due to the nature of the PHEMT structure, reliability concerns exist in terms of long term and short term repeatable performance. The PHEMT suffers from several well known "flaws" in its design. This includes the following. (1) InGaAs's small bandgap. This induces the first point of breakdown in the devices; (2) The AlGaAs spacer layer. This material is prone to DX traps which have been known to degrade DC performance and cause threshold voltage, V_T, shifts [1-8]; (3) The shottky interface: If an oxide is present in between the gate metal and AlGaAs spacer layer, charges may become trapped, causing V_T shifts as well [2]. Additionally, metal interdiffusion (or gate metal sinking) may also occur if stressed to long.

The first aspect, the InGaAs channel's small bandgap raises the most concern, as this is the starting point of impact ionization. Impact ionization is caused by high electric fields that induce electron-hole pairs to be created which in turn create more electron hole pairs (an exponentially increasing process).

Impact ionization is essentially the dominant mechanism behind the reliability of a PHEMT. This is due to the following: high sudden amounts of current, as well as expected (or unexpected) higher power dissipation, which may burn out a device.

The high sudden amount of current merits discussion and has been the scope of many a researcher's work [2-8]. This current arises from impact ionization due to a high drain voltage. The becomes composed with what has become known as "hot carriers," "hot electrons," or "hot holes". The hot carriers are the "offspring" of impact ionization and are cause for several types of degradation mechanisms, including the following: Gate current, negative charge removal (hole trapping in DX centers or hole compensation) in the AlGaAs spacer layer, trapping in the

passivation layer, and charge trapping at the interface of the gate shottky barrier and possible activation of planar dopants [5]. The last two have scantily been reported by other work. The rest have become well known mechanisms for degradation.

Temperature reliability also raises another concern. A high temperature environment is known to degrade performance of electrical components in general, and immediately. The PHEMT fairs no differently. In this study, temperature is observed through self-heating and by adjusting the ambient temperature of the device in simulation. Its effect on DC stress is observed. It will be shown that higher temperatures in fact cause less hot carrier DC stress (whether it is due to self-heating or ambient temperature changes).

Effects of Stress

Several authors have evaluated the reliability of the PHEMT through various stress techniques. This section briefly describes and reports the results observed by them.

Depending on the specific type of PHEMT, bias points, and stress endured (along with the duration of the stress), hot carrier degradation can cause varying effects. This includes a negative shift in V_T [2,5,7,8], a negative (horizontal) shift of the transconductance (g_m) bell curve [2,5,8], a negative (vertical) peak shift of the g_m bell curve [3,4], and a drain current increase [2,5,7,8].

On the other hand, a drain current decrease has also been reported [3-6], as well as an increase of the peak transconductance [7]. Canali et. al, even reports a device that shows no significant change whatsoever post stress (for their given stress condition) [7].

In this work, DC stress measurements are carried out and reported. They are consistent with some of the aforementioned authors' findings [2,5,7,8]. Specifically, after a period of stress,

in high drain voltage (V_{DS}) low drain current (I_{DS}) (relative to normal operation), drain current is found to increase while S21 (small-signal gain) decreases, once the bias is returned back to the normal mode bias points (the initial pre-stress gate and drain voltages).

CHAPTER 4: EVALUATING THE PHEMT THROUGH TCAD

Taking into account the reliability concerns addressed in the previous section, it is the scope of this work to evaluate the mechanisms involved in reliability. Through TCAD device simulation one can observe the following: impact ionization, hole current density, electron current density, and lattice temperature. These are the four essential mechanisms when evaluating expected reliability within a device and will be assessed in detail.

Figure 4 shows the basic PHEMT structure used and simulated throughout this study. As can be seen, it contains all of the basic properties of the PHEMT, as shown in Figure 1, and possesses the same bandgap properties of Figure 2. The doping and mole fractions are listed. Note that just above the InGaAs channel, the AlGaAs layer is undoped—this is the setback layer and permits high mobility with little to no scattering effects from impurity dopants.

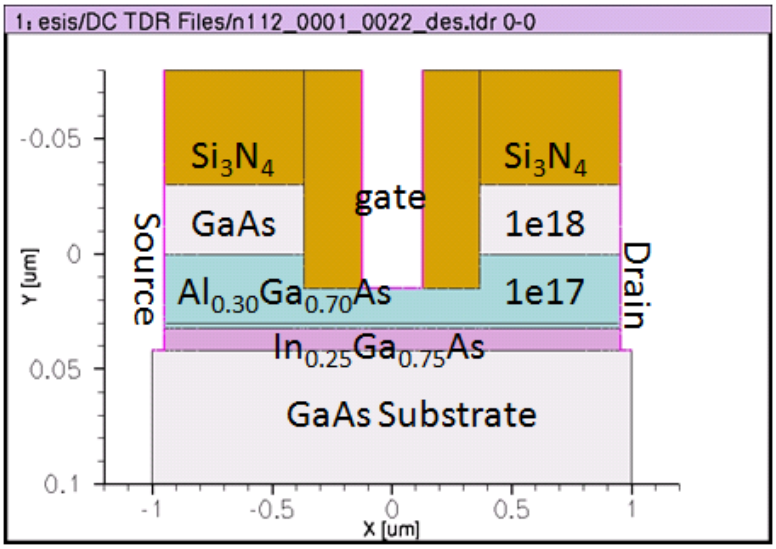


Figure 4: PHEMT structure from TCAD

Characterization of the PHEMT in TCAD

In order to evaluate the PHEMT under DC conditions, Sentaurus Workbench permits a DC simulation. This includes I_{DS} vs. V_{GS}, used to obtain V_T for a given V_{DS} and a curve trace to

see a family of curves for I_{DS} vs. V_{DS}. Table 1 shows a list of the DC characteristics, including R_{on}, and two V_T for this single PHEMT device.

Table 1: Extracted DC values for a PHEMT from Sentaurus Workbench

V_{Tgm} (V)	V_{Ti} (V)	RDSON (ohms)
-0.944 (VD=1.5 V)	-1.093 (VD=1.5 V)	0.056
-0.983 (VD=3 V)	-1.212 (VD=3 V)	--

The device in Figure 4 was designed arbitrarily to achieve the shown threshold voltages. This was done through adjusting the depletion layer width of the shottky barrier, by choosing appropriate spacer doping and depth (between the gate and the InGaAs layer).

Equations (4.1)-(4.4) describes the basic operation for a MESFET, which behaves identically to the PHEMT, where μ_n is the mobility of the channel, C_S is the capacitance of the metal-semiconductor depletion region (similar to an oxide in a metal-oxide-semiconductor), W is the width of the device, V_{GS} is the gate-source voltage applied to the gate, V_{OFF} is the turn-off gate voltage, L is the channel length, V_{bi} is the built in potential of the shottky metal-semiconductor interface (usually around 0.9V), V_{po} is the pinchoff voltage of the channel, ΔE_c is the conduction band energy, q is the elemental electron charge. N_D is the doping (of the AlGaAs layer in this case) and d is the vertical distance from the gate to the channel. Notice that V_{OFF} is dependent on both the spacing and doping of the AlGaAs layer. These equations will later help describe the physical change that occurs within a PHEMT after stress.

$$I_D = \mu_n C_S W (V_{GS} - V_{OFF})^2 / 2L \tag{4.1}$$

$$g_m = \mu_n C_S W (V_{GS} - V_{OFF})^1 / L \tag{4.2}$$

$$V_{OFF} = V_{bi} - V_{po} - (\Delta E_c / q) \tag{4.3}$$

$$V_{po} = qN_D d^2/2\varepsilon_r\varepsilon_0 \quad (4.4)$$

Simulations of the PHEMT

The type of simulations that are performed for the single PHEMT include the following: DC curve trace (varying V_{GS} and ramping V_{DS} to observe the drain current) and a DC curve trace (same as above) with increasing temperatures. In the next section, multiple devices with varying geometries will be evaluated and compared to showcase impact ionization and hot carrier effects for similar biasings.

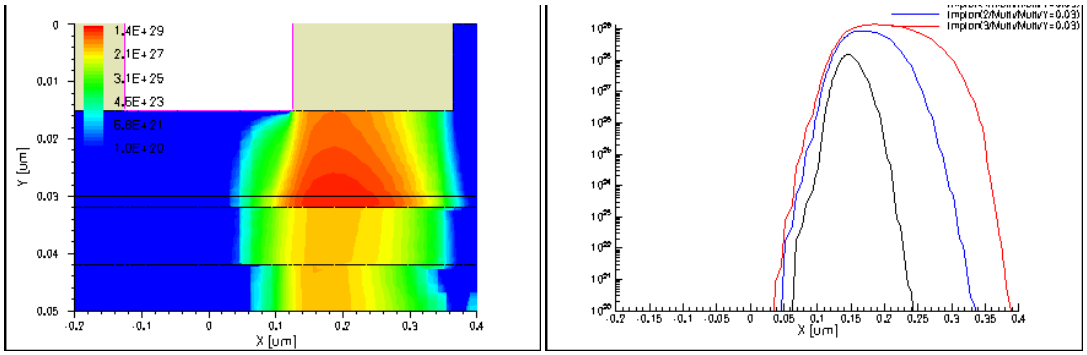
RF performance for each of the devices at a similar drain voltage (6 volts) while sweeping V_{GS}, will be evaluated through observing s-parameters, maximum stable gain (MSG), and maximum available gain (MAG). They will each be correlated to varying hot carrier effects for each bias point. This will introduce figure of merits based on gate (hole) current vs. MAG and MSG.

These figures of merit could prove useful for device engineers and monolithic microwave integrated circuit (MMIC) designers, giving them a reliability measure, such as hot carriers versus immediate performance measure (S21, MSG, and/or MAG).

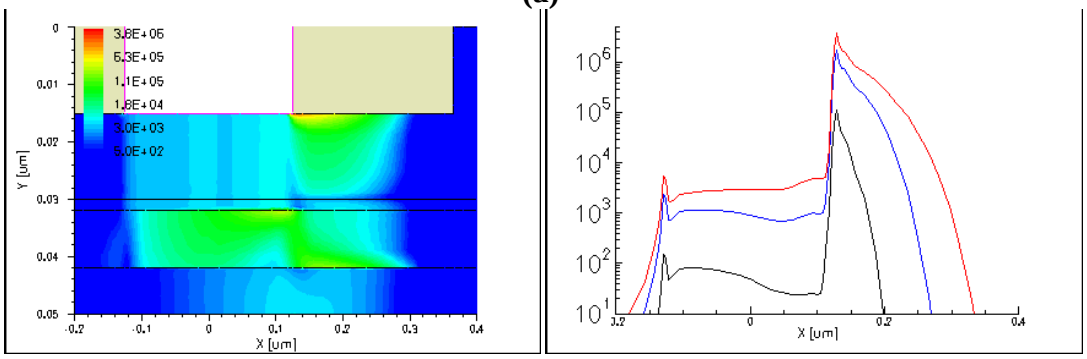
Increasing Drain Voltage Stress for a Given Gate Voltage

To first evaluate hot carrier stress on a PHEMT, a simple drain voltage sweep is performed for a set gate voltage. It is well known that as drain voltage increase, electric field within the device increases and causes impact ionization. This is the process where secondary electrons and holes gain enough energy to become free and in turn collide with other electron hole pairs, freeing even more electrons and holes. Figure 5 showcases this effect for an increase of drain-source voltages for 3, 6 and 9 volts at a gate-source bias of -0.8 volts. A cross section of

the device is shown at 9 volts (left) while the cutline to the right is shown to the right for each drain voltage (3 ,6 ,9)—for each case, as drain voltage increases, so does the height of the cutlines.



(a)



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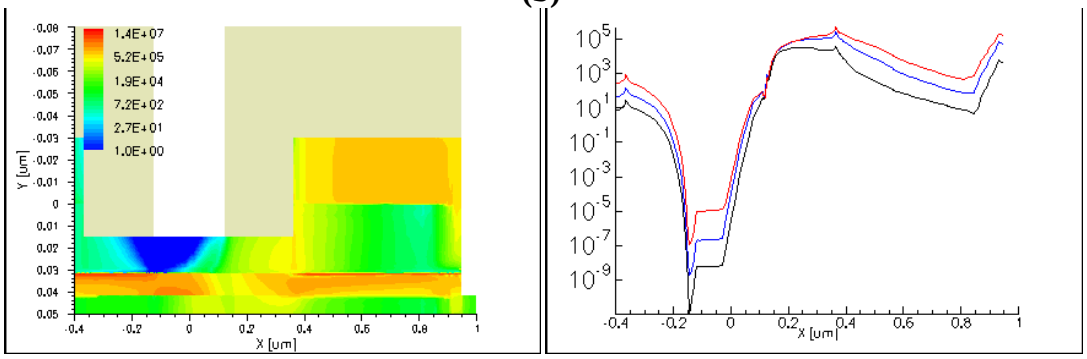

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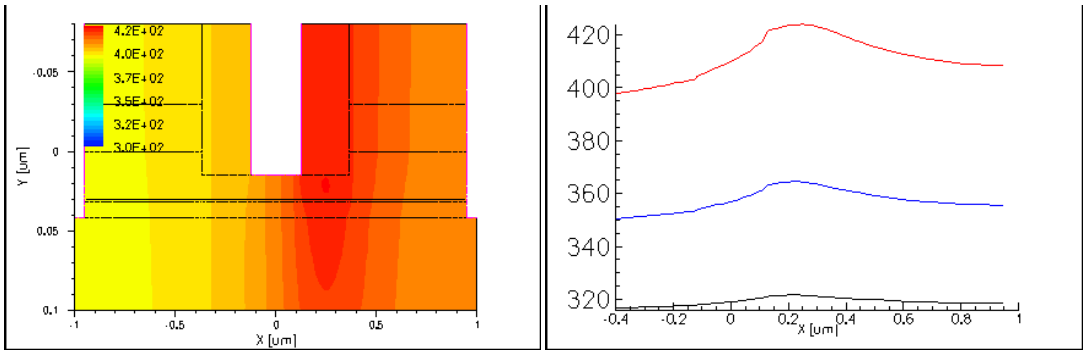


(d)

Figure 5: Increasing drain voltage stress (V_{DS} = 3 ,6 ,9 V) for a given gate bias (V_{GS} = -0.8 V) showing (a) impact ionization, (b) hole current density, (c) electron current density, (d) lattice temperature.

These plots showcase the physical mechanisms involved that determine reliability. Notice that as impact ionization increases, so does hole current (flowing towards the gate), electron current (flowing upwards and rightwards toward the drain). Recall the discussions of Chapter 3. As hole current increases, more DX traps become compensated by holes, causing V_T shifts. Electrons become trapped in the passivation, shifting current behavior and performance. Also, lattice temperature increases. If the drain voltage is set to high, these "hot carriers" can exponentially increase and burn out the device.

Ambient Temperature Effects

Any electronic device may become exposed to temperatures other than room temperature, such as in harsh fluctuating space environments, seen by satellites. It is the purpose of this work to observe what occurs within a PHEMT for a given bias, at various ambient temperatures, from a reliability point of view.

Figure 6 shows the I-V characteristics of the PHEMT of Figure 4 for various temperatures (300K, 350K, and 400K). As the device becomes more "on" (V_{GS} increases), the

saturation current begins to decrease for a given temperature. Additionally, impact ionization decreases, causing less hot carriers, including gate hole current.

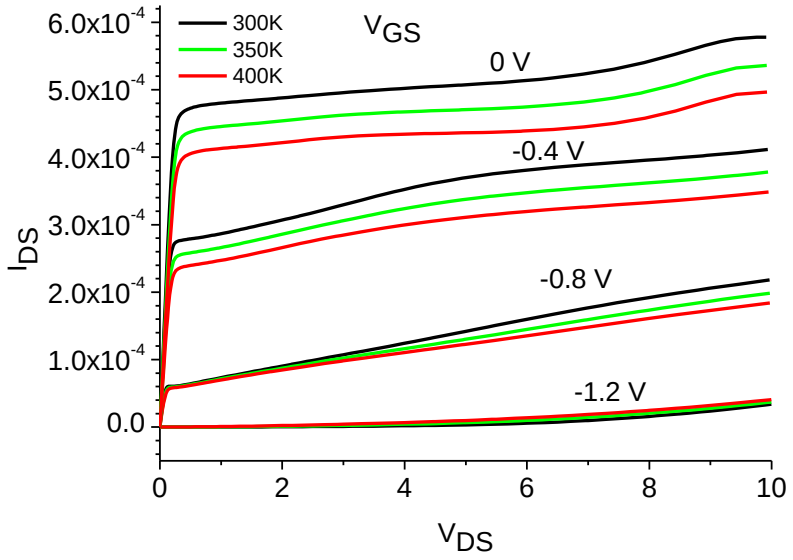
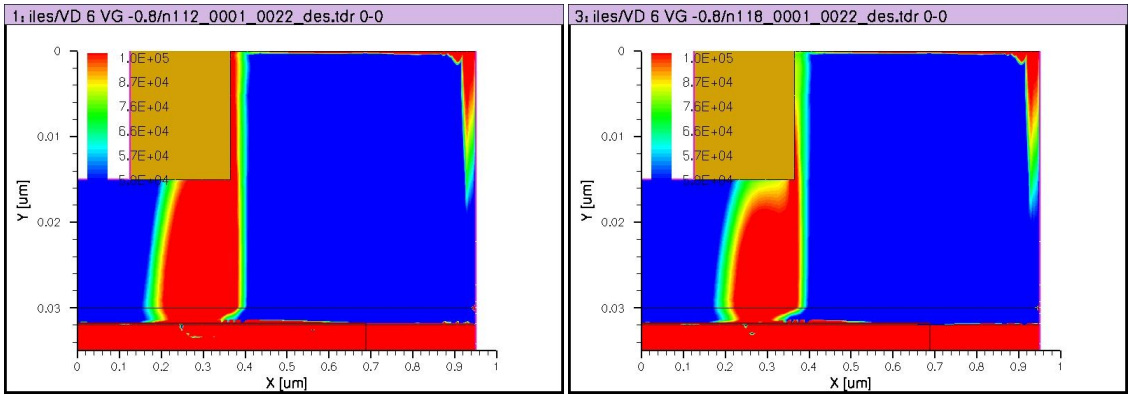


Figure 6: Ambient temperature effects on DC characteristics

Figure 7 below shows the corresponding device cross sections and stress mechanisms at 300K (left) and 400K (right) for V_{GS} = -0.8 V and V_{DS} = 6 V. Observe the decrease in electron current density, hole current density, and impact ionization. It can be said that DC stress at room temperatures provides worst-case conditions for hot-carrier reliability.



(a)

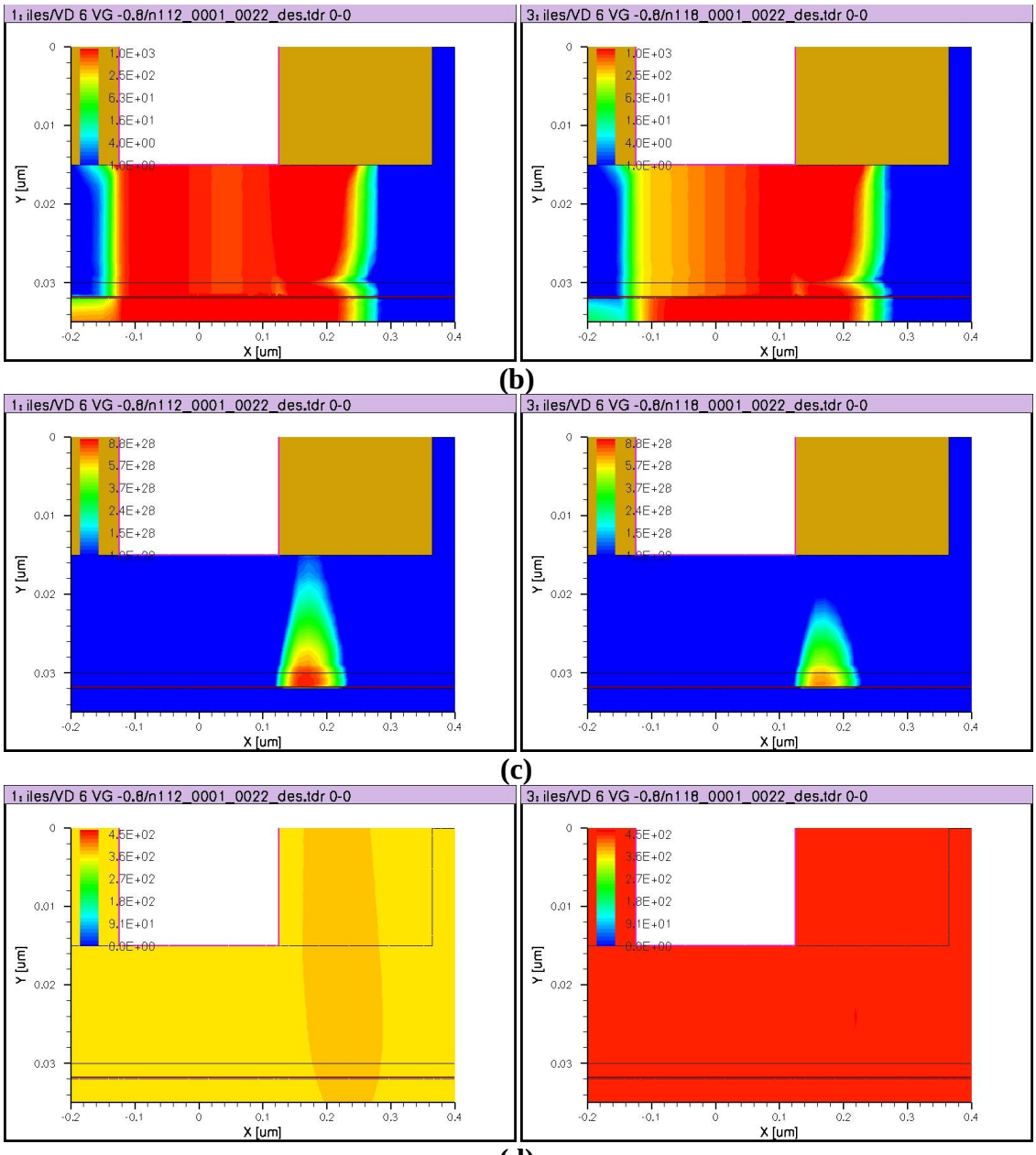


Figure 7: Corresponding cross sections for V_{GS} = -0.8 V and V_{DS} = 6 V at ambient temperatures of 300K (left) and 400K (right) showing (a) electron current density, (b) hole current density, (c) impact ionization, and (d) lattice temperature.

CHAPTER 5: DEVICE TRADE STUDY

After observing the physical mechanisms of a single device, it is the scope of this work to assess and attempt to improve the reliability of the PHEMT by adjusting its geometric properties. Figure 8 shows a PHEMT and indicates the device geometry change taking place. Table 2 describes each of the TCAD structures that are implemented in this study.

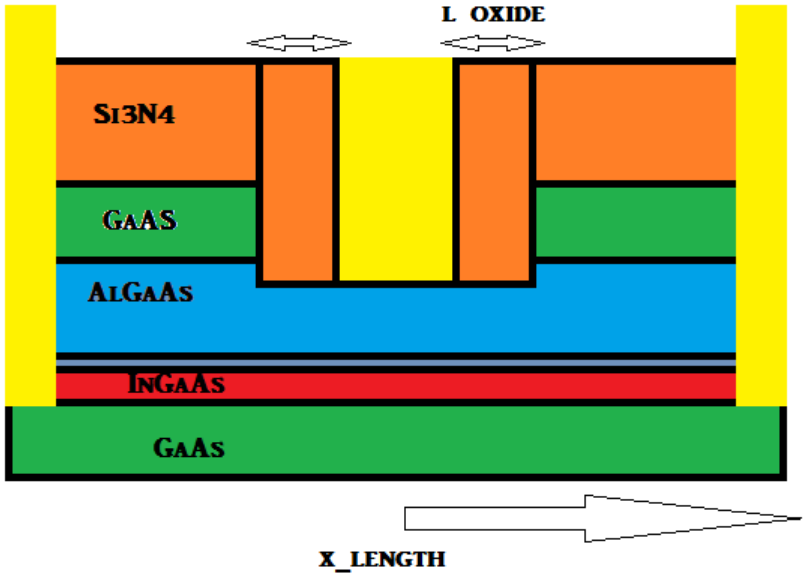


Figure 8: PHEMT adjusted for trade-study

Table 2: List of TCAD PHEMT structures

Device	L_oxide (µm)	X_length (µm)	Notes
D1	0.24	1.0	Base device
D2	0.44	1.2	L_Oxide increase with X_length increase
D3	0.24	0.8	X_Length decrease
D4	0.44	0.8	L_Oxide increase with X_length decrease

To evaluate reliability, the devices (D1 through D4) with different gate-drain lengths (cell pitches) and oxide/passivation lengths are simulated under DC operation. A certain geometry

will permit a higher "breakdown voltage" and therefore should handle higher drain voltage before breakdown, i.e. generation of secondary hole and electron current, or hot carriers. The goal of this work is not to improve breakdown voltage, but to observe how a "more reliable" device fairs under DC operation and RF operation versus a "less reliable" device. "Reliability" is analyzed in a vivid, qualitative manner and in a quantitative manner. Gate current will be used as a measure for evaluating hot carrier effects. Several authors have used gate current as a means for assessing breakdown in a device. Basically, a sudden increase of gate current (for a given V_{GS}) is an indication of impact ionization within a PHEMT device [3].

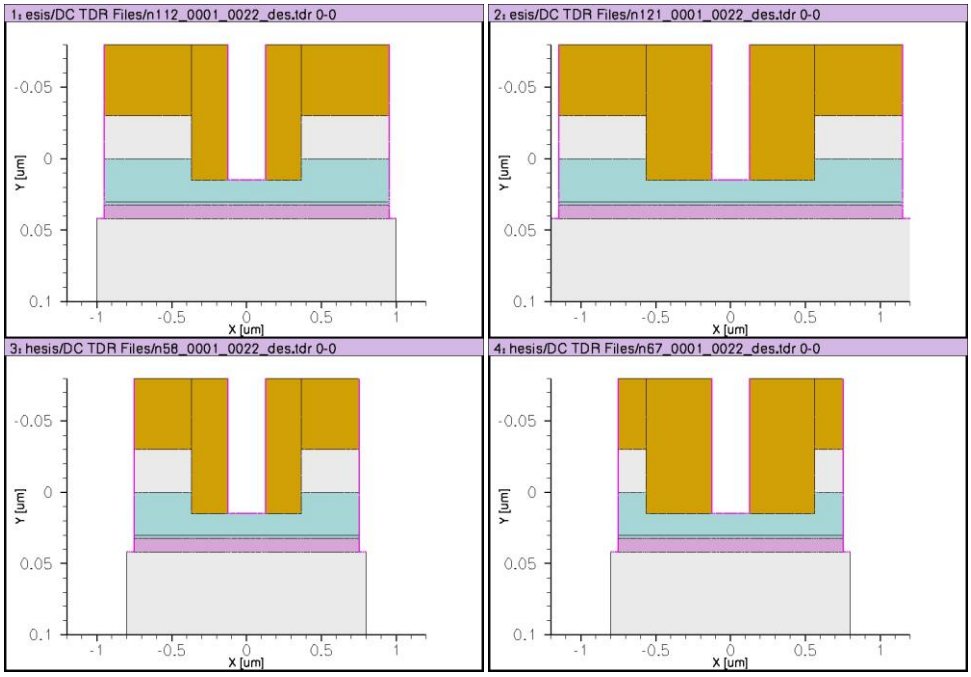


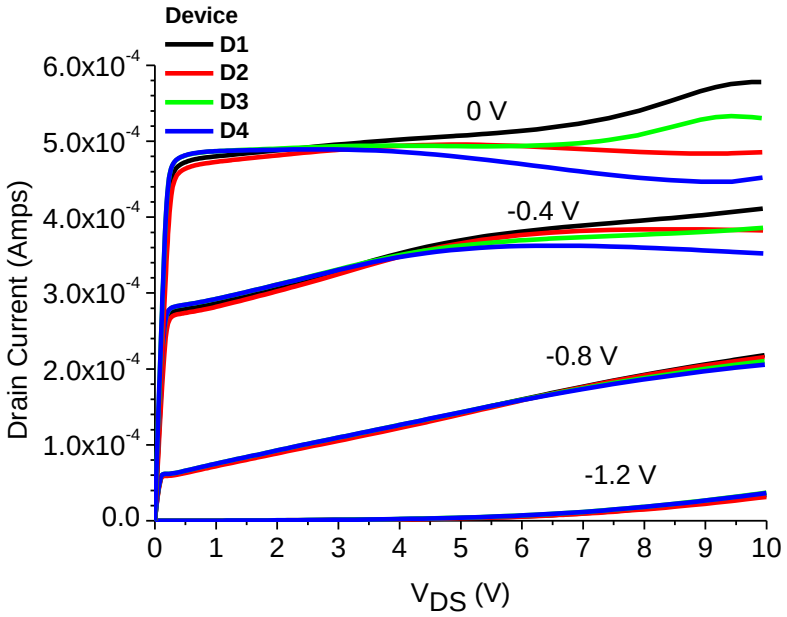
Figure 9: Devices D1, D2, D3, D4

Figure 9 shows the devices as simulated in Sentaurus. Notice the range in cell pitch and gate recess lengths (the depths remain the same). As used in Chapter 4, TCAD device cross sections will also be analyzed in the same manner so as to observe the distribution of hot holes, hot electrons, and impact ionization.

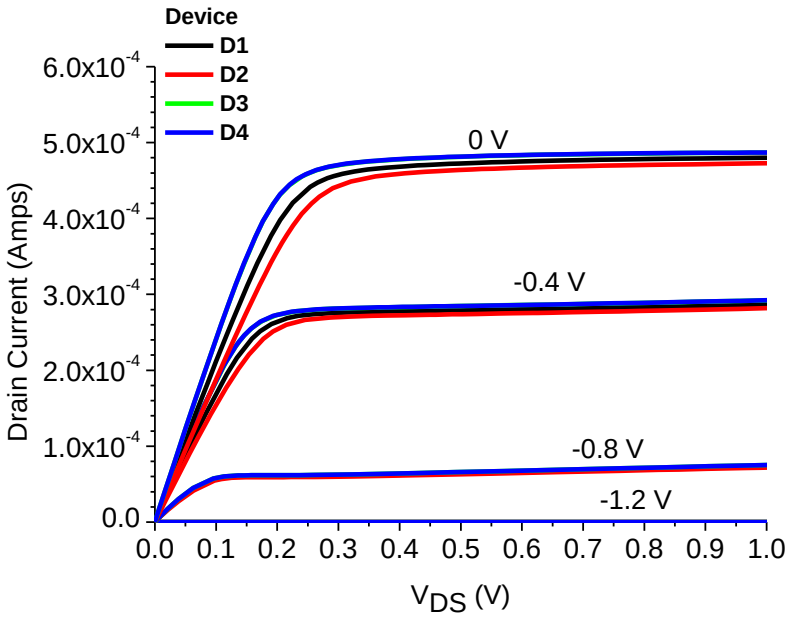
Observing Stress

While stress is not simulated in this section, a fair prediction of which type of device may fair better can be made, from a reliability stand point. A post-stress device will be simulated in Chapter 7 based on measurements observed in Chapter 6 and one group's observations and physical explanation [5].

The four devices of Figure 9, corresponding to Table 2, will each be evaluated for stress and DC and RF performance. Figure 10 shows the I-V curves for all of the devices. Observe the difference in current as well as corresponding on-resistance. The device with the largest cell-pitch also observes the highest on resistance (as shown in the linear region of Figure 10(b)).



(a)



(b)

Figure 10: I-V characteristics of devices D1, D2, D3, and D4 for VGS = -1.2V, -0.8V, -0.4V, and 0 V showing (a) the high drain voltage region where impact ionization occurs and (b) a zoomed in view of the linear resistive region.

Figure 11 shows I_{DS} , g_m, and I_{GS} vs. V_{GS} for all of the devices. Observe the difference in drain current (at higher gate voltages), peak transconductance, and peak hole current. It is easily observed that the device with the highest peak transconductance also possesses the highest peak gate current (the reason for the peak in the gate current will be explained later). Furthermore, this suggests that at high drain voltages, the impact ionization current could very well contribute to the transconductance of a device.

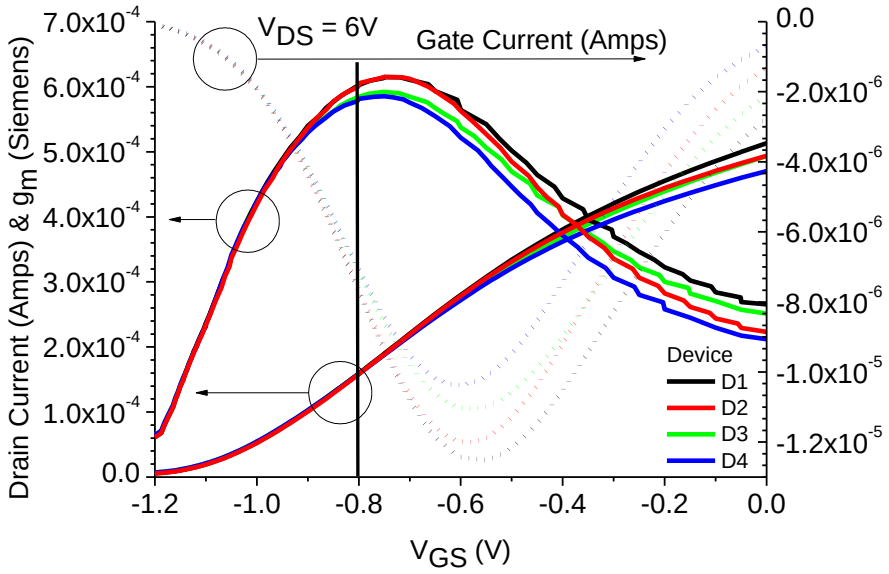


Figure 11: Drain current, gate current, and transconductance versus gate-source voltage for V_{DS} = 6 V

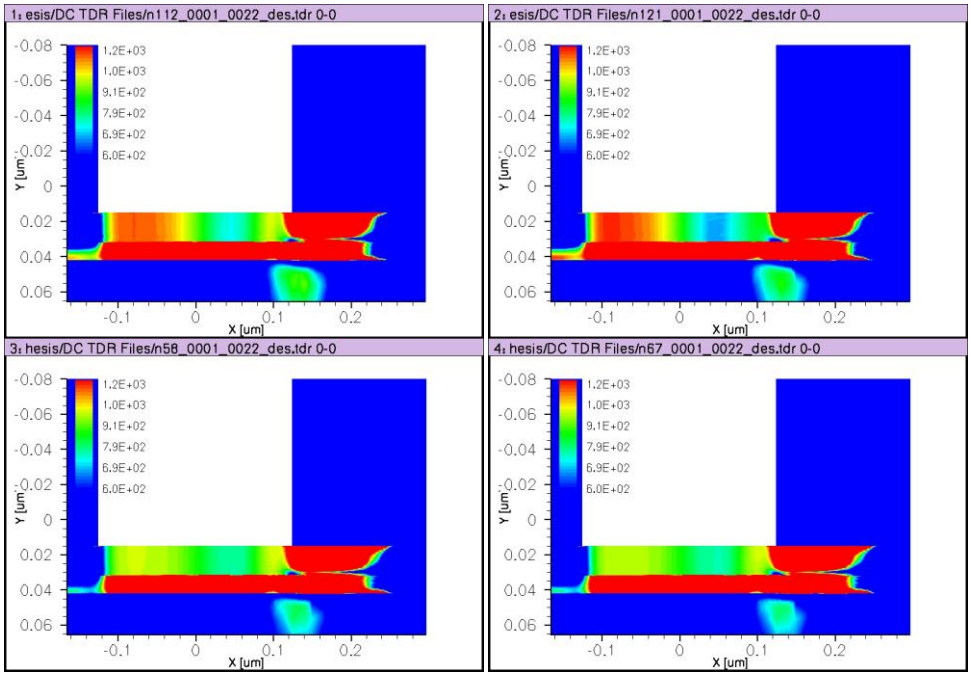


Figure 12: Devices D1, D2, D3, D4-hole current density

Figure 12 shows the hole current density for each of the devices. Notice that they correspond directly to the higher gate current as shown in Figure 11. This is the main

degradation mechanism that is responsible for the V_T shifts and g_m shifts, observed by authors and later in Chapter 6. A higher hole current density within the device would translate to higher expectation of a V_T shift during operation for a given bias. Due to the DX traps becoming compensated by holes.

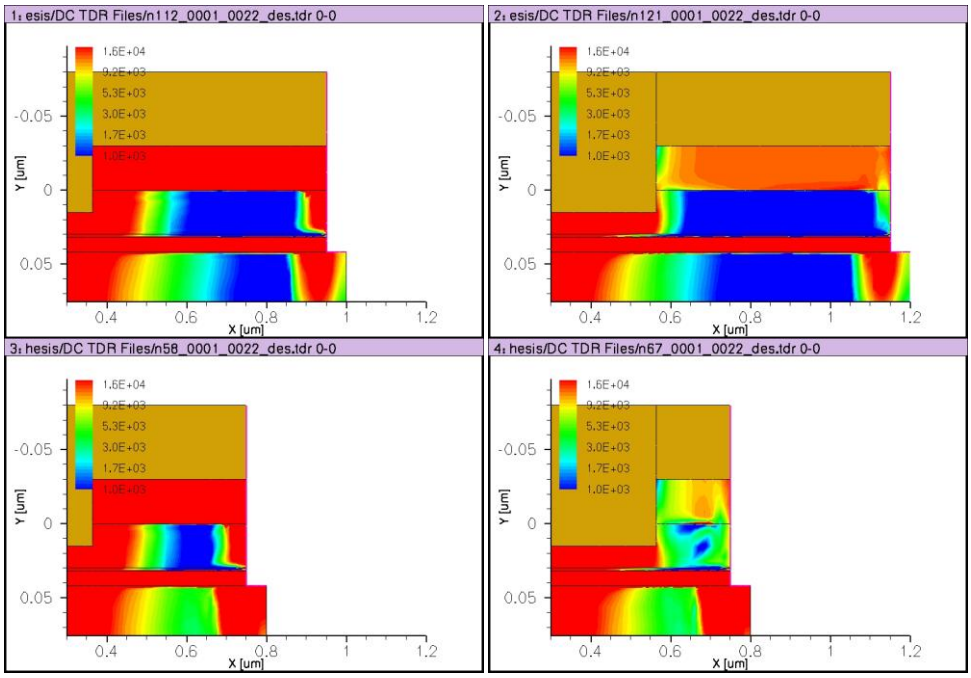


Figure 13: Devices D1, D2, D3, D4-electron current density

Figure 13 shows the electron current density, with focus on the gate-drain access region. Recall, that as electrons become trapped in this region, the electric field at the channel is decreased due to a shift of the electric field distribution. This is known as "breakdown walkout." It can be said that for a given bias and approximately the same drain current, the devices with higher electron density at the gate-drain access region would expect to see an increase in breakdown voltage throughout operating life. i.e. it is possible that the device will continue to degrade at a decreasing rate.

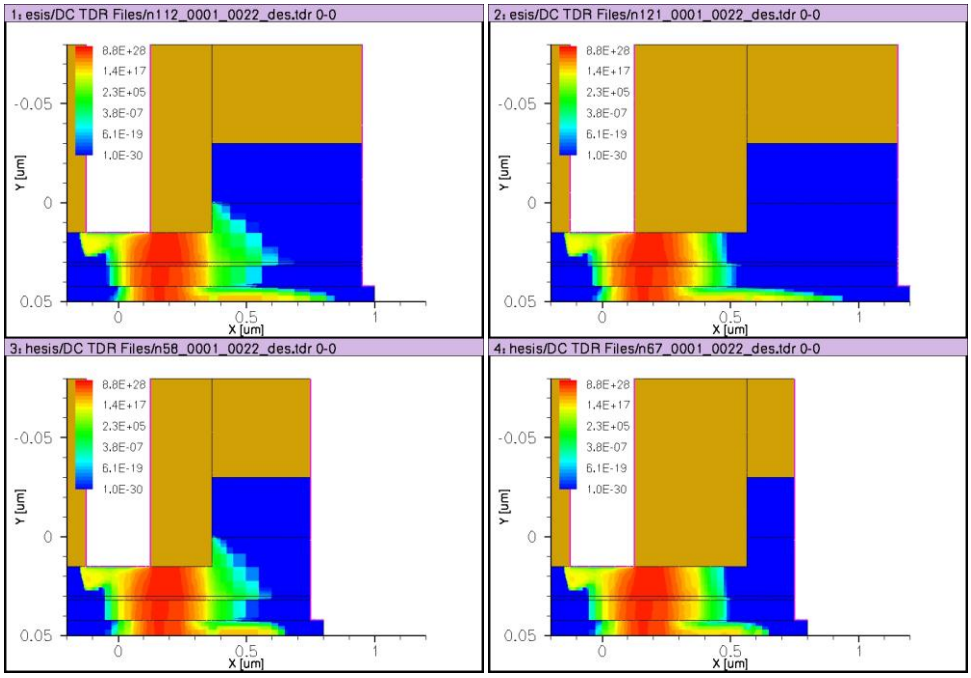


Figure 14: Devices D1, D2, D3, D4-impact ionization rate

Figure 14 shows the impact ionization rates for each device. This is the mechanism responsible for secondary holes and electrons, from which gate current rapidly increases and gate-drain access region adjacent electrons increase as well. Observe that the peak of impact ionization is occurring just at/near the InGaAs channel region. This is due to the high population of electrons as well as the relatively small bandgap of InGaAs.

Table 3 shows the peak impact ionization rates for each device. Notice the consistence in hole current as impact ionization increases. Impact ionization is directly dependent on the electric fields and electrostatic potentials within a device. It is shown that these are consistent as well.

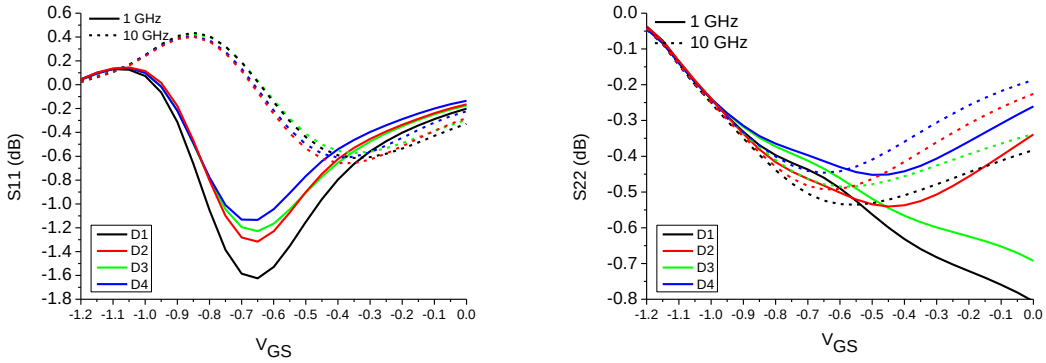
Table 3: Impact ionization values for each device

	D1	D2	D3	D4
Impact Ionization (cm^{-3}/s)	8.477×10^{28}	8.200×10^{28}	8.015×10^{28}	7.938×10^{28}
Electric Field (V/cm)	564123	561646	548088	546538
Electrostatic Potential (V)	3.61447	3.60027	3.5782	3.56938

RF and S-parameters

In this section, the trade-study is continued with a focus now on the RF parameters. The small signal RF performances of each device in this work are observed. This includes S21, MSG, MAG, f_T, and f_{max}.

Figure 15 shows the small signal gain, S21, of each of the devices for varying gate voltages, at a set drain voltage of 6 volts, and frequencies of 1 and 10 GHz. Observe the effect that frequency has on S21. D2, which shows a maximum gain at $V_{GS} = 0.7$ V for 1 GHz, degrades the most as frequency hits 10 GHz.



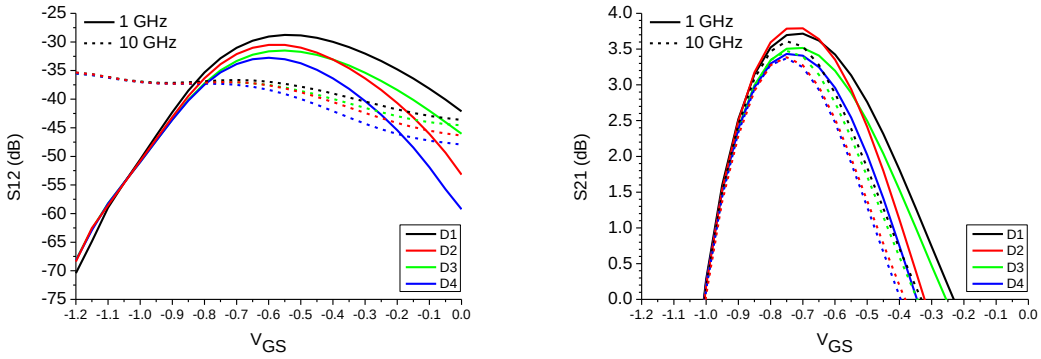
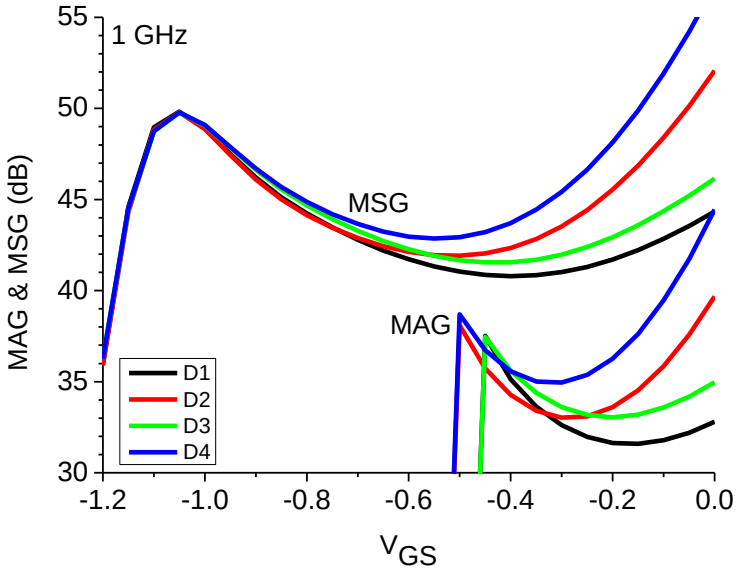
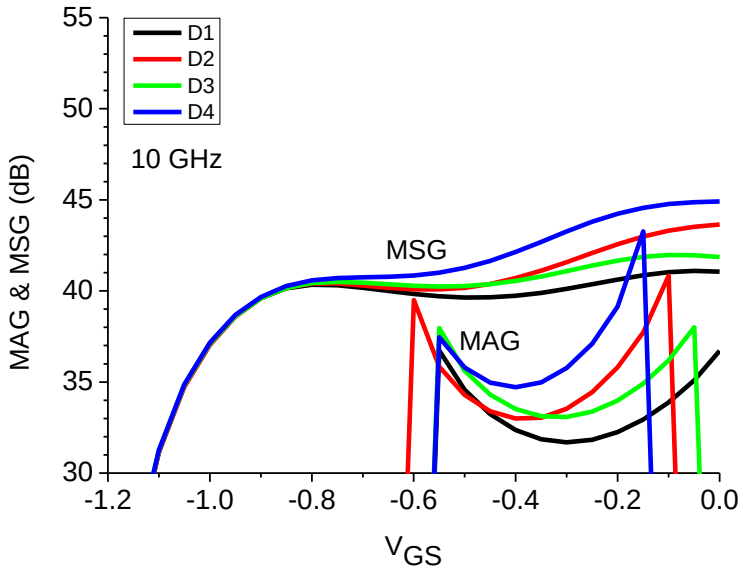


Figure 15: S-parameters of each device for 1 and 10 GHz at V_{DS} = 6 V

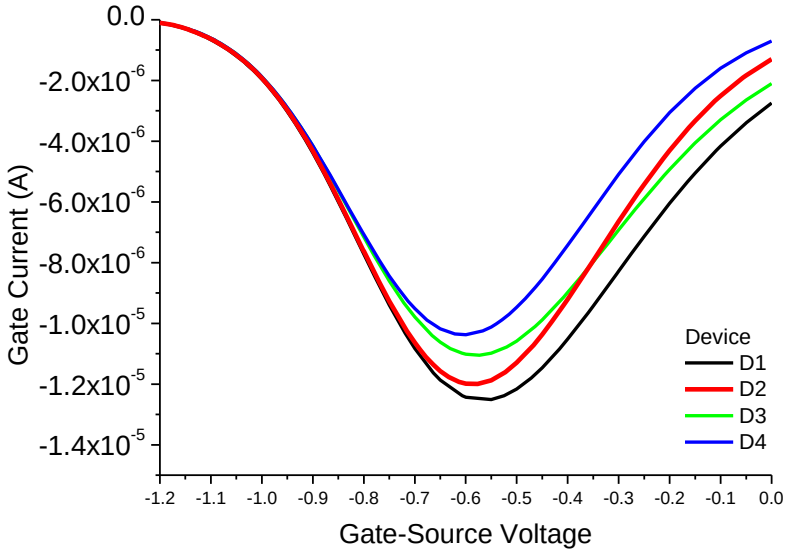
In an RF amplifier, whether it be a low noise amplifier or high power amplifier, high gain is a desirable characteristic. It is therefore worth evaluating the tradeoff between "high gain capability" and "reliability." Two important values to an RF amplifier designer include maximum available gain (MAG) and maximum stable gain (MSG). Figure 16 shows this for 1 and 10 GHz at V_{DS} = 6 V for a range of V_{GS}.



(a)



(b)



(c)

Figure 16: MAG and MSG at (a) 1 GHz and (b) 2GHz, and (c) corresponding DC gate current

Summary of Device Trade Study

One can deduce that the device (D1) with the highest hole current may not be as reliable (and consistent in performance) as the device with the lowest hole current (D4), for a large bias

range—due to DX traps and/or activation of planar dopants [5]. Furthermore, it is impressive to see that the most reliable device (D4) possesses highest maximum available gains (both MSG and MAG) at 1 GHz and 10 GHz, for the largest range of biasing. Table 4 summarizes the results of the trade study with a figure of merit for DC and RF characterization: $g_m/|I_{GS}|$, $MAG/|I_{GS}|$, $MSG/|I_{GS}|$. Choosing the bias point of V_{GS} = -0.6 V and V_{DS} = 6 V, each device observes it's maximum gate (hole) current. From this trade study, an MMIC or device designer, can equally weigh gate current against desired performance, and assess according. Also, it appears that to achieve a wide bias range of low hole current, one must have a higher ratio of gate recess (vertical) distance to cell pitch (horizontal) (see Figure 17) [1].

Table 4: Summary of trade study exhibiting g_m/I_{GS}, MAG/I_{GS}, and MSG/I_{GS} at peak gate current (V_{GS} = -0.6 V and V_{DS} = 6 V)

Freq.	-	-	-	1 GHz	1 GHz	10 GHz	10 GHz
Device	g_m (S)	I_{GS} max (Amperes)	$g_m/\|I_{GS}\|$ (S/Amperes)	$MAG/\|I_{GS}\|$ (dB/Amperes)	$MSG/\|I_{GS}\|$ (dB/Amperes)	$MAG/\|I_{GS}\|$ (dB/Amperes)	$MSG/\|I_{GS}\|$ (dB/Amperes)
D1	5.64E-04	-1.24E-05	4.54E+01	3.94E+06	4.95E+06	3.83E+06	4.85E+06
D2	5.62E-04	-1.20E-05	4.69E+01	4.97E+06	6.55E+06	5.05E+06	6.26E+06
D3	5.37E-04	-1.10E-05	4.88E+01	4.86E+06	6.07E+06	4.78E+06	5.94E+06
D4	5.22E-04	-1.04E-05	5.03E+01	6.87E+06	8.92E+06	7.03E+06	8.50E+06

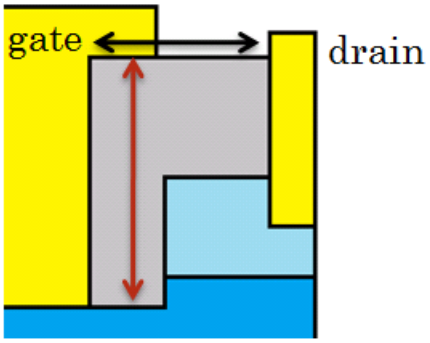


Figure 17: Geometry of the passivation layer of a PHEMT

CHAPTER 6: STRESS MEASUREMENT RESULTS AND ANALYSIS

In order to gain a true understating of hot carrier effects, it is worthwhile to investigate the results of stressing a commercial grade PHEMT, used for handsets etc. A PHEMT device with evaluation board (power matched for 1.85 GHz), was provided courtesy of RFMD. A one hour stress scheme was implemented to observe it effect on DC and RF performance. Table 5 describes the normal operation mode and the stress regime. A stress was introduced in the following way: high drain voltage and low drain current for one hour.

Table 5: Normal operation and stress mode for experiment

	V_{GG}	V_{DD}	I_{DD}
Operation mode	-0.43724 V	5.0568 V	423 mA
Stress mode	-0.9868 V	11.19 V	98 mA

Figure 18 shows the evaluation board and device along with the measurement equipment. A brass block was shaped and mounted underneath the PCB for heat dissipation. A Rohde & Schwarz vector network analyzer was used for s-parameter measurements. The DC bias is provided by two power supplies for both gate and drain voltages (DK Precision and HP, respectively). Voltages were monitored by an HP digital multimeter, while drain current was digitally monitored by the HP supply.

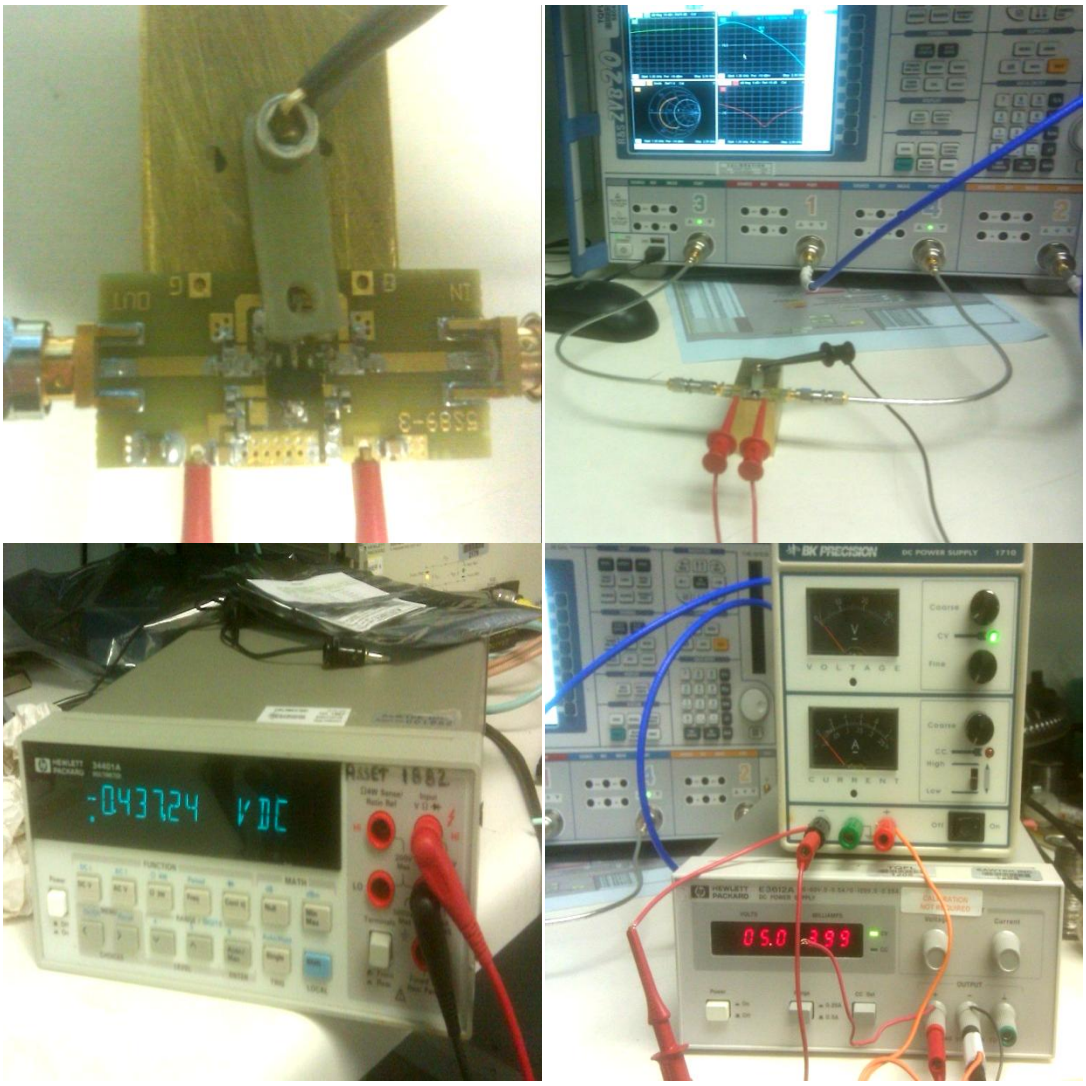


Figure 18: PHEMT evaluation board and measurement setup

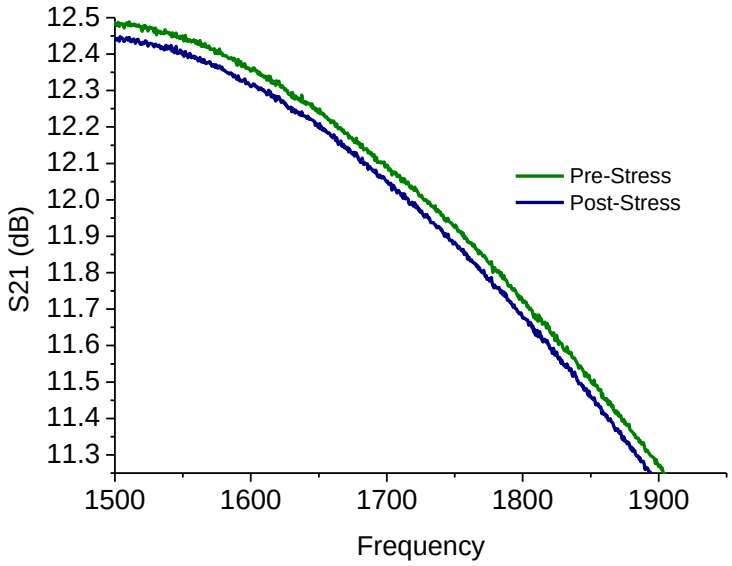
Table 6 shows the DC characteristics measured throughout the experiment—before, during, and after stress. Notice that after the stress begins, the drain current, slowly decreases. This can be attributed to the "breakdown walkout" effect from which hot electrons formed by impact ionization, enter the gate-drain access region oxide, causing a decrease in the peak electric field above the channel. The effect is that impact ionization is in fact decreasing with stress time.

Table 6: Log of stress measurement results – before, during and after stress

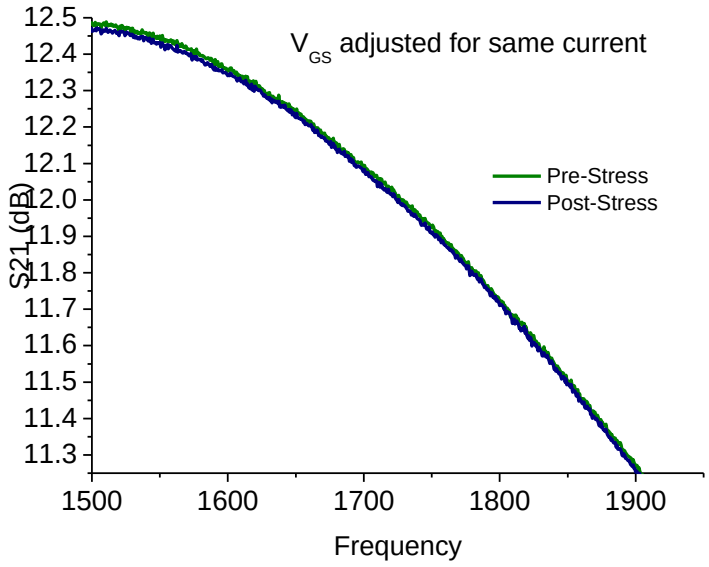
Time (p.m.)	V_{GG} (V)	V_{DD} (V)	I_{DD} (mA)	Notes
7:41	-0.4372	5.056	**399**	*Initial Test: operating point*
7:56	-0.4372	5.0565	**399**	*15 minute burn-in*
7:59	-0.9868	11.19	98	*Stress mode initialization (one hour)*
8:05	-0.9867	11.191	96	
8:11	-0.9867	11.191	95	
8:16	-0.9865	11.191	94	
8:22	-0.98667	11.191	93	
8:36	-0.986(67~73)	11.191	91	
9:00	-0.98672	11.191	90	*End of stress*
9:08	-0.4372	2.93	398-399	*Post-stress: Initial adjustment for same I_{DD}*
9:12	-0.465	5.0561	397-398	*Post-stress: Adjusted VGS to obtain pre-stress current, for same VDS*
9:14	-0.4642	5.0568	399	
9:30	-0.46426	5.0568	399	
9:33	-0.4372(4~8)	5.0568	422-423	*Post-stress with same VGS and VDS as pre-stress*
9:38	0.4372(5~7)	5.0568	**423**	*5 minute burn-in*
9:48	0.4372(29~32)	5.0568	**423**	*15 minute burn-in*

Once the stress ends (9:00 p.m.), an attempt to bias the device to the original V_{GG} and V_{DD} is made by first biasing the gate, then by increasing the drain voltage. However, due to the stress, a higher current is now seen for the same V_{GG} and V_{DD}. At 9:12 p.m, the device is biased at the pre-stress V_{DD}, but with V_{GG} adjusted for the pre-stress I_{DD}. Between 9:12 p.m and 9:30 p.m. it is shown that V_{GG} had to be decreased (more negatively biased) to achieve the same pre-stress I_{DD} and V_{DD}.

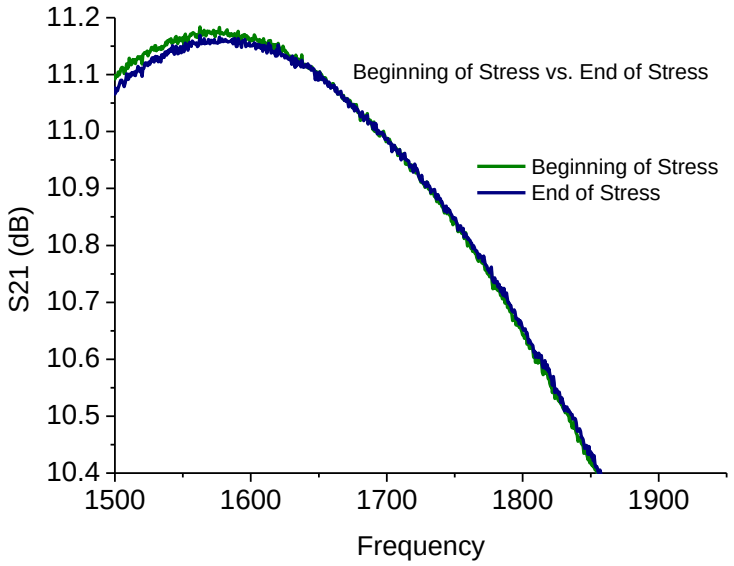
Lastly, between 9:38 p.m and 9:48 p.m. the device was biased to the original pre-stress V_{GG} and V_{DD}. The current was shown to increase by 24mA (6.015%).


12.5
12.4
12.3
12.2
12.1
12.0
11.9
11.8
11.7
11.6
11.5
11.4
11.3
S21 (dB)
1500
1600
1700
1800
1900
Frequency
Pre-Stress
Post-Stress

(a)


12.5
12.4
12.3
12.2
12.1
12.0
11.9
11.8
11.7
11.6
11.5
11.4
11.3
S21 (dB)
V GS adjusted for same current
1500
1600
1700
1800
1900
Frequency
Pre-Stress
Post-Stress

(b)



(c)

Figure 19: S21 stress experiment results: (a) before and after stress, biased at pre-stress V_{GG} and V_{DD}, (b) before and after stress, biased at pre-stress I_{DD} and V_{DD}, and (c) beginning and end of stress operation V_{GG} and V_{DD},

Figure 19 shows the S21 post-stress results, compared to the pre-stress results. Notice the downward shift of S21 in Figure 19(a). Despite the DC drain current increase, S21 gain has decreased. This can be attributed to the decrease of g_m. In fact, g_m and S21 are closely related through the following relationship:

$$S21 \sim g_m / f. \tag{6.1}$$

From Equation 6.1, it is expected that a decrease of g_m would cause a decrease of S21. Figure 20 shows, qualitatively, what has occurred. Notice the leftward shift of the g_m and I_{DS} curves for a given V_{GS}, V1. It is safely assumed that for this device, V1 lies to the right of the peak transconductance. Therefore, a leftward shift causes a decrease in g_m, whereas if V1 had been to the left of the peak transconductance, g_m and consequently S21 would have increased. Meanwhile, I_{DS} increases regardless.

Figure 19(b) shows that the effect of stress can be nearly completely compensated by adjusting V_{GG} so as to achieve the same I_{DD}. In circuit operation, this would require a gate compensation circuit, adding an additional complexity. Figure 19(c) shows S21 at the beginning and end of the stress regime. Notice the slight decrease at frequencies nearing the peak S21 gain.

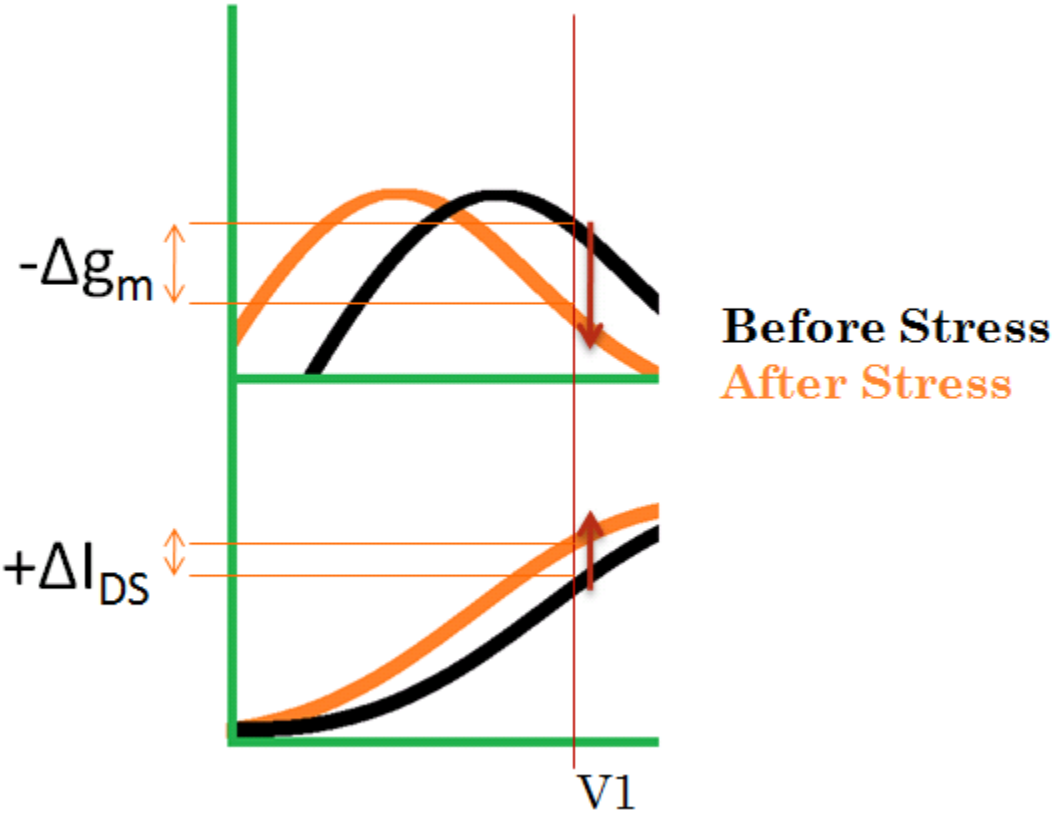


Figure 20: Qualitative effect of hot carrier stress on drain current and transconductance

Simulation of the Stress Regime versus Normal Operation

In order to gain physical insight into the mechanisms involved in the stress scheme versus the normal operation mode, two relative simulations were performed in Sentaurus. Figure 21 shows the bias points of the two modes, showcasing the drain current and hole current for the specific gate and drain biases.

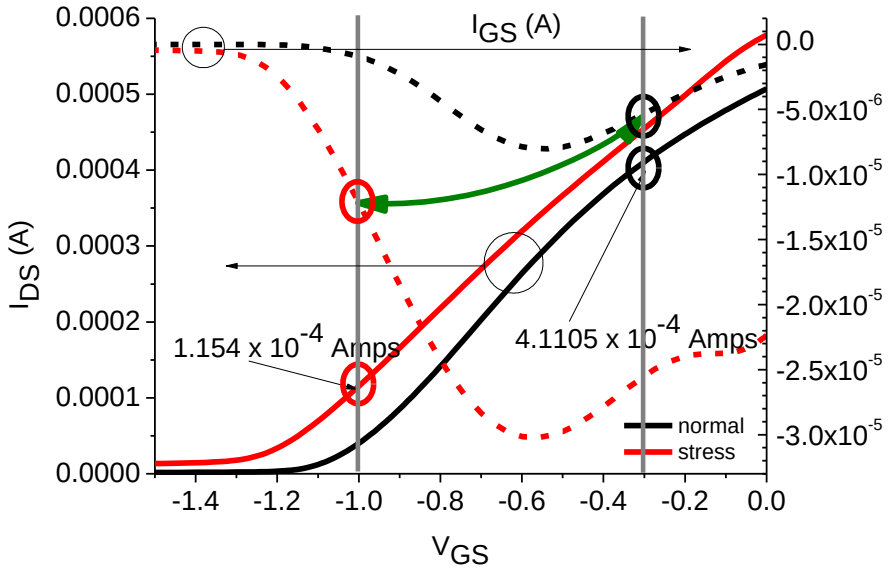
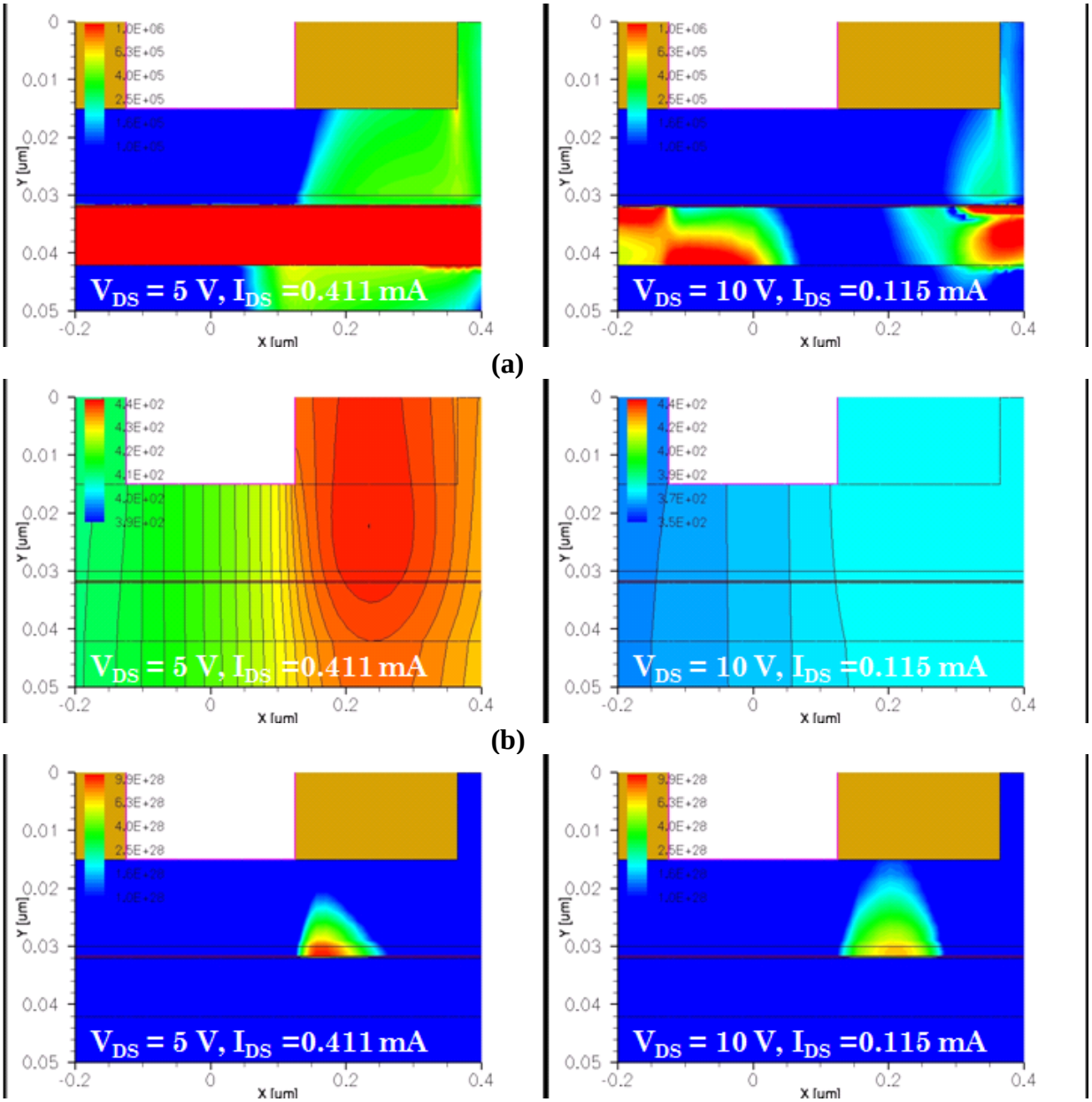


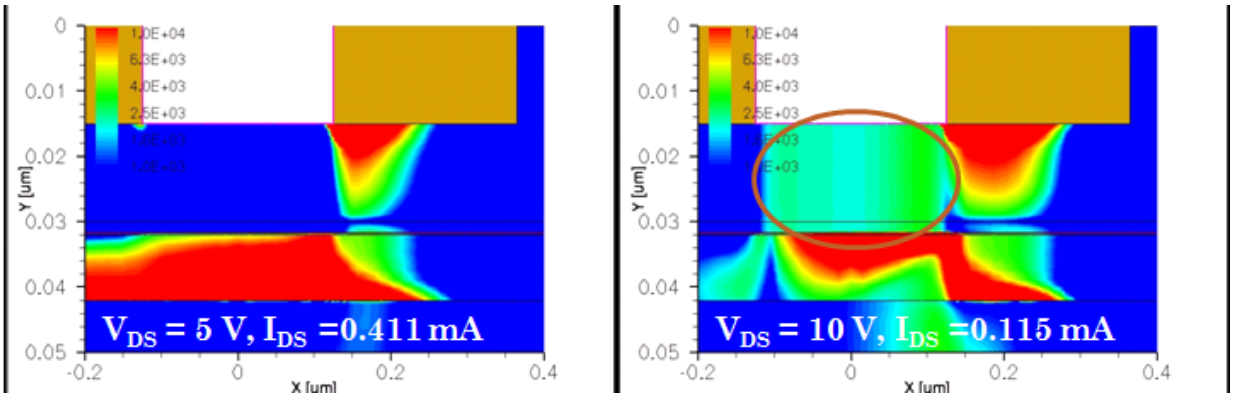
Figure 21: Simulation of stress mode (V_{DS} = 10 V) versus normal mode (V_{DS} = 5 V)

Observing the two bias points, the idea is to show how the device is sustaining operation for the following conditions (as approximately implemented in the previously described experiment): $I_{DS(\text{stress mode})} = 1/4 \times I_{DS(\text{normal operation})}$ and $V_{DS(\text{stress mode})} = 2 \times V_{DS(\text{normal operation})}$. Specifically, $V_{DS(\text{stress mode})} = 10$ V and $V_{DS(\text{normal operation})} = 5$ V.

Figure 22 below showcases the physical mechanism of both operating regimes. Notice that the stress regimes sees a more negative gate voltage and therefore observes a lower electron current, lower temperature, even lower impact ionization, but higher hole current! This

introduces an important concept; hot hole current, i.e. gate current is dependent not only on V_{DS} but also V_{GS}. As V_{GS} increases, the biasing begins to pull holes towards the gate through the shottky interface (similarly to a diode on the verge of becoming forward biased).





(d)

Figure 22: Simulation of stress regime versus normal operation showing (a) electron current density, (b) lattice temperature, (c) impact ionization, and (d) hole current density

Note on Self-Heating

As a device sustains high electric field and high current, it begins to self-heat. As current increases for a given drain voltage, self-heating increases and begins to affect an important aspect in regards to reliability, impact ionization. When temperature increases, impact ionization begins to decrease for a given drain voltage.

The effect of self heating for a given drain voltage, with a sweeping gate voltage produces a dip in hole current. This is due to an increase in carriers along with an increase in lattice temperature, as shown in Figure 23. Observe that as I_{DS} increases (by increasing V_{GS}) the lattice temperature increases. Moreover, at a certain point, the lattice temperature begins to cause a decrease in impact ionization. This is the effect of self-heating. When ambient temperatures are changed, the effect is offset accordingly.

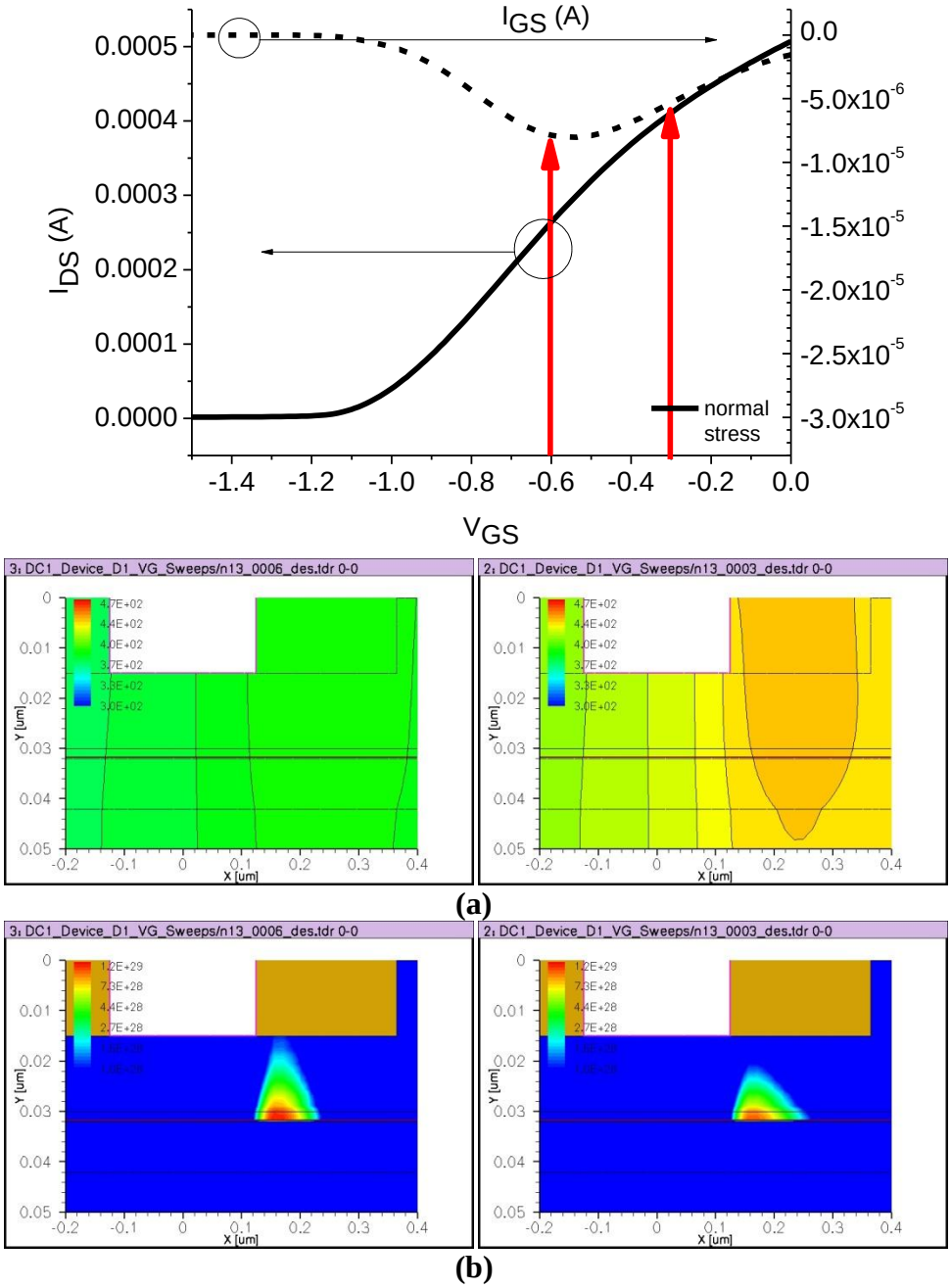


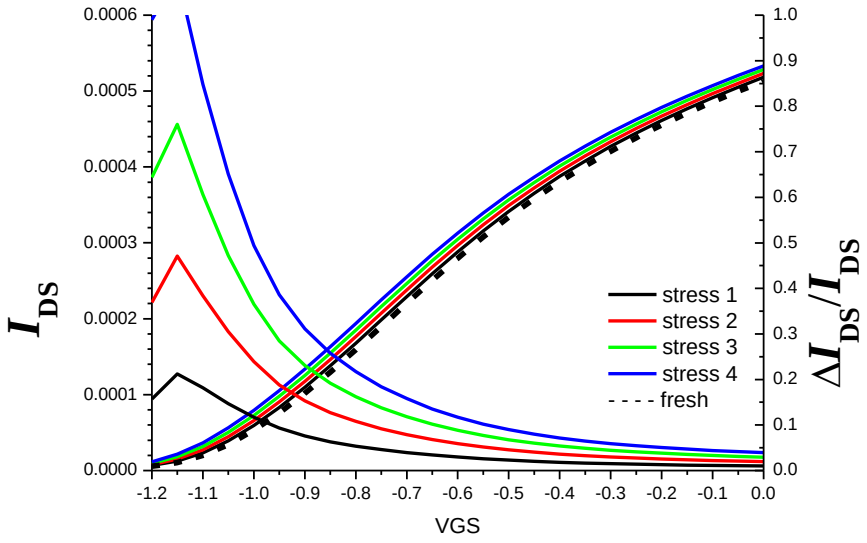
Figure 23: Self heating of the PHEMT, showing (a) I_{DS} and I_{GS} vs. V_{GS} and the corresponding (b) lattice temperature and (c) impact ionization for V_{GS} = -0.6 V (left) and - V_{GS} = 0.3 V (right) at V_{DS} = 6 V

CHAPTER 7: POST-STRESS SIMULATION AND RESULTS

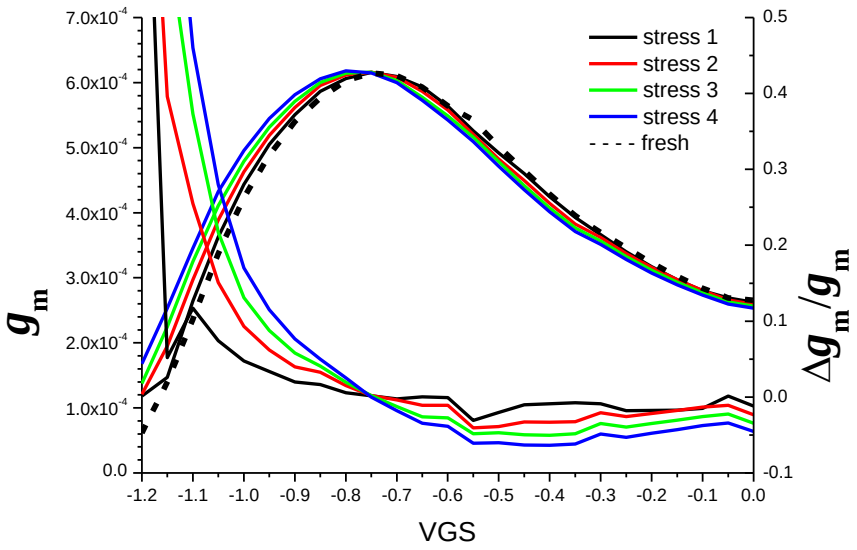
Several degradation mechanisms exist for the PHEMT. In this work, it is our interest to model the observed changes from measurements found in this work and measurements found from other authors [5,7]. This is done through implementing a physical change that is believed to occur after a PHEMT undergoes DC stress: The activation of planar dopants near and just above the channel [5].

The setback layer (between the 2DEG & delta doping) was given a doping of 3e17/cm^3, 6e17/cm^3, 9e17/cm^3, and 12e17/cm^3 (it was previously undoped). This is the area closest to peak impact ionization and large hole currents. It is believed that these hot carrier stress mechanisms are responsible for "activating" the planar doping just above the channel.

First, observe the effect of this post-stress simulation on drain current and transconductance. Figure 24(a) shows the observed changes for I_{DS} while Figure 24(b) shows the observed changes for g_m.



(a)



(b)

Figure 24: Simulation of post-stress effect on (a) I_{DS} and (b) g_m

Observe the leftward shifts of the drain current and transconductance curve. This is a well known characteristic found after stress and was also seen in the post-stress measurement of Chapter 6. Figure 24(b) also shows a slight increase of peak transconductance. This is consistent with the findings of [5,7] and believed to be present in the measurements of Chapter 6 (note that g_m was not physically measured).

The I_{DS} increase/shift and and peak g_m increase/shift can be correlated to Equations (4.1)-(4.4) (repeated here for convenience as Equations (7.1)-(7.4)). Since the effective doping, N_D, is increasing, V_{OFF} decreases (requires a more negative gate voltage to turn off). This causes an leftward shift and increase in I_D for a given V_{GS} and increase in the peak transonductance, g_m, for a given V_{GS}.

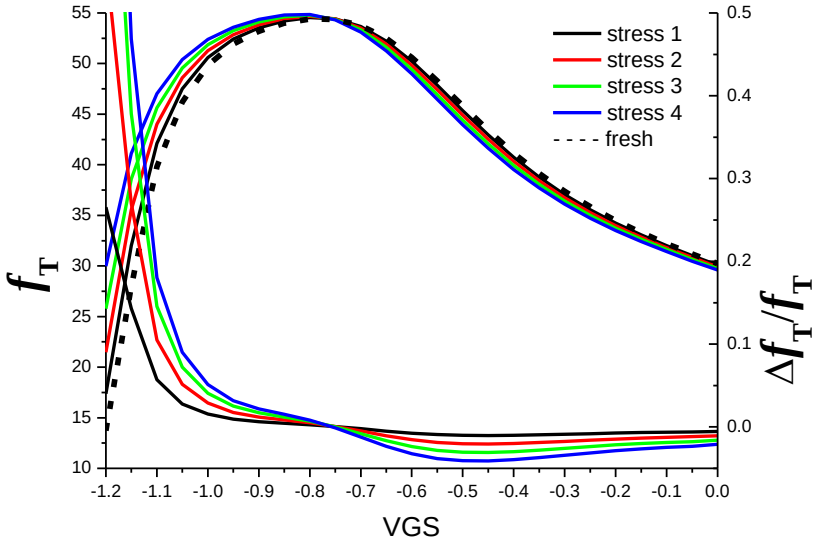
$$I_D = \mu_n C_S W (V_{GS} - V_{OFF})^2 / 2L \tag{7.1}$$

$$g_m = \mu_n C_S W (V_{GS} - V_{OFF})^1 / L \tag{7.2}$$

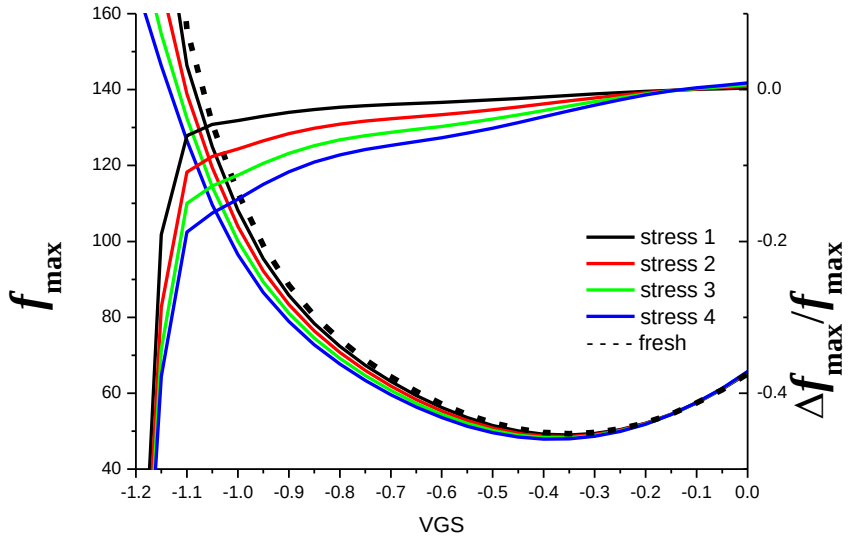
$$V_{OFF} = V_{bi} - V_{po} - (\Delta E_c / q) \tag{7.3}$$

$$V_{po} = q N_D d^2 / 2\varepsilon_r \varepsilon_0 \tag{7.4}$$

Next, observe the effect of post stress on f_T and f_{max}, as shown in Figure 25. Recall Equations (2.3) and (2.4). The effect that post-stress has on transconductance, almost linearly transfers over to f_T and f_{max}. This post-stress mechanism hence serves as a predictive indicator of what to expect for f_T and f_{max} and can be attributed to the large signal model of the PHEMT (see Chapter 4).



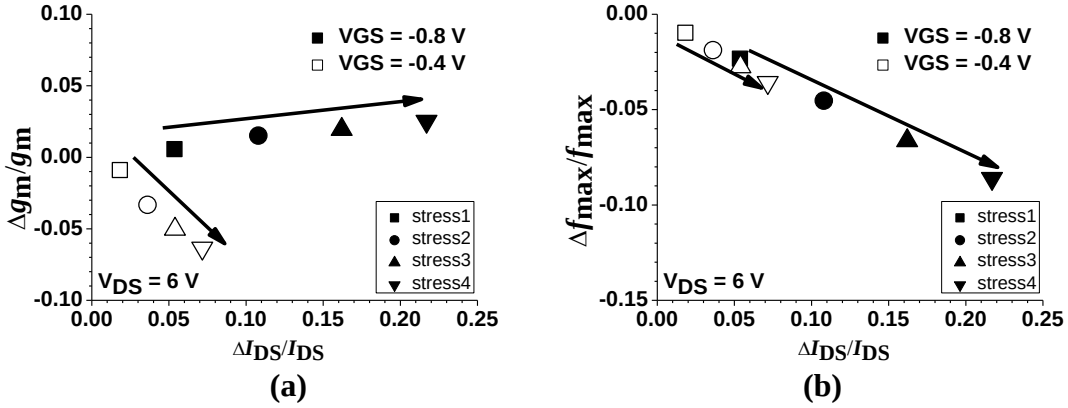
(a)

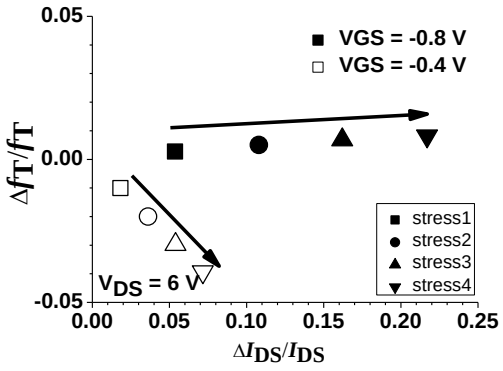


(b)

Figure 25: Simulation of post-stress effect on (a) f_T and (b) f_{max}

To observe the effects of stress on RF performance (and transconductance), Figure 26 and 27 show the stress deltas where $\Delta X/X = (X_{stress} - X_{unstressed})/X_{unstressed}$.

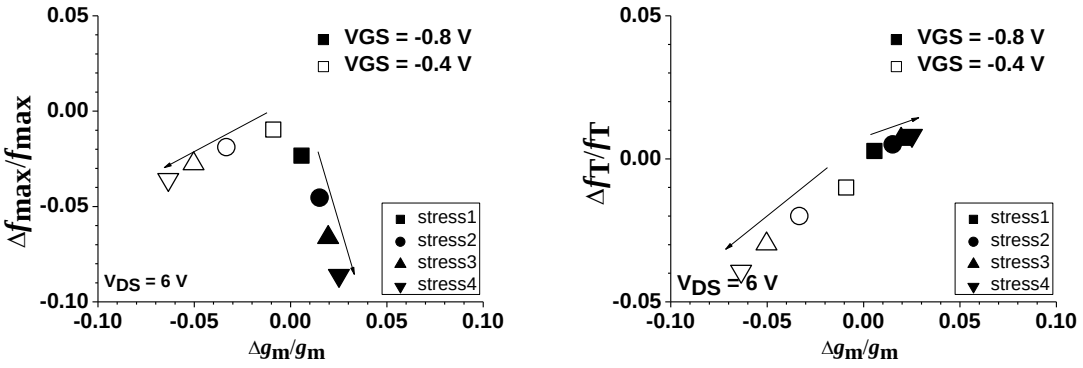




(c)

Figure 26: Post stress simulation of $\Delta I_{DS}/I_{DS}$ dependence for (a) $\Delta g_m/g_m$, (b) $\Delta f_{max}/f_{max}$,and (c) $\Delta f_T/f_T$

Notice the variation, based on the bias points. As stress increases, and current increases, a given change of current will yield a linear change in g_m, f_{max} and f_T.



(a) **(b)**

Figure 27: Post stress simulation of $\Delta g_m/g_m$ dependence for (a) $\Delta f_{max}/f_{max}$,and (b) $\Delta f_T/f_T$.

Similarly, for g_m, notice the variation of $\Delta f_{max}/f_{max}$ and $\Delta f_T/f_T$ in Figure 27. As stress increases, and g_m changes (at a given V_{GS}), it will yield a linear change in f_{max} and f_T. This is expected. However, as frequency increases, this change is no longer linear for a given bias of V_{GS} = -0.4 V, as shown in Figure 28. S21 is shown to not be linear dependent at V_{GS} = -0.8 V, as frequency increases.

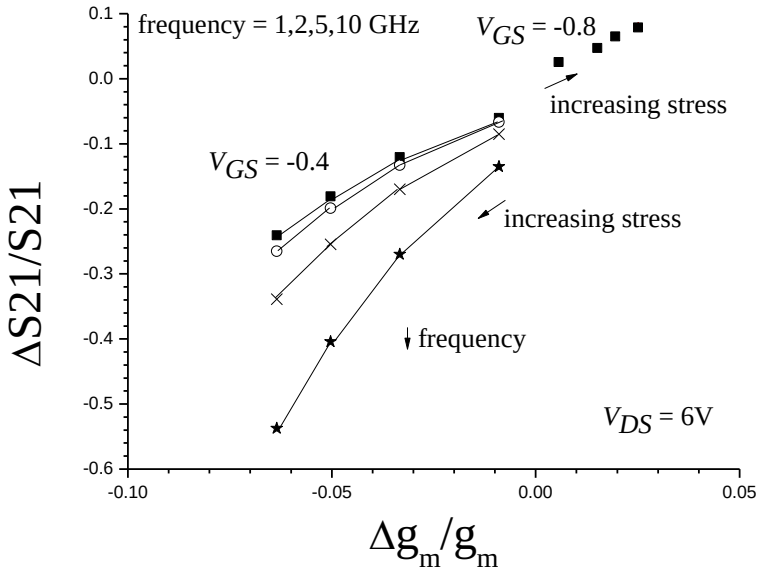


Figure 28: Post-stress simulation of $\Delta g_m/g_m$ dependence for $\Delta S21/S21$

CHAPTER 8: CONCLUSIONS

Summary of Work

In this work, a comprehensive and unified study has been carried out on the hot carrier reliability of the PHEMT. This included the following: (1) Investigation of hot carrier mechanisms; (2) Trade study of four various device geometries; (3) Ambient Temperature effects on stress; (4) Experimental measurements of stress and the observed effect on V_T, I_{DS}, and S21; (5) Simulation of a stress regime versus normal regime through TCAD; (6) Simulation of post stress for various levels of stress, as well as analysis and predictive effect on several parameters (I_{DS}, g_m, f_T, and f_{max}).

Future Work

To facilitate a more applicable and hands-on study for industry, obtaining control of process and fabricating devices with various geometries would need to be in order. Further, it would be worthwhile to perform high power DC curve tracing measurements (to observe I_{GS}, and g_m directly from measurement). Also, large signal RF stress should be the next mechanism evaluated.

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