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THREE-DIMENSIONAL SIMULATION STUDY OF LOW VOLTAGE ($<100\text{V}$)
SUPERJUNCTION LATERAL DMOS POWER TRANSISTORS

by

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B.S. Universidad Autonoma de Manizales, 2008

A thesis submitted in partial fulfilment of the requirements
for the degree of Master of Science
in the Department of Electrical Engineering and Computer Science
in the College of Engineering and Computer Science
at the University of Central Florida
Orlando, Florida

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2016

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ABSTRACT

A new revolutionary concept was presented two decades ago, known as "semiconductor Super-junction (SJ) theory" to enhance the trade-off relationship between specific on resistance, R_{SP} , and off-state breakdown voltage, BV , in medium to high voltages (more than 100 V) power MOSFETs. The SJ concept was first applied and commercialized to vertical structures, but it hasn't been used yet in low voltage MOSFETs with lateral structures. This thesis provides a review of the most common structures, principles and design techniques for discrete power MOSFETs. It also presents a simulation study of the application of these SJ concepts in the design of a Low Voltage SJ LDMOS transistor, using TCAD software. To make the device commercially feasible, this device design targets aggressive goals such as an off-state Breakdown Voltage of 60V with R_{SP} of $20m\Omega \cdot mm^2$. This study includes the analysis of the flow process for the fabrication of this transistor, using semiconductor technologies, and the simulation results, including Breakdown Voltage, on-state resistance, electric field distribution among others simulation analysis.

To Jesse

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CHAPTER 1: INTRODUCTION

According to ABB, around 40 percent of the world's power needs are currently met by electrical energy and that proportion is expected to rise as countries cut carbon emissions and shift to renewable energy sources. As the trend towards electrification and renewable energies increases, enabling technologies such as power electronics are becoming ever more important. The systems and machines of the modern world increasingly depend on power electronics to run efficiently and sustainably. Without this technology, electric motors would always run at full speed and renewables, such as solar and wind power, could not be fed into the electricity grid [1].

Power electronics is the application of solid-state electronics for the control and conversion of electric power. It applies to both the systems and products involved in converting and controlling the flow of electrical energy, allowing the electricity needed for everyday products to be delivered with maximum efficiency in the smallest and lightest package.

Historically, power electronic systems have greatly benefited from advances in power semiconductor technology. Applications that have provided a technology pull for power discretes are in the computer, telecommunications, and automotive industries for devices operating at below 200 V and motor control, robotics, and power distribution for devices operating at above 200 V.

The social implications are as impressive as the economic considerations. The increasing utilization of power devices for control of power and energy leads to conservation of fossil fuels and reduces urban environmental pollution.

Power discrete devices used in systems can be broadly classified into two categories: power rectifiers and power switches. Although much emphasis was given to improving the performance of power switches in the 1970s and 1980s, the benefits accruing from enhancements in power

rectifiers are being increasingly appreciated [2].

This thesis provides a review of the most common structures, principles and design techniques for power switches, It also presents a simulation study of an specific power switch structure, the Super Junction LDMOS Transistor, using TCAD software. This study includes the analysis of the flow process for the fabrication of this transistor using semiconductor technologies, and the simulation results, including Breakdwon Voltage, on-resitance, gate charge, electric field distribution among the others.

CHAPTER 2: POWER TRANSISTORS

The optimum choice for the power switch depends upon the requirements in the application for blocking voltage and switching speed. Today, it is commonplace to use power metal oxide semiconductor field-effect transistors (MOSFETs) for applications such as power supplies and disk drives that require relatively low (<100 V) blocking voltages and high switching speeds (>100 kHz operation). When the operating voltage exceeds 300 V, the insulated gate bipolar transistor (IGBT) has become the favored device due to its lower on-state voltage drop. The performance of these devices continues to improve due to the structural optimization and innovation [2].

2.1 Insulated Gate Bipolar Transistor (IGBT)

For high-voltage-power electronic applications, the IGBT has replaced silicon bipolar power transistors. The IGBT structure, first proposed in 1982 [3], consists of a wide-base p-n-p transistor driven by an integrated short channel MOSFET. This combination produces a very high power gain (typically $>10^6$) because of the high-input impedance resulting from the MOS-gate structure, and the low on-state voltage drop resulting from high-level injection of minority carriers in the n-drift region [2].

The switching speed of the IGBT can be adjusted by lifetime control processes making it suitable for a wide variety of medium and high-power applications [4].

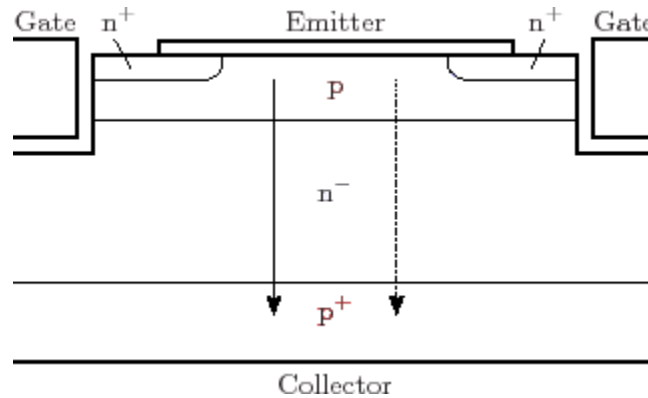


Figure 2.1: IGBT device based on the DMOS-technology. This structure can be used for high current applications.

2.2 Power Metal Oxide Field Effect Transistors (Power MOSFETs)

In the power and high-voltage domain the BJT was widely used until the 1980's [5]. The major drawback of the BJT in this regime is the low current gain which required complex and expensive control circuits to generate the base current. These circuits required additional power and the increased heat dissipation was a big issue. On the other hand, field effect transistors are voltage controlled and no static control current is required. This helped to overcome the control circuit problems.

An additional advantage of MOSFET devices is that there is no second breakdown. Higher temperatures lead to a decrease of the carrier mobility, and consequently, the drain current is reduced. This results in a reduced power loss and heat generation. Therefore, in contrast to BJTs, MOSFET devices can be simply connected in parallel [6], which is the basis for the design of power MOSFET structures.

2.3 Power Device Design Techniques

Various design techniques are available to optimize the device behavior and to integrate high-voltage devices in integrated circuits. In the following considerations the two important properties blocking voltage and on-current are of special interest. Closely related is the on-resistance which also determines the power losses in the device. To achieve a cost efficient design the required chip surface is one of the most important constraints which has to be minimized [7].

2.3.1 Vertical and Lateral Devices

Devices in vertical orientation are typically used for discrete power devices. Here, the main current flow is oriented vertically, meaning perpendicular to the semiconductor surface. The drain/collector contacts are placed at the bottom of the devices. This is a common method to achieve a high current component and is especially used for discrete high current power devices.[7] In contrast to the vertical devices, the dominant current flow of lateral devices is in horizontal direction, that is, in parallel to the semiconductor surface [8]. For low-voltage and low-power transistors like in CMOS environments, this is the typical design method for MOSFET devices.

2.3.1.1 Double Diffusion MOSFETs (DMOS)

For applications operating at low voltages, the predominant choice is silicon power MOSFETs because of their high input impedance, low on-resistance, ruggedness, and fast switching speed. Until recently, most of the commercially available power MOSFETs were being manufactured with the DMOS. This is a typical power MOSFET structure. It derives its name from the fact that DMOS process uses double diffusion to define the channel length. Its compatibility with mainstream MOS processing technology has lead to a rapid development of DMOS devices in recent years.

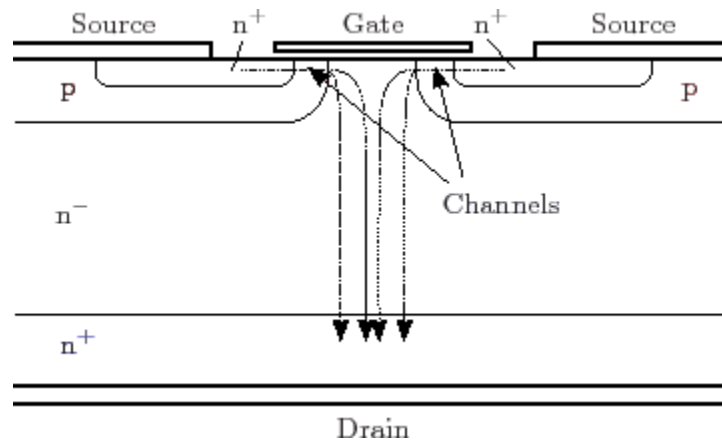


Figure 2.2: DMOS device with its lateral channel which is fabricated by lateral diffusion.

DMOS process technology is well established and documentation is abundant in literature and textbooks [9] [10]

DMOS devices are characterized by their direction of current flow. LDMOS is a type of DMOS device with lateral current flow while VDMOS has a vertical current flow through the device.

2.3.1.2 VDMOS

VMOS is an acronym for "vertical metal oxide semiconductor", or "V-groove MOS" [11]. The "V" shape of the MOSFET's gate allows the device to deliver a higher amount of current from the source to the drain of the device. The shape of the depletion region creates a wider channel, allowing more current to flow through it. This structure has a V-groove at the gate region and was used for the first commercial devices. The device's use was a power device until more suitable geometries, like the UMOS (or Trench-Gate MOS) were introduced in order to lower the maximum electric field at the top of the V shape and thus leading to higher maximum voltages than in case of the VMOS.

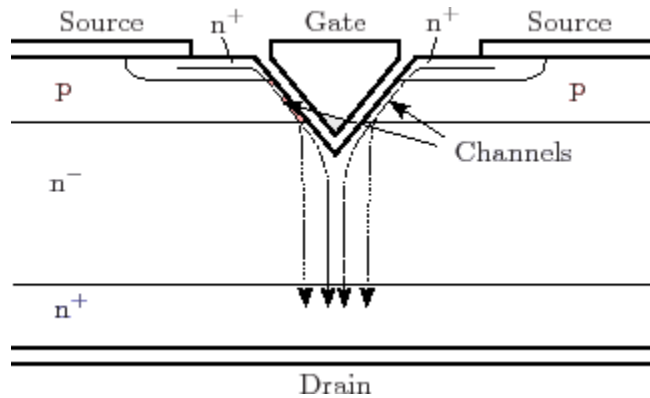


Figure 2.3: MOS devices with V-shaped gate structures used for power MOSFET devices.

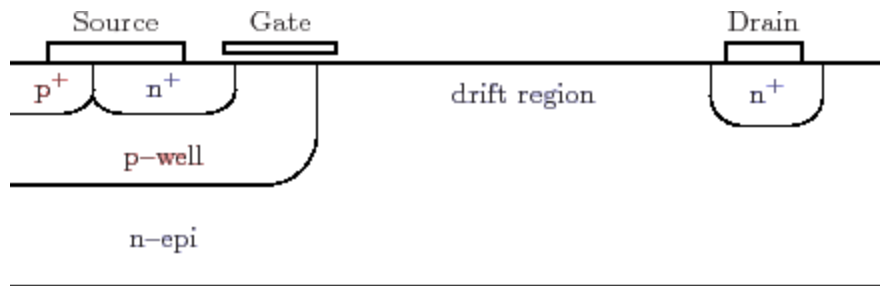


Figure 2.4: Basic lateral high voltage double diffused MOS transistor (LDMOS). The electric field is consumed by the relatively low doped drift region.

2.3.1.3 LDMOS

LDMOS is a type of DMOS device with lateral current flow. There are other modifications to the conventional DMOS structure. One of them is LDMOS with a Lightly-Doped Drain (LDD) that utilizes Reduced-Surface Electric field (RESURF) to enhance the device breakdown capability[12].

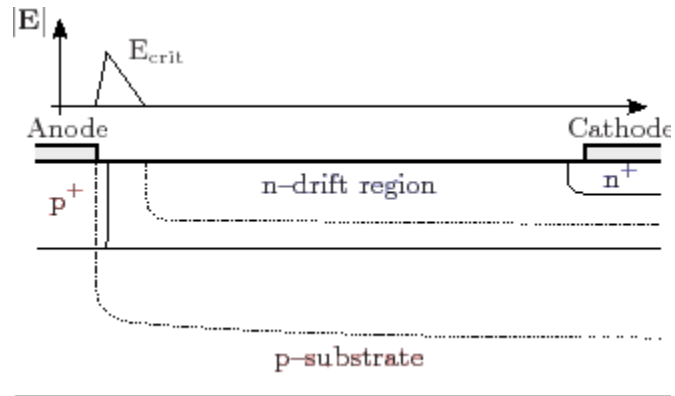


Figure 2.5: (a) Classical Diode Structure

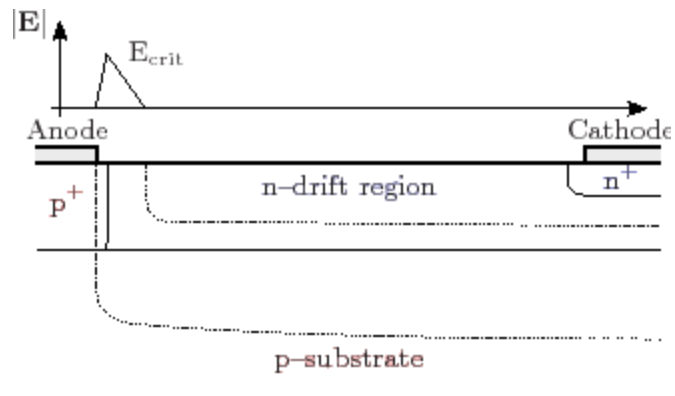


Figure 2.6: (b) RESURF Diode Structure

2.4 Reduced Surface Field Technique (RESURF)

To resist high blocking voltages, the simplest approach is to make long and lowly doped drift regions. Both parameters, length and low doping, lead to large on-resistance ($R_{DS,on}$) and therefore to higher drop voltages, and higher power loss. Another aspect of long, lateral drift regions is the additionally required chip area which increases costs. A trade off between blocking voltage and on-resistance has to be found. For a given breakdown voltage the optimal drift length and doping can be determined [13,14].

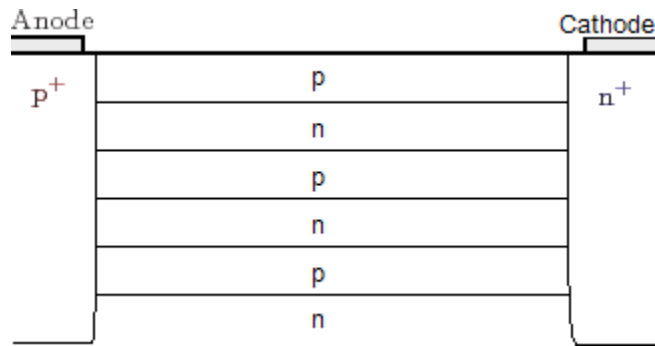


Figure 2.7: Basic structure of a Super Junction diode.

The peak electric field is typically concentrated near the pn-junction close to the surface, with the RESURF (Reduced Surface Field) concept introduced by Appels and Vaes this maximum field can be reduced [15,16]. This is accomplished by changing the design such that the space charge region in the blocking state extends over the whole drift zone. The resulting charge distribution leads to a continuous potential drop along the whole drift zone and not only across the junctions. Therefore the same terminal voltages cause lower electric fields in the device. RESURF is used in modern LDMOS devices. In n-channel LDMOS devices commonly a p-doped layer is introduced below the drift region and the thickness of the drift region is chosen that in blocking mode the space charge region extends up to the silicon surface. For a given maximum blocking voltage the length of the drift region can therefore be reduced. This minimizes both critical parameters, the on-resistance and the chip surface.

2.5 Super Junction

An extension of the RESURF concept is the Super Junction (SJ) structure which basically consists of layers or stripes of alternating n- and p-doped areas. With reverse bias, the space charge region extends throughout the whole drift area and removes all free carriers. Electric field peaks are

avoided which allows high blocking voltages. Also a high doping can be chosen for the stripes, which results in a very low on-resistance.

CHAPTER 3: SUPER JUNCTION POWER LDMOS TRANSISTOR

Power LDMOS devices generally can operate at higher frequencies than vertical devices, such as VDMOS and IGBTs, due to their smaller parasitic capacitances [17]. They are easier to integrate in power integrated circuits, but they have lower current handling capability.

It is also well known that in conventional power LDMOS devices, considering the ideal case where all other resistances are unimportant, the specific on-state resistance is approximately determined by the drift region alone. Also the trade-off relationship between the specific on-state resistance and the breakdown voltage leads to the formulation of an ideal limit on the device performance, beyond which no further reduction in R_{on} is possible without affecting breakdown voltage.

When designing power MOSFETs, engineers make great efforts to achieve the best trade-off relationship between off-state breakdown voltage BV , and specific on-state resistance R_{sp} (which is the product of on-resistance, R_{on} , and active area, A , of the device and represents low conduction loss characteristics), as well to scale down the device as much as possible, without degrading its performance.

Although great advances have been accomplished in conventional devices in this BV and R_{sp} trade-off relationship, [8] shows that there is a limit given by the Silicon.

A decade ago, a new theory has been presented, known as "semiconductor super junction (SJ) theory" to overcome the trade-off relationship between R_{sp} and BV in medium to high voltages. When compared with conventional semiconductor devices, SJ devices have achieved significant improvement [9]. The SJ concept was first applied and commercialized to vertical structures [10-13]

The SJ structure basically consists of layers or stripes of alternating n- and p-doped areas. With

reverse bias, the space charge region extends throughout the whole drift area and removes all free carriers. Electric field peaks are avoided which allows high blocking voltages. Also a high doping can be chosen for the stripes, which results in a very low on-resistance.

Doping concentration increases with decreasing stripe width, however, small stripes are more and more difficult to produce. Lateral Super Junction combination with SOI (Silicon On Insulator) structure can be the one possible solution to overcome the process difficulties, but the implementation of SOI technology increases the price of the device considerably, for this reason the SOI implementation is avoided in the design of the SJ LDMOS in this present work.

Silicon on insulator (SOI) technology refers to the use of a layered silicon—insulator—silicon substrate in place of conventional silicon substrates in semiconductor manufacturing, especially microelectronics, to reduce parasitic device capacitance, thereby improving performance.

SJ devices have shown to make significant improvements on the R_{on} and V_{br} relationship; this is because that, besides a smaller specific on-state resistance, superjunction devices can also achieve a higher breakdown voltage compared to the conventional power MOSFET with the same drift region length. [18][19]

3.1 On-state Resistance of Power LDMOS

The on-resistance of the conventional power LDMOS can be analyzed by different resistances connected in series [11]. Figure 3 shows the resistance components of an LDMOS. The total resistance is the sum of these components:

$$R_{on} = R_{cs} + R_{ch} + R_{acc} + R_{drift} + R_{cd}$$

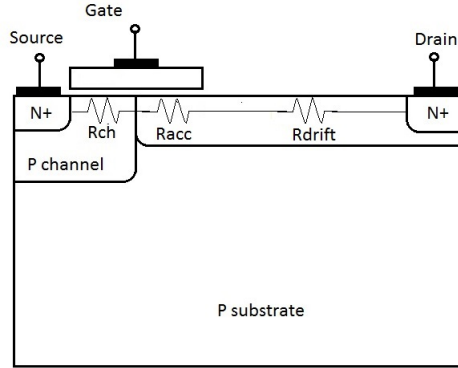


Figure 3.1: Conventional LDMOS on-resistance

R_{cs} and R_{cd} are the contact resistances of source and drain, which are usually very small and can be disregarded. R_{ch} is the channel resistance and can be calculated using the standard equation that is used for digital and analog MOSFETs:

$$R_{ch} = \frac{L}{2\mu_i C_{ox}(V_G - V_{th})}$$

where μ_i is the inversion layer mobility for electrons (n-LDMOS) and holes (p-LDMOS), V_G is the gate voltage, V_{th} is the threshold voltage, and L is the channel length. C_{ox} is the gate capacitance and can be calculated in 2D by

$$C_{ox} = \frac{\epsilon_{ox}}{t}$$

where ϵ_{ox} is the dielectric constant of oxide, t is the gate oxide thickness.

The accumulation resistance R_{acc} is unique for DMOS (LDMOS and VDMOS). It represents the

resistance in the silicon area that is overlapped by gate and drain. The word *accumulation* means that the overlapped area is in accumulation mode when the gate is turned on. The accumulation resistance can be calculated by

$$R_{\text{acc}} = \frac{L_{\text{acc}}}{4\mu_a C_{\text{ox}}(V_G - V_{\text{th}})}$$

where L_{acc} is the drift accumulation length, which is from the body/drain PN junction to the gate edge in the drain, and μ_a is the electron or hole mobility in the accumulation layer.

The drift region resistance R_{drift} is calculated using

$$R_{\text{drift}} = \rho \frac{L_{\text{drift}}}{d_{\text{eff}}} = \frac{L_{\text{drift}}}{q\mu_n N_d d_{\text{eff}}} = \frac{L_{\text{drift}}}{q\mu_n D_{\text{eff}}}$$

$$D_{\text{eff}} = N_d d_{\text{eff}}$$

where L_{drift} is the drift length, d_{eff} is the effective N-well thickness due to unequal rent flow, N_d is the doping concentration in the drain, μ_n is the electron mobility and D_{eff} is the effective total dose in the drain.

3.2 Specific On-state Resistance of Power LDMOS

To compare resistance of LDMOS with different technology or vendors, it is convenient to use specific on-resistance, $R_{\text{on,sp}}$ or R_{sp} instead of pure resistance; the difference is that specific on-

resistance takes the device pitch size into consideration. The pitch size is calculated from body contact edge to drain edge. [11]

The simulated SJ LDMOS in this work use a pitch size of $1 \mu m$, and the unit used for specific resistance is $m\Omega \cdot mm^2$

3.3 Power LDMOS Specific On-resistance and BV trade-off relationship

Considering the ideal case where the R_{sp} of the LDMOS is determined by the drift region only, and assuming that the current flows uniformly through the drift region without current spreading effects. Then the relation between the on-resistance and the BV can be expressed as

Figure 3.2 shows the state-of-the-art trade-off between R_{sp} and BV of standard power MOSFETs and theoretical silicon limit, respectively [12]. As can be seen in the figure, the on-resistance of power MOSFETs increases sharply with the BV. This has prevented the use of power MOSFETs at high voltages. A high blocking voltage of a standard power MOSFET requires a thick and low doped epitaxial layer (n -drift region) which causes an increase in the on-resistance. A variety of MOS structures can be used for power MOSFETs. In the medium- and high-voltage applications, reliability and SOA (safe operating area) of the device are more important than the on-resistance. Therefore, planar structure is frequently used in the high-voltage power MOSFETs, and the trench structure is used in the low-voltage MOSFETs (see Figure 3.2).

$$R_{sp} = 5.93 \times 10^{-9} BV^{2.5} [m\Omega \cdot cm^2]$$

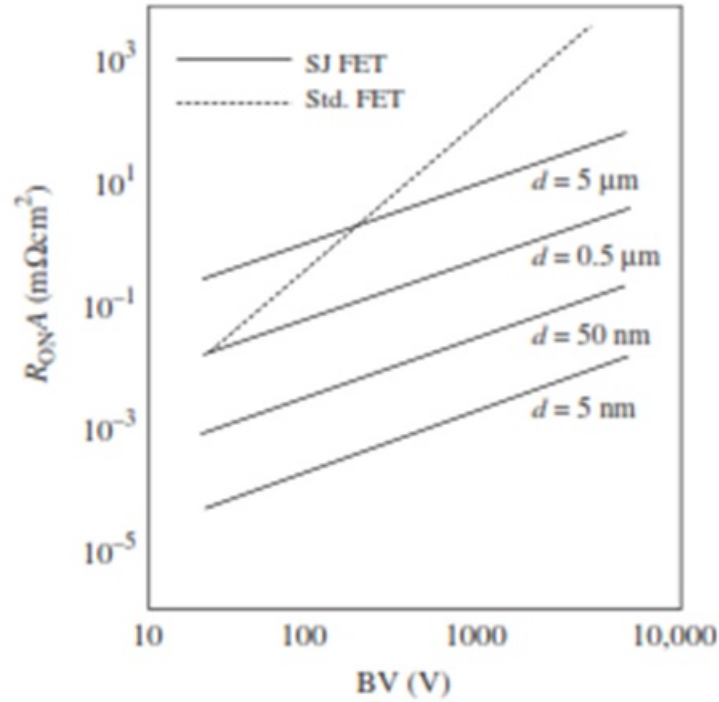


Figure 3.2: R_{sp} versus BV relation as reported by T. Fujihira and Miyasaka [22]. Where d is the width of the stripes of the superjunction. The silicon limit is the dashed line.

3.4 Super Junction LDMOS

The purpose of this work is to use the superjunction concepts in the design of a low voltage lateral power transistor (30V SJ-LDMOS). Figure 3.3 shows the diagram for the SJ-LDMOS design presented and simulated in this work.

This structure allows a doping level of the n -region, which is typically one order of magnitude higher than that in standard high-voltage LDMOS.

The additional charge is counterbalanced by the adjacent charges of the p -column, thus contributing to a sideways electrical field without affecting the lateral field distribution.

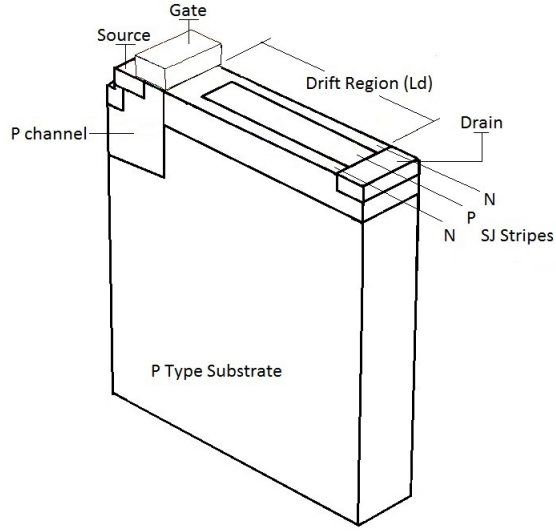


Figure 3.3: 3D schematic view SJ-LDMOS proposed in this work

The electric field inside the structure is fixed by the net charge of the two oppositely doped columns. Thus a nearly flat field distribution similar to that in SJ pn -structures can be achieved, if both regions counterbalance each other perfectly.

For higher blocking voltages only the depth of the columns has to be increased without any change of the doping. This leads to a linear relationship between blocking voltage and on-resistance instead of the power relationship for the case of conventional LDMOS.

Considering the drift region of a SJ LDMOSFET has a length L_d , the p - and n -column widths are $d_N = d_P = d_{PN}$, and the p - and n -column dopings are N_N and N_P , respectively, and assuming that the n - and p -stripes are completely depleted before breakdown and perfect charge balance of each column, the BV and the charge Q of the column are given by

$$BV = E_{\text{crit}}L_d$$

$$Q = \frac{N_N d_{PN}}{2} = \frac{\epsilon_{si} E_{crit}}{q}$$

Where the critical electric field E_c is also increased by the increased doping concentration of the stripe. Because the current flows only through the n -column, the specific on-resistance R_{sp} can be expressed as

$$R_{sp} = \frac{L_d}{q\mu_n N_N} = \frac{d_{PN} BV}{2\mu_n \epsilon_{si} E_{crit}^2}$$

This equation clearly shows the linear relationship between the BV and the specific on-resistance of SJ LDMOS instead of the power relationship for the case of conventional LDMOS.

Practically the main advantage of SJ LDMOSFETs is the drastic reduction of the device area because of its low specific on-resistance. This small chip size of the SJ LDMOSFET leads to a low gate charge, which results in a short turn-on delay time compared to that of conventional LDMOS with comparable voltage and current ratings.

In the SJ power MOSFET structure, the heavily doped alternative p-n columns replace the lightly doped drift region of the conventional power MOSFETs. The pn junctions in the drift region are reversed biased. During OFF state (gate/source voltage V_{gs} less than threshold voltage V_t), drift region can be fully depleted by the inserted lateral electric field before the breakdown happens. As a result, the drain/source voltage (V_{ds}) is supported by the whole drift region. The electric field along the drift region becomes trapezoidal or even rectangular shape as compared to the triangular shape in the conventional device drift region. Therefore, the breakdown voltage of the SJ device

is proportional to the drift region length but independent of the drift region doping concentration. Thus, the n-drift region can afford to be doped at a much higher concentration to reduce the on-state resistance of the drift region below that of the conventional structure without affecting the breakdown rating.

To achieve the best performance in the SJ structure, precisely charge-balanced p and n columns must be formed at exactly the same doping levels to have equal amount of positive and negative charges. By carefully choosing the suitable p-n column width, doping concentration and drift region depth, the SJ device can substantially outperform the conventional power MOSFETs.

CHAPTER 4: RESULTS

4.1 TCAD Process Simulation

This project provides the process flow simulation for the Super Junction Laterally Diffused MOS (SJ LDMOS) using Synopsis TCAD Sentaurus tools.

The flow process simulation is performed using Synopsys Sentaurus Process simulator, this is an advanced 1D, 2D, and 3D process simulator suitable for silicon and nonsilicon semiconductor devices. It features modern software architecture and state-of-the-art models to address current and future process technologies.

Sentaurus Process simulates all standard process simulation steps, diffusion, analytic implantation, Monte Carlo implantation, oxidation, etching, deposition, and silicidation.

Sentaurus Process uses the Alagator scripting language that allows users to solve their own diffusion equations. Alagator can be used to solve any diffusion equation including dopant, defect, impurity, and oxidant diffusion equations [20].

The process flow steps for the process simulated in this project are shown below:

1. P well Implant
2. P well Drive
3. Gate Oxide
4. Poly-Silicon Deposition
5. Poly-Silicon Anneal

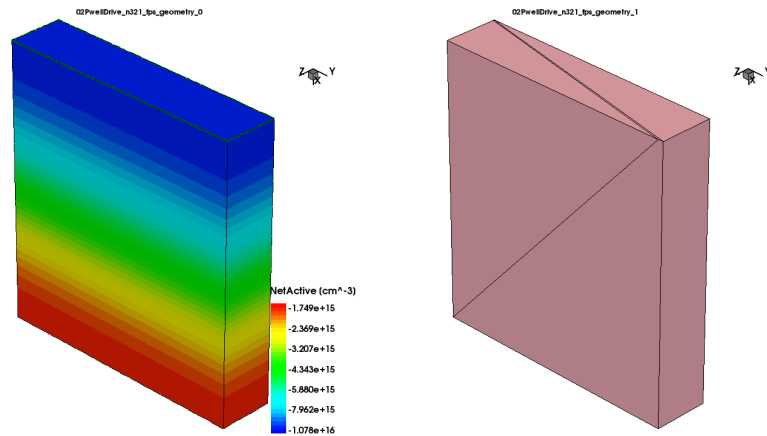


Figure 4.1: 3D TCAD SJ-LDMOS Sentaurus Process Simulation: P Well Drive

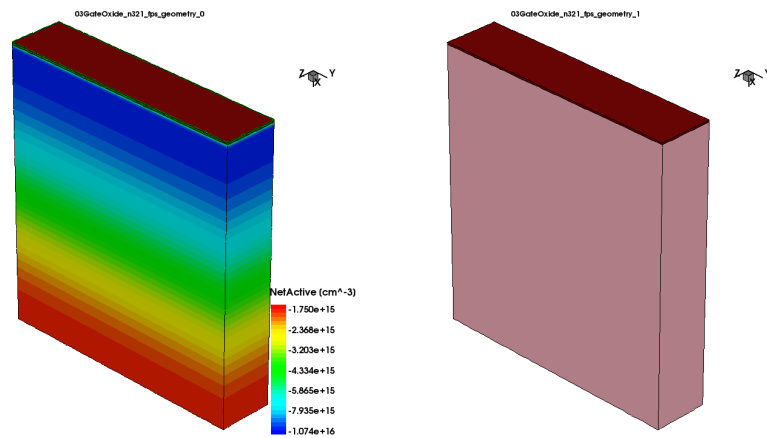


Figure 4.2: 3D TCAD SJ-LDMOS Sentaurus Process Simulation: Gate Oxide

6. Gate Etch

7. Nitride Hard Mask #1

8. P Channel Implant

9. P Channel N well Drive

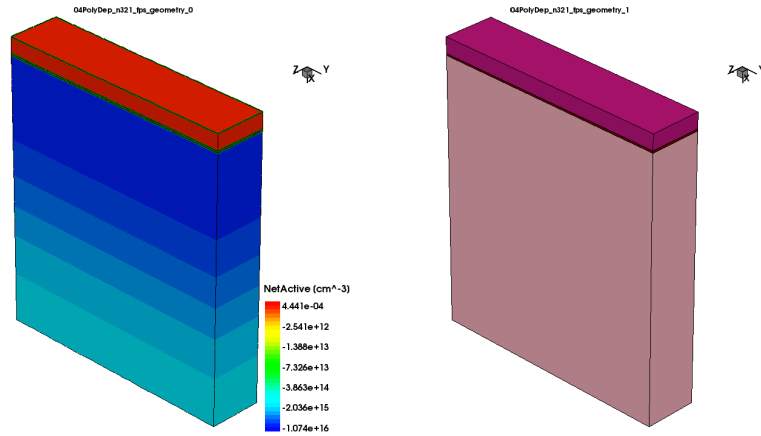


Figure 4.3: 3D TCAD SJ-LDMOS Sentaurus Process Simulation: Poly-Silicon Deposition

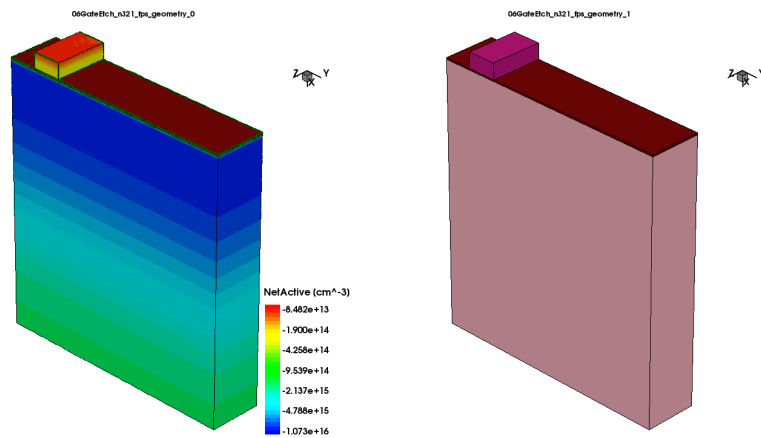


Figure 4.4: 3D TCAD SJ-LDMOS Sentaurus Process Simulation: Gate Etch

10. Nitride Hard Mask #2

11. N+ Implant

12. LDD Blanket

13. Drift Region Oxide Hard Mask

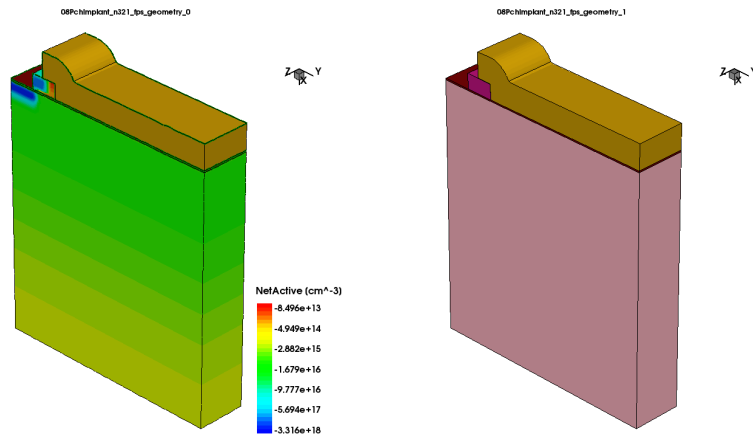


Figure 4.5: 3D TCAD SJ-LDMOS Sentaurus Process Simulation: P channel Implant

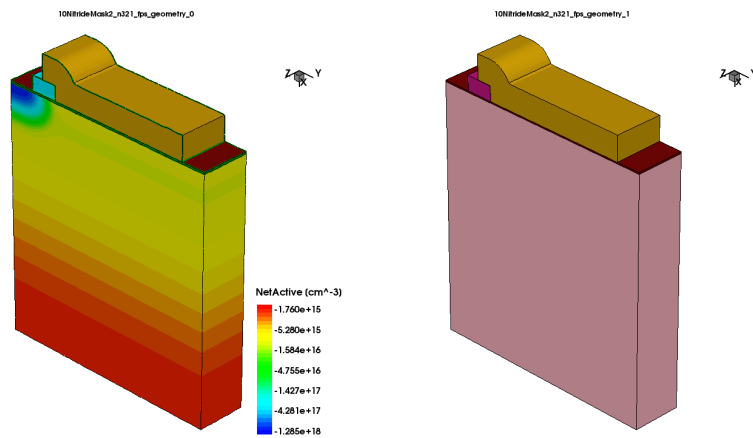


Figure 4.6: 3D TCAD SJ-LDMOS Sentaurus Process Simulation: Nitride Hard Mask #2

14. N Well Drift Region

15. P stripe Oxide Hard Mask

16. P Stripe Implant

17. Interlayer Dielectric

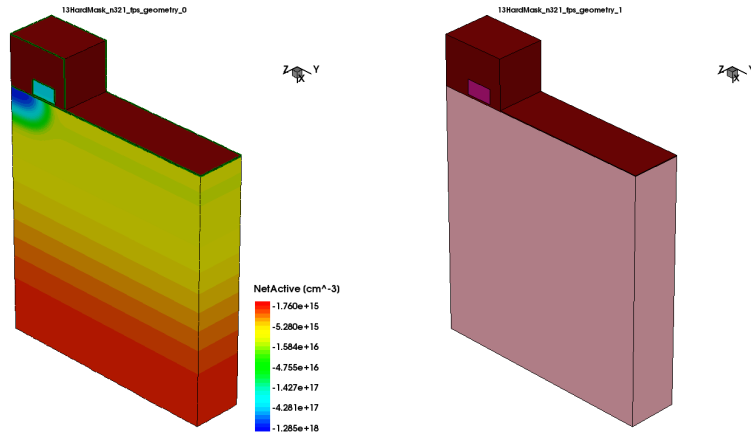


Figure 4.7: 3D TCAD SJ-LDMOS Sentaurus Process Simulation: Drift Region Oxide Hard Mask

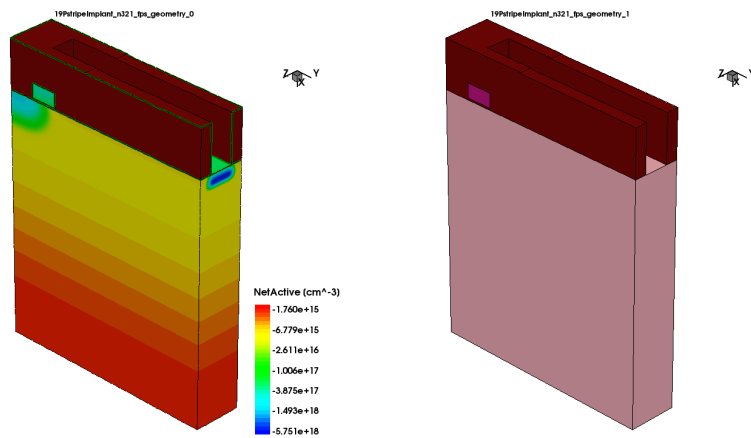


Figure 4.8: 3D TCAD SJ-LDMOS Sentaurus Process Simulation: P Stripe Implant

18. P+ Trench Etch

19. Source Drain Anneal

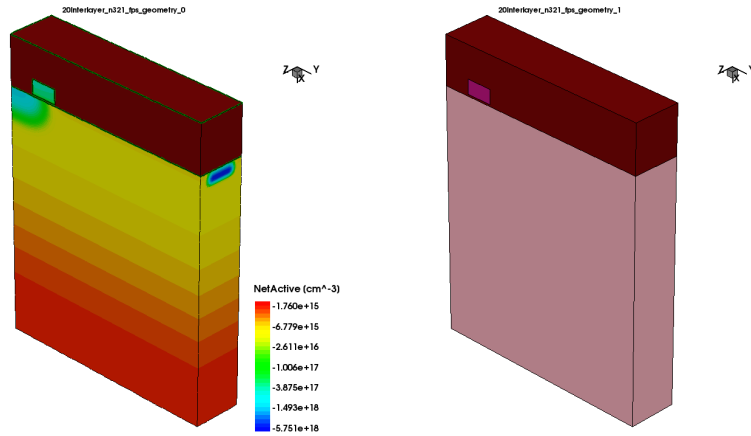


Figure 4.9: 3D TCAD SJ-LDMOS Sentaurus Process Simulation: Interlayer Dielectric

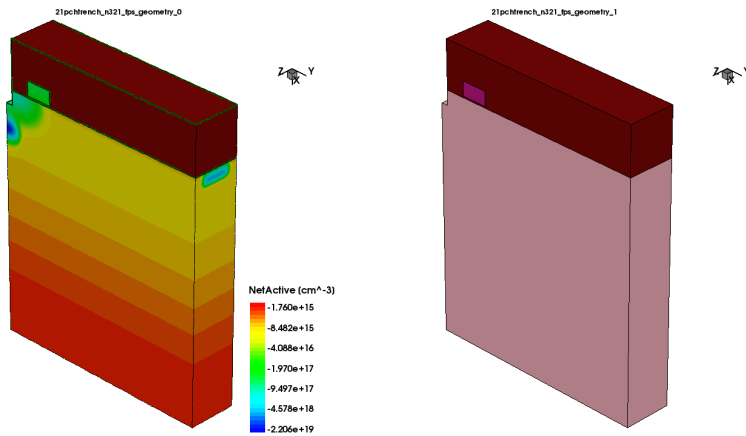


Figure 4.10: 3D TCAD SJ-LDMOS Sentaurus Process Simulation: P+ Trench Etch

4.2 TCAD Device Simulation

This project provides the device simulation for the parameters extraction of the Super Junction Laterally Diffused MOS (SJ LDMOS), such as Specific On-state Resistance and Breakdown Voltage, using Synopsys TCAD Sentaurus tools.

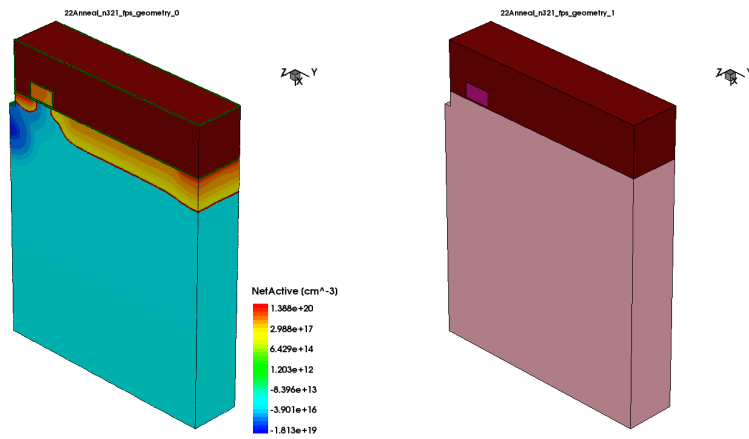


Figure 4.11: 3D TCAD SJ-LDMOS Sentaurus Process Simulation: Source/Drain Anneal

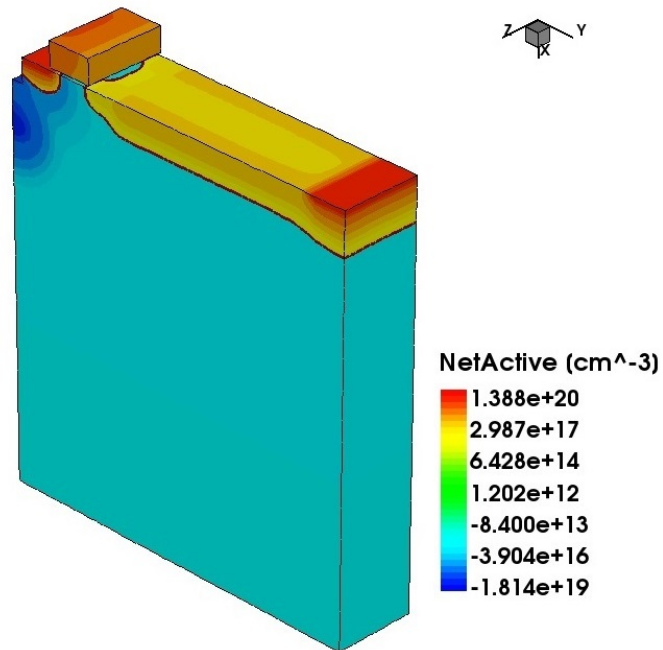


Figure 4.12: 3D TCAD SJ-LDMOS Sentaurus Process Simulation: Net Doping

Table 4.1: Device Specifications of SJ-LDMOS Simulated using Synopsys Sentaurus Process

Parameter	Magnitude
Channel length	1 μm
Drift length, L_d	3 μm
N Stripe width, d_N	0.5 μm
N Stripe Doping, N_N	9e12
P Stripe width, d_P	0.5 μm
P Stripe Doping, N_P	9e12
Gate Oxide Thickness, t_{ox}	300nm

The device simulation is performed using Synopsys Sentaurus Device simulator; it simulates numerically the electrical behavior of the SJ LDMOS in isolation or several physical devices combined in a circuit.

Terminal currents, voltages, and charges are computed based on a set of physical device equations that describes the carrier distribution and conduction mechanisms.

The SJ LDMOS device of this project, is represented in the simulator as a "virtual" device whose physical properties are discretized onto a nonuniform "grid" (or "mesh") of nodes. Therefore, this virtual device is an approximation of the real SJ LDMOS device.

Continuous properties such as doping profiles are represented on a sparse mesh and, therefore, are only defined at a finite number of discrete points in space. The doping at any point between nodes (or any physical quantity calculated by Sentaurus Device) can be obtained by interpolation [21].

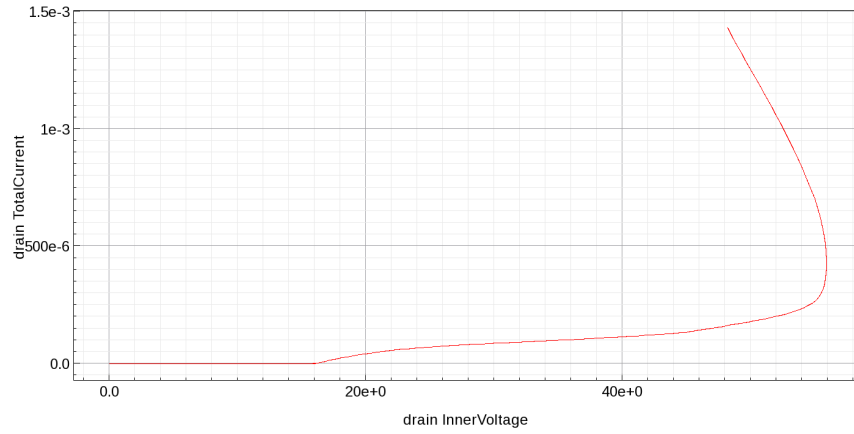


Figure 4.13: 3D TCAD SJ-LDMOS Sentaurus Device Simulation: Breakdown Voltage

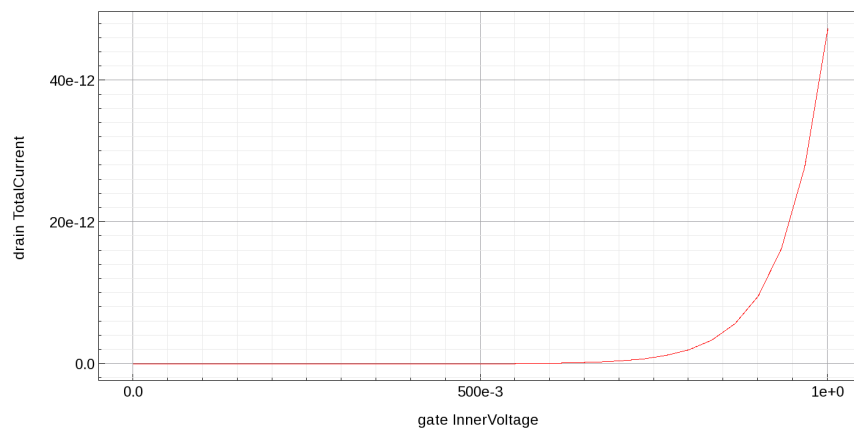


Figure 4.14: 3D TCAD SJ-LDMOS Sentaurus Device Simulation: Threshold Voltage

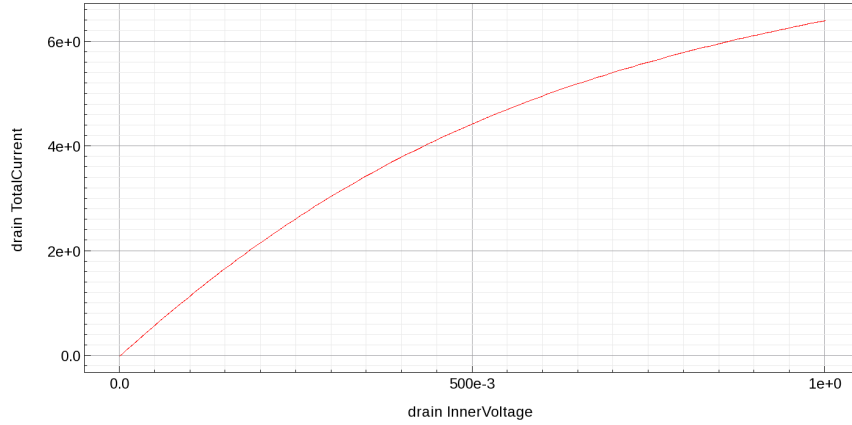


Figure 4.15: 3D TCAD SJ-LDMOS Sentaurus Device Simulation: Specific on-state resistance

Table 4.2: Device Specifications of SJ-LDMOS Simulated using Synopsys Sentaurus Process

Parameter	Magnitude
Channel length	1 μm
Drift length, L_d	3 μm
N Stripe width, d_N	0.5 μm
N Stripe Doping, N_N	9e12
P Stripe width, d_P	0.5 μm
P Stripe Doping, N_P	9e12
Gate Oxide Thickness, t_{ox}	300nm

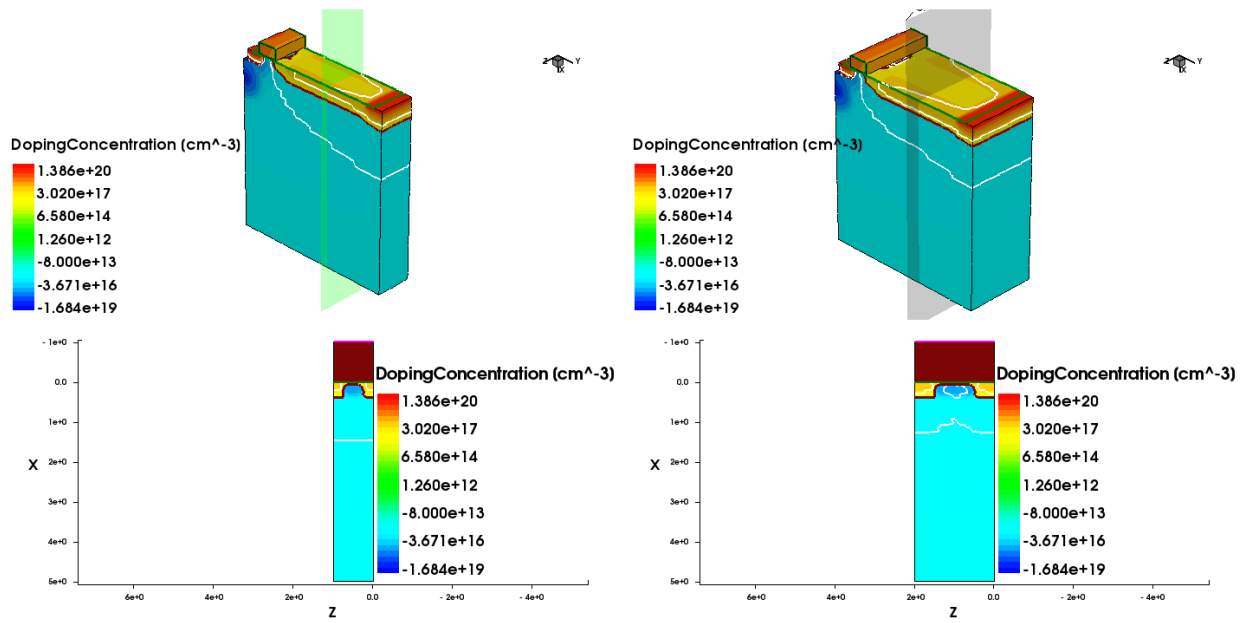


Figure 4.16: 3D TCAD SJ-LDMOS Sentaurus Device Simulation: Stripe Widths

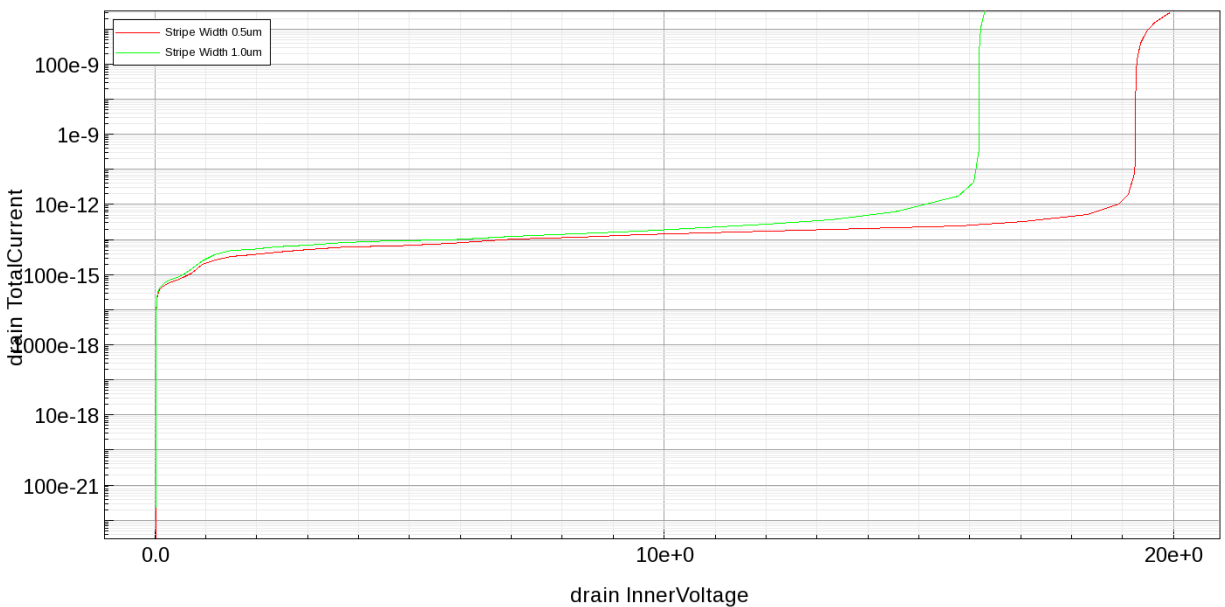


Figure 4.17: 3D TCAD SJ-LDMOS Sentaurus Device Simulation: Stripe Widths

Table 4.3: Device Simulation Results

Pwell	DriftLenght	StripeWidth	PCH	NwellDrift	pStripeDose	BV
2.00E+12	3	0.5	5.00E+13	9.00E+12	1.70E+13	19.907
2.00E+12	3	0.5	5.00E+13	9.00E+12	0	22.636
2.00E+12	3	0.5	5.00E+14	9.00E+12	0	20.807
2.00E+12	3	0.5	5.00E+14	9.00E+12	1.80E+12	21.713
2.00E+12	3	1.0	5.00E+13	9.00E+12	1.70E+13	16.284
2.00E+12	4	0.5	5.00E+13	9.00E+12	0	22.851
2.00E+12	4	0.5	5.00E+13	9.00E+12	1.70E+13	20.128
2.00E+12	6	0.5	5.00E+13	9.00E+12	0	22.801
2.00E+12	6	0.5	5.00E+13	9.00E+12	1.70E+13	19.604

Table 4.4: Device Simulation Results

DriftLenght	StripeWidth	PCH	NwellDrift	pStripeDose	BV	Vth	RDSON
3	0.5	5.00E+13	3.00E+13	1.00E+13	18.721	0.809	5.35E-02
3	0.5	5.00E+13	2.00E+13	2.00E+13	13.848	0.815	8.54E-02
3	0.5	5.00E+14	2.00E+13	1.00E+13	17.407	0.81	5.99E-02
3	0.5	5.00E+14	1.00E+13	1.00E+13	19.368	0.812	7.75E-02
3	0.5	5.00E+14	1.00E+13	1.00E+12	22.191	0.794	4.13E-02
3	0.5	5.00E+14	1.00E+13	1.00E+11	22.017	0.784	3.90E-02
3	0.5	5.00E+14	9.00E+12	1.80E+13	16.278	0.816	
3	0.5	5.00E+14	9.00E+12	1.70E+13	17.164	0.816	
3	0.5	5.00E+14	9.00E+12	1.60E+13	17.537	0.815	
3	0.5	5.00E+14	9.00E+12	1.50E+13	17.733	0.815	
3	0.5	5.00E+14	9.00E+12	1.40E+13	17.932	0.814	9.98E-02
3	0.5	5.00E+14	9.00E+12	1.20E+13	18.57	0.814	9.10E-02
3	0.5	5.00E+14	9.00E+12	1.00E+13	19.813	0.813	8.16E-02
3	0.5	5.00E+14	9.00E+12	9.00E+12	20.944		7.68E-02
3	0.5	5.00E+14	9.00E+12	8.00E+12	22.234	0.811	7.17E-02
3	0.5	5.00E+14	9.00E+12	4.00E+12	22.968	0.804	5.28E-02
3	0.5	5.00E+14	9.00E+12	1.00E+12	22.471	0.795	4.25E-02

CHAPTER 5: CONCLUSION AND FUTURE WORK

In the medium- and high-voltage MOSFETs, the resistance is dominated by doping concentration and thickness of the drift region. However, in low voltage LDMOS, which is the target of the present work, that is not the case. When compared with the conventional LDMOS with the same drift and channel length, the simulation of the SJ LDMOS, shows an increment of the BV by 68 percent but also an increment of the R substantially (more than 100 percent), due to: i-) the implementation of the SJ in the drift region reduces the area for the current to flow, therefore increasing the resistance and ii-) the channel resistance and the charge accumulation layer resistance are the dominant factors in the total on-resistance of the device. These resistances account more than 80 percent of the total resistance in this SJ LDMOS. Therefore, in order to make a big impact in the overall specific on-resistance, other resistance components must be reduced, such as channel resistance and accumulation resistance, one possible solution could be the SJ FinFET or the SJ TrenchFET LDMOS.

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