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## Design, Simulation and Characterization of Novel Electrostatic Discharge Protection Devices and Circuits in Advanced Silicon Technologies

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*University of Central Florida*



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DESIGN, SIMULATION AND CHARACTERIZATION OF NOVEL  
ELECTROSTATIC DISCHARGE PROTECTION DEVICES AND CIRCUITS  
IN ADVANCED SILICON TECHNOLOGIES

by

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M.S. University of Central Florida, 2016

A dissertation submitted in partial fulfillment of the requirements  
for the degree of Doctor of Philosophy  
in the Department of Electrical and Computer Engineering  
in the College of Engineering and Computer Science  
at the University of Central Florida  
Orlando, Florida

Summer Term  
2017

Major Professor: Kalpathy B. Sundaram

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## ABSTRACT

Electrostatic Discharge (ESD) has been one of the major reliability concerns in the advanced silicon technologies and it becomes more important with technology scaling. It has been reported that more than 35% of the failures in integrated circuits (ICs) are ESD induced. ESD event is a phenomenon that a finite amount of charges transfer between two objects with different potential in a quite short time. Such event contains a large energy and the ICs without proper ESD protection could be destroyed easily, so ESD protection solutions are essential to semiconductor industry.

ESD protection design consists of on-chip and off-chip ESD protection design, and the research works in this dissertation are all conducted in on-chip level, which incorporate the ESD protection devices and circuits into the microchip, to provide with basic ESD protection from manufacturing to customer use. The basic idea of ESD protection design is to provide a path with low impedance which directs most of the ESD current to flow through itself instead of the core circuit, and the ESD protection path must be robust enough to make sure that it does not fail before the core circuit. In this way, proper design on protection devices and circuits should be considered carefully.

To assist the understanding and design of ESD protection, the ESD event in real world has been classified into a few ESD model including Human Body Model (HBM), Machine Model (MM), Charged Device Model (CDM), etc. Some mainstream testing method and industry standard are also introduced, including Transmission Line Pulse (TLP), and IEC 61000-4-2. ESD protection devices including diode, Gate-Grounded N-type MOSFET (GGNMOS),

Silicon Controlled Rectifier (SCR) are basic elements for ESD protection design. In this dissertation, the device characteristics in ESD event and their applications are introduced. From the perspective of the whole chip ESD protection design, the concept of circuit level ESD protection and the ESD clamps are also briefly introduced.

Technology Computer Aided Design (TCAD) and Simulation Program with Integrated Circuit Emphasis (SPICE) simulation is widely used in ESD protection design. In this dissertation, TCAD and SPICE simulation are carried out for a few times for both of pre-tapeout evaluation on characteristics of the proposed device and circuit and post-tapeout analysis on structure operating mechanism.

Automotive electronics has been a popular subject in semiconductor industry, and due to the special requirement of the automotive applications like the capacitive pins, the ESD protection device used in such applications need to be specially designed. In this dissertation, a few SCRs without snapback are discussed in detail. To avoid core circuit damages caused the displacement current induced by the large snapback in conventional SCR, an eliminated/minimized snapback is preferred in a selection of the protection device. Two novel SCRs are proposed for High Voltage (HV), Medium Voltage (MV), and Low Voltage (LV) automotive ESD protection.

The typical operating temperature for ICs is up to 125 °C, however in automotive applications, the operating temperature may extend up to 850 °C. In this way, the characteristics of the ESD protection device under the elevated temperatures will be an essential part to investigate for automotive ESD protection design. In this dissertation, the high temperature characteristics of ESD protection devices including diode and a few SCRs is measured and

discussed in detail. TCAD simulation are also conducted to explain the underlying physical mechanism. This work provides with a useful insight and information to ESD protection design in high temperature applications.

Besides the high temperature environment, ESD protection are also highly needed for electronics working in other extreme environment like the space. Space is an environment that contains kinds of radiation source and at the same time can generate abundant ESD. The ESD adhering to the space systems could be a potential threat to the space electronics. At the same time, the characteristics of the ESD protection part especially the basic protection device used in the space electronics could be influenced after the irradiation in the space. Therefore, the investigation of the radiation effects on ESD protection devices are necessary. In this dissertation, the total ionizing dose (TID) effects on ESD protection devices are investigated. The devices are irradiated with 1.5 MeV He<sup>+</sup> and characterized with TLP tester. The pre- and post-irradiation characteristics are compared and the variation on key ESD parameters are analyzed and discussed. This work offers a useful insight on ESD devices' operation under TID and help with the device designing on ESD protection devices for space electronics.

Single ESD protection devices are essential part constructing the ESD protection network, however the optimization on ESD clamp circuit design is also important on building an efficient whole chip ESD protection network. In this dissertation, the design and simulation of a novel voltage triggered ESD detection circuit are introduced. The voltage triggered ESD detection circuit is proposed in a 0.18 um CMOS technology. Comparing with the conventional RC based detection circuit, the proposed circuit realizes a higher triggering efficiency with a much smaller

footprint, and is immune to false triggering under fast power-up events. The proposed circuit has a better sensitivity to ESD event and is more reliable in ESD protection applications.

The leakage current has been a concern with the scaling down of the thickness of the gate oxide. Therefore, a proper design of the ESD clamp for power rail ESD protection need to be specially considered. In this dissertation, a design of a novel ESD clamp with low leakage current is analyzed. The proposed clamp realized a pretty low leakage current up to 12 nA, and has a smaller footprint than conventional design. It also has a long hold-on time under ESD event and a quick turn-off mechanism for false triggering. SPICE simulation is carried out to evaluate the operation of the proposed ESD clamp.

To my fiancée Xuejiao Yang, my parents Xiaodong Liang and Qingling Guo, and my  
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# TABLE OF CONTENTS

LIST OF FIGURES .....	xiii
LIST OF TABLES .....	xvii
LIST OF ACRONYMS .....	xviii
CHAPTER 1 INTRODUCTION.....	1
1.1 ESD Event and Protection Methodology .....	1
1.2 ESD Models and Testing Standard .....	3
1.2.1 Human Body Model .....	3
1.2.2 Machine Model .....	4
1.2.3 Charged Device Model.....	5
1.2.4 IEC 61000-4-2.....	6
1.2.5 Transmission Line Pulse Tester .....	7
1.3 ESD Protection Device.....	9
1.3.1 Diode .....	9
1.3.2 GGNMOS.....	10
1.3.3 SCR .....	11
1.4 ESD Protection Circuit.....	12
1.4.1 Two-Stage Protection Scheme .....	14
1.4.2 ESD Power Clamp .....	15

1.4.3	ESD Protection for Multi-Power Domain .....	16
1.5	Dissertation Outline.....	17
CHAPTER 2	DESIGN OF NO-SNAPBACK SILICON CONTROLLED RECTIFIER FOR AUTOMOTIVE ESD PROTECTION .....	18
2.1	Introduction .....	18
2.2	NSSCR .....	18
2.3	DCSCR.....	24
2.4	Conclusion.....	28
CHAPTER 3	DESIGN, CHARACTERIZATION AND SIMULATION OF ESD PROTECTION DEVICES UNDER ELEVATED TEMPERATURES.....	29
3.1	Introduction .....	29
3.2	Experiment Setup Description .....	30
3.3	Experimental Result and Discussion.....	31
3.4	Conclusion.....	46
CHAPTER 4	CHARACTERIZATION AND ANALYSIS OF ESD PROTECTION DEVICES UNDER TOTAL IONIZING DOSE IRRADIATION .....	47
4.1	Introduction .....	47
4.2	Experiment Setup Description .....	49
4.3	Experimental Result and Discussion.....	49
4.4	Conclusion.....	56

CHAPTER 5	DESIGN AND SIMULATION OF NOVEL VOLTAGE TRIGGERED ESD	
DETECTION CIRCUIT .....		57
5.1	Introduction .....	57
5.2	Conventional Detection Circuit Operation.....	58
5.3	Novel Detection Circuit Operation and Simulation .....	60
5.4	Conclusion.....	66
CHAPTER 6	DESIGN AND SIMULATION OF NOVEL ESD CLAMP CIRCUIT WITH	
LOW LEAKAGE CURRENT .....		67
6.1	Introduction .....	67
6.2	Proposed Circuit Schematic and Operation .....	68
6.3	Simulation Result and Discussion.....	70
6.4	Conclusion.....	74
CHAPTER 7	SUMMARY AND OUTLOOK .....	76
LIST OF REFERENCES .....		79

## LIST OF FIGURES

Figure 1-1 Drain junction damage induced by ESD stress. ....	2
Figure 1-2 Interconnect damage induced by ESD stress. ....	2
Figure 1-3 ESD protection design window.....	2
Figure 1-4 An equivalent circuit of HBM.....	3
Figure 1-5 An equivalent circuit of MM.....	4
Figure 1-6 An equivalent circuit of CDM.....	5
Figure 1-7 An equivalent circuit of IEC. ....	6
Figure 1-8 An equivalent circuit of TLP tester.....	7
Figure 1-9 Sample I-V characteristics in TLP measurement.....	8
Figure 1-10 Sample DC sweep plot in TLP measurement. ....	8
Figure 1-11 Circuit symbol and cross section view of a P+/NW diode.....	9
Figure 1-12 Circuit symbol and cross section view of a Zener diode. ....	9
Figure 1-13 I-V characteristics of diode. ....	10
Figure 1-14 Equivalent circuit and cross section view with parasite NPN of a GGNMOS. ....	11
Figure 1-15 Equivalent circuit and cross section view with parasite BJTs of a LSCR. ....	12
Figure 1-16 Whole chip ESD protection scheme. ....	13
Figure 1-17 Chip-level ESD testing method.....	13
Figure 1-18 Primary-Secondary protection scheme. ....	14
Figure 1-19 Three-stage RC delay power clamp. ....	15
Figure 1-20 ESD protection scheme for multi-power domain.....	16
Figure 2-1 Cross section view of NSSCR. ....	19

Figure 2-2 Equivalent circuit of NSSCR. ....	19
Figure 2-3 TLP measurement for the NSSCR's with D1 changing from 0.2 $\mu\text{m}$ to 0.6 $\mu\text{m}$ . Inserted graph shows the variation of $V_{t1}$ by changing D1.....	20
Figure 2-4 TLP measurement for the NSSCR's with D2 changing from 1 $\mu\text{m}$ to 4 $\mu\text{m}$ and D1 stays constant at 0.6 $\mu\text{m}$ . ....	20
Figure 2-5 Captured pre-triggering ((a) and (b)) and post-triggering ((c) and (d)) electric field in TCA simulation of the NSSCR. D2 equals to 2 $\mu\text{m}$ in (a) and (c), and D2 equals to 4 $\mu\text{m}$ in (b) and (d). ....	21
Figure 2-6 TLP I-V curves for stacked Cell A and Cell B. ....	23
Figure 2-7 DC measurement of devices under temperature of 25 $^{\circ}\text{C}$ and 125 $^{\circ}\text{C}$ . ....	23
Figure 2-8 Cross section view of DCSCR. ....	24
Figure 2-9 Equivalent circuit and layout geometry of DCSCR.....	25
Figure 2-10 TLP IV characteristics of DCSCR, diode, DTSCR, and LSCR.....	26
Figure 2-11 Cross section view of stacked DCSCR. ....	27
Figure 2-12 TLP I-V characteristics of stacked DCSCR.....	27
Figure 2-13 DC sweep of devices at temperature of 25 $^{\circ}\text{C}$ and 125 $^{\circ}\text{C}$ . ....	28
Figure 3-1 (a) Cross section view of LSCR, (b) TLP I-V characteristics of LSCR, and (c) $V_{BD}$ , $V_t$ and $V_h$ versus temperature. ....	33
Figure 3-2 (a) Simulated cross section view of LSCR, (b) Simulated quasi-static I-V characteristics of LSCR with log scale y, (c) Captured electric field at NW/PW junction under various ambient temperatures. ....	34

Figure 3-3 (a) Cross section view of MLSCR, (b) TLP I-V characteristics of MLSCR, and (c) $V_{BD}$ , $V_t$ and $V_h$ versus temperature. ....	36
Figure 3-4 (a) Cross section view of NSSCR, (b) TLP I-V characteristics of NSSCR, and (c) $V_{BD}$ , $V_t$ and $V_h$ versus temperature.....	39
Figure 3-5 (a) Cross section view of LVTSCR, (b) TLP I-V characteristics of LVTSCR, and (c) $V_t$ and $V_h$ versus temperature.....	40
Figure 3-6 (a) Simulated cross section view of LVTSCR, (b) Simulated quasi-static I-V characteristics of LVTSCR with log scale y. ....	41
Figure 3-7 (a) Cross section view of PSTSCR, (b) TLP I-V characteristics of PSTSCR, and (c) $V_{BD}$ , $V_t$ and $V_h$ versus temperature. ....	43
Figure 3-8 (a) Structure of P+/NW diode, (b) TLP I-V characteristics of forward-biased diode, and (c) TLP I-V characteristics of reversed-biased diode. ....	45
Figure 4-1 (a) Cross-section view of P+/NW diode, (b) TLP I-V characteristics of forward-biased diode (solid line for measurement and dashed line for DC leakage current), and (c) TLP I-V characteristics of reverse-biased diode (solid line for measurement and dashed line for DC leakage current).....	51
Figure 4-2 (a) Cross-section view of Zener diode, and (b) TLP I-V characteristics of Zener diode (solid line for measurement and dashed line for DC leakage current). ....	52
Figure 4-3 (a) Cross-section view of GGNMOS, and (b) TLP I-V characteristics of GGNMOS (solid line for measurement and dashed line for DC leakage current). ....	54
Figure 4-4 (a) Cross-section view of LSCR, and (b) TLP I-V characteristics of LSCR (solid line for measurement and dashed line for DC leakage current).....	55



Figure 5-1 Schematic of the conventional voltage triggered $2 \times V_{DD}$ -tolerant ESD detection circuit and the clamping device. ....	58
Figure 5-2 Relationship between $R_0$ and Triggering Current. ....	59
Figure 5-3 Schematic of the proposed voltage triggered $2 \times V_{DD}$ -tolerant ESD detection circuit. ....	61
Figure 5-4 Nodes voltages of the proposed circuit in under $2 \times V_{DD}$ condition. ....	62
Figure 5-5 (a) Nodes voltages and (b) triggering current of the proposed circuit under the ESD stress. ....	64
Figure 5-6 Turn-on performance of the proposed circuit. ....	65
Figure 5-7 Triggering current of proposed circuit under fast power-up events. ....	65
Figure 6-1 Schematic of proposed ESD clamp circuit. ....	69
Figure 6-2 Waveforms of the nodes voltages under the ESD event. ....	71
Figure 6-3 Waveforms of the nodes voltages and leakage current under normal condition. ....	72
Figure 6-4 Waveforms of nodes voltage under HBM simulation. ....	73
Figure 6-5 Waveforms of gate voltage under fast power-up event. ....	74

## LIST OF TABLES

Table 1-1 HBM classification criteria by JEDEC.....	4
Table 1-2 MM classification criteria by JEDEC.....	5
Table 1-3 CDM classification criteria by JEDEC.....	6
Table 2-1 Layout parameter of Cell A and Cell B.....	22
Table 2-2 Comparison of devices on key ESD parameters. ....	28
Table 3-1 Summary of ESD Parameters Variations with Increasing Temperature. ....	45
Table 4-1 Summary of Irradiation Setup. ....	49
Table 4-2 Summary of TID Effects on Key ESD Parameters. ....	56
Table 5-1 Dimensions of Devices Used in the Proposed Detection Circuit. ....	60
Table 6-1 Dimensions of Devices Used in the Proposed Detection Circuit. ....	70

## LIST OF ACRONYMS

BCD	Bipolar-CMOS-DMOS
BJT	Bipolar Junction Transistor
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide-Semiconductor
DMOS	Doublediffusion Metal-Oxide-Semiconductor
DCSCR	Direct-Connected Silicon Controlled Rectifier
DUT	Device Under Test
EOS	Electrical Overstress
ESD	Electrostatic Discharge
GGNMOS	Grounded-Gate N-type MOSFET
HBM	Human Body Model
HMM	Human Metal Model
HV	High Voltage
IC	Integrated Circuit
IEC	International Electrotechnical Commission
LSCR	Lateral Silicon Controlled Rectifier
LV	Low Voltage
LVTSCR	Low Voltage Triggering Silicon Controlled Rectifier
MLSCR	Modified Lateral Silicon Controlled Rectifier

MM	Machine Model
MV	Medium Voltage
NSSCR	No-Snapback Silicon Controlled Rectifier
PBT	Parasite Bipolar Transistor
PIN	P-type/Intrinsic/N-type
PSTSCR	P-Substrate Triggered Silicon Controlled Rectifier
SCR	Silicon Controlled Rectifier
SEE	Single Event Effect
SoC	System-on-a-Chip
SPICE	Simulation Program with Integrated Circuit Emphasis
TCAD	Technology Computer Aided Design
TID	Total Ionizing Dose
TLP	Transmission Line Pulse

# CHAPTER 1 INTRODUCTION

## 1.1 ESD Event and Protection Methodology

Electrostatic Discharge, which is usually abbreviated as ESD, is a natural phenomenon that people are familiar with even in their daily life. Conceptually, it is a phenomenon that a finite amount of charges transfer between two objects with the different potential in a very short time, which is as short as nanosecond (ns) to millisecond (ms) [1]. The short duration of ESD event is one of its major characteristics. The other major characteristics of ESD is its high energy, which could results in a high voltage at the level of a few kilovolts (kV) and large current at the level of amps (A). Such a high voltage and large current induced by ESD could cause serious damages to semiconductor device or circuits, so ESD has been one of the major reliability concern in semiconductor industry. The example of silicon and interconnect damages induced by ESD are shown in Figure 1-1 [2] and Figure 1-2 [3], respectively.

The basic idea of ESD protection design is to add a path with a low impedance to shunt the ESD current away from the internal core circuit as well as to clamp the I/O and power pad voltage to a relative safe level. There are also some of other requirement for ESD protection design including a quick and accurate response to ESD events, a low parasite which brings in minimal influence to the core circuit function, a small footprint, a high ESD robustness, and the proposed design should fit in the ESD design window [4]. Figure 1-3 shows the scheme of ESD design window. ESD design window is a design voltage range defined between edges of the normal operation voltage and the gate oxide breakdown voltage. In Figure 1-3, the I-V characteristics of the snapback and non-snapback type ESD protection device are depicted with

solid and dash line, respectively. The I-V characteristics of the devices should always stay within the ESD design window.

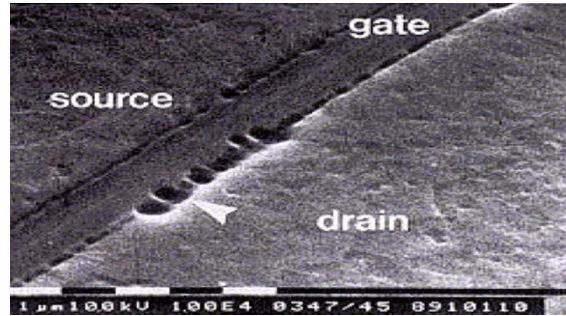


Figure 1-1 Drain junction damage induced by ESD stress.

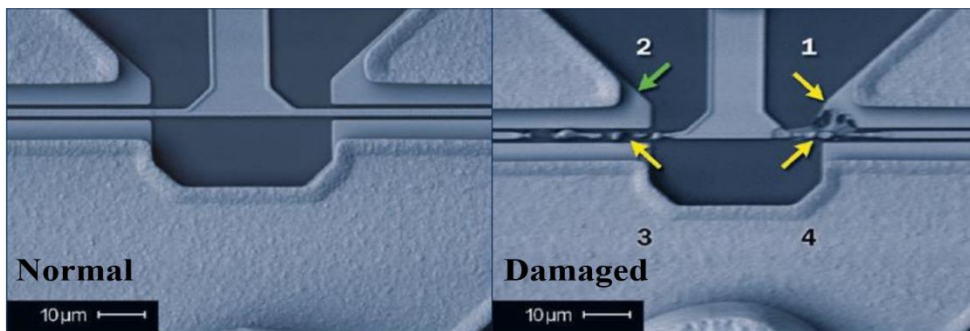


Figure 1-2 Interconnect damage induced by ESD stress.

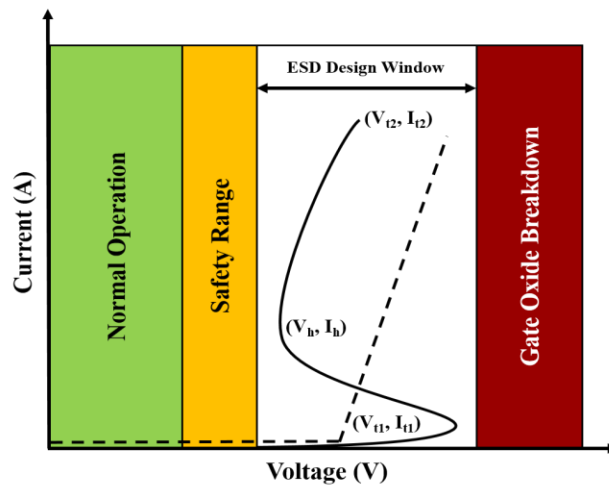


Figure 1-3 ESD protection design window.

## 1.2 ESD Models and Testing Standard

ESD event is a phenomenon happened in nature. To better understand the ESD events, and mimic the ESD events in real world to assist the designing process of ESD protection, the ESD events have been classified into a few models including Human Body Model (HBM), Machine Model (MM), Charged Device Model (CDM), and some testing standards and techniques are proposed to guide the ESD protection design, including IEC 61000-4-2, and Transmission Line Pulse (TLP) Tester. Standard testing will be conducted following the published ESD standards to evaluate the product performance under different ESD stress.

### 1.2.1 Human Body Model

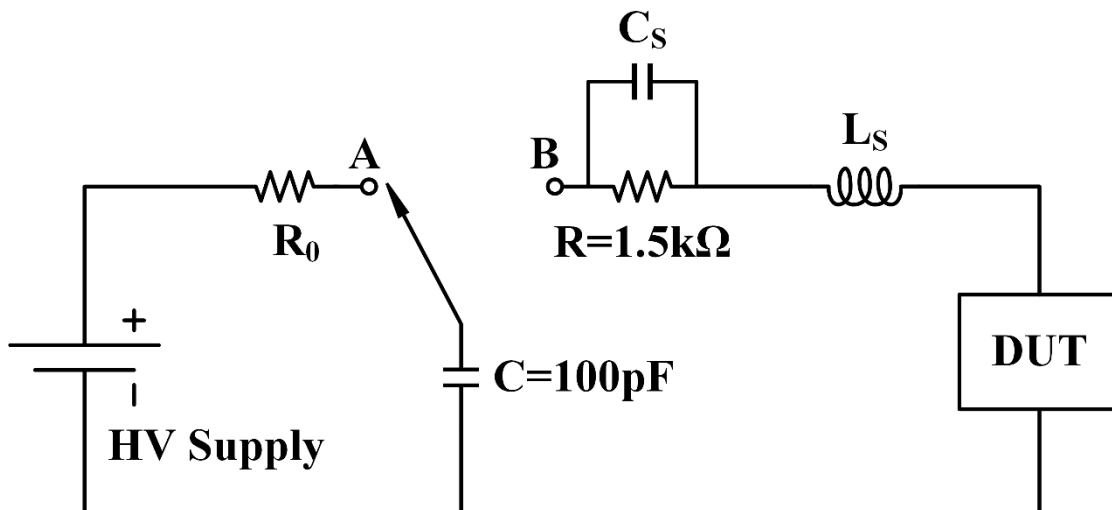


Figure 1-4 An equivalent circuit of HBM.

HBM is proposed to mimic a charged human body in the ESD event. Semiconductor products are suspect to HBM type ESD stress from manufacturing to applications. Typically, it has a rise time of 2 to 10 ns, and a decay time of 130 to 170 ns. Figure 1-4 shows an equivalent

circuit of the HBM. In the equivalent circuit, there are two key elements including an ESD capacitor of 100 pF and an ESD resistor of 1500  $\Omega$  are key elements. There are a few popular HBM standards published by different organization including MIL-STD-883E [5], JESD22-A114F [6], etc. HBM is one of the most important ESD standard for semiconductor IC and according to the threshold failure voltage in the HBM testing, the HBM level has been classified into seven levels in the HBM standard published by JEDEC. Table 1-1 shows the HBM classification criteria published by JEDEC.

Table 1-1 HBM classification criteria by JEDEC.

Classification	Voltage Range (V)
0	< 250
1A	250 to < 500
1B	500 to < 1000
1C	1000 to < 2000
2	2000 to < 4000
3A	4000 to < 8000
3B	> 8000

### 1.2.2 Machine Model

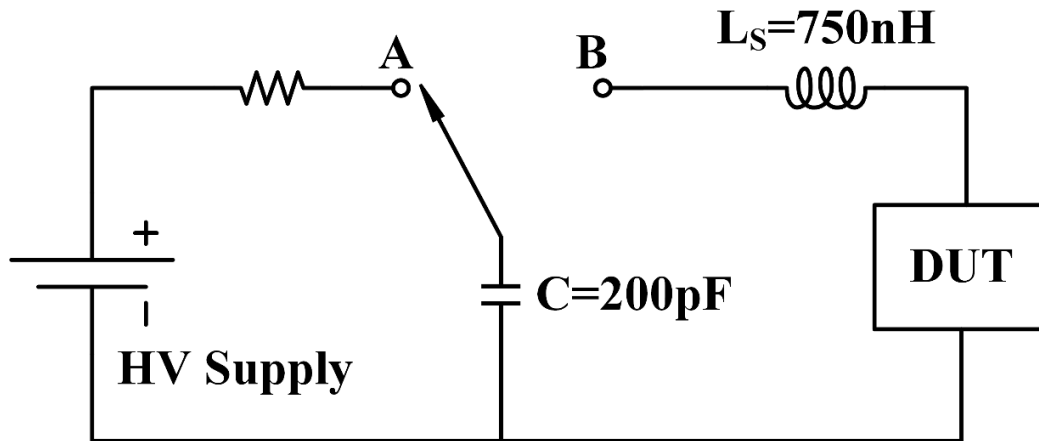


Figure 1-5 An equivalent circuit of MM.



MM is a model to simulate the charged equipment which could generate a ESD pulse with a rise time of 6 to 8 ns and a decay time of 66 to 90 ns [4]. JESD22-A115A [7] is a standard published by JEDEC which is popular in industry. Like HBM, MM has been classified into three levels based on the passing level 200 V and 400 V. Table 1-2 shows the MM classification criteria published by JEDEC [7]. Figure 1-5 shows the equivalent circuit of MM, and an ESD inductor of 750 nH and an ESD capacitor of 200 pF are included in the circuit.

Table 1-2 MM classification criteria by JEDEC.

Classification	Voltage Range (V)
A	< 200
B	200 to < 400
C	> 400

### 1.2.3 Charged Device Model

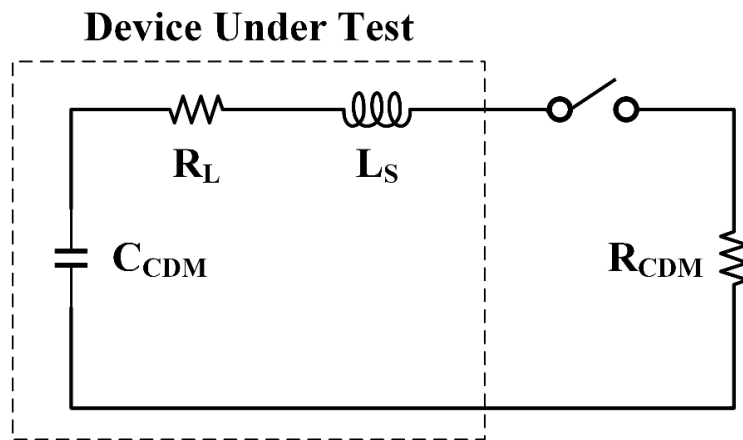


Figure 1-6 An equivalent circuit of CDM.

CDM is another important model in ESD protection design. It mimics an event that a self-charged device discharge through its pin when the pin touches the grounded objects. CDM has a rise time of 200 to 400 ps and a pulse width of  $1 \pm 0.5$  ns [4]. Figure 1-6 shows an

equivalent circuit of CDM, and for a 500 V CDM, the circuits consists of a ESD capacitor of 10 pF, a ESD resistor of 10  $\Omega$ , a load resistor of 10  $\Omega$  and a ESD inductor of 10 nH. JESD22-C101D [8] is a popular CDM standard published by JEDEC, and the CDM has been classified into 4 levels based on its passing level. Table 1-3 shows the CDM classification criteria by JEDEC [8].

Table 1-3 CDM classification criteria by JEDEC.

Classification	Voltage Range (V)
I	< 200
II	200 to < 500
III	500 to < 1000
IV	> 400

#### 1.2.4 IEC 61000-4-2

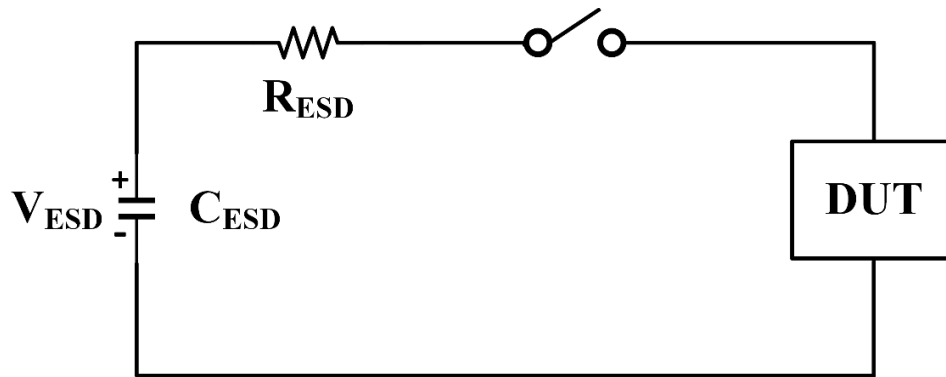


Figure 1-7 An equivalent circuit of IEC.

IEC 61000-4-2 is a standard published aimed the system-level ESD protection. It mimics a charged human body with a metal object and then discharge to the system. There are two types of discharge in IEC standard, the air-gap discharge and direct discharge. The IEC event has a rise time of 0.7 to 1 ns, and a duration of around 80 ns [4]. In the equivalent circuit of IEC model, it consists of a ESD capacitor of 150 Pf and a ESD resistor of 330  $\Omega$ . In a IEC event, it could

generate a ESD pulse up to 30 kV and first peak current of 3.75 A/kV [4, 9, 10]. Figure 1-7 shows the equivalent circuit of the IEC model.

### 1.2.5 Transmission Line Pulse Tester

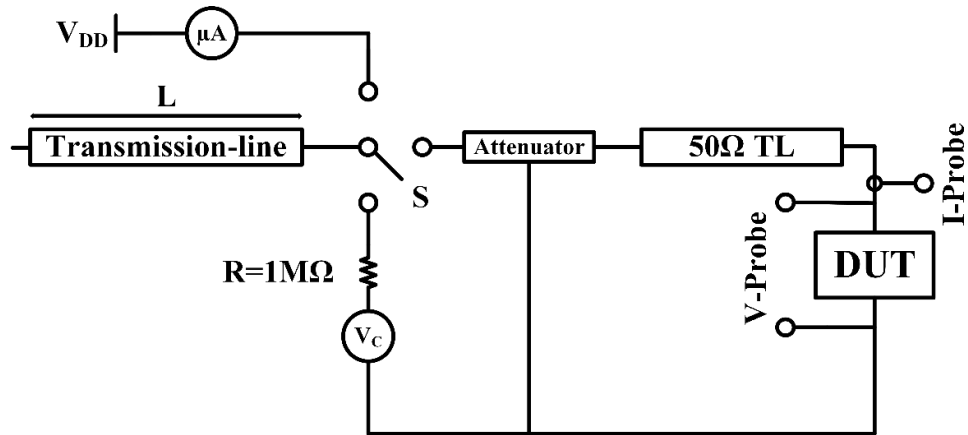


Figure 1-8 An equivalent circuit of TLP tester.

Transmission Line Pulse Tester (TLP) is not a standard, but a testing method which could generate a ESD-like pulse with a rise time of 0.5 to 10 ns and a pulse width of 50 to 150 ns [4, 11]. The testing standards introduced in previous sections including HBM, MM, CDM and IEC are all destructive testing method, which means you could get a failure threshold of the device under test (DUT), however the device is destroyed when you obtain the threshold. Compared to these destructive testing method, TLP is a non-destructive testing way which could offer insights to failure mechanism [4]. The pulse starts at a very low voltage level and the zap voltage increase with a certain voltage step. Key ESD parameters could be obtained from the TLP measurement, including triggering voltage/current  $V_{t1}/I_{t1}$ , holding voltage/current  $V_h/I_h$ , failure voltage/current  $V_{t2}/I_{t2}$ , DC leakage current, On-Resistance  $R_{ON}$  and DC breakdown voltage  $V_{BD}$ . With a certain rise time and pulse width, the TLP could set up a correlation between other ESD models, like the

TLP pulse with a rise time of 10 ns and a pulse width of 100 ns, is used to correlate a HBM pulse with a ESD resistor of 1500  $\Omega$  [1]. Figure 1-8 shows the equivalent circuit of the TLP tester [11]. A sample TLP I-V measurement and DC sweep measurement are shown in Figure 1-9 and Figure 1-10, respectively.

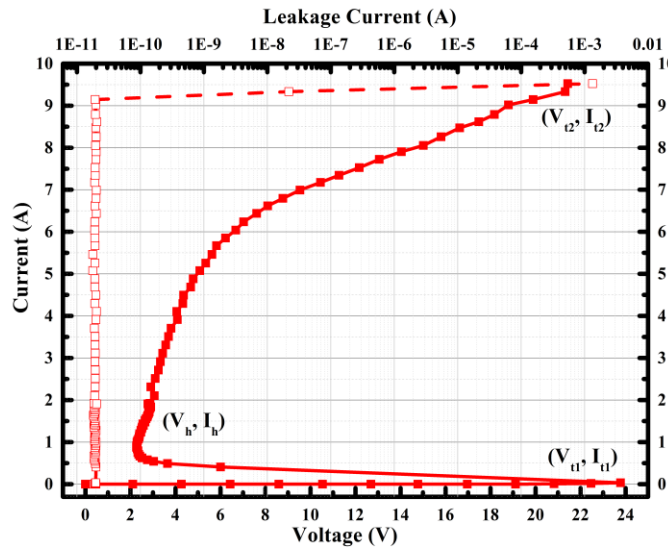


Figure 1-9 Sample I-V characteristics in TLP measurement.

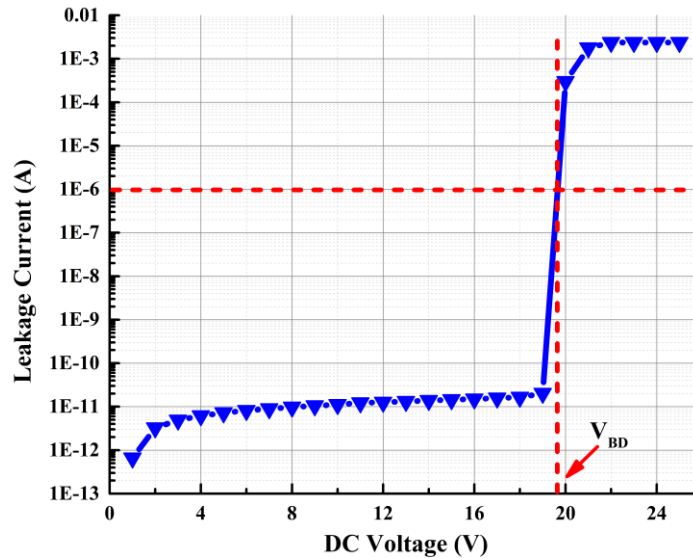


Figure 1-10 Sample DC sweep plot in TLP measurement.

### 1.3 ESD Protection Device

After introducing the concept of ESD event, we will continue with the topic of ESD design. In the ESD design, some basic semiconductor devices could be directly used as ESD protection devices, like the diode in forward bias. Some other devices need to be modified to adapt to the ESD protection design, like the Grounded Gate N-type MOSFET (GGNMOS). There are also some other novel devices like Silicon Controlled Rectifier (SCR) proposed specially for ESD protection design. In this section, we will introduce the basic concept of the ESD protection devices and its operation under ESD events.

#### 1.3.1 Diode

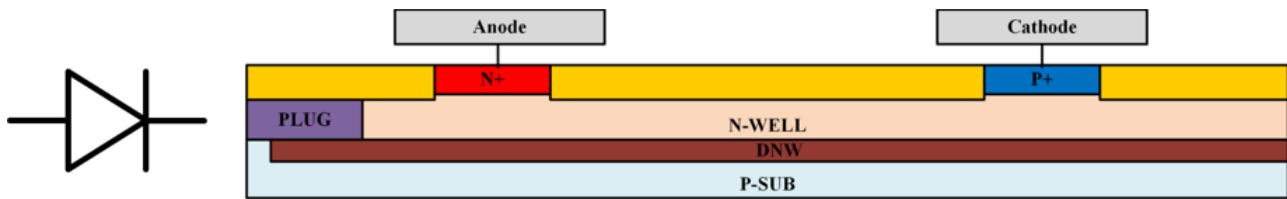


Figure 1-11 Circuit symbol and cross section view of a P+/NW diode.

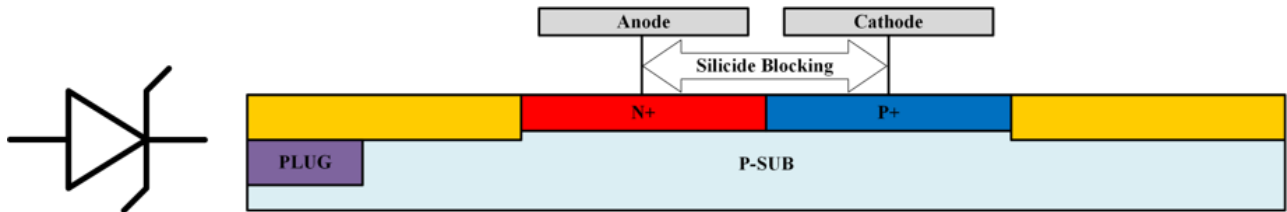


Figure 1-12 Circuit symbol and cross section view of a Zener diode.

Diode is one of the mostly used device for ESD protection design due to its high protection efficiency in its forward bias [11]. And because of its no-snapback characteristics, it is perfect for modeling, which could be used in the circuit simulation [4]. Zener diode in reversed

bias could also be used in ESD protection. Figure 1-11 and Figure 1-12 show the circuit symbol and cross section view of a P+/NW diode and a Zener diode, respectively [4]. And the I-V characteristics of the diode is shown in Figure 1-13. Because of its low turn on voltage, stacked diodes are usually used for a higher voltage node. However, due to the parasite Bipolar Junction Transistor (BJT) in the stacked diodes, the structure is suspect to the Darlington effect [11] and has a concern to the footprint.

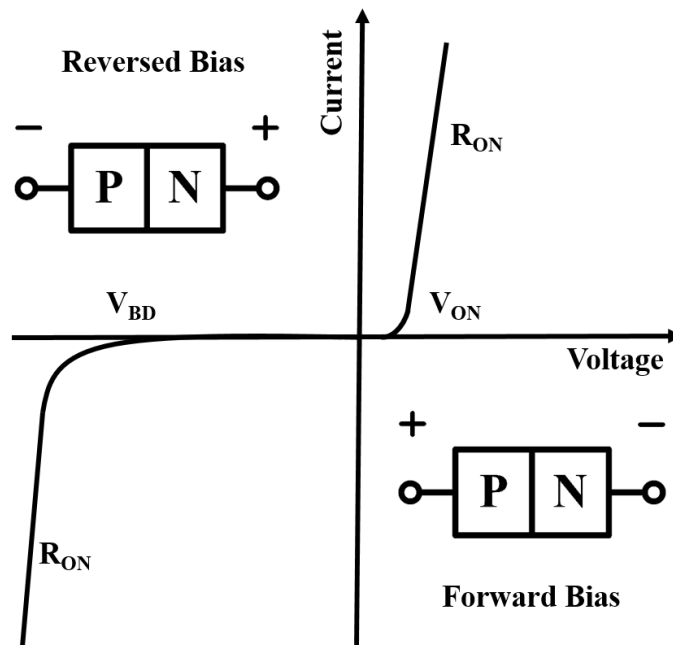


Figure 1-13 I-V characteristics of diode.

### 1.3.2 GGNMOS

GGNMOS is a variation based on the normal NMOS. In the ESD design, the drain of NMOS serves as the anode, and the shorted gate, source and body contact serve as the cathode. Figure 1-14 shows the equivalent circuit and cross section view with parasite BJT of a GGNMOS.

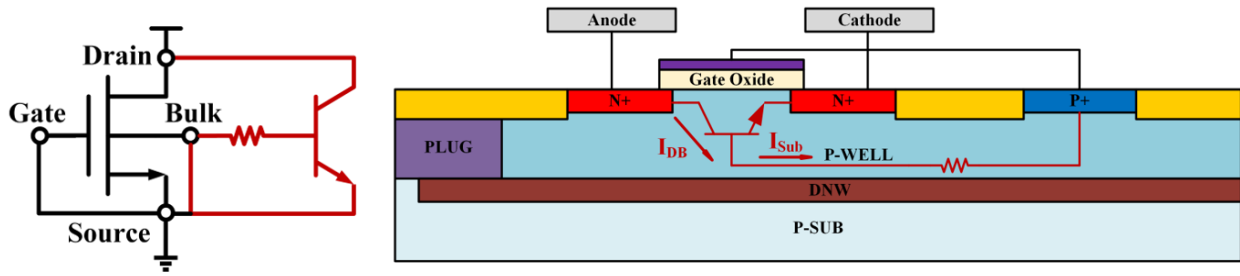


Figure 1-14 Equivalent circuit and cross section view with parasite NPN of a GGNMOS.

In a ESD event, the ESD pulse arrives at the anode, and the drain voltage increases and leads to an increasing drain-body current, which contributes to the total substrate current. As the bias at the PW/N+ junction increase and when  $V_{BE}$  of the parasite BJT exceeds 0.7 V, the parasite NPN turns on. The drain voltage at this moment is the triggering voltage of the device. After GGNMOS turning on, the drain voltage drops to a lower level due to the bipolar action in the device which we call holding voltage. With drain voltage further increases, it finally reaches the thermal failure [4, 11].

Due to its relative low triggering voltage, it is usually used in applications requiring fast turn-on in ESD event. And in real application, the GGNMOS is usually designed as a multi-finger layout style, and a silicide-block could be used to obtain a better triggering behavior.

### 1.3.3 SCR

SCR is one of the most popular device because of its high efficiency on ESD robustness and footprint [12]. The cross section view and the equivalent circuit of a Lateral SCR (LSCR) are shown in Figure 1-15 [4].

In an ESD event, when ESD pulse arrives at the anode, the anode voltage increases, and the electric field at the NW/PW junction increases. Finally, the avalanche breakdown happens at the NW/PW junction and the current anode voltage is the triggering voltage. Due to the impact

ionization after the device turning on, the junction finally get into the conductivity modulation. Because of the strong bipolar action at the breakdown junction, the anode voltage drop to a lower voltage level and the device exhibits a snapback-type I-V characteristics [13]. With anode voltage continue to increase, it finally reaches the thermal failure. Because of its very high triggering voltage and the low holding voltage, the LSCR could not directly used in the ESD protection design, and it need to be improved to adapt to the different ESD design window.

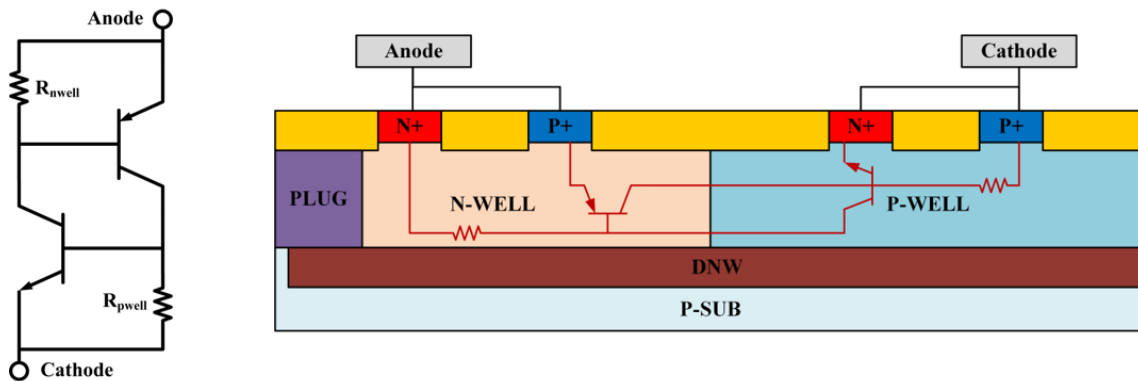


Figure 1-15 Equivalent circuit and cross section view with parasite BJTs of a LSCR.

#### 1.4 ESD Protection Circuit

We introduced the basic ESD protection devices in last section, and in actual ESD protection design, the ESD protection elements in circuit level are also widely used, which we call ESD clamp, and the ESD protection devices are key elements used in the ESD clamps. Figure 1-16 shows a scheme for a whole chip ESD protection [4]. Proper clamp should be designed and placed between any combination of I/O,  $V_{DD}$ ,  $V_{SS}$ . To verify the ESD protection design in a chip, the chip should be tested in a standard method. Figure 1-17 shows the typical



standard ESD testing method of a chip. ESD testing should be conducted between every two I/O, I/O to  $V_{DD}$  (PD),  $V_{DD}$  to I/O (ND), I/O to  $V_{SS}$  (PS), and  $V_{SS}$  to I/O (NS) [14].

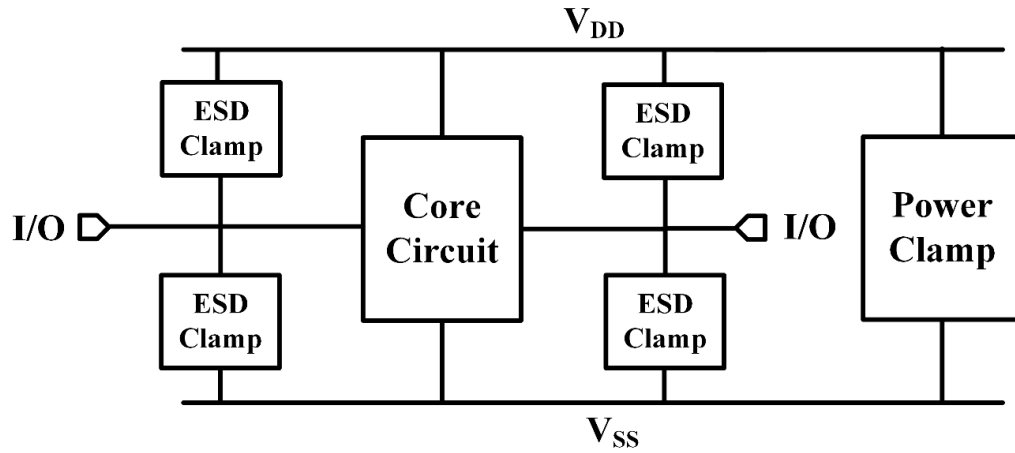


Figure 1-16 Whole chip ESD protection scheme.

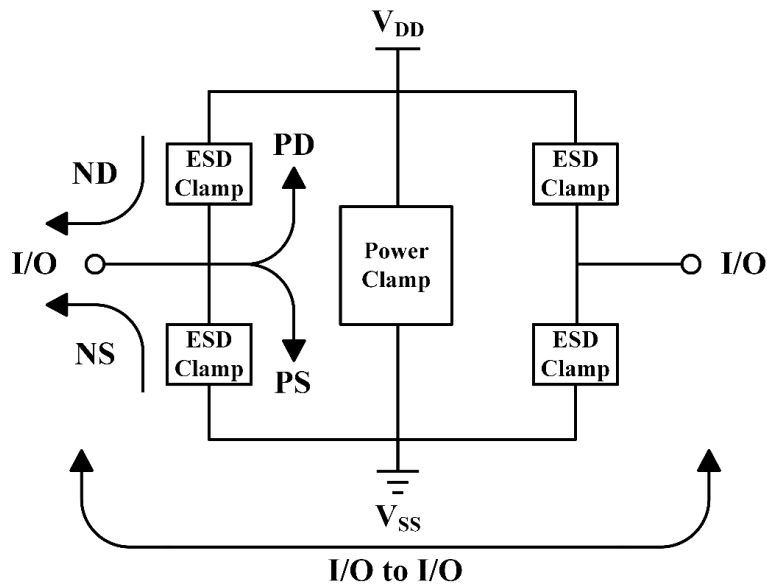


Figure 1-17 Chip-level ESD testing method.

### 1.4.1 Two-Stage Protection Scheme

In some ESD event, the single protection device could not turn on fast enough and induce a overshoot voltage which could destroy the gate of the inner circuit. In this case, the two-stage ESD protection design is proposed, which we also call Primary-Secondary protection scheme. The structure consists of a primary clamp, a secondary clamp as well as an isolation resistor. Figure 1-18 shows the schematic of the two-stage clamp [4, 11, 14]. In an ESD event, the ESD pulse goes into the I/O and the secondary clamp firstly turns on to shunt part of the ESD current. Device with fast turn-on speed like diode in forward bias and GGNMOS could be used as the secondary clamp. The isolation resistor is used to limit the current flowing through the resistor to avoid damage to inner gate and build up the voltage to trigger the primary clamp. The primary clamp may have a slower turn-on speed than the secondary clamp, but will shunt the most of the ESD current after turned on. Devices with high ESD robustness like SCR could be used as primary clamp.

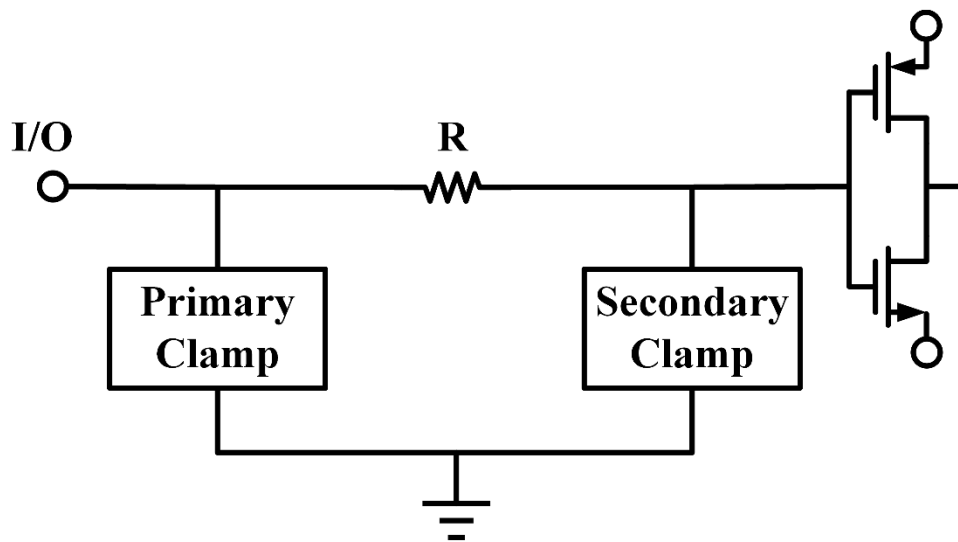


Figure 1-18 Primary-Secondary protection scheme.

### 1.4.2 ESD Power Clamp

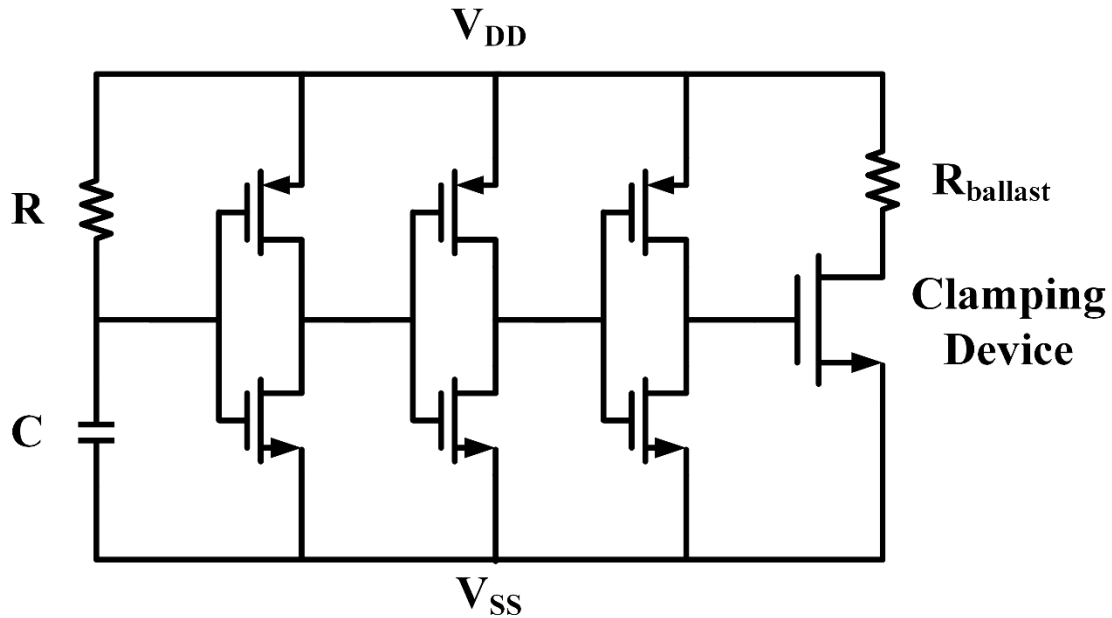


Figure 1-19 Three-stage RC delay power clamp.

We introduced the whole chip ESD protection scheme in previous section, and it is important to design a discharging path between the power line  $V_{DD}$  and  $V_{SS}$ , to optimize the overall discharging path and allow most of the ESD current to flow through. We call such discharging clamp as power clamp. The three-stage RC delay power clamp is one of the mostly used power clamp. It consists of a RC detection part and three inverters in series to serve as the delay buffer. A large MOSFET or SCR serves as the clamping device. Figure 1-19 shows the schematic of a three-stage RC delay power clamp [4, 14]. In a ESD event, the positive voltage difference between the power line and the capacitor turns the PMOS in first inverter on to generate signal 1. The clamping device finally turns on to discharge the ESD current. After the ESD event, the negative voltage difference between the power line and the capacitor makes the

NMOS turns on then turns the clamping device off. Following the clamp operation, we want minimum delay in the turn-on process to ensure fast response to ESD and longer delay in turn-off process to get enough discharging time. We could adjust the width of the PMOS and NMOS to affect the resistance of the MOSFET to control the delay time [14]. The RC delay clamp is controlled by the voltage threshold instead of the rising edge, so it is immune to the false triggering.

### 1.4.3 ESD Protection for Multi-Power Domain

In modern ICs, there are always multiple power domain in a single chip. In this case, the ESD protection design need to be specially considered. One of the most widely used method is to place reversed diode strings in parallel between different power domain. Figure 1-20 shows the design concept of the ESD protection for multi-power domain [4]. The noise from different power domain could be blocked by diode strings because of its rectification characteristics. However, such protection design is not acceptable in low voltage (LV) application due to the  $N \times 0.7$  V voltage drop across the power line (N stands for the number of diodes in the diode string). One possible solution is to introduce the additional common ESD bus for all power domains [4].

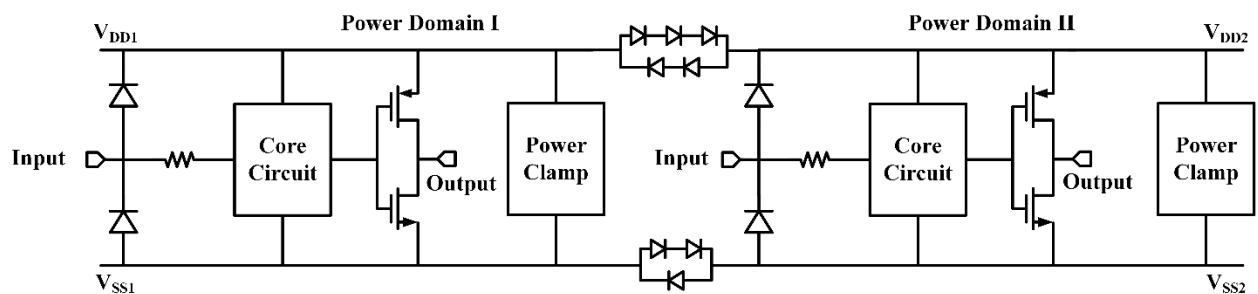


Figure 1-20 ESD protection scheme for multi-power domain.

## 1.5 Dissertation Outline

In this dissertation, design, simulation, and characterization of ESD protection device and circuits are introduced based on a few research works conducted during my Ph.D. study.

Chapter 1 introduces the ESD fundamentals which are helpful to understand this dissertation. In Chapter 2, the design of a few novel SCR-based device without snapback are introduced. In Chapter 3, the investigation of high temperature characteristics of ESD protection devices are introduced. Chapter 4 shows an investigation of the Total Ionizing Dose (TID) effects on ESD protection device. A novel ESD detection circuit and a novel ESD power clamp with low leakage current are introduced in Chapter 5 and Chapter 6, respectively.

## **CHAPTER 2      DESIGN OF NO-SNAPBACK SILICON CONTROLLED RECTIFIER FOR AUTOMOTIVE ESD PROTECTION**

### 2.1 Introduction

Automotive electronics has been a hot topic for the past a few years. Due to the some of the special application of automotive electronics, ESD protection design for automotive application need to be considered specially. In the ESD protection design for the capacitive pins, the snapback in the I-V characteristics of the ESD protection devices is not welcomed. This is because that at the capacitive pins, large voltage difference induced by the large snapback could leads to a large displacement current, which could generate a serious damage to the inner circuit. Thus, a ESD protection device with minimal/without snapback is expected in such application. However, conventional no-snapback device like diode is limited for high voltage (HV) ESD protection, and its protection efficiency is also relative low. Therefore, a no-snapback ESD protection device with a protection efficiency like SCR is expected [12]. In this chapter, two novel SCR-based device structures with minimized/without snapback are introduced including No-Snapback SCR (NSSCR) [13] and Direct-Connected SCR (DCSCR) [15].

### 2.2 NSSCR

Aimed to the HV automotive ESD protection, a novel SCR-based ESD protection device without snapback named NSSCR is proposed in a 0.35 HV Bipolar-CMOS-DMOS (BCD) technology. The cross section view and the equivalent circuit are shown in Figure 2-1 and Figure 2-2, respectively.

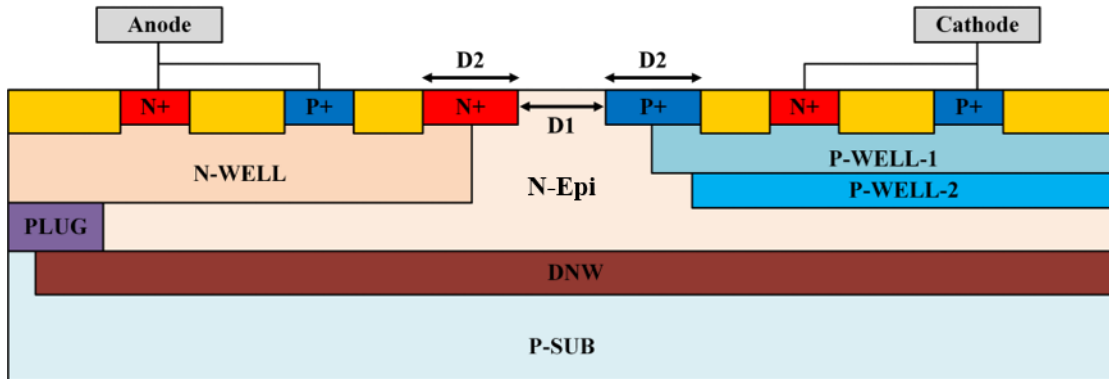


Figure 2-1 Cross section view of NSSCR.

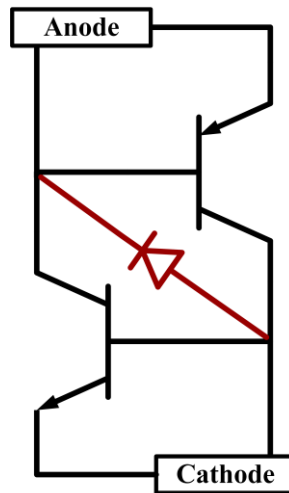


Figure 2-2 Equivalent circuit of NSSCR.

It could be observed from Figure 2-1 that the NSSCR is a variation based on the LSCR. The major innovation of this novel structure is to insert a parasite P-type/Intrinsic/N-type (PIN) diode between the anode and cathode of the LSCR. The inserted element could be used to adjust both triggering voltage  $V_{t1}$  and holding voltage  $V_h$ . The width between the inserted N+ and P+ extension is defined as D1, which is responsible adjusting the  $V_{t1}$ . The width of the inserted P+ and N+ extension, is defined as D2, which is a part of the base width of the parasite bipolar

transistor (PBT), and changing D2 could adjust  $V_h$  by influencing the breakdown junction electric field.

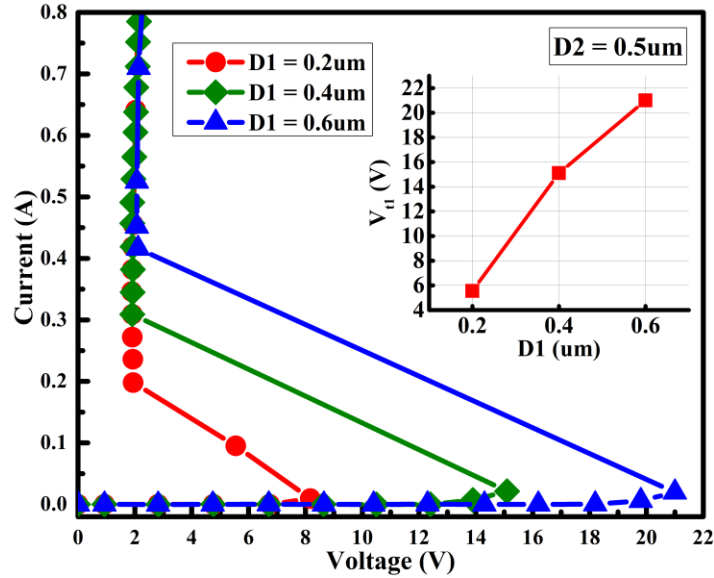


Figure 2-3 TLP measurement for the NSSCR's with D1 changing from 0.2 um to 0.6 um. Inserted graph shows the variation of  $V_{t1}$  by changing D1.

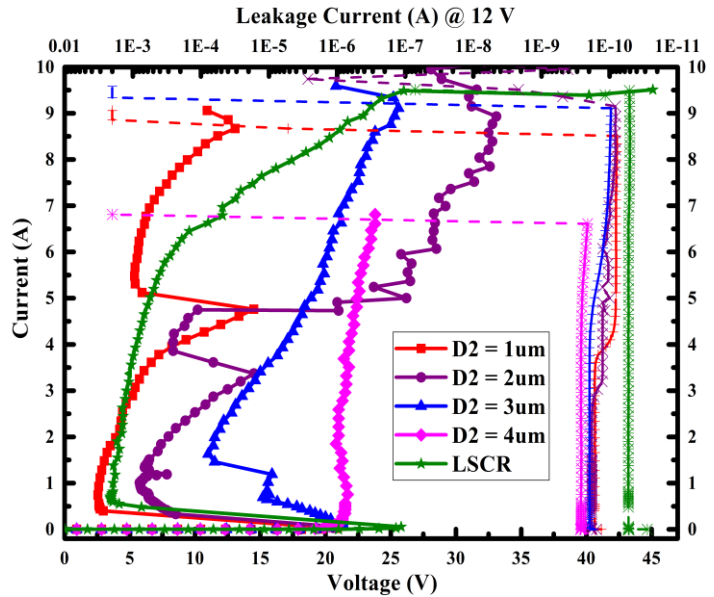


Figure 2-4 TLP measurement for the NSSCR's with D2 changing from 1 um to 4 um and D1 stays constant at 0.6 um.



Figure 2-3 shows the TLP measured I-V characteristics of NSSCR when D2 is fixed at 0.5  $\mu\text{m}$  and D1 varies from 0.2  $\mu\text{m}$  to 0.6  $\mu\text{m}$ . It could be observed from the inserted graph that when D2 is fixed,  $V_{\text{tl}}$  has a linear relationship with the changing D1. And it is also clear that the changing D1 has rare influence on holding voltage. Figure 2-4 shows the TLP measured I-V curves of NSSCR when D1 is fixed at 0.6  $\mu\text{m}$  and D2 changes from 1  $\mu\text{m}$  to 4  $\mu\text{m}$ . We also added a TLP I-V curve of a SCR fabricated from the same technology for comparison in the same figure. It is clear that the  $V_{\text{h}}$  goes up when D2 increases, and when D2 reaches 4  $\mu\text{m}$ , the  $V_{\text{h}}$  equals to 21 V which is the same as the  $V_{\text{tl}}$ , and we obtain the no-snapback I-V characteristics.

It is an interesting fact that the increasing D2 results in a higher  $V_{\text{h}}$ , and it is necessary for us to make the underlying physical mechanism of the variation on  $V_{\text{h}}$  clear. The TCAD simulation is carried out to explain the mechanism of the higher  $V_{\text{h}}$ .

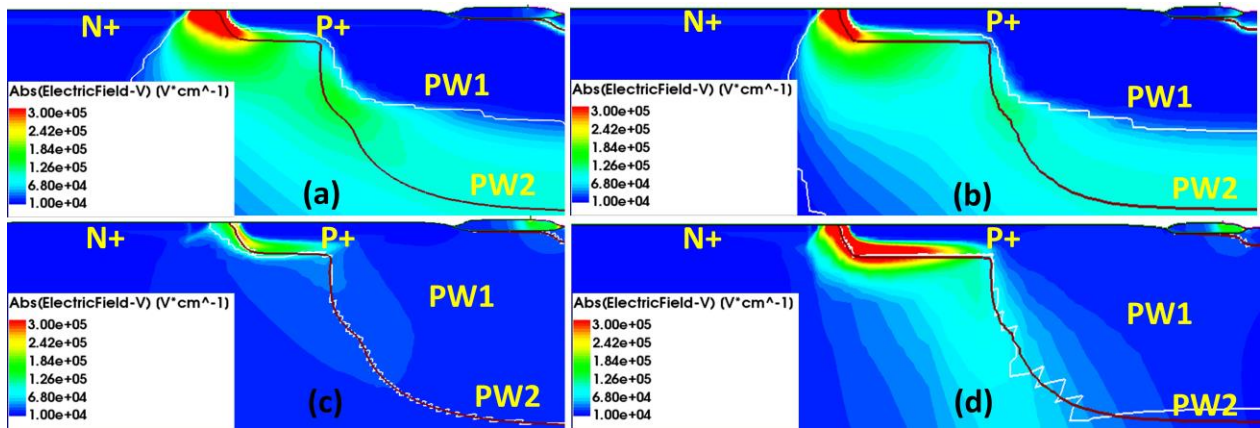


Figure 2-5 Captured pre-triggering ((a) and (b)) and post-triggering ((c) and (d)) electric field in TCA simulation of the NSSCR. D2 equals to 2  $\mu\text{m}$  in (a) and (c), and D2 equals to 4  $\mu\text{m}$  in (b) and (d).

Figure 2-5 [13] shows the TCAD simulation results of NSSCR. The electric field is captured in two cases, the pre-triggering and the post-triggering, from two devices with a D2 equals to 2  $\mu\text{m}$  and 4  $\mu\text{m}$ , respectively. TLP like pulse of 15 V and 250 V were employed to the

device model to simulate these two conditions, respectively. It could be observed from Figure 2-5 (a) and (b) that the electric field at the inserted P+ extension is similar in two devices with different D2 for the pre-triggering condition. However, the electric field with D2 equals to 4  $\mu\text{m}$  increases significantly in the post-triggering condition compared with the one with D2 equals to 2  $\mu\text{m}$ . And it is also clear that in the post-triggering condition, the electric field at the breakdown junction (N-Epi/PW1/PW2) of the device with larger D2 is much higher than the one with smaller D2. Because of the existence of the inserted P+ extension in PIN diode, the peak electric field is transferred to the P+/N-Epi junction rather than the N-Epi/PW1/PW2 junction. Therefore, the electric field at the N-Epi/PW1/PW2 junction which is also the major flowing path of ESD current never exceeds the critical electric field and this junction never get into the high-level conductivity modulation. Thus, with a larger D2, the electric field at the breakdown junction does not drop to a very low level after triggering and this mechanism results in a much higher  $V_h$  than the device with small D2.

Table 2-1 Layout parameter of Cell A and Cell B.

	D1 ( $\mu\text{m}$ )	D2 ( $\mu\text{m}$ )
Cell A	0.4	4
Cell B	0.6	4

Table 2-1 shows the layout parameters of two variation of NSSCR. Based on our experiment, the proposed structure is perfect to use as stacked devices to fit the device in various ESD protection voltage node. Figure 2-6 shows the TLP I-V characteristics for stacked Cell A and Cell B. It is clear that two stacked Cell B could be used for ESD protection up to 45 V.

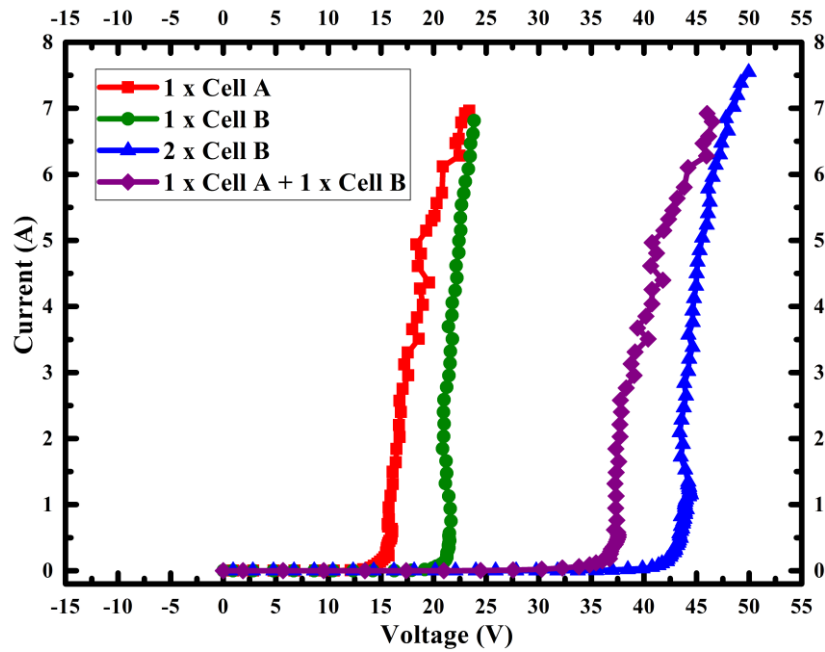


Figure 2-6 TLP I-V curves for stacked Cell A and Cell B.

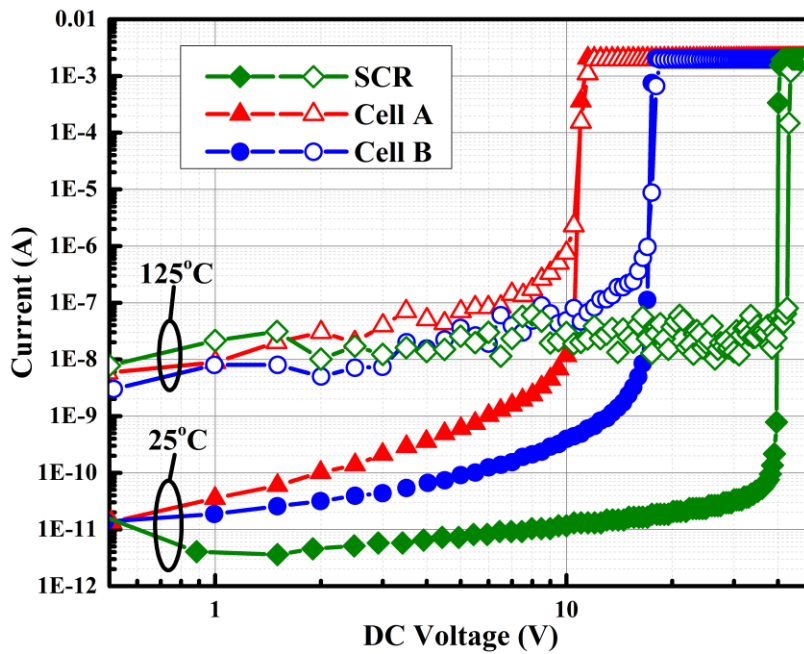


Figure 2-7 DC measurement of devices under temperature of 25 °C and 125 °C.

As the device is proposed for automotive applications, the performance under high temperature is also concerned. We evaluated the DC leakage current of Cell A, Cell B and a LSCR for comparison. Figure 2-7 shows that under room temperature, all three devices have an excellent leakage current level [13]. Under elevated temperature, the leakage current increase around 100 times higher for all the three devices, but still within an acceptable level.

### 2.3 DCSCR

SCR has been one of the most widely used ESD protection device [12]. With the development of the advanced silicon technology with a low operating voltage, the ESD protection design has been a challenge in such LV applications because of the narrow ESD design window allowed for ESD designers. In this section, we will introduce a novel SCR-based ESD protection device called DCSCR. It is proposed in a 0.18  $\mu\text{m}$  CMOS technology. The DCSCR has a perfect no-snapback I-V characteristics like diode, but exhibits a SCR-like robustness and ESD protection efficiency for LV ESD protection [15].

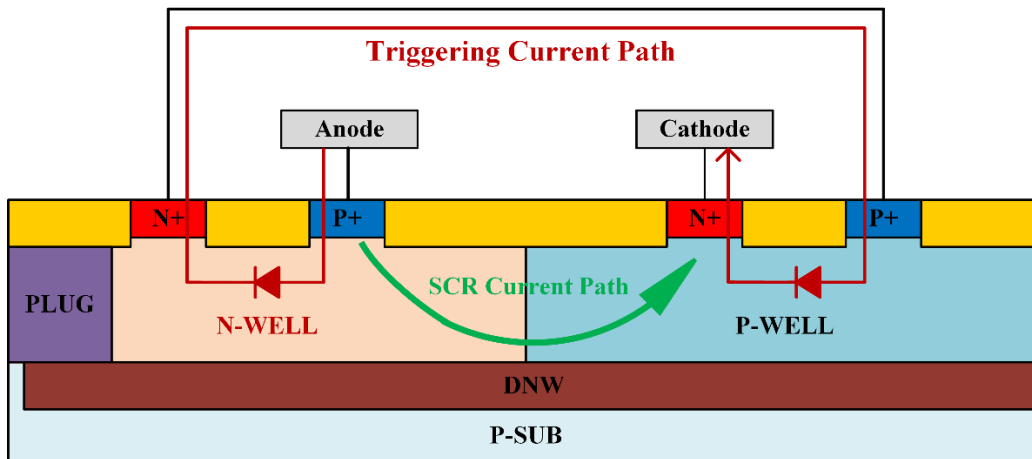


Figure 2-8 Cross section view of DCSCR.

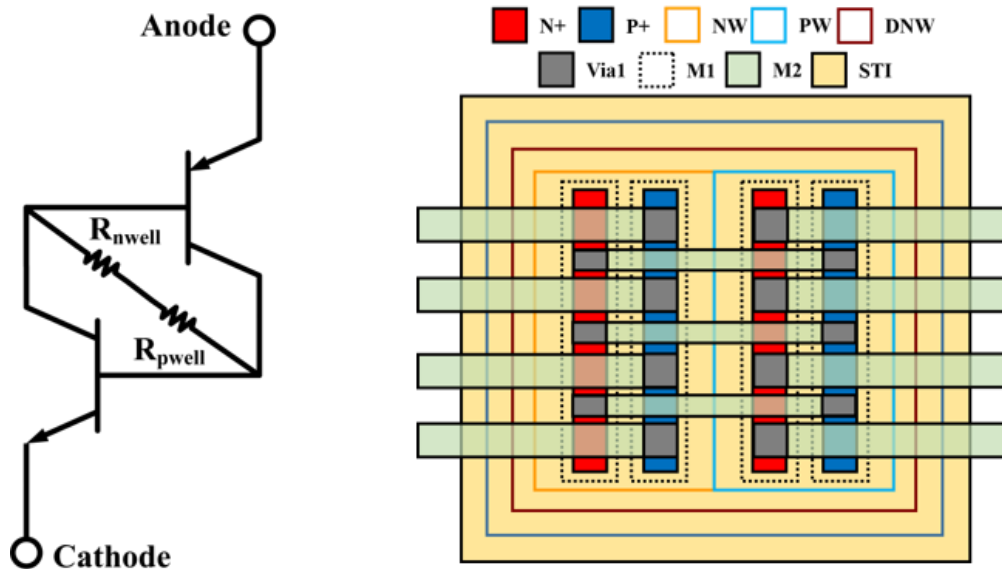


Figure 2-9 Equivalent circuit and layout geometry of DCSCR.

The cross section view of DCSCR is shown in Figure 2-8. Figure 2-9 gives the equivalent circuit and layout geometry of DCSCR [16]. It could be observed from the cross section view that the N+ in NW and P+ in PW are directly connected with a metal line. The P+ in NW and N+ in PW serve as the anode and cathode, respectively. In a ESD event, the ESD current arrives at the anode, and then go through the triggering path which is marked with red in Figure 2-8. When the anode voltage exceeds twice the diode's forward turn-on threshold, the P+ in NW and N+ in PW start to inject free carriers in to the NW/PW, then the SCR current path is finally turned on and the DCSCR is triggered without a snapback [15].

Figure 2-10 shows the measured TLP I-V curves of the DCSCR and a few other devices for comparison. It could be observed from Figure 2-10 that the DCSCR has a near zero snapback with a same  $V_{t1}$  and  $V_h$  which equals to 1.3 V. Comparing with diode, DCSCR has a much better ESD robustness, as well as a higher triggering voltage which allows fewer stacking number of

devices for applications at a higher voltage node. Comparing with the Diode Triggered SCR (DTSCR), DCSCR has a better snapback window for automotive ESD protection as well as a better area efficiency. Comparing with LSCR, DCSCR is far more suitable for the LV ESD protection. Table 2-2 summarizes the key ESD parameters of the devices we investigated and our discussion could also be verified through the measurement data [15, 16].

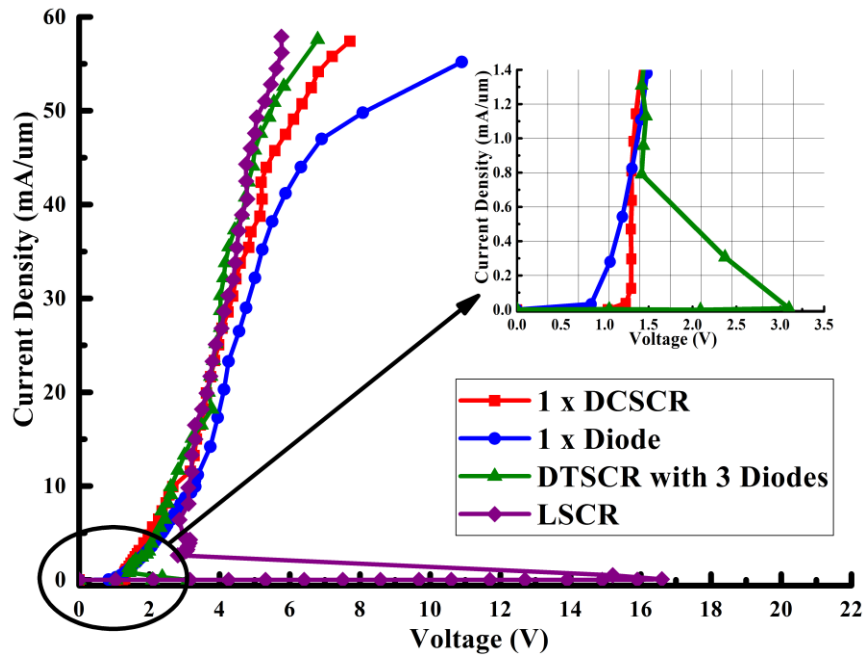


Figure 2-10 TLP IV characteristics of DCSCR, diode, DTSCR, and LSCR.

Like the NSSCR and diode, the DCSCR could also be stacked in series to adapt to a higher protection voltage node. Figure 2-11 shows the cross section of the stacked DCSCR and the metal connection between electrodes. The measured TLP I-V curves of the stacked DCSCRs are given in Figure 2-12. We can conclude from Figure 2-12 that the  $V_{t1}$  and  $V_h$  near linearly increase with the increasing stacking number. Our proposed structure is flexible to be used in LV and MV ESD protection.

We also evaluated the leakage current under the high temperature and the DC sweep is shown in Figure 2-13 [15]. We can observe from Figure 2-13 that the DCSCR has an acceptable leakage current at nA level before 1 V, however will increase to a level higher than 1 uA when temperature is elevated to 125 °C which is not acceptable for high temperature application. Thus, the DCSCR need to be considered specially for low leakage and high temperature applications.

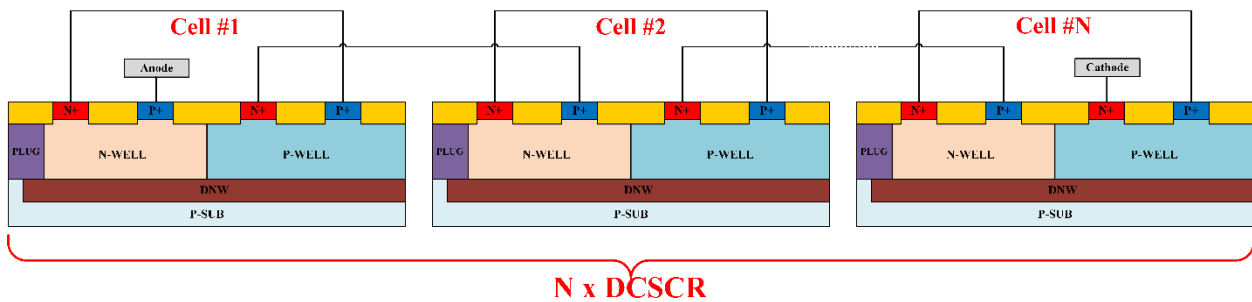


Figure 2-11 Cross section view of stacked DCSCR.

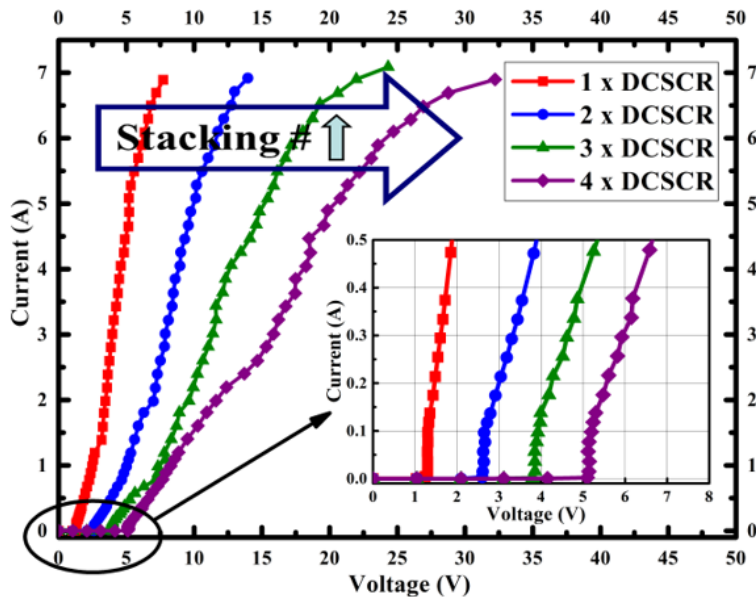


Figure 2-12 TLP I-V characteristics of stacked DCSCR.

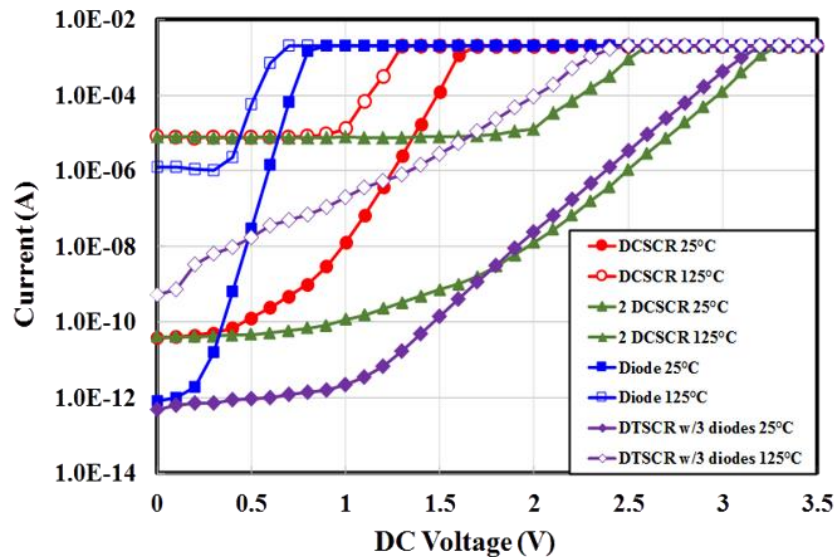


Figure 2-13 DC sweep of devices at temperature of 25 °C and 125 °C.

Table 2-2 Comparison of devices on key ESD parameters.

Device	TLP $I_{t2}$ (A)	Area ( $\mu\text{m}^2$ )	TLP $J_{t2}$ ( $\text{mA}/\mu\text{m}^2$ )	Capacitance (fF)	$V_{t1}$ (V)	$V_h$ (V)	Overshoot (V)
Diode	3.2	702	9.4	570	0.7	0.7	7.38
LSCR	7	702	9.97	464	16.6	2.8	20.5
DTSCR	6.9	1188	5.81	443	3.1	1.4	14.7
DCSCR	7	702	9.97	278	1.3	1.3	7.38

## 2.4 Conclusion

In this chapter, two novel SCR-based ESD protection devices without snapback are introduced in detail. NSSCR is proposed for HV automotive ESD protection, and the key innovation is the PIN diode inserted into the LSCR. It offers a good choice for HV capacitive pin protection. DCSCR is proposed for LV and MV automotive ESD protection which shows a reduced overshoot voltage and a fast triggering behavior. It offers a good option for LV/MV I/O ESD protection.



## **CHAPTER 3      DESIGN, CHARACTERIZATION AND SIMULATION OF ESD PROTECTION DEVICES UNDER ELEVATED TEMPERATURES**

### 3.1 Introduction

As we mentioned in previous chapters, the ESD has been one of the major reliability issue in industry. Proper ESD design could mitigate such concerns and ESD protection devices are frequently used in such ESD designs. As the technology advances, these devices become more susceptible to ESD-induced failures [17]. This is compounded by the fact that the assembly and/or operation of integrated circuits in some cases are taken place at elevated temperature, and the ESD protection designs become more complex due to the thermally-induced variations of ESD parameters [18]. Thus, it is necessary to systematically and comprehensively analyze the characteristics of ESD protection devices to ensure they are suitable for operations under elevated temperatures.

Lin et al. [18, 19] introduced the temperature-dependence steady-state and dynamic-state characteristics of some SCR-based ESD protection circuits. They primarily focused on the triggering and holding behavior of such circuits. Meneghesso et al. [20] and Koo et al. [21] reported the holding voltages of new SCRs under high temperatures and explained the underlying physical mechanisms using TCAD simulation results. Other studies [13, 15, 22-31] looked into the ESD testing results under elevated temperatures to verify the temperature stability of the proposed devices. However, those papers only discussed the triggering and/or holding manners of their proposed SCRs under high temperatures and did not provide the underlying physical mechanisms and simulation results.

In this chapter, the investigation of temperature-dependent characteristics of ESD protection devices including a diode and several SCRs will be introduced. The TLP I-V characteristics will be measured, and key parameters such as the breakdown voltage  $V_{BD}$ , trigger voltage/current  $V_{t1}/I_{t1}$ , holding voltage/current  $V_h/I_h$ , failure current  $I_{f2}$ , on-resistance  $R_{ON}$  and DC leakage current will be studied and discussed. TCAD simulation were carried out to offer physical insights into the high temperature operations and key ESD parameters including the failure current, on-resistance and DC leakage current, etc. under high temperatures are also very important and are characterized for the first time [32].

### 3.2 Experiment Setup Description

The devices are fabricated in a 0.35  $\mu\text{m}$  BCD technology. The measurements are targeted for the HBM and are conducted using the Barth 4002 TLP tester with a pulse width of 100 ns and a rise time of 10 ns. The Signatone S1060 heating module is used to generate the different ambient temperatures of 300K (25 °C), 400K (125 °C) and 500K (225 °C). The typical operating temperature requirement for electronics is up to 400K (125 °C). However, the temperature requirements may vary for different applications. Our ESD devices were aimed for automotive applications which have a temperature requirement higher than 400K. The temperature ranges of automotive electronics may extend up to 850 °C [33]. As such, the study of characteristics of ESD devices operating at temperatures higher than 400K will be desired for such products. We will first characterize several SCRs that are targeted for different ESD metric, and followed by the study of a diode which is used widely for ESD applications as well.

### 3.3 Experimental Result and Discussion

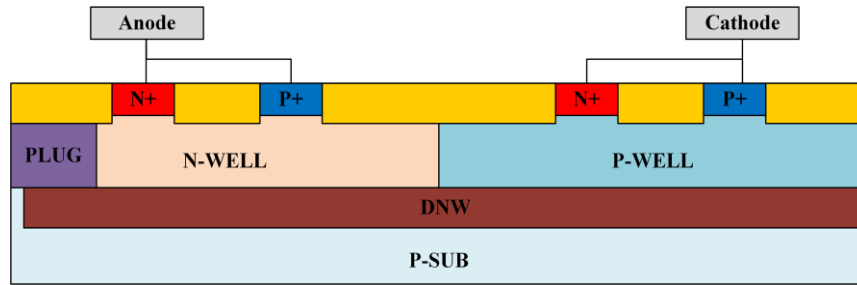
Figure 3-1(a) and (b) show the cross section view and TLP I-V curves, respectively, of the lateral SCR (LSCR), a widely used and highly robust ESD protection device, under the three different temperatures. The variations of  $V_{BD}$ ,  $V_{t1}$  and  $V_h$  with respect to temperature are shown in Figure 3-1(c). Figure 3-2(a) and (b) show the simulated cross-section view of LSCR and simulated quasi-static I-V curves. The electric field at the NW/PW junction under various ambient temperatures is shown in Figure 3-2(c).

The measurement results suggest that  $V_{BD}$  and  $V_{t1}$  increase with increasing temperature which agrees well with the simulated I-V characteristics given in Figure 3-2(b). This is because the triggering mechanism of LSCR is governed by the avalanche breakdown in the NW/PW junction and the thermal coefficient of the avalanche mechanism is positive vs. temperature. The electric field at NW/PW junction in Figure 3-2(c) is captured at the same device voltage ( $V_{Device}=20V$ ) before the device triggering. We could learn from Figure 3-2(c) that at the same device voltage before device triggering, the electric field at the breakdown junction decreases when temperature goes up, which suggests that the breakdown voltage, required to reach the critical electric field increases with elevated temperature. This mechanism applies to all the ESD protection devices whose device triggering are governed by the avalanche breakdown.

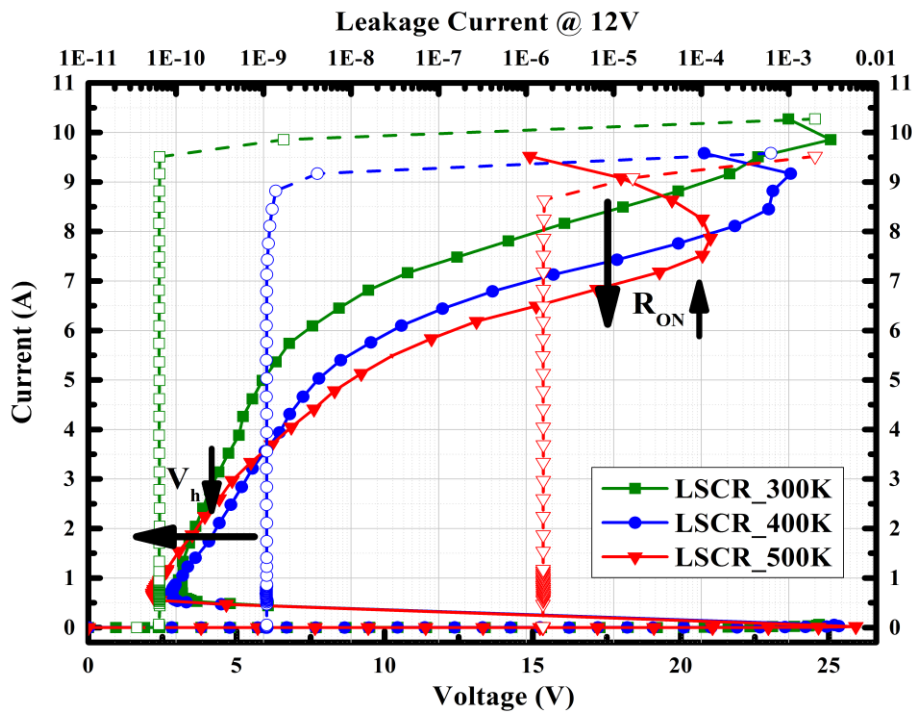
On the other hand,  $V_h$  decreases with increasing temperature which is also perfectly matched with the simulated I-V characteristics presented in Figure 3-2(b). This is because increasing the temperature increases the intrinsic carrier concentration, which in turn decreases the barrier of PN junction in silicon [34]. Thus, the higher temperature results in a lower  $V_h$ . This theory works with all the SCRs we discussed in this paper. However, the free-carrier mobility

decreases, which results in an increased resistivity, when the temperature goes up. Thus, the turn-on resistance  $R_{ON}$  increases with increasing temperature.

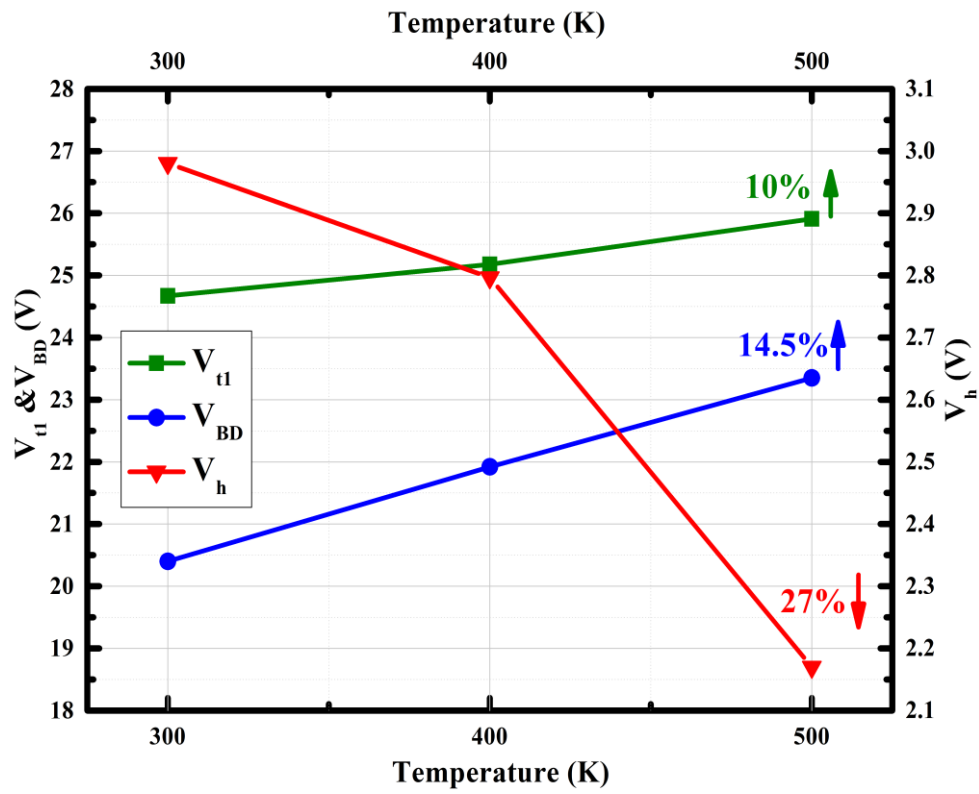
The DC leakage current is measured at 12 V, and it increases with increasing temperature because the leakage current is related to the intrinsic carrier concentration whose coefficient is positive vs. temperature. We could also conclude from the results in Figure 3-1 that  $I_{t2}$ ,  $I_{t1}$  and  $I_h$  all decrease with increasing temperature.



(a)

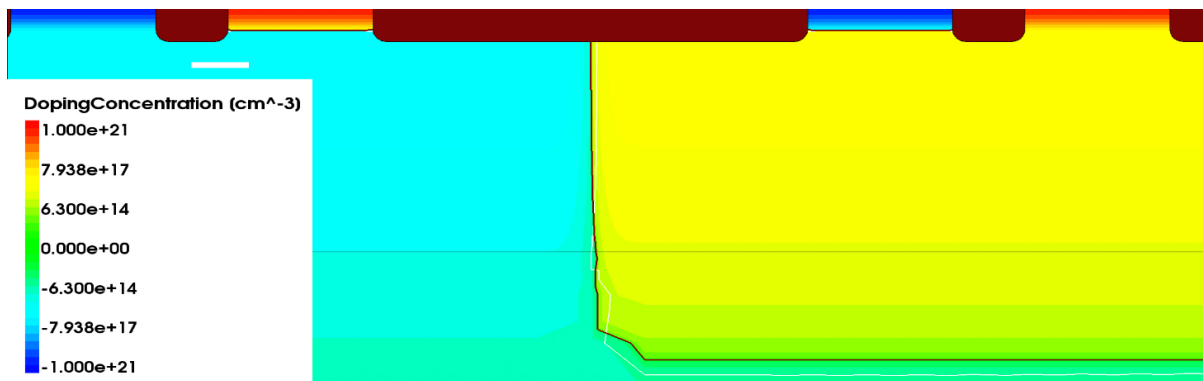


(b)

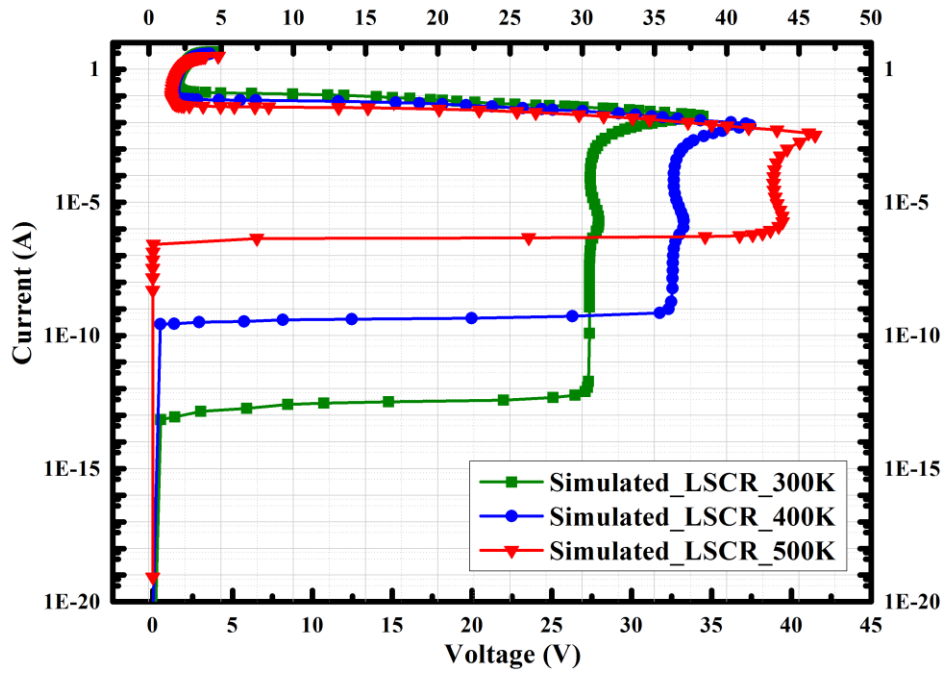


(c)

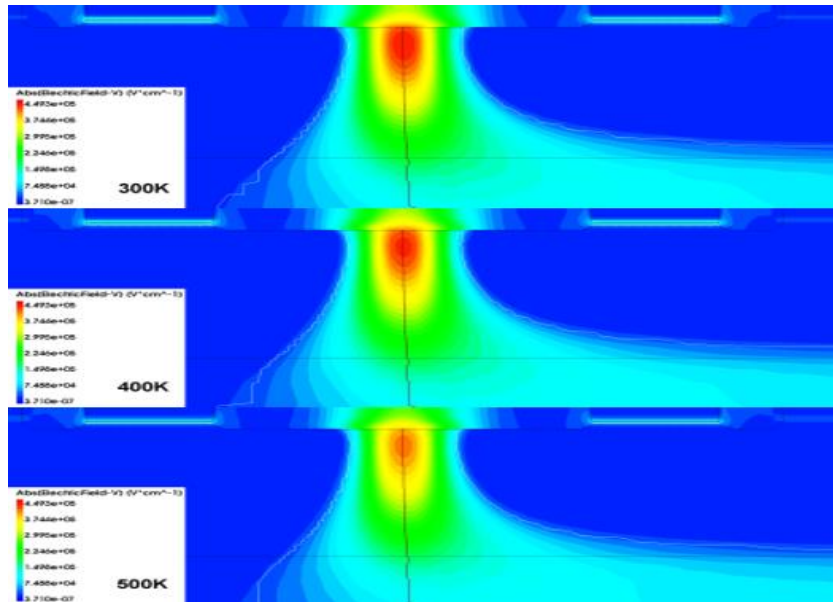
Figure 3-1 (a) Cross section view of LSCR, (b) TLP I-V characteristics of LSCR, and (c)  $V_{BD}$ ,  $V_t$  and  $V_h$  versus temperature.



(a)

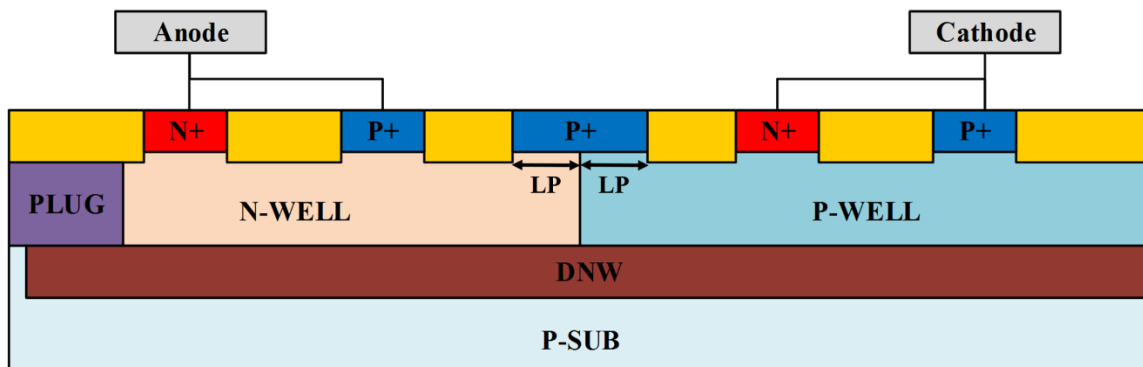


(b)

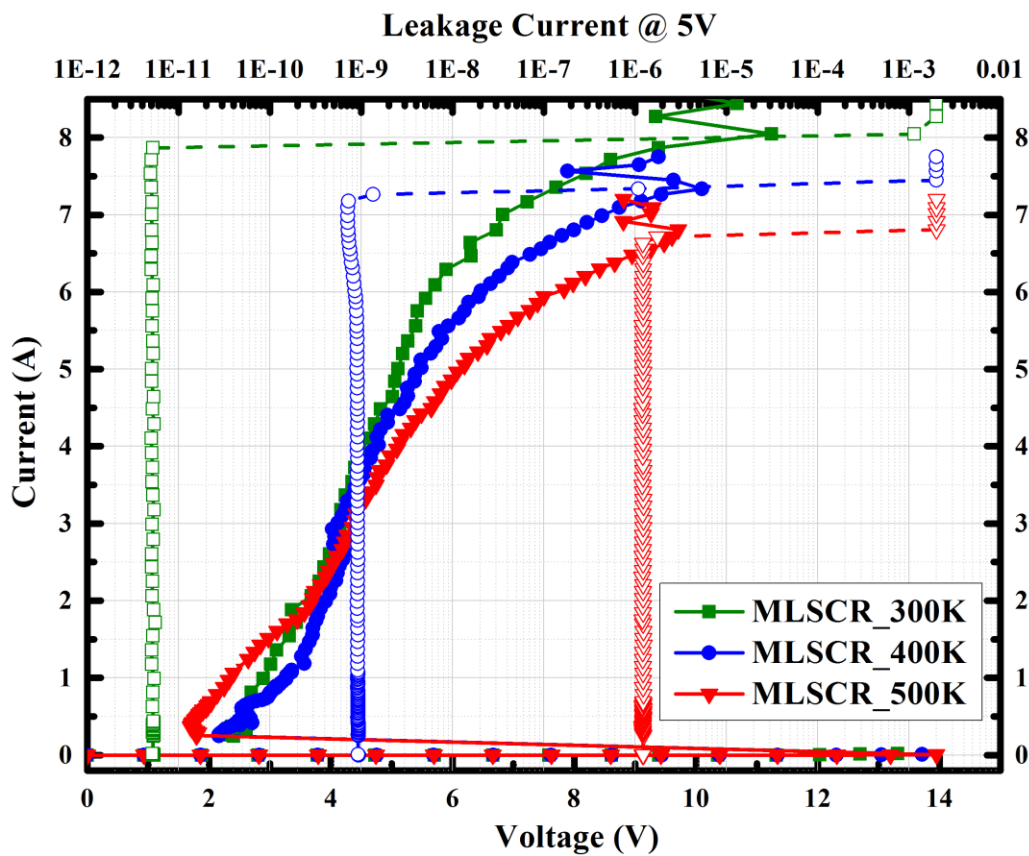


(c)

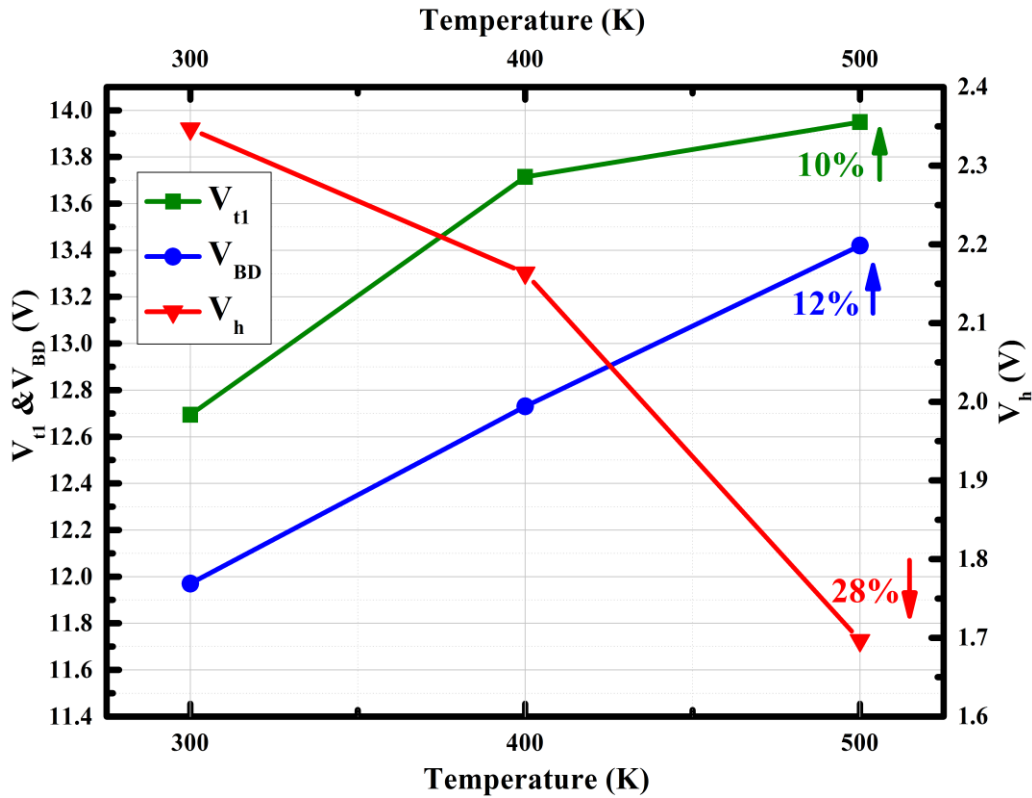
Figure 3-2 (a) Simulated cross section view of LSCR, (b) Simulated quasi-static I-V characteristics of LSCR with log scale y, (c) Captured electric field at NW/PW junction under various ambient temperatures.



(a)



(b)



(c)

Figure 3-3 (a) Cross section view of MLSCR, (b) TLP I-V characteristics of MLSCR, and (c)  $V_{BD}$ ,  $V_t$  and  $V_h$  versus temperature.

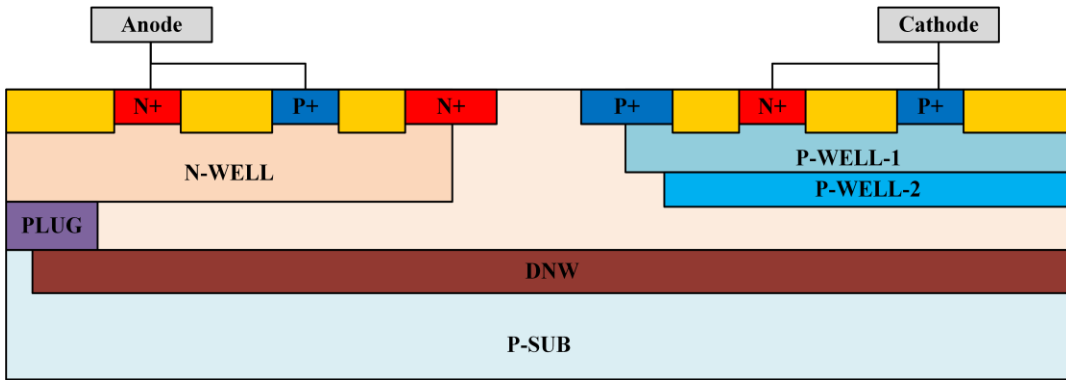
Figure 3-3(a) and (b) show the cross section view and TLP I-V curves, respectively, of the modified lateral SCR (MLSCR), a revised version of the LSCR. The temperature-dependent  $V_{BD}$ ,  $V_t$  and  $V_h$  results are given in Figure 3-3(c). Clearly,  $V_{BD}$  and  $V_{t1}$  go up with increasing temperature, like the case with LSCR, as the triggering mechanism of MLSCR is also governed by the avalanche breakdown in the NW/P+/PW junction and the temperature coefficient of the avalanche mechanism is positive. Like the LSCR, the MLSCR exhibits decreasing  $V_h$ ,  $I_{t2}$ ,  $I_{t1}$ , and  $I_h$ , but increasing  $R_{ON}$  and DC leakage current with temperature.



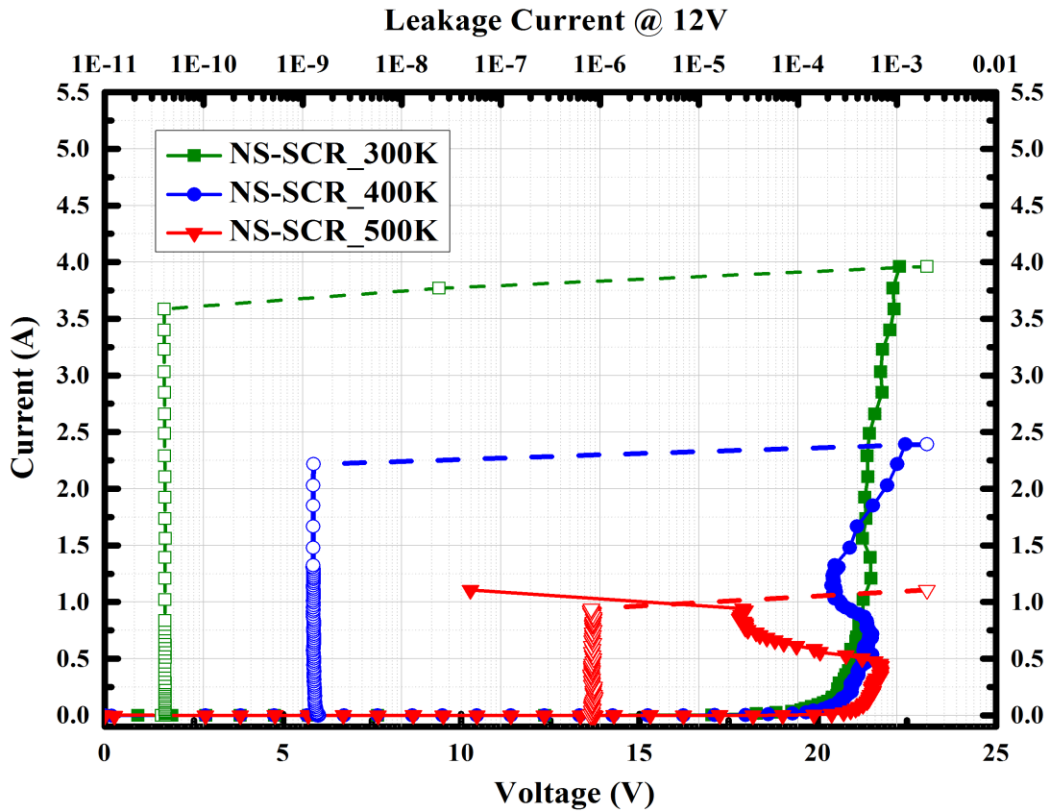
Figure 3-4(a) and (b) show the cross section view and TLP I-V curves, respectively, of a new SCR device structure, called NSSCR proposed by Wang. et al. [13] for automotive ESD applications. The variations of  $V_{BD}$ ,  $V_t$  and  $V_h$  with increasing temperature are shown in Figure 3-4(c). It can be seen from Figure 3-4(b) and (c) that  $V_{BD}$  and  $V_t$  increase with increasing temperature but  $V_h$  drops when the temperature goes up. Further, the NSSCR loses its no-snapback characteristics under an elevated temperature. The triggering mechanism of NSSCR is governed by the avalanche breakdown in the N-Epi/PW1/PW2 junction so  $V_{BD}$  and  $V_t$  vs. temperature characteristics change in a similar manner as those of the LSCR. The elevated temperature induces a higher electric field at the N-Epi/PW1/PW2 junction and enhances the conductivity modulation which impairs the ability to sustain a high holding voltage. Therefore,  $V_h$  decreases with temperature. It could be observed from Figure 3-4(b) that  $I_{t2}$  decreases and DC leakage current increases with increasing temperature.

Figure 3-5(a) and (b) show the cross section view and TLP I-V curves, respectively, of the low voltage triggering SCR (LVTSCR) which is aimed for low-voltage ESD applications. The variations of  $V_{BD}$ ,  $V_{t1}$  and  $V_h$  with increasing temperature are shown in Figure 3-5(c). The simulated cross-section view of LVTSCR and simulated quasi-static I-V curves are shown in Figure 3-6(a) and (b). These results indicate that in the LVTSCR,  $V_{t1}$  decreases with increasing temperature. Different from the LSCR, the triggering mechanism of LVTSCR is governed by the embedded NMOS. After the breakdown, the channel resistance of NMOS decreases with increasing temperature which leads to a lower trigger voltage [34]. The variations of channel resistance due to temperature could also be observed from the region between breakdown and device triggering in Figure 3-6(b). Like other SCRs,  $V_h$  and  $I_h$  decrease when the temperature

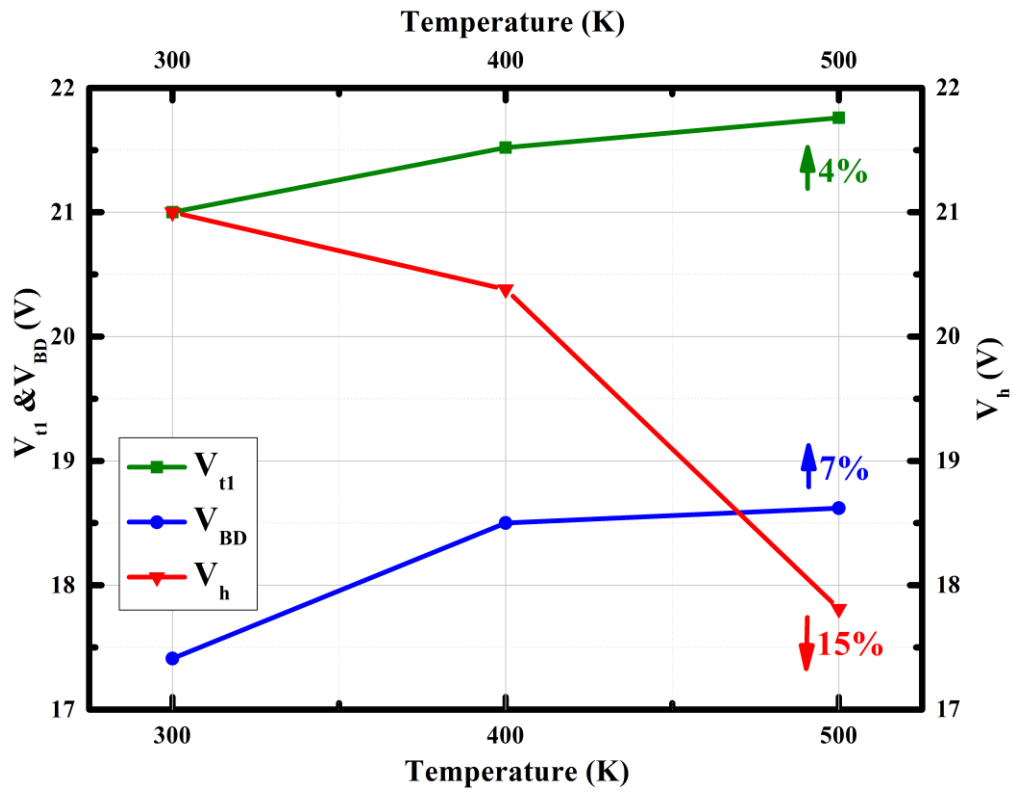
goes up which means the latch-up-immune capability of LVTSCR is degraded as the temperature increases [27].  $I_{I1}$  and  $I_{I2}$  decrease but  $R_{ON}$  and DC leakage current increase when the temperature is elevated.



(a)

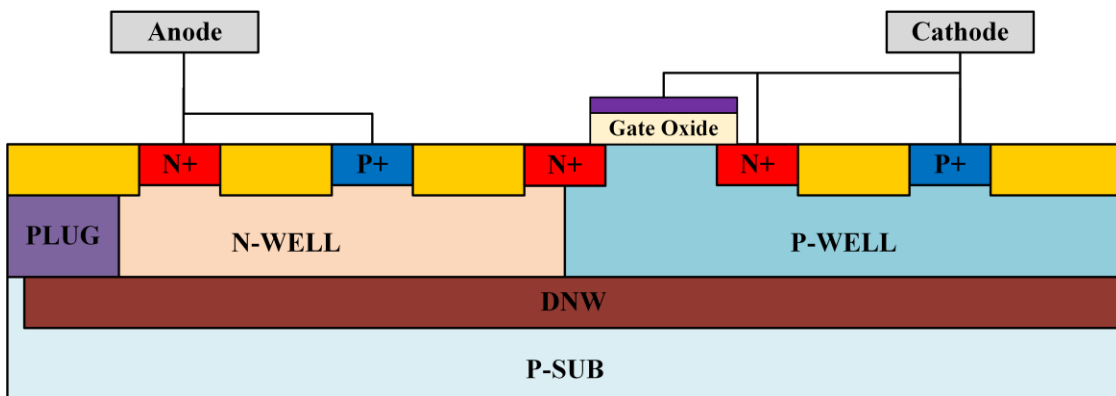


(b)

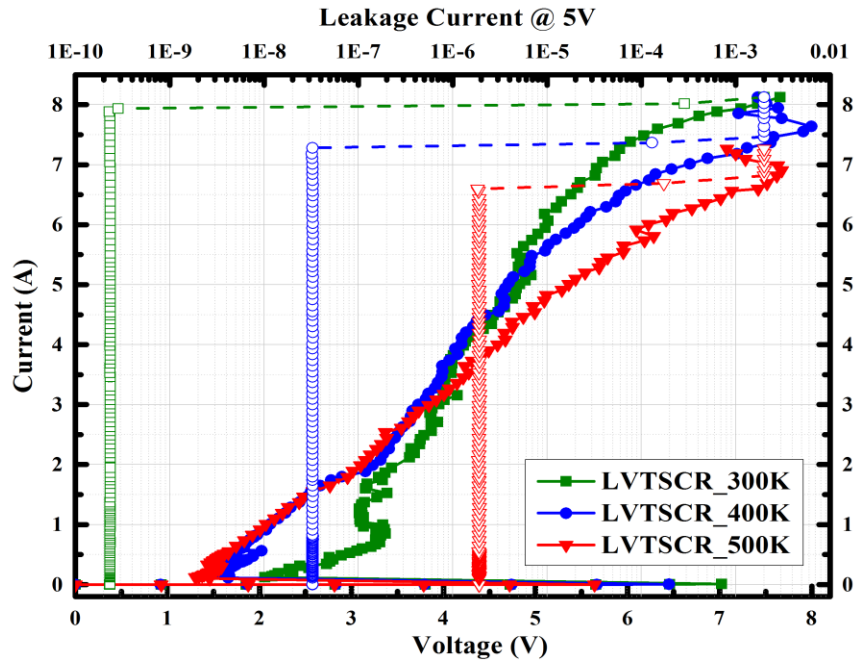


(c)

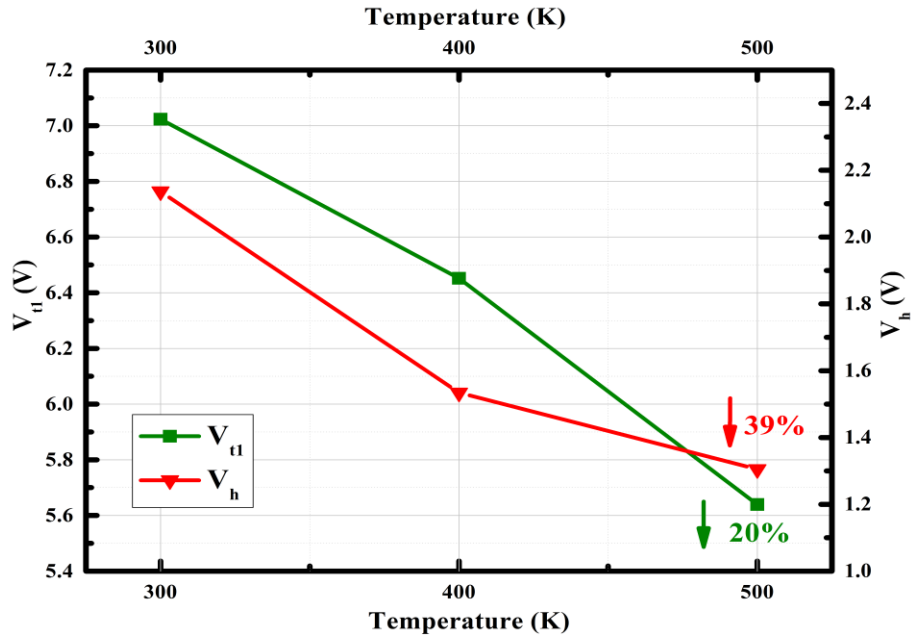
Figure 3-4 (a) Cross section view of NSSCR, (b) TLP I-V characteristics of NSSCR, and (c)  $V_{BD}$ ,  $V_t$  and  $V_h$  versus temperature.



(a)

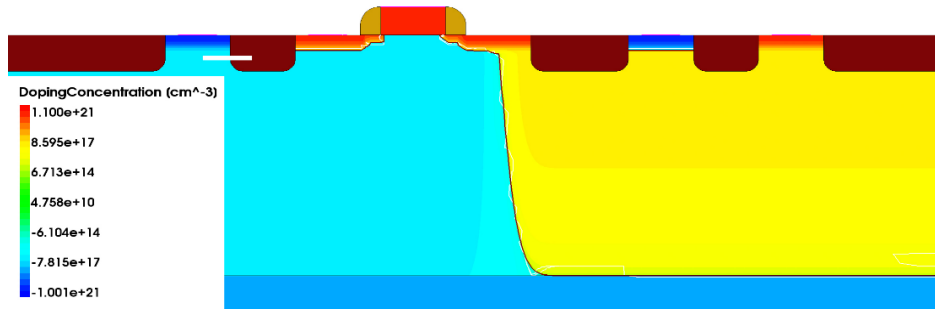


(b)

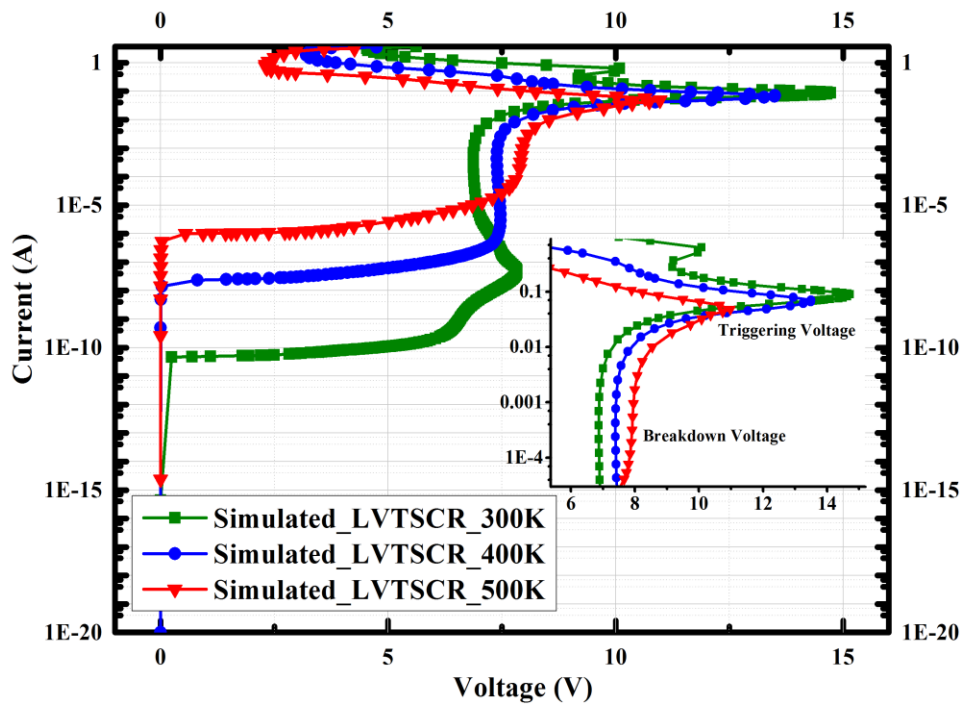


(c)

Figure 3-5 (a) Cross section view of LVTSCR, (b) TLP I-V characteristics of LVTSCR, and (c)  $V_t$  and  $V_h$  versus temperature.



(a)

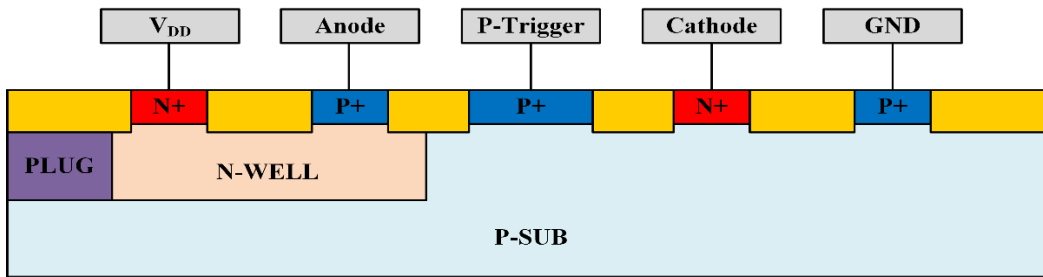


(b)

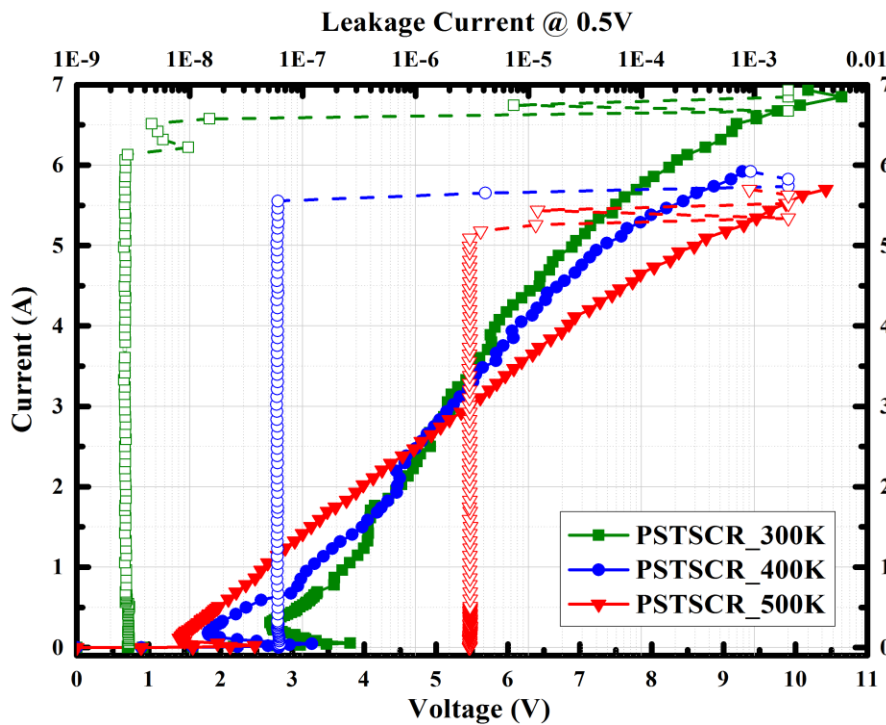
Figure 3-6 (a) Simulated cross section view of LVTSCR, (b) Simulated quasi-static I-V characteristics of LVTSCR with log scale y.

Figure 3-7(a) and (b) show the cross section view and TLP I-V curves, respectively, of a conventional SCR called the p-substrate triggered SCR (PSTSCR). The substrate triggering node is labeled in Figure 3-7(a) and the substrate triggering current used was 5 mA. The temperature-dependent  $V_{BD}$ ,  $V_{T1}$  and  $V_h$  results are given in Figure 3-7(c). It is shown that in PSTSCR,  $V_{BD}$

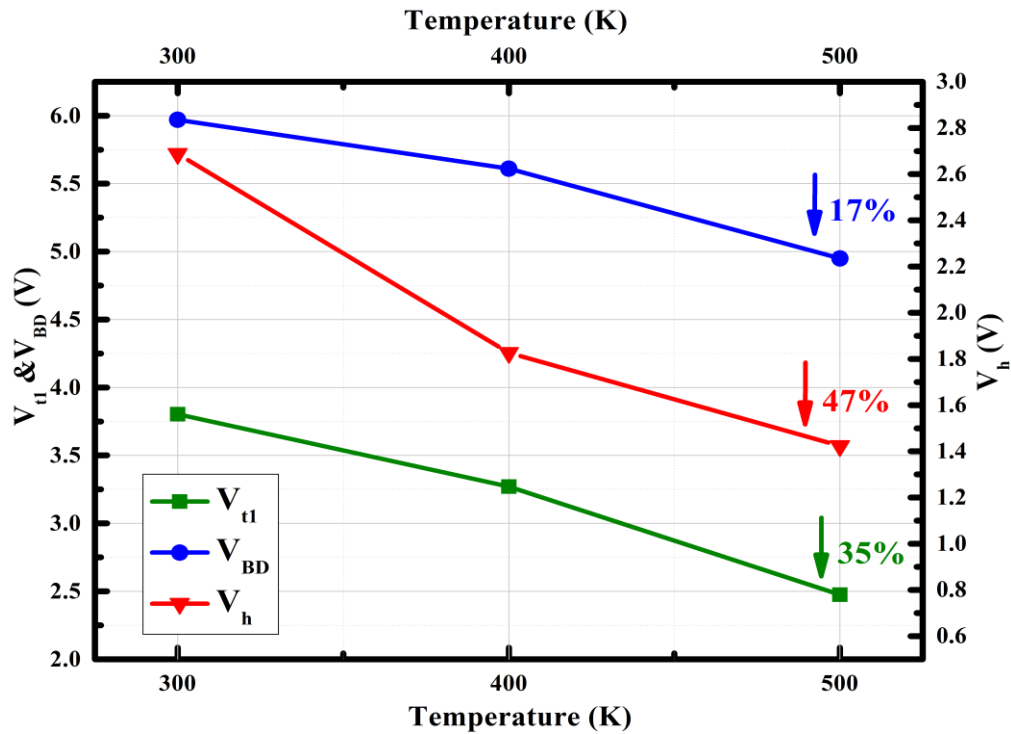
and  $V_{t1}$  decrease with increasing temperature. The increasing temperature elevates the intrinsic carrier concentration, and the threshold needed to reach the conductivity modulation state is decreased. Thus, the PSTSCR is triggered at a lower voltage when the temperature goes up.  $V_h$  declines when the temperature is elevated because the current gain of the parasite BJT in PSTSCR is increased with increasing temperature [35]. Like the LSCR, the PSTSCR exhibits decreasing  $I_2$ ,  $I_{t1}$ , and  $I_h$ , but increasing  $R_{ON}$  and DC leakage current with increasing temperature.



(a)



(b)



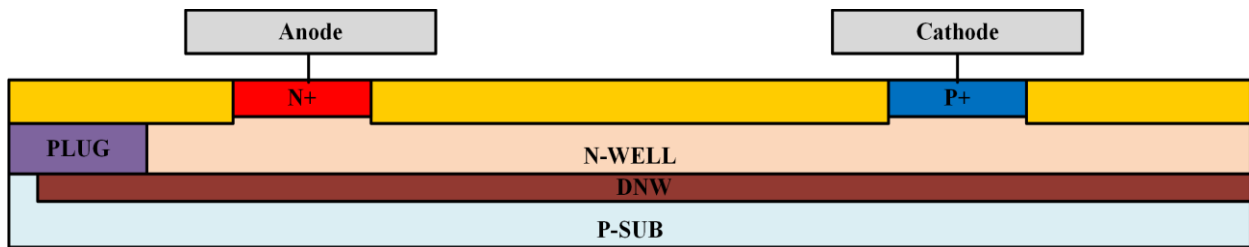
(c)

Figure 3-7 (a) Cross section view of PSTSCR, (b) TLP I-V characteristics of PSTSCR, and (c)  $V_{BD}$ ,  $V_t$  and  $V_h$  versus temperature.

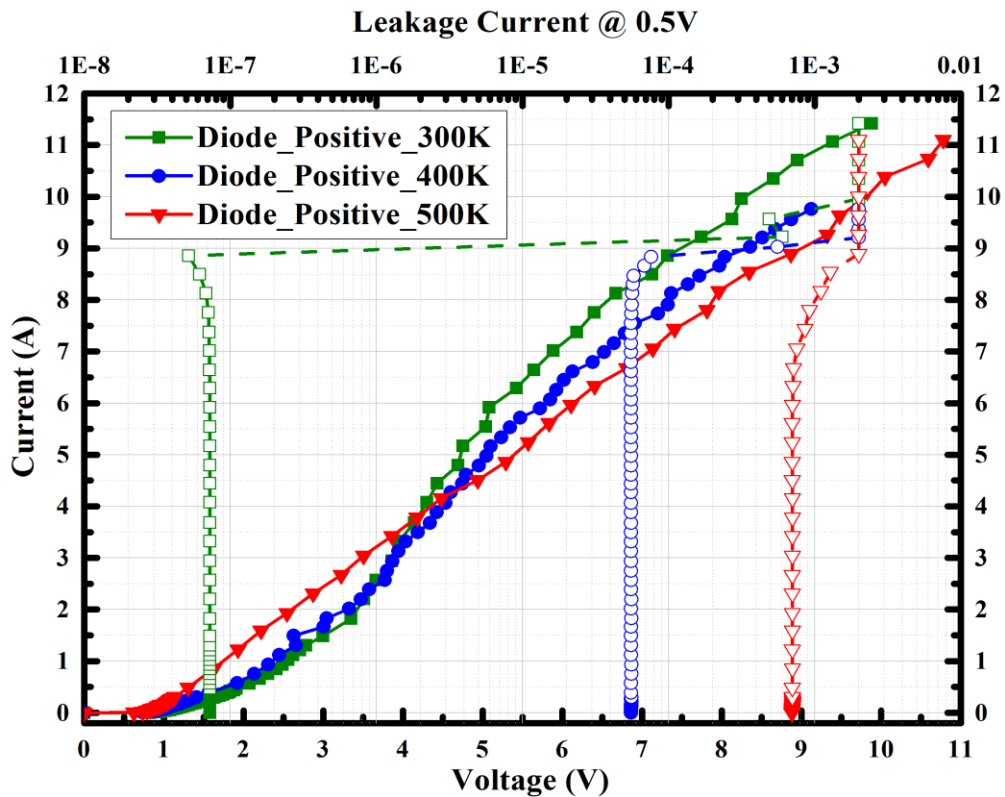
Diodes are popular ESD devices, particularly for protecting circuits that are operating at relatively low voltages. Figure 3-8(a) shows the structure of a P+/NW diode. The TLP I-V curves of the diode operating under the forward and reverse biases are illustrated in Figure 3-8(b) and (c), respectively. It can be seen from Figure 3-8(b) that the turn-on voltage decreases slightly with increasing temperature in the forward bias condition, while the leakage current is increased due to the Darlington effect [4].  $R_{ON}$  increases and  $I_{t2}$  decreases slightly with increasing temperature. For the reverse bias condition, shown in Figure 3-8(c), the turn-on voltage increases with increasing temperature due to the positive temperature-dependent avalanche coefficient.  $I_{t2}$  and  $V_{t2}$  degrade with increasing temperature because a higher temperature makes the device

more susceptible to ESD-induced failure. Both  $R_{ON}$  and DC leakage current increase with increasing temperature.

Table 3-1 summarizes the trends of temperature-dependent key ESD parameters of the devices considered and discussed above. Symbols + and – stand for increase and decrease, respectively, of the parameter values with increasing temperature.

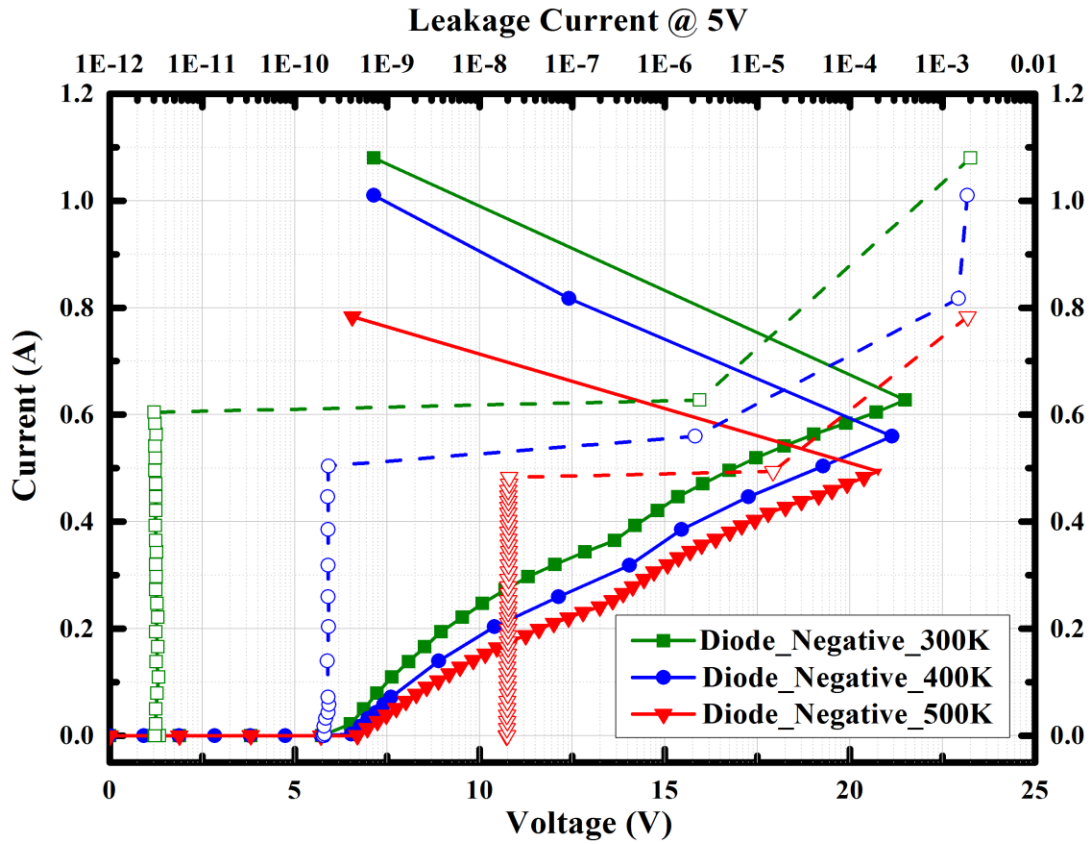


(a)



(b)





(c)

Figure 3-8 (a) Structure of P+/NW diode, (b) TLP I-V characteristics of forward-biased diode, and (c) TLP I-V characteristics of reversed-biased diode.

Table 3-1 Summary of ESD Parameters Variations with Increasing Temperature.

Device	$V_{t1}$	$I_{t1}$	$V_h$	$I_h$	$V_{BD}$	$I_{t2}$	Leakage	$R_{ON}$
LSCR	+	-	-	-	+	-	+	+
MLSCR	+	-	-	-	+	-	+	+
NSSCR	+	-	-	-	+	-	+	N/A
LVTSCR	-	-	-	-	N/A	-	+	+
PSTSCR	-	-	-	-	-	-	+	+
Diode	F:-/R:+	N/A	N/A	N/A	N/A	-	+	+

### 3.4 Conclusion

We have investigated the key parameters of various ESD protection devices operating under the Human Body Model (HBM) and different elevated temperatures. Because of the specific triggering mechanisms, some of these devices exhibited different trends on the trigger voltage vs. temperature characteristics. All other key ESD parameters, including the holding voltage, failure current, on-state resistance and leakage current, showed various degrees of degradation under elevated temperatures. This study offers a useful insight and information on obtaining the safe margin needed for the successful design and optimization of ESD protection solutions that are required to meet high-temperature qualifications.

## **CHAPTER 4 CHARACTERIZATION AND ANALYSIS OF ESD PROTECTION DEVICES UNDER TOTAL IONIZING DOSE IRRADIATION**

### 4.1 Introduction

Radiation hardness in semiconductor devices is important for space applications. A multitude of trapped particles in the Earth's radiation belt, solar and cosmic rays can cause numerous effects which can interfere with the operation of space electronics. There are two most important categories among these effects, the total ionizing dose (TID) and single event (SEE) effects. The TID represents cumulative damage which produces gradual changes in the characteristics of semiconductor devices, whereas the SEE can cause abrupt behavior changes in semiconductor devices [36, 37].

This study will focus solely on the TID effect on the key parameters of ESD protection devices. TID is the energy deposited per unit mass of material because of ionization [38]. When energetic charged particles strike a semiconductor device, electron-hole pairs are generated. A few electrons and holes that are generated will initially recombine but the rest of the electrons are swept out of the oxide, and radiation-induced trap centers are formed resulting from the ionization [36]. Such trapped charges can cause degradation to key parameters of a semiconductor device, such as the threshold voltage, radiation-induced leakage current, and degenerated power consumption [38]. The performance of irradiated devices decreases with increasing TID, and a sufficiently large TID can lead to permanent failure.

Space is an environment that can generate abundant electrostatic charges, and these charges often adhere to space equipment and electronic systems, such as the solar panels,

communication apparatuses, and power management units. In the event these charges are unevenly distributed on the space electronics systems, the ESD can take place between the highly and lowly charged areas due to the large potential difference created. When this occurs, the flow of these charges generates a huge current and causes catastrophe damages to the systems [39]. Another possible ESD event is a charged astronaut touching an electronic system during the human exploration mission [40]. As such, implementation of robust ESD protection solutions is of paramount importance to the well-being of electronics used in space applications. Linten et al. [41] investigated the SEE effects on the DC characteristics of an MLSCR and proposed an alternative ESD clamp with higher radiation hardness. Other studies [42-45] have briefly discussed ESD concerns in space electronics.

The TID effects on the performance of various widely used ESD protection devices are studied and discussed for the first time in this work. These devices include diodes, GGNMOS, and SCR. TID irradiation will be performed on the ESD devices, and the pre- and post-irradiated I-V curves were measured using the TLP tester, which generates HBM like pulses. While there can be other ESD events in space, such as the CDM and human metal model (HMM), the HBM has been the industry benchmark for assessing the ESD protection capability. In addition, it is possible to correlate the HBM and other ESD events based on the key parameters obtained from the TLP testing [46]. As such, the characterization of ESD devices subject to the TLP stress can offer useful insight into space ESD applications. TID effects on key ESD parameters such as the trigger voltage  $V_{t1}$ , holding voltage  $V_h$ , failure current  $I_{f2}$ , on-state resistance  $R_{ON}$  and DC leakage current were addressed and analyzed.

## 4.2 Experiment Setup Description

The devices were fabricated in a 0.35  $\mu\text{m}$  BCD technology. The 1.5 MeV He<sup>+</sup> from a RPEA 4.0 MV Dynamitron accelerator was used for the irradiation process. Three experimental groups of device samples were irradiated with different total ionizing doses called Irradiation Dose 1, Dose 2 and Dose 3. A control group without irradiation was used for comparison called Pre-Irradiation. Table 4-1 summarizes the setup of irradiations and the magnitudes of total dose selected based on the major divisions within the natural space environment [36, 47, 48]. The ESD measurements were conducted using the Barth 4002 TLP tester with a pulse width of 100 ns and a rise time of 10 ns.

Table 4-1 Summary of Irradiation Setup.

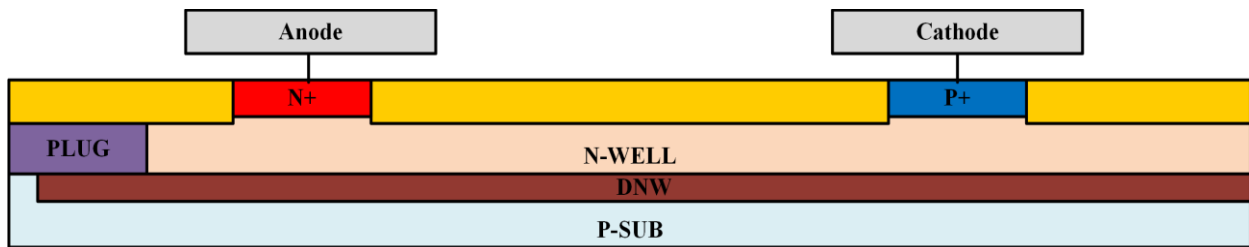
Device Groups	Irradiation Source Ion	Ion Energy (MeV)	Total Dose (e/cm <sup>2</sup> )	Post Process Time
Dose 1	He <sup>+</sup>	1.5	1014	300 °C for 3 hrs.
Dose 2	He <sup>+</sup>	1.5	2×1014	300 °C for 3 hrs.
Dose 3	He <sup>+</sup>	1.5	1015	300 °C for 3 hrs.
No Dose	N/A	N/A	N/A	300 °C for 3 hrs.

## 4.3 Experimental Result and Discussion

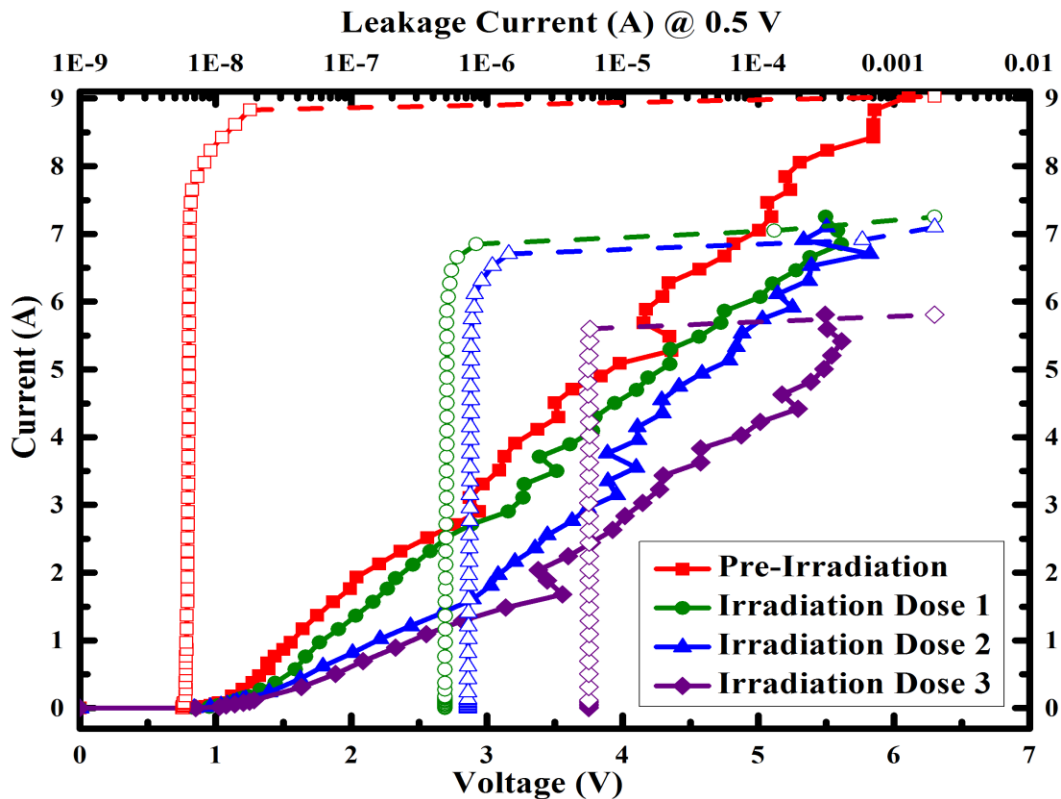
Diodes are popular ESD protection devices, especially for low voltage ESD applications. Figure 4-1(a) shows the cross-sectional view of a P<sup>+</sup>/NW diode. The TLP I-V characteristics of the diode operating in forward and reverse bias are given in Figure 4-1(b) and (c).

The measurement results in Figure 4-1(b) show that the trigger voltage of the diode increases slightly when the irradiation dose goes up. It could be observed that the DC leakage current increases remarkably with increasing total dose. This results from a parasite leakage current path between the anode and cathode formed by radiation-induced positive charge

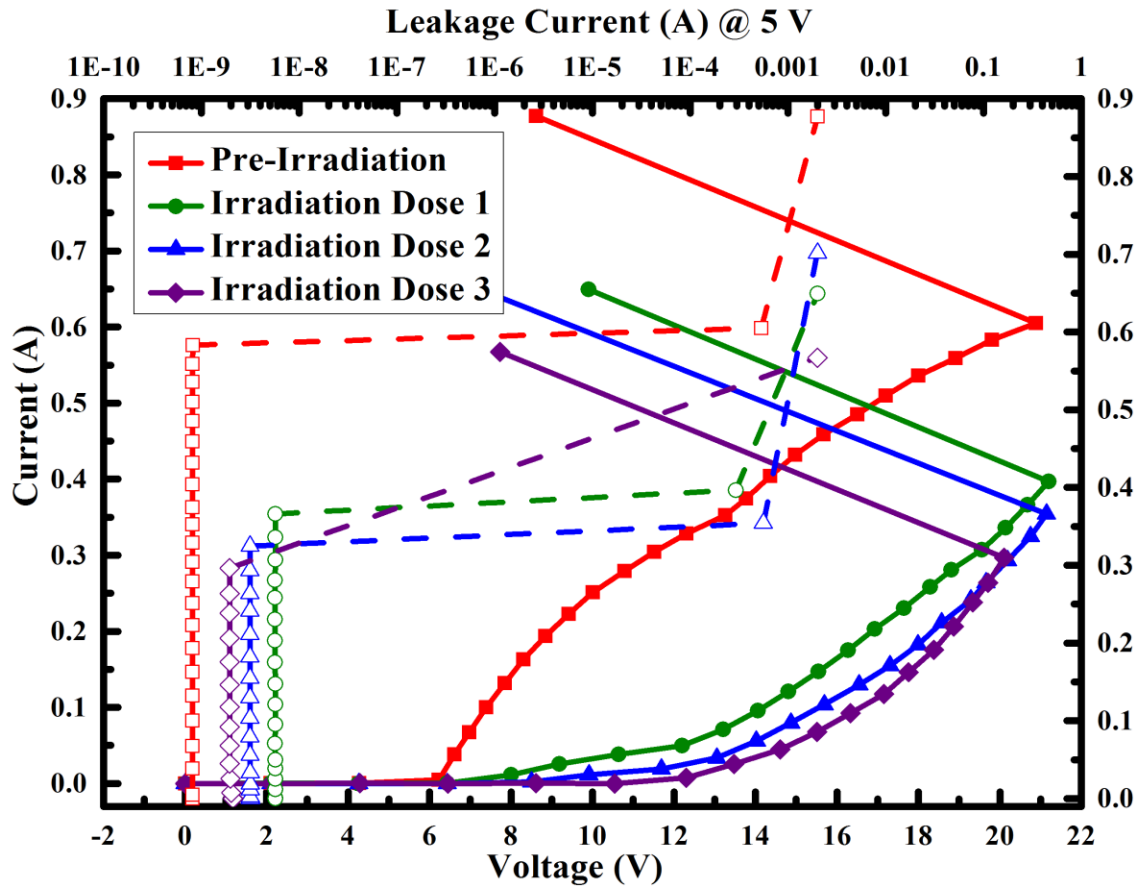
trapping in the field oxide and N-Well [41]. The on-state resistance  $R_{ON}$  increases, but the failure current  $I_{L2}$  decreases notably with a higher irradiation dose. Figure 4-1(c) shows that, in the reverse bias condition, the trigger voltage and  $R_{ON}$  increase significantly but  $I_{L2}$  decreases with increasing total dose. The DC leakage current goes up initially after irradiation, but it decreases slightly when the total dose further increases.



(a)



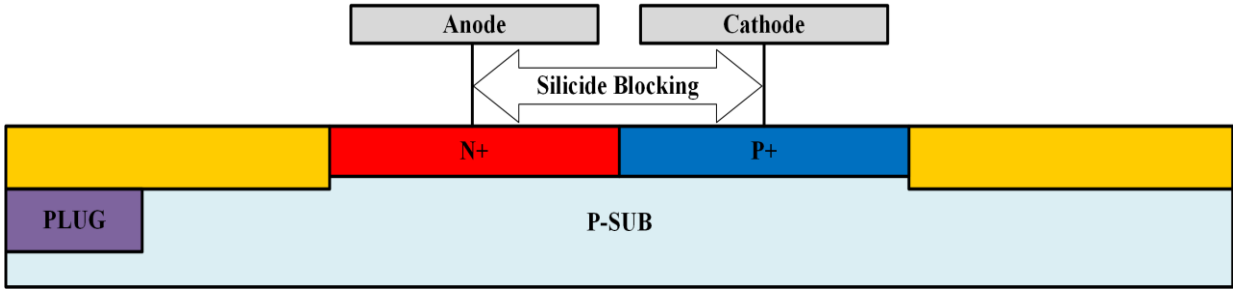
(b)



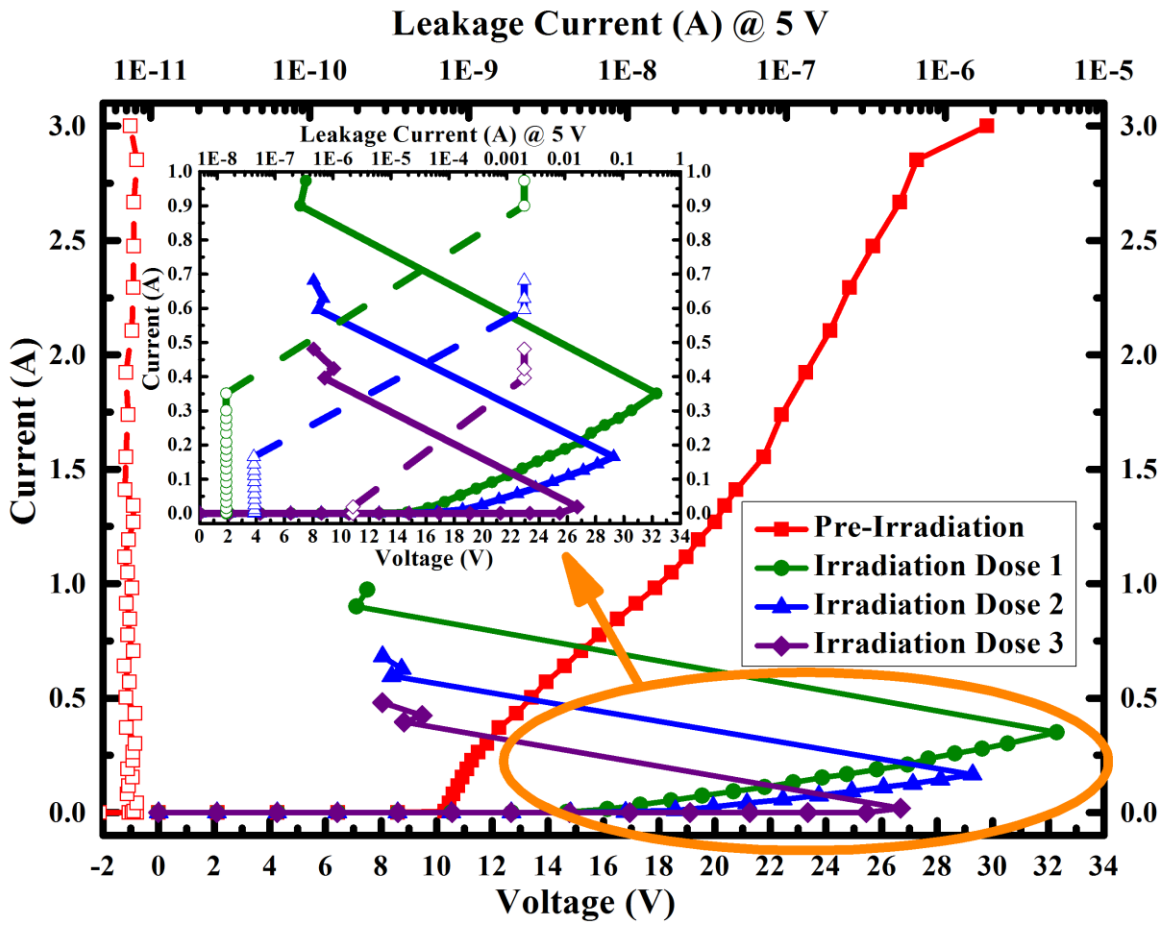
(c)

Figure 4-1 (a) Cross-section view of P+/NW diode, (b) TLP I-V characteristics of forward-biased diode (solid line for measurement and dashed line for DC leakage current), and (c) TLP I-V characteristics of reverse-biased diode (solid line for measurement and dashed line for DC leakage current).

Figure 4-2(a) and (b) show the cross-sectional view and TLP I-V curves, respectively, of a Zener diode which is typically used in ESD protection of high voltage circuits. Figure 4-2(b) suggests that the trigger voltage and  $R_{ON}$  increase significantly with increasing irradiation dose. The DC leakage current increases and a remarkable decrease in  $I_{t2}$  could be observed when the total dose is increased.



(a)



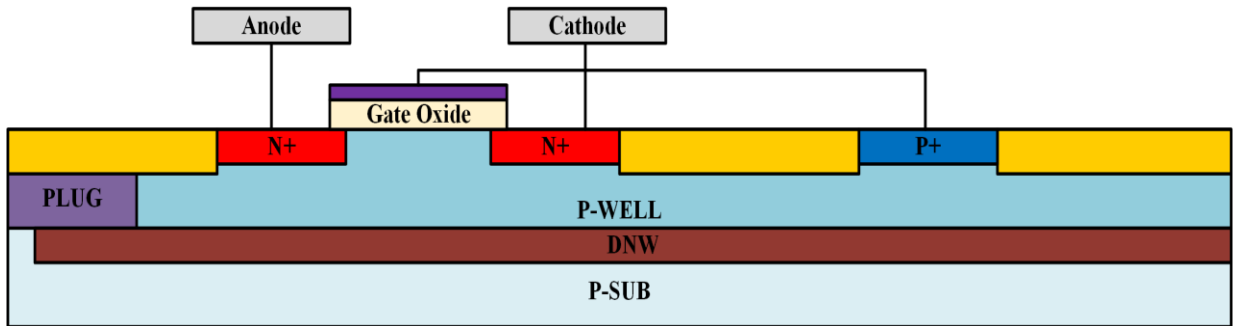
(b)

Figure 4-2 (a) Cross-section view of Zener diode, and (b) TLP I-V characteristics of Zener diode (solid line for measurement and dashed line for DC leakage current).

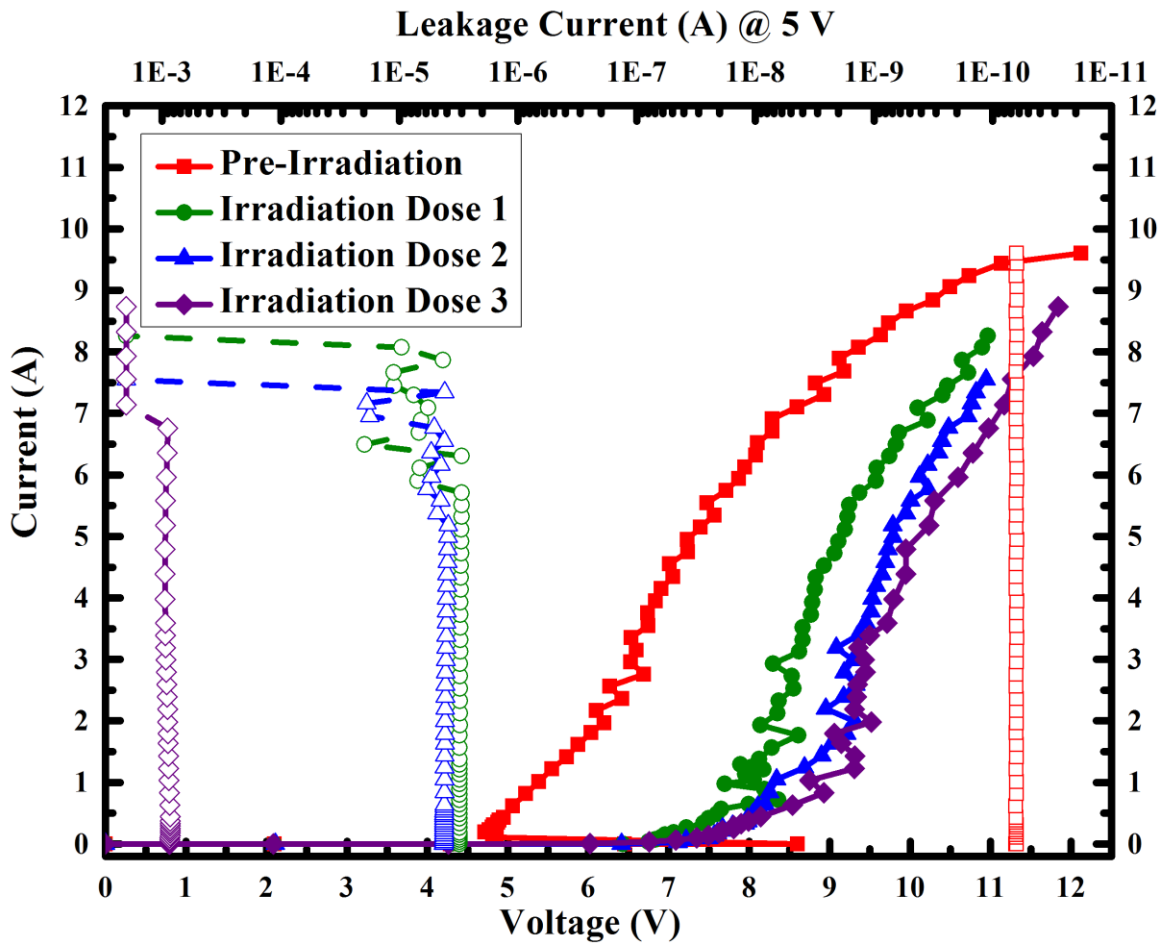


Figure 4-3(a) and (b) show the cross-sectional view and TLP I-V curves, respectively, of the GGNMOS which is widely used in ESD clamps. The measurement results indicate, interestingly, that the snapback behavior vanishes after irradiation and the GGNMOS shows a diode-like I-V characteristics once irradiated. The trigger voltage after irradiation is smaller than that of the pre-irradiation case and increases slightly with increasing total dose. The DC leakage current also increases but  $I_{t2}$  drops when the total dose is increased.  $R_{ON}$  is nearly constant under different irradiation levels. Irradiation induces trapped charges in gate oxide, and the charge trapping-induced threshold shift is the major degradation on GGNMOS. This effect only affects the triggering behavior of the device.

Figure 4-4(a) and (b) show the cross-sectional view and TLP I-V curves, respectively, of the lateral SCR (LSCR), a widely used and highly robust ESD protection device. The trigger voltage  $V_{t1}$  increases significantly with increasing total dose. However, none of the irradiated LSCRs survives before the snapback point, and a significant decrease in  $I_{t2}$  can be observed in Figure 4-4(b). The DC leakage current increases remarkably after a low dose of irradiation but stays almost the same with further increasing total dose.

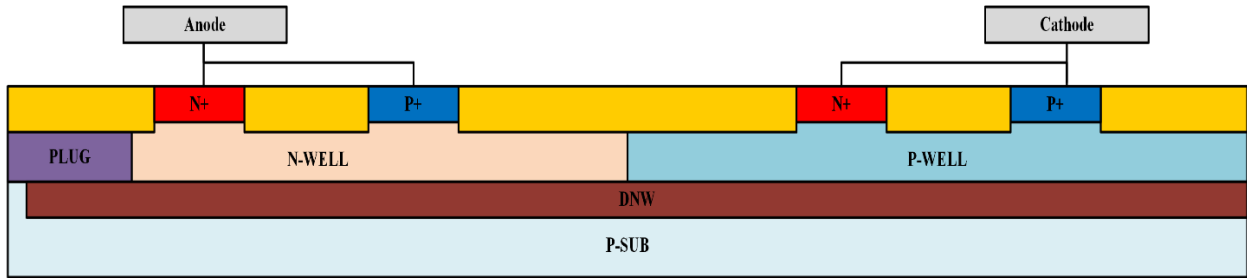


(a)

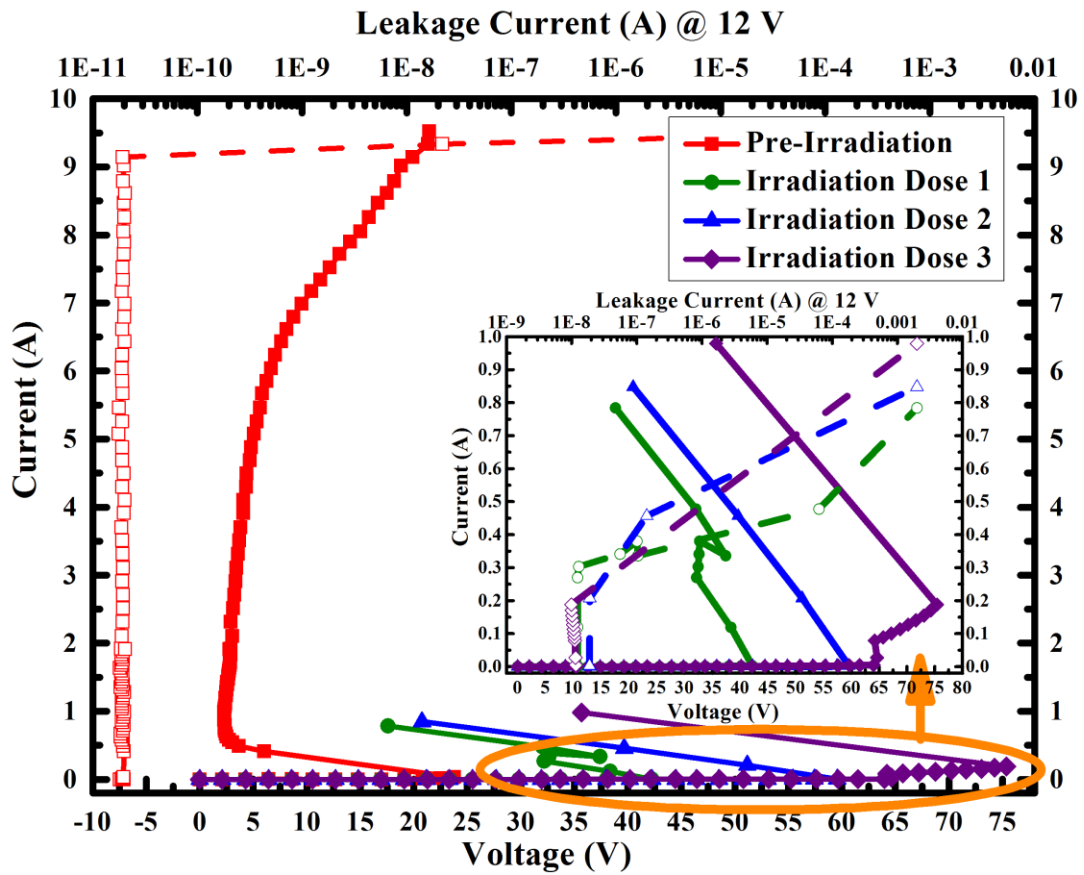


(b)

Figure 4-3 (a) Cross-section view of GGNMOS, and (b) TLP I-V characteristics of GGNMOS (solid line for measurement and dashed line for DC leakage current).



(a)



(b)

Figure 4-4 (a) Cross-section view of LSCR, and (b) TLP I-V characteristics of LSCR (solid line for measurement and dashed line for DC leakage current).

Table 4-2 Summary of TID Effects on Key ESD Parameters.

Device	$V_{t1}$	Leakage	$I_{t2}$	$R_{ON}$
Diode (Fwd.)	-	---	-	-
Diode (Rev.)	--	---	--	--
Zener Diode	--	---	---	---
GGNMOS	---	---	-	+++
LSCR	---	---	---	N/A

Table 4-2 summarizes the TID effects on key ESD parameters of the devices considered. Symbols + and – stand for radiation hardness and degradation, respectively. For example, more minuses mean the parameter is more degraded after irradiation. Generally speaking, the ESD robustness of forward-biased diode and GGNMOS are less susceptible to irradiation effect and thus are more suited for space ESD applications.

#### 4.4 Conclusion

This work investigated the TID effects on key parameters of various ESD devices aimed for protecting space. The diode keeps its basic I-V characteristics after irradiation but shows notable degradation with higher irradiation doses. The Zener diode, GGNMOS and SCR lose their typical functionality after irradiation and are quite sensitive to the irradiation level. This paper offers useful insights into how ESD protection devices operate under the space environment and what devices would be more suitable for constructing robust ESD protection solutions for space electronics.

## CHAPTER 5 DESIGN AND SIMULATION OF NOVEL VOLTAGE TRIGGERED ESD DETECTION CIRCUIT

### 5.1 Introduction

Electrostatic discharge (ESD) has become a major reliability concern in integrated circuits (ICs) industry [49, 50]. The internal circuit of ICs can be easily damaged without proper ESD protection. System-on-a-chip (SoC) has become popular because of the large number of devices on a single chip. However, some issues arise due to the different power domains contained in the same SoC, including gate-oxide reliability and the undesired leakage current paths, etc. [51]. The concept of ESD\_BUS for on-chip mixed-voltage I/O ESD protection is proposed to avoid leakage current paths formed by the traditional diodes [51]. Concerning about the cost, it is beneficial to use low-voltage devices to sustain a high-voltage stress. [49, 51-60] proposed a few detection circuits using low-voltage device for high voltage applications which are free from gate-oxide reliability concerns. As known, RC triggered ESD clamps may suffer from false triggering under fast power-up events which could damage the internal circuit. On the contrary, the voltage triggered ESD clamp circuit is immune to the fast power-up events [61, 62].

In this chapter, a voltage triggered  $2 \times V_{DD}$ -tolerant ESD detection circuit is proposed in a 0.18  $\mu\text{m}$  low-voltage CMOS process. SPICE simulation is carried out and comparing with the conventional voltage triggered detection circuit, improvement on triggering efficiency could be observed from the proposed detection circuit.

## 5.2 Conventional Detection Circuit Operation

Figure 5-1 shows a conventional voltage triggered  $2 \times V_{DD}$ -tolerant ESD detection circuit with a STSCR as well as the diode string serving as the clamping device.  $R_{SUB}$  stands for the equivalent resistance of the substrate. Eight diodes D1 to D8 in series and resistor R0 serve as the voltage detector which will respond to the ESD event. Mp1 and Mp2, which are P-type MOSFET (PMOS) with a large dimension (W/L: 200  $\mu\text{m}$ /0.18  $\mu\text{m}$ ), serve as the triggering part.

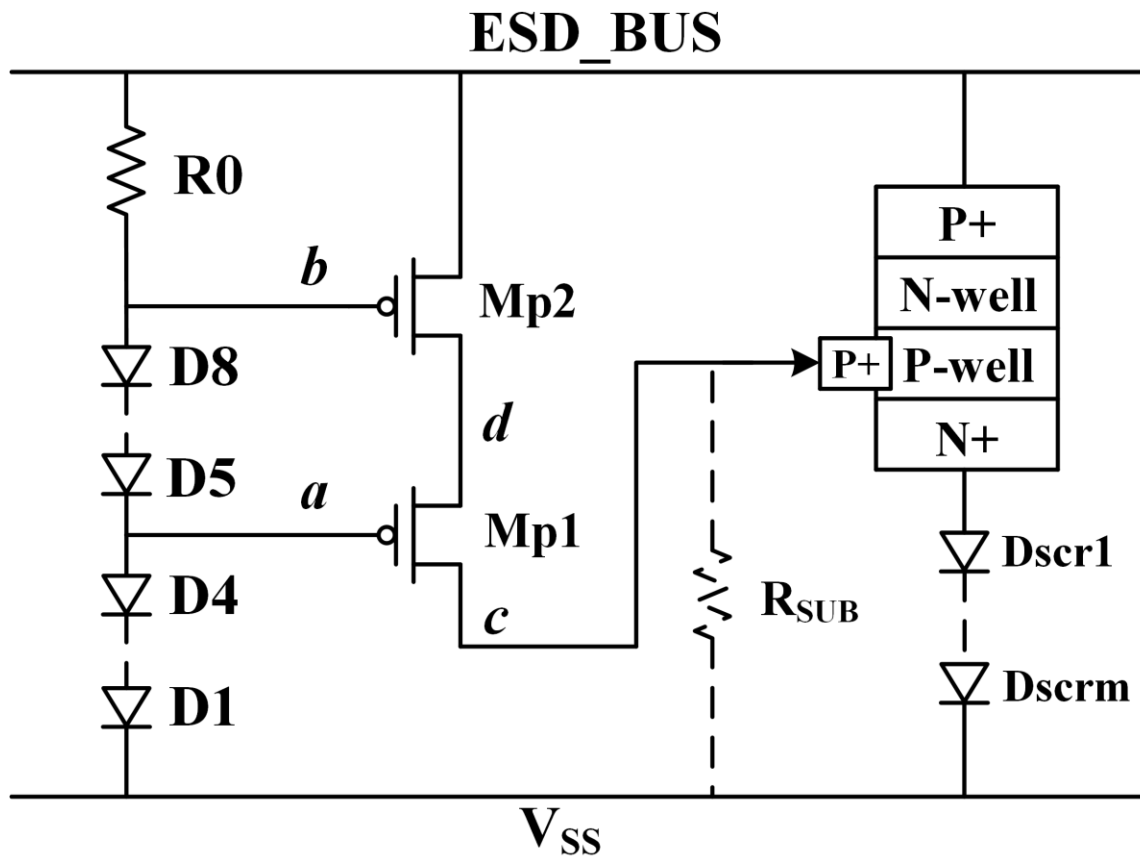


Figure 5-1 Schematic of the conventional voltage triggered  $2 \times V_{DD}$ -tolerant ESD detection circuit and the clamping device.

When the circuit in Figure 5-1 operates under normal condition, the  $2 \times V_{DD}$  of 3.3 V does not exceed the turn on voltage of the voltage detector which is around 5.6 V, so no current

flows through the voltage detector.  $V_b$  equals to 3.3 V which is pulled up by  $R_0$ . Both of Mp1 and Mp2 keeps off, and the clamping device will not be triggered.

In an ESD event, when the ESD voltage exceeds the turn on voltage of the voltage detector, it turns on and the current flowing through the detector results in a voltage drop across  $R_0$ , then both of Mp2 and Mp1 are turned on in order. A triggering current is injected into the clamping device through node c and the SCR is finally turned on.

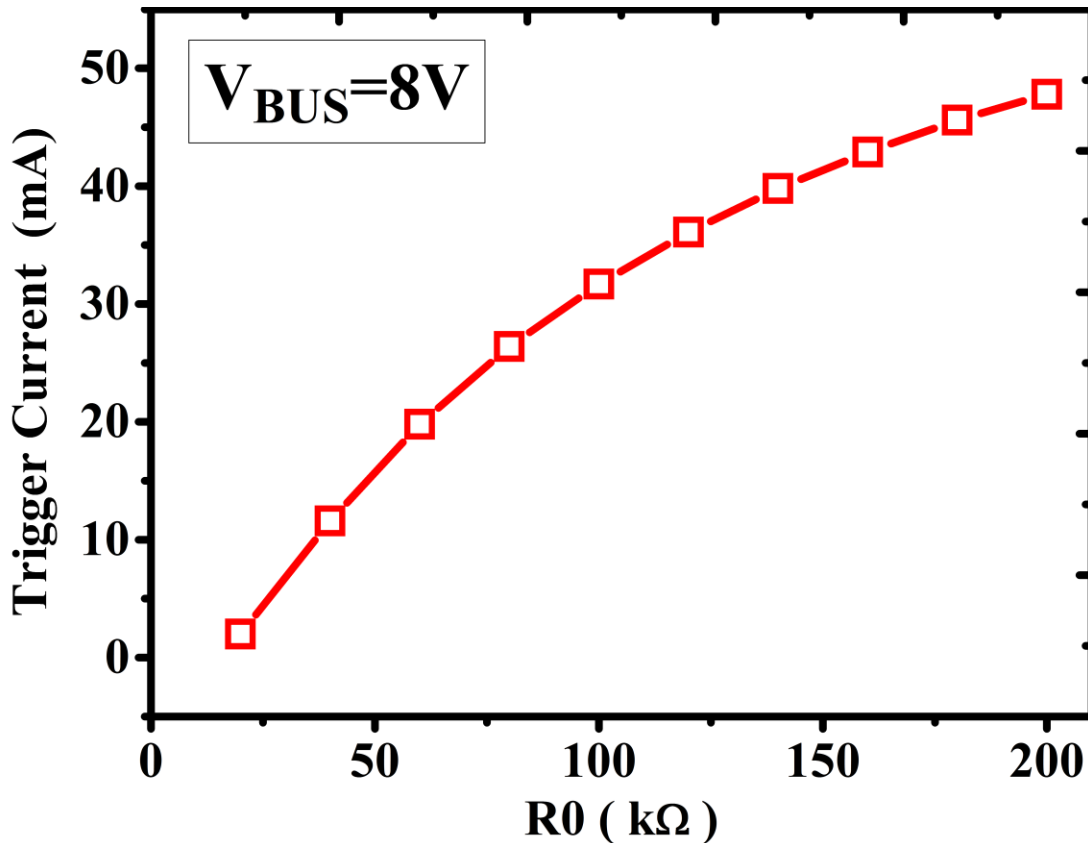


Figure 5-2 Relationship between  $R_0$  and Triggering Current.

However, the triggering efficiency is quite low in the conventional voltage triggered detection circuit. As we mentioned, the turn on voltage of the 8 diodes in series equals to 5.6 V.  $V_{GS}$ , the source to gate voltage of Mp1, equals to the ESD\_BUS voltage  $V_{BUS}$  minus 5.6 V.

According to the drain current equation [34], the relative small  $V_{GS}$  results in a small triggering current, which could be too low to trigger the SCR, and leads to a low triggering efficiency. The simulated relationship between  $R_0$  and the triggering current, when the  $V_{BUS}$  equals to 8 V, is shown in Figure 5-2. Though it could be observed that the triggering efficiency goes up when  $R_0$  increases, it is still not acceptable due to the increased footprint considering the cost. The simulated result when  $V_{BUS}$  equals to 6 V indicates that the triggering current is only around the level of  $\mu A$ , which is too small to turn on a SCR.

### 5.3 Novel Detection Circuit Operation and Simulation

The schematic of the proposed  $2 \times V_{DD}$ -tolerant detection circuit is shown in Figure 5-3. Comparing to the circuit shown in Figure 5-1,  $R_0$  is replaced with a n-type MOSFET (NMOS)  $Mn1$  which costs much less layout area. Another two NMOS  $Mn2$  and  $Mn3$ , and a resistor  $R1$  of 40 k $\Omega$  are added to amplify the detected voltage. Table 5-1 shows the dimensions of the devices used in the proposed detection circuit.

Table 5-1 Dimensions of Devices Used in the Proposed Detection Circuit.

Device	Dimension (W/L)
D1 to D8	4 $\mu m$ / 4 $\mu m$
$Mn1$	0.3 $\mu m$ / 20 $\mu m$
$Mn2$ & $Mn3$	20 $\mu m$ / 0.18 $\mu m$
$Mp1$ & $Mp2$	200 $\mu m$ / 0.18 $\mu m$



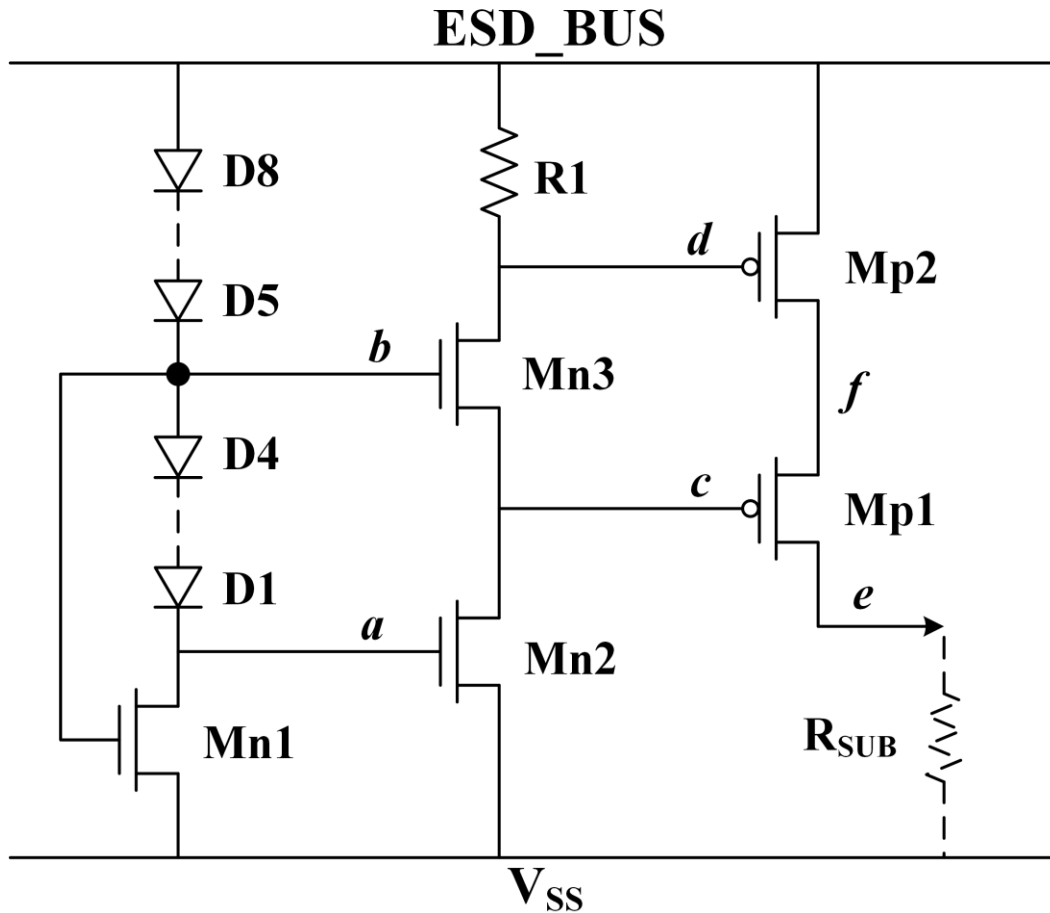


Figure 5-3 Schematic of the proposed voltage triggered  $2 \times V_{DD}$ -tolerant ESD detection circuit.

When the circuit in Figure 5-3 operates under normal condition, the I/O pad receive a signal of  $2 \times V_{DD}$  3.3 V, which does not exceed the turn on voltage of the voltage detector, so the diode string does not conduct. Node b is biased at half of  $V_{BUS}$  so  $V_b$  equals to  $1 \times V_{DD}$ . Mn1 turns on and  $V_a$  is pulled down to 0 V, thus Mn2 and Mn3 keep off and no current flows through the amplifying path.  $V_c$  equals to  $V_b$  so the  $V_{GS}$  of Mn3 equals to 0 V.  $V_d$  equals to  $2 \times V_{DD}$  and both of Mp2 and Mp1 keep off. Therefore, no triggering current is generated under normal operating condition.

A ramp pulse from 0 to 3.3 V within 1 ms is applied to ESD\_BUS to simulate the  $2 \times V_{DD}$  signal processing condition. Simulation results are shown in Figure 5-4 that  $V_a$  equals to 0 V,  $V_b$ ,  $V_c$  and  $V_f$  are all around  $1 \times V_{DD}$ , and  $V_d$  equals to  $2 \times V_{DD}$ . It could be observed that all the devices are in a safe voltage region.

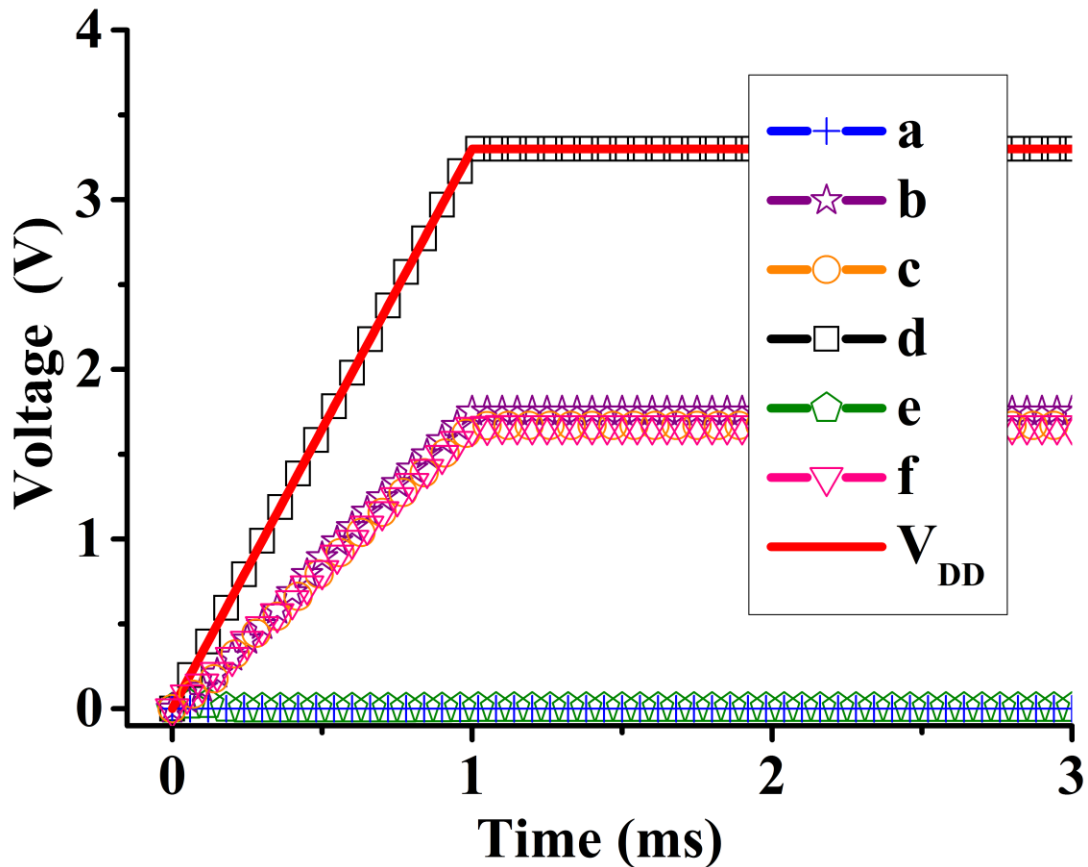


Figure 5-4 Nodes voltages of the proposed circuit in under  $2 \times V_{DD}$  condition.

In an ESD event, the voltage detector turns on when high-voltage ESD pulse comes. A voltage drop exists across Mn1 and Mn2 is turned on then pull  $V_c$  down. A relative low  $V_c$  leads to a large  $V_{GS}$  on Mn3, which pulls  $V_d$  down. Therefore, Mp1 and Mp2 turn on and could generate a large triggering current which could turn on the clamping device.

An ESD-like pulse of 0 to 6 V with a rise time of 10 ns is applied to the ESD\_BUS in the simulation. The voltage of all nodes in the proposed circuit is shown in Figure 5-5(a) and it could be observed that,  $V_c$  and  $V_d$  increase when  $V_{BUS}$  goes up and  $V_e$  stays at a low level. When  $V_{BUS}$  exceed 5 V,  $V_c$  and  $V_d$  fall to a pretty low level rapidly, and it could be observed from Figure 5-5(b) that the triggering current increases up to 50.1 mA when  $V_{BUS}$  reaches 6 V.

We also evaluated the turn-on performance of the proposed circuit.  $V_{BUS}$  firstly increases from 0 to 8 V in 1 ms, and then falls back to 0 in another 1 ms. Figure 5-6 shows the simulation results and it could be observed that when  $V_{BUS}$  exceeds 5.6 V, the voltage of each node change rapidly. When  $V_{BUS}$  reaches 8 V, we observed a triggering current of 65.6 mA, which is much higher than the triggering current shown in Figure 5-2 when a same resistor of 40 k $\Omega$  is used in the conventional detection circuit.

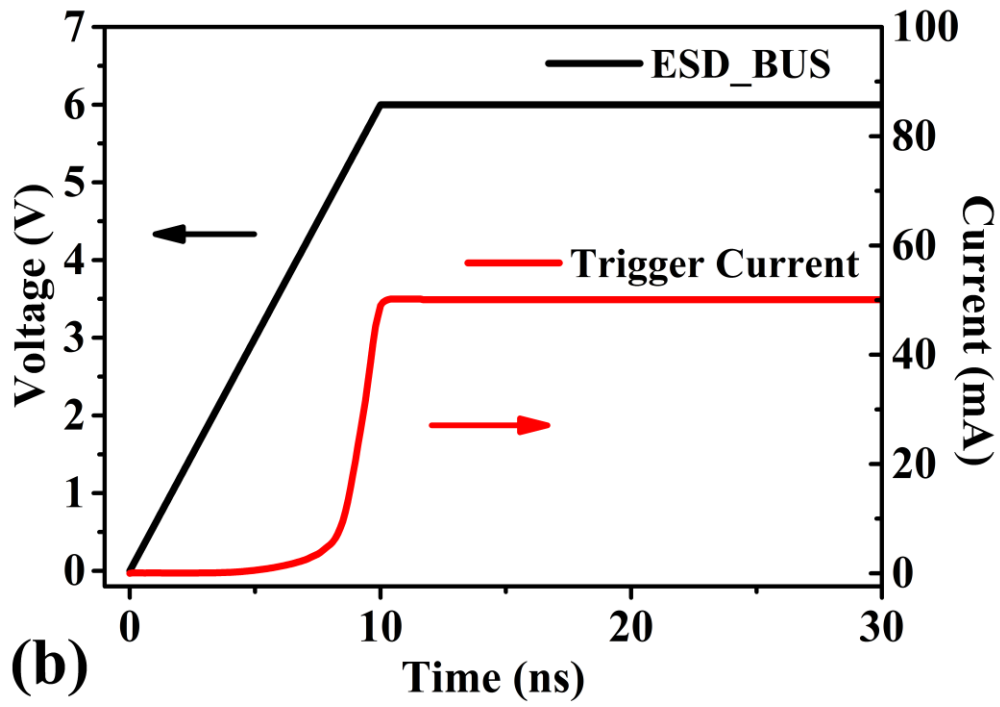
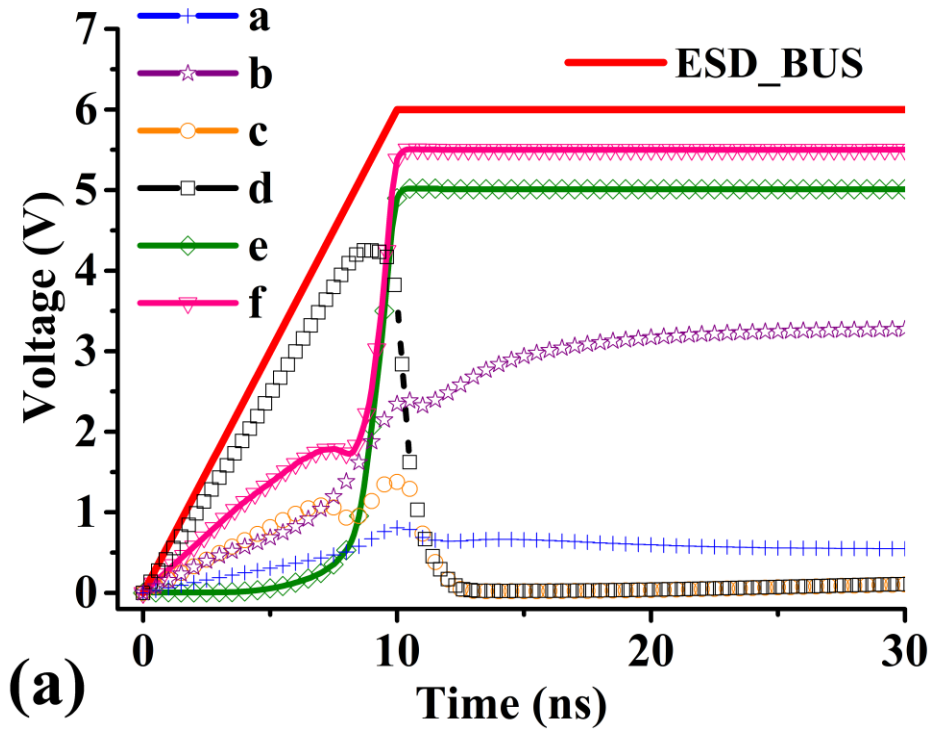


Figure 5-5 (a) Nodes voltages and (b) triggering current of the proposed circuit under the ESD stress.

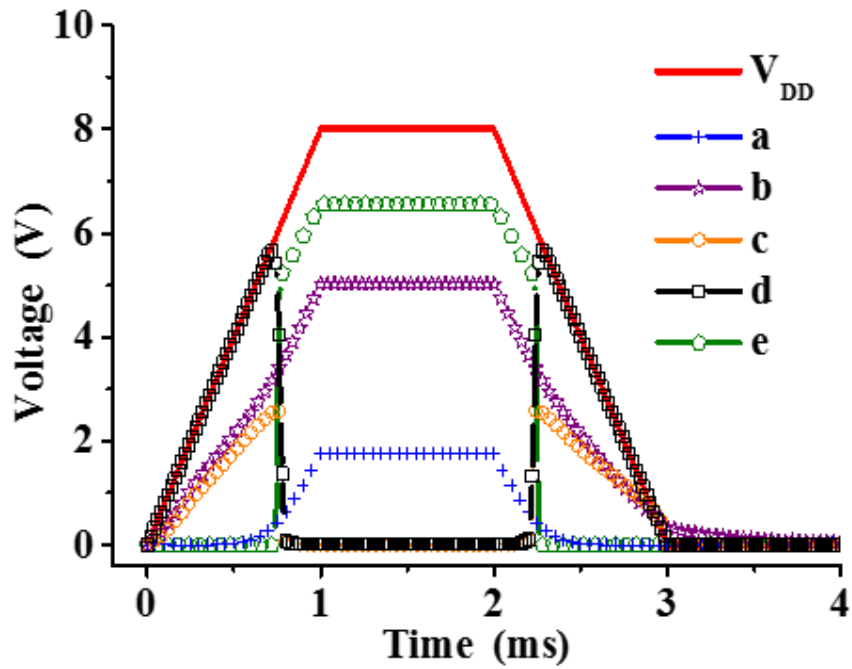


Figure 5-6 Turn-on performance of the proposed circuit.

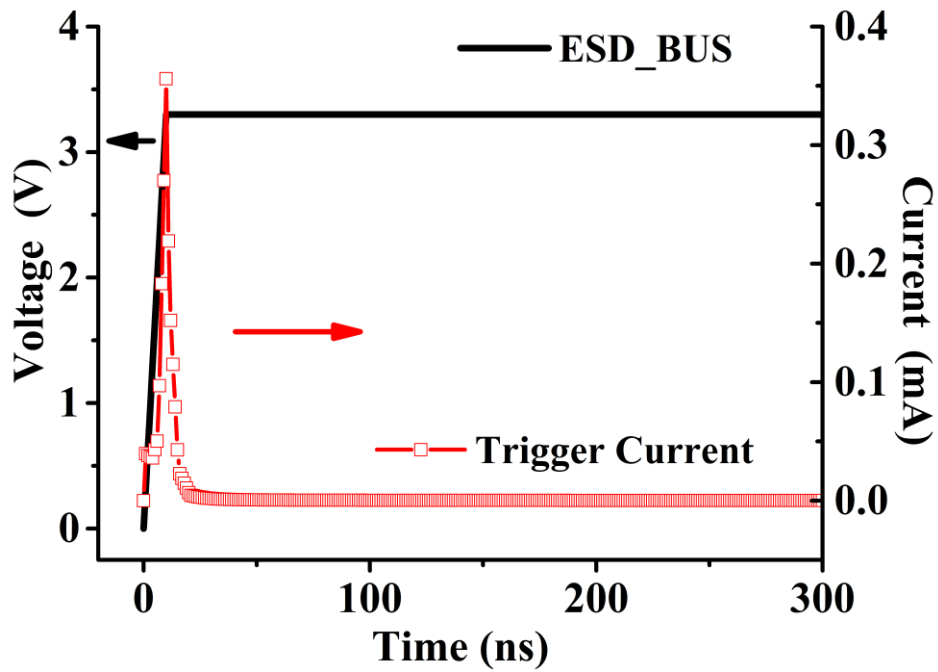


Figure 5-7 Triggering current of proposed circuit under fast power-up events.

To evaluate the immunity from false triggering under fast power-up events, a ramp pulse from 0 to 3.3 V with a rise time of 100 ns is applied to the ESD\_BUS to mimic the fast power-up events. Figure 5-7 shows the simulated triggering current injected into the clamping device, which is only 0.36 mA. To turn on a SCR with diode string, the minimum triggering current need to reach to a few mA. It is obvious that the proposed detection circuit is immune to most of the fast power-up events.

#### 5.4 Conclusion

In this paper, a novel ESD detection circuit with high triggering efficiency for  $2 \times V_{DD}$ -tolerant I/O buffer is proposed and discussed. All the devices operate in a safe voltage region under normal conditions. The proposed voltage triggered detection circuit improves the triggering efficiency with a smaller footprint. The conventional detection circuit with a resistor of 200 k $\Omega$  could generate a triggering current of a few uA and 47.8 mA when  $V_{BUS}$  equals to 6 V and 8 V, respectively. As a comparison, our proposed circuit with a resistor of only 40 k $\Omega$  can generate a triggering current of 50.1 mA and 65.6 mA when  $V_{BUS}$  equals to 6 V and 8 V, respectively. The proposed detection circuit possesses a better sensitivity to ESD event which make it a more reliable ESD protection. Furthermore, the proposed detection circuit is immune to most of the fast power-up events comparing with the RC-based ESD detection circuit. The proposed detection circuit could be a good reference for future ESD power clamp designs.

## CHAPTER 6 DESIGN AND SIMULATION OF NOVEL ESD CLAMP CIRCUIT WITH LOW LEAKAGE CURRENT

### 6.1 Introduction

With the development of silicon technology, the thickness of the gate oxide is scaling down, and a large leakage current could be induced due to such a thin gate oxide if without a proper design and consideration. The static power consumption plays more important role for the total power consumption of integrated circuits (ICs) [63-66], so the leakage issue must be taken care of. As an indispensable part of the whole chip ESD protection, the power supply clamp circuit plays an important role to prevent the thermoelectric breakdown in the internal circuit of ICs [49, 67], and it need to provide a path with low-impedance for each IC to discharge the ESD energy from  $V_{DD}$  to  $V_{SS}$ . The conventional transient ESD clamp circuit usually consists of an RC network as the detection circuit and a MOSFET with a large size as the clamping device, whose size always reaches more than  $500 \text{ um}^2$ . MOS capacitor has the largest capacitance per unit area among the several kinds of capacitors in CMOS process, but its gate leakage current at a relative high level could not be neglected. [62, 68-70] proposed a few designs to enhance the circuit performance or to save footprint, but the leakage issue was not considered. Some recent work studied the reduction of leakage current for the power-rail ESD clamp circuit [71, 72] and the mixed-voltage I/O buffer [54, 60].

In this paper, an ESD clamp circuit for power-rail ESD protection, consisting of the stacked transistors and biased RC network, is proposed in a 90 nm CMOS process. SPICE simulation is carried out and the simulation result shows that it successfully turns on the clamping device under ESD events and reduces the leakage current. It achieves a better

performance with a smaller footprint, and it is also immune to the false triggering and power supply noise.

## 6.2 Proposed Circuit Schematic and Operation

In design of the RC network of the ESD clamps, MOSFET is widely used as resistor which greatly reduce the footprint comparing with the conventional resistor. However, the conventional capacitor still costs a large layout area, and induces a large leakage current at the same time. In our proposed ESD clamp, maintaining a same RC constant, the capacitor area is reduced by increasing the equivalent resistance of the MOSFET resistor. Figure 6-1 shows the schematic of the proposed ESD clamp circuit. As shown on Figure 6-1, a bias circuit consisting of three P-type MOSFET (PMOS) Mp1 to Mp3 are embedded on the left side of the classic RC network and it generates a signal named bias1 for the n-type MOSFET (NMOS) Mn1 and a signal named bias 2 for the PMOS Mp4. Mp1 and Mp3 are two diode-like-connected PMOS. The gate of Mp2 is connected to its source which makes it constantly turned off and results in a pretty small power consumption in the bias path. Both of Mp1 and Mp3 operate in the sub-threshold region due to the minimized current in the bias path, and the voltages across the Mp1 and Mp3 are relative small. Therefore, the gate voltage  $V_G$  of Mn1 is small too, which results in a greatly increased equivalent resistance of the MOSFET resistor, Mn1 and a greatly reduced capacitance C1 and C2 that are only 50 fF with a size of 1.9 um by 1.9 um. The total layout area of the capacitor is only 7.2 um<sup>2</sup>. The stacked capacitance generates a pretty small leakage current. When the proposed circuit operates under normal condition, Mn1 is in the sub-threshold region and CLK is tied to 0, which make Mn2 thoroughly turned off. Mp4 also operates in the sub-



threshold region so CLK\_b is tied to  $V_{DD}$  which makes Mp5 turned off. Mn3 pulls  $V_G$  of Mn0 to 0 so Mn0 is turned off. When the proposed circuit is falsely triggered by some certain factors, M0 will turn on and last a delay time then finally turns off due to the sub-threshold current. In such a turn-off mechanism, our proposed ESD clamp can turn off in a quite short time even if it is falsely triggered.

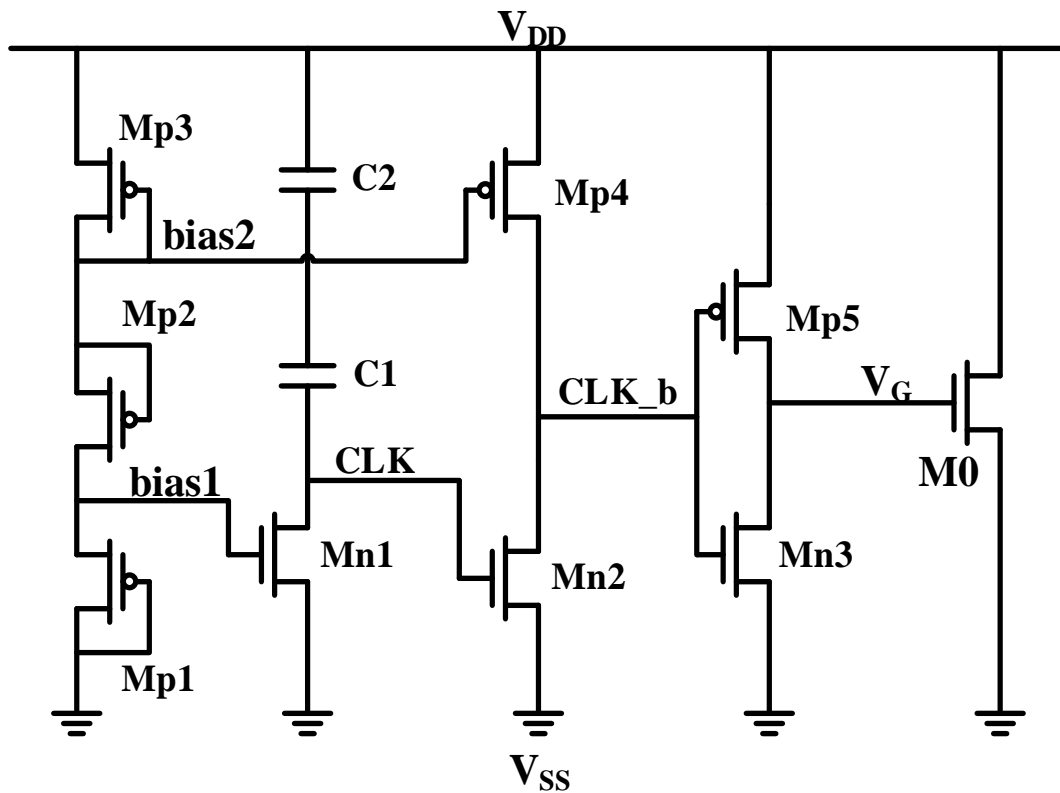


Figure 6-1 Schematic of proposed ESD clamp circuit.

When the ESD event comes, CLK is tied to a high voltage when RC network responds to the fast power-up event and Mn2 turns on. As the gate of Mp4 is connected to bias2, the  $V_{GS}$  of Mp4 is much smaller than  $V_{DD}$ . Mn2 pulls down the signal CLK\_b. Due to the relative large W/L ratio of Mp5,  $V_G$  of M0 is pulled up quickly and M0 finally turns on to discharge the ESD

energy. With the RC network being charged, CLK gradually falls to 0 and the sub-threshold current of Mp4 pulls CLK\_b up with a low speed which results in a long hold-on time for ESD discharging. If the gate of Mp4 is connected to CLK instead of bias2,  $V_G$  of M0 will fall to 0 quickly which requires a much larger RC constant for a long enough discharge time.

### 6.3 Simulation Result and Discussion

SPICE simulation is carried out in Cadence Spectre. Table 6-1 shows the dimensions of the devices used in the proposed ESD clamp.

Table 6-1 Dimensions of Devices Used in the Proposed Detection Circuit.

Device	Dimension (W/L)
C1 & C2	1.9 $\mu\text{m}$ / 1.9 $\mu\text{m}$
Mp1 to Mp3	0.5 $\mu\text{m}$ / 0.2 $\mu\text{m}$
Mp4	1 $\mu\text{m}$ / 0.18 $\mu\text{m}$
Mp5	80 $\mu\text{m}$ / 0.12 $\mu\text{m}$
Mn1	0.2 $\mu\text{m}$ / 2 $\mu\text{m}$
Mn2	1 $\mu\text{m}$ / 0.1 $\mu\text{m}$
Mn3	2 $\mu\text{m}$ / 0.1 $\mu\text{m}$

Figure 6-2 shows the simulated waveform of each node under the ESD event. An ESD-like pulse of 0 to 3V with a rise time of 10 ns is applied in the simulation. It could be observed from Figure 6-2 that  $V_{\text{CLK}}$  is tied to a high voltage at the beginning and Mn2 is turned on. Then

$V_{CLK\_b}$  goes down and Mp5 is turned on, which pulls  $V_G$  of M0 up so M0 is finally turned on to discharge the ESD energy. The simulation result also shows that the total hold-on time is more than 800 ns, which is long enough for ESD discharging.

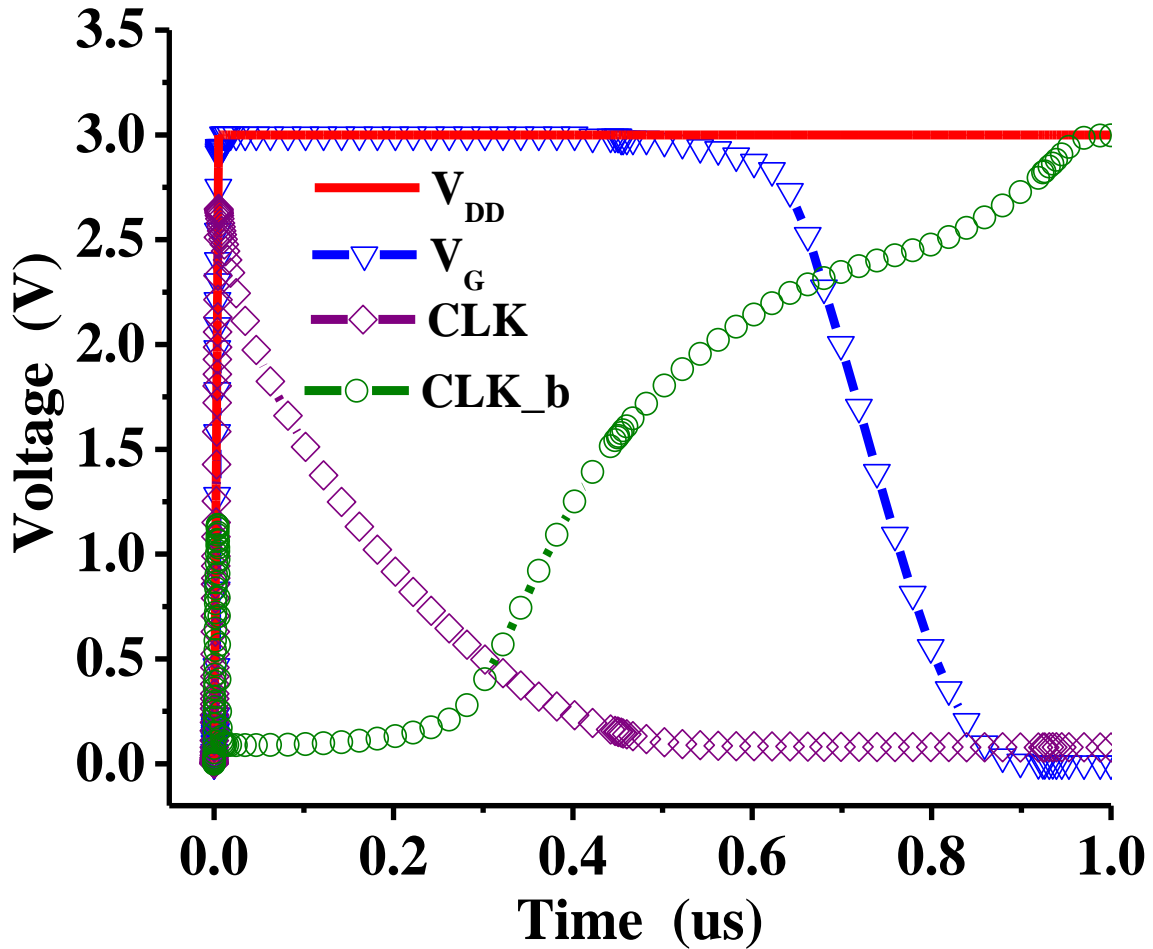


Figure 6-2 Waveforms of the nodes voltages under the ESD event.

Figure 6-3 shows the simulated voltage waveforms of each node and triggering current when the proposed circuit operates under the normal condition. A  $V_{DD}$  rising from 0 to 1.2 V in 1 ms is used to mimic the normal power-up event. The RC network does not respond to the normal operation due to the slower transient frequency. Bias 1 and bias 2 are measured as 0.106 V and

1.09 V, respectively and it could be seen that M0 is turned off. The leakage current of the RC detection circuit keeps at 12 nA which his pretty small, and it could also be observed that the total leakage current is 117 nA which is also much smaller than conventional designs.

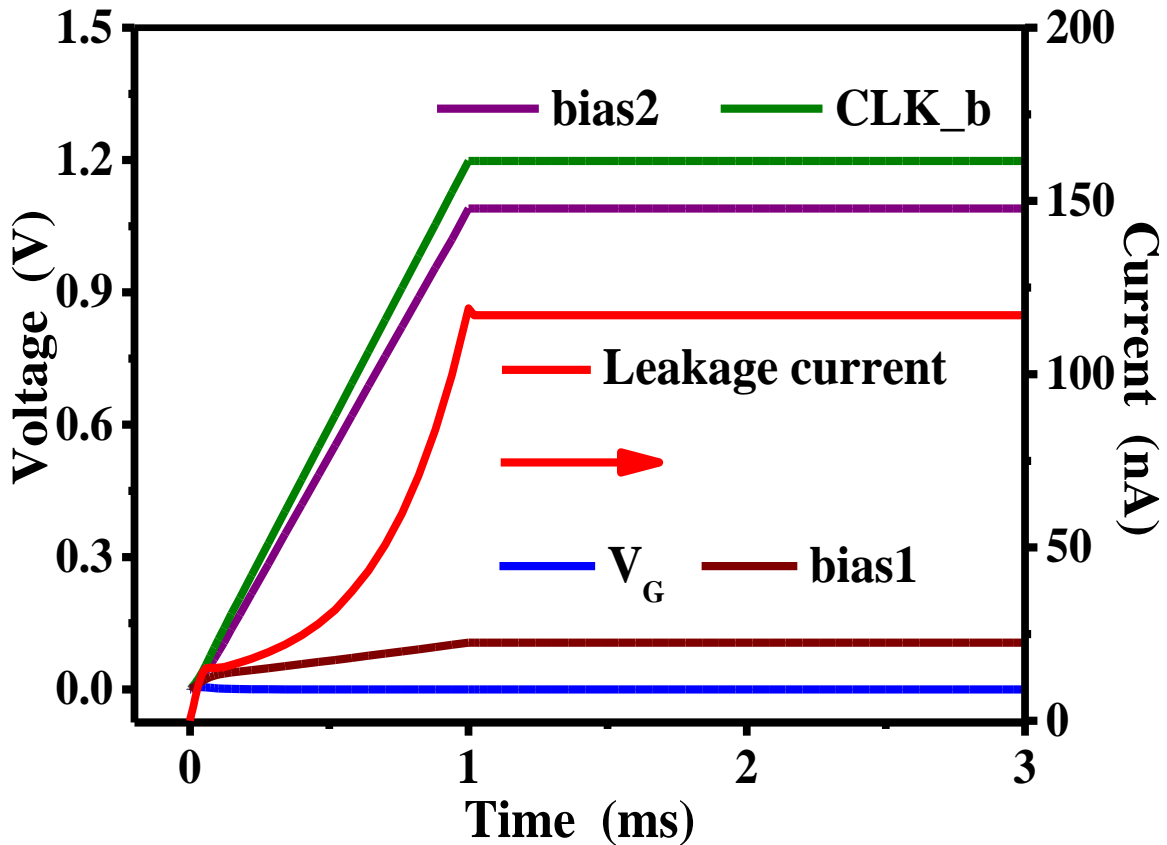


Figure 6-3 Waveforms of the nodes voltages and leakage current under normal condition.

A HBM simulation is also conducted on the proposed circuit. A HBM pulse of 2 kV is applied in this simulation. Figure 6-4 shows the simulation results and it could be observed that maximum  $V_{DD}$  and  $V_G$  of M0 reach to 3.5 V and 3.3 V, respectively, and then fall to 0. The simulation result indicates that our proposed design passes the HBM protection requirement of a

90 nm process, and the clamp could sustain a higher HBM stress by enlarging the size of the clamping device M0.

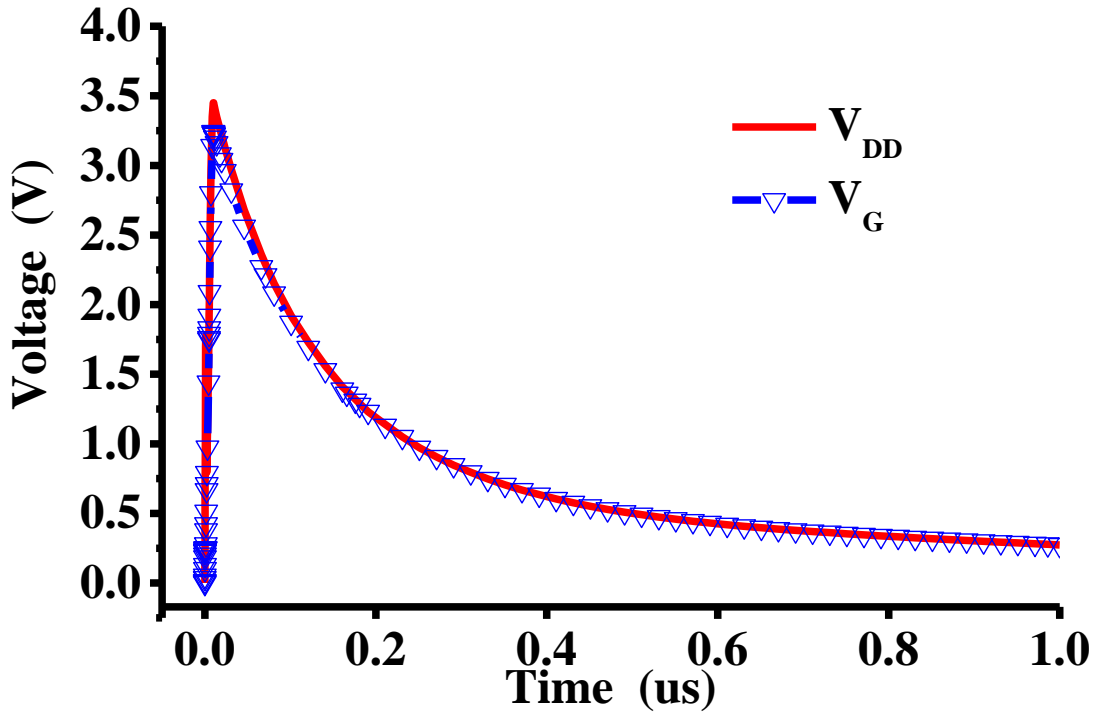


Figure 6-4 Waveforms of nodes voltage under HBM simulation.

Figure 6-5 shows the simulation result of  $V_G$  of M0 under three different fast false triggering event.  $V_{DD}$  rises from 0 to 1.2 V with a rise time of 400 ns, 500 ns, and 600 ns, respectively. It could be observed that in the case with rise time of 400 ns, M0 is turned on but turned off within 1 us. The clamp is not triggered with a rise time longer than 500 ns. This simulation verifies that our proposed ESD clamp is immune to most false triggering, and there is a quick turn-off mechanism once falsely triggered.

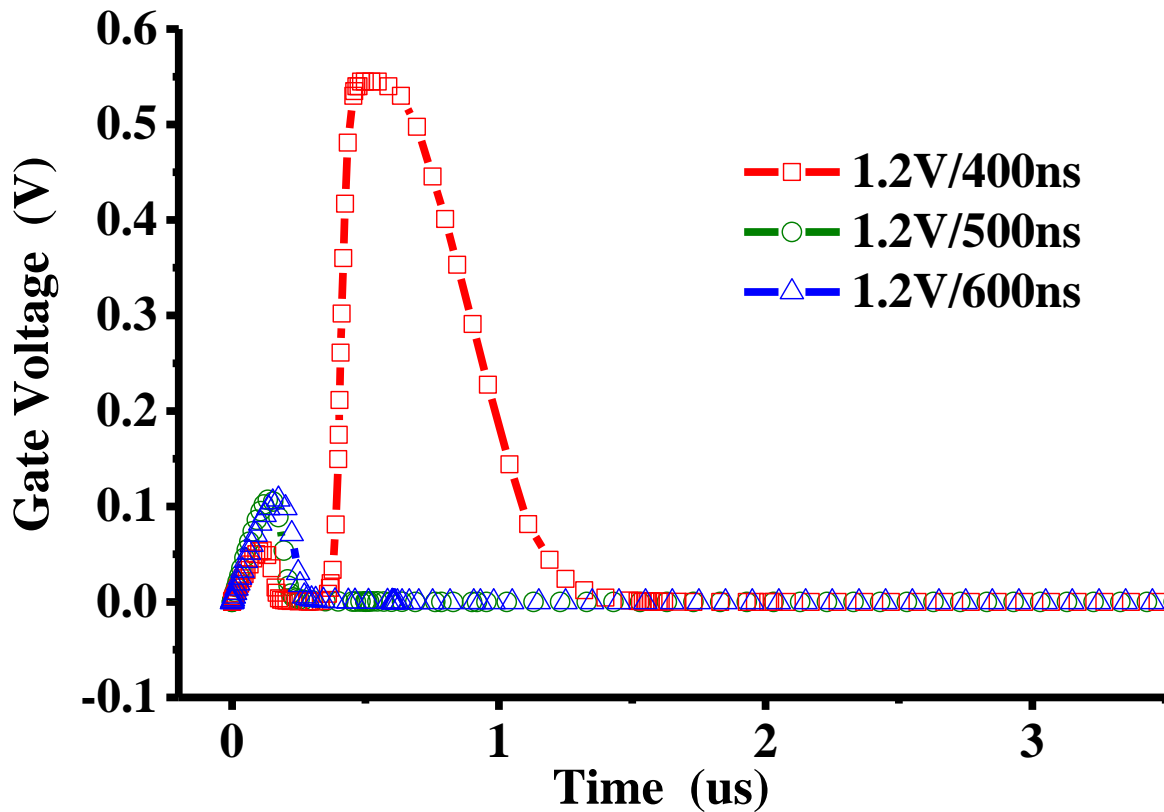


Figure 6-5 Waveforms of gate voltage under fast power-up event.

#### 6.4 Conclusion

In this paper, a novel ESD clamp consisting of biased RC network and the stacked transistors is proposed in a 90 nm CMOS process. Comparing with the conventional RC based ESD clamps, the footprint, the leakage current and the power consumption are greatly reduced in our proposed design. The proposed ESD clamp has a long hold-on time of 800 ns under ESD event and is immune to most of the false triggering. A quick turn-off mechanism also exists once the clamp is falsely triggered. Simulation is carried out to verify our design and our proposed

ESD clamp could be a good reference for future ESD power clamp designs which require low leakage current and small footprint.

## CHAPTER 7 SUMMARY AND OUTLOOK

As we discussed in this dissertation, ESD induced failures in IC has been one of the major reliability concerns in semiconductor industry and with the development of advanced semiconductor technologies, the concern of ESD will not vanish, but become more severe.

The ESD protection design for different applications need to be considered and designed case by case, especially for some special applications. LSCR is the simplest and the most basic SCR-based ESD protection device. However, it could not be directly used in ESD protection due to its large snapback window. Therefore, the variations based on LSCR have been proposed for different applications over the decades. Some of the automotive ESD protection requires a ESD protection device without snapback for its capacitive pins to avoid the displacement current induced by the large snapback from the ESD protection device. We have proposed the NSSCR for HV ESD protection and DCSCR for LV and MV ESD protection. Our proposed devices provide with flexible options to ESD designers in designing work for different voltage node, and by understanding the physical mechanism of how we get a higher holding voltage or quick triggering process, people get insights which is helpful to their designs with similar circumstances.

ESD protection devices without snapback are not the only challenge in automotive electronics. In some cases, the automotive electronics need to work under temperatures much higher than the typical highest working temperature requirement of general ICs which is 125 °C. Therefore, understanding the operation of ESD protection devices under high temperature is essential to automotive ESD protection design. In this dissertation, we introduced our investigation of characteristics of ESD protection devices under elevated temperatures, and some



of the parameters are investigated and reported for the first time. Our work could provide with designers with insights on their selection of ESD protection devices for high temperature applications, and by providing with the physical mechanism behind the variations of ESD parameters, people get better understanding on the high temperature operation and also get insights how to optimize the devices if they need to.

Space electronics is a hot topic recently, and as we mentioned, the space is an environment with kinds of irradiation sources as well as ESD. Meantime, ESD protection devices are essential elements needed in designing of space electronics. Therefore, understanding the operation characteristics of ESD protection devices under irradiation is very important. In this dissertation, for the first time, we investigated the characteristics of a few ESD protection devices under TID effects and analyzed the variations of the key ESD parameters. Through this work, we provide with insights to designers on selection of ESD protection devices for such application.

Sole ESD protection device is not enough for the whole chip ESD protection design. ESD clamp circuits are very important part of ESD protection designs, too. In the ESD clamp circuit, the detection circuit is an essential part as it is responsible to the very first response to ESD signal in a ESD event. In this dissertation, we introduced a novel voltage controlled ESD detection circuit we proposed, and comparing with the conventional design, our novel detection circuit realize a much better triggering efficiency with a much smaller footprint. Meantime, it is also immune to most of the false triggering by fast power-up events. Our novel design gives insights to IC designers on optimization of ESD detection circuit.

Leakage current is also a concern in the ESD clamp circuit. A high leakage current not only increases the power consumption of ICs, but degrades the performance of the ESD protection part. In this dissertation, we introduced a novel power clamp we proposed which has a very low leakage current. Our proposed clamp realizes a low leakage current with a very good footprint efficiency, and also has a long hold-on time to ensure enough time for ESD current discharge. It also has a quick turn-off mechanism for false triggering. Our proposed circuit gives a new option for designers on power line ESD protection design.

As a summary, a few research works on design, simulation and characterization of ESD protection devices and circuits in advanced semiconductor technologies are introduced in this dissertation. This dissertation could be a good reference for future ESD protection design.

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