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## Investigation Of High-k Gate Dielectrics And Metals For Mosfet Devices.

Sriram Mannargudi Seshadri  
*University of Central Florida*

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INVESTIGATION OF HIGH- $k$  GATE DIELECTRICS AND METALS FOR  
MOSFET DEVICES

by

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B.E. PSG College of Technology, 2000

A thesis submitted in partial fulfillment of the requirements  
for the degree of Master of Science  
in the Department of Electrical and Computer Engineering  
in the College of Engineering and Computer Science  
at the University of Central Florida  
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2005

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## ABSTRACT

Progress in advanced microlithography and deposition techniques have made feasible high- k dielectric materials for MOS transistors. The continued scaling of CMOS devices is pushing the Si-SiO<sub>2</sub> to its limit to consider high-k gate dielectrics. The demand for faster, low power, smaller, less expensive devices with good functionality and higher performance increases the demand for high-k dielectric based MOS devices. This thesis gives an in-depth study of threshold voltages of PMOS and NMOS transistors using various high-k dielectric materials like Tantalum pent oxide (Ta<sub>2</sub>O<sub>5</sub>), Hafnium oxide (HfO<sub>2</sub>), Zirconium oxide (ZrO<sub>2</sub>) and Aluminum oxide (Al<sub>2</sub>O<sub>3</sub>) gate oxides. Higher dielectric constant may lead to high oxide capacitance (C<sub>ox</sub>), which affects the threshold voltage (V<sub>T</sub>) of the device. The working potential of MOS devices can be increased by high dielectric gate oxide and work function of gate metal which may also influence the threshold voltage (V<sub>T</sub>). High dielectric materials have low gate leakage current, high breakdown voltage and are thermally stable on Silicon Substrate (Si).

Different kinds of deposition techniques for different gate oxides, gate metals and stability over silicon substrates are analyzed theoretically. The impact of the properties of gate oxides such as oxide thickness, interface trap charges, doping concentration on threshold voltage were simulated, plotted and studied. This study involved comparisons of oxides-oxides, metals-metals, and metals-oxides. Gate metals and alloys with work function of less than 5eV would be suitable candidates for aluminum oxide, hafnium oxide etc. based MOSFETs.

Dedicated to my parents and brother

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## LIST OF ACRONYMS/ABBREVIATIONS

$V_T$	Threshold voltage
$T_{OX}$	Oxide thickness of the film
$Q_I$	Interface trap charge
$Q_D$	Depletion charge
$\epsilon_0$	Relative permittivity at vacuum
$K$	Dielectric constant of gate dielectric
$C_{OX}$	Oxide Capacitance
$\Phi_{MS}$	Metal-Semiconductor work function
$\Phi_M$	Metal work function
$\Phi_S$	Semiconductor work function
$\Phi_F$	Fermi potential of the substrate
$k$	Boltzmann's constant
$T$	Temperature in Kelvin
$q$	Electronic charge
$N_A$	Acceptor doping concentration
$N_D$	Dopant doping concentration
$n_i$	Intrinsic charge
$L$	Channel Length
$Q_{OT}$	Oxide trapped charge
$X_j$	Junction depth

# CHAPTER ONE: INTRODUCTION

## 1.1 Overview

Since the early 1970s, the metal oxide-semiconductor-field-effect-transistor (MOSFET) has been the most widely used device in VLSI circuits, because of its simpler structure, less cost to fabricate and less power consumption compared to bipolar and junction field-effect transistors (BJTs and JFETs). The demand for greater integrated circuits in the industry for functionality and low cost performance requires an increase in current density. The device scaling is one of the main factors which results in shrinking of gate dielectric thickness ( $T_{OX}$ ) and channel length ( $L$ ) [1]. The dielectric material used as gate oxide in MOSFETs plays an important role in the threshold voltage ( $V_T$ ) and working potential of the device. High-k dielectric materials are currently in consideration for gate insulators in silicon MOS devices which affects the threshold voltage ( $V_T$ ). These materials having high dielectric constants improves the oxide capacitance ( $C_{OX}$ ), provides better stability over silicon substrates, has low gate leakage current, low power dissipation and high breakdown voltages.

As the demand for more number of device components in ICs increases, the transistor size decreases and occupies less area. The increase of transistors on a chip has reduced the oxide thickness of MOS devices to such an extent that nowadays the  $SiO_2$  thickness is 2nm or less. Figure 1.1 illustrates the trend in oxide thicknesses over the past decade in MOS devices [2].

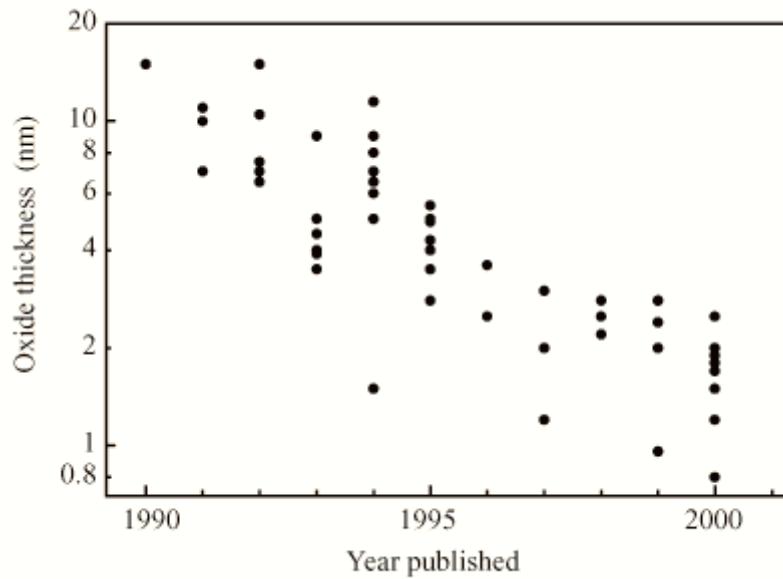


Figure 1.1 Historical trend of SiO<sub>2</sub> insulator thickness vs. year

The International Technology Roadmap for Semiconductors (ITRS) describes the technology of device feature size to be reduced in the years ahead. The traditional scaling with respect to feature size and key scaling factors are listed in Table 1 [12].

Table 1 Feature size and scaling factors of MOS device.

FEATURE	LIMIT	REASON
Oxide Thickness	2.3 nm	Leakage ( $I_{GATE}$ )
Junction Depth	30 nm	Resistance ( $R_{SDE}$ )
Channel Doping	$V_T=0.25$ V	Leakage ( $I_{OFF}$ )
SDE Under Diffusion	15 nm	Resistance ( $R_{INV}$ )
Channel Length	0.06 $\mu$ m	Leakage ( $I_{OFF}$ )
Gate Length	0.10 $\mu$ m	Leakage ( $I_{OFF}$ )

Figure 1.2 illustrates the technology node trends in the years ahead. Figure 1.3 shows the Intel's Lithography Roadmap trend in the feature size in the future [3].

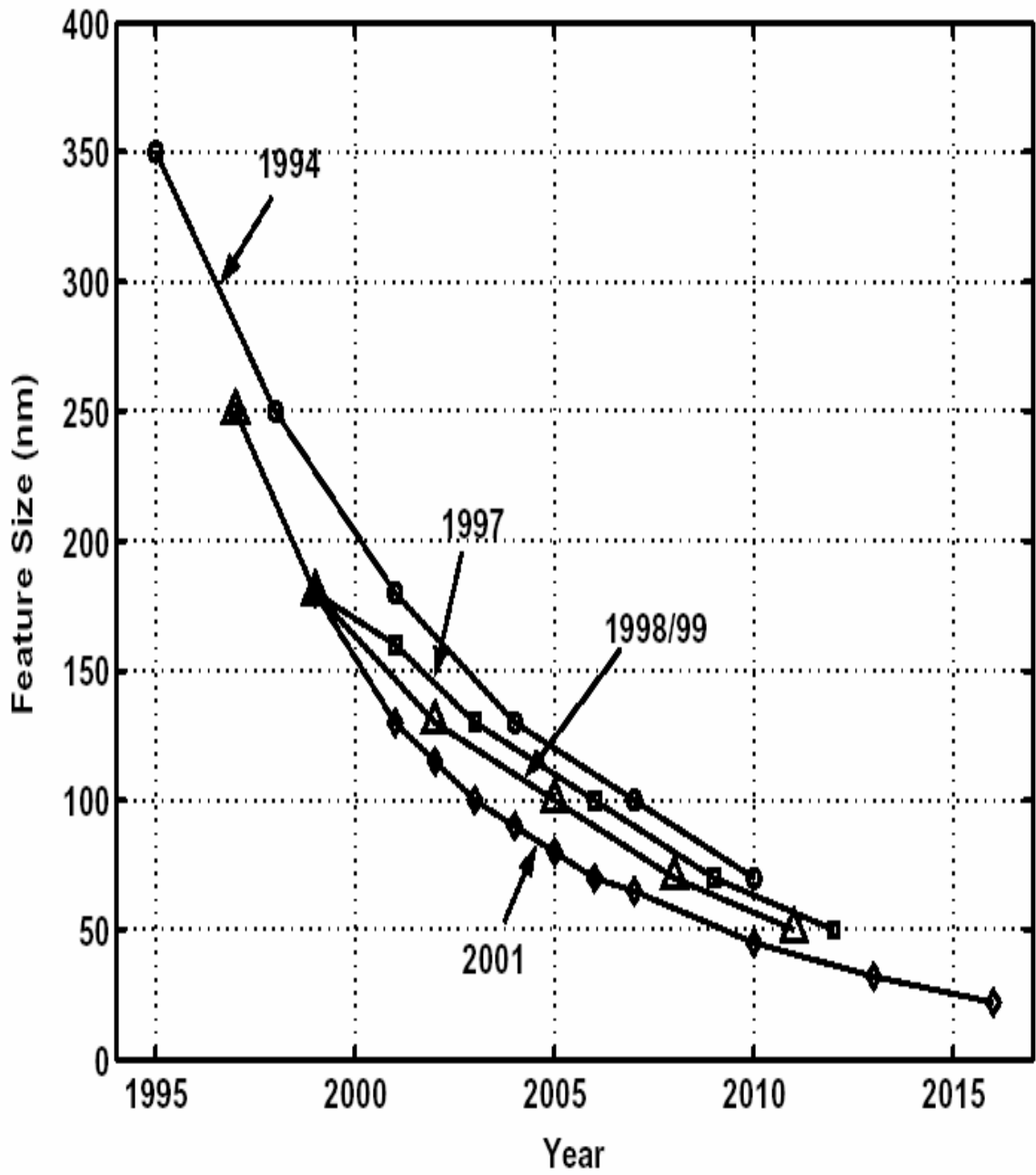


Figure 1.2 Technology Road Trends for ITRS Roadmap

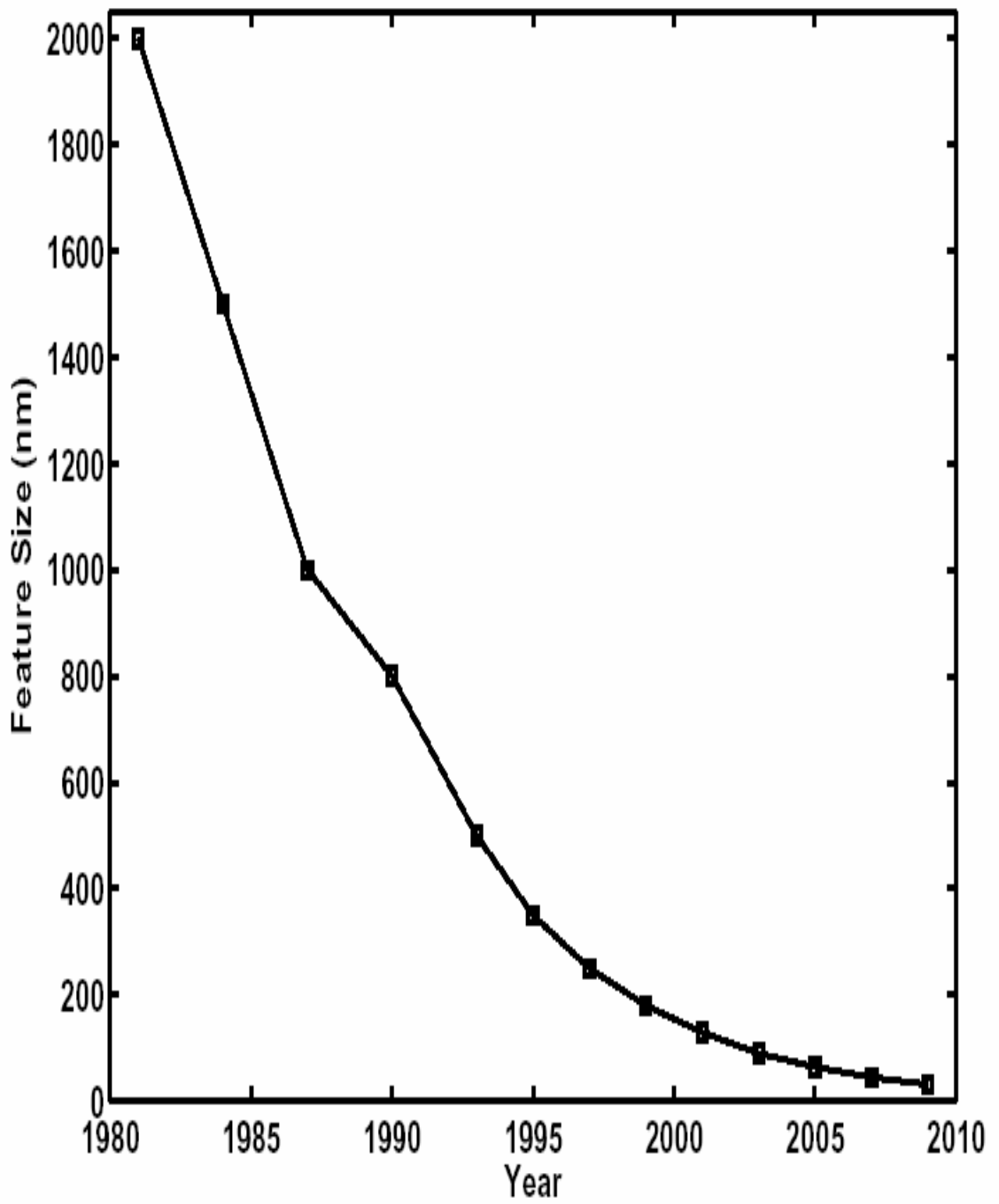


Figure 1.3 Technology node trends for Intel Lithography Roadmap



### **1.1.1 Limitations of SiO<sub>2</sub>**

Advances in scaling and technology have led to reduce the gate oxide thickness less than 20Å and significant challenges for dielectric materials. As we go below 20Å, direct tunneling through potential barrier can lead to high leakage current, which may lead to circuit instability and high power dissipation. There is a good chance of dielectric breakdown, which may lead to defects; non-uniformity in the film thickness, dopant penetration into the substrate, increase in interface trap charges (Q<sub>IT</sub>) and oxide trapped charges (Q<sub>OT</sub>). Silicon dioxide has been extensively used as gate dielectric for many years [4]. Because of all the above reasons, there is need to find alternative high k dielectric materials which can solve the problem.

### **1.2 What is a dielectric material?**

Dielectric materials are substances which are poor conductor of electricity, an insulator but an effective supporter of electrostatic fields. The flow of current is kept to a minimum between opposite electric charge poles without interrupting the electrostatic lines of flux; electrostatic field can also store energy. This is the property which we use in capacitors. The property of dielectric material is to support electrostatic field while dissipating minimal energy in the form of heat. The lower the energy dissipated in the form of heat, more effective is the dielectric material. Metal oxides in general have high dielectric constants [5]. The important property of high dielectric substances, such as aluminum oxide, hafnium oxide, tantalum oxide, zirconium oxide etc. are, they make high value oxide capacitance with less physical thickness.

### **1.2.1 High k dielectric materials**

Dielectric materials having high dielectric constants are used as gate dielectric in MOSFETs. The dielectric materials which are looked into this study in detail are aluminum oxide ( $\text{Al}_2\text{O}_3$ ), hafnium oxide ( $\text{HfO}_2$ ), tantalum pent oxide ( $\text{Ta}_2\text{O}_5$ ) and zirconium oxide ( $\text{ZrO}_2$ ). High dielectric materials make high value of oxide capacitance ( $C_{\text{OX}}$ ) which may influence the threshold voltage ( $V_T$ ) and working of the device. The high-k dielectric materials should reduce the leakage current, lower the power consumption, lower direct tunneling effect and be stable over silicon substrates. These materials should have high breakdown voltage and less prone to time dependent dielectric breakdown (TDDB). The dielectric constants of these materials totally depend upon the way they are deposited over the silicon substrate. The dielectric constant for the same oxide may vary using different deposition techniques. The dielectric layers with higher electrical permittivity are used for thicker films to reduce the leakage current and improve upon the reliability of the gate dielectric layer with electrical thickness equal to ultra thin  $\text{SiO}_2$  layer.

### **1.2.2 Materials properties**

There are many dielectric materials whose dielectric constant is more than 3.9 ( $\text{SiO}_2$ -dielectric constant). However, the materials should be chosen with properties such as permittivity, barrier height, stability in direct contact with silicon, device processing and integration. The materials should also have good interface quality, compatible with the gate, process compatible and reliable. For limiting the leakage current, barrier height should also be taken into consideration. Figure 1.4 shows the energy band diagrams for ideal MOS for both n-type and p-type semiconductor.

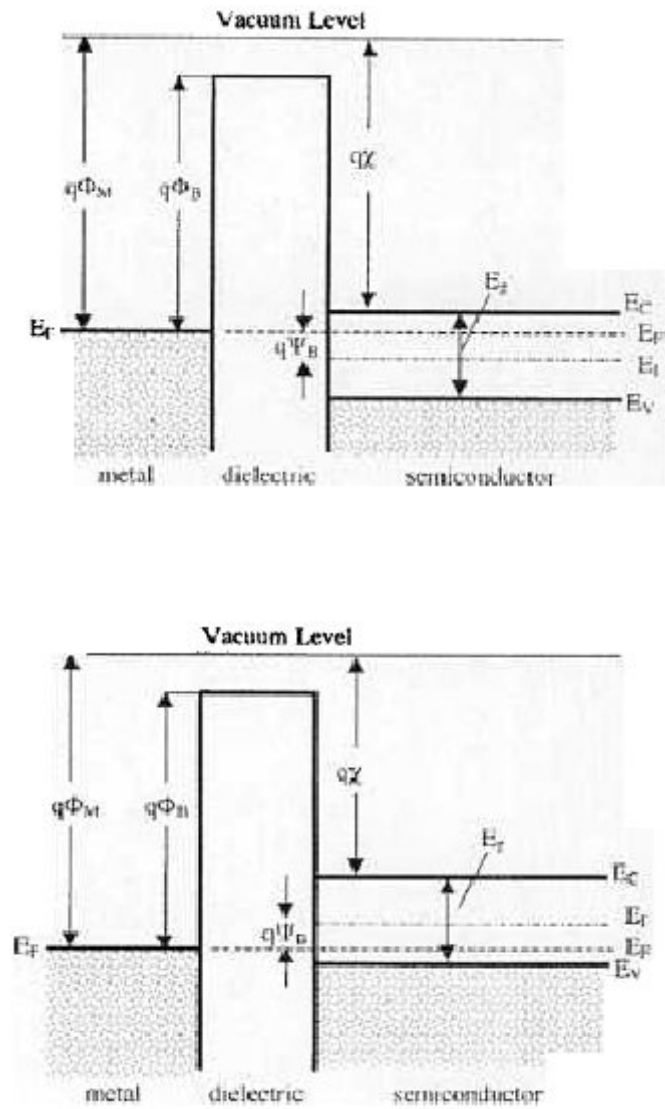


Figure 1.4 Energy band diagrams of ideal MOS n-type and p-type semiconductor

The calculated band offsets for some dielectrics are shown in figure 1.5. The large band gap of dielectrics is due to a large  $\Delta E_c$ . The band gap should be more than 5eV to achieve good conduction band offset [1, 6-7].

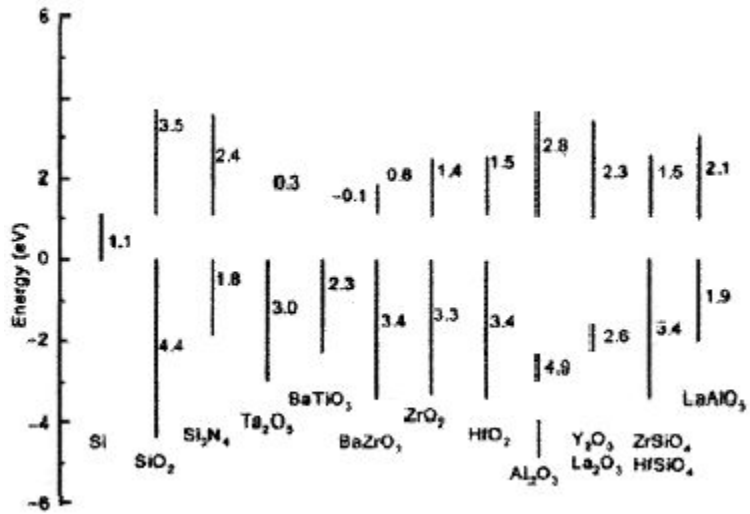


Figure 1.5 Band offset of different oxides on Silicon Substrates

The dielectric constants of different dielectric materials corresponding to their band gap are shown in figure 1.6.

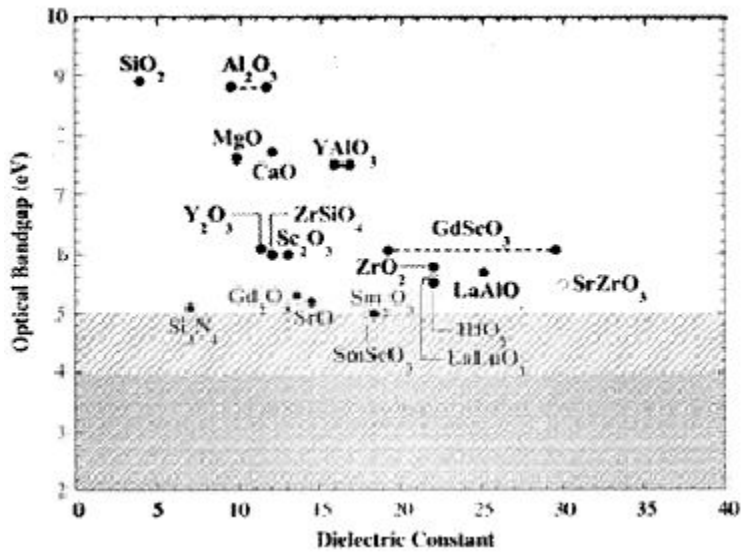


Figure 1.6 Plot of dielectric constants of various oxides vs. band gap

### 1.2.3 High-k dielectric materials: challenges

The challenges of high-k dielectric material are

- Mobility degradation.
- Fixed charges.
- Charge trapping and threshold voltage ( $V_T$ ) shifts.
- Hot carrier effects due to reduced energy barriers for electrons and holes.
- Diffusion of oxygen and dopant on to the silicon substrate.

### 1.3 Limitations of Poly silicon as gate electrode

As we scale the gate oxide thickness, the importance of poly silicon/ gate dielectric interface becomes necessary to consider different gate electrodes. Even though the metal work function of poly-silicon is very low, there are some problems as gate electrode. The poly silicon itself gets depleted as scaling goes beyond 20Å. So poly silicon should be replaced by more conductive materials. The recent advances in technology have made to deposit gate electrode before the oxide to be grown over the device to work. The gate electrode should be of such a material which should eliminate the depletion capacitance compared to poly-silicon. The gate electrode or gate metals which have been discussed in this work are aluminum, ruthenium and Pt-Ru alloys.

## **1.4 Purpose of the research**

The goal of the thesis is to investigate different dielectric materials for gate oxides by MOSFETs with Aluminum, Ruthenium and Pt-Ru alloys as gate metals. The impact of threshold voltage using different gate oxides, gate metals for NMOS and PMOS field effect transistors are investigated theoretically, studied and plotted.

Chapter 2 of this work discusses in detail on the operation of MOSFETs and importance of threshold voltage.

Chapter 3 gives an overview of gate oxides, gate metals, deposition techniques investigated for this work.

In Chapter 4, results, calculations and impact of interface trap charges, doping concentration, oxide thickness on threshold voltage are discussed.

In Chapter 5, conclusion of this thesis is summarized and discussed. The further scope of improvements based on simulation and future work are also suggested.

## **CHAPTER TWO: METAL-OXIDE-SEMICONDUCTOR -FIELD-EFFECT-TRANSISTORS**

### **2.1 Introduction of MOSFETs**

MOSFETs as the name suggests are known as metal-oxide-semiconductor-field-effect-transistors. They are most important devices for microprocessors, VLSI circuits and DRAM cells. They are also used in power applications, communications and in the computer industry. The current in MOSFET is field controlled and is transported predominantly by carriers of any one polarity (e.g. holes in p-channel MOS and electrons in n-channel MOS). The MOSFET is a four terminal device consisting of gate, source, drain and substrate terminals. The substrate terminal is usually grounded for testing purposes. The source and drain are heavily doped regions to reduce their resistance and are back to back p-n junctions in which depletion region is entirely into the substrate.

The metal contact over the insulator is known as gate electrode. The gate electrode is usually made of aluminum or poly-silicon according to design specifications. The gate electrode is isolated from the substrate (conducting channel) by a dielectric which is an oxide usually of  $\text{SiO}_2$  or any other high-k dielectric oxide. The oxide reduces the leakage current; however, there may be interface trap charges near the oxide-semiconductor interface. This may degrade our device performance.

## 2.2 Principle of Operation

A n-channel MOSFET is shown in Figure 2.1 [8]. Two  $n^+$  regions are formed in the p-type silicon using diffusion or implantation. The gate electrode and conducting channel ( $L$ ) are separated with the help of silicon di-oxide layer, which is beneath the gate and sandwiched between drain and source regions.

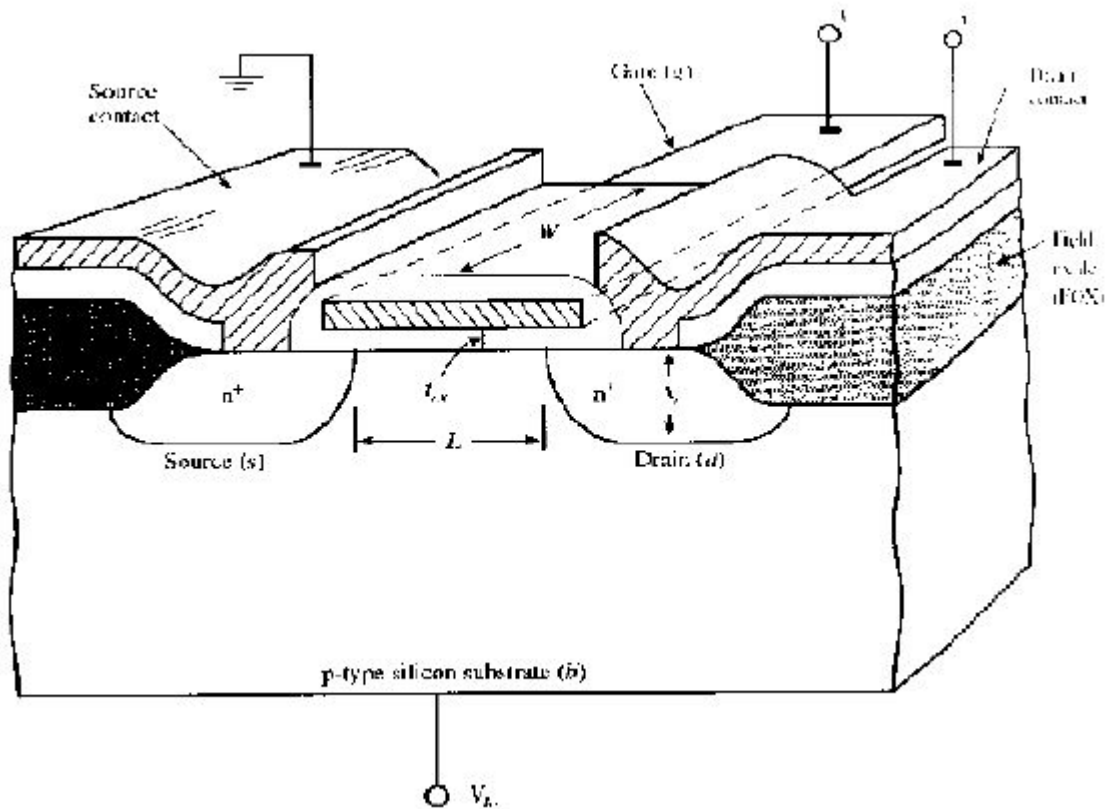


Figure 2.1 Three-dimensional Cross-Section of n-MOSFET

The device parameters are oxide thickness ( $T_{OX}$ ), channel width ( $W$ ), channel length ( $L$ ), which is the distance between two  $n^+$  regions, junction depth  $X_j$  (depth of the two  $n^+$  regions) and the doping concentration ( $N_D$ ). Field oxide is thick enough to isolate MOSFET from other devices in VLSI circuits.



The drain-source current is controlled by the gate voltage applied to the gate electrode. No current flows from drain to source if there is no conducting n-channel between them. When no voltage is applied to the gate, it looks as if there are two back to back p-n junction diodes connected. MOSFET is considered in OFF state when no charge is applied to the gate and no channel is formed. When a positive voltage is applied at the gate relative to the substrate, positive charges are formed and are deposited on the gate metal. This voltage repels the holes from the Si-SiO<sub>2</sub> interface. Similarly negative charges are induced in the Si substrate, by the formation of depletion region and thin surface region containing mobile electrons. These electrons form the channel of the field-effect-transistor, and allow current to flow from drain to source. MOSFET is considered in ON state when the channel is formed between drain and source. The conductance of this channel can be modulated by varying the gate voltage ( $V_G$ ). The critical or the minimum gate voltage, at which thin layer of region of electrons is formed near the interface is called threshold voltage ( $V_T$ ) [9].

The MOSFET is a gate controlled device, should have low leakage p-n junctions and high quality to ensure better operation. Similarly for a p-channel MOSFET, positive charges are induced in the Si substrate by applying a negative voltage on to the gate metal. These holes form the channel of the field-effect-transistor, and allow current to flow from drain to source. Both n-channel and p-channel MOS transistors are used in many applications. However, n-channel MOS transistors are preferred because of the electron mobility in silicon substrates is more than mobility of holes in p-channel MOS transistors.

### 2.2.1 Importance of gate oxide

Moore's law suggests gate oxide thickness would be as low as 1.5nm in the year 2006. As the scaling of devices continues and need for high speed processors, SiO<sub>2</sub> simply does not have the dielectric constant,  $k$ , to withstand scaling till 2006. If the thickness is reduced, hot electrons are high energy electrons which can tunnel through the oxide layer and become excess charge in the oxide. This may lead to failure of the device with time. The effect of direct tunneling is shown in Figure 2.2 [11].

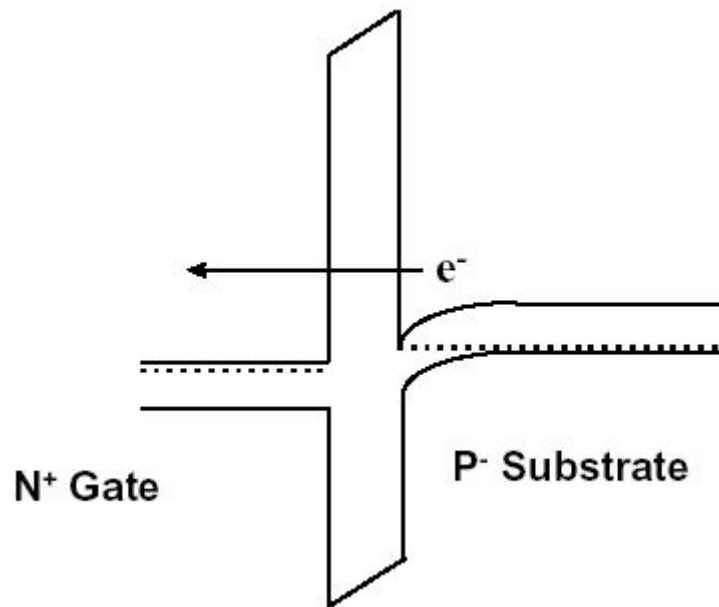


Figure 2.2 Direct tunneling effect.

The overall capacitance or oxide capacitance ( $C_{OX}$ ) behaves as a parallel plate capacitor whose plates are separated by gate oxide thickness ( $T_{OX}$ ). Current flow in MOS transistor is inversely proportional to the gate oxide thickness. Decreasing oxide thickness will also lead to electron tunneling and causing loss of voltage control in the gate [10]. The oxide capacitance is given by the following equation 2.1.

$$C_{OX} = \frac{\epsilon_0 \cdot k}{T_{OX}} \quad (\text{Equation 2.1})$$

where  $C_{OX}$  is the oxide capacitance,  $\epsilon_0$  is the relative permittivity of free space,  $k$  is the dielectric constant of the dielectric material used a gate oxide and  $T_{OX}$  is the oxide thickness. As we can see oxide thickness is a major factor in calculating oxide capacitance, reduce leakage current and in prevention of direct tunneling. So there is a lot of research going on to have high-k dielectric materials which will use thicker oxides without reducing the capacitance and transconductance of the transistor.

### 2.2.2 Equivalent oxide thickness

The gate oxide thickness determines the good control of the MOSFET depending upon the oxide capacitance of the given film. Equivalent-oxide-thickness (EOT) is defined as the thickness of  $\text{SiO}_2$  which can obtain same capacitance density as any other high k-dielectric oxide. Let us assume EOT to be the equivalent oxide thickness needed,  $\epsilon_{\text{SiO}_2}$  is the dielectric constant of  $\text{SiO}_2$ ,  $T_{\text{DES}}$  be the desired film thickness and  $\epsilon_{\text{HIGHK}}$  is the dielectric constant of high-k dielectric material to be used. They are all related by the following equation 2.2 and equation 2.3 [11].

$$\text{EOT} = \left( \frac{\epsilon_{\text{SiO}_2}}{\epsilon_{\text{HIGHK}}} \right) \cdot T_{\text{DES}} \quad (\text{Equation 2.2})$$

$$EOT = \left( \frac{3.9}{\epsilon_{\text{HIGHK}}} \right) \cdot T_{\text{DES}} \quad (\text{Equation 2.3})$$

The above equation shows oxide thickness more than that of SiO<sub>2</sub> would yield the same gate oxide capacitance and have the same command over MOSFET.

### 2.2.3 Effect of charges in MOSFETs

There are four type of charges associated with a MOS device. They are

- Interface trapped charges (Q<sub>IT</sub>)
- Fixed oxide charges (Q<sub>F</sub>)
- Oxide trapped charges (Q<sub>OT</sub>)
- Mobile oxide charges (Q<sub>M</sub>)

Interface trapped charges are positive or negative charges which arise due to structural defects, oxidation induced effects, metal impurities, or through bond-breaking process. These charges are located at Si-SiO<sub>2</sub> interface. Interface trapped charges can be reduced by following proper cleaning procedures and be neutralized by low temperature anneals.

Fixed oxide charges occurs during oxidation where Si is removed from the surface and reacts with oxygen. Some ionic Si is left near the interface during oxidation is stopped, during which these ions combine with uncompleted Si bonds results in positive charge near the interface.

Oxide trapped charges occurs during contamination of the oxide with Na which forms an oxide and due to imperfections in the oxide SiO<sub>2</sub>.

Mobile oxide charges occur when sodium ions introduce positive charges in the oxide. This charge is mainly contributed by ionic impurities such as  $\text{Na}^+$ ,  $\text{Li}^+$ ,  $\text{K}^+$  and  $\text{H}^+$ . Negative ions and heavy metals contribute to these charges [9, 10].

The effect of interface charges should be reduced to a minimum. The interface charges are more in 111 surfaces rather than in 100 surfaces. This is the reason why MOSFETs are made on 100 Silicon.

### 2.3 Threshold Voltage

Threshold voltage is the important parameter which determines the gate voltage required to induce the conducting channel for the operation of the MOS device. The threshold voltage [9] for p-MOSFETs is given by equation 2.4.

$$V_T = \phi_{ms} - \frac{Q_i}{C_{ox}} - \frac{Q_d}{C_{ox}} - 2 \cdot \phi_F \quad (\text{Equation 2.4})$$

The threshold voltage for n-MOSFET is given by equation 2.5.

$$V_T = \phi_{ms} - \frac{Q_i}{C_{ox}} + \frac{Q_d}{C_{ox}} + 2 \cdot \phi_F \quad (\text{Equation 2.5})$$

Where  $V_T$  is the threshold voltage of the device,  $\Phi_{MS}$  is the metal-semiconductor work function,  $Q_i$  is the interface trap charge between the substrate-oxide interface,  $C_{OX}$  is the oxide capacitance of the dielectric material which is sandwiched between metal and substrate,  $Q_D$  is the depletion charge in MOS devices and  $\Phi_F$  is the Fermi potential of the substrate and depends upon the doping of the substrate.

The threshold voltage is controlled by the gate oxide thickness and doping concentration of the substrate. The threshold voltage remains negative for p-channel MOSFETs and for n-channel MOSFETs it may remain positive or negative some times.

The threshold voltage increases with increase in  $N_A$  or  $N_D$  which is a factor in  $Q_D$  and  $\Phi_F$  term. The interface charge  $Q_I$  should be kept to a minimum to have low threshold voltages. Similarly, materials having high dielectric constant value increase the oxide capacitance ( $C_{OX}$ ) which in turn minimizes the threshold voltage ( $V_T$ ). The threshold voltage should be around -1 to 1 volt for n-channel MOSFETs and 0 to -1 volt for p-channel MOSFETs.

### 2.3.1 Threshold Voltage Adjustment

The threshold voltage can be controlled by ion implantation [9]. Precise quantities of boron impurities are added to the p-channel MOSFETs to reduce the donor ions in the n-substrate. This is done to reduce the depletion charge  $Q_D$  and to make threshold voltage less negative. Similarly, the boron implant is made shallow in a p-substrate of an n-channel MOSFETs to make threshold voltage less positive. The relationship between shift in threshold voltage  $\Delta V_T$  and implanted dose  $Q_{IM}$  is given by the following equation 2.6 [10].

$$\Delta V_T = \frac{q \cdot Q_{IM}}{C_{OX}} \quad (\text{Equation 2.6})$$

Where  $C_{OX}$  is the oxide capacitance and  $q$  is the electronic charge of an electron. This kind of adjustment is usually done in industries having large scale production of MOS devices. These are the reasons having thicker oxide thickness with high dielectric constant and withstand direct tunneling.

## CHAPTER THREE: STUDY OF DIFFERENT OXIDES AND METALS

High-k materials are being used to replace silicon dioxide in near future. The high-k materials which are focused in this work are hafnium oxide ( $\text{HfO}_2$ ), aluminum oxide ( $\text{Al}_2\text{O}_3$ ), tantalum pent oxide ( $\text{Ta}_2\text{O}_5$ ) and zirconium oxide ( $\text{ZrO}_2$ ). These materials were chosen because of their relevant structural and special properties. The dielectric constants of these materials vary from 9 to 25. The high k layers should be thick enough to prevent direct tunneling between the gate and silicon substrate. The gate metals discussed are aluminum, ruthenium and Pt-Ru alloy. The increase in film thickness can reduce tunneling leakage current and improve reliability while scaling capacitance equivalent oxide thickness below the direct tunneling limit [13].

### 3.1 Hafnium oxide

Hafnium oxide is a high-k dielectric material whose average dielectric constant is around 22 – 25 [13, 14]. It has high dielectric constant compared to  $\text{Al}_2\text{O}_3$  and  $\text{ZrO}_2$  dielectric films. It is thermally stable over silicon substrate and has a high band energy band gap around 5.8 eV.  $\text{HfO}_2$  has around 271 kCal/mol as high heat of formation with silicon [13, 15]. They are also used in nano scaled CMOS and memory devices such as DRAM cells [16]. Hafnium oxide has higher electrical permittivity and improves the gate dielectric layer with their properties. They are used for low power applications and have uniform thickness over the substrate. The effects of direct tunneling and TDDB are reduced by  $\text{HfO}_2$  as gate oxide. The leakage current of  $\text{HfO}_2$  should be lower than the same equivalent oxide thickness of  $\text{SiO}_2$  film. Because of the large barrier in  $\text{HfO}_2$  holes (3.4eV) as to electrons (1.5eV), the injection of holes is much smaller than the injection of electrons for  $\text{HfO}_2$  film. The hafnium oxide should be able to withstand dynamic stress in a long

term for MOS devices so that the time for breakdown increases and has less interface traps formed [17].

### **3.1.1 Deposition techniques of HfO<sub>2</sub>**

The hafnium oxide can be deposited by different methods. The dielectric constant of hafnium oxide differs for different depositions. The most challenging for any dielectric film would be to try avoiding formation of interface layer during processing or deposition at high temperatures over silicon substrate. There are different deposition techniques to reduce the interface layer to get good oxide capacitance and have dielectric constant of the high-k materials used. The interface layer which forms with hafnium oxide over silicon substrate is hafnium silicate and silicon dioxide most of the times. The different methods to form hafnium oxide are using metal-organic-chemical-vapor-deposition (MOCVD), rapid-thermal-chemical-vapor-deposition (RTCVD), sputtering, jet-vapor-deposition (JVD), dc magnetron sputtering, two-step reactive dc magnetron sputtering and reactive sputtering [13, 14, 18-21]. These deposition techniques need very precise equipment which is costly. The dielectric constants by these depositions for hafnium oxide are listed in table 2.



Table 2 Different deposition methods of HfO<sub>2</sub> with their dielectric constants.

Deposition Techniques	Dielectric constant values (k)
<b>MOCVD</b>	<b>26</b>
<b>RTCVD</b>	<b>24</b>
<b>JVD</b>	<b>25</b>
<b>DC Magnetron sputtering</b>	<b>22</b>
<b>Two step reactive DC magnetron sputtering</b>	<b>18</b>
<b>Reactive sputtering</b>	<b>22</b>

The metal-organic-chemical-vapor-deposition is mostly used for deposition because; the interface layer formation is very less compared to others as studied by C.Hobbs et.al [21]. The hafnium oxide is much stable over the silicon substrate using this technique. The leakage current decreases as there is an increase in annealing temperature as studied by N.Zhan et.al [19]. The breakdown voltage is also high using this deposition technique.

DC magnetron sputtering and two step reactive dc magnetron sputtering give dielectric constant of 22 and 18 respectively. But, there are lot of drawbacks such as there is formation of a

hafnium silicate interfacial layer and has high interface trap density. The interface trap density degrades the mobility of carriers which affects the threshold voltage ( $V_T$ ) delaying the formation of conducting channel. The hafnium silicate would cause decrease in overall dielectric constant of hafnium oxide and decrease in the oxide capacitance ( $C_{OX}$ ) [19, 21]. The interfacial layer should be minimal to have good reliability and interface properties.

The defects in semiconductor devices may be due to lattice mismatch. If the interface layer is thick enough, then silicon atom content increases number of charge traps. The oxide deposited should be amorphous in nature and not to be crystalline because crystalline structure material does not have uniform deposition of film over the substrate.

The breakdown voltage increases with decreasing oxide thickness. The break down field of  $HfO_2$  based film is 8.5 MV/cm for 45Å to 80Å films as studied by L.Kang et.al [13].

Aluminum is deposited as gate metal over the hafnium oxide to act as hafnium oxide based MOSFET. The  $HfO_2 / Si$  barrier height is between 1.13+/- 0.13 eV and Al/ $HfO_2$  is around 1.28 eV as studied in W.J.Zhu et.al [22]. The band diagram of  $HfO_2$  with Al gate is show in Fig 3.1.

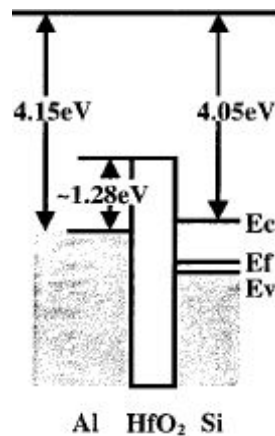


Figure 3.1 Band diagram of  $HfO_2$  with Al gate

## 3.2 Aluminum oxide

Aluminum oxide ( $\text{Al}_2\text{O}_3$ ) is also a candidate to replace the existing silicon dioxide because of its order to reduce leakage current, high thermal stability, large band gap and large band offset with silicon. Aluminum oxide dielectric constant varies from 8-11 [23]. The band gap of aluminum oxide is around 8.7 -9 eV. The presence of any defect in a dielectric material would be critical to cause dielectric to break down at low electric fields. The increase in dielectric constant would increase the gate oxide capacitance with less leakage or tunneling current. Aluminum oxide based MOSFETs are used in storage cells and in DRAM capacitors. One of the important property of aluminum oxide is it remains amorphous even at high temperatures. The aluminum oxide is used in flash memory circuits because of its high dielectric constant. This increases the capacitive coupling which in turn increases the circuit speed [26]. The properties of aluminum oxide allow them to be used in silicon microelectronics, insulator in thin film industries, ionic barrier and as protective coating [24].

### 3.2.1 Deposition techniques of $\text{Al}_2\text{O}_3$

Similar to hafnium oxide, aluminum oxide can also be deposited by different methods. The dielectric constant also varies with different methods. The effective method of deposition is to get an aluminum oxide layer deposited on silicon substrate with no interfacial layer and less interface trap charges. The methods to deposit aluminum oxide are rf magnetron sputtering, metal-organic-chemical-vapor-deposition (MOCVD), plasma-enhanced-chemical-vapor-deposition (PECVD), ultra-high-vacuum-reactive-atomic-beam-deposition (UHVBE), low-

temperature-atomic-layer-deposition (ALD) and through atomic plasma [25-29]. The varying dielectric constants using different deposition methods are shown in Table 3.

Table 3 Different deposition methods of Al<sub>2</sub>O<sub>3</sub> with their dielectric constants.

Deposition methods	Dielectric constant (k)
<b>RF magnetron power sputtering</b>	<b>9</b>
<b>MOCVD</b>	<b>8.1</b>
<b>PECVD</b>	<b>10</b>
<b>UHVBE</b>	<b>10</b>
<b>Low temperature ALD</b>	<b>9</b>
<b>Atomic plasma anodization</b>	<b>7.6</b>

For aluminum oxide, MOCVD is a good method to deposit. The dielectric constant of the film is around 8.1. The interfacial layer formation is very less compared to other deposition methods. MOCVD gives one of the best methods to deposit aluminum oxide because of its precise composition, uniform distribution and gives high quality films as studied by Q.Y. Shao

et.al. The precursor used is also aluminum acetylacetonate which is non-toxic, amorphous and easy to handle in room temperatures [26].

RF magnetron sputtering gives high dielectric constant of 9. They were deposited by sputtering using Al as a metal target as studied by J.Kolodozey et.al [25]. The interfacial layer is very less compared to atomic plasma anodization and atomic layer deposition methods. The oxide trapped charge  $Q_{OX}$  is around  $10^{11} \text{cm}^{-2}$  as studied by J.Kolodozey et.al which is low and good for aluminum oxide based MOSFETs. The dielectric breakdown by this mechanism is around 4.5- 9 MV/cm.

Ultra-high-vacuum-reactive-atomic-beam-deposition (UHVBE) is also a method to deposit aluminum oxide. This method does not form interfacial layer with substrate. Aluminum oxide is deposited in a molecular beam epitaxy chamber with effusion source for aluminum and rf discharge source for oxygen as studied by S.Guha et.al. The interface state density is around  $10^{-10} \text{eV}^{-1} \text{cm}^{-2}$  [28]. This method is good, but the cost of this equipment and maintenance costs are high. These methods are used by industries and foundries.

Another method to deposit aluminum oxide is by atomic-layer-deposition (ALD). The dielectric constant from this method is around 9. Since this method is done at low temperatures, this method cannot be used for making precise applications. It is also difficult to pattern and etch because of damaging the device. Even though the film is deposited at low temperatures and increase in deposition time, the films are uniform as studied by M.J.Biercuk et.al. The gate dielectric materials are always amorphous because of smoothness of material and high break down fields. The breakdown fields are around 6 – 9 MV/cm [27].

Another method to deposit aluminum oxide is by atomic plasma anodization. The oxide film was formed by depositing aluminum on silicon substrate and anodizing the aluminum in

oxygen plasma as studied by A. Waxman et.al. The interfacial layer formation is less than 50Å which affects the gate oxide capacitance of MOSFET and decrease the dielectric constant of aluminum oxide to be around 7.6 [29]. Due to very low dielectric constant this method is not a good method to deposit aluminum oxide.

The energy band diagram of Al<sub>2</sub>O<sub>3</sub> with any metal gate is shown in Figure 3.2 [15].

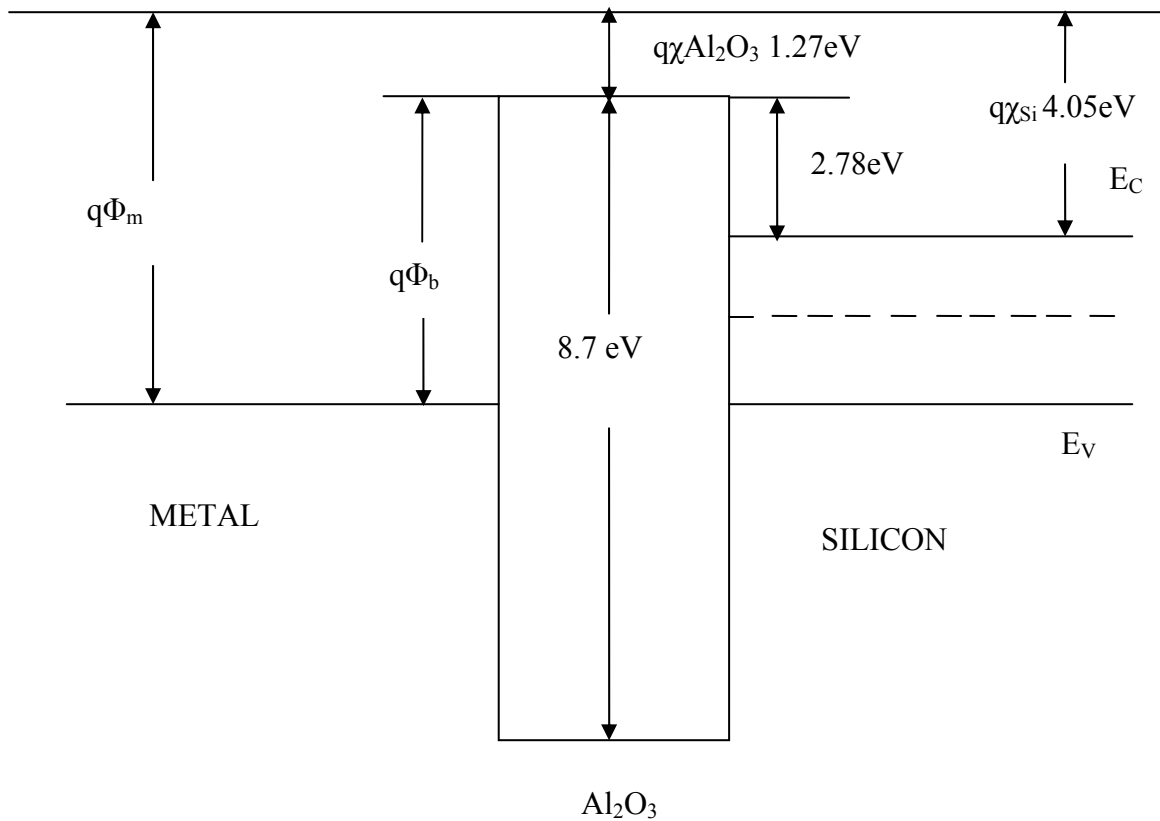


Figure 3.2 Band diagram of Al<sub>2</sub>O<sub>3</sub> using any metal gate

### 3.3 Tantalum oxide

Tantalum oxide is another high-k dielectric material that can replace SiO<sub>2</sub>. The dielectric constant of Ta<sub>2</sub>O<sub>5</sub> is around 25-35. Tantalum oxide has low leakage current of around 10<sup>-8</sup>A/cm<sup>2</sup> and has high break down strength of 7-9 MV/cm. Tantalum oxide is used in many semiconductor devices such as capacitor dielectric of DRAM, thin film transistor, lightly doped drain spacer and ion-sensitive field effect transistor (ISFET) [15]. The energy band gap of tantalum oxide is 4.2 eV. The properties of the dielectric film are based on dielectric constant, oxide charge, interface charge, leakage current density and mostly breakdown strength. Tantalum oxide is compatible in the manufacturing of integrate circuits [35]. As tantalum oxide has high dielectric constant, the more charge we can store. So it is used in Giga bit DRAMs.

#### 3.3.1 Deposition techniques of Ta<sub>2</sub>O<sub>5</sub>

The tantalum oxide can be deposited by different methods. Here also the dielectric constant varies with different deposition methods. The best way of deposition is to have no interfacial layer and less interface trap charges. The quality of film deposited should be good, with low defects and uniform. The methods of depositing tantalum oxide are chemical-vapor-deposition (CVD), rf sputtering, reactive sputtering, metal-organic-chemical-vapor-deposition (MOCVD) and rf sputtering with hydrogen annealing [30-34]. The different deposition methods and their dielectric constants are shown in table 4.

Table 4 Different deposition methods of Ta<sub>2</sub>O<sub>5</sub> with their dielectric constants.

Deposition methods	Dielectric constant (k)
<b>CVD</b>	<b>25</b>
<b>PECVD</b>	<b>27</b>
<b>RF Sputtering</b>	<b>32-35</b>
<b>Reactive Sputtering</b>	<b>25-30</b>
<b>MOCVD</b>	<b>23</b>
<b>RF Sputtering + hydrogen anneal</b>	<b>28-35</b>

Tantalum oxide can be deposited by chemical-vapor-deposition (CVD). This process after post deposition annealing with high temperature can reduce the leakage current of the film, but it will also affect electrical and physical properties of the film. The film may turn from amorphous to crystalline which would result in decrease in oxide thickness which would cause high leakage current. The dielectric constant by this method is around 25. When doing high temperature annealing using O<sub>2</sub>, the oxygen atoms may diffuse into Ta<sub>2</sub>O<sub>5</sub> film and may also even react with the silicon substrate to form interfacial layer as studied by J.S.Lee et.al [30].

As compared to CVD process metal-organic-chemical-vapor-deposition (MOCVD) is used to deposit tantalum oxide to prevent trap generation which results in degradation of films. The dielectric constant by this method is around 23. The substrates were post annealed in oxygen to reduce interface trap density and reduce the leakage current of the film. The low temperature annealing is usually done in MOCVD for Ta<sub>2</sub>O<sub>5</sub> to prevent the film from crystallization. The



crystallization would result in decrease of dielectric thickness which may result in high leakage current. A layer of oxy nitride is formed as the interfacial layer. Electrons are trapped in this process for the dielectric film which can result in bond relaxation and bond breaking which may result in degradation of Ta<sub>2</sub>O<sub>5</sub> layer as studied by M. Houssa et.al [31].

RF sputtering is also used to deposit tantalum oxide. This uses a tantalum target in an argon atmosphere and was oxidized at low temperature. The temperature is maintained at low because to prevent formation of tantalum silicides. The oxide charge is around  $5 \cdot 10^{11} \text{ cm}^{-2} - 10^{12} \text{ cm}^{-2}$  because of interfacial layer SiO<sub>2</sub> formation. The interfacial layer formation decreases the dielectric constant of tantalum oxide and decreases the gate oxide capacitance. The dielectric constant by this method is found to be around 32-35 as studied by E. Atanassova et.al [32].

Tantalum oxide could be deposited by reactive sputtering of tantalum target in a mixture of argon and oxygen gases. The film deposition form is crystalline using this method. The dielectric constant is around 37. Even though the dielectric constant is high, silicon dioxide is formed as interfacial layer. This interfacial layer forms because of the interfacial defects and dangling bonds on to the SiO<sub>2</sub>. The leakage current is around  $10^{-7} \text{ A/cm}^2$  by this method. The film is crystalline near the Si-Ta<sub>2</sub>O<sub>5</sub> interface as studied by A. Paskaleva et.al [33].

The other method to deposit tantalum oxide is RF sputtering followed by an hydrogen anneal. The targets discussed are the same as discussed in RF sputtering. Hydrogen anneals decreases the fixed oxide charge. Even though this method gives a dielectric constant of 37, the interfacial layer formation of SiO<sub>2</sub> cannot be minimized. The interfacial layer has less Ta-O bonds. The hydrogen annealing also helps in the improvement of properties of tantalum oxide. The leakage current is around  $10^{-8} \text{ A/cm}^2$ . The disadvantage of this method is the double layer

structure formation of the dielectric film and interfacial layer which decreases the oxide capacitance as studied by D. Spassov et.al [34].

The gate electrode materials used in my study are aluminum, ruthenium and Ru-Ta alloys. The aluminum can be deposited by evaporation. The energy band diagram of tantalum oxide with any metal is shown in Figure 3.3 [15].

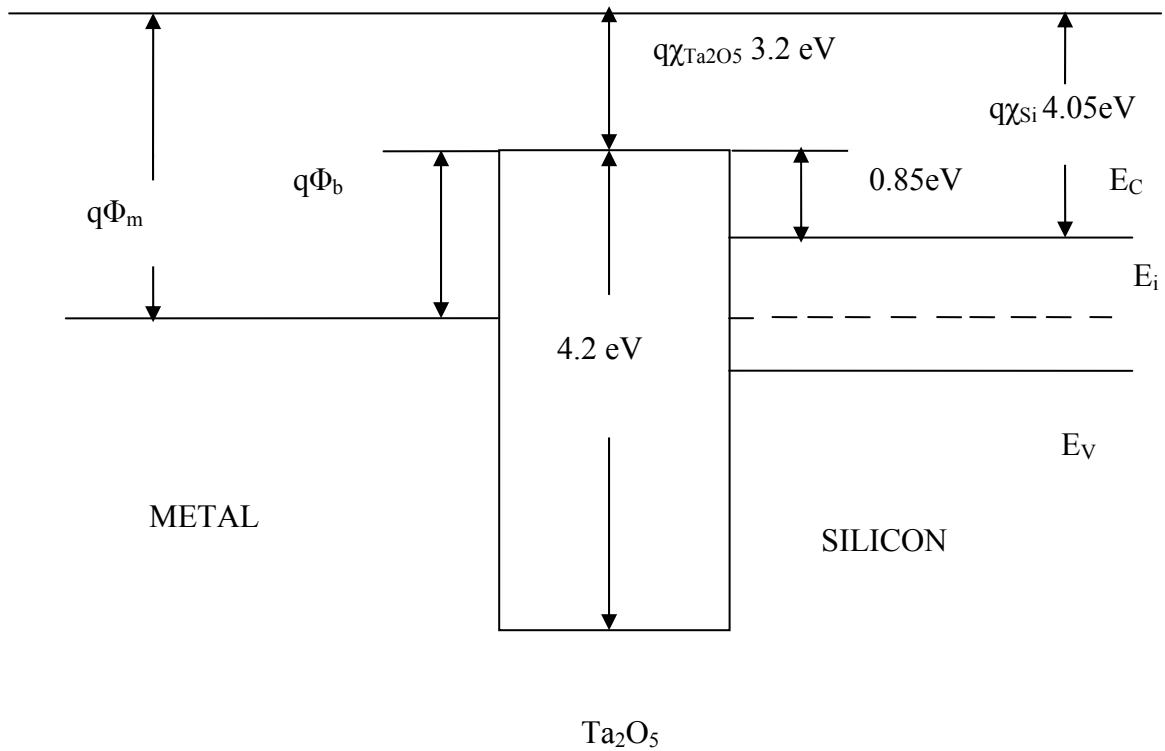


Figure 3.3 Band diagram of Ta<sub>2</sub>O<sub>5</sub> with any metal gate

### **3.4 Zirconium Oxide**

Another material which is of our interest is zirconium oxide which too can replace the existing silicon dioxide as gate oxide. This has dielectric constant of around 15-25. Zirconium oxide has band gap between 5.16 eV – 7.8 eV [15]. Zirconium oxide is more thermodynamically stable over silicon substrate and has breakdown strength of around 15-20 MV/cm. It has very good insulation to prevent high leakage currents and also the attractive characteristic of high-k materials for use of gate oxide. This also has smooth uniformity of thin film deposition which is required in manufacturing devices for stability and reliability. Zirconium oxide has low interface trapped density and low leakage current compared to other high-k dielectric materials discussed above.

#### **3.4.1 Deposition techniques of $ZrO_2$**

Zirconium oxide can be deposited by different methods and dielectric constants too vary with different methods. The deposited thin film should be amorphous rather than crystalline in nature. The film should have low leakage current and high oxide capacitance ( $C_{OX}$ ). The deposition technique should provide film to be chemically, physically stable and be free of any interfacial layer between film and silicon substrate. Zirconium oxide can be deposited by high-vacuum-electron-beam-evaporation (HVEBE), sputtering, atomic-layer-chemical-vapor-deposition (ALD) and sputter deposition methods [35-38]. The deposition methods and their corresponding dielectric constants are shown in Table 5.

Table 5 Different deposition methods of ZrO<sub>2</sub> with their dielectric constants.

Deposition methods	Dielectric constant (K)
<b>HVEBE</b>	<b>18-30</b>
<b>Sputtering</b>	<b>18</b>
<b>ALCVD</b>	<b>15-18</b>
<b>DC sputtering + Post deposition annealing</b>	<b>20</b>

One of the best methods to deposit zirconium oxide is by high-vacuum-electron-beam-evaporation (HVEBE). This method is done at room temperature using quadruple mass spectrometer in situ. ZrO<sub>2</sub> is used as the target. This is also done at very low pressure to improve the mean free path and to be free of any impurities. By this method there is no interfacial layer formation between ZrO<sub>2</sub> and substrate. Zirconium oxide is also stable on direct contact with silicon. The thin films deposited by this method are amorphous, which in fact is really good for low leakage current and better conformity. The dielectric film should not be crystalline because it may form non-uniform device electrical characteristics. This method of depositing ZrO<sub>2</sub> is studied by Ninglin Zhang et.al [35].

Another method to deposit zirconium oxide is by atomic-layer-chemical-vapor-deposition (ALCVD). Zirconium t-butoxide and oxygen were used to deposit zirconium oxide on to Si substrate. This method is done at a low pressure and around 350 -450°C. The precursors are

atomically controlled to form uniform deposition on to the substrate. The film deposited by this method is amorphous. This method forms an interfacial layer between  $ZrO_2$  and silicon substrate forming zirconium silicate. This interfacial layer decreases the over all dielectric constant and simultaneously gate oxide capacitance ( $C_{OX}$ ). Aluminum as gate electrode is deposited by physical vapor deposition (PVD) over the zirconium oxide layer to form Al/ $ZrO_2$ /Si based MOSFETs. The dielectric constant of  $ZrO_2$  is around 18. The MOSFETs made by this method have low leakage current and low interface state density around  $2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  as studied by J.P.Chang et.al [36].

Another method to reduce the diffusion of oxygen and other impurities during zirconium oxide deposition is by DC sputtering using zirconium target in argon ambient at low pressure and room temperature. Nitrogen doped  $ZrO_2$  has good thermal stability and chemical stability. Post deposition anneal (PDA) is done to oxidize and to make  $ZrO_2$  dense. This process uses nitrogen ambient with traces of oxygen. There is lot of oxide trapped charge ( $Q_{OT}$ ) near the oxide-silicon interface. The increase in the charge is because of nitrated surface formation between silicon and zirconium oxide. The interfacial layer is also thick compared to other methods. This decreases the dielectric constant to around 20 and oxide capacitance of the high-k dielectric film as studied by R. Nieh et.al [37].

Zirconium oxide also can be deposited by sputtering zirconium target in a mixture of oxygen and argon at room temperature. Annealing is done on the substrates after deposition to reduce the leakage current. Aluminum can be deposited as the gate electrode by co sputtering using aluminum target. This method gives dielectric constant of zirconium oxide to be around 18. This method gives lower electron affinity and barriers for electrons and holes. There is lot of

charge trapping in the oxide surface. The charge trapping by sputtering is studied by Yanjun Ma et.al [38].

So the other method to deposit  $ZrO_2$  is by high vacuum electron beam evaporation.

The energy band diagram of  $ZrO_2$  with any metal as gate is shown in Figure 3.4 [15].

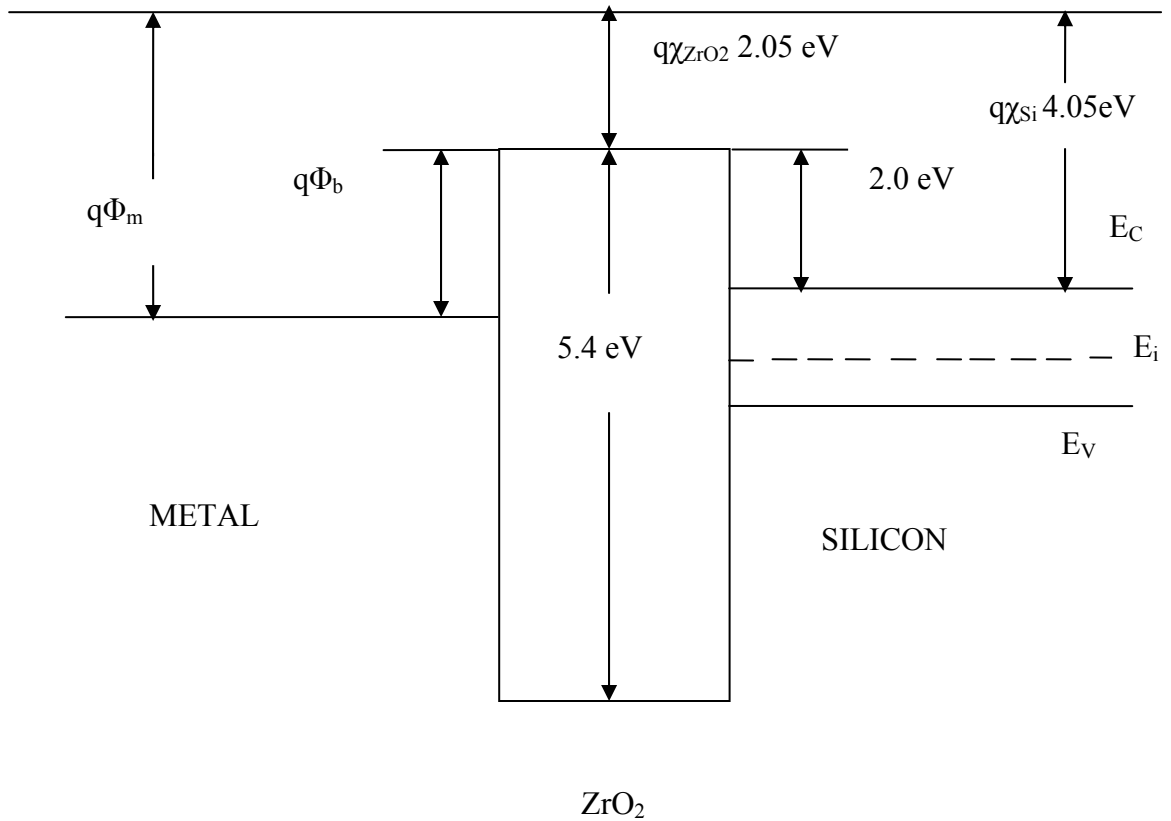


Figure 3.4 Band diagram of  $ZrO_2$  with any metal gate

### **3.5 Study of gate metals**

Gate metal is the important part of a MOSFET by which the voltage applied induces the conducting channel for the MOS device. The metal work function also plays a major role for the threshold voltage to increase and decrease. The metal-semiconductor ( $\Phi_{MS}$ ) work function is the difference between metal work function and semiconductor work function. The need for study of different metals and alloys is because poly-silicon which had been used as gate, cannot withstand very high temperatures during deposition of gate oxide and has good chance of reacting with the high-k dielectric material to form undesired interfacial layer. Poly-silicon has effect of intolerable parasitic capacitance and resistances beyond the scaling limit. The metals should be thermally stable during source to drain activation. We need to look for metals to improve this problem. The metals that are interested in the present work are aluminum, ruthenium and Pt-Ru alloys with work function 4.9eV and 5.2eV.

#### **3.5.1 Study of Aluminum metal**

Aluminum has been used widely for a long time as gate metal in MOSFETs because of its good conductivity. Aluminum can withstand high temperatures of deposition and has good interconnect reliability. Aluminum is also stable with most of the high-k oxides discussed above. The metal work function of aluminum used in the study is 4.2 eV. The deposition of aluminum can be achieved by simple method such as PVD.

### 3.5.2 Study of Ruthenium metal

Ruthenium can also be used as gate to improve the threshold voltage of MOSFETs as compared to using aluminum as gate metal. Ruthenium is one such metal whose work function lies in the mid-gap of the Figure 3.5 which shows the best work function of any gate metal to be used in MOSFETs.

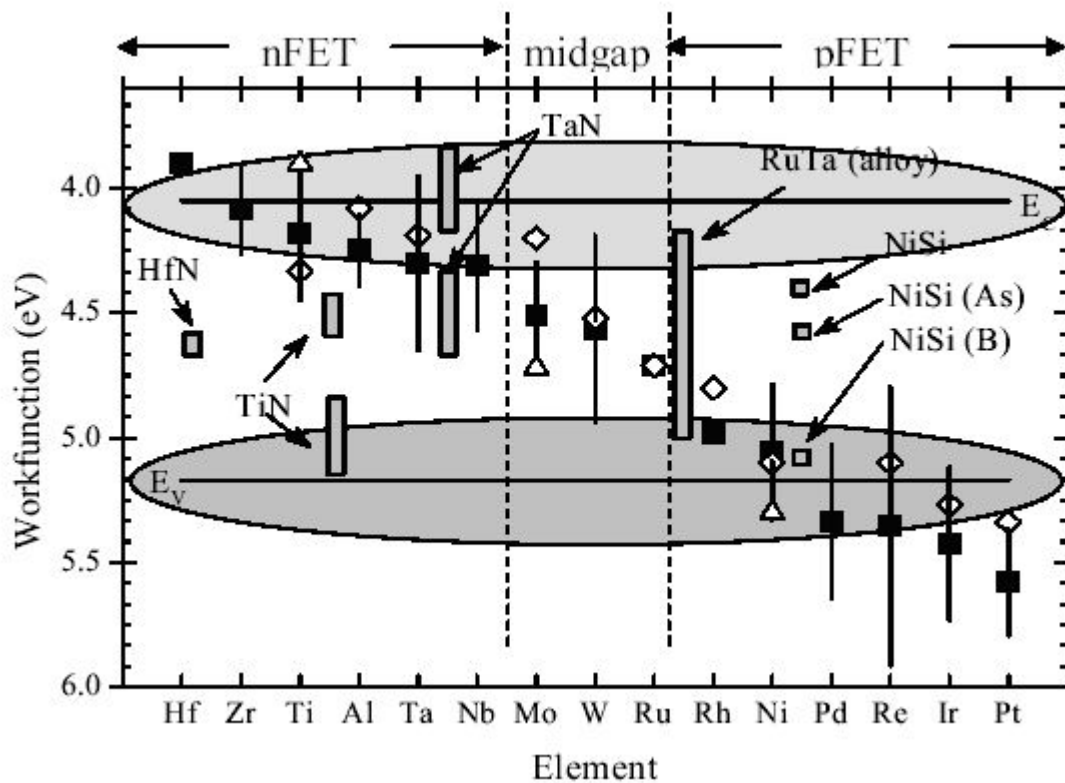


Figure 3.5 Work functions of possible metal gate applications

The metal work function of ruthenium used in this study is 4.71 eV. The deposition of ruthenium can be done by MOCVD and PEALD. The best method to deposit ruthenium is by plasma-enhanced-atomic-layer-deposition (PEALD).



### **3.5.3 Study of Pt-Ru alloy as gate metal**

A lot of research is going on to replace metals with alloys as gate in MOSFETs. Alloy of Pt-Ru can be used as gate metal. This study involves Pt-Ru alloy with two work functions

- 4.9eV (the work function is near to ruthenium work function)
- 5.2eV (the work function is near to platinum work function)

The two work functions are chosen in such a way to find out which gives the best threshold voltage values for MOSFETs.

## CHAPTER FOUR: RESULTS AND SIMULATIONS

The investigation involved in this study was to determine the variations in threshold voltage for both PMOS and NMOS devices, an important factor in MOSFETs. The materials which are selected in this study are high-k dielectric materials. The dielectric constant selected is the average of different dielectric constants obtained by using different deposition methods. The dielectric constants studied are listed below in Table 6 for the corresponding dielectric materials.

Table 6 Average dielectric constant of studied high-k materials

Dielectric materials	Dielectric constant (K)
<b>HfO<sub>2</sub></b> (Hafnium oxide)	<b>23</b>
<b>Al<sub>2</sub>O<sub>3</sub></b> (Aluminum oxide)	<b>10</b>
<b>Ta<sub>2</sub>O<sub>5</sub></b> (Tantalum oxide)	<b>25</b>
<b>ZrO<sub>2</sub></b> (Zirconium oxide)	<b>18</b>

The best deposition method for deposition of gate oxide having no interfacial layer is chosen for calculations. The choice of gate metal is determined by the work function as well as the ability to decrease threshold voltage in NMOS and increase the threshold voltage in PMOS field effect transistors. The work function should be fairly high but not too high to be used as gate electrode. The gate metals studied include Aluminum, Ruthenium, and Pt-Ru alloy with estimated work function of 4.9eV and 5.2eV respectively. The simulations are done by MATHCAD software.

## 4.1 MOSFETS with aluminum as gate metal

### 4.1.1 Al/HfO<sub>2</sub> based MOSFET

In the present work, the effect of interface trap charges, doping concentration, and oxide thickness on the  $V_T$  were studied. Several variations of the above physical parameters were used to calculate the  $V_T$  for NMOS and PMOS devices. In the first case, simulations were performed using aluminum as gate metal and hafnium oxide as gate oxide for PMOS and NMOS field effect transistors. Firstly the interface trap charge is kept at  $5 \times 10^{10}$  qC/cm<sup>2</sup>. The doping concentration ( $N_A, N_D$ ) is varied from  $5 \times 10^{14}$  cm<sup>-3</sup>,  $10^{15}$  cm<sup>-3</sup>,  $5 \times 10^{15}$  cm<sup>-3</sup>,  $10^{16}$  cm<sup>-3</sup>,  $5 \times 10^{16}$  cm<sup>-3</sup> and  $10^{17}$  cm<sup>-3</sup> respectively. The oxide thickness ( $T_{OX}$ ) is varied from 50Å, 100Å, 200Å, 400Å, 600Å, 800Å and 1000Å respectively. Next, the interface trap charge ( $Q_i$ ) is varied from  $10^{11}$  qC/cm<sup>2</sup>,  $5 \times 10^{11}$  qC/cm<sup>2</sup>,  $10^{12}$  qC/cm<sup>2</sup>,  $5 \times 10^{12}$  qC/cm<sup>2</sup> and  $10^{13}$  qC/cm<sup>2</sup>. The above  $V_T$  calculations were repeated for all doping concentrations and oxide thicknesses. The threshold voltages vs. oxide thickness for various doping concentrations at constant interface trap charge ( $Q_i = 5 \times 10^{10}$  qC/cm<sup>2</sup>) are plotted. While the oxide thickness is varied for a range of values, the values of interest are in the category of thin, medium and thick oxides. For this thicknesses selected are 100Å, 400Å and 800Å. The above process of simulation were repeated by changing the interface trap charge ( $Q_i$ ) from  $10^{11}$  qC/cm<sup>2</sup> to  $10^{13}$  qC/cm<sup>2</sup> which are plotted in Fig 4.1, 4.2, 4.3 and 4.4 respectively. The simulated results show that threshold voltage for NMOS devices are in the range of -0.11V to 0.59V with oxide thicknesses having 100Å, 400Å, 800Å for corresponding  $10^{15}$ cm<sup>-3</sup>,  $10^{16}$ cm<sup>-3</sup>,  $10^{17}$ cm<sup>-3</sup> doping concentrations. At  $10^{13}$  qC/cm<sup>2</sup> interface charge, the  $V_T$  was found to be high (-1.7V). At 800Å oxide thickness for PMOS devices at various doping concentrations for any

value of interface trap charges, the  $V_T$  is found to be high (-7.739V). The increase in interface trap charges increases the threshold voltage on the negative side.

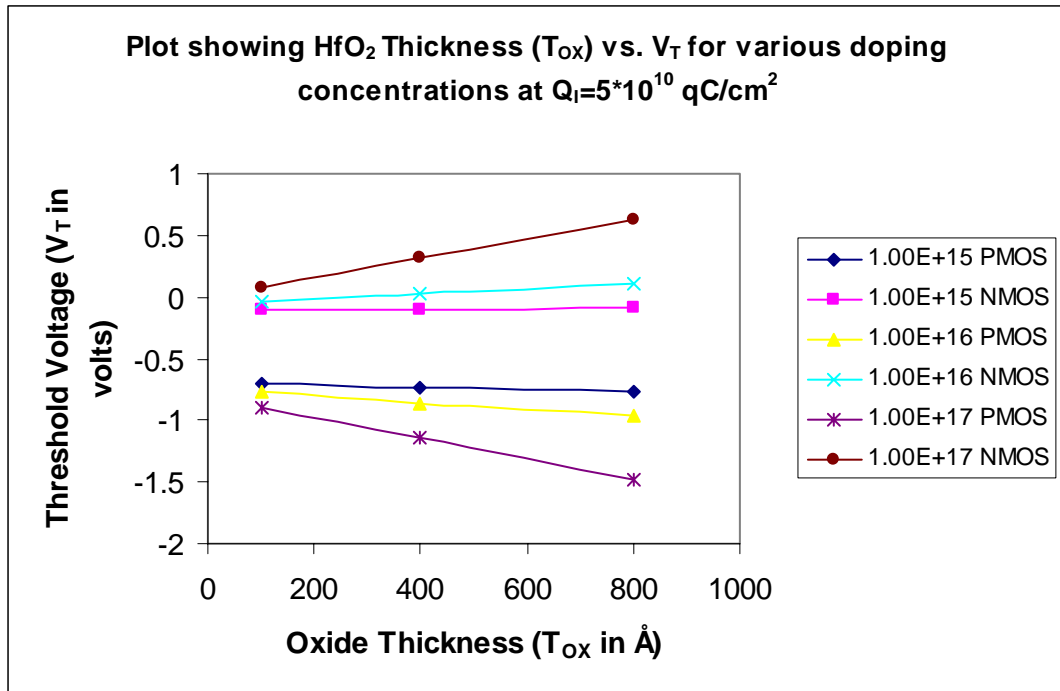


Figure 4.1 Plot showing  $V_T$  vs. HfO<sub>2</sub> Thickness for various  $N_A$ ,  $N_D$  at  $Q_i=5 \times 10^{10}$  qC/cm<sup>2</sup>

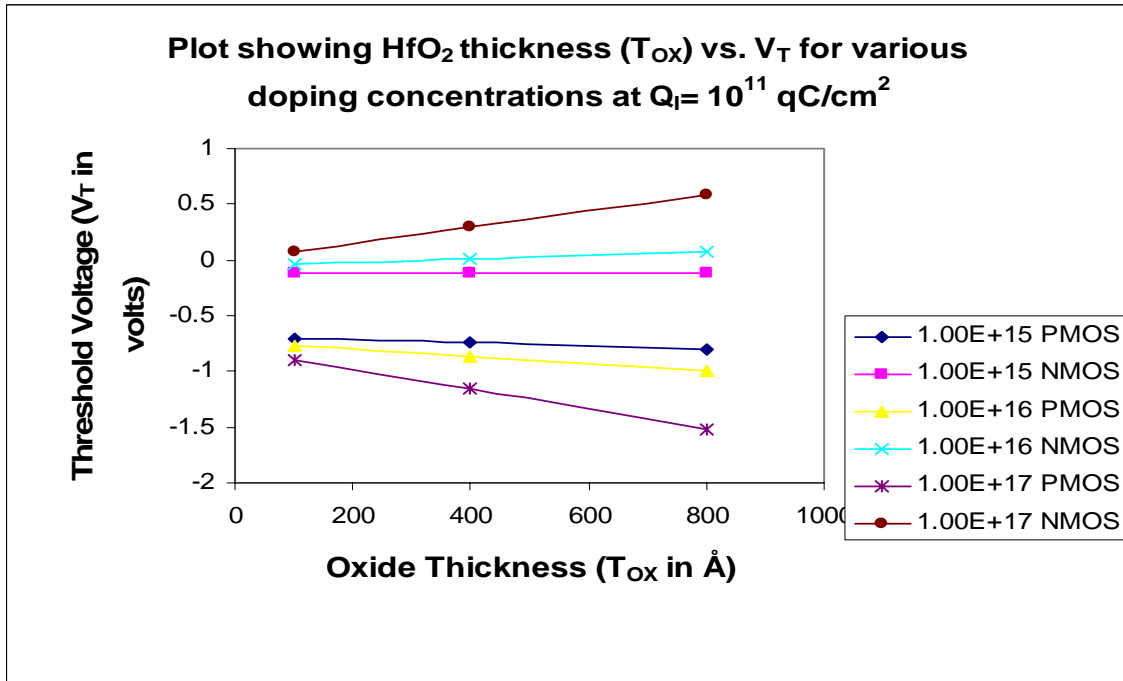


Figure 4.2 Plot showing V<sub>T</sub> vs. HfO<sub>2</sub> Thickness for various N<sub>A</sub>, N<sub>D</sub> at Q<sub>I</sub>=10<sup>11</sup> qC/cm<sup>2</sup>

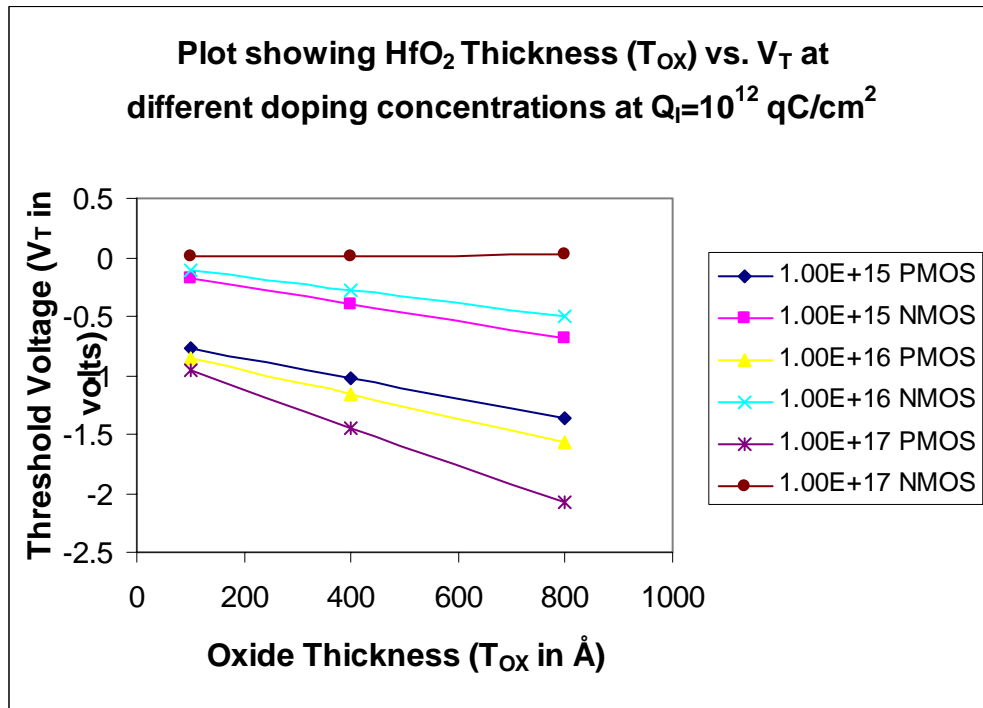


Figure 4.3 Plot showing V<sub>T</sub> vs. HfO<sub>2</sub> Thickness for various N<sub>A</sub>, N<sub>D</sub> at Q<sub>I</sub>=10<sup>12</sup> qC/cm<sup>2</sup>

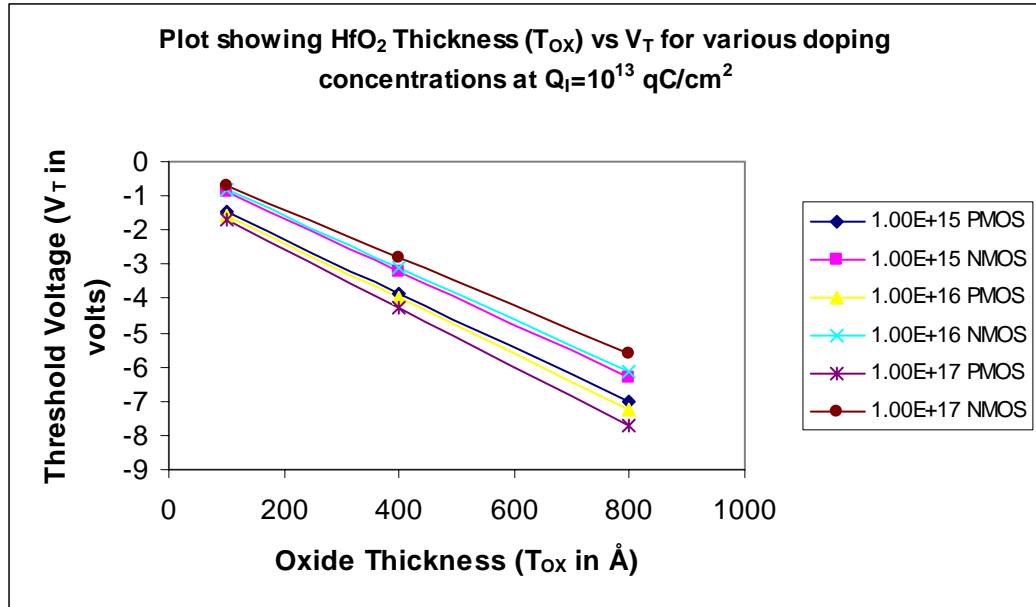


Figure 4.4 Plot showing  $V_T$  vs.  $\text{HfO}_2$  Thickness for various  $N_A$ ,  $N_D$  at  $Q_i=10^{13} \text{ qC/cm}^2$

For the Al/ $\text{HfO}_2$  system, the interface trap charge ( $Q_i$ ) is kept constant at  $5 \cdot 10^{10} \text{ qC/cm}^2$ . Now by varying oxide thickness (initially  $100\text{\AA}$ ,  $400\text{\AA}$  and  $800\text{\AA}$ ), the threshold voltage is calculated and plotted for various doping concentrations ( $N_A$ ,  $N_D$ ). The above process of simulation is repeated by varying the interface trap charges from  $10^{11} \text{ qC/cm}^2$  to  $10^{13} \text{ qC/cm}^2$  and are plotted in Fig 4.5, 4.6, 4.7 and 4.8 respectively. The oxide thickness with  $800\text{\AA}$  for PMOS devices shows threshold voltage very bad ( $-2.082\text{V}$ ) for several interface charges. At doping concentration of  $10^{17} \text{ cm}^{-3}$  with oxide thickness more than  $800\text{\AA}$ , the  $V_T$  values were found to be too high ( $-7.783\text{V}$  and  $-5.632\text{V}$ ) for both NMOS and PMOS devices having interface charges more than  $10^{12} \text{ qC/cm}^2$ . The interesting thing was that, at  $Q_i=10^{12} \text{ qC/cm}^2$  all oxide thicknesses have nearly same threshold voltage for NMOS devices.

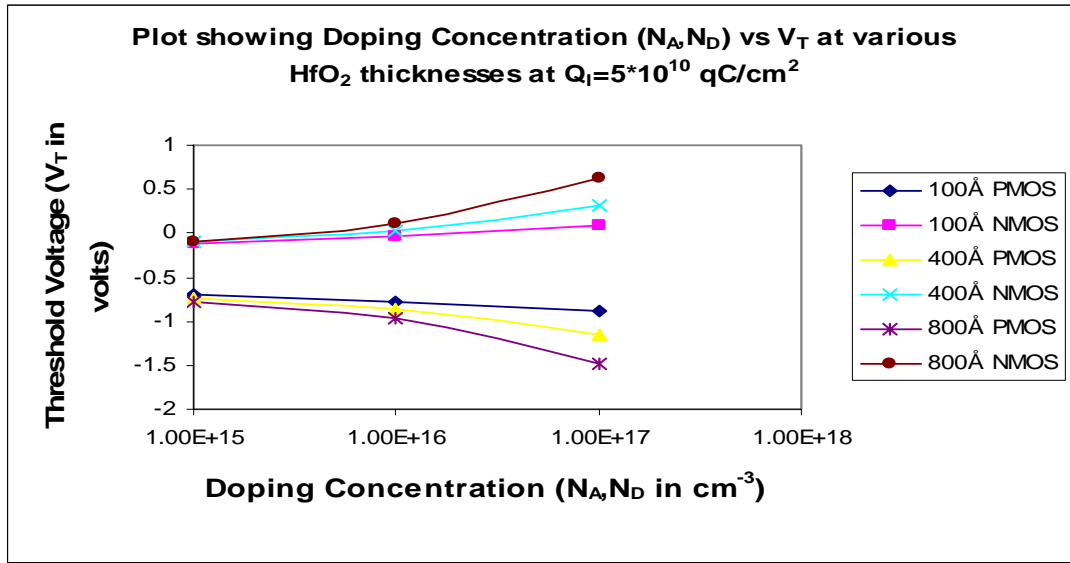


Figure 4.5 Plot showing Doping Concentration vs.  $V_T$  for various  $HfO_2$  thicknesses at  $Q_I=5 \cdot 10^{10} \text{ qC/cm}^2$

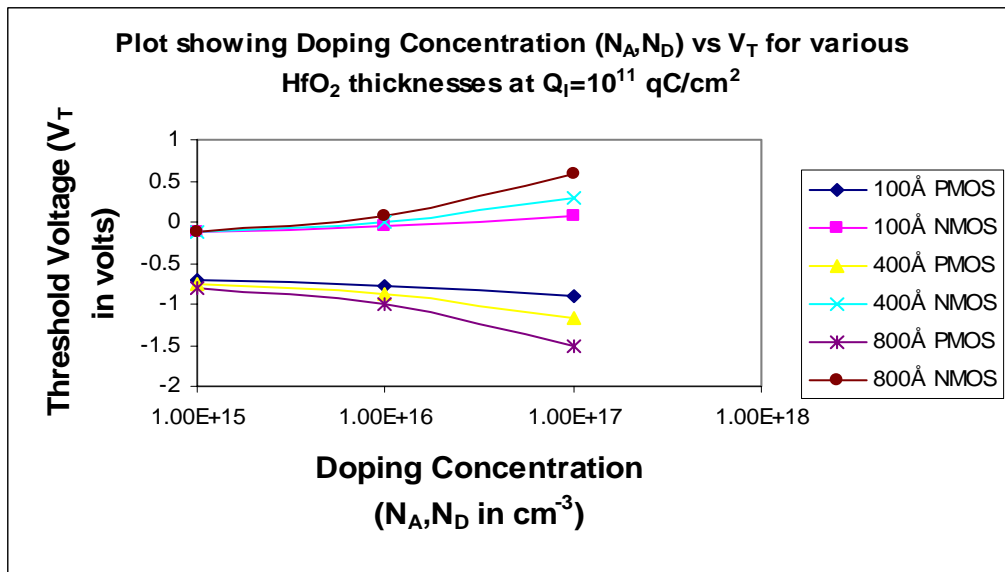


Figure 4.6 Plot showing Doping Concentration vs.  $V_T$  for various  $HfO_2$  thicknesses at  $Q_I=10^{11} \text{ qC/cm}^2$

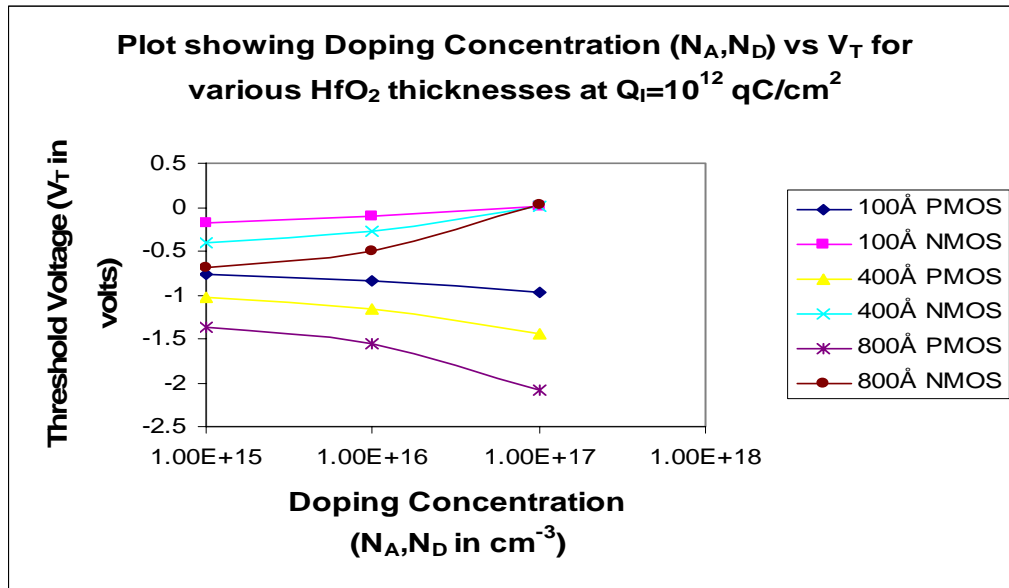


Figure 4.7 Plot showing Doping Concentration vs.  $V_T$  for various  $HfO_2$  thicknesses at  $Q_I=10^{12} \text{ qC/cm}^2$

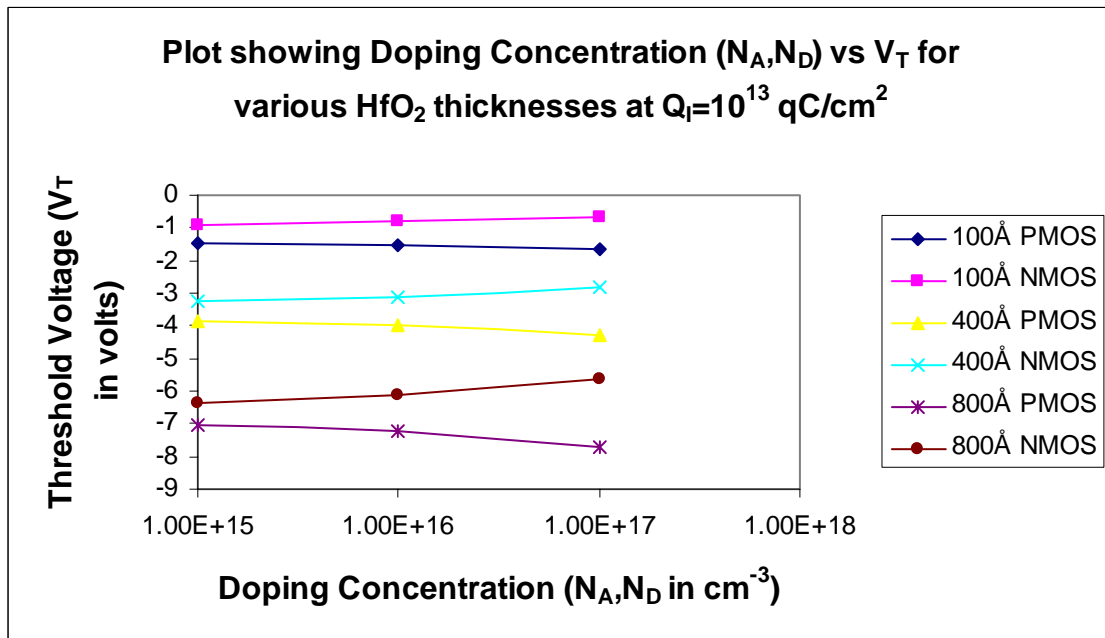


Figure 4.8 Plot showing Doping Concentration vs.  $V_T$  for various  $HfO_2$  thicknesses at  $Q_I=10^{13} \text{ qC/cm}^2$



For Al/HfO<sub>2</sub> system, now the doping concentration ( $N_A, N_D$ ) is held constant at  $10^{15} \text{ cm}^{-3}$ . Now by varying oxide thickness (initially 100Å, 400Å and 800Å), the threshold voltage is calculated and plotted against different values of interface trap charges ( $Q_I$ ) Fig 4.9. The above process of simulation is repeated by changing the doping concentrations to  $10^{16} \text{ cm}^{-3}$  and  $10^{17} \text{ cm}^{-3}$  are plotted in Fig 4.10 and 4.11 respectively. The threshold voltage values are too high (-3.984V and -3.149V) for PMOS and NMOS devices having more than 400Å thickness at  $Q_I=10^{13} \text{ qC/cm}^2$  and  $10^{15} \text{ cm}^{-3}$ ,  $10^{16} \text{ cm}^{-3}$  and  $10^{17} \text{ cm}^{-3}$  doping concentrations.

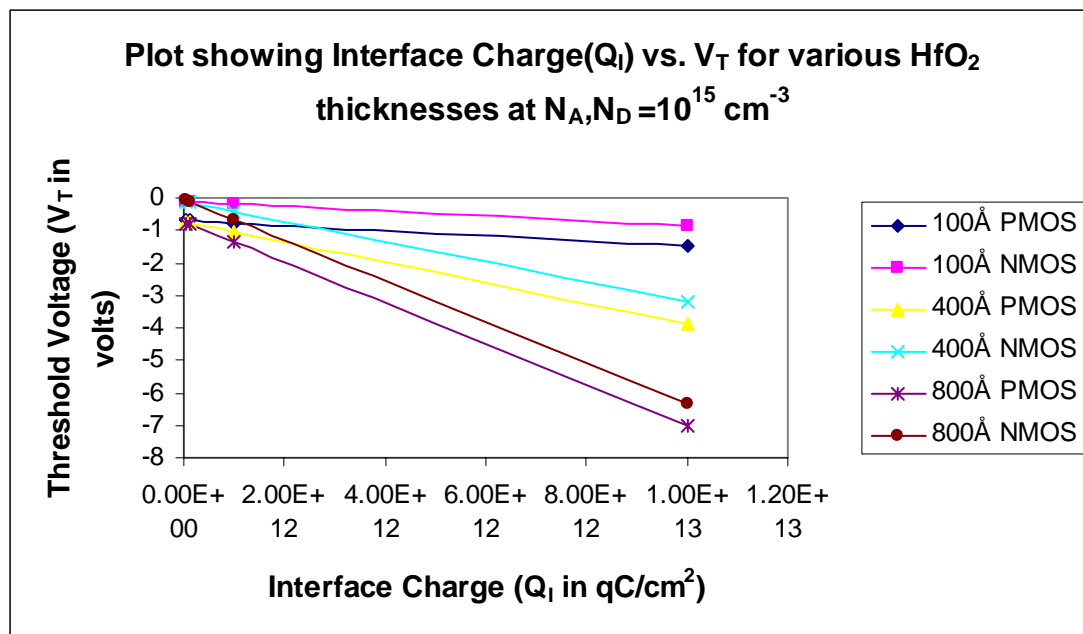


Figure 4.9 Plot showing  $V_T$  vs.  $Q_I$  for various HfO<sub>2</sub> thicknesses at  $N_A, N_D = 10^{15} \text{ cm}^{-3}$

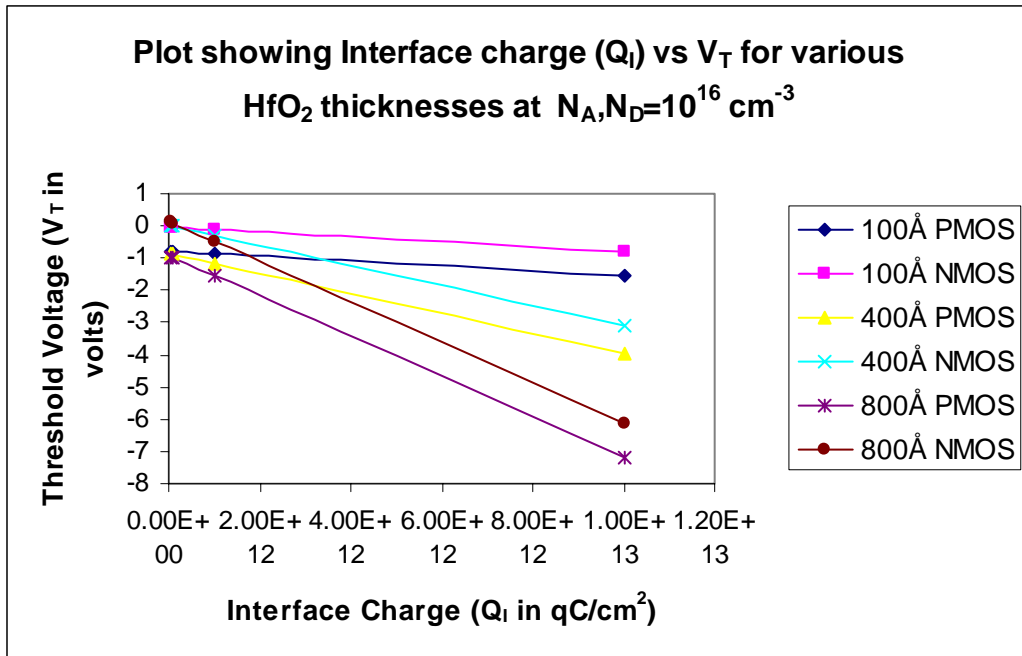


Figure 4.10 Plot showing  $V_T$  vs.  $Q_i$  for various  $HfO_2$  thicknesses at  $N_A, N_D = 10^{16} \text{ cm}^{-3}$

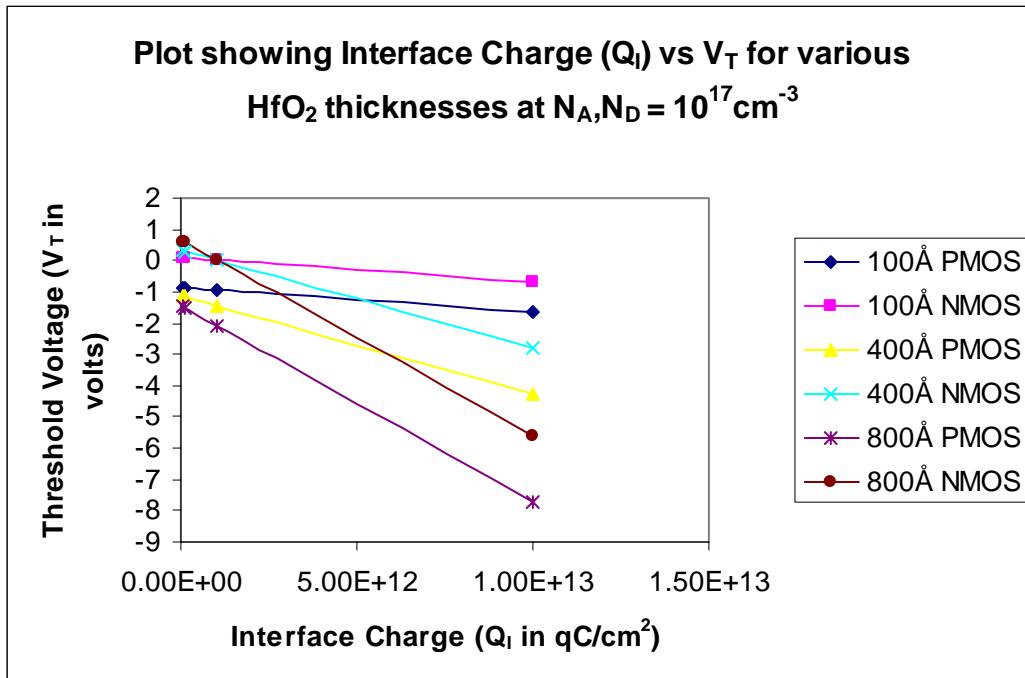


Figure 4.11 Plot showing  $V_T$  vs.  $Q_i$  for various  $HfO_2$  thicknesses at  $N_A, N_D = 10^{17} \text{ cm}^{-3}$

#### 4.1.2 Al/Al<sub>2</sub>O<sub>3</sub> based MOSFET

In this case, the work focused on using aluminum as gate metal and aluminum oxide as gate oxide for PMOS and NMOS field effect transistors. Firstly, the interface trap charge is kept at  $5 \cdot 10^{10} \text{ qC/cm}^2$ . The doping concentration ( $N_A, N_D$ ) is varied from  $5 \cdot 10^{14} \text{ cm}^{-3}$ ,  $10^{15} \text{ cm}^{-3}$ ,  $5 \cdot 10^{15} \text{ cm}^{-3}$ ,  $10^{16} \text{ cm}^{-3}$ ,  $5 \cdot 10^{16} \text{ cm}^{-3}$  and  $10^{17} \text{ cm}^{-3}$  respectively. The oxide thickness ( $T_{OX}$ ) is varied from  $50 \text{ \AA}$ ,  $100 \text{ \AA}$ ,  $200 \text{ \AA}$ ,  $400 \text{ \AA}$ ,  $600 \text{ \AA}$ ,  $800 \text{ \AA}$  and  $1000 \text{ \AA}$  respectively. Next, the interface trap charge ( $Q_I$ ) is varied from  $10^{11} \text{ qC/cm}^2$ ,  $5 \cdot 10^{11} \text{ qC/cm}^2$ ,  $10^{12} \text{ qC/cm}^2$ ,  $5 \cdot 10^{12} \text{ qC/cm}^2$  and  $10^{13} \text{ qC/cm}^2$ . The above  $V_T$  calculations were repeated for all doping concentrations and oxide thicknesses. The threshold voltages vs. oxide thickness for various doping concentrations at constant interface trap charge ( $Q_I = 5 \cdot 10^{10} \text{ qC/cm}^2$ ) are plotted. While the oxide thickness is varied for a range of values, the values which are of interest upon are in the category of thin, medium and thick oxides. For this, thicknesses selected are  $100 \text{ \AA}$ ,  $400 \text{ \AA}$  and  $800 \text{ \AA}$ . The above process of simulations were repeated by changing the interface trap charge ( $Q_I$ ) from  $10^{11} \text{ qC/cm}^2$  to  $10^{13} \text{ qC/cm}^2$  which are plotted in Fig 4.12, 4.13, 4.14 and 4.15 respectively. The threshold voltage for NMOS devices is high ( $-1.527 \text{ V}$ ) for oxide thickness more than  $800 \text{ \AA}$  at  $10^{17} \text{ cm}^{-3}$  doping concentration having any interface charges ( $Q_I$ ).  $V_T$  is low for PMOS devices ( $-0.737 \text{ V}$ ) having oxide thickness less than  $400 \text{ \AA}$  at  $10^{15} \text{ cm}^{-3}$ ,  $10^{16} \text{ cm}^{-3}$  at  $5 \cdot 10^{10} \text{ qC/cm}^2$  and  $10^{11} \text{ qC/cm}^2$  interface charges respectively.

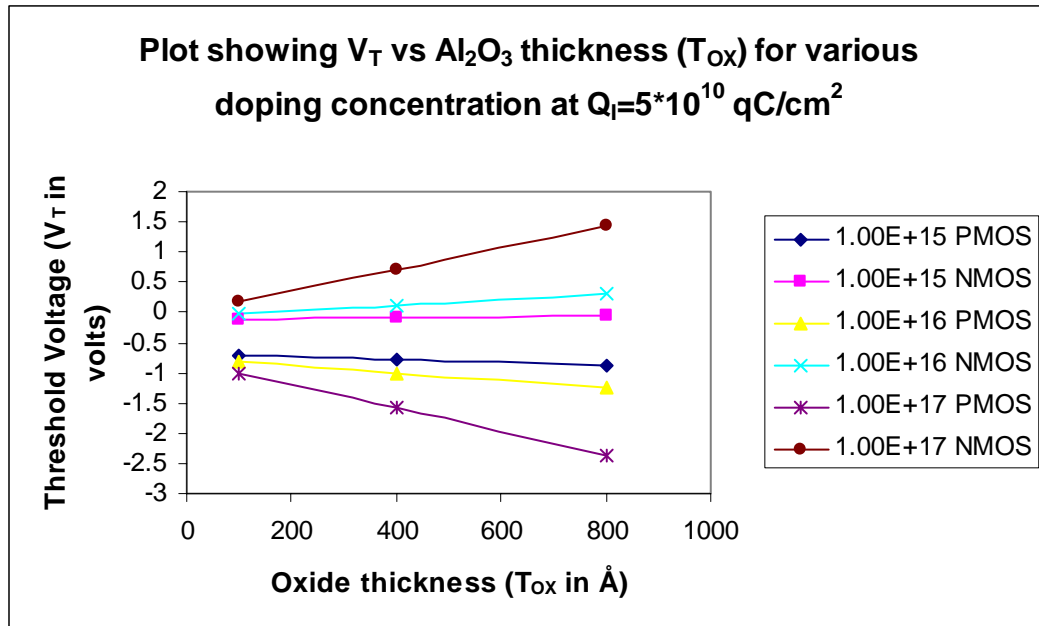


Figure 4.12 Plot showing  $V_T$  vs.  $Al_2O_3$  oxide thickness for various  $N_A$ ,  $N_D$  at  $Q_I=5*10^{10}$  qC/cm<sup>2</sup>

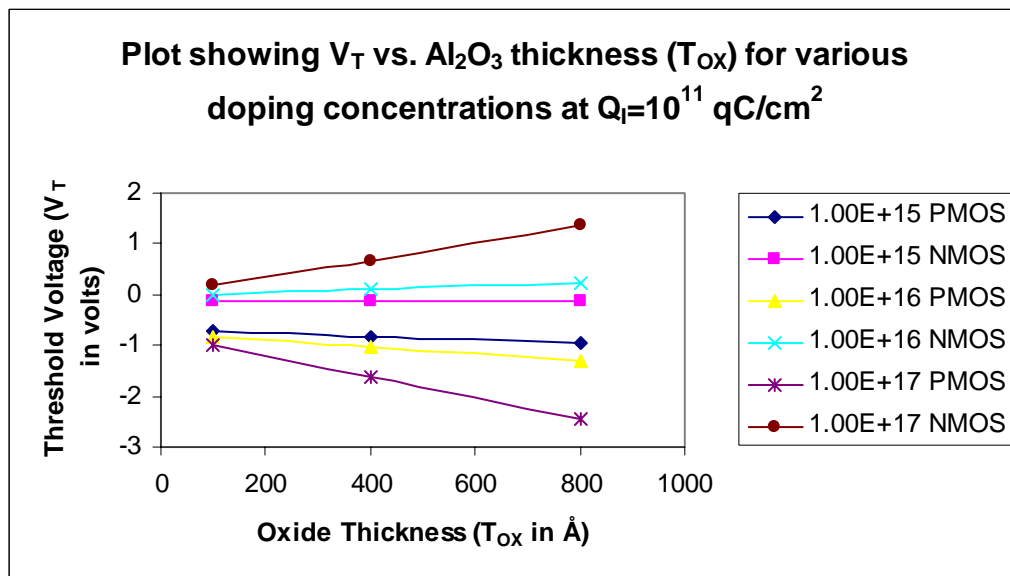


Figure 4.13 Plot showing  $V_T$  vs.  $Al_2O_3$  oxide thickness for various  $N_A$ ,  $N_D$  at  $Q_I=10^{11}$  qC/cm<sup>2</sup>

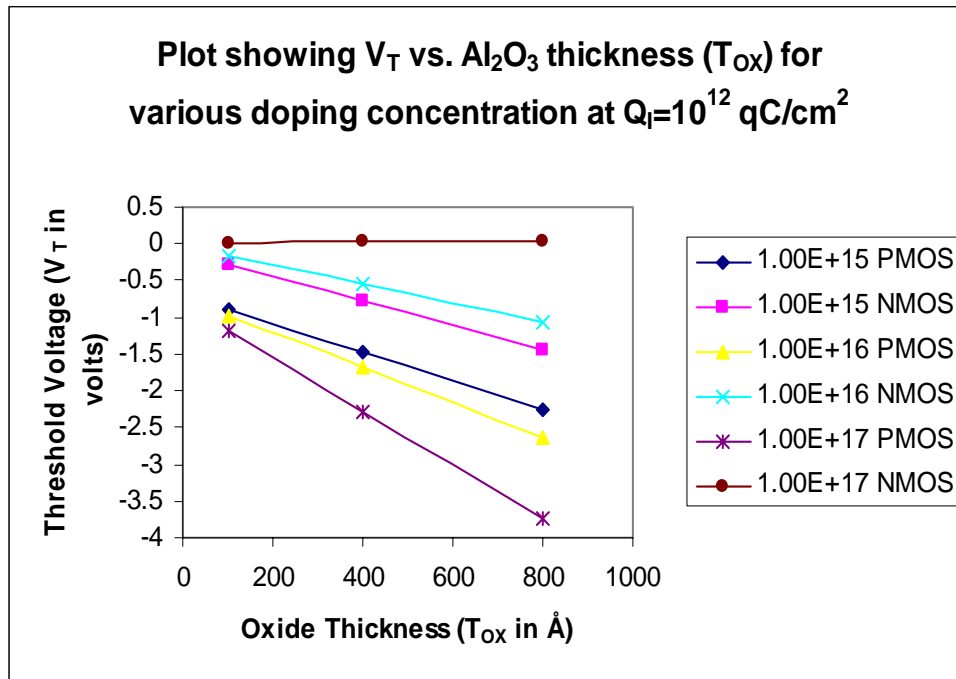


Figure 4.14 Plot showing  $V_T$  vs.  $\text{Al}_2\text{O}_3$  oxide thickness for various  $N_A$ ,  $N_D$  at  $Q_f=10^{12} \text{ qC/cm}^2$

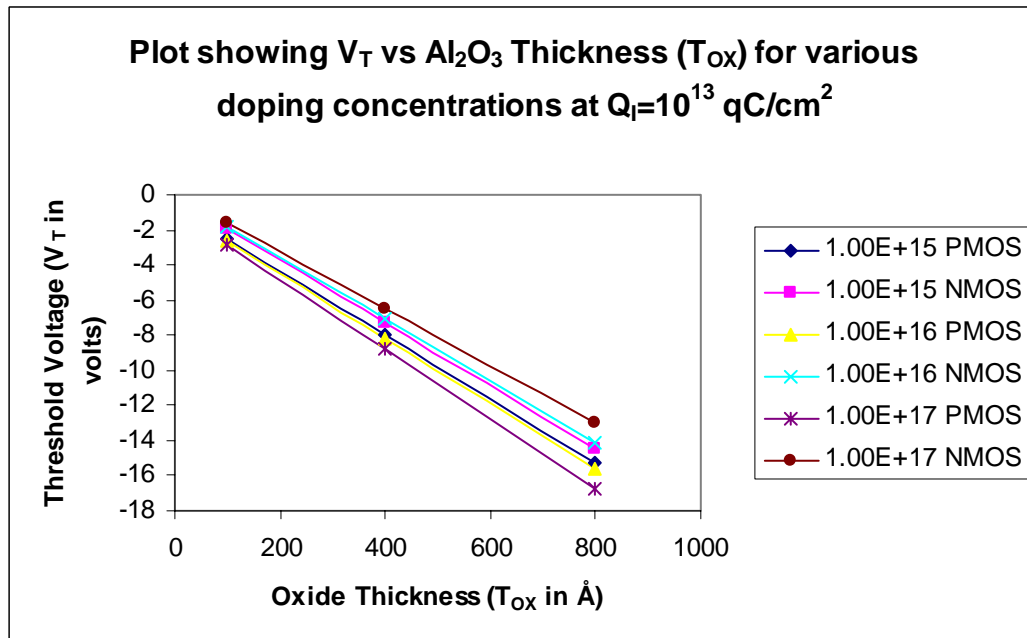


Figure 4.15 Plot showing  $V_T$  vs.  $\text{Al}_2\text{O}_3$  oxide thickness for various  $N_A$ ,  $N_D$  at  $Q_f=10^{13} \text{ qC/cm}^2$

For the Al/Al<sub>2</sub>O<sub>3</sub> system, the interface trap charge (Q<sub>i</sub>) is kept constant at 5\*10<sup>10</sup> qC/cm<sup>2</sup>. Now by varying oxide thickness (initially 100Å, 400Å and 800Å), the threshold voltage is calculated and plotted against doping concentrations (N<sub>A</sub>, N<sub>D</sub>). The above process of simulation is repeated by changing the interface trap charges from 10<sup>11</sup> qC/cm<sup>2</sup> to 10<sup>13</sup> qC/cm<sup>2</sup> which are plotted in Fig 4.16, 4.17, 4.18 and 4.19 respectively. The threshold voltage for PMOS devices is good (-0.786V) with oxide thickness 400Å for doping concentration less than 10<sup>16</sup> cm<sup>-3</sup> at 5\*10<sup>10</sup> qC/cm<sup>2</sup> and 10<sup>11</sup> qC/cm<sup>2</sup> interface charges respectively. V<sub>T</sub> values are in the range of -0.086V to -1.064V for NMOS devices for all oxide thicknesses studied with doping concentrations 10<sup>15</sup> cm<sup>-3</sup> and 10<sup>16</sup> cm<sup>-3</sup>.

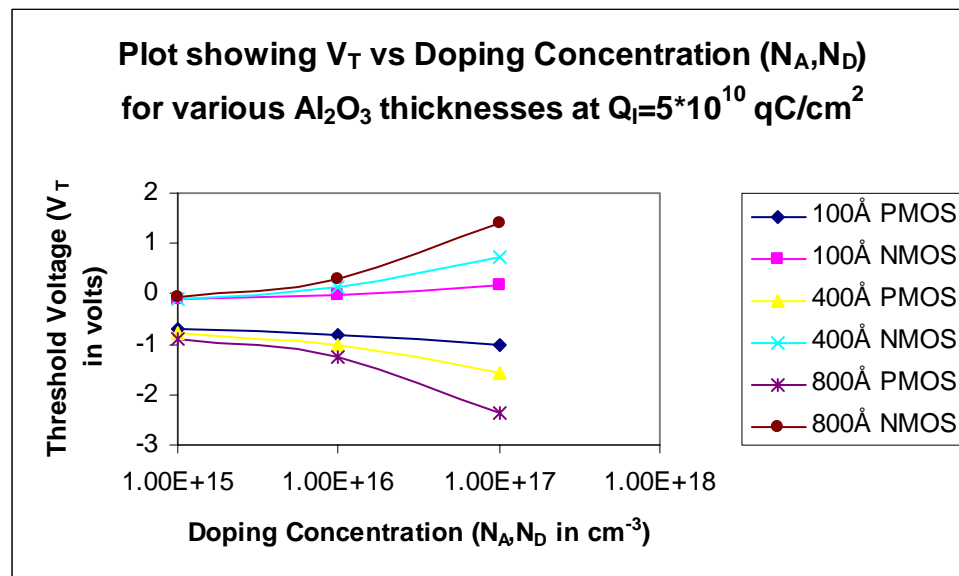


Figure 4.16 Plot showing Doping Concentration vs. V<sub>T</sub> for various Al<sub>2</sub>O<sub>3</sub> thickness at Q<sub>i</sub>=5\*10<sup>10</sup> qC/cm<sup>2</sup>

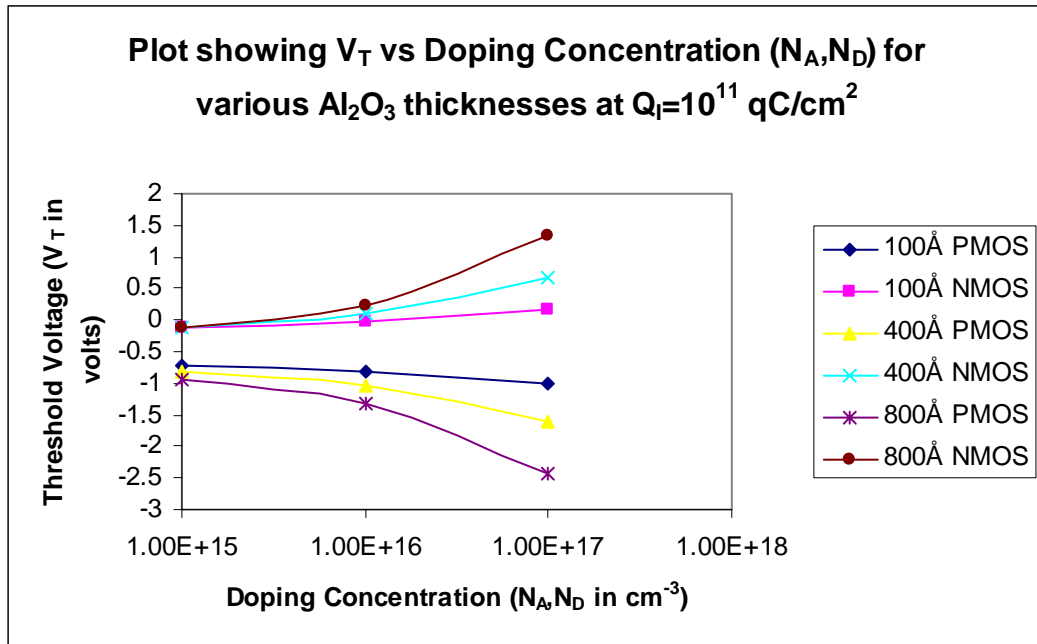


Figure 4.17 Plot showing Doping Concentration vs.  $V_T$  for various  $Al_2O_3$  thickness at  $Q_f=10^{11}$  qC/cm<sup>2</sup>

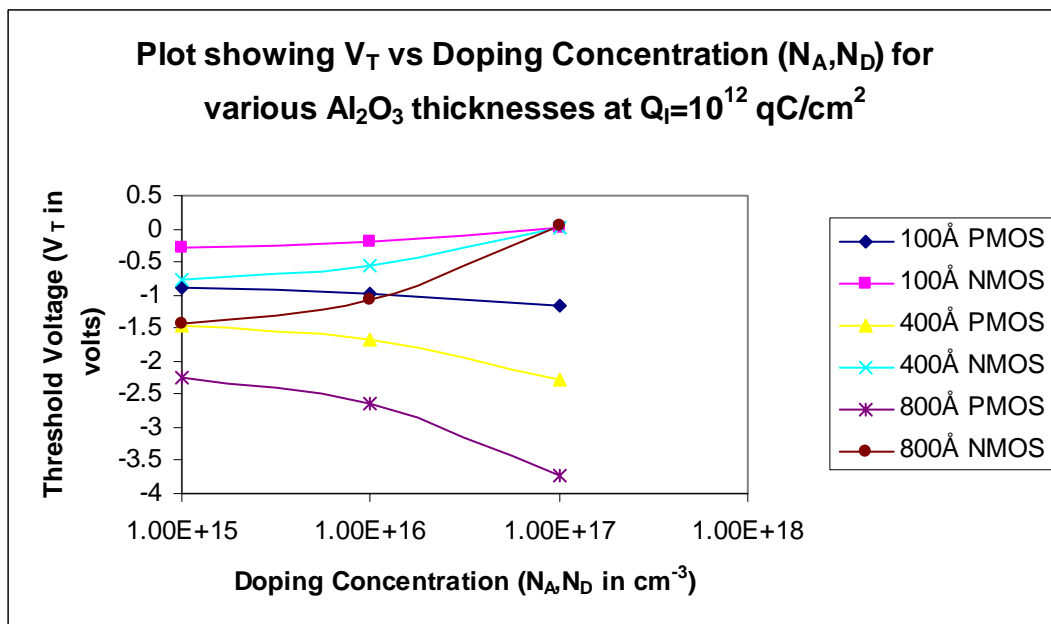


Figure 4.18 Plot showing Doping Concentration vs.  $V_T$  for various  $Al_2O_3$  thickness at  $Q_f=10^{12}$  qC/cm<sup>2</sup>

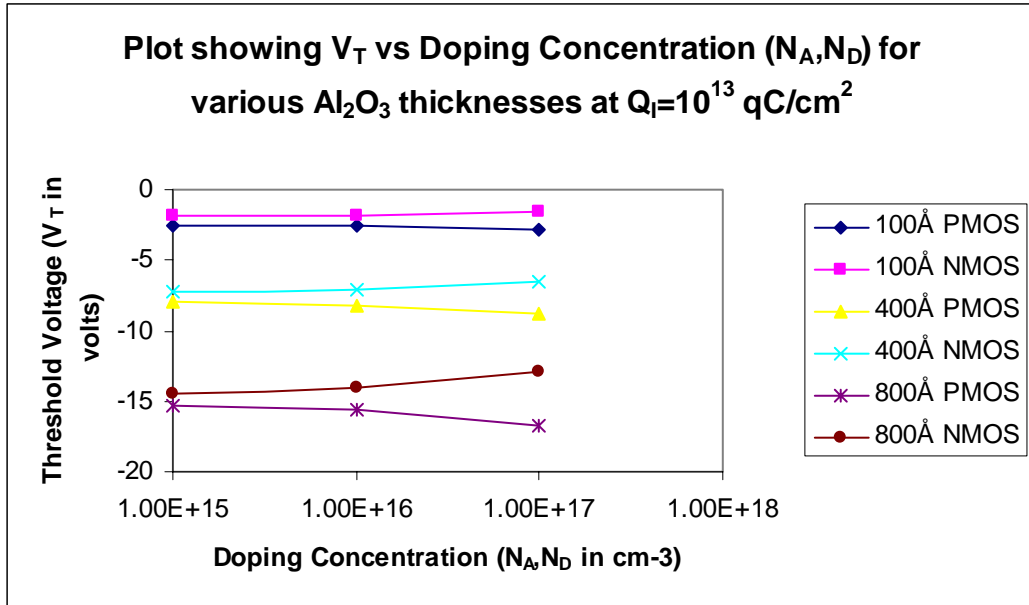


Figure 4.19 Plot showing Doping Concentration vs.  $V_T$  for various  $\text{Al}_2\text{O}_3$  thickness at  $Q_I=10^{13}$   $\text{qC}/\text{cm}^2$

For the Al/ $\text{Al}_2\text{O}_3$  system, now the doping concentration ( $N_A, N_D$ ) is held constant at  $10^{15}$   $\text{cm}^{-3}$ . Now by varying oxide thickness (initially 100Å, 400Å and 800Å), the threshold voltage is calculated and plotted against different values of interface trap charges ( $Q_I$ ) Fig 4.20. The above process of simulation is repeated by changing the doping concentrations from  $10^{16}$   $\text{cm}^{-3}$  and  $10^{17}$   $\text{cm}^{-3}$  are plotted in Fig 4.21 and 4.22 respectively. The threshold voltage is good for PMOS (-0.885V) at doping concentration of  $10^{15}$   $\text{cm}^{-3}$  for all oxide thicknesses at interface charge  $5 \cdot 10^{10}$   $\text{qC}/\text{cm}^2$ . The  $V_T$  is good for NMOS (0.987V) for all oxide thicknesses at various interface charges. At  $10^{13}$   $\text{qC}/\text{cm}^2$  the threshold voltage is too high (-1.94V).



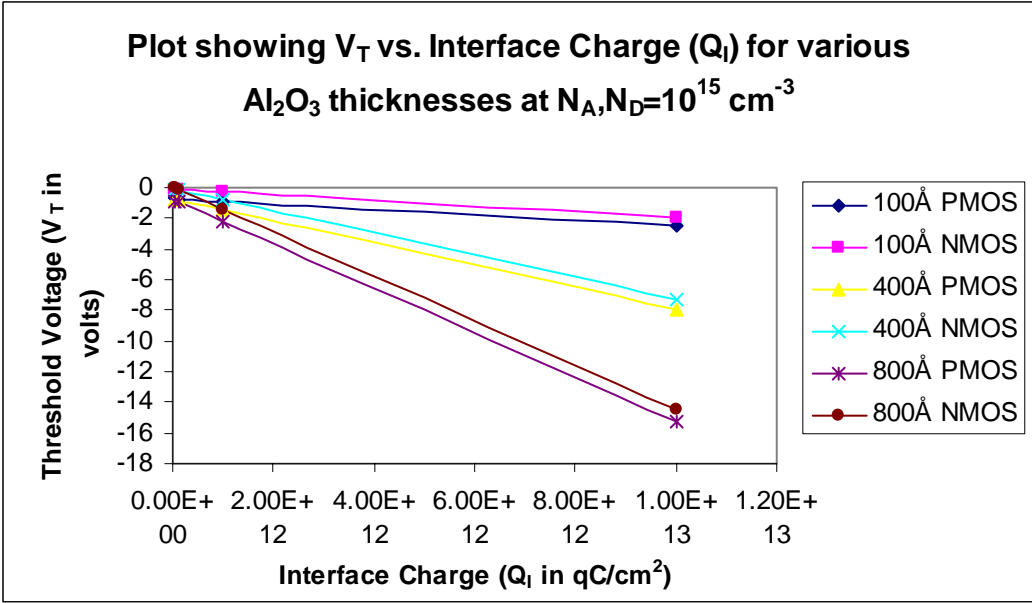


Figure 4.20 Plot showing  $V_T$  vs.  $Q_I$  for various  $Al_2O_3$  thicknesses at  $N_A, N_D = 10^{15} \text{ cm}^{-3}$

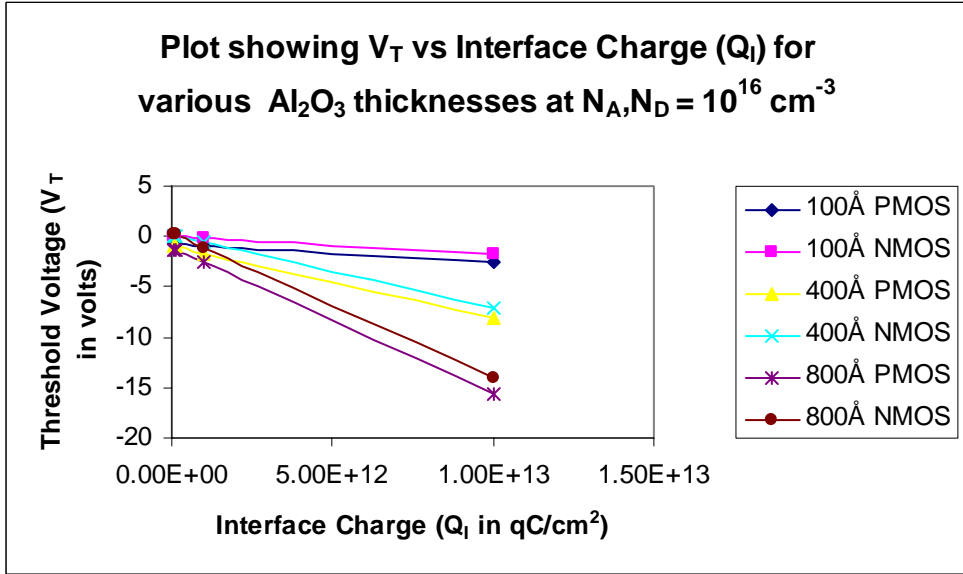


Figure 4.21 Plot showing  $V_T$  vs.  $Q_I$  for various  $Al_2O_3$  thicknesses at  $N_A, N_D = 10^{16} \text{ cm}^{-3}$

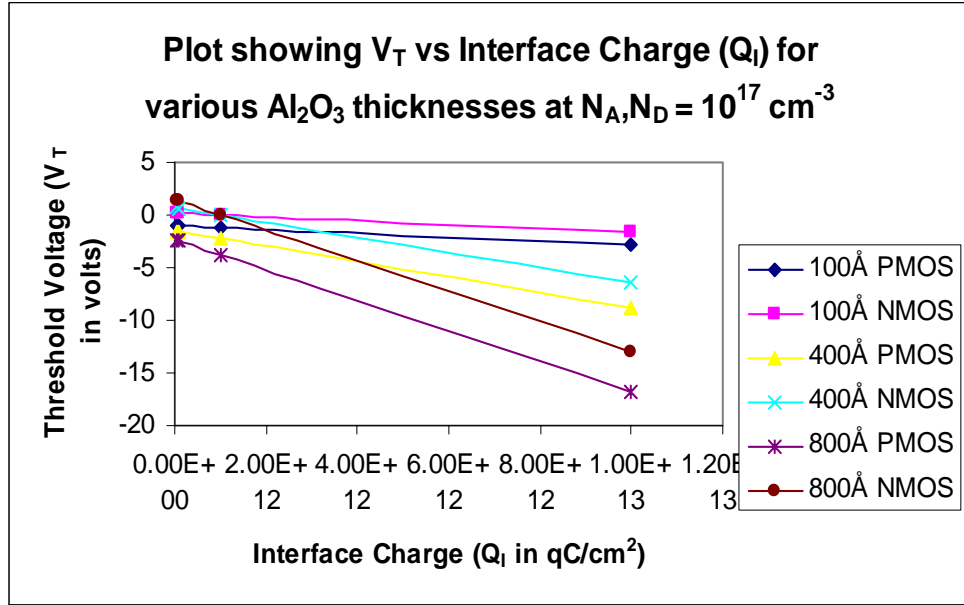


Figure 4.22 Plot showing  $V_T$  vs.  $Q_I$  for various  $Al_2O_3$  thicknesses at  $N_A, N_D=10^{17} \text{ cm}^{-3}$

#### 4.1.3 Al/Ta<sub>2</sub>O<sub>5</sub> based MOSFET

In this case, the work focused on using aluminum as gate metal and tantalum oxide as gate oxide for PMOS and NMOS field effect transistors. Firstly, the interface trap charge is kept at  $5 \cdot 10^{10} \text{ qC/cm}^2$ . The doping concentration ( $N_A, N_D$ ) is varied from  $5 \cdot 10^{14} \text{ cm}^{-3}$ ,  $10^{15} \text{ cm}^{-3}$ ,  $5 \cdot 10^{15} \text{ cm}^{-3}$ ,  $10^{16} \text{ cm}^{-3}$ ,  $5 \cdot 10^{16} \text{ cm}^{-3}$  and  $10^{17} \text{ cm}^{-3}$  respectively. The oxide thickness ( $T_{OX}$ ) is varied from 50Å, 100Å, 200Å, 400Å, 600Å, 800Å and 1000Å respectively. Next the interface trap charge ( $Q_I$ ) is varied from  $10^{11} \text{ qC/cm}^2$ ,  $5 \cdot 10^{11} \text{ qC/cm}^2$ ,  $10^{12} \text{ qC/cm}^2$ ,  $5 \cdot 10^{12} \text{ qC/cm}^2$  and  $10^{13} \text{ qC/cm}^2$ . The above  $V_T$  calculations were repeated for all doping concentrations and oxide thicknesses. The threshold voltages vs. oxide thickness for various doping concentrations at constant interface trap charge ( $Q_I=5 \cdot 10^{10} \text{ qC/cm}^2$ ) are plotted. While the oxide thickness is varied for a range of values, the values which are of interest are in the category of thin, medium

and thick oxides. For this, thicknesses selected are 100Å, 400Å and 800Å. The above process of simulations were repeated by changing the interface trap charge ( $Q_I$ ) from  $10^{11}$  qC/cm<sup>2</sup> to  $10^{13}$  qC/cm<sup>2</sup> which are plotted in Fig 4.23, 4.24, 4.25 and 4.26 respectively. The simulated results show that threshold voltage for NMOS devices are in the range of -0.06V to 0.573V having various oxide thicknesses at various doping concentrations with different interface trap charges. At  $10^{13}$  qC/cm<sup>2</sup> the threshold voltage is too high (-5.181V). The threshold voltage of PMOS is optimum (-0.95V) only for 100Å, 400Å, 800Å thickness with substrate doping concentration of  $10^{15}$ cm<sup>-3</sup>,  $10^{16}$ cm<sup>-3</sup> at  $5 \cdot 10^{10}$  qC/cm<sup>2</sup> and  $10^{11}$  qC/cm<sup>2</sup> interface charges.

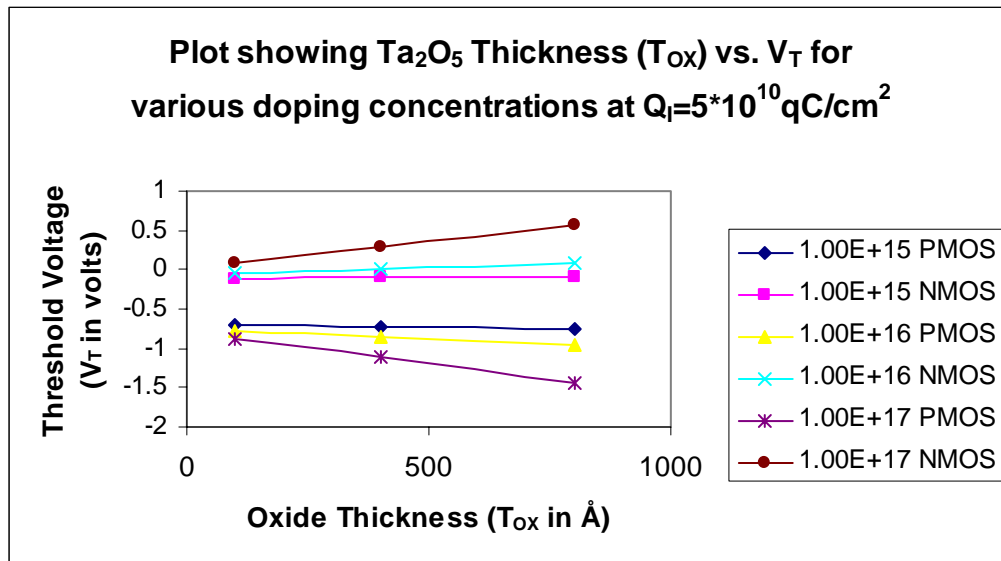


Figure 4.23 Plot showing V<sub>T</sub> vs. Ta<sub>2</sub>O<sub>5</sub> thickness for various N<sub>A</sub>, N<sub>D</sub> at Q<sub>I</sub>=5\*10<sup>10</sup> qC/cm<sup>2</sup>

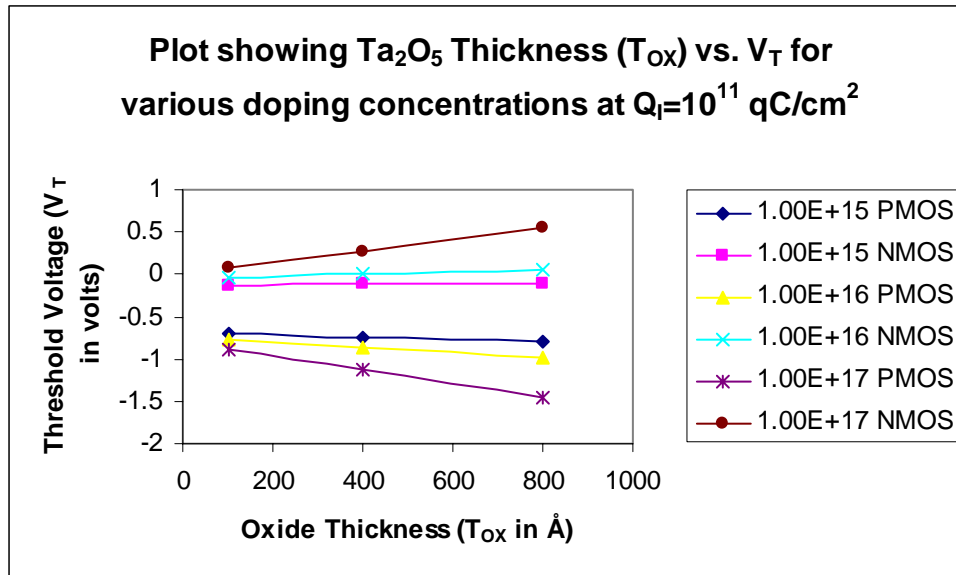


Figure 4.24 Plot showing V<sub>T</sub> vs. Ta<sub>2</sub>O<sub>5</sub> thickness for various N<sub>A</sub>, N<sub>D</sub> at Q<sub>I</sub>=10<sup>11</sup> qC/cm<sup>2</sup>

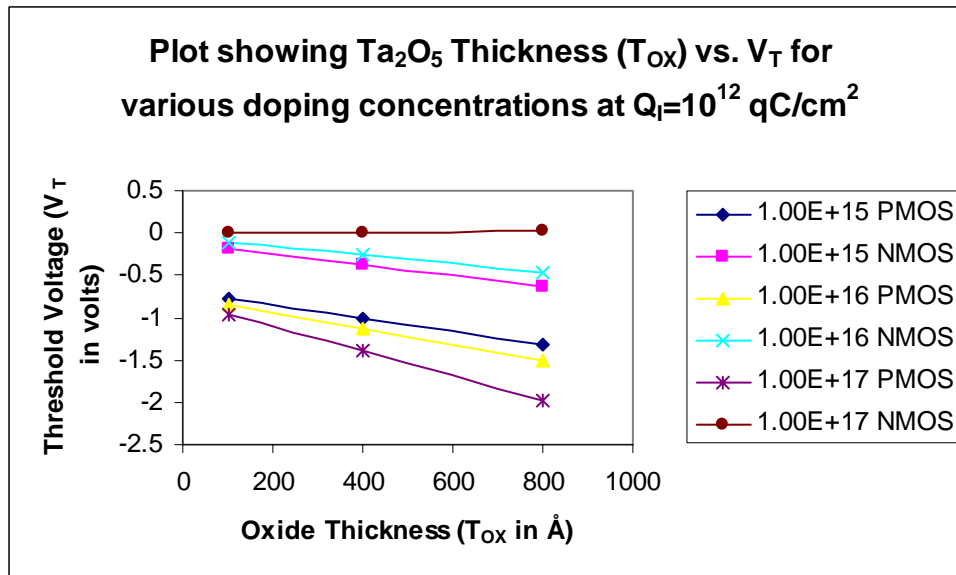


Figure 4.25 Plot showing V<sub>T</sub> vs. Ta<sub>2</sub>O<sub>5</sub> thickness for various N<sub>A</sub>, N<sub>D</sub> at Q<sub>I</sub>=10<sup>12</sup> qC/cm<sup>2</sup>

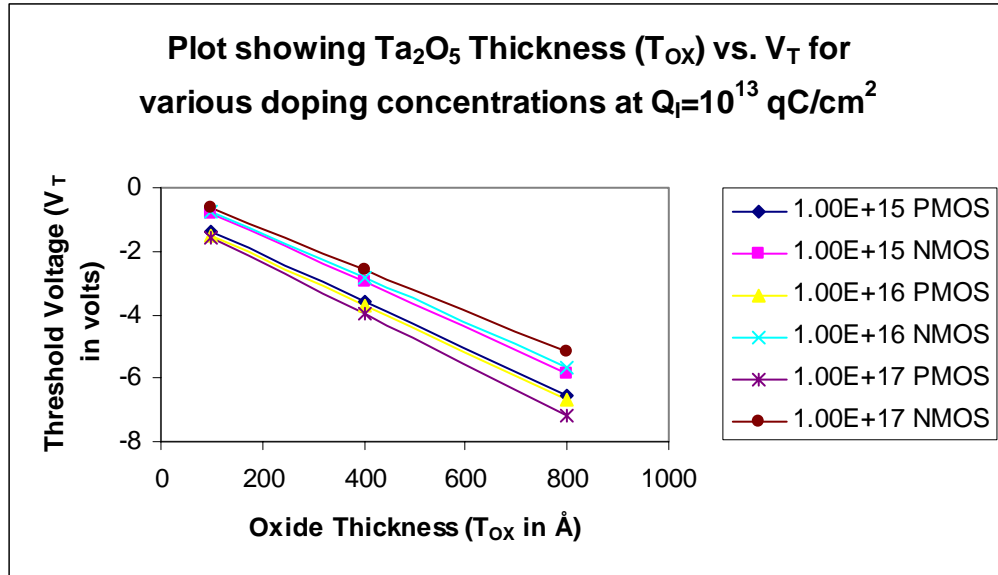


Figure 4.26 Plot showing V<sub>T</sub> vs. Ta<sub>2</sub>O<sub>5</sub> thickness for various N<sub>A</sub>, N<sub>D</sub> at Q<sub>I</sub>=10<sup>13</sup> qC/cm<sup>2</sup>

For the same Al/Ta<sub>2</sub>O<sub>5</sub> system, the interface trap charge (Q<sub>I</sub>) is kept constant at 5\*10<sup>10</sup> qC/cm<sup>2</sup>. Now by varying oxide thickness (initially 100Å, 400Å and 800Å), the threshold voltage is calculated and plotted against doping concentrations (N<sub>A</sub>, N<sub>D</sub>). The above processes of simulation is repeated by changing the interface trap charges from 10<sup>11</sup> qC/cm<sup>2</sup> to 10<sup>13</sup> qC/cm<sup>2</sup> and are plotted in Fig 4.27, 4.28, 4.29 and 4.30 respectively. The threshold voltage for PMOS devices is good (-0.863V) with oxide thickness 400Å for doping concentration less than 10<sup>16</sup> cm<sup>-3</sup> at 5\*10<sup>10</sup> qC/cm<sup>2</sup> and 10<sup>11</sup> qC/cm<sup>2</sup> interface charges respectively. V<sub>T</sub> is low (-1.005V) for NMOS devices at various oxide thicknesses at different interface charges and doping concentrations except at 10<sup>13</sup> qC/cm<sup>2</sup> and 10<sup>17</sup> cm<sup>-3</sup> respectively.

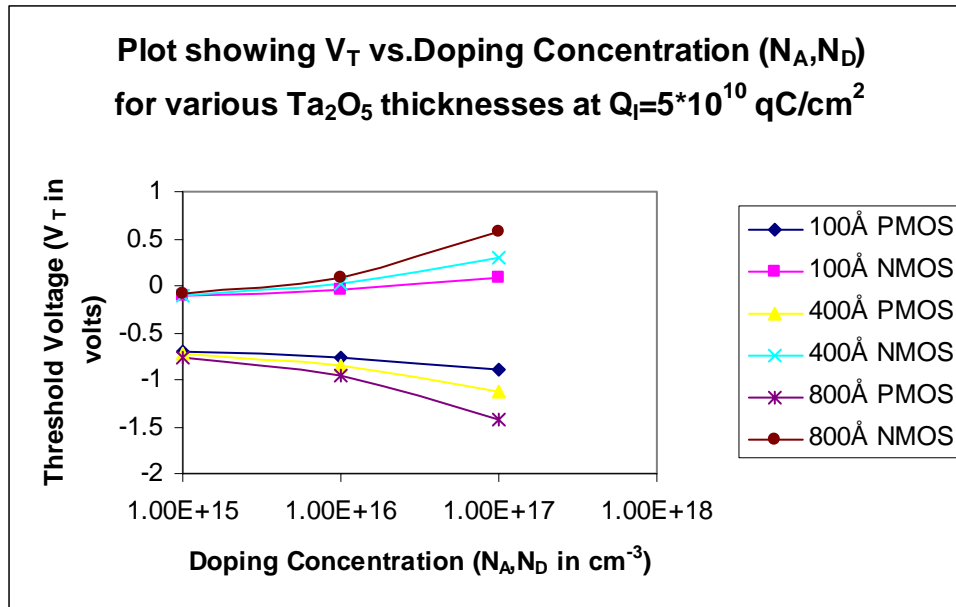


Figure 4.27 Plot showing Doping Concentration vs.  $V_T$  for various  $Ta_2O_5$  thicknesses at  $Q_I = 5 \cdot 10^{10} \text{ qC/cm}^2$

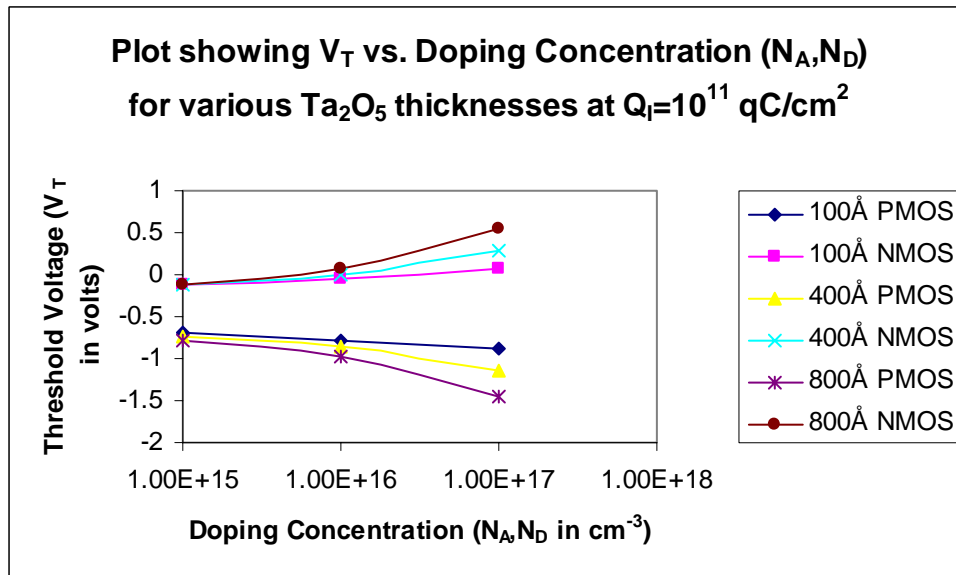


Figure 4.28 Plot showing Doping Concentration vs.  $V_T$  for various  $Ta_2O_5$  thicknesses at  $Q_I = 10^{11} \text{ qC/cm}^2$

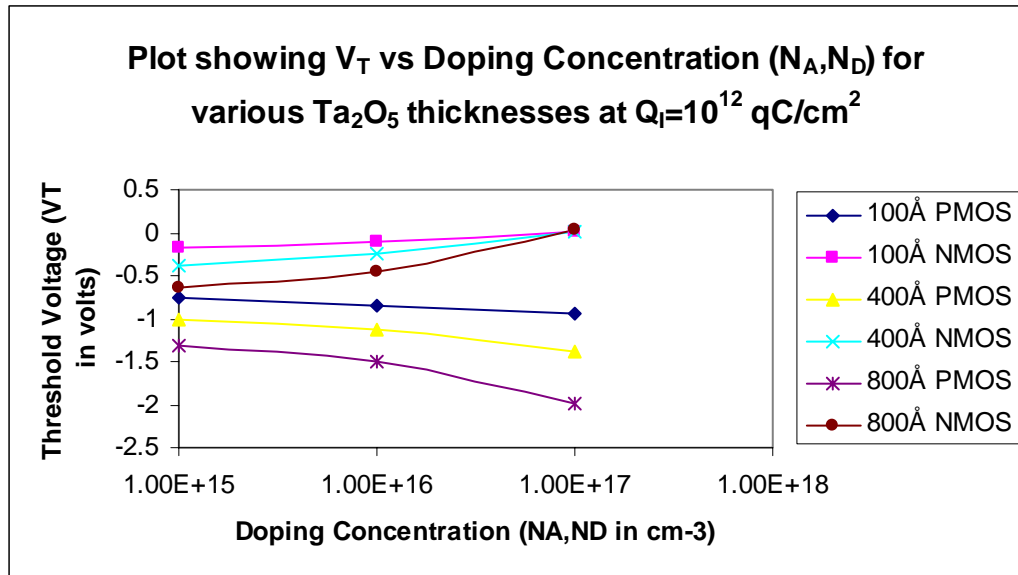


Figure 4.29 Plot showing Doping Concentration vs.  $V_T$  for various  $Ta_2O_5$  thicknesses at  $Q_f=10^{12}$  qC/cm<sup>2</sup>

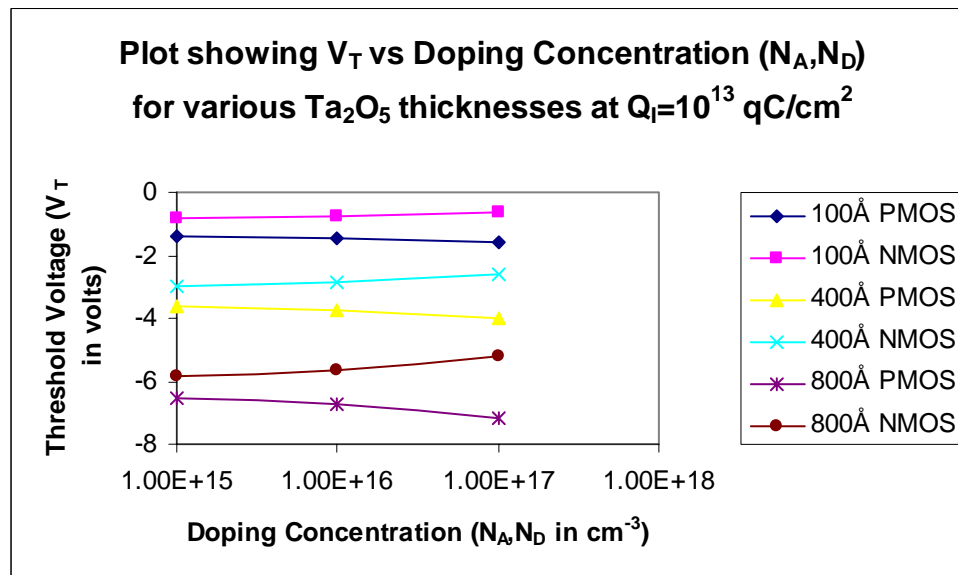


Figure 4.30 Plot showing Doping Concentration vs.  $V_T$  for various  $Ta_2O_5$  thicknesses at  $Q_f=10^{13}$  qC/cm<sup>2</sup>

For the Al/Ta<sub>2</sub>O<sub>5</sub> system, now the doping concentration ( $N_A$ ,  $N_D$ ) is held constant at  $10^{15}$  cm<sup>-3</sup>. Now by varying oxide thickness (initially 100Å, 400Å and 800Å), the threshold voltage is calculated and plotted against different values of interface trap charges ( $Q_I$ ) Fig 4.31. The above process of simulation is repeated by changing the doping concentrations from  $10^{16}$  cm<sup>-3</sup> and  $10^{17}$  cm<sup>-3</sup> are plotted in Fig 4.32 and 4.33 respectively. The threshold voltage is low for PMOS (-0.97V) and NMOS (0.573V) devices at doping concentrations  $10^{15}$  cm<sup>-3</sup> and  $10^{16}$  cm<sup>-3</sup> for all oxide thicknesses at interface charges  $5 \cdot 10^{10}$  qC/cm<sup>2</sup>,  $10^{11}$  qC/cm<sup>2</sup> and  $10^{12}$  qC/cm<sup>2</sup> respectively.

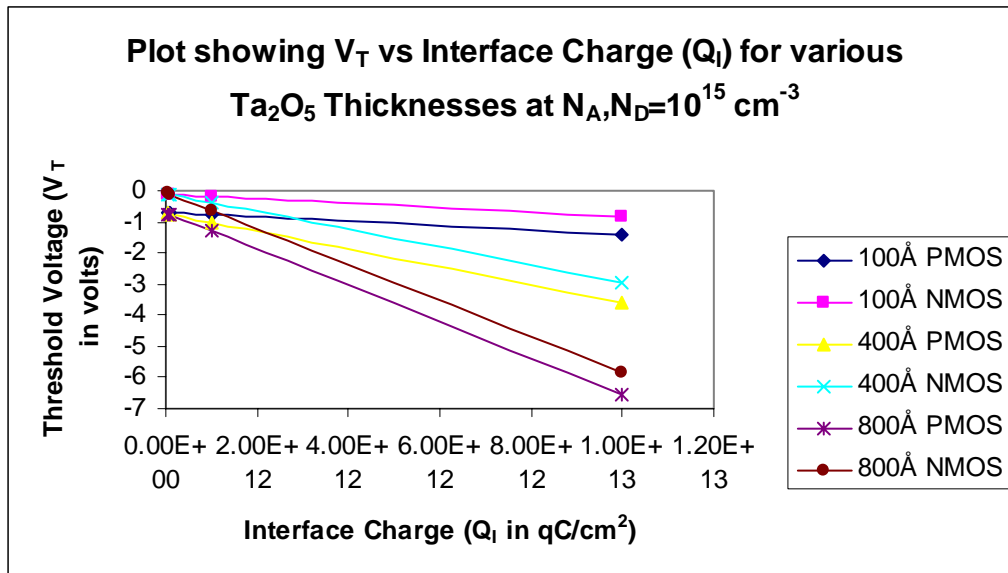


Figure 4.31 Plot showing  $V_T$  vs.  $Q_I$  for various  $Ta_2O_5$  thicknesses at  $N_A, N_D = 10^{15}$  cm<sup>-3</sup>



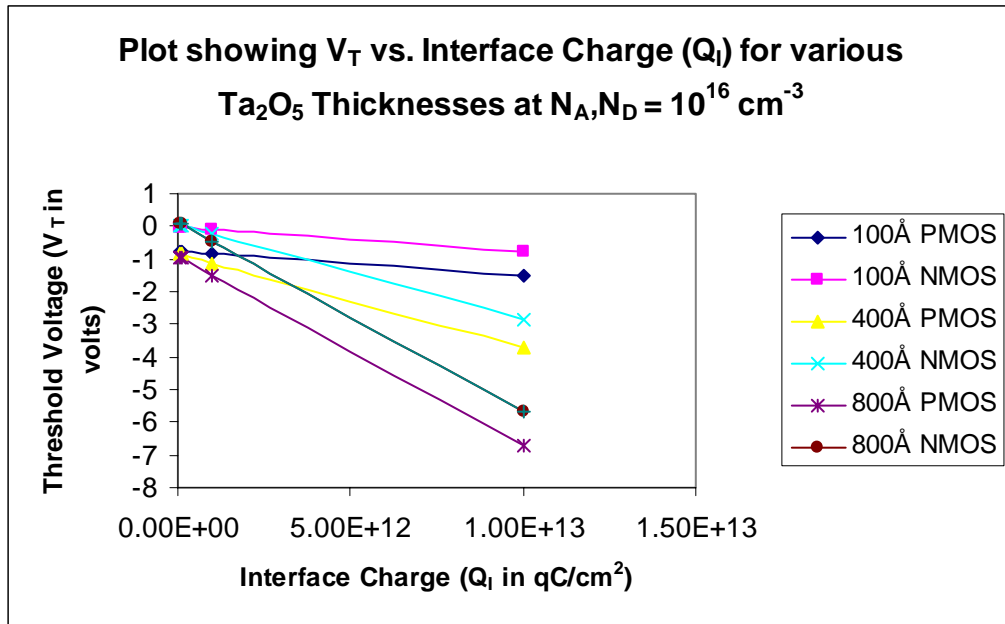


Figure 4.32 Plot showing  $V_T$  vs.  $Q_I$  for various  $Ta_2O_5$  thicknesses at  $N_A, N_D=10^{16} \text{ cm}^{-3}$

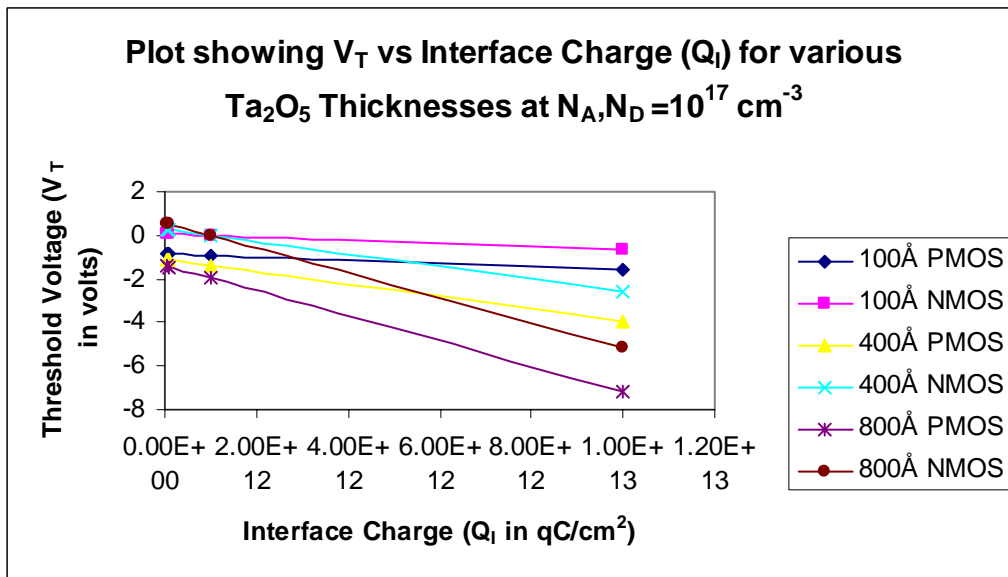


Figure 4.33 Plot showing  $V_T$  vs.  $Q_I$  for various  $Ta_2O_5$  thicknesses at  $N_A, N_D=10^{17} \text{ cm}^{-3}$

#### 4.1.4 Al/ZrO<sub>2</sub> based MOSFET

In this case, the work focused on using aluminum as gate metal and zirconium oxide as gate oxide for PMOS and NMOS field effect transistors. Firstly the interface trap charge is kept at  $5 \times 10^{10} \text{ qC/cm}^2$ . The doping concentration ( $N_A, N_D$ ) is varied from  $5 \times 10^{14} \text{ cm}^{-3}$ ,  $10^{15} \text{ cm}^{-3}$ ,  $5 \times 10^{15} \text{ cm}^{-3}$ ,  $10^{16} \text{ cm}^{-3}$ ,  $5 \times 10^{16} \text{ cm}^{-3}$  and  $10^{17} \text{ cm}^{-3}$  respectively. The oxide thickness ( $T_{OX}$ ) is varied from  $50 \text{ \AA}$ ,  $100 \text{ \AA}$ ,  $200 \text{ \AA}$ ,  $400 \text{ \AA}$ ,  $600 \text{ \AA}$ ,  $800 \text{ \AA}$  and  $1000 \text{ \AA}$  respectively. The interface trap charge ( $Q_I$ ) is varied from  $10^{11} \text{ qC/cm}^2$ ,  $5 \times 10^{11} \text{ qC/cm}^2$ ,  $10^{12} \text{ qC/cm}^2$ ,  $5 \times 10^{12} \text{ qC/cm}^2$  and  $10^{13} \text{ qC/cm}^2$  respectively. The above  $V_T$  calculations were repeated for all doping concentrations and oxide thicknesses. The threshold voltages vs. oxide thickness for various doping concentrations at constant interface trap charge ( $Q_I = 5 \times 10^{10} \text{ qC/cm}^2$ ) are plotted. While the oxide thickness is varied for a range of values, the values of interest are in the category of thin, medium and thick oxides. For this thicknesses selected are  $100 \text{ \AA}$ ,  $400 \text{ \AA}$  and  $800 \text{ \AA}$ . The above process of simulations were repeated by changing the interface trap charge ( $Q_I$ ) from  $10^{11} \text{ qC/cm}^2$  to  $10^{13} \text{ qC/cm}^2$  which are plotted in Fig 4.34, 4.35, 4.36 and 4.37 respectively. The simulated results show that threshold voltage for PMOS is low ( $-0.888 \text{ V}$ ) for oxide thicknesses less than  $400 \text{ \AA}$  at doping concentrations  $10^{15} \text{ cm}^{-3}$  and  $10^{16} \text{ cm}^{-3}$  having interface charges  $5 \times 10^{10} \text{ qC/cm}^2$  and  $10^{11} \text{ qC/cm}^2$  respectively. The  $V_T$  for NMOS devices are in the range of  $-0.13 \text{ V}$  to  $0.432 \text{ V}$  for various doping concentrations studied at different interface charges for all oxide thicknesses. At interface charge of  $10^{13} \text{ qC/cm}^2$  the value of  $V_T$  for NMOS devices is too high ( $-7.198 \text{ V}$ ).

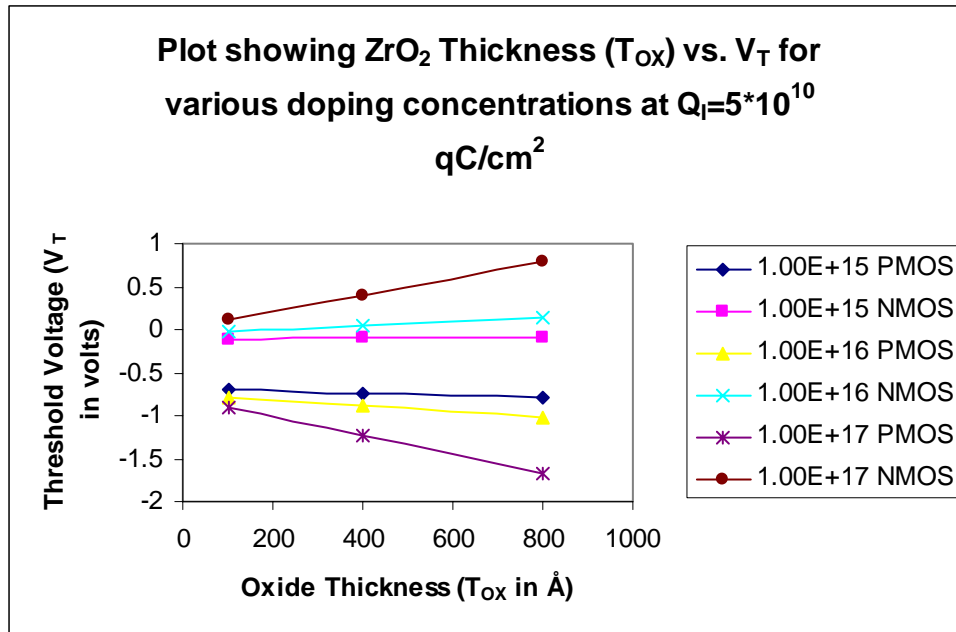


Figure 4.34 Plot showing V<sub>T</sub> vs. ZrO<sub>2</sub> thickness for various N<sub>A</sub>, N<sub>D</sub> at Q<sub>i</sub>=5\*10<sup>10</sup> qC/cm<sup>2</sup>

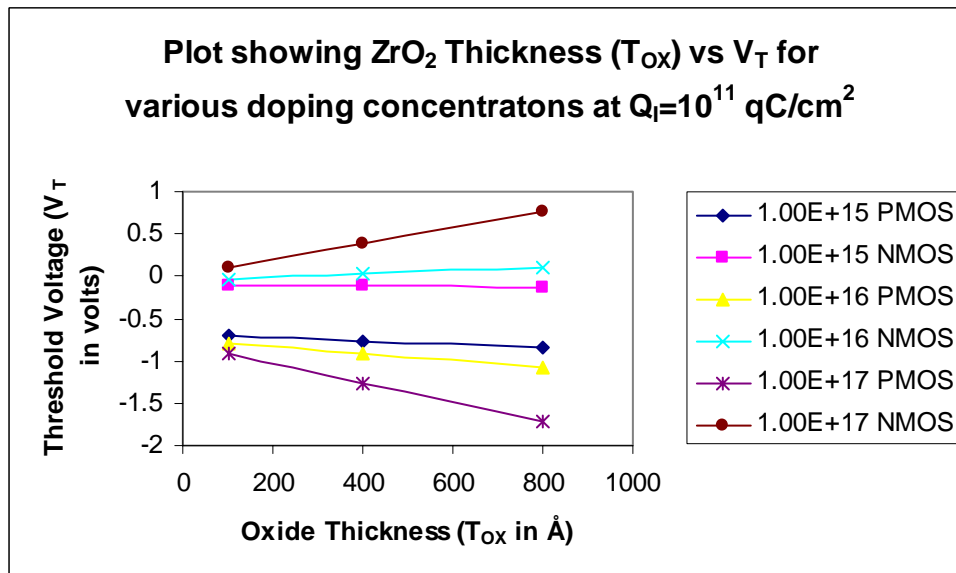


Figure 4.35 Plot showing V<sub>T</sub> vs. ZrO<sub>2</sub> thickness for various N<sub>A</sub>, N<sub>D</sub> at Q<sub>i</sub>=10<sup>11</sup> qC/cm<sup>2</sup>

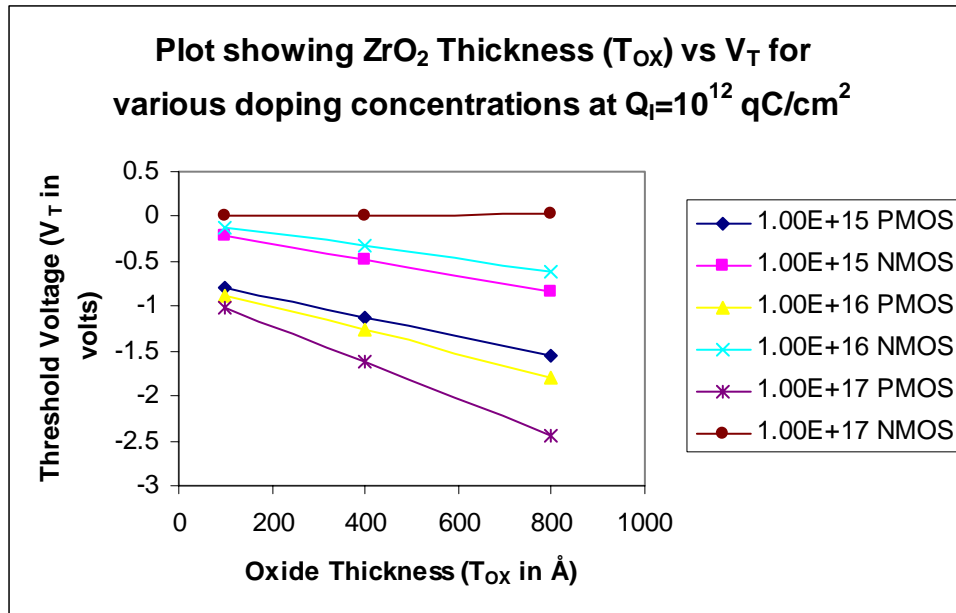


Figure 4.36 Plot showing V<sub>T</sub> vs. ZrO<sub>2</sub> thickness for various N<sub>A</sub>, N<sub>D</sub> at Q<sub>I</sub>=10<sup>12</sup> qC/cm<sup>2</sup>

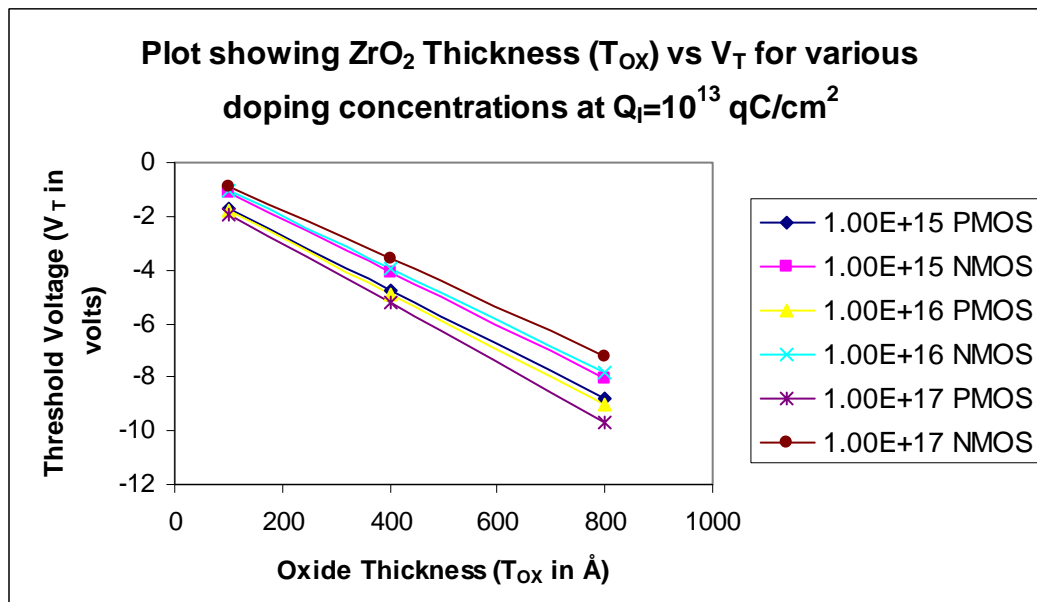


Figure 4.37 Plot showing V<sub>T</sub> vs. ZrO<sub>2</sub> thickness for various N<sub>A</sub>, N<sub>D</sub> at Q<sub>I</sub>=10<sup>13</sup> qC/cm<sup>2</sup>

For the Al/ZrO<sub>2</sub> system, the interface trap charge (Q<sub>i</sub>) is kept constant at 5\*10<sup>10</sup> qC/cm<sup>2</sup>. Now by varying oxide thickness (initially 100Å, 400Å and 800Å), the threshold voltage is calculated and plotted for various doping concentrations (N<sub>A</sub>, N<sub>D</sub>). The above process of simulation is repeated by varying the interface trap charges from 10<sup>11</sup> qC/cm<sup>2</sup> to 10<sup>13</sup> qC/cm<sup>2</sup> and is plotted in Fig 4.38, 4.39, 4.40 and 4.41 respectively. The simulated results show that threshold voltage for PMOS devices are low in the range of -0.701V to -1.069V for oxide thicknesses of less than 400Å and interface trap charges of 5\*10<sup>10</sup> qC/cm<sup>2</sup> and 10<sup>11</sup> qC/cm<sup>2</sup>. Similarly for NMOS devices V<sub>T</sub> is low in the range of -0.109V to 0.38V for oxide thicknesses of less than 400Å and interface trap charges except 10<sup>13</sup> qC/cm<sup>2</sup>. At interface charge of 10<sup>13</sup> qC/cm<sup>2</sup> threshold voltage is too high (-7.198V).

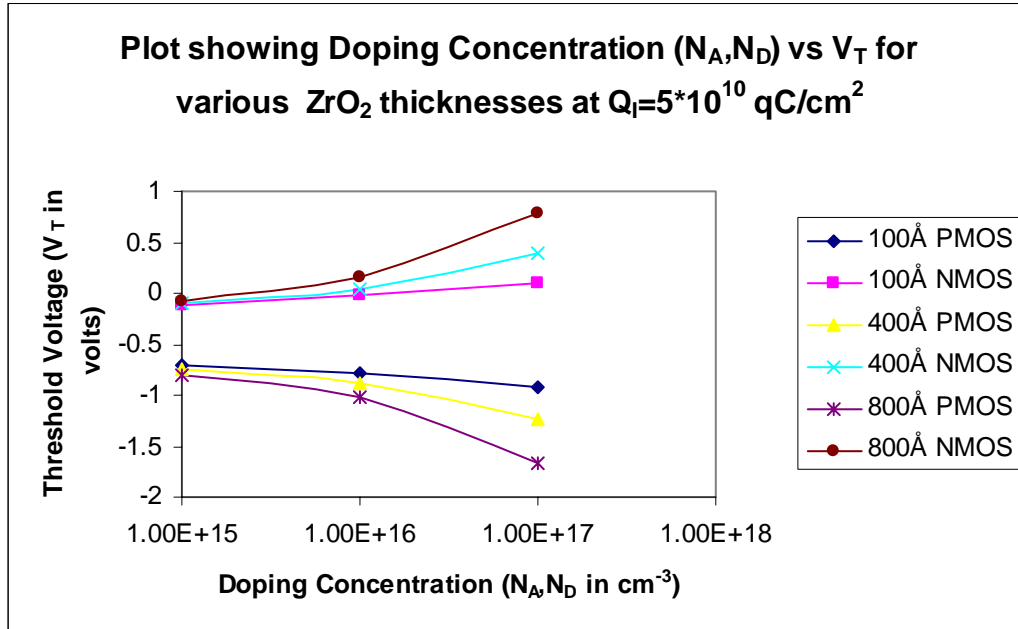


Figure 4.38 Plot showing Doping Concentration vs. V<sub>T</sub> for various ZrO<sub>2</sub> thicknesses at Q<sub>i</sub>=5\*10<sup>10</sup> qC/cm<sup>2</sup>

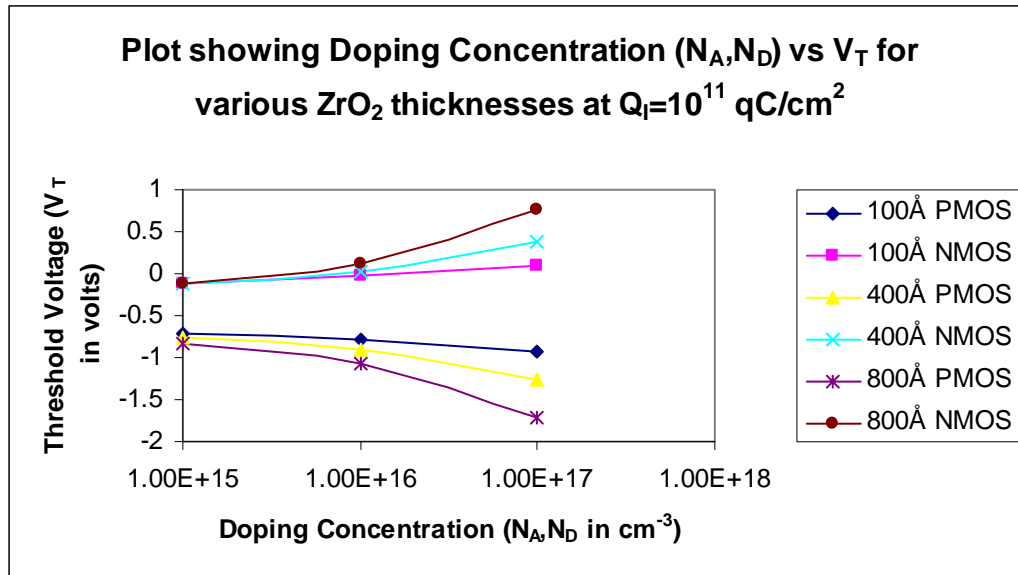


Figure 4.39 Plot showing Doping Concentration vs.  $V_T$  for various  $ZrO_2$  thicknesses at  $Q_f=10^{11}$   $qC/cm^2$

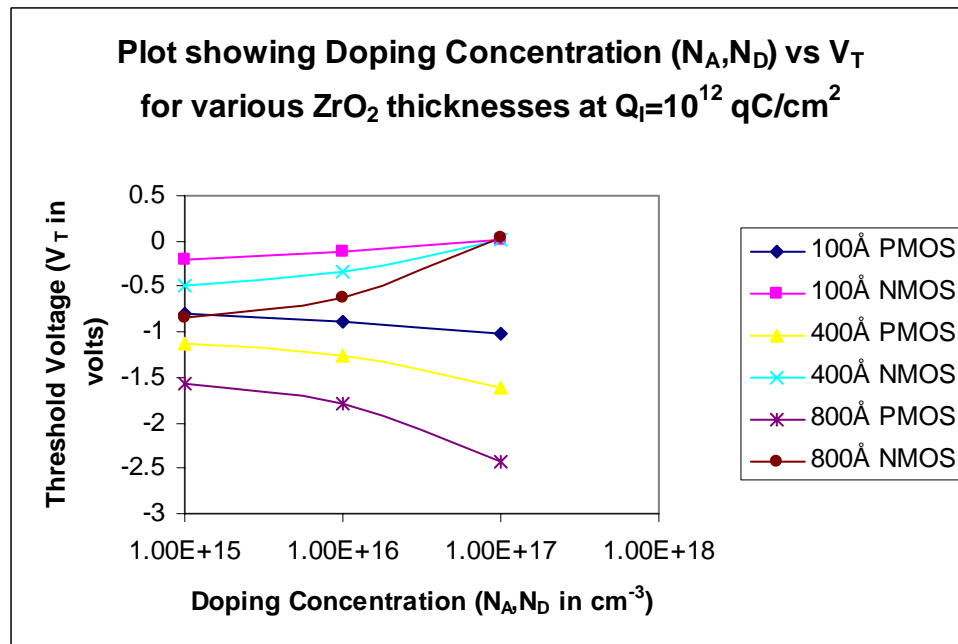


Figure 4.40 Plot showing Doping Concentration vs.  $V_T$  for various  $ZrO_2$  thicknesses at  $Q_f=10^{12}$   $qC/cm^2$

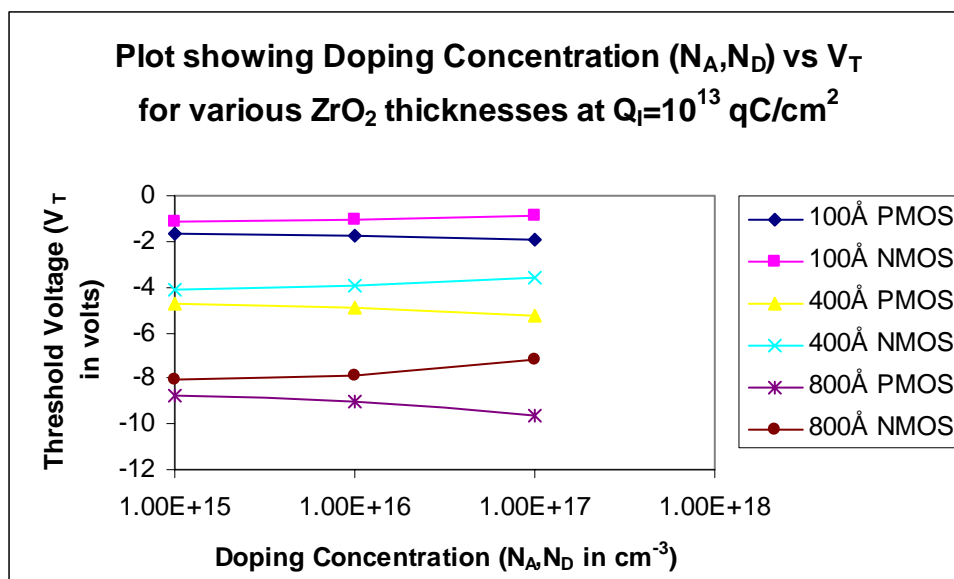


Figure 4.41 Plot showing Doping Concentration vs.  $V_T$  for various  $\text{ZrO}_2$  thicknesses at  $Q_i=10^{13}$   $\text{qC/cm}^2$

For the Al/ $\text{ZrO}_2$  system, now the doping concentration ( $N_A, N_D$ ) is held constant at  $10^{15}$   $\text{cm}^{-3}$ . Now by varying oxide thickness (initially 100Å, 400Å and 800Å), the threshold voltage is calculated and plotted against different values of interface trap charges ( $Q_i$ ) Fig 4.42. The above process of simulation is repeated by changing the doping concentrations from  $10^{16}$   $\text{cm}^{-3}$  to  $10^{17}$   $\text{cm}^{-3}$  are plotted in Fig 4.43 and 4.44 respectively. Threshold voltage values are low (-0.742V) for doping concentrations of  $10^{15}$   $\text{cm}^{-3}$  and  $10^{16}$   $\text{cm}^{-3}$  for all oxide thicknesses for PMOS devices. The  $V_T$  values are low in the range of -0.098V to 0.432V for doping concentrations of  $10^{15}$   $\text{cm}^{-3}$ ,  $10^{16}$   $\text{cm}^{-3}$  and  $10^{17}$   $\text{cm}^{-3}$  for all oxide thicknesses for NMOS devices.

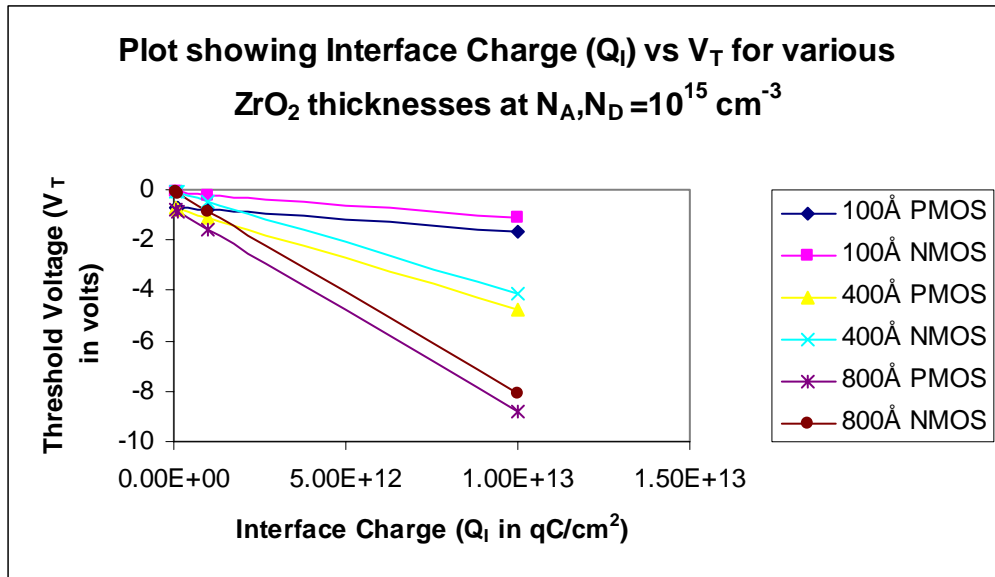


Figure 4.42 Plot showing  $V_T$  vs.  $Q_i$  for various  $ZrO_2$  thicknesses at  $N_A, N_D = 10^{15} \text{ cm}^{-3}$

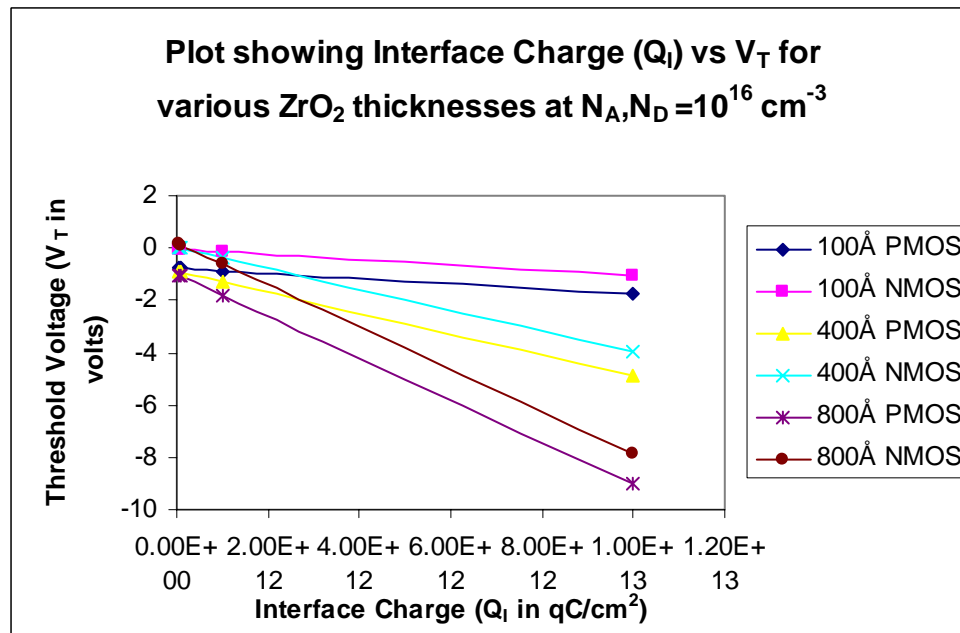


Figure 4.43 Plot showing  $V_T$  vs.  $Q_i$  for various  $ZrO_2$  thicknesses at  $N_A, N_D = 10^{16} \text{ cm}^{-3}$



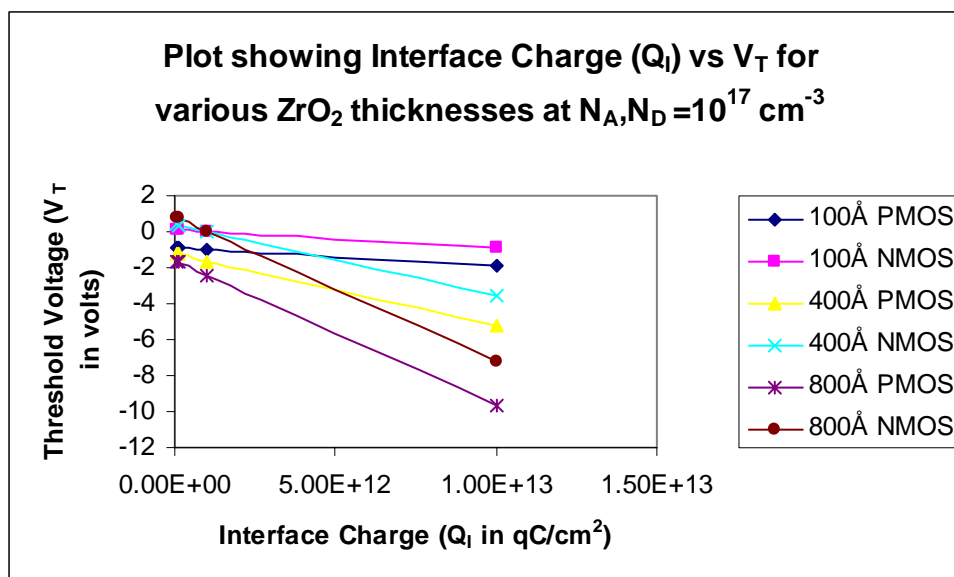


Figure 4.44 Plot showing  $V_T$  vs.  $Q_i$  for various  $ZrO_2$  thicknesses at  $N_A, N_D = 10^{17} \text{ cm}^{-3}$

## 4.2 MOSFETS with ruthenium as gate metal

The need to improve threshold voltage for PMOS and NMOS devices has lead to study Ruthenium as gate metal in substitution for usage of aluminum. The metal work function of ruthenium is 4.71eV. The study involved hafnium oxide and aluminum oxide based MOSFETs with ruthenium as gate metal.

### 4.2.1 Ru/HfO<sub>2</sub> based MOSFET

In the present work, the effect of interface trap charges, doping concentration, and oxide thickness on the  $V_T$  were studied. Several variations of the above physical parameters were used to calculate the  $V_T$  for NMOS and PMOS devices. In the first case, simulations were performed using ruthenium as gate metal and hafnium oxide as gate oxide for PMOS and NMOS field

effect transistors. Firstly the interface trap charge is kept at  $5 \cdot 10^{10} \text{ qC/cm}^2$ . The doping concentration ( $N_A, N_D$ ) is varied from  $5 \cdot 10^{14} \text{ cm}^{-3}$ ,  $10^{15} \text{ cm}^{-3}$ ,  $5 \cdot 10^{15} \text{ cm}^{-3}$ ,  $10^{16} \text{ cm}^{-3}$ ,  $5 \cdot 10^{16} \text{ cm}^{-3}$  and  $10^{17} \text{ cm}^{-3}$  respectively. The oxide thickness ( $T_{OX}$ ) is varied from  $50 \text{ \AA}$ ,  $100 \text{ \AA}$ ,  $200 \text{ \AA}$ ,  $400 \text{ \AA}$ ,  $600 \text{ \AA}$ ,  $800 \text{ \AA}$  and  $1000 \text{ \AA}$  respectively. Next, the interface trap charge ( $Q_I$ ) is varied from  $10^{11} \text{ qC/cm}^2$ ,  $5 \cdot 10^{11} \text{ qC/cm}^2$ ,  $10^{12} \text{ qC/cm}^2$ ,  $5 \cdot 10^{12} \text{ qC/cm}^2$  and  $10^{13} \text{ qC/cm}^2$  respectively. The above  $V_T$  calculations were repeated for all doping concentrations and oxide thicknesses. The threshold voltages vs. oxide thickness for various doping concentrations at constant interface trap charge ( $Q_I = 5 \cdot 10^{10} \text{ qC/cm}^2$ ) are plotted. While the oxide thickness is varied for a range of values, the values of interest are in the category of thin, medium and thick oxides. For this thicknesses selected are  $100 \text{ \AA}$ ,  $400 \text{ \AA}$  and  $800 \text{ \AA}$ . The above process of simulations were repeated by changing the interface trap density ( $Q_I$ ) from  $10^{11} \text{ qC/cm}^2$  to  $10^{13} \text{ qC/cm}^2$  which are plotted in Fig 4.45, 4.46, 4.47 and 4.48 respectively. The simulated results show that threshold voltage is low for both PMOS ( $-0.168 \text{ V}$  to  $-0.934 \text{ V}$ ) and NMOS ( $0.38 \text{ V}$  to  $0.535 \text{ V}$ ) for various doping concentrations at different interface charges. At interface charge of  $10^{13} \text{ qC/cm}^2$  threshold voltage is too high ( $-7.229 \text{ V}$  and  $-5.122 \text{ V}$ ) for PMOS and NMOS devices.

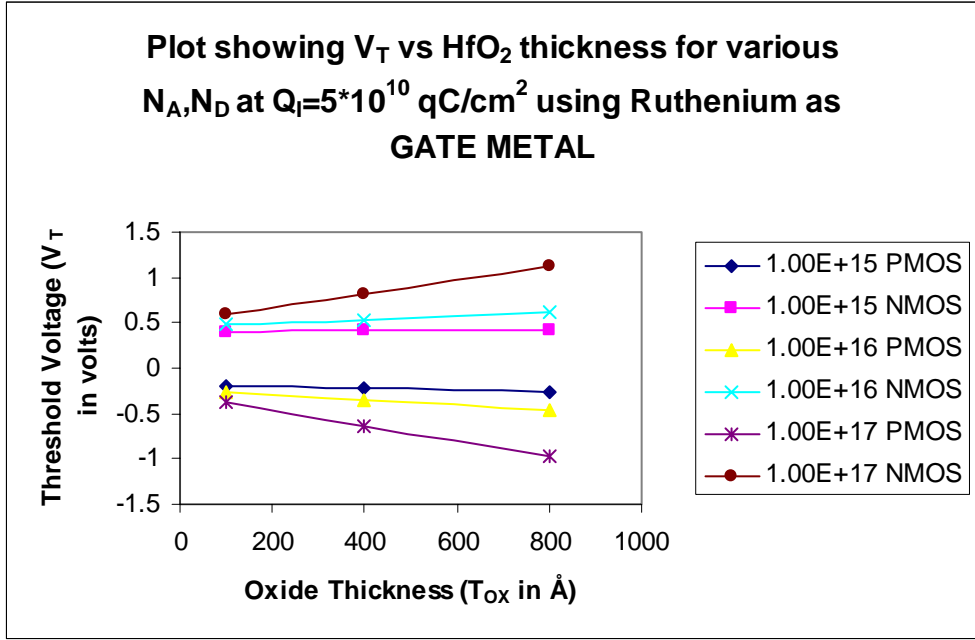


Figure 4.45 Plot showing  $V_T$  vs.  $\text{HfO}_2$  thickness for various  $N_A, N_D$  at  $Q_I=5 \times 10^{10} \text{ qC/cm}^2$  with Ruthenium as gate metal

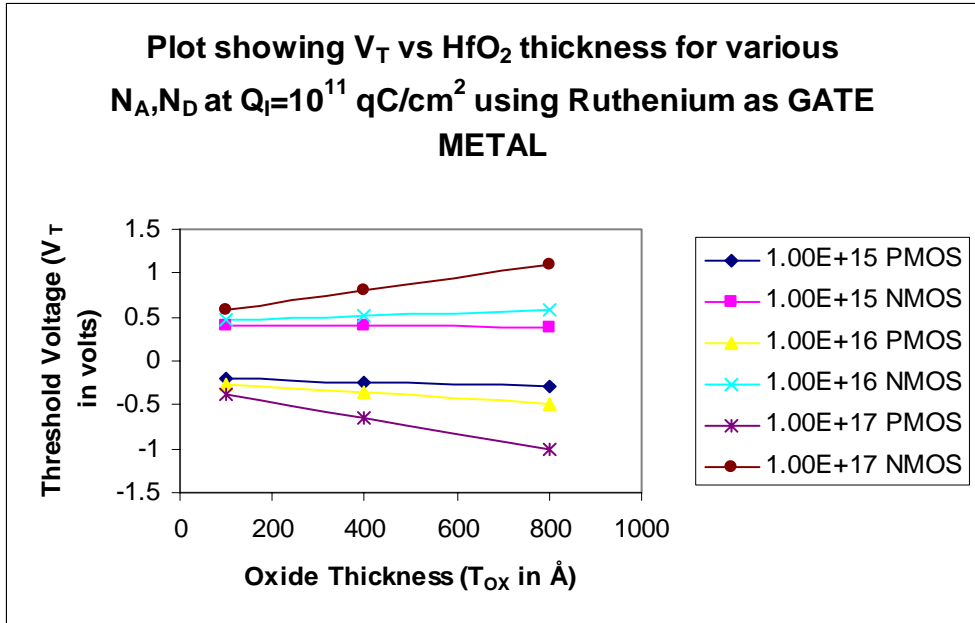


Figure 4.46 Plot showing  $V_T$  vs.  $\text{HfO}_2$  thickness for various  $N_A, N_D$  at  $Q_I=10^{11} \text{ qC/cm}^2$  with Ruthenium as gate metal

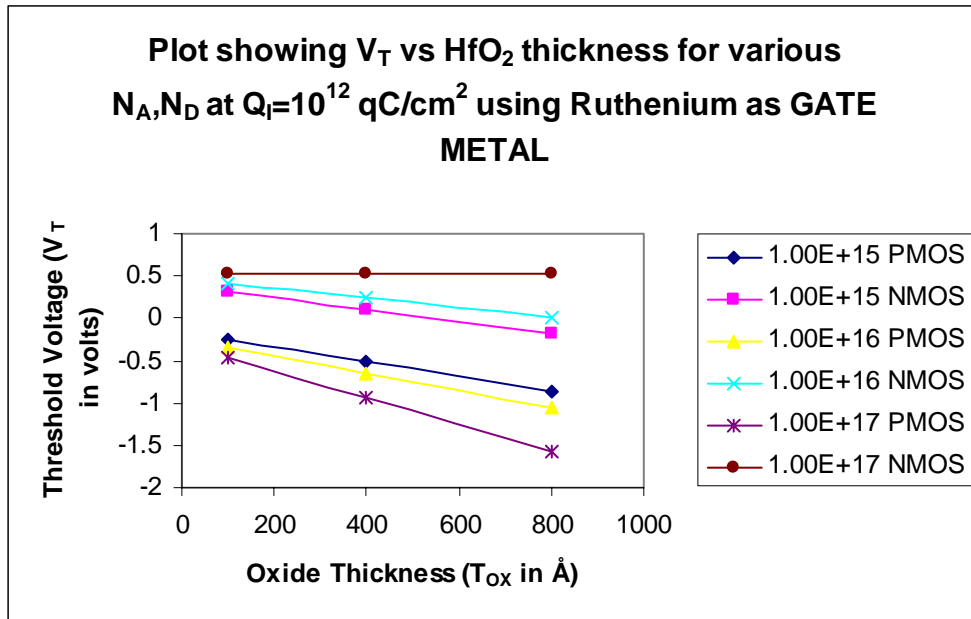


Figure 4.47 Plot showing  $V_T$  vs.  $HfO_2$  thickness for various  $N_A, N_D$  at  $Q_f=10^{12} \text{ qC/cm}^2$  with Ruthenium as gate metal

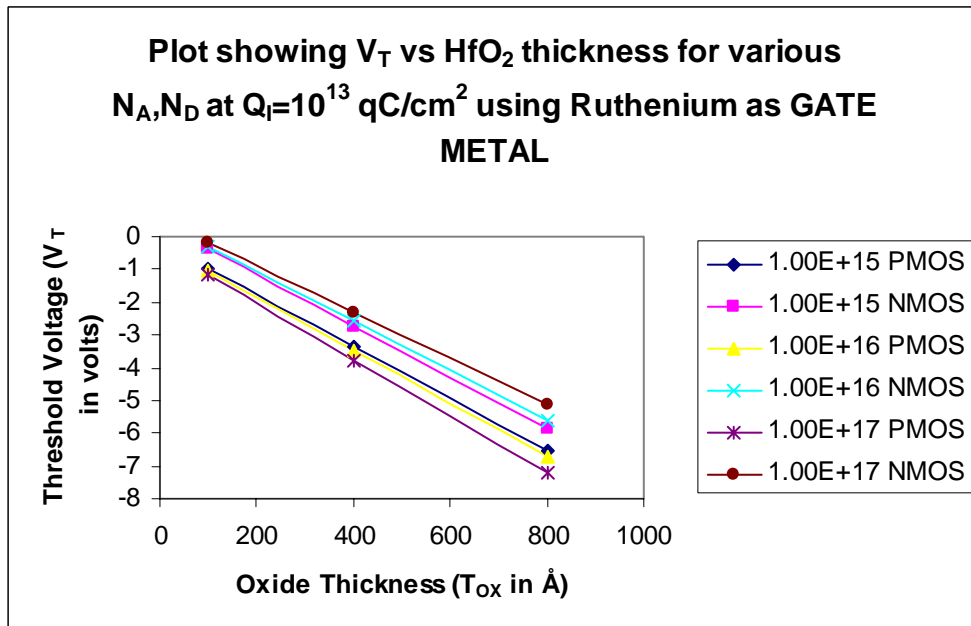


Figure 4.48 Plot showing  $V_T$  vs.  $HfO_2$  thickness for various  $N_A, N_D$  at  $Q_f=10^{13} \text{ qC/cm}^2$  with Ruthenium as gate metal

For the Ru/HfO<sub>2</sub> system, the interface trap charge ( $Q_I$ ) is kept constant at  $5 \cdot 10^{10}$  qC/cm<sup>2</sup>. Now by varying oxide thickness (initially 100Å, 400Å and 800Å), the threshold voltage is calculated and plotted against doping concentrations ( $N_A$ ,  $N_D$ ). The above process of simulation is repeated by varying the interface trap charges from  $10^{11}$  qC/cm<sup>2</sup> to  $10^{13}$  qC/cm<sup>2</sup> and is plotted in Fig 4.49, 4.50, 4.51 and 4.52 respectively. The oxide thicknesses 100Å, 400Å, 800Å at all interface charges except at  $10^{13}$  qC/cm<sup>2</sup> gives low threshold voltage for both NMOS and PMOS devices.

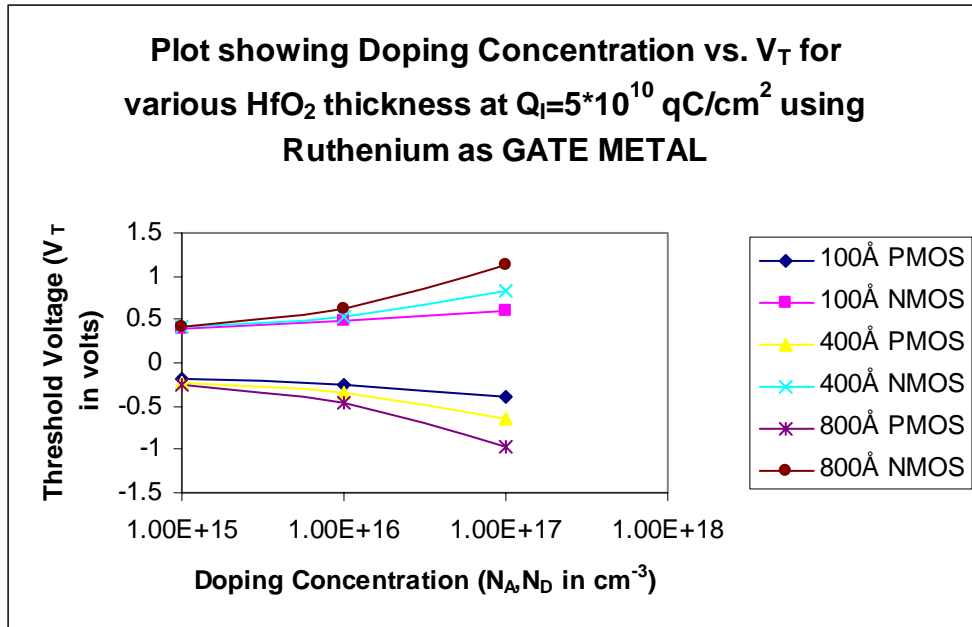


Figure 4.49 Plot showing Doping Concentration vs.  $V_T$  for various HfO<sub>2</sub> thickness at  $Q_I=5 \cdot 10^{10}$  qC/cm<sup>2</sup> with Ruthenium as gate metal

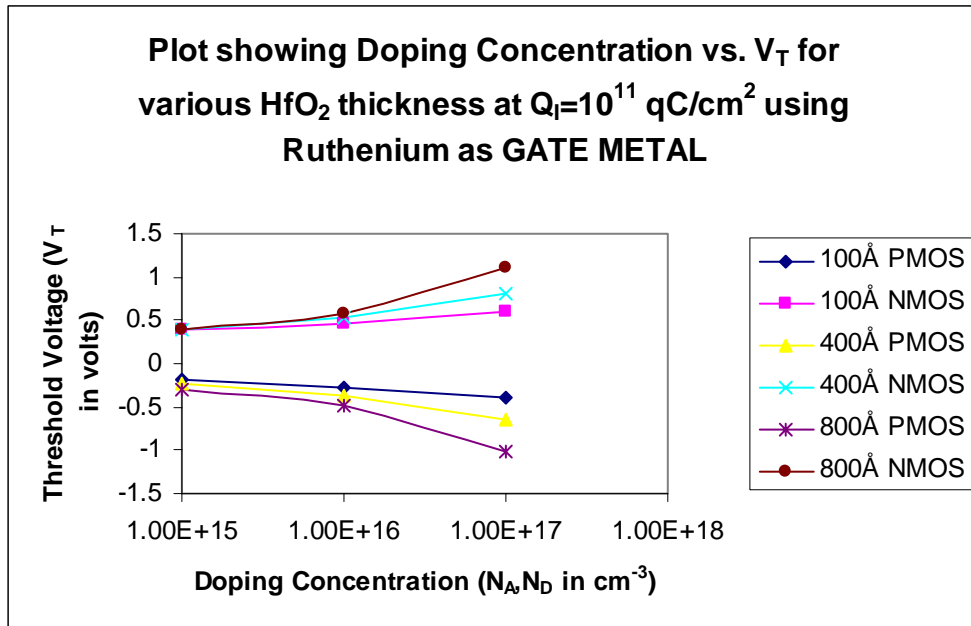


Figure 4.50 Plot showing Doping Concentration vs.  $V_T$  for various  $\text{HfO}_2$  thickness at  $Q_f=10^{11}$  qC/cm<sup>2</sup> with Ruthenium as gate metal

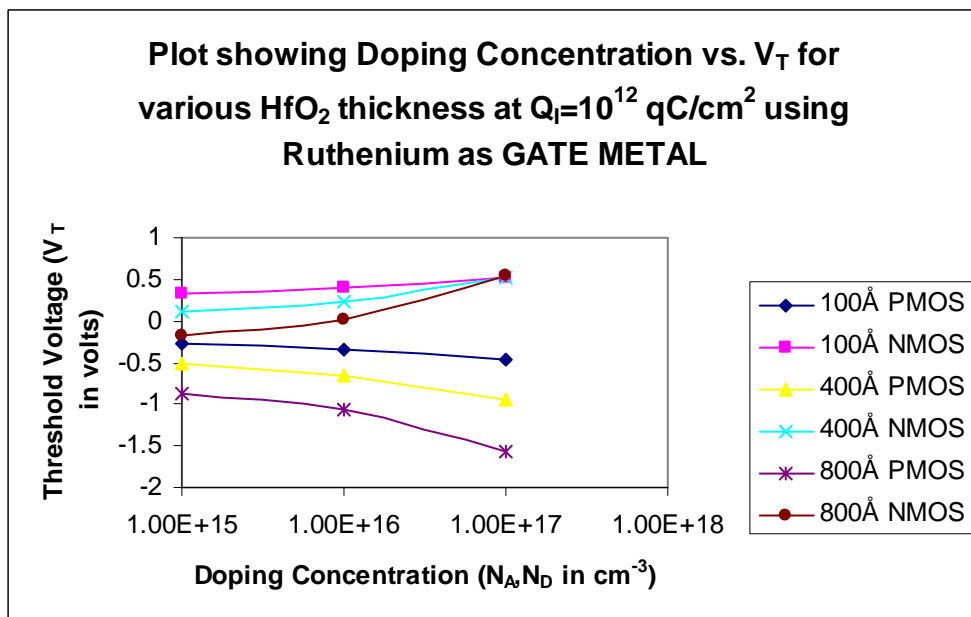


Figure 4.51 Plot showing Doping Concentration vs.  $V_T$  for various  $\text{HfO}_2$  thickness at  $Q_f=10^{12}$  qC/cm<sup>2</sup> with Ruthenium as gate metal

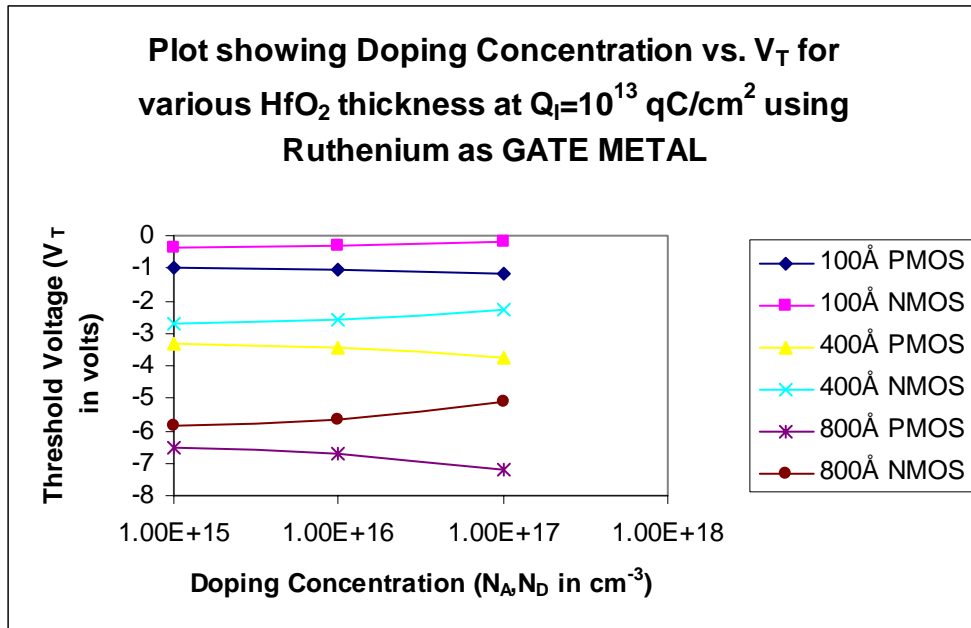


Figure 4.52 Plot showing Doping Concentration vs.  $V_T$  for various  $\text{HfO}_2$  thickness at  $Q_I=10^{13}$   $\text{qC}/\text{cm}^2$  with Ruthenium as gate metal

For the Ru/ $\text{HfO}_2$  system, the doping concentration ( $N_A, N_D$ ) is held constant at  $10^{15} \text{ cm}^{-3}$ . Now by varying oxide thickness (initially 100Å, 400Å and 800Å), the threshold voltage is calculated and plotted against different values of interface trap charges ( $Q_I$ ) Fig 4.53. The above process of simulation is repeated by changing the doping concentrations from  $10^{16} \text{ cm}^{-3}$  to  $10^{17} \text{ cm}^{-3}$  are plotted in Fig 4.54 and 4.55 respectively. The threshold voltage is low for doping concentrations of  $10^{15} \text{ cm}^{-3}$ ,  $10^{16} \text{ cm}^{-3}$ ,  $10^{17} \text{ cm}^{-3}$  and oxide thicknesses 100Å, 400Å, 800Å for PMOS and NMOS devices.

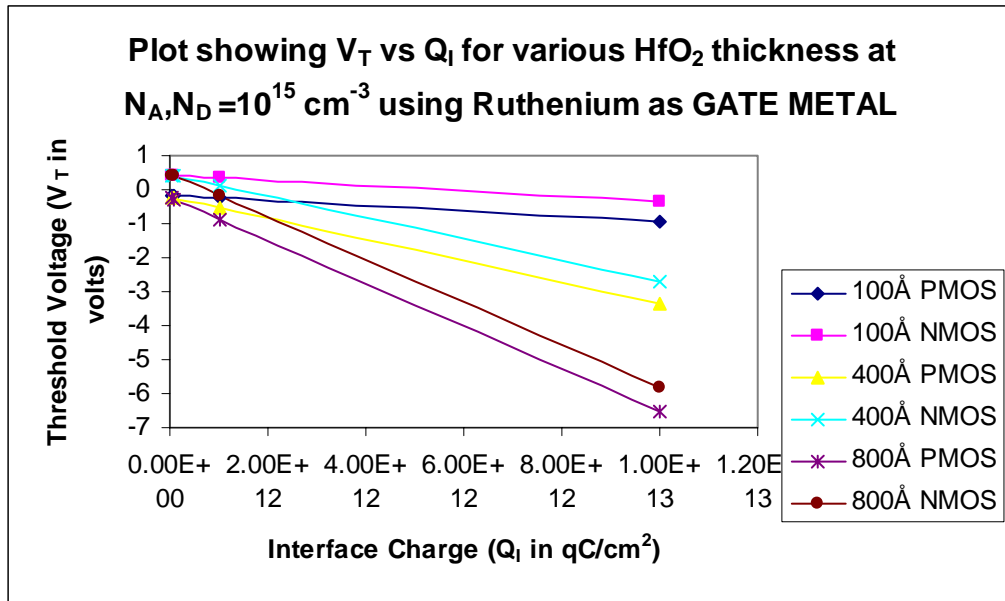


Figure 4.53 Plot showing  $V_T$  vs.  $Q_I$  for various  $HfO_2$  thickness at  $N_A, N_D = 10^{15} \text{ cm}^{-3}$  with Ruthenium as gate metal

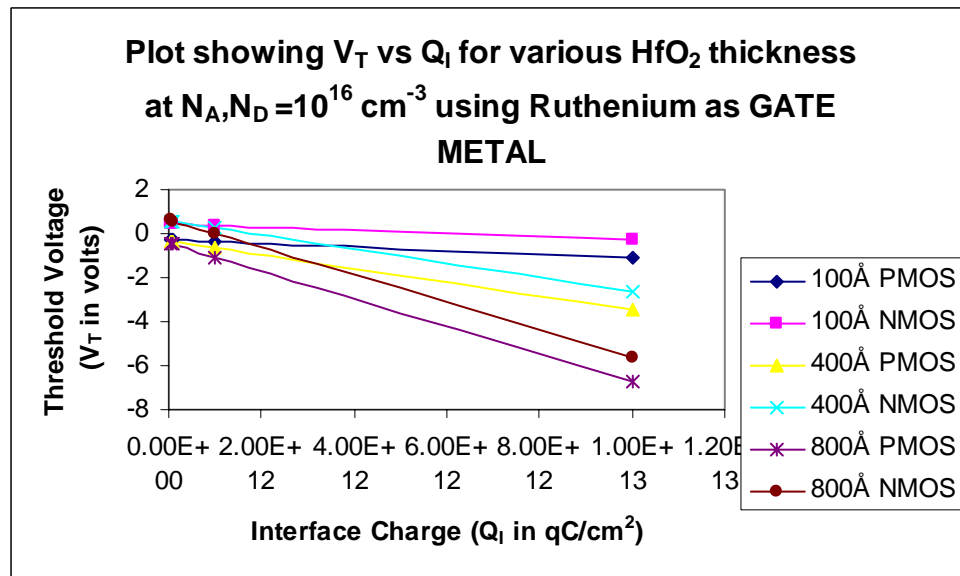


Figure 4.54 Plot showing  $V_T$  vs.  $Q_I$  for various  $HfO_2$  thickness at  $N_A, N_D = 10^{16} \text{ cm}^{-3}$  with Ruthenium as gate metal



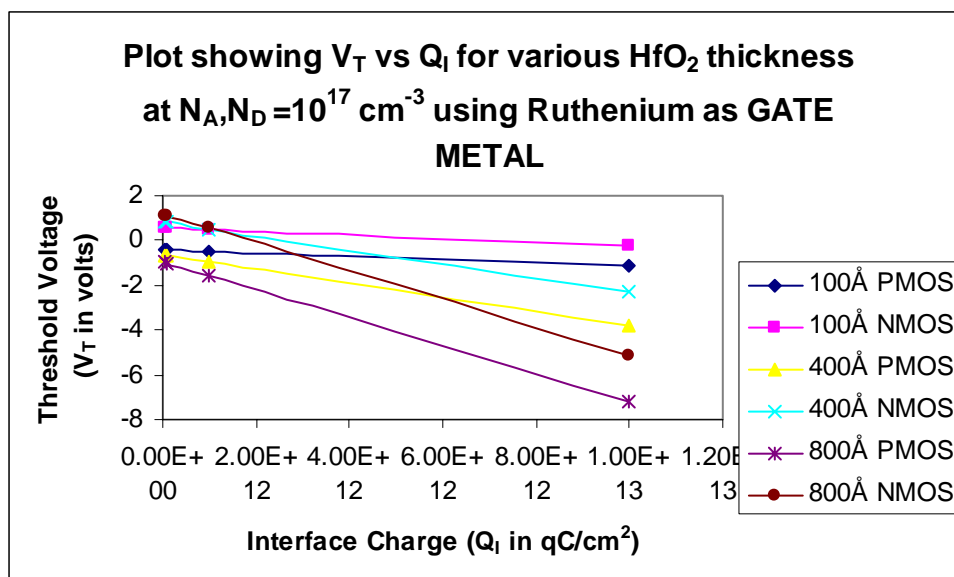


Figure 4.55 Plot showing  $V_T$  vs.  $Q_I$  for various  $HfO_2$  thickness at  $N_A, N_D=10^{17} \text{ cm}^{-3}$  with Ruthenium as gate metal

#### 4.2.2 Ru/ $Al_2O_3$ based MOSFET

In the first case, the work focused on using ruthenium as gate metal and aluminum oxide as gate oxide for PMOS and NMOS field effect transistors. Firstly the interface trap charge is kept at  $5 \times 10^{10} \text{ qC/cm}^2$ . The doping concentration ( $N_A, N_D$ ) is varied from  $5 \times 10^{14} \text{ cm}^{-3}$ ,  $10^{15} \text{ cm}^{-3}$ ,  $5 \times 10^{15} \text{ cm}^{-3}$ ,  $10^{16} \text{ cm}^{-3}$ ,  $5 \times 10^{16} \text{ cm}^{-3}$  and  $10^{17} \text{ cm}^{-3}$  respectively. The oxide thickness ( $T_{OX}$ ) is varied from 50Å, 100Å, 200Å, 400Å, 600Å, 800Å and 1000Å respectively. Next, the interface trap charge ( $Q_I$ ) is varied from  $10^{11} \text{ qC/cm}^2$ ,  $5 \times 10^{11} \text{ qC/cm}^2$ ,  $10^{12} \text{ qC/cm}^2$ ,  $5 \times 10^{12} \text{ qC/cm}^2$  and  $10^{13} \text{ qC/cm}^2$ . The above  $V_T$  calculations were repeated for all doping concentrations and oxide thicknesses. The threshold voltages vs. oxide thickness for various doping concentrations at constant interface trap charge ( $Q_I=5 \times 10^{10} \text{ qC/cm}^2$ ) are plotted. While the oxide thickness is

varied for a range of values, the values of interest are in the category of thin, medium and thick oxides. For this thicknesses selected are 100Å, 400Å and 800Å. The above process of simulation were repeated by changing the interface trap charge ( $Q_I$ ) from  $10^{11}$  qC/cm<sup>2</sup> to  $10^{13}$  qC/cm<sup>2</sup> which are plotted in Fig 4.56, 4.57, 4.58 and 4.59 respectively. The threshold voltage becomes very low for ruthenium as gate metal compared to using aluminum as gate metal for aluminum oxide based MOS device. The  $V_T$  was found to be low (-0.202V and -0.312V) for PMOS devices for various doping concentrations of  $10^{15}$  cm<sup>-3</sup>,  $10^{16}$  cm<sup>-3</sup> for various oxide thicknesses with interface charge  $5 \cdot 10^{10}$  qC/cm<sup>2</sup> and  $10^{11}$  qC/cm<sup>2</sup>. For NMOS devices the  $V_T$  is low (-0.923V to 0.549V) for various doping concentrations having  $5 \cdot 10^{10}$  qC/cm<sup>2</sup>,  $10^{11}$  qC/cm<sup>2</sup> and  $10^{12}$  qC/cm<sup>2</sup> interface charges. At  $10^{17}$  cm<sup>-3</sup> doping concentration with interface charges  $5 \cdot 10^{10}$  qC/cm<sup>2</sup> and  $10^{11}$  qC/cm<sup>2</sup> having oxide thicknesses 400Å and 800Å the  $V_T$  was found to be very high (1.933V).

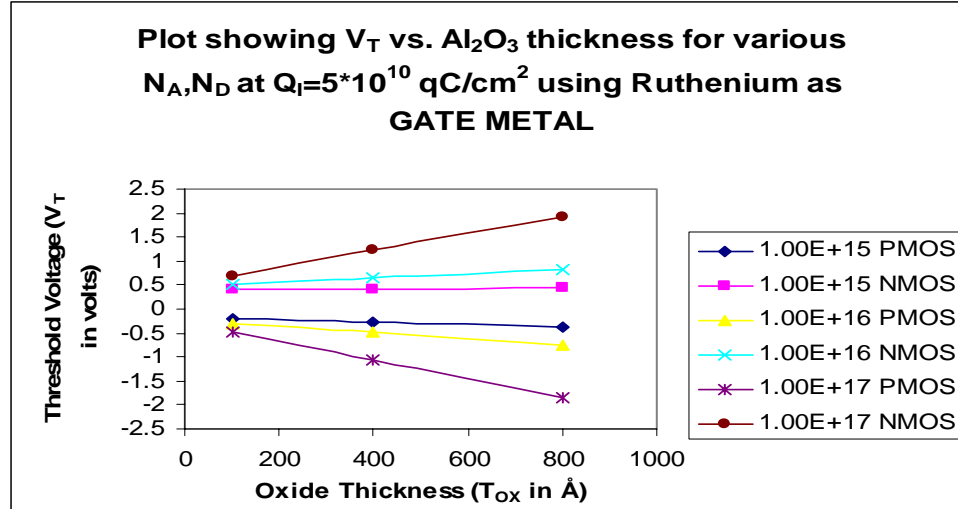


Figure 4.56 Plot showing  $V_T$  vs.  $Al_2O_3$  thickness for various  $N_A$ ,  $N_D$  at  $Q_I=5 \cdot 10^{10}$  qC/cm<sup>2</sup> with Ruthenium as gate metal

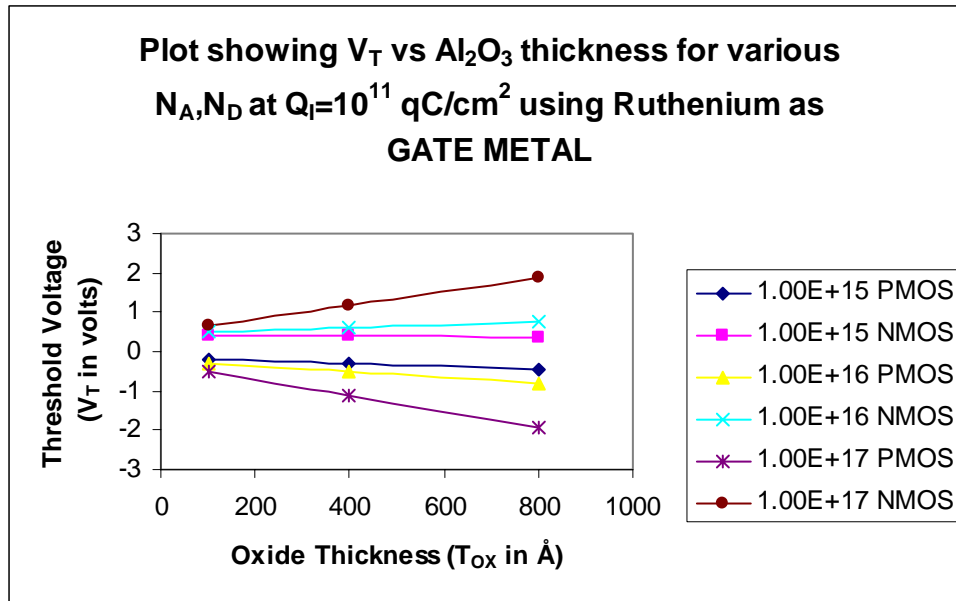


Figure 4.57 Plot showing  $V_T$  vs.  $Al_2O_3$  thickness for various  $N_A, N_D$  at  $Q_f=10^{11}$  qC/cm<sup>2</sup> with Ruthenium as gate metal

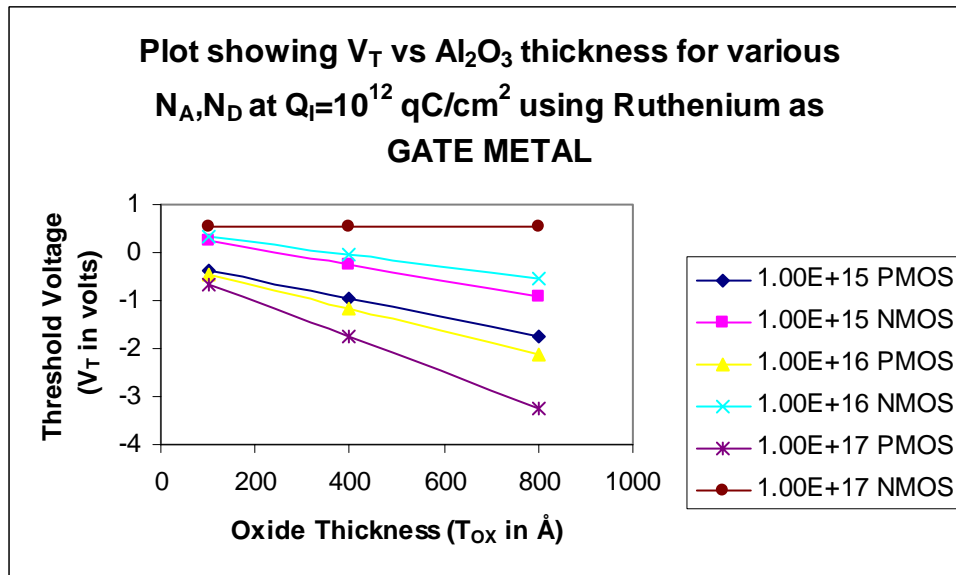


Figure 4.58 Plot showing  $V_T$  vs.  $Al_2O_3$  thickness for various  $N_A, N_D$  at  $Q_f=10^{12}$  qC/cm<sup>2</sup> with Ruthenium as gate metal

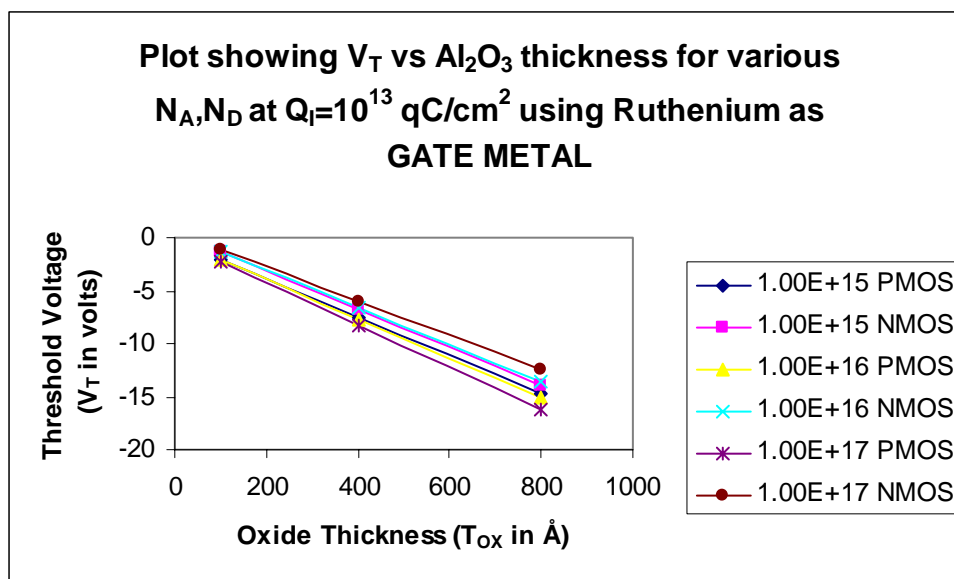


Figure 4.59 Plot showing  $V_T$  vs.  $Al_2O_3$  thickness for various  $N_A, N_D$  at  $Q_I=10^{13} \text{ qC/cm}^2$  with Ruthenium as gate metal

For the Ru/ $Al_2O_3$  system, the interface trap charge ( $Q_I$ ) is kept constant at  $5 \cdot 10^{10} \text{ qC/cm}^2$ . Now by varying oxide thickness (initially  $100 \text{ \AA}$ ,  $400 \text{ \AA}$  and  $800 \text{ \AA}$ ), the threshold voltage is calculated and plotted for various doping concentrations ( $N_A, N_D$ ). The above process of simulation is repeated by changing the interface trap charges from  $10^{11} \text{ qC/cm}^2$  to  $10^{13} \text{ qC/cm}^2$  and are plotted in Fig 4.60, 4.61, 4.62 and 4.63 respectively.  $V_T$  values were found to be low ( $-0.202 \text{ V}$  and  $0.404 \text{ V}$ ) for PMOS and NMOS devices having oxide thicknesses  $100 \text{ \AA}$ ,  $400 \text{ \AA}$ ,  $800 \text{ \AA}$  and interface trap charges of  $5 \cdot 10^{10} \text{ qC/cm}^2$  and  $10^{11} \text{ qC/cm}^2$ .

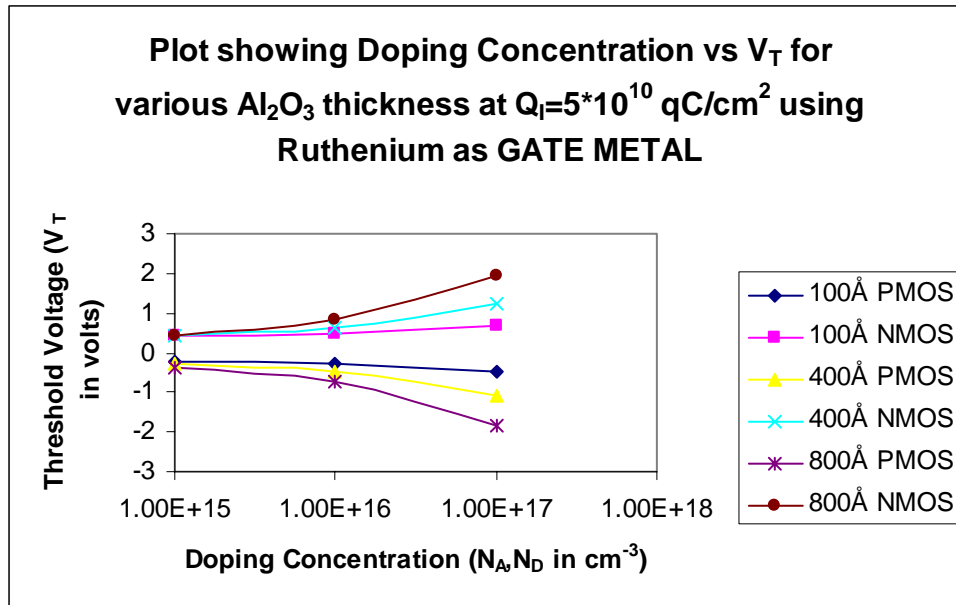


Figure 4.60 Plot showing Doping Concentration vs.  $V_T$  for various  $\text{Al}_2\text{O}_3$  thickness at  $Q_i=5 \cdot 10^{10}$  qC/cm<sup>2</sup> with Ruthenium as gate metal

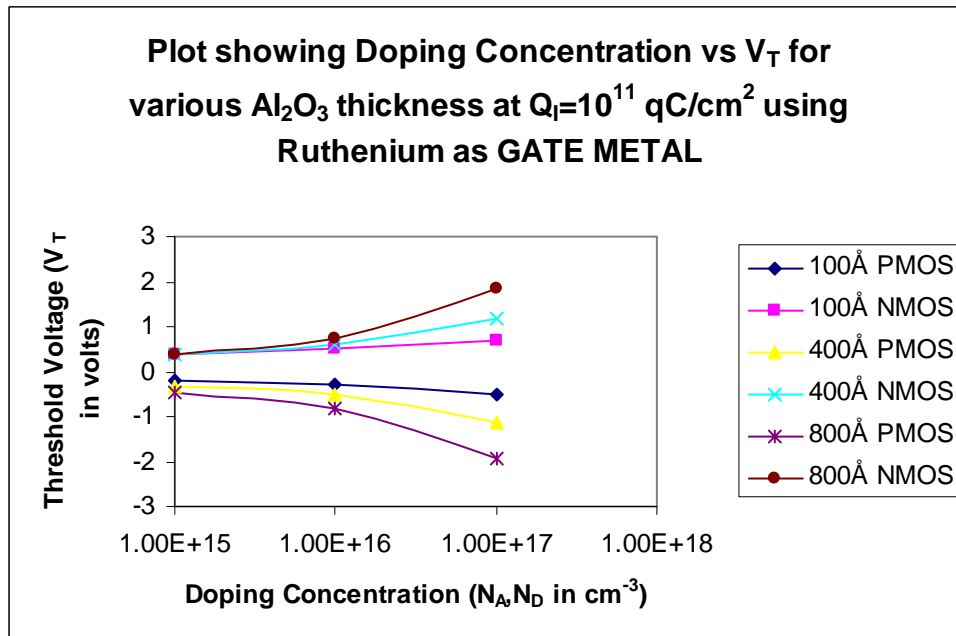


Figure 4.61 Plot showing Doping Concentration vs.  $V_T$  for various  $\text{Al}_2\text{O}_3$  thickness at  $Q_i=10^{11}$  qC/cm<sup>2</sup> with Ruthenium as gate metal

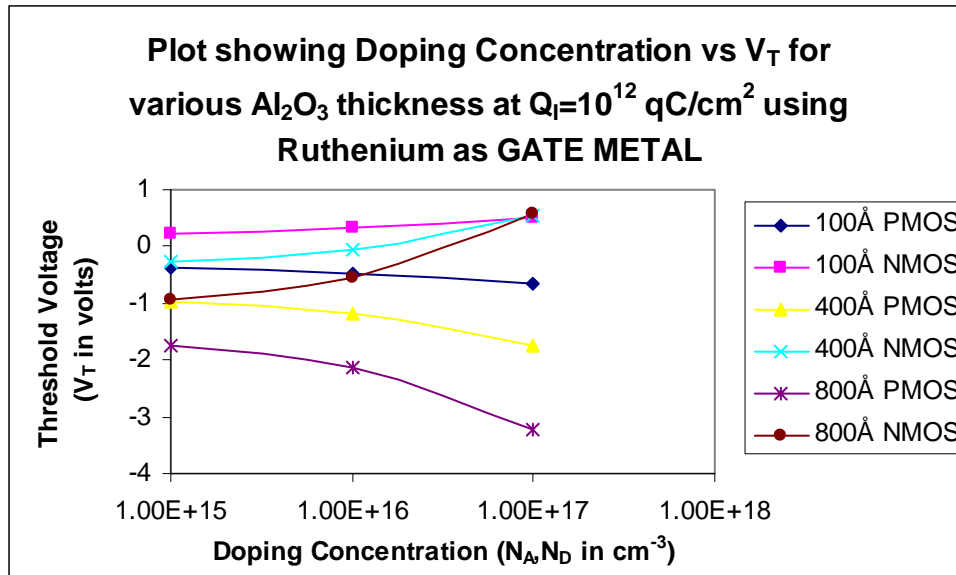


Figure 4.62 Plot showing Doping Concentration vs.  $V_T$  for various  $\text{Al}_2\text{O}_3$  thickness at  $Q_f=10^{12}$  qC/cm<sup>2</sup> with Ruthenium as gate metal

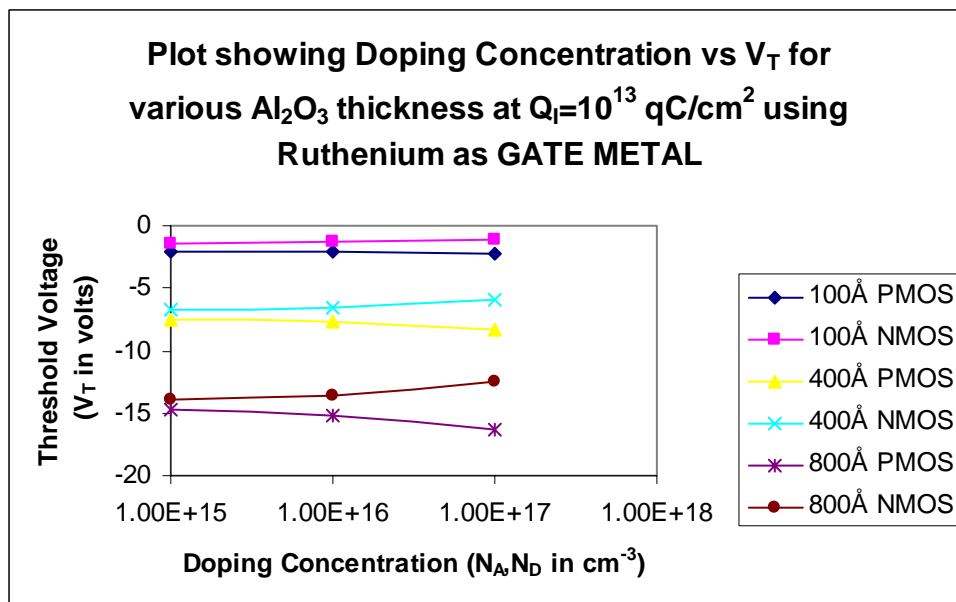


Figure 4.63 Plot showing Doping Concentration vs.  $V_T$  for various  $\text{Al}_2\text{O}_3$  thickness at  $Q_f=10^{13}$  qC/cm<sup>2</sup> with Ruthenium as gate metal

For the Ru/Al<sub>2</sub>O<sub>3</sub> system, the doping concentration ( $N_A$ ,  $N_D$ ) is held constant at  $10^{15} \text{ cm}^{-3}$ . Now by varying oxide thickness (initially 100Å, 400Å and 800Å), the threshold voltage is calculated and plotted against different values of interface trap charges ( $Q_I$ ) Fig 4.64. The above process of simulation is repeated by changing the doping concentrations from  $10^{16} \text{ cm}^{-3}$  to  $10^{17} \text{ cm}^{-3}$  are plotted in Fig 4.65 and 4.66 respectively. The threshold voltage values are found to be low (-0.405V and 0.552V) for PMOS and NMOS having doping concentration of  $10^{15} \text{ cm}^{-3}$ ,  $10^{16} \text{ cm}^{-3}$ ,  $10^{17} \text{ cm}^{-3}$  for interface charges  $5 \cdot 10^{10} \text{ qC/cm}^2$  and  $10^{11} \text{ qC/cm}^2$  for oxide thicknesses 100Å and 400Å.

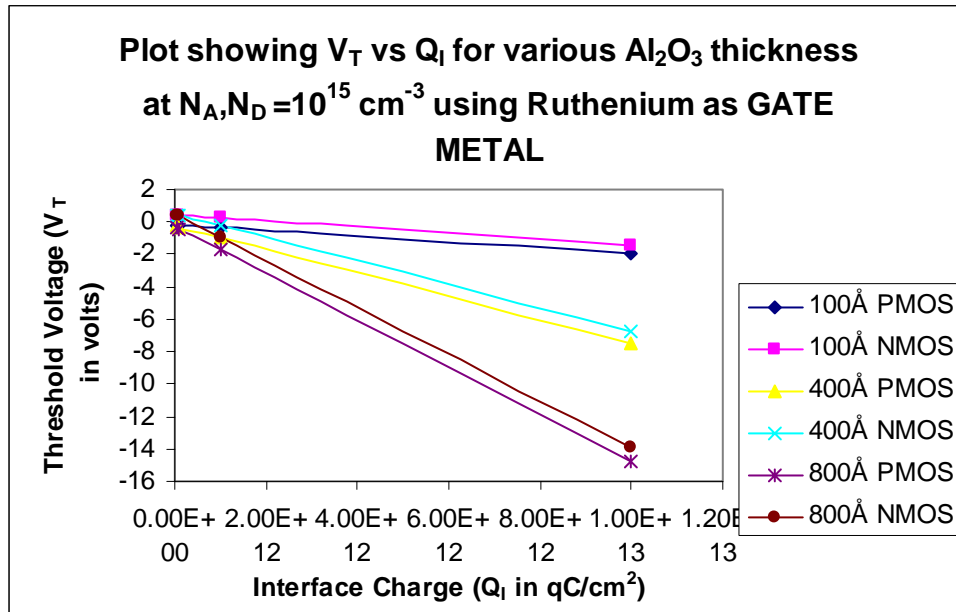


Figure 4.64 Plot showing  $V_T$  vs.  $Q_I$  for various  $\text{Al}_2\text{O}_3$  thickness at  $N_A, N_D = 10^{15} \text{ cm}^{-3}$  with Ruthenium as gate metal

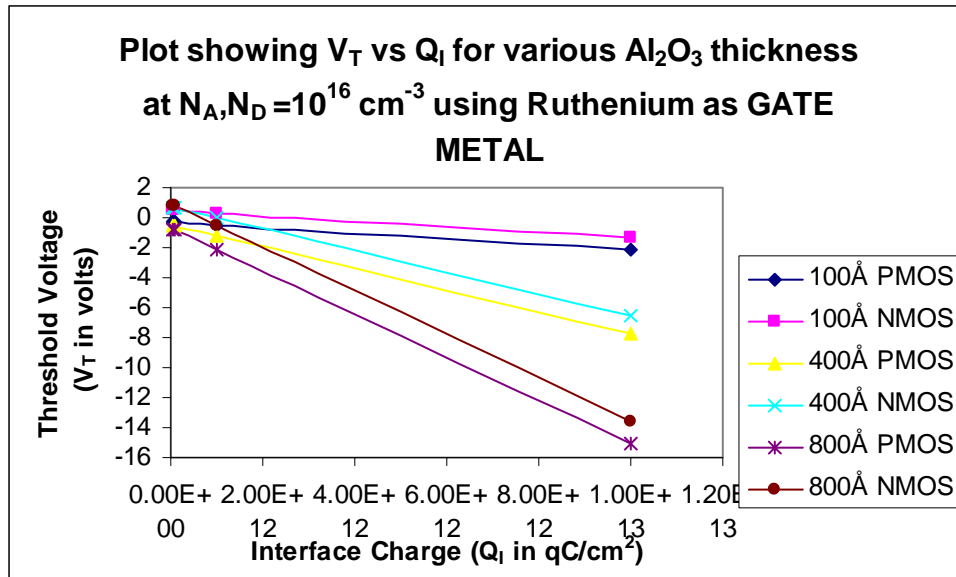


Figure 4.65 Plot showing  $V_T$  vs.  $Q_I$  for various  $Al_2O_3$  thickness at  $N_A, N_D = 10^{16} \text{ cm}^{-3}$  with Ruthenium as gate metal

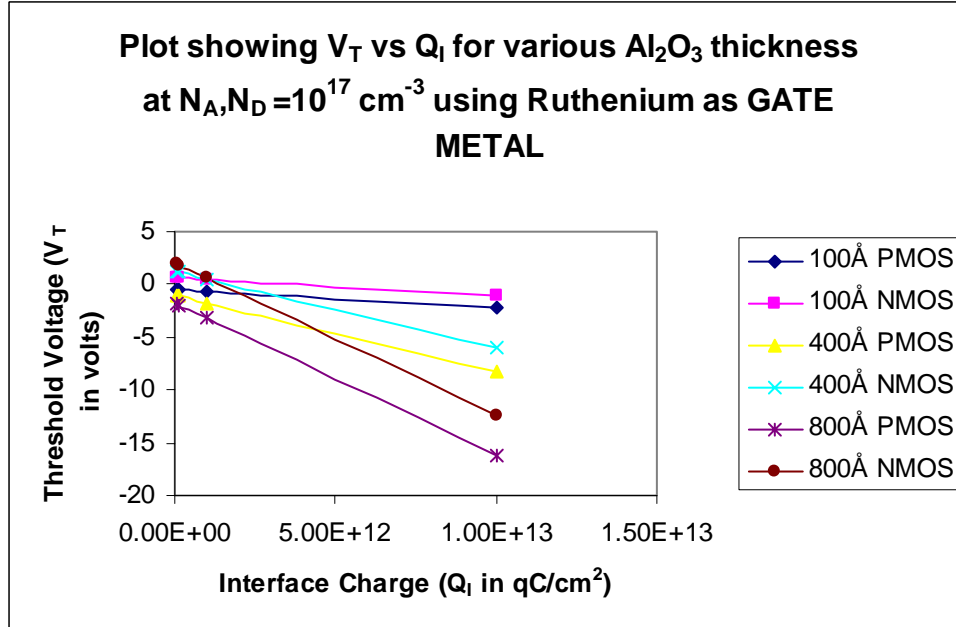


Figure 4.66 Plot showing  $V_T$  vs.  $Q_I$  for various  $Al_2O_3$  thickness at  $N_A, N_D = 10^{17} \text{ cm}^{-3}$  with Ruthenium as gate metal



### 4.3 MOSFETS with Pt-Ru alloy (4.9eV) as gate

Lot of research is going on alloys to replace existing metals as gate. The Pt-Ru alloy work function is chosen to be 4.9eV which is in between the work function of platinum and ruthenium metals.

#### 4.3.1 Pt-Ru alloy (4.9eV)/HfO<sub>2</sub> based MOSFET

In the present work, the effect of interface trap charges, doping concentration, and oxide thickness on the  $V_T$  were studied. Several variations of the above physical parameters were used to calculate the  $V_T$  for NMOS and PMOS devices. In the first case, simulations were performed using platinum-ruthenium alloy with work function of 4.9eV as gate and hafnium oxide as gate oxide for PMOS and NMOS field effect transistors. Firstly, the interface trap charge is kept at  $5 \times 10^{10}$  qC/cm<sup>2</sup>. The doping concentration ( $N_A, N_D$ ) is varied from  $5 \times 10^{14}$  cm<sup>-3</sup>,  $10^{15}$  cm<sup>-3</sup>,  $5 \times 10^{15}$  cm<sup>-3</sup>,  $10^{16}$  cm<sup>-3</sup>,  $5 \times 10^{16}$  cm<sup>-3</sup> and  $10^{17}$  cm<sup>-3</sup> respectively. The oxide thickness ( $T_{OX}$ ) is varied from 50Å, 100Å, 200Å, 400Å, 600Å, 800Å and 1000Å respectively. The interface trap charge ( $Q_I$ ) is varied from  $10^{11}$  qC/cm<sup>2</sup>,  $5 \times 10^{11}$  qC/cm<sup>2</sup> and  $10^{12}$  qC/cm<sup>2</sup> respectively. The interface charge  $10^{13}$  qC/cm<sup>2</sup> was not chosen because the simulations using ruthenium and aluminum showed threshold voltages to be high for those devices. The above  $V_T$  calculations were repeated for all doping concentrations and oxide thicknesses. The threshold voltages vs. oxide thickness for various doping concentrations at constant interface trap charge ( $Q_I = 5 \times 10^{10}$  qC/cm<sup>2</sup>) are plotted. While the oxide thickness is varied for a range of values, the values of interest are in the category of thin, medium and thick oxides. For this oxide thicknesses selected are 100Å, 400Å and 800Å. The above process of simulations were repeated by changing the interface trap charge ( $Q_I$ ) from

$10^{11}$  qC/cm<sup>2</sup> to  $10^{13}$  qC/cm<sup>2</sup> which are plotted in Fig 4.67, 4.68 and 4.69 respectively. The simulated results show that threshold voltages are low (0.61V and -0.267V) for both NMOS and PMOS devices for oxide thickness 100Å, 400Å, 800Å at interface charges  $5 \cdot 10^{10}$  qC/cm<sup>2</sup> and  $10^{11}$  qC/cm<sup>2</sup>.

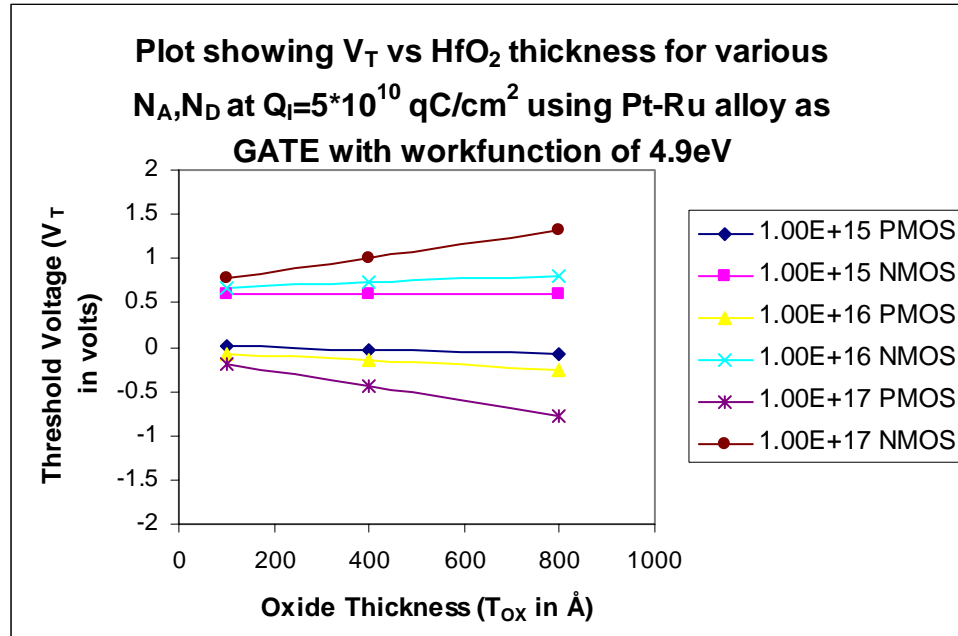


Figure 4.67 Plot showing  $V_T$  vs.  $HfO_2$  thickness for various  $N_A, N_D$  at  $Q_I = 5 \cdot 10^{10}$  qC/cm<sup>2</sup> using Pt-Ru alloy with work function 4.9eV as gate

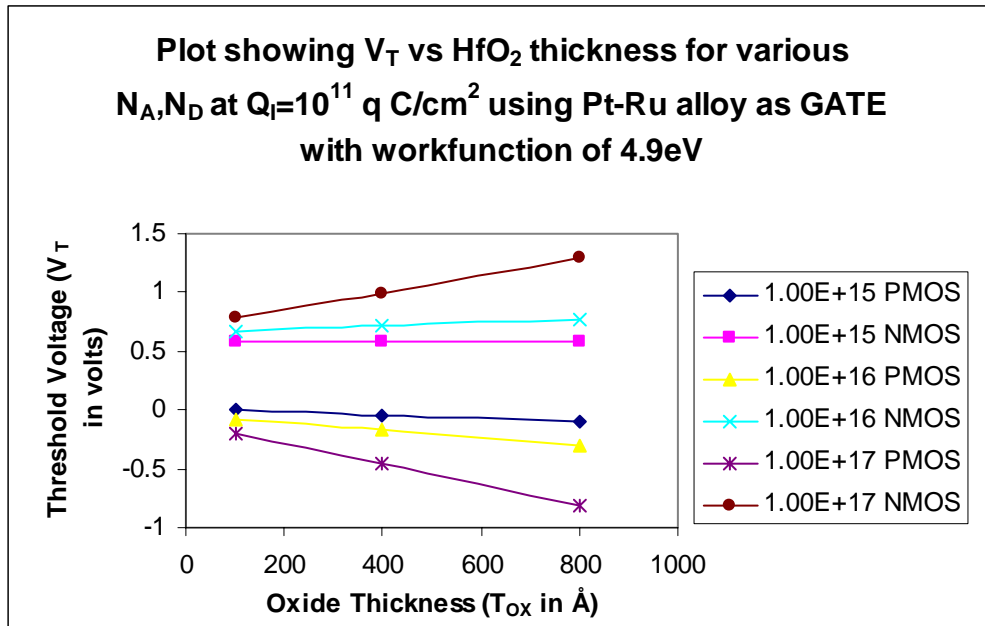


Figure 4.68 Plot showing  $V_T$  vs.  $HfO_2$  thickness for various  $N_A, N_D$  at  $Q_f=10^{11}$  qC/cm<sup>2</sup> using Pt-Ru alloy with work function 4.9eV as gate

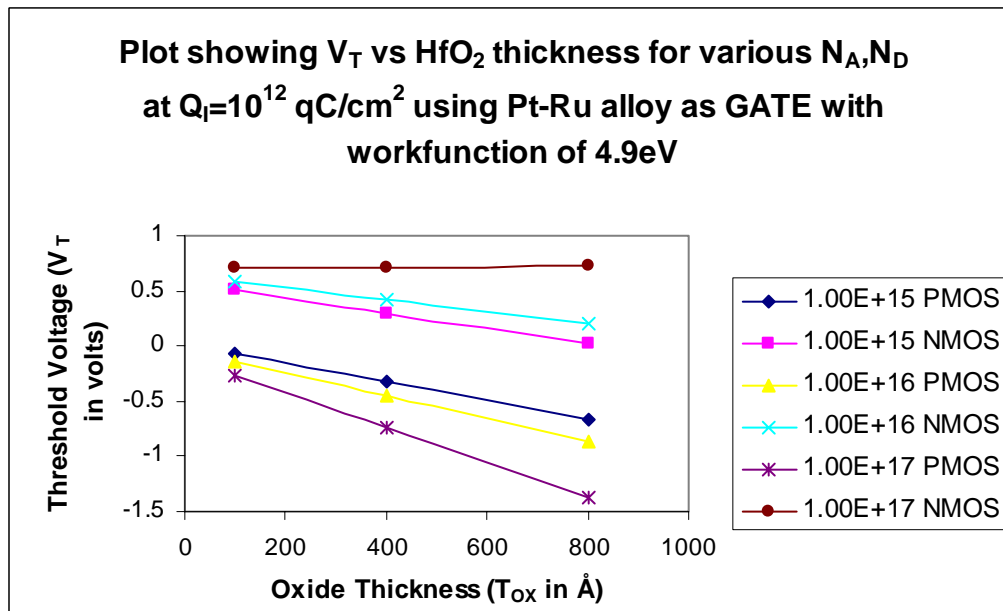


Figure 4.69 Plot showing  $V_T$  vs.  $HfO_2$  thickness for various  $N_A, N_D$  at  $Q_f=10^{12}$  qC/cm<sup>2</sup> using Pt-Ru alloy with work function 4.9eV as gate

For the Pt-Ru (4.9eV)/HfO<sub>2</sub> system, the interface trap charge (Q<sub>i</sub>) is kept constant at 5\*10<sup>10</sup> qC/cm<sup>2</sup>. Now by varying oxide thickness (initially 100Å, 400Å and 800Å), the threshold voltage is calculated and plotted for various doping concentrations (N<sub>A</sub>, N<sub>D</sub>). The above process of simulation is repeated by changing the interface trap charges from 5\*10<sup>10</sup> qC/cm<sup>2</sup> to 10<sup>12</sup> qC/cm<sup>2</sup> are plotted in Fig 4.70, 4.71 and 4.72 respectively. The simulations show threshold voltages to be low (-0.073V and 0.59V) for PMOS and NMOS devices for oxide thicknesses 100Å, 400Å, 800Å at interface charges 5\*10<sup>10</sup> qC/cm<sup>2</sup> and 10<sup>11</sup> qC/cm<sup>2</sup>. At interface trap charge of 10<sup>12</sup> qC/cm<sup>2</sup> the threshold voltage is too high.

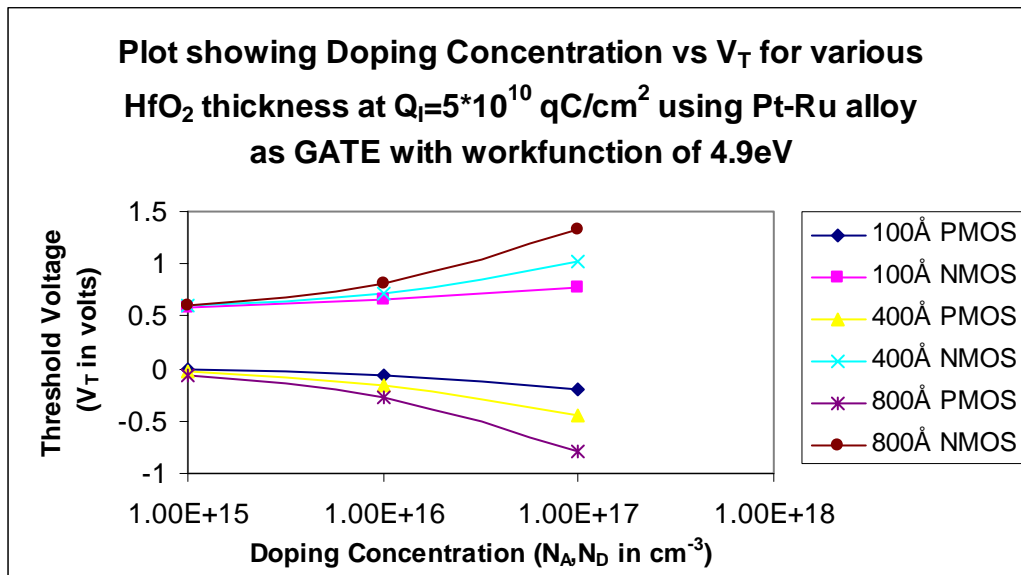


Figure 4.70 Plot showing Doping Concentration vs. V<sub>T</sub> for various HfO<sub>2</sub> thickness at Q<sub>i</sub>=5\*10<sup>10</sup> qC/cm<sup>2</sup> using Pt-Ru alloy with work function 4.9eV

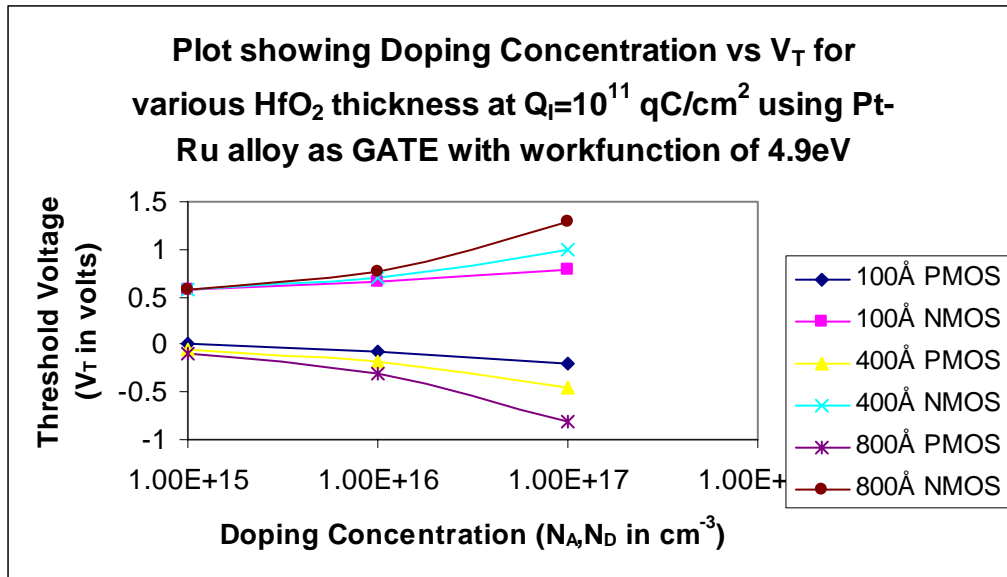


Figure 4.71 Plot showing Doping Concentration vs.  $V_T$  for various  $\text{HfO}_2$  thickness at  $Q_I=10^{11}$  qC/cm<sup>2</sup> using Pt-Ru alloy with work function 4.9eV

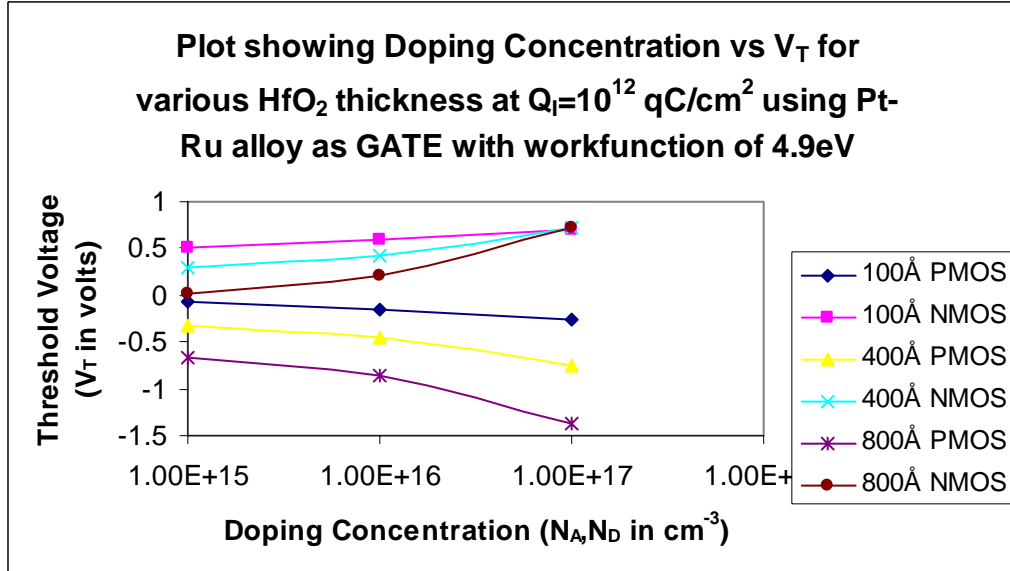


Figure 4.72 Plot showing Doping Concentration vs.  $V_T$  for various  $\text{HfO}_2$  thickness at  $Q_I=10^{12}$  qC/cm<sup>2</sup> using Pt-Ru alloy with work function 4.9eV

For the Pt-Ru (4.9eV)/HfO<sub>2</sub> system, the doping concentration ( $N_A$ ,  $N_D$ ) is held constant at  $10^{15} \text{ cm}^{-3}$ . Now by varying oxide thickness (initially 100Å, 400Å and 800Å), the threshold voltage is calculated and plotted against different values of interface trap charges ( $Q_I$ ) Fig 4.73. The above process of simulation is repeated by changing the doping concentrations from  $10^{16} \text{ cm}^{-3}$  to  $10^{17} \text{ cm}^{-3}$  which are plotted in Fig 4.74 and 4.75 respectively. The doping concentrations  $10^{15} \text{ cm}^{-3}$ ,  $10^{16} \text{ cm}^{-3}$  and  $10^{17} \text{ cm}^{-3}$  gives low threshold voltages for various oxide thicknesses except at interface charge of  $10^{17} \text{ cm}^{-3}$  for oxide thickness 800Å is very high.

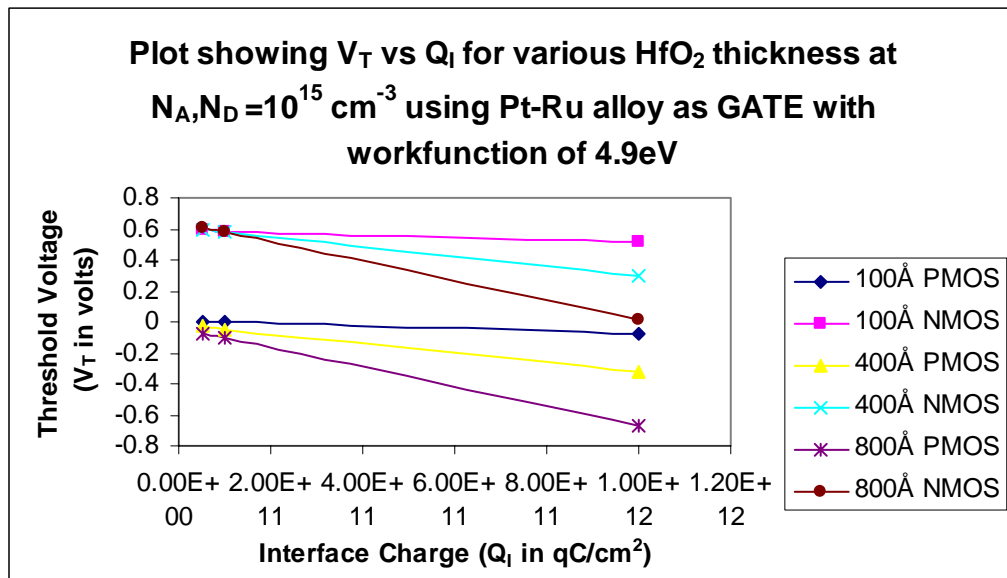


Figure 4.73 Plot showing  $V_T$  vs.  $Q_I$  for various HfO<sub>2</sub> thickness at  $N_A$ ,  $N_D = 10^{15} \text{ cm}^{-3}$  using Pt-Ru alloy with work function 4.9eV

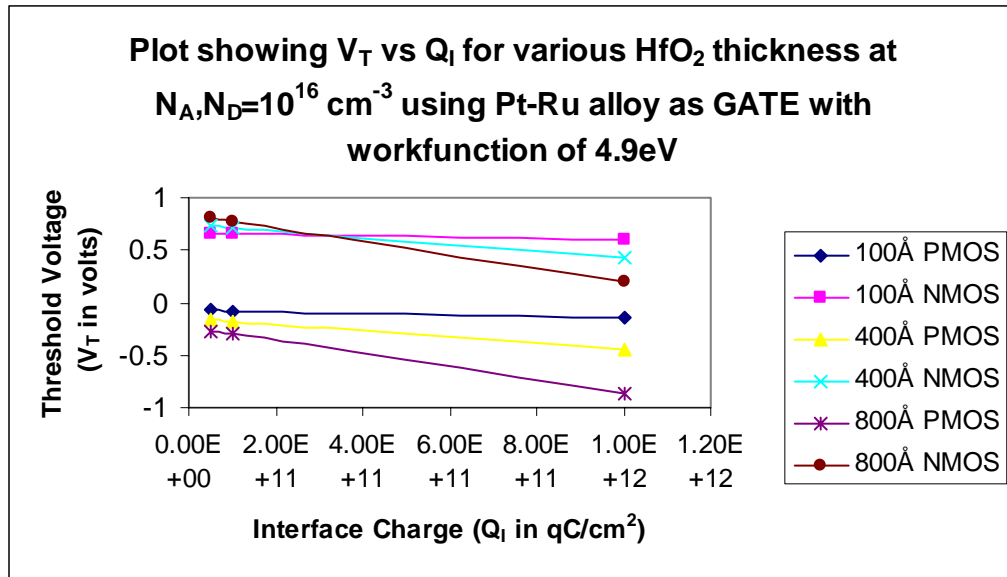


Figure 4.74 Plot showing  $V_T$  vs.  $Q_I$  for various  $HfO_2$  thickness at  $N_A, N_D = 10^{16} \text{ cm}^{-3}$  using Pt-Ru alloy with work function 4.9eV

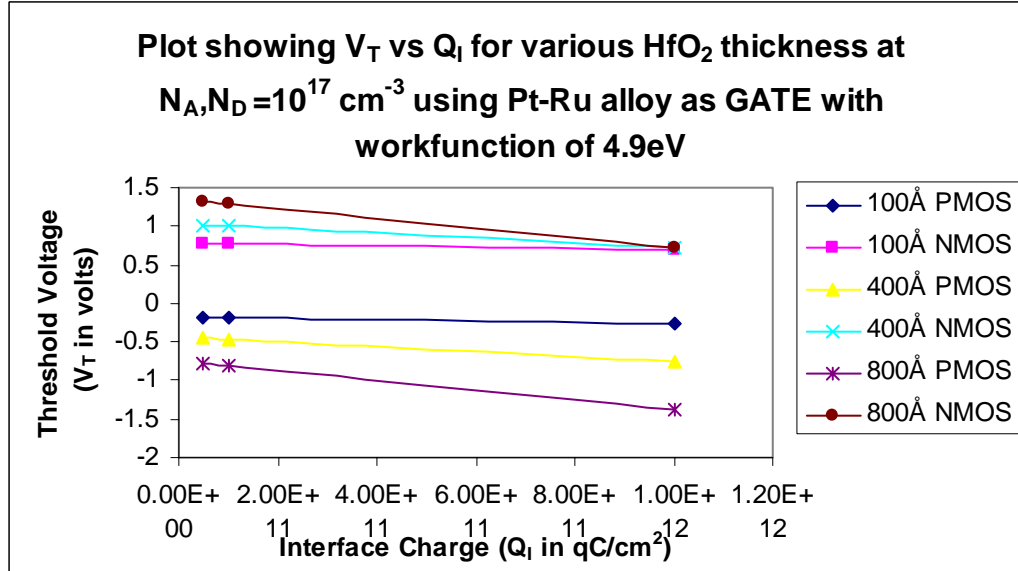


Figure 4.75 Plot showing  $V_T$  vs.  $Q_I$  for various  $HfO_2$  thickness at  $N_A, N_D = 10^{17} \text{ cm}^{-3}$  using Pt-Ru alloy with work function 4.9eV

### 4.3.2 Pt-Ru alloy (4.9eV)/Al<sub>2</sub>O<sub>3</sub> based MOSFET

In the first case, the work focuses on using platinum-ruthenium alloy with work function of 4.9eV as gate and aluminum oxide as gate oxide for PMOS and NMOS field effect transistors. The interface trap charge is chosen to be  $5 \cdot 10^{10}$  qC/cm<sup>2</sup> and kept constant for calculating threshold voltage. The doping concentration ( $N_A, N_D$ ) is varied from  $5 \cdot 10^{14}$  cm<sup>-3</sup>,  $10^{15}$  cm<sup>-3</sup>,  $5 \cdot 10^{15}$  cm<sup>-3</sup>,  $10^{16}$  cm<sup>-3</sup>,  $5 \cdot 10^{16}$  cm<sup>-3</sup> and  $10^{17}$  cm<sup>-3</sup> respectively. The oxide thickness ( $T_{OX}$ ) is varied from 50Å, 100Å, 200Å, 400Å, 600Å, 800Å and 1000Å respectively. The interface trap charge ( $Q_I$ ) is varied from  $5 \cdot 10^{10}$  qC/cm<sup>2</sup>,  $10^{11}$  qC/cm<sup>2</sup>,  $5 \cdot 10^{11}$  qC/cm<sup>2</sup> and  $10^{12}$  qC/cm<sup>2</sup> respectively. The interface charge  $10^{13}$  qC/cm<sup>2</sup> was not chosen because the simulations using ruthenium and aluminum showed threshold voltages to be bad for those devices. Threshold voltages for different doping concentrations, at constant interface trap charge are calculated. The threshold voltages vs. oxide thickness for different doping concentrations at constant interface trap charge ( $Q_I = 5 \cdot 10^{10}$  qC/cm<sup>2</sup>) are plotted. While the oxide thickness is varied for a range of values, the values which we are interested upon are high-k dielectric materials having thin, medium and thick gate oxides. The oxide thicknesses which we have selected to study are 100Å, 400Å and 800Å. The above process of simulation is repeated by changing the interface trap charge ( $Q_I$ ) from  $10^{11}$  qC/cm<sup>2</sup> to  $10^{13}$  qC/cm<sup>2</sup> are plotted in Fig 4.76, 4.77 and 4.78 respectively. The interface charge  $5 \cdot 10^{10}$  qC/cm<sup>2</sup> and  $10^{11}$  qC/cm<sup>2</sup> at  $10^{15}$  cm<sup>-3</sup> and  $10^{16}$  cm<sup>-3</sup> is good for PMOS devices. For NMOS devices interface charge  $10^{12}$  qC/cm<sup>2</sup> at various doping concentrations gives good threshold values. The variation of threshold voltage is studied and the doping concentration and interface trap charge best suitable for fabricating a Pt-Ru alloy (4.9eV) /aluminum oxide based MOS device is selected.



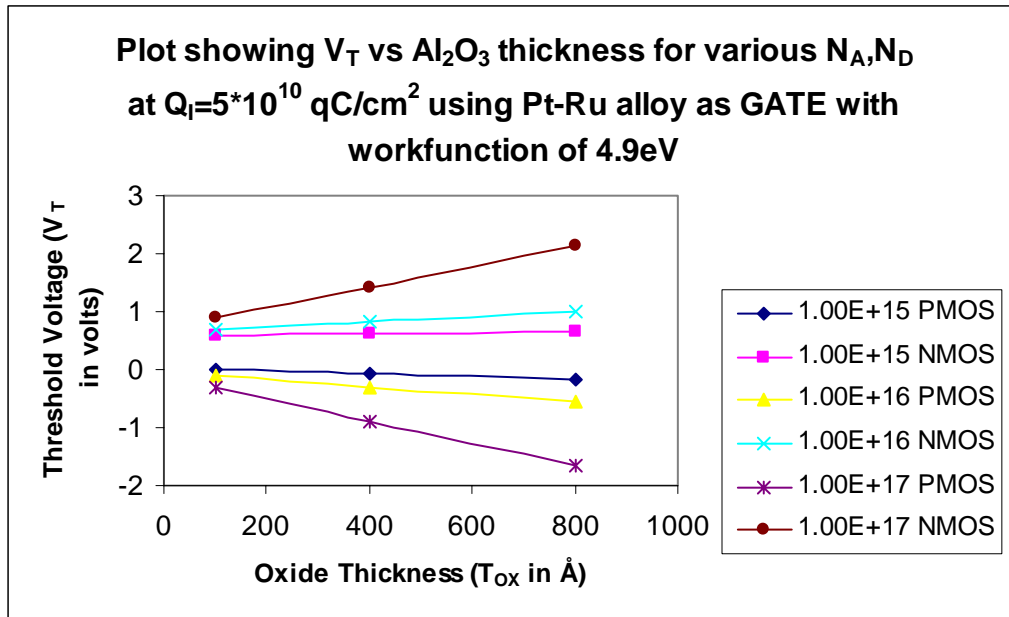


Figure 4.76 Plot showing  $V_T$  vs.  $Al_2O_3$  thickness for various  $N_A, N_D$  at  $Q_I=5 \cdot 10^{10}$  qC/cm<sup>2</sup> using Pt-Ru alloy with work function 4.9eV

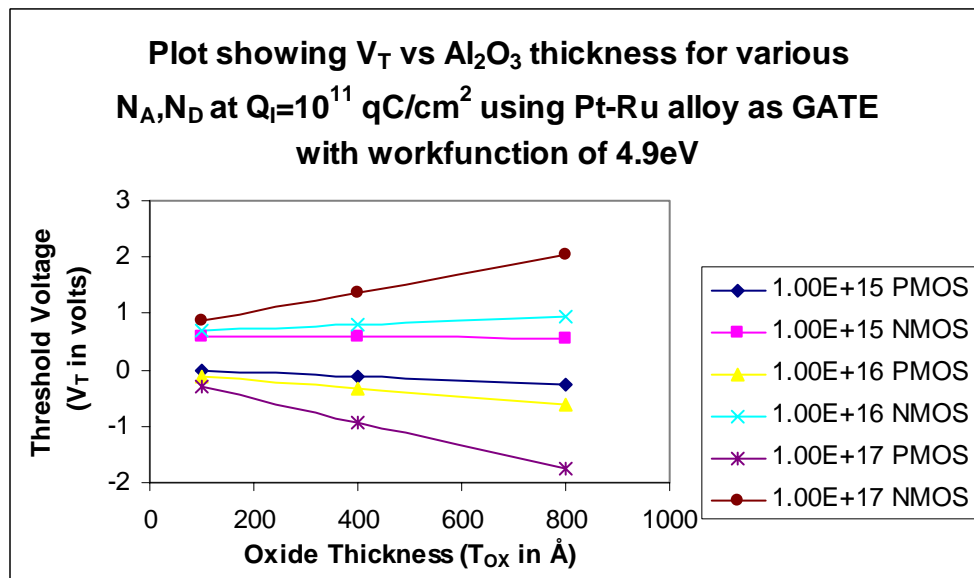


Figure 4.77 Plot showing  $V_T$  vs.  $Al_2O_3$  thickness for various  $N_A, N_D$  at  $Q_I=10^{11}$  qC/cm<sup>2</sup> using Pt-Ru alloy with work function 4.9eV

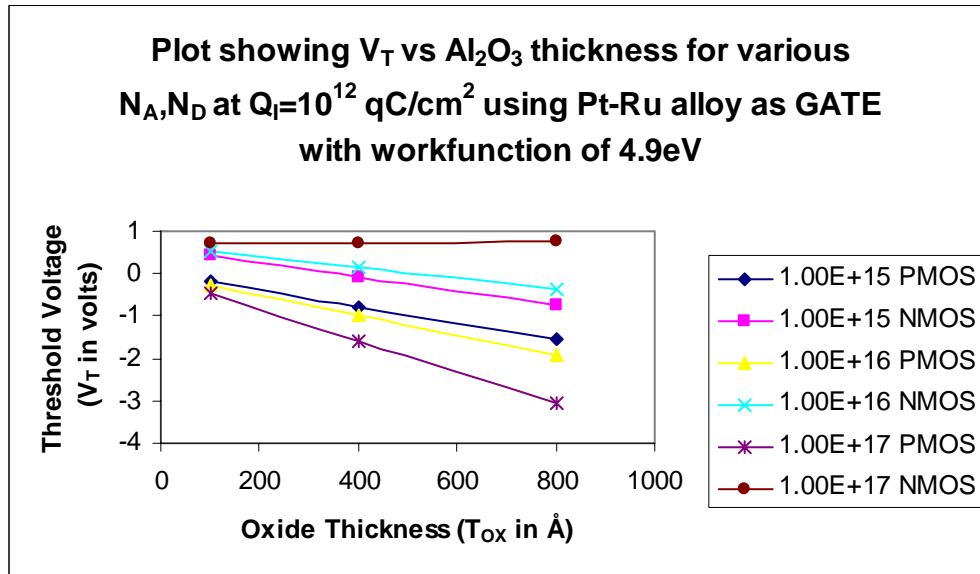


Figure 4.78 Plot showing  $V_T$  vs.  $Al_2O_3$  thickness for various  $N_A, N_D$  at  $Q_i=10^{12}$  qC/cm<sup>2</sup> using Pt-Ru alloy with work function 4.9eV

For the same gate platinum-ruthenium alloy with work function 4.9eV and same gate oxide aluminum, the interface trap charge ( $Q_i$ ) is kept constant at  $5 \cdot 10^{10}$  qC/cm<sup>2</sup>. Now by varying oxide thickness (initially 100Å, 400Å and 800Å), the threshold voltage is calculated and plotted against doping concentrations ( $N_A, N_D$ ). The above process of simulation is repeated by changing the interface trap charges from  $5 \cdot 10^{10}$  qC/cm<sup>2</sup> to  $10^{12}$  qC/cm<sup>2</sup> are plotted in Fig 4.79, 4.80 and 4.81 respectively. The oxide thickness 100Å and 400Å at  $5 \cdot 10^{10}$  qC/cm<sup>2</sup> and  $10^{11}$  qC/cm<sup>2</sup> gives good threshold values for both NMOS and PMOS devices. The variation of threshold voltage is studied and the oxide thickness and interface trap charge suitable for fabricating Pt-Ru alloy (4.9eV) /aluminum oxide based MOS device is selected.

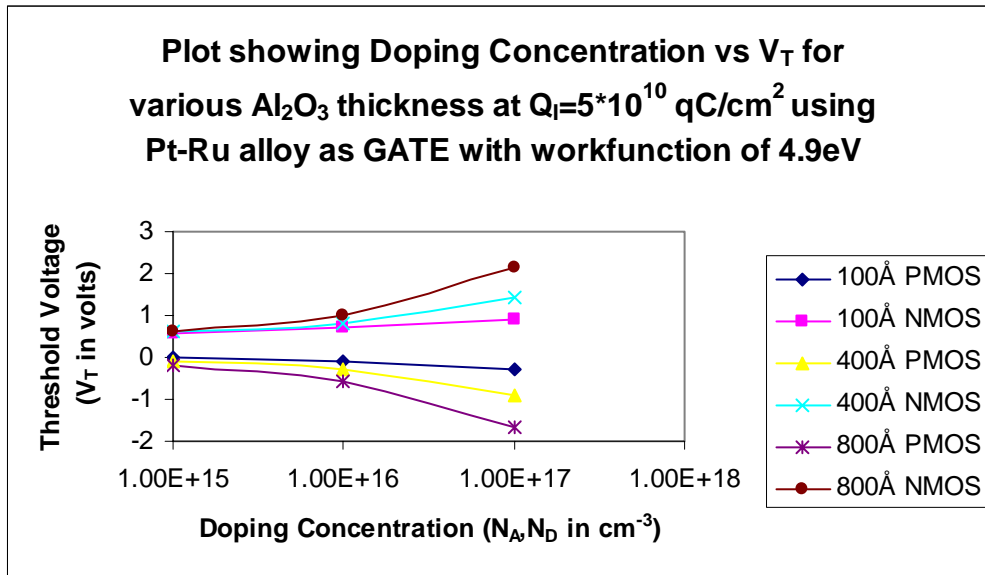


Figure 4.79 Plot showing Doping Concentration vs.  $V_T$  for various  $\text{Al}_2\text{O}_3$  thickness at  $Q_i=5*10^{10}$  qC/cm<sup>2</sup> using Pt-Ru alloy with work function 4.9eV

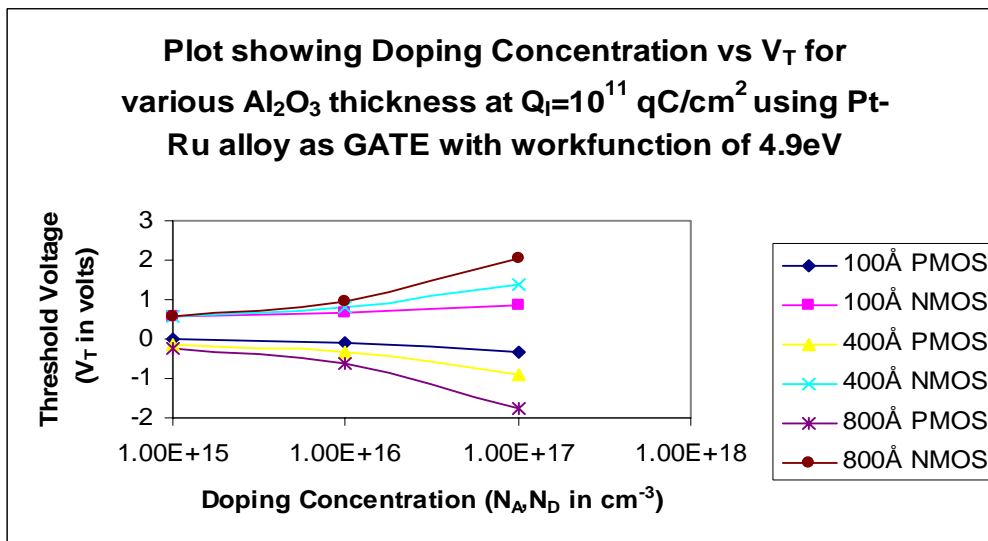


Figure 4.80 Plot showing Doping Concentration vs.  $V_T$  for various  $\text{Al}_2\text{O}_3$  thickness at  $Q_i=10^{11}$  qC/cm<sup>2</sup> using Pt-Ru alloy with work function 4.9eV

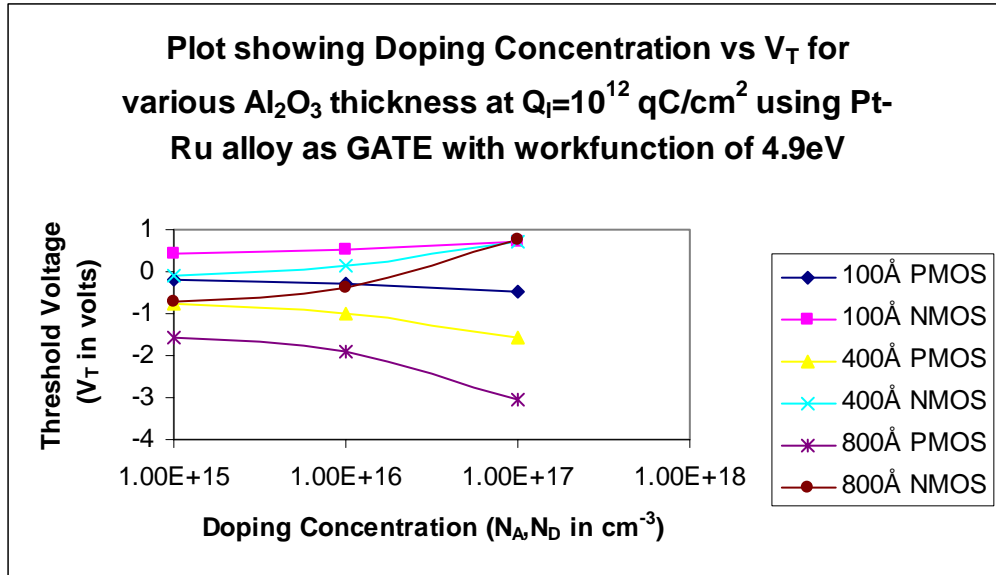


Figure 4.81 Plot showing Doping Concentration vs.  $V_T$  for various  $\text{Al}_2\text{O}_3$  thickness at  $Q_I=10^{12}$   $\text{qC}/\text{cm}^2$  using Pt-Ru alloy with work function 4.9eV

For the same gate platinum-ruthenium alloy with work function 4.9eV and same gate oxide hafnium, the doping concentration ( $N_A$ ,  $N_D$ ) is held constant at  $10^{15} \text{ cm}^{-3}$ . Now by varying oxide thickness (initially 100Å, 400Å and 800Å), the threshold voltage is calculated and plotted against different values of interface trap charges ( $Q_I$ ). The above process of simulation is repeated by changing the doping concentrations from  $10^{15} \text{ cm}^{-3}$  to  $10^{17} \text{ cm}^{-3}$  are plotted in Fig 4.82, 4.83 and 4.84 respectively. The doping concentration  $10^{15} \text{ cm}^{-3}$  and  $10^{16} \text{ cm}^{-3}$  at oxide thickness less than 400Å give good threshold values for NMOS and PMOS devices. The variation of threshold voltage is studied and the doping concentration and oxide thickness suitable for fabricating a Pt-Ru alloy (4.9eV)/aluminum oxide based MOS device are selected.

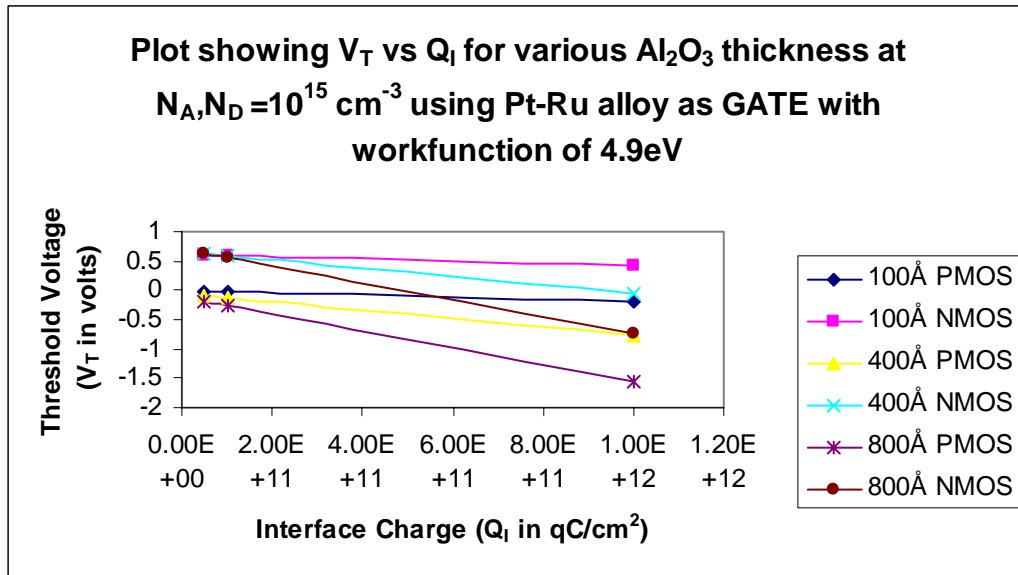


Figure 4.82 Plot showing  $V_T$  vs.  $Q_I$  for various  $Al_2O_3$  thickness at  $N_A, N_D = 10^{15} \text{ cm}^{-3}$  using Pt-Ru alloy with work function 4.9eV

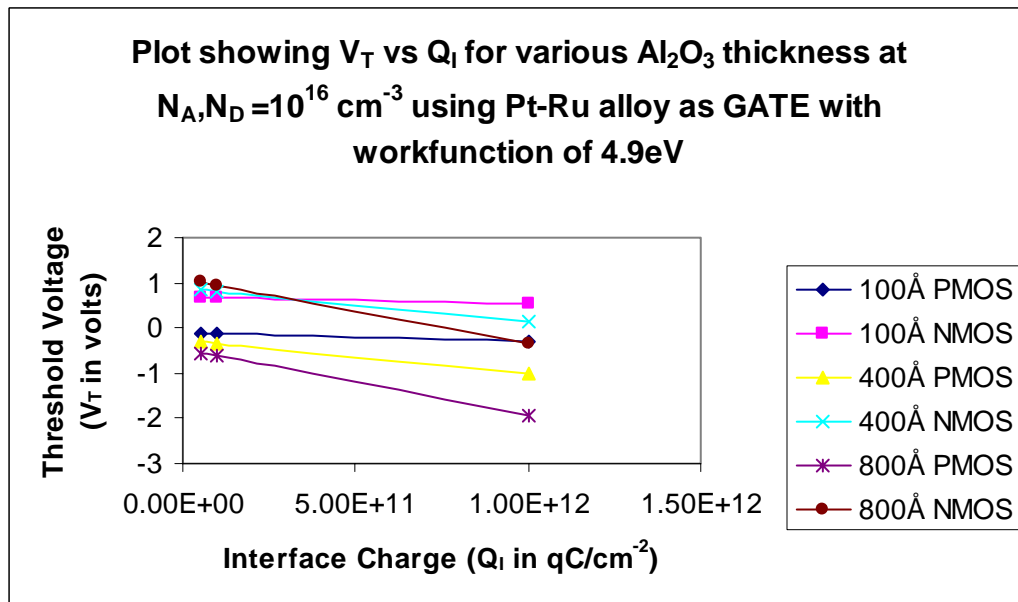


Figure 4.83 Plot showing  $V_T$  vs.  $Q_I$  for various  $Al_2O_3$  thickness at  $N_A, N_D = 10^{16} \text{ cm}^{-3}$  using Pt-Ru alloy with work function 4.9eV

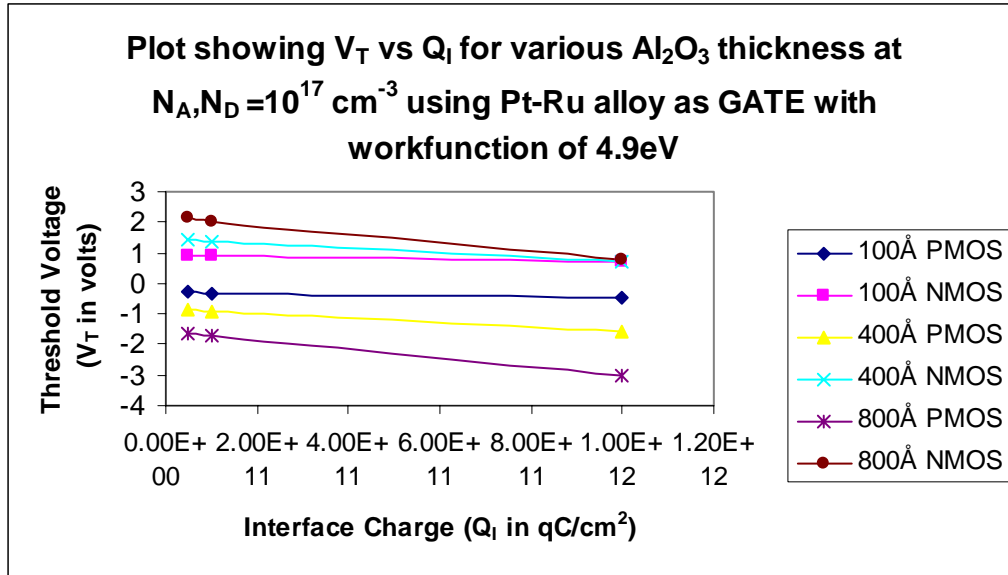


Figure 4.84 Plot showing  $V_T$  vs.  $Q_I$  for various  $Al_2O_3$  thickness at  $N_A, N_D = 10^{17} \text{ cm}^{-3}$  using Pt-Ru alloy with work function 4.9eV

#### 4.4 MOSFETS with Pt-Ru alloy (5.2eV) as gate

Lot of research is going on alloys to replace existing metals as gate. The Pt-Ru alloy work function is chosen to be 5.2eV which is in between the work function of platinum and ruthenium metals. This work function is near to the platinum work function of 5.6eV.

##### 4.4.1 Pt-Ru alloy (5.2eV)/ $HfO_2$ based MOSFET

In the first case, the work focuses on using platinum-ruthenium alloy with work function of 5.2eV as gate and hafnium oxide as gate oxide for PMOS and NMOS field effect transistors. The interface trap charge is chosen to be  $5 \times 10^{10} \text{ qC/cm}^2$  and kept constant for calculating threshold voltage. The doping concentration ( $N_A, N_D$ ) is varied from  $5 \times 10^{14} \text{ cm}^{-3}$ ,  $10^{15} \text{ cm}^{-3}$ ,

$5 \cdot 10^{15} \text{ cm}^{-3}$ ,  $10^{16} \text{ cm}^{-3}$ ,  $5 \cdot 10^{16} \text{ cm}^{-3}$  and  $10^{17} \text{ cm}^{-3}$  respectively. The oxide thickness ( $T_{\text{OX}}$ ) is varied from 50Å, 100Å, 200Å, 400Å, 600Å, 800Å and 1000Å respectively. The interface trap charge ( $Q_{\text{I}}$ ) is varied from  $5 \cdot 10^{10} \text{ qC/cm}^2$ ,  $10^{11} \text{ qC/cm}^2$ ,  $5 \cdot 10^{11} \text{ qC/cm}^2$  and  $10^{12} \text{ qC/cm}^2$  respectively. The interface charge  $10^{13} \text{ qC/cm}^2$  was not chosen because the simulations using ruthenium and aluminum as gate metal showed threshold voltages to be bad for those devices. Threshold voltages for different doping concentrations, at constant interface trap charge are calculated. The threshold voltages vs. oxide thickness for different doping concentrations at constant interface trap charge ( $Q_{\text{I}}=5 \cdot 10^{10} \text{ qC/cm}^2$ ) are plotted. While the oxide thickness is varied for a range of values, the values which we are interested upon are high-k dielectric materials having thin, medium and thick gate oxides. The oxide thicknesses which we have selected to study are 100Å, 400Å and 800Å. The above process of simulation is repeated by changing the interface trap charge ( $Q_{\text{I}}$ ) from  $10^{11} \text{ qC/cm}^2$  to  $10^{13} \text{ qC/cm}^2$  are plotted in Fig 4.85, 4.86 and 4.87 respectively. The  $V_{\text{T}}$  values for PMOS devices at various interface charges are positive which is not good as threshold voltage should be negative. The PMOS devices give good  $V_{\text{T}}$  values at  $10^{17} \text{ cm}^{-3}$  doping concentration at  $10^{12} \text{ qC/cm}^2$  interface charge which is not suitable as we need to make a good device.  $V_{\text{T}}$  values for NMOS are good except at  $10^{17} \text{ cm}^{-3}$  doping concentration and at various interface charges. The variation of threshold voltage is studied and the doping concentration and interface trap charge best suitable for fabricating a Pt-Ru alloy (5.2eV) /hafnium oxide based MOS device is selected.

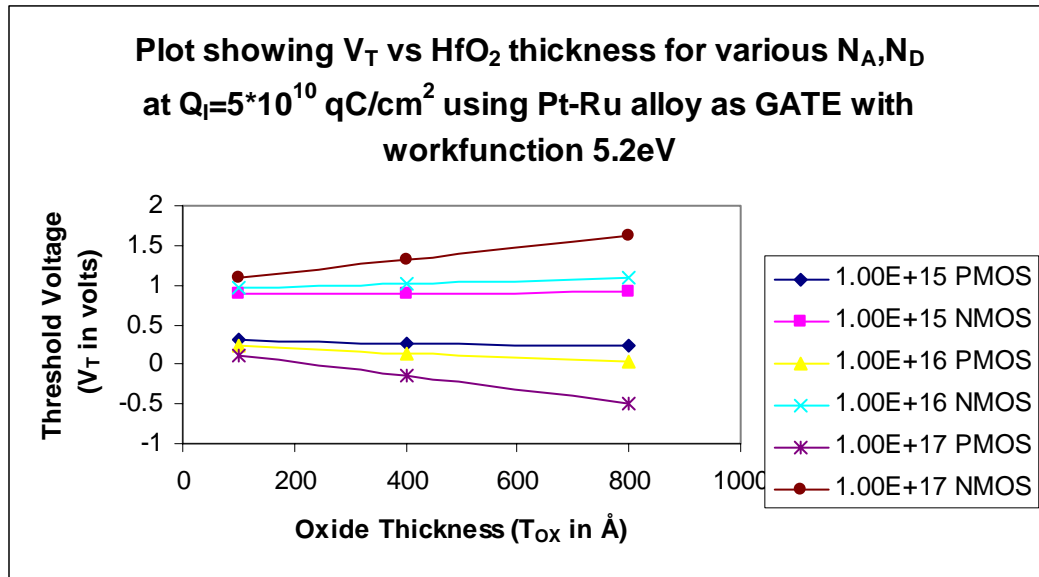


Figure 4.85 Plot showing  $V_T$  vs.  $HfO_2$  thickness for various  $N_A, N_D$  at  $Q_i=5 \cdot 10^{10} \text{ qC/cm}^2$  using Pt-Ru alloy with work function 5.2eV

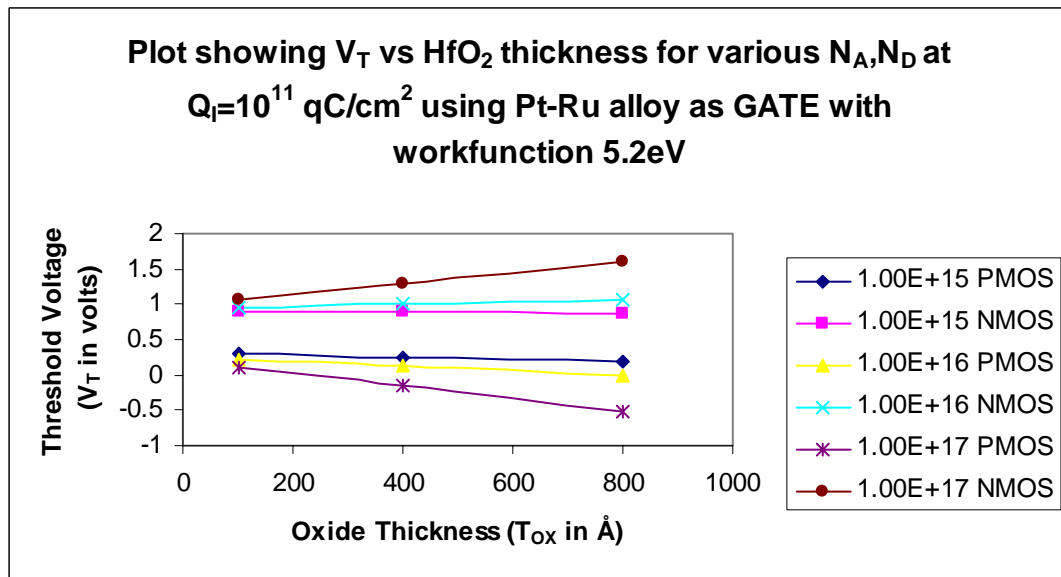


Figure 4.86 Plot showing  $V_T$  vs.  $HfO_2$  thickness for various  $N_A, N_D$  at  $Q_i=10^{11} \text{ qC/cm}^2$  using Pt-Ru alloy with work function 5.2eV



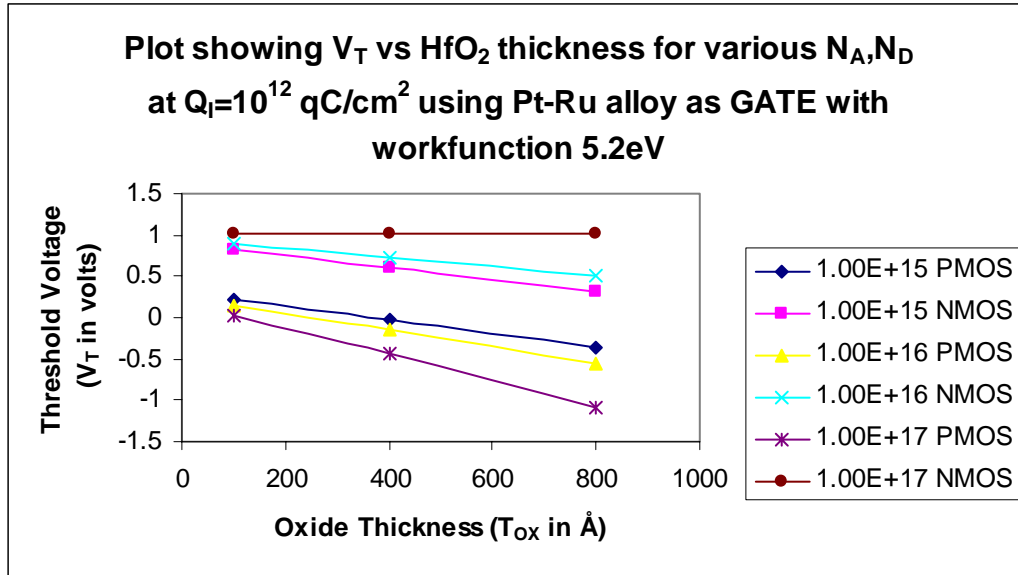


Figure 4.87 Plot showing  $V_T$  vs.  $\text{HfO}_2$  thickness for various  $N_A, N_D$  at  $Q_i=10^{12} \text{ qC/cm}^2$  using Pt-Ru alloy with work function 5.2eV

For the same gate platinum-ruthenium alloy with work function 5.2eV and same gate oxide hafnium, the interface trap charge ( $Q_i$ ) is kept constant at  $5 \times 10^{10} \text{ qC/cm}^2$ . Now by varying oxide thickness (initially 100Å, 400Å and 800Å), the threshold voltage is calculated and plotted against doping concentrations ( $N_A, N_D$ ). The above process of simulation is repeated by changing the interface trap charges from  $5 \times 10^{10} \text{ qC/cm}^2$  to  $10^{12} \text{ qC/cm}^2$  are plotted in Fig 4.88, 4.89 and 4.90 respectively. PMOS devices give good threshold voltage for oxide thicknesses 100Å, 400Å, and 800Å at various interface charges having substrate concentration of  $10^{17} \text{ cm}^{-3}$ . For NMOS devices  $V_T$  values is good for oxide thicknesses less than 400Å at various interface trap charges. The variation of threshold voltage is studied and the oxide thickness and interface trap charge suitable for fabricating Pt-Ru alloy (5.2eV) /hafnium oxide based MOS device is selected.

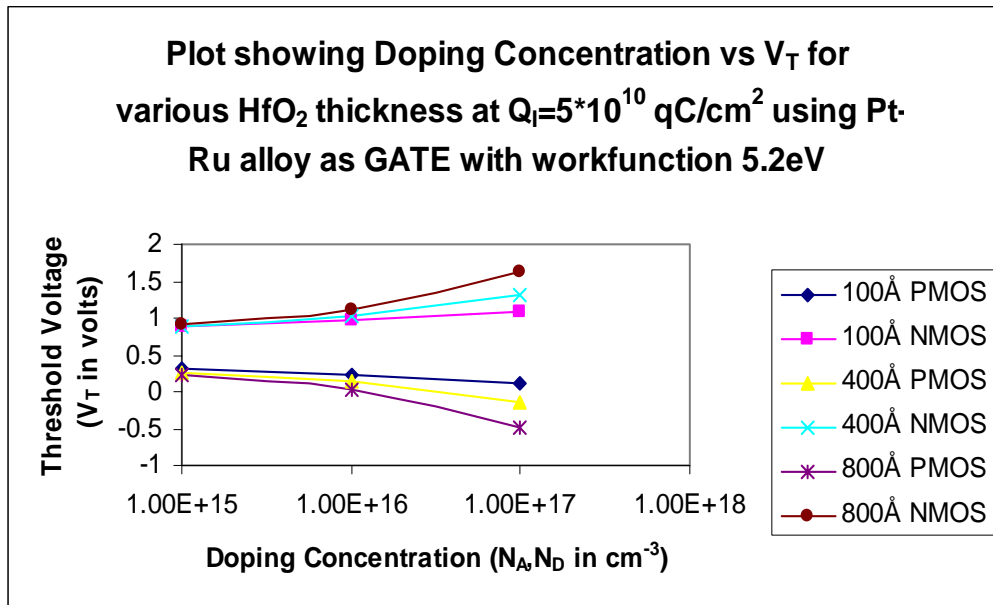


Figure 4.88 Plot showing Doping Concentration vs.  $V_T$  for various  $\text{HfO}_2$  thickness at  $Q_I=5 \cdot 10^{10}$  qC/cm<sup>2</sup> using Pt-Ru alloy with work function 5.2eV

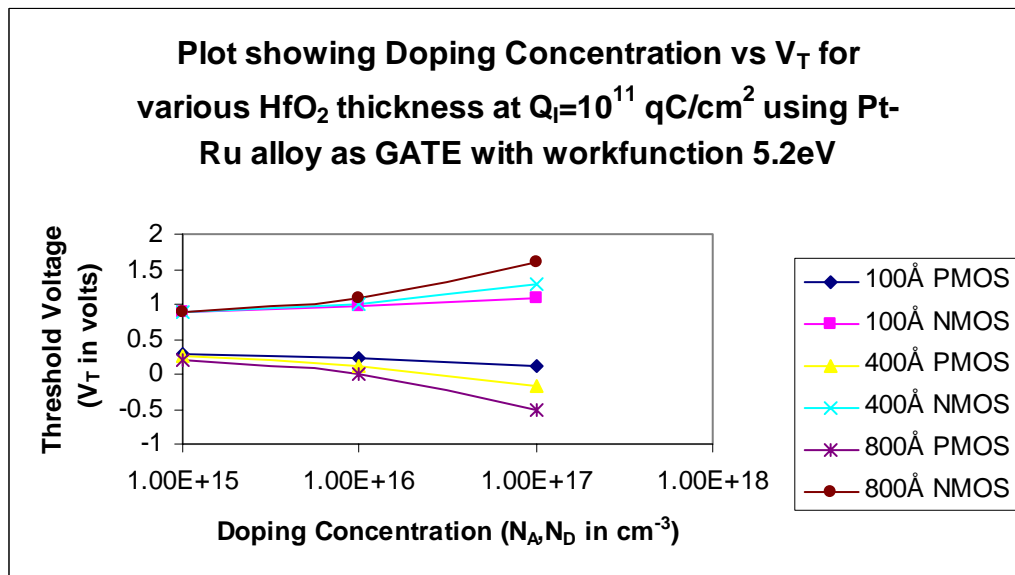


Figure 4.89 Plot showing Doping Concentration vs.  $V_T$  for various  $\text{HfO}_2$  thickness at  $Q_I=10^{11}$  qC/cm<sup>2</sup> using Pt-Ru alloy with work function 5.2eV

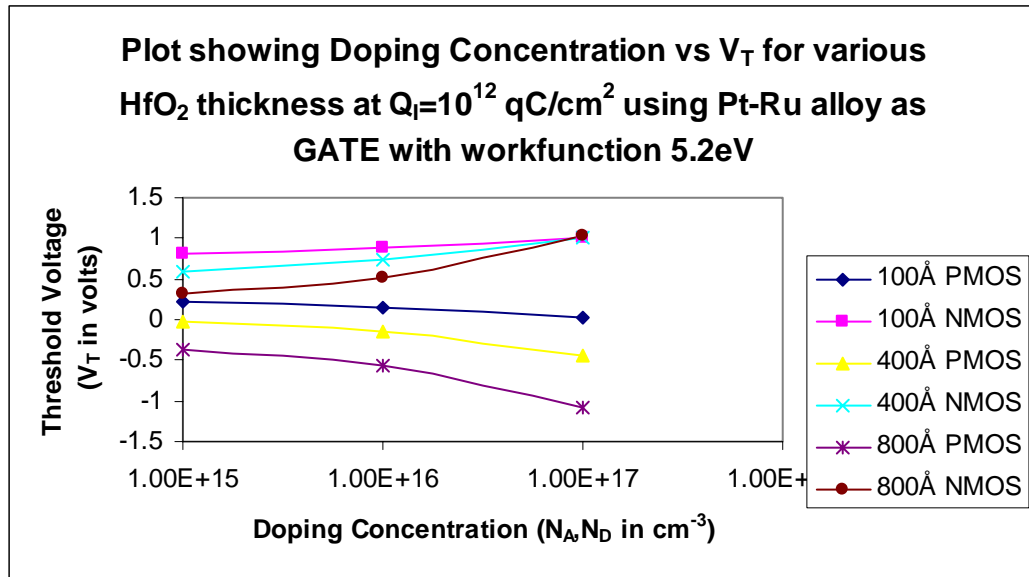


Figure 4.90 Plot showing Doping Concentration vs.  $V_T$  for various  $\text{HfO}_2$  thickness at  $Q_i=10^{12}$   $\text{qC/cm}^2$  using Pt-Ru alloy with work function 5.2eV

For the same gate platinum-ruthenium alloy with work function 5.2eV and same gate oxide hafnium, the doping concentration ( $N_A$ ,  $N_D$ ) is held constant at  $10^{15} \text{ cm}^{-3}$ . Now by varying oxide thickness (initially 100Å, 400Å and 800Å), the threshold voltage is calculated and plotted against different values of interface trap charges ( $Q_i$ ). The above process of simulation is repeated by changing the doping concentrations from  $10^{15} \text{ cm}^{-3}$  to  $10^{17} \text{ cm}^{-3}$  are plotted in Fig 4.91, 4.92 and 4.93 respectively. PMOS devices give good values of  $V_T$  at  $10^{17} \text{ cm}^{-3}$  doping concentration at various interface charges. NMOS devices show promising values at for doping concentrations  $10^{15} \text{ cm}^{-3}$ ,  $10^{16} \text{ cm}^{-3}$  at various interface charges. The variation of threshold voltage is studied and the doping concentration and oxide thickness suitable for fabricating a Pt-Ru alloy (5.2eV)/hafnium oxide based MOS device are selected.

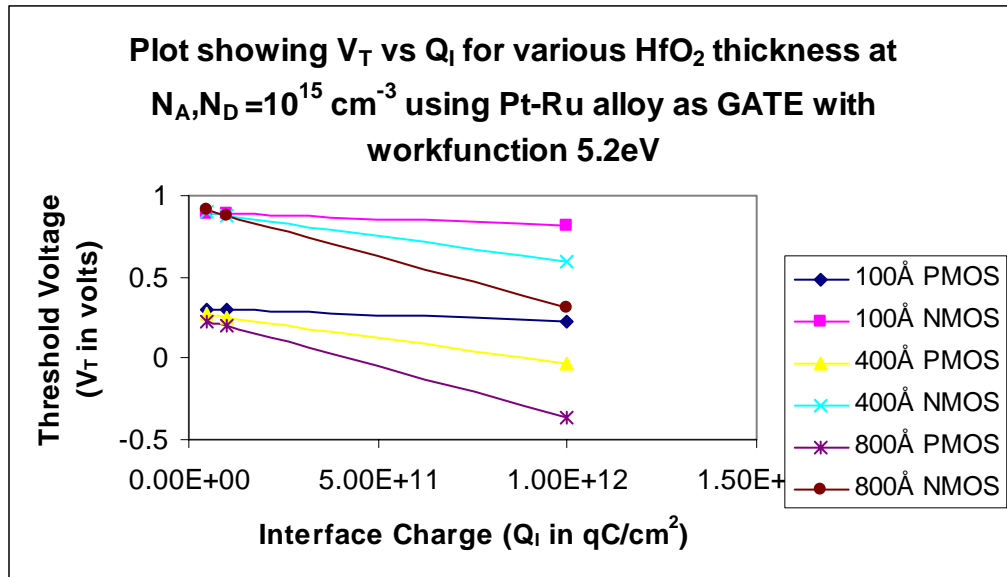


Figure 4.91 Plot showing  $V_T$  vs.  $Q_I$  for various  $HfO_2$  thickness at  $N_A, N_D = 10^{15} \text{ cm}^{-3}$  using Pt-Ru alloy with work function 5.2eV

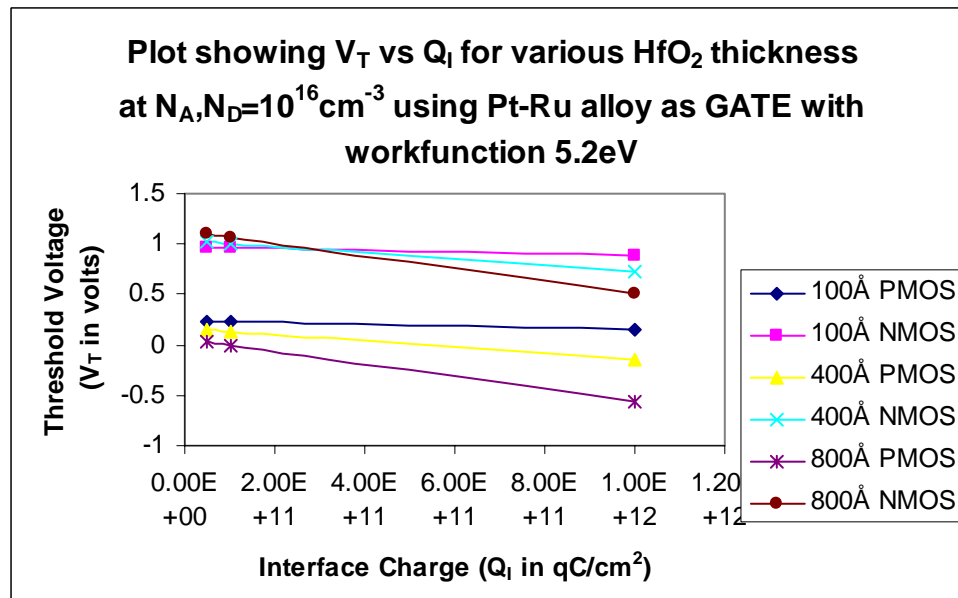


Figure 4.92 Plot showing  $V_T$  vs.  $Q_I$  for various  $HfO_2$  thickness at  $N_A, N_D = 10^{16} \text{ cm}^{-3}$  using Pt-Ru alloy with work function 5.2eV

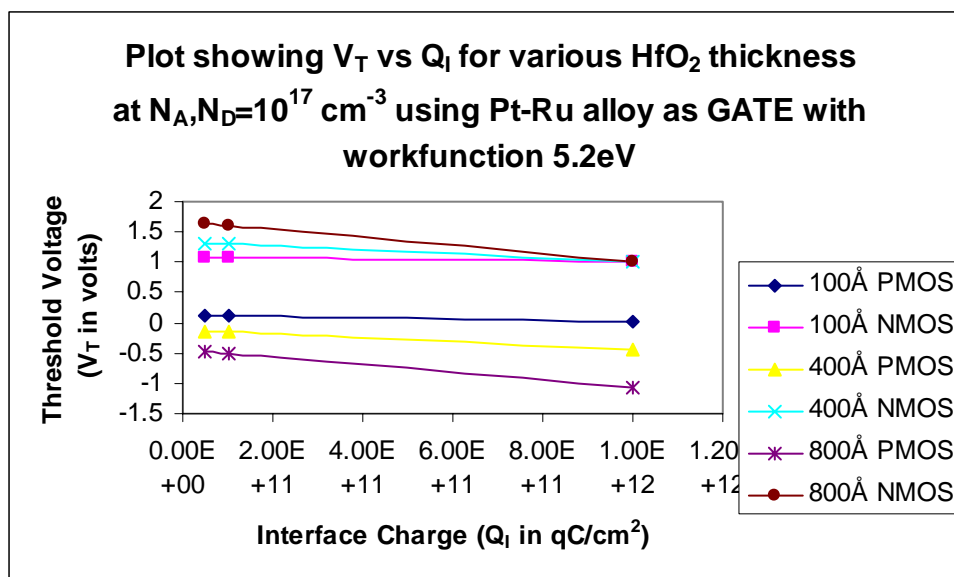


Figure 4.93 Plot showing  $V_T$  vs.  $Q_I$  for various  $HfO_2$  thickness at  $N_A, N_D=10^{17} \text{ cm}^{-3}$  using Pt-Ru alloy with work function 5.2eV

#### 4.4.2 Pt-Ru alloy (5.2eV)/ $Al_2O_3$ based MOSFET

In the first case, the work focuses on using platinum-ruthenium alloy with work function of 5.2eV as gate and aluminum oxide as gate oxide for PMOS and NMOS field effect transistors. The interface trap charge is chosen to be  $5 \cdot 10^{10} \text{ qC/cm}^2$  and kept constant for calculating threshold voltage. The doping concentration ( $N_A, N_D$ ) is varied from  $5 \cdot 10^{14} \text{ cm}^{-3}$ ,  $10^{15} \text{ cm}^{-3}$ ,  $5 \cdot 10^{15} \text{ cm}^{-3}$ ,  $10^{16} \text{ cm}^{-3}$ ,  $5 \cdot 10^{16} \text{ cm}^{-3}$  and  $10^{17} \text{ cm}^{-3}$  respectively. The oxide thickness ( $T_{OX}$ ) is varied from 50Å, 100Å, 200Å, 400Å, 600Å, 800Å and 1000Å respectively. The interface trap charge ( $Q_I$ ) is varied from  $5 \cdot 10^{10} \text{ qC/cm}^2$ ,  $10^{11} \text{ qC/cm}^2$ ,  $5 \cdot 10^{11} \text{ qC/cm}^2$  and  $10^{12} \text{ qC/cm}^2$  respectively. The interface charge  $10^{13} \text{ qC/cm}^2$  was not chosen because the simulations using ruthenium and aluminum showed threshold voltages to be bad for those devices. Threshold

voltages for different doping concentrations, at constant interface trap charge are calculated. The threshold voltages vs. oxide thickness for different doping concentrations at constant interface trap charge ( $Q_I=5*10^{10}$  qC/cm<sup>2</sup>) are plotted. While the oxide thickness is varied for a range of values, the values which we are interested upon are high-k dielectric materials having thin, medium and thick gate oxides. The oxide thicknesses which we have selected to study are 100Å, 400Å and 800Å. The above process of simulation is repeated by changing the interface trap charge ( $Q_I$ ) from  $10^{11}$  qC/cm<sup>2</sup> to  $10^{13}$  qC/cm<sup>2</sup> are plotted in Fig 4.94, 4.95 and 4.96 respectively. The  $V_T$  values for PMOS at various interface charges and doping concentrations is not good except at higher doping concentration  $10^{17}$  cm<sup>-3</sup>. The NMOS devices  $V_T$  value is good at  $10^{15}$  cm<sup>-3</sup> concentration and at various interface charges. The variation of threshold voltage is studied and the doping concentration and interface trap charge best suitable for fabricating a Pt-Ru alloy (5.2eV) /aluminum oxide based MOS device is selected.

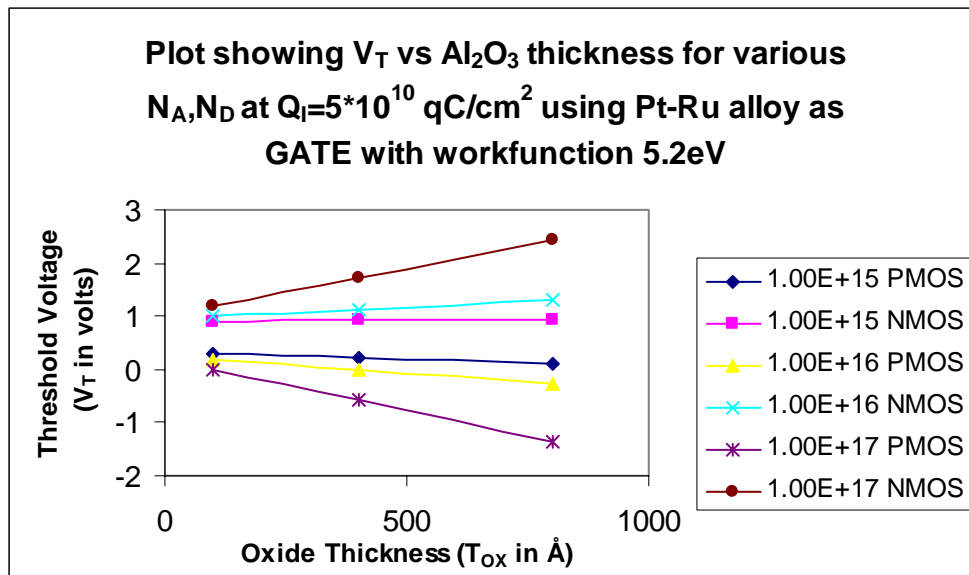


Figure 4.94 Plot showing  $V_T$  vs.  $Al_2O_3$  thickness for various  $N_A, N_D$  at  $Q_I=5*10^{10}$  qC/cm<sup>2</sup> using Pt-Ru alloy with work function 5.2eV

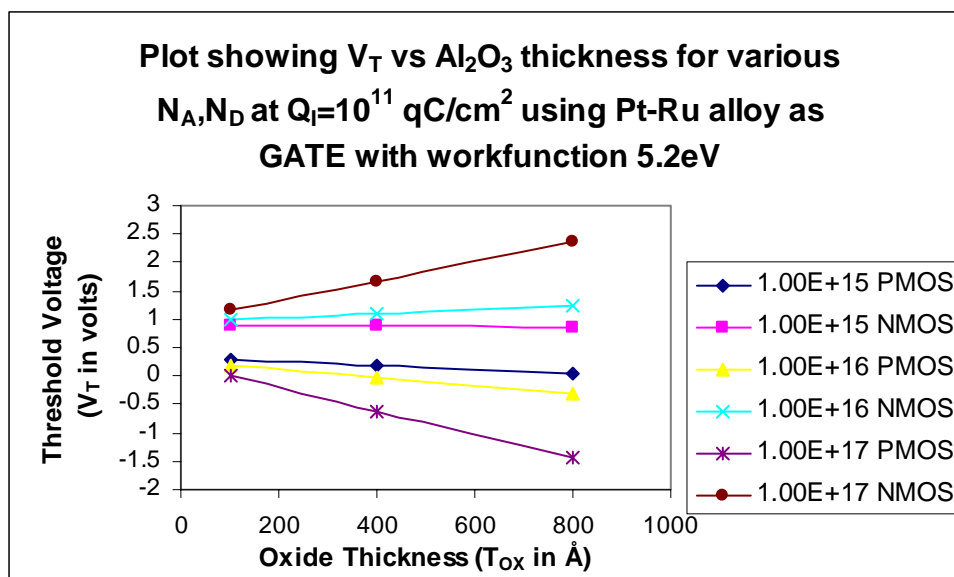


Figure 4.95 Plot showing  $V_T$  vs.  $Al_2O_3$  thickness for various  $N_A, N_D$  at  $Q_f=10^{11}$  qC/cm<sup>2</sup> using Pt-Ru alloy with work function 5.2eV

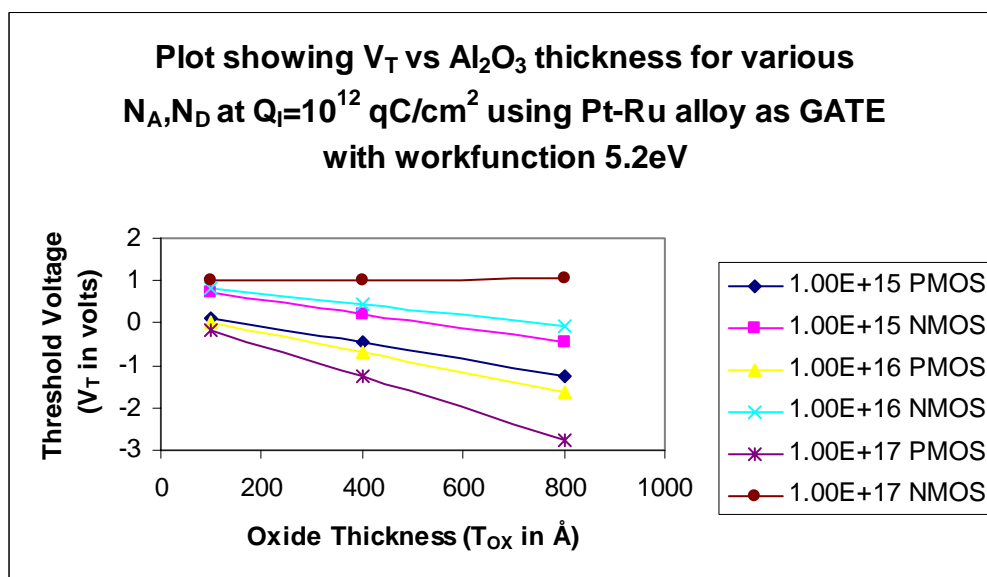


Figure 4.96 Plot showing  $V_T$  vs.  $Al_2O_3$  thickness for various  $N_A, N_D$  at  $Q_f=10^{12}$  qC/cm<sup>2</sup> using Pt-Ru alloy with work function 5.2eV

For the same gate platinum-ruthenium alloy with work function 5.2eV and same gate oxide aluminum, the interface trap charge ( $Q_i$ ) is kept constant at  $5 \cdot 10^{10}$  qC/cm<sup>2</sup>. Now by varying oxide thickness (initially 100Å, 400Å and 800Å), the threshold voltage is calculated and plotted against doping concentrations ( $N_A$ ,  $N_D$ ). The above process of simulation is repeated by changing the interface trap charges from  $5 \cdot 10^{10}$  qC/cm<sup>2</sup> to  $10^{12}$  qC/cm<sup>2</sup> are plotted in Fig 4.97, 4.98 and 4.99 respectively. NMOS devices have  $V_T$  values good at 100Å for various interface charges. For PMOS devices the values are good around 400Å at various interface charges for all doping concentrations. The variation of threshold voltage is studied and the oxide thickness and interface trap charge suitable for fabricating Pt-Ru alloy (5.2eV) /aluminum oxide based MOS device is selected.

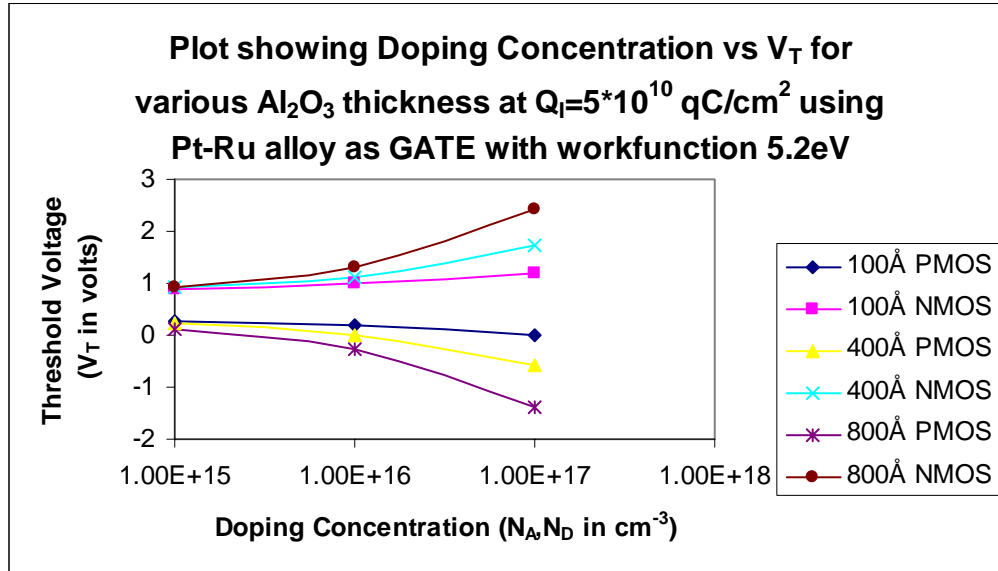


Figure 4.97 Plot showing Doping Concentration vs.  $V_T$  for various  $Al_2O_3$  thickness at  $Q_i=5 \cdot 10^{10}$  qC/cm<sup>2</sup> using Pt-Ru alloy with work function 5.2eV



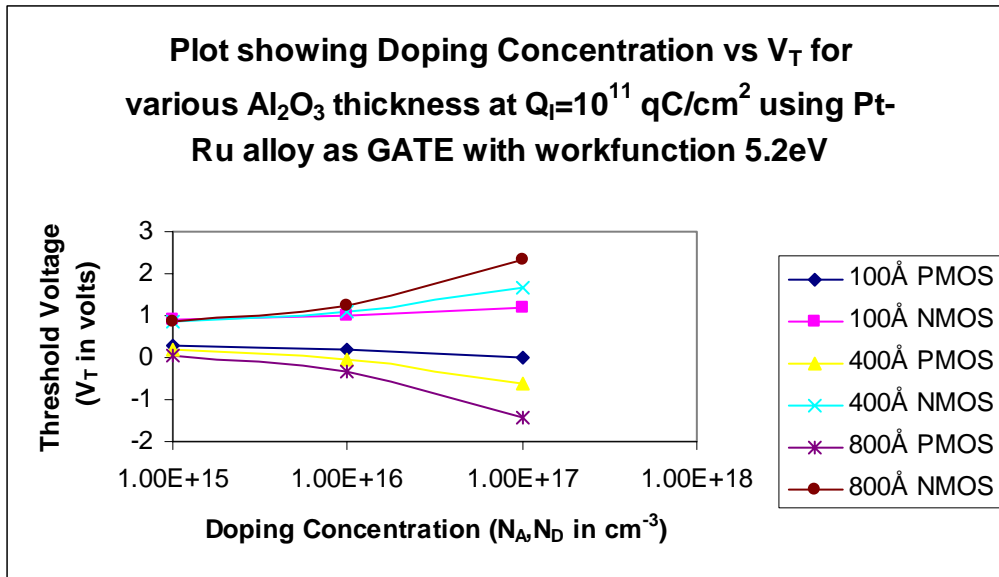


Figure 4.98 Plot showing Doping Concentration vs.  $V_T$  for various  $\text{Al}_2\text{O}_3$  thickness at  $Q_f=10^{11}$  qC/cm<sup>2</sup> using Pt-Ru alloy with work function 5.2eV

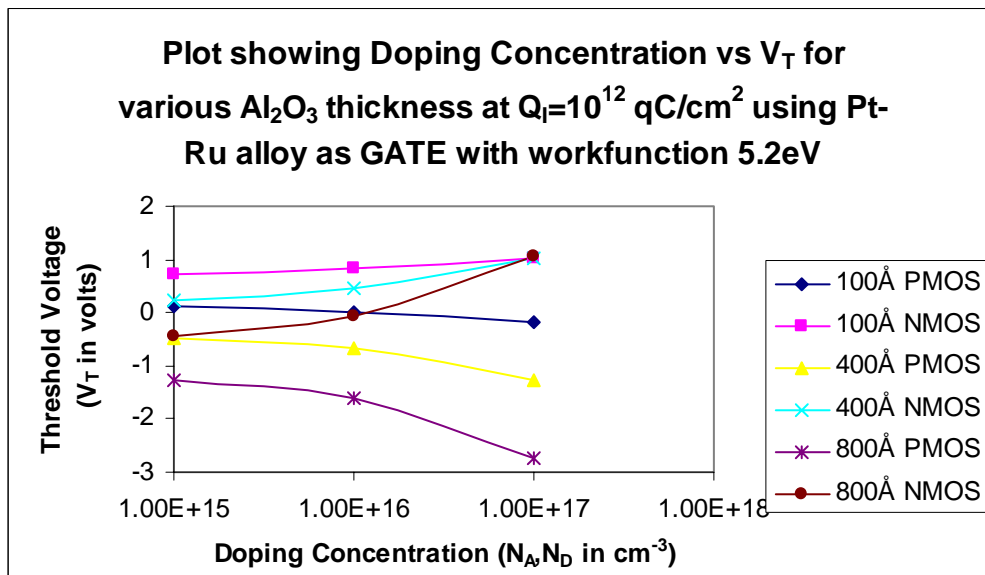


Figure 4.99 Plot showing Doping Concentration vs.  $V_T$  for various  $\text{Al}_2\text{O}_3$  thickness at  $Q_f=10^{12}$  qC/cm<sup>2</sup> using Pt-Ru alloy with work function 5.2eV

For the same gate platinum-ruthenium alloy with work function 5.2eV and same gate oxide hafnium, the doping concentration ( $N_A$ ,  $N_D$ ) is held constant at  $10^{15} \text{ cm}^{-3}$ . Now by varying oxide thickness (initially 100Å, 400Å and 800Å), the threshold voltage is calculated and plotted against different values of interface trap charges ( $Q_I$ ). The above process of simulation is repeated by changing the doping concentrations from  $10^{15} \text{ cm}^{-3}$  to  $10^{17} \text{ cm}^{-3}$  are plotted in Fig 4.100, 4.101 and 4.102 respectively. NMOS devices give good threshold values for all oxide thicknesses at doping concentration  $10^{15} \text{ cm}^{-3}$ . PMOS devices give good threshold values for 400Å for doping concentration  $10^{16} \text{ cm}^{-3}$  and  $10^{17} \text{ cm}^{-3}$  at interface charge  $10^{12} \text{ qC/cm}^2$  which is not ideal for a MOS device. The variation of threshold voltage is studied and the doping concentration and oxide thickness suitable for fabricating a Pt-Ru alloy (5.2eV)/hafnium oxide based MOS device are selected.

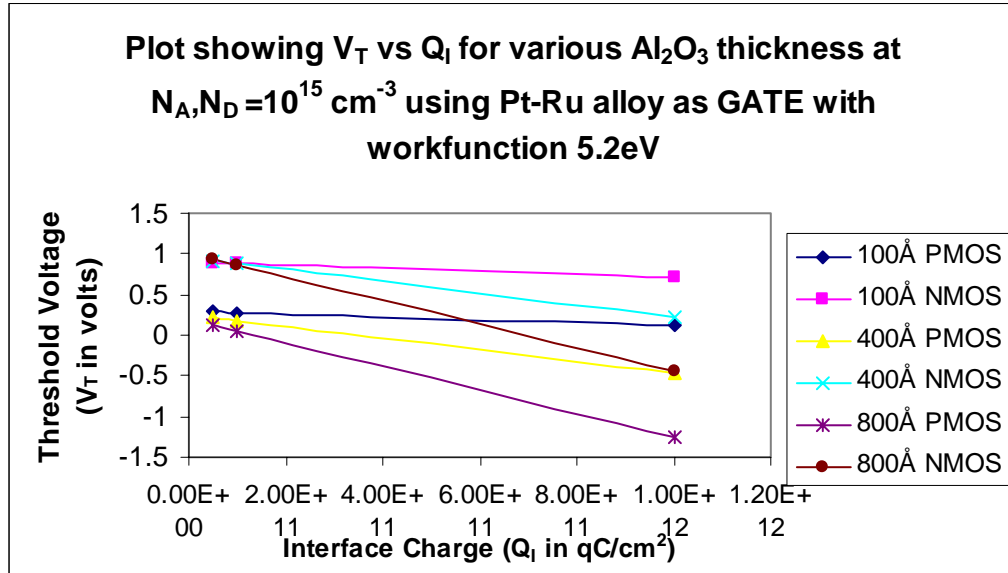


Figure 4.100 Plot showing  $V_T$  vs.  $Q_I$  for various  $\text{Al}_2\text{O}_3$  thickness at  $N_A, N_D = 10^{15} \text{ cm}^{-3}$  using Pt-Ru alloy with work function 5.2eV

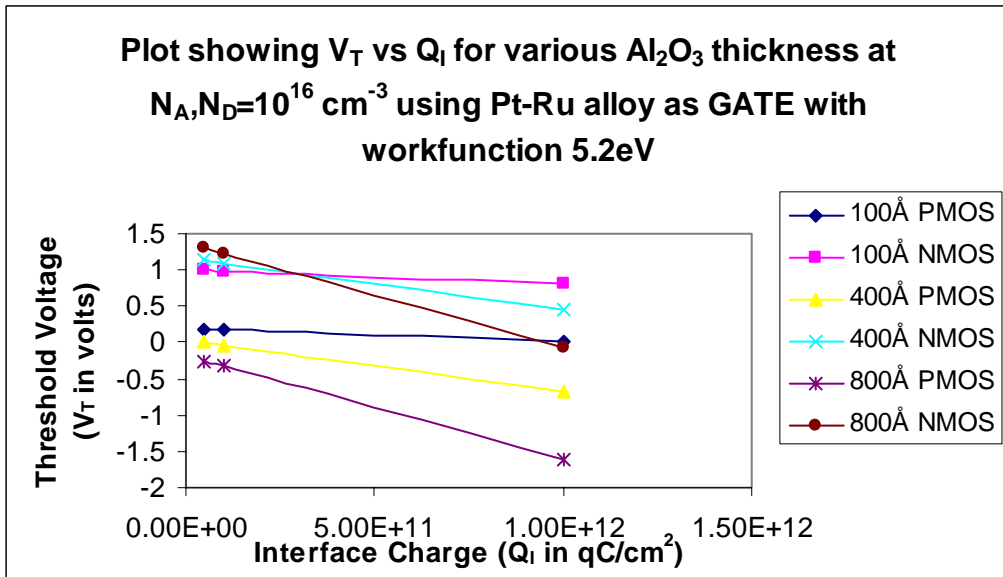


Figure 4.101 Plot showing  $V_T$  vs.  $Q_i$  for various  $Al_2O_3$  thickness at  $N_A, N_D = 10^{16} \text{ cm}^{-3}$  using Pt-Ru alloy with work function 5.2eV

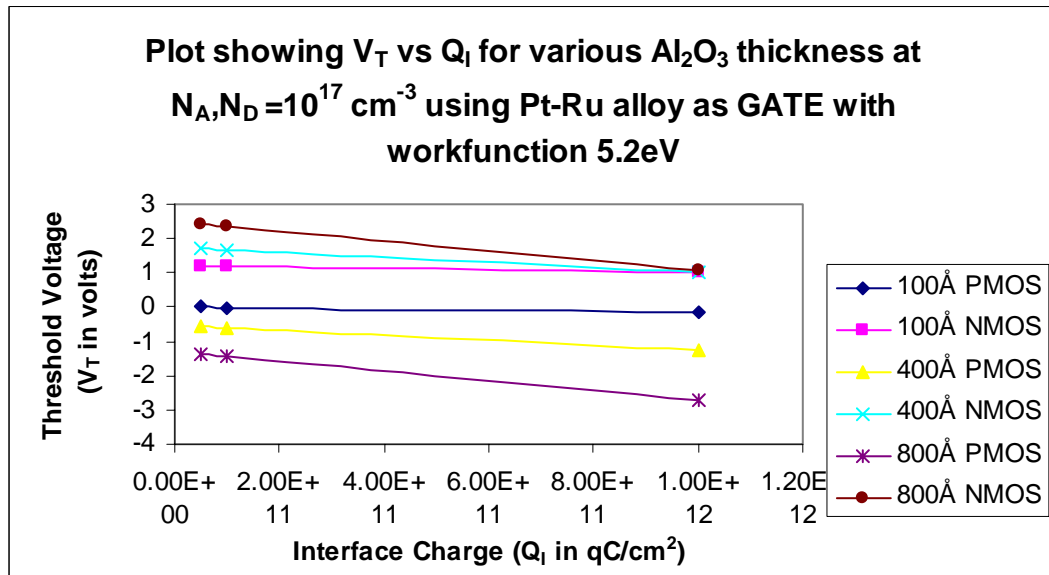


Figure 4.102 Plot showing  $V_T$  vs.  $Q_i$  for various  $Al_2O_3$  thickness at  $N_A, N_D = 10^{17} \text{ cm}^{-3}$  using Pt-Ru alloy with work function 5.2eV

## CHAPTER FIVE: CONCLUSIONS AND FUTURE WORK

In the present work, high-k dielectric materials and gate metals were studied in detail. Deposition methods which are suitable for dielectric materials and gate metals have been discussed. The threshold voltage values were calculated for MOS device as a function of oxide thickness, interface trap charges and doping concentrations of substrate. The desired values of threshold voltage values, PMOS ranged between 0 to -1 volts and NMOS devices -1 to +1 volts respectively.

In the first case, aluminum as gate metal with hafnium oxide, aluminum oxide, tantalum oxide and zirconium oxide as gate insulators are studied. The MOSFET with aluminum as gate metal and gate dielectric as hafnium oxide is suitable for device fabrication because of no interfacial layer formation with silicon and has good threshold voltage values for both PMOS and NMOS field-effect-transistors. Low threshold voltages can be achieved even with interface charges of  $10^{12}$  qC/cm<sup>2</sup>, substrate doping concentrations of  $10^{17}$  cm<sup>-3</sup> for NMOS and  $10^{16}$  cm<sup>-3</sup> for PMOS having oxide thicknesses 800Å.

In the second case, ruthenium as gate metal with hafnium oxide and aluminum oxide as gate insulators were studied. The MOSFET with ruthenium as gate metal and hafnium oxide as gate insulator combination, has good threshold values for both PMOS and NMOS field effect transistors. The best performance were seen for devices which has low threshold voltages for both MOS devices even with interface charges of  $10^{12}$  qC/cm<sup>2</sup>, having substrate doping concentrations of  $10^{17}$  cm<sup>-3</sup> and having oxide thicknesses 800Å.

In third case, Pt-Ru alloy having work function of 4.9eV as gate metal and hafnium oxide and aluminum oxide as gate insulators were studied. The MOSFET with Pt-Ru alloy with

hafnium oxide is suggested for fabrication because of its low threshold values for PMOS and NMOS devices. The optimum values at which we have low threshold voltages for both MOS devices even with interface charges of  $10^{11}$  qC/cm<sup>2</sup>, having substrate doping concentrations of  $10^{17}$  cm<sup>-3</sup> and oxide thicknesses 400Å.

In fourth case, Pt-Ru alloy having work function of 5.2eV as gate and hafnium oxide and aluminum oxide as gate insulators were studied. The MOSFET with Pt-Ru alloy with hafnium oxide is suggested for fabrication and has low threshold values for only NMOS devices. The threshold values of PMOS devices are not good using this combination. The optimum values suggested for fabricating NMOS device gives low threshold voltages even with interface charges of  $10^{12}$  qC/cm<sup>2</sup>, having substrate doping concentrations of  $10^{16}$  cm<sup>-3</sup> and oxide thicknesses 400Å. The PMOS devices cannot be made using having Pt-Ru alloy having work function 5.2eV.

To conclude the work, comparing several gate oxides, hafnium oxide is found to form no interfacial layer and stable over silicon substrate. For gate metals, ruthenium with HfO<sub>2</sub> is found to offer low threshold voltages for both NMOS and PMOS devices even with 800Å oxide thickness compared to aluminum metal. Metals-oxides combination of ruthenium/hafnium oxide based MOSFET is suggested for fabrication because of its low threshold values having interface charges of  $10^{12}$  qC/cm<sup>2</sup>, doping concentrations of  $10^{17}$  cm<sup>-3</sup> and oxide thicknesses 800Å.

For future work, alloys and gate metals, having different work functions can be studied in detail (4.5eV, 4.6eV and 4.8eV). Further, gate dielectrics such as BST, ZnO, Ce<sub>2</sub>O<sub>3</sub>, TiO<sub>2</sub> can be investigated to provide good threshold voltages (0 to -1 volts for PMOS and -1 to +1 volts for NMOS) because of its high dielectric constant, low leakage current and stability over silicon substrates. Deposition methods to prevent formation of interfacial layer and stability between oxide-silicon interfaces can be studied in detail. Gate metals of interest in the future are Ru-Ta

and Pt-Ta alloys, TiN and TaN (nitrogen doped concentrations). The alloys can have different work functions depending upon the chemical composition they are deposited. A lot of research is still necessary to get a good gate metal and gate dielectric combination that can give fairly good threshold voltage for MOS devices.

## **APPENDIX**

### **MATCAD SIMULATIONS AND CALCULATIONS FOR FINDING THRESHOLD VOLTAGE**

$$\epsilon_0 := 8.854 \cdot 10^{-14} \frac{\text{F}}{\text{cm}}$$

$$q := 1.6 \cdot 10^{-19} \cdot \text{coul}$$

$$eV := q \cdot V$$

Intrinsic Carrier Concentration

$$n_i := 1.5 \cdot 10^{10} \cdot \frac{1}{\text{cm}^3}$$

$$E_g := 1.1V$$

$$\chi_{\text{Si}} := 4.05V$$

The first P-MOSFET we are going to discuss is using **Aluminum** as Gate metal and Gate oxide as **Hafnium oxide** which has average dielectric constant of **23**.

First we are going to give the values of  $Q_i$  (Interface charge) and Doping concentration ( $N_D$ ) constant and vary the values corresponding to threshold voltage equation.

$$Q_i := 5 \cdot 10^{10} \cdot 1.6 \cdot 10^{-19} \cdot \frac{\text{C}}{\text{cm}^2}$$

Dielectric constant of **Hafnium oxide**  $\text{HfO}_2$

$$\epsilon_d := 23$$

The Doping Concentration is given by

$$N_D := 5 \cdot 10^{14} \cdot \frac{1}{\text{cm}^3}$$

$$k := 8.617 \cdot 10^{-5} \frac{\text{eV}}{\text{K}}$$

$$\text{Temp} := 300\text{K}$$

The fermi potential is given by the below eqn

$$\phi_F := \frac{k \cdot \text{Temp}}{q} \ln \left( \frac{N_D}{n_i} \right)$$

$$\phi_F = 0.269V$$

**Metal workfunction of Aluminum is given by**

$$\phi_m := 4.2 V$$

**Substrate workfunction is given by**

$$\phi_s := \chi_{\text{Si}} + \frac{E_g}{2} - \phi_F$$

**Metal Semiconductor work function is given by**

$$\phi_{\text{ms}} := \phi_m - \phi_s$$

$$\phi_{\text{ms}} = -0.131V$$

The **dielectric constant** of **Silicon** is given by

$$K_{\text{Si}} := 11.8$$



The **depletion width** is given by

$$W_d := 2 \cdot \sqrt{\frac{K_{Si} \cdot \epsilon_0 \cdot \phi_F}{q \cdot N_D}}$$

$$W_d = 1.186 \text{ } \mu\text{m}$$

The **depletion region charge Qd** is given by

$$Q_d := q \cdot N_D \cdot W_d$$

$$Q_d = 9.487 \times 10^{-9} \frac{\text{C}}{\text{cm}^2}$$

**Oxide Thickness (Tox)** is varied from **50 Angstrom** to **1000 Angstrom**

$$i := 0..6$$

$$t_{ox_i} :=$$

50·Angstrom
100·Angstrom
200·Angstrom
400·Angstrom
600·Angstrom
800·Angstrom
1000·Angstrom

$$C_{ox_i} := \frac{\epsilon_0 \cdot \epsilon_d}{t_{ox_i}}$$

$$C_{ox_i} =$$

4.073·10 <sup>6</sup>	$\frac{\text{pF}}{\text{cm}^2}$
2.036·10 <sup>6</sup>	
1.018·10 <sup>6</sup>	
5.091·10 <sup>5</sup>	
3.394·10 <sup>5</sup>	
2.546·10 <sup>5</sup>	
2.036·10 <sup>5</sup>	

The **Threshold Voltage ( $V_T$ )** for PMOS is given by

$$V_{T_i} := \phi_{ms} - \frac{Q_i}{C_{ox_i}} - \frac{Q_d}{C_{ox_i}} - 2 \cdot \phi_F$$

$V_{T_i} =$

-0.674
-0.678
-0.686
-0.704
-0.721
-0.738
-0.755

V

$$R_0 := \begin{pmatrix} -0.674 & 50 \\ -0.678 & 100 \\ -0.686 & 200 \\ -0.704 & 400 \\ -0.721 & 600 \\ -0.738 & 800 \\ -0.755 & 1000 \end{pmatrix}$$

The first N-MOSFET we are going to discuss is using **Aluminum** as Gate metal and Gate oxide as **Hafnium oxide**.

First we are going to give the values of  $Q_i$  (Interface charge) and Doping concentration

( $N_A$ ) constant and vary the values corresponding to threshold voltage equation.

$$Q_{i1} := 5 \cdot 10^{10} \cdot 1.6 \cdot 10^{-19} \cdot \frac{C}{cm^2}$$

Dielectric constant of Hafnium oxide  $HfO_2$  is different for different growth and mechanisms, the average dielectric constant from my literature survey is **23**

The **Doping Concentration** is given by

$$N_A := 5 \cdot 10^{14} \cdot \frac{1}{cm^3}$$

The **fermi potential** is given by the below eqn

$$\phi_{F1} := \frac{k \cdot Temp}{q} \ln \left( \frac{N_A}{n_i} \right)$$

$$\phi_{F1} = 0.269V$$

**Metal workfunction of Aluminum** is given by

**Substrate workfunction** is given by

$$\phi_{s1} := \chi_{Si} + \frac{E_g}{2} + \phi_{F1}$$

**Metal Semiconductor work function** is given by

$$\phi_{ms1} := \phi_m - \phi_{s1}$$

$$\phi_{ms1} = -0.669V$$

The **depletion width** is given by

$$W_{d1} := 2 \cdot \sqrt{\frac{K_{Si} \cdot \epsilon_o \cdot \phi_{F1}}{q \cdot N_A}}$$

$$W_d = 1.186 \mu\text{m}$$

The **depletion region charge Qd** is given by

$$Q_{d1} := q \cdot N_A \cdot W_d$$

$$Q_{d1} = 9.487 \times 10^{-9} \text{ C} \frac{1}{\text{cm}^2}$$

**Oxide Thickness (Tox)** is varied from **50 Angstrom** to **1000 Angstrom**

il := 0 .. 6

$t_{\text{ox},i1} =$

50	Angstrom
100	
200	
400	
600	
800	
1 · 10 <sup>3</sup>	

The oxide capacitance **Cox** is given by

$C_{\text{ox},i1} =$

4.073 · 10 <sup>6</sup>	$\frac{\text{pF}}{\text{cm}^2}$
2.036 · 10 <sup>6</sup>	
1.018 · 10 <sup>6</sup>	
5.091 · 10 <sup>5</sup>	
3.394 · 10 <sup>5</sup>	
2.546 · 10 <sup>5</sup>	
2.036 · 10 <sup>5</sup>	

The **Threshold Voltage for NMOS** is given by

$$V_{T1_{i1}} := \phi_{ms1} - \frac{Q_{i1}}{C_{ox_{i1}}} + \frac{Q_{d1}}{C_{ox_{i1}}} + 2 \cdot \phi_{F1}$$

$$V_{T1_{i1}} =$$

-0.13
-0.13
-0.129
-0.128
-0.126
-0.125
-0.123

V

$$R_1 := \begin{pmatrix} -0.13 & 50 \\ -0.13 & 100 \\ -0.129 & 200 \\ -0.128 & 400 \\ -0.126 & 600 \\ -0.125 & 800 \\ -0.123 & 1000 \end{pmatrix}$$

The first P-MOSFET we are going to discuss is using **Aluminum** as Gate metal and Gate oxide as **Hafnium oxide** which has average dielectric constant of **23**

First we are going to give the values of Qi (Interface charge) and Doping concentration (Nd) constant and vary the values corresponding to threshold voltage equation.

$$Q_{i2} := 5 \cdot 10^{10} \cdot 1.6 \cdot 10^{-19} \cdot \frac{C}{cm^2}$$

Dielectric constant of **Hafnium oxide** HfO<sub>2</sub>

The Doping Concentration is given by

$$N_{D1} := 10^{15} \cdot \frac{1}{cm^3}$$

The fermi potential is given by the below eqn

$$\phi_{F2} := \frac{k \cdot Temp}{q} \ln \left( \frac{N_{D1}}{n_i} \right)$$

$$\phi_{F2} = 0.287V$$

**Metal workfunction of Aluminum is given by**

**Substrate workfunction is given by**

$$\phi_{s2} := \chi_{Si} + \frac{E_g}{2} - \phi_{F2}$$

**Metal Semiconductor work function is given by**

$$\phi_{ms2} := \phi_m - \phi_{s2}$$

$$\phi_{ms2} = -0.113V$$

The **depletion width** is given by

$$W_{d2} := 2 \cdot \sqrt{\frac{K_{Si} \cdot \epsilon_0 \cdot \phi_{F2}}{q \cdot N_{D1}}} \quad W_{d2} = 0.866 \mu\text{m}$$

The **depletion region charge Qd** is given by

$$Q_{d2} := q \cdot N_{D1} \cdot W_{d2} \quad Q_d = 9.487 \times 10^{-9} \text{ C} \frac{1}{\text{cm}^2}$$

**Oxide Thickness (Tox)** is varied from **50 Angstrom** to **1000 Angstrom**

i2 := 0..6

$t_{\text{ox}_{i2}} =$

50	Angstrom
100	
200	
400	
600	
800	
1.10 <sup>3</sup>	

The oxide capacitance Cox is given by

$C_{\text{ox}_i} =$

4.073 · 10 <sup>6</sup>	$\frac{\text{pF}}{\text{cm}^2}$
2.036 · 10 <sup>6</sup>	
1.018 · 10 <sup>6</sup>	
5.091 · 10 <sup>5</sup>	
3.394 · 10 <sup>5</sup>	
2.546 · 10 <sup>5</sup>	
2.036 · 10 <sup>5</sup>	

The **Threshold Voltage (V<sub>T</sub>)** for PMOS is given by

$$V_{T2_{i2}} := \phi_{\text{ms}2} - \frac{Q_{i2}}{C_{\text{ox}_{i2}}} - \frac{Q_{d2}}{C_{\text{ox}_{i2}}} - 2 \cdot \phi_{F2}$$

$V_{T2_{i2}} =$

-0.693	V
-0.698	
-0.709	
-0.73	
-0.752	
-0.773	
-0.794	

$R_2 :=$

-0.693	50
-0.698	100
-0.709	200
-0.73	400
-0.752	600
-0.773	800
-0.794	1000

The first N-MOSFET we are going to discuss is using **Aluminum** as Gate metal and Gate oxide as **Hafnium oxide**.

First we are going to give the values of  $Q_i$  (Interface charge) and Doping concentration

( $N_A$ ) constant and vary the values corresponding to threshold voltage equation.

$$Q_{i3} := 5 \cdot 10^{10} \cdot 1.6 \cdot 10^{-19} \cdot \frac{C}{cm^2}$$

Dielectric constant of **Hafnium oxide**  $HfO_2$  is different for different growth and mechanisms, the average dielectric constant from my literature survey is **23**

The **Doping Concentration** is given by

$$N_{A1} := 10^{15} \cdot \frac{1}{cm^3}$$

The **fermi potential** is given by the below eqn

$$\phi_{F3} := \frac{k \cdot Temp}{q} \ln \left( \frac{N_{A1}}{n_i} \right) \quad \phi_{F3} = 0.287V$$

**Substrate workfunction** is given by

$$\phi_{s3} := \chi_{Si} + \frac{E_g}{2} + \phi_{F3}$$

**Metal Semiconductor work function** is given by

$$\phi_{ms3} := \phi_m - \phi_{s3}$$

$$\phi_{ms3} = -0.687V$$

The **depletion width** is given by

$$W_{d3} := 2 \cdot \sqrt{\frac{K_{Si} \cdot \epsilon_0 \cdot \phi_{F3}}{q \cdot N_{A1}}} \quad W_{d3} = 0.866 \mu m$$

The **depletion region charge Qd** is given by

$$Q_{d3} := q \cdot N_{A1} \cdot W_{d3} \quad Q_{d3} = 1.386 \times 10^{-8} C \frac{1}{cm^2}$$

**Oxide Thickness (Tox)** is varied from **50 Angstrom** to **1000 Angstrom**

i3 := 0..6

$$t_{ox_{i3}} =$$

50	Angstrom
100	
200	
400	
600	
800	
1·10 <sup>3</sup>	

The oxide capacitance is given by **Cox**

$$C_{ox_i} =$$

4.073·10 <sup>6</sup>	pF cm <sup>2</sup>
2.036·10 <sup>6</sup>	
1.018·10 <sup>6</sup>	
5.091·10 <sup>5</sup>	
3.394·10 <sup>5</sup>	
2.546·10 <sup>5</sup>	
2.036·10 <sup>5</sup>	

The **Threshold Voltage for NMOS** is given by

$$V_{T3_{i3}} := \phi_{ms3} - \frac{Q_{i3}}{C_{ox_{i3}}} + \frac{Q_{d3}}{C_{ox_{i3}}} + 2 \cdot \phi_{F3}$$

$$V_{T3_{i3}} =$$

-0.111	V
-0.11	
-0.107	
-0.101	
-0.096	
-0.09	
-0.084	

$$R_3 := \begin{pmatrix} -0.111 & 50 \\ -0.11 & 100 \\ -0.107 & 200 \\ -0.101 & 400 \\ -0.096 & 600 \\ -0.09 & 800 \\ -0.084 & 1000 \end{pmatrix}$$

The first P-MOSFET we are going to discuss is using **Aluminum** as Gate metal and Gate oxide as **Hafnium oxide** which has average dielectric constant of **23**.

First we are going to give the values of  $Q_i$  (Interface charge) and Doping concentration ( $N_d$ ) constant and vary the values corresponding to threshold voltage equation.

$$Q_{i4} := 5 \cdot 10^{10} \cdot 1.6 \cdot 10^{-19} \cdot \frac{\text{C}}{\text{cm}^2}$$

The **Doping Concentration** is given by

$$N_{D2} := 5 \cdot 10^{15} \cdot \frac{1}{\text{cm}^3}$$

The **fermi potential** is given by the below eqn

$$\phi_{F4} := \frac{k \cdot \text{Temp}}{q} \ln \left( \frac{N_{D2}}{n_i} \right) \quad \phi_{F4} = 0.329 \text{V}$$

**Substrate workfunction** is given by

$$\phi_{s4} := \chi_{\text{Si}} + \frac{E_g}{2} - \phi_{F4}$$

**Metal Semiconductor work function** is given by

$$\phi_{ms4} := \phi_m - \phi_{s4} \quad \phi_{ms4} = -0.071 \text{V}$$

The **depletion width** is given by

$$W_{d4} := 2 \cdot \sqrt{\frac{K_{\text{Si}} \cdot \epsilon_0 \cdot \phi_{F4}}{q \cdot N_{D2}}} \quad W_{d4} = 0.414 \mu\text{m}$$

The **depletion region charge Qd** is given by

$$Q_{d4} := q \cdot N_{D2} \cdot W_{d4}$$

$$Q_{d4} = 3.315 \times 10^{-8} \text{C} \cdot \frac{1}{\text{cm}^2}$$



Oxide Thickness (Tox) is varied from 50 Angstrom to 1000 Angstrom

$$i4 := 0 .. 6$$

$t_{ox_{i4}} =$

50
100
200
400
600
800
1·10 <sup>3</sup>

Angstrom

$C_{ox_i} =$

4.073·10 <sup>6</sup>
2.036·10 <sup>6</sup>
1.018·10 <sup>6</sup>
5.091·10 <sup>5</sup>
3.394·10 <sup>5</sup>
2.546·10 <sup>5</sup>
2.036·10 <sup>5</sup>

$\frac{pF}{cm^2}$

The Threshold Voltage (V<sub>T</sub>) for PMOS is given by

$$V_{T4_{i4}} := \phi_{ms4} - \frac{Q_{i4}}{C_{ox_{i4}}} - \frac{Q_{d4}}{C_{ox_{i4}}} - 2 \cdot \phi_{F4}$$

$V_{T4_{i4}} =$

-0.739
-0.749
-0.769
-0.81
-0.85
-0.89
-0.931

V

$R_4 :=$

-0.739	50
-0.749	100
-0.769	200
-0.81	400
-0.85	600
-0.89	800
-0.931	1000

The first N-MOSFET we are going to discuss is using **Aluminum** as Gate metal and Gate oxide as **Hafnium oxide**.

First we are going to give the values of Qi (Interface charge) and Doping concentration (Na) constant and vary the values corresponding to threshold voltage equation.

$$Q_{i5} := 5 \cdot 10^{10} \cdot 1.6 \cdot 10^{-19} \cdot \frac{C}{cm^2}$$

Dielectric constant of Hafnium oxide  $\text{HfO}_2$  is different for different growth and mechanisms, the average dielectric constant from my literature survey is **23**

The **Doping Concentration** is given by 
$$N_{A2} := 5 \cdot 10^{15} \cdot \frac{1}{\text{cm}^3}$$

The **fermi potential** is given by the below eqn 
$$\phi_{F5} := \frac{k \cdot \text{Temp}}{q} \ln \left( \frac{N_{A2}}{n_i} \right) \quad \phi_{F5} = 0.329 \text{ V}$$

**Substrate workfunction** is given by 
$$\phi_{s5} := \chi_{\text{Si}} + \frac{E_g}{2} + \phi_{F5}$$

**Metal Semiconductor work function** is given by 
$$\phi_{ms5} := \phi_m - \phi_{s5}$$
  

$$\phi_{ms5} = -0.729 \text{ V}$$

The **depletion width** is given by 
$$W_{d5} := 2 \cdot \sqrt{\frac{K_{\text{Si}} \cdot \epsilon_o \cdot \phi_{F5}}{q \cdot N_{A2}}} \quad W_{d5} = 0.414 \mu\text{m}$$

The **depletion region charge Qd** is given by 
$$Q_{d5} := q \cdot N_{A2} \cdot W_{d5} \quad Q_{d5} = 3.315 \times 10^{-8} \text{ C} \frac{1}{\text{cm}^2}$$

**Oxide Thickness (Tox)** is varied from **50 Angstrom** to **1000 Angstrom**

$i5 := 0 .. 6$

$t_{\text{ox}_i5} =$

50	Angstrom
100	
200	
400	
600	
800	
1·10 <sup>3</sup>	

The oxide capacitance **Cox** is given by

$C_{\text{ox}_i} =$

4.073·10 <sup>6</sup>	$\frac{\text{pF}}{\text{cm}^2}$
2.036·10 <sup>6</sup>	
1.018·10 <sup>6</sup>	
5.091·10 <sup>5</sup>	
3.394·10 <sup>5</sup>	
2.546·10 <sup>5</sup>	
2.036·10 <sup>5</sup>	

The **Threshold Voltage for NMOS** is given by equation  $V_{T5_{i5}} := \phi_{ms5} - \frac{Q_{i5}}{C_{ox_{i5}}} + \frac{Q_{d5}}{C_{ox_{i5}}} + 2 \cdot \phi_{F5}$

$$V_{T5_{i5}} = \begin{array}{|c|} \hline -0.065 \\ \hline -0.059 \\ \hline -0.047 \\ \hline -0.022 \\ \hline 2.852 \cdot 10^{-3} \\ \hline 0.028 \\ \hline 0.052 \\ \hline \end{array} \text{ V}$$

$$R_5 := \begin{pmatrix} -0.065 & 50 \\ -0.059 & 100 \\ -0.047 & 200 \\ -0.022 & 400 \\ 2.852 \cdot 10^{-3} & 600 \\ 0.028 & 800 \\ 0.052 & 1000 \end{pmatrix}$$

The first P-MOSFET we are going to discuss is using **Aluminum** as Gate metal and Gate oxide as **Hafnium oxide** which has average dielectric constant of **23**.

First we are going to give the values of  $Q_i$  (Interface charge) and Doping concentration ( $N_d$ ) constant and vary the values corresponding to threshold voltage equation.

$$Q_{i6} := 5 \cdot 10^{10} \cdot 1.6 \cdot 10^{-19} \cdot \frac{\text{C}}{\text{cm}^2}$$

The **Doping Concentration** is given by  $N_{D3} := 10^{16} \cdot \frac{1}{\text{cm}^3}$

The **fermi potential** is given by the below eqn  $\phi_{F6} := \frac{k \cdot \text{Temp}}{q} \ln \left( \frac{N_{D3}}{n_i} \right)$   $\phi_{F6} = 0.347 \text{ V}$

**Substrate workfunction** is given by  $\phi_{s6} := \chi_{Si} + \frac{E_g}{2} - \phi_{F6}$

**Metal Semiconductor work function** is given by  $\phi_{ms6} := \phi_m - \phi_{s6}$   
 $\phi_{ms6} = -0.053 \text{ V}$

The **depletion width** is given by  $W_{d6} := 2 \cdot \sqrt{\frac{K_{Si} \cdot \epsilon_0 \cdot \phi_{F6}}{q \cdot N_{D3}}}$   $W_{d6} = 0.301 \mu\text{m}$

The **depletion region charge Qd** is given by  $Q_{d6} := q \cdot N_{D3} \cdot W_{d6}$   $Q_{d6} = 4.815 \times 10^{-8} \text{ C} \cdot \frac{1}{\text{cm}^2}$

Oxide Thickness ( $T_{ox}$ ) is varied from 50 Angstrom to 1000 Angstrom

$$i6 := 0..6$$

$$t_{ox_{i6}} =$$

50	Angstrom
100	
200	
400	
600	
800	
$1 \cdot 10^3$	

The oxide capacitance  $C_{ox}$  is given by

$$C_{ox_i} =$$

$4.073 \cdot 10^6$	$\frac{\text{pF}}{\text{cm}^2}$
$2.036 \cdot 10^6$	
$1.018 \cdot 10^6$	
$5.091 \cdot 10^5$	
$3.394 \cdot 10^5$	
$2.546 \cdot 10^5$	
$2.036 \cdot 10^5$	

The Threshold Voltage of NMOS is given by

$$V_{T6_{i6}} := \phi_{ms6} - \frac{Q_{i6}}{C_{ox_{i6}}} - \frac{Q_{d6}}{C_{ox_{i6}}} - 2 \cdot \phi_{F6}$$

$$V_{T6_{i6}} =$$

-0.76	V
-0.774	
-0.802	
-0.857	
-0.912	
-0.967	
-1.022	

$$R_6 := \begin{pmatrix} -0.76 & 50 \\ -0.774 & 100 \\ -0.802 & 200 \\ -0.857 & 400 \\ -0.912 & 600 \\ -0.967 & 800 \\ -1.022 & 1000 \end{pmatrix}$$

The first N-MOSFET we are going to discuss is using **Aluminum** as Gate metal and Gate oxide as **Hafnium oxide**.

First we are going to give the values of Qi (Interface charge) and Doping concentration (Na) constant and vary the values corresponding to threshold voltage equation.

$$Q_{i7} := 5 \cdot 10^{10} \cdot 1.6 \cdot 10^{-19} \cdot \frac{C}{cm^2}$$

Dielectric constant of Hafnium oxide HfO<sub>2</sub> is different for different growth and mechanisms, the average dielectric constant from my literature survey is **23**

The **Doping Concentration** is given by  $N_{A3} := 10^{16} \cdot \frac{1}{cm^3}$

The **fermi potential** is given by the below eqn  $\phi_{F7} := \frac{k \cdot Temp}{q} \ln\left(\frac{N_{A3}}{n_i}\right)$   $\phi_{F7} = 0.347V$

**Substrate workfunction** is given by  $\phi_{s7} := \chi_{Si} + \frac{E_g}{2} + \phi_{F7}$

**Metal Semiconductor work function** is given by  $\phi_{ms7} := \phi_m - \phi_{s7}$   $\phi_{ms7} = -0.747V$

The **depletion width** is given by  $W_{d7} := 2 \cdot \sqrt{\frac{K_{Si} \cdot \epsilon_o \cdot \phi_{F7}}{q \cdot N_{A3}}}$   $W_{d7} = 0.301 \mu m$

The **depletion region charge Qd** is given by  $Q_{d7} := q \cdot N_{A3} \cdot W_{d7}$   $Q_d = 9.487 \times 10^{-9} C \frac{1}{cm^2}$

**Oxide Thickness (Tox)** is varied from **50 Angstrom** to **1000 Angstrom**

$$i7 := 0..6$$

$t_{ox_{i7}} =$

50	Angstrom
100	
200	
400	
600	
800	
1.10 <sup>3</sup>	

The oxide capacitance is given by **Cox**

$$C_{ox_i} = \begin{array}{|c|} \hline 4.073 \cdot 10^6 \\ \hline 2.036 \cdot 10^6 \\ \hline 1.018 \cdot 10^6 \\ \hline 5.091 \cdot 10^5 \\ \hline 3.394 \cdot 10^5 \\ \hline 2.546 \cdot 10^5 \\ \hline 2.036 \cdot 10^5 \\ \hline \end{array} \frac{\text{pF}}{\text{cm}^2}$$

The **Threshold voltage of NMOS** is given by the following equation

$$V_{T7_{i7}} := \phi_{ms7} - \frac{Q_{i7}}{C_{ox_{i7}}} + \frac{Q_{d7}}{C_{ox_{i7}}} + 2 \cdot \phi_{F7}$$

$$V_{T7_{i7}} =$$

-0.043
-0.034
-0.014
0.026
0.065
0.104
0.144

V

$$R_7 := \begin{pmatrix} -0.043 & 50 \\ -0.034 & 100 \\ -0.014 & 200 \\ 0.026 & 400 \\ 0.065 & 600 \\ 0.104 & 800 \\ 0.144 & 1000 \end{pmatrix}$$

The first P-MOSFET we are going to discuss is using **Aluminum** as Gate metal and Gate oxide as **Hafnium oxide** which has average dielectric constant of **23**.

First we are going to give the values of Qi (Interface charge) and Doping concentration (Nd) constant and vary the values corresponding to threshold voltage equation.

$$Q_{i8} := 5 \cdot 10^{10} \cdot 1.6 \cdot 10^{-19} \cdot \frac{\text{C}}{\text{cm}^2}$$

The **Doping Concentration** is given by  $N_{D4} := 5 \cdot 10^{16} \cdot \frac{1}{\text{cm}^3}$

The **fermi potential** is given by the below eqn  $\phi_{F8} := \frac{k \cdot \text{Temp}}{q} \ln\left(\frac{N_{D4}}{n_i}\right)$   $\phi_{F8} = 0.388 \text{ V}$

**Substrate workfunction** is given by  $\phi_{s8} := \chi_{Si} + \frac{E_g}{2} - \phi_{F8}$

**Metal Semiconductor work function** is given by  $\phi_{ms8} := \phi_m - \phi_{s8}$   
 $\phi_{ms8} = -0.012 \text{ V}$

The **depletion width** is given by  $W_{d8} := 2 \cdot \sqrt{\frac{K_{Si} \cdot \epsilon_o \cdot \phi_{F8}}{q \cdot N_{D4}}}$   $W_{d8} = 0.142 \text{ } \mu\text{m}$

The **depletion region charge Qd** is given by  $Q_{d8} := q \cdot N_{D4} \cdot W_{d8}$   $Q_d = 9.487 \times 10^{-9} \text{ C} \cdot \frac{1}{\text{cm}^2}$

**Oxide Thickness (Tox)** is varied from **50 Angstrom** to **1000 Angstrom**

i8 := 0..6

$t_{ox_{i8}} =$

50	Angstrom
100	
200	
400	
600	
800	
1 · 10 <sup>3</sup>	

The oxide capacitance Cox is given by

$C_{ox_i} =$

4.073 · 10 <sup>6</sup>	$\frac{\text{pF}}{\text{cm}^2}$
2.036 · 10 <sup>6</sup>	
1.018 · 10 <sup>6</sup>	
5.091 · 10 <sup>5</sup>	
3.394 · 10 <sup>5</sup>	
2.546 · 10 <sup>5</sup>	
2.036 · 10 <sup>5</sup>	

The **Threshold voltage of PMOS** is given by

$$V_{T8_{i8}} := \phi_{ms8} - \frac{Q_{i8}}{C_{ox_{i8}}} - \frac{Q_{d8}}{C_{ox_{i8}}} - 2 \cdot \phi_{F8}$$

$$V_{T8_{i8}} =$$

-0.818
-0.848
-0.908
-1.028
-1.148
-1.267
-1.387

V

$$R_8 := \begin{pmatrix} -0.818 & 50 \\ -0.848 & 100 \\ -0.908 & 200 \\ -1.028 & 400 \\ -1.148 & 600 \\ -1.267 & 800 \\ -1.387 & 1000 \end{pmatrix}$$

The first N-MOSFET we are going to discuss is using **Aluminum** as Gate metal and Gate oxide as **Hafnium oxide**.

First we are going to give the values of Qi (Interface charge) and Doping concentration

(Na) constant and vary the values corresponding to threshold voltage equation.

$$Q_{i9} := 5 \cdot 10^{10} \cdot 1.6 \cdot 10^{-19} \cdot \frac{C}{cm^2}$$

**Dielectric constant of Hafnium oxide HfO<sub>2</sub>** is different for different growth and mechanisms, the **average dielectric constant** from my literature survey is **23**

The **Doping Concentration** is given by

$$N_{A4} := 5 \cdot 10^{16} \cdot cm^{-3}$$

The **fermi potential** is given by the below eqn

$$\phi_{F9} := \frac{k \cdot Temp}{q} \ln \left( \frac{N_{A4}}{n_i} \right) \quad \phi_{F9} = 0.388 V$$

**Substrate workfunction** is given by

$$\phi_{s9} := \chi_{Si} + \frac{E_g}{2} + \phi_{F9}$$

**Metal Semiconductor work function** is given by

$$\phi_{ms9} := \phi_m - \phi_{s9}$$

$$\phi_{ms9} = -0.788 V$$



The **depletion width** is given by 
$$W_{d9} := 2 \cdot \sqrt{\frac{K_{Si} \cdot \epsilon_0 \cdot \phi_{F9}}{q \cdot N_{A4}}} \quad W_{d9} = 0.142 \mu\text{m}$$

The **depletion region charge Qd** is given by 
$$Q_{d9} := q \cdot N_{A4} \cdot W_{d9} \quad Q_{d9} = 1.139 \times 10^{-7} \text{ C} \frac{1}{\text{cm}^2}$$

**Oxide Thickness (Tox)** is varied from **50 Angstrom** to **1000 Angstrom**

$i9 := 0..6$

$t_{\text{ox}_i9} =$

50	Angstrom
100	
200	
400	
600	
800	
1 · 10 <sup>3</sup>	

The oxide capacitance **Cox** is given by

$C_{\text{ox}_i} =$

4.073 · 10 <sup>6</sup>	$\frac{\text{pF}}{\text{cm}^2}$
2.036 · 10 <sup>6</sup>	
1.018 · 10 <sup>6</sup>	
5.091 · 10 <sup>5</sup>	
3.394 · 10 <sup>5</sup>	
2.546 · 10 <sup>5</sup>	
2.036 · 10 <sup>5</sup>	

The **threshold voltage of NMOS** is given by the following equation

$$V_{T9_{i9}} := \phi_{\text{ms}9} - \frac{Q_{i9}}{C_{\text{ox}_i9}} + \frac{Q_{d9}}{C_{\text{ox}_i9}} + 2 \cdot \phi_{F9}$$

$V_{T9_{i9}} =$

0.014	V
0.04	
0.092	
0.196	
0.3	
0.404	
0.508	

$R_9 :=$

0.014	50
0.04	100
0.092	200
0.196	400
0.3	600
0.404	800
0.508	1000

The first P-MOSFET we are going to discuss is using **Aluminum** as Gate metal and Gate oxide as **Hafnium oxide** which has average dielectric constant of **23**.

First we are going to give the values of  $Q_i$  (Interface charge) and Doping concentration ( $N_d$ ) constant and vary the values corresponding to threshold voltage equation.

$$Q_{i10} := 5 \cdot 10^{10} \cdot 1.6 \cdot 10^{-19} \cdot \frac{C}{cm^2}$$

The **Doping Concentration** is given by 
$$N_{D5} := 10^{17} \cdot \frac{1}{cm^3}$$

The **fermi potential** is given by the below eqn 
$$\phi_{F10} := \frac{k \cdot Temp}{q} \ln \left( \frac{N_{D5}}{n_i} \right) \quad \phi_{F10} = 0.406 V$$

**Substrate workfunction** is given by 
$$\phi_{s10} := \chi_{Si} + \frac{E_g}{2} - \phi_{F10}$$

**Metal Semiconductor work function** is given by 
$$\phi_{ms10} := \phi_m - \phi_{s10}$$

$$\phi_{ms10} = 6.187 \times 10^{-3} V$$

The **depletion width** is given by 
$$W_{d10} := 2 \cdot \sqrt{\frac{K_{Si} \cdot \epsilon_0 \cdot \phi_{F10}}{q \cdot N_{D5}}} \quad W_{d10} = 0.103 \mu m$$

The **depletion region charge Qd** is given by 
$$Q_{d10} := q \cdot N_{D5} \cdot W_{d10} \quad Q_{d10} = 1.648 \times 10^{-7} C \frac{1}{cm^2}$$

Oxide Thickness ( $T_{ox}$ ) is varied from 50 Angstrom to 1000 Angstrom

i10 := 0..6

$t_{ox_{i10}} =$	
50	Angstrom
100	
200	
400	
600	
800	
$1 \cdot 10^3$	

The oxide capacitance is given by **Cox**

$C_{ox_1} =$

$4.073 \cdot 10^6$	$\frac{\text{pF}}{\text{cm}^2}$
$2.036 \cdot 10^6$	
$1.018 \cdot 10^6$	
$5.091 \cdot 10^5$	
$3.394 \cdot 10^5$	
$2.546 \cdot 10^5$	
$2.036 \cdot 10^5$	

The **threshold voltage of PMOS** is given by the equation

$$V_{T10_{i10}} := \phi_{ms10} - \frac{Q_{i10}}{C_{ox_{i10}}} - \frac{Q_{d10}}{C_{ox_{i10}}} - 2 \cdot \phi_{F10}$$

$V_{T10_{i10}} =$

-0.849
-0.891
-0.976
-1.146
-1.315
-1.485
-1.655

V

$$R_{10} := \begin{pmatrix} -0.849 & 50 \\ -0.891 & 100 \\ -0.976 & 200 \\ -1.146 & 400 \\ -1.315 & 600 \\ -1.485 & 800 \\ -1.655 & 1000 \end{pmatrix}$$

The first N-MOSFET we are going to discuss is using **Aluminum** as Gate metal and Gate oxide as **Hafnium oxide**.

First we are going to give the values of  $Q_i$  (Interface charge) and Doping concentration ( $N_A$ ) constant and vary the values corresponding to threshold voltage equation.

$$Q_{i11} := 5 \cdot 10^{10} \cdot 1.6 \cdot 10^{-19} \cdot \frac{C}{cm^2}$$

**Dielectric constant of Hafnium oxide** HfO<sub>2</sub> is different for different growth and mechanisms, the **average dielectric constant** from my literature survey is **23**

The **Doping Concentration** is given by  $N_{A5} := 10^{17} \cdot cm^{-3}$

The **fermi potential** is given by the below eqn  $\phi_{F11} := \frac{k \cdot Temp}{q} \ln\left(\frac{N_{A5}}{n_i}\right)$   $\phi_{F11} = 0.406V$

**Substrate workfunction** is given by  $\phi_{s11} := \chi_{Si} + \frac{E_g}{2} + \phi_{F11}$

**Metal Semiconductor work function** is given by  $\phi_{ms11} := \phi_m - \phi_{s11}$

$$\phi_{ms11} = -0.806V$$

The **depletion width** is given by  $W_{d11} := 2 \cdot \sqrt{\frac{K_{Si} \cdot \epsilon_0 \cdot \phi_{F11}}{q \cdot N_{A5}}}$   $W_{d11} = 0.103 \mu m$

The **depletion region charge Qd** is given by  $Q_{d11} := q \cdot N_{A5} \cdot W_{d11}$

$$Q_{d11} = 1.648 \times 10^{-7} C \frac{1}{cm^2}$$

**Oxide Thickness (Tox)** is varied from **50 Angstrom** to **1000 Angstrom**

$$i11 := 0..6$$

$$t_{ox_{i11}} =$$

50	Angstrom
100	
200	
400	
600	
800	
1·10 <sup>3</sup>	

The oxide capacitance **Cox** is given by

$$C_{ox_i} =$$

4.073·10 <sup>6</sup>	$\frac{\text{pF}}{\text{cm}^2}$
2.036·10 <sup>6</sup>	
1.018·10 <sup>6</sup>	
5.091·10 <sup>5</sup>	
3.394·10 <sup>5</sup>	
2.546·10 <sup>5</sup>	
2.036·10 <sup>5</sup>	

The **Threshold voltage of NMOS** is given by the following equation

$$V_{T11_{i11}} := \phi_{ms11} - \frac{Q_{i11}}{C_{ox_{i11}}} + \frac{Q_{d11}}{C_{ox_{i11}}} + 2 \cdot \phi_{F11}$$

$$V_{T11_{i11}} =$$

0.045	V
0.083	
0.16	
0.314	
0.468	
0.622	
0.776	

$$R_{11} := \begin{pmatrix} 0.045 & 50 \\ 0.083 & 100 \\ 0.16 & 200 \\ 0.314 & 400 \\ 0.468 & 600 \\ 0.622 & 800 \\ 0.776 & 1000 \end{pmatrix}$$

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