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Finite Element Method Modeling Of Advanced Electronic Devices

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FINITE ELEMENT METHOD MODELING OF ADVANCED ELECTRONIC DEVICES

by

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ABSTRACT

In this dissertation, we use finite element method together with other numerical techniques to study advanced electron devices. We study the radiation properties in electron waveguide structure with multi-step discontinuities and soft wall lateral confinement. Radiation mechanism and conditions are examined by numerical simulation of dispersion relations and transport properties. The study of geometry variations shows its significant impact on the radiation intensity and direction. In particular, the periodic corrugation structure exhibits strong directional radiation. This interesting feature may be useful to design a nano-scale transmitter, a communication device for future nano-scale system.

Non-quasi-static effects in AC characteristics of carbon nanotube field-effect transistors are examined by solving a full time-dependent, open-boundary Schrödinger equation. The non-quasi-static characteristics, such as the finite channel charging time, and the dependence of small signal transconductance and gate capacitance on the frequency, are explored. The validity of the widely used quasi-static approximation is examined. The results show that the quasi-static approximation overestimates the transconductance and gate capacitance at high frequencies, but gives a more accurate value for the intrinsic cut-off frequency over a wide range of bias conditions.

The influence of metal interconnect resistance on the performance of vertical and lateral power MOSFETs is studied. Vertical MOSFETs in a D^2PAK and DirectFET package, and lateral MOSFETs in power IC and flip chip are investigated as the case studies. The impact of various layout patterns and material properties on $R_{DS(on)}$ will provide useful guidelines for practical vertical and lateral power MOSFETs design.

To my beloved Parents, my Brother and my Wife *Chong*

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ACKNOWLEDGMENTS

I am deeply indebted to my advisor and mentor, Prof. Thomas X. Wu, for his insightful guidance. It is whole life experience for me to be a student of him. This work would not have been possible without his sharing experience, his dedication and his encouragement. It is him who teaches me how to describe a complicated problem in a simple and elegant way. It is him who teaches me how to use computational tools to understand the interesting physics deeply. It is him who spends a lot of time to train me to be a professional researcher. All of these will be invaluable assets for my future life.

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It is a great pleasure to work in the Applied Electromagnetics & High Speed Electronics group at UCF. I would like to thank all the group members for their kindness and enthusiasm to build a harmonic atmosphere for study and research.

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CHAPTER ONE: INTRODUCTION

Semiconductor devices have dominated electronics for several decades, since the invention of the first transistor in the late 1940's. Two major research trends accompany the spectacular development of semiconductor devices. One is to improve and optimize the existing technology to meet the requirements of the emerging applications [1], e.g. metal interconnection or packaging technology for MOSFETs [2, 3]. The other one is to develop alternative device structures to break though the ultimate physical scaling limits of traditional devices especially MOSFET [4], e.g. electron waveguides [5] and carbon nanotube transistors [6]. During these two trends, numerical simulations play essential roles, not only to improve the device performance but also to understand or discover the unknown device physics for novel device design. Among various numerical methods, finite element method is favored for electronic device simulations because of the geometrical flexibility and the ease with which the equations can be assembled for complicated problems.

1.1. Finite Element Method

The finite element method (FEM) is a numerical technique for obtaining approximate solutions to boundary value problems of mathematical physics [7]. The method has a history of about 50 years. It was first proposed in the 1940s and its use began in the 1950s for aircraft design. Thereafter, the method was developed and applied extensively to problems of structural analysis and increasingly to problems in other fields. Today, the finite element method has become recognized as a general method widely applicable to engineering and mathematical problems. The principle of this method is to replace an entire continuous domain by a number of

subdomains in which the unknown function is represented by simple interpolation functions with unknown coefficients. Thus, the original boundary-value problem with an infinite number of degrees of freedom is converted into a problem with a finite number of degrees of freedom, or in other words, the solution of the entire system is approximated by a finite number of unknown coefficients. Then a system of algebraic equations is obtained by applying the Ritz variational or Galerkin procedure, and finally, solution of the boundary-value problem is achieved by solving the system of equations. Therefore, a finite element analysis of a boundary-value problem should include the following basic steps [7]:

1. Discretization or subdivision of the domain
2. Selection of the interpolation functions
3. Formulation of the system of equations
4. Solution of the system of equations

We will demonstrate these steps in greater detail in chapter 2 – 4 for each kind of devices.

The following features of FEM are worth noting:

1. The piecewise approximation of the physical field (continuum) on finite elements provides good precision even with simple approximating functions. Simply increasing the number of elements can achieve increasing precision.
2. The locality of the approximation leads to sparse equation systems for a discretized problem. This helps to ease the solution of problems having very large numbers of nodal unknowns.
3. Easily applied to complex, irregular-shaped objects composed of several different materials and having complex boundary conditions.

4. Applicable to steady-state, time dependent and eigenvalue problems and applicable to linear and nonlinear problems.
5. One method can solve a wide variety of problems, including problems in solid mechanics, fluid mechanics, chemical reactions, semiconductor devices, electromagnetics, quantum mechanics, biomechanics, heat transfer and acoustics, etc.

1.2 Organization of the Dissertation

In the dissertation, we will focus on finite element method simulations of three kinds of electronics device according to these two trends: electron waveguides, carbon nanotube transistors and power MOSFETs.

In Chapter 2, we study the properties of electron radiation in electron waveguide devices with multi-step discontinuities and soft wall lateral confinement. A numerical approach based on FEM and rigorous mode-matching method is described. Radiation mechanism and conditions are examined by numerical simulation of dispersion relations and transport properties. In particular, the impact of geometry on the radiation intensity and direction of the structure is examined in detail. Physical properties governing the radiation characteristics are discussed.

In Chapter 3, we focus on comprehensive study of high frequency response for CNT FETs by numerical modeling. Non-quasi-static (NQS) effects in AC characteristics of carbon nanotube field-effect transistors (CNTFETs) are examined for the first time by solving a full time-dependent, open-boundary Schrödinger equation. The NQS characteristics, such as the finite channel charging time, and the dependence of small signal transconductance and gate

capacitance on the frequency, are explored. The validity of the widely used quasi-static approximation is examined.

In Chapter 4, we introduce a three-dimensional finite element analysis (FEA) approach to quantitatively study the influence of metal interconnect resistance on the performance of lateral and vertical power MOSFET with ultra low on-resistance for the first time. A new FEA modeling methodology and customized FEA software are developed. The $R_{DS(on)}$ of vertical MOSFETs in a D^2PAK and DirectFET package, and lateral MOSFETs in power IC and flip chip are improved using the FEA software by optimizing the device layout patterns and material properties, which will provide useful guidelines for practical vertical and lateral power MOSFETs design. The scaling and "debiasing" effects of power MOSFET are also investigated.

In Chapter 5, the conclusion is drawn.

CHAPTER TWO: RADIATION PROPERTIES IN ELECTRON WAVEGUIDE

2.1 Introduction

Recently, there have been a lot of research efforts to investigate nano-scale systems, which have the features of high density, low power consumption, and high computation speed [4–24]. One of the challenges is the communication between the nano-scale components in the system, such as nano-sensors and nano-machines. Conventional communication approaches by optical or electromagnetic propagation are inadequate because of limitations of system size as well as the medium in which the nano-scale components are deployed [10]. Other schemes are needed to enable the interconnectivity among nano-scale systems and I/O with the macro world. Furthermore, suitable nano-scale transmitting and receiving devices are indispensable to the systems. Specifically, radiation properties are of great significance in nano-scale transmitter design. In this chapter, we propose a nano-scale transmitter device using soft walled electron waveguide structure with multi-step discontinuities and explore its radiation performance in terms of radiation intensity and direction.

Electron waveguide is a nano-structure in which the electron wave is locally trapped and is guided along an arbitrary direction. It is well known that the wavelike behavior of electrons in the nano-scale structures is dominant so that the transport of electrons through the heterostructure device is analogous to the propagation of electromagnetic waves in dielectric waveguides [25]. It may be feasible to design an electron antenna in nano-scale similar to electromagnetic wave antenna in macro-scale. To date, most of the investigations with simple

geometries and hard wall confinement have given many fundamental properties of electron conduction in these systems, but in realistic electron waveguides, where the boundaries are defined via electrostatic confinement from metal gates the geometries and the lateral confinement potential profile are complicated [15]. Electrons transporting through the structure with finite-height confinement potential (soft wall) have the possibility of escaping from the channel. This escaping (radiation) phenomenon is more observable if the structure has discontinuities along the channel. Discontinuity in electron waveguide structure is very important not only for the unavoidable surface roughness problem caused by the manufacture process, but also for some structures in which discontinuity is introduced intentionally. The optimization of the structure is to minimize the electron radiation in the former, whereas to maximize the radiation for specific usages in the latter. As a result, a thorough study of radiation properties is essential in both cases. Although several papers dealing with the discontinuity problem either analytically or numerically have been published [20-25], so far there has no systematic study of radiation properties of soft walled electron waveguide structures with multi-step discontinuities.

In this chapter, we make an attempt to study the radiation mechanism and to determine their relation to the geometry of the structure. The chapter is organized as follows. In section 2.2, theoretical equations governing the electron wave in the device are introduced. Mode matching method based on microwave transmission line theory is used to model step discontinuity in terms of the boundary conditions. A detailed finite element method (FEM) formalism to solve the system model numerically is given in section 2.3. In section 2.4, radiation mechanism and conditions are examined by numerical simulation of dispersion relations and transport properties. In section 2.5, geometry dependent radiation intensity and direction are analyzed for double step discontinues and periodic corrugation structures.

2.2 Theoretical Model

The electron waveguide as Fig. 2.1(a) can be decomposed into uniform waveguides and the junctions connecting them. To describe the behavior of electrons in electron waveguides with multi-step discontinuities and soft wall lateral confinement, Schrödinger wave equation with finite lateral boundary condition is used for uniform waveguides and rigorous mode-matching method is used for the junctions.

Assuming electron motion in a uniform electron waveguide section is ballistic (without any scattering), the electron wave is governed by the time-independent Schrödinger equation under the effective mass approximation given as [8]

$$\nabla \cdot (\frac{1}{m^*} \nabla \Psi) + \frac{2}{\hbar^2}(E - U)\Psi = 0 \tag{2.1}$$

where Ψ is electron wave function, E is the electron's total energy, U is the potential energy, m^* is effective mass and $\hbar$ is the reduced Planck constant.

For simplicity, we assume wave function Ψ is invariant along the y direction $(\partial / \partial y = 0)$ and propagating along the z direction as shown in Fig. 2.1 (a). Thus, Ψ can be expressed as

$$\Psi(x, z) = \Phi(x) e^{-jk_z z} \tag{2.2}$$

The wave function for continuity of probability flow [8, 11, 20] is

$$\psi(x, z) = \frac{\hbar k_z}{m^*(x)} \Phi(x) e^{-jk_z z} \tag{2.3}$$

where transverse wave function $\Phi(x)$ satisfies the following 1-D Sturm-Liouville generalized eigenvalue problem

$$\left\{\frac{d}{dx}\frac{1}{m^*(x)}\frac{d}{dx}+\frac{2}{\hbar^2}[E-U(x)]\right\}\Phi_m(x)=k_{z(m)}^2\frac{1}{m^*(x)}\Phi_m(x) \tag{2.4}$$

subject to the boundary conditions

$$\Phi_m(0)=\Phi_m(h)=0 \tag{2.5}$$

An infinite set of eigensolutions of Eq. (4) constitutes wave modes (energy subbands) of the electron waveguide. Eigenvalue $k_{z(m)}$ is the longitudinal propagation constant of the mth mode and a corresponding eigenfunction $\Phi_m(x)$ is the mth mode transverse wave function. The eigenfunction set Φ_m satisfies the orthonormalization relation as

$$\left\langle \Phi_m \left| \frac{1}{m^*} \right| \Phi_n \right\rangle = \int_0^h \frac{1}{m^*(x)}\Phi_m(x)\Phi_n(x)dx=\delta_{mn} \tag{2.6}$$

In order to analyze the discontinuities in electron waveguide, mode matching method based on transmission line model is adopted as the follows [20]

$$\begin{cases}\Psi(x,z)=\sum_{m=1}^{\infty}V_m(z)\Phi_m(x)\\ \psi(x,z)=\sum_{m=1}^{\infty}I_m(z)\frac{\sqrt{E}}{m^*(x)}\Phi_m(x)\end{cases} \tag{2.7}$$

The total wave function in each uniform waveguide can be expressed in terms of the superposition of a complete set of mode functions as indicated in Fig. 2.1. In the transmission line model, k_{zm} is the propagation wavenumber of the mth mode, the characteristic impedance of the mth mode in the z direction is

$$Z_m=\frac{\sqrt{E}}{\hbar k_{zm}} \tag{2.8}$$

At the step discontinuity between two waveguides i and i+1, the two wave functions must be continuous such as

$$\Psi(x, z^{(i,i+1)^-}) = \Psi(x, z^{(i,i+1)^+}) \tag{2.9}$$

$$\psi(x, z^{(i,i+1)^-}) = \psi(x, z^{(i,i+1)^+}) \tag{2.10}$$

Combing boundary conditions Eq. (2.9) and Eq. (2.10) with orthonormalizatoin relation Eq. (2.6), we can get

$$\begin{bmatrix} V^i \\ I^i \end{bmatrix} = M^{(i,i+1)} \begin{bmatrix} V^{i+1} \\ I^{i+1} \end{bmatrix} \tag{2.11}$$

$$M^{(i,i+1)} = \begin{bmatrix} P^{(i,i+1)} & 0 \\ 0 & Q^{(i,i+1)} \end{bmatrix} \tag{2.12}$$

where

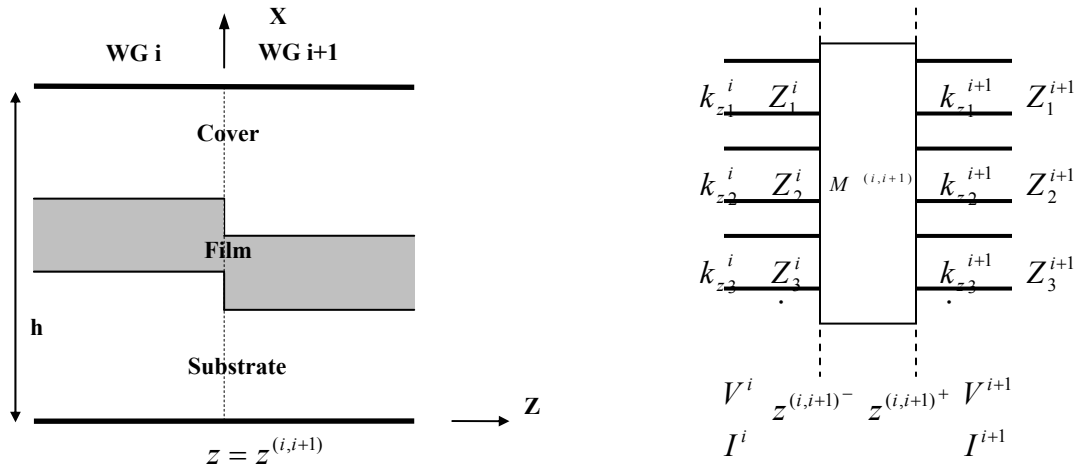
$$\begin{aligned} P_{mn}^{(i,i+1)} &= \left\langle \Phi_m^i \,|\, \frac{1}{m^{*(i)}} \,|\, \Phi_n^{i+1} \right\rangle \\ &= \int_0^h \frac{1}{m^{*(i)}(x)} \Phi_m^i(x) \Phi_n^{i+1}(x) dx \end{aligned} \tag{2.13}$$

$$\begin{aligned} Q_{mn}^{(i,i+1)} &= \left\langle \Phi_m^i \,|\, \frac{1}{m^{*(i+1)}} \,|\, \Phi_n^{i+1} \right\rangle \\ &= \int_0^h \frac{1}{m^{*(i+1)}(x)} \Phi_m^i(x) \Phi_n^{i+1}(x) dx \end{aligned} \tag{2.14}$$

We can then obtain the scattering matrix S of the step discontinuity by the conversion between transmission (ABCD) matrix M and scattering matrix S [28].

In our approach, the electron waveguide with multistep discontinuities is first decomposed into uniform waveguides and the junctions connecting them. Eigenvalue and eigenfuction sets found from Eq. (2.4) of each uniform waveguide are used for mode matching

of junctions to get scattering matrix of each junction. Then, the scattering matrix of the whole structure is obtained by cascading the individual scattering matrix of the uniform parts and junction parts.



(a) (b)

Fig. 2.1 Junction of two uniform electron waveguide and its equivalent transmission line model.

2.3 FEM Formalism

Finite element method (FEM) [7] is adopted to solve the system models. The wave function can be approximated by the node value in each element as

$$\Phi(x) = \sum_{e=1}^{N_e} \sum_{i=1}^{2} \Phi_i^e N_i^e(x) \tag{2.15}$$

where 1-D linear interpolation functions are given by

$$N_1^e(x) = \begin{cases} \dfrac{x_2^e - x}{x_2^e - x_1^e}, & x_1^e < x < x_2^e \\ 0 & otherwise \end{cases} \tag{2.16}$$

$$N_2^e(x) = \begin{cases} \dfrac{x - x_1^e}{x_2^e - x_1^e}, & x_1^e < x < x_2^e \\ 0 & otherwise \end{cases} \tag{2.17}$$

Using Galerkin's method [7] with weighting function $W_m(x) = N_j^e(x)$, we obtain

$$\sum_{i=1}^{2} \Phi_i^e \{ \int_{x_1^e}^{x_2^e} [-\frac{1}{m^*(x)} \frac{dN_i^e(x)}{dx} \frac{dN_j^e(x)}{dx} + \frac{2}{\hbar^2}(E - U(x)) - \frac{1}{m^*(x)} k_z^2 N_i^e(x) N_j^e(x)] dx \}$$

$$+ [\frac{1}{m^*(x)} \frac{d\Phi}{dx}\Big|_{x=h} - \frac{1}{m^*(x)} \frac{d\Phi}{dx}\Big|_{x=0}] = 0 \tag{2.18}$$

We can change it to elemental matrix form

$$[A_{ij}^e]\{\Phi_j^e\} + [end] = k_z^2 [D_{ij}^e]\{\Phi_j^e\} \tag{2.19}$$

where

$$A_{ij}^e = \int_{x_1^e}^{x_2^e} [-\frac{1}{m^*(x)} \frac{dN_i^e(x)}{dx} \frac{dN_j^e(x)}{dx} + \frac{2}{\hbar^2}(E - U(x))] dx \tag{2.20}$$

$$D_{ij}^e = \int_{x_1^e}^{x_2^e} \frac{1}{m^*(x)} N_i^e(x) N_j^e(x) dx \tag{2.21}$$

$$[end] = \begin{cases} -\dfrac{1}{m^*(x)} \dfrac{d\Phi}{dx}\Big|_{x=0} & at\ boundary\ node\ x = x_1^1 = 0 \\ \dfrac{1}{m^*(x)} \dfrac{d\Phi}{dx}\Big|_{x=h} & at\ boundary\ node\ x = x_2^{N_e} = h \\ 0 & otherwise \end{cases} \tag{2.22}$$

Each wave function mode is normalized as

$$\overline{\Phi_m} = \Phi_m / \sqrt{A_m} \tag{2.23}$$

where

$$A_m = \int_0^h \frac{1}{m^*(x)} \Phi_m(x)\Phi_m(x)dx$$

$$= \sum_{e=1}^{N_e} \frac{1}{m^*(x_1^e)} \begin{bmatrix} \Phi_{m1}^{\ e} & \Phi_{m2}^{\ e} \end{bmatrix} \begin{bmatrix} \int_{x_1^e}^{x_2^e} N_1^e(x)N_1^e(x)dx & \int_{x_1^e}^{x_2^e} N_1^e(x)N_2^e(x)dx \\ \int_{x_1^e}^{x_2^e} N_1^e(x)N_2^e(x)dx & \int_{x_1^e}^{x_2^e} N_1^e(x)N_1^e(x)dx \end{bmatrix} \begin{bmatrix} \Phi_{m1}^{\ e} \\ \Phi_{m2}^{\ e} \end{bmatrix} \quad (2.24)$$

2.4 Radiation Mechanism and Conditions

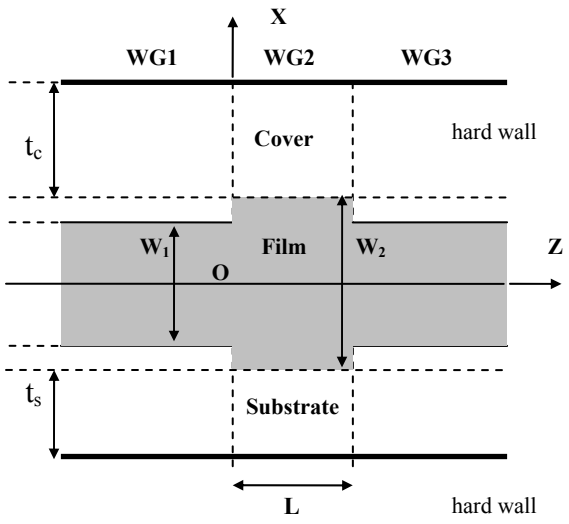


Fig. 2.2 Double step continuities structure configurations.

Fig.2.2 gives a three layered electron waveguide with double step discontinuities in 2-D $GaAs/Al_rGa_{1-r}As$ semiconductor heterostructure material configurations (as Fig. 2.2), where hard walls with infinite potential are placed far enough away from the film surface as FEM boundaries to discrete the continuous spectrum of radiation modes [21]. Electron potential energy U and electron effective mass m^* for Al concentration ratio r are given by [20]

$$U = 0.7731r \quad (eV) \tag{2.25}$$

$$m^* = (0.067 + 0.083r)m_0 \ (kg) \tag{2.26}$$

where m_0 is the rest mass of an electron, and r in three layers is given as $(r_s, r_f, r_c) = (0.2, 0, 0.2)$, which results in a quantum well potential profile with symmetrical finite potential barriers.

With the incidence of the guided mode from the left side of waveguide 1, non-guided modes including the propagating radiation modes are excited at the junctions of the three uniform waveguides because of the discontinuities. On such a discontinuous structure, the fields vary with the successive positions along it. Thus it is necessary to consider rigorously the field continuity conditions on the whole boundary surface of the structure by taking into account the effect not only of the conversion of power among the guided modes and the scattering of power into the radiation modes but also of the coupling of the power of the radiation mode into both guided modes and the other radiation modes. As a result, a complete set of modes analysis is necessary to explain the radiation phenomena.

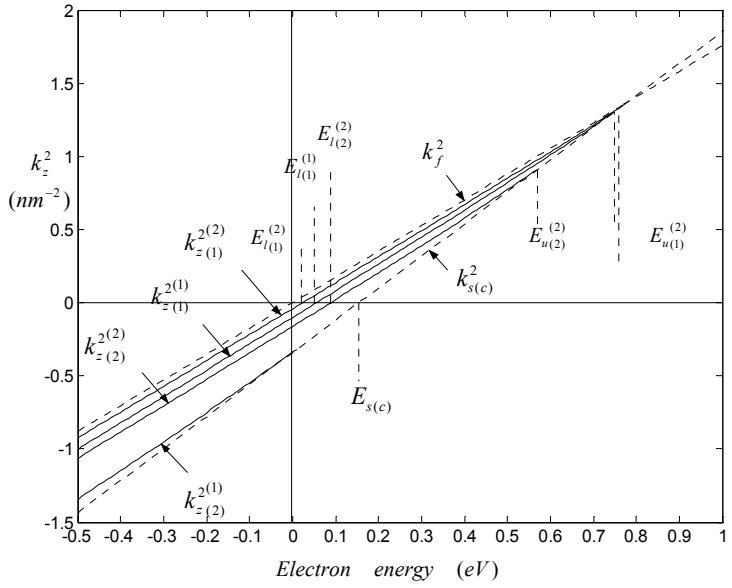


Fig. 2.3 Dispersion curves of the first two guide modes in WG1 and WG2

Dispersion relations (Electron energy vs. k_z^2) for the first two modes of the uniform waveguides 1 and 2 in Fig. 2.2 are depicted in Fig. 2.3, where $W_2 = 2W_1 = 11.3068\,nm$. The propagating guided wave modes [21] are determined by wave number (k_s, k_f, k_c) in the three layer regions as

$$0 \le k_z^2 \le k_f^2, k_z^2 > k_s^2 \text{ and } k_z^2 > k_c^2 \tag{2.27}$$

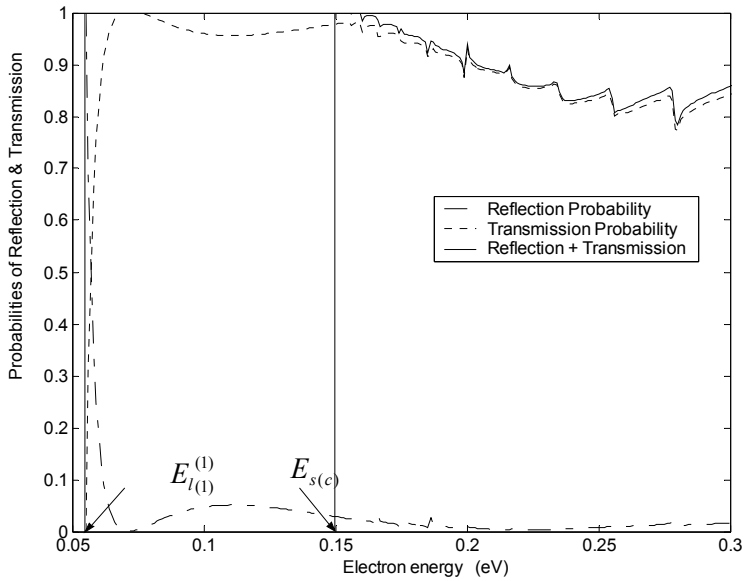
where $k_i^2 = \frac{2m_i^*}{\hbar^2}(E - U_i) \quad i = s, f, c$.

As indicated in Fig. 2.3, two types of cutoff energy can be found from Eq. (2.27) as low cutoff energy $E_{l(m)}^{(i)}$ and upper cutoff energy $E_{u(m)}^{(i)}$ for the m_{th} mode in waveguide i. As shown in Fig. 2.3, during the simulated energy range, both waveguides have the dispersion curves of the first two normal modes, whereas only waveguide 1 is a single guided mode structure.

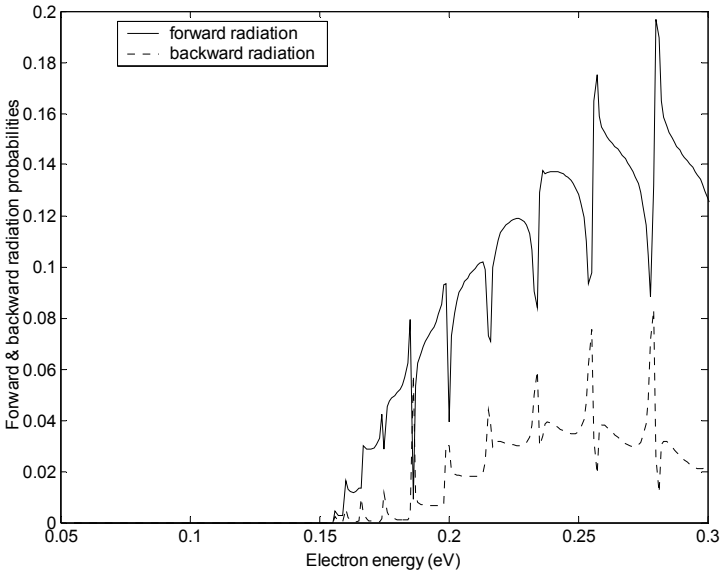
When the guided mode is incident from the left side of waveguide 1, the transport properties are given in Fig. 2.4 (a) as a function of electron energy, where $L = W_2$. Transport properties can be classified according to three energy range cases: 1) When $E < E_{l(1)}^{(1)}$, as shown in Fig. 2.3, no propagating guided mode exists in three waveguides and no transmission occurs; 2) When $E_{l(1)}^{(1)} \le E \le E_{s(c)}$, as indicated in Fig. 2.3, guided modes exist in three waveguides, but no radiation mode is propagating. So the addition of guided mode reflection and transmission is equal to 1; 3) When $E > E_{s(c)}$, as found in Fig. 2.3, propagating radiation modes begin to appear. As a result, the addition of guided mode reflection and transmission is smaller than 1.

Radiation probabilities as shown in Fig. 2.4 (b), coinciding with the result of transport properties, are greater than zero at electron energy range $E > E_{s(c)}$. Forward radiation probability is larger than the backward one. During the simulated energy range, radiations tend to increase with the increasing energy in large energy range, but oscillate in short energy range.

Radiation mechanism can be further explained by the probabilities distribution of electron along x direction derived from the transverse wave mode function as Fig. 2.5. As can be seen from Fig. 2.5(a), for the fundamental mode, electron wave propagates mainly in film region. And the electron wave penetrates into substrate and cover regions near upper cutoff energy. Fig. 2.5(b) plots the case for the first high order mode in waveguide 1. We can find that propagating mode occurs when electron energy is greater than $E_{s(c)}$. Since waveguide 1 is a single guided mode structure, such propagating mode is due to the radiation of electron wave into the substrate and cover regions. It will result in the escaping of electrons for soft walled waveguide structure in practice.

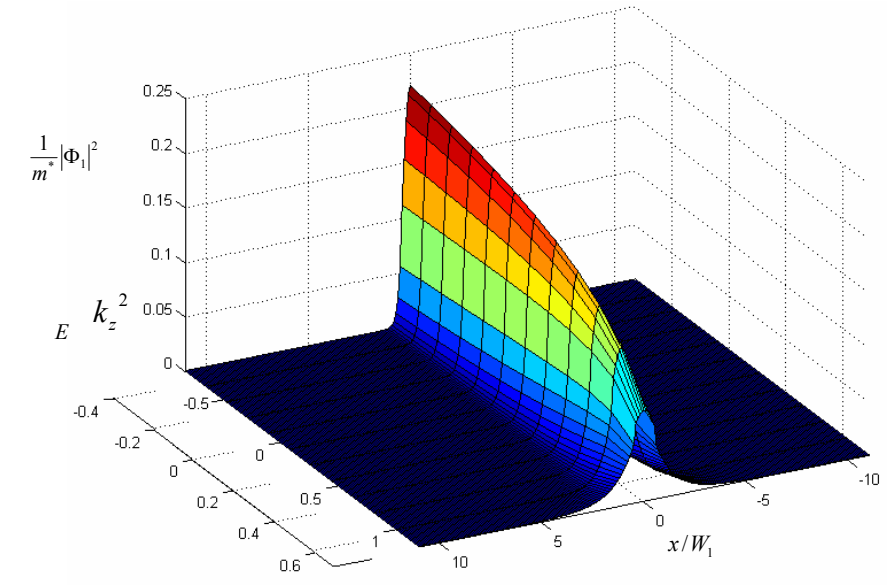


(a)



(b)

Fig. 2.4 (a) Guided mode transport properties as a function of electron energy of the structure in Fig. 2.2. (b) Guided mode radiation characteristics as a function of electron energy of the structure in Fig. 2.2.



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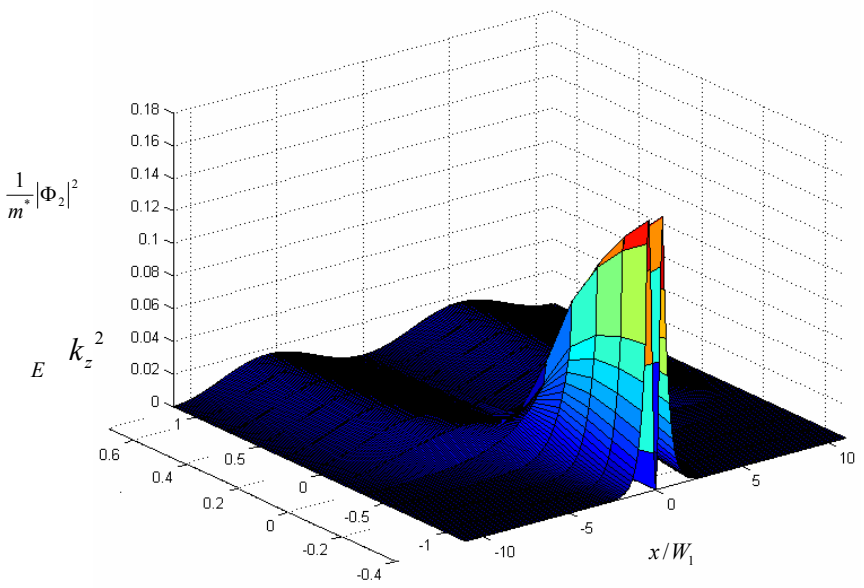


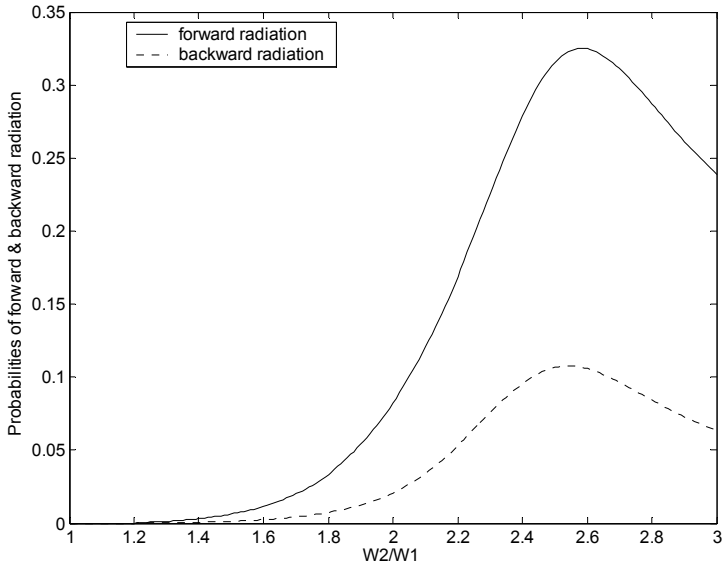
(b)

Fig. 2.5 (a) k_z^2 and E dependence of the transverse wave function for the fundamental mode in WG 1. (b) k_z^2 and E dependence of the transverse wave function for the first high order mode in WG 1.

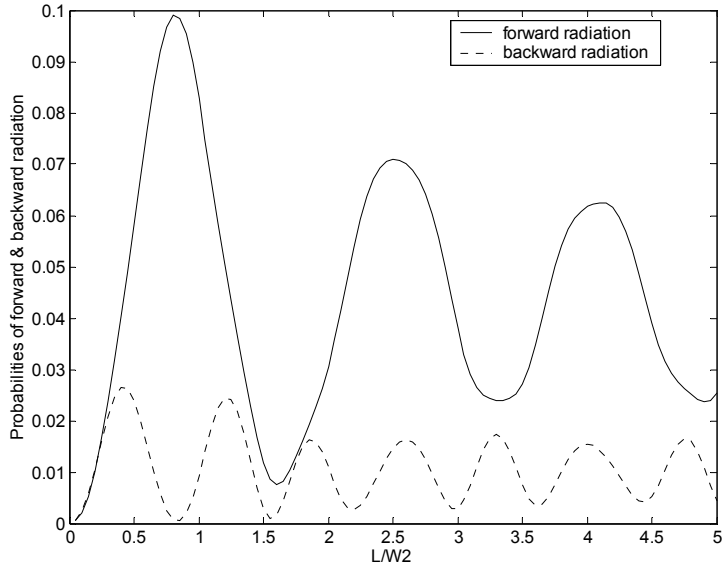
2.5 Geometry Dependent Radiation Intensity and Direction

As we can expect, if there are no discontinuities along the film layer, there will be no radiation mode excited. Geometry should have strong impact on the radiation properties, which are further investigated for specific energy as shown in Fig. 2.6 in terms of the degree of step discontinuity and the width of middle waveguide for double step discontinuities structure

As indicated in Fig. 2.6(a), guided mode transports through the structure without radiation for small step discontinuity. With the increasing of step discontinuity, guided mode radiates more until it reaches maximum radiation point at specific step discontinuity. After that point, radiations decrease with the increasing of step discontinuity. As shown in Fig. 2.6(b), radiation characteristics are simulated as a function of the width of wavguide 2 for E = 0.2 eV. Guided mode will transmit without radiation at very small width as can be expected. With the increasing of width, radiations tend to oscillate. This phenomenon can be explained by the phase shift of the electron wave propagating in the middle waveguide. The oscillation period can be estimated by the half guide wavelength of the major guided mode in the WG 2. From Fig. 2.3, k_Z^2 of the major guided mode in the WG 2 is $0.4\,nm^{-2}$, which is equal to the half guide wavelength of $0.45\,W_2$. The deviation of the period is caused by the existing of high order guided mode in WG 2.



(a)



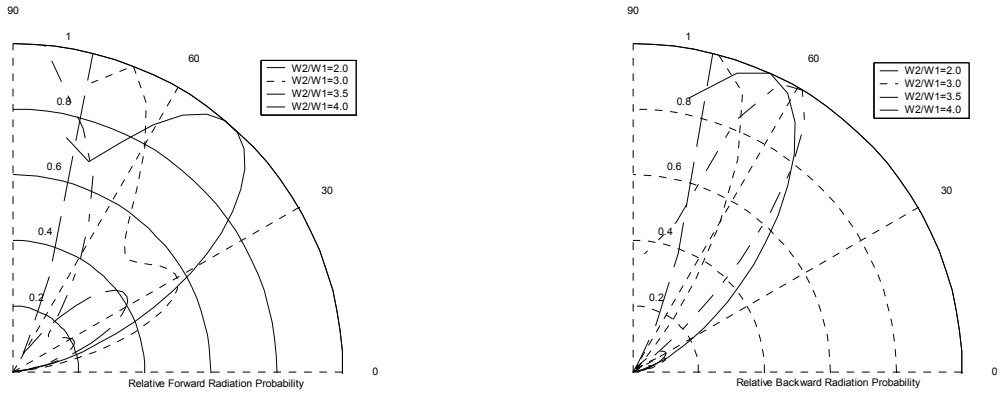
(b)

Fig. 2.6 (a) Guided mode radiation characteristics as a function of W2/W1 at E = 0.2 eV. (b) Guided mode radiation characteristics as a function of WG 2 width L at E = 0.2 eV.

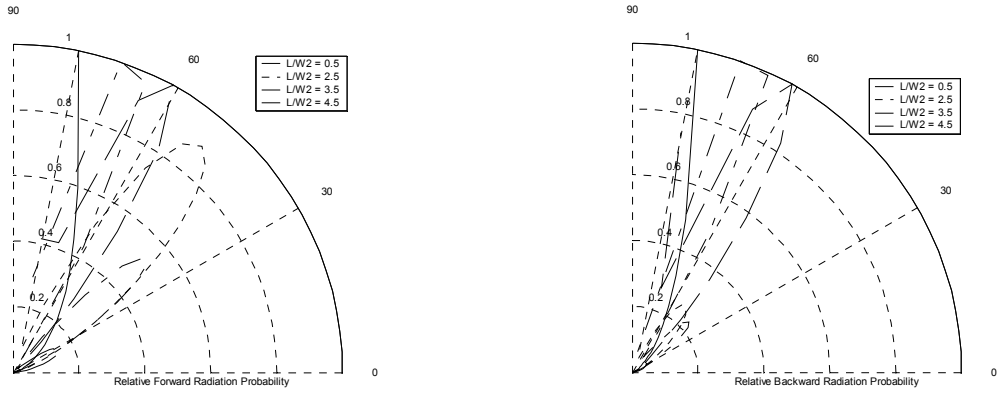
In addition to the magnitude, the space radiation direction properties are of great significance. It is possible to control the radiation direction and intensity by adjusting the geometry. Radiation pattern is investigated with respect to W_1/W_2 and L/W_2 as shown in Fig. 2.7. The results show for the double step discontinuity structure, the radiation direction is not quite selective although the radiation direction and intensity is still a strong function of the geometry.

In order to take advantage of the possible high radiation direction selectivity, let us next consider the periodic corrugations of finite length [27] as shown in the inset of Fig. 2.8(a). This structure is given by the cascade connection of a finite number of networks given by Fig. 2.2. By applying our approach described in section 2.2, we can obtain the numerical results shown in Fig. 2.8. These examples are obtained for a structure with the dimensions indicated in the inset and for a different number N_c of corrugations. In order to explain the results physically, the parameters of the structure are chosen so that only the major guiding mode propagates in each uniform waveguide section and we consider that this mode incident from the left-hand side excites the structure. Fig. 2.8(a) shows the reflected probability of the major guiding mode where N_c = 10 and 20 corrugations, as a function of the normalized period $2L/\lambda_f$. λ_f is the wavelength of the electron wave in the film layer. Fig. 2.8 (b) shows the forward and backward radiation probability. If the structure under consideration is infinite in length, the center of the Bragg reflection can be calculated by $2(k_{Z1}L_1 + k_{Z2}L_2) = 2n\pi$. From the structure dimensions, we can derive that the center of the first Bragg reflection is at $2L/\lambda_f = 0.55$, while the second Bragg reflection is at $2L/\lambda_f = 1.10$. As seen from Fig. 2.8 (a), it found that strong reflection indeed appears at around $2L/\lambda_f = 0.55$, corresponding to the center of the first Bragg reflection region and also that significant radiation occurs between the first Bragg reflection and the second Bragg

reflection region. However there are many subsidiary reflection peaks even outside the first Bragg reflection region, and the radiation still occurs in the first Bragg reflection region with a complicated feature arising from the finite length of the periodic structure.

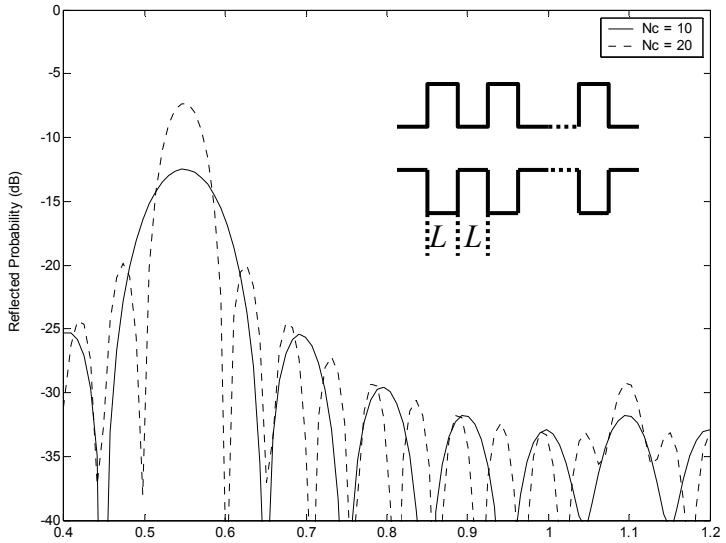


(a)

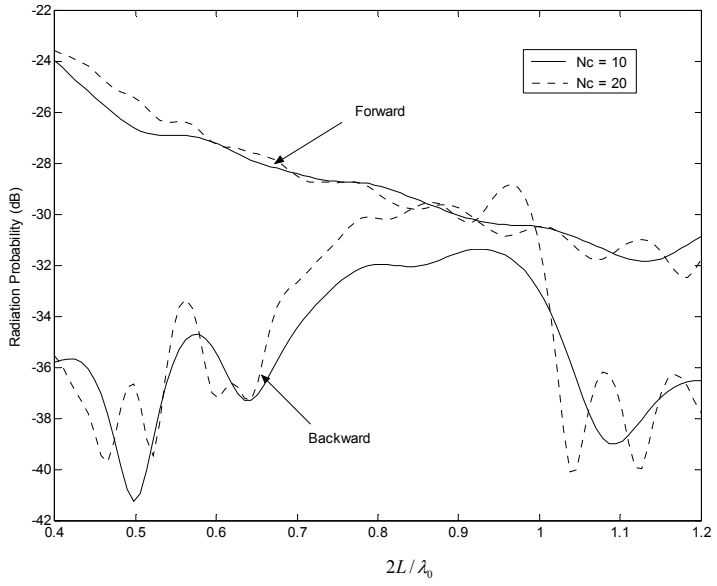


(b)

Fig. 2.7 Radiation patterns for the double step discontinuity structure (a) vs. W2/W1 with L = W2 and E = 0.2 eV : (left) Forward, and (right) Backward. (b) vs. L/W2 with W2 = 2W1 and E = 0.2 eV: (left) Forward, and (right) Backward.



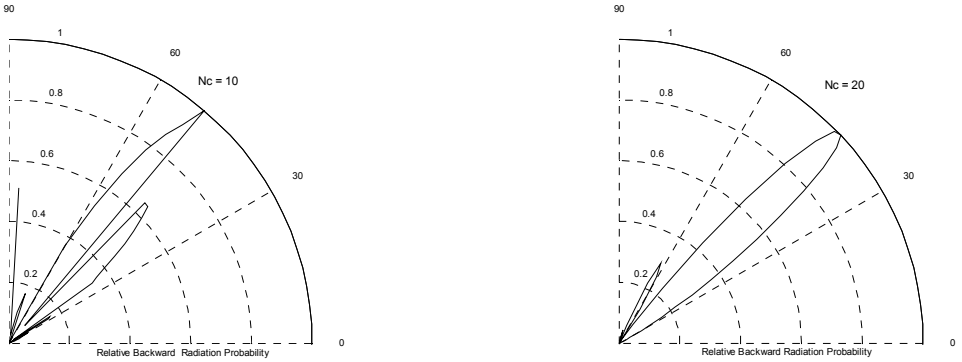
(a)



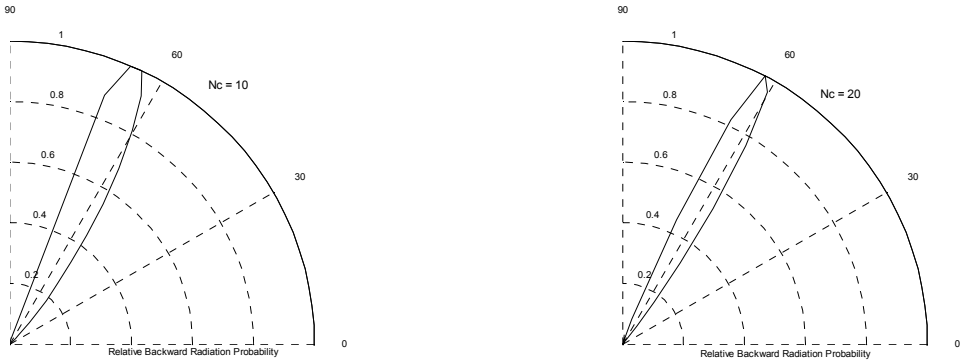
(b)

Fig. 2.8 The periodic structure with a finite number N_c of corrugations: (a) reflected probability of the incident major guided mode and (b) radiation probabilities vs. the normalize period $2L/\lambda_f$.

The backward radiation patterns of the periodic structure are simulated as shown in Fig. 2.9 for structures with $2L/\lambda_f = 0.7, 0.8, \textit{and}\ 0.9$ in the case where N_c = 10 and 20. The peak value is normalized to unity for each radiation pattern, and the axes along $\theta = 0°$ and $90°$ coincide with the x and the negative z directions, respectively. The effect of the finite length is indeed clearly seen in the narrowing main lobe as the number of corrugations increases, but more significantly, such an effect results in complicated spurious lobes. However, the direction of each maximum lob is in good agreement with each other ($\theta = 41°$ for Fig. 2.9 (a), $\theta = 60°$ for (b) and $\theta = 73°$ for (c)). If the structure under consideration is infinite in length, the radiation direction can be calculated by $\theta = \cos^{-1}\left|\dfrac{k_{z(1)}^{(1)}k_{z(1)}^{(2)} - \dfrac{\pi}{L}}{k_{s(c)}}\right|$, ($\theta = 41.36°$ for Fig. 2.9 (a), $\theta = 60.54°$ for (b) and $\theta = 73.11°$ for (c)). The numerical simulation matches the theoretical analysis very well.



(a)



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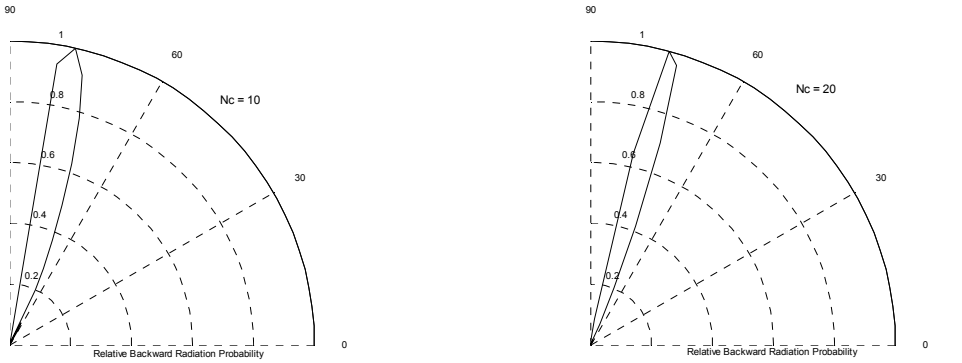


(c)

Fig. 2.9 Radiation patterns for the periodic structure with a finite number N_c of corrugations: (a) normalized period $2L/\lambda_f = 0.7$ (b) normalized period $2L/\lambda_f = 0.8$, (c) normalized period $2L/\lambda_f = 0.9$. (left) Nc = 10, and (right) Nc = 20.

CHAPTER THREE: TIME-DEPENDENT QUANTUM TRANSPORT AND NON-QUASI-STATIC EFFECTS IN CARBON NANOTUBE FILED EFFECT TRANSISTOR

3.1 Introduction

Since the invention of the first transistor in 1947, critical dimensions of the transistor devices have decreased dramatically. The limits of scaling CMOS have been revised several times over the past decades with novel materials and device structures. Today, silicon CMOS has been scaled down to the nanoscale regime, which is close to the fundamental limit imposed by quantum mechanical effects. Novel device technologies, which may play important roles at the scaling limit of silicon CMOS and beyond, are attracting extensive research interests. Various potential nanoelectronic transistors such as carbon nanotube field effect transistors (CNTFETs) [29,30], single electron transistors [31], double gate MOSFETs [32], new channel material FETs [33], schottky barrier FETs [34], and quantum dot transistors [35], are extensively investigated. Since carbon nanotubes (CNTs) were reported in 1991 [36], significant progress on their electrical, mechanical and chemical properties has been witnessed [37, 38]. Among numerous potential applications of CNTs, such as transistors, sensors, displays, and electro-mechanical devices, CNTFETs have attracted much attention due to their smallness and unique electrical properties. CNTFETs with performance greatly exceeding MOSFETs have been reported [39, 40]. Simple circuit applications beyond a single device, for example, the inverters, logic gates, and ring oscillators, have also been realized [41]. Rapid advances of both experimental and theoretical work show that CNTFET is becoming a promising candidate for future nanoscale electronic devices [37, 38].

Due to one-dimensional transport properties of CNT even at room temperature, the modeling of CNT devices, which need to consider quantum transport effects, can be quite different from conventional devices. Much research has been devoted to the development of CNTFETs experimentally or simulationally [39-44]. Recently, AC characteristics of carbon nanotube field-effect transistors (FETs) are attracting extensive research interests due to their high mobility and near ballistic transport. Seemingly, the relatively high quantum resistance (25 kΩ) of the device may restrict the operational speed of CNTFETs. However, ultra-short channel length and generally small capacitance of CNTFETs result in small carrier transit time [45]. Consequently, CNTFETs may have a potential for very high frequency applications. Generally speaking, the maximum frequency at which current gain can be achieved is given by the transconductance g_m divided by the gate source capacitance C_{gs} . If we use the largest transconductance measured to date of 20 μs , the predictions are very promising, suggesting that a nanotube transistor with THz cutoff frequencies should be possible [45]. Appenzeller and Frank performed the pioneering experimental work on the AC characteristics of CNTFETs with a frequency up to 580MHz [46]. The measurements with a frequency of 2.6GHz [47] and 10GHz [48] were subsequently reported. Very recently, a five stage CNT ring oscillators with a frequency of 52MHz has been successfully demonstrated [49] and AC characterization of a CNTFET up to 50GHz was reported [50]. The ultimate goal is to benefit from the intrinsic high speed of CNTFET and achieve the theoretically predicted THz intrinsic frequency. Self-consistent, quasi-static (QS) quantum simulations have been applied to assess the high-frequency performance [51, 52]. The validity of the QS approximation at very high frequencies, however, should be questioned. Previous studies have shown that non quasi-static effects (NQS) play an

important role on the characteristics of conventional high-speed transistors [53]. Little, however, is known about the NQS effects in carbon nanotube transistors.

In this work, NQS effects in ballistic CNTFETs are investigated for the first time by solving a full time-dependent open boundary Schrödinger equation for CNTFETs using the finite difference time domain (FDTD) method [42]. The dependence of small signal transconductance and gate capacitance on the frequency of the applied bias is examined. The intrinsic cut-off frequency (f_T), a device metric important for radio-frequency (RF) applications, is computed using the full time-dependent simulations. The validity of the widely used QS approximation is examined.

3.2 Device Physics of CNTFETS at High Frequency

Dynamic and nonlinear quantum transport in nanostructures is a challenging subject since a consistent treatment requires knowledge of the nonequilibrium state. In contrast, the linear static response (DC conductance) of a nanostructure is determined by the equilibrium state only. Once the equilibrium potential is known, the transmission and reflection probabilities of a nanostructure completely specify its DC conductance. That is the principle of Landauer-Buttiker formula [54, 55] which is widely adopted in nanoelectronic device simulations. However, the dynamic response and the nonlinear response of a nanostructure depend on the charge and current distributions established away from equilibrium (non quasi-static effects). Buttiker and co-workers [56-58] succeeded in extending the Landauer approach to mesoscopic systems assuring overall current and charge conservation under ac conditions in the low-frequency limit, where any kinetic electron time associated with the device is much shorter than the reciprocal of

the external ac frequency. Very recently, some researchers [59, 60] propose to overcome this limit by using a dynamic quantum mechanical (QM) transmission coefficient or time-dependent transport approach for high-frequency conditions.

However, at present there are no detailed theoretical models for the high frequency properties of carbon nanotube transistors. Self-consistent, quasi-static (QS) quantum simulations have been applied to assess the high-frequency performance [51, 52]. In QS approach, an equivalent small-signal model is extracted as shown in Fig. 3.1. The parameters of the equivalent circuit model for the intrinsic CNTFET, which is shown within the dashed rectangle in Fig. 3.1., are obtained by running self-consistent quantum simulations and numerically evaluating the derivatives. The intrinsic gate capacitance, C_g and the transconductance, g_m, are

$$C_g = \left.\frac{\partial Q_{ch}}{\partial V_g}\right|_{Vd}, \; g_m = \left.\frac{\partial I_d}{\partial V_g}\right|_{Vd} \tag{3.1}$$

where Q_{ch} is the total charge in the CNT channel, and I_d is the source-drain current.

Additional elements like $C_{pS}(C_{pD})$ and $R_{ps}(R_{pd})$ are added the equivalent circuit to take parasitic capacitances and resistance into account. The extrinsic cut-off frequency is given by

$$f_T \approx \frac{1}{2\pi}\frac{g_m}{C_g + C_{pS} + C_{pD}} \tag{3.2}$$

The intrinsic cut-off frequency excluding parasitic capacitance is given by

$$f_T \approx \frac{1}{2\pi}\frac{g_m}{C_g} \tag{3.3}$$

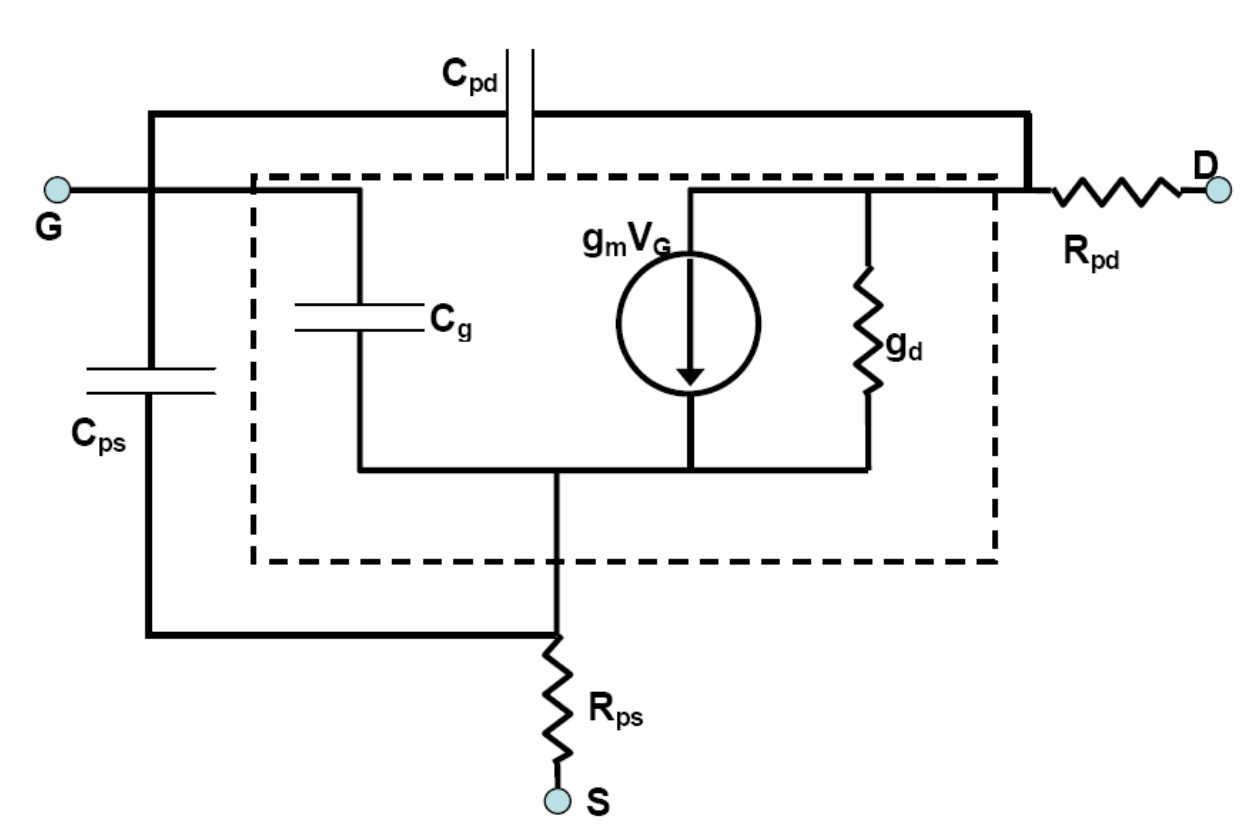


Fig. 3.1. A small-signal equivalent circuit model for a CNTFET in QS approach [52].

The validity of the QS approximation at very high frequencies, however, should be questioned. The quasi-static treatment works well when then signal varies slowly compared to the time constant determined by the intrinsic gate capacitance and channel inductance. It is the case when extrinsic cut-off frequency is assessed. But the kinetic inductance, omitted in the equivalent circuit model, may begin to play an important role when the intrinsic cut-off frequency is assessed [52]. In addition, the QS approach fails to explore non quasi-static effects (NQS) in carbon nanotube transistor. A new approach is needed to solve this problem.

3.3 Modeling Approach

3.3.1 General Methodology

A general description of our methodology is shown in Fig. 3.2. The active quantum device model is based on the quantum transport equation. The moving carriers inside the device become a source of electromagnetic (EM) fields. These EM fields, in turn, affect carrier transport. The coupling between the two models is thus established by using fields obtained from the solutions of Maxwell's equations in the active quantum device model to calculate the current densities inside the device [61, 62]. These current densities are used to update the electric and magnetic fields. The problem is solved in the time domain because the carrier transport processes are highly nonlinear.

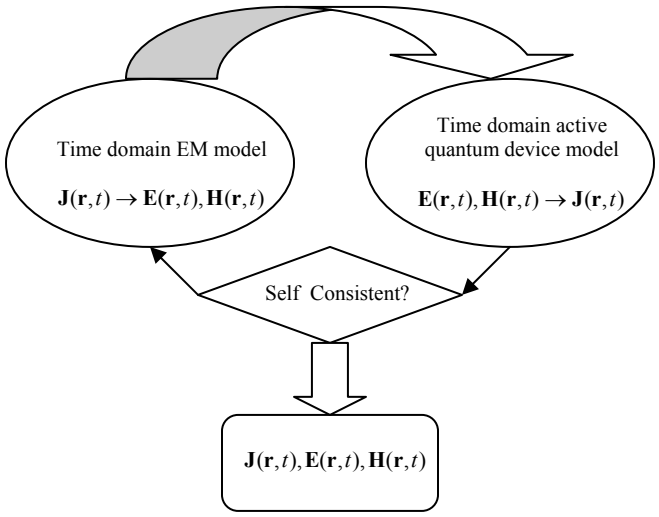
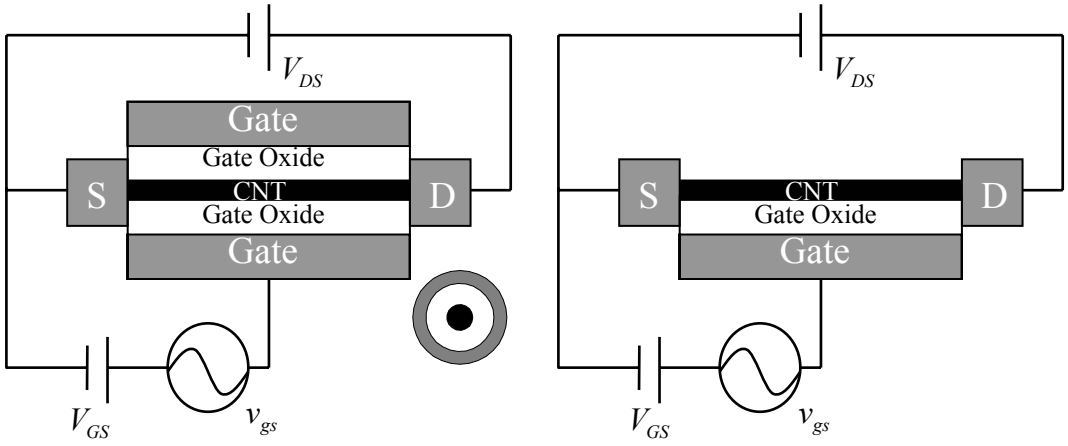


Fig. 3.2 A general description of the methodology

3.3.2 Flow of Algorithms



(a) Coaxially gated CNTFET (b) Planar gated CNTFET

Fig. 3.3 Two major carbon nanotube transistor geometries

We focus on the two major CNTFET structures as shown in Fig. 3.3, in (a) the cylindrical gate surrounds the tube and is insulated from it by the dielectric, while (b) depicts the planar gated structure, like a conventional MOSFET. The device is biased by DC voltage V_{DS} and V_{GS}. Microwave frequency ac signal $v_{gs} = V_0 \cos(2\pi ft + \theta)$ is superimposed to the gate. The coaxially gate geometry is ideal for suppressing short channel effects and for simplifying the treatment of self-consistent electrostatics [42]. But, it will bring much difficulty to the fabrications. As a result, most of the experiments on CNTFETs are based on structure (b) [63]. In this work, a coaxially gated CNTFET is modeled. The qualitative conclusions of this work also apply to planar gated CNTFETs.

The nanotube device technology, however, is still at an early stage of development. Although several CNTFETs have been reported, it is still unclear how CNTFETs operate, or

even if they all operate in the same way. One possibility is that the gate modulates the conductance of the channel as in a MOSFET [40]. Another possibility is that the gate modulates the transmission through a Schottky barrier between the source metal and the nanotube channel [64]. In this work, we study the Schottky barrier like CNTFET. Another complicated issue is the question of whether the transport is diffusive or ballistic (i.e. scattering free) from source to drain. Experiments indicate that the mean free path in semiconducting nanotubes at room temperature is at least $1\ \mu m$, so that nanotubes shorter than $1\ \mu m$ may behave as ballistic transistors [37]. In this work, we treat the quantum transport in the CNTFETs as ballistic.

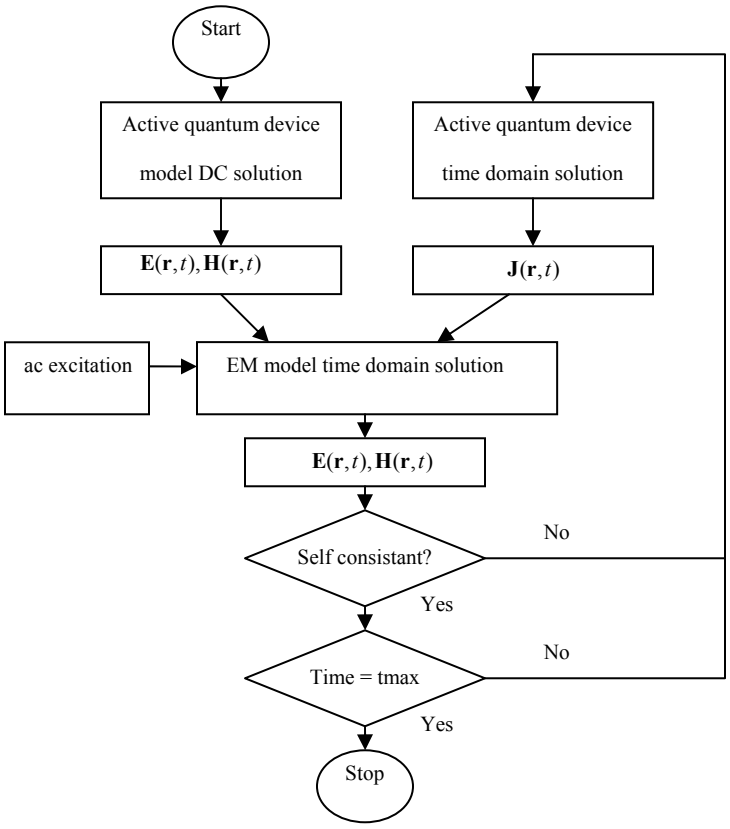


Fig. 3.4 Flowchart describing the simulation process

The flowchart in Fig. 3.4 outlines the simulation steps and the coupling between the quantum device model and electromagnetic model. Model descriptions and implementation details are discussed in later sections

3.3.3 DC Device Simulations

Firstly, we assume the device is under dc bias condition, Poisson equation (3.4) is solved self-consistently with the time-independent Schrödinger equation (3.5) under open boundary conditions, which is used to describe ballistic quantum transport [65]. Equation (3.6) relates (3.4) with (3.5) by charge density ρ_v.

$$\nabla \cdot \varepsilon \nabla \phi(\mathbf{r}) = -\rho_v \tag{3.4}$$

$$\nabla^2 \psi(\mathbf{r}) = -\frac{2m^*}{\hbar^2}(E - U(\mathbf{r}))\psi(\mathbf{r}) \tag{3.5}$$

$$\rho_v = \int [|\psi_S(\mathbf{r})|^2 + |\psi_D(\mathbf{r})|^2] dE \tag{3.6}$$

where $\phi(\mathbf{r})$ is the electrostatic potential in the device, ρ_v is charge density, m^* is the effective mass, and the potential energy $U(\mathbf{r})$ is determined by the nanotube band structure, which is shifted by electrostatic potential $\phi(\mathbf{r})$.

The source-drain dc current is determined by [65]

$$\mathbf{I}_{dc}(\mathbf{r}) = \frac{4q}{h}\int T_{dc}(E)[f(E - E_{fS}) - f(E - E_{fD})]dE \tag{3.7}$$

where $T_{dc}(E)$ is the dc transmission coefficient evaluated from Schrödinger equation with open boundary conditions, E_{fS} (E_{fD}) is the Fermi level of source (drain) determined by V_S (V_D), and f is Fermi-Dirac statistics.

At the DC biasing condition, Maxwell equations become

$$\nabla \times \mathbf{E}_{dc} = 0 \tag{3.8}$$

$$\nabla \times \mathbf{H}_{dc} = \mathbf{J}_{dc} \tag{3.9}$$

Equation (3.9) suggests that it's not necessary to find the dc distributions of the static magnetic field, since the dc current density carries the needed information about the dc magnetic field distribution.

3.3.3.1 Finite Element Method Formulations

1) Poisson equation

From equation (3.4) in the cylinder coordination, we can get

$$\frac{1}{\rho}[\frac{\partial}{\partial \rho}(\varepsilon \rho \frac{\partial V}{\partial \rho}) + \frac{\partial}{\partial z}(\varepsilon \rho \frac{\partial V}{\partial z})] = -q_v \tag{3.10}$$

Applying Galerkin method [7, 13] with the weighting function equal to 2-D linear interpolation function N_i^e, we can get

$$\iint_{\Omega_e}[\frac{\partial}{\partial \rho}(\varepsilon \rho \frac{\partial V}{\partial \rho}) + \frac{\partial}{\partial z}(\varepsilon \rho \frac{\partial V}{\partial z})]N_i^e d\rho dz = -\iint_{\Omega_e} N_i^e q_v \rho d\rho dz \tag{3.11}$$

Expanding equation (3.11) results in

$$\iint_{\Omega_e}(\varepsilon \rho \frac{\partial V}{\partial z}\frac{\partial N_i^e}{\partial z} + \varepsilon \rho \frac{\partial V}{\partial \rho}\frac{\partial N_i^e}{\partial \rho})d\rho dz = \iint_{\Omega_e} N_i^e q_v \rho d\rho dz + \int_{\Gamma_e}[(\varepsilon \rho \frac{\partial V}{\partial z} N_i^e)\hat{z} + (\varepsilon \rho \frac{\partial V}{\partial \rho} N_i^e)\hat{\rho}] \cdot \hat{n}_e d\Gamma \tag{3.12}$$

$V(\rho, z)$ can be approximated by the node value in each element as

$$V^e = \sum_{i=1}^{3} V_j^e N_j^e \tag{3.13}$$

By substituting equation (3.13) into equation (3.12), the elemental form of equation (3.12) is

$$[K_{ij}^e]\{V_j^e\} = \{g_i^e\} + \{f_i^e\} \tag{3.14}$$

where

$$K_{ij}^e = \iint_{\Omega_e} \varepsilon\rho\left(\frac{\partial N_i^e}{\partial z}\frac{\partial N_j^e}{\partial z} + \frac{\partial N_i^e}{\partial \rho}\frac{\partial N_j^e}{\partial \rho}\right) d\rho dz \tag{3.15}$$

$$g_i^e = \iint_{\Omega_e} N_i^e q_v \rho d\rho dz \tag{3.16}$$

$$f_i^e = \int_{\Gamma_e} \left[\left(\varepsilon\rho\frac{\partial V}{\partial z}N_i^e\right)\hat{z} + \left(\varepsilon\rho\frac{\partial V}{\partial \rho}N_i^e\right)\hat{\rho}\right]\cdot\hat{n}_e d\Gamma \tag{3.17}$$

The boundary conditions to be considered here are 1) If node i is on the contact, V_i^e is specified on contact (dirichlet boundary), so we can disregard f_i^e. 2) If node i is on parts of Γ lying between contacts (insulating boundary), $\nabla V \cdot \hat{n}_e = 0$, so $f_i^e = 0$.

Specifically, on the contact, V is given by

$$\begin{cases} V(R_g, z) = V_{GS} - \phi_G / q \\ V(\rho, 0) = -\phi_S / q \\ V(\rho, L_t) = V_{DS} - \phi_D / q \end{cases} \tag{3.18}$$

where $\phi_{G,S,D}$ represent the work functions of the gate, source and drain contacts, respectively, and V_{GS} and V_{DS} are the gate-source and drain-source voltages.

2) Schrödinger equation [66]

We treat the nanotube as a quasi-1D conductor. From equation (3.5) in the z coordination, we can obtain

$$\frac{d^2\psi}{dz^2} = -\frac{2m_t^*}{\hbar^2}(E-U)\Psi \tag{3.19}$$

The potential energy U seen by electrons and holes in the nanotube are

$$\begin{cases} U_e(z) = -qV(R_t, z) - \chi_{CNT} \\ U_h(z) = -U_e(z) + E_g \end{cases} \tag{3.20}$$

where E_g is the nanotube bandgap, χ_{CNT} is the electron affinity and $V(R_t, z)$ is the electrostatic potential on the surface of the nanotube calculated from Poisson equation (3.10).

Applying Galerkin method with the weighting function equal to 1-D linear interpolation function N_i^e, we can get

$$\int_{z_1^e}^{z_2^e}[-\frac{dN_i^e}{dz}\frac{d\psi}{dz} + \frac{2m_t^*}{\hbar^2}(E-U)N_i^e\psi]dz + N_i^e\frac{d\psi}{dz}\Big|_{z_1^e}^{z_2^e} = 0 \tag{3.21}$$

$\psi(z)$ can be approximated by the node value in each element as

$$\psi^e = \sum_{i=1}^{3}\psi_j^e N_j^e \tag{3.22}$$

By substituting equation (37) into equation (36), the elemental form of equation (36) is

$$[R_{ij}^e]\{\psi_j^e\} = \{b_i^e\} \tag{3.23}$$

where

$$R_{ij}^e = \int_{z_1^e}^{z_2^e} -\frac{dN_i^e}{dz}\frac{dN_j^e}{dz} + \frac{2m_t^*}{\hbar^2}(E-U)N_i^e N_j^e]dz \tag{3.24}$$

$$b_i^e = -N_i^e\frac{d\psi}{dz}\Big|_{z_1^e}^{z_2^e} \tag{3.25}$$

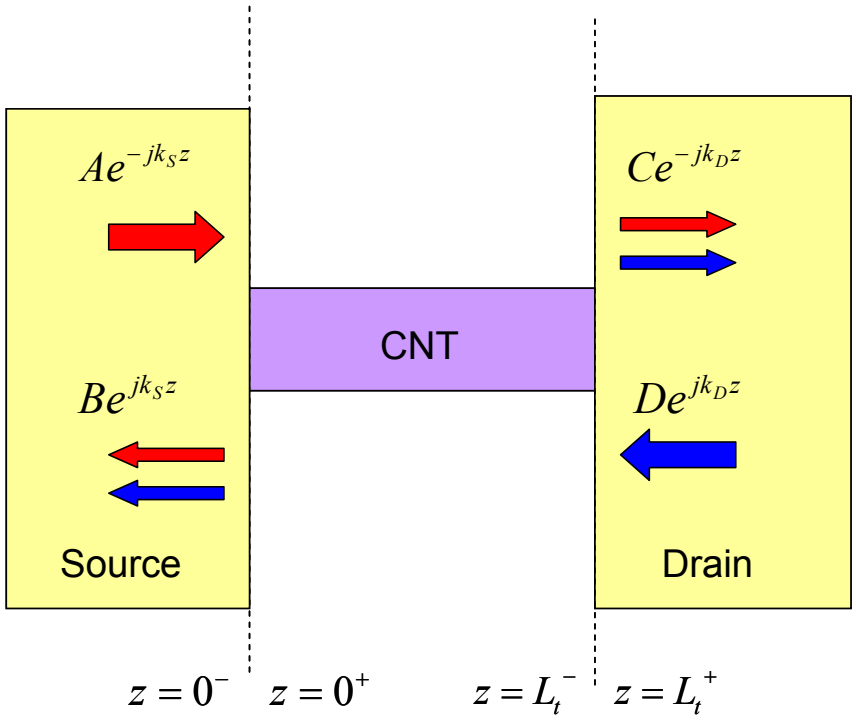


Fig. 3.5 Absorption boundary conditions treatment

We use the absorption boundary conditions as shown in Fig. 3.5. The following steps are adopted to derive the boundary conditions at $Z = 0$ and $Z = L_t$.

In the two contacts, the wave function at a given energy is of the form

$$\psi = \begin{cases} Ae^{-jk_S z} + Be^{jk_S z} & z < 0 \\ Ce^{-jk_D z} + De^{jk_D z} & z > L_t \end{cases} \tag{3.26}$$

where k_S and k_D are the wave vectors in the source an drain contacts, respectively, and A, B, C, and D are constants.

If we assume that only the source injections happen, then $D = 0$ for all energies as equation (3.27)

$$\Psi_S = \begin{cases} Ae^{-jk_S z} + Be^{jk_S z} & z < 0 \\ Ce^{-jk_D z} & z > L_t \end{cases} \tag{3.27}$$

By evaluating equation (3.26) at the two boundaries $z = 0^-$ and $z = L_t^+$, the equation (3.28) is derived

$$\begin{cases} [\dfrac{d\psi_S}{dz} - jk_S\psi_S]_{z=0^-} = -2jAk_S \\ [\dfrac{d\psi_S}{dz} + jk_D\psi_S]_{z=L_t^+} = 0 \end{cases} \tag{3.28}$$

Applying the equation (3.29) as the boundary conditions at $z = 0$ and $z = L_t$,

$$\begin{cases} \psi_S(z=0^-) = \psi_S(z=0^+) \\ \dfrac{1}{m_S^*}\dfrac{d\psi_S}{dz}\Big|_{z=0^-} = \dfrac{1}{m_t^*}\dfrac{d\psi_S}{dz}\Big|_{z=0^+} \end{cases} \quad \begin{cases} \psi_S(z=L_t^-) = \psi_S(z=L_t^+) \\ \dfrac{1}{m_t^*}\dfrac{d\psi_S}{dz}\Big|_{z=L_t^-} = \dfrac{1}{m_D^*}\dfrac{d\psi_S}{dz}\Big|_{z=L_t^+} \end{cases} \tag{3.29}$$

the absorption boundary conditions for the wave function ψ_S at $z = 0^+$ and $z = L_t^-$ are

$$\begin{cases} \dfrac{d\psi_S}{dz}\Big|_{z=0^+} = \dfrac{m_t^*}{m_S^*}[jk_S\psi_S(z=0^+) - 2jAk_S] \\ -\dfrac{d\psi_S}{dz}\Big|_{z=L_t^-} = \dfrac{m_t^*}{m_D^*}jk_D\psi_S(z=L_t^-) \end{cases} \tag{3.30}$$

In addition, Landauer will hold for flux and must equal to the probability current. For the transmitted wave this yields

$$\frac{2q}{\pi\hbar} f_S T = \frac{q\hbar}{m_S^*} k_D |C|^2 \tag{3.31}$$

The current transmission probability is specified by equation (3.32), which yields the normalization condition as equation (3.33).

$$T_S = \frac{m_S^* k_D |C|^2}{m_D^* k_S |A|^2} \tag{3.32}$$

$$|A|^2 = \frac{2m_D^* f_S}{\pi\hbar^2 k_S} \tag{3.33}$$

Similarly, the absorption boundary conditions for drain injections are as

$$\begin{cases} \left.\dfrac{d\psi_D}{dz}\right|_{z=0^+} = \dfrac{m_t^*}{m_S^*} jk_S \psi_D(z=0^+) \\ -\left.\dfrac{d\psi_D}{dz}\right|_{z=L_t^-} = \dfrac{m_t^*}{m_D^*}[jk_D \psi_D(z=L_t^-) - 2jk_D D e^{jk_D L_t^-}] \end{cases} \tag{3.34}$$

The current transmission probability is specified by equation (3.35) and the normalization condition is given by equation (3.36).

$$T_D = \frac{m_D^* k_S |B|^2}{m_S^* k_D |D|^2} \tag{3.35}$$

$$|D|^2 = \frac{2m_S^* f_D}{\pi\hbar^2 k_D} \tag{3.36}$$

Including source and drain injections, the normalized wavefunction yield the total carrier densities in the system,

$$\begin{cases} n(z) = \int_{E_e}^{\infty} |\Psi_{e,S}|^2 + |\Psi_{e,D}|^2 \, dE \\ p(z) = \int_{E_h}^{\infty} |\Psi_{h,S}|^2 + |\Psi_{h,D}|^2 \, dE \end{cases} \tag{3.37}$$

where $E_{e,h}$ is taken to be the bottom of the band, for either electrons or holes, in the appropriate metallic contacts.

3.3.4 AC Device Simulations

The time-dependent wave-like nature of electrons is described by wave packet $\psi(\mathbf{r},t)$ in time-dependent Schrödinger equation [13]

$$i\hbar\frac{\partial\psi(\mathbf{r},t)}{\partial t}=\frac{1}{2m^*}(\frac{\hbar}{i}\nabla-\frac{q}{c}\mathbf{A}(\mathbf{r},t))^2\psi(\mathbf{r},t)+U(\mathbf{r},t)\psi(\mathbf{r},t) \tag{3.38}$$

If we introduce ac signal v_{gs} on the gate, the ac excitation is applied. The time-domain distributions of the electromagnetic fields are obtained using Maxwell's equations as

$$\begin{cases}\mathbf{H}(\mathbf{r},t)=\dfrac{1}{\mu}\nabla\times\mathbf{A}(\mathbf{r},t)\\ \mathbf{E}(\mathbf{r},t)=-\nabla V(\mathbf{r},t)\\ \dfrac{\partial\mathbf{E}}{\partial t}=\dfrac{1}{\varepsilon}(\nabla\times\mathbf{H}-\mathbf{J}_{total})\\ \dfrac{\partial\mathbf{H}}{\partial t}=-\dfrac{1}{\mu}\nabla\times\mathbf{E}\end{cases} \tag{3.39}$$

When the frequency is much smaller than the speed of the wave propagation ($\sqrt{5}$ times Fermi velocity) divided by the channel length (which is ~100 THz for the simulated device with a channel length of 20 nm) electrostatic simulation can be used instead of full-wave electromagnetics simulation. Because the frequency range of interest is much smaller than ~100 THz, the time-dependent quantum transport equation is solved self-consistently with the Poisson equation. Under the electrostatic assumption, the time-dependent Schrödinger equation is simplified as

$$i\hbar\frac{\partial\psi(\mathbf{r},t)}{\partial t}=-\frac{1}{2m^*}\hbar^2\nabla^2\psi(\mathbf{r},t)+U(\mathbf{r},t)\psi(\mathbf{r},t) \tag{3.40}$$

3.3.4.1 Finite Difference Time Domain Formulations

The importance of this task lies in the following aspects. First, solving the time-dependent Schrödinger equation is a computationally heavy process. Therefore, the investigations of the efficient formalisms are needed with respect to the device structures. Second, self-consistent coupling between quantum device model and EM model needs careful design of the algorithms to assure the convergence of the total program.

In order to treat time-dependent transport in the channel and quantum tunneling through the metal/CNT Schottky barriers, we solve the time-dependent Schrodinger equation by extending the finite difference time domain quantum (FDTD-Q) method as described in Ref. [67] with the treatment of the open boundary condition.

3.3.4.2 Extended FDTD-Q Method

First, the complex wave function $\psi(z,t)$ is separated into two real functions that correspond to its real and imaginary parts.

$$\psi(z,t) = \psi_R(z,t) + j\psi_I(z,t) \tag{3.41}$$

(3.41) is divided into two equations involving real functions corresponding to ψ_R and ψ_I

$$\hbar \frac{\partial \psi_R(z,t)}{\partial t} = -\frac{\hbar^2}{2m^*} \frac{\partial^2 \psi_I(z,t)}{\partial z^2} + U(z,t)\psi_I(z,t) \tag{3.42}$$

$$\hbar \frac{\partial \psi_I(z,t)}{\partial t} = \frac{\hbar^2}{2m^*} \frac{\partial^2 \psi_R(z,t)}{\partial z^2} - U(z,t)\psi_R(z,t) \tag{3.43}$$

A mesh is defined in an absorption boundary value problem as shown in Fig. 3.6, where the continuous complex wave function is represented in the computational domain as two discrete functions. The simulation domain includes two contacts regions and CNT region. The electron waves excited in the source contact transport along the CNT channel. Because of the time and space variation of the potential profile, only part of the waves can transmit through the CNT channel and reach the drain contact. The transmitted electron waves finally are absorbed by the drain contact on the edge. The reflected electron waves are collected by the source edge.

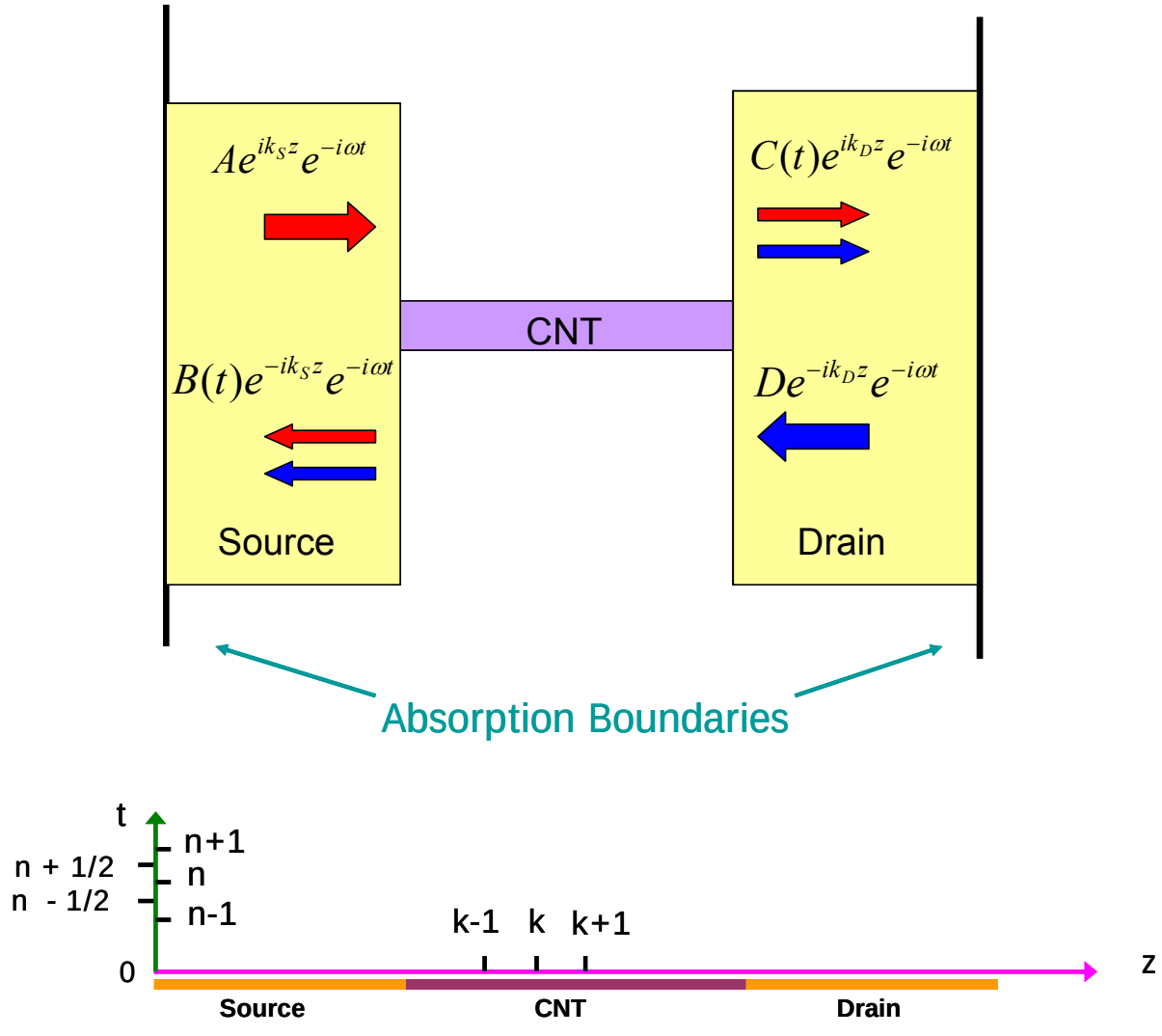


Fig. 3.6 Computation domain discretization

Applying (3.42) at $t = (n + \frac{1}{2})\Delta t$ and $z = k\Delta z$

$$\hbar \frac{\partial \psi_R(z,t)}{\partial t}\bigg|_k^{n+\frac{1}{2}} = -\frac{\hbar^2}{2m^*} \frac{\partial^2 \psi_I(z,t)}{\partial z^2}\bigg|_k^{n+\frac{1}{2}} + U(z,t)\big|_k^{n+\frac{1}{2}} \psi_I(z,t)\big|_k^{n+\frac{1}{2}} \tag{3.44}$$

The derivatives are discretized using the central difference as

$$\frac{\partial \psi_R(z,t)}{\partial t}\bigg|_k^{n+\frac{1}{2}} = \frac{\psi_R^{n+1}(k) - \psi_R^n(k)}{\Delta t} \tag{3.45}$$

$$\begin{aligned} \frac{\partial^2 \psi_I(z,t)}{\partial z^2}\bigg|_k^{n+\frac{1}{2}} &= \frac{1}{\Delta z}\left[\frac{\partial \psi_I^{n+\frac{1}{2}}(k+\frac{1}{2})}{\partial z} - \frac{\partial \psi_I^{n+\frac{1}{2}}(k-\frac{1}{2})}{\partial z}\right] \\ &= \frac{1}{\Delta z}\left[\frac{\psi_I^{n+\frac{1}{2}}(k+1) - \psi_I^{n+\frac{1}{2}}(k)}{\Delta z} - \frac{\psi_I^{n+\frac{1}{2}}(k) - \psi_I^{n+\frac{1}{2}}(k-1)}{\Delta z}\right] \\ &= \frac{\psi_I^{n+\frac{1}{2}}(k+1) - 2\psi_I^{n+\frac{1}{2}}(k) + \psi_I^{n+\frac{1}{2}}(k-1)}{\Delta z^2} \end{aligned} \tag{3.46}$$

Plug (3.45) and (3.46) into (3.44), we can get

$$\psi_R^{n+1}(k) = \psi_R^n(k) + \left[\frac{U(k,n+\frac{1}{2})\Delta t}{\hbar} + \frac{\hbar \Delta t}{m^* \Delta z^2}\right]\psi_I^{n+\frac{1}{2}}(k) - \frac{\hbar \Delta t}{2m^* \Delta z^2}\left[\psi_I^{n+\frac{1}{2}}(k+1) + \psi_I^{n+\frac{1}{2}}(k-1)\right] \tag{3.47}$$

Similarly, applying (3.43) at $t = n\Delta t$ and $z = k\Delta z$, we have

$$\psi_I^{n+\frac{1}{2}}(k) = \psi_I^{n-\frac{1}{2}}(k) - \left[\frac{U(k,n)\Delta t}{\hbar} + \frac{\hbar \Delta t}{m^* \Delta z^2}\right]\psi_R^n(k) + \frac{\hbar \Delta t}{2m^* \Delta z^2}\left[\psi_R^n(k+1) + \psi_R^n(k-1)\right] \tag{3.48}$$

3.3.4.3 Absorbing Boundary Condition

Artificial absorbing boundaries are added at the two end points $k = 0$ and $k = n$ of the simulation domain to absorb the transmitted waves at the drain contact and the reflected waves at the source contact due to the source contact excitations.

1-D case, First-order, absorption boundary conditions is applied at two end points as equation (3.49) and (3.50) [68].

$$\psi^{n+1}(k=0) = \psi^{n}(k=1) + \frac{p-1}{p+1}\left[\psi^{n+1}(k=1) - \psi^{n}(k=0)\right] \tag{3.49}$$

$$\psi^{n+1}(k=n) = \psi^{n}(k=n-1) + \frac{p-1}{p+1}\left[\psi^{n+1}(k=n-1) - \psi^{n}(k=n)\right] \tag{3.50}$$

where $p = \frac{c\Delta t}{\Delta z}$ and c is the phase velocity of the wave calculated by (3.51)

$$c = \frac{E}{\hbar k_{s(D)}} \tag{3.51}$$

Here, $k_{s(D)}$ is the wave number in the source contact or drain contact.

3.3.4.4 Source Wave Excitation

Assume at $z = m\Delta z$ in the source contact, an incident wave $\psi_{inc} = e^{-i\frac{E}{\hbar}t + ik_z z}$ with

$\psi_R = \cos(-\frac{E}{\hbar}t + k_z z)$ and $\psi_I = \sin(-\frac{E}{\hbar}t + k_z z)$ is excited.

The total wave is usually represented as the sum of the incident and the scattered wave.

Within $0 \le k < m$ region, only the scattered wave is propagating. Within $k \ge m$ region, the wave is the sum of the incident and scattered wave. As a result, during the interaction of each time step, the calculated electron wave functions should be modified at $z = m\Delta z$ and $z = (m-1)\Delta z$ as

$$\begin{cases} \psi_R^{n+1(total)}(m) = Calculated - \dfrac{\hbar \Delta t}{2m^* \Delta z^2} \psi_{Iinc}^{n+\frac{1}{2}}(m-1) \\ \psi_R^{n+1(scatt)}(m-1) = Calculated + \dfrac{\hbar \Delta t}{2m^* \Delta z^2} \psi_{Iinc}^{n+\frac{1}{2}}(m) \\ \psi_I^{n+\frac{1}{2}(total)}(m) = Calculated + \dfrac{\hbar \Delta t}{2m^* \Delta z^2} \psi_{Rinc}^{n}(m-1) \\ \psi_I^{n+\frac{1}{2}(scatt)}(m) = Calculated - \dfrac{\hbar \Delta t}{2m^* \Delta z^2} \psi_{Rinc}^{n}(m) \end{cases} \tag{3.52}$$

3.3.4.5 Stability of the Algorithm

In order to ensure the stability of the algorithm, a maximum value for the time step is given by [67]

$$\Delta t \le \frac{\hbar}{\dfrac{\hbar^2}{m^* \Delta z^2} + U} \tag{3.53}$$

Since U is a function of time and space, in practical implementation, Δt is determined by maximum U value in time and space domain.

3.3.4.6 Current and Charge Density Formulas

The time-dependent drain to source current and charge density are calculated by the probability current density and probability density [69] from the solved time-dependent wave function $\psi(z,t)$. The time-dependent wave function in contact due to the unitary wave injection

is

$$\psi_{contact}(z,t) = \frac{1}{\sqrt{L}} e^{ikz - i\omega t} \tag{3.54}$$

where L is the length of the contact.

The normalized probability current density contributed by wave number k is

$$J_k(z,t) = \frac{1}{L} \cdot \frac{e\hbar}{2m^* i} (\psi(z,t)^* \frac{\partial \psi(z,t)}{\partial z} - \psi(z,t) \frac{\partial \psi(z,t)^*}{\partial z}) \tag{3.55}$$

The drain to source current is obtained by summation over k in the contact

$$i_{DS}(z,t) = (\sum_{k>0} J_k(z,t)) \times 4 \tag{3.56a}$$

(where 4 accounts for, spin degeneracy x 2 and CNT valley degeneracy x2)

$$i_{DS}(z,t) = \frac{1}{L} \cdot \frac{L}{2\pi} \cdot 4 \int_0^{+\infty} \frac{e\hbar}{2m^* i} (\psi(z,t)^* \frac{\partial \psi(z,t)}{\partial z} - \psi(z,t) \frac{\partial \psi(z,t)^*}{\partial z}) dk \tag{3.56b}$$

$$i_{DS}(z,t) = \frac{2e\hbar}{m^* \pi} \int_{E_c}^{+\infty} \frac{1}{(\frac{dE}{dk})} I_m(\psi(z,t)^* \frac{\partial \psi(z,t)}{\partial z}) dE \tag{3.56c}$$

If we use the parabolic E-k relation, $E = \frac{\hbar^2 k^2}{2m^*} + E_c$, in the contacts, equation (3.57) is derived.

$$i_{DS}(z,t) = \sqrt{\frac{2}{m^*}} \frac{e}{\pi} \int_{E_c}^{+\infty} \frac{1}{\sqrt{E - E_c}} \mathrm{Im}(\psi(z,t)^* \frac{\partial \psi(z,t)}{\partial z}) dE \tag{3.57}$$

Similarly, the time-dependent charge density is produced from $\rho_k(z,t) = \frac{e}{L} |\psi(z,t)|^2$ and $\rho_v(z,t) = (\sum_{k>0} \rho_k) \times 4$ as

$$\rho_v(z,t) = \frac{\sqrt{2m^*}e}{\pi\hbar}\int_{E_c}^{+\infty}\frac{1}{\sqrt{E-E_c}}\left|\psi(z,t)\right|^2 dE \tag{3.58}$$

3.3.4.7 Simulation Steps

The following steps are introduced to solve quantum device equations (3.42) and (3.43) self consistently with Poisson equation (3.10).

Step 1 Impose initial boundary conditions on ψ_R and ψ_I at $t = 0$;

Step 2 Add excitation of ψ_I at time $t + \Delta t/2$;

Step 3 Calculation of ψ_I at time $t + \Delta t/2$;

Step 4 Absorption boundary conditions on ψ_I;

Step 5 Add excitation of ψ_R at time $t + \Delta t$;

Step 6 Calculation of ψ_R at time $t + \Delta t$;

Step 7 Absorption boundary conditions on ψ_R;

Step 8 Calculation the ρ_v with wave functions on ψ_R and ψ_I;

Step 9 Updating the potential profile U by solving Poisson equation;

Step 10 If U is converged, go to Step 11, else go to Step 2

Step 11 Time is increased to $t + \Delta t$;

Step 12 If $t >$ total pre-set simulation time, then stop the loops, else go to the Step 2, and continue the iterations.

3.4 DC Simulation Results

We now present results for an intrinsic (17, 0) zigzag CNT channel has a channel length of $L_{ch} = 20\,\text{nm}$, and a diameter of $d_{CNT} \approx 1.33$ nm, which results in a band gap of $E_g \approx 0.65\,\text{eV}$. The Schottky barrier height, Φ_B, between the metal source and drain contacts and the intrinsic CNT channel depends on the contact material and tube diameter. In this work, we use $\Phi_B = 0.33\,\text{eV}$. The high-κ gate insulator thickness is *tins*=2.5nm and the dielectric constant $\kappa \approx$ 25. The relative effective mass of the CNT is 0.06 [70]. All work function are taken to be $4.5\,eV$, and $\chi_{CNT} = 4.2eV$. $E_{e,h}$ is taken be $1.0\,eV$ below the metal Fermi level. Effective masses in the two contacts are assumed the same as the nanotube.

Fig. 3.7 shows the energy diagram when V_{GS} = 0.25V and V_{DS} = 0.5V where assume source Fermi level is zero. The schottky barrier height for electron is 0.33V, and the Fermi level is at the middle of the bandgap. For this kind of configurations, the transistor is ambiploar, showing symmetric electron and hole conduction (see Fig. 3.8). The minimum current occurs when the gate voltage is one-half the drain voltage, and the conduction and valance band are symmetric (see Fig. 3.7).

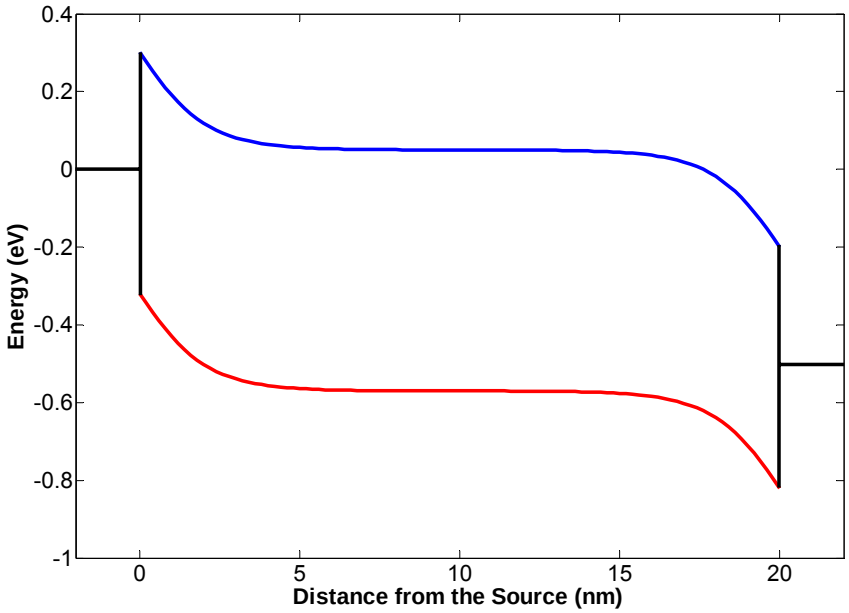


Fig. 3.7 Energy band diagram when V_{GS} = 0.25V and V_{DS} = 0.5V, the energy is respect to the source Fermi level

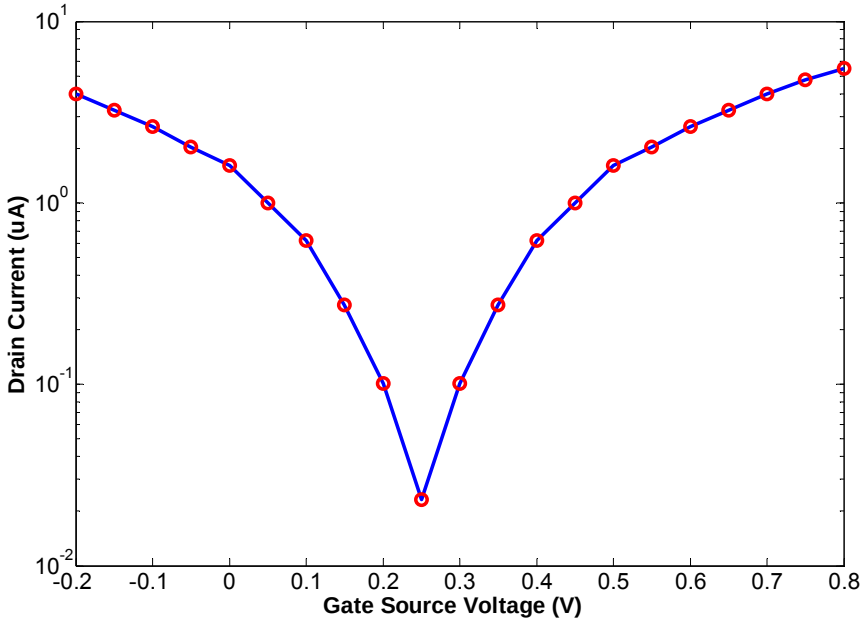


Fig. 3.8 Drain current versus Gate-Source Voltage when V_{DS} =0.5 V

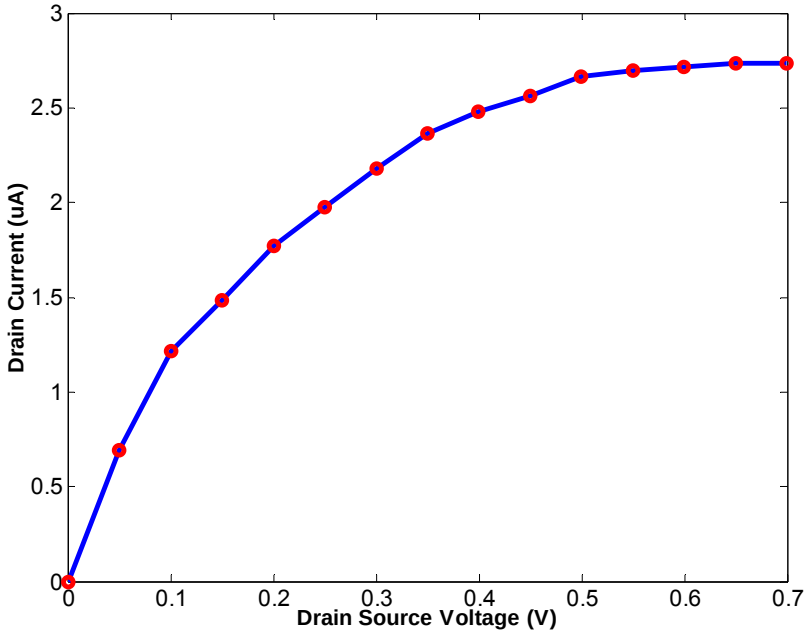
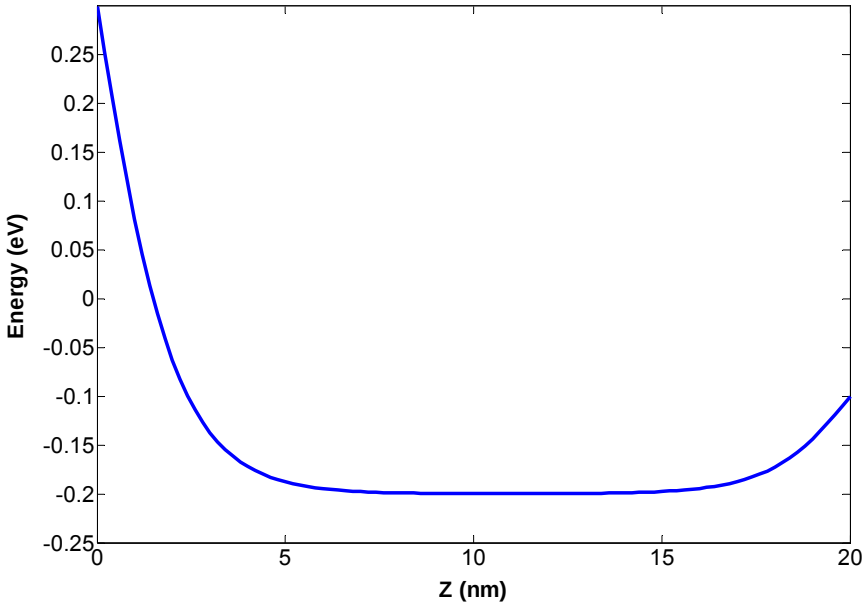
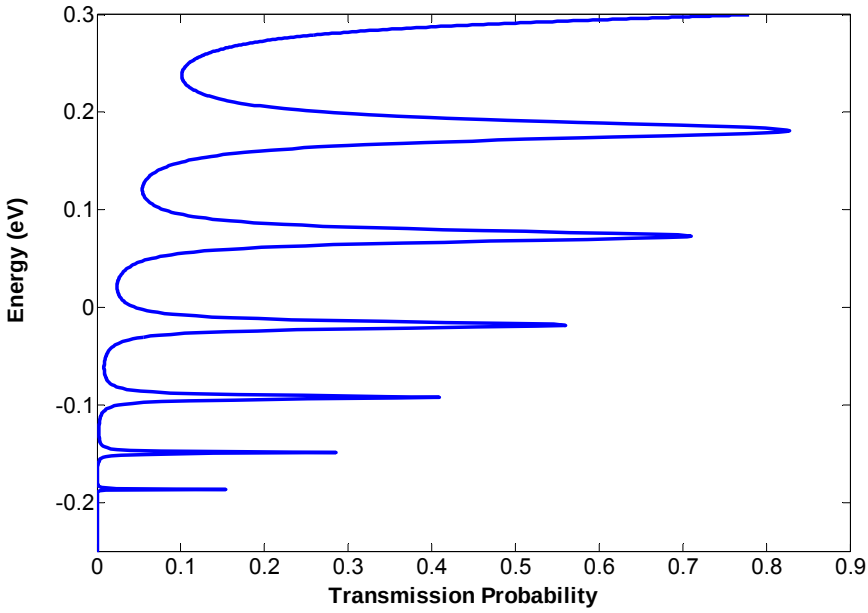


Fig 3.9 Drain current versus drain-source voltage at $V_{GS} = 0.5V$

The drain current versus drain-source voltage is shown in Fig. 3.9 at $V_{GS} = 0.5V$. The saturation current for this case is around $2.7\,\mu A$. We also note that it is important to treat carrier wave transport full quantum mechanically. Figs. 3.10 and 3.11 illustrate this concept. Classical mechanic says that the carriers above the barrier height are assumed to have a transmission probability near unity and below the barrier are assumed to have a transmission probability near zero. However, from Fig. 3.10, we can find there is sill transmission when the carrier is below the barrier height. For the negative barrier device as shown in Fig. 3.11, the transmission probability is not unity for the carriers are above the barriers. In addition, those transmission peaks, which are caused by the phase coherency, are highly influenced by Schottky-barrier contacts.

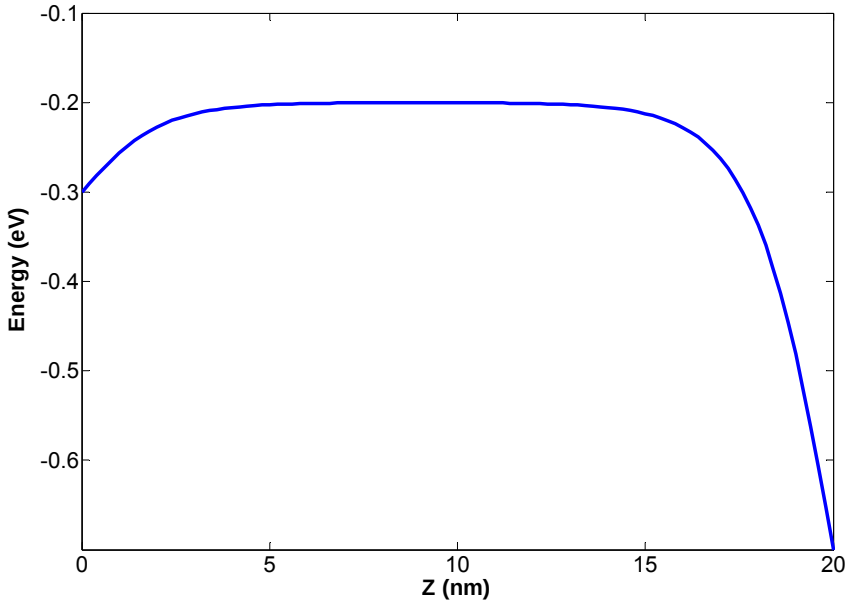


(a)

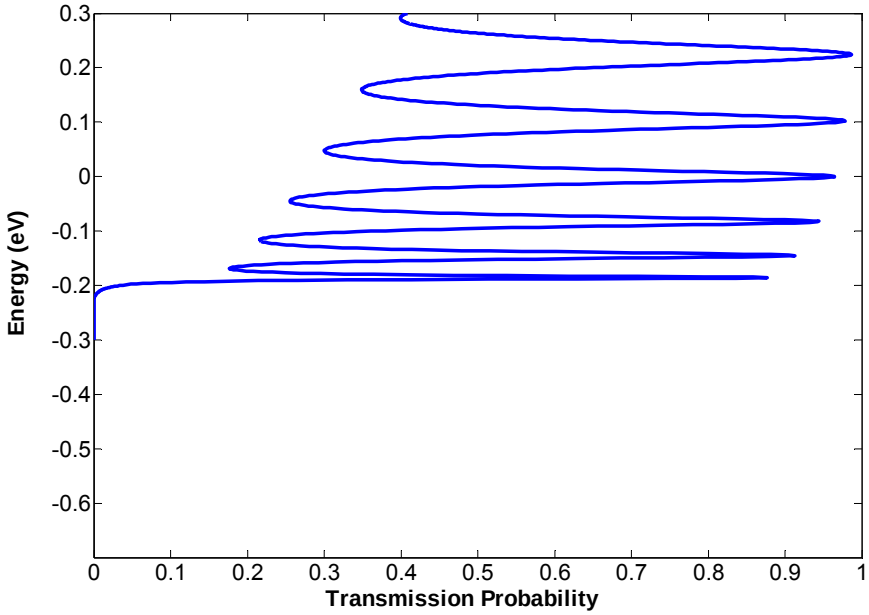


(b)

Fig. 3.10 (a) Conduction band edges and (b) transmission probability when V_{GS} = 0.5V and V_{DS} = 0.4V (positive barriers)



(a)



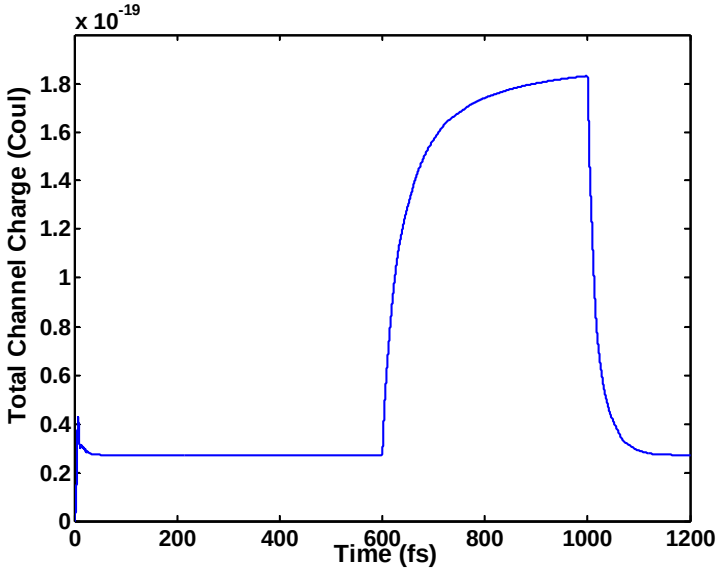
(b)

Fig. 3.11 (a) Conduction band edges and (b) transmission probability when V_{GS} = 0.5V and V_{DS} = 0.4V (negative barriers with $\phi_{S,D} = 3.9eV$).

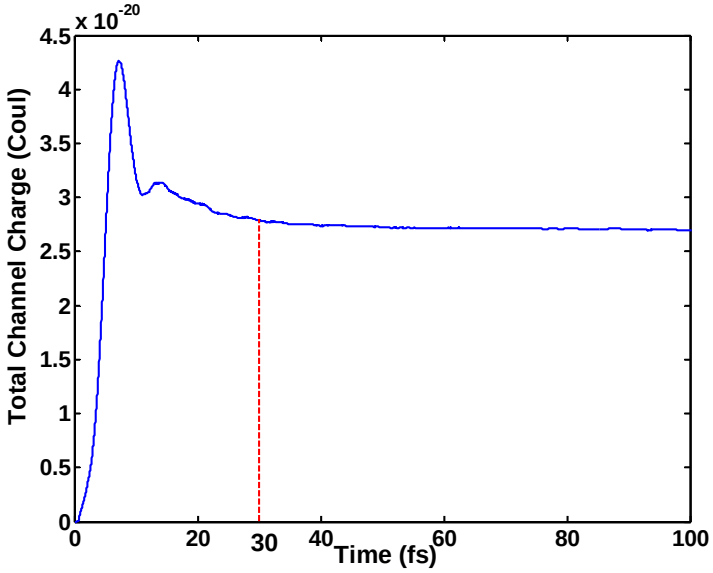
3.5 AC Simulation Results

AC simulation is performed by assuming an AC signal with amplitude of 10 mV is applied at the gate to modulate the transport of the carriers. Because the conduction and valence bands of CNTs are symmetric, n-type conduction is modeled for simplicity. The simulations are performed at the room temperature, $T = 300$ K. A power supply voltage of V_{DS}=0.5V.

Ballistic transport in the CNT channel is assumed. An effective mass description of the CNT band structure is used [66]. The parasitic capacitances between the gate electrode and source (drain) contact, which significantly decrease the operation frequency of the devices in the current experiments, are neglected. The simulation results based on the above assumptions set the high-frequency performance limit of CNTFETs (The effects of parasitic capacitances and scattering are briefly discussed later).



(a)



(b)

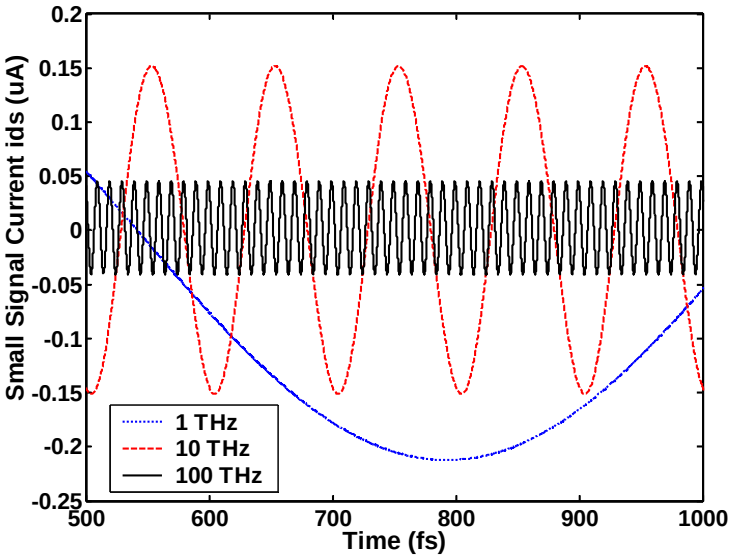
Fig. 3.12 (a) Switching transient characteristics of the channel charge with the applied rectangular pulse (V_{GS} from 0 V to 0.5 V to 0 V, between 600 fs and 1000 fs) to the gate. (b) Power-on transient characteristics of the channel charge. The transistor is turned on (V_{DS} from 0 V to 0.5 V) at t=0. The settling time is 30 fs.

In quasi-static approximation, it is assumed that the charge in a transistor channel responds instantaneously as the terminal voltage is applied. We first explore the finite time that takes to charge and discharge the CNT channel using the time-dependent simulation. Fig. 1 plots the simulated total amount of charge in the channel as a function of time when a rectangular pulse signal is applied on the gate, where Fig. 1(a) plots the time period with the gate voltage pulse and Fig. 1(b) plots the power-on (drain voltage step) time period. At $t = 0$, the device is powered on with $V_{DS} = 0.5$ V and $V_{GS} = 0$ V. The channel charge goes to steady state after an overshoot time period, which is caused by zero rising time of the drain voltage step. The approximate rising time (for the charge to increase to the steady state value) is about 30 fs. The finite charging time is due to the facts that the charge in the channel is supplied by carrier injection from the source and that the source-injected carriers travel at a speed below the band-structure-limited speed. In order to characterize how fast carriers travel to charge the channel, an effective velocity, which is defined as the channel length divided by the rising time, is computed to be $\sim 6.67 \times 10^5$m/s. It is in the same order of magnitude but still smaller than the Fermi velocity in metallic CNTs (about 9.6×10^5 m/s) because of the following two reasons. First, tunneling through the Schottky barrier at the source end of the channel slows down the carriers. Second, carriers populate the bottom portion of a semiconducting *E-k* relation, which has a smaller band-structure-limited velocity.

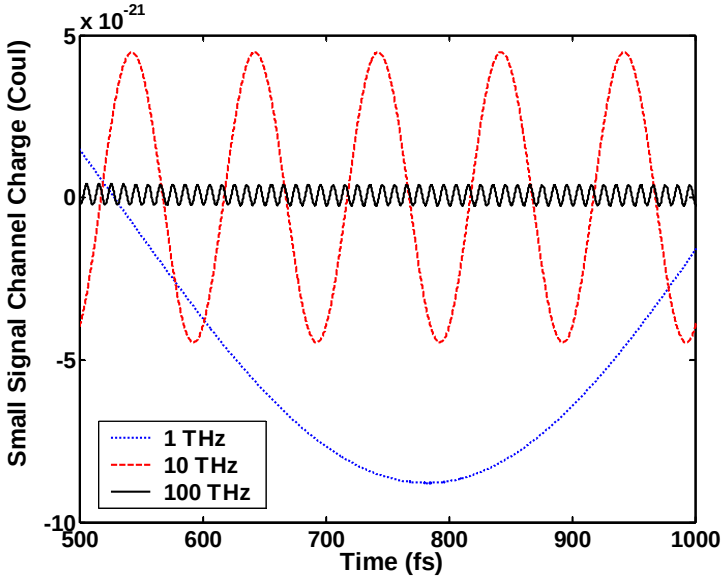
We next explore the NQS effect in the small signal configurations. A small signal sinusoidal wave with amplitude of 10 mV is superimposed with DC biasing on the gate. Fig. 3.13 (a) shows the resulting time-dependent small signal drain to source current for different frequencies (1 THz, 10 THz and 100 THz). With the increasing of the frequency, the small signal amplitude of the AC current is gradually decreased. This is because the transit time is

comparable to the period of the small signal at high frequency. At very high frequency, the small signal voltage on the gate cannot modulate the transport current, which means that the gate will lose the control of the device at such high frequency. Similar behavior can be expected for time dependent channel charge as shown in Fig. 3.13 (b). At very high frequency, the potential in the channel will change before the channel charge accumulates to the new level. So, the channel charge is almost constant, which is close to DC charge.

Based on the results of Fig. 3.13, we can obtain the frequency dependent small signal transconductance and gate capacitance as shown in Fig. 3.14. Comparing these NQS values with QS simulation results [51, 52], we find that up to the frequency of ~1 THz, the results of NQS approach are close to that of QS approach. However, when the frequency is above 1 THz, the NQS results show that the small signal transconductance and gate capacitance decrease accordingly, while the QS approach cannot show frequency dependent results. As indicated in Fig. 3.14(a), 3 dB bandwidth of the transconductance is around 10 THz, which is a very important specification for the amplifier applications.

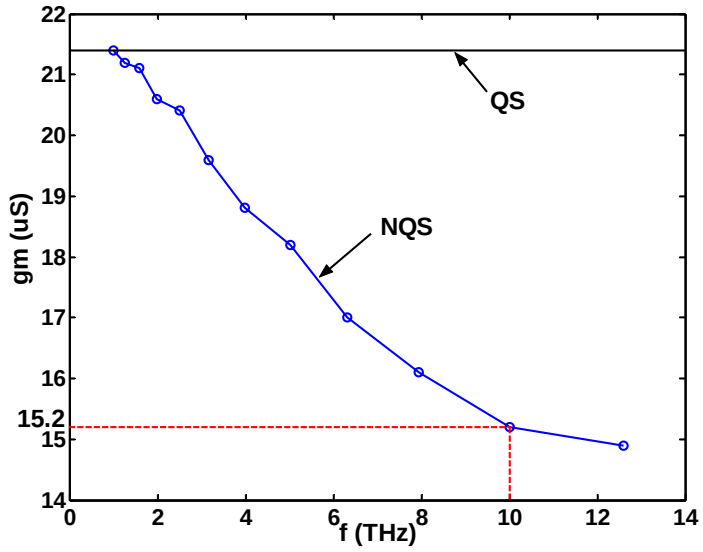


(a)

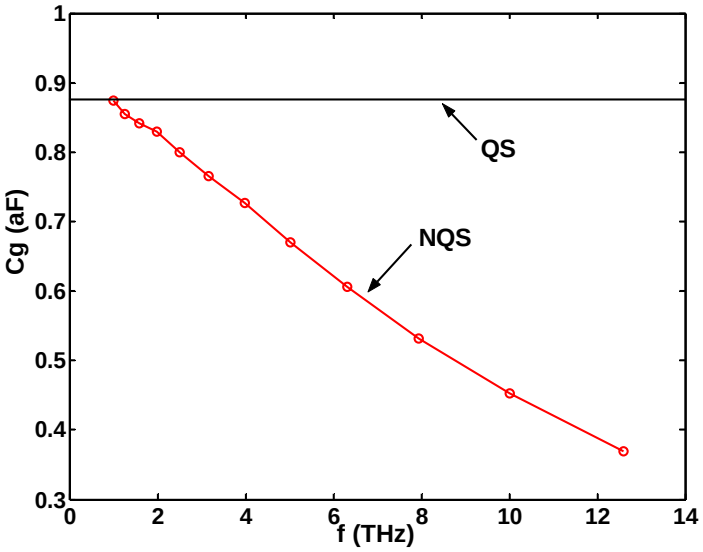


(b)

Fig. 3.13 (a) Small signal time dependent drain to source current (b) Small signal time dependent channel charge at V_{DS} = 0.5 V , V_{GS} = 0.5 V and vgs = 10 mV.



(a)



(b)

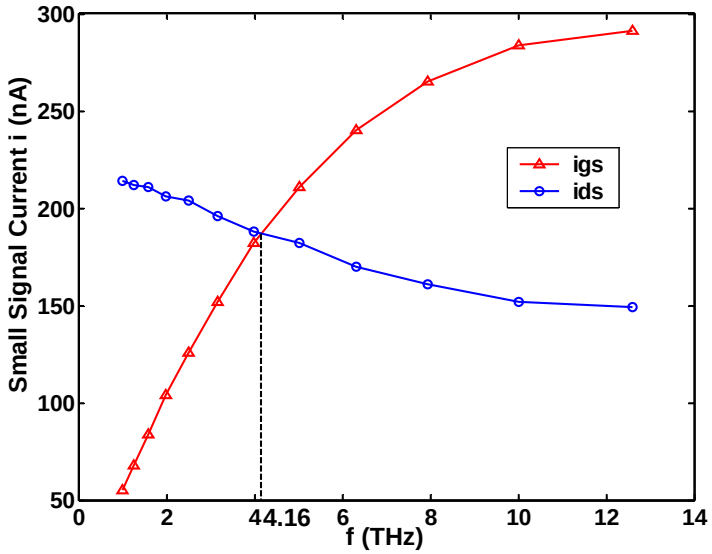
Fig. 3.14 (a) AC transconductance and (b) gate capacitance vs. frequency at V_{DS} = 0.5 V and V_{GS} = 0.5 V.

An important performance metric for high frequency analog application is the cut-off frequency. Next we examine the validity of QS approximation for computing the cut-off frequency. Fig. 3.15(a) shows how the cut-off frequency is computed in a time-dependent simulation. It plots the gate current and the source-drain current as a function of the frequency of the applied gate voltage. As frequency increases, the impedance of the gate capacitor decreases, and the gate current increases. On the other hand, when the frequency increases, the source-drain current decreases because the transconductance decreases as a function of the frequency as shown in Fig. 3.14. The cut-off frequency, which is defined as the unit current gain frequency, is 4.16 THz as shown in Fig. 3.15 (a). (This value is well below 100 THz, which justified the approximation that Poisson equation applies). Using the QS approach [51, 52], the intrinsic cutoff frequency can be computed as $g_m/(2\pi C_g)$, where g_m and C_g are the DC transconductance and gate capacitance, respectively. The intrinsic cutoff frequency f_T computed by the QS approximation is 3.86 THz, which is different from that computed by time-dependent simulation by about 7%. We notice that although the QS approximation overestimates the transconductance at f_T by 14% and the intrinsic gate capacitance by 21%, it results in an intrinsic cut-off frequency much closer to that computed by the time-dependent simulation due to the following reason. As frequency increases, the simultaneous decrease of the transconductance and the gate capacitance makes their ratio (which determines f_T) less affected. The QS estimation of the cut-off frequency is expected to be even more accurate when a state-of-the-art experimental CNTFET is considered, which operates well below its high-frequency performance limit because the parasitic capacitances between the gate electrode and source (drain) electrode dominate [3.24]. Because the parasitic capacitances are nearly bias-independent, the frequency dependent gate capacitance will have little effect on the total capacitance. Since the extrinsic cut-off frequency is

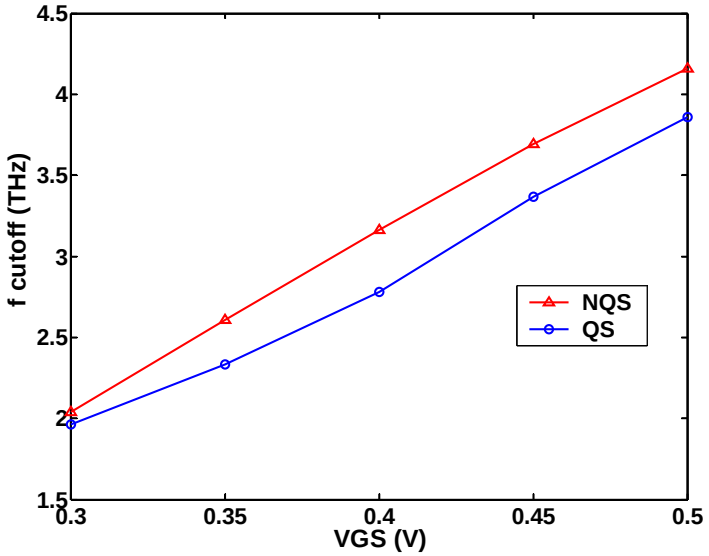
orders of magnitude smaller than the intrinsic cut-off frequency, the transconductance and the gate capacitance are close to the QS estimations at such a low frequency. In this case, the QS approach gives a good estimation of the extrinsic cutoff frequency.

The above comparison is performed at a specific bias condition. Next, we explore the voltage dependence. Fig. 3.15(b) plots f_T computed by QS approximation and that computed from the time-dependent simulation as a function of the applied DC gate voltage. The qualitative feature of the curve by QS simulation [51, 52] is similar to that of time-dependent simulation. The intrinsic cutoff frequency of the CNTFET increases with gate biasing when the gate voltage is relatively small and tends to remain constant as V_G further increases but still smaller than V_D. Over the whole simulated bias regime, the difference between the quasi-static approximation and the time-dependent simulation is less than 7%, which indicates the validity of quasi-static approximation for computing the cut-off frequency over a wide range of bias conditions.

Ballistic transport is assumed in this study. At low V_D, acoustic phonon scattering (with a mean free path of ~1μm) dominates and the simulated 20nm long channel is near ballistic. At high V_D, optical and zone boundary phonon scattering (with a mean free path of ~10nm) dominates, which occur even in a 20nm long channel. The NQS effects are due to the fact that carriers travel at a finite average velocity, so that the device can not respond instantaneously. We, therefore, expect that NQS effects become important at a lower frequency in the presence of scattering because the average carrier velocity decreases. The effect of scattering warrants a careful future study, but this work indicates that at the ballistic limit, the NQS effect becomes important when the frequency approaches the intrinsic cut-off frequency.



(a)



(b)

Fig. 3.15 (a) Small signal drain to source and gate to source current vs. frequency at V_{DS} = 0.5 V and V_{GS} = 0.5 V (b) The cutoff frequency vs. gate voltage at V_{DS} = 0.5 V by NQS (line with triangle) and QS (circled line) approaches.

CHAPTER FOUR: ANALYSIS OF METAL INTERCONNECT RESISTANCE OF POWER MOSFET

4.1 Introduction

Power MOSFETs, arguably the most important switching device in modern power electronics, are widely used in computer, telecommunication, and consumer power management as well as automotive systems. During the past decade the power semiconductor industry has made tremendous progress in reducing the on-resistance ($R_{DS(on)}$) of both planar and trench power MOSFETs, particularly in the voltage range below 60 volts. For example, the specific on-resistance ($R_{DS(on,sp)}$) for 30V power MOSFETs was quickly reduced from 100 mΩ·mm^2 for planar DMOS technology [71] to less than 20 mΩ·mm^2 for trench gate DMOS technology [72, 73] in less than five years. Commercial power MOSFETs with $R_{DS(on)}$ as low as 2-3 mΩ are now available from several semiconductor manufacturers. Recently a low-voltage power MOSFET with $R_{DS(on)}$ less than 1 mΩ was also reported by Shen et al. [74]. $R_{DS(on)}$ of a power MOSFET is the resistance between the transistor's source and drain at a specific gate voltage (higher than the threshold voltage), that usually dictates the power loss and efficiency of the power converter where the MOSFET is employed. The rapid reduction in $R_{DS(on)}$ is largely driven by the ever-increasing demands in load current, power efficiency, and power density of power electronic applications in the computer, telecommunication, consumer, and automotive markets.

With the rapid progress in power MOSFET technology, the silicon-contributed $R_{DS(on)}$ has approached the sub-mΩ range. Parasitic elements in a power MOSFET, such as package bond wires and device source metal interconnect, begin to contribute an increasingly large

percentage to the total $R_{DS(on)}$, and become the bottleneck for bringing out the silicon performance. Metal interconnect of a power MOSFET, which is usually a 3-5 μm thick aluminum film on the top side of the MOSFET chip, conducts current from hundreds and thousands parallel MOS cells to the external bond wires or solder pads. Currently, there is, however, insufficient effort in understanding the influence of metal interconnect on the performance of power MOSFET with ultra-low intrinsic $R_{DS(on)}$. It is not a viable solution to simply increase the thickness of the metal film since the aluminum thickness is often limited by the wafer fabrication throughput, and more importantly by the photolithography requirement after the metal deposition. Instead, the design of the metal interconnect layout and the package of a power MOSFET have to be fully optimized to reduce the resistive contribution of the metal interconnect. To this end, computer aided modeling approaches become necessary. However, to the best of our knowledge, no systematic investigation on the subject has ever been reported.

In this chapter, we describe a finite element analysis (FEA) approach to study the influence of metal interconnect on vertical and lateral power MOSFET performance comprehensively. A power MOSFET with an ultra low $R_{DS(on)}$ typically has a large chip size but at the same time a very fine cell pitch (typically 2-4 μm), presenting a difficult case for FEA modeling with a reasonable number of mesh nodes. Certain approximations and assumptions have to be made to simplify the FEA model. We discuss the fundamental physical equations, boundary conditions, and modeling methodology of the FEA model. Vertical power MOSFETs are studied comprehensively for two commercial discrete packages, the D^2PAK and DirectFET^{TM} in terms of various source/gate metal interconnect layout and wirebonds or solder pads designs. The effect of metal interconnect resistance on vertical power MOSFET $R_{DS(on)}$ is investigated assuming the silicon-only specific $R_{DS(on,sp),si}$ of vertical power MOSFETs can be

further reduced to as low as 1 mΩ·mm^2. Lateral power MOSFETs are studied comprehensively for smart power IC and flip chip discrete power MOSFETs. Multi-layer metal interconnect layout of lateral power MOSFETs are optimized to achieve smallest $R_{DS(on)}$. The "debiasing" effect in active device cells caused by interconnect resistance is examined for lateral power MOSFETs.

4.2 Vertical vs. Lateral Power MOSFETs

Vertical trench MOSFETs, which currently dominate the DC/DC converter market, offer very low specific $R_{DS(ON)}$, but suffer from high gate charge and gate capacitance due to the inherent vertical trench gate structure [74]. As the output/input voltages of DC/DC converters continue to decrease, the voltage rating of the synchronous rectifier MOSFETs for many applications can be reduced to below 10V. Within this voltage range, the low channel resistance of trench MOSFET's is overshadowed by the parasitic resistance from the device substrate and package (mainly wirebonds). The concept of lateral power MOSFETs is not new. It was extensively studied long before the trench MOSFET technology became commercially successful a decade ago. Figure 4.1 illustrates the device cross-sectional views of a vertical trench MOSFET and a lateral N-channel MOSFET [74]. The parasitic gate-drain capacitance Cgd (the Miller capacitance) is also labeled in both devices. It is evident that the lateral MOSFET inherently has a much smaller overlap area between its polysilicon gate electrode and N+ drain than the trench MOSFET, and therefore offers a much lower gate capacitance and gate charge. Lateral power MOSFETs used to suffer from relatively high on-resistance since the current flows horizontally along the silicon surface, not as effective as vertical trench MOSFETs in terms of silicon

utilization. However, the on-resistance of lateral MOSFETs has been improved significantly during the last few years. Now the difference in specific $RDS_{(ON)}$ between lateral and trench MOSFETs is only in the range of 10-30% depending on the voltage rating. This factor, in conjunction with an ultra-low gate charge and capacitance, makes the lateral MOSFETs extremely suitable in the high frequency DC/DC converters [74].

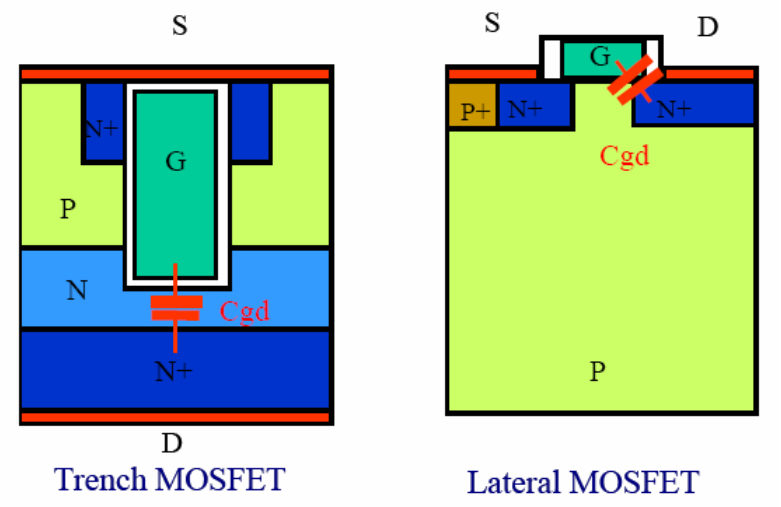


Fig. 4.1 Cross-sectional views of vertical trench MOSFET and lateral N-channel MOSFET with gate-drain capacitance C_{gd} labeled [74].

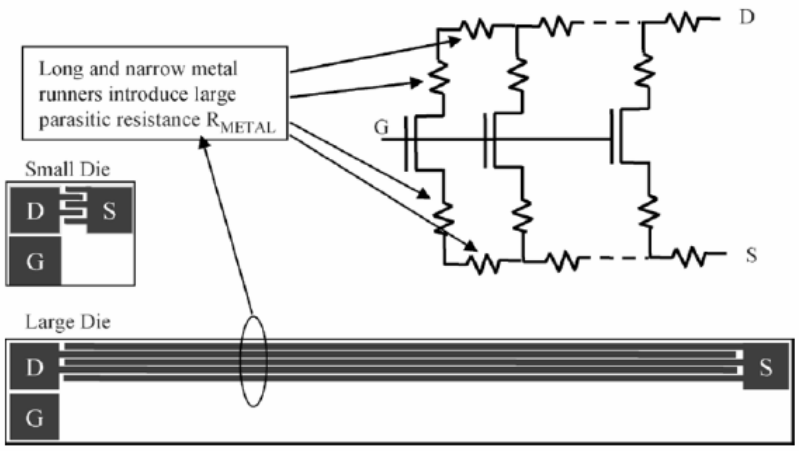


Fig. 4.2 Effect of metal interconnect resistance on lateral MOSFETs [74].

However, the $R_{DS(ON)}$ of conventional lateral MOSFETs deteriorates considerably with increasing device size due to the parasitic resistance of metal interconnects, commonly known as the "scaling issue" [75]. This imposes a fundamental limit on the maximum die size practically achievable by lateral device structures. This is also the main reason why most smart power ICs and lateral discrete MOSFETs only offer a limited power and current rating and are generally not considered sufficiently cost-effective for high current switching power applications. Interconnect resistance does not only add to drain/source series resistance but also causes a "debiasing" effect in active device cells [76], as shown in Fig. 4.2. At the same specific gate voltage, the channel conductivity is reduced because of the increased source voltage. How "debiasing" affect $R_{DS(ON)}$ needs to be examined in detail. All these technical barriers need to be overcome before lateral MOSFETs become a viable solution for high current DC/DC converter applications.

4.3 Modeling Approach

4.3.1 Vertical Power MOSFET

Fig. 4.3(a) illustrates a typical vertical power MOSFET in a wirebond package. Note that the thickness of the MOSFET chip is not up to scale for the purpose of model approximation. The bottom side of the power MOSFET chip is soldered to a metal leadframe, and serves as the drain of the MOSFET. The metal interconnect patterns on the top side of the MOSFET are connected to the source and gate bondwires respectively. The power MOSFET is comprised of many identical cells, which are connected in parallel by the top source metal interconnect. As shown in Fig. 4.3(a), the MOSFET drain current flows vertically from the drain on the bottom, through the MOS channels, to the source metal interconnect on the top. Once reaching the top surface of the MOSFET chip, it starts to flow horizontally along the source metal interconnect to the wirebond(s). Historically, the resistance of source metal interconnect and wirebonds was insignificant when compared to the intrinsic resistance of the MOSFET cells. However, this situation has changed considerably with the continuous reduction of MOS cell on-resistance. For power MOSFETs with a voltage rating below 60 volts, the resistance of source metal interconnect and wirebonds becomes an non-negligible or even the most significant portion in some cases, of the total on-resistance. While the wirebond resistance can be easily calculated and estimated as a lumped resistor, the effect of the source metal interconnect is far more distributive in nature and far more complicated to model and analyze. We propose a three dimensional (3D) finite element analysis (FEA) approach to model the influence of source metal interconnect on power MOSFET performance in this chapter.

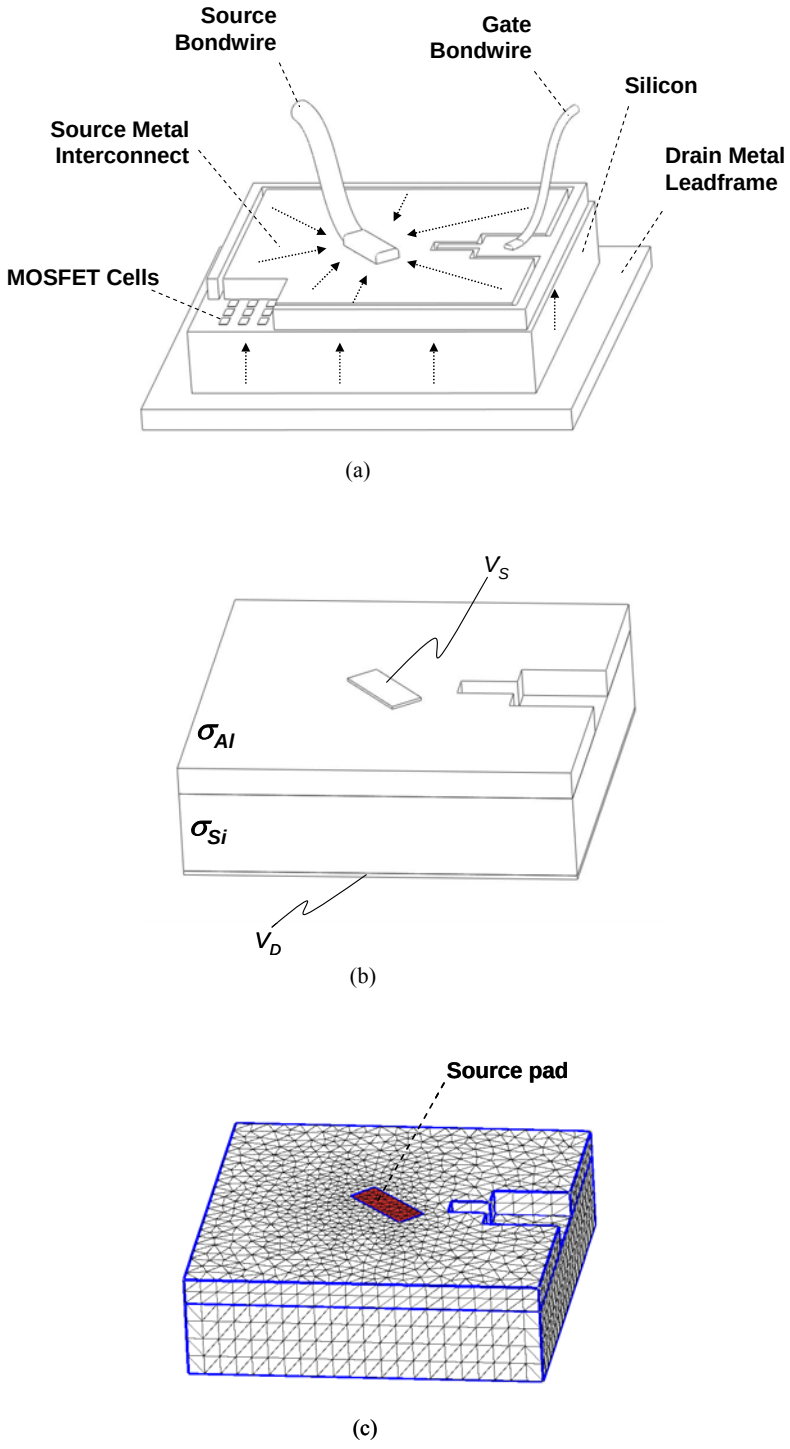


Fig. 4.3 Power MOSFET in a wirebond package: (a) device structure showing wirebonds, front side metal interconnect, silicon die and back side metal, (b) simplified structure for FEA modeling, and (c) tetrahedral discretized mesh structure.

A power MOSFET with an ultra low $R_{DS(on)}$ typically has a large chip size (5-20 mm^2) but at the same time a very fine cell pitch (typically 2-4 μm), making it difficult to build a FEA model for the power MOSFET with a reasonable number of mesh nodes. We have made the following approximations and assumptions to simplify the FEA model:

1. We assume that the silicon part of the power MOSFET is treated as a homogenous silicon "block" that excludes the structural details of the MOS cells. To reduce the number of FEA mesh nodes needed, the silicon "block" is chosen to be just a few micrometers thick, much thinner than the actual MOSFET chip. At the same time, we assume a resistivity for the silicon "block" which is much higher than the actual MOSFET chip so that the silicon "block" has the same specific resistance as the actual power MOSFET (silicon portion only). Note that this equivalent resistivity accounts for all resistive contributions of the MOSFET (including the MOS channel resistance, epi resistance, and substrate resistance) except for that of the source metal interconnect. This approximation allows us to use a limited number of mesh nodes to model a rather complicated chip structure. The uniform current distribution approximation is reasonably accurate since the MOS cell pitch is several thousand times smaller than the chip dimension. Furthermore, while the MOS cells do have slightly different channel resistance due to the difference in their actual gate-source biasing voltage (the so-called debiasing effect), this difference is very small and can be neglected for vertical power MOSFETs biased at a large gate voltage, as will be confirmed by the modeling results in Sections III and IV.
2. We assume that the wirebond footprint area has the same potential since the wirebond is much thicker and thus much more conductive than the source metal interconnect. We assign a single source contact potential V_S to the rectangular-shape wirebond area, and

define that as one of the boundary conditions. However, the bondwire itself is not included into the FEA model since its resistance can be easily calculated as a discrete resistor.

3. We neglect the resistance from the drain metal since its contribution to the total on-resistance is very minimal. We assign a single drain contact potential V_D to the bottom of the silicon "block", and define that as another boundary condition.
4. Various gate voltages will result in different channel resistance of the MOS cells. In order to compare the modeling and measurement data, we select the resistivity of the silicon "block" for a fixed gate voltage . However, the results and conclusions from the modeling work should not be affected by this assumption.
5. The gate finger and pad patterns are excluded from the metal interconnect layer since they do not conduct the drain-source current of the MOSFET.
6. The conductivity of the source metal interconnect σ_{Al} is based on the measured sheet resistance and thickness of the Al source metal. A σ_{Al} of $2.5\times10^5\Omega^{-1}cm^{-1}$ is used for an Al layer of 4 μm in thickness, this corresponds to a sheet resistance of 10 mΩ per square. The equivalent conductivity of the silicon "block" σ_{Si} is selected based on the measured silicon-only $R_{DS(on)}$ of the MOSFET and the selected thickness of the silicon "block", as discussed early.

Figs. 4.3(b) shows the final FEA model used in our analysis respectively. A voltage is applied between the drain contact (V_D) and the source contact (V_S). The total on-resistance of the power MOSFET (excluding the wirebond resistance) can then be calculated based on the voltage and current between the drain and source contacts.

4.3.2 Lateral Power MOSFET

Fig. 4.4 illustrates a typical multi-layer metal interconnect scheme of lateral power MOSFET. Alternate double-layer source and drain metal runners are used to interconnect the slicide source, drain metal in the silicon chip to the top metal pads by via plugs as shown in Fig. 4.4. The source and drain top metal pads are arranged in a checkerboard or interleaved pattern to guarantee that any active cells in the silicon chip have access to one or more of the source or drain pads within a short distance to achieve smaller interconnect resistance. In this kind of structure, layout and metal interconnection variations can be numerous and layout optimization becomes more complex when more metal layers are used.

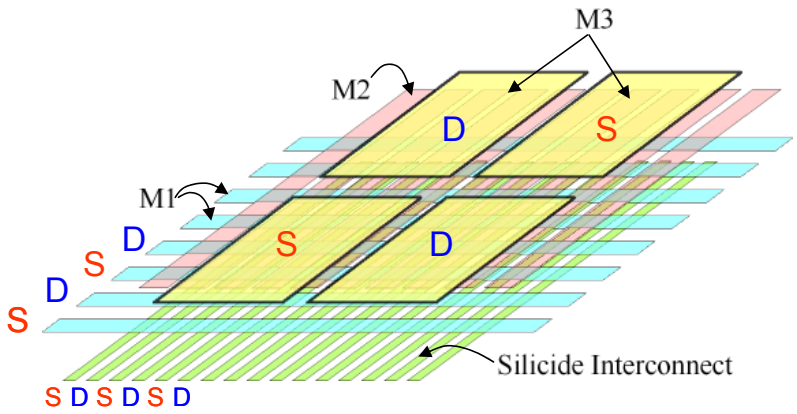


Fig. 4.4 Multi-layer metal interconnect scheme of lateral power MOSFET.

A lateral power MOSFET typically has large chip dimensions of hundreds or thousands of microns but at the same time a fine cell pitch of 2-4 μm. However, compared with vertical power MOSFET modeling, we have to include the very fine cell pitch (typically 2-4 μm) structure into

our model to account for the non-uniform distribution of the current, which presenting a challenge for FEA modeling where only a limited number of mesh nodes may be used. Certain approximations and assumptions must be made to simplify the FEA model as follows:

1. We reduce the actual three-dimensional (3D) device structure to a set of coupled two-dimensional (2D) planes which correspond to different metal layers.
2. We treat via plugs coupling each metal layers as highly conductive and no resistance contributions to the model. As a result, the coupling mesh nodes connecting two layers can be simplified to the same nodes.
3. We reduce the active channel regions of the MOSFET to a two-dimensional "active device layer" that has a variable sheet conductivity σ(x, y) to approximate the resistive behavior of the actual MOS channel regions. In another word, LDMOS channels are treated as a continuous conductive media block.
4. An analytical or empirical σ(x, y) model similar to SPICE models of submicron MOSFETs is used in FEA calculation. Note that σ(x, y) is dependent on the source voltage $V_s(x,y)$ of the MOS channel area at location (x, y), and therefore will account for the "debiasing" effect as $\sigma(x,y) = \sigma_0(1 - \frac{V_S(x,y)}{V_{GT}})$ where σ_0 is the channel sheet conductivity without "debiasing" effect at a specific gate voltage, V_{GT} is the overdrive voltage of the device.
5. Various gate voltages will result in different channel resistance of the MOS cells. In order to compare the modeling and measurement data, we select the resistivity of the silicon "block" for a fixed gate voltage. However, the results and conclusions from the modeling work should not be affected by this assumption.

6. The gate finger and pad patterns are excluded from the metal interconnect layer since they do not conduct the drain-source current of the MOSFET.
7. We assume that in the discrete lateral MOSFET structure, the solder bump area has the same potential since the solder bump is much thicker and thus much more conductive than the metal interconnect. We assign a single contact potential V_S or V_D to the rectangular-shape solder bump area, and define that as one of the boundary conditions. However, the solder bump itself is not included into the FEA model since its resistance can be easily calculated as a discrete resistor.

4.3.3 Model Equations and Boundary Conditions

Our FEA modeling starts from the charge conservation equation:

$$\nabla \cdot \mathbf{J} + \frac{\partial \rho_v}{\partial t} = 0 \tag{4.1}$$

where $\mathbf{J}$ is the current density and ρ_v is the volume charge density.

In our case, the divergence of $\mathbf{J}$ is equal to zero due to the static current condition, i.e.

$$\nabla \cdot \mathbf{J} = 0 \tag{4.2}$$

where $\mathbf{J}$ is related to the intensity of electric field $\mathbf{E}$ by Ohm's law

$$\mathbf{J} = \sigma \mathbf{E} \tag{4.3}$$

Here, σ is the conductivity of the media which can be space dependent.

By substituting equation (4.3) into equation (4.2) and replacing $\mathbf{E}$ with the electrostatic potential V as

$$\mathbf{E} = -\nabla V \tag{4.4}$$

Laplace equation in a 3-D non-uniform media is derived to be

$$\nabla \cdot (\sigma(x,y,z)\nabla V(x,y,z)) = 0 \tag{4.5}$$

Using the Galerkin method [7, 78], equation (4.5) is expressed in the weak form as

$$\iiint_{\Omega} \sigma(\frac{\partial V}{\partial x}\frac{\partial W_m}{\partial x} + \frac{\partial V}{\partial y}\frac{\partial W_m}{\partial y} + \frac{\partial V}{\partial z}\frac{\partial W_m}{\partial z})dxdydz - \iint_{\Gamma} W_m \sigma(\frac{\partial V}{\partial x}\hat{x} + \frac{\partial V}{\partial y}\hat{y} + \frac{\partial V}{\partial z}\hat{z}) \cdot \hat{n} d\Gamma = 0 \tag{4.6}$$

where $\hat{n}$ is normal to Γ, the boundary of device region Ω and W_m is the weighting function.

Before applying the finite element calculation, the device regions must be discretized. Fig. 4.1(c) shows the discretized structure with tetrahedral elements.

Then, by using the potential value at the nodes of each element, $V(x,y,z)$ can be approximated as

$$V(x,y,z) = \sum_{e=1}^{N_e}\sum_{j=1}^{4} V_j^e N_j^e(x,y,z) \tag{4.7}$$

where V_j^e is the unknown electrostatic potential at the node i of element e and $N_j^e(x,y,z)$ is the 3D linear interpolation function at the node i of the element e [7].

By substituting equation (4.7) into equation (4.6) with $W_m = N_i^e$, the elemental form of equation (4.6) is

$$[K_{ij}^e]\{V_j^e\} = \{g_i^e\} \qquad i,j = 1,2,3,4 \tag{4.8}$$

where

$$K_{ij}^e = \iiint_{\Omega^e} \sigma(x,y,z)(\frac{\partial N_i^e}{\partial x}\frac{\partial N_j^e}{\partial x} + \frac{\partial N_i^e}{\partial y}\frac{\partial N_j^e}{\partial y} + \frac{\partial N_i^e}{\partial z}\frac{\partial N_j^e}{\partial z})dxdydz \tag{4.9}$$

$$g_i^e = \iint_{\Gamma^e} N_i^e \sigma(x,y,z)(\frac{\partial V}{\partial x}\hat{x} + \frac{\partial V}{\partial y}\hat{y} + \frac{\partial V}{\partial z}\hat{z}) \cdot \hat{n}_e d\Gamma \tag{4.10}$$

The boundary conditions to be considered here are 1) If node i is on the contact, V_i takes the value of contact potential (Dirichlet boundary). 2) If node i is on parts of Γ lying between contacts (insulating boundary), $\nabla V \cdot \hat{n}_e = 0$, so $g_i = 0$.

Assembling K_{ij}^e, V_j^e, g_j^e to the systematic matrix $\mathbf{K}, \mathbf{V}, \mathbf{G}$ will result in the following expression, with which V at each node is solved.

$$[K]\{V\} = \{\mathbf{G}\} \tag{4.11}$$

For the vertical MOSFET structure, equation (4.11) is a linear equation and can be solved directly. But for the lateral MOSFET structure, equation (4.11) becomes a nonlinear equation since matrix $\mathbf{K}, \mathbf{G}$ is a function of $\mathbf{V}$ because of the "debiasing" effect. The iteration algorithm is necessarily employed to solve this nonlinear equation. The simulation steps are listed as follows:

Step 1: Initialize the channel conductivity as σ_0.

Step 2: Solve the equation (4.11) to get $\mathbf{V}_0$.

Step 3: Update the channel conductivity by $\mathbf{V}_0$.

Step 4: Solve the equation (4.11) with the updated channel conductivity to get $\mathbf{V}_1$.

Step 5: If the error between the new and old $\mathbf{V}$ is within the predefined tolerance, the simulation stops, otherwise go to **Step 2** for iteration.

The current density at each node is calculated by combing equations (4.3) and (4.4). The total current I is evaluated at the drain contact by

$$I = \iint_{S_D} \mathbf{J} \cdot \hat{m} ds \tag{4.12}$$

where $\hat{m}$ is normal to the drain contact area S_D.

Finally, the on-resistance $R_{DS(on)}$ of the power MOSFET is calculated by using

$$R_{DS(on)} = \frac{V_{DS}}{I} \tag{4.13}$$

4.4 Case Study A: A 40V/85A Power MOSFET in D^{2}PAK Package

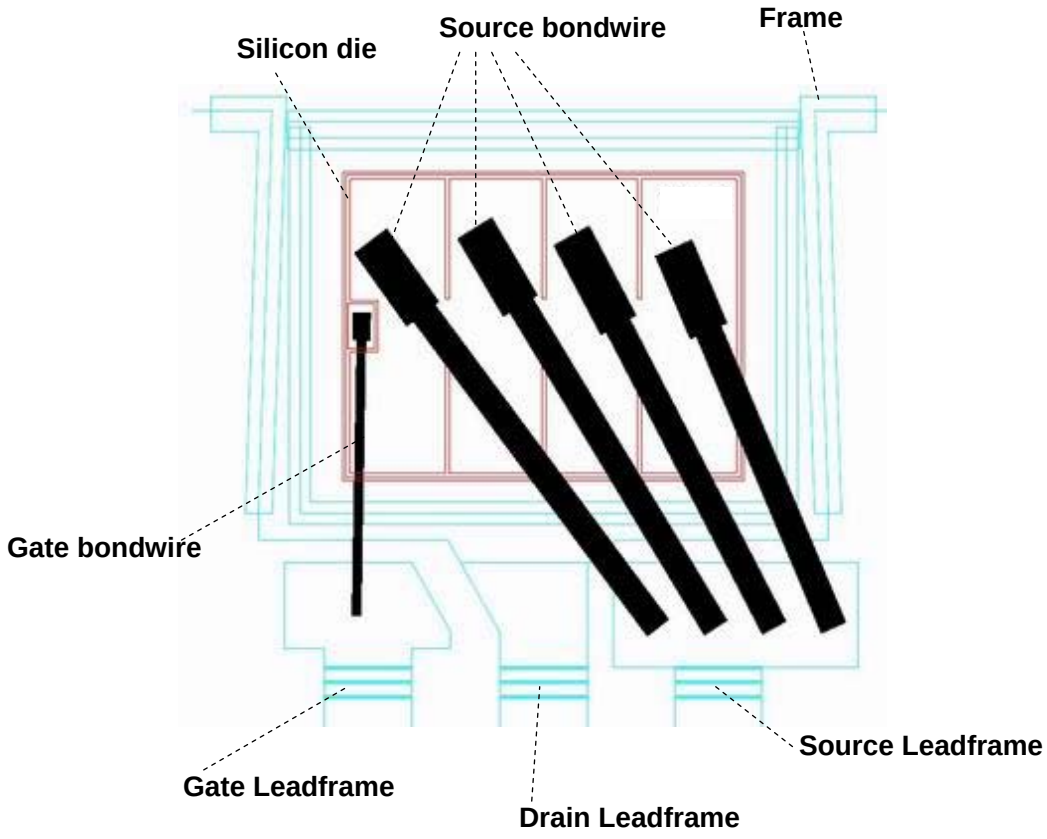


Fig. 4.5 Wirebond diagram of a 40V/85A power MOSFET packaged in D2PAK.

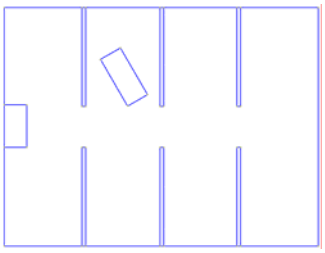
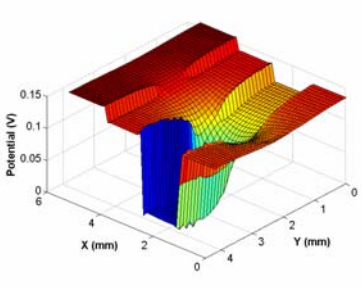
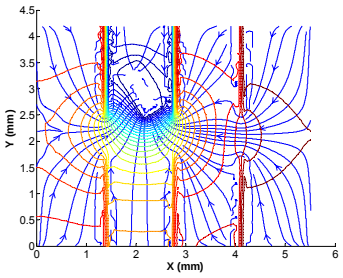
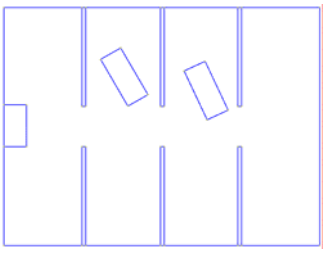
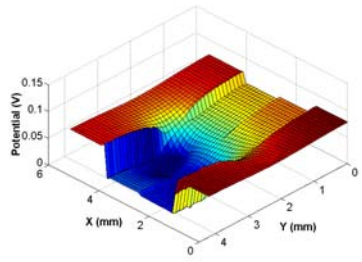
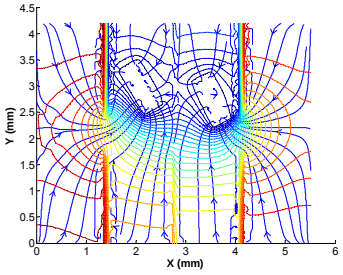
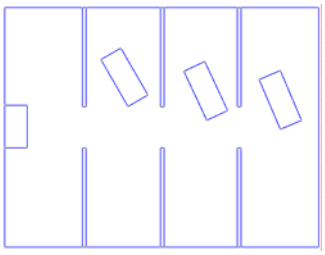
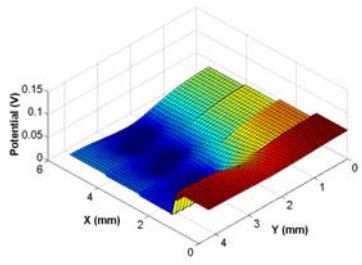
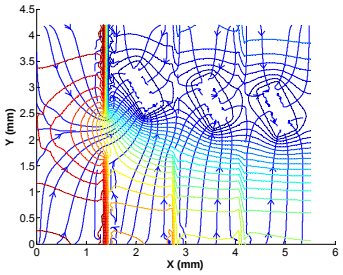
We study the influence of source metal interconnect on a commercial 40V/85A power MOSFET packaged in D^{2}PAK package by applying the FEA methodology described above. D^{2}PAK is one of the most commonly used standard surface mount (SMT) packages for power

MOSFETs. Similar to what is shown in Fig. 4.3(a), the drain of a power MOSFET die on its back side is soldered onto the copper leadframe of a D^2PAK package. The source and gate of the power MOSFET on its top side are connected to the package leads through bondwires. The top view of the surface metal connection is shown in Fig. 4.5. More than one source bond wires are often used to minimize the package resistance. The D^2PAK package is finally encapsulated with plastic molding compound. The power MOSFET under study has a die size of 5.84 mm by 4.37 mm, which is also the maximum die size that a D^2PAK package can accommodate. The power MOSFET has a typical $R_{DS(on)}$ of 3.0 mΩ at a gate voltage of 10V. The resistance of the four aluminum bond wires of 0.38 mm (or 15 mils) in diameter is estimated to be 0.45 mΩ (or 1.8 mΩ for each bond wire). The on-resistance of the 40V/85A power MOSFET excluding the wirebond contribution is approximately 2.55 mΩ.

The source metal interconnect is typically a solid metal slab which is interrupted only by the gate runners and gate pad at several locations as shown in Fig. 4.5. The purpose of the gate metal runners is to help propagate the gate signal quickly to all MOS cells on the chip. However, their existence inadvertently changes the source current flow pattern and increase the interconnect resistance. It is therefore interesting to study the influence of the source/gate metal layout on the total $R_{DS(on)}$ of the power MOSFET, and to find an optimum layout design which offers both a low source metal resistance and a small gate signal propagation delay time. It is also interesting to know how much the source metal interconnect contributes to the total $R_{DS(on)}$ for a given MOSFET design.

The actual MOSFET chip under study has four aluminum wirebonds at the locations shown in Fig. 4.5. The use of multiple source wirebonds helps reduce both the total wirebond

resistance and the source interconnect resistance contribution, but adds extra packaging cost. The source metal resistance is also influenced by the location of wirebonds. It is therefore interesting to find the most effective number and locations of wirebonds for a given MOSFET chip. Ideally this factor should be taken into consideration for the layout design of the source and gate metal interconnect layer.

	Device Source Metal Interconnect Pattern (top view)	**Potential Distribution of Source Metal Interconnect**	**Current Flowlines & Equi-Potential lines of Source Metal Interconnect**
(a)			
(b)			
(c)			

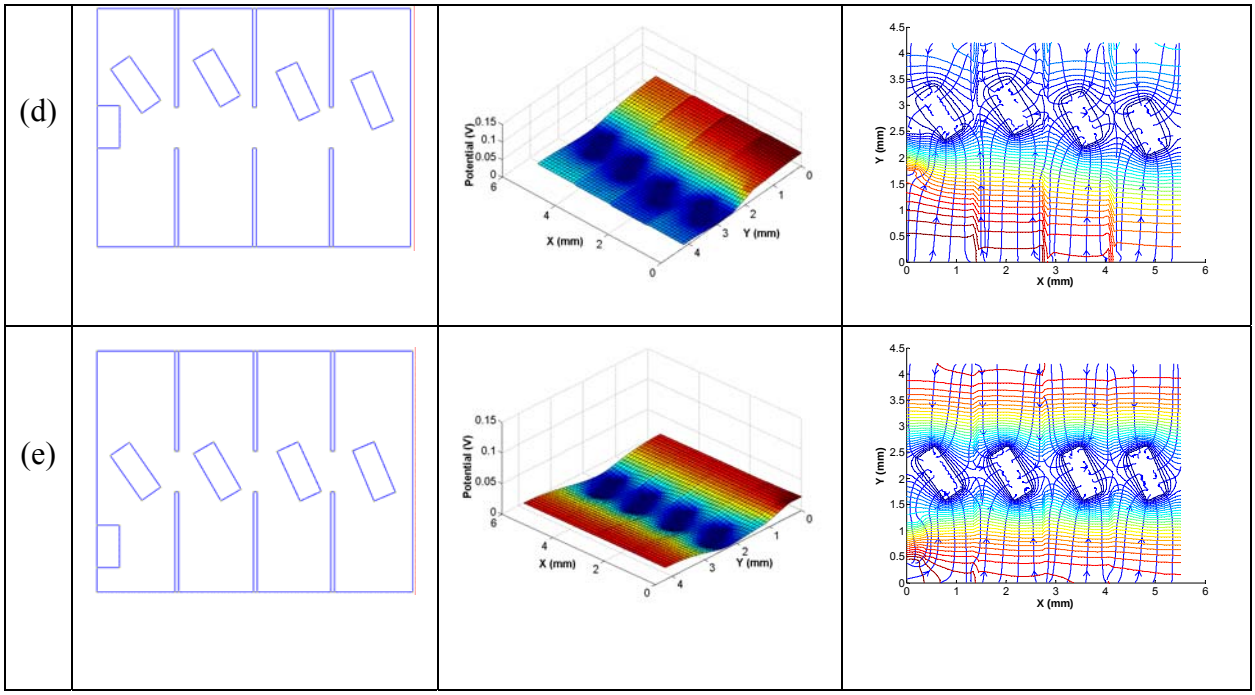


Fig. 4.6 Surface potential distributions, equi-potential lines, and current flowlines from FEA modeling for different number and location of wirebonds in D2PAK: (a) single- wirebond, (b) two-wirebonds, (c) three-wirebonds, (d) four-wirebonds and (f) four- wirebonds with central locations.

We investigate the cases of using one, two, three and four wirebonds with the same silicon substrate and source/gate metal layout design. The wirebond locations for these four cases are shown in Figs. 4.6(a), (b), (c), and (d) respectively. Fig 4.6(d) represents the case of the actual power MOSFET. We also study the effect of moving the four wirebonds to more center locations on the MOSFET chip as shown in Fig 4.6 (e). Figs 4.6(a)-(e) also shows the 3D potential distribution contours, 2D equi-potential lines and current flow lines on the source metal interconnect, based on our FEA modeling results with a current of 30A flowing from the drain to source of the power MOSFET. As shown in Figs. 4.6, the top source metal layer is divided into four regions by the gate metal runners. In each region, the source metal will bring up the current

from the underneath silicon MOS cells to the wirebonds. In the case of single-wirebond, the current in all four source metal regions have to converge to a single wirebond outlet. This leads to a long current path (refer to the current flowlines in Fig. 4.6(a)) and a large voltage drop across the source metal layer (refer to the potential distribution contours in Fig. 4.6(a)). As a result, the equivalent metal interconnect resistance is high. The situation is gradually improved in the cases of two- and three-wirebonds. In the case of four-wirebonds, the currents in the four source metal regions are mostly collected locally by the source pad in each region. This eliminates the long current path and results in a low equivalent metal interconnect resistance. The effect of the source metal interconnect resistance can be further reduced when the four wirebonds are placed along the center line of the MOSFET chip. Note that we did not include the debiasing effect of the MOS cells into the FEA model. This assumption is further justified by the modeling result. Even with the worst case of single-wirebond, the difference in the source voltage among the MOS cells are shown to be below 0.15 volts, which is insignificant when compared to the 10V gate voltage used.

Fig. 4.7 compares the $R_{DS(on)}$ of the power MOSFET for the five cases included in Fig. 3(a)-(e). The $R_{DS(on)}$ excluding the contribution from the source metal interconnect, or the so-called silicon-only on-resistance, is included as a reference point to demonstrate the effect of the source metal resistance. Note that all the $R_{DS(on)}$ data in Fig. 4.7 exclude the contribution of the wirebond resistance. One can simply add 1.8 mΩ, 0.9 mΩ, 0.6 mΩ, and 0.45 mΩ as the estimated wirebond resistance to get the total $R_{DS(on)}$ for the cases of one-, two-, three-, and four-

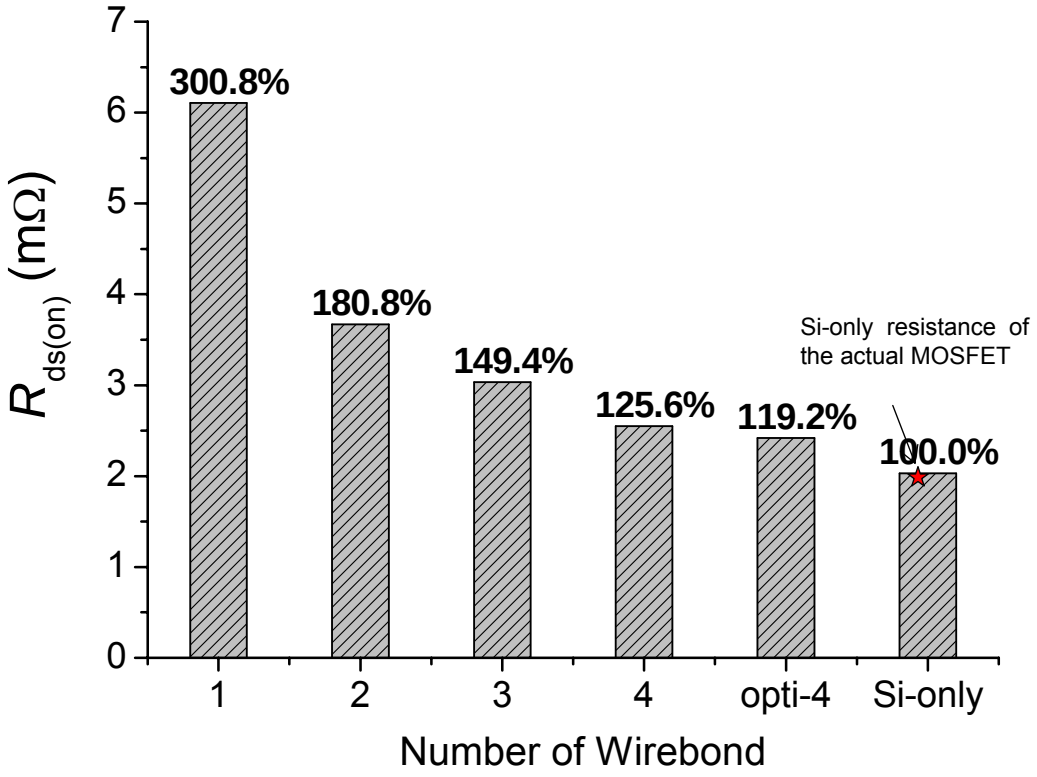


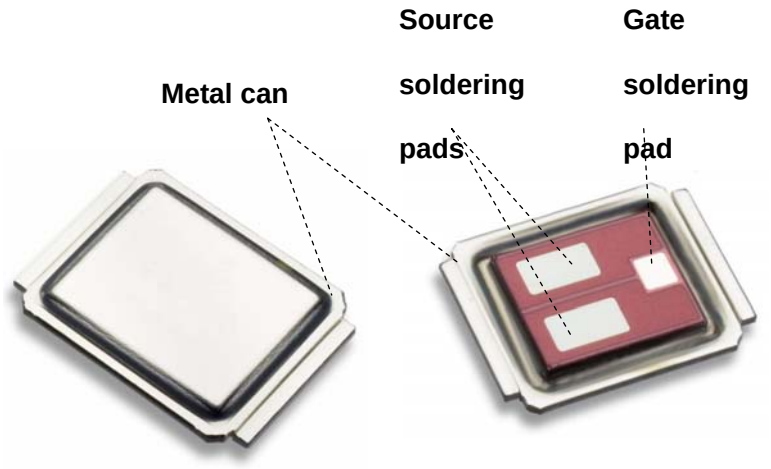
Fig. 4.7 Effects of metal interconnect resistance on the total on-resistance of the power MOSFET for different number of wirebonds in D2PAK.

wirebond D^2PAK respectively. The silicon-only on-resistance is obtained by increasing conductivity of the metal interconnect layer by a factor of 10^5 in the FEA calculation. The influence of metal interconnect on the $R_{DS(on)}$ of the power MOSFET is clearly shown by the percentages normalized by the silicon-only on-resistance. The four-wirebond design shown in Fig. 4.6 (d) is the actual design of the commercial part. The source metal interconnect adds about 0.5 mΩ or 25.6% more parasitic resistance to the intrinsic silicon on-resistance in this case, which is about the same as the contribution from the wirebonds themselves. The FEA model

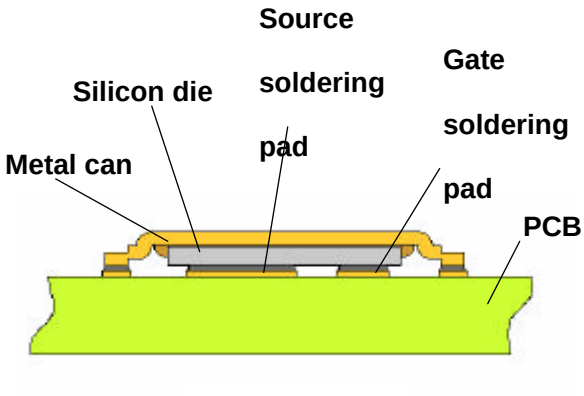
predicts a total $R_{DS(on)}$ of 3.0 mΩ (after adding the wirebond resistance of 0.45 mΩ) for the power MOSFET, which agrees reasonably well with the typically measured $R_{DS(on)}$ of 3 mΩ. By moving the wirbonds to the center line of the MOSFET chip as shown in Fig. 4.6 (e), the parasitic interconnect resistance can be reduced to 19.2% of the intrinsic silicon on-resistance. For the cases of one-, two-, and three-wirebonds, the contribution from the source metal interconnect is much more significant, each adding 200.8%, 80.8%, and 49.4% more parasitic resistance to the intrinsic silicon on-resistance respectively.

With the specific $R_{DS(on)}$ of today's low-voltage power MOSFETs being reduced to below 40 mΩ·mm^2, the parasitic resistance of the source metal interconnect of power MOSFET chips as large as the D^{2}PAK size becomes increasingly significant. It may even exceed the sum of the intrinsic silicon and wirebond resistance altogether in some designs. For D^{2}PAK power MOSFETs, it is wise to use at least four wirebonds to leverage the latest advances in power MOSFET fabrication technology. In the long run, packages without using wirebonds such as the DirectFET^{TM} to be discussed in the next section are preferred in terms of minimizing the parasitic resistance of power MOSFETs.

4.5 Case Study B: 30V/30A POWER MOSFET in DirectFET™ Package



(a)



(b)

Fig. 4.8 Concept of DirectFETTM package: (a) device photo and (b) cross-sectional view.

DirectFET™ is a new wirebondless package developed by International Rectifier [79]. As shown in Fig. 4.8, a power MOSFET chip is placed into a metal can with its drain surface bonded to the internal can shell. The source surface has solderable gate and source pads which can be directly soldered onto the printed circuit board. This structure totally eliminates any lead-

frames and wirebonds. It is reported that the DirectFET^{TM} package can reduce the parasitic package resistance (Die-Free Package Resistance, or DFPR) to as low as 0.15 mΩ [80].

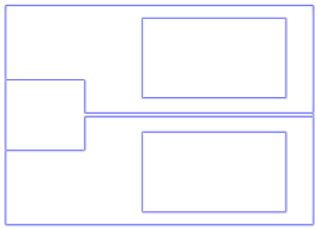
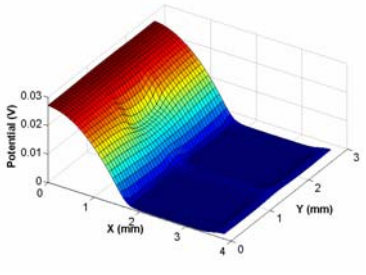
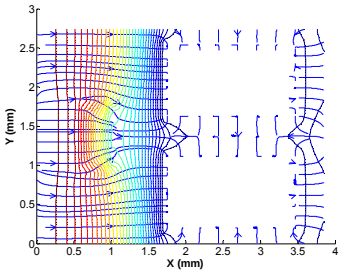
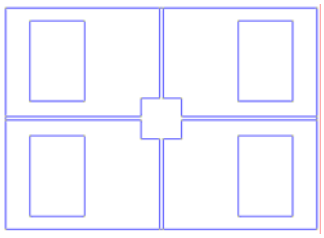
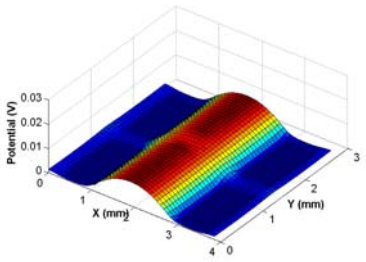
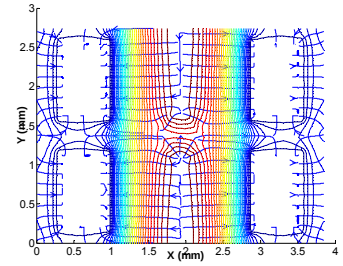
	Device Surface Metal Interconnection Pattern (top view)	**Potential Distribution of Surface Metal Interconnection**	**Current Flowlines & Equi-Potential lines of Surface Metal Interconnection**
(a)			
(b)			

Fig. 4.9 Surface potential distributions, equi-potential lines, and current flowlines from FEA modeling for different interconnection patterns in DirectFETTM: (a) design of the commercial MOSFET, (b) optimized layout design.

By applying the FEA methodology, we investigate the effect of source metal interconnect resistance on a commercial 30V/30A power MOSFET in DirectFET^{TM} package (IRF6618). This commercial power MOSFET has chip size of 3.85 mm by 2.74 mm, and a typical $R_{DS(on)}$ of 2.2 mΩ at a gate voltage of 10V. It has one gate pad and two large source pads as shown in Fig. 4.8.

The DirectFET^{TM} chip is divided into two identical halves by a central gate runner. It is interesting to know how much the source metal interconnect contributes to the total $R_{DS(on)}$ for the DirectFET^{TM} as in comparison to the conventional packages such as D^{2}PAK. We first model the DirectFET^{TM} in its current source/gate layout form (Fig. 4.9(a)), and then propose a new layout design to further reduce the parasitic metal resistance as shown in Fig. 4.9(b). The new layout has four identical sections divided by gate runners, and a smaller gate pad right at the center of the MOSFET chip. A smaller source pad is placed in each of the four sections. Care is taken to make sure that PCB assembly design rules are followed, and the requirements on the minimum dimensions of and spacing between solder pads are met. Note that we assign a single source contact potential V_S to all the source pads in the FEA model since these source pads are effectively shorted by the highly conductive copper interconnect on the PCB.

Figs. 4.9(a) and (b) shows the 3D potential distribution contours, 2D equi-potential lines and current flow lines on the source metal interconnect for the two DirectFET^{TM} layout designs respectively, based on our FEA modeling results with a fixed current of 30A flowing from the drain to source of the power MOSFET. Fig. 4.10 compares the $R_{DS(on)}$ of the two layout designs and the intrinsic silicon on-resistance. Again the silicon-only on-resistance is obtained by increasing conductivity of the metal interconnect layer by a factor of 10^5 in the FEA calculation. It is observed that the source metal interconnect of the existing layout design adds 0.36 mΩ or 19.8% more parasitic resistance to the intrinsic silicon on-resistance. This is a quite significant contribution considering that the wirebond parasitic resistance is completely absent in the DirectFET^{TM} package. In contrast, the source metal interconnect of the new optimized layout design adds only 0.13 mΩ or 7.3% more parasitic resistance to the intrinsic silicon on-resistance. The rationale behind this improved layout design is to shorten the current paths in the source

metal interconnect. By comparing the current flowline plots in Figs. 4.9(a) and (b), it can be seen that the surface current in the new source layout takes a much shorter path to reach the source pad in each of the four sections on the MOSFET chip. A much larger variation in potential across the surface interconnect is observed in the existing design than the new design.

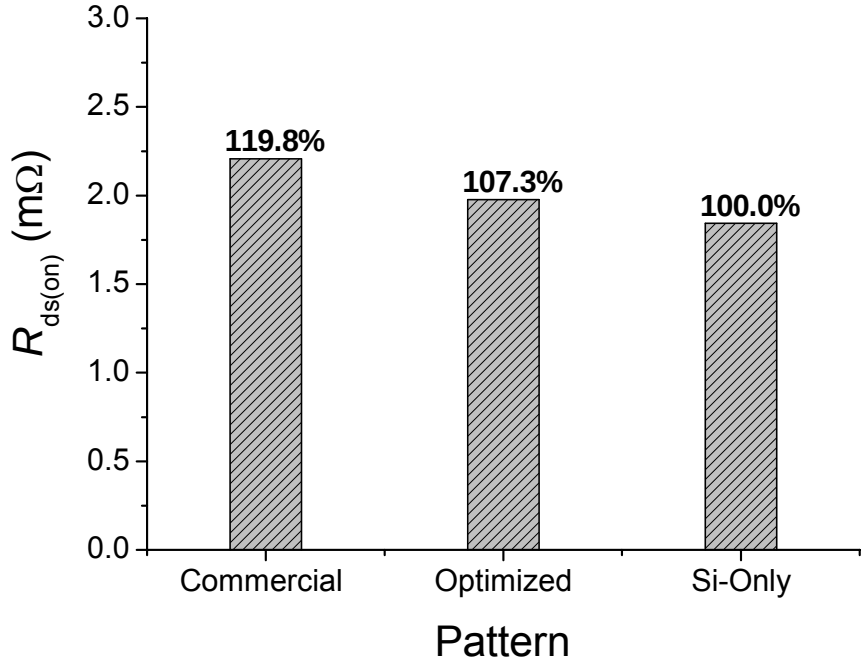


Fig. 4.10 Effects of metal interconnect resistance on the total on-resistance of the power MOSFET for different metal interconnect patterns in DirectFETTM.

In short, despite of the absence of wirebond parasitic resistance, the DirectFET still suffers from a 19.8% increase in $R_{DS(on)}$ due to the contribution from the source metal interconnect. An improved layout design can help reduce this contribution to below 7.3%.

4.6 Effect of Metal Interconnect Resistance with Further Reduction of Intrinsic Silicon On-resistance of Vertical Power MOSFETs

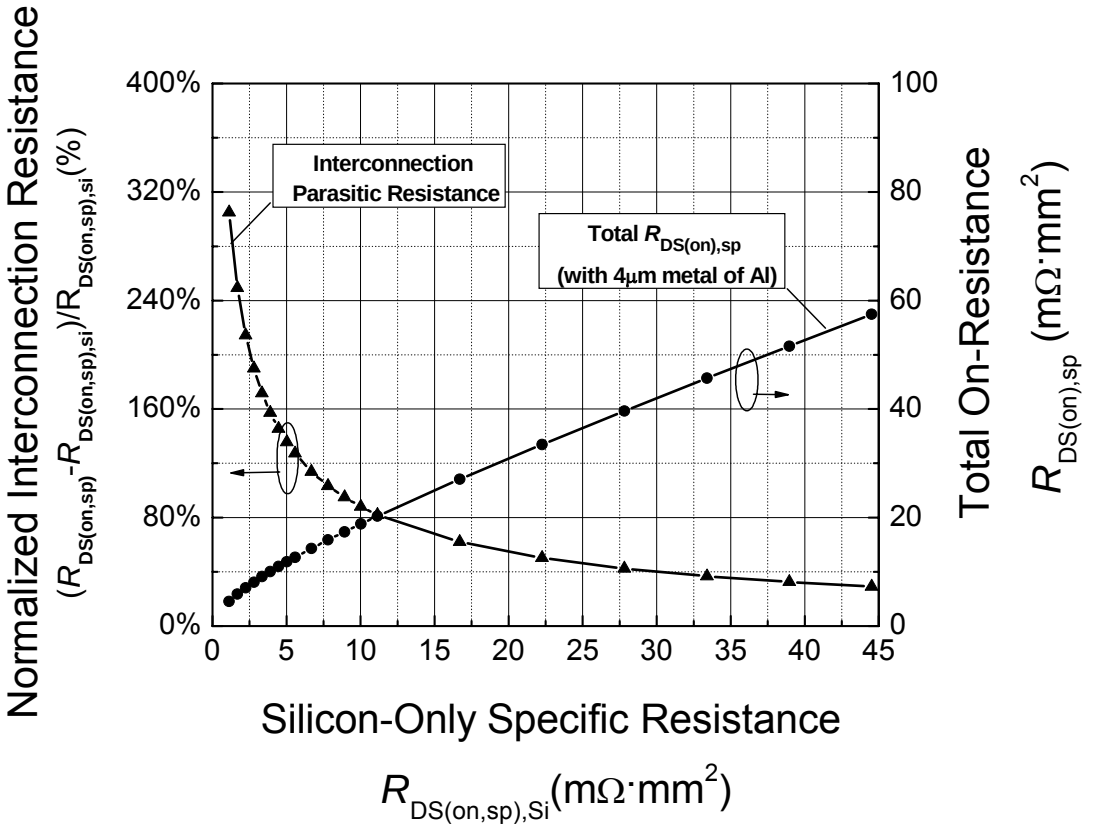


Fig. 4.11 Contribution of the source metal interconnect resistance vs. intrinsic silicon specific on-resistance.

The influence of source metal interconnect resistance is investigated assuming that technological advances can further reduce the intrinsic silicon on-resistance to a level much lower than what is achieved today. The question is whether or not the parasitic resistance can also be reduced at a similar rate as the intrinsic silicon specific on-resistance being reduced to as low as 1mΩ·mm^2 for low-voltage power MOSFETs. The basic four-wirebond D^{2}PAK power

MOSFET shown in Fig. 4.5 is used as an example to conduct this study. Fig. 4.11 shows the total specific $R_{DS(on)}$ and the ratio between the parasitic resistance from metal interconnect and the intrinsic on-resistance of the MOS cells as a function of the intrinsic silicon specific on-resistance. It is observed that the total $R_{DS(on)}$ decreases with decreasing intrinsic silicon on-resistance but at a slower rate. This is due to the increasing contribution from the parasitic metal interconnect resistance. As the intrinsic silicon on-resistance is reduced, the influence of the metal interconnect becomes more and more significant.

When the intrinsic silicon specific on-resistance is between 10 and 45 mΩ·mm^2, the contribution of the metal interconnect parasitic resistance is about 40-100% of the intrinsic silicon specific on-resistance. This contribution is mainly in the form of added series resistance along the horizontal current path on the top surface metal of the chip. Note that all MOS cells conduct current vertically across the entire chip. While the source metal resistance remains the same, its relative contribution to the total $R_{DS(on)}$ continues to increase with the decreasing intrinsic silicon on-resistance.

If the intrinsic silicon specific on-resistance is between 5 and 10 mΩ·mm^2, the resistance contribution from the metal interconnect exceeds that of the silicon MOS cells. If the intrinsic silicon specific on-resistance is further reduced to less than 5 mΩ·mm^2, the contribution from the metal interconnect resistance increases dramatically. For example, the interconnect resistance contribution will be three times greater than the intrinsic silicon resistance if the silicon technology could deliver an intrinsic specific on-resistance of 1mΩ·mm^2. This is mainly due to the effect of current crowding under the wirebonds and the reduction of effective MOSFET active area. When the vertical on-resistance of the MOS cells is reduced to less than the lateral

resistance of the source metal interconnect, the MOSFET current from the drain will be confined only to the MOS cells directly under the wirebond rather than across the entire chip since this provides the least resistive path. The $R_{DS(on)}$ of the power MOSFET no longer depends on the total chip area but rather only the area of the wirebond footprint. Figs. 4.12(a) and (b) illustrate the current flows for a moderate and ultra-low intrinsic silicon on-resistance respectively. Figs. 4.13(a) and (b) compare the potential distributions across the surface metal interconnect layer for an intrinsic silicon specific on-resistance of 40mΩ·mm^2 and 1mΩ·mm^2 respectively. Under the same conducting current of 30A, Fig. 4.13(a) shows a significant potential change across the whole interconnect surface. This indicates that the lateral current in the interconnect layer is quite substantial. In the contrast, Fig. 4.13(b) shows a flat potential profile in most part of the interconnect surface as a result of very little lateral current in these regions. The potential changes dramatically only near the wirebond footprint regions, indicating the current crowding effect.

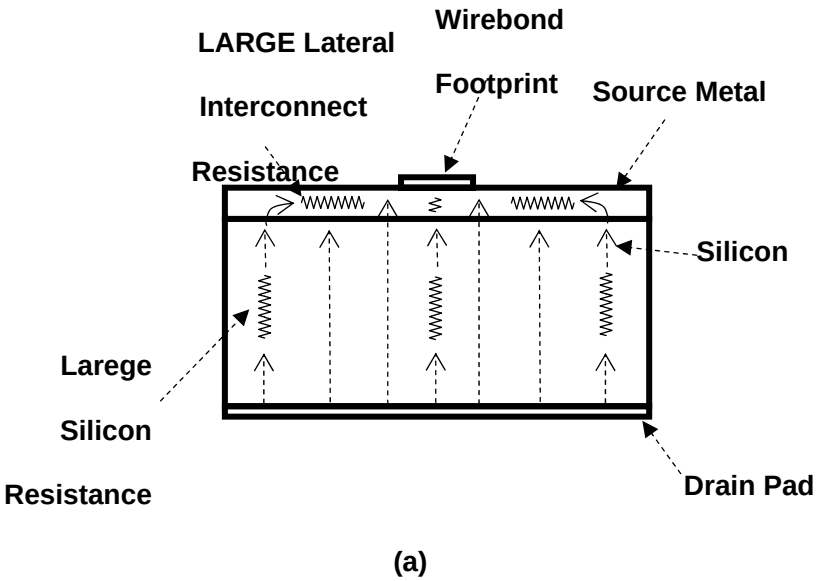
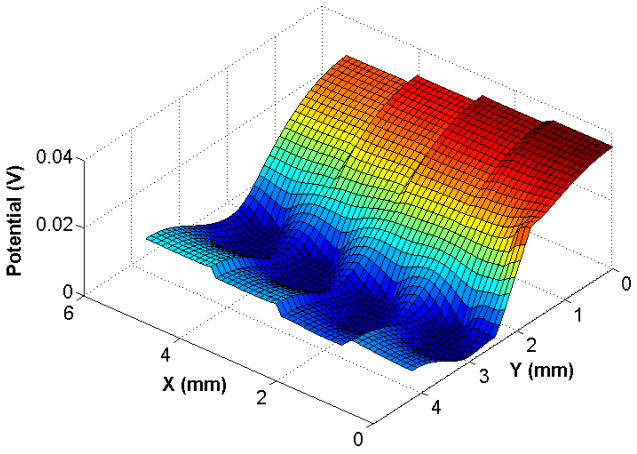
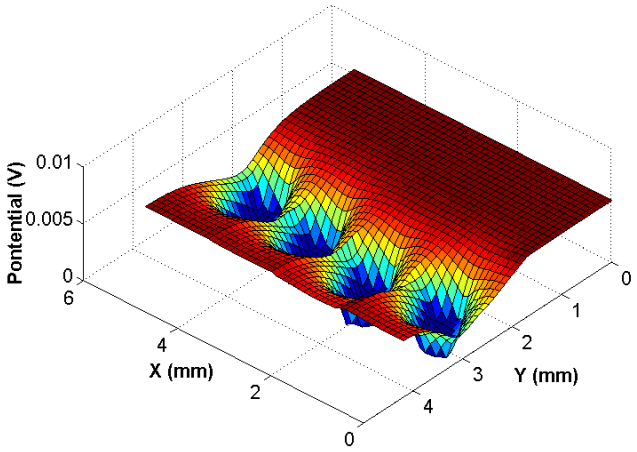


Fig. 4.12 Surface metal potential distributions for: (a) intrinsic silicon on-resistance of 40mΩ·mm2, and (b) intrinsic silicon on-resistance of of 1mΩ·mm2.



(a)



(b)

Fig. 4.13 Comparison of the normalized potential profiles along the cutline of x=2.1368mm.

The source metal interconnect will become a major limiting factor of bringing out the full silicon performance as technological advances further reduce the intrinsic silicon on-resistance. Power MOSFETs with 3-5 μm aluminum metal in wirebond packages will no longer be sufficient. Electro-plated thicker copper top metal and/or wirebondless packages may be required to overcome this technical barrier.

4.7 Case Study C: Lateral Power MOSFET in Smart Power IC

The increasing requirements of multi-functionality and compact size electronic system inevitably necessitated power IC development. To achieve high current carrying capability with minimum power dissipation, the approaches of scaling the power MOSFET are adopted [75] as 1) the channel length is scaled down; 2) a multi-cell layout pattern is used to maximize the effective channel width per unit area; 3) scaling of metal interconnect pitch and an increase in the number of metal layers is used to lower the on-resistance. The following sections will give a comprehensive study of the interconnect limitation, scaling issues and metal interconnect layout optimizations for large area lateral power MOSFETs.

4.7.1 Single Metal Layer LDMOS Finger

Single metal-layer LDMOS finger is the basic building block of more complicated multi-metal layer LDMOS structures. It is also used in low-cost single-metal layer power ICs. The metal runners in a finger structure can be either designed with the same side source and drain contact or the opposite side source and drain contact placement as shown in Fig. 4.14.

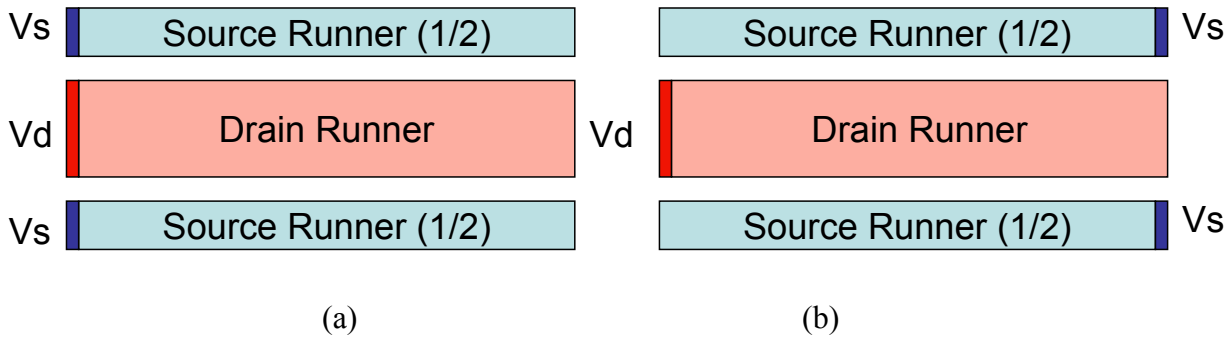


Fig. 4.14 (a) Same side S/D arrangement (b) Opposite side S/D arrangement.

A cell pitch of 5 μm, a source and drain metal runner of 2 μm, a MOSFET (Si only) specific R_{DSON} of 30 mΩ-mm^2, and a metal sheet resistance of 80 mΩ per square are assumed.

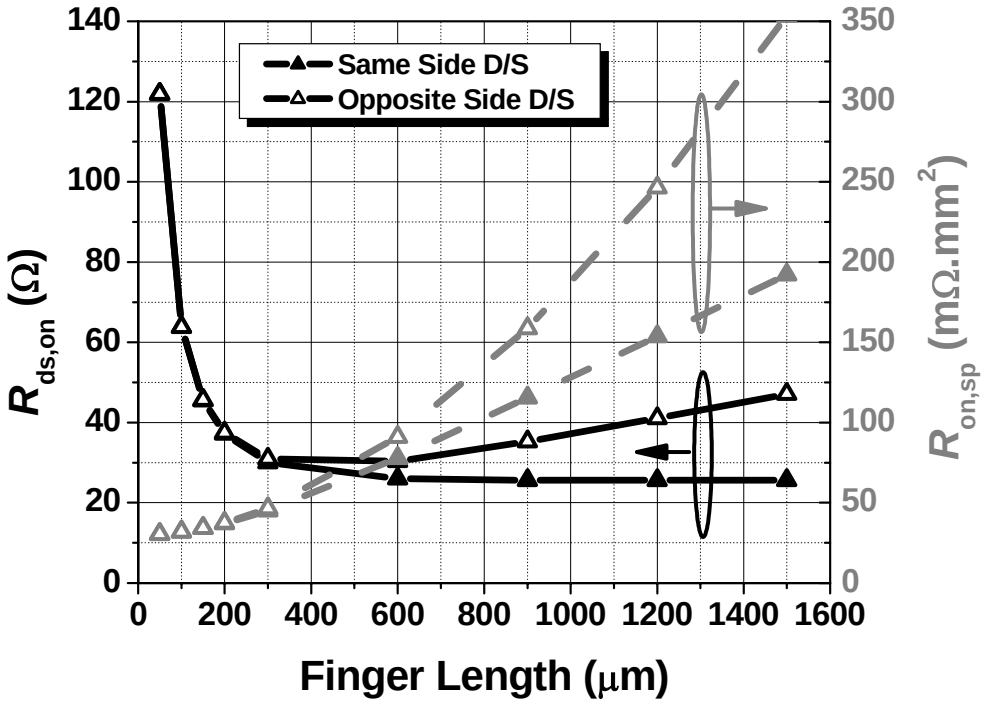


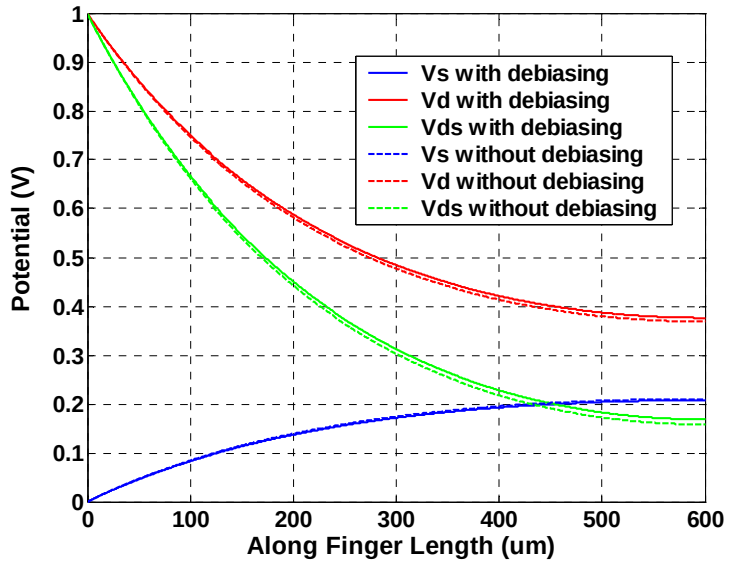
Fig. 4.15 Finger length dependence of Rds,on and Ron,sp.

Finger length dependence of $R_{ds,on}$ and $R_{on,sp}$ ($R_{ds,on} \cdot A$) for two types of S/D arrangement is shown in Fig. 4.15. When the finger length is below 300 μm, with the increasing of the finger length, the total $R_{ds,on}$ of the MOSFET finger is dramatically decreased due to the decreased silicon channel resistance. Beyond 300 μm, the total $R_{ds,on}$ of the MOSFET finger saturates for the same side D/S case, and actually starts increasing for the opposite side D/S case. This phenomenon implies that the increasing of metal interconnect resistance will outweigh the decreasing of silicon channel resistance for longer finger length. For opposite side D/S case,

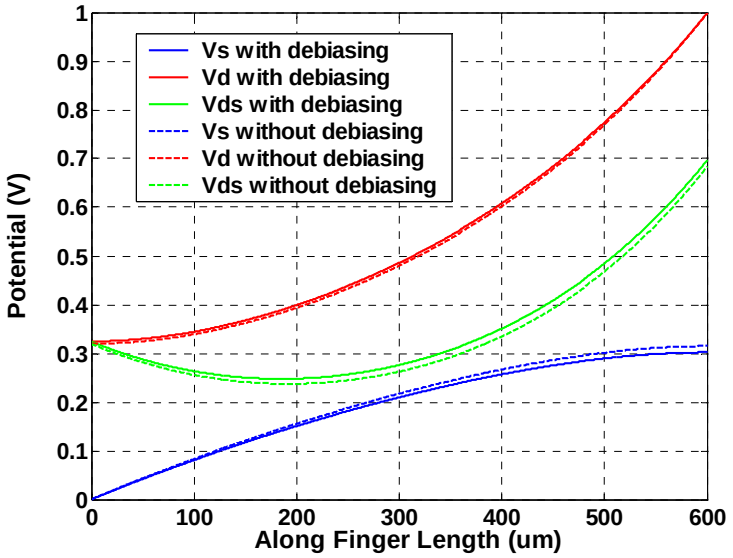
more chip area leads to higher $R_{ds,on}$. Similarly, specific $R_{ds,on}$ increases dramatically for finger length longer than 300 μm. As a result, there is a maximum finger length limit, only below which the scaling of the device width can decease the $R_{ds,on}$ effectively. This finger length limit is also a function of finger pitch, metal sheet resistance and MOSFET (Si only) specific R_{DSON}. As we can expect, smaller pitch or higher metal sheet resistance or lower MOSFET (Si only) specific R_{DSON} will result in smaller finger length limit because the metal resistance will begin to dominate the total resistance at a smaller finger length. Because of the metal resistance, the potential profile along the metal trace is highly non-uniform as shown in Fig. 4.16. The drain voltage drops ~60% and ~70% for the same side and opposite side, respectively. The source voltage increases ~20% and ~30% for the same side and opposite side, respectively.

As we mentioned in previous sections, it is necessary to examine how "debiasing" affect $R_{DS(ON)}$. For the finger length of 600 μm, $R_{DS(ON)}$ of the same side arrangement are 25.96 Ω and 25.62 Ω for the simulation with debiasing and without debiasing, respectively. $R_{DS(ON)}$ of the opposite side arrangement are 30.34 Ω and 29.53 Ω for the simulation with debiasing and without debiasing, respectively. As a result, the debiasing effects only introduce ~2% more resistance. This conclusion can be further verified by Fig. 4.16, which shows the comparison of the potential profiles between the simulation with the debiasing effect and without debiasing effect. The potential profiles have very small difference between these two cases. This can be explained from the nonlinear silicon channel sheet conductivity of $\sigma(x,y) = \sigma_0(1 - \frac{V_S(x,y)}{V_{GT}})$. Generally, the source voltage $V_S(x,y)$ is very small compared with the gate overdrive voltage V_{GT}, which causes the nonlinear effects of this problem are very weak even for the case with large metal interconnection resistance. The "debiasing effect" due to the reduction of the effective V_{GS}

is insignificant comparing to other effects of the metal interconnect. The misconceptions in the previous literature regarding the effect of metal interconnect resistance overestimate this effect.



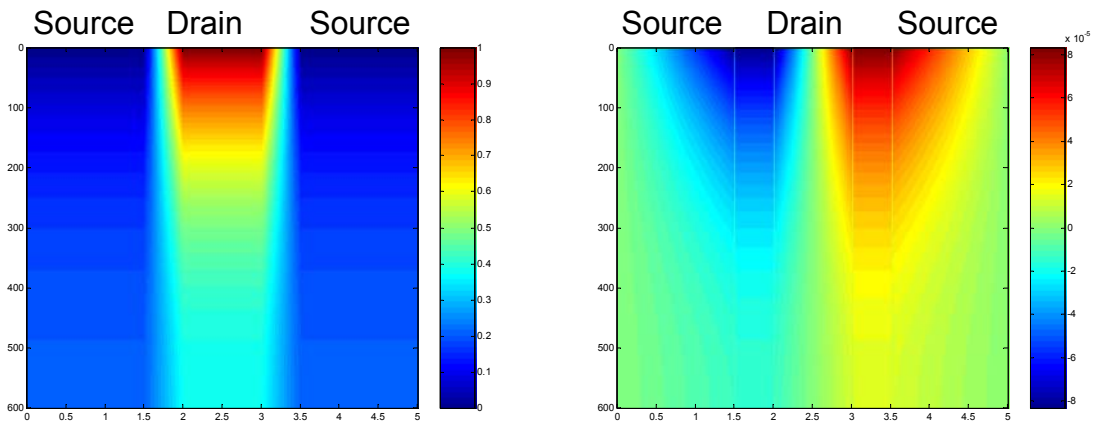
(a)



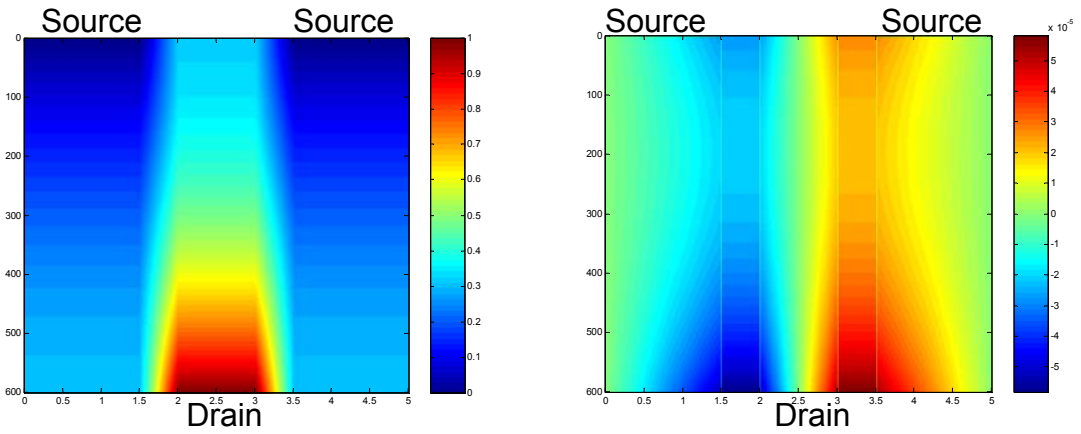
(b)

Fig. 4.16 The potential profile along the 600 μm metal trace for (a) same side S/D arrangement (b) opposite side S/D arrangement. Solid lines are results with debiasing and dash line are results without debiasing.

Both Fig. 4.15 and Fig. 4.16 show that the same side S/D arrangement has better performance than the opposite side S/D arrangement. In order to better understand this, 2D potential and horizontal current density distribution are plotted in Fig. 4.17. In the same side arrangement, due to the shorter path from the drain contact to the source contact, the current flows along the channel experiences less resistance than the opposite counterpart. Consequently, the horizontal current is distributed more non-uniformly in the same side arrangement than the opposite side arrangement. In addition, the same side arrangement has larger maximum horizontal current density near the contacts. Although the same side arrangement has better performance from on-resistance point of view, the non-uniform current distribution is not preferred from ESD point of view. In practical design, systematic considerations need to be taken into account.



(a)



(b)

Fig. 4.17 2D potential (left) and horizontal current distribution (right) for (a) same side S/D arrangement (b) opposite side S/D arrangement.

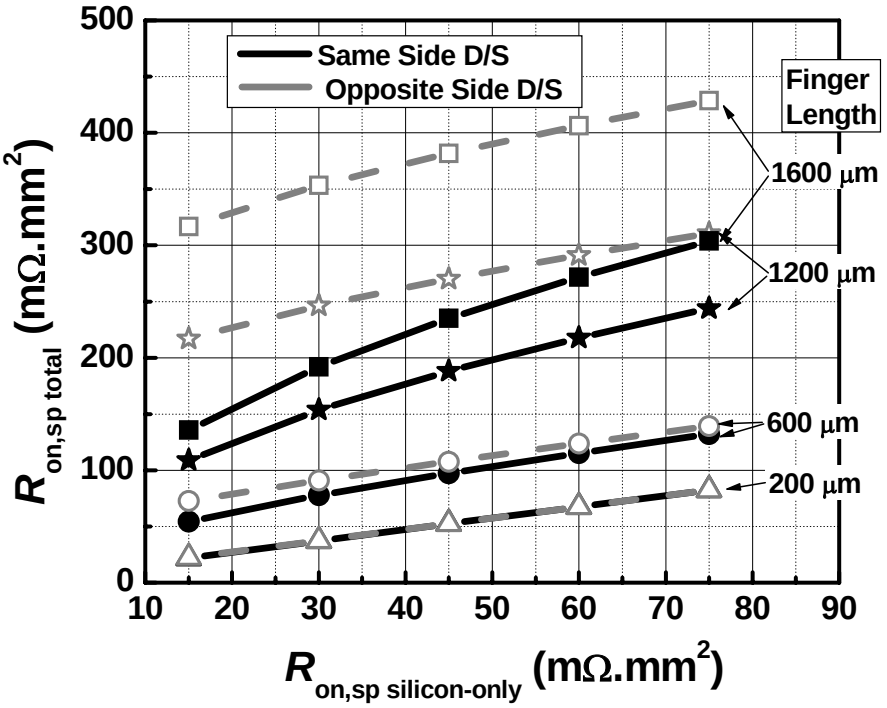


Fig. 4.18 Silicon-only Ron,sp dependence of total Ron,sp for finger length of 200 μm, 600 μm, 1200 μm and 1600 μm.

We further investigate the influence of metal interconnect resistance for different applications where the intrinsic silicon on-resistance is scaled with the requirements of breakdown voltage. Fig. 4.18 shows the total specific $R_{DS(on)}$ as a function of the intrinsic silicon specific on-resistance. It is observed that whether or not the parasitic resistance can also be reduced at a similar rate as the intrinsic silicon specific on-resistance reduced depending on the finger length. For long finger length (e.g. 1600 μm), the total $R_{DS(on)}$ decreases with decreasing intrinsic silicon on-resistance but at a slower rate. But, for short finger length (e.g. 1600 μm), the total $R_{DS(on)}$ decreases with decreasing intrinsic silicon on-resistance at a similar rate. This is due

to the increasing contribution from the parasitic metal interconnect resistance for long finger length case compared with short one. As the intrinsic silicon on-resistance is reduced, the influence of the metal interconnect becomes more and more significant especially for long finger length. For short finger length, the same side arrangement and different side arrangement show little difference for scaling rate. However, for long finger length, the same side arrangement has better performance than the different side arrangement especially for smaller intrinsic silicon on-resistance when the parasitic metal interconnect resistance become more significant.

4.7.2 Multi Metal Layer LDMOS

From the Fig. 4.15, for the single unit cell with finger length of 1000 um, the total $R_{on,sp}$ is 125 mΩ-mm^2 and 175 mΩ-mm^2 for the same side and different side arrangement, respectively. The total $R_{on,sp}$ keeps the same values for 1mm×1mm device composed of multiple unit cell. One question is how to decrease the total $R_{on,sp}$ if the intrinsic silicon-only $R_{on,sp}$ can not be reduced. Multi-layer metal interconnect provides the solution. As shown in Fig. 4.4, additional layer M1, M2 and M3 provides parallel paths for current flow so that each cell in silicon chip have access to top source and drain pad in short distance. The long metal traces in one layer configurations are broken into small piece of metal trace connected in parallel resistance network in multi-layer configurations. However, one more metal layer introduces additional metal trace resistance of itself, which will tradeoff the reduced resistance because of the parallel resistance network. The metal trace resistance is a function of metal thickness, metal trace width. Obviously, from the process point of view, lower metal sheet resistance by using thicker metal or higher conductivity material is preferred for top metal layers. But, if the process available to the design engineers can

not changed, the optimization is necessary to find the optimum metal trace width and appropriate number of metal layers.

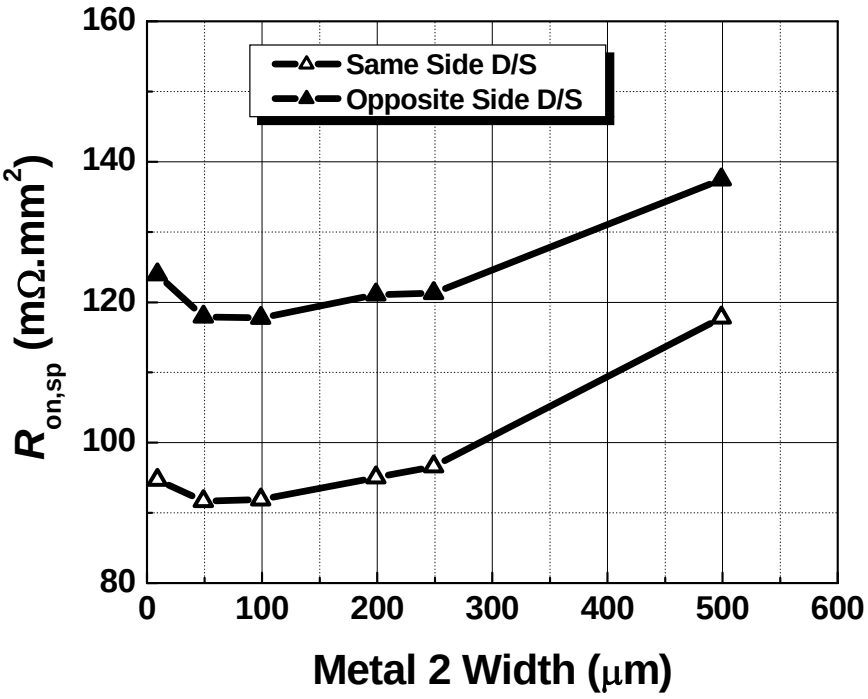


Fig. 4.19 Metal 2 width dependence of total Ron,sp for 1mm×1mm device in two metal layer configurations.

Fig. 4.19 shows Metal 2 width dependence of total $R_{on,sp}$ for 1mm×1mm device in two metal layer configurations as Fig. 4.4, where layer 1 is composed multiple unit cell with finger length of 1000 μm, layer 2 metal sheet resistance is 80 mΩ per square same as layer 1, the spacing between two metal trace is 1 μm ,and the boundaries are added at the vertical edges of metal layer 2. It is observed from Fig. 4.19, an optimum metal 2 width of ~50 μm is obtained. With the metal 2 width smaller than 50 μm, the increased metal resistance because of narrow metal trace outweighs the reduced metal resistance because of the increased parallel resistance path. On the

other hand, with the metal 2 width larger than 50 μm, the increased metal resistance because of the decreased parallel resistance path outweighs the decreased metal resistance because of wider metal trace.

Applying the same idea, the total $R_{on,sp}$ can be further reduced with three layers configurations as shown in Fig. 4.20. The layer 3 metal keeps the same sheet resistance as layer 1 an 2 and the spacing between metal trace is 1 μm.

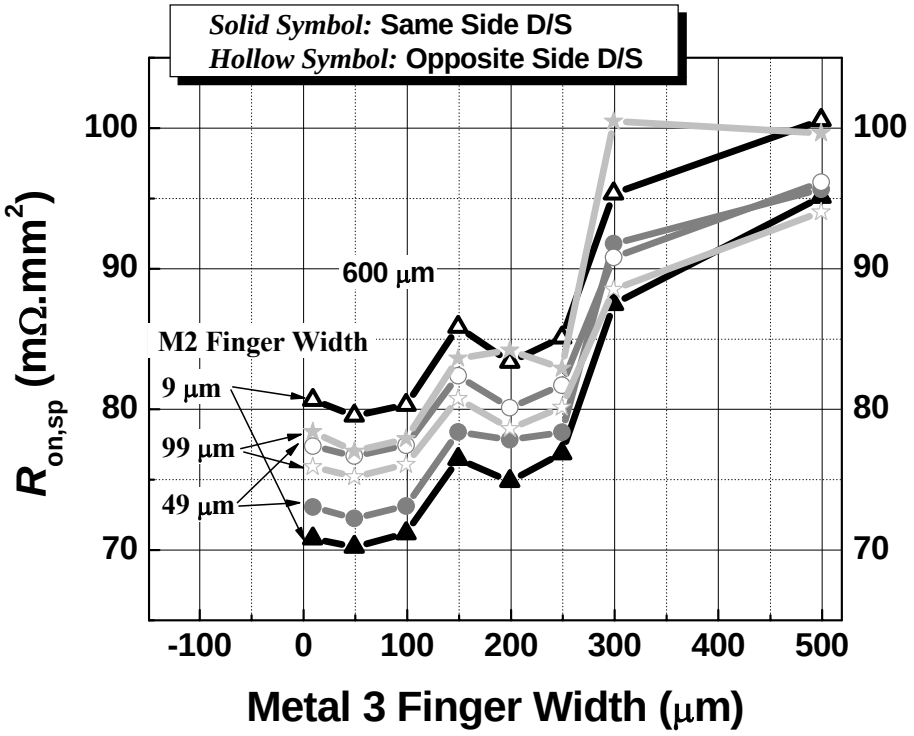


Fig. 4.20 Metal 2 and 3 width dependence of total Ron,sp for 1mm×1mm device in three metal layer configurations.

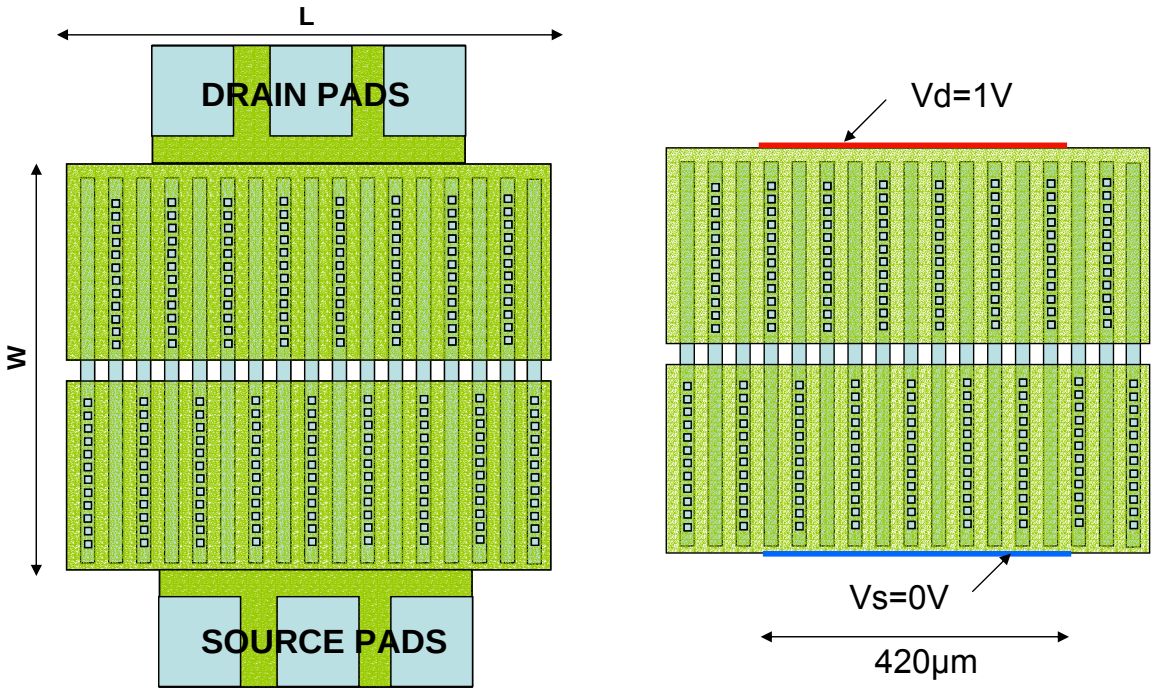
In three metal layer configurations, we have additional freedom to optimize the metal 3 width. We can find from Fig. 4.20, the metal 2 metal width and the metal 3 metal width interact with each other. The optimum metal 2 width of ~50 μm in two layer configurations is no longer

the optimum width in three layer configurations. The optimum metal 2 width and metal 3 width is 9 μm and 50 μm, respectively for the same side D/S arrangement. In contrast, the optimum metal 2 width and metal 3 width is 99 μm and 50 μm, respectively for the different side D/S arrangement. This shows the boundary conditions have strong impact on the way of the current distributes along the multi-layer resistance network, which results in different optimum finger widths.

In multi-layer structure, layout and metal interconnection variations can be numerous and layout optimization becomes more complex. The numerical tools are of significant importance to overcome this problem and improve the device performance.

4.7.3 LDMOS Metal Interconnect Optimization

In this section, we will demonstrate the effectiveness of our approach by optimizing a practical design problem. As shown in Fig. 4.21, a baseline LDMOS design with three layer metals. Layer 1 metal form S/D fingers. Layer 2 and layer 3 metal 100% overlap by via form S/D buses. The sheet resistance of metal 1, metal 2 and metal 3 are 82.5 mΩ per square, 54.0 mΩ per square, and 59.0 mΩ per square, respectively. S/D finger pitch is 4.27 μm with the metal width of 3.22 μm and space of 1.05μm. The source and drain contact pads are on the horizontal edges of S/D buses. Since layer 2 and layer 3 metal 100% overlap, this design can be treated as two layer problem. Since the drain and pad is very wide, we simplify our model as simple voltage boundary condition as shown in Fig. 4.21 (b) by neglecting the contribution of S/D pad regions. The length of boundary is fixed at 420μm for all design options.



(a) (b)

Fig. 4.21 (a) Layout of baseline design (b) simplified boundary condition model.

MOS channel is approximated by a 1μm long, 12KΩ per square, silicon sheet resistor. This 12KΩ silicon sheet resistance is from very small die measurement data, where the metal interconnect resistance can be neglected.

Table 4.1 shows the comparison between measurement data and modeling data for three device size. Our FEA modeling data closely match the measurement data on all three die sizes within 5% accuracy and provide sufficient evidence of the model validity.

Table 4.1 LDMOS baseline measurement data vs. modeling data for three device sizes.

Device Size W *L (μm^2)	Measured Rdson (mΩ)	Modeled Rdson (mΩ)	Si only Rdson from measurement (mΩ)	Modeled Si only Rdson (mΩ)
500x500	233.15	243.2	208.7	208.7
700x685	140.26	145.41	108.1	107.8
1000x1000	93.56	92.91	51.7	51.5

After verifying our modeling approach, our target is to reduce the total on resistance without modifying the device process and die size so as to keep the same manufacture cost. By varying the design layout, we can find the optimum layout pattern with smallest on resistance. Although some of the layout arrangements may not be practical in real power ICs design, the modeling results provide useful guidance in the practical design.

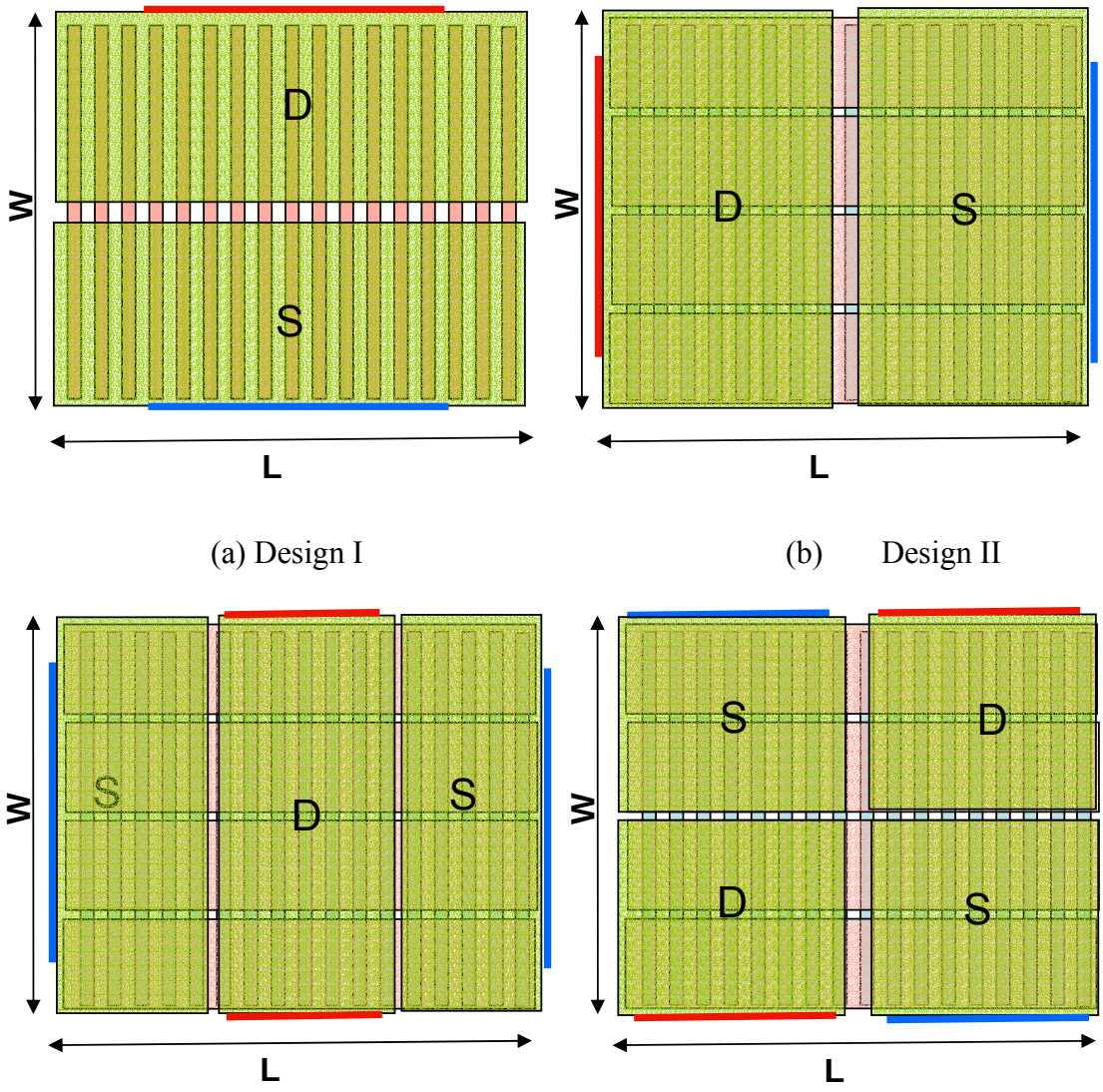
Based on our previous study, the parasitic metal interconnect resistance become more significant in large devices, so we select 1000 μm×1000 μm as baseline device size and all the process data keep the same.

One possible layout variation is to change the aspect ratio W/L of the device. As shown in Table 4.2, for the baseline design, an optimum aspect ratio W/L of 2/5 offers a 13% reduction over the 1/1 aspect ratio design. There are two metal resistance sources balancing each other. Metal resistance of S/D buses is smaller for larger W and smaller L. Metal resistance of S/D finger is smaller for smaller W. It is believed that the resistance from M1 S/D fingers and the resistance from S/D buses (M1&M2) reach a sweet spot at the aspect ratio of 2/5.

Table 4.2 Aspect ratio variation of 1mm×1mm baseline design.

W/L	Rdson (mOhm)
1:3	81.713
1:2.5	81.440
1:2	82.285
1:1	92.911
1.2:1	98.358
1.5:1	106.456

Fig. 4.22 shows other possible layout variations as (a) Design I uses metal 1 and metal 2 as S/D fingers and metal 3 as S/D buses and optimizes the aspect ratio W/L. (b) Design II uses multiple metal 2 S/D buses with a width between 9 to 499 μm, and two metal 3 S/D buses orthogonal to metal 2 buses and optimizes the aspect ratio and metal 2 bus width. (c) Design III uses multiple metal 2 S/D buses with a width between 9 to 499 μm, and three Split metal 3 S/D buses orthogonal to metal 2 buses and optimizes the aspect ratio, the metal 2 bus width , and the drain pad number (1 or 2). (d) Design IV uses multiple M2 S/D buses with a width between 9 to 499 μm, and quad split metal 3 S/D buses and optimizes the aspect ratio, the metal 2 bus width.



(a) Design I (b) Design II

(c) Design III (d) Design IV

Fig. 4.22 Four types of possible layout variations from baseline design.

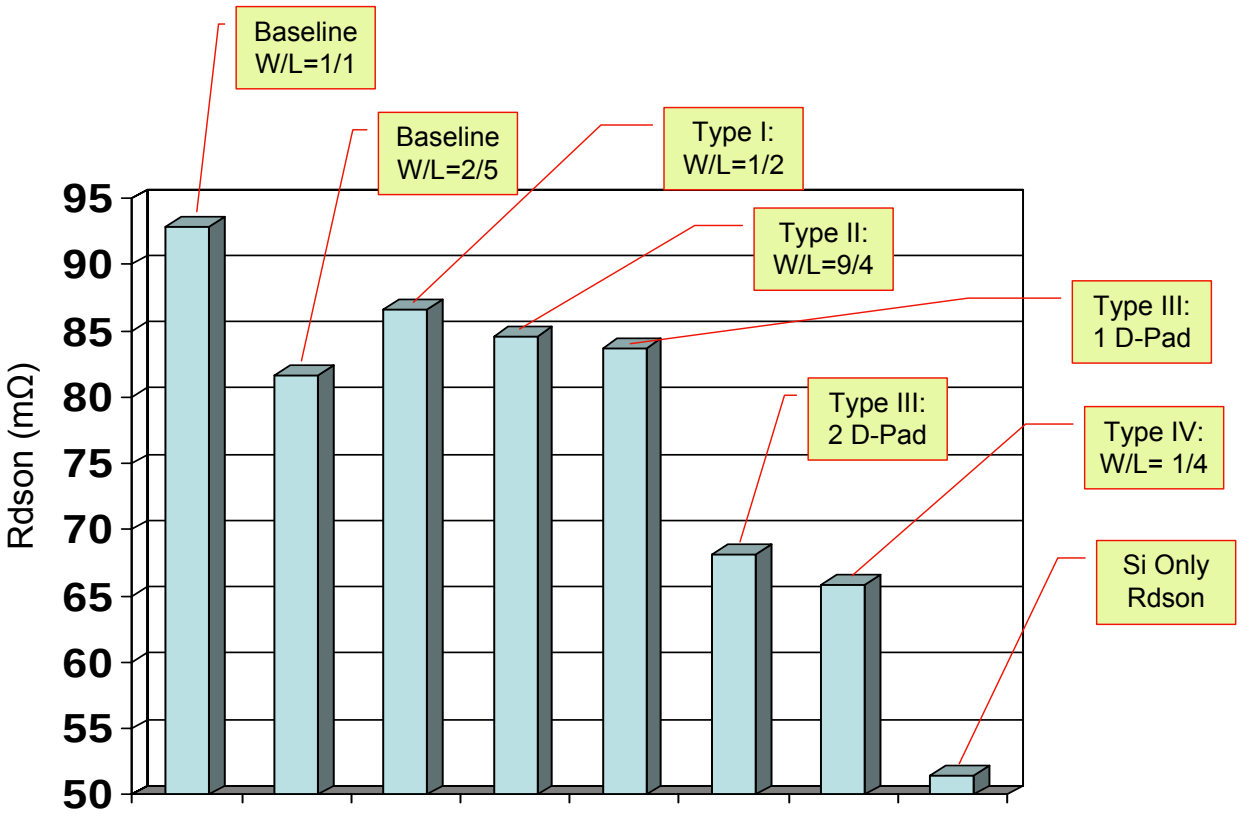


Fig. 4.23 Comparison of optimized results for each design variations with the baseline design.

Fig.4.23 gives a comparison of optimized results for each design variations with the baseline design. For baseline design, an optimum aspect ratio W/L of 2/5 offers a 13% reduction over the 1/1 aspect ratio design. Design I with an aspect ratio W/L of 1/2 shows a 7% reduction over the baseline design of 1/1 aspect ratio. Design II with an aspect ratio W/L of 9/4 and metal 2 width of 49 µm shows a 9% reduction over the baseline design of 1/1 aspect ratio. Design III offers significant improvement over the baseline design of an aspect ratio of 1/1, 10% for single drain pad with metal 2 width of 24 µm and 27% for double drain pads metal 2 width of 99 µm. Design IV with an aspect ratio W/L of 1/4 offers significant improvement of 29% over the baseline design with the baseline design of an aspect ratio of 1/1. Furthermore, in baseline W/L=1:1

design, the metal resistance contribution of the total on-resistance is about 44%. By optimizing the layout pattern, in design IV with optimized aspect ratio of W/L = 1/4, the metal resistance contribution of the total on-resistance is reduced to about 21%.

4.8 Case Study D: Sub-mΩ Flip-Chip Lateral Power MOSFET

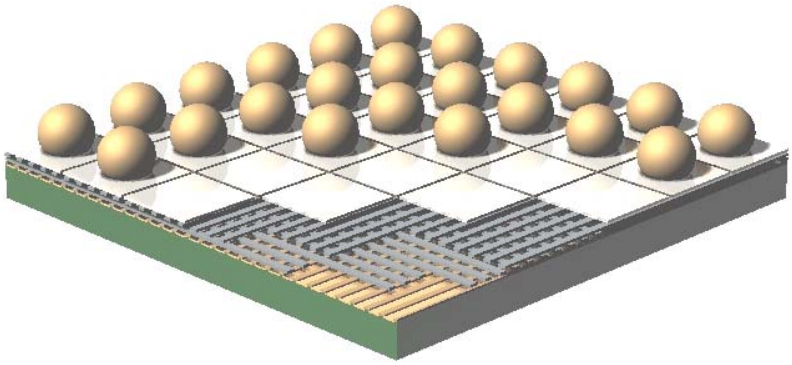


Fig. 4.24 A Sub-mΩ Flip-Chip Lateral Power MOSFET [74].

Fig. 4.24 shows a sub-mΩ flip-chip lateral power MOSFET with an innovative metal interconnect and CSP concept to overcome the lateral scaling limitation by integrating standard CMOS and wafer bumping processes [74]. A large-area lateral MOSFET of 3mm × 3mm (an LDD NMOS in this case for a targeted BV of 7 V) is formed in silicon with source, drain, and gate regions (details not shown). Multiple source and drain pads are formed in the top metal layer of a three-layer metal interconnect scheme. These source, drain, and gate pads are of approximately 500 μm × 500 μm. Single- or double-layer metal runners can be used to interconnect the source, drain, and gate regions in the silicon chip to the top metal pads, as shown in more detail in Fig.4.25. The source and drain top metal pads are arranged in a checkerboard or interleaved pattern to guarantee that any active cells in the silicon chip have

access to one or more of the source or drain pads within a short distance (less than 250 μm). Solder bumps are subsequently applied to all source/drain/gate pads using a well-established wafer bumping technique. The overlap area between the solder bump and top metal pad is about 250 × 250 μm. This is the industry's first power MOSFET below the 1-mΩ mark. This device demonstrates a record low of 1 mΩ at a gate voltage of 6 V, or 1.25 mΩ at a gate voltage of 4.5 V. This low R_{DSON} is actually measured with the MOSFET mounted on the PCB, and therefore includes all possible parasitic resistance.

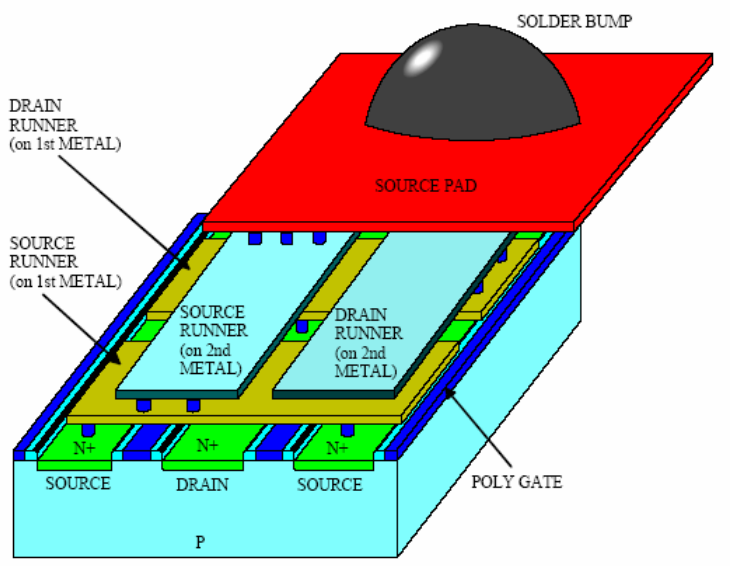


Fig. 4.25 Detailed NMOS device structure and multi-layer metal interconnect scheme to reduce parasitic resistance of lateral power MOSFETs [74].

Using the same method as in modeling bonding wires, the resistance of solder bumps, directly calculated by the resistor equation, is excluded from our model to simplify the computations. In contrast, the boundary conditions are applied on the surface area of top source and drain pads where solder bumps touch with instead of on the edge of top pads in power IC. In

addition, modeling the device size of 3mm × 3mm with fine pitch sizes is highly computationally heavy. In practical, the optimization of the algorithms is needed to improve the efficiency.

There are totally four layers in the model. The baseline layout settings of the model are: the device size is 3mm × 3mm; layer 1 metal trace width is 2 μm and gap is 0.5 μm; layer 2 metal trace width is 9 μm and gap is 1 μm; layer 3 metal trace width is 49 μm and gap is 1 μm; layer 4 metal pad width and length is 490 μm and gap is 10 μm. The silicon sheet resistance from small die measurement is 4 kOhm per square at a gate voltage of 4.5 V. Layer 1 metal sheet resistance is 4 Ohm per square. Layer 2 and 3 metal sheet resistance is 40 mOhm per square.

With the baseline settings above, applying our simulation approach, we can obtain Si only R_{DSON}= 0.556072 mΩ and the total R_{DSON}= 0.834934 mΩ. The parasitic resistance from the metal interconnect contributes about 33.4% of the total on-resistance. The total on-resistance including the solder bumps is 1.034934 mΩ. Compared with the measurement results of 1.25 mΩ, ~0.2 mΩ difference comes from the parasitic resistance of the PCB board.

Based on the baseline design, our next target is to reduce the total on-resistance without modifying the device process and die size so as to keep the same manufacture cost. By varying the design layout, we can find the optimum layout pattern with smallest on resistance. Fig.4.26 shows Metal 2 width dependence of total R_{dson} with Metal 3 width of 49 μm. It is observed from Fig. 4.26, a metal 2 width of 9 μm is a relatively optimum point and the metal 2 width has strong impact on the total on-resistance. Similarly, metal 3 width dependence of total R_{dson} with Metal 2 width of 9 μm is shown in Fig. 4.27. In contrast with the effect of metal 2 width, the metal 3 width has weak impact on the total on-resistance. As a result, the layout patterns of the baseline design is relatively optimum in term of metal 2 width and metal 3 width for the current process parameters. Another approach to reduce the total on-resistance is to increase the overlapped area

between solder bumps and top metal pads, which is equal to increasing the area of voltage boundary. Assume an ideal case that the solder bumps and top metal pads are 100% overlapping, the total on-resistance with the new boundary conditions is 0.684007 mΩ. The parasitic resistance from the metal interconnect contributes about 18.7% of the total on-resistance compared with 33.4% in the baseline design. But this approach is limited by the practical solder bump design rules because the solder bumps can not be too closed to each other.

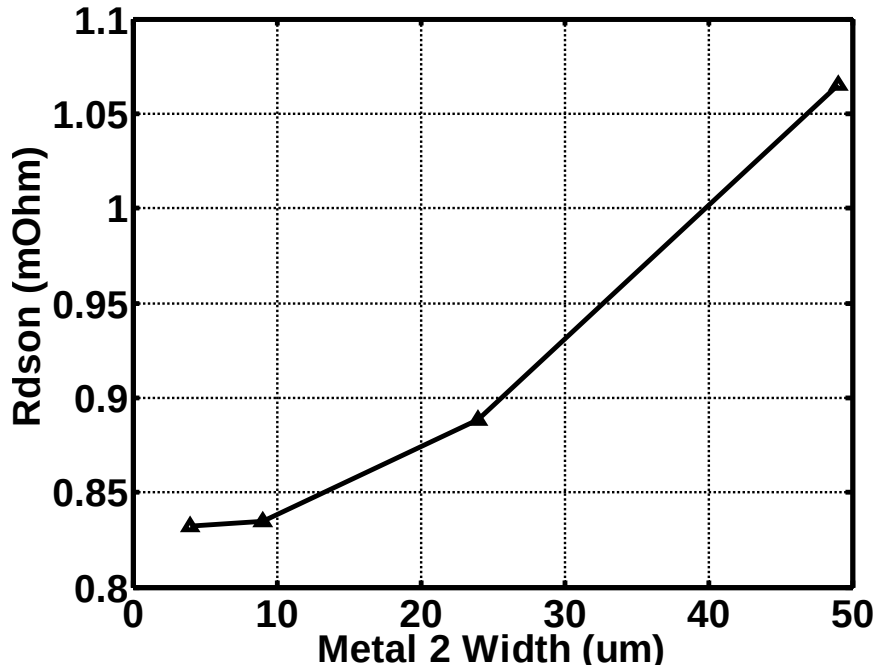


Fig. 4.26 Metal 2 width dependence of total Rdson with Metal 3 width of 49 μm of flip chip lateral power MOSFET.

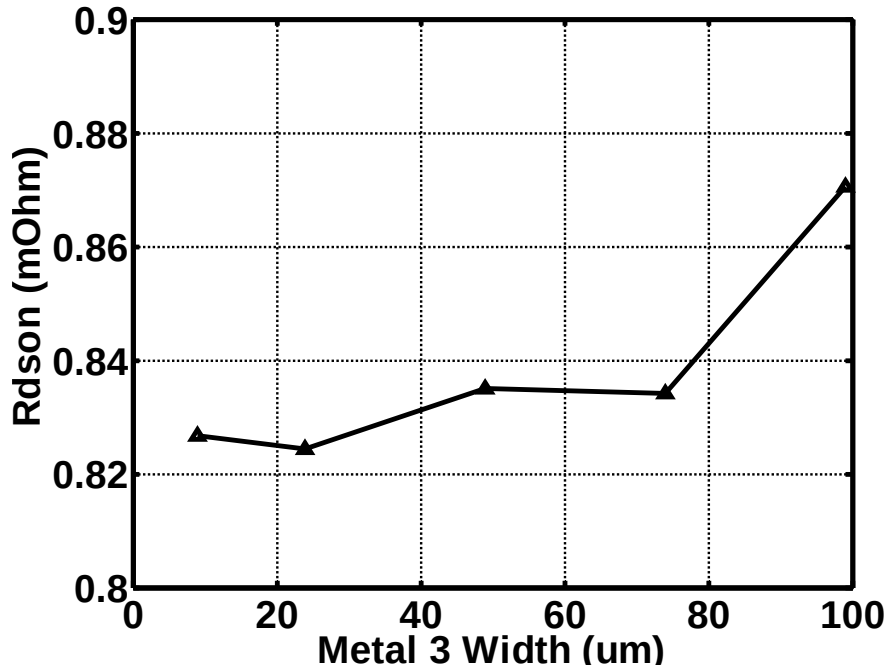


Fig. 4.27 Metal 3 width dependence of total Rdson with Metal 2 width of 9 μm of flip chip lateral power MOSFET.

If the process technology as the sheet resistance of metal interconnects and Si channel can be improved, the total on-resistance can be further reduced. The metal 2(3) sheet resistance dependence of the total on-resistance is shown in Fig. 4.28. It is observed that the total on-resistance is reduced with a decreased of metal 2(3) sheet resistance, but at a faster rate. This trend is common to various widths of metal 2. This is due to the decreasing contribution from the parasitic metal interconnect resistance for low metal 2(3) sheet resistance compared with high one. The metal 1 sheet resistance dependence of the total on-resistance is shown in Fig. 4.29. As we can expect, the total on-resistance is reduced with a decreased metal 1 sheet resistance. However, the decreasing rate is highly dependent on the width of metal 2. For the narrow width of metal 2 as 4 μm and 9 μm, the decreasing rate is very small and the total on-resistance is not

sensitive to the variation of the sheet resistance of metal 1. In contrast, for the wide width of metal 2 as 24 μm and 49 μm, the total on-resistance is very sensitive to the variation of the sheet resistance of metal 1 and the decreasing rate is larger for a wider width of metal 2. This result provides a very useful guideline for the practical design that reducing the sheet resistance of M1 will not be an effective way to improve the performance of the baseline design. Another approach to reduce the total on-resistance is to decrease the silicon sheet resistance as shown in Fig. 4.30. Similar to the results we have for the lateral power MOSFETs, the total on-resistance is reduced with a smaller silicon sheet resistance, but at a slower rate due to the increasing contribution of the metal interconnects. In the practical power MOSFET design, the scaling of the silicon sheet resistance should trade-off with the scaling of the breakdown voltage.

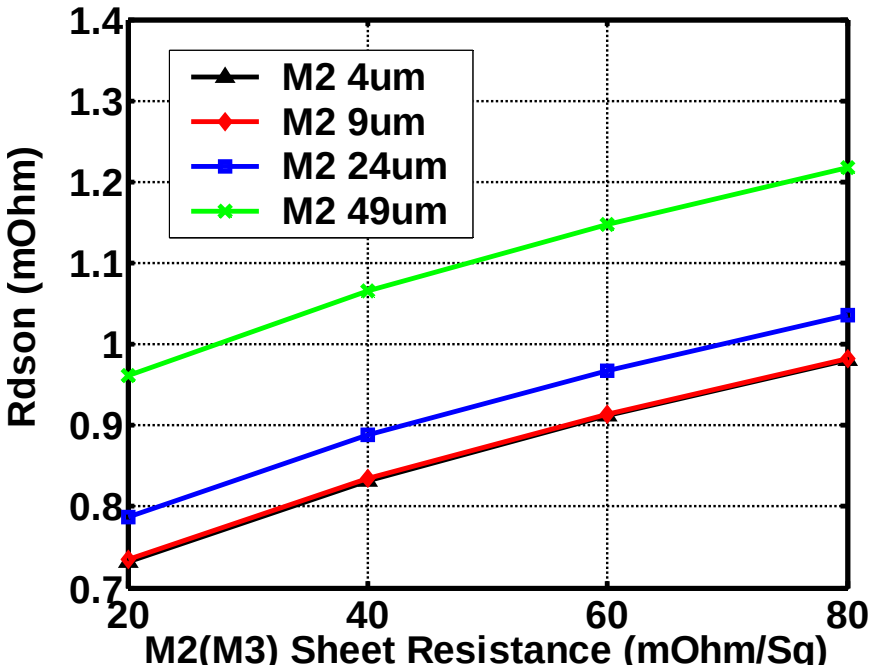


Fig. 4.28 Metal 2(3) sheet resistance dependence of total Rdson of flip chip lateral power MOSFET.

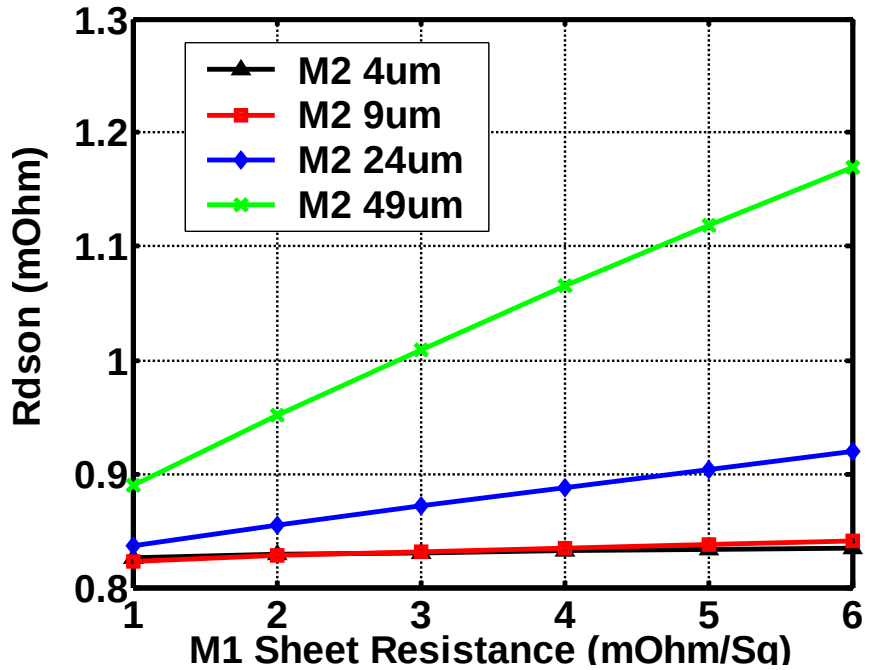


Fig. 4.29 Metal 1 sheet resistance dependence of total Rdson of flip chip lateral power MOSFET.

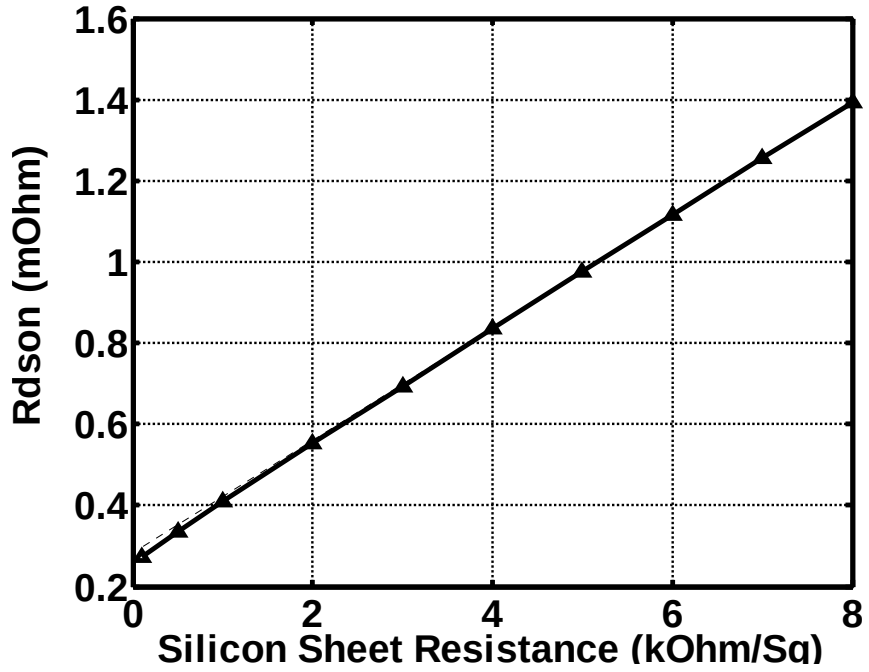


Fig. 4.30 Silicon sheet resistance dependence of total Rdson of flip chip lateral power baseline MOSFET.

CHAPTER FIVE: CONCLUSIONS

Our research has demonstrated the numerical modeling approach of three different types of advanced electronic devices with the finite element method. From our simulation results and discussions, it has shown the effectiveness and versatility of this approach in broad applications including the optimization of performance in the existing device structures and the development of novel device structures to break though the ultimate physical scaling limits of traditional devices. This chapter summarizes the contributions of the research.

In Chapter 2, radiation mechanism and geometry dependent properties are studied for electron waveguides with multi-step discontinuities and soft wall lateral confinement based on the finite element method (FEM) and rigorous mode-matching method [81]. This systematic study of radiation properties will deepen our understandings of radiation mechanism and conditions in electron waveguides. The study of the geometry variations shows its significant impact on the radiation intensity and direction. It will provide us guidance on how to minimize the radiations in some waveguide structures where the discontinuities are induced by the manufacture process. Also, the presented strong directional radiation in the periodic corrugation structure will propose a new idea to design "leaky electron antenna", a novel electron waveguide device for future nanoelectronics. Possible extension of the presented work is to study the non-thermal equilibrium conditions [82, 83], which provides us with new degrees of freedom to control the radiation properties of the devices compared with quasi-thermal equilibrium.

In Chapter 3, we present a new approach solving a full time-dependent, open-boundary Schrödinger equation self-consistently to study the high frequency response in CNTFETs [84]. We extend the FDTD-Q method for the treatment of the open boundary condition with FEM.

The equations of normalized time-dependent current and charge densities are derived from time-dependent wave function, which is solved from the effective mass based time-dependent Schrödinger equation. Non quasi-static effects in ballistic CNTFETs, which play an important role on the characteristics of conventional high-speed transistors, are investigated for the first time in carbon nanotube transistors. The results show that the intrinsic gate capacitance and transconductance significantly decreases as the frequency increases to a value comparable to the intrinsic cut-off frequency. The channel charging time is limited by the band-structure-limited velocity. The quasi-static approximation gives a much more accurate value for the intrinsic cut-off frequency over a wide range of bias conditions than for the gate capacitance and transconductance. Possible extension of the presented work is to adopt the atomistic description of the energy band structure [85] in CNTFETs instead of the effective mass description currently used. Compared with the effective mass approach, the atomistic approach gives a more accurate description of electron confinement in the circumferential direction, but results in more computational complexity.

In Chapter 4, the finite element analysis approach has shown the strong flexibility in the modeling of the arbitrary geometry, which enables us for the first time to quantitatively and systematically evaluate the metal interconnection effect on the on-resistance of vertical and lateral power MOSFETs. Through the investigation of different layouts of metal interconnection and material parameters, we have successfully improved the metal interconnection designs of commercial products. The impact of various layout patterns and material properties on $R_{DS(on)}$ will provide useful guidelines for practical vertical and lateral power MOSFETs design. The "debiasing" effect in active device cells caused by interconnect resistance is examined for lateral power MOSFETs. The "debiasing effect" due to the reduction of the effective V_{GS} is

insignificant comparing to other effects of the metal interconnect. The misconceptions in the previous literature regarding the effect of metal interconnect resistance overestimate this effect. Possible extension of the presented work is to include automatic optimization algorithms to find the optimum structure with lowest $R_{DS(on)}$ by the program itself, which can improve the efficiency of the work greatly and maximize the output of the design process.

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