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Study of Novel Power Semiconductor Devices for Performance and Reliability.

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STUDY OF NOVEL POWER SEMICONDUCTOR DEVICES FOR PERFORMANCE AND RELIABILITY

by

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ABSTRACT

Power Semiconductor Devices are crucial components in present day power electronic systems. The performance and efficiency of the devices have a direct correlation with the power system efficiency. This dissertation will examine some of the components that are commonly used in a power system, with emphasis on their performance characteristics and reliability.

In recent times, there has a proliferation of charge balance devices in high voltage discrete power devices. We examine the same charge balance concept in a fast recovery diode and a MOSFET. This is crucial in the extending system performance at compact dimensions. At smaller device and system sizes, the performance trade-off between the ON and OFF states becomes all the more critical. The focus on reducing the switching losses while maintaining system reliability increases. In a conventional planar technology, the technology places a limit on the switching performance owing to the larger die sizes. Using a charge balance structure helps achieve the improved trade-off, while working towards ultimately improving system reliability, size and cost.

Chapter 1 introduces the basic power system based on an inductive switching circuit, and the various components that determine its efficiency. Chapter 2 presents a novel Trench Fast Recovery Diode (FRD) structure with injection control is proposed in this dissertation. The proposed structure achieves improved carrier profile without the need for excess lifetime control. This substantially improves the device performance, especially at extreme temperatures (-40^{o}C to 175^{o}C). The device maintains low leakage at high temperatures, and it's Qrr and Irm do not

degrade as is the usual case in heavily electron radiated devices. A 1600 diode using this structure has been developed, with a low forward turn-on voltage and good reverse recovery properties. The experimental results show that the structure maintains its performance at high temperatures.

In chapter 3, we develop a termination scheme for the previously mentioned diode. A major limitation on the performance of high voltage power semiconductor is the edge termination of the device. It is critical to maintain the breakdown voltage of the device without compromising the reliability of the device by controlling the surface electric field. A good termination structure is critical to the reliability of the power semiconductor device. The proposed termination uses a novel trench MOS with buried guard ring structure to completely eliminate high surface electric field in the silicon region of the termination. The termination scheme was applied towards a 1350 V fast recovery diode, and showed excellent results. It achieved 98% of parallel plane breakdown voltage, with low leakage and no shifts after High Temperature Reverse Bias testing due to mobile ion contamination from packaging mold compound.

In chapter 4, we also investigate the device physics behind a superjunction MOSFET structure for improved robustness. The biggest issue with a completely charge balanced MOSFET is decreased robustness in an Unclamped Inductive Switching (UIS) Circuit. The equally charged P and N pillars result in a flat electric field profile, with the peak carrier density closer to the P-N junction at the surface. This results in an almost negligible positive dynamic Rds-on effect in the MOSFET. By changing the charge profile of the P-column, either by increasing it completely or

by implementing a graded profile with the heavier P on top, we can change the field profile and shift the carrier density deeper into silicon, increasing the positive dynamic Rds-on effect. Simulation and experimental results are presented to support the theory and understanding.

Chapter 5 summarizes all the theories presented and the contributions made by them in the field. It also seeks to highlight future work to be done in these areas.

To my parents T.V. and Jaya Padmanabhan

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Last but not the least, they say family plays a huge role in everything you accomplish, and my case is no different. I would like to especially like to thank my parents and my sister, Vidhya, for supporting me and putting up with me while I finished my PhD. Apart from my own family, the role played by my uncle N.C.Murthy in constantly pushing me to complete my PhD is both invaluable and vital in me doing so. Beyond them, all assistance from my friends and extended family for this task is most appreciated.

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BGR	Buried Guard Ring
BI	Burn In
BJT	Bipolar Junction Transistor
BV	Breakdown Voltage
DUT	Device Under Test
ER	Electron Radiation
FLR	Field Limiting Ring
FP	Field Plate
FRD	Fast Recovery Diode
GR	Guard Ring
IGBT	Insulated Gate Bipolar Transistor
JTE	Junction Termination Extension
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
QRR	Reverse Recovery Charge
RDYN	Dynamic Resistance
SJ	Super-Junction
UIS	Unclamped Inductive Switching
VF	Forward Voltage

CHAPTER 1
INTRODUCTION

Inductive Switching Circuit

Power electronic systems, especially at high power levels, place a premium on system efficiency. Even a marginal shift in efficiency can greatly impact the system performance. It is for this reason that the power semiconductor devices which are commonly used in these systems are constantly upgraded in technology for better performance characteristics.

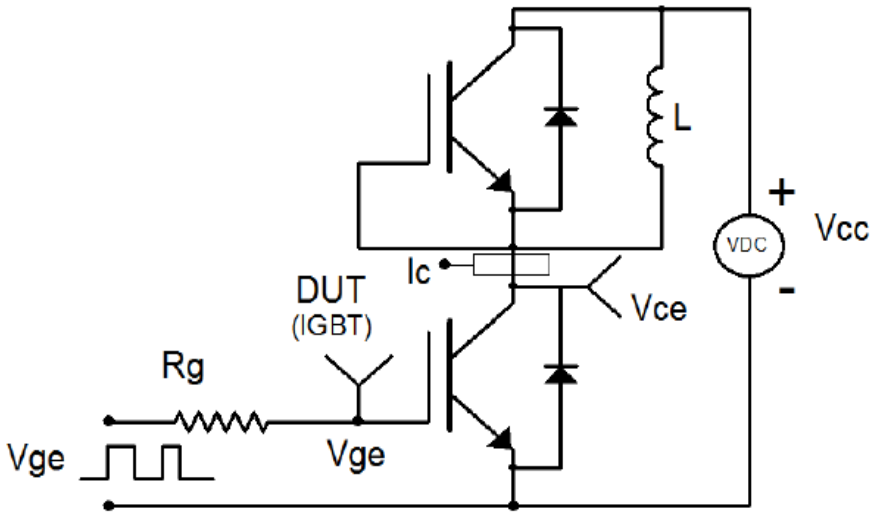


Figure 1.1. A Conventional Inductive Switching Circuit.

Figure 1.1 shows the commonly used switching circuit for most power systems, which happens to be the inductive switching circuit. The circuit is part of a half-bridge configuration, with a low side and high side switch, where they alternate between conducting and blocking mode. The semiconductor switches used in this circuit are conventionally either MOSFETs or IGBTs. Primarily, the circuit requires the high side device to have a free-wheeling diode.

When the low side FET is operational, the high side diode is in blocking mode. When the low side FET is turned off, the current through the inductor needs to cycle through the diode, thus putting the diode into conducting mode. While the MOSFET has an anti-parallel diode built into the structure, the presence of the P type drain in the IGBT prevents the IGBT from having the same. This necessitates the addition of a diode along with the IGBT when used in this configuration. This is also beneficial form a design stand-point because it allows the designed to individually optimize the diode performance to increase the overall system efficiency.

The Vf of the diode is crucial in determining the conduction losses, while Qrr is essential in determining the Eon of the low-side FET. This is illustrated in Figure. 1.2.

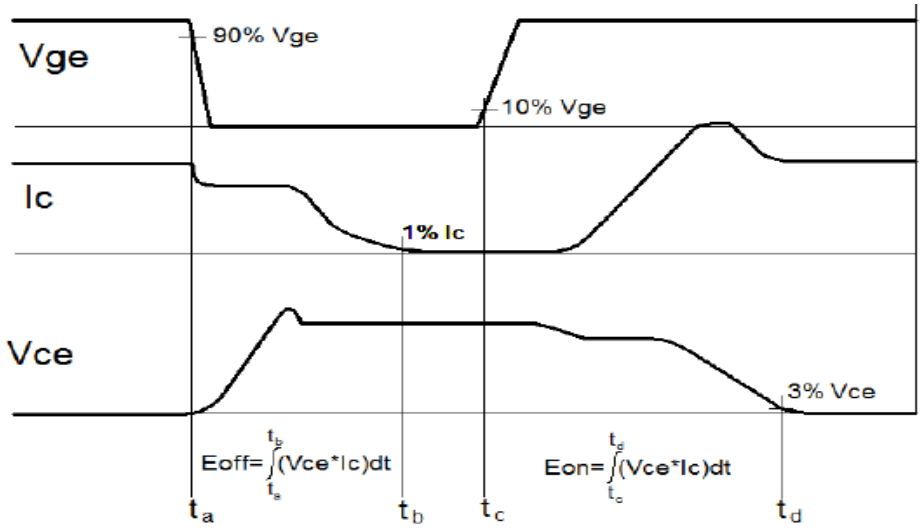


Figure 1.2. Switching waveforms in an Inductive Switching Circuit.

As seen in Figure 1.2, the reverse recovery current from the diode flows through the low-side IGBT. The voltage curve is controlled by the capacitance of the IGBT, but the amount of current

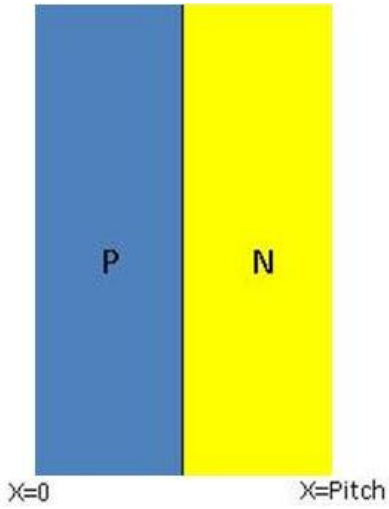
overshoot in the IGBT is determined by the diode. A smaller diode Qrr reflects in a lower Eon for the IGBT, thereby improving the overall system efficiency. A higher Qrr has the inverse effect.

Charge Balanced Devices

As mentioned earlier, the individual characteristics of the devices used play a huge role in determining the overall efficiency of the circuit. For this reason, there has been an increased shift towards using superjunction or charge balanced devices.

The concept of a charge balance is one that has been explored previously in [1]. The basic principle is to use alternating highly doped P and N columns to essentially generate a net intrinsic epi of negligible doping concentration. This way, the device can still support the requisite breakdown voltage, but due to the significantly higher N column doping concentration, can achieve significantly better performance specifications in most aspects.

The breakdown voltage is determined by the charge, depth of the drift region and the pitch of the alternating P and N columns. The basic structure is most commonly applied to MOSFETs, wherein they have the most benefit with regards to a BV-Rds-on trade-off, due to the increased N column doping concentration. The basic superjunction structure is as shown in Figure 1.3, along with the corresponding equation governing the charge distribution.



$$\text{Net } Q(y) = \int_{X=0}^{X=Pitch} (N_D^+ - N_A^- + p - n)\, dx$$

Figure 1.3. A conventional charge balance structure and the accompanying equation governing the net charge.

This concept can technically be extended to IGBT and FRD, but has a few issues which is outside the scope of this dissertation. The primary issue with using a superjunction structure in a diode is that increased P column doping would result in significantly higher carrier injection. This increased carrier injection leads to a low diode forward voltage (Vf), but a severely degraded reverse recovery charge (Qrr).

We can still, however, apply the concept with a Trench MOS structure forming a partial charge balanced structure for the diode. The P column is replaced by a trench filled with heavily doped polysilicon and a thick liner oxide, with the polysilicon being connected to the ground. The

potential lines are supported by the liner oxide. This structure forms the basis for the diode and the termination scheme implemented for it. The basic cell structure is shown in Figure 1.4.

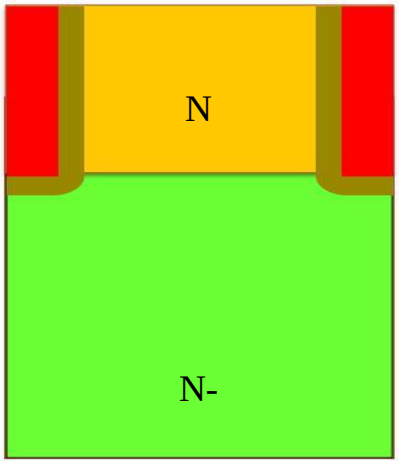


Figure 1.4. A partial superjunction epi with a Trench MOS structure on top.

This structure is also called the Trench MOS structure. The main idea being implementing a partial charge balance concept to the diode is to have the N region act as an injection control layer in the diode. This injection control is important because it helps achieve a better Vf-Qrr trade-off.

High Voltage Edge Termination

Since the diode makes use of the trench charge balance structure, the termination scheme follows suit. In a conventional vertical DMOS structure, the active area is biased at ground voltage, while the edge of die at the bus voltage. The purpose of an edge termination in a die is to help transition the voltage from the edge of the active area to the edge of the die, as shown in Figure 1.5.

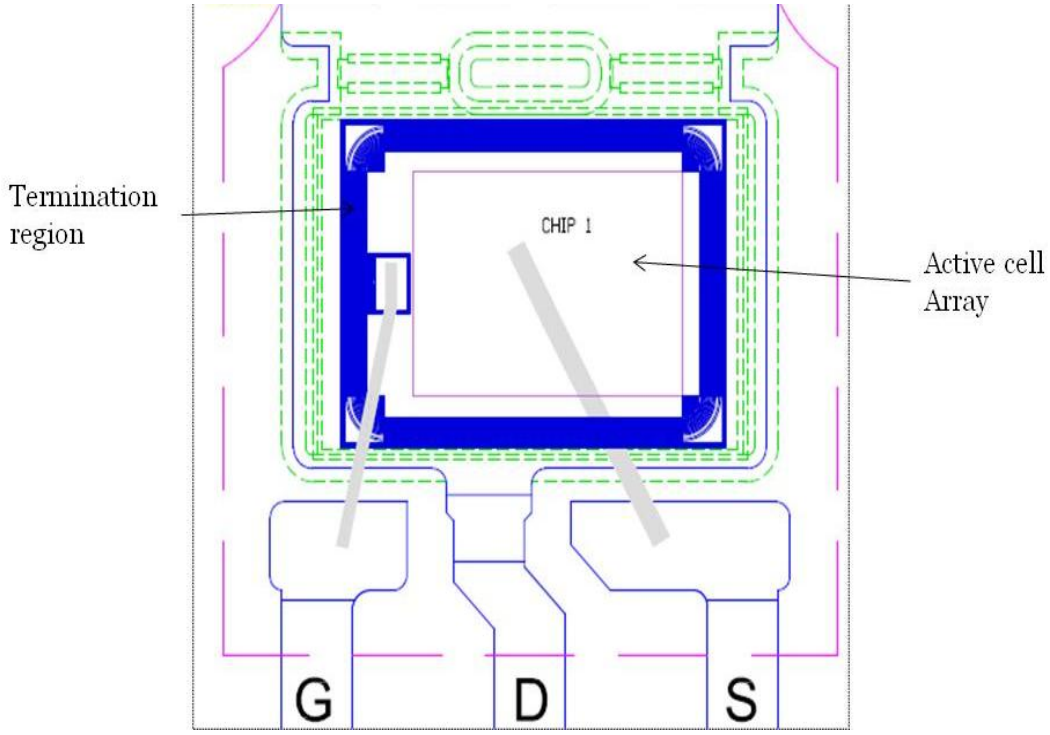


Figure 1.5. Die layout in a package.

The high N concentration at the surface makes it difficult to implement a regular planar termination as mentioned above. For a conventional planar MOSFET, a simple structure like a guard ring termination is efficient. It alters the potential lines and terminates them at the surface. Given a peak silicon E-field on 3e5V/cm, the guard ring spacing can be adjusted to support the required BV. But in the proposed structure, as we showed earlier, this is more complicated. The high surface N charge makes it more difficult to implement a conventional edge termination where the field terminated in silicon because the electric field increases exponentially at the P-N junction. Also, a higher N charge can also punch-through the surface P concentration if the dose it low. While a higher P implant can prevent punch-through, it still cannot eliminate the higher electric field at the junction, and the field limitation of 3e5V/cm makes that more difficult.

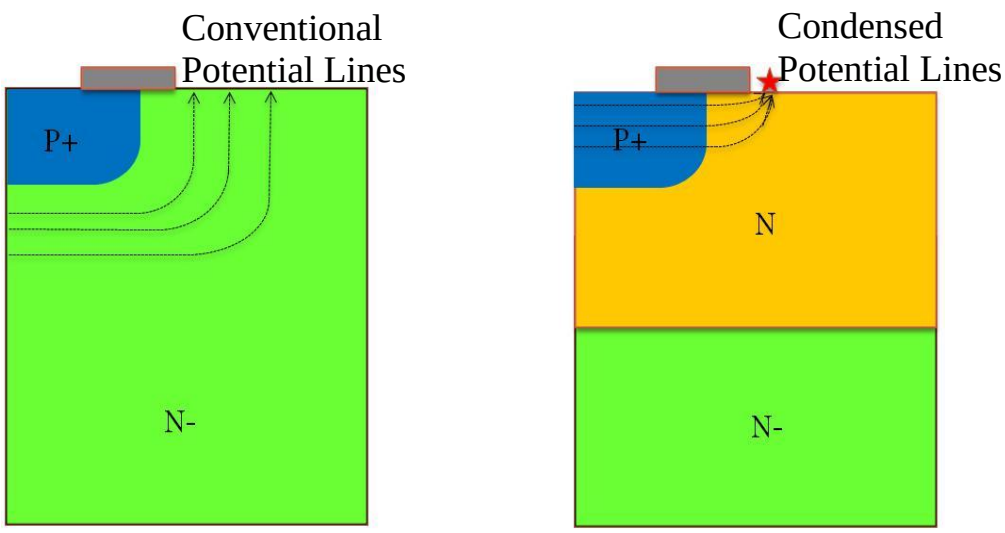


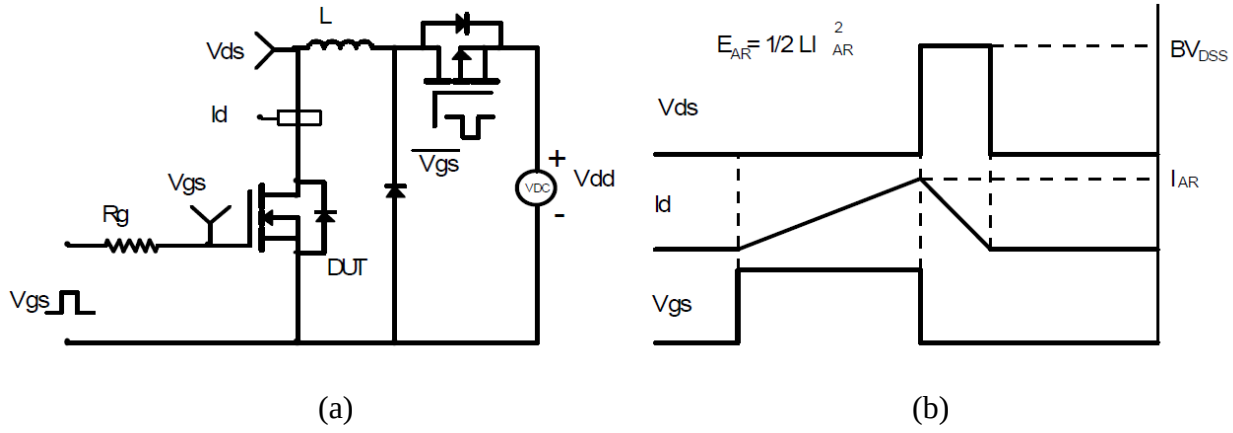
Figure 1.6. Effect of highly doped topside N region on the potential lines around a surface field guard ring.

Most common terminations that involve the potential lines terminating in the surface are therefore hampered by the presence of the high surface N concentration and that electric field limit of Silicon. So, it is necessary to implement a novel termination scheme for the structure under consideration. As a result, a novel termination scheme for the same is studied and its enhanced reliability compared to a regular planar termination structure.

Superjunction Ruggedness

If the device used in the low side is a MOSFET, then the ruggedness of the device becomes critical. The measure of a MOSFET's ruggedness is made typically through its performance in an unclamped inductive switching circuit. In an unclamped inductive switching (UIS) circuit, the inductor is quickly turned off, and the resulting magnetic field causes the switch to sustain high

voltages. In the case of a MOSFET, this voltage buildup, coupled with the increased current flow, results in power dissipation which exceeds the rated value of the MOSFET. A commonly used circuit is shown in Figure 1.7.



(a) (b)

Figure 1.7. (a) A UIS circuit and (b) the accompanying current and voltage waveforms seen in the DUT (MOSFET).

In the UIS test, the MOSFET can undergo two modes of failure, active and passive. While the active mode is caused by the latchup of the bipolar junction transistor (BJT) in the MOSFET, the passive mode is caused by external factors when the chip temperature reaches a very high value, causing thermal runaway. For the purposes of this dissertation, we focus exclusively on the active failure mode which is caused by the avalanche currents from the bipolar latchup.

During the UIS mode, the current flowing through the parasitic resistance from the p region causes a voltage drop from the conduction current, thus activating the parasitic BJT. If the P-base dose is low, then the effective dopant resistance is high, which in this case happens to be the base resistance of the BJT. As the current through the MOSFET increases during the UIS avalanche

period, the voltage drop across the parasitic base resistance triggers the parasitic BJT. Once the parasitic BJT is triggered, the BJT is on a self-sustaining mode wherein it results in a thermal runaway of the MOSFET, eventually causing MOSFET failure.

The maximum current allowed by the MOSFET before failure is dependent on the size of the inductor used in the circuit. So, based on the inductor used in the circuit, we can characterize both the maximum voltage seen by the MOSFET and the maximum energy dissipation in the MOSFET (Eas). The equations for the same are as given by the following:

$$\mathbf{V=L(di/dt)+V_{DD}}$$

$$\mathbf{Eas=(1/2)*L*I^2}$$

MOSFETs are generally characterized by the maximum energy dissipation in the UIS mode as a reflection of their ruggedness.

The peak energy dissipation occurs at time t=0, when the MOSFET experiences peak current and voltage levels. This peak energy point can be captured in the avalanche snapback curves of a MOSFET. The avalanche snapback property in a MOSFET has a similar trigger mechanism as the UIS failure, i.e. turn-on of the parasitic BJT.

If the MOSFET in question happens to be a superjunction MOSFET, then the robustness of the device becomes even more critical. While a fully charge balanced, superjunction MOSFET

offers many advantages, it does show degradation in a couple of areas, specifically the diode reverse recovery characteristics and its ruggedness. While the diode characteristics can be somewhat controlled through some sort of lifetime control, a pure SJ device has inherently weak ruggedness due its structure.

In the superjunction MOSFET, the superior Rdson of a unit cell due to higher N column doping concentration results in a lower effective Rds*A figure of merit. So, for the same Rds-on, the superjunction MOSFET has a smaller chip size compared to a planar MOSFET. A smaller chip area results in a lower energy handling capability. Another detail to consider is that the increased doping concentration of the N column leads to a much higher carrier density at the surface. The increased carrier density leads to a higher current when the device avalanches during the UIS test, leading to a larger IR drop across the parasitic resistor triggering the intrinsic bipolar transistor.

While the UIS test is one common way to test the ruggedness of the MOSFET, another approach for verifying the same is the BV avalanche test. If current is continually pushed through the MOSFET even after it enters the avalanche mode, the avalanche current will eventually trigger the bipolar BJT. This can however be influenced by the column charge. By introducing a charge imbalance in the SJ structure, we can alter the electric field and the carrier density profile to alter the avalanche breakdown property of the MOSFET.

CHAPTER 2
FAST RECOVERY DIDOE

Introduction

While the previously mentioned inductive switching circuit is the common topology, it is usually component of the half-bridge rectifier. Half-bridge rectifiers usually form the back-bone of modern power electronic systems. In most of these applications, the circuit is hard-switched, where the forced commutation of the diode is crucial in determining the switching losses.

The rectifier usually has two semiconductor switches which conduct alternately. The previously mentioned inductive switching circuit is predominantly controlled by the switches used in the circuit. The device used and the corresponding topology greatly determines the efficiency of the system. The low and high side switches are most commonly implemented in one of two ways.

- **MOSFET**: This is usually the case if the low side device is a MOSFET too. In this case, the anti-parallel diode of the MOSFET is the diode on the high side. The MOSFET is gradually being replaced by the IGBTs at the higher voltage ranges (>600V).

- **IGBT + Fast Recovery Diode**: This is usually the solution if the low side device is an IGBT. Since IGBTs structurally do not have an internal body diode, they are usually co-packaged with an external diode to allow for current conduction when the low side is switched off. The exception in this case is when an RC-IGBT, but there is a severe drop-off in the diode performance in this instance, as explained in detail later. This solution usually applies to applications with voltage ranges >600V.

The reason why IGBTs are the preferred choice for higher voltage ranges is because of the advantageous operating principle. Due to the fact that the IGBT is a bipolar device compared to the unipolar nature of the MOSFET, the conduction energy of the IGBT at higher operating voltages is lower. Beyond an operating voltage of typically 600V, the Vce(sat) of the IGBT has a better performance trade-off compared to the Rds-on of a comparable MOSFET.

The issue with using an IGBT however is the lack of an anti-parallel diode. In a MOSFET, the P+ source and the N+ drain inherently form a diode. The diode is basic and will have high injection and consequently a large Qrr. While this is a by-product of the MOSFET structure, the IGBT unfortunately does not have the same advantage due to the P+ drain in the structure. This creates a problem when the IGBT replaces the MOSFET in a switching circuit for the higher voltage applications. To address this, the IGBT is usually co-packaged with a standalone fast recovery diode (FRD), which forms the basis of this chapter.

In case of the MOSFET, as mentioned earlier, the injection characteristics are difficult to modify since they are set based on the MOSFET design. In case of the IGBT, since the diode characteristics can now be de-coupled from the main switching device, the diode can be engineered individually for much better switching characteristics and increased efficiency. A diode's performance is ideally characterized by the Vf-Qrr trade-off. A lower Vf leads to a higher Qrr, and vice-versa. This can best be explained using the Vf-Qrr curve.

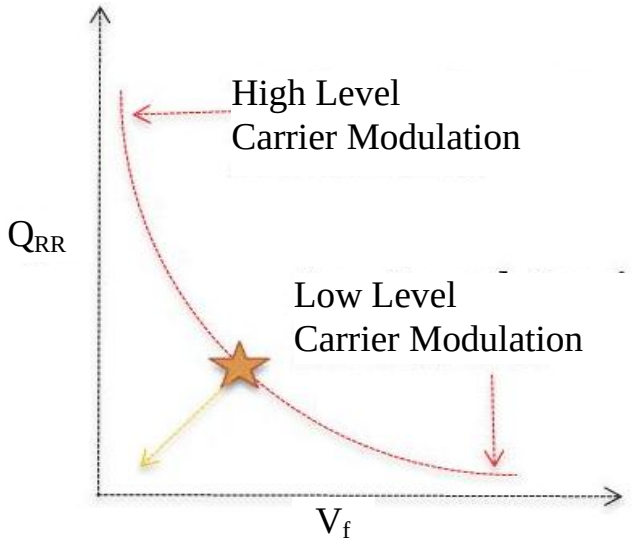


Figure 2.1. Performance Curve illustrating the Vf-Qrr trade-off.

For ideal diode characteristics, we would like to have minimum V_f to go with minimum Q_{rr}. The V_f of the diode comes into play during the conduction mode of the diode, while the Q_{rr} is essential during the switching mode. Both these characteristics are controlled by the amount of carrier injection in the diode, both from the cathode and anode, due to the FRD being bipolar in nature.

There is a way to introduce diode characteristics in an IGBT. This structure is commonly known as the Reverse Conducting IGBT (RC-IGBT) [2]. In an RC-IGBT, there is an anode short on the cathode side wherein some of the P+ region is killed in favour of an N+ contact. This once again introduces the anti-parallel diode structure into the IGBT. The basic structure of an RC-IGBT as shown in Figure 2.2 [2].

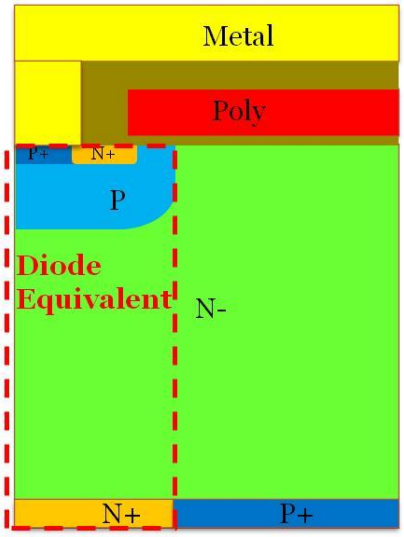


Figure 2.2. RC-IGBT Structure.

The RC-IGBT has its share of advantages and disadvantages. On the plus side, the RC-IGBT is more compact than an IGBT+FRD combinations, and consequently more economical and cost effective. It however has limitations. As seen with the MOSFET, the injection is largely dictated by the IGBT design criteria, so optimizing the diode performance in the structure has limitations with regards to the IGBT parameters. When designing the anode short, the ratio of N+/P+ contact directly impacts both the IGBT and FRD characteristics. Also, if the N+ contact dose is insufficient or is not sufficiently activated, it adversely affects the Vf of the device. For industrial motor drives which require optimum Vf and Qrr, targeting the ideal Vf-Qrr trade-off point becomes difficult.

It is for this reason that a standalone FRD is preferred for applications where the efficiency is paramount. The diode specifically comes into play when the low side IGBT is turned off. At this point, the current path needs to be maintained. So, the current cycles through the diode. When

the low side IGBT is turned on again, the diode needs to turn off as soon as possible so that the current can flow through the IGBT again.

The switching losses in the circuit are calculated when the devices transition between states. The high side current which commutes through the diode now flows through the low side device when it turns on. Since the diode is bipolar, the switching mechanism inside the diode is a function of how the P-N junctions are designed. The commonly used application circuit which forms the basis for the half bridge rectifier is the inductive switching circuit, as shown in Fig 2.3.

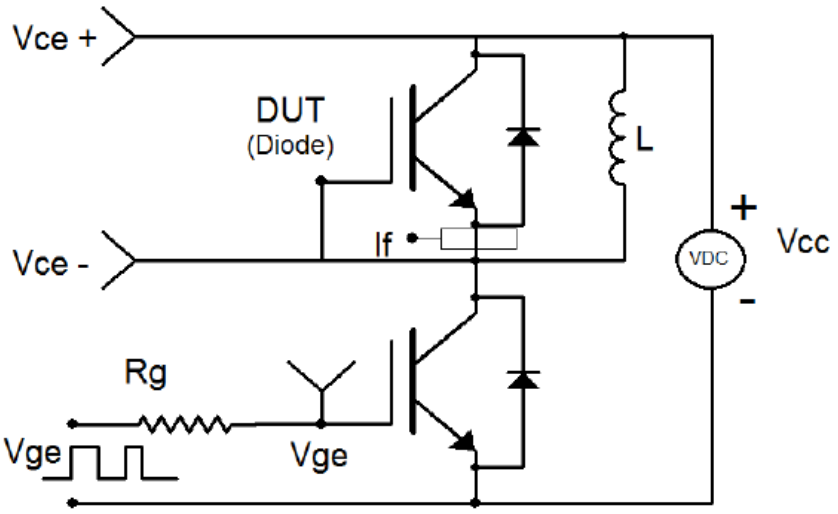
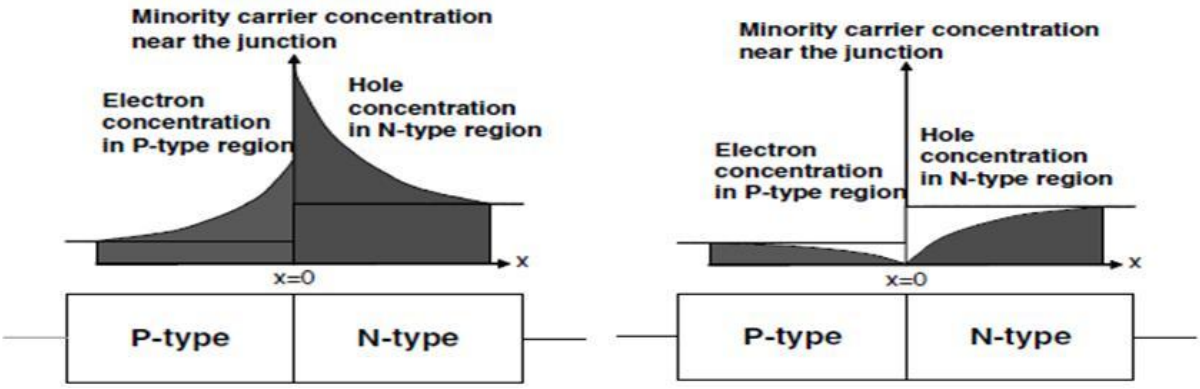


Figure 2.3. Application circuit for the diode.

The high side diode in this application supports the inductor current when the low side IGBT is switched off. This means the diode is in the ON state, and conducts the current. When the low-side IGBT is turned on again, the diode is forced to change to an OFF-state, but the current being conducted takes a little longer to reduce to 0 because the carriers need to deplete from the drift

region. A pictorial representation the device physics which form the operating principle behind the diode commutation property is shown in Figure 2.4 [3].



(a) (b)

Figure 2.4. Device theory behind (a) conduction and (b) blocking modes of the diode [3].

For the diode to switch from the On to Off state, the charge distribution in the device needs to change. As shown above, the density of the minority carriers is the main parameter governing the charge distribution in the structure, as well as the rate it dissipates. The carrier density itself is a function of the background doping concentration of the N-region and the area of the diode.

The breakdown in the current flow is shown in Figure 2.5. When the low side FET is turned on, the current in the FET starts rising once the gate voltage exceeds the threshold voltage (Vth). This increase in current corresponds with the decrease in diode current, maintaining the constant inductor load current at all times.

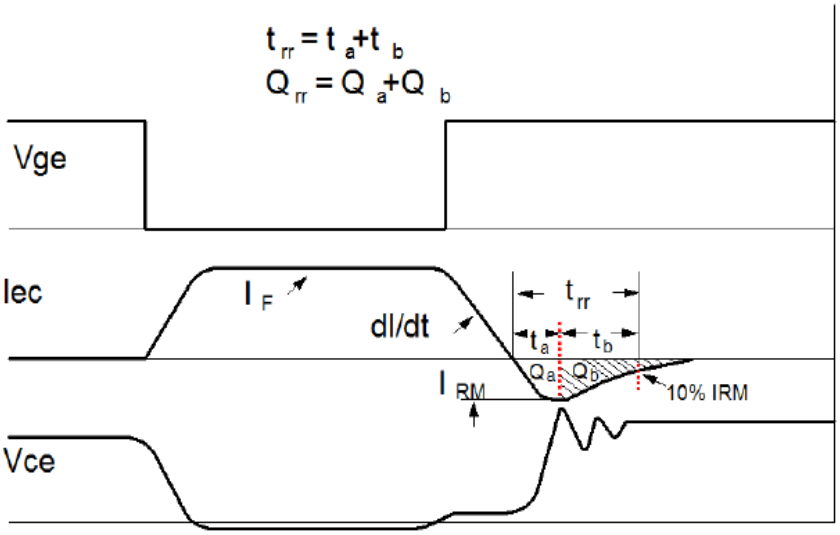


Figure 2.5. A typical diode reverse recovery curve.

The different circuits used to characterize the diode performance is mentioned in [4], and the diode behaviour duing the reverse recovery stage is explained in [5]-[8]. The total reverse recovery time (Ta+Tb) determines the total switching losses during reverse recovery. The smaller the net charge, the lower the switching losses. While the di/dt parameter is a circuit characteristic, the Irm, ta and tb are determined by the diode structure. A lower carrier injection leads to a smaller Irm, leading to a smaller ta, and inturn results in a faster discharge of the carriers during the tb phase. The tb of the curve can also be influenced by the adding a buffer region, which tends to act as a carrier layer and delays the removal of carriers form the drift region. This increases the softness factor (tb/ta) , which increases the switching losses slightly, but at the same time greatly reduces the probability of voltage ringing during switching. Ringing due to a fast di/dt slope during the tb phase can cause device failure if the overshoot exceeds the rated avalanche breakdown voltage.

Conventionally, the easiest way to control this reverse recovery charge is through carrier lifetime control. This can be achieved through multiple methods, but the core purpose of this approach is to affect the natural lifetime of the carriers so as to control the amount of carriers that need to be depleted from the drift region when the diode enters a reverse bias state. The lower the amount of carriers to be flushed out, the faster the diode depletes during turn off. This results in a reduction of the net Qrr.

Prior Art

Given the proliferation of high power systems and the increased need for their efficiency, various concepts for improving the diode performance have been studied before. These can be broadly classified into two primary groups:

- External Lifetime Control: Under this category, the diode structure used is mostly a regular planar structure, but uses external lifetime control techniques like electron radiation and proton radiation to control the recombination rates of the carriers.
- Injection Control: Under this category, the diode structure itself serves to control carrier injection and improve the Vf-Qrr trade-off.

The earliest innovations in improving the diode characteristics pertain to external lifetime control, while the structural improvements are a lot more recent. While both display markedly improved characteristics at room temperature (RT), external lifetime control techniques do not hold at high temperatures since the defects are annealed away, causing the carrier lifetime control to revert to normal.

External Lifetime Control

There are multiple ways to implement lifetime control in a diode. Some of the common methods include electron radiation, proton radiation and heavy metal (gold) radiation [9]-[13]. The basic concept involves introduction of defects into the silicon which act as recombination centers for the carriers, as shown in Figure 2.6

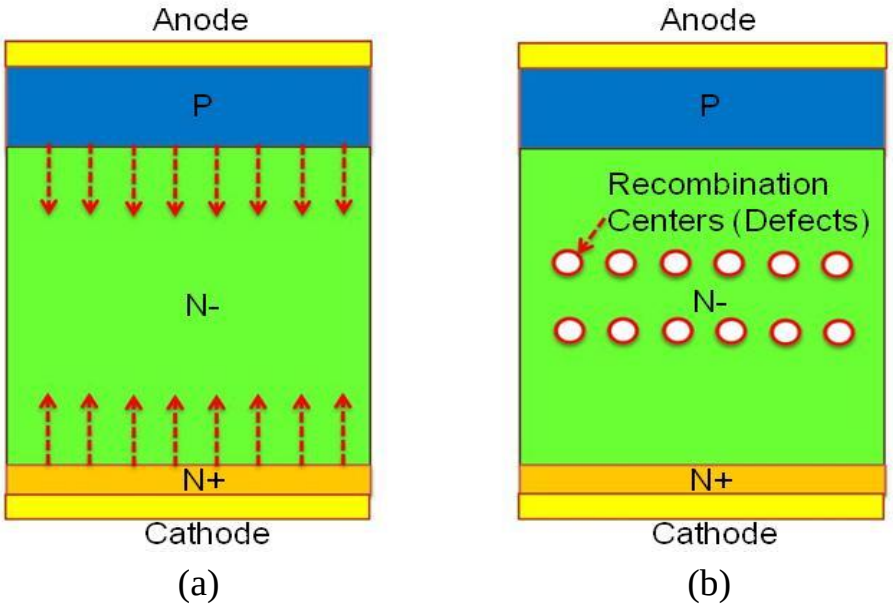


Figure 2.6. Device structure indication carrier flow for both a non-lifetime controlled and a lifetime controlled device.

Electron Radiation

The most common method of lifetime control is electron irradiation. In this method, the device is bombarded with electrons at high energy. This introduces physical defects in the silicon, which usually occur in the drift region. The defects in turn act as recombination centers for the carriers, thus limiting the amount of uncombined carriers in the region. The higher the energy at which the electrons are irradiated, the more defects formed in the Silicon, leading to an even larger

decrease in the carrier lifetime and the reverse recovery charge. This can be shown in the following figure.

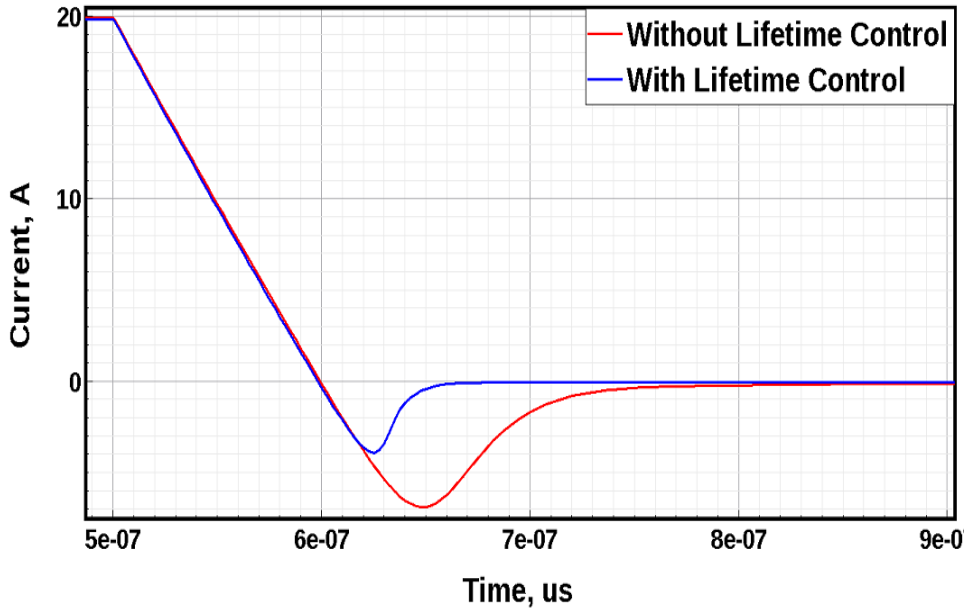


Figure 2.7. Effect of carrier lifetime control on the reverse recovery charge.

As clearly seen in Figure 2.7, carrier lifetime control leads to a faster recombination of the holes and electrons in the drift region. A faster recombination results in a lower Irm, and a lower Tb. This significantly lowers the Eon of the low side MOSFET, thereby increasing the system efficiency.

While this approach is quite common and widely used, there are many issues with electron irradiation. Firstly, the amount of defects introduced leads to higher leakage level. Secondly, at higher temperatures, some of the defects get annealed away, returning the carrier lifetimes closer to their intrinsic values. The Qrr respectively increases as the defects get annealed away, leading

to higher Qrr at higher operating temperatures. This is especially an issue for applications which require the device to operate at higher temperature ranges exceeding 150C.

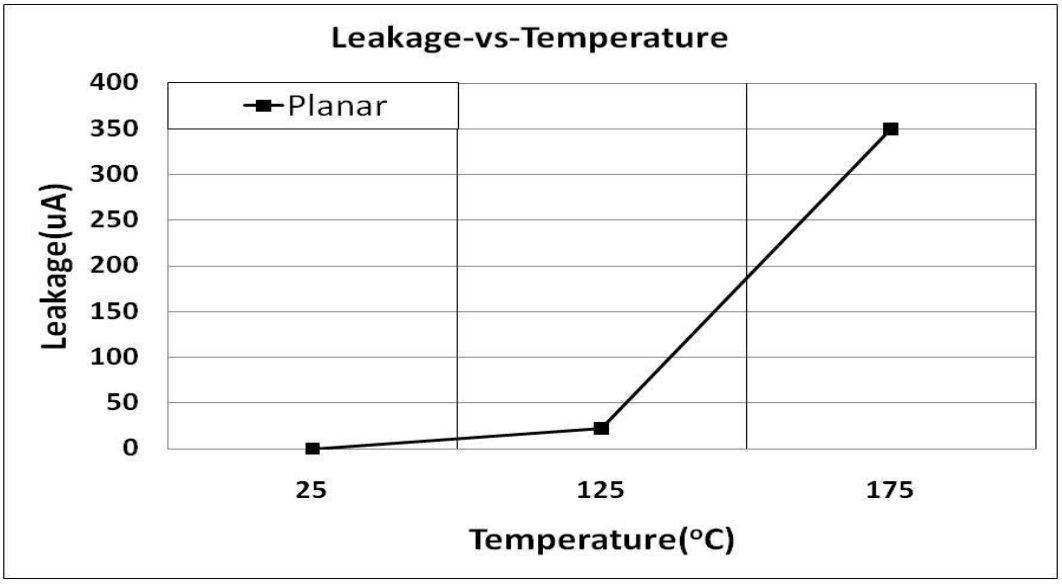


Figure 2.8. Effect of electron radiation on leakage current of a conventional planar device.

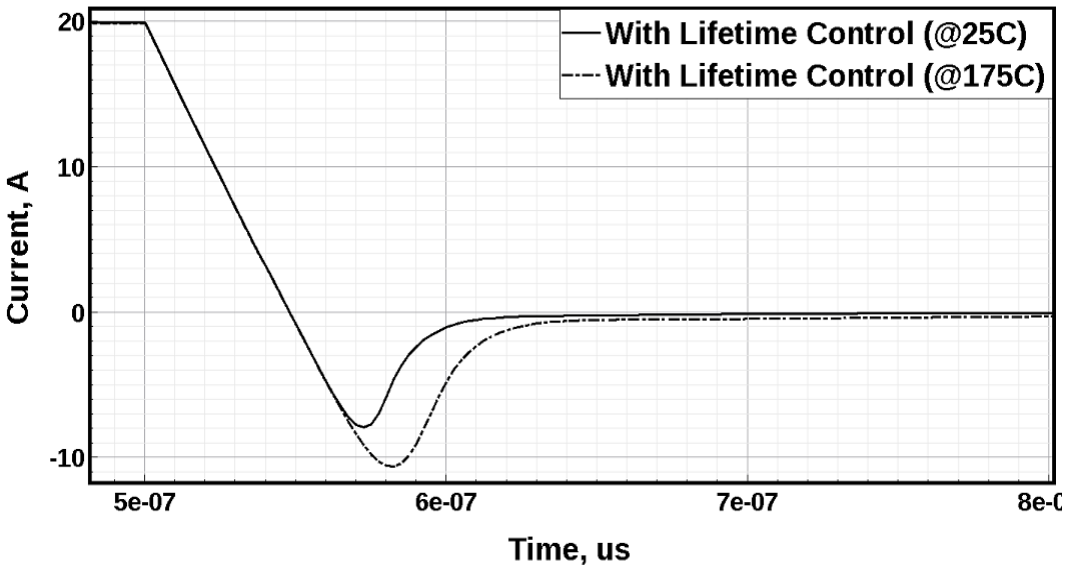


Figure 2.9. Effect of electron radiation on the reverse recovery charge of a conventional planar device

Thirdly, while the electron irradiation decreases the Qrr at room temperature, there is a corresponding increase in the Vf. While this does not play a role in the switching losses, it does

play a role when the diode conducts, increasing the heat dissipation within the device. This again harms the overall efficiency of the system.

The higher the electron radiation energy, the more the change in the Vf and the Qrr specs, but the more severe the degradation in the leakage and the high temperature characteristics

Gold Diffusion

Another approach to lifetime control is through gold diffusion. This approach was commonly used previously, but has multiple issues associated with it [9]. Gold being heavier does not diffuse deep enough in the silicon, so the defects tend to be localized close to the contacts. Also, the recombination centers arising from the Gold diffusion is in the center of the silicon energy gap, causing a significantly higher leakage current.

Platinum Diffusion

Platinum diffusion is another option for lifetime control using heavy metals. While it does show better leakage characteristics, it demonstrates much more degraded high temperature reverse recovery characteristics [9].

There are other lifetime control processes used to varying degrees, which are explained in detail in [14]-[22]. All the above mentioned lifetime control techniques operate on the same principle, that of introducing physical defects into silicon which act as recombination centers for the carriers, hence reducing their lifetime and the net charge during commutation. They show varying degrees of improvement with regards to the reverse recovery characteristics of the diode,

but with invariably similar penalties of higher leakage current and forward voltage, Vf. The effect of a process like electron radiation is explained in [23].

Injection Control

While the above mentioned methods address the carrier density using external lifetime control techniques, they don't actually improve the Vf-Qrr trade-off. They only change the operating point along the Vf-Qrr curve. Diode structures with inherent injection control, on the other hand, seek to limit the actual amount of carriers which are modulated in the device, thereby greatly reducing or completely eliminating the need for any extra lifetime control.

Reducing the Qrr in the diode through injection control is described in [24]-[28]. The operating principle for this category of diodes is essentially similar. A form of localized injection control, implemented either on the anode or cathode side, controls the amount of carriers injected into the drift region. Some of the popular ones are as listed below:

Schottky Controlled Injection Diode

This structure controls carrier injection though schottky contacts on both the anode and cathode side. By killing parts of the P-anode injection through P-schottky regions, the diode sees reduced hole injection form the anode side. On the cathode side of the diode, the structure uses a transparent anode structure, again by killing some of the N+ cathode injection by replacing parts of it with a P-schottky contact. The structure is shown below in Figure 2.10 [24].

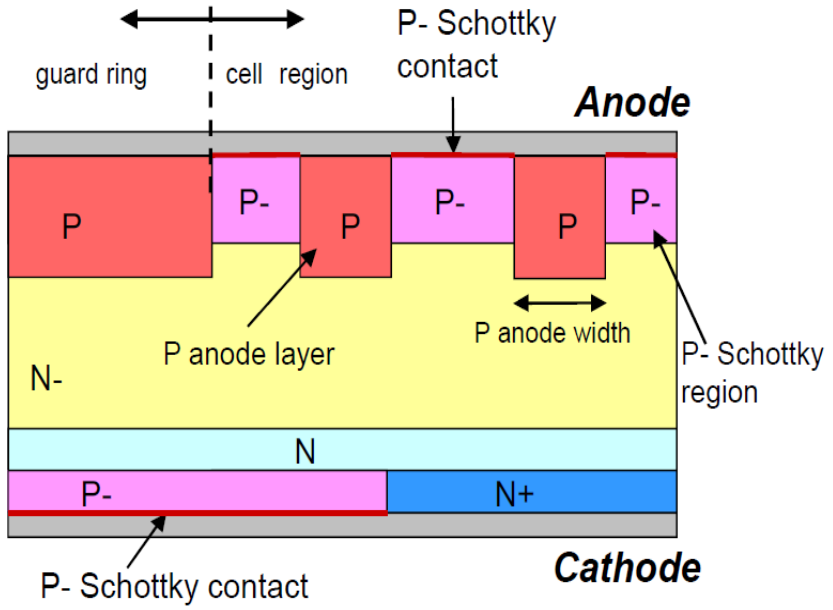


Figure 2.10. Schottky Controlled Injection Diode [24].

While this structure helps realize a flat carrier profile, it still requires significant backside engineering. Also, the N+ contact might have activation issues, which means the backside contact might have a few issues. Also, while schottky diodes offers great trade-offs with Vf and Qrr due to almost instantaneous recovery, they are generally not very compatible with high power systems.

Hydrogen Implant

A commonly used method is that of Hydrogen Implant, as mentioned in [28]. In this approach, a multi-step hydrogen implant helps form the buffer and the backside collector implant. The basic structure for a device with Hydrogen implant is as shown below in Figure 2.11

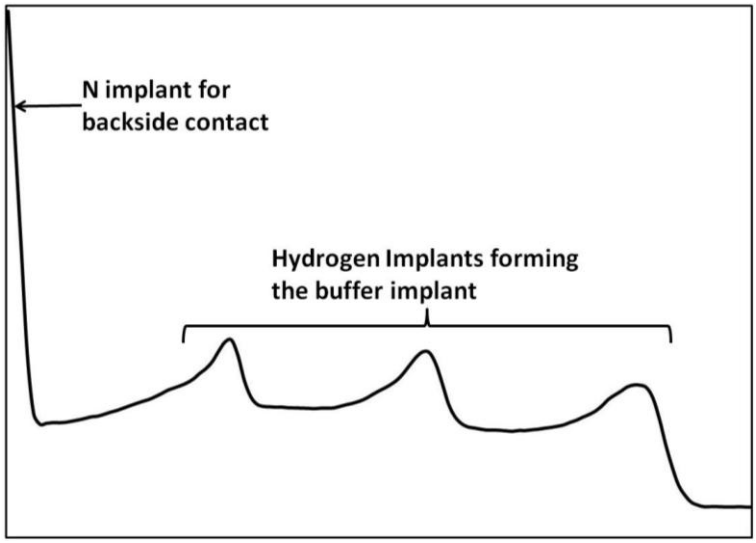


Figure 2.11. Buffer formation and backside injection control using hydrogen implant.

This approach is beneficial for multiple reasons. Apart from the injection control afforded by the hydrogen implants, the three-tiered hydrogen implants are different energies also act as the buffer for the structure. This is also used for IGBT structures, where the backside implant for contact purposed is a P-type implant. While efficient and popular, this approach is more expensive. Hydrogen implants are more expensive to implement, and usually have restrictions with regards to the wafer handling capabilities for the equipment.

CIBH Diode

Another form of injection control was also implemented in a structure called the CIBH diode [25]. In this structure, the injection control is performed by patterned implants of a P type dopant like boron on the backside to control any injection from the N type cathode. The structure is shown in Figure 2.12 [25].

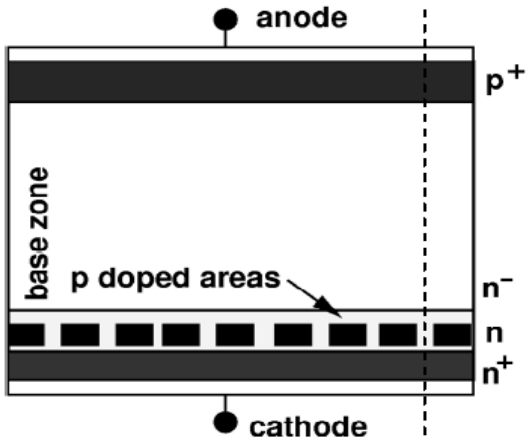


Figure 2.12. Construction of the CIBH Diode [25].

While extremely effective, the CIBH diode again comes with its share of issues. The CIBH structure also needs a thin wafer due to backside processing involved. So the structure is extremely sensitive to the backside process conditions, including variations in the backgrind thickness of the wafer and the amount of N+ concentration required to form a good ohmic contact with the backside metal.

Other structures used for injection control are mentioned in [29-[39], including the commonly used Merged PiN Schottky Diode, Static Shielding Diode, Soft and Fast Recovery Diode and the SPEED Diode. All these diodes seek to improve the Vf-Qrr trade-off inside the diode by directly addressing the carrier injection within the diode. They offer improved performance of the diode at room temperature, without the side-effects of degraded leakage and increased Qrr at high temperatures.

Trench Shielded Fast Recovery Diode

Along the same lines, a Trench Shielded Fast Recovery Diode [40], [41] is proposed. The basic structure for this is as shown below in Figure 2.13. The basis of the structure is the topside injection control. In this case, the N+ region as shown in the figure helps control the injection from the topside P implant. If used as a standalone concept, this would lead to a punch-through effect. So to achieve this, we have to use a trench MOS, charge balance structure where the grounded polysilicon filled trench helps charge balance the heavy N+ region. In essence, this is similar to trench based super junction structure on top.

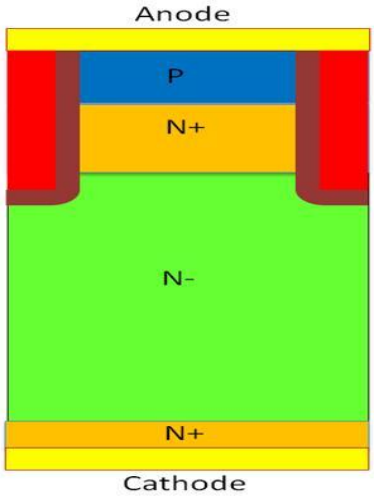


Figure 2.13. Basic cell structure of the proposed trench shielded fast recovery diode.

If we did not have the super junction structure on top, the N+ concentration required to achieve the desired level of injection control would easily deplete the P region and punch-through, leading to almost instant breakdown. This can clearly be illustrated in the following Figure 2.14. By inserting a polysilicon filled trench extending unto the depth of the N+ region at regular intervals (determined by the amount of charge in the N+ region), we can extend the ground

potential deeper into silicon. This helps maintain a higher breakdown potential of the device while enabling the N+ region help suppress injection from the P without punching through.

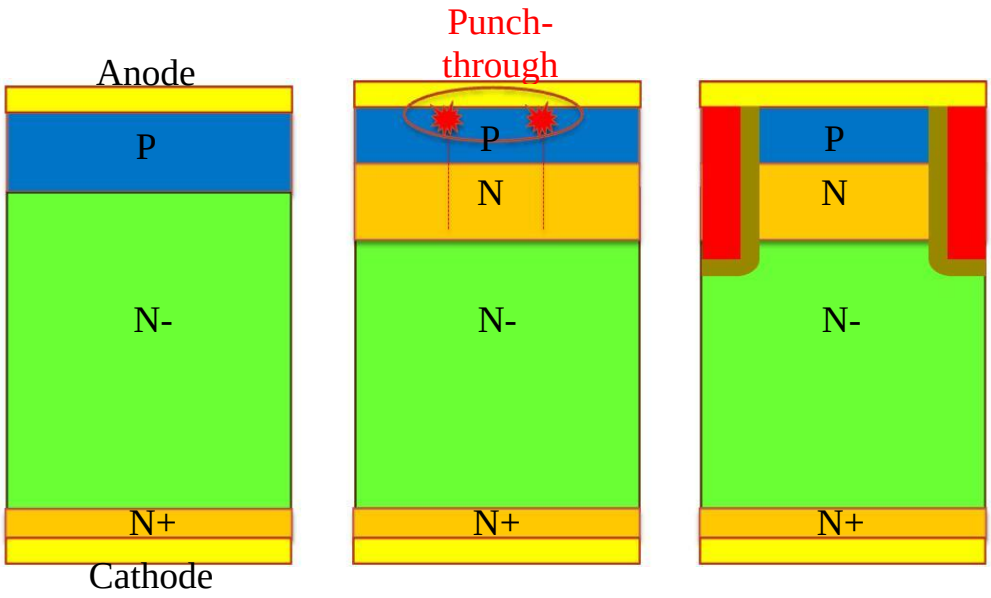


Figure 2.14. Effect of the polysilicon filled trench on the device avalanche capability compared to a conventional planar structure.

Our initial design is for an application voltage of 1350V. This however can easily be implemented for lower breakdown regions like 650V applications. The higher or lower voltage rating is achieved by changing the N- drift region thickness and resistivity. Meanwhile the topside partial superjunction is the same. This means all diodes with this structure share similar electric filed profiles and impact ionization points. The electric potential lines and impact ionization points for the structure are as shown in Figures 2.15 and 2.16.

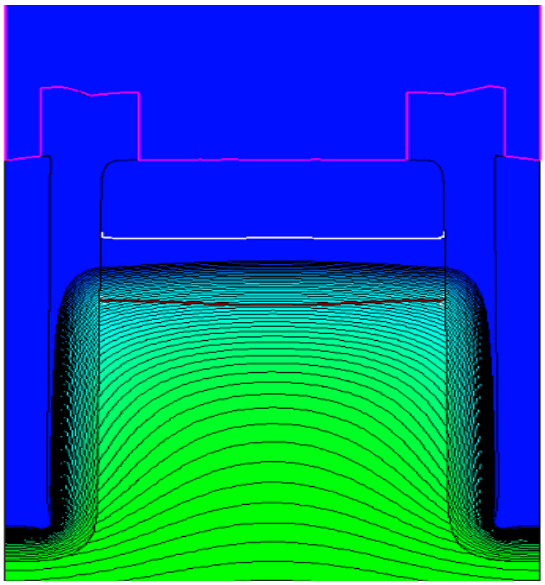


Figure 2.15. Distribution of electrostatic potential lines around the trench and in the trench liner oxide.

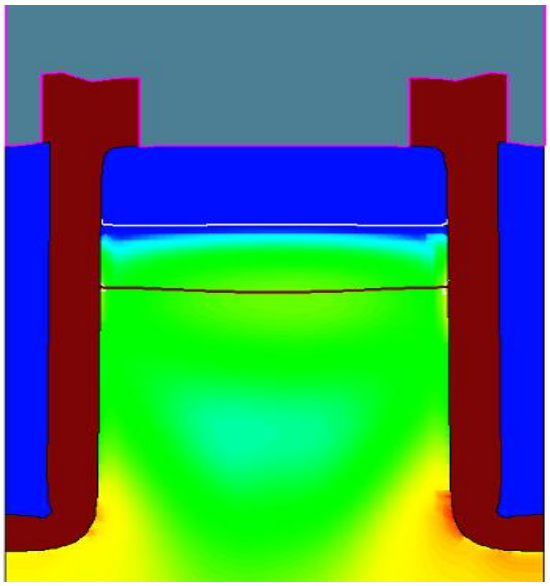


Figure 2.16. Impact Ionization point in the proposed structure which shows the region where avalanche occurs.

The initial step involved in designing this diode was the decision to use a soft punch through diode. This would involve adding a buffer at the backside to help terminate the electric field.

This buffer also serves the additional purpose of adding a bit of softness to the Qrr curve of the diode. The next step was to determine the resistivity and thickness of the diode required to support this high a voltage. Considering a tolerance of an additional 20% for a 1350V diode, the design would have to support a voltage in excess of 1620V. Through simulation, a thickness of 105um with a resistivity of 85ohm-cm was arrived at. The electrostatic potential and electric field for this is shown below in Figure 2.17.

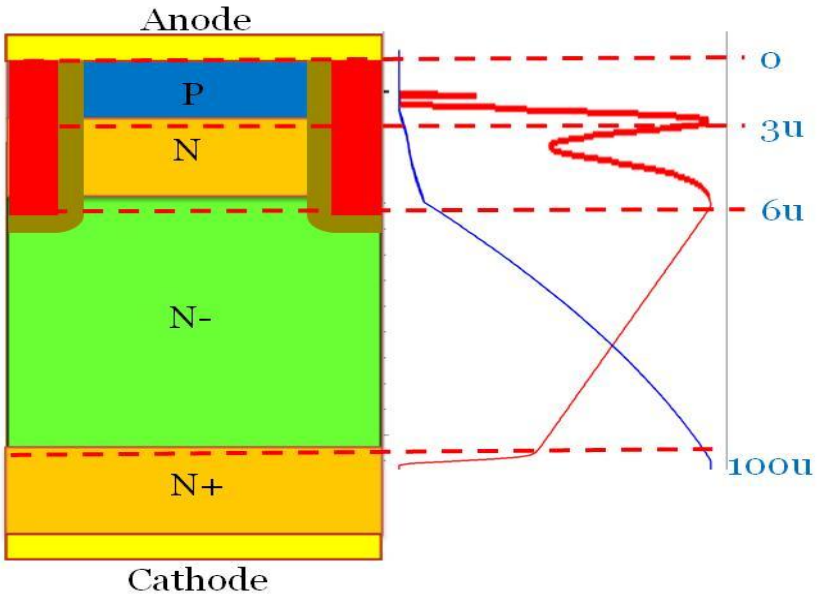


Figure 2.17. Electric Field distribution in the structure.

Focussing exclusively on the charge balance region on top, we observe that the trench MOS structure successfully helps shift the peak electric field deeper into silicon, thus alleviating the stress at the P-N junction and helps achieve the intended injection control without sacrificing the breakdown. The peak electric field at the base of the trench is supported by the thickness of the liner oxide used. The liner oxide needs to be thick enough to support the potential lines in the

structure because this is the region where the maximum impact ionization takes place in the structure.

It is critical that the trench extend atleast till the depth of the N+ region. If the trench is not as deep, the heavier N+ underneath the trench bottom will result in impact ionization before the desired breakdown voltage is reached. The width of the trench, thickness of the liner oxide and charge in the N+ determine the pitch of the structure. This again was arrived at 6um through simulation. If the N+ charge is increased, the liner oxide thickness is increased accordingly to accommodate the additional potential lines. But for a given trench width, the thickness of the liner oxide has an upper limit. In this case, the pitch would have to decrease to allow for the same.

Through simulation, the thickness of the topside N+ region was arrived at 4.5um for the desired amount of injection control. Accounting for the diffusion of the N+ charge into the N- drift region, a trench depth of 6um, with a width of 2.5um and a liner oxide thickness of 6.5um was deemed to be optimal.

Even though the trench MOS structure supports a majority of the diode breakdown, the P base still needs to have a minimal charge to prevent punch-through. The resulting doping profile is shown in Figure 2.18.

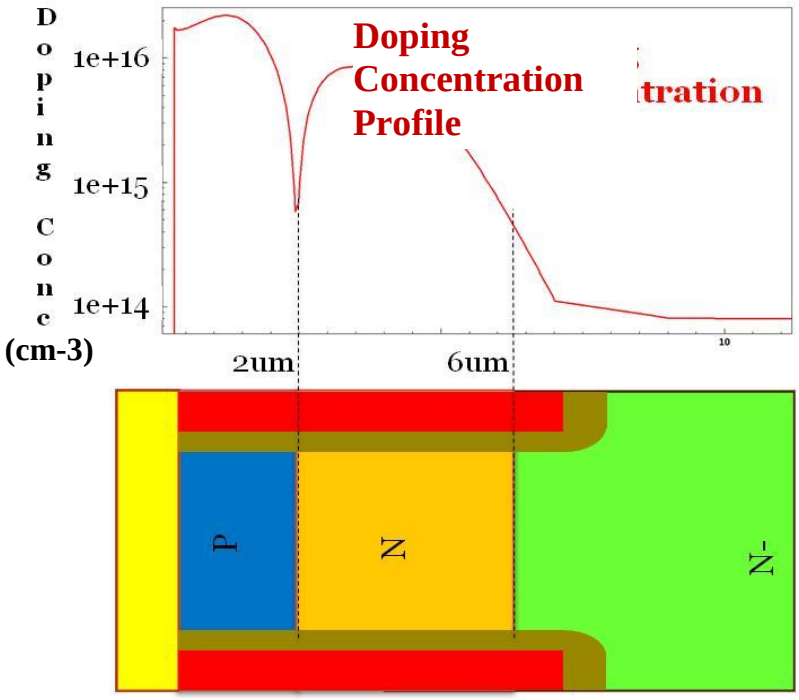


Figure 2.18. Doping Concentration Profile showing the effect the topside N heavy region has on the injection from the P-base.

Fabrication

The process steps involved in creating this structure are as follows:

Step 1: Epi Growth

The first step is to grow the drift region epitaxial layer as decided through design. The starting material is an Arsenic substrate with resistivity <.003 ohm-cm. The subsequent epitaxial growth for the drift region is carried out in a high pressure chamber at a temperature of 1100C. The first layer to be grown is the buffer region. There are two ways to design the buffer as desired in the structure:

- Implant from the backside and apply a thermal cycle to diffuse the N type dopant deep enough to form the desired buffer layer.

- Grow the N+ buffer as part of the drift region growth.

Implanting the buffer from the backside would involve using a thin wafer without the substrate. For our purposes, we retain the substrate on the backside. So, we grow the buffer region, with a thickness of 10um and resistivity of 0.5ohm-cm. The thickness and resistivity of the buffer region are decided based on the amount of softness required in the Qrr curve.

After the buffer region is grown, the drift region epitaxial layer is then grown, based on the design target for the breakdown voltage. For a higher breakdown voltage characteristic, the drift region needs to be thicker and have a lower resistivity since it supports the bulk of the electric field. This is worked out to be around 105um thick with a resistivity of 55 ohm-cm.

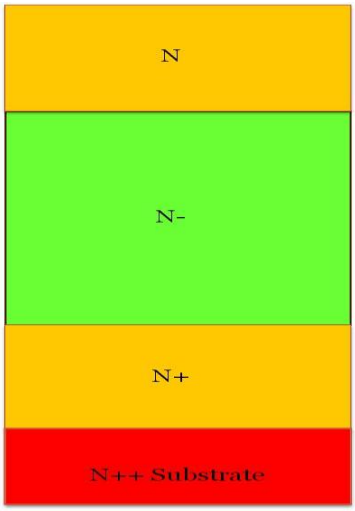


Figure 2.19. Starting epi structure profile for the diode.

Once the drift region is grown, the topside N region is grown. The thickness and resistivity of this region is dictated by the depth and width of the trench, and more critically the thickness of

the liner oxide in the trench. The principle behind this was discussed in the previous chapter. For this structure, the specifications of the topside N heavy region are 4.5um thickness and 0.5 ohm-cm resistivity. The resulting epi structure is as shown in Figure 2.19:

Step 2: Trench Etch

The next step is to form the trench. This is done by first covering the epi structure by Photo-Resist. Following that, we use a patterned mask to expose selective areas where we need to etch the trench. The exposed PR is then chemically washed away and we implement a chemical etch process wherein a 6um deep etch is made in Silicon. After the etch is completed, the remaining PR is washed away. This results in a structure as shown in Figure 2.20.

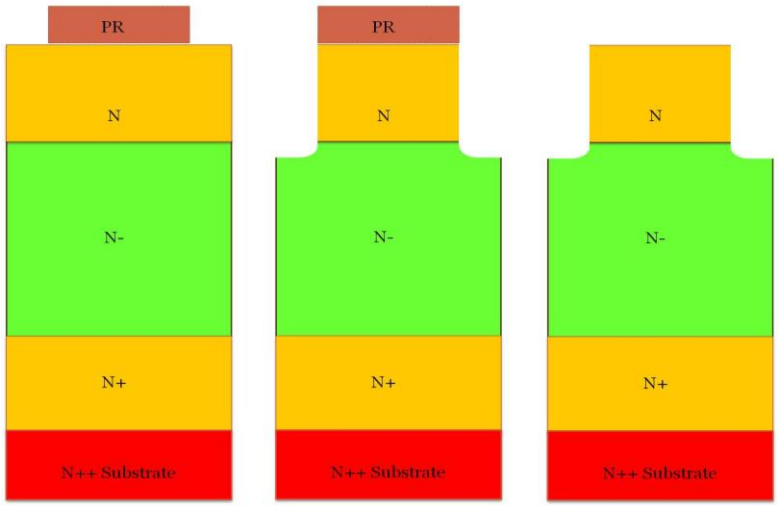


Figure 2.20. Process steps involved in forming the trench.

Step 3: Thermal Drive

Once the trench etch is completed, the next step is for a thermal cycle. This step is required for two reasons:

1. Grow the trench liner oxide to support the required breakdown voltage. The thickness of the liner oxide depends on the resistivity of the N+ top epi region grown and the pitch of the device structure. The optimum oxide thickness for this application was found to be ~6700A. The liner oxide thickness is essential for the charge balance region in the diode. A smaller liner oxide thickness is insufficient to support the electric field at that location. On the other hand, if the oxide is much ticker than expected, the amount of polysilison required for shielding is reduced. This again would reduce in a BV drop. This is shown in Figure 2.21.

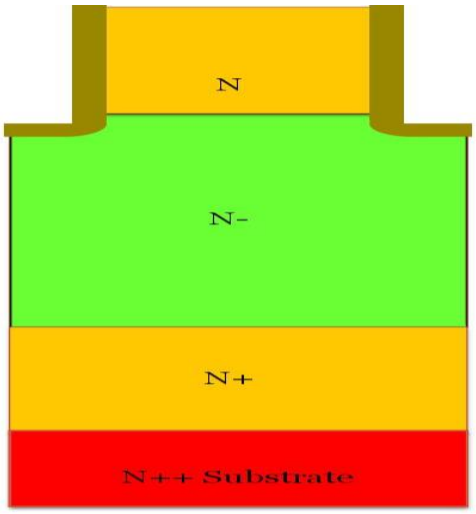


Figure 2.21. Process steps showing formation of the trench liner oxide.

Step 4: Polysilicon Deposition

After the trench liner oxide is grown, the N++ doped polysilicon is then deposited on the wafer. Since the polysilicon is desired only in the trench, after deposition, the surface polysilicon is etched away. After the etch step, a CMP (Chemical Mechanical Polarization) step is down to smooth out the silicon surface. This removes any surface irregularities that occurred as a result of the etching process. The final structure looks as shown in Figure 2.22:

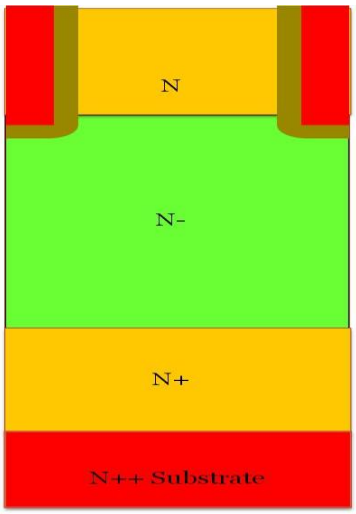


Figure 2.22. Process steps showing deposition of the heavily N-doped polysilicon in the trench.

Step 5: P-Base Implant

Once the basic epic structure is grown, the next step is to implant the P-base dose. The dose is dictated by3 factors:

- The target forward voltage of the diode, Vf. The implant dose controls the amount of hole injection into the drift region.
- The target breakdown voltage of the diode. The resulting P base concentration should be enough to prevent the topside heavy N region from punching through and maintain the target breakdown voltage , which in this case exceeds 1600V.
- The contact resistance of the topside Metal contact. The amount of Boron at the surface plays a huge role in determining the contact resistance after metallization. A higher P concentration at the surface results in a much lower resistance, thereby leading to faster injection.

Taking the above-mentioned factors into consideration, the boron implant specification of 6.5e12 @ 480 KeV was arrived at through TCAD simulations, followed by a thermal cycle @1150C for 60 minutes to diffuse the boron enough to support the required BV. Figure 2.23 shows the structure at the end of this process step.

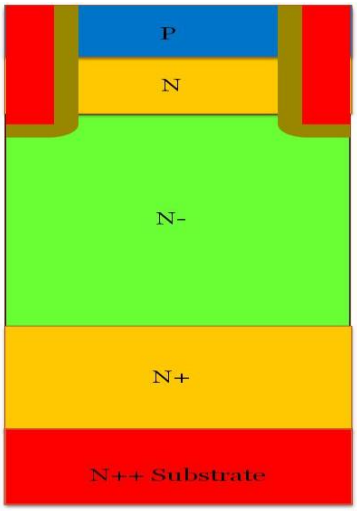


Figure 2.23. Structure after P-Base implant and diffusion.

Step 6: Topside Metallization

The next step is to form the metal contacts to the P base (Anode). To do this, we first need to use a mask layer to establish where the metal will contact the silicon. In this case, we will form a metal contact to both the silicon between the polysilicon filled trenches, and the polysilicon in the trench itself. But we cannot form a blanket metal contact because that could create some of the liner oxide to get etched away and cause a metal spike in the silicon-oxide junction. If the metal spikes into the junction and goes deeper into the silicon, the current flow will bypass the P-base and go through the metal, which would lead to a reduced breakdown. So the contact

opening is to be established only at the silicon and the polysilicon regions. Figure 2.24 illustrates this process step.

Following this, the Metal is then deposited. In this case, the metal would be an Aluminum mixed with Silicon so as to form a good low resistivity contact with the silicon surface. The low resistivity is important, because if the metal contact to the silicon is insufficient, the injection from P-base is minimal, resulting in a much higher Vf.

This is also a consideration for deciding on the P-base dose. The P doping concentration at the surface where the metal contacts the silicon is also critical in determining the quality of the contact. A low P concentration reduces the contact resistivity. The energy of the P-implant also plays a role in this scenario. A higher energy implant shifts the profile deeper into the silicon, reducing the amount of P in the silicon. So there is a trade-off between the depth of the P-N+ junction and the doping concentration of the P at the surface.

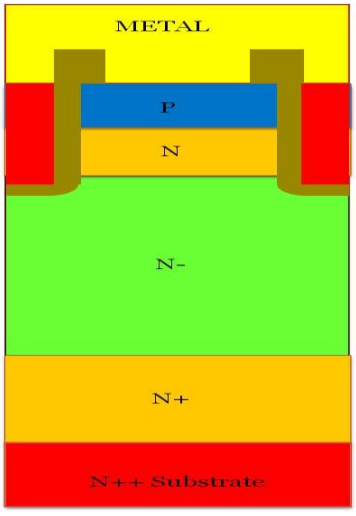


Figure 2.24. Structure after topside metallization.

Step 7: Backside Metallization

Once the topside is processed, the wafer is flipped and background to a thickness of ~200um. Since the wafer around that thickness is usually just the substrate, any variation in the backgrind would not cause a major issue. After the backgrind, we implant an N+ dose to help ensure a good, low resistivity contact with the back-metal. The metal used for the backside drain contact is usually a combination of Ti+Ni+Ag. The final structure is then showed in Figure 2.25.

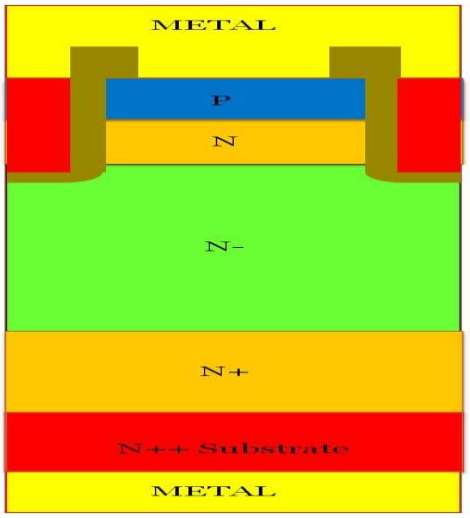


Figure 2.25. Structure after backside metallization.

Impact of Injection Control

As mentioned earlier, the whole reason for injection control was to avoid the pitfalls associated with electron irradiation. The proposed structure seeks to address that. The N+ region acts as a suppressant for any injection from the P base region, thus enabling a lower catenary profile in the drift region. Figure 2.26 shows the difference in the carrier density profiles between the different structures.

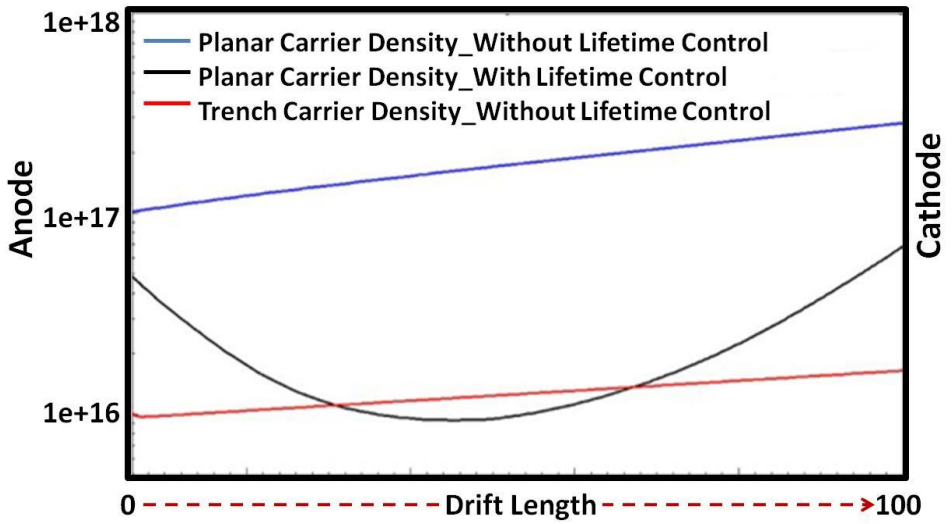


Figure 2.26. Effect of lifetime and injection control on the catenary profile in the diode drift region.

As seen above, when electron irradiation is used, the catenary dips in the middle of the drift region. As mentioned earlier, this is due to the defects created in the region. This dip in the profile is what results in the performance enhancement in the device. However, at higher temperatures, the defects get annealed out, and the profile starts trending towards that of the non-irradiated device, thereby neutralizing any effect on the carrier lifetimes.

By implementing a form of localized lifetime control, we can reduce the net carrier density close to levels post electron irradiation. This means we can achieve a flat catenary at room temperature and maintain it at higher temperatures. This greatly improves the Vf-Qrr trade-off of the device. The effect of this can clearly be seen when the device is applied to the inductive switching circuit mentioned in Figure 2.3.

Results

The proposed structure was implemented in Silicon and the results obtained were pretty close to what was expected. For this diode, we used a current density of 500A/cm2. The device was designed for a BV of 1600V with a target V_F=1.4V. The FRD easily met the desired specifications, as seen in Figure 2.27.

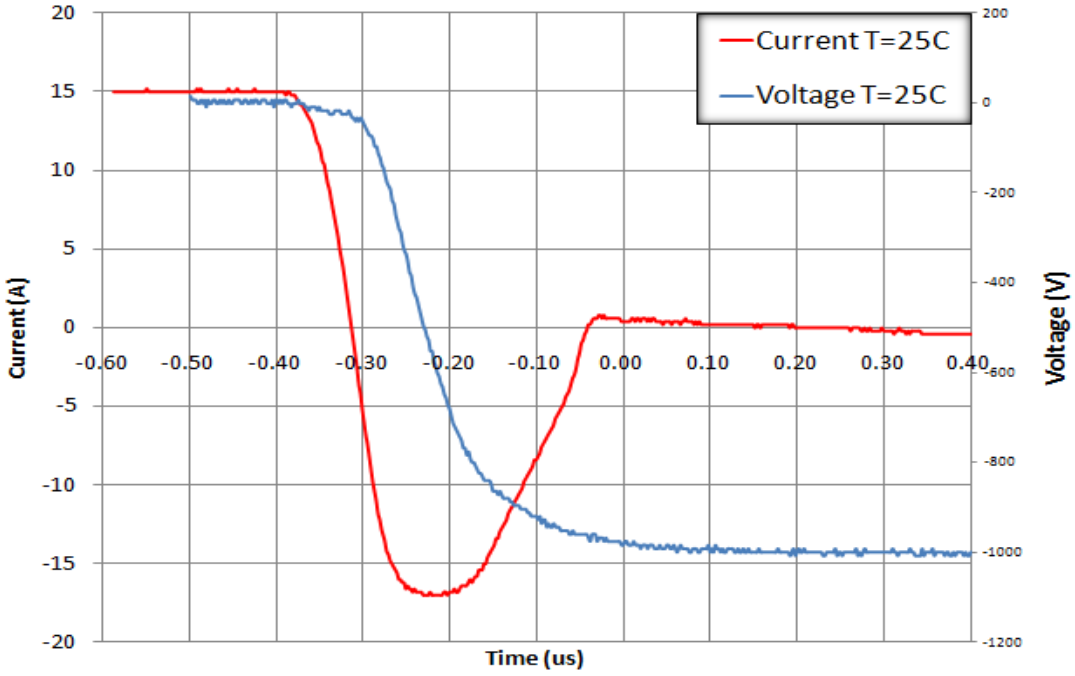


Figure 2.27. Measured Voltage and Current waveforms of the FRD during reverse recovery phase.

The above figure shows the Voltage and Current waveforms of the fabricated device during reverse recovery at room temperature. The test was conducted at a V_R=1000V, with an I_F=15A and a Di/Dt=400A/us.

We then compared the performance of the fabricated diode with that of a regular lifetime controlled planar device with similar specifications. As seen in Figure 2.28, we compare the

leakage of the device across the desired temperate range. It is clearly observed that the fabricated device shows minimal degradation at higher temperatures which is critical for industrial applications such as Induction Heating cookers and motor drives. In comparison, due to the presence of induced defects from ER, the planar diode shows significantly worse leakage at 175°C.

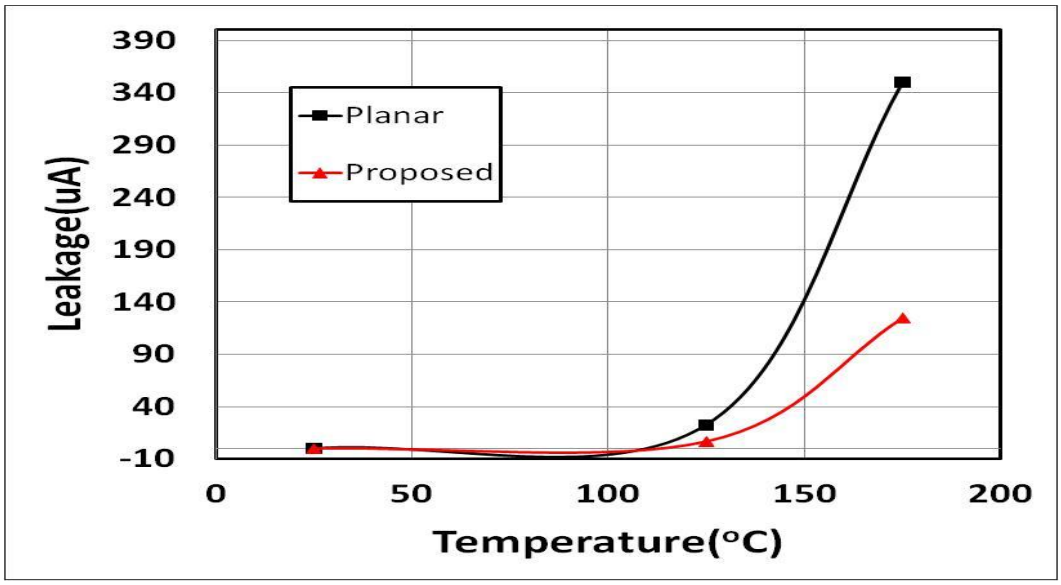


Figure 2.28. Measured Idss values of conventional Electron Radiated Device and proposed structure at room temperature and higher temperatures.

Next, we compare the reverse recovery curve of the FRD with that of a lifetime controlled planar diode. All comparisons were made at a V_R=1000V, with an I_F=15A and a Di/Dt=400A/us. As seen in Figure 2.29, the proposed FRD displays similar reverse recovery characteristics to that of the planar FRD at room temperature. But at 175°C, the lifetime controlled planar device showed degraded reverse recovery characteristics.

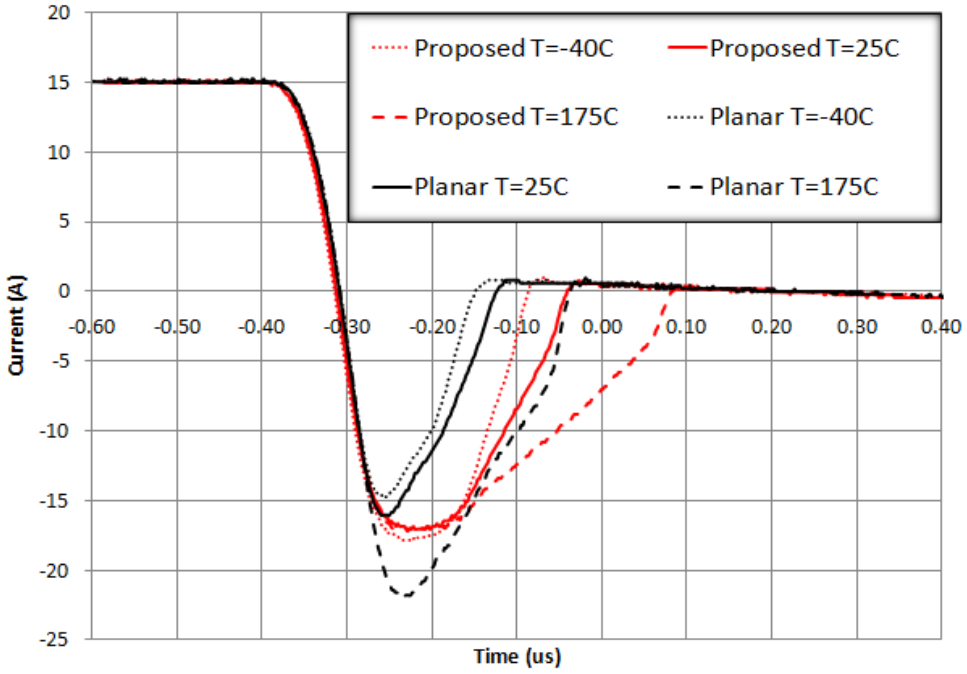


Figure 2.29. Measured Qrr curves of proposed structure compared with a conventional Electron Radiated Device at -40, 25 and 175°C.

As observed in the above figure, the trench FRD maintains the peak reverse recovery current from -40-175°C. This is critical because the typical temperature during industrial applications is between 90-100°C. This greatly helps reduce the conductions losses in the co-packaged device during reverse conduction.

It is also observed from Figure 29 that the proposed figure without lifetime control also has better softness than the planar structure. Table 2.1 lists the I_{RM} and softness factors of the two devices measured from the curves from the previous figure.

Table 2.1. I_{RM} and softness values of compared devices

Device	Temperature (°C)	I_{RM} (A)	S
Proposed	-40	17.8	1.5
	25	17.2	2.32
	175	17	3.78
Planar	-40	14.8	2.16
	25	16	2.83
	175	22	2.65

Conclusion

The results support our claim that the proposed structure displays significantly improved performance over traditionally electron radiated devices, especially at high temperatures. This expands the scope for designing diodes for industrial applications which require stability at temperatures rated as high as 175^{o}C. A couple of things are to be noted here:

- Both diodes were designed to have similar forward voltage of 1.6V.
- At Room Temperature (25°C), the Irm of the trench diode is similar to that of a planar diode which undergoes electron irradiation. However, at a higher operating temperature (175°C), the Irm increases significantly for the planar diode, which the trench diode maintains the Irm current level. This clearly shows the benefit of an injection control mechanism as opposed to an external lifetime control approach.
- Another thing to be noted is the softness of the curve. External life time control reduces the Irm current tail during the tb phase. For the trench diode, at room temperature, the

softness if quite significant. This is mostly due to improper Epi design. By adjusting the drift layer resistivity and the buffer layer characteristics.

- Both devices show increased softness at higher temperatures, because higher temperatures naturally increase the carrier lifetime, increasing the time it takes to remove them from the drift region.

Advances are also being made in designing fast recovery diodes in alternate materials like SiC, GaN and GaAs [42]-[47]. These structures show various improvements over the conventional Silicon technology, especially in terms of reverse recovery. But given the still relatively nascent stages of development for these technologies, and the issues regarding cost and compatibility with Silicon structures in the circuit, the adoption of these technologies for conventional applications is still further down the road.

CHAPTER 3
HIGH VOLTAGE EDGE TERMINATION

Introduction

High voltage power semiconductor devices are used in a wide range of applications. These include the high voltage power MOSFETs in power supplies for Flyback, PFC and LLC topologies, insulating gate bipolar transistors (IGBTs) and fast recover diodes (FRDs) for motor drives, induction heating and solar inverters. As mentioned in the previous chapter, the trench MOS structure is a commonly used technique for improving the performance of these high voltage devices. It has been demonstrated for and injection control in an FRD [41]. With the addition of a buried P-type guard ring though the trench, this technology is extended to a MOSFET [48] and an IGBT [49]. The increased N doping concentration is used to lower the on resistance of the MOSFET and increase the injection enhancement of the IGBT.

One of the major challenges in the design of these high voltage devices is their edge termination. The purpose of the termination region is to avoid premature avalanche breakdown due to electric field crowding near the device edge. It achieves this by spreading out the depletion region at the device surface in order to support the full voltage from drain to source. This also results in high surface electric field in the termination region, in silicon and the passivation layer. The presence of the high surface N concentration makes it difficult to implement most conventional edge termination schemes. This necessitates a novel termination for that very reason.

Prior Art

The most commonly used termination techniques include the abrupt parallel plane junction [50], junction termination edge (JTE) [51]-[54], field rings [55], planar junction [56], metal plates [57], [58] etc. There is a comparative review of the above mentioned schemes along with a few others in [59]. Some of the most common schemes used in high voltage vertical power devices are listed below.

Junction Termination Edge

A Junction Termination Edge Structure was one of the earliest structures used for high voltage edge termination. The concept behind this approach was simply to appropriately counter-dope the surface to shape the electric field as it transitions towards the edge. The JTE is simple to implement, and a very convenient way to implement edge termination. A conventional JTE structure is shown in Figure 3.1 [51].

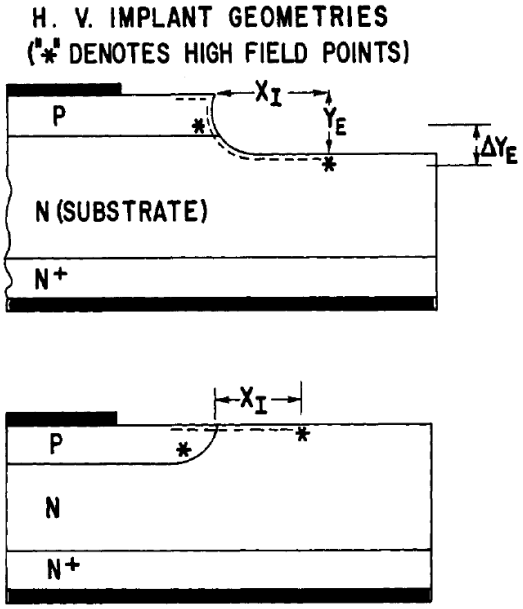


Figure 3.1. JTE Termination schemes in a plane and planar p-n junctions [51].

Field Rings

Field Rings based edge termination structure is the most commonly used termination scheme for vertical power structures. The concept of a field ring is extremely similar to that of a JTE, in that it helps shape the electric field in an efficient manner, but differs in the implementation. While the JTE is just one large cylindrical junction, field rings are multiple in number, helping spread the electric field efficiently along the termination scheme, as shown in Figure 3.2.

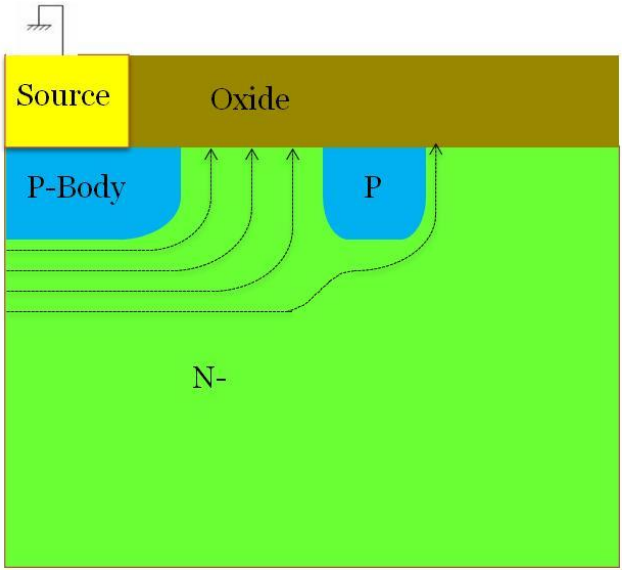


Figure 3.2. A conventional field limiting ring structure.

Metal Plates

Metal plates are used at the surface to prevent the field from collapsing at that point. The potential lines are shaped by the length of the plates, and terminate at the end of the metal plates. The metal plates are usually biased to shape the field accordingly. An example implementation is shown in Figure 3.3.

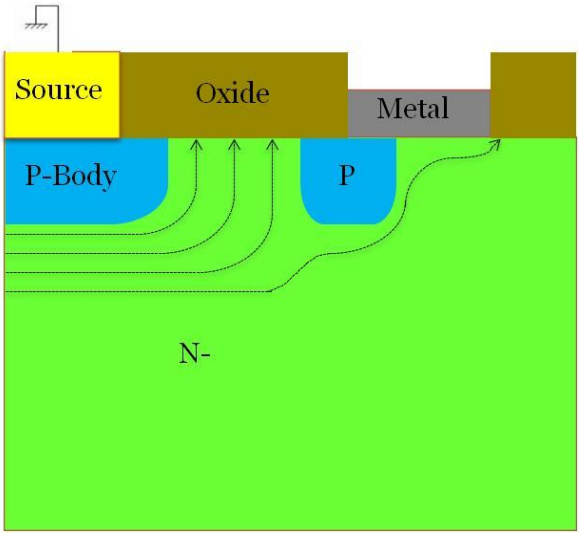


Figure 3.3. An edge termination scheme combining a field limiting ring and a field plate.

Since superjunction structures have a higher drift region doping concentration, conventional termination schemes don't work very well. So, the terminations schemes for charge compensated structures need to be slightly modified for the same. One of the major limitations of these termination techniques is their high surface electric field in silicon. This makes these termination techniques more susceptible to mobile charges during reliability tests. During high temperature, high voltage bias burn-in tests, mobile ions from packaging mold compound and outside sources can accumulate in the termination region and alter its electric field shape, which can increase leakage and lower breakdown voltage (BV) of the device. The silicon region is more susceptible compared to SiO_2 and Si_3N_4 films because of the higher order of magnitude of lower critical electric field strength compared to these passivation films.

Field Plate Based Edge Termination Structures

This structure is similar to a metal plate based edge termination scheme, but the difference being that the field plates are embedded deeper into Silicon through trenches [60]. The breakdown voltage of the scheme is now limited by the spacing between the active cell and edge termination regions, the distance between the p-well regions and the dielectric used in the trench for the metal plates. Figure 3.4 [60] illustrates this concept.

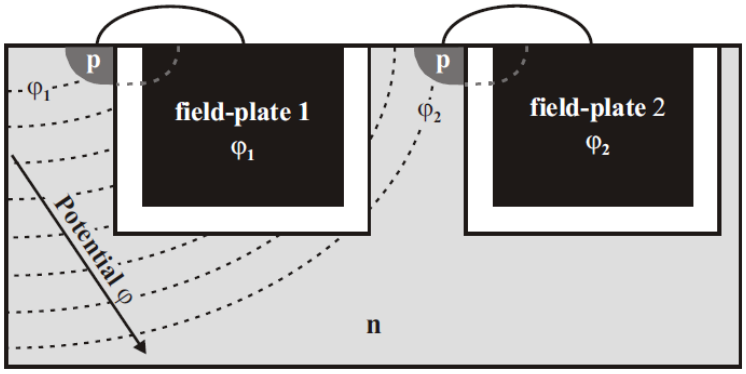


Figure 3.4. A Trench filled metal plate termination for superjunction structures [60].

Charge Imbalance Termination

A charge imbalanced based termination uses a varying P-N ratio to change the way the termination depletes out [61]. By making P column heavier than the N, the imbalance makes the N column deplete out much faster. This reduces the electric field at the surface due to the P heavy columns, and drops the voltage and field conservatively along the termination width. Figure 3.5 shows the same.

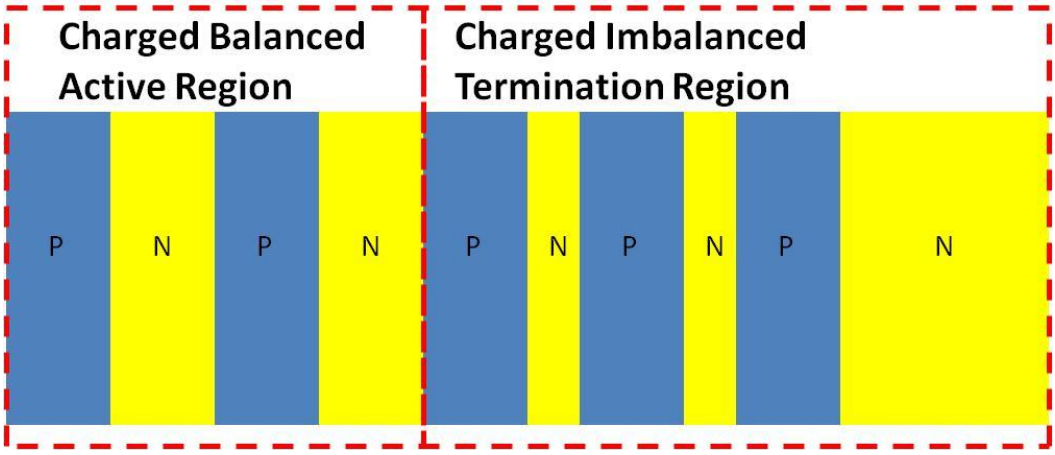


Figure 3.5. A charge imbalance based termination scheme for superjunction devices.

Edge Termination Based on Oxide Filled Trenches

There are multiple ways to implement a deep oxide filled trench based termination for a superjunction device [60], [62], [63]. The basic foundation for this termination principle is to have a trench etched as deep as the P and N columns in the active cell structure, and the electric field terminates in the oxide at the surface. But [62] is of particular interest with regards to how the trench and the P region is implemented.

Oxide filled trenches, with a P region under the trench is another commonly used structure for superjunction edge termination. The P region prevents the electric field from collapsing too early, while the oxide helps terminate the electric field at the surface. This is illustrated in Figure 3.6 [60]

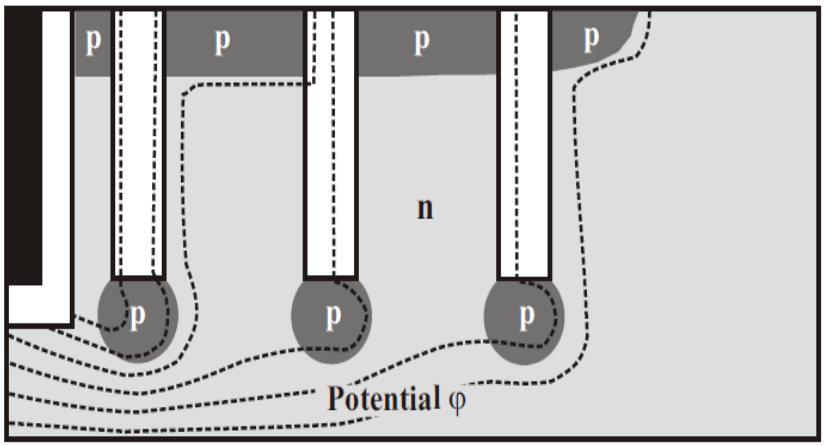


Figure 3.6. An oxide filled trench based termination scheme for superjunction devices [60].

The proposed structure is a variation of the above mentioned termination scheme. It eliminates the high electric field near silicon surface, thereby providing a more robust structure which is less susceptible to mobile charges during reliability testing, as mentioned in [64] and [65]. It fits well with the charge balanced structures presented in [41], [48] and [49], but can be also be used for planar and super junction structures.

Proposed Structure Design

The basic building block used in the proposed termination is shown in Figure. 3.7. It consists of a deep trench MOS structure with a floating P-type guard ring under the trench. A heavily doped P-type region, which typically forms the body region in the active cell, is present throughout surface of the termination region. A heavily doped N-type region, which forms part of the drift region in the active, is also present in the termination region under the heavily doped P-region at the surface. The doping concentration for the higher doped N-region is around 1e16 cm^{-3}, compared to the drift region concentration of 8e13 cm^{-3}.

The N-region typically extends to a depth of 6 µm or more. The presence of the heavily doped N-region makes it difficult to implement a conventional field limiting ring (FLR) structure, or most of the termination schemes referenced above. The complete termination structure is implemented by using several such unit cells with optimized spacing, as shown in Figure. 3.8. It is also important to note that the poly electrode for each of the termination unit cells is strapped to the adjacent inner or outer mesa using a metal. This ensures that the polysilicon electrode potential gets clamped to the silicon mesa voltage as the depletion region spreads in the termination region.

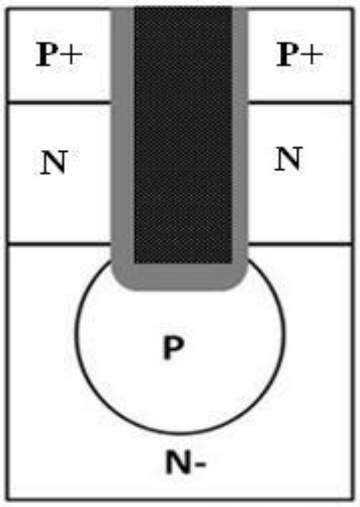


Figure 3.7. Basic building block of the proposed termination structure.

Spacing between the buried guard rings determines the voltage drop between adjacent mesas, as illustrated by the electric potential lines in Figure 3.8. Similar to conventional guard rings, the spacing will be less for unit cells closer to the active region because of the high vertical component of electric field. As we go farther and farther away from the active region, the spacing will increase to accommodate higher voltage drop between adjacent mesas. However,

the key difference in this termination technique is that the electric field transition from silicon into the trench liner oxide near the surface due to the presence of heavily doped P-body region at the top. This makes the silicon mesa of the termination surface field free with all the potential dropping in the trench oxide.

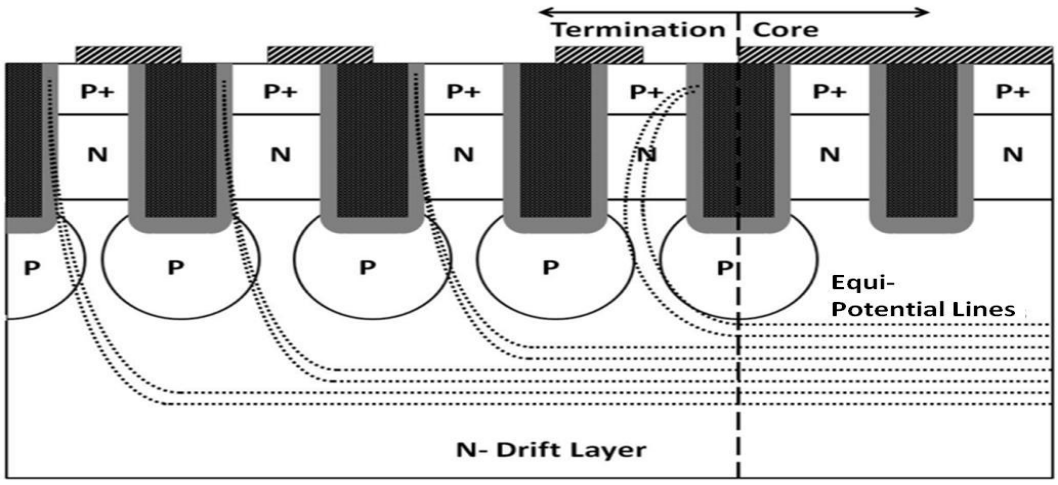


Figure 3.8. Proposed termination scheme.

Since the bulk of the electric field is supported in the trench liner oxide, the thickness of the oxide is critical in determining the maximum blocking voltage of the unit cell. The limit usually comes from the critical electric field in silicon near the oxide silicon interface. It is important to choose a buried guard ring spacing that does not drop voltage higher than what the unit cell can support.

Figure. 3.9 above shows the breakup of the electric field components along a single poly filled trench. The thicker liner oxide also makes the structure more immune to any trapped charge.

Figure 3.9(b) shows the breakdown of the electric field between the different components. Point [A] signifies the peak electric field component in the trench liner oxide, and [B] signifies the electric field strength in the silicon junction. The region between the trenches is covered by the P-base implant, so the only way the potential lines can terminate is through the trench liner oxide. Since the potential lines converge in the trench liner oxide, the peak electric field occurs in that region.

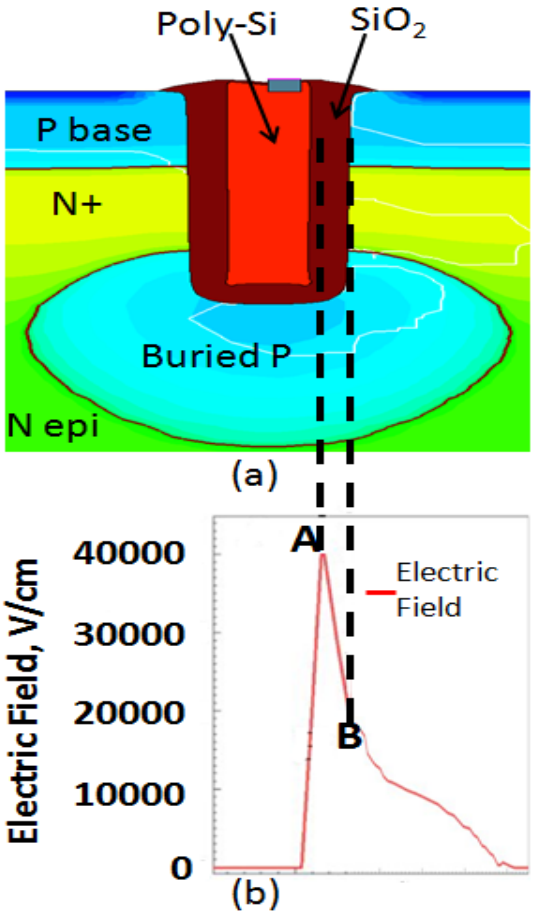


Figure 3.9. (a) Cross section of a single polysilicon filled trench and the buried guard ring, and (b) accompanying electric field.

Even though the oxide has a higher critical electric field (1×10^7 V/cm), the silicon junction breakdown voltage is what determines the overall BV since it has the lower critical electric field (3×10^5 V/cm). So the spacing has to be designed in a manner so as to not exceed that limit.

Another interesting aspect of this termination structure is the creation of several PMOS transistor connected in series from drain to source. Each PMOS transistor consists of a source formed by the outer mesa, gate by the trench poly and drain formed by the inner mesa (closer to the active). If the trench poly of a termination cell (gate of the PMOS) is connected to the inner mesa (PMOS drain), the blocking voltage of that guard ring may be limited by its field threshold voltage if it happens to be lower than the pinch-off voltage of the guard rings. If the trench poly is connected to the outer mesa (PMOS source), the blocking voltage of that guard ring is determined by its pinch-off voltage.

The drain connected trenches are useful in the initial part of the termination because that is the area which sees maximum vertical component of the electric field. Once most of the electric field is controlled, the source connected trenches help transition the rest of the electric field to the surface.

Fabrication

The main advantage of this approach is the compatibility with devices that have a similar topology. This termination scheme is designed primarily for structures like the trench fast recovery diode which was explained in the previous chapter. The only difference is the addition

of a P implant during the trench etch stage, a slight variation in the previously mentioned Step 2 of the process cycle.

Step 2B: Trench Etch+BGR Implant

In conjunction with the fabrication steps for the diode, the Buried Guard Ring implant takes place right after the trench is etched. During the PR step of the trench etch, a blanket P-type implant (typically Boron) at low energy is implanted. The existing PR enables the implant only through the trench etch and prevents any surface boron implant. The resulting structure looks as shown in Figure 3.10

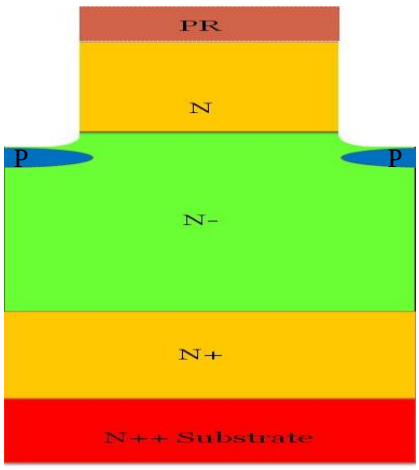


Figure 3.10. Structure illustrating the addition of P implant during the trench etch phase.

Beyond this point, the rest of the fabrications steps are exactly the same as followed for the diode fabrication, with the only except being the presence of an additional buried P implant in the final structure. The diffused structure following the thermal drive is shown in Figure 3.11.

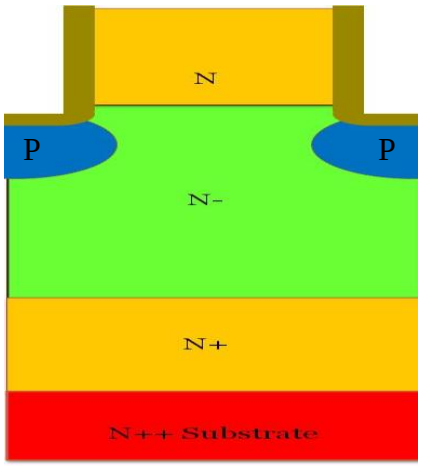


Figure 3.11. Final structure of termination unit cell after thermal drive.

The thermal drive diffuses the implanted P dose wider and deeper to form the buried guard ring, while at the same time forming the trench liner oxide required for the charge balance, Care must be taken to use the right dose and energy. Since the implant is done prior to the liner oxide growth, some of the silicon will be consumed to form the oxide, which will include the P type dopant implanted. If the dose is too low, then the percentage of dopant lost during the oxide growth is higher. The same theory applies to the implant energy. Too low an energy will implant the P shallower than needed, causing boron loss.

The different process steps involved in the fabrication all play a vital role in the termination efficiency. While the structure is designed in a way to have as wide a margin as possible to ensure against all the various process variations, a few process parameters play a much wider role the others.

Process Variations

A critical factor controlling the BV is the dose of the buried P-ring. A heavier doping of the buried P-ring will ensure a lower pinch-off voltage with low electric field at the trench bottom similar to a guard ring. A lighter doping of the buried P-layer will cause higher electric field near the trench bottom due to depletion of the buried P-layer, similar to a JTE. In either case, adjustment of the mesa widths/guard ring spacing can be used to optimize the breakdown voltage.

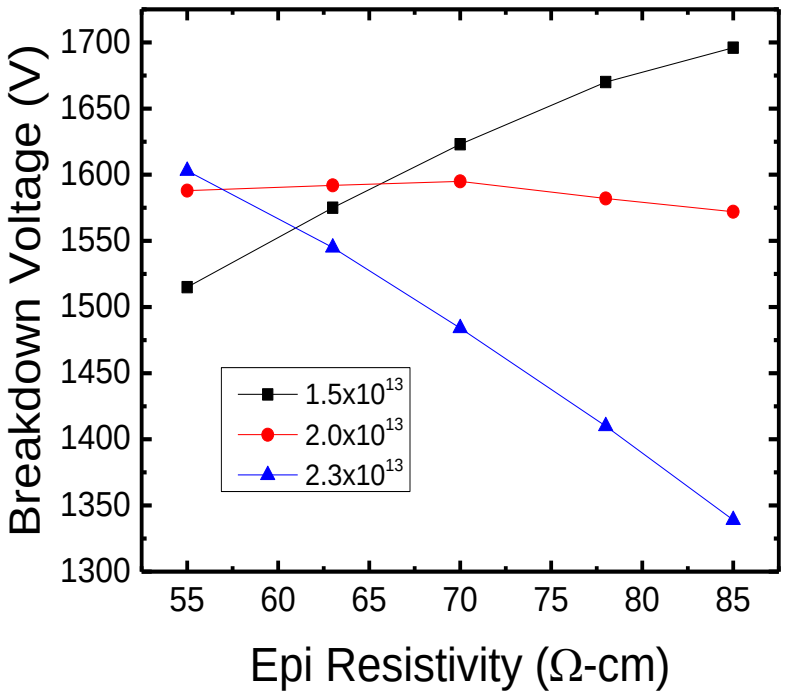


Figure 3.12. Breakdown voltage versus epi resistivity for different p-doping concentrations.

Other factors affecting the termination breakdown voltage is the resistivity of the drift epi. For a given buried P-ring dose, the resistivity determines the lateral spread of the P-ring, controlling the amount of pinch-off between the trenches, and hence, the pinch-off voltage. Figure 3.12

shows the variation of BV for different combinations of the buried P-ring and drift resistivity for a given trench depth of 6 µm.

Another important factor that impacts the termination design is the trench depth. For a given drift resistivity (70 Ω-cm), variation in BV for different combinations of the buried P-ring dose and trench depth are shown in Figure 3.13. Trench depth affects the charge balance of the device, so changes in the trench depth would alter the net charge balance combined with the buried P-ring and dose and resistivity. The breakdown threshold for the source connected trench is much lower, so the spacing has to be conservative initially while increasing outward to balance the remaining electric field.

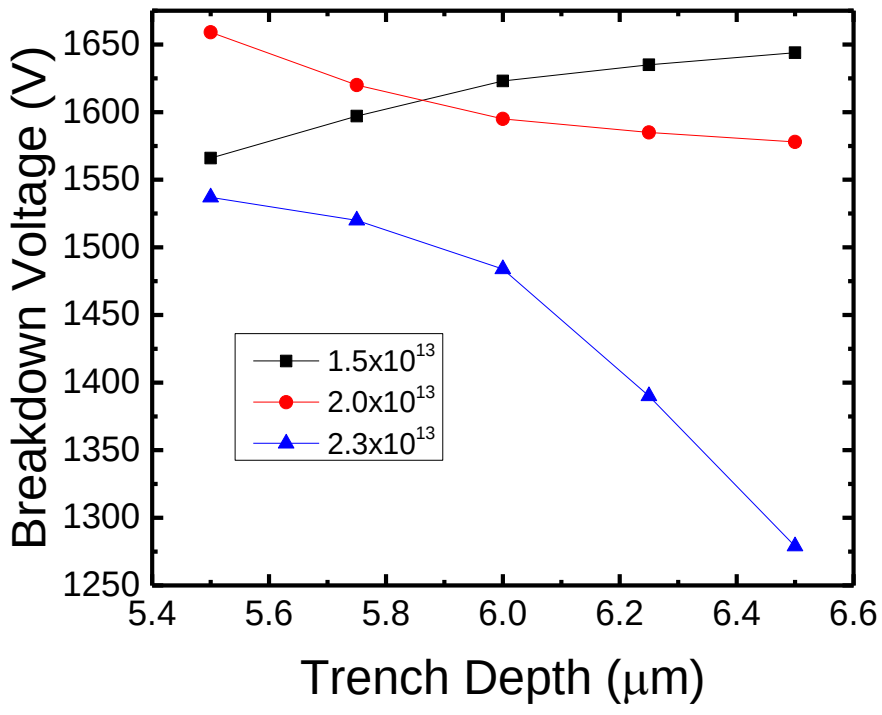


Figure 3.13. Breakdown voltage versus trench depth for different p-doping concentrations.

Design Features

As discussed previously, a significant advantage of this termination structure over a traditional guard ring structure is its robustness against influence of mobile ions during high temperature reverse bias. Since the silicon junction interface in the proposed structure occurs deeper in the silicon, the presence of mobile ions induces a negligible shift in the breakdown voltage.

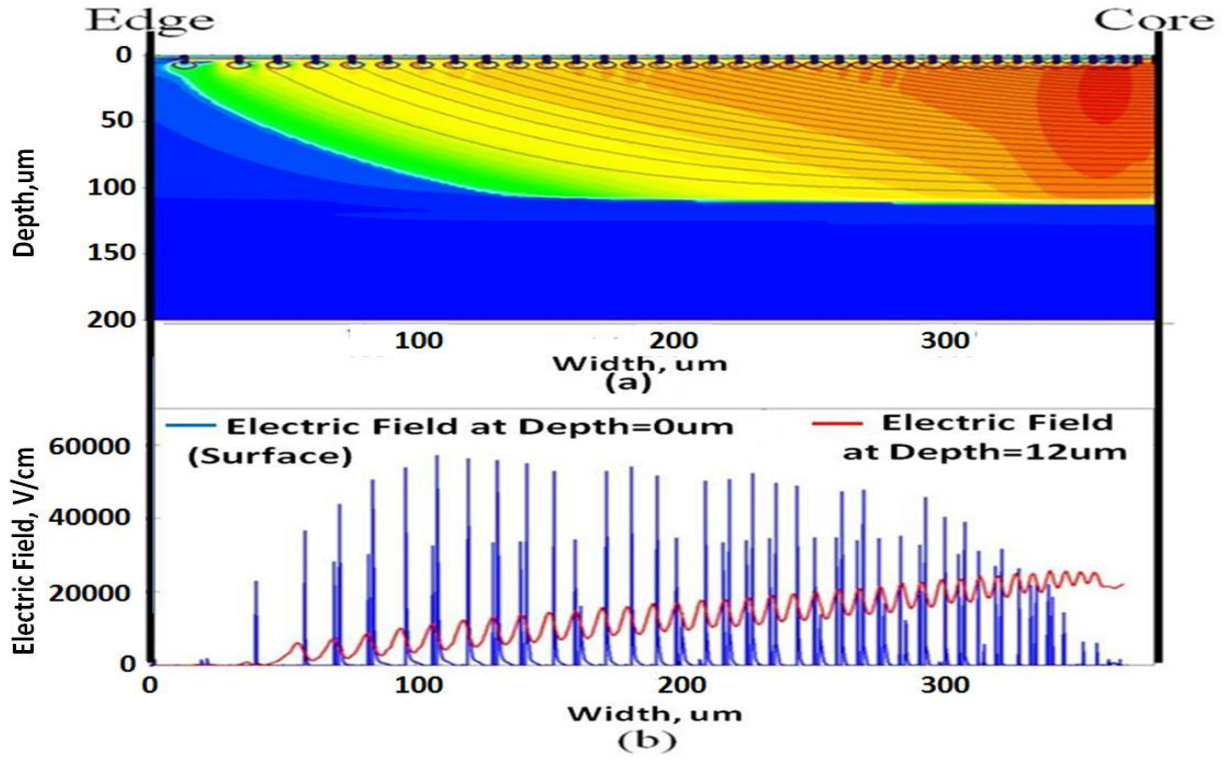


Figure 3.14. Different characteristics of the termination scheme are shown. (a) full termination with location of impact ionization hot spot and (b) distribution of the electric field.

In Figure 3.14(a) a termination design blocking 1350V is shown along with the location of the impact ionization hotspot. Figure 3.14(b) shows the electric field both at the surface, and below the buried guard ring (BGR) implant. It should be noted that the active area is to the right of the

termination scheme shown. The impact ionization spot is where the peak electric field in silicon occurs, can be observed to be deep inside the silicon bulk. The peak electric field at the surface occurs in the oxide as mentioned earlier. The critical E-field in silicon dioxide (1×10^7 V/cm) is higher than the critical E-field in silicon (3×10^5 V/cm). The maximum E-fields observed in the oxide and silicon in the scheme are both within the acceptable theoretical limits.

All of the above data and discussion serve to underline the impact of this termination scheme on the reliability of the structure. Figure 3.15 shows two different termination structures: a) a regular planar guard ring termination; and b) a trench based structure. The guard ring in Figure 3.15(a) terminates the electric potential lines at the Silicon surface, while the trench in Figure 3.15(b) has the potential lines converge in the liner oxide. This causes the peak electric field to occur at the edge of the guard ring for a planar termination, which the peak electric field for the trench based structure occurs in the oxide.

For the guard ring structure, since the peak electric field limit in silicon is 3×10^5 V/cm, this makes the termination more susceptible to increased leakage at high temperature. Under reliability testing conditions like high temperature reverse bias (HTRB), this leakage worsens over time. In contrast, the trench FRD supports most of the electric field in the liner oxide, which has much higher threshold for the peak electric field (1×10^7 V/cm). This makes it immune to surface charge, and hence more reliable.

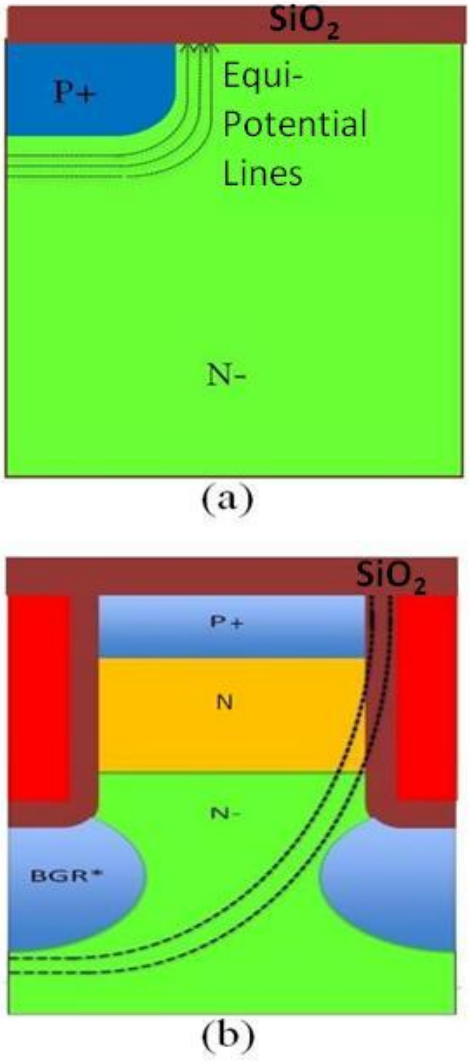


Figure 3.15. Comparison of the termination schemes and the shape of the electric potential lines for (a) planar FLR, and (b) trench structure.

The impact of parasitic charge in the termination is studied in detail in [66]. The buried guard ring in the proposed structure by virtue of its position is pretty immune to the effects mentioned in [39]. The impact of surface charge on the breakdown voltage of trench based termination and planar FLR termination has been simulated. The results are shown in Figure 3.16. Both

termination schemes have a width of ~370μm. As seen in Figure 3.16 the breakdown voltage of planar FLR termination decreases when the trapped charge increases, while the breakdown voltage of trench based termination is relatively insensitive to trapped charge.

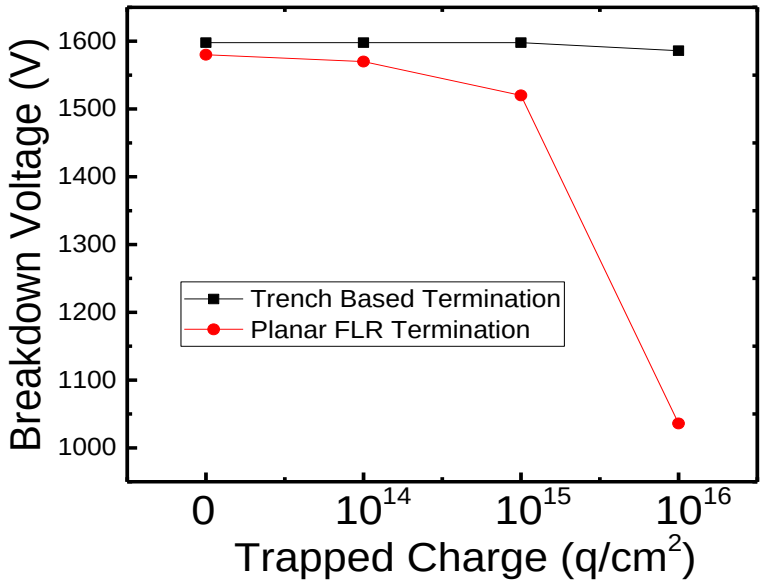


Figure 3.16. Breakdown voltage as a function of trapped oxide charge.

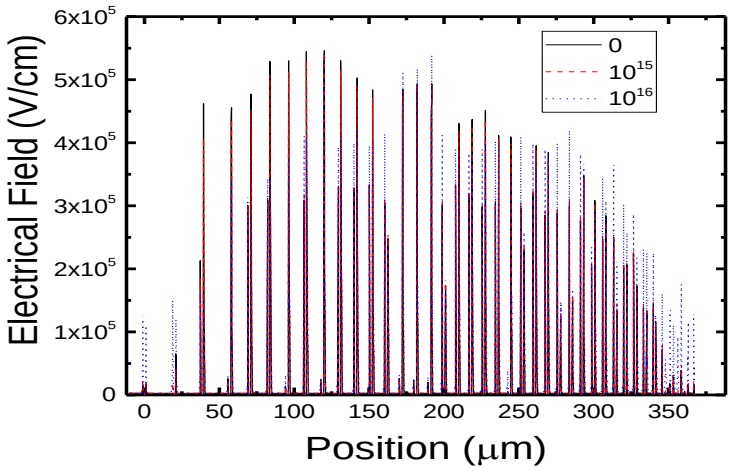


Figure 3.17. Effect of trapped oxide charge on the electric field distribution lines for the proposed trench based termination.

Figure 3.17 shows the effect of the trapped charge on the electric field distribution in the silicon at the surface in the proposed trench termination. In trench based termination the electric field does not vary much with increasing interface charge. Due to the depth of the buried guard ring, the effect of the trapped charge is greatly minimized. The electric field is well below the critical field on silicon dioxide (1×10^{7} V/cm

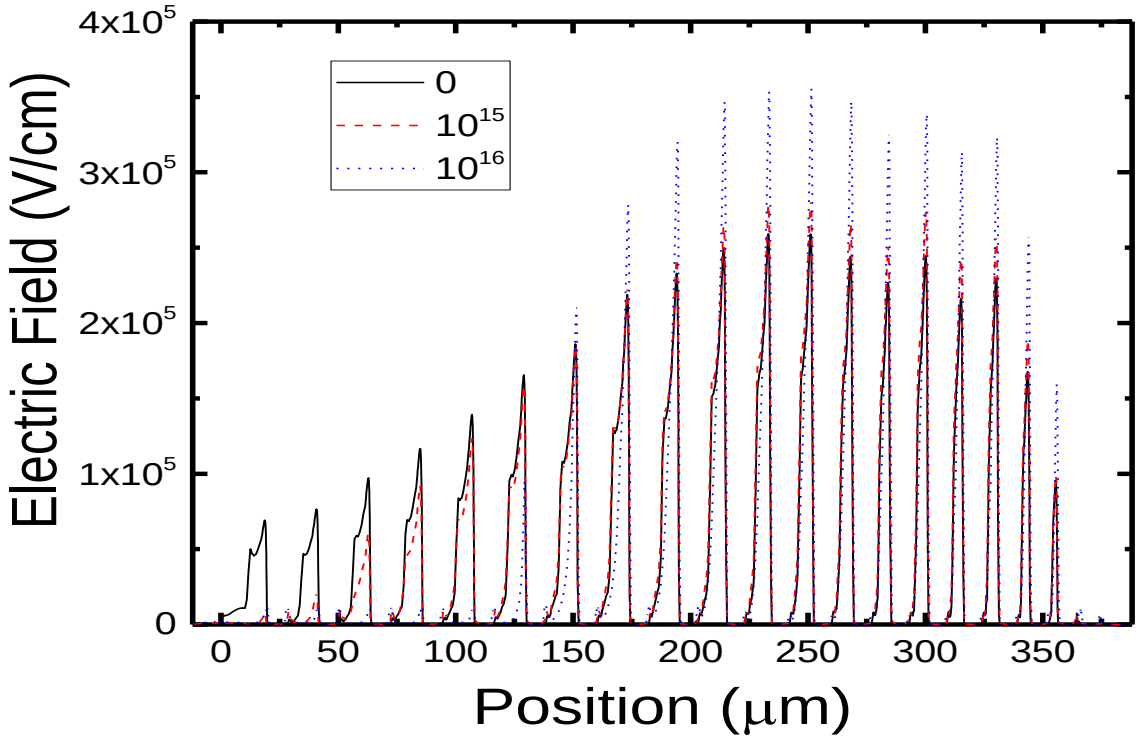


Figure 3.18. Effect of trapped oxide charge on the electric field distribution lines for a planar FLR based termination.

Figure 3.18 shows the effect of the trapped electric charge on the electric field distribution at the surface in a regular FLR termination applied to a planar structure. As shown in this figure, the effect of the trapped charge is more severe in this scenario due to the peak silicon E-field

occurring at the surface. The higher interface charge leads to the field rising above 3×10^5 V/cm, which causes a drop in the breakdown voltage

Results and Discussion

The proposed termination structure was implemented in silicon for a 1350 V FRD and the resulting breakdown voltage met the blocking voltage requirements. In our design the trench depth is 6 μm, the trench width is 2.5 μm, linear oxide thickness is 6700 Å, the total epi thickness is 120 μm, and the total termination width is 380 μm. Assuming a 20% BV margin, we are able to achieve a breakdown voltage of 1640 V against a parallel plane breakdown voltage of 1675 V. That realizes a 98% efficiency for high voltage termination.

The HTRB reliability data for planar and trench based terminations are compared after high temperature stress (150 ºC) for 1000 hours over a wide range of 80 samples. The bias voltage for the HTRB test is 1350V. As seen in Figures 3.19 and 3.20, the leakage current increases significantly for the planar termination after high temperature stress, while the leakage current does not change much for the trench based termination after HTRB. The proposed termination structure also passed all reliability tests stress condition set by the limit of 10^{-5} A, while a few data points of planar termination jump beyond 10^{-5} A after high temperature stress for 1000 hours. The leakage current is measured at 1350V.

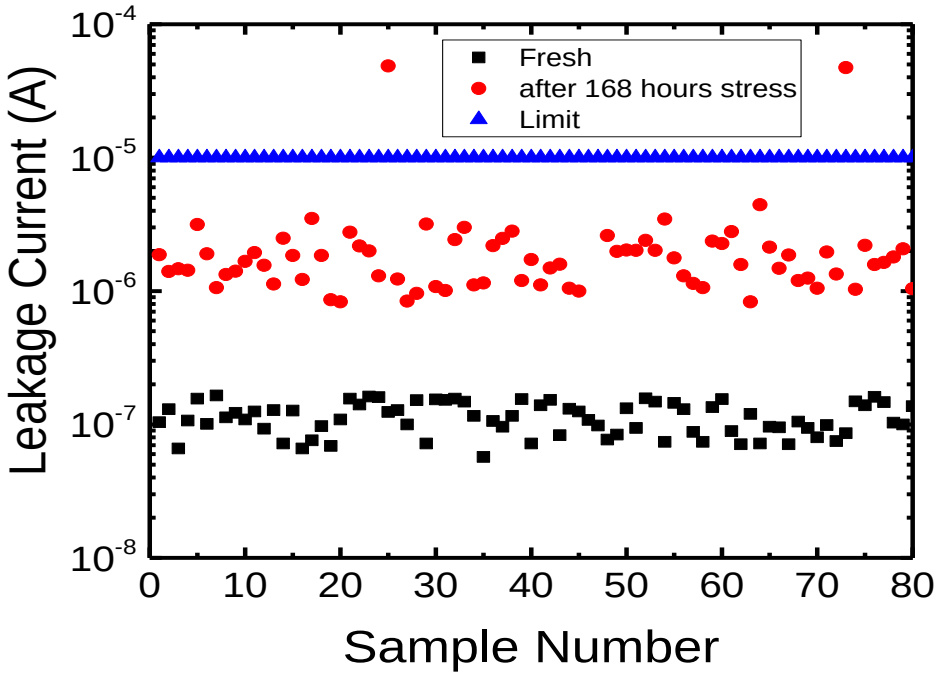


Figure 3.19. Leakage current reliability data for planar termination.

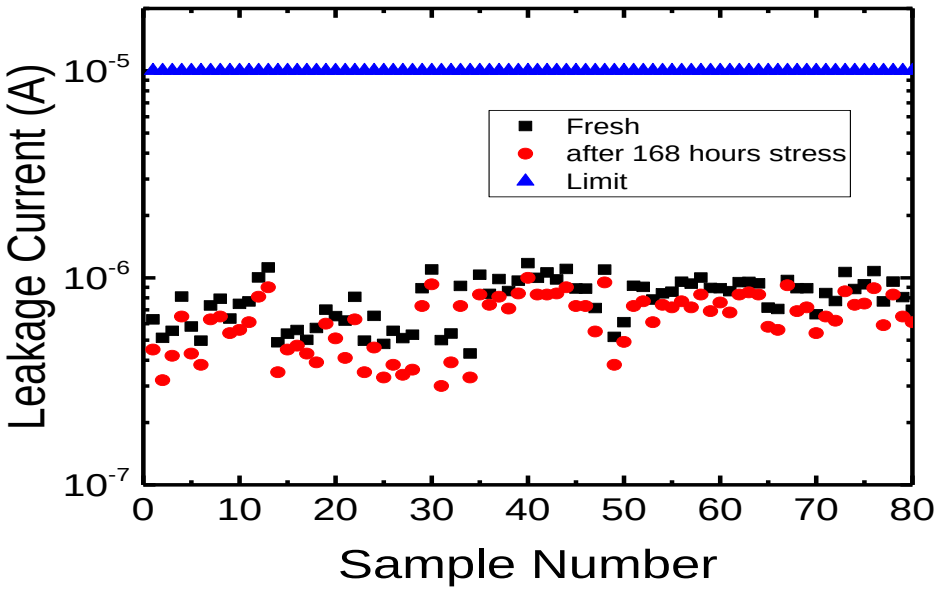


Figure 3.20. Leakage current reliability data for trench based termination.

Conclusion

This brief shows a novel termination scheme based on a trench and a buried p-ring to implement a robust termination structure for high voltage devices. This termination shows good ruggedness with regards to high temperature leakage current reliability.

The present work deals only with a high voltage rating of 1350V, but the scheme can be applied for all voltage ratings >400V. We can also extend this concept to a full superjunction structure by just extending the topside heavier N-region deeper into the silicon while simultaneously adding more P- rings to charge balance the N.

CHAPTER 4
SUPERJUNCTION MOSFET RUGGEDNESS

Introduction

Given the huge emphasis on overall system efficiency as discussed earlier, there is a need for the system components to operate more efficiently, especially at higher power ratings. For this reason, super junction MOSFETs are widely used in power supplies today. The basic concept of the SJ MOSFET, and the design and modeling principles behind it are explained in [67]-[71]. These devices can achieve a significant reduction in conduction and switching losses compared to a planar DMOSFET. This fundamental improvement of 4x to 8x in the MOSFET specific on resistance comes from the replacement of the lightly doped drift region of a DMOSFET with alternating P and N columns to achieve charge balance, which in turn de-couples the drift region doping from the Breakdown Voltage.

The performance of SJ MOSFETs in power supply system applications are described in [72] and [73]. However, a key requirement for power MOSFETs used in circuits such as the power factor correction (PFC) and Flyback converter is its Unclamped Inductive load Switching (UIS) robustness [74]. During hard switched turn-off, the energy stored in stray inductances causes voltage overshoot and causes the power MOSFET to undergo avalanche breakdown and conduct current in order to dissipate the inductor stored energy. If the MOSFET is not optimized to withstand this energy dissipation, it will result in the MOSFET failing. This failure, as explained earlier, can be characterized as active or passive failure.

In this chapter, we analyze the UIS performance of a super junction structure and explain the impact of adding a P column in the drift region for charge balance on the avalanche robustness. We also look at design optimization for superior UIS performance of a super junction MOSFET.

Prior Art

The theory of MOSFET ruggedness, and specifically the UIS characteristic of the MOSFET, has been explained previously, but how the theory applies to superjunction MOSFETs is a relatively new area of study. In [75], the basic concept behind the UIS failure and the mechanism that controls it is explained, and in [76], a numerical model to quantify it is proposed. While these apply primarily for a planar MOSFET, the core concept of UIS failure can be extended to a superjunction MOSFET. In [77]-[79], the MOSFET UIS capability and the effect of the charge imbalance in superjunction MOSFETs is studied. The above mentioned references clearly show the inherent weakness of the superjunction MOSFET stricture with regards to UIS capability, and show that with the help of the switching waveforms. This chapter seeks to explain the theory with the help of avalanche snapback curves.

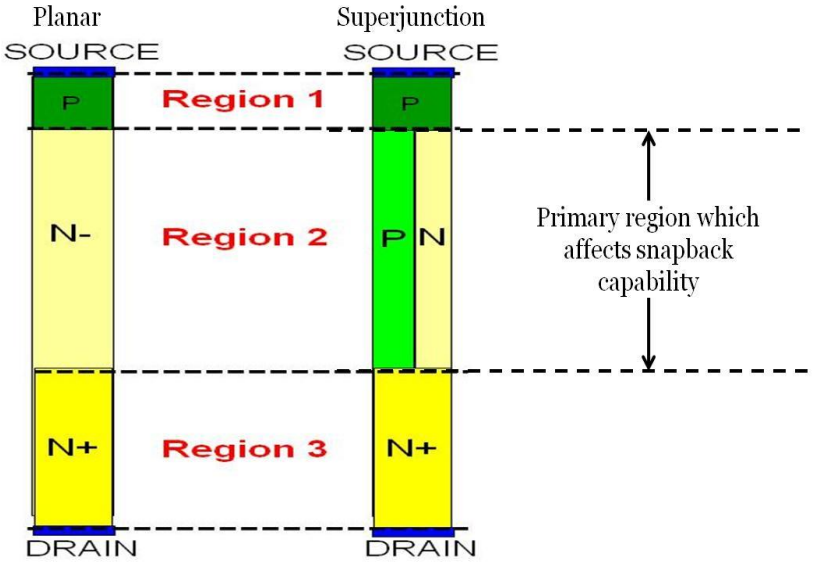


Figure 4.1. Simulated body diode core cells of a planar DMOSFET and a superjunction MOSFET.

Figure 4.1 shows the core cell structure of a planar DMOSFET (a) and a super-junction FET (b). In order to simplify the simulation and analysis, only the body diode portion of the core cell structure was simulated. The MOS gate and source were removed from the simulation structure since they do not play a significant role in the UIS failure mechanism.

The drift region doping for the planar DMOSFET body diode structure was 2.5e14 and the thickness was 37um. For the superjunction body diode structure, a pitch of 11um with an equal P and N column width of 5.5um and a doping of 1.5e15 each were used. The total thickness of the drift region was 35um.

Figure 4.2 shows the simulated breakdown curves for the two structures. It can be observed that the planar DMOS body diode structure shows a positive dynamic resistance (R_{DYN}) in the IV curve after avalanche breakdown before eventually snapping back to low voltages. This region plays an important role in the avalanche robustness of the device. It facilitates the spreading of avalanche current throughout the device active area.

On the other hand, a positive R_{DYN} is absent in the IV curve of the superjunction body diode cell. As a result, the device forms current filaments after avalanche breakdown and undergoes destructive failure. This explains why perfectly charge balanced superjunction devices are inherent weak in UIS.

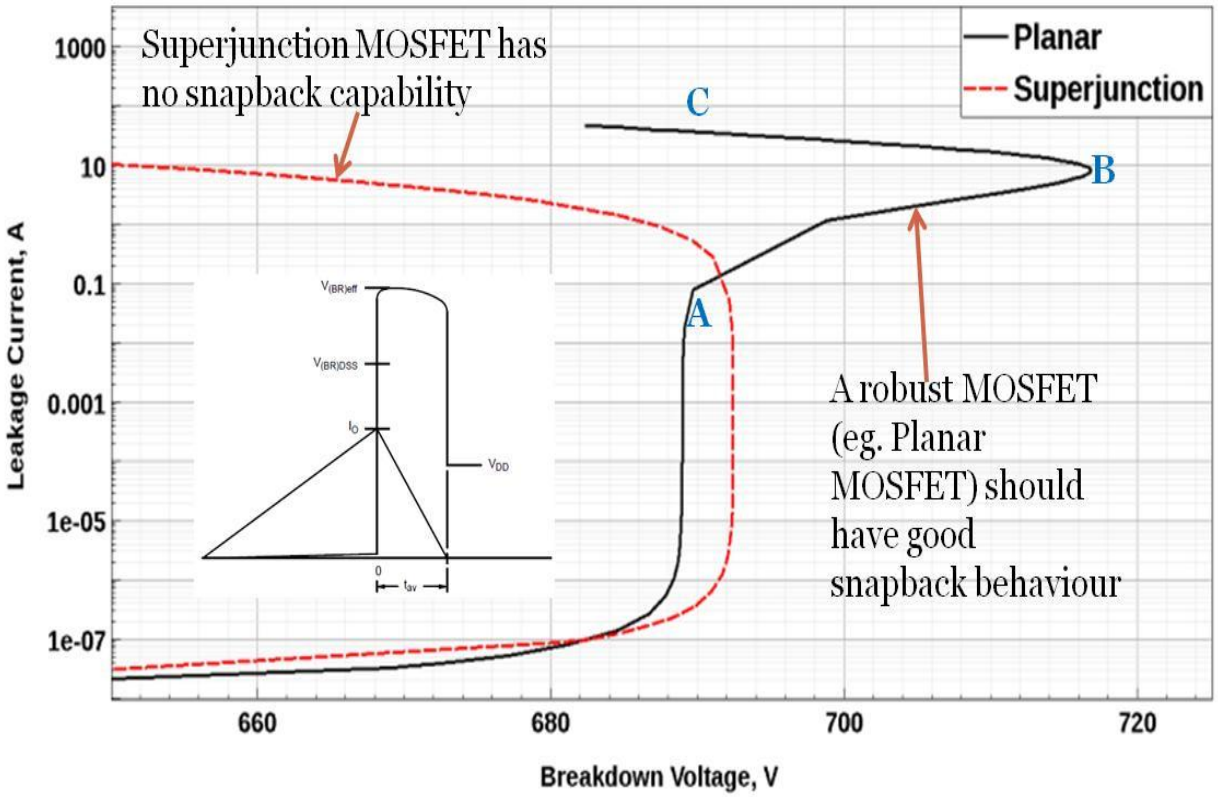
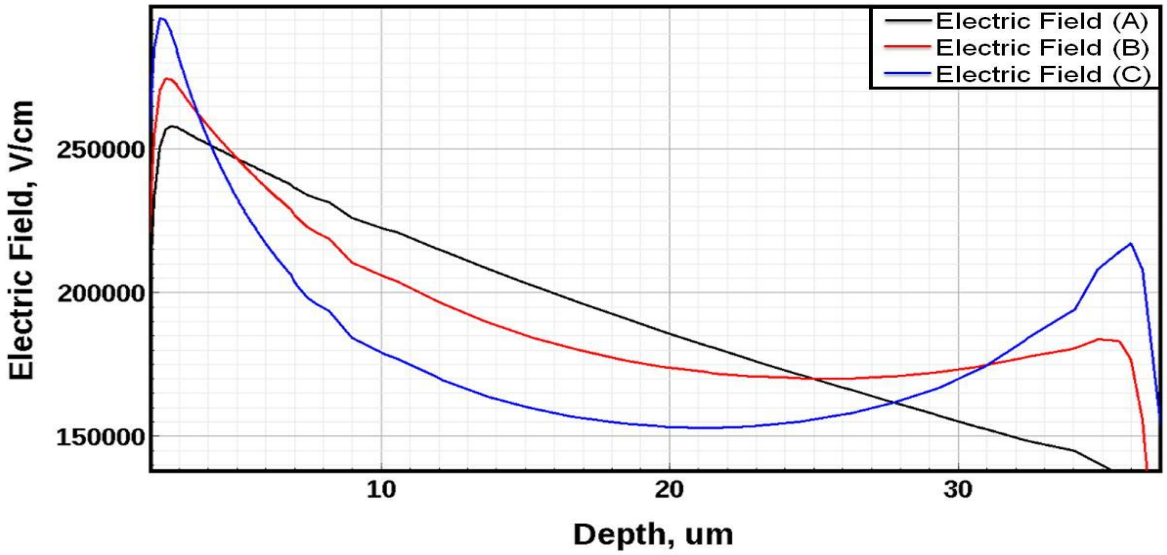
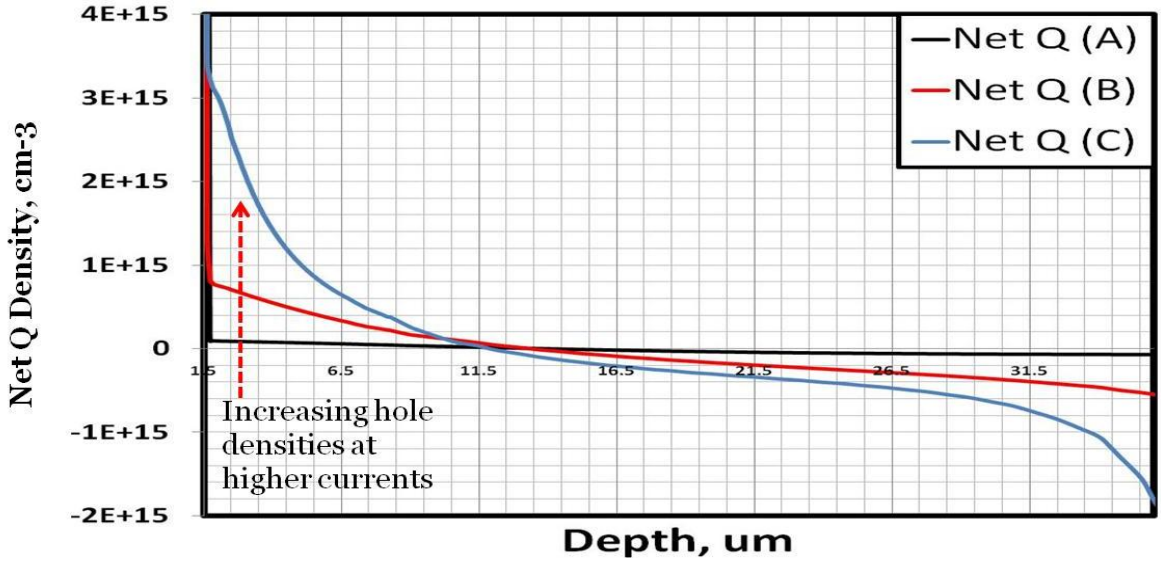


Figure 4.2. Simulated Breakdown Voltage I-V curve comparison between planar and superjunction MOSFET.

In order to explain the difference in the breakdown IV curves of the two structures, the drift region electric field and total charge is analyzed at 3 different current level, marked A,B, and C in the I-V curve shown in Figure 4.2. Figure 4.3 shows (a) the electric field, and (b) the net charge in the drift region as a function of depth for the planar structure.



(a)



(b)

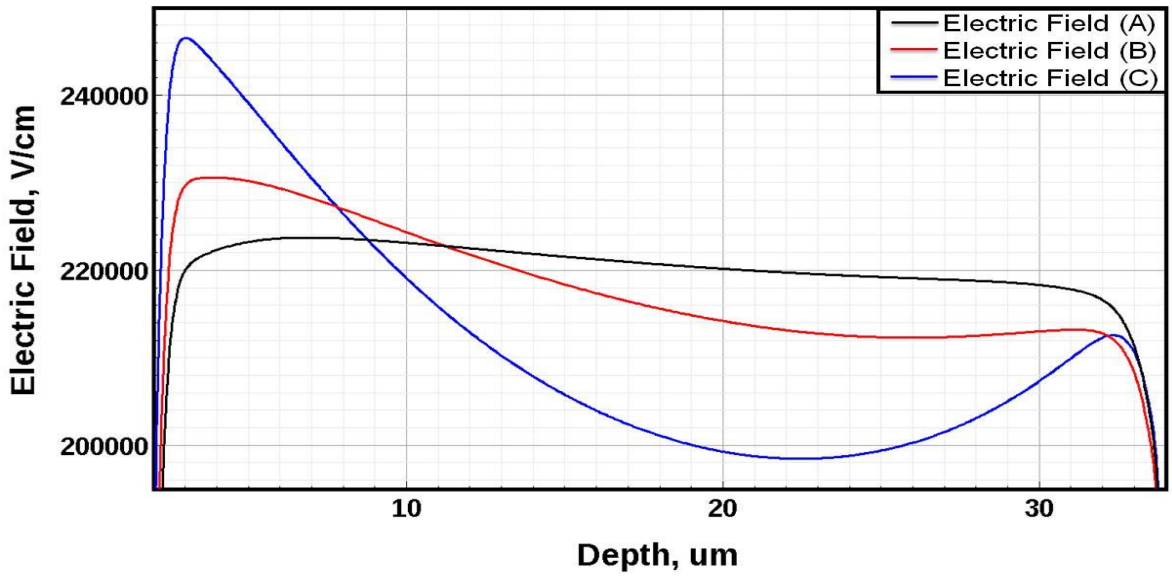
Figure 4.3. Comparing the (a) electric fields and (b) net charge distribution for the planar MOSFET.

At the onset of avalanche, the electric field has a trapezoidal shape with a slope proportional the doping concentration in the drift region. The net charge in the drift region is a straight line matching the doping concentration in the drift region. However, as the current level during avalanche increases, the net charge in the drift region shift from a straight line to sloped, due to build up of electrons near the bottom drain electrode and holes near the topside source. This causes the electric field to peak near the two corners of the drift region. This reduced the slope of the electric field which in turn enables the drift region to block more voltage. So, current flow during avalanche allows the sub optimal electric field in a planar DMOS to improve and the extra voltage blocking capability adds the positive R_{DYN} in the breakdown I-V curve. At very high current level however, a significant build up of free carrier near the top and bottom of the drift region collapses the electric field in the middle of the drift region, thereby causing snapback in the I-V curve.

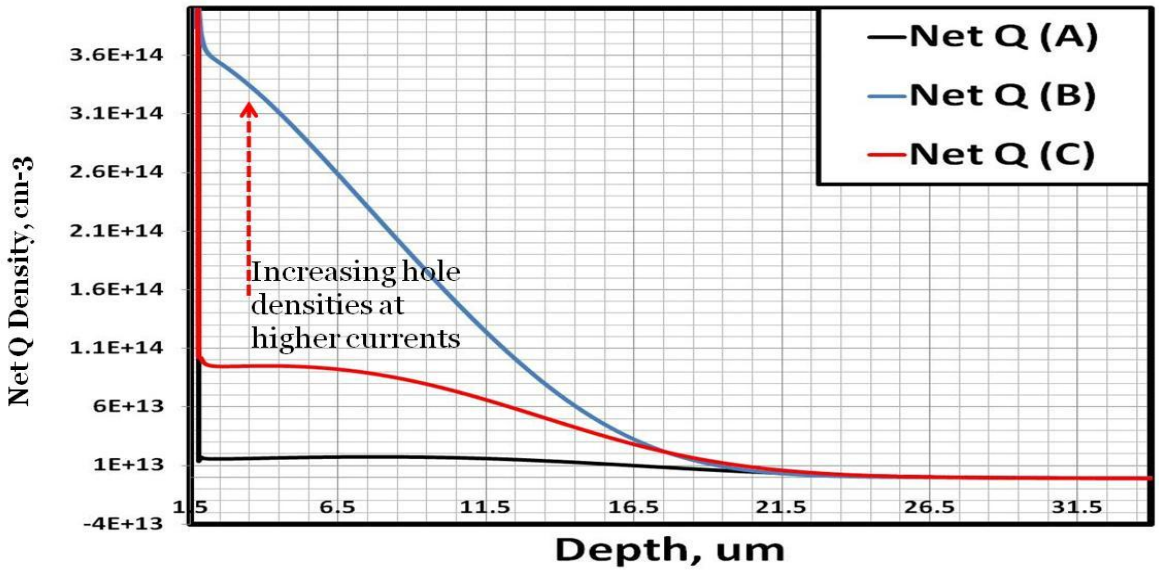
In case of the super junction body diode, the situation is quite different. This device has the ideal rectangular electric field at the onset of avalanche breakdown, as can been seen in Figure 4.4a. This happens because the net charge in the drift region is almost zero as shown in Figure 4.4b. The net charge in case of super junction is obtained by integrating the charge along a horizontal cutline through the device cross section.

Since the superjunction already has optimum rectangular electric field, it is already blocking the maximum possible voltage it can at avalanche. This implies that it is impossible to achieve a positive R_{DYN} characteristic in the breakdown I-V curve and any electric field distortion in the

drift region due to mobile carrier build up can only reduce the blocking voltage. As observed from the net charge and electric field profiles at high current, a hole build up at the top junction and electron build up at the bottom electrode causes the electric field to peak at the edges of the drift region, thereby causing snap-back at higher currents.



(a)



(b)

Figure 4.4. Comparing the (a) electric fields and (b) net charge distribution for the SJ MOSFET.

Superjunction MOSFET Design for Improved UIS

From the discussion in previous section, it should be clear that an optimized epi design with rectangular cannot be practically used to make super junction transistor. In order to make the device achieve robust UIS, it is necessary to distort the electric field a little bit, to allow the device to block more voltage during current flow and achieve a positive R_{DYN} in the breakdown I-V curve

The easiest way to distort the electric field is to change the charge balance in the structure. Foe example, by varying the P column charge, we can alter the electric field because the peak electric field now matches the point where impact ionization now occurs in the MOSFET. The resulting electric field profiles and carrier densities at the onset of avalanche can be seen in Figures 4.5 and 4.6 respectively.

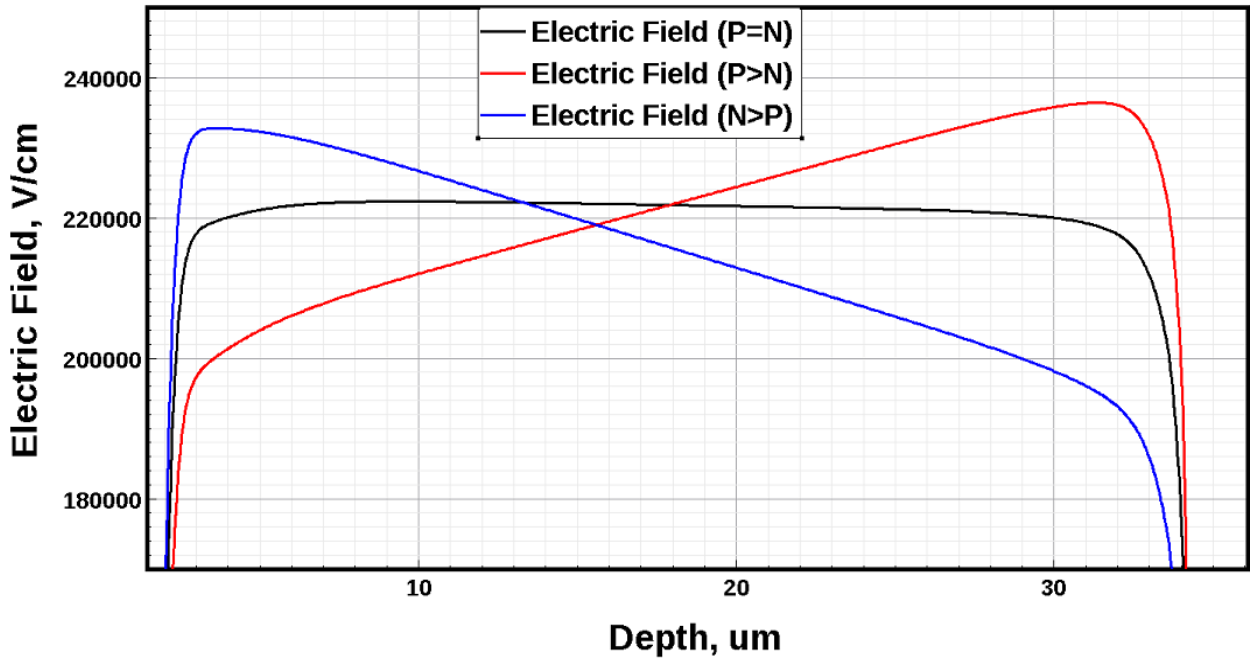


Figure 4.5. Effect of charge imbalance on the electric field profile.

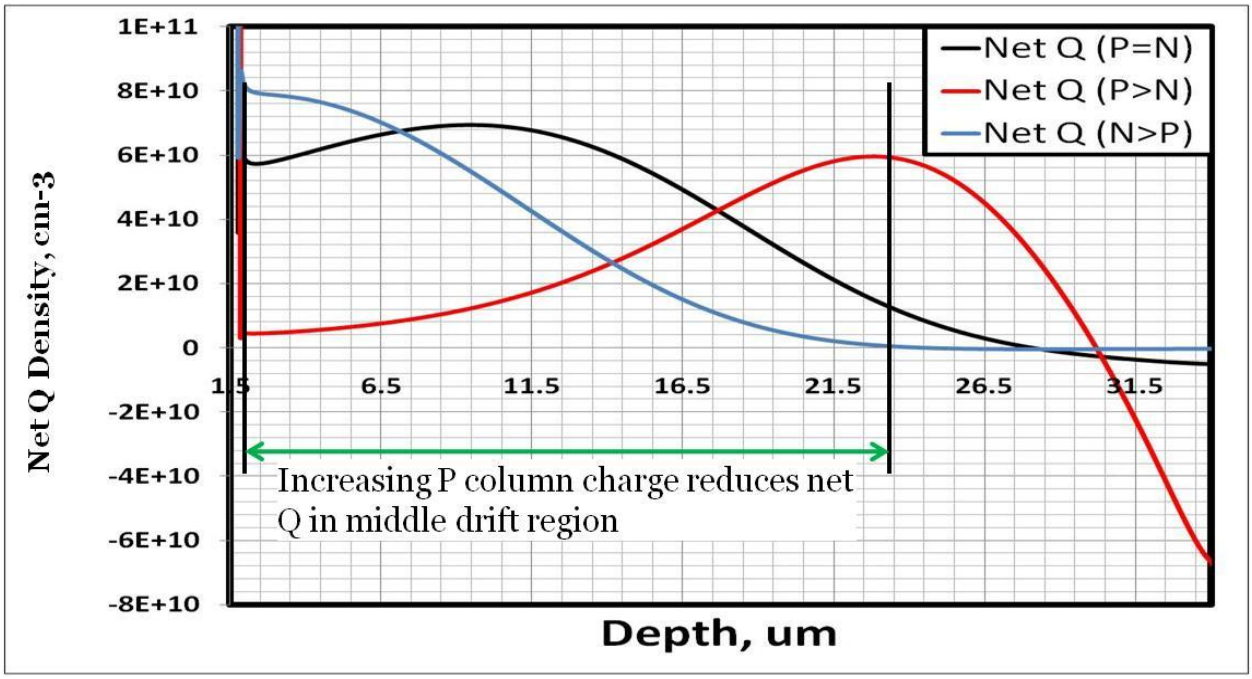


Figure 4.6. Effect of charge imbalance on the net charge density.

As seen in the previous figures, increasing the P column charge shifts the net carrier charge density deeper into the silicon toward the bottom of the P column at the drain, greatly reducing the amount of charge in the epi region which controls the $R_{DYN.}$ It also minimizes the amount of carrier at the surface closer to the emitter side, which delays the parasitic BJT from getting engaged.

Reducing the P column charge has the opposite effect. With an N heavy structure, the impact ionization point now shifts closer to the P-N junction close to the source. The amount of carriers in the drift region increases drastically, thereby reducing the R_{DYN} even further. The effect of the charge imbalance on the BV snapback curves is illustrated in Figure. 4.7

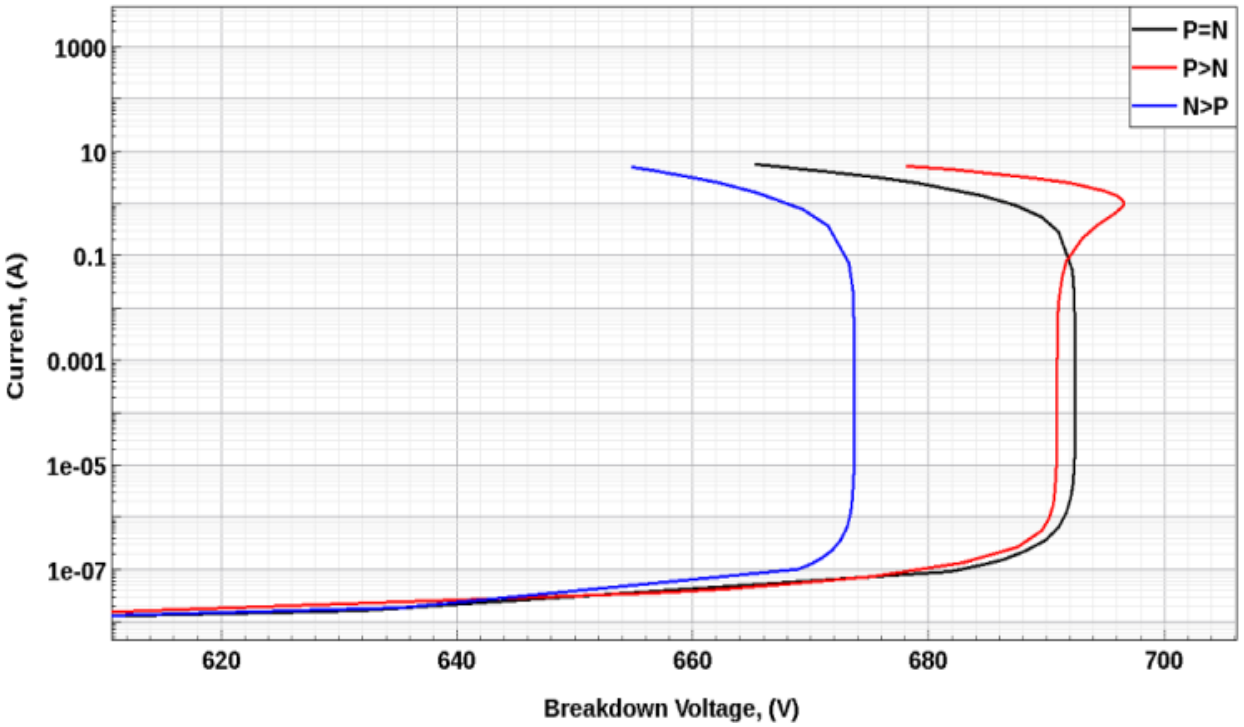


Figure 4.7. Effect of charge imbalance on the BV snapback curves.

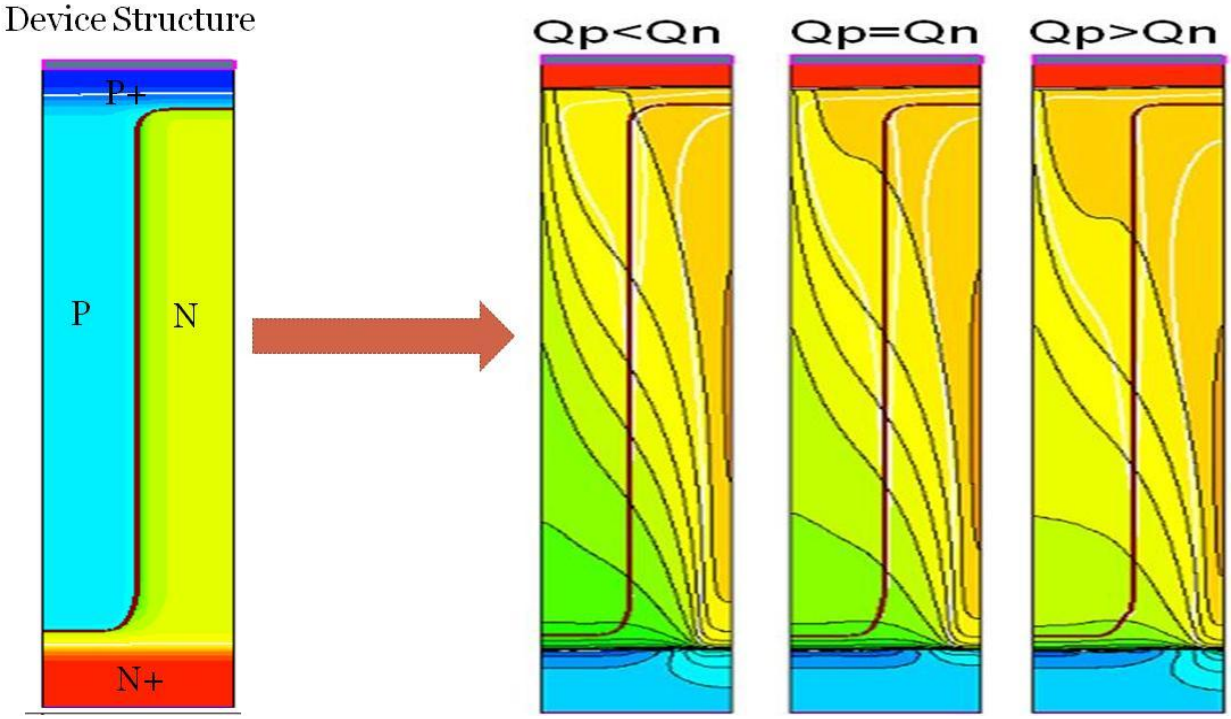


Figure 4.8. Effect of charge imbalance on the current flow density.

The difference in the UIS capability can be further explained using the current flow density lines as shown in Figure 4.8. The P heavy device has reduced current density at the P+/N junction at the source, greatly reducing the chance for any bipolar latch-up at his junction. leading to improved UIS capability, while the equally balanced and N heavy device have increased current density at the same junction.

P Heavy Structure

The effect of the P heavy structure can further be explained by analyzing the device characteristics at the previous mentioned current levels(A, B and C) along the BV snapback curve. At the onset of avalanche, due to the extra P charge, the carrier build-up at the base of the P column leads to a distorted electric field. Since this is not an ideal electric field, increasing the current level starts changing the electric field back towards an optimal profile, which corresponds with current level B on the curve. The device has a positive R_{DYN} upto this point.

As the current level increases further, there is no further optimization of the electric field. It assumes a trapezoidal shape and the accumulation of carriers at the two electrodes causes the field to spike. The build up of carriers at the ends eventually causes thermal runaway and failure of the device. Figure 4.9 shows the different electric field profiles at the different current levels, and Figure 4.10 shows the net charge distribution for the same.

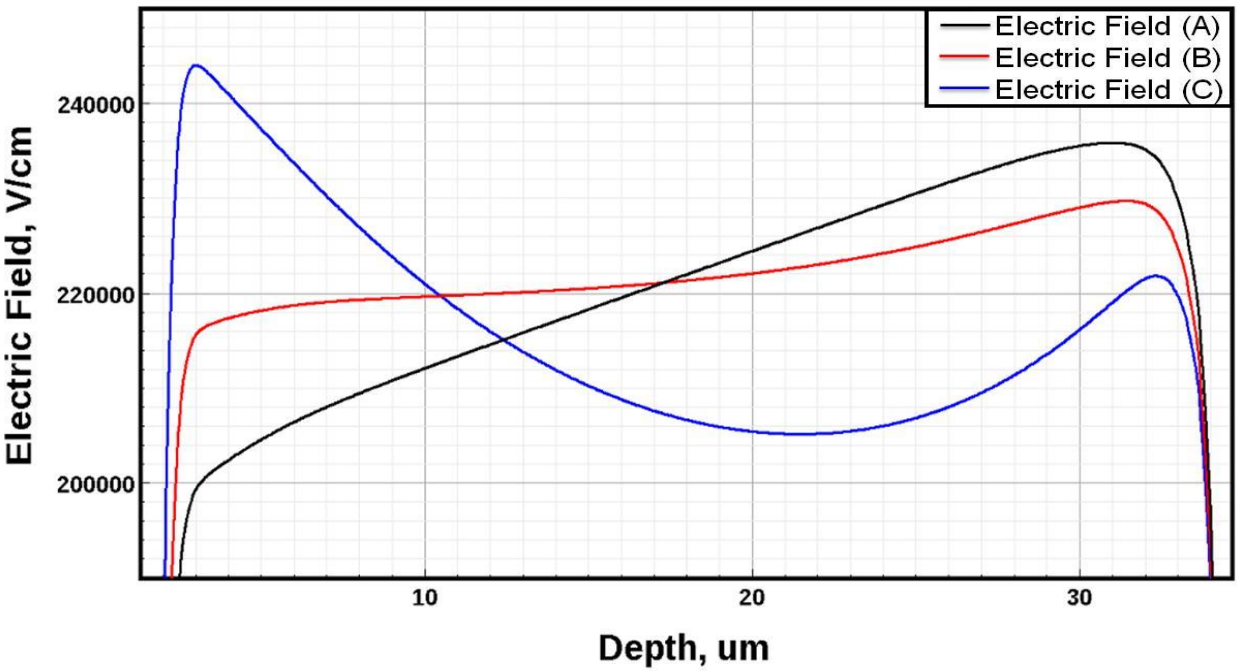


Figure 4.9. Electric field profiles for a P heavy SJ MOSFET at different points on the BV snapback curve.

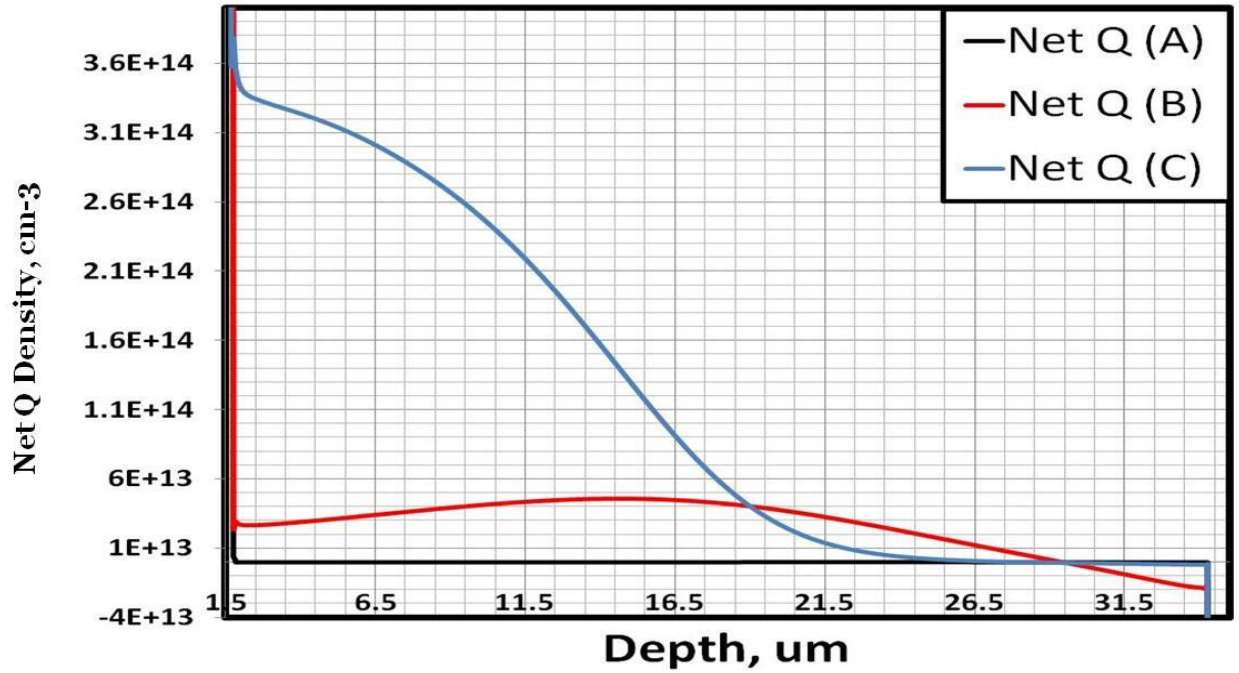


Figure 4.10. Net charge density distribution profiles for a P heavy SJ MOSFET at different points on the BV snapback curve.

N Heavy Structure

On the other hand, an N heavy structure has the opposite effect, but only upto a certain charge balance point. As the device starts becoming N heavy, the impact ionization point is pushed up close to the P+/N junction close to the source electrode. While in a charge balanced structure the peak charge density occurs deeper in Silicon away from the surface, an n-heavy structure causes the carrier profile to shift closer to the P/N junction close to the surface. This automatically increases the parasitic BJT latch-up at avalanche. The electric field too starts assuming an increasingly trapezoidal shape, diminishing any positive dynamic R_{DYN} the device. This causes current filamentation in the MOSFET and snapback as the current keeps increasing.

This behaviour however changes as the N column charge keeps increasing. While the electric field is pretty much trapezoidal, and even though the peak carrier concentration has shifted closer to the surface, further increase in the N column charge starts diminishing the carrier density at the surface and deeper into silicon. This reduces the latch-up probability in the MOSFET, and again increases the positive R_{DYN}. So despite having a non-ideal, trapezoidal electric field, the device has a positive R_{DYN}. At this point, the carrier and electric field profiles resemble that of a planar MOSFET. The net charge densities for the different stages of imbalance are in Figure 4.11, and the corresponding avalanche breakdown curves are shown in Figure 4.12.

So now, we have two different methods of introducing UIS capability for a SJ MOSFET

- Increase P column charge - Shifts electric field deeper, inducing a positive R_{DYN} positive resulting in UIS capability.

- Increase N column charge – Sufficiently heavy N column charge greatly reduces the net carrier charge in the drift region, again resulting in .a positive R_{DYN}.

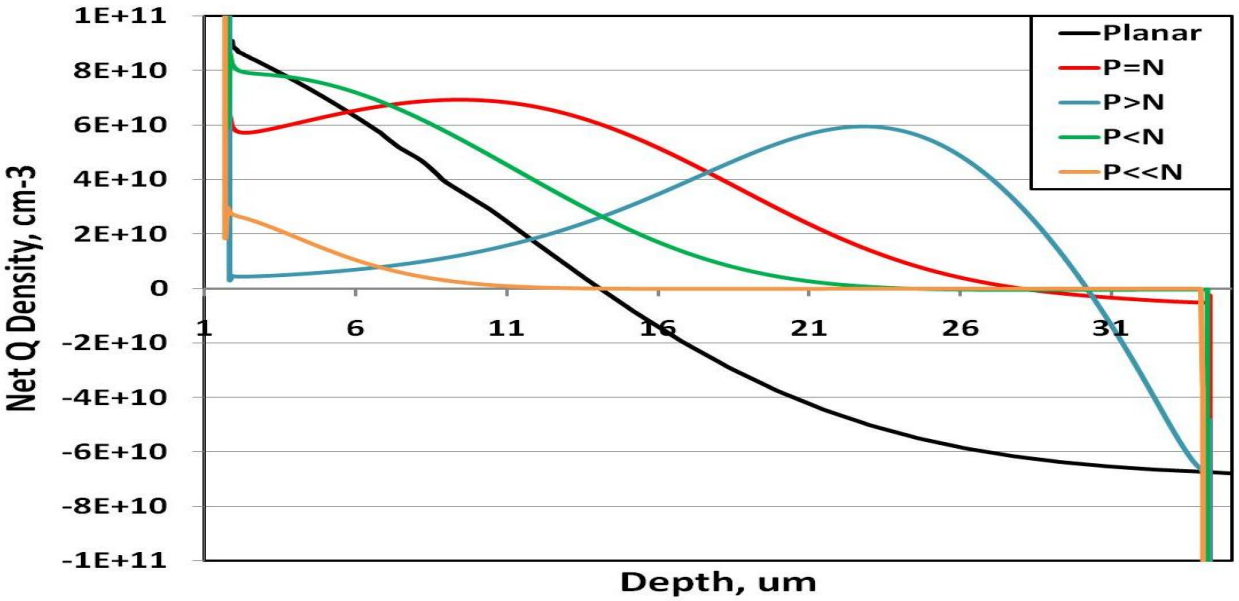


Figure 4.11. Net charge density distribution profiles for different degrees of charge imbalance in an SJ MOSFET.

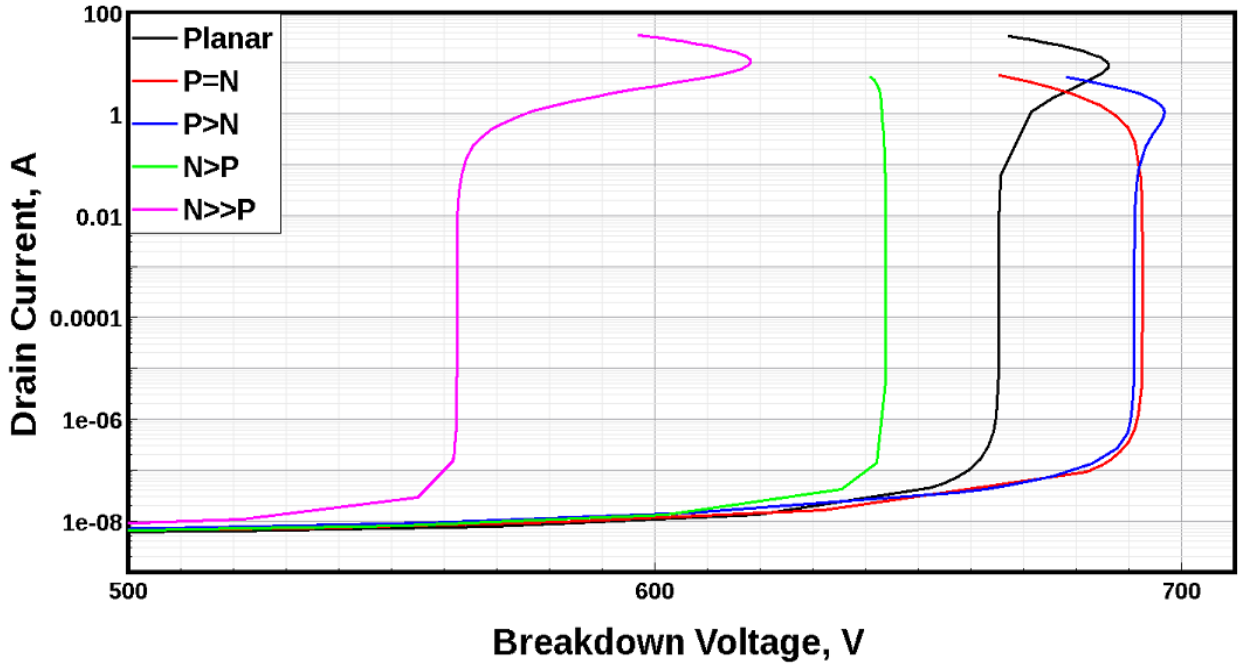


Figure 4.12. BV snapback curves for different degrees of charge imbalance in an SJ MOSFET.

Unfortunately, while the significantly higher N column charge results in much better UIS improvement, it also drops the BV a lot. This is not a practically design point for an SJ MOSFET. On the flip side, we can get the benefit on an improved UIS capability by just slightly increasing the P column charge. This becomes an easier design point in comparison, and thererefore much easier to implement. The slightly higher P column charge however does result in a higher Rds-on as a result of a narrower N-column charge.

Graded SJ MOSFET Structure

To improve the BV-Rds-on trade-off from a constant P heavy design, we can also design a SJ MOSFET having a partial P heavy column [80]. This way, the electric field is still distorted, but not all the way to the bottom of the P-column, as shown in Figure 4.13. We can make the bottom of the P column lighter to reduce the effect the imbalance would have on the Rds-on of the device.

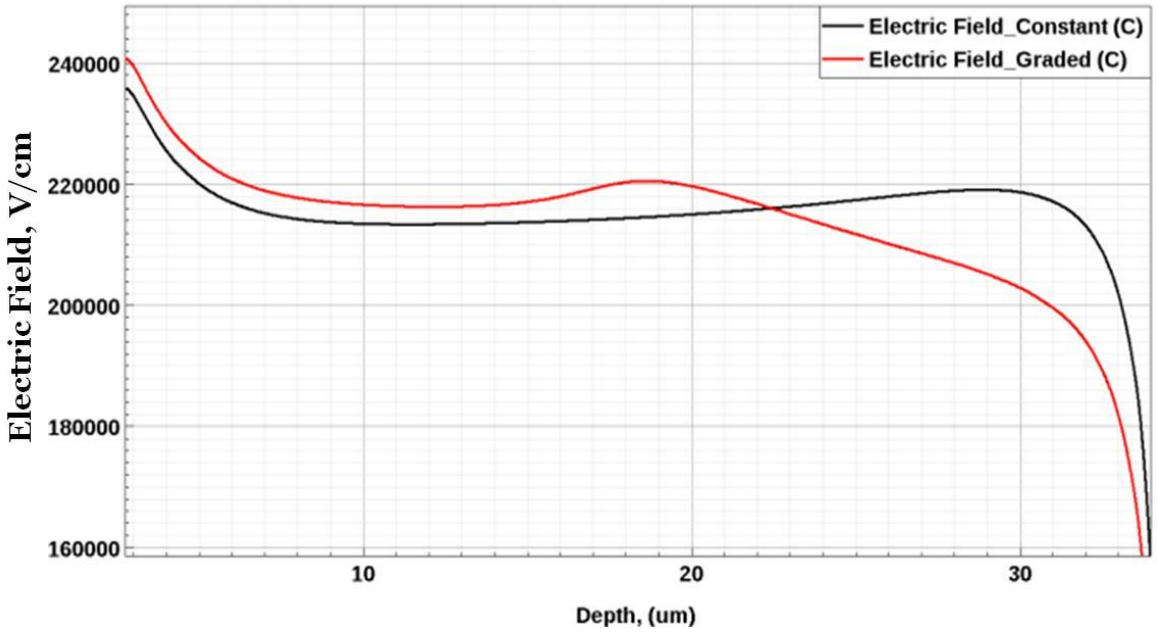


Figure 4.13. Comparing electric field profiles in constant and graded P heavy SJ MOSFETs.

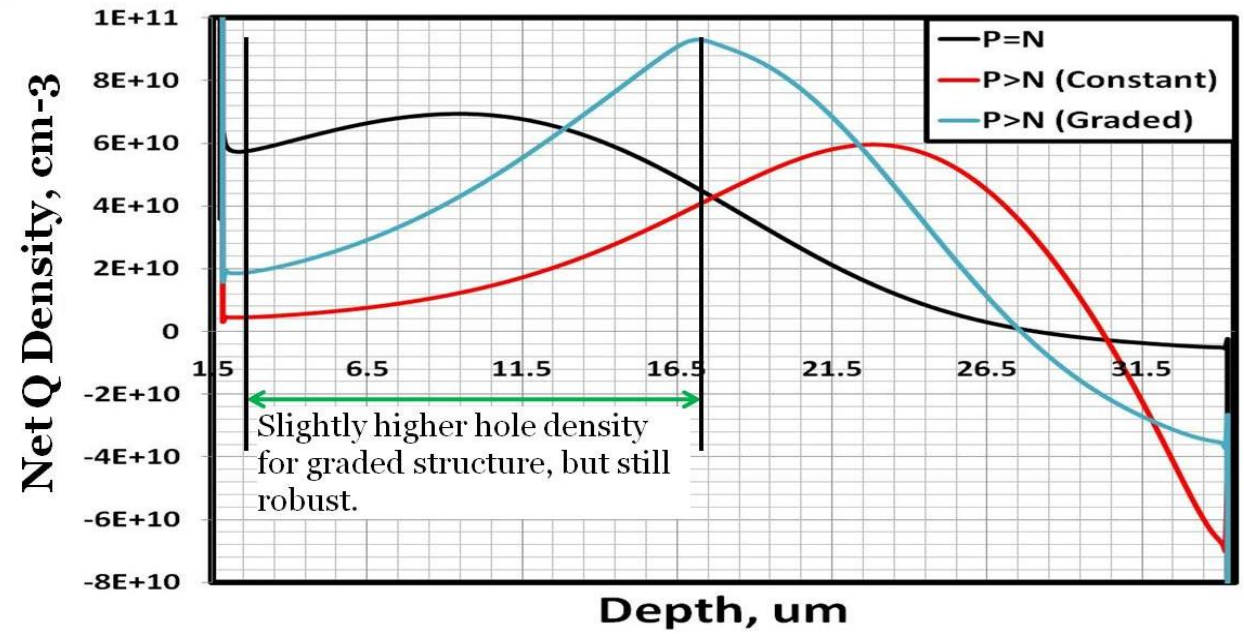


Figure 4.14. Comparing net carrier density distribution profiles in constant and graded P heavy SJ MOSFETs.

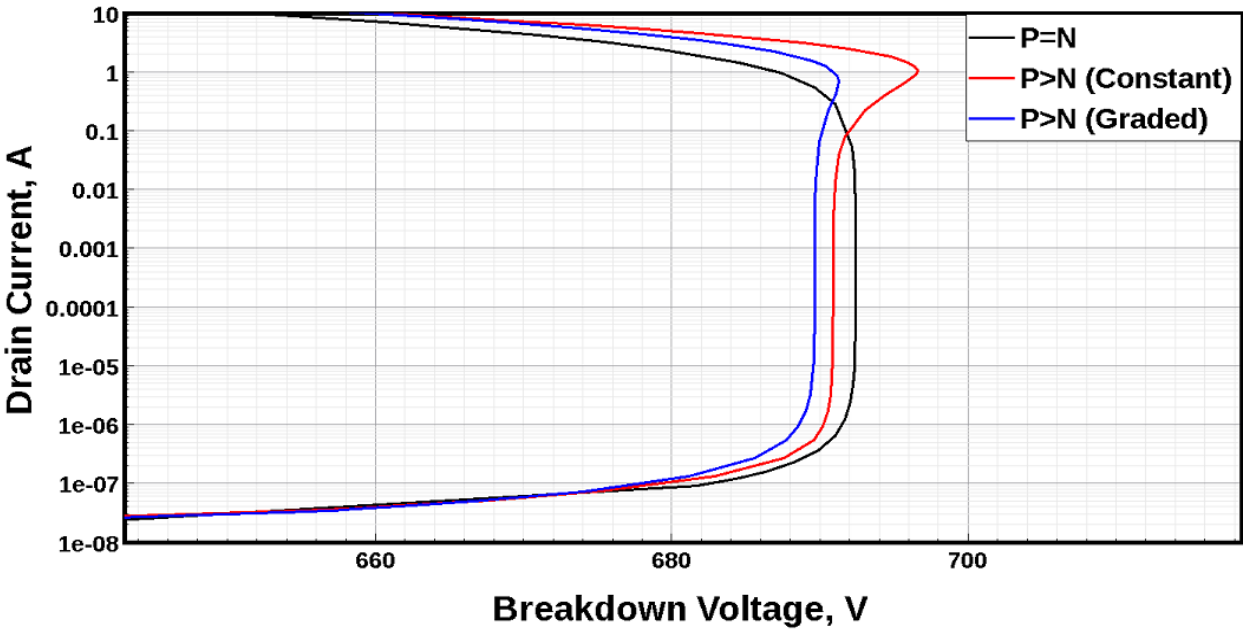


Figure 4.15. Comparing BV snapback curves for constant and graded P heavy SJ MOSFETs.

The effect this graded doping has on the charge density is shown in Figure 4.14. By grading the P-column, we can still achieve a reduced carrier density close the surface and in the drift region

compared to a charge balanced structure. This is still sufficient to result in a positive R_{DYN} while delaying the parasitic BJT from turning on.

The effect of the graded P column charge can be seen in the avalanche snapback curves shown in Figure 4.15. While the graded doping results in an improved curve compared to a balanced structure, it is still worse than a contact P heavy structure, because the electric field and charge density are not distorted enough.

Summary

Figure 4.16 provides an accurate summary of the main trade-offs involved with designing a robust SJ MOSFET with good UIS capability. Based on the results shown above, the graded SJ MOSFET provides us with the optimum design for ruggedness while maintaining BV and Rds-on.

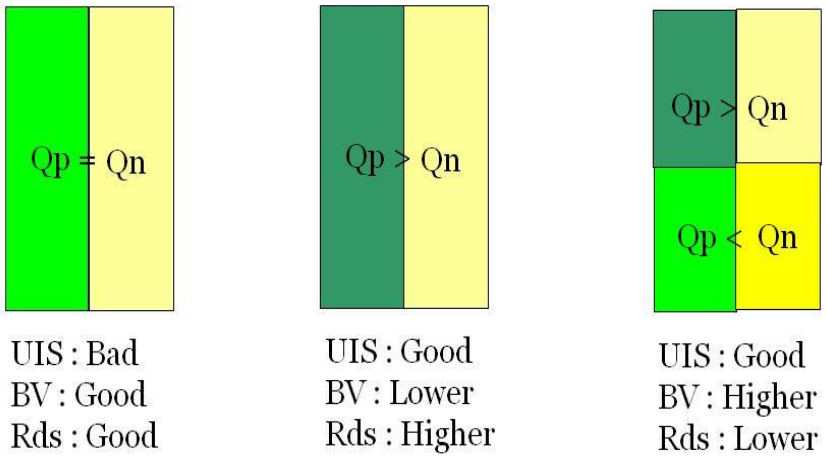


Figure 4.16. Summary of the trade-offs involved with designing a charge imbalanced SJ MOSFET for improved robustness.

CHAPTER 5
CONCLUSION AND FUTURE WORK

Summary

Given the need for increased efficiency in industrial power systems in the high voltage range, the previous chapters all address different aspects of the power system. For the high side device, a partial superjunction based trench diode for fast recovery is proposed. Through topside injection control, we can significantly improve upon carrier density profile and the resulting V_f-Q_{rr} trade-off.

Table 5.1 compares the different technologies and their pros and cons compared to the trench FRD structure. The trench based fast recovery diode addresses injection control in a high voltage diode which improves the VF-Qrr trade-off, thereby increasing the efficiency of the entire system during the switching phase.

If the diode structure changes, the termination scheme changes accordingly. The proposed termination scheme shows the inherent advantage of a trench based termination to support higher electric fields, thus enabling a more compact termination. The increased reliability of the structure with respect to a conventional termination where the potential lines terminate at the surface in silicon is also demonstrated. The termination scheme can easily be adapted to any changes in the Trench MOS structure because the core concept of the termination scheme remains the same irrespective of the dimensions of the Trench MOS structure. The comparison of the different termination schemes is shown in Table 5.2/

Table 5.1. Comparison of different diode technologies

Technology	Pro	Con
Planar	Easy to fabricate; Extremely good contact resistance; Cheap	No inherent injection control mechanism
Planar (With Lifetime Control)	Improved Qrr	Increased Vf, leakage current at RT; Degraded Qrr at HT;
Shottky Contact Diode	Schottky Contact enables flat carrier profile; Enhanced Vf-Qrr trade-off	Requires precise backside process control; Activation of backside N could be inadequate; Possible high backside contact resistance
CIBH Diode	Excellent backside injection control; Good Vf-Qrr Control	Requires precise backside process control; Activation of backside N could be inadequate; Possible high backside contact resistance; More expensive to fabricate
Hydrogen Implant	Improved Vf-Qrr trade-off	Has fabrication limitations; Hydrogen implants not common; More expensive
Trench FRD (Proposed)	Improved Vf-Qrr trade-off; Smaller drop-off in performance from RT to HT	Slightly more expensive; Will require a bit of process variation to comply with other diode active structures.

Table 5.2. Comparison of different edge termination schemes

Technology	Pro	Con
Planar Termination Structures (JTE, Field Rings, Metal Plates, etc).	Easy to implement; Cheap	Not compatible with trench MOS structure; Peak Electric Field occurs in Silicon;
Metal Plates based SJ termination	Metal plates greatly help shape the electric field; Very Efficient	Does not translate well to partial trench MOS structure; Peak Electric Field occurs in Silicon.
Charge Imbalanced SJ termination	Easily implemented for a SJ structure; Very Efficient.	Does not translate well to partial trench MOS structure; Peak Electric Field occurs in Silicon.
Oxide Filled Trench termination	Very efficient; Peak Electric Field occurs in Oxide.	Absence of trench polysilicon creates a additional process steps
Proposed Structure	Very efficient; Peak Electric Field occurs in Oxide; Combination of field plate and trench oxide further maximizes the efficiency.	Currently unique to structures with trench MOS structure; Does not easily translate to pure superjunction structures.

In Chapter 4, the mechanism of the UIS current handling capability of the superjunction MOSFET as it pertains to its robustness is explained. The relationship between the UIS capability and the BV avalanche snapback curve is examined, and the effect of the different charge balance states of the superjunction MOSFET is also explained. This information is critical in designing a robust superjunction MOSFET, especially as they continually scale towards smaller pitches and higher column charges.

Future Work

While the proposed structures show advantages with regards to their application and their performance, work is still ongoing to find more ways to improve upon their existing performance specs.

Trench Based Fast Recovery Diode.

While the proposed diode shows good performance mcharacteristics, it still has a variety of areas where further improvements are being worked on, namely:

- Trench MOS Depth: The trench MOS structure can be extended deeper into the silicon to increase the SJ part of the diode. The P base dose will have to be increased accordingly to account for the increased N charge.

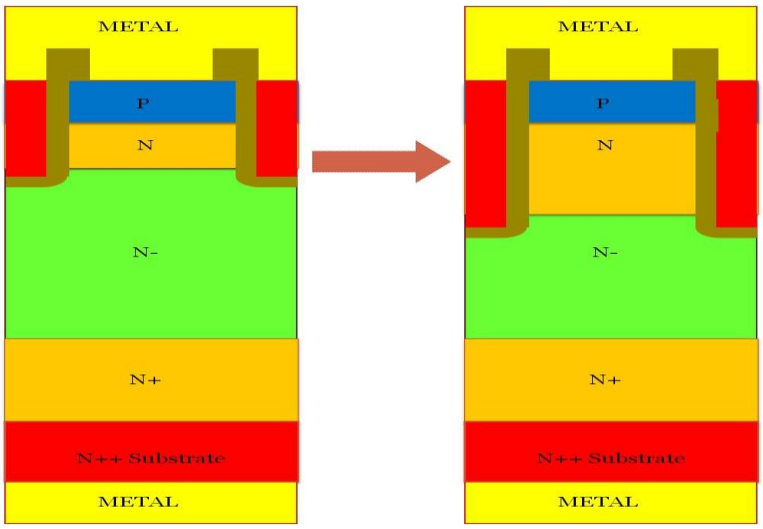


Figure 5.1. Extension of the Trench MOS structure within the design for improved efficiency.

- Contact Resistance: The presence of a trench MOS structure at the surface allows us to use a significantly lower P-base dose at the cathode side, though heavy enough to prevent

punch-through. This is not an issue with a planar diode. So, improvement in this area is being further explored. This would improve the Vf-Qrr trade-off even further

- Additional Backside improvement: The performance of the diode could be improved further by reducing the thickness of the diode. Presently, the diode still uses the substrate, but by removing the substrate, we could engineer the backside of the diode even further to combine topside and backside injection control.

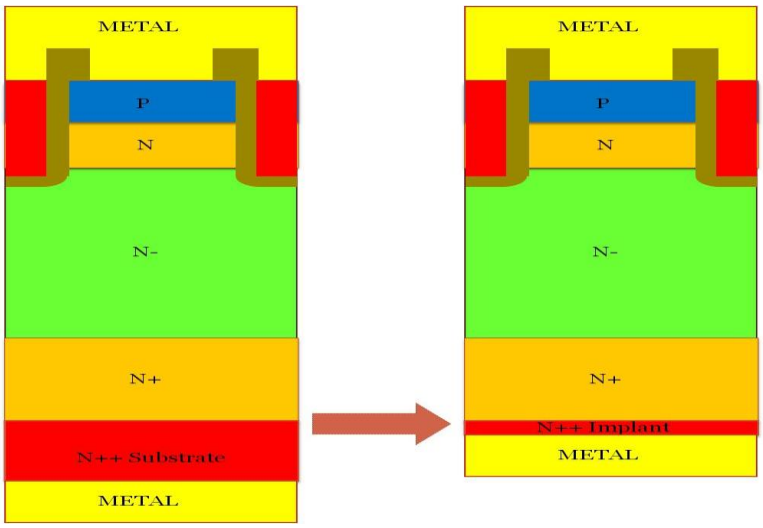


Figure 5.2. Removal of substrate for backside injection control.

Edge Termination

The current termination scheme which uses the shielded trench structure is an effective and compact way for edge termination for partial superjunction devices. Future work on this front too is ongoing. Further work on this front involves the following topics:

- Changing the metal field plate arrangement can lead to a more compact termination.

- Using a different trench CD in the active and termination regions can result in a much more efficient distribution of the electric field along the termination.
- We can also use varying trench depth along the termination to alter the electric field.

While all the above mentioned ideas can result in a more compact and efficient termination, they are also usually accompanied with the caveat of higher cost and increased process complexity.

Superjunction Robustness

Superjunction technology in itself is a relatively new technology compared to most other power semiconductor technologies, so the work on this field is still pretty recent and developing. This applied especially to suprejunction robustness. While the current work focuses on the UIS capability of the MOSFET as it relates to the avalanche snapback phenomenon, this concept needs further study with regards to how charge imbalance and the device structure affect and change the UIS capability. This study is presently ongoing.

APPENDIX A: TRENCH DIODE SCHEME CODE

```
$driver ts4_init
$module epi_poly:4
$step define_grid

line x loc=0 spacing=0.1
line x loc=@PITCH@ spacing=0.1
line y loc=@TEPI@+@TEPI2@+@TEPI3@+@TEPI4@ spacing=0.25
line y loc=200 spacing=30

init orient=100 arsenic=0.003 resistiv
epitaxy temp=1150 time=@TEPI@ thickness=@TEPI@ phosphor=@REPI@ spaces=10 resistiv
epitaxy temp=1150 time=@TEPI2@ thickness=@TEPI2@ phosphor=@REPI2@ spaces=20
resistiv
epitaxy temp=1150 time=2.5 thickness=2.5 phosphor=@REPI3@ spaces=20 resistiv
epitaxy temp=1150 time=@TEPI3@-5 thickness=@TEPI3@-5 phosphor=@REPI3@ spaces=50
resistiv
epitaxy temp=1150 time=2.5 thickness=2.5 phosphor=@REPI3@ spaces=10 resistiv
epitaxy temp=1150 time=@TEPI4@-0.5 thickness=@TEPI4@-0.5 phosphor=@REPI4@
spaces=50 resistiv
epitaxy temp=1150 time=0.5 thickness=0.5 phosphor=@REPI4@ spaces=25 resistiv

method fermi compress dy.ox=0.01 init=0.05 ^dif.adap ^imp.adap
```

```
etch oxide all
$step Fab trench G and S poly
deposit oxide thickness=1 spaces=6
etch oxide start x=0 y=-60
etch oxide cont x=0 y=1
etch oxide cont x=@TWIDTH@/2 y=1
etch oxide done x=@TWIDTH@/2 y=-60
etch oxide start x=@PITCH@-@TWIDTH@/2 y=-60
etch oxide cont x=@PITCH@-@TWIDTH@/2 y=1
etch oxide cont x=@PITCH@ y=1
etch oxide done x=@PITCH@ y=-60
etch silicon trapezoi thick=@TDEPTH@-@ISO@ angle=89.5 undercut=0
etch silicon isotropic thick=@ISO@
etch oxide all

$step Sac_ox
DIFFUSE TEMPERA=750 TIME=45 F.N2=10 F.O2=0.1
DIFFUSE TEMPERA=850 TIME=20 F.N2=10 F.O2=0.1
DIFFUSE TEMPERA=850 TIME=60 F.O2=15
DIFFUSE TEMPERA=850 T.FINAL=1050 TIME=20 F.N2=10 F.O2=0.1
DIFFUSE TEMPERA=1050 TIME=5 F.N2=10 F.O2=0.1
DIFFUSE TEMPERA=1050 TIME=15 F.O2=15
```

```
DIFFUSE TEMPERA=1050 TIME=15 F.O2=15 F.HCL=0.2
DIFFUSE TEMPERA=1050 TIME=15 F.O2=15
DIFFUSE TEMPERA=1050 TIME=10 F.N2=10
DIFFUSE TEMPERA=1050 T.FINAL=750 TIME=100 F.N2=10
etch oxide all

$step FieldOxD007
method fermi compress dy.ox=0.1 init=0.05 ^dif.adap ^imp.adap
diffuse temperature=800 time=20.167 f.n2=20 f.o2=.4
diffuse temperature=800 time=15 f.n2=10 f.o2=.2
diffuse temperature=800 t.final=950 time=18.75 f.n2=10 f.o2=.2
diffuse temperature=950 t.final=1000 time=10 f.n2=10 f.o2=.2
diffuse temperature=1000 t.final=1050 time=16.67 f.n2=10 f.o2=.2
diffuse temperature=1050 t.final=1100 time=25 f.n2=10 f.o2=.2
diffuse temperature=1100 time=15 f.n2=10 f.o2=.2
diffuse temperature=1100 time=60 f.o2=6.5 f.h2=6.5
diffuse temperature=1100 time=5 f.o2=10
diffuse temperature=1100 time=30 f.n2=10
diffuse temperature=1100 t.final=800 time=100 f.n2=10
diffuse temperature=800 time=20.167 f.n2=20
deposit oxide thickness=0.1 spaces=5
etch oxide thickness=0.1 isotropic
```

```
deposit polysilicon thickness=3 spaces=8 phos=2e20
etch polysilicon thickness=3.4
%extract oxide x=@PITCH@/2 name=ox print
etch oxide thickness=@{ox} isotropic
deposit oxide thickness=1
etch oxide thickness=1

$driver ts4
$module body:0
$step load
method ^imp.adap
method fermi compress dy.ox=0.01 init=0.02 ^dif.adap
implant boron dose=@bodydose@ energy=@bodyegy@ tilt=0
$step Body_driveD101
impurity imp=boron mat=sili /mat=oxide trans.0=0
diffuse temperature=800 time=35 f.n2=10 f.o2=.2
diffuse temperature=800 t.final=950 time=18.75 f.n2=10 f.o2=.2
diffuse temperature=950 t.final=1000 time=10 f.n2=10 f.o2=.2
diffuse temperature=1000 t.final=1050 time=16.667 f.n2=10 f.o2=.2
diffuse temperature=1050 t.final=1100 time=25 f.n2=10 f.o2=.2
diffuse temperature=1100 time=3 f.o2=15
diffuse temperature=1100 time=7.5 f.o2=15 f.hcl=.410
```

```
diffuse temperature=1100 time=3 f.o2=15

diffuse temperature=1100 t.final=1150 time=50 f.n2=10

diffuse temperature=1150 time=@Dt@ f.n2=10

diffuse temperature=1150 t.final=800 time=117 f.n2=10

diffuse temperature=800 time=30 f.n2=20


%extract oxide x=@PITCH@/2 name=oxpplus print

etch oxide thickness=@{oxpplus}+.025 isotropic


$driver ts4_med

$module contact_metal:0

$step load

method ^imp.adap

method fermi compress dy.ox=0.01 init=0.02 ^dif.adap

$step BPSGReFlowD105

impurity imp=boron mat=sili /mat=oxide trans.0=0

DIFFUSE TEMPERA=800 TIME=35

DIFFUSE TEMPERA=800 T.FINAL=900 TIME=12.5 F.O2=0.2 F.N2=10

DIFFUSE TEMPERA=900 TIME=5 F.N2=10

DIFFUSE TEMPERA=900 TIME=30 F.O2=10

DIFFUSE TEMPERA=900 T.FINAL=800 TIME=35 F.N2=10
```

```
etch oxide start x=0 y=-60
etch oxide cont x=0 y=0.3
etch oxide cont x=@trenchc@  y=0.3
etch oxide done x=@trenchc@ y=-60

etch oxide start x=@PITCH@-@trenchc@  y=-60
etch oxide cont x=@PITCH@-@trenchc@ y=0.3
etch oxide cont x=@PITCH@ y=0.3
etch oxide done x=@PITCH@ y=-60

etch oxide start x=@x1c@ y=-60
etch oxide cont x=@x1c@ y=0.3
etch oxide cont x=@x2c@ y=0.3
etch oxide done x=@x2c@ y=-60

#%extract oxide x=@PITCH@/2 name=ox print
#etch oxide thickness=@{ox}+0.05 isotropic



etch silicon thickness=@depth@
```

```
deposit aluminum thickness=0.05 spaces=4

deposit aluminum thickness=3 spaces=4

electrode x=2.75 y=-1 name=source


(define TIFstem "n@previous@_ts4")

(define TDRstem "n@node@_tif")


(define hp (* 0.5 (+ @PITCH@ 0)))


(system:command  (string-append "tdx -f "TIFstem " " TDRstem))

(define TDR (string-append TDRstem ".tdr"))

(sde:extract-tdr-boundary TDR)

(sdeio:read-tdr-bnd "n@node@_tif_new_bnd.tdr")



(sdegeo:2d-cut (position -1 -5 0.0) (position @PITCH@ @Twafer@ 0.0))


(sdegeo:mirror-selected (get-body-list) (transform:reflection (position 0 0 0) (gvector 0 1 0)) #f)

(sdedr:define-refeval-window "RefLine.Shbottom" "Line"  (position 0 @Twafer@ 0)  (position

@Nwidth@ @Twafer@ 0) )

(sdedr:define-analytical-profile-placement "PlaceAP.Shbottom" "DefAP.Shbottom"

"RefLine.Shbottom" "Positive" "NoReplace" "Eval")
```

(sdedr:define-gaussian-profile "DefAP.Shbottom" "PhosphorusActiveConcentration" "PeakPos" 0 "PeakVal" @NPdose@ "ValueAtDepth" 1e14 "Depth" 0.5 "Gauss" "Factor" 0.1)

(sdegeo:mirror-selected (get-body-list) (transform:reflection (position 0 0 0) (gvector 0 1 0)) #f)

(sdedr:define-submesh "ExternalProfileDefinition_1" TDR)

(sdedr:define-refeval-window "RefEvalWin_1" "Rectangle" (position 0 0 0) (position @PITCH@ @Twafer@ 0))

(sdedr:define-submesh-placement "extplace1" "ExternalProfileDefinition_1" "RefEvalWin_1" "NoReplace")

(sdedr:define-submesh "ExternalProfileDefinition_1" TDR)

(sdedr:define-refeval-window "topwin" "Cuboid" (position 0 0 0)(position @PITCH@ 8 0))

(sdedr:define-refinement-size "refdef2" 0.1 0.1 0 0.05 0.05 0)

(sdedr:define-refinement-function "refdef2" "DopingConcentration" "MaxTransDiff" 1)

(sdedr:define-refinement-placement "placetop" "refdef2" "topwin")

(sdedr:define-refeval-window "epi" "Cuboid" (position 0 6 0)(position @PITCH@ @Twafer@ 0))

(sdedr:define-refinement-size "refdef1" 1 1 0 0.1 0.1 0)

(sdedr:define-refinement-function "refdef1" "DopingConcentration" "MaxTransDiff" 1)

(sdedr:define-refinement-placement "placeepi" "refdef1" "epi")

(sdedr:define-refeval-window "botwin" "Cuboid" (position 0 50 0)(position @PITCH@ @Twafer@ 0))

```
(sedr:define-refinement-size "refdef3" 1 1 0 0.05 0.05 0 )
(sedr:define-refinement-function "refdef3" "DopingConcentration" "MaxTransDiff" 1)
(sedr:define-refinement-placement "placebottom" "refdef3" "botwin" )

;(sedr:define-refeval-window "rfwin" "Rectangle" (position 0 -5 0) (position (- @PITCH@
0.0001) @Twafer@ 0))
;(sedr:define-submesh-placement "extp" "ExternalProfileDefinition_1" "rfwin" "NoReplace"
"ShiftVector" (gvector  0 0 0))

(sdegeo:define-contact-set "drain" 4  (color:rgb 0 1 0 ) "##" )
(sdegeo:set-current-contact-set "drain")
(sdegeo:define-2d-contact (find-edge-id (position 4 @Twafer@ 0)) (sdegeo:get-current-contact-
set))

(sde:set-meshing-command "snmesh -a -c boxmethod")
(sdedr:append-cmd-file "")
(sde:build-mesh "snmesh" "-a -c boxmethod" "n@node@")
```

APPENDIX B: TERMINATION SCHEME CODE

```
$driver ts4_init
$module epi_poly:4
$step define_grid

line x loc=0 spacing=0.1
line x loc=@PITCH@ spacing=0.1
line y loc=@TEPI@+@TEPI2@+@TEPI3@+@TEPI4@ spacing=0.25
line y loc=200 spacing=30

init orient=100 arsenic=0.003 resistiv
epitaxy temp=1150 time=@TEPI@ thickness=@TEPI@ phosphor=@REPI@ spaces=10 resistiv
epitaxy temp=1150 time=@TEPI2@ thickness=@TEPI2@ phosphor=@REPI2@ spaces=20
resistiv
epitaxy temp=1150 time=2.5 thickness=2.5 phosphor=@REPI3@ spaces=20 resistiv
epitaxy temp=1150 time=@TEPI3@-5 thickness=@TEPI3@-5 phosphor=@REPI3@ spaces=50
resistiv
epitaxy temp=1150 time=2.5 thickness=2.5 phosphor=@REPI3@ spaces=10 resistiv
epitaxy temp=1150 time=@TEPI4@-0.5 thickness=@TEPI4@-0.5 phosphor=@REPI4@
spaces=50 resistiv
epitaxy temp=1150 time=0.5 thickness=0.5 phosphor=@REPI4@ spaces=25 resistiv

method fermi compress dy.ox=0.01 init=0.05 ^dif.adap ^imp.adap
```

```
etch oxide all
$step Fab trench G and S poly
deposit oxide thickness=1 spaces=6
etch oxide start x=0 y=-60
etch oxide cont x=0 y=1
etch oxide cont x=@TWIDTH@/2 y=1
etch oxide done x=@TWIDTH@/2 y=-60
etch oxide start x=@PITCH@-@TWIDTH@/2 y=-60
etch oxide cont x=@PITCH@-@TWIDTH@/2 y=1
etch oxide cont x=@PITCH@ y=1
etch oxide done x=@PITCH@ y=-60
etch silicon trapezoi thick=@TDEPTH@-@ISO@ angle=89.5 undercut=0
etch silicon isotropic thick=@ISO@
etch oxide all

# Buried Guard Ring Implant
method ^imp.adap
method fermi compress dy.ox=0.01 init=0.02 ^dif.adap
deposit photores thickness=1 spaces=5
etch photores all
implant boron dose=@bgrdose@/4 energy=@bgregy@ tilt=@bgrang@
implant boron dose=@bgrdose@/4 energy=@bgregy@ tilt=@bgrang@
```

```
implant boron dose=@bgrdose@/4 energy=@bgregy@ tilt=@bgrang@

implant boron dose=@bgrdose@/4 energy=@bgregy@ tilt=@bgrang@

etch photores all

etch oxide all



$step Sac_ox

DIFFUSE TEMPERA=750 TIME=45 F.N2=10 F.O2=0.1

DIFFUSE TEMPERA=850 TIME=20 F.N2=10 F.O2=0.1

DIFFUSE TEMPERA=850 TIME=60 F.O2=15

DIFFUSE TEMPERA=850 T.FINAL=1050 TIME=20 F.N2=10 F.O2=0.1

DIFFUSE TEMPERA=1050 TIME=5 F.N2=10 F.O2=0.1

DIFFUSE TEMPERA=1050 TIME=15 F.O2=15

DIFFUSE TEMPERA=1050 TIME=15 F.O2=15 F.HCL=0.2

DIFFUSE TEMPERA=1050 TIME=15 F.O2=15

DIFFUSE TEMPERA=1050 TIME=10 F.N2=10

DIFFUSE TEMPERA=1050 T.FINAL=750 TIME=100 F.N2=10

etch oxide all



$step FieldOxD007

method fermi compress dy.ox=0.1 init=0.05 ^dif.adap ^imp.adap

diffuse temperature=800 time=20.167 f.n2=20 f.o2=.4
```

```
diffuse temperature=800 time=15 f.n2=10 f.o2=.2
diffuse temperature=800 t.final=950 time=18.75 f.n2=10 f.o2=.2
diffuse temperature=950 t.final=1000 time=10 f.n2=10 f.o2=.2
diffuse temperature=1000 t.final=1050 time=16.67 f.n2=10 f.o2=.2
diffuse temperature=1050 t.final=1100 time=25 f.n2=10 f.o2=.2
diffuse temperature=1100 time=15 f.n2=10 f.o2=.2
diffuse temperature=1100 time=60 f.o2=6.5 f.h2=6.5
diffuse temperature=1100 time=5 f.o2=10
diffuse temperature=1100 time=30 f.n2=10
diffuse temperature=1100 t.final=800 time=100 f.n2=10
diffuse temperature=800 time=20.167 f.n2=20
deposit oxide thickness=0.1 spaces=5
etch oxide thickness=0.1 isotropic
deposit polysilicon thickness=3 spaces=8 phos=2e20
etch polysilicon thickness=3.4
%extract oxide x=@PITCH@/2 name=ox print
etch oxide thickness=@{ox} isotropic
deposit oxide thickness=1
etch oxide thickness=1

$driver ts4
$module body:0
```

```
$step load
method ^imp.adap
method fermi compress dy.ox=0.01 init=0.02 ^dif.adap
implant boron dose=@bodydose@ energy=@bodyegy@ tilt=0
$step Body_driveD101
impurity imp=boron mat=sili /mat=oxide trans.0=0
diffuse temperature=800 time=35 f.n2=10 f.o2=.2
diffuse temperature=800 t.final=950 time=18.75 f.n2=10 f.o2=.2
diffuse temperature=950 t.final=1000 time=10 f.n2=10 f.o2=.2
diffuse temperature=1000 t.final=1050 time=16.667 f.n2=10 f.o2=.2
diffuse temperature=1050 t.final=1100 time=25 f.n2=10 f.o2=.2
diffuse temperature=1100 time=3 f.o2=15
diffuse temperature=1100 time=7.5 f.o2=15 f.hcl=.410
diffuse temperature=1100 time=3 f.o2=15
diffuse temperature=1100 t.final=1150 time=50 f.n2=10
diffuse temperature=1150 time=@Dt@ f.n2=10
diffuse temperature=1150 t.final=800 time=117 f.n2=10
diffuse temperature=800 time=30 f.n2=20

%extract oxide x=@PITCH@/2 name=oxpplus print
etch oxide thickness=@{oxpplus}+.025 isotropic
```

```
$driver ts4_med
$module contact_metal:0
$step load
method ^imp.adap
method fermi compress dy.ox=0.01 init=0.02 ^dif.adap
$step BPSGReFlowD105
impurity imp=boron mat=sili /mat=oxide trans.0=0
DIFFUSE TEMPERA=800 TIME=35
DIFFUSE TEMPERA=800 T.FINAL=900 TIME=12.5 F.O2=0.2 F.N2=10
DIFFUSE TEMPERA=900 TIME=5 F.N2=10
DIFFUSE TEMPERA=900 TIME=30 F.O2=10
DIFFUSE TEMPERA=900 T.FINAL=800 TIME=35 F.N2=10

(define TIFstem "n@previous@_ts4")
(define TDRstem "n@node@_tif")
(define thick @Twafer@)
(define wtr 2)
(define mesa 4)
(define fs 18)
(define offset 15)
 (define spacings (list @s1@ @s2@ @s3@ @s4@ @s5@ @s6@ @s7@ @s8@ @s9@ @s10@
@s11@ @s12@ @s13@ @s14@ @s15@ @s16@ @s17@ @s18@ @s19@ @s20@ @s21@
```

```
@s22@ @s23@ @s24@ @s25@ @s26@ @s27@ @s28@ @s29@ @s30@ @s31@ @s32@
@s33@ @s34@ @s35@ @s36@ @s37@))
 (define RN (length spacings))
(define origin (* (* (+ wtr fs) 0.5) -1))
(define start origin)
(define stop 0)
(define end (* origin -1))
(define s 0)
(define rfwin "string")
(define extp "string")
(define Elec "string")
(define reg "string")

(system:command  (string-append "tdx -f "TIFstem " " TDRstem))
(define TDR (string-append TDRstem ".tdr"))
(sde:extract-tdr-boundary TDR)
(sdeio:read-tdr-bnd "n@node@_tif_new_bnd.tdr")

(do ( (i RN (- i 1)) )
        ((= i -2))
                (begin
                        (cond
```

```
((= i RN)
        (begin
                (set! start origin)
                (set! stop 0)
                (set! end (* origin -1))
                (sdegeo:mirror-selected (get-body-list)
(transform:reflection (position stop 0 0) (gvector -1 0 0)) #t)
                (sdegeo:2d-cut (position origin -2 0.0) (position end
thick 0.0))

        )
)
((= i 0)
        (begin
                (set! s (+ wtr (list-ref spacings i)))
                (set! start end)
                (set! stop (+ start (- start stop)))
                (set! end (+ stop (* s 0.5)))
                (sdegeo:mirror-selected (get-body-list)
(transform:reflection (position start 0 0) (gvector -1 0 0)) #t)
                (sdegeo:2d-cut (position origin -2 0.0) (position end
thick 0.0))
```

```
                )
            )
            ((= i -1)
                (begin
                    (set! s (+ mesa wtr))
                    (set! start end)
                    (set! stop (+ start (- start stop)))
                    (set! end (+ stop (* s 0.5)))
                    (sdegeo:mirror-selected (get-body-list)
(transform:reflection (position start 0 0) (gvector -1 0 0)) #t)
                    (sdegeo:2d-cut (position origin -2 0.0) (position end
thick 0.0))
                    (sdegeo:mirror-selected (get-body-list)
(transform:reflection (position end 0 0) (gvector -1 0 0)) #t)
                    (set! end (+ stop s))
                    (sdegeo:2d-cut (position origin -2 0.0) (position end
thick 0.0))

                )
            )
            (else
```

```
                                        (begin
                                                (set! s (+ wtr (list-ref spacings i)))
                                                (set! start end)
                                                (set! stop (+ start (- start stop)))
                                                (set! end (+ stop (* s 0.5)))
                                                (sdegeo:mirror-selected (get-body-
list)(transform:reflection (position start 0 0)(gvector 1 0 0)) #t)
                                                (sdegeo:2d-cut (position origin -2 0.0) (position end
thick 0.0))

                                        )
                                )
                        )
                )
)
(define term end)
(sdedr:define-submesh "ExternalProfileDefinition_1" TDR)
(sdedr:define-refeval-window "topwin" "Cuboid" (position origin -1 0)(position term 6 0))
(sdedr:define-refinement-size "refdef2" 1 1 0 0.1 0.1 0 )
(sdedr:define-refinement-function "refdef2" "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "placetop" "refdef2" "topwin" )
(sdedr:define-refeval-window "epi" "Cuboid" (position origin 6 0)(position term thick 0))
```

```
(sdedr:define-refinement-size "refdef1" 2 2 0 0.1 0.1 0 )
(sdedr:define-refinement-function "refdef1" "DopingConcentration" "MaxTransDiff" 1)
(sdedr:define-refinement-placement "placeepi" "refdef1" "epi" )

(do ( (j RN (- j 1)) )
   ( (= j -2) )
        (begin
                    (cond
                        ((= j RN)
                            (begin
                                (set! start origin)
                                (set! stop 0)
                                (set! end (* origin -1))

                            )
                        )
                        ((= j (- RN 1))
                            (begin
                                (set! s (+ wtr (list-ref spacings j)))
                                (set! start end)
                                (set! stop (+ start (- start stop)))
                                (set! end (+ stop (* s 0.5)))
```

```
                                        (set! rfwin (string-append "RefEvalWin_"
(number->string (* j 2))))
                                        (set! extp (string-append "extplace" (number-
>string (* j 2))))
                                        (sdedr:define-refeval-window rfwin "Rectangle"
(position origin 0 0) (position (- stop 0.0001) thick 0))
                                        (sdedr:define-submesh-placement extp
"ExternalProfileDefinition_1" rfwin "NoReplace" "ShiftVector" (gvector  (* -1 (- stop offset)) 0
0) "Reflect" "X")
                                        (set! rfwin (string-append "RefEvalWin_"
(number->string (- (* j 2) 1))))
                                        (set! extp (string-append "extplace" (number-
>string (- (* j 2) 1))))
                                        (sdedr:define-refeval-window rfwin "Rectangle"
(position stop 0 0) (position (- end 0.0001) thick 0))
                                        (sdedr:define-submesh-placement extp
"ExternalProfileDefinition_1" rfwin "NoReplace" "ShiftVector" (gvector  stop 0 0))

                                )
                        )
                        ((= j 0)
                                (begin
```

```
                                        (set! s (+ wtr (list-ref spacings j)))
                                        (set! start end)
                                        (set! stop (+ start (- start stop)))
                                        (set! end (+ stop (* s 0.5)))
                                        (set! rfwin (string-append "RefEvalWin_"
(number->string (* j 2))))
                                        (set! extp (string-append "extplace" (number-
>string (* j 2))))
                                        (sdedr:define-refeval-window rfwin "Rectangle"
(position start  0 0) (position (- stop 0.0001) thick 0))
                                        (sdedr:define-submesh-placement extp
"ExternalProfileDefinition_1" rfwin "NoReplace" "ShiftVector" (gvector  (* -1 (- stop offset)) 0
0) "Reflect" "X")
                                        (set! rfwin (string-append "RefEvalWin_"
(number->string (- (* j 2) 1))))
                                        (set! extp (string-append "extplace" (number-
>string (- (* j 2) 1))))
                                        (sdedr:define-refeval-window rfwin "Rectangle"
(position stop 0 0) (position term thick 0))
                                        (sdedr:define-submesh-placement extp
"ExternalProfileDefinition_1" rfwin "NoReplace" "ShiftVector" (gvector  stop 0 0))
```

```
        )
    )
    ((= j -1)
        (begin
            (set! s (+ mesa wtr))
            (set! start end)
            (set! stop (+ start (- start stop)))
            (set! end (+ stop (* s 0.5)))
            (set! end (+ stop 0.5))

        )
    )
    ((= j -2)
        (begin
            (set! s (+ mesa wtr))
            (set! start end)
            (set! stop (+ start (- start stop)))
            (set! end (+ stop (* s 0.5)))
            (set! end (+ stop 0.5))

        )
    )
```

```
                (else
                    (begin
                        (set! s (+ wtr (list-ref spacings j)))
                        (set! start end)
                        (set! stop (+ start (- start stop)))
                        (set! end (+ stop (* s 0.5)))
                        (set! rfwin (string-append "RefEvalWin_"
(number->string (* j 2))))
                        (set! extp (string-append "extplace" (number-
>string (* j 2))))
                        (sdedr:define-refeval-window rfwin "Rectangle"
(position start  0 0) (position (- stop 0.0001) thick 0))
                        (sdedr:define-submesh-placement extp
"ExternalProfileDefinition_1" rfwin "NoReplace" "ShiftVector" (gvector  (* -1 (- stop offset)) 0
0) "Reflect" "X")
                        (set! rfwin (string-append "RefEvalWin_"
(number->string (- (* j 2) 1))))
                        (set! extp (string-append "extplace" (number-
>string (- (* j 2) 1))))
                        (sdedr:define-refeval-window rfwin "Rectangle"
(position stop 0 0) (position (- end 0.0001) thick 0))
```

```
                                        (sdedr:define-submesh-placement extp
"ExternalProfileDefinition_1" rfwin "NoReplace" "ShiftVector" (gvector  stop 0 0))

                                    )
                                )
                            )
                        )
)

(do ( (m RN (- m 1)) )
    ( (= m -2) )
        (begin
                (cond
                    ((= m RN)
                        (begin
                            (set! start origin)
                            (set! stop 0)
                            (set! end (* origin -1))
                            (set! reg (string-append "Al_" (number->string m)))

                            (sdegeo:create-rectangle (position (+ start 0.5)  0  0)
(position start  0.36  0) "Aluminum" reg )
```

```
                                        (sdegeo:create-rectangle (position (+ stop 0.5)  0  0)
(position  stop   0.36  0) "Aluminum" reg )

                                        (set! Elec "drain")
                                        (sdegeo:define-contact-set Elec 4  (color:rgb 0 1 0 )
"##" )

                                        (sdegeo:set-current-contact-set Elec)
                                        (sdegeo:define-2d-contact (find-edge-id (position (
+ start  0.1) 0 0)) (sdegeo:get-current-contact-set))
                                        (sdegeo:define-2d-contact (find-edge-id (position (
+ stop 0.1) 0 0)) (sdegeo:get-current-contact-set))
                                        (sdegeo:define-2d-contact (find-edge-id (position
offset thick 0)) (sdegeo:get-current-contact-set))
                                )
                        )
                        ((= m (- RN 1))
                                (begin
                                        (set! s (+ wtr (list-ref spacings m)))
                                        (set! start end)
                                        (set! stop (+ start (- start stop)))
                                        (set! end (+ stop (* s 0.5)))
```

```
                                        (set! reg (string-append "Al_" (number->string m)))
                                        (sdegeo:create-rectangle (position (+ start 0.5)  0  0)
(position start  0.36  0) "Aluminum" reg )
                                        (sdegeo:create-rectangle (position (+ stop 0.5)  0  0)
(position  stop   0.36  0) "Aluminum" reg )

                                        (set! Elec (string-append "E" (number->string m)))
                                        (sdegeo:define-contact-set Elec 4  (color:rgb 0 1 0 )
"##" )

                                        (sdegeo:set-current-contact-set Elec)
                                        (sdegeo:define-2d-contact (find-edge-id (position (
+ start  0.1) 0 0)) (sdegeo:get-current-contact-set))
                                        (sdegeo:define-2d-contact (find-edge-id (position (
+ stop 0.1) 0 0)) (sdegeo:get-current-contact-set))
                                    )
                                )

                                ((= m -1)
                                    (begin
                                        (set! s (+ mesa wtr))
```

```
                                        (set! start end)
                                        (set! stop (+ start (- start stop)))
                                        (set! end (+ stop (* s 0.5)))

                                        (sdegeo:create-rectangle (position (- end 0.5)  0  0)
(position end  0.36  0) "Aluminum" "cont1" )
                                        (sdegeo:create-rectangle (position (- term 0.5)  0  0)
(position term  0.36  0) "Aluminum" "cont1" )
                                        (sdegeo:create-rectangle (position (+ stop 0.5)  0  0)
(position  stop   0.36  0) "Aluminum" "cont2" )

                                        (sdegeo:define-contact-set "source" 4  (color:rgb 0 1
0 ) "##" )

                                        (sdegeo:set-current-contact-set "source")
                                        (sdegeo:define-2d-contact (find-edge-id (position ( -
end  0.1) 0 0)) (sdegeo:get-current-contact-set))
                                        (sdegeo:define-2d-contact (find-edge-id (position ( -
term  0.1) 0 0)) (sdegeo:get-current-contact-set))
                                        (sdegeo:define-2d-contact (find-edge-id (position (
+ stop 0.1) 0 0)) (sdegeo:get-current-contact-set))
```

```
                    )
                )
                (else
                    (begin
                        (set! s (+ wtr (list-ref spacings m)))
                        (set! start end)
                        (set! stop (+ start (- start stop)))
                        (set! end (+ stop (* s 0.5)))

                        (set! reg (string-append "Al_" (number->string m)))
                        (sdegeo:create-rectangle (position (+ start 0.5)  0  0)
(position start  0.36  0) "Aluminum" reg )
                        (sdegeo:create-rectangle (position (+ stop 0.5)  0  0)
(position  stop   0.36  0) "Aluminum" reg )

                        (set! Elec (string-append "E" (number->string m)))
                        (sdegeo:define-contact-set Elec 4  (color:rgb 0 1 0 )
"##" )

                        (sdegeo:set-current-contact-set Elec)
                        (sdegeo:define-2d-contact (find-edge-id (position (
+ start  0.1) 0 0)) (sdegeo:get-current-contact-set))
```

(sdegeo:define-2d-contact (find-edge-id (position (

+ stop 0.1) 0 0)) (sdegeo:get-current-contact-set))

)

)

)

)

)

#(sdegeo:2d-cut (position 357.4 -5 0.0) (position 500 @Twafer@ 0.0))

(sde:set-meshing-command "snmesh -a -c boxmethod")

(sdedr:append-cmd-file "")

(sde:build-mesh "snmesh" "-a -c boxmethod" "n@node@")

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