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DESIGN OF NOVEL DEVICES AND CIRCUITS FOR ELECTROSTATIC DISCHARGE
PROTECTION APPLICATIONS IN ADVANCED SEMICONDUCTOR TECHNOLOGIES

by

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A dissertation submitted in partial fulfilment of the requirements
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ABSTRACT

Electrostatic Discharge (ESD), as a subset of Electrical Overstress (EOS), was reported to be in charge of more than 35% of failure in integrated circuits (ICs). Especially in the manufacturing process, the silicon wafer turns out to be a functional ICs after numerous physical, chemical and mechanical processes, each of which expose the sensitive and fragile ICs to ESD environment. In normal end-user applications, ESD from human and machine handling, surge and spike signals in the power supply, and wrong supplying signals, will probably cause severe damage to the ICs and even the whole systems.

Generally, ESD protections are evaluated after wafer and even system fabrication, increasing the development period and cost if the protections cannot meet customer's requirements. Therefore, it is important to design and customize robust and area-efficient ESD protections for the ICs at the early development stage. As the technologies generally scaling down, however, ESD protection clamps remain comparable area consumption in the recent years because they provide the discharging path for the ESD energy which rarely scales down. Diode is the most simple and effective device for ESD protection in ICs, but the usage is significantly limited by its low turn-on voltage. MOS devices can be triggered by a dynamic-triggered RC circuit for IOs operating at low voltage, while the one triggered by a static-triggered network, e.g., zener-resistor circuit or grounded-gate configuration, provides a high trigger voltage for high-voltage applications. However, the relatively low current discharging capability makes MOS devices as the secondary choice. Silicon-controlled rectifier (SCR) has become famous due to its high robustness and area efficiency, compared to diode and MOS. In this dissertation, a comprehensive design methodology for SCR based on simulation and measurement are presented for different advanced commercial technologies. Furthermore, an ESD clamp is designed and verified for the first time for the emerging GaN technology.

For the SCR, no matter what modification is going to be made, the first concern when drawing the layout is to determine the layout geometrical style, finger width and finger number. This problem for diode and MOS device were studied in detail, so the same method was usually used in SCR. The research in this dissertation provides a closer look into the metal layout effect to the SCR, finding out the optimized robustness and minimized side-effect can be obtained by using specific layout geometry. Another concern about SCR is the relatively low turn-on speed when the IOs under protection is stressed by ESD pulses having very fast rising time, e.g., CDM and IEC 61000-4-2 pulses. On this occasion a large overshoot voltage is generated and cause damage to internal circuit component like gate oxides of MOS devices. The key determination of turn-on speed of SCR is physically investigated, followed by a novel design on SCR by directly connecting the Anode Gate and Cathode Gate to form internal trigger (DCSCR), with improved performance verified experimentally in this dissertation. The overshoot voltage and trigger voltage of the DCSCR will be significantly reduced, in return a better protection for internal circuit component is offered without scarifying neither area nor robustness.

Even though two SCR's with single direction of ESD current path can be constructed in reverse parallel to form bidirectional protection to pins, stand-alone bidirectional SCR (BSCR) is always desirable for sake of smaller area. The inherent high trigger voltage of BSCR that only fit in high-voltage technologies is overcome by embedding a PMOS transistor as trigger element, making it highly suitable for low-voltage ESD protection applications. More than that, this modification simultaneously introduces benefits including high robustness and low overshoot voltage.

For high voltage pins, however, it presents another story for ESD designs. The high operation voltages require that a high trigger voltage and high holding voltage, so as to reduce the false trigger and latch-up risk. For several capacitive pins, the displacement current induced by a large snapback will cause severe damage to internal circuits. A novel design on SCR is proposed to minimize the snapback with adjustable trigger and holding voltage. Thanks to the additional a PIN

diode, the similar high robustness and stable thermal leakage performance to SCR is maintained.

For academic purpose of ESD design, it is always difficult to obtain the complete process deck in TCAD simulation because those information are highly confidential to the companies. Another challenge of using TCAD is the difficulty of maintaining the accuracy of physics models and predicting the performance of the other structures. In this dissertation a TCAD-aid ESD design methodology is used to evaluate ESD performance before the silicon shuttle.

GaN is a promising material for high-voltage high-power RF application compared to the GaAs. However, distinct from GaAs, the leaky problem of the schottky junction and the lack of choice of passive/active components in GaN technology limit the ESD protection design, which will be discussed in this dissertation. However, a promising ESD protection clamp is finally developed based on depletion-mode pHEMT with adjustable trigger voltage, reasonable leakage current and high robustness.

To my wife Jiaqi Tan, my parents Shikun Wang and Cuilian Guo, my parents in law Guozao Tan and Fengyi Yu.

ACKNOWLEDGMENTS

Model upgrade on the traditional TLP system.

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CHAPTER 1: INTRODUCTION

1.1 ESD Nature and Protection for ICs

Electrostatic Discharge (ESD) is a common phenomenon in the nature. It is regarded as a subset of Electrical Overstress (EOS) in reliability, comprising discharging stress with pulse widths from sub-microsecond to nanosecond. ESD event drives charges between two objects with various electrical potential or imbalanced charges, mainly resulting from triboelectrification, induction or conduction. Compared to normal switching signals in electronic systems, these discharging events can be extremely fast (in the order of nanoseconds) and contain high energy (with voltage up to a few kilovolts), leading to fatal failure in semiconductor devices and circuits. Major failures from ESD events include current induced damages such as thin film fusing, filamentation and junction spiking, and voltage induced damages such as charge injection and dielectric rupture [1]. Generally, it is nontrivial to diagnose and analyze the ESD-induced failures because one or more damages can be simultaneously active during the ESD event.

In order to protect the electronic systems from the ESD event, two types of design are widely adopted in semiconductor industry. On one hand, the protections are pre-developed along with the technologies, focusing on specific on-wafer design of devices and circuits that are placed on I/O pins and power supply pins domain. On the other hand, system level of protections are considered based on on-board components. No matter which one is applied, the key mechanism is to create a low-resistance path to bypass ESD energy in the form of current when ESD event happens.

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1.2 ESD Characterization Standards

ESD events are considered as the most significant factor to the early life failure and breakdown throughout the lifetime of ICs. Although specific protection circuits and devices are integrated in ICs, the effectiveness and robustness of the protections should be determined in a manner of guarantee for given applications. The ESD events could discharge amperes of current in a short period, typically from hundreds of picoseconds to hundreds of nanoseconds. For the purpose of repeatable and controllable ESD stress, four categories are broadly used for the ESD testing and characterization, according to the pulse rise and fall time, peak current, amount of energy, and the pulse duration.

1.2.1 Human Body Model (HBM)

HBM represents an ESD stress caused by a charged human discharging the current into the grounded ICs. Because the internal resistance of human is large (1.5 Kohm in average), the ESD event discharges relatively slow with low peak current. Such current pules normally rises in 2 to 10 ns, and falls in 150 to 200 ns. The peak current is typically 1.2 to 1.48 A for 2 kV HBM ESD stress. Different organizations, such as MIL-STD, JEDEC, ESDA, etc, will have their own standard models for HBM testing, and the parasitic parameters in the circuit will vary. Figure 1.1 represent the equivalent circuit of HBM, and Table 1.1 lists the common HBM ESD Component Classification Levels from ANSI/ESDA joint standard [2]. R=1500 ohm and C=100 pF are chosen in the equivalent circuit.
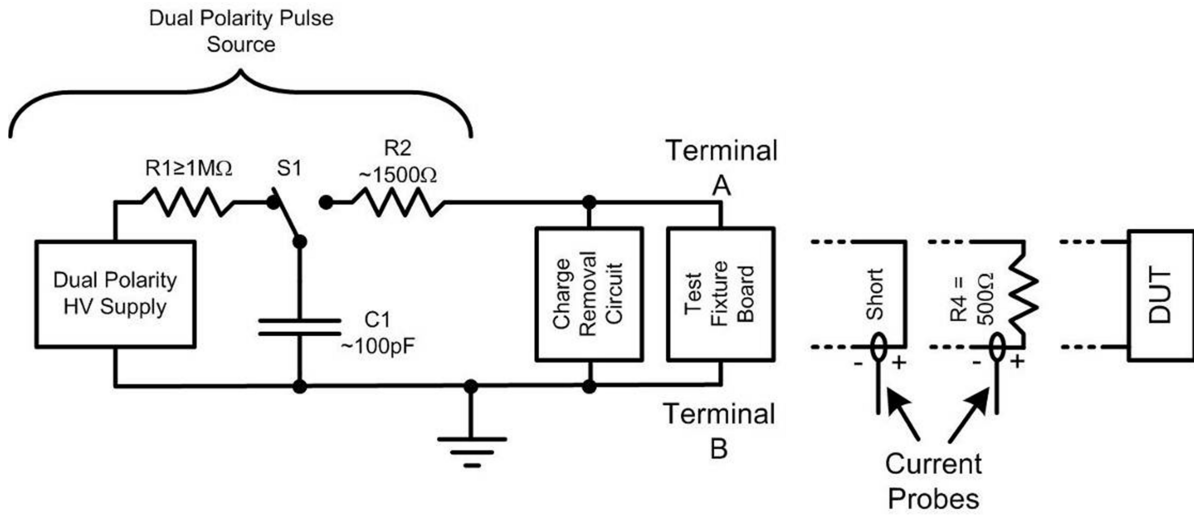
Figure 1.1: Equivalent HBM Simulator Circuit with Loads.

Table 1.1: HBM ESD Component Classification Levels.

Classification	Voltage Range (V)
0A	<125
0B	125 to <250
1A	250 to <500
1B	500 to <1000
1C	1000 to <2000
2	2000 to <4000
3A	4000 to <8000
3B	>8000

1.2.2 Machine Model (MM)

MM represents an ESD stress from a charged machine into the grounded ICs, which usually happens in automotive assembly lines. Due to the small parasitic resistance and large parasitic capacitance of metal, such kind of event discharges stress with similar rising time but much higher peak current, compared to HBM. One special characteristic of MM current waveform is the damped

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oscillation due to the parasitic inductance, whose negative portion may cause fatal failure in ICs. Same as HBM, the parameters of the equivalent circuit are distinct in various standard organizations. Figure 1.2 shows the equivalent circuit of the MM from ANSI standard [3].
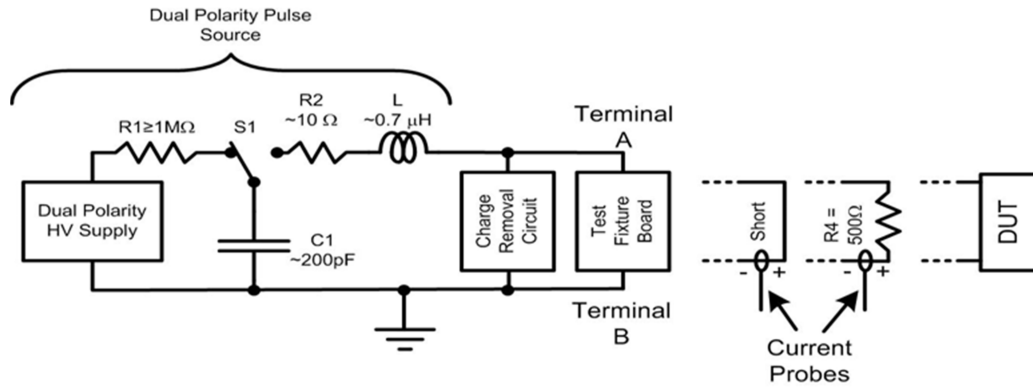
Figure 1.2: Equivalent MM Simulator Circuit with Loads.

1.2.3   Charged Device Model (CDM)

CDM describes an ESD stress from a self-charged IC during the manufacturing process when it contacts with ground or grounded equipments. Different from HBM and MM, the charge of CDM generally comes from contact-separation electrification and electric-field-induced electrification. With quite small internal resistance, the CDM event can discharge stress with very fast rising time and very high peak current. Theoretically, the rise time and hold time of CDM event can be 0.2 to 0.4, and 60 to 80 ns respectively, and the peak current can be up to 15-20 times more than those of HBM. Figure 1.3 shows the conceptual schematic of CDM tester, and Table 1.2 lists the common HBM ESD Component Classification Levels based on the ANSI standard [4].

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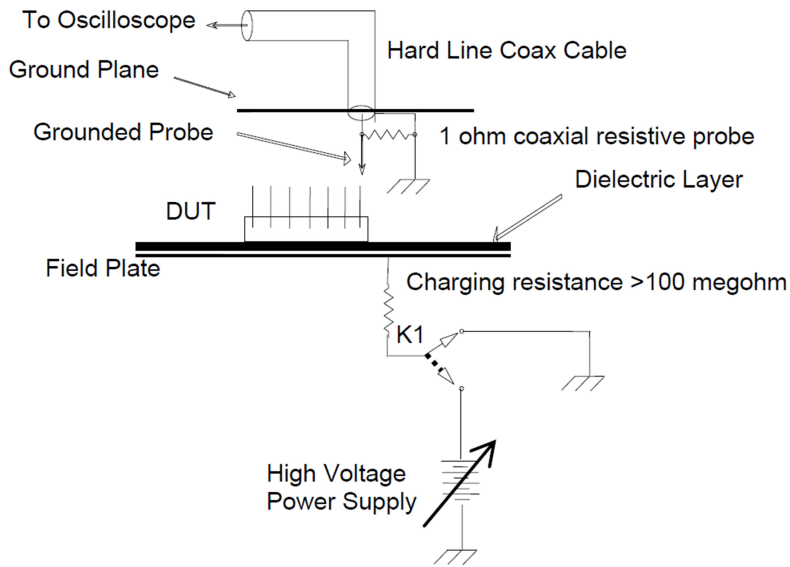
Figure 1.3: Conceptual Schematic of the CDM tester.

Table 1.2: CDM ESD Component Classification Levels.

Class	Voltage Range (V)
C1	<125
C2	125 to <250
C3	250 to <500
C4	500 to <1000
C5	1000 to <1500
C6	1500 to <2000
C7	≥ 2000

1.2.4 System Level IEC 61000-4-2

HBM, MM and CDM are standards specifically developed for component level ESD sensitivity testing so as to ensure effective and robustness ESD protection. However, these testing could be misunderstood and sometimes interchangeably used for system level ESD protection characterization. As a result, a protected system based on these standards fails later in consumer's applications.

Theoretically, component level ESD standards are designed for manufacturing environment, while system level one is mostly used to investigate ESD protection in end user environment. As the scale down of advanced technologies, the manufacturing geometries and stress levels that can cause ESD failures are decreasing. Since system level ESD stress usually carry large peak voltage and energy, it has been recommended to reduce the levels of on-chip ESD protection that is not sufficient for system protection, and to improve system reliability by using external ESD protection circuits.

IEC 61000-4-2 standard replicates the electrostatic discharge into a system in end user environment from a charged person. It defines two different testing methodologies: contact discharge and air discharge. Figure 1.4 shows the equivalent diagram of the ESD generator that generate the IEC 61000-4-2 compatible stress. Cd is a distributed capacitance between the generator and its surroundings. The typical value of Cd+Cs is 150 pF, while the one for Rd is 330 ohm. Table 1.3 lists the test levels for both contact and air discharges. "x" can be any level, and the corresponding special test voltage can be determined in the dedicated equipment specification [5].
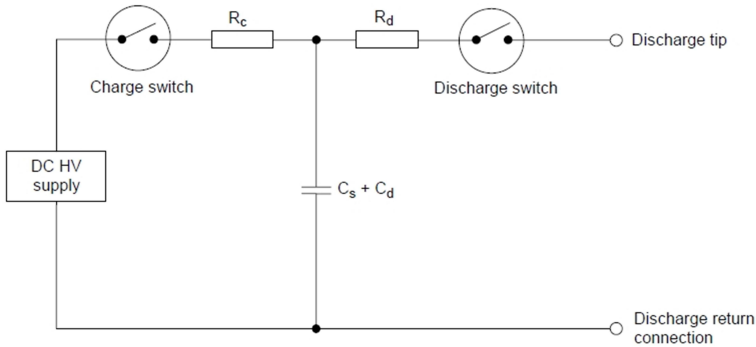
Figure 1.4: Equivalent diagram of the IEC 61000-4-2 generator.

Table 1.3: IEC 61000-4-2 Test Levels.

Contact Discharge		Air Discharge	
Level	Test Voltage (kV)	Level	Test Voltage (kV)
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15
x	Special	x	Special

1.2.5   Human Metal Model (HMM)

Nowadays, increasing number of customers will request system level classification, such as IEC 61000-4-2 rating for component level electronic products. However, system level ESD standard only defines how to test the system as a whole such as mobile phones and laptops. Therefore, ESDA released the HMM, replicating IEC 61000-4-2 waveform and it is completely compatible for component level ESD measurement. The ability of surviving in the system level IEC 61000-4-2 test of different components can be evaluated at an earlier development stage, such that the cost of re-design and re-manufacturing can be effectively minimized.

HMM simulates the ESD situation where the grounded IC is touched by a charged person via a metal objects. The typical waveform of HMM contains an initial current spike with 800+-200 ps rising time, followed by a current pulse with much long fall time of about 50 ns. Such initial current spike stems from the very low resistance in the metal, while the larger resistance in human body generates the broader current pulse. The pulse source of HMM can be the general IEC 61000-4-2 compliant ESD gun. However, due to the different design of circuit board and manufacturing variation, the IEC 61000-4-2 compliant pulse waveforms from distinct manufacturers exhibit deviations from each other. Therefore, it is critical to use the same ESD gun during the whole measurement period for repeatable test result [6] and [7].

1.2.6   Transmission Line Pulsing (TLP) Tester

Traditional extraction of IV characteristic from semiconductor devices are based on DC measurement. Thermal degradation and even breakdown happens in ESD investigation because of the self-heating effect from the inherent low-resistive current path created in ESD devices under DC condition. TLP, instead, provides the ability for accurate measurement and closer investigate at higher current level by using the short pulse (50 ns to 200 ns) measurement [8]. Furthermore, such short TLP pulses simulate the short ESD threats in the real world, resulting in good correlation of robustness to ESD model such as HBM.

Figure 1.5 shows the equivalent circuit for the most popular TLP tester. It uses the constant impedance transmission line in the pulse source to reduce the degradation in the pulse rise time [9]. Time Domain Reflection (TDR) technique is commonly used in the commercial TLP tester, where the current and voltage signals are measured at the same location. Improved version of TLP using Time Domain Reflection-Transmission (TDRT) technique is proposed for flexible adjustment in the impedance, which should be increased from 50 ohm to higher value, e.g., 500 ohm, for closer illustration of the snapback behavior of high voltage ESD devices in static IV characteristic [10]. The charged capacitor discharge energy via the transmission cable with 50 ohm impedance and generate a flat-top rectangular pulse. As shown in Figures 1.6 and 1.7 are the square voltage and current pulses with 100 ns width and 20V pre-charged voltage captured from TLP system on an OEPN. The TDR technique overlaps the transmission and reflection pulses and a certain calibration will be applied by the system to generate the accurate data. A portion of data points on the flat-top region are averaged so that the static IV points are calculated to plot the static TLP IV curve.
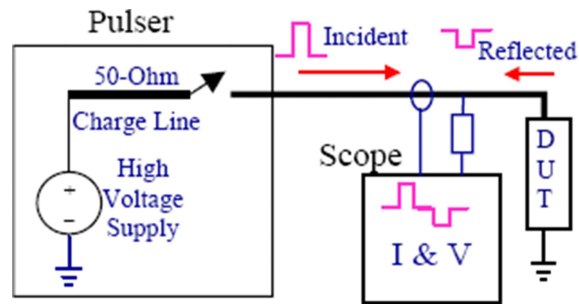
Figure 1.5: Equivalent circuit of TDR TLP tester with 50 ohm impedance.
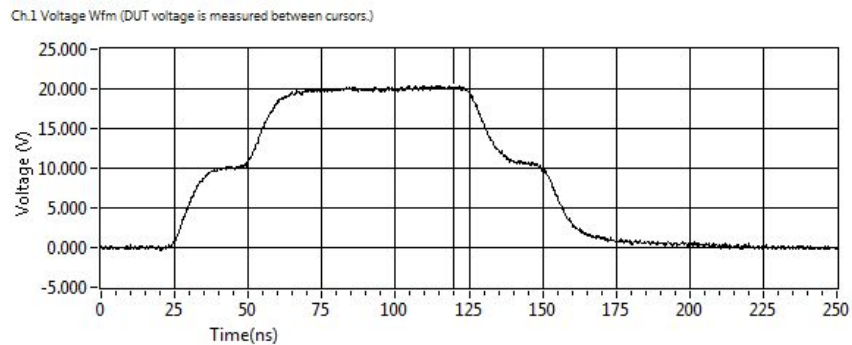
Figure 1.6: TLP-measured voltage waveform with 20V pre-charged voltage on an OPEN.

1.2.7   ESD Test Methods

The ESD robustness of IC products are investigated using the ESD characterization standards before delivered to customers, such that their ESD protection capabilities are guaranteed. HBM, MM and CDM are three traditional standards that are widely used and accepted in the market. A typical set of requirement have the product under test 2000V, 200V and 750V for HBM, MM and CDM respectively.

In the fabrication and delivery process, the ESD damage can be caused by positive or negative

charges, requiring that the pins in the product are clearly evaluated by positive and negative ESD stresses. Due to the distinctions of pulse generation and discharging, HBM and MM tests are classified to three categories (pin-to-pin, pin-to-power and power-to-power). However, direct discharge and field-induced discharge are the two major categories for CDM test, performed on the CDM tester shown in Figure 1.3.

In pin-to-pin test , the ESD stress is injected to one I/O pin of the product, while another I/O pin is grounded. Therefore, two types of test modes, which are the positive mode and negative mode, are consequently classified. During the test, all the I/O pins are also grounded so as to reduce testing time, even though the discharge usually happens between one single pin to another. However, power pins are configure to be floating since such ESD events take place when the products are un-powered. Figures 1.8 and 1.9 show the equivalent testing diagrams.

In pin-to-power test, considering the two power supply (VDD and VSS), four types of testing modes, which are positive-to-VDD, negative-to-VDD, positive-to-VSS, negative-to-VSS, must be evaluated individually. Shown in Figures 1.10, 1.11, 1.12 and 1.13 are the equivalent testing diagrams. It should be noted that all the other I/O and power pins are configured to be floating.
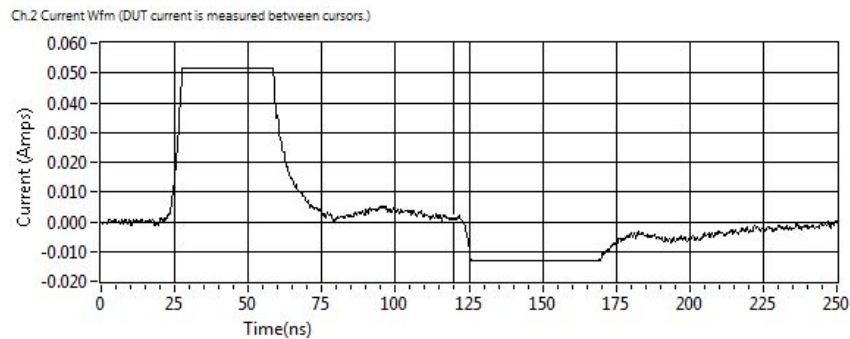
Figure 1.7: TLP-measured current waveform with 20V pre-charged voltage on an OPEN.
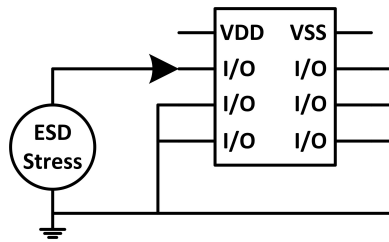
Figure 1.8: Positive pin-to-pin ESD test mode
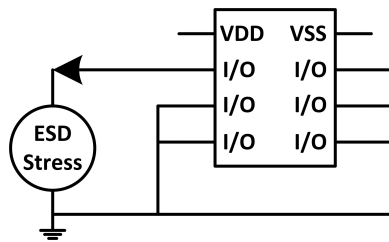
Figure 1.9: Negative pin-to-pin ESD test mode

In power-to-power pins, only VDD and VSS are considered, resulting in positive and negative modes shown in Figures 1.14 and 1.15. During the test, all the I/O pins are configured to be floating.
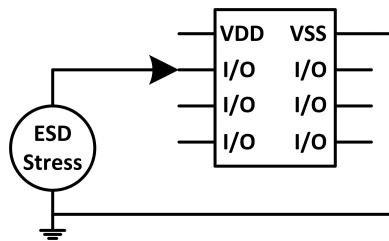
Figure 1.10: Positive-pin-to-VSS ESD test mode
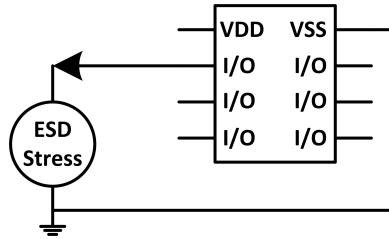
Figure 1.11: Negative-pin-to-VSS ESD test mode
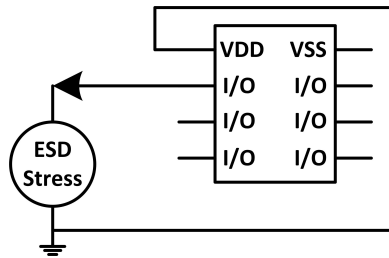
Figure 1.12: Positive-pin-to-VDD ESD test mode

1.3 ESD Protection Performance Criteria

1.3.1 Static Performance

In order to characterize the performance of the on-chip ESD protection, the typical ESD design window for the device operations is shown in Figure 1.16 based on TLP measurement. In voltage regime, V_{MAXOP} is the maximum operation voltage of the power supply line, while the V_{MAXABS} is considered as the absolutely maximum voltage, which takes account of the overlap of the voltage spike and noisy signals. $V_{FAILURE}$ is equal to the upper voltage limit of the pins under protected, over which the internal circuits will be damaged.

According to the operation behavior, the ESD protections can be classified into two types: no-

snapback versus snapback. On the I-V plane, the black line curve represents the I-V characteristics of traditional snapback ESD device such as grounded-gate MOS (ggMOS) and Silicon-controlled Rectifier (SCR) with important performance matrix, including breakdown point (breakdown voltage V_{BD}, breakdown current I_{BD}), trigger point (trigger voltage V_{t1}, trigger current I_{t1}), holding point (holding voltage V_h, holding current I_h), and the thermal-induced secondary breakdown point (V_{t2}, I_{t2}). The blue line, instead, represents the no-snapback IV characteristic from ESD devices such as diode with key ESD matrix of rigger point (V_{t1}, I_{t1}) and and the thermal-induced secondary breakdown point (V_{t2}, I_{t2}). For both cases, I_{t2} is considered as the robustness of the on-chip ESD protection.

Technically, four criteria must be completely satisfied for a successfully on-chip ESD protection design.

1) V_{BD} and V_{t1} should be larger than V_{MAXABS} to limit the occurrence of false trigger and reasonable leakage current under normal circuit operations.

2) V_{t1} and V_{t2} should be smaller than $V_{FAILURE}$ to protect internal circuits.

3) V_h for snapback devices should be larger than V_{MAXABS} to immune latch-up effect.

4) I_{t2} should be reach specific values so that the ESD protections meet industrial standards.
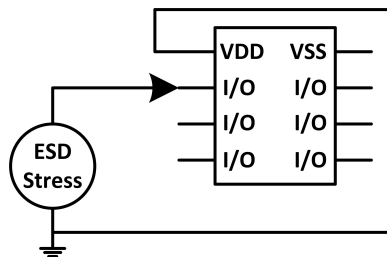
Figure 1.13: Negative-pin-to-VDD ESD test mode
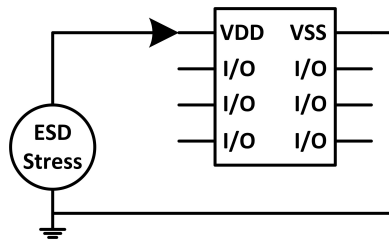
Figure 1.14: Positive-VDD-to-VSS ESD test mode
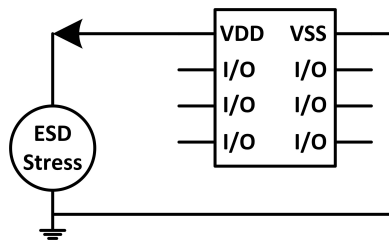
Figure 1.15: Negative-VDD-to-VSS ESD test mode

1.3.2 Dynamic Performance

While the TLP tester offers the capability to evaluate the static performance and good correlation to the HBM level, its measurement mechanism and relatively-slow rising time limit to illustrate the dynamic performance of the ESD protection. VF-TLP, instead, measures the real transient waveforms from the separated transmitted and reflected pulse. It can generate pulse with very fast rising time in sub-nanosecond regime to simulate real-world stress like CDM. In such situation, the turn-on behavior of the ESD protection can be clearly studied, by using dynamic design matrix including turn-on time T_{on} and overshoot voltage $V_{overshoot}$.

Similar to TLP measurement, four criteria must be completely satisfied for a successfully on-chip ESD protection design.
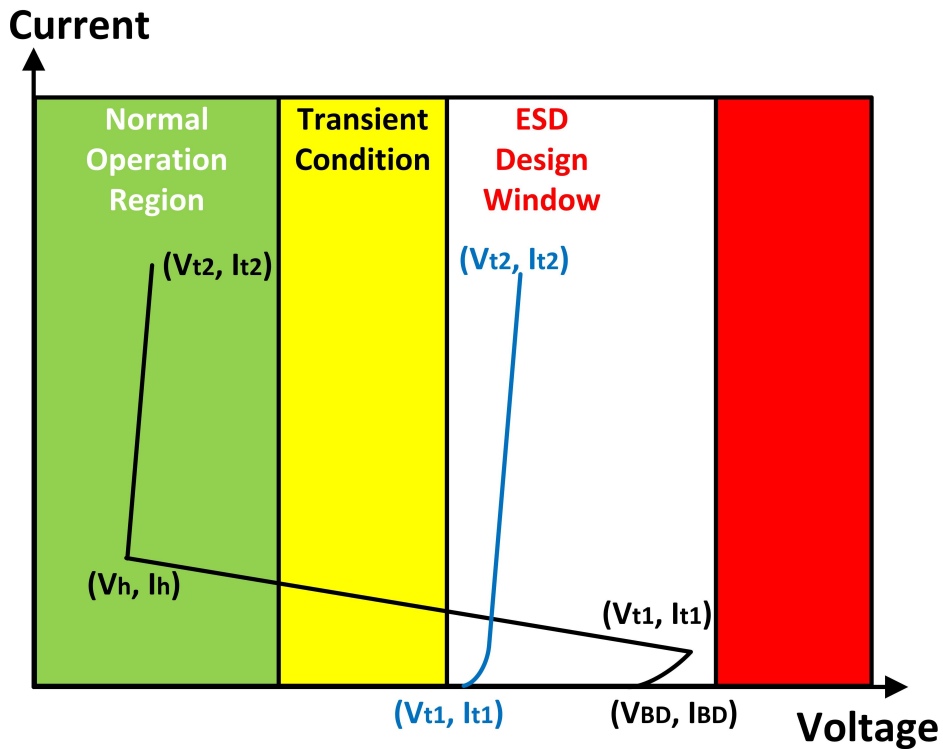
Figure 1.16: Typical ESD Design Window.

1) T_{on} should be small enough to ensure the quick response to fast pulse like CDM.

2) $V_{overshoot}$ should be smaller than the $V_{FAILURE}$ defined specially by the technology.

The dynamic performance of ESD protection becomes very important as the development of the advanced manufacturing technologies scales down the oxide thickness of the MOS devices, which mainly determine the $V_{FAILURE}$ in ESD design window. Figure 1.17 clearly shows the continuous decrease of $V_{FAILURE}$ of the gate oxide and the slower reduction of the circuit operation voltage, dramatically shrinking the ESD design window [11]. Additional consideration should be taken although the ESD protection has good enough HBM immunity.

1.4 ESD Protection Strategy

A single IC contains multiple I/O and power supply pins for different application purpose, so the ESD protection should be considered ad planned not only on device level but also on chip level. Since the basic idea of ESD protection is to form a low-resistive path for discharging between the stressed pin and ground, rail-based and localized pin-based ESD protections are verified to the effective.
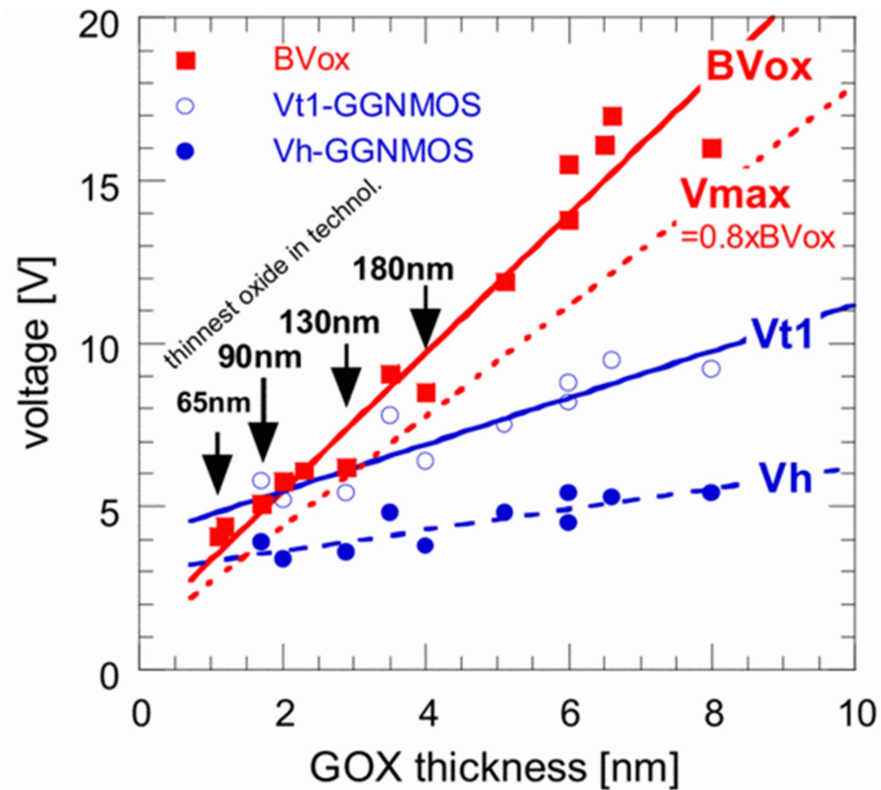
Figure 1.17: Transient breakdown of MOS gate oxide versus oxide thickness.

1.4.1 Rail-based ESD Protections

The rail-based ESD protections utilize the power supply rail (VDD and VSS) to assist the ESD discharge. As shown in Figure 1.18 is an example of such method, in which the ESD discharging path includes two clamps between I/O pins and power supplies, and one major clamp between the two power supplies. Therefore, a close loop connecting I/O and power pins is formed for effective ESD protection. The clamps between power supplies are usually placed across the whole chip. A larger rail resistance will hurt the ESD performance if the clamp is distributed far away from I/O pins.Therefore, the trade-off between the its placement and the area should be carefully considered.
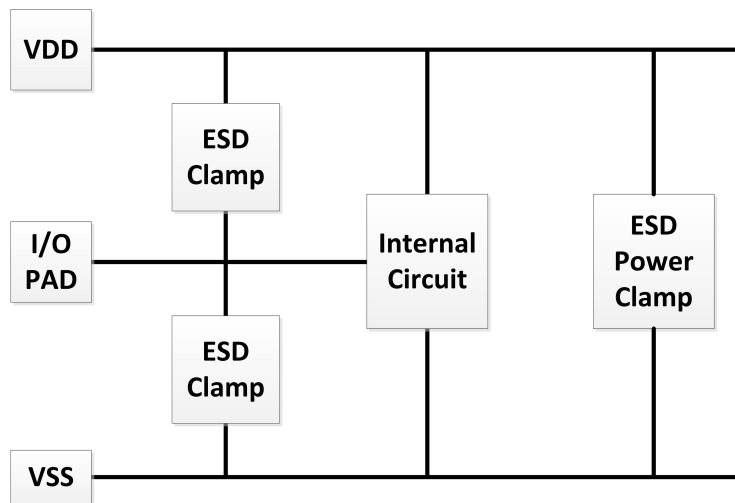
Figure 1.18: Conceptual diagram of rail-based ESD protection.

1.4.2 Localized ESD Protections

The ESD clamp can also be placed beside or under the PAD for localized and effective protection, as shown in Figure 1.19. This is usually used in chip with small pin number. A bidirectional clamp in this protection is capable of further reducing the area but at the same time increase the design

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difficulties of the clamp.
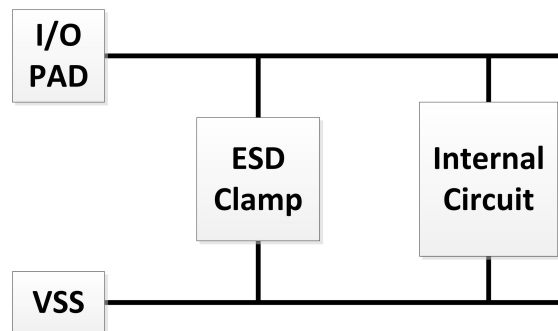
Figure 1.19: Conceptual diagram of localized ESD protection.

1.5 Conclusion and Remark

This chapter briefly discusses the industrial ESD standards and fundamental knowledge of successfully ESD protection design for semiconductor technologies. Due to the difference between various technologies, ESD protection designs are still quite customized and specialized.

CHAPTER 2: LAYOUT OPTIMIZATION FOR SILICON-CONTROLLED RECTIFIER

We investigate the geometry layout and metal pattern in order to seek robust and optimized electrostatic discharge (ESD) performance for the silicon controlled rectifier (SCR). Parallel and crossing topologies, and different emitter lengths of the parasitic bipolar transistors, finger widths, and finger numbers are shown to significantly affect not only the ESD robustness but also the holding voltage of SCR. This paper provides useful guidelines to ameliorate the SCR performance for ESD protection applications.

2.1   Introduction

Silicon-controlled rectifier (SCR) has been thoroughly investigated and verified to be a promising candidate for constructing effective electrostatic discharge (ESD) protection solutions because of its high area efficiency and robustness, compared to the other counterparts such as ggMOS. Plenty of research work were done on the improvement of its triggering technique [12], latch-up immunity [13] and [14], uniform trigger [15] and [16], and high turn-on speed [17]. It was commonly performed that the similar layout mechanism can be also applied to SCR based on previous research results of diode and ggMOS. Therefore, very limited work has been done about the influence of geometry layout and metal pattern to SCR's ESD performance. Parallel and crossing metal patterns of SCR were compared in [18], but no geometry-related issue nor the optimization of robustness were covered. The work in [19] discovered that the incorrect allocation of anode and cathode in the the individual finger of SCR would cause dramatic degradation on the current distribution and even robustness. Other research in [20], [21] and [22] just studied the geometry and metal pattern effect of diode on ESD protection capability. Therefore, a general instruction

about how to draw the layout for optimum performance is expected to be very specific and unique for SCR, because its operation mechanism is completely distinct from the other counterparts.

In this chapter, we conduct a comprehensive study geometry layout and metal pattern based on the most typical lateral SCR (LSCR), and find out how they affect it's ESD protection capability. The findings reveal an interesting consequence and thus very useful optimization guidelines for ESD applications of SCR can be given finally, which will be applied to the research of SCR in the next two chapters.

2.2   Geometry and Metal Pattern of LSCR

LSCR devices fabricated in a 0.18 μm CMOS technology are used to this work. According to [19], cathode-anode-cathode configuration are used in these devices to minimize the current non-uniformity effect, as shown in Figure 2.1 is the cross-section view of transitional LSCR. As a result, two parallel SCR current paths exist in such configuration. Since it is a twin-well based technology, no deep well/region is needed for substrate isolation. Metal 1 covers The active regions of SCR are fully covered by Metal 1 via the plugs, while Metal 2 to Metal 4 are used to connect the Anode and Cathode of the LSCR to PADs, such that the series metal resistance in the current path can be minimized.

The parallel and crossing topologies for metal routing are compared to each other in Figures 2.2 and 2.3. They lead to different current flow direction between the bulk and the back-end metal of LSCR. As shown in Figure 2.2, after trigger, the current flow of LSCR in the Anode and Cathode metals is perpendicular to that in the SCR bulk region. Instead, for the crossing topology, the current shown in Figure 2.3 will flow in the same direction in the Anode and Cathode Metals as that in the SCR bulk region.
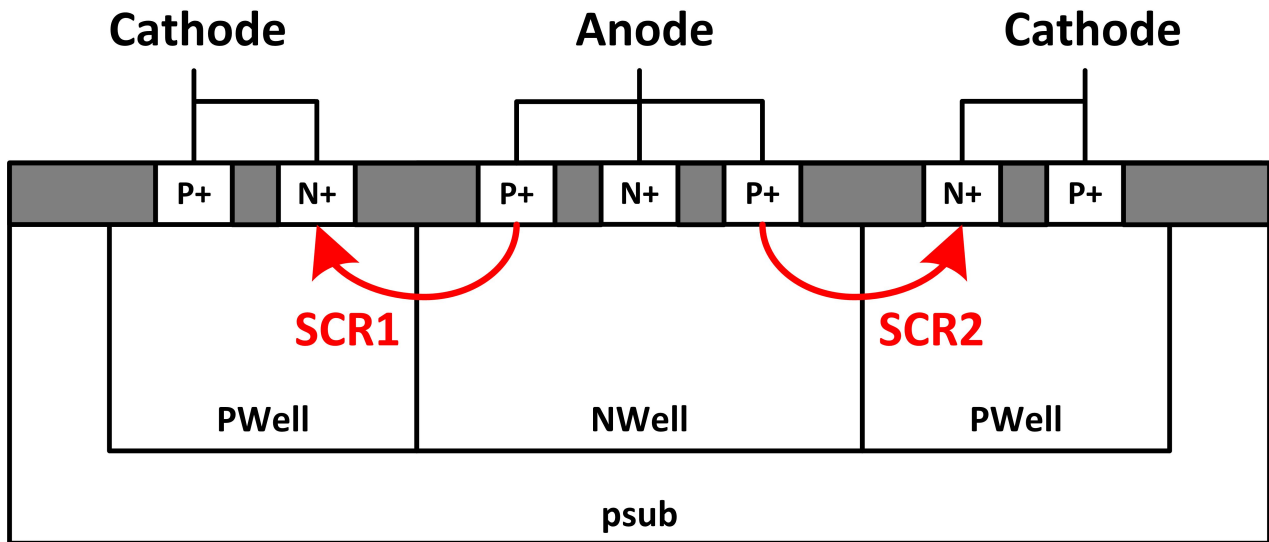
Figure 2.1: Cross-section view of traditional LSCR.

Three critical parameters, the length of parasitic bipolar transistors in LSCR, defined as Le, the width of each finger, defined as W, and the total number of finger, defined as N, will be investigated and optimized for the SCR's ESD protection performance. It should be noted that N is also equivalent to the number of current paths in the SCR. For example, in Figure 2.1, two SCR current paths exist and hence N=2 for this case. A Barth 4002 TLP tester generating square pulses with a 10 ns rising time and a 100 ns pulse width was utilized to evaluate the ESD performance of SCR devices. The robustness, or the failure current It2, and related current density Jt2 of the measured devices were extracted when the leakage current increases more than three orders of from its original magnitude.
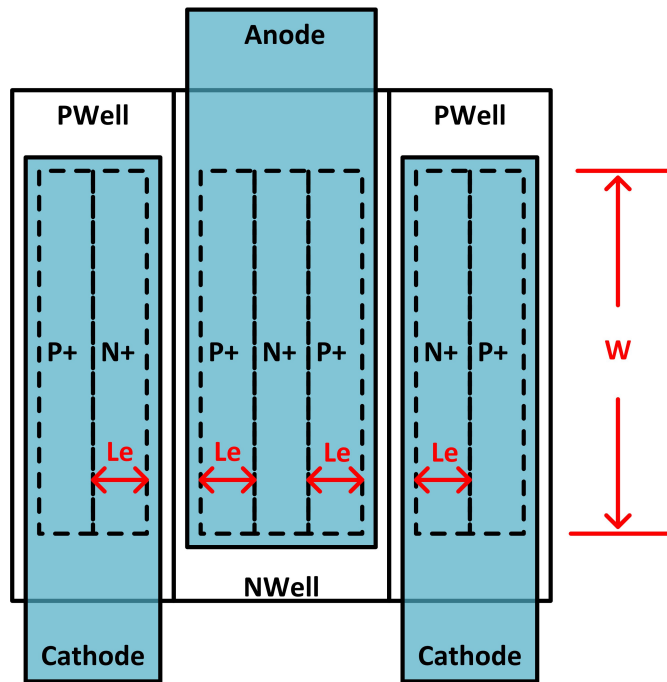
Figure 2.2: Metal routing of SCR for parallel topology. W denotes the finger width. Le denotes the emitter lengths of bipolar transistors in SCR. Patterns in blue denote metal connections between SCR and Pads.

2.3 Results and Discussions

Figure 2.4 shows the TLP I-V curves with leakage currents from Barth 4002 TLP tester. 1.8V DC voltage is applied between Anode and Cathode for post-stress DC leakage current measurement. Both parallel and crossing topologies have the same parameters of W=40 μm, N=2, and Le=0.9 μm. From the Figure 2.4, very little variation can be observed on the important ESD matrix, including trigger voltage, holding voltage, robustness, and leakage current. However, when the parameters change, the ESD performances of SCR for these two different topologies are distinct from each other. Figure 2.5 compares the robustness It2 and the corresponding failure current density as a function of W for both parallel and crossing topologies with a finger number N=2

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and an emitter length Le=0.9 μm. It clearly shows that the robustness depends linearly on W for both topologies, because the larger the device's width, the higher the heat dissipation and thus the current conduction capability. However, it is interesting that the failure current density actually degrades when increasing W for both cases. Such a degradation indicates that all the fingers in the SCR may not be simultaneously triggered on when a relatively large W is used. Another interesting phenomenon is also illustrated in Figure 2.5, suggesting that the parallel topology can sustain a higher current density than the crossing topology when W is less than 20 μm. However, this advantage is diminished if W is larger than 20 μm.

Results in Figure 2.6 indicate that increasing N increases the SCR robustness for both topologies with W=20 μm and Le=0.9 μm. However, a current degradation trend for both topologies is observed when increasing the finger number. This is due to the non-uniform current distribution within the various fingers when a relatively large N is employed.
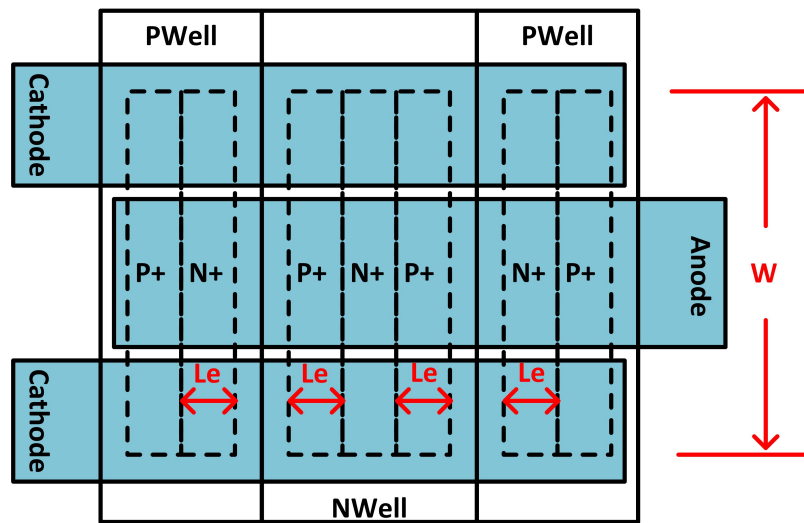
Figure 2.3: Metal routing of SCR for crossing topology. W denotes the finger width. Le denotes the emitter lengths of bipolar transistors in SCR. Patterns in blue denote metal connections between SCR and Pads.

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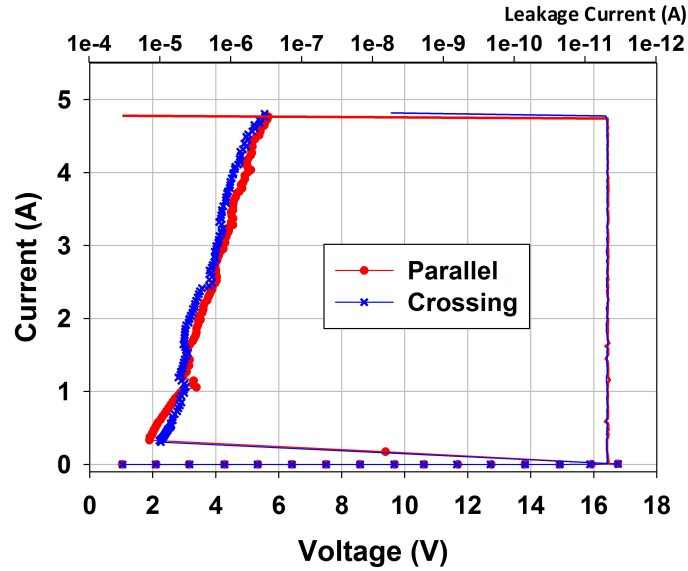
Figure 2.4: TLP I-V curves with leakage current measurement for parallel and crossing topologies with W=40 μm, N=2 and Le=0.9 μm.

Figure 2.7 shows the failure current density for both parallel and crossing topologies having the same total width (equal to W*N=40 μm) but various N and W combinations. Obviously with the fixed total width of SCR, the current densities peak for both topologies in the case of using two fingers, which is exactly the same cathode-anode-cathode configuration shown in Figure 2.1. For the case of N larger than 2, the non-uniform current distribution in multiple fingers becomes prominent, which results in the current density degradation. Furthermore, the parallel topology has a larger degradation than the crossing topology, but the difference tends to become smaller when increasing N. On the other hand, when N is reduced from 2 to 1, which is the single anode-cathode configuration, the current densities for both topologies also degrade. This is a result of the fact that there is only one current path in the SCR. Therefore, for a fixed total width, the use of two fingers in cathode-anode-cathode configuration will be beneficial to obtain the highest robustness/area efficiency.

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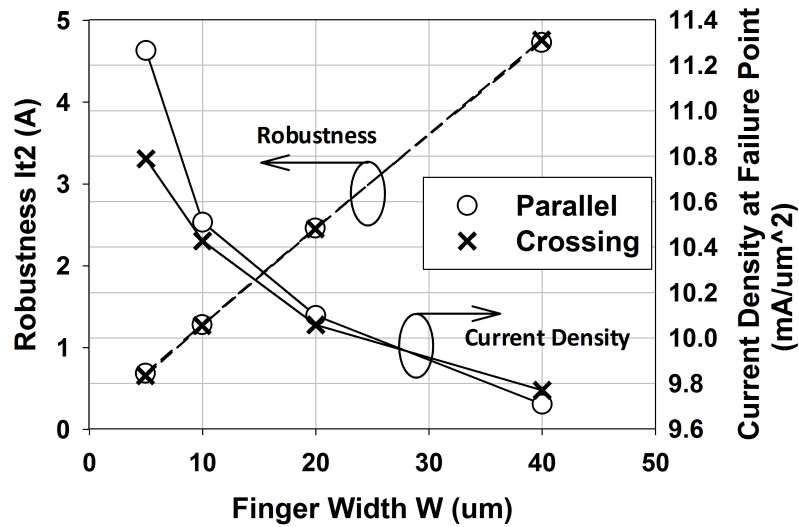
Figure 2.5: Robustness and Current Density versus Device Width W for parallel and crossing topologies. Finger number N=2 and emitter length Le=0.9 μm.

When the SCR enters the snapback region, the emitter length Le affects the SCR's conductivity modulation and thus the holding voltage [23]. A similar effect can be observed and depicted in Figure 2.8. The parallel topology shows a linear dependency of holding voltage Vh on Le. However, there is a risk of inducing the latch-up when using the crossing topology if Le is larger than 3 μm, due to the fact that Vh is lower than the power supply VDD which is 1.8V. Moreover, we also found Le will greatly affect the current density. The larger the Le, the larger the current densities for both topologies, but such trends tend to saturate when Le is larger than 3 μm. Beyond this, increasing Le will degrade the current density. Therefore, when optimizing the current density and holding voltage, using Le=2 μm would be a good choice, and it corresponds to two contact columns in the active region in this technology. Trigger voltage and leakage current are another two important figures of merit for evaluating the ESD protection performance of SCR. However, no significant influence is found on them when varying the layout geometry or the metal pattern. It should be pointed out that the measured leakage current for all devices are at the typical pA level.

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2.4 Conclusion and Remark

Geometry and metal pattern effects on the ESD robustness of SCR were investigated. Both parallel and crossing topologies showed similar robustness dependencies on the geometric parameters. For a relatively small finger width W, the parallel topology demonstrated a higher robustness and better latch-up immunity than the crossing topology. However, the crossing topology yielded a higher robustness when using a relatively large finger width, but at the expense of a smaller holding voltage. Moreover, increasing the finger width W and finger number N will actually degrade the current density at the failure point for both topologies. It was concluded that a geometry of two fingers, cathode-anode-cathode configuration, and two contact columns can offer the optimized ESD performance of SCR.
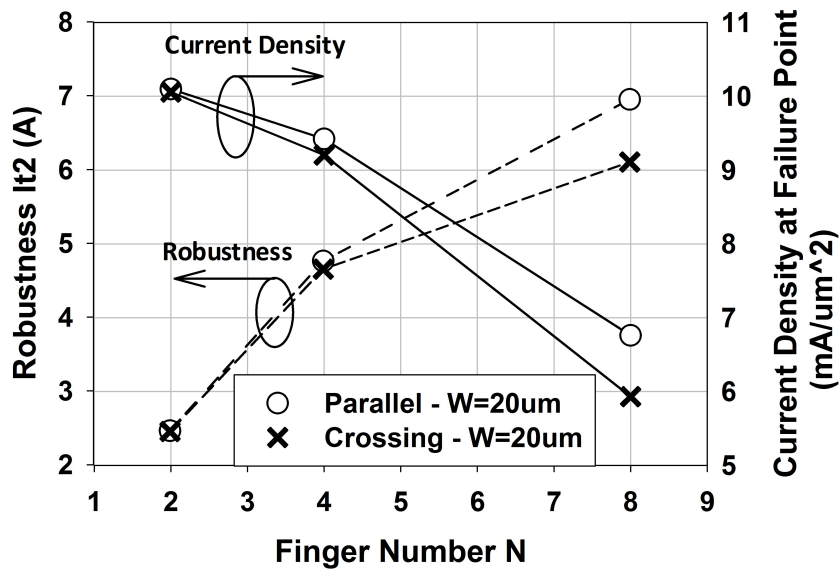
Figure 2.6: Robustness and Current Density versus Finger Number N for parallel and crossing topologies. Device width W=20 μm and emitter length Le=0.9 μm.
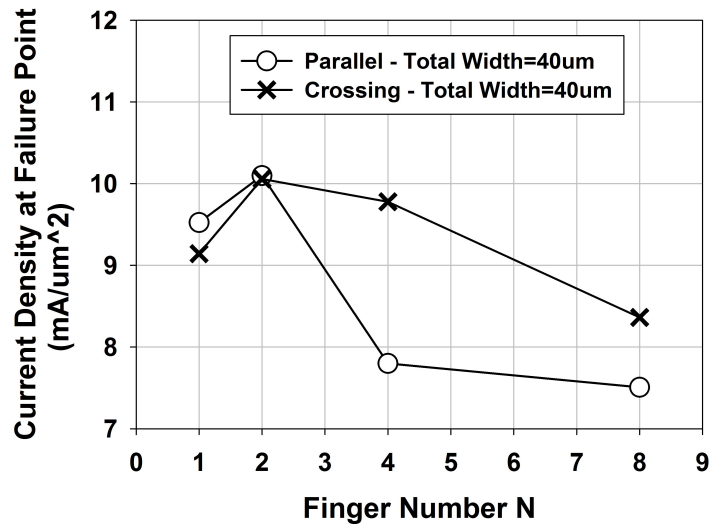
Figure 2.7: Current Density versus Finger Number N for parallel and crossing topologies. Total width (W*N) is fixed at 40 μm when changing the finger number.
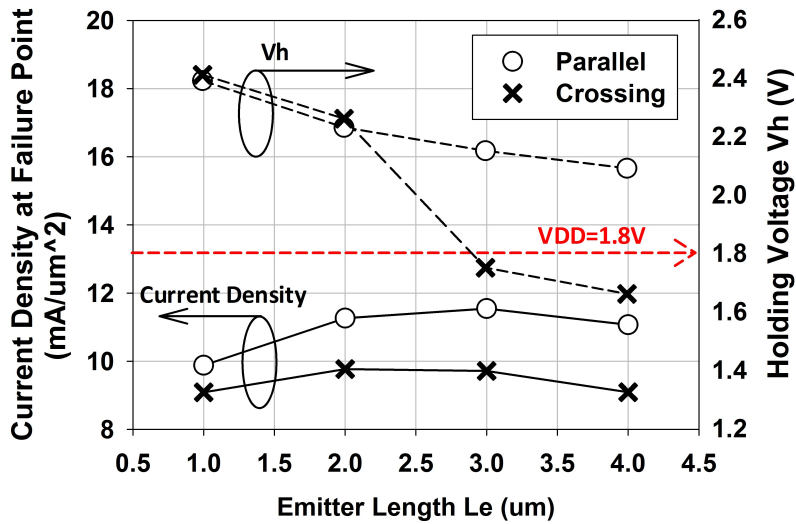
Figure 2.8: Current Density and Holding Voltage versus Emitter Length Le for parallel and crossing topologies.

CHAPTER 3: HIGH SPEED ESD PROTECTION DESIGN FOR LOW-VOLTAGE CMOS TECHNOLOGY

An electrostatic discharge protection structure constructed by the stacking of multiple anode gate-cathode gate directly connected silicon controlled rectifiers, called the DCSCRs, fabricated in a 0.18 μm CMOS technology is studied in this chapter. Two parasitic diodes in the DCSCR dictate the turn-on mechanism and hence give rise to a trigger voltage equal to twice the diode's turn-on voltage. This approach enables the DCSCR to offer a diode-like TLP IV characteristic with a minimal snapback and at the same time improves the voltage step-up capability and offers a SCR-like high ESD robustness. This internal-triggering mechanism simultaneously turn on the parasitic bipolar transistors in SCR, booting up the SCR's speed of response to fast-rising pulses, as a consequence the overshoot voltage can be dramatically reduced. Finally, an ESD clamp constructed by stacking a selected number of DCSCRs can offer a flexible trigger/holding voltage and is highly suitable for low and medium voltage ESD protection applications.

3.1 Introduction

Electrostatic Discharge (ESD) induced failure is a major concern for the Metal-Oxide-Semiconductor (MOS) transistor based integrated circuits in main-stream technologies. This reliability issue is further worsened in advanced technology including sub-micron Complementary-Metal-Oxide-Semiconductor (CMOS) with very low operation voltage. Nowadays, there has been a growing demand for the availability of robust ESD protection solutions for advanced and main-stream technologies that are capable of operating in a very narrow ESD design window. Silicon Controlled Rectifier (SCR) is a typical apparatus for ESD protection. Figure 3.1 shows the cross-section view and equivalent circuit of the traditional SCR. It is an old fashion to name the four nodes, which are

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SCR's electrical terminals, to be "Anode Gate" (AG), "Anode", "Cathode Gate" (CG), "Cathode". In this typical SCR, AG and Anode are tied together and connected to pin under protected. On the other hand, CG and Cathode are tied together and connected to GND.
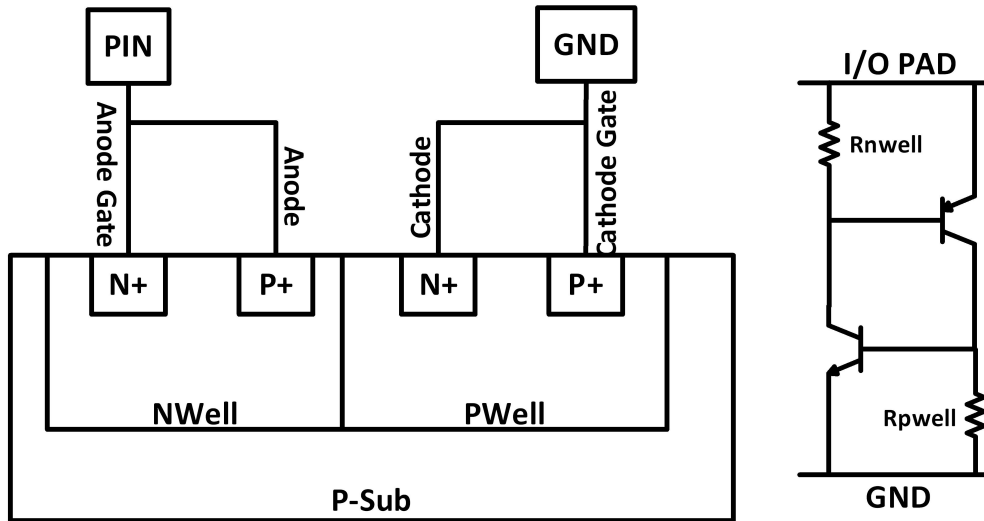
Figure 3.1: Cross-section view and equivalent circuit of traditional SCR.

When the ESD event happens on the pin subject to the ground, voltage builds up and the middle NWell/PWell junction sustain the major electric field, where the impact ionization starts to generate electrons and holes that are able to move freely. When it reaches a critical electric field value, a chain-effect, which is called avalanche breakdown, gives born to large quantity of such free excess carriers. Electrons flow to pin and holes flow to ground, creating voltage drops in the well regions, and thus the SCR is turned on as the parasitic bipolar transistor operations dominate. Since this triggering mechanism relies on the junction breakdown, a relatively high trigger voltage is required (e.g., in 0.18 μm technology, the junction breakdown voltage equals to 10-16V, depending the combination and doping concentration). However, at the specific point when SCR is triggered, the voltage drop between pin and ground, which is called holding voltage, is a combination of a saturation voltage between collector and emitter in a bipolar transistor, and a threshold voltage of

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a diode (e.g., VCE of PNP and VBE of NPN in Figure 3.1). Therefore, a snapback region always exists in the usual TLP IV curve.Such triggering mechanism also limits the turn-on speed of SCR because of its complicated processes, which can be divided into four steps.

STEP 1: Impact ionization and avalanche breakdown in the middle revere bias junction. In Figure 3.1 it is NWell/PWell junction.

STEP 2: Free carriers flow thought well regions and generate voltage dorp.

STEP 3: One of the parasitic bipolar transistors (typically it is NPN) start to inject carriers into well regions, modulating their conductivity and start the SCR operation.

STEP 4: Another parasitic bipolar transistors (typically it is PNP) is triggered and start to inject carriers into well regions, strongly modulating their conductivity and start the SCR operation.

These characteristics of SCR will introduce two critical problems. On one hand, the ESD in the environment will not scale down even though size of ICs keep decreasing, following the famous Moore's Law nowadays. The thinner gate oxide set up a lower gate oxide breakdown voltage, which significantly decrease the upper limit of available ESD design window. On the other hand, the ICs with small scales become very fragile and sensitive to the electrical overstress, e.g., over-shoot voltage, which can be generated simply by the ESD protection device in ESD event due to its low turn-on speed.

Plenty of works have been done to improve the triggering performance of SCR, and the major concept is to use external triggering techniques. For example, the work in [12] summarized various techniques for reducing the SCR's trigger voltage, but this come at the expense of a larger area. A typical realization is to use diode to trigger the SCR [24], and its equivalent circuits are shown in Figure 3.2. In this structure the trigger voltage is determined by the number of diode that are used in the external diode string. However, this method do little help on improving the turn-on speed

in fast-rising pulse because only one bipolar transistor is triggered at a time. Substrate trigger technique was proposed to trigger both parasitic bipolar transistors at the same time in [25] but it also needs a complicated design of external trigger circuit. Recently a gate-bounded structure is used to increase the turn-on speed of SCR, in which a high-K metal gate is required to compress the leakage current [17].
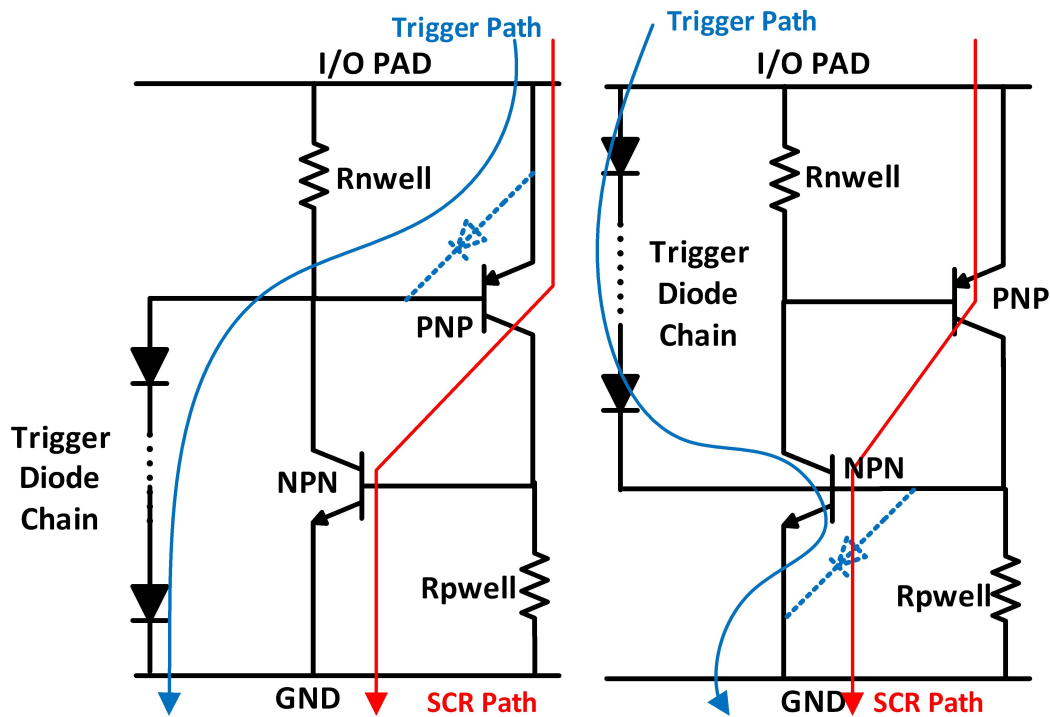
Figure 3.2: Equivalent circuit of diode-triggered SCR.

In this chapter an SCR-like device, called the direct-connected SCR (DCSCR), with the anode gate and cathode gate terminals connected together, is studied to fulfill objectives of the low-trigger voltage and fast turn-on speed. Meanwhile, Absence of a sizable snapback, the structure's trigger and holding voltages can be easily tuned by stacking a different number of DCSCRs, giving rise to an attractive ESD clamp with a proper trigger voltage, proper holding voltage, near-zero snapback

window, high robustness, and minimal number of cells required for low and medium voltage ESD applications.

3.2 Direct-connected SCR

Figure 3.3 shows the cross-section view and equivalent circuit of the DCSCR unit cell, whose top view of layout is represented in Figure 3.4. It can be easily realized in advanced and main-stream low-voltage semiconductor technologies with simple modification on the back-end layers. Like the traditional SCR (see Figure 3.1), the A and C terminals of DCSCR are connected to the pin and ground, respectively. In addition, the AG and CG terminals of the DCSCR are connected together using a metal layer. Such a connection gives rise to two internally connected PWell/N+ and NWell/P+ diodes. On top of that, the parasitic NPN and PNP transistors can be simultaneously triggered. Note that the PWell is not grounded and thus the deep NWell (DNW) is needed and used for substrate isolation. The DNW also increase the effective base width of the vertical parasitic PNP transistor, so that the carriers injected into the substrate can be greatly reduced. The red arrow in Figure 3.3 illustrates the internal trigger current, which flows through the two parasitic diodes in the DCSCR. When the voltage at the A terminal is larger than twice of the diode's turn-on voltage, the P-emitter connected to the A terminal and the N-emitter connected to the C terminal start to inject free carriers into the base regions (i.e., PWell and NWell) of the parasitic NPN and PNP bipolar transistors and consequently trigger the DCSCR without a snapback (see purple arrow in Figure 3.3). To the turn-on speed point of view, the DCSCR can be switched on quicker following two steps to trigger the internal SCR operation, one steps fewer than that of traditional SCR.

STEP 1: The two internally connected PWell/N+ and NWell/P+ diodes are turned on and start to inject carriers into well regions when voltage increases.

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STEP 2: SCR operation is triggered and dominate the major ESD current discharge.
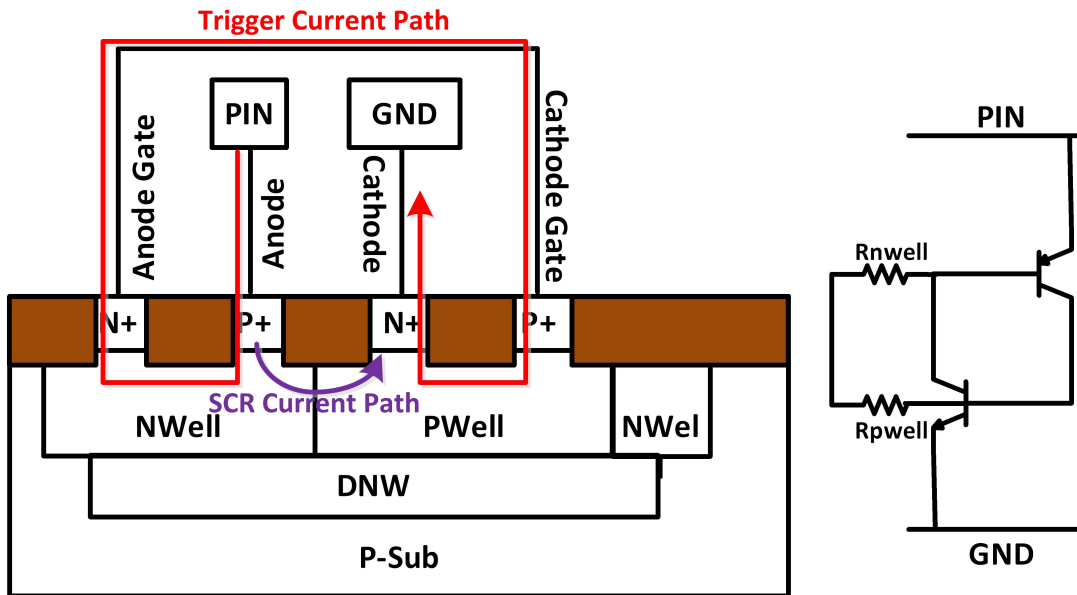
Figure 3.3: Cross-section view and equivalent circuit of traditional SCR.

In order to effectively raise the trigger and holding voltages needed for the low or medium ESD protection solutions, a number of DCSCRs can be stacked together. Figure 3.5shows the concept of implementing novel SCR cell in high voltage technologies. This approach is to stack several novel SCR cells to achieve a desirable high trigger and high holding voltages. The stacking number depends on the required trigger voltage, or the ESD design window. Since a single DCSCR cell does not possess a snapback behavior, the stacking of multiple cells also lacks snapback, thus providing an excellent ESD design window with adequate trigger and holding voltages for immunity of potential latch-up and core circuit damage. Figure 3.6 and Figure 3.7 shows the schematic and conceptual IV characteristics of the proposed stacking structure. It is turned on once the voltage applied to the structure's anode terminal exceeds the value of $2 \times N \times V$, where V is the diode's turn-on voltage and N is the DCSCR stacking number.
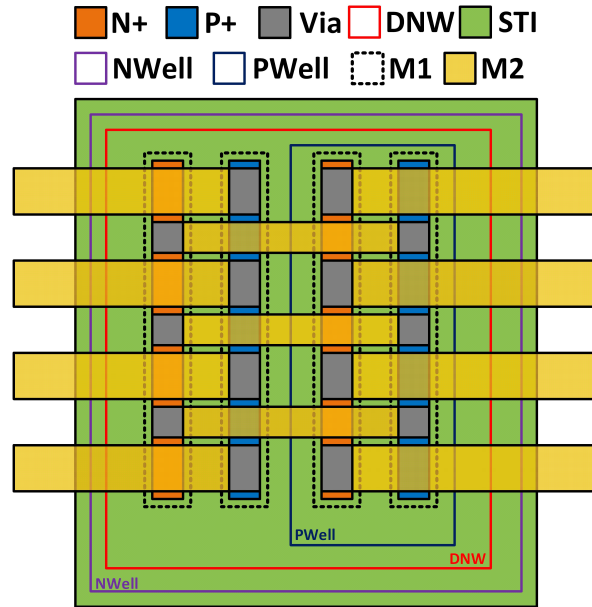
Figure 3.4: Top view of the layout of DCSCR.
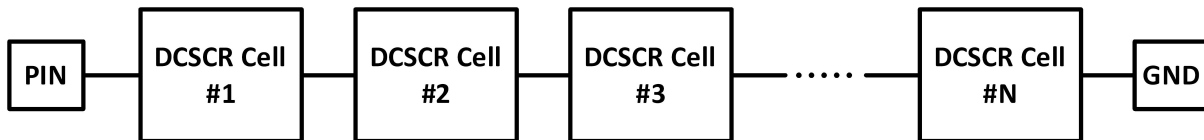
Figure 3.5: Concept of stacking DCSCR cells for low-to-medium voltage ESD applications.

Dummy gate technique has been proved to be an effective way to increase the turn-on speed of ESD protection devices, examples of this usage includes the applications on diode and SCR [26], [17] and [27]. Under the dummy gate region, the trench isolation (e.g., STI and DTI) and the field oxide (FOX) will be removed, making the current path shorter. Figure 3.8 shows the cross-section view of the DCSCR with dummy gate technique. Clearly, the trigger current denoted by the red line flow closer to the silicon surface.
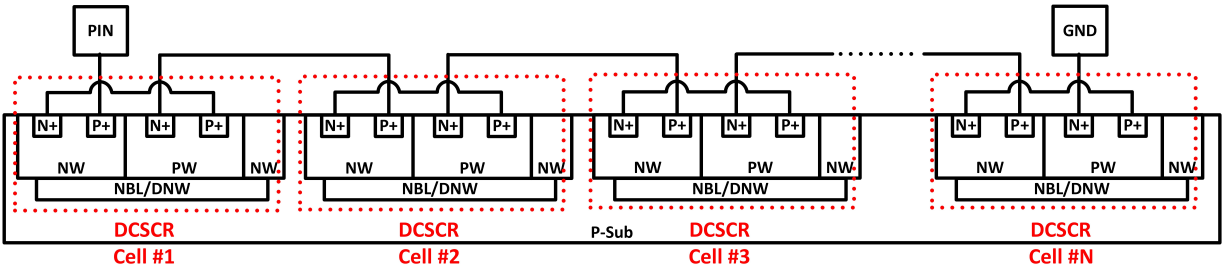
Figure 3.6: Cross-section view of stacking of multiple DCSCR cells for low-to-medium voltage ESD applications
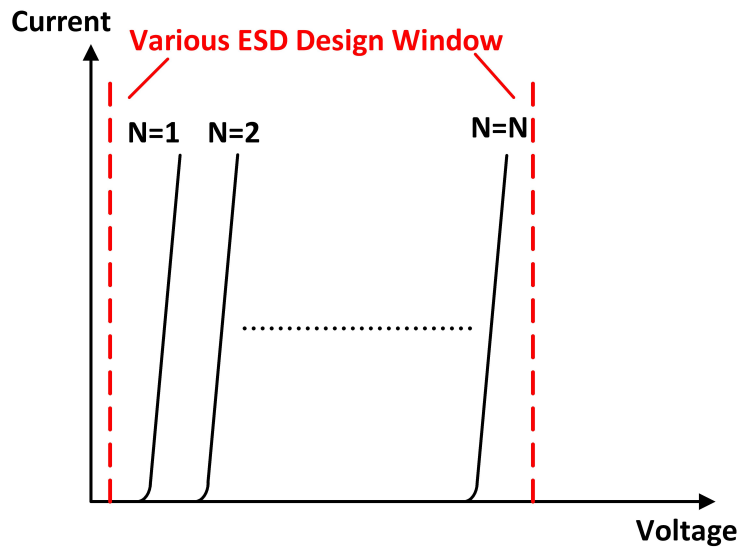
Figure 3.7: Conceptual IV curves of stacked structure having different numbers of DCSCRs.

3.3   TLP Measurement

DCSCR with STI, DCSCR with dummy gate, diode, traditional SCR and DTSCR were fabricated in a 0.18 μm CMOS technology and measured using the Barth 4002 transmission line pulsing (TLP) tester. Cathode-Anode-Cathode configuration was used for all the devices to improve the

current uniformity [19]. Figure 3.9 compares the measured TLP IV curves of a DCSCR, a DCSCR with dummy gate, a diode, a traditional SCR, and a DTSCR with a string of 3 diodes. The diode has 60 μm. while the other devices have the total width of 120 μm. As expected, the DCSCR demonstrates a minimal snapback window with the same trigger voltage Vt1 and holding voltage Vh of 1.3 V (see inset in Figure 3.9). For the dummy gate version, its trigger voltage is increased from 1.3 V to 1.75 V, because the emitter lengths of it is half of that of DCSCR with STI, resulting in a smaller carrier injections and thus a higher holding voltage [23]. After the triggering, the SCR element carries out the current conduction, and the DCSCR behaves similarly to the traditional SCR. Furthermore, while the DCSCR has a similar robustness as the other SCR-based structures, but a small degradation on robustness is seen on dummy gate version. These, together with the fact that Vt1 of DCSCR is twice of that of diode, indicates that the DCSCR is a better cell than the diode when building a stacking ESD structure for low voltage applications. For example, designing a power clamp for a circuit with a VDD = 3 V would require 5 diodes but take only 3 DCSCR's.
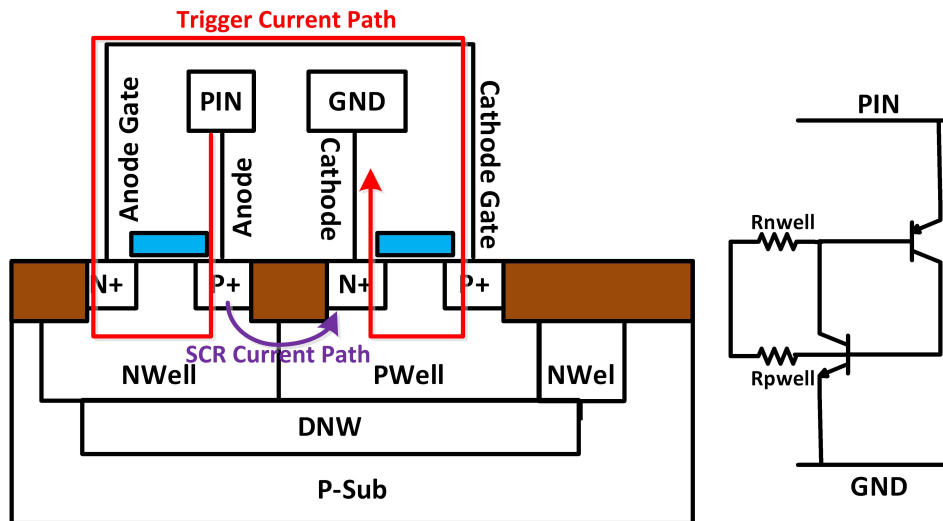
Figure 3.8: Cross-section view of DCSCR with dummy gate technique.

As such, the DCSCR-based clamp would occupy a smaller area and offer a higher robustness over its ESD-based counterpart.
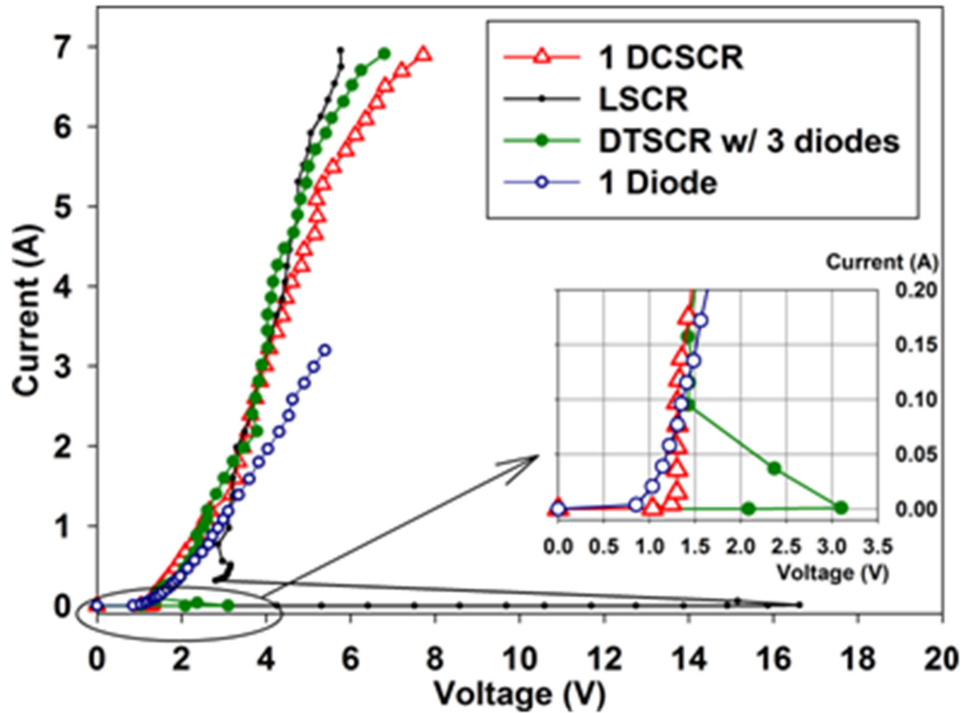
Figure 3.9: Comparison of TLP IV curves measured from the DCSCR with STI, DCSCR with dummy gate technique, traditional SCR, diode, and DTSCR.

Stacking technique is a common method to increase the voltage compatibility of ESD clamp in high voltage pins. Figure 3.10 shows the measured TLP IV curves of the proposed stacked DC-SCR clamps (with STI) having N=1, 2, 3 and 4. Clearly, with the absence of the snapback, the trigger and holding voltages can be flexibly and coordinately increased with increasing the stacking number. It should be noted that the on-resistance also increase when stacking up, but it can be reduced if large device width and/or more metal connection are used.
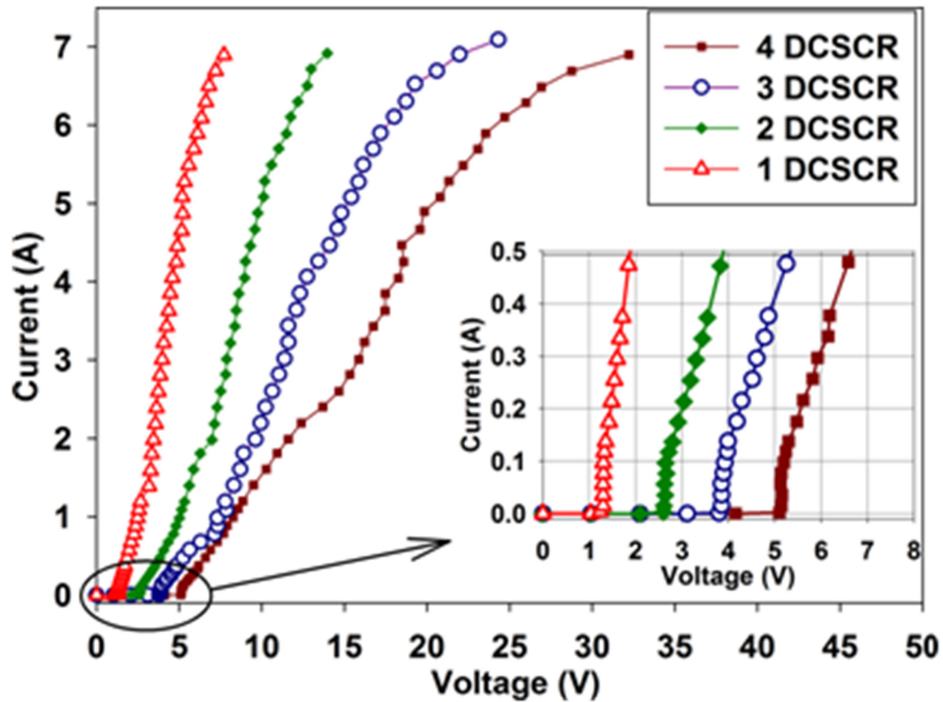
Figure 3.10: Measured TLP IV curves of proposed stacking structures having different stacking numbers.

3.4   vf-TLP Measurement

As the technology scaling down, advanced ICs becomes more and more fragile to sustain damages from ESD events with fast-rising pulse due to the overshoot voltage if the ESD clamps cannot turn on in time. DCSCR (with STI and dummy gate) is specifically designed for low votlage ESD applications, in return its turn on performance is an important ESD matrix. A Barth 4012 vf-TLP is used as the pulse source, which generates very-fast rising pulse having 100 ps rising time, and the pulse witdth is chosen to be 10 ns so as to simulate the worst ESD case. Figure 3.11 compares the voltage waveform versus transient time of diode, traditional SCR, DTSCR with three external diodes connecting to PNP base, DTSCR with three external diodes connecting to NPN base, DCSCR with STI and DCSCR wtih dummy gate. According to [24], the transient gate

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oxide breakdown voltage is 10 V, indicating that the overshoot voltage must be clamped under 10 V. Diode, LSCR and DTSCRs are verified not to be suitable for such kind of protection even though they have similar robustness as DCSCR. However, an interesting result is observed for DTSCRs, showing that it is slightly effective to connect the external diode string to NPN base compared to PNP base (14.7 V vs. 16.4 V), due to the fact that electrons, the major carriers in NPN, has higher mobility than that holes, the major carriers in PNP. Oppositely, the overshoot voltages of DCSCR with STI is compressed to 7.38 V, thanks to the direct connection between AG and CG. It is interesting to observe that the dummy gate technique further reduce the overshoot voltage ot 3.77 V, which is similar to the transient voltage at the steady state. Therefore, a no-snapback behavior also exists in the transient voltage waveform, indicating that DCSCR type of devices are high suitable for constructing protection solutions for a high-speed ESD event, such as CDM.

3.5   Thermal Stability of Leakage Current

It is very critical to evaluate the leakage current of DCSCRs at high temperature environment, because it is triggered on by two embedded diodes, whose leakage current increase exponentially when temperature goes up. Large leakage current is dangerous to ICs because it not only increases power consumption but also induce risk of false triggering and latch-up. Figure 3.12 compares the DC sweep of diode, DTSCR with three external diodes, DCSCR with STI and 2-stacked DCSCR with STI at 25 and 125 deg-C respectively. The results indicate that the DCSCR has an acceptable nA-level leakage current at 25 deg-C when it is biased below 1 V. A smaller leakage current is found for the DTSCR due to the presence of several external diodes added to the structure. The leakage current performance of DCSCR with dummy gate has similar result as the STI versions. The diode has the fastest increase in the leakage current when the voltage goes up, followed by the DCSCR and the 2-stacked DCSCR.
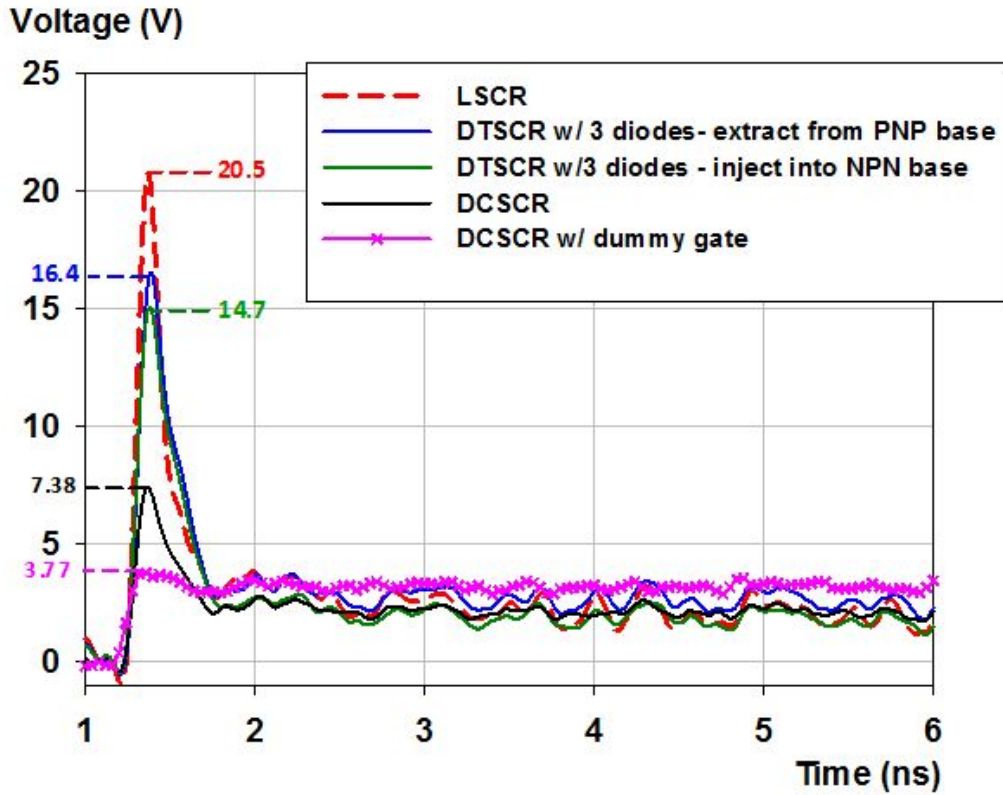
Figure 3.11: Measured transient waveforms of LSCR, DTSCRs, diode, the proposed DCSCR, and the DCSCR with dummy gate structures.

At an elevated temperature of 125 deg-C, the leakage currents of these devices are jumped to the μA level at relatively small voltages. As the voltage increases, the diode's leakage current again increases much more rapidly than the DCSCR devices. This illustrates that the DCSCR and its stacked structure are superior to the diode in term of the leakage current performance.
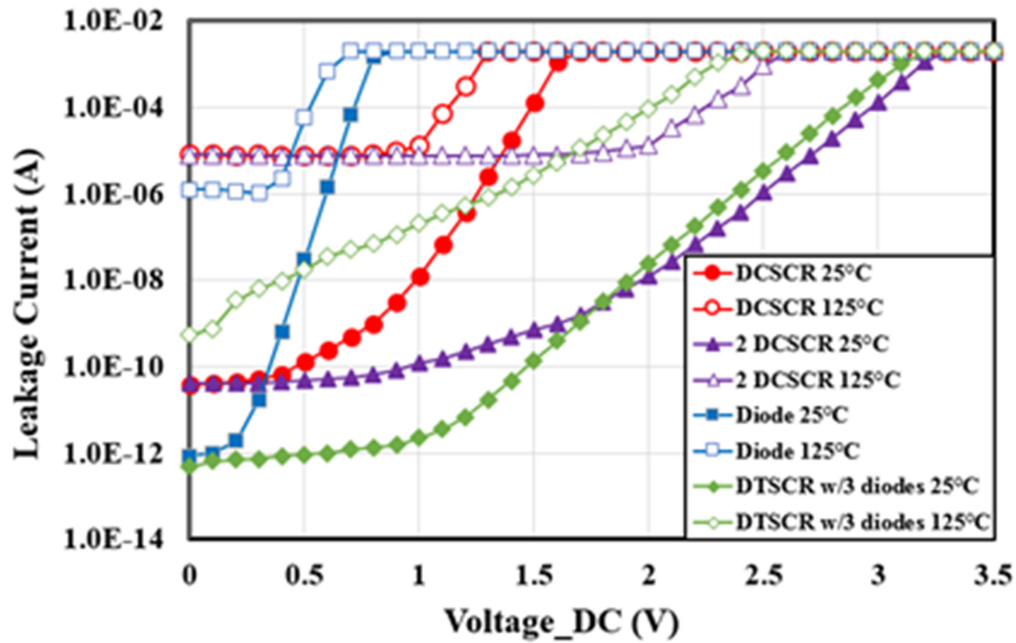
Figure 3.12: DC sweep of the DCSCR, 2-stacked DCSCR, diode and DTSCR with three external diodes at 25 deg-C and 125 deg-C.

3.6   ESD Performance Comparisons

Table 3.1 lists the trigger voltages, holding voltages, areas, failure currents It2, failure current densities Jt2, overshoot voltage and parasitic capacitances of the DCSCR with STI, DCSCR with dummy gate technique, diode, traditional SCR, and DTSCR. The DCSCRs and traditional SCR have the same robustness and area, but the DCSCRs with trigger voltages of 1.3 V and a near-zero snapback window is far more suitable for low and medium voltage ESD applications than the traditional SCR. Comparing to the diode, the DCSCRs demonstrate a much higher robustness and an improved voltage step-up capability. With regard to the DTSCR, the DCSCR is superior in terms of the snapback window and area. In addition, the DCSCR possesses the smallest capacitance among all devices considered, measured by AC signal with 1MHz frequency, thanks to the

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novel direct connection. However, the capacitance slightly increase when dummy gate technique is applied due to the gate parasitic capacitance.

Table 3.1: ESD Performance Comparisons of Diode, LSCR, DTSCR with three diode connecting to NPN base, DCSCR with STI, and DCSCR with dummy gate.

Device	Diode	LSCR	DTSCR (NPN)	DCSCR (STI)	DCSCR (dummy gate)
TLP It2 (A)	3.2	7	6.9	7	7
Area (um^2)	702	702	1188	702	702
TLP Jt2 (mA/um^2)	9.4	9.97	5.81	9.97	9.97
Capacitance (fF)	570	464	443	278	393
Vt1 (V)	0.7	16.6	3.1	1.3	1.75
Vh (V)	0.7	2.8	1.4	1.3	1.75
Overshoot (V)	7.38	20.5	14.7	7.38	3.77

3.7   Conclusion and Remark

A new SCR-based stacking structure realized in a 0.18 μm CMOS technology was developed. The structure utilized the DCSCR as the unit cell, which is an SCR with the anode gate and cathode gate connected to form two internal diodes, thus resulted in an internal trigger path with a trigger voltage of about 1.3 V and a near-zero snapback window. For small or medium voltage ESD applications, the ESD clamps built with stacking different numbers of DCSCRs were shown to successfully operate within the targeted design windows. It is demonstrated to be superior to the conventional diode and DTSCRs in term of turn-on speed/overshoot voltage, thermal stability of leakage current and parasitic capacitance.

CHAPTER 4: BIDIRECTIONAL ESD PROTECTION DESIGN FOR LOW-VOLTAGE CMOS TECHNOLOGY

In this chapter, an optimized pMOS-triggered bidirectional silicon-controlled rectifier (PTBSCR) fabricated in a 0.18-μm CMOS technology is proposed as a viable electrostatic discharge (ESD) protection solution. Capable of working under both the power-ON and power-OFF conditions, this structure is verified to provide bidirectional ESD protection performance superior to those reported in the literatures. Critical ESD parameters, such as the trigger voltage, holding voltage, and leakage current, can be flexibly adjusted via layout changes. With a low trigger voltage, a small ESD design window, a high robustness, and a small silicon area consumption, the PTBSCR is very suitable for low-voltage and low-power ESD protection applications.

4.1   Introduction

Constantly scaling of CMOS technology makes it harder for designing electrostatic discharge (ESD) protection solutions that must operate within a very small window, with the pin operating voltage and gate oxide transient breakdown voltage typically serving as the lower and upper bounds, respectively, of the window [24]. A bidirectional ESD device is needed for protecting a pin with an operating voltage varying between positive and negative values, and a bidirectional silicon-controlled rectifier (BSCR) capable of operating in the NS and PS modes of ESD stresses is suitable for such an application. However, the relatively high trigger voltage (i.e., 10 to 16 V) found in typical BSCRs limits severely their applicability in the low-voltage CMOS technologies [28], [29], [30]. To overcome this drawback, an ESD structure with dual MOS devices embedded in BSCR to realize a low trigger voltage was proposed [31]. Furthermore, a diode-triggered BSCR was recently developed aiming at reducing the trigger voltage [32], but in this design, trade-

off between the trigger voltage and leakage current must be considered. Another solution was to connect two opposing-polarity one-directional SCRs in parallel, but this was at the expense of larger area consumption [30]. Furthermore, floating gate was placed between anode and cathode in bidirectional SCR to block the formation of shallow trench isolation (STI). Enhanced avalanche effect was reached to reduce trigger voltage. However, only simulation results were provided to show that such a technique was capable of reducing the trigger voltage [33].

In this paper, we develop an optimized pMOS-triggered bidirectional SCR (PTBSCR) in a 0.18-μm CMOS technology. This structure aims at protecting I/O pins operating in the ± 1.8 V range. It can offer superior performance with a very small trigger voltage, a small snapback region, a small leakage current, a high ESD robustness, and good area efficiency.

4.2   Design and Operation of PTBSCR

Figure 4.1 shows the cross-sectional view and equivalent circuit of the proposed PTBSCR. It consists of a BSCR and an embedded pMOS device serving as the triggering element. Peripheral NWell and Deep NWell (DNW) are used to isolate the active region from the substrate. The polysilicon gate on top of the middle NWell region is connected to the power supply rail VDD which is 1.8 V in this technology. Also in the PTBSCR structure (see Figure 1), the two NWell/PWell junctions are fixed to the middle of the two P+ regions next to the gate, and D2 is the length of each P+ region. Therefore, increasing D2 will consequently move the left-hand- and right-hand-side NWell/PWell junctions away from the gate, respectively. Conversely, if D2 is reduced, the NWell/PWell junctions will move toward the gate.

The PTBSCR works differently under the power-ON and power-OFF conditions. In the case of power-ON and absence of ESD, the gate is pulled up to VDD, and the pMOS channel is depleted.

Therefore the leakage current is limited. When the terminal 1 (T1) of the PTBSCR is subject to a positive ESD stress and the terminal 2 (T2) is grounded, a voltage buildup at the drain of pMOS will cause the ESD-induced current to flow via the channel. Such a current flow will trigger the internal SCR. The same mechanism applies to the ESD stress zapping at T2 when T1 is grounded. However, under the power-OFF condition (i.e., VDD and the gate are floating), the pMOS can respond very quickly to the ESD stress and activate the internal SCR as the pMOS is initially on [34]. Such a triggering mechanism results in a very low trigger voltage of the proposed PTBSCR. After the PTBSCR is fully activated, the internal SCR dominates the ESD current conduction and offers a high robustness.
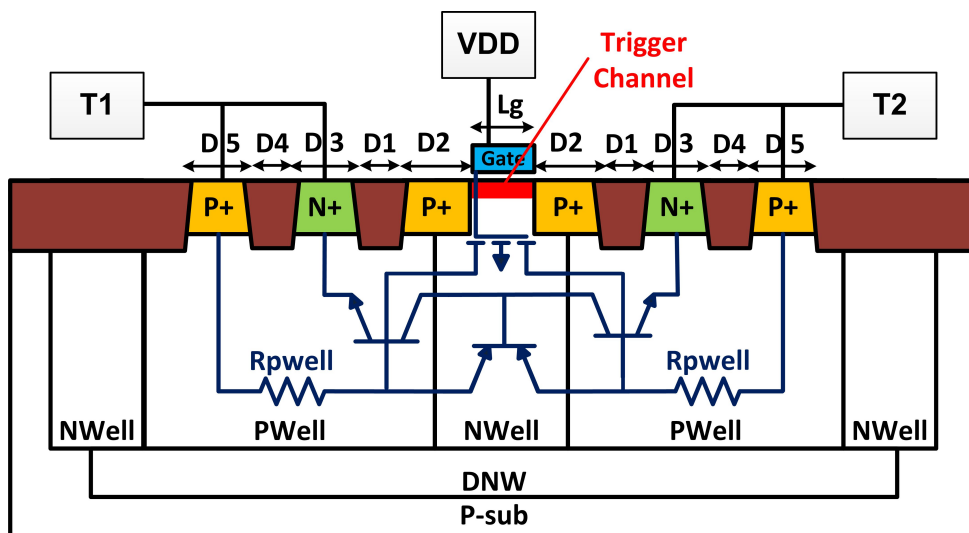
Figure 4.1: Cross-sectional view and equivalent circuit of the proposed PTBSCR. Red region: pMOS channel serving as the triggering path during ESD stress.

4.3 Result and Discussion

4.3.1 TLP Results and Turn-On Mechanism

A Barth 4002 transmission line pulsing (TLP) tester was used to generate HBM-like pulses with a 10 ns rising time and 100 ns pulse width. In the power-ON case, the TLP measurement was done with the power supply VDD connected to the gate of pMOS [7]. In the power-OFF case, the device was zapped with the gate floating. It is worth mentioning that the gate was biased to VDD when measuring the post-stress dc leakage currents in both cases.

Figure 4.2 shows the TLP I-V curves and leakage currents for the BSCR [28], IBSCR [29], and the proposed PTBSCR under the power-ON and power-OFF modes. Device parameters of PTBSCR are Lg=0.18 μm, D1=0.9 μm, and D2=1.3 μm. The BSCR and IBSCR have the same geometry size as the PTBSCR. As expected, the trigger voltage of PTBSCR in the power-ON case is larger than that in the power-OFF case (4.2 V versus 2.95 V), as the presence of the gate bias mandates a higher drain voltage to form the conducting channel in the pMOS. The insets in Figure 4.2 elaborate that the pMOS is initially on with a very small pre-snapback current in the power-OFF mode, and such a mechanism further reduces the trigger voltage [34]. The BSCR and IBSCR possess much higher trigger voltages, 15.9 and 11.4 V, respectively, because the triggering in these devices was governed by the p/n junction breakdown. These high trigger voltages limit their ESD protection applications for low-voltage I/O pins. Moreover, the PTBSCR offers a relatively small holding voltage of 2.4 V, creating a snapback region $\triangle$V of less than 0.5 V. The failure currents It2 of the three devices are comparable with each other.

To gain insights of PTBSCRs operations, we conducted 2-D, TLP-like numerical simulations with a 50 ohm external series resistor [35]. The parameters of PTBSCR in simulation were selected as Lg=0.18 μm, D1=0.9 μm, and D2=1.3 μm. T1 was stressed and T2 was grounded. The device

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simulator, Sentaurus by Synopsys, was calibrated by tuning the minority-carrier lifetimes, recombination rates, and avalanche ionization coefficients in the recombination, generation, and impact ionization models. The fidelity of the simulation results can be established by the comparison of the simulated and measured IV curves under the power-OFF condition shown in Figure 4.3.
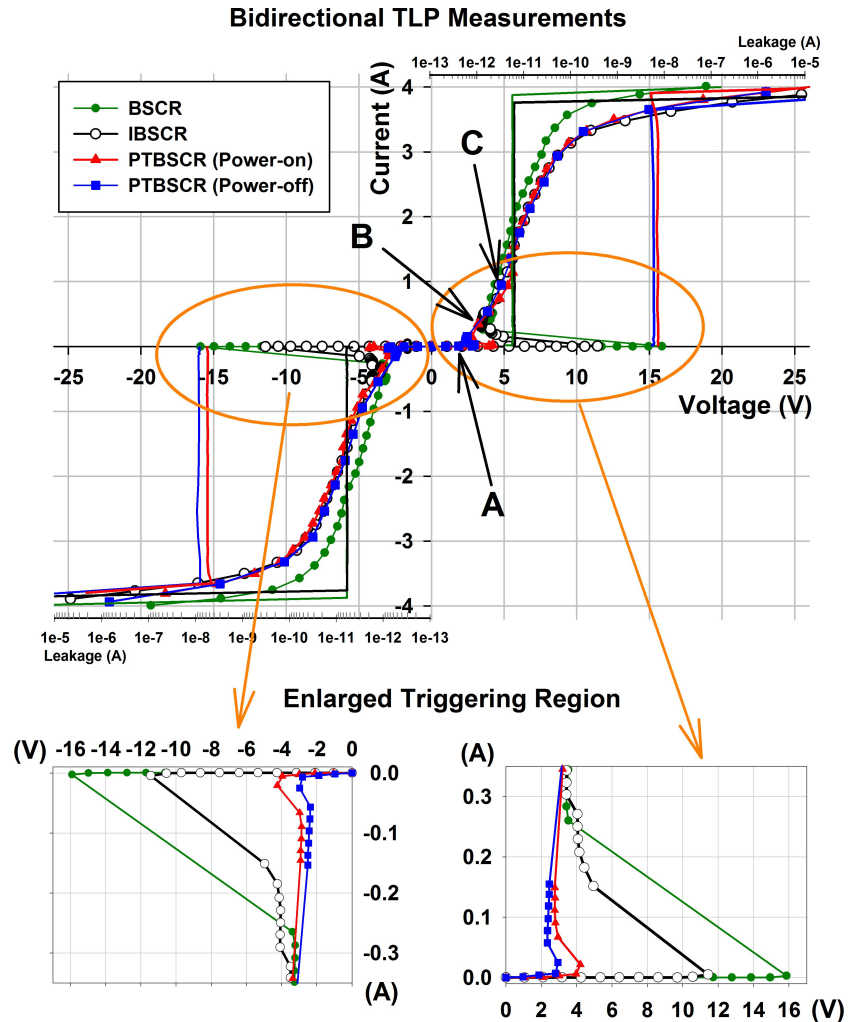
Figure 4.2: TLP I-V curves and leakage currents for the BSCR, IBSCR, and PTBSCR with gate floating (power-OFF) and gate biased at VDD=1.8 V (power-ON). Enlarged figures: detailed triggering behaviors for these devices. Lg=0.18 μm, D1 =0.9 μm, and D2=1.3 μm for the PTBSCR under measurement.
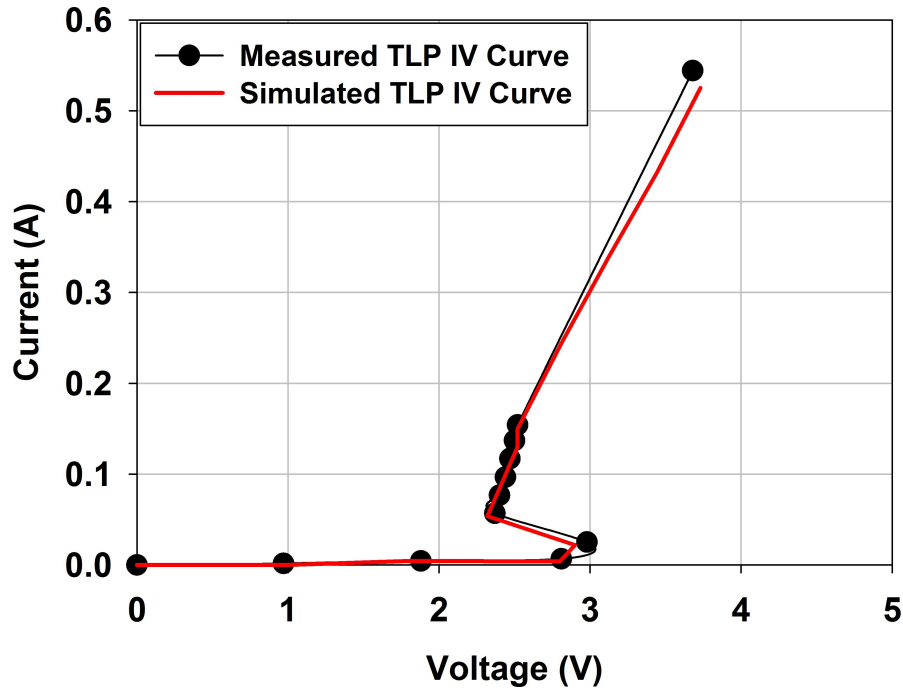
Figure 4.3: Simulated and measured I-V curves of PTBSCR under power-off condition. Lg=0.18 μm, D1=0.9 μm, and D2= 1.3 μm.

The turn-on behavior of the proposed PTBSCR can be illustrated with the simulated current distributions of the structure under the pre-snapback and post-snapback conditions shown in Figures 4.4, 4.5 and 4.6. The pulse voltages were selected as 2 and 20 V, which correspond to points A and B marked on the IV curve shown in Figure 4.2, respectively, for the pre- and post-snapback cases. With the gate floating, the simulation result in Figure 4.4 clearly demonstrates that, when the voltage between T1 and T2 is reduced less than the trigger voltage, only the embedded pMOS conducts a small amount of current. Once triggered, a large amount of current exists in the pMOS and SCR, as shown in Figure 4.5. When the gate is biased (i.e., power-ON), in pre-snapback condition the amount of current flowing in pMOS is smaller than that in power-OFF case, as shown in Figure 4.6, indicating that the gate biasing can reduce the leakage current.
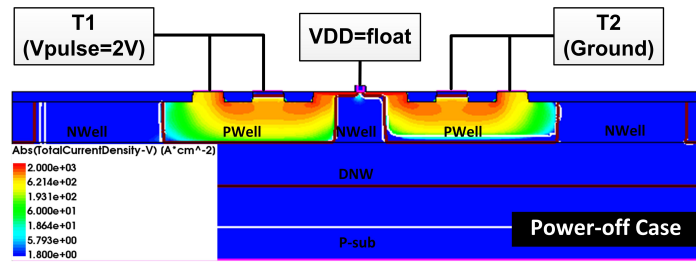
Figure 4.4: TCAD-simulated current distribution of PTBSCT at pre- and post-snapback points. Lg=0.18 μm, D1=0.9 μm, D2=1.3 μm. Vpulse = 2 V with floating gate,
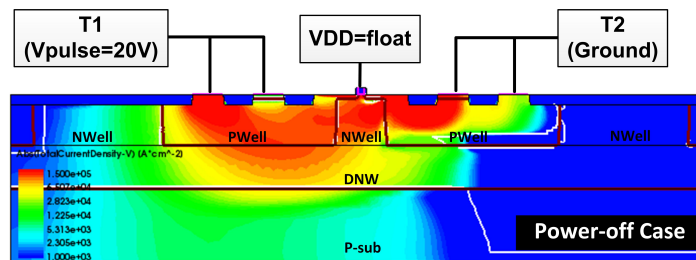
Figure 4.5: TCAD-simulated current distribution of PTBSCT at pre and post-snapback points. Lg=0.18 μm, D1=0.9 μm, D2=1.3 μm. Vpulse = 20 V with floating gate,

4.3.2   Layout Parameters

Three critical layout parameters, Formula, D1, and D2 were found to affect notably the PTBSCRs ESD performances. Figures 4.7, 4.8 and 4.9 show the effects of Formula, D1, and D2 on the trigger voltage Formula, holding voltage Formula, and failure current Formula, respectively. In these comparisons, one parameter is changed each time and the other two are kept constant. In Figure 4.7, Lg is varying while D1= 0.9 μm and D2 =1.3 μm are used. The same measurement principle applies to Figures 4.8 and 4.9. In the former case, D1 is the varying parameter with Lg=0.18 μm and D2=1.3 μm, while in the latter case D2 is varying parameter with Lg=0.18 μm and D1=0.9 μm.

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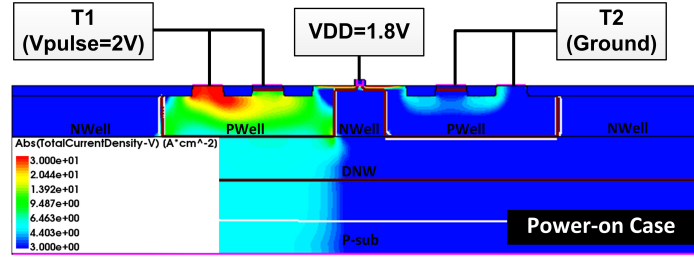
Figure 4.6: TCAD-simulated current distribution of PTBSCT at pre- and post-snapback points. Lg=0.18 μm, D1=0.9 μm, D2=1.3 μm. Vpulse = 2 V with gate biased at VDD=1.8 V

It can be derived from Figure 5 that Formula affects these ESD parameters in a parabolic manner, while from Figures 4.8 and 4.9, Vt1, Vh, and It2 exhibit fairly linear dependencies on D1 and D2. Table 4.1 summarizes the linear increments of ESD parameters versus D1 and D2, with Formula kept at 0.18 μm. The base value in Table 4.1 denotes the measurement results of the reference PTBSCR (Lg=0.18 μm, D1=0.9 μm, D2=1.3 μm). The signs + and - represent the positive and negative increments, respectively, of Vt1, Vh, and It2 with respect to D1 or D2 increase.

Table 4.1: ESD Parameters of PTBSCR with Respect to D1 and D2 Increase (Lg=0.18 μm).

		Base Value (Power-off/Power-on)	Increment (Power-off/Power-on)
D1	Vt1	2.95V/4.25V	+0.86/+0.57 (V/μm)
D1	Vh	2.35V/2.86V	+0.34/+0.27 (V/μm)
D1	It2	3720mA/3900mA	-6.9/-88.9 (mA/μm)
D2	Vt1	2.95V/4.25V	+0.03/+0.01 (V/μm)
D2	Vh	2.35V/2.86V	+0.12/+0.15 (V/μm)
D1	It2	3720mA/3900mA	-297/-282 (mA/μm)

From the results shown in Figure 4.7, it is clear that a larger Lg increases Vt1 in both the power-ON and power-OFF conditions. This is due to the trigger current originated from the pMOS is inversely proportional to Lg. As such, to maintain the same amount of trigger current, a higher voltage at the terminal is needed to build up a sufficiently large voltage drop in the base-emitter

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junction of the parasitic bipolar transistor for triggering the SCR. A conclusion can be made by comparing the effects of D1 and D2 on Formula (see Figures 4.8 and 4.9, and Table 4.1), where increasing D1 will be more effective in making Vt1 larger than increasing D2, as D1 governs the resistance of the triggering path.

Holding voltage is another important ESD matrix. Its value should be larger than 110% of the pin's operation voltage to effectively suppress latchup threat. Influences on holding voltage from changing Lg, D1, and D2 are shown in Figures 4.7, 4.8, 4.9, and Table 4.1. Clearly, increasing Lg can increase the holding voltage owing to the reduced current gain β of the parasitic bipolar transistors embedded in SCR. D1 plays a similar role on the holding voltage, but a weaker D2 on Vh effect is found.
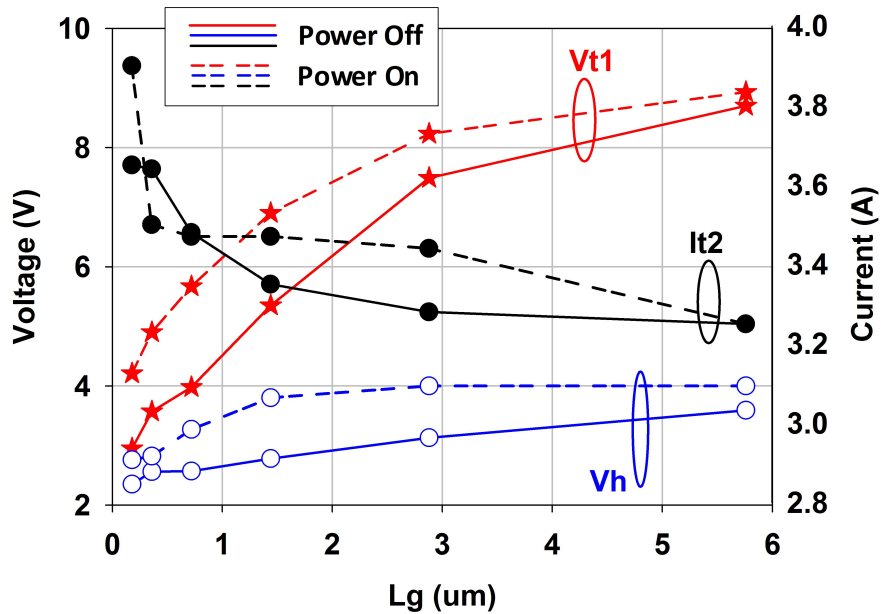
Figure 4.7: Trigger voltage, holding voltage, and failure current of PTBSCR versus the gate length Lg in both power-OFF and power-ON conditions. D1=0.9 μm, and D2=1.3 μm.
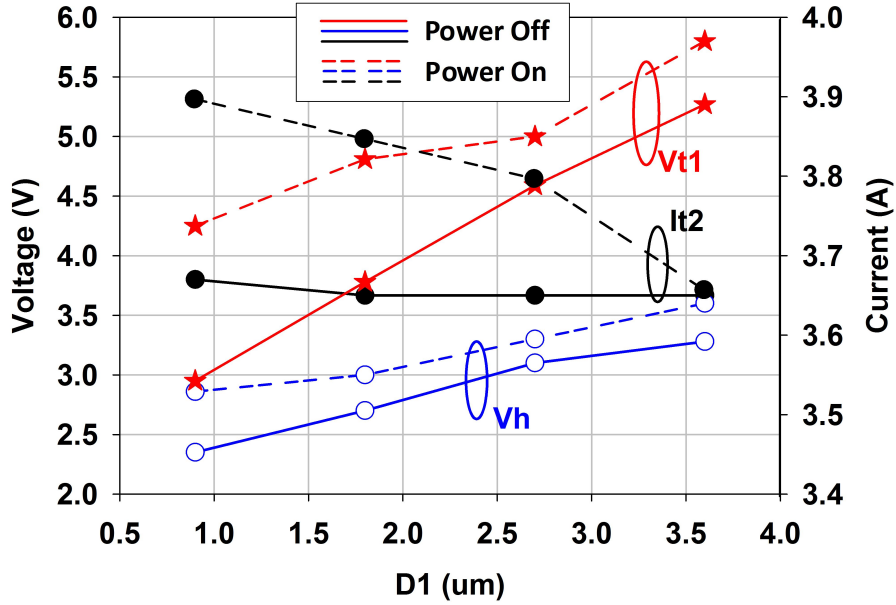
Figure 4.8: Trigger voltage, holding voltage, and failure current of PTBSCR versus D1 in both power-OFF and power-ON conditions. Lg=0.18 μm, and D2=1.3 μm.

The reason for this effect is because after the snapback, a portion of the region described by D2 is depleted of the injected free carriers, and thus changing D2 has very little influence on the current gain β and thus Vh. This mechanism can be verified from the TCAD-simulated recombination rate contours. In Figure 4.10, the device parameters used in the simulation were Lg=0.18 μm, D1=0.9 μm, and D2=1.3 μm. In Figures 4.11, 4.12 and 4.13, Lg, D1, and D2 were increased to 0.72, 1.8, and 2.6 μm, respectively. Stressed ESD pulse has a pulse amplitude Vpulse=50 V for all cases, which corresponds to point C marked on the IV curve in Figure 4.2. In Figure 4.10, a much smaller recombination rate in the partial D2 region than those in the Lg and D1 regions (Regions 1 and 2) is observed. Moreover, more minority carriers recombine in the Lg and D1 regions when increasing the dimensions of these two regions [see Figures 4.11 and 4.12], where the high recombination rates are shown. It clearly confirms the stronger dominance of Lg and D1 on Vh. However, when the D2 is increased, the effective recombination region stays almost unchanged [see Figure 4.13].
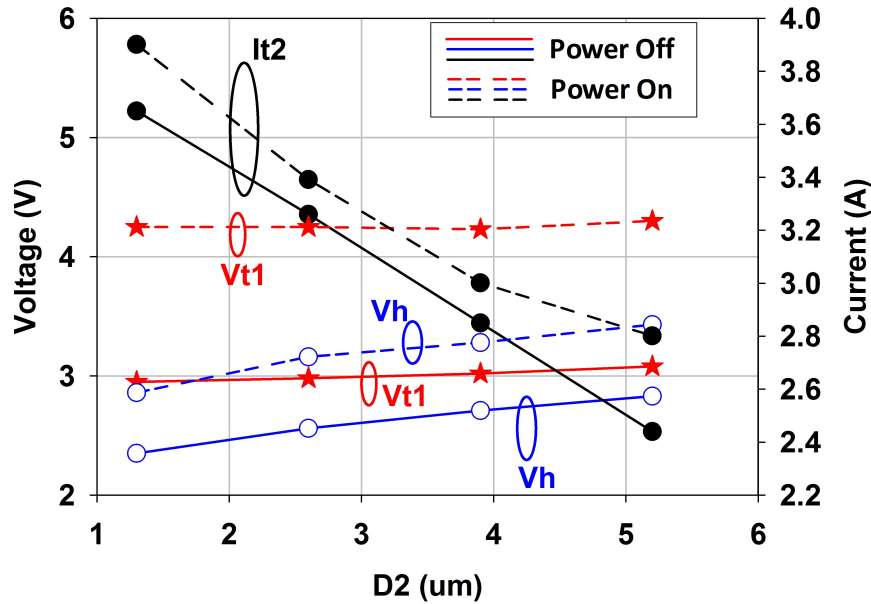
Figure 4.9: Trigger voltage, holding voltage, and failure current of PTBSCR versus D2 in both power-OFF and power-ON conditions. Lg=0.18 μm and D1=0.9 μm.

Such a smaller recombination contributes to the weak influence of D2 on Vh.

We next investigate the effects of layout parameters on the ESD robustness (see Figures 4.7, 4.8, 4.9 and Table 4.1). On one hand, the embedded BJT's current gains are reduced when increasing Lg or D1, because Lg and D1 govern the embedded PNP and NPN BJT's base widths, respectively. As such, a higher voltage drop builds up in the device when these dimensions increase. The larger voltage drop generates a larger amount of power dissipation and consequently the PTBSCR's robustness is degraded. On the other hand, since the region describes by D2 has a low recombination rate, increasing D2 will cause a larger voltage drop, and the effect of D2 on It2 is more significant than those of Lg and D1. Figures 4.14 and 4.15 show the voltage contours in the P+ region with D2=1.3 μm and 3.9 μm, respectively, under the same stress condition (Vpulse=100 V) from TCAD simulation. Larger voltage drops in the NWell/PWell regions are seen for the case of D2=3.9 μm.

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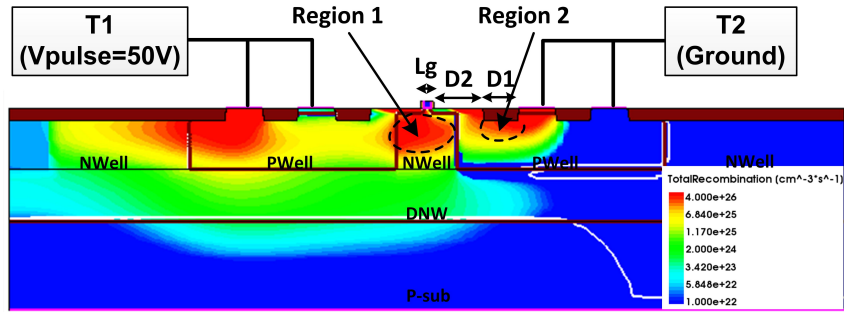
Figure 4.10: TCAD-simulated recombination rate contours in PTBSCR subject to a stress of Vpulse=50 V for Lg=0.18 μm, D1=0.9 μm and D2=1.3 μm.

Based on the preceding analysis, one can effectively increase the trigger and holding voltages by increasing Lg and D1 simultaneously or by stacking several PTBSCR devices. D2 is recommended to be kept small considering its greater degradation on It2.

D3 and D4 can also affect the ESD design to some extent. Increasing D3 gives rise to a slightly lower holding voltage due to an increase in the emitter efficiency of parasitic bipolar transistors, while changing D4 mainly impacts the PWell resistance. Generally speaking, these two dimensions should be kept reasonably small to minimize the layout area.
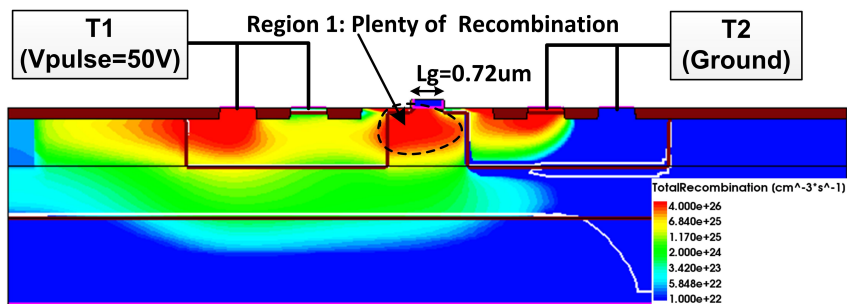
Figure 4.11: TCAD-simulated recombination rate contours in PTBSCR subject to a stress of Vpulse=50 V for Lg=0.72 μm, D1=0.9 μm and D2=1.3 μm.
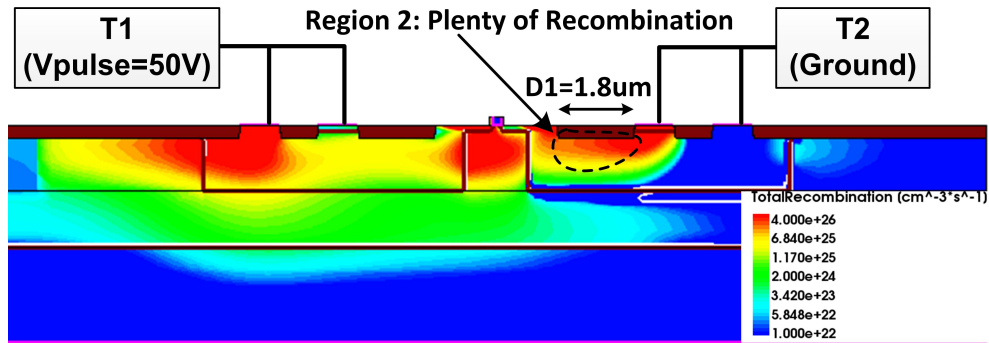
Figure 4.12: TCAD-simulated recombination rate contours in PTBSCR subject to a stress of Vpulse=50 V for Lg=0.18 μm, D1=1.8 μm and D2=1.3 μm.
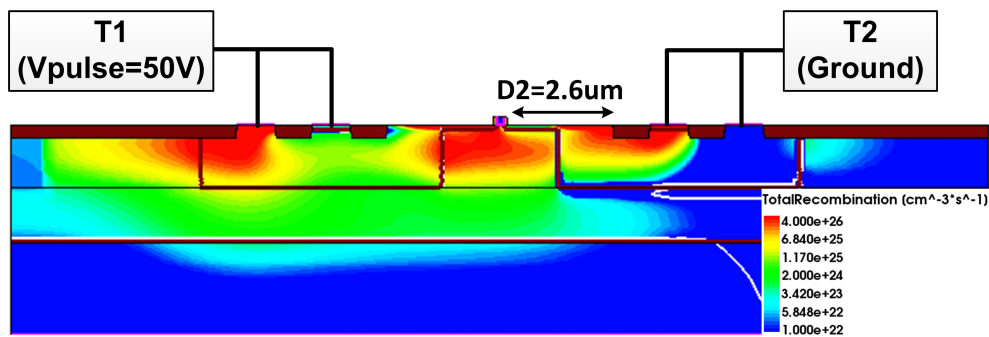
Figure 4.13: TCAD-simulated recombination rate contours in PTBSCR subject to a stress of Vpulse=50 V for Lg=0.18 μm, D1=0.9 μm and D2=2.6 μm.

4.3.3   Leakage Current

Leakage current plays an important role in affecting the static power consumption of the PTBSCR in normal circuit operation. Figures 4.16, 4.17 and 4.18 show the leakage current versus some key device parameters, including Lg, D1 and D2, under the power-on condition. Increasing Lg reduces the leakage current considerably, because the PMOS is less leaky if the channel length becomes larger. However, increasing D1 and D2 reduce the leakage current only slightly.
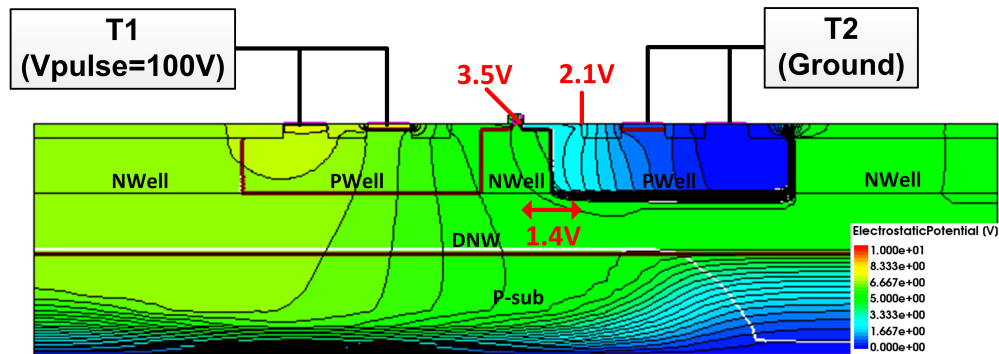
Figure 4.14: TCAD-simulated voltage contours in the PTBSCR under the same stress condition with D2=1.3 μm. Lg=0.18 μm, D1=0.9 μm, and Vpulse=100 V for both cases.
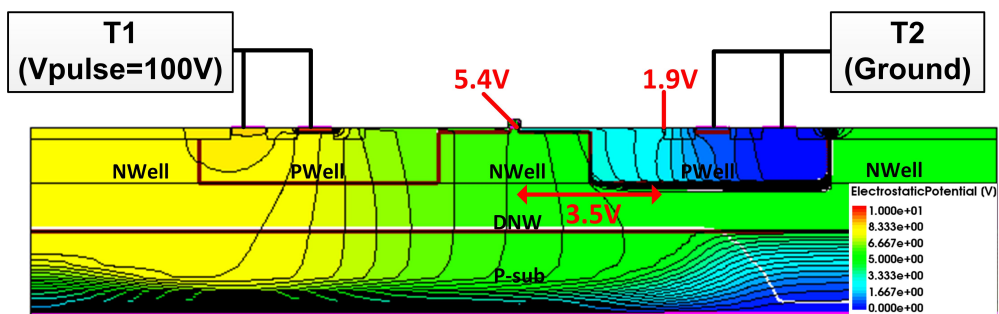
Figure 4.15: TCAD-simulated voltage contours in the PTBSCR under the same stress condition with D2=3.9 μm. Lg=0.18 μm, D1=0.9 μm, and Vpulse=100 V for both cases.

Furthermore, the gate bias voltage VDD can greatly affect the leakage current under the power-on condition. Figure 4.19 shows the leakage current versus gate bias voltage characteristics. Clearly, a larger gate bias voltage effectively suppresses the leakage current from 0.1 mA level to 10 pA level when it is less than 2.4 V, because the embedded PMOS becomes more "cut-off" with such a bias condition. When the gate bias voltage is larger than 2.4 V, the leakage current increases because of the increased electric field on the thin gate oxide. Also given in Figure 4.19 is the trend of Vt1 vs. gate bias voltage. The trigger voltage is increased linearly with increasing gate bias

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voltage. This is due to the fact that it is more difficult to turn on the PTBSCR when the PMOS is more "cut-off". However, no significant influence is found from gate bias voltage to Vh.

To examine the gate-VDD coupling effect on the PTBSCR operation, TCAD simulation with capacitances ranging from μmF to fF coupled between the gate and ground in the power-off condition was conducted. The effect of VDD-coupled capacitance was negligible, as the results yielded a very small post-snapback gate current of around 100 pA. We have also tested the PTBSCR with the protected pin coupled to VDD, and the ESD clamp was found working normally under this condition.
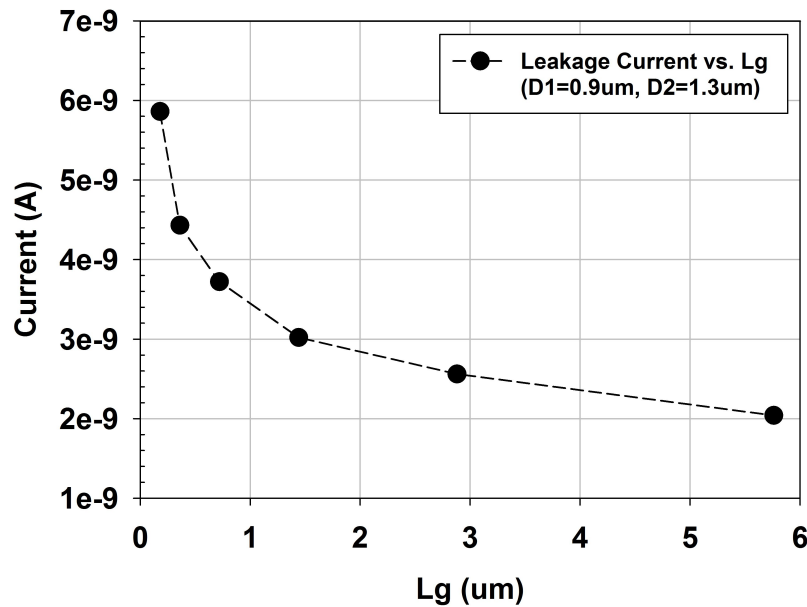
Figure 4.16: Leakage current versus Lg under the power-on condition..

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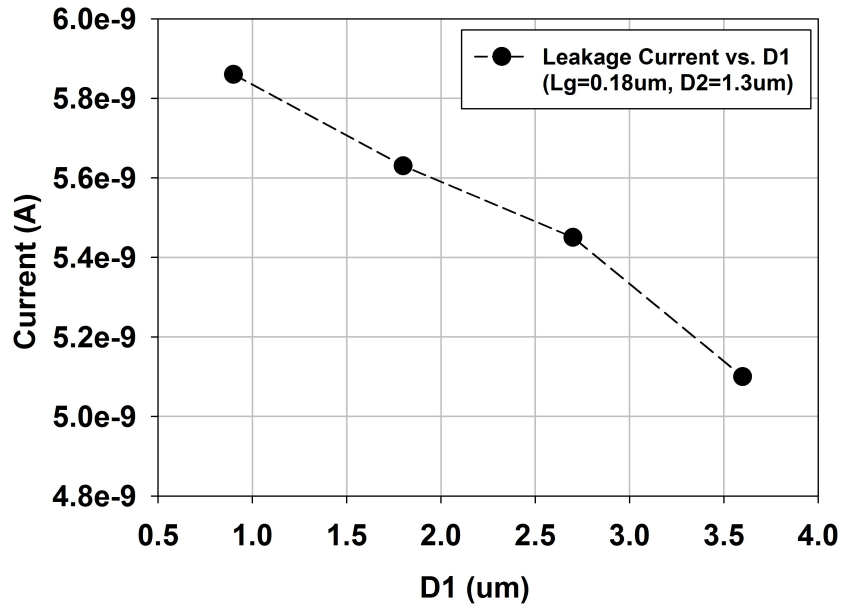
Figure 4.17: Leakage current versus D1 under the power-on condition.

4.3.4 vf-TLP Results

In order to evaluate the CDM performance, a Barth 4012 vf-TLP tester was used to apply fast-rising pulses (rising time Tr=200 ps, pulse duration Td=10 ns) on the BSCR, IBSCR and the proposed PTBSCR. The measured data listed in Table 4.2 indicate a 13% degradation on the vf-TLP robustness due to the presence of the embedded PMOS. On the other hand, the embedded PMOS can reduce the PTBSCR's overshoot voltage, as illustrated in Figure 4.20 which shows the transient voltage waveforms of these three devices stressed using a vf-TLP pulse with a magnitude of 16 V. This voltage level is sufficiently large to ensure all devices under test were operating in the post-snapback region. Clearly, the PTBSCR possesses the smallest overshoot voltage among the three devices. As shown in Figure 4.4, the trigger current needs to flow from P+ in T1 to another P+ in T2, and such a distance is key to the overshoot voltage. Therefore, D1, D2, D3, D4, and Lg

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should be reduced to their minimum values so as to further pull down the overshoot voltage. One can also apply the dummy-gate technique, which blocks the formation of the STI between pick-up implantations, to further reduce the overshoot voltage [36].

4.3.5 Comparisons

Table 4.2 summarizes the ESD performances of the optimized PTBSCR and existing bidirectional SCRs. The PTBSCR, under the TLP stressing, is proved to be superior to the other structures in terms of the small trigger voltage, small holding voltage, small leakage current, small layout area, and enhanced robustness. The trigger voltage and holding voltage can be flexibly and easily tuned by changing Lg, D1, and D2 to meet the different ESD design requirements.
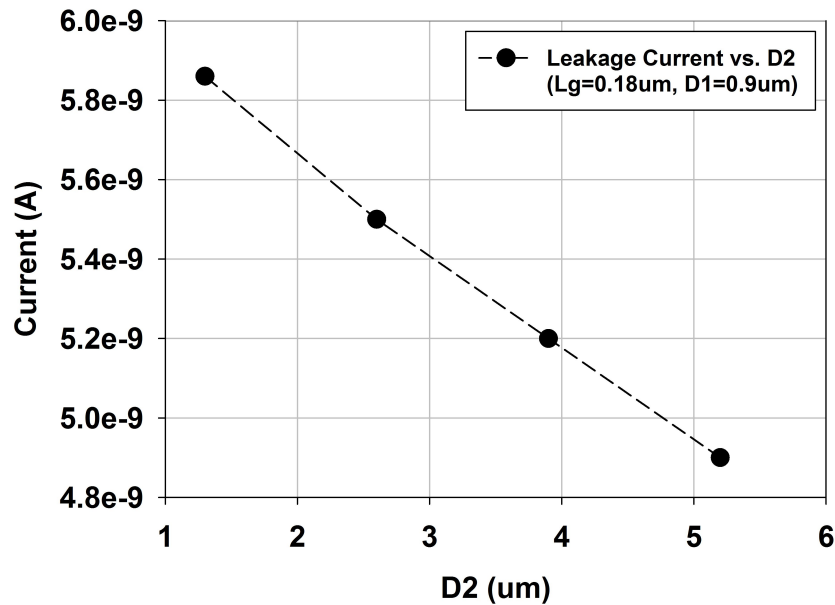
Figure 4.18: Leakage current versus D2 under the power-on condition.
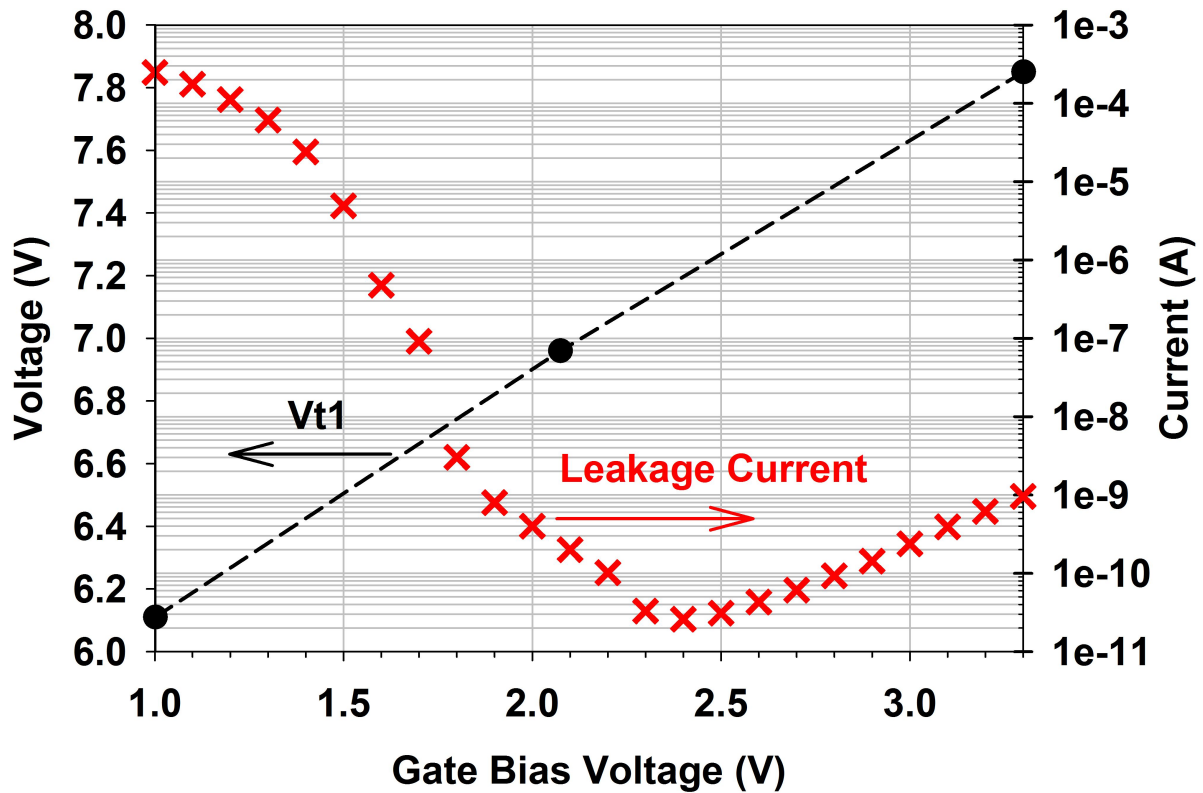
Figure 4.19: Measured leakage current and trigger voltage versus gate bias voltage (or VDD). Lg=1.44 μm, D1=0.9 μm, D2=1.3 μm. T1=1.8 V, T2=0 V for leakage current measurement.

A figure-of-merit (FOM) defined as It2/(Area $\times$ Vt1) is used to better evaluate the ESD performances of different devices. As shown in Table 4.2, the PTBSCR has the smallest area consumption and the highest FOM among all of the devices considered.

4.4   Conclusion and Remark

An optimized PMOS-triggered bidirectional SCR realized in a 0.18 μm CMOS technology was developed, and its ESD characteristics were verified using the TLP, vf-TLP, and TCAD simulator.
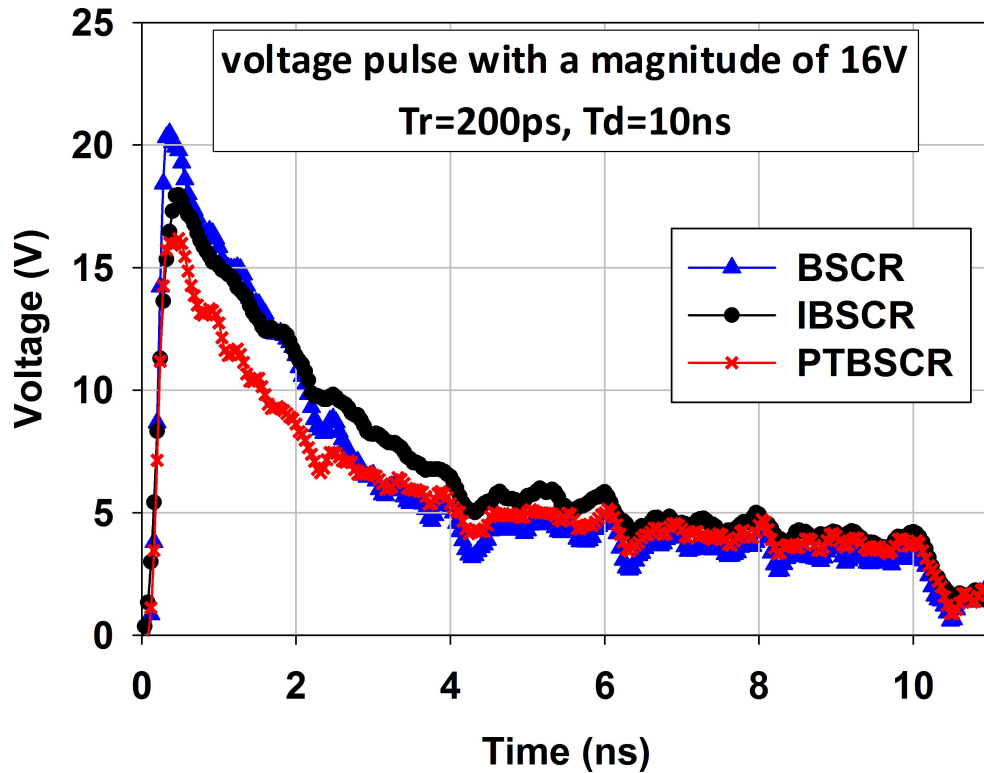
Figure 4.20: vf-TLP transient voltage waveforms of BSCR, IBSCR and PTBSCR. Lg=0.18 μm, D1=0.9 μm, D2=1.3 μm.

Due mainly to an embedded PMOS structure, the proposed PTBSCR under the TLP stress offered improved low-voltage ESD protection capability, including small trigger and holding voltages with a very narrow snapback region to satisfy a small ESD design window, a high ESD robustness, and a low leakage current without the expense of occupying a large layout area. Slight improvement was also seen in the overshoot voltage and turn-on speed compared to traditional dual-directional SCR, which will be beneficial to protect CDM-like events. The turn-on performance of the proposed PTBSCR in CDM-like events could be further improved by using the minimized layout parameters, and using the dummy gate technique, which can effectively shorten the trigger current path.

Table 4.2: ESD Performance of PTBSCR and Existing Bidirectional SCRs.

Device	BSCR [28]	IBSCR [29]	Ref [31]	Ref [32][1]	This work
Technology	0.18 μm	0.18 μm	0.18 μm	90 nm	0.18 μm
TLP Ronustness (mA/μm)	64.7	62.8	56.3	58.3	65
vf-TLP Ronustness (mA/μm)	75.2	75	45.6	N/A	65
Vt1 (V)	15.9	11.4	3.8-6.2	3.4-5.5	2.95-8.93
Vh (V)	3.48	4.06	2.99	3.2-5.3	2.4-4.9
Leakage Current (A)	1e-12	1e-12	1e-8	1e-9	1e-11[2]
Area (μm^2)	651	651	1085	1061	651
FOM (mA/μm^2V)	0.394	0.532	1.23	1.05	2.03

[1] Requires more than four external diodes for small leakage current.
[2] Leakage current was measured in power-on condition.

This area-efficient, latch-up immune ESD device is useful in constructing bidirectional ESD protection solutions for low-voltage/low-power CMOS ICs.

CHAPTER 5: NO-SNAPBACK ESD PROTECTION DESIGN FOR HIGH-VOLTAGE BCD TECHNOLOGY

In this letter, we develop a no-snapback silicon-controlled rectifier (NS-SCR) in a 0.35 μm BCD technology. This device is constructed by embedding in a typical SCR a P-type/intrinsic/N-type (PIN) diode as the trigger element and two highly-doped extension regions as parts of the bases of the parasitic bipolar transistors (PBTs). These added features allow for a high electric field to be maintained at the reverse biased n/p junction in the ESD current path, prevent the onset of strong conductivity modulation, and result in a no-snapback TLP I-V characteristic. Stacking the NS-SCR's offers an ESD protection solution that is area-efficient, robust, and latch-up immune. The high temperature effect on the leakage current of NS-SCR is also studied.

5.1 Introduction

Automotive and power electronics operating in the range of tens of volts require ESD protection clamps with a relatively high trigger voltage. Due to its adjustable high trigger voltage and relatively high robustness, the silicon-controlled rectifier (SCR) would be an attractive protection device [12]. At the same time, a high holding voltage is also desired in order to mitigate the latch-up risk in the noisy operating environment of automotive applications. These call for a SCR, which can ideally exhibit a zero snapback yet maintain a satisfactory robustness. Stretching the base regions of the parasitic bipolar transistors (PBTs) in SCR is a simple method used to increase the SCR's holding voltage, but it cannot effectively eliminate the snapback [37]. Segmentation technique was also suggested to reduce the emitter areas of the PBTs and hence increase the holding voltage, but such an approach is not applicable in some technologies [23]. Stacking several SCR's was proposed in [38], but this still gives rise to a notable snapback, particularly when the number

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of stacking is relatively large. An SCR was incorporated in the BJT, forming a reverse-biased diode to increase the holding voltage. However, a sizable snapback still occurs due to the inherently high trigger voltage of the BJT [39]. More recently, a ring-resistance-triggered technique was proposed to keep the trigger voltage unchanged while stacking LDMOS-SCR's, but its low holding voltage requires a large stacking number to meet the high voltage ESD requirements [40].

In this letter, a no-snapback SCR, called the NS-SCR, is realized in a 0.35 μm BCD technology. The key novelty of this device is an embedding of a parasitic P-type/intrinsic/N-type (PIN) diode, a feature that enables effective adjustment of both the trigger and the holding voltages. The ESD performances and the thermal stability of the leakage current are studied experimentally using the Barth 4002 transmission line pulsing (TLP) tester.
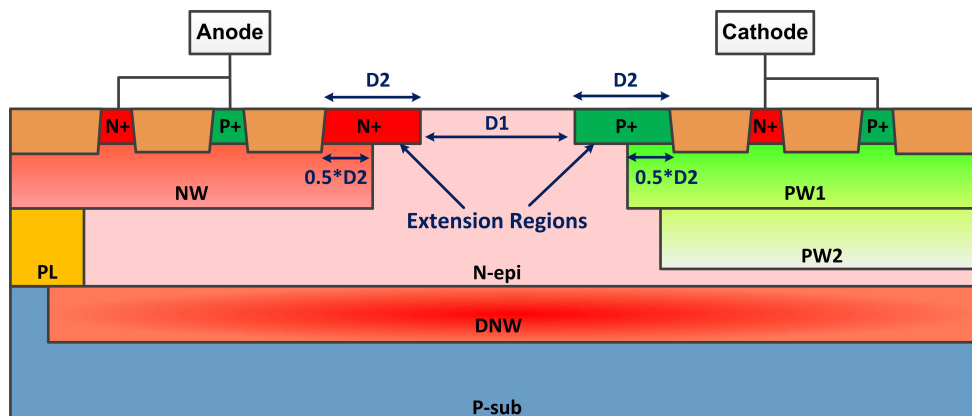
Figure 5.1: Cross-section view of the left-hand half of 2-finger NS-SCR.

5.2   NS-SCR Structure and Operation

The traditional SCR contains a PNPN structure, in which the n/p junction (i.e., blocking junction) located in the middle of the SCR is reverse biased. After triggering, the breakdown of this junc-

tion gives way to a large free-carrier injection from the parasitic bipolar transistors (PBTs), thus resulting in a high-level conductivity modulation and a low holding voltage. If the high electric field in the vicinity of the reverse biased junction that initiates the triggering could somehow be maintained, then such an electric field could minimize the conductivity modulation, thus resulting in a high holding voltage and mitigate the snapback.
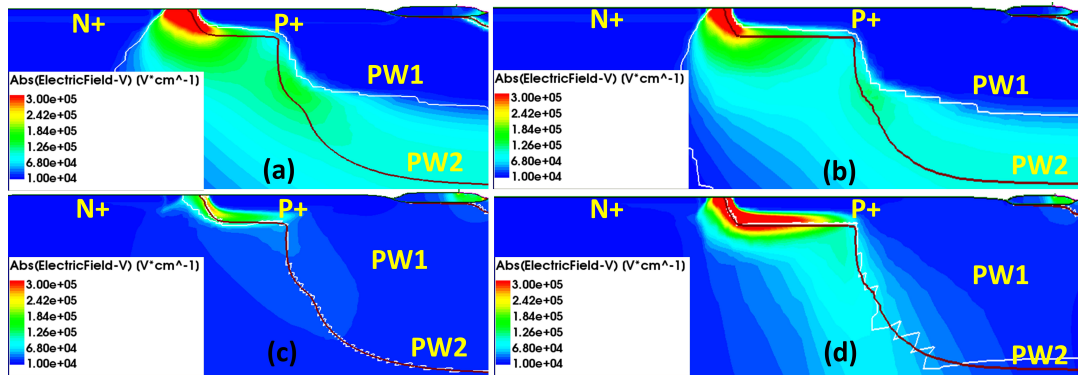
Figure 5.2: TCAD-simulated pre-trigger ((a) and (b)) and post-trigger ((c) and (d)) electric field contours for the NS-SCR. D2 = 2 μm in (a) and (c), and D2 = 4 μm in (b) and (d). TLP-like pulse voltages of 15 and 250 V were employed for the pre- and post-trigger cases, respectively.

The NS-SCR is designed using the above-mentioned concept. As illustrated in Figure 5.1, which represents the left-hand half of device's symmetrical structure, the N+ and P+ extension regions are the main added features of the NS-SCR. In the structure, PL is the high voltage N-type plug diffusion region, which reaches down to the N-type buried layer (DNW), and PW2 is the deep P-type well. The traditional N-type and P-type well regions (NW and PW1 in Figure 5.1, respectively), as well as the highly doped N+ and P+ extension regions, are separated by the N-type epitaxial region (N-epi). These extension regions, together with the N-epi region, form the PIN diode. The spacing between the N+ and P+ extension regions, denoted as D1, strongly affects the trigger voltage of NS-SCR. During the ESD stress, the N-epi/P+/PW1/PW2 junctions are reverse biased and sustain most of the stress voltage. Thanks to the P+ extension region, the peak electric

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field is primarily concentrating at the P+/N-epi junction. As such, the N-epi/PW1 and N-epi/PW2 junctions, through which most of the ESD current flows, will not be converted into the state of high-level conductivity modulation because the electric fields in these junctions are relatively low. The length of D2, which denotes part of the PBT's base width, strongly affects the blocking junction electric field. The electric field contours of the NS-SCR for the cases of D2 = 2 and 4 μm under the pre- and post-trigger conditions are shown in Figure 5.2. The results were simulated using the Sentaurus device simulator. TLP-like pulses with 15 and 250 V were employed to simulate the pre- and post-trigger conditions, respectively. Clearly, the two devices (2 and 4 μm) have very similar electric field contours before triggering. But the post-trigger electric field in the vicinity of n/p blocking junction is significantly increased when D2 is increased from 2 to 4 μm. Thus, the proposed structure, in combination with a relatively large D2, can yield a high holding voltage and at the same time retain a high robustness. It should be noted that in the regions designated by D1 and D2, a silicide block mask must be used to ensure that the ESD current does not flow via the silicide.

5.3 Measurement and Discussion

Table 5.1: Layout Parameters for Cell A and Cell B.

	D1 (μm)	D2 (μm)		D1 (μm)	D2 (μm)
Cell A	0.4	4	Cell B	0.6	4

Next we investigate the ESD performance of the proposed NS-SCR. Figure 5.3 shows the measured TLP I-V curves, and the insert shows the extracted trigger voltages vs. D1, indicating a fairly linear relationship. A very weak influence of D1 on the holding voltage is observed. This is because D1 defines the width of lower doped epitaxial region, which can be easily and completely depleted when subjected to an ESD stress.
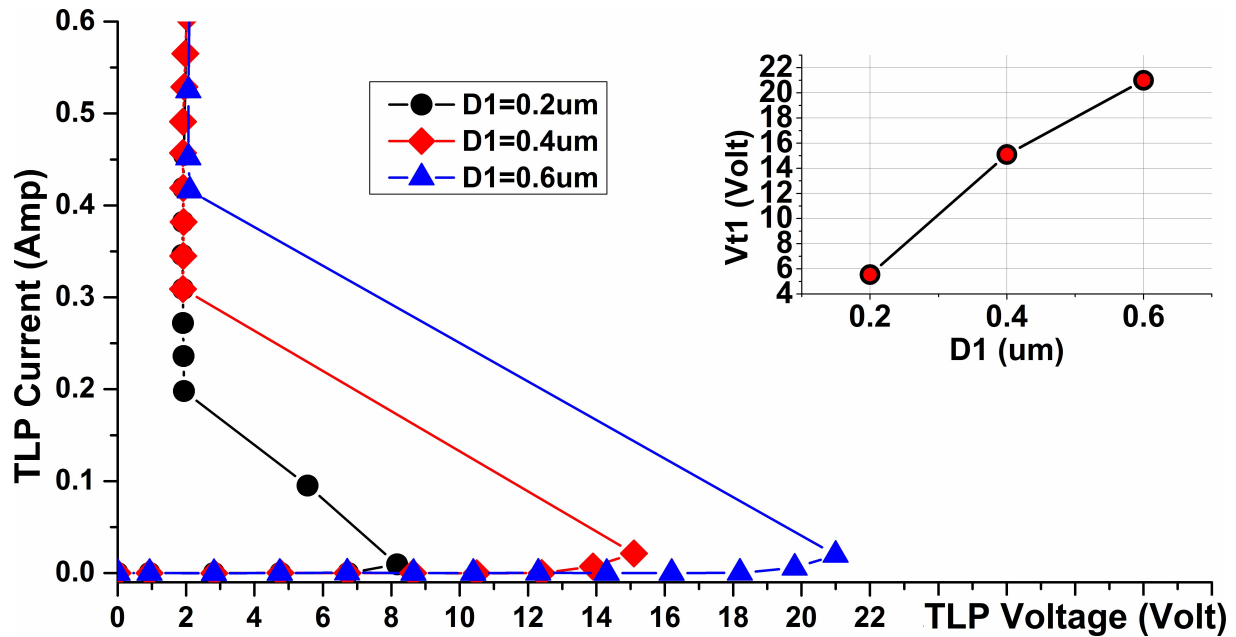
Figure 5.3: TLP I-V characteristics for the NS-SCR's with D1 changing from 0.2 μm to 0.6 μm. Insert shows the effect of D1 on the trigger voltage. D2 is fixed at 0.5 μm for all cases.

As expected, D2 is found to play a more important role in determining the holding voltage rather than the trigger voltage. Figure 5.4 compares the different TLP I-V curves for different D2 dimensions, increasing from 1 μm to 4 μm. With D1 being fixed at 0.6 μm, the NS-SCR possesses a trigger voltage of 21 V for all D2 cases. At D2 = 4 μm, the holding voltage is increased to 22 V and the snapback disappears. The device also achieves a high robustness (47 mA/μm) and low on-resistance (0.36 ohm) due to the fact that the ESD current flows via the bulk rather than along the surface. However, the device does suffer a degraded robustness when the snapback is reduced.

For pins operating at even higher voltages, the stacking technique is typically used to meet the ESD design window. To this end, we propose two NS-SCR cells (Cell A and Cell B with D1 and D2 listed in Table 5.1) as the stacking units. These cells are optimized to operate without snapback, and clamps that meet various ESD design windows can be constructed by stacking different numbers

of Cell A and Cell B. Figure 5.5 shows the TLP I-V curves of three example configurations. These cases of 1xCell B, 2xCell B, and 1xCellA+1xCellB are ideal ESD clamps for protecting pins operating below 18, 30 and 36 V, respectively. The 2xCell B structure consumes 41% less area than the stacking MLSCR reported in [23]. It should be pointed out that the failure current It2 of the stacking structure is primarily determined by the robustness level of the individual cell, such that the robustness of the stack does not depend on the stacking number.
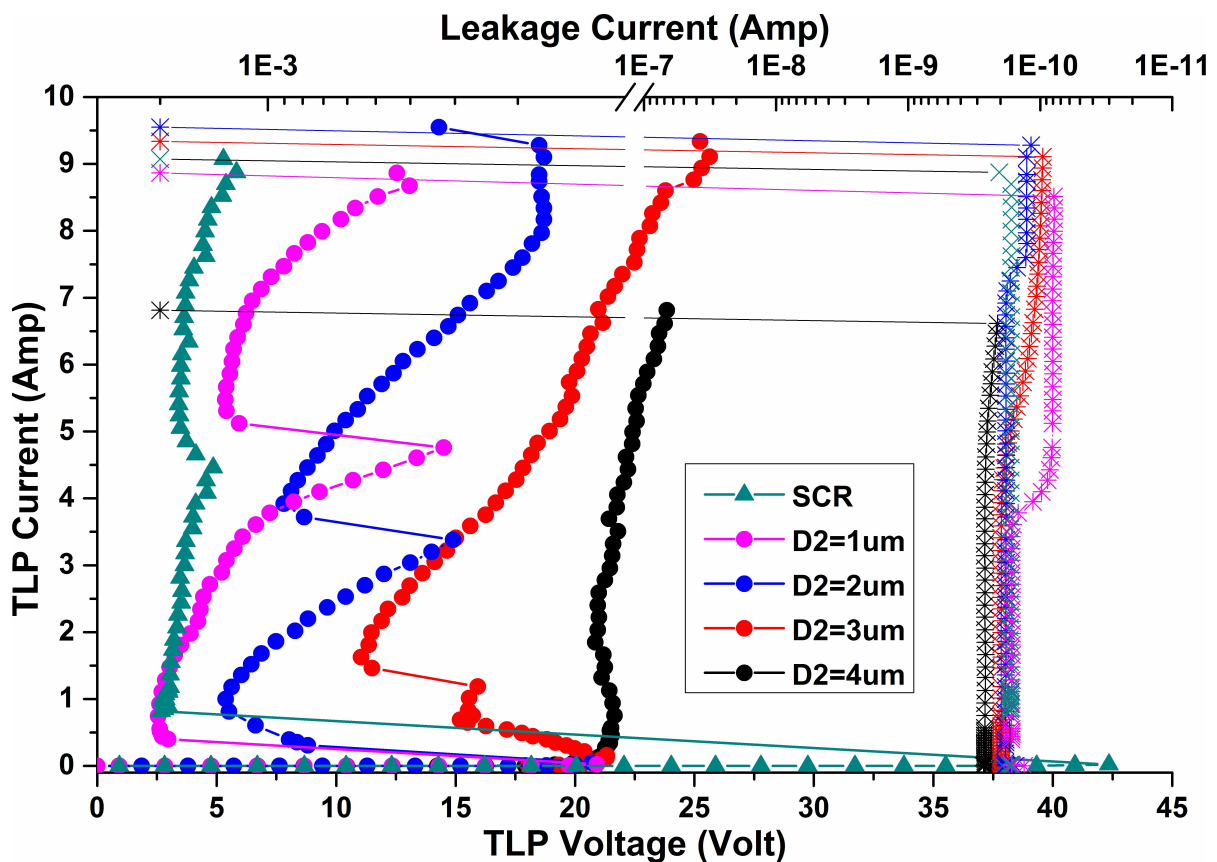
Figure 5.4: TLP I-V characteristics for the traditional SCR and NS-SCR's with D2 changing from 1 μm to 4 μm. D1 is fixed at 0.6 μm for all cases.
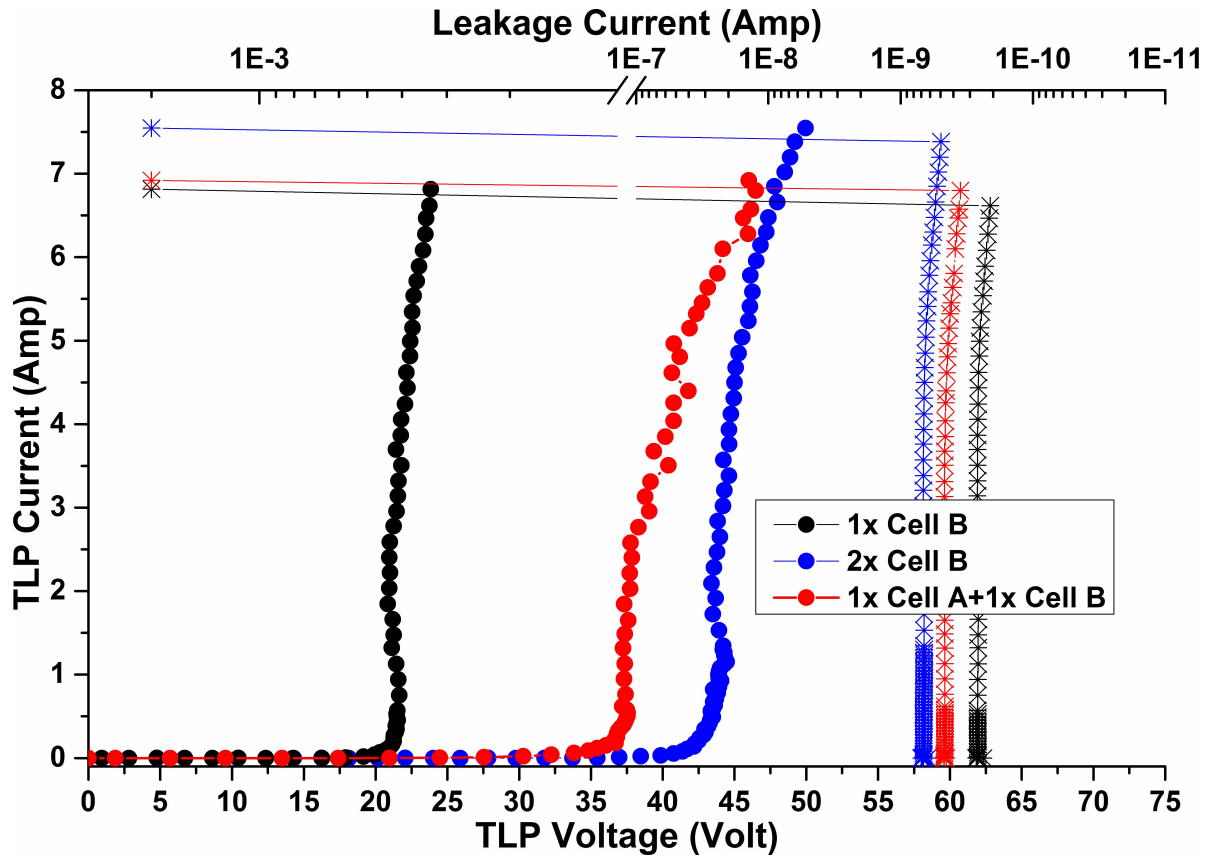
Figure 5.5: TLP I-V characteristics for stacked Cell A and Cell B.

5.4   Thermal Stability of Leakage Current

High temperature environments, in which the automotive and power electronics operate, can give rise to an unacceptably high leakage current in SCR-based clamps. Increased power consumption or even damage to the circuit or system may occur if the protection clamp becomes leaky. To evaluate the leakage current performance of the traditional SCR and proposed Cell A and Cell B under high temperature conditions, DC sweeps were conducted at 25 (room temperature) and 125 deg-C. Figure 5.6 shows the leakage current vs. DC voltage characteristics of the three devices. At room temperature, Cell A and Cell B become leaky when the DC voltages reach 11 and 17

V, respectively. As the temperature increases from 25 to 125 deg-C, about a 100x increase in the leakage current is observed for all three devices. While the proposed NS-SCR's are slightly more leaky than the traditional SCR, particularly at room temperature, their leakage currents nonetheless are still within an acceptable range under elevated temperature conditions.
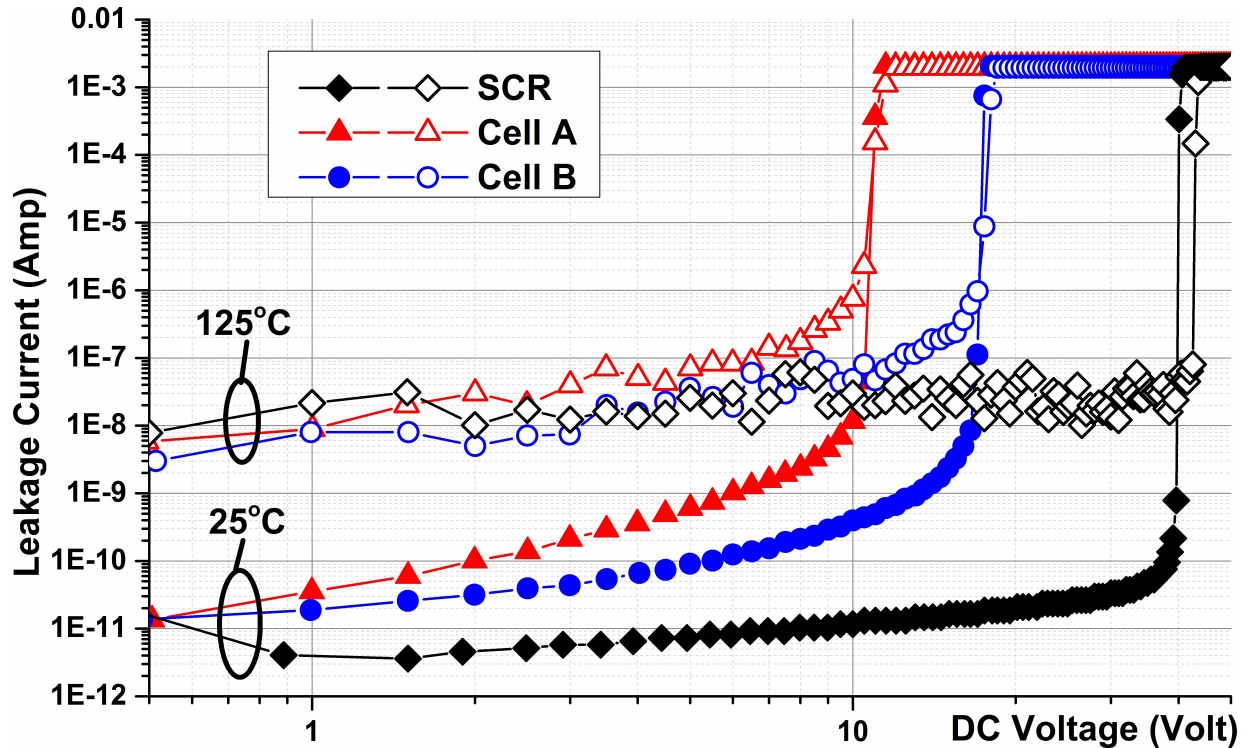
Figure 5.6: Leakage current vs. DC voltage characteristics of SCR, Cell A and Cell B at temperatures of 25 and 125 deg-C.

5.5   Conclusion and Remark

A new SCR, called the NS-SCR, fabricated in a 0.35 μm BCD technology was realized and evaluated. By embedding a PIN diode in the traditional SCR, the NS-SCR's trigger voltage can be tuned and the holding voltage can be increased to equal the trigger voltage, thus resulting in an

ESD clamp with a no-snapback characteristic highly suitable for ESD protection of high voltage integrated circuits. The study further demonstrated that stacking the NS-SCRs can offer improved flexibility, better area efficiency, and higher robustness than the existing approaches for circuits that operate at even higher voltages. The leakage currents of NS-SCRs at 25 and 125 deg-C were also examined, and the devices demonstrated a fairly good thermal stability under elevated temperature condition. This work has useful applications to the development of effective ESD protection solutions for automotive and power integrated circuits.

CHAPTER 6: ESD PROTECTION DESIGN FOR GAN TECHNOLOGY

In this chapter, a robust and effective GaN-pHEMT-based electrostatic discharge (ESD) protection structure is developed for the first time. The structure consists of a depletion-mode GaN pHEMT, a trigger diode chain, a pinch-off diode chain, and a current limiter. Results pertinent to critical ESD parameters, such as the trigger voltage, leakage current, on-state resistance, and robustness are measured using the transmission line pulsing (TLP) tester. It is demonstrated that such an ESD clamp can sustain a TLP stress of up to 3 A. The two diode chains are found to play critical roles in determining the trigger voltage and leakage current. Increasing the trigger diode number increases the trigger voltage. On the other hand, adding more pinch-off diodes also increases the trigger voltage and at the same time reduces the leakage current. The design trade-offs for the proposed ESD clamp are also discussed.

6.1   Introduction

Radio frequency (RF) and microwave power amplifiers are increasingly important to modern communication systems. A frequently used compound semiconductor technology, e.g., gallium arsenide (GaAs), does not offer sufficiently high power density, efficiency, and linearity. Gallium nitride (GaN) technology has gained popularity recently as it possesses improved power performance due mainly to its wide bandgap characteristics [41], [42]. However, damages resulting from the electrostatic discharge (ESD) events are key reliability issues in RF electronics, and ESD protection issues must be properly addressed before the emerging GaN technology can be widely used in the consumer market.

Research works on ESD in GaN technology have been very limited to date. The ESD robustness

of a GaN Schottky diode was studied in detail in [43]. Failure mechanisms of a GaN pHEMT under the ESD stress were reported in [44]. However, these works focused mainly on the basic characterizations of GaN devices under the transmission line pulsing (TLP) stress, and issues specific to the development of a practical and implementable GaN-pHEMT-technology-based ESD protection solution are still not yet being addressed in the literature. It is worth mentioning that GaAs-pHEMT-technology-based ESD clamps were developed recently [45], [46].

This letter aims to develop for the first time an effective and operational ESD clamp fabricated in a 0.35-μm depletion-mode (D-mode) GaN pHEMT technology. The targeted applications are ESD protection of I/O pins of GaN-pHEMT-based power and low-noise amplifiers used in wireless communication applications with an operating voltage in the range 2 to 4 V [47]. Parameters critical to ESD design, such as the trigger voltage, leakage current, on-state resistance, and robustness, will be characterized using the TLP tester. The subject of GaN-pHEMT-based ESD protection for circuits operating in a higher voltage regime is beyond the present scope and will be developed in the future.

6.2   ESD Clamp Structure

Figure 6.1 shows the cross-sectional view and equivalent circuit for the proposed ESD clamp, which consists of a single-gate, D-mode GaN pHEMT, a trigger diode chain, a pinchoff diode chain, and a current limiter. The GaN devices (i.e., pHEMT and Schottky diodes) are fabricated on a silicon wafer. AlGaN and GaN layers are deposited on top of the buffer layer. It should be noted that, in theory, the pinchoff diode chain is not needed for constructing an enhancement-mode-pHEMT-based ESD clamp. Figure 6.2 shows the Formula characteristics of the pHEMT biased under the dc condition. The GaN pHEMT itself would not work properly under the TLP regime.

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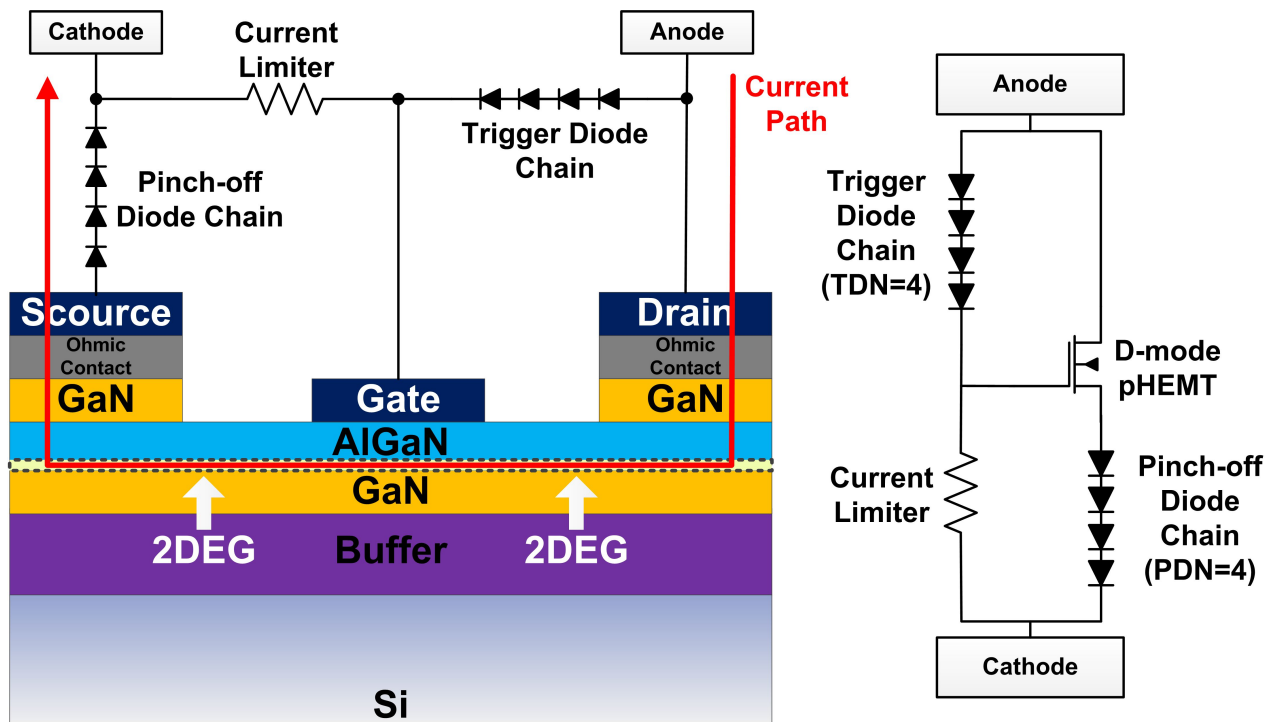
Figure 6.1: Cross-sectional view and equivalent circuit of the proposed ESD protection clamp, consisting of a single-gate D-mode GaN pHEMT, a trigger diode chain, a pinch-off diode chain, and a resistor (current limiter). Red line: the current path after the clamp is turned on.

The IV curves shown in Figure 6.2 are the dc characteristics of the GaN pHEMT without the trigger diode chain, pinchoff diode chain, or current limiter. The D-mode pHEMT must be turned off during the normal core circuit operation, thus requiring the placement of the pinchoff diode chain. The trigger diode chain is needed to turn on the pHEMT when the pin is subjected to an ESD event.

The pHEMT-based clamp can still be triggered without the trigger diode chain, under a triggering mechanism similar to that of the traditional grounded-gate n-MOS clamp, but in this case, the trigger voltage will become uncertain as it depends heavily on the pHEMT structure and the resistance connected between the gate and source terminals.
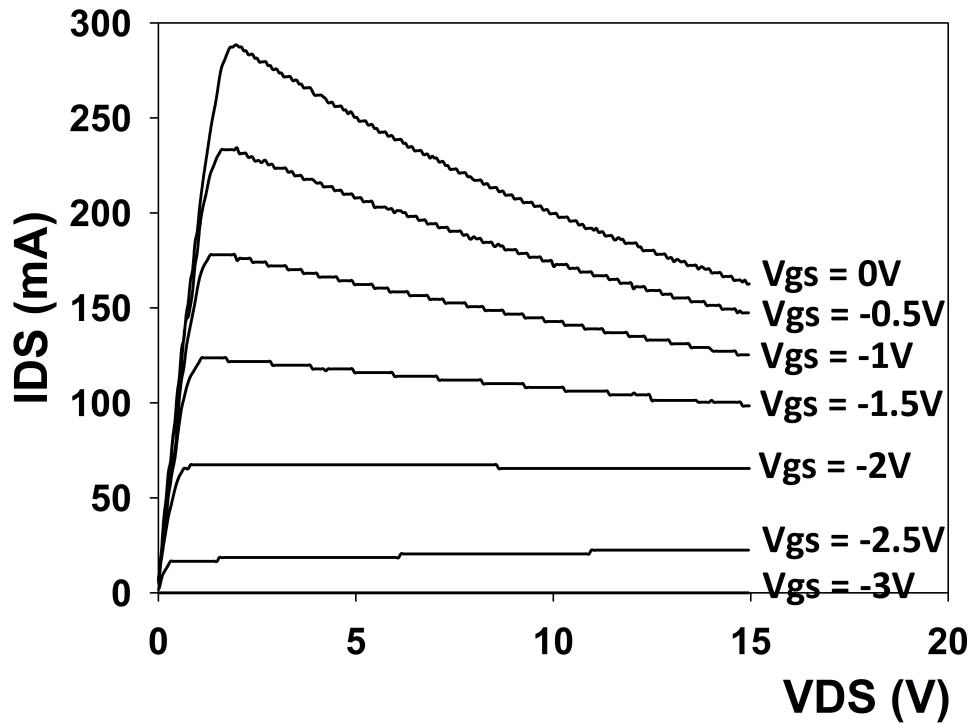
Figure 6.2: Measured steady-state Formula curves of the pHEMT used in the proposed ESD clamp.

The pinchoff diode chain plays another role in limiting the leakage current passing through the GaN pHEMT under the normal operation. As will be shown later, the larger the number of pinchoff diodes, the smaller the leakage current. This of course comes at the expense of a larger footprint and on-resistance. The current limiter produces a voltage drop between the gate of pHEMT and the ground when the trigger diode chain is turned on, thus influencing the triggering of the clamp. The areas of the pHEMT, diode in the trigger diode chain, and diode in the pinchoff diode chain are $188\mu m \times 184\mu m$, $106\mu m \times 111\mu m$, and $196\mu m \times 169\mu m$, respectively.

The trigger diode number and pinchoff diode number are hereafter denoted as TDN and PDN, respectively. Let us consider the case of TDN=PDN=4. Under the normal operation, the gate voltage of the D-mode pHEMT is pulled down through the current limiter, whereas the source

voltage is pulled up due to the pinchoff diode chain. Thus, the clamp is turned off and the current flowing between the anode and cathode is small. When an ESD event occurs and the voltage at the anode is larger than the turn-on voltage of the trigger diode chain, a current starts to flow through the current limiter, and a voltage is built up at the gate terminal. When the gate-source voltage Vgs is higher than the threshold voltage of pHEMT (about -2V), the depletion region underneath the gate is reduced, and the 2-D electron gas channel near the AlGaN/GaN interface is formed. A current conducting path is then created in the pHEMT and is capable of shunting the ESD-induced current [see the red line shown in Figure 6.2].

6.3   Measurement Results and Discussions

A Barth 4002 TLP tester is used to evaluate the ESD performance of the GaN-pHEMT-based clamp. Explanations on the correlation of TLP and human body model (HBM) are necessary. The usual correlation of 1 A of TLP failure current equal to 1.5 kV of HBM passing voltage was derived from the theory that, in the HBM event, the human body skin serves as the current discharging path. However, it has been found that the traditional TLP and HBM correlation can become invalid for some technologies [48]. As such, we will describe the stressing conditions used in this letter only in the TLP terms.

We will first demonstrate the rationale of using the proposed ESD clamp, as opposed to a conventional diode chain. Figure 6.3 compares the TLP IV curves measured from the GaN pHEMT clamp (with PND=TDN=4) and a chain of five GaN Schottky diodes connected in series. To make a sensible comparison, these two structures have similar trigger voltages and areas. Clearly, the GaN pHEMT clamp is superior to the diode chain in terms of the leakage current (1 μA versus 10 μA), on-state resistance, and failure current (3 versus 2 A). The robustness of the pHEMT clamp is much higher than that of the diode chain due to the significant current saturation effect in the

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diodes. The smaller leakage current of the pHEMT clamp stems from the fact that the pHEMT is fully turned off under the normal operation such that the leakage current is effectively blocked.
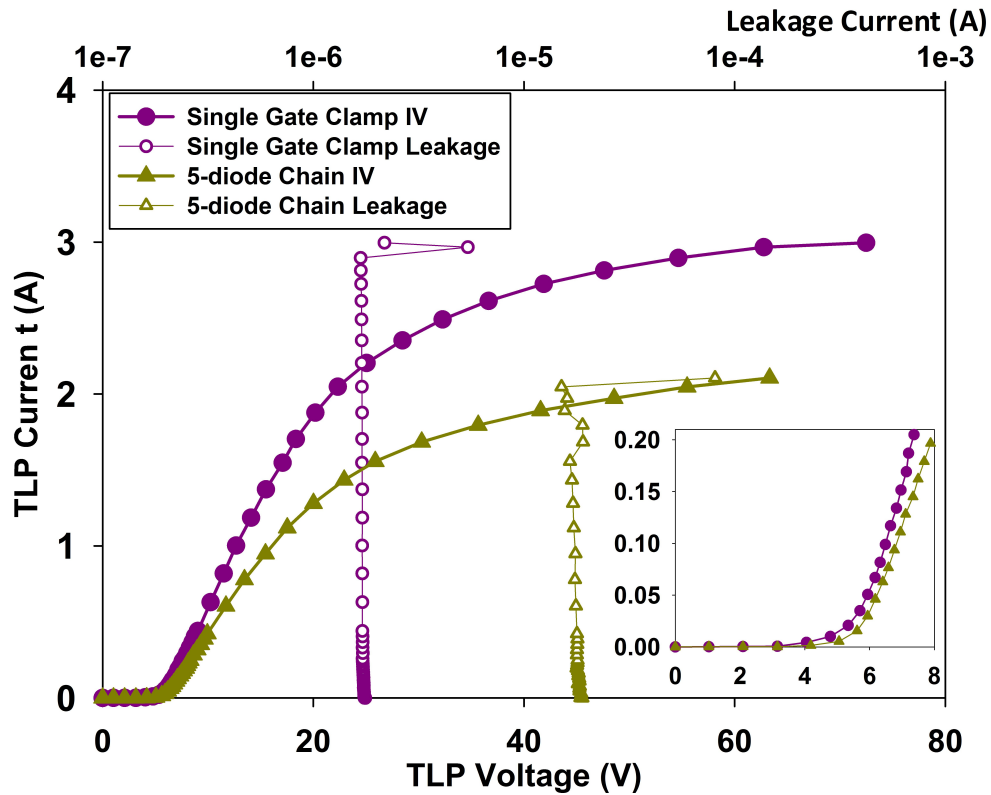
Figure 6.3: Comparison of TLP IV curves measured from the GaN pHEMT clamp and five-diode chain.

We next investigate and discuss the effects of the TDN and PDN on the trigger voltage, leakage current, on-state resistance (Ron), and failure current (It2). Table 6.1 lists the data of these parameters measured from the GaN pHEMT clamp with different TDN and PDN combinations. As the TDN increases from two to four, the trigger voltage increases linearly. This is because, during an ESD event, the voltage on the anode needs to be larger than the blocking voltage of the trigger diode chain to pump a current through the current limiter for triggering the clamp. The blocking voltage of the trigger diode chain equals the number of diodes times the turn-on voltage of the

individual diode, which is about 0.7 V. The pinchoff diode chain provides a similar effect on the trigger voltage; that is, reducing the PDN also decreases the trigger voltage. When a diode is added to the pinchoff diode chain, the pHEMT's turn-on voltage, as thus the trigger voltage of the ESD clamp needs to be increased by the turn-on voltage of the diode.

Table 6.1: Comparisons of Trigger Voltage, Leakage Current, On-state Resistance, and Failure Current using different TDNs And PDNs.

TDN	PDN	Trigger Voltage (V)	Leakage Current (A)	Ron (ohm)	It2 (A)
2	4	4.6	1.50e-4	3.54 to 377	2.73
3	4	5.2	2.23e-5	3.42 to 348	2.97
4	4	6	1.93e-6	3.36 to 335	3
4	3	4	9.42e-5	3.46 to 9.75	3.72
4	2	N/A	2e-3	N/A	N/A
4	1	N/A	2e-3	N/A	N/A

Both the TDN and the PDN can influence greatly the leakage current. As the TDN is reduced, the leakage current increases because the voltage drop on each trigger diode is higher, and a larger leakage current is therefore generated. Reducing the PDN will also increase the leakage current, as a smaller PDN decreases the voltage on the source of pHEMT, resulting in a larger Vgs and a higher leakage current through the clamp. For the case of a relatively small PDN, such as PDN=1 or 2, no valid TLP results can be obtained, as a chain of one or two pinchoff diodes is not enough to fully turn off the pHEMT, and the resulting leakage current (larger than 2 mA) is far beyond the acceptable value for practical applications.

Also shown in Table 6.1 is that changing TDN does not affect strongly the pHEMT clamp's on-state resistance or robustness. This is because the majority of the ESD-induced current flows through the pHEMT and pinchoff diodes. This also explains the trend in which the on-state resistance is decreased when the PDN is reduced. The smaller PDN also leads to a higher robustness (higher It2) because of a smaller voltage drop and thus a smaller power dissipation in the pinchoff diode

chain under the same current level.

For ESD applications requiring a higher trigger voltage, using a larger TDN is an option. However, the tradeoff is increased area consumption. Another option is to use a reverse-biased diode. Increasing the PDN can also increase the trigger voltage, but this approach is not recommended since it will give rise to an increase in the on-state resistance and to a decrease in the failure current. Nevertheless, a reasonably large PDN should be employed so that the leakage current is suppressed to an acceptable level. The above-mentioned tradeoffs are a key to the design and development of effective ESD clamps in the GaN pHEMT technology.

6.4　Failure Analysis

Figure 6.4 shows a photograph of the topology of the GaN pHEMT clamp taken after the clamp had a hard failure under the TLP stress. From the enlarged pictures, damages can be seen on the pinchoff diode chain. Furthermore, the failures are found to be located close to anode sides of pinchoff diodes, suggesting that the nonuniform current crowding occurs at these locations. Thus, pinchoff diodes with shorter finger lengths and larger finger numbers can provide more uniform current distribution and therefore higher robustness for the proposed ESD clamp. The pHEMT and trigger diode chain do not exhibit any damage. This, together with the fact that the areas of the pHEMT and pinchoff diode are comparable with each other but the area of the trigger diode is smaller than that of the pHEMT and pinchoff diode, indicates the pinchoff diode chain is the component limiting the robustness of the proposed ESD clamp.
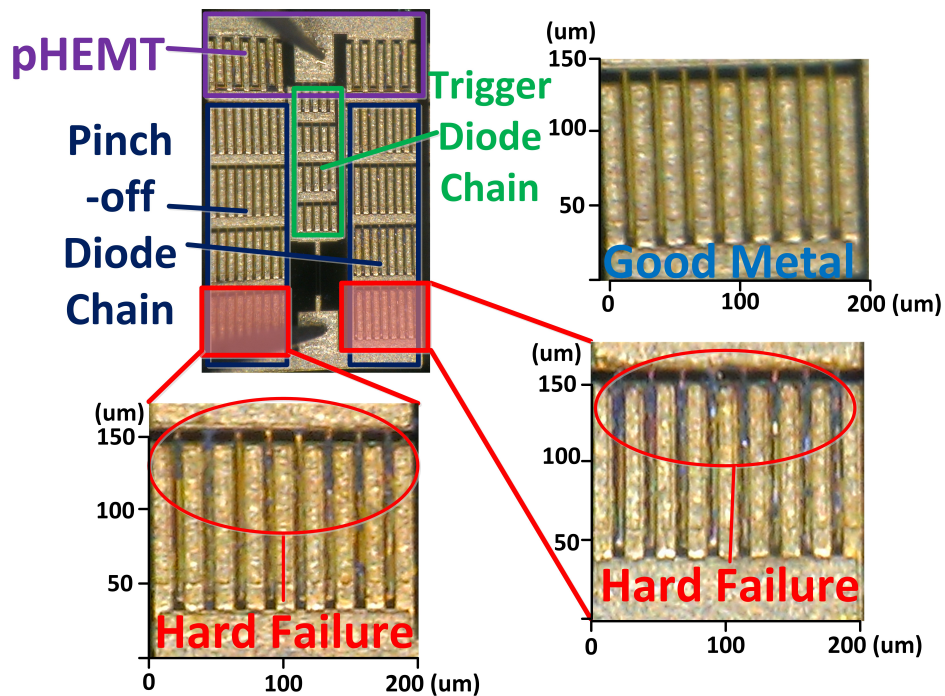
Figure 6.4: Photograph of the GaN pHEMT clamp, with enlarged pictures showing hard failures on the pinchoff diode chain.

6.5   Conclusion and Remark

A practical and effective ESD clamp intended to protect RF power and low-noise amplifiers fabricated in the emerging GaN pHEMT technology was developed for the first time. It was verified that the proposed clamp is superior to the conventionally used diode chain. The clamp consisted of a GaN pHEMT, two diode chains, and a resistor. Critical issues pertinent to the ESD design, including the trigger voltage, leakage current, on-state resistance, and robustness, were analyzed. The impact of the two diode chains on the ESD performances of the GaN pHEMT clamp was also discussed. It offers useful applications to the realization of ESD protection solutions in the emerging GaN technology.

CHAPTER 7: CONCLUSION

The rail-based ESD protection network containing diodes and power clamp used to be the general solution for silicon-based semiconductor technologies, but the story has changed since the fabrication techniques evolve to an new era. The technologies are still being pushing more and more closer to the physical limit of a single atom, and even the Moore's Law has been extended to be available for the usages in the future. However, one tendency that can be always found in current advanced technologies is the increasing complexity, such as the high-K metal gate, the multiple doping wells, fin-fet, and new semiconductor materials like GaN, GaAs, etc. ESD protection for these developing technologies is no exception. The physical scaling down of technologies shrink the ESD protection window. The portable applications of electronics such as cell phone, pad, laptop induce complicated system-level ESD/EOS damages. More and more ESD standards are created to regulate the reliability of ICs. All of these require that the ESD protection design shall be performed in both customized and systematic way.

However, the core of ESD protection design remains unchanged, which is to create an ESD discharge path with low resistance. The variations of technologies also provide lots of possibility to design ESD protection. In this dissertation, the first part discusses the optimization design of the popular SCR and provides very useful design guideline when drawing its layout. A basic SCR is used with research conducted on the geometry and metal pattern layout. It is found out that a Cathode-Anode-Cathode structure with two fingers configuration, and two contact columns in the emitter active regions of parasitic bipolar transistors can offer the optimized ESD performance. The research in the second and third parts apply this rule in the layout of SCR-type devices.

The second part in this dissertation discusses the high-speed design of the SCR, which normally turn on very slow because of the triggering mechanism using avalanche breakdown. External trig-

ger can increase its response speed to a small extend but at the expense of larger area consumption. Recently dummy gate technique gains much attraction due to its effectiveness in speeding up SCR. The main innovation of DCSCR studied in this part is to utilize the internally embedded diodes as the triggering element to turn on the parasitic bipolar transistors, or, the SCR, realizing by connecting Anode Gate to Cathode Gate. It is capable of saving the time that the carriers in trigger current need to flow from anode to cathode because the trigger current shares the path of SCR current. With a very simple layout modification from LSCR, it is proved that the DCSCR not only maintains the same robustness and area efficiency as LSCR, but also offers superior performance including faster turn on speed, lower overshoot voltage, smaller parasitic capacitance, and a very stable thermal leakage current in an acceptable range. The dummy gate technique can be easily applied on DCSCR to further increase its turn-on speed. With a no-snapback and diode-like IV characteristic, the compact DCSCR is also suitable for stacking so as to fit in ESD design window with higher operating voltage.

The third part in this dissertation discusses the bidirectional design of SCR. The proposed PTBSCR embeds a PMOS device into the traditional BSCR so that the trigger voltage can be reduced to 2.95 V. The gate on the PMOS can also be biased up to VDD to further decrease the leakage current. Sentaurus TCAD is used to help explain the operation mechanism of the PTBSCR. Finally the vf-TLP performance of PTBSCR is verified to be improved from the previous bidirectional SCR.

The fourth part in this dissertation proposes a novel design on traditional high voltage SCR, named as NS-SCR. A PIN diode in embedded in the middle epitaxial region. This diode has three critical functions in NS-SCR's ESD performance. At first the width of the intrinsic region in the PID diode can effectively adjust the trigger voltage. Experimental results are verified that the trigger voltage can be increased from 8 V to 21 V. Secondly, this PID diode relocates the peak electric field in the reverse PN junction in SCR after it is triggered. A high holding voltage (22 V) can be achieved with 21 V trigger voltage, thanks to that the high electric field in maintained in the main ESD

current path. A TLP curve without snapback is observed with very high robustness (47 mA/um). Finally, due to the PIN diode, the NS-SCR is verified to have stable and good leakage current at high temperature. These characteristics are very important and attractive for high voltage and high temperature ESD protection applications.

The topic in the last part in this dissertation is changed from silicon to GaN, which is a promising material to construct ICs for high-voltage high-power RF applications. The static diode-trigger pHEMT clamp proposed in this part is the first usable ESD clamp for GaN technology. A string of schottky diodes is used as the triggering element so that the trigger voltage of the clamp is controllable. A additional diode string is necessary in series with the pHEMT so that the leakage current is compressed in normal circuit operation. The effects of the trigger diode and pinch-off diode to ESD performance are studied, following by a brief failure analysis. It is found out that the pinch-off diode limit the robustness of the proposed ESD clamp.

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