2004

Circuit Design And Reliability Of A Cmos Receiver

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CIRCUIT DESIGN AND RELIABILITY OF A CMOS RECEIVER

by

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M.S. University of Central Florida, 2002

A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy
in the Department of Electrical and Computer Engineering
in the College of Engineering and Computer Science
at the University of Central Florida
Orlando, Florida

Fall Term
2004

ABSTRACT

This dissertation explores CMOS RF design and reliability for portable wireless receivers. The objective behind this research is to achieve an increase in integration level, and gain more understanding for RF reliability. The fields covered include device, circuit and system.

What is under investigation is a multi-band multi-mode receiver with GSM, DCS-1800 and CDMA compatibility. To my understanding, GSM and CDMA dual-mode mobile phones are progressively investigated in industries, and few commercial products are available.

The receiver adopts direct conversion architecture. Some improved circuit design methods are proposed, for example, for low noise amplifier (LNA). Except for band filters, local oscillators, and analog-digital converters which are usually implemented by COTS SAW filters and ICs, all the remaining blocks such as switch, LNA, mixer, and local oscillator are designed in MOSIS TSMC 0.35μm technology in one chip.

Meanwhile, this work discusses related circuit reliability issues, which are gaining more and more attention. Breakdown (BD) and hot carrier (HC) effects are important issues in semiconductor industry. Soft-breakdown (SBD) and HC effects on device and RF performance

has been reported. Hard-breakdown (HBD) effects on digital circuits have also been investigated. This work uniquely address HBD effects on the RF device and circuit performance, taking low noise amplifier and power amplifier as targets.

ACKNOWLEDGMENTS

First, my greatest thanks go to Dr. Jiann S. Yuan, for bringing me in UCF and CDRL, and over the past four years, for his continuous financial support, for guiding and challenging me in the pursuit of knowledge, for providing other non-technical advice.

I am grateful to my committee members, Dr. Abdel Ejnioui, Dr. Xin Li, Dr. Kalpathy B. Sundaram, and Dr. Thomas Xinzhang Wu, for their valuable suggestions and comments. Dr. Xin Li corrected typos in equations.

My colleagues in the Chip Design and Reliability Lab are talented people I enjoyed working with. Appreciated are their interactive learning and discussion, cooperation and support.

I would like to thank all those people who helped me from different respects during my stay at UCF.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER ONE: INTRODUCTION

1.1 Motivation

The wireless communication market has grown explosively in recent years with the fast development of new products and services. Current wireless communication systems such as BlueTooth, GSM, PCS, Wireless LANs, and GPS/satellite receivers, utilize the frequency spectrum between 800 MHz to 5 GHz for communication. As technology advances, the consumers demand wireless systems to be low-cost, low- power and with a small form-factor. Scaling of CMOS technologies has defied all predictions of technology limitations, and continues unabatedly toward the deep-submicron region. This not only promises gigabit integration, gigahertz clock rate, and systems on a chip, but also arouses great expectations for CMOS RF circuits in the 1-5 GHz range, where the dominant technologies are currently silicon bipolar and GaAs. Therefore, much recent effort in circuit design for wireless systems has been devoted to the design of a single-chip transceiver implemented in the low-cost CMOS technology [1], [2].

The twentieth century saw the explosion of hardware defined radio (HDR) as a means of communicating all forms of audible; visual, and machine-generated information over vast distances. Most radios are hardware defined with little or no software control; they are fixed in function for mostly consumer items for broadcast reception. They have a short life and are designed to be discarded and replaced. Software radio (SR) uses programmable digital devices to perform the signal processing necessary to transmit and receive baseband information at radio frequency. Devices such as digital signal processors (DSPs) and field programmable gate arrays (FPGAs) use software to provide them with the required signal processing functionality. This technology offers greater flexibility and potentially longer product life, since the radio can be upgraded very cost effectively with software.

With so many wireless standards deployed in the world, even several in one country, a multi-band multi-mode handheld device is a basis for convenient and effective communication.

Gate oxide breakdown has been studied extensively over the past few years. Many papers investigated the defect generation leading to breakdown and the nature of the conduction after breakdown. Recently, researches on the impact of MOSFET gate oxide breakdown on circuits have been reported [3]–[6]. In [6] it was demonstrated that digital circuits would remain functional beyond the first gate oxide hard breakdown, and an equivalent circuit was proposed describing the gate current in an nMOSFET after gate oxide breakdown. On one hand, RF circuits are sensitive to the parameters of their components; therefore BD is reckoned to have

severe impact on the performance of the circuits due to impedance mismatch and gain reduction [7]. On the other hand, big transistors are used in RF circuits; one small spot of BD path [8], [9] through the gate may not cause too much characteristic change. So it is worth investigating the performance of RF circuits after device BD.

1.2 Research Goals

This dissertation tries to design a multi-band multi-mode CMOS cellular transceiver suitable for SDR application, while exploring the possibility of integrating all the building blocks before baseband processing into one chip.

Moreover, this research work deals with breakdown effects on RF performance. The degradation of S-parameters of 0.16 μm NMOS devices due to gate oxide breakdown is examined. An equivalent circuit model for MOSFETs after gate oxide breakdown is proposed. The influence of nMOSFET gate oxide breakdown on the performance of a low-noise amplifier and a power amplifier is studied using the equivalent circuit model.

1.3 Outline

The receiver architectures will be reviewed in Chapter 2.

In Chapter 3, a signle-pole three-throw switch design is presented. In chapter 4, low noise amplifier design issue is addressed. An improvement over existing design method is proposed. Chapter 5 deals with mixer.

In Chapter 6, gate-oxide breakdown effect on device and circuit RF performance is explored. An equivalent BD circuit model is proposed, and used to evaluate BD impact on RF circuits.

CHAPTER TWO: TRANSCIEVER ARCHITECUTURE

2.1 RF Front-end Circuit Fundamental

As described in last section, in a transceiver, RF front-end circuits are usually composed of low noise amplifier, local oscillator, and mixer. The RF signal is received through the antenna, and then amplified by low noise amplifier to improve the signal-to-noise ratio. The output of low noise amplifier is down-converted from RF band to IF or baseband by a mixer. The reference frequency signal is provided by the local oscillator. The front-end circuits are most important blocks because they determine the selectivity and the sensitivity of the transceiver. And they are also the most difficult blocks to design because all of them work in very high frequency band, and are very susceptible to noises and interferences from inside or outside of the transceiver. Therefore, most efforts are put into the RF front-end circuits design.

2.1.1 Low Noise Amplifier

For low noise amplifiers (LNA) in receiving systems, it is important to have low reflection coefficient at the input port, so that the energy of the received signal is totally absorbed and not reflected back causing an inefficient reception. The performance of the antenna filter may also be dependent on a well-defined termination. Thereby it is important to present a well-defined resistance to the antenna or antenna filter. The CMOS common source input port is capacitive and therefore an input resistance of for example 50 Ω has to be achieved by other means.

The first stage in an amplifier is the most important part, as it will have a large influence on the noise figure. The ideal LNA should match the input impedance, be suitable for low voltage applications, and have lower noise contribution, higher gain, and good linearity. The inductively degenerated transconductance is quite often found in articles [10], [21] as a useful LNA. The circuit provides high gain while it still gives a good control of the input impedance.

Another benefit of the inductive series feedback is that the noise can be kept lower than with other solutions to control the input impedance, such as resistive termination, common gate stages and shunt-series feedback.

One way of increasing the gain is to use a cascode with a resonant tank at the output [11]. The current is transformed into a voltage in a resonant tank containing an inductor and a capacitance. Instead of using a lumped capacitance, it is possible to use the input capacitance of

a voltage follower. The voltage follower improves the driving of the next stage (in this case a mixer).

The quality of the input matching is expressed by the input "return loss", S11, one of the s-parameters for LNA.

The reverse isolation of LNAs determines the amount of LO signal that leaks from the mixer to the antenna. The leakage arises from capacitive paths, substrate coupling, and bond wire coupling. In heterodyne receivers with a high first IF, the image-reject filter and the front-end duplexer significantly suppress the leakage because the LO frequency falls in their stopband. In homodyne topologies, on the other hand, the leakage is attenuated primarily by the LNA reverse characteristics. The reverse isolation can also be represented by S_{12}, one of S-parameters for LNA.

In addition to the above parameters, the stability of LNAs is also of concern. In the presence of feedback paths from the output to the input, the circuit may become unstable fro certain combinations of source and load impedances. Since the terminal impedances of duplexers and image-reject filters cannot be modeled accurately now, an LNA design that is nominally stable may oscillate at the extremes of manufacturing variations and perhaps at unexpectedly high or low frequencies.

A constant often used to characterize the stability of circuits is the Stem stability factor, defined as $K = \frac{1+|\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|}$, where S_{11} and S_{22} are input and output return loss, S_{21} and S_{12} are LNA gain and reverse isolation, and $\Delta = S_{11}S_{22} - S_{12}S_{21}$. If K>1 and A<1, then the circuit is unconditionally stable. That means it does not oscillate with any combinations of source and load impedances. The difficulty in using K is that the S parameters of the circuit must be calculated (or measured) for a wide frequency range to ensure that K remains greater than unity at all working frequencies.

From the equation, it is obvious that the LNA stability improves as S_{12} decreases, which means that the reverse isolation of the circuit increases. This can be obtained by using the cascode configuration. The cost of using cascode structure is a little bit higher noise figure.

In addition, a LNA may become unstable because of ac ground and supply loops resulting from bond wire inductance. For BlueTooth and Wireless LAN applications, because of the very high working frequency, even a few nanohenries of inductance may provide considerable coupling between two stages through the ground node, thereby causing oscillation. Therefore, precautions in the design and layout as well as accurate package modeling are essential.

As will be seen, the low noise required of LNAs typically governs the choice of the topologies and parameter values used in the design. This often means that only one transistor can be the

dominant contributor to NF, which usually is the input device, thus ruling out configurations such as source follower and resistive feedback.

2.1.2 Mixer

In a radio transceiver system, it is important that the transmitter does not generate unwanted signals outside the wanted frequency band that can interfere with other transmitted signals, as well as it is important for the receiver to reject unwanted signals. The selectivity of the receiver can be controlled either by a tunable filter or a superheterodyne receiver. The benefit with the tunable filter is that the demodulation can take place at a lower fixed frequency and that it is hard to make a simple tunable high frequency filter.

The single mixer receiver converts both the desired radio frequency (RF) and the image frequency to the intermediate frequency (IF). The suppression of the image RF can be done with an RF filter in front of the RF amplifier or between the RF amplifier and the mixer, but then the IF need to be high enough for the image RF to be outside the receiver frequency band. It is also possible to exchange the single mixer with image-reject mixer architecture. This mixer architecture enables the use of very low IF.

By integrating the receiver mixer on a chip, including the LO quadrature decomposition, it is common to retrieve 30-35 dB of image rejection. It is also possible to find articles reporting

minimum image rejection lower than 30 dB, waiving some of the requirements. A high image rejection is still feasible. The degree of image rejection relies on how well the in-phase (I) and the quadrature phase (Q) branches are matched in terms of gain and phase. The major errors arise from the quadrature decomposition of the local oscillator (LO) and the IF phase shift, but to retrieve a really high image rejection the mixer imbalance becomes equally important.

There is always some kind of imbalance between mixers due to statistical spread in the semiconductor process. The major random variations in a semiconductor process are observed from one batch to another, but even within a batch there are some small variations between the components, usually termed mismatch.

The transfer function of the mixer is time-variant and therefore it is usually simulated with a transient simulation where the output data if Fourier-transformed to get the frequency information of interest. It is possible to use a time-invariant approximation, and thereby be able to evaluate the statistical spread in the frequency domain directly.

2.1.3 Frequency Synthesizer

Frequency synthesizers can be implemented in many ways [12]. For an integrated multi-standard radio transceiver, we want the synthesizer to be able to generate a tunable frequency in the GHz range with low phase noise and low spurious tones using minimum power.

A phase-locked-loop (PLL) based frequency synthesizer with narrow loop bandwidth is the most commonly used technique due to its high performance, namely, low phase noise and low spurious tones. But the need for off-chip high-Q components is not amenable to the integration of the synthesizer. In addition, the narrow loop bandwidth makes it unsuitable in an agile system where fast frequency switching is needed. As will be shown in later chapters, the VCO phase noise is dominant for the whole PLL output phase noise.

2.2 Review of Receiver Architectures

2.2.1 Basic Receiver Architecture

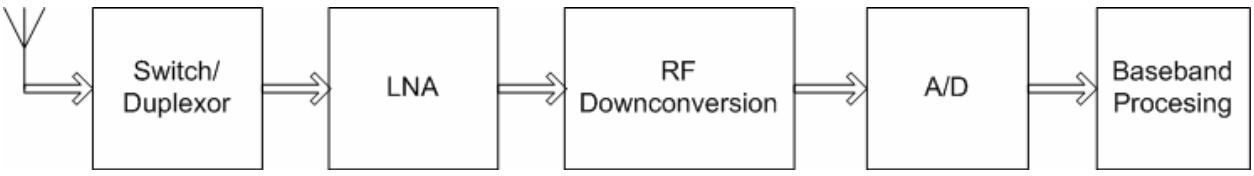


Fig. 1 Basic receiver architecture.

2.2.2 Conventional Superheterodyne Receiver

Most RF communication transceivers manufactured today utilize some variant of the conventional super-heterodyne approach. In this system, shown in Fig. 2, the receiver is implemented with a collection of discrete-component filters and various technologies such as GaAs, silicon bipolar and CMOS.

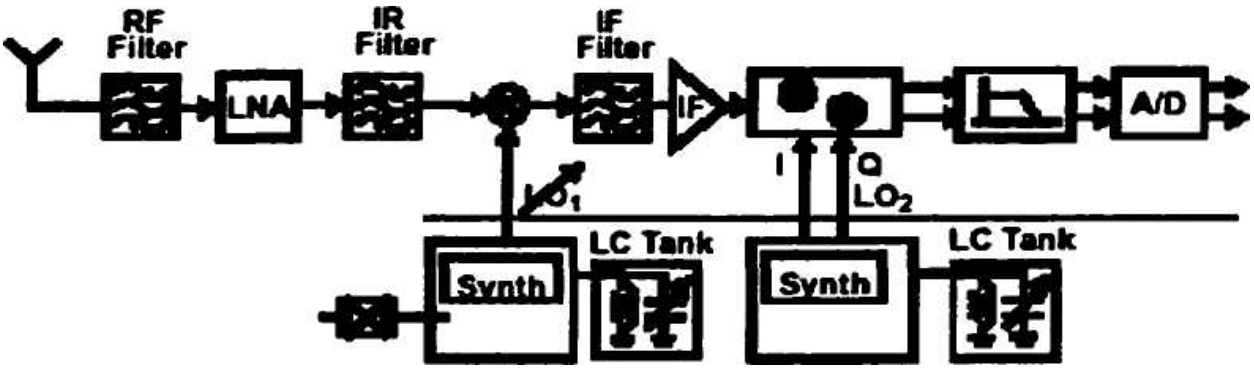


Fig. 2 Conventional superheterodyne receiver.

The purpose of the discrete-component RF front-end filter is to remove out-of-band energy and perform rejection of image-band signals. The noise, or image-rejection filter, which follows the LNA, further attenuates the undesired signals present at the image frequencies. A RF channel-select frequency synthesizer tunes the desired band to a fixed intermediate frequency where a discrete-component filter performs a first order attenuation of out-of-channel energy. High quality, low phase-noise, Voltage Controlled Oscillators (VCO) are typically contain with discrete-component high-Q inductors and varactor diodes.

The challenge of fully integrating a receiver is to replace the functions traditionally implemented by high performance, high-Q discrete components with integrated on-chip solutions. Problems associated with full integration of the receiver can be separated into two categories. First, the integration of the receiver signal path requires the elimination of both the noise, or image-rejection, filter and the discrete-component IF filter. Second, an integrated low-phase noise channel-select synthesizer must be realized using relatively low-Q on-chip VCOs with associated poor phase-noise performance. Three receiver architectures, which attempt to integrate much of the functionality of a discrete component receiver were studied for the promise of integration and providing multi-mode/multi-standard operation.

Depending on the number of mixing stages and A/D sampling position/method, RF downconversion and A/D have the following structures:

2.2.3 Direct Sampling

See Fig. 3.

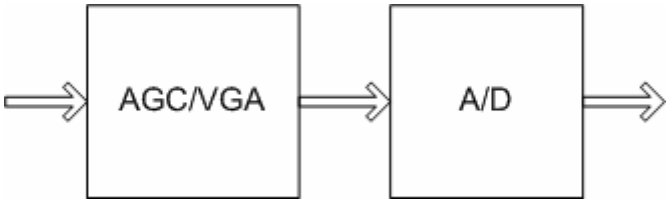


Fig. 3 Direct sampling.

Here, the ADC is doing RF sampling, the sampling method is bandpass sampling because Nyquist sampling or oversampling requires a higher frequency than the one no ADC can operates at in today's technology.

2.2.4 Direct Conversion

It is also called single conversion, homodyne, or zero IF. In this approach, shown in Fig. 4, all of the potential in-band channels are frequency translated from the carrier directly to baseband frequencies using a single mixer stage. Energy from undesired channels is removed with on-chip filtering at the baseband frequency. In a direct conversion receiver, the IF stage is eliminated along with the need for image-rejection filtering.

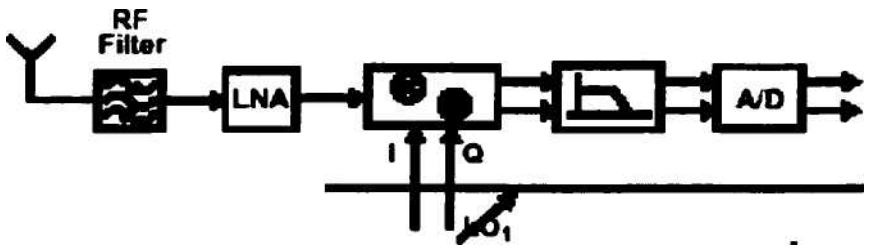


Fig. 4 Direct conversion architecture.

In a homodyne receiver, all of the channels are frequency translated to baseband before any channel filtering is performed. This allows the possibility of on-chip programmable filter structures to accommodate the variable channel bandwidth therefore facilitating multi-mode or multi-standard operation.

Although the direct conversion receiver allows for higher levels of integration than a super-heterodyne system, there are problems associated with this architecture. Because the local oscillator is at the same frequency as the RF carrier, the potential exists for LO leakage to either the mixer input or to the antenna where radiation may occur. The unintentionally transmitted LO signal may reflect off nearby objects and be "re-received" leading to self-mixing with the local oscillator which results in a time-varying or "wandering" DC offset at the output of the mixer. This time varying DC offset, together with inherent baseband circuit offsets as well as DC components arising from second order intermodulation and 1/f noise, significantly reduces the dynamic range of the receiver. In addition, a direct conversion receiver requires a high

frequency, low phase-noise, channel-select frequency synthesizer, which is difficult to achieve with a relatively low-Q integrated VCO.

ADC is doing baseband sampling. Usually it adopts oversampling.

2.2.5 Low-IF

See Fig. 5.

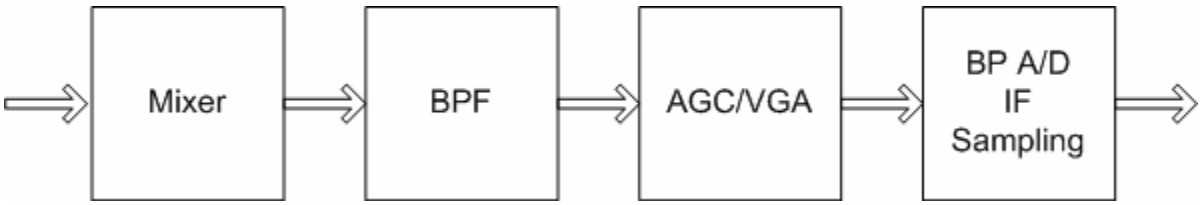


Fig.5 Low-IF.

2.2.6 Dual Conversion

An alternative architecture, well suited for integration of the entire receiver, is the wide-band IF with double conversion architecture [13]. Shown in Fig. 6, this receiver system takes all of the potential channels and frequency translates them from RF to IF using a mixer with a fixed

frequency local oscillator (LO1). A simple low-pass filter is used at IF to remove any upconverted frequency components, therefore allowing all channels to pass to the second stage of mixers. All of the channels at IF are then frequency translated directly to baseband using a tunable, channel-select frequency synthesizer (LO2). Alternate channel energy is then removed with a baseband filter network where variable gain may be provided.

This approach is similar to superheterodyne receiver architecture in that the frequency translation is accomplished in multiple steps. However, unlike a conventional superheterodyne receiver, the first local oscillator frequency translates all of the received channels, therefore maintaining a large bandwidth signal at IF. The channel selection is then realized with the lower frequency tunable second LO. As in the case of direct conversion, channel filtering can be performed at baseband, where digitally programmable filter implementations can potentially enable more multi-standard capable receiver features.

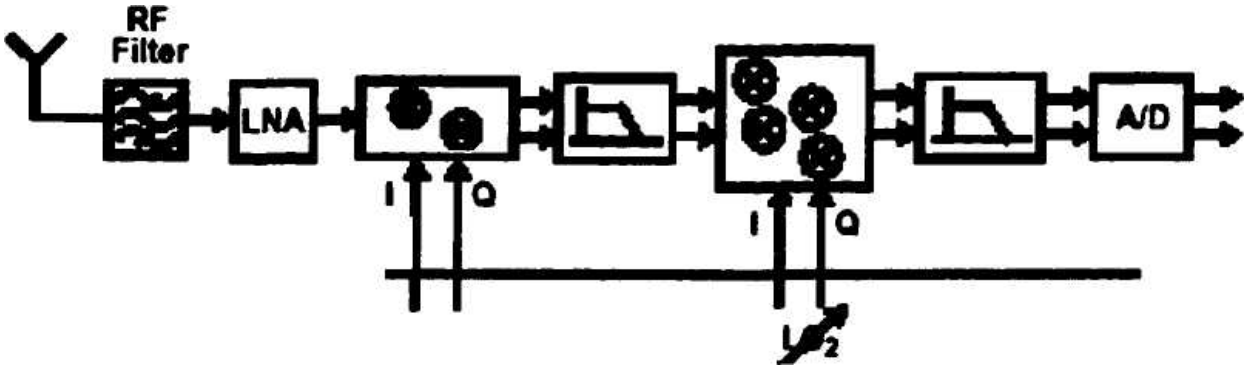


Fig. 6 Wide-band IF with double conversion.

The wide-band IF architecture offers two potential advantages with respect to integrating the frequency synthesizer over a direct conversion approach. The foremost advantage is the fact that the channel tuning is performed using the second lower-frequency, or IF, local oscillator and not the first, or RF, synthesizer. Consequently, the RF local oscillator can be implemented as a fixed-frequency crystal-controlled oscillator, and can be realized by several techniques which allow the realization of low phase noise in the local oscillator output with low-Q on-chip components. One such approach is the use of wide phase-locked loop (PLL) bandwidth in the synthesizer to suppress the VCO contribution to phase noise near the carrier.

2.2.7 Digital IF

See Fig. 7.

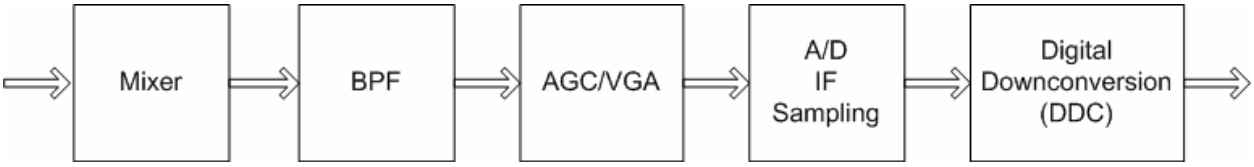


Fig. 7 Digital IF.

2.2.8 Summary

Among the five receiver architectures, zero-IF is the most promising candidate for multi-standard terminals as discussed in [14].

2.3 Different Wireless Standards

Table 1 Different Wireless Standards

Wireless Standard	Access Scheme	Frequency Spectrum(MHz)	Channel Spacing	Modulation Technique
AMPS	FDD	824-849(Tx) 869-894(Rx)	30kHz	FM
DCS-1800	TDMA	1710-1785(Tx) 1805-1850(Rx)	200kHz	GMSK
GSM	TDMA/FDMA/FDD	890-915(Tx) 935-960(Rx)	200kHz	GMSK
EGSM	TDMA	880-915(Tx) 925-960(Rx)	200kHz	GMSK
PCS-1900	TDMA	1880-1910(Tx) 1930-1930(Rx)	200kHz	GMSK
IS-54(IS-136)(D-AMPS)	TDMA/FDD	824-849(Tx) 869-894(Rx)	30kHz	/4 QPSK
DECT	TDMA/TDD	1881-1897	1.728MHz	GFSK
802.11(DSSS)	CDMA	2400-2483		QPSK
WCDMA(UMTS)	CDMA	1920-1980(Tx) 2110-2170(Rx)	5MHz	QPSK
IS-95	CDMA	824-849(Tx) 869-894(Rx)	1.25MHz	OQPSK
Bluetooth(802.11FH)	CDMA/FH	2400-2483	1MHz	GFSK

The most widely used are GSM, DCS-1800 and IS-95. GSM is a standard that was developed by the European standards committee. The original version of GSM was used in the 900 MHz band through Europe. Then an upband version of GSM was added in the 1800 MHz band, which is now DCS-1800. GSM and DCS-1800 have been adopted by a large number of operators worldwide and have been captured the largest global subscriber base among current digital cellular mobile systems. IS-95 is gaining rapid deployment in Asia and North America.

2.4 Architecture

Based on the previous two sections, I am proposing to design and implement a GSM, DCS-1800 and IS-95 compatible digital cellular transceiver, which one can carry traveling around the world without a second mobile phone. There have been multi-band mobile phones, but they are in the same mode, for example, GSM. This transceiver is specifically suitable for China, where GSM, DCS-1800 and CDMA coexist, and the government is managing to realize seamless service transfer between these different networks.

The transceiver architecture is shown below in Fig. 8.

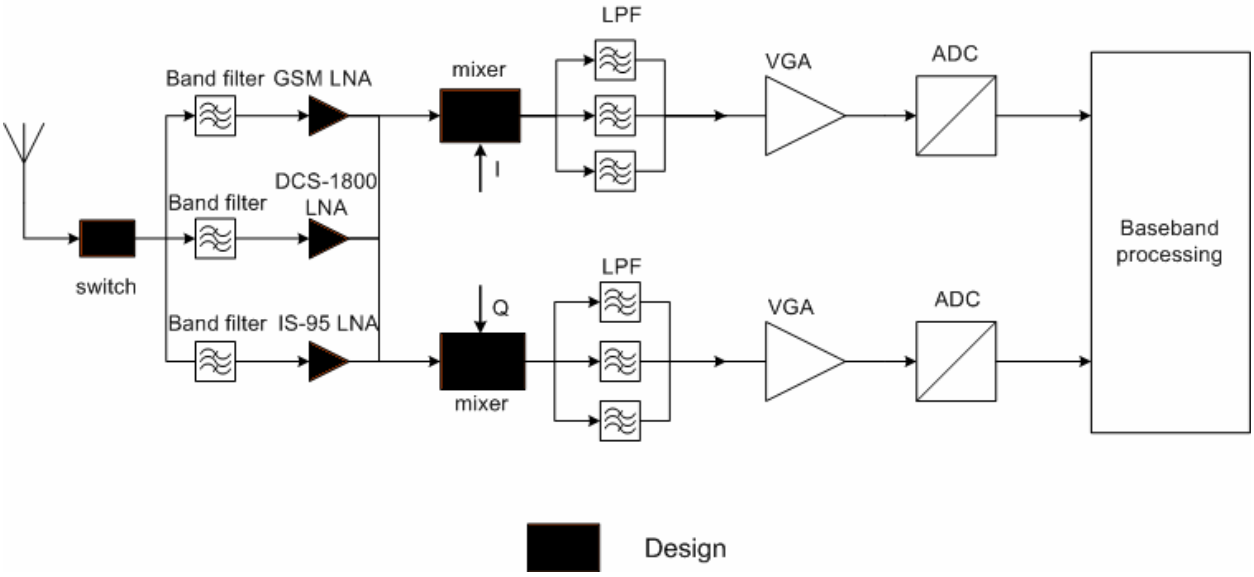


Fig. 8 Receiver architecture.

Signals from antenna will first be band filtered according to the standard the user is using, then amplified and direct down-converted to baseband. After a low-pass filter, the signal is ready to be put into ADC. VGA is need before ADC for proper loading of ADC. Switch, LNA, mixer, and local oscillator is designed in MOSIS TSMC 0.35μm technology.

CHAPTER THREE: SWITCH DESIGN

3.1 Introduction

3.1.1 Switch Parameter Definitions

Switches are used primarily for controlling the signal flow. In wireless applications, switches are used to select different antennas or connect an antenna to a transmitter or to a receiver. The RF power transmitted is high and therefore switch must have loss insertion lost and hide power handling capability to maintain higher power-added-efficiency (PAE) of the power amplifiers. Basic requirements for such switches are low loss, high power handling, high linearity, high switch speeding, single low-voltage power supply operation, low power consumption, small size, and low cost. For the digital cellular communication system, the switch should have low distortion which requires $P_{1dB} > 30$ dBm, and insertion loss of about 1.0 dB at 1.9 GHz [15].

Because of finite impedance of the switching devices, the switch circuits do not have idea performance. The performance of the practical switch can be expressed by specifying its insertion laws and isolation as the basic design parameters.

Insertion loss (*IL*) [16] is defined as the ratio of the power delivered to the load in the ON state of the ideal switch to the actual power delivered to the practical switch, in the ON state.

Isolation (I_{SO}) is defined as the ratio of the power delivered to load for an ideal switch in the ON state to the actual power delivered to the load when the switch is in the OFF state.

3.1.2 Devices for Switches

PIN diodes, MESFETs, and GaAs FETs are used extensively for switches.

PIN diode circuits have lower loss and handle high power levels than do MESFET components; conversely, the latter have greater flexibility in the design of integrated subsystems, consume negligible power, and cost less. A MESFET can provide possible power gain if the device is used in the active mode, that is, the drain is positively biased and the control voltage is applied to the gate.

The microelectromechanical systems (MEMS) for ultr-low-loss switching applications have also been reported.

CMOS switches are relatively less reported in the literature.

3.1.3 Switch Types and Configurations

There are several types of switches, such as single pole single throw (SPST) switch, single pole double throw (SPDT) switch, and single pole multi throw (SPMT) switch. These switches further are further classified into two categories: reflective and nonreflective.

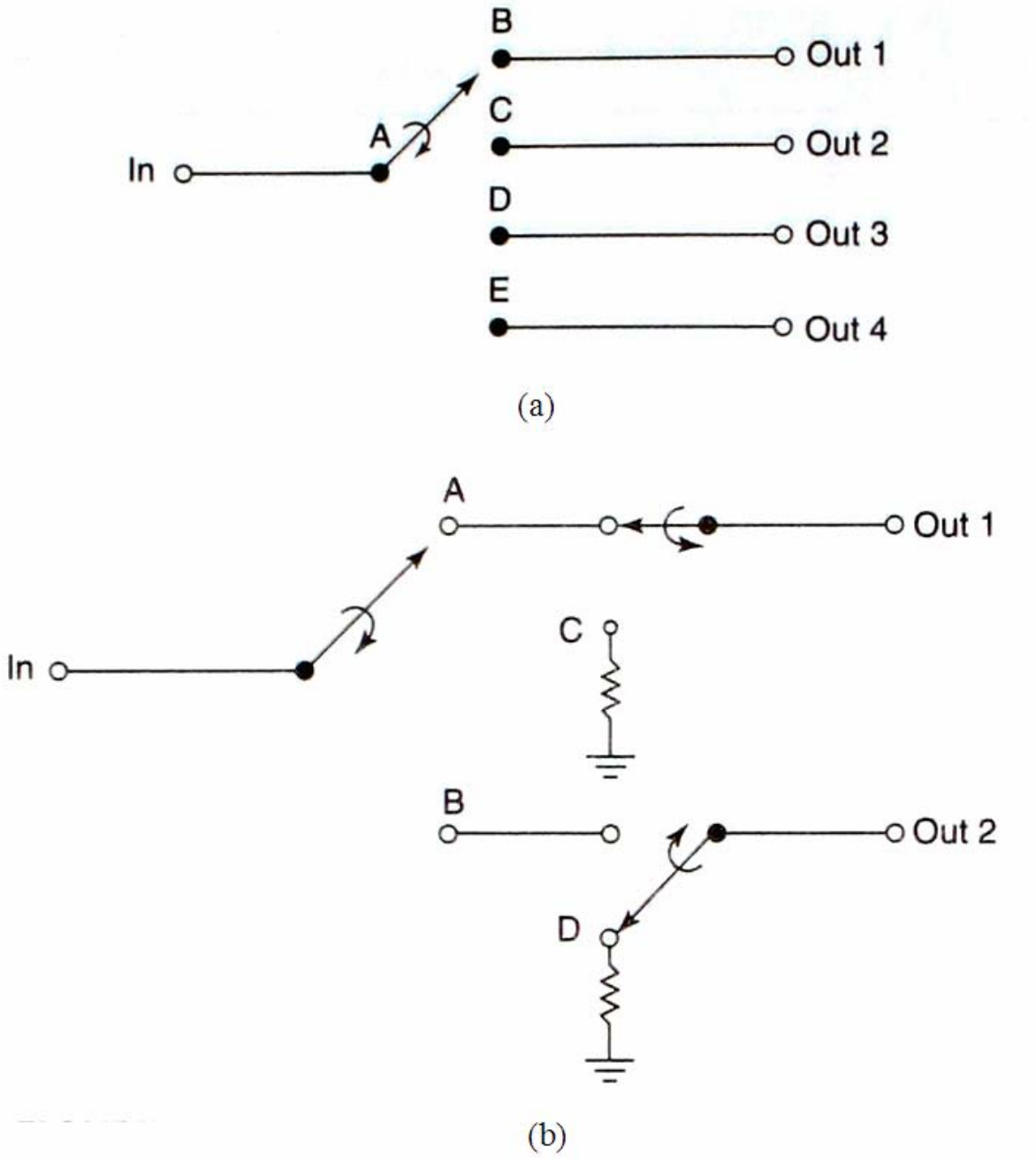


Fig. 9 Switch types: (a) feflective, and (b) nonflective.

The switch shown in Fig. 9(a) is known reflective. This means when the switch is closed between ports In and Out1, port Out2 is not connected or it is open and any signal appearing at this port will be reflected. Switches having the used port terminated in 50 Ω as shown in Fig. 9(b) is called nonreflective. These switches are released by adding a single series FET and 50 Ω resistor combination shunted to ground at each output port. The reflective switch configurations provide lower insertion loss than the nonreflective switch topologies. However, they have low output impedances for a shunt FET or high output impedance for a series FET when the switch is in the OFF state.

There are three basic configurations that may be used for simple switch designed to control the flow of RF signals between various ports. These are shown in Fig. 10 for a SPDT switch, which consist of series, shunt, and series-shunt configurations. The series-shunt configuration is the most popular. The switch is ON when the series device is in the low impedance state and the shunt device is in the high impedance state. In the OFF state of the switch, the series device in the high impedance state and the shunt device is in the low impedance state. Isolation obtained with a series-shunt configuration is much better than that for either series or shunt switch. The insertion loss for the series-shunt configuration is worse than that for a shunt switch but better than that for a series switch.

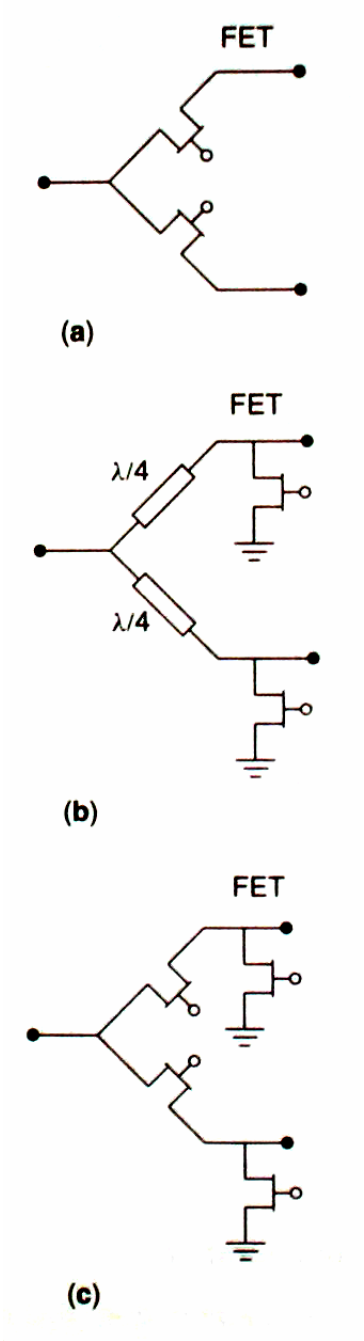


Fig. 10 Switch configurations: (a) series, (b) shunt, and (c) series-shunt.

3.2 Switch Analysis

The switch is designed as a reflective single pole 3 throw (SP3T) switch, shown in Fig. 11. Since the number of throws is small, decoder/driver logic is not needed.

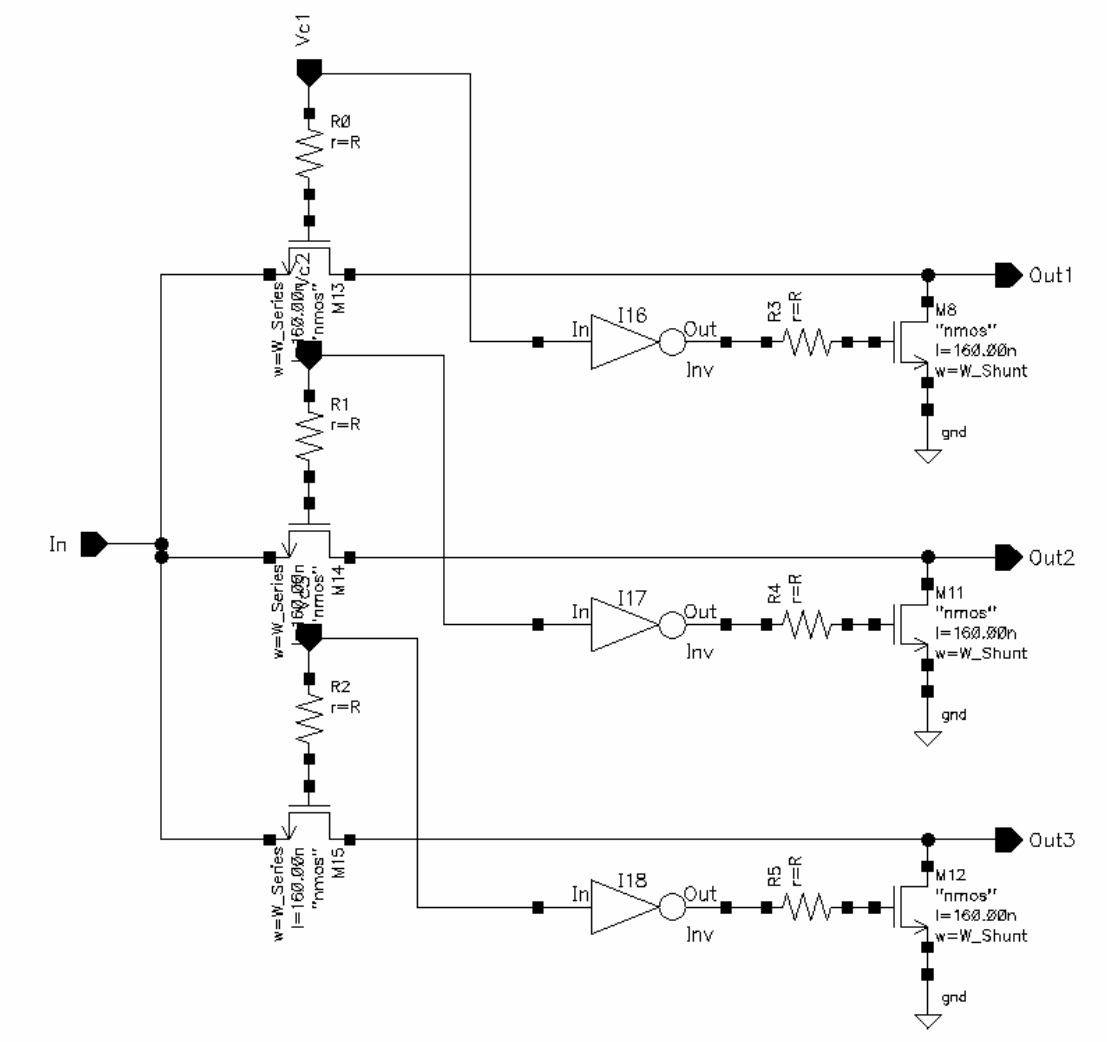


Fig. 11 SP3T schematic.

Switching FETs are modeled by two lumped element equivalent circuit models: one when the deive is ON, and the second one is OFF [17], [18]. Fig. 12 illustrates the circuit schematics and their ON- and OFF-state equivalent circuits for series and shunt arms. The resistance R_s and capacitance C_s represent the parasitic resistance and capacitance resulting from the substrate. R_{on} is the ON-state resistance. The resistance R_{off} and capacitance C_{off} denote the OFF-state resistance and capacitance.

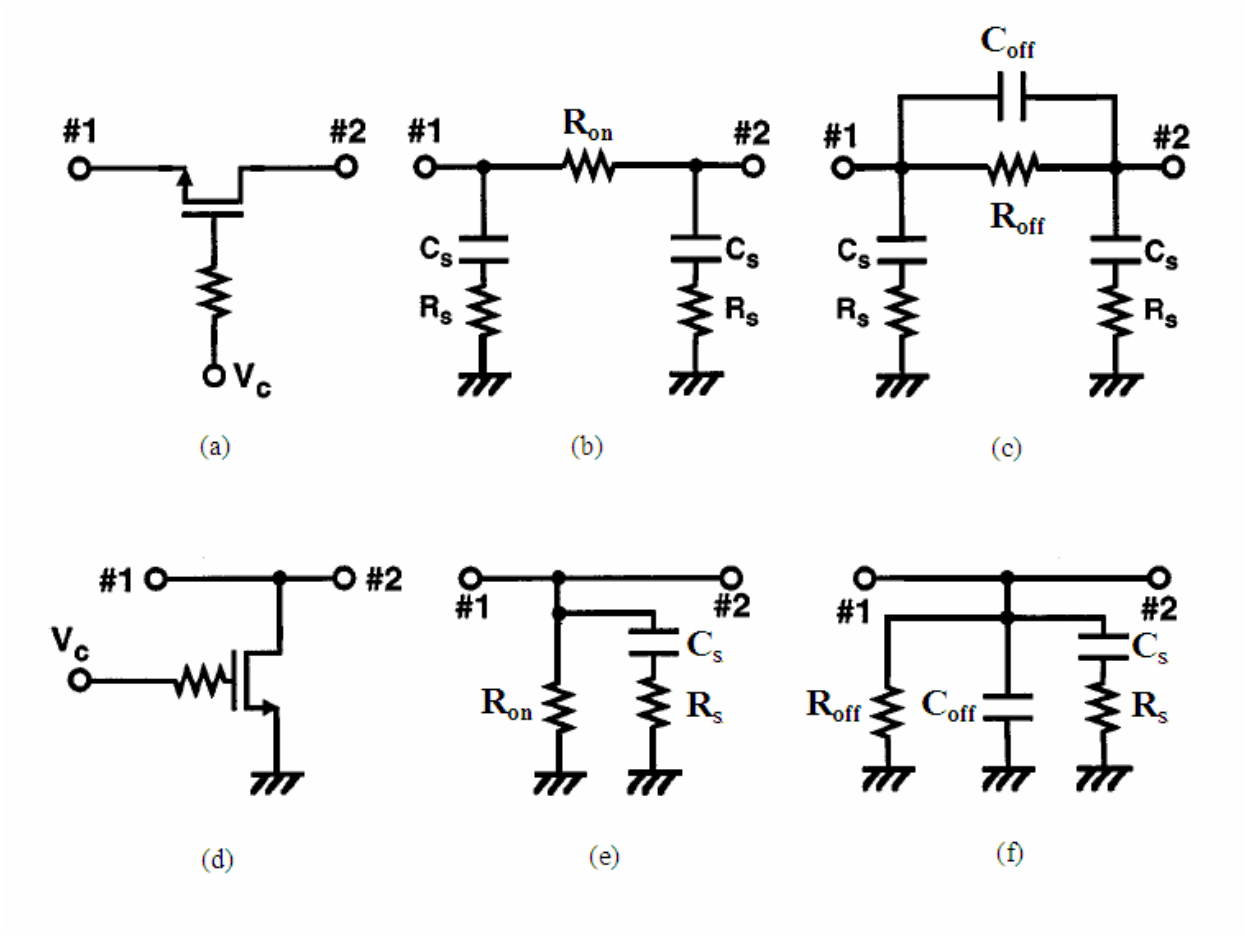
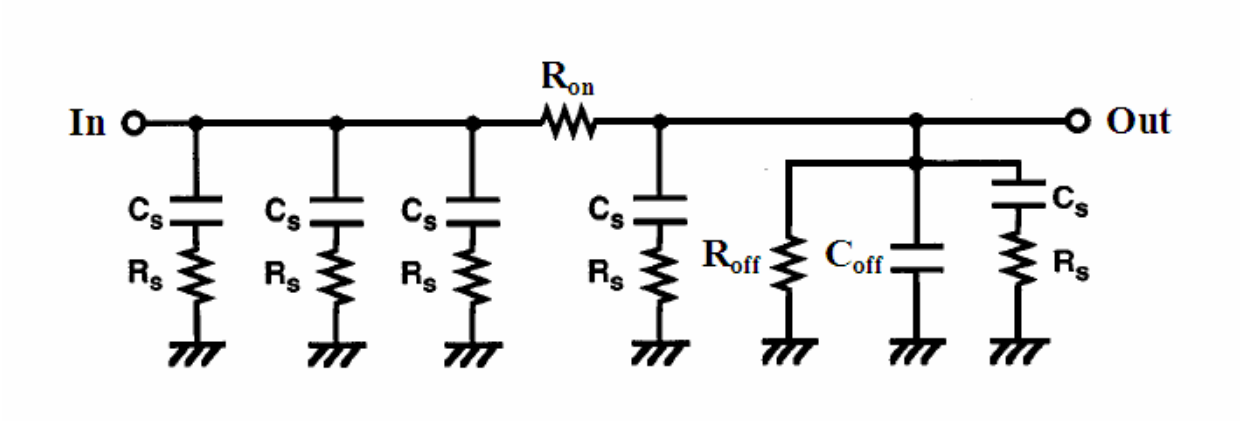
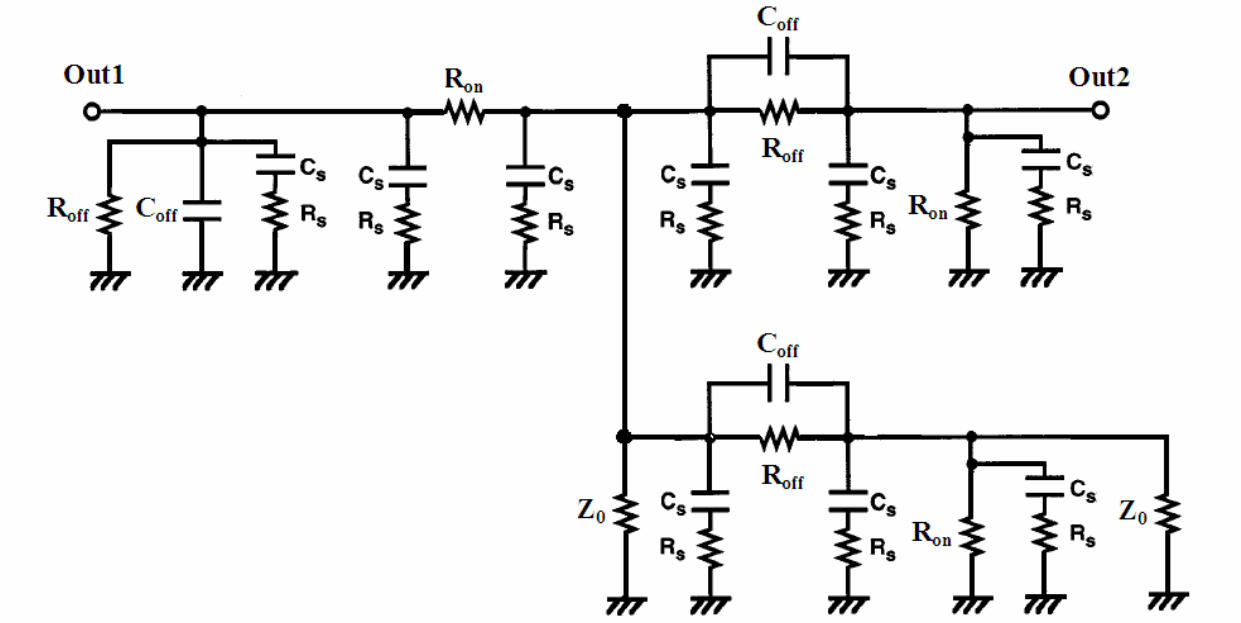


Fig. 12 Circuit schematics and their ON- and OFF-state equivalent circuits for series and shunt arms.

The equivalent circuits for calculating the insertion loss between antenna and output port, and isolation between two output ports are shown in Fig. 13.



(a)



(b)

Fig. 13 The equivalent circuits for calculating the insertion loss between antenna and output port, and isolation between two output ports.

From Fig. 13, IL is expressed by (3.1), where $Q = 1/(j\omega C_s)$ and $Z_0 = 50\Omega$.

$$IL = \left| 1 + \frac{R_{on}\left[(Q + R_s) R_{off} Z_0 + (Q + R_s)(R_{off} + Z_0) C_{off} + 2 R_{off} C_{off} Z_0 \right]}{(Q + R_s) R_{off} C_{off} Z_0} \right|^2 \qquad (3.1)$$

In the first order approximation, R_{on} and R_{off} are inversely proportional to the gate width, and C_{off}, C_s are proportional to the width, equation (3.1) can be written in the following form: $IL = f(W_{se}, W_{sh})$, where W_{se} and W_{sh} are the width of the series and shunt device respectively. The optimum W_{se} and W_{sh} can be found to provides the minimum insertion loss.

3.3 Design and Results

Since the ON resistance is in the same order of the load. i.e., 50 Ω, the insertion loss is very sensitive to its value. Then choosing the size of the series device is critical during design. On the contrary, the OFF impedance is high enough, the size of the shunt device is not so important. As can be seen from the following simulations.

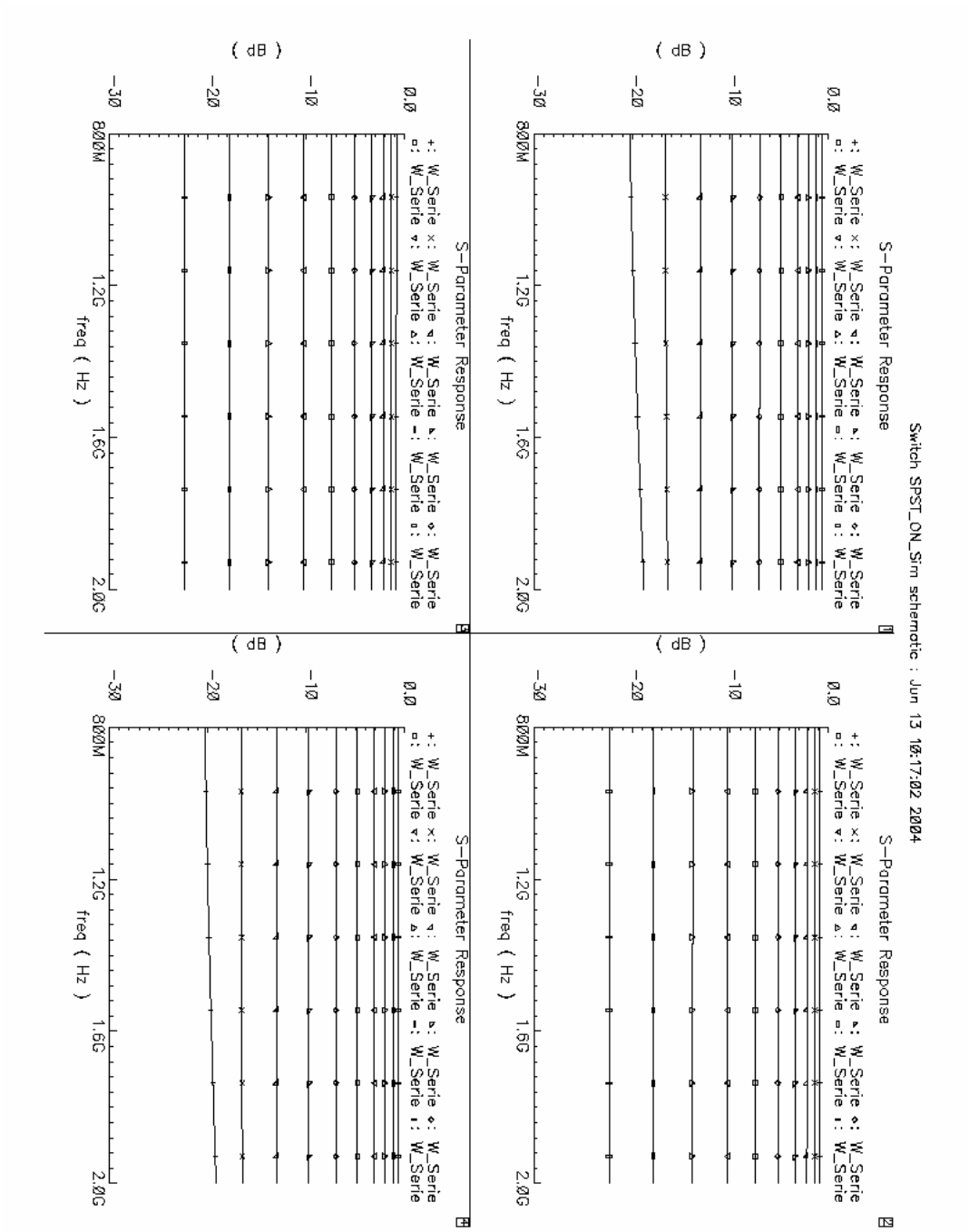


Fig. 14 The width of the series transistor has very strong impact on the switch characteristics.

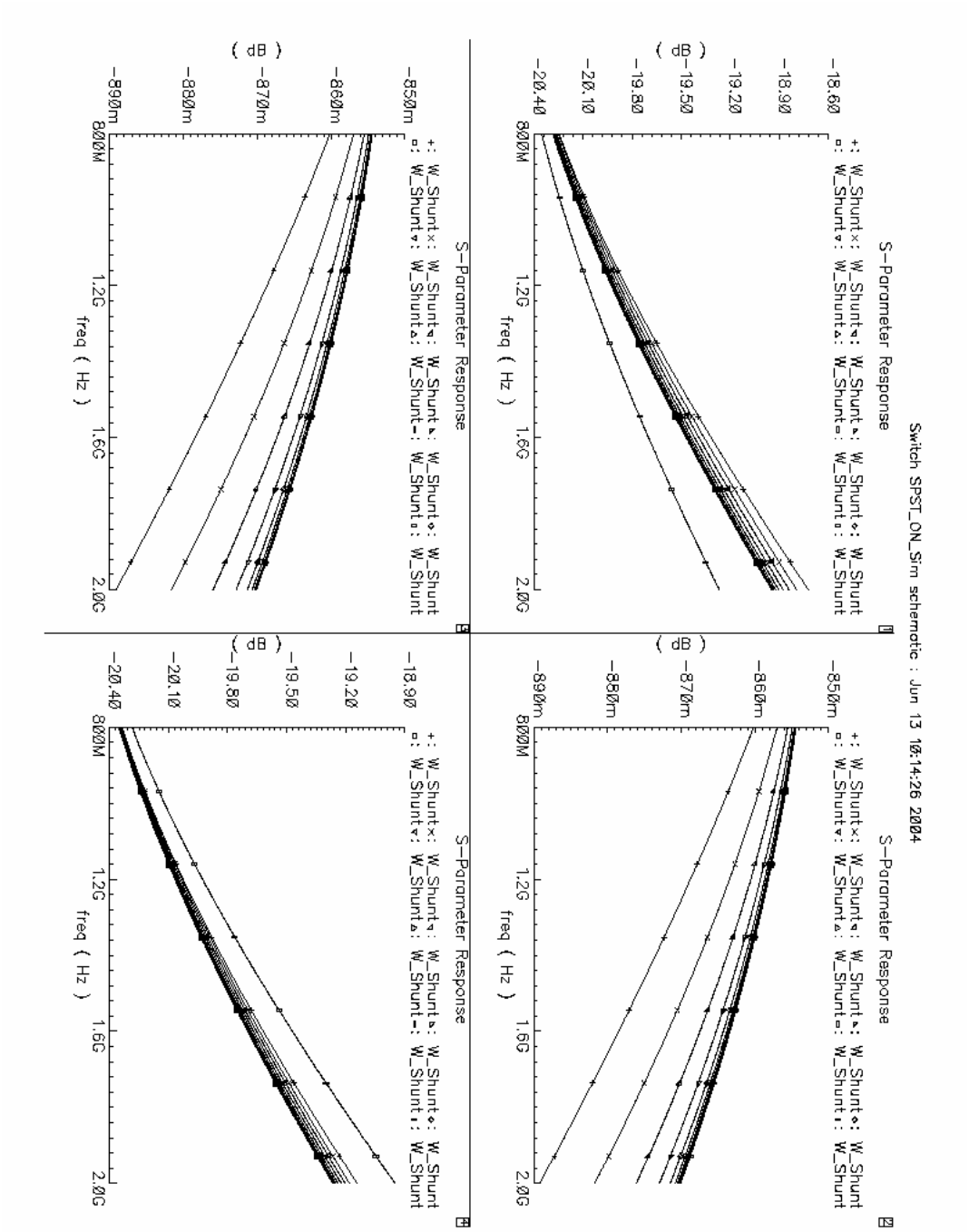


Fig. 15 The width of the shunt transistor has minor impact on the switch characteristics.

The final design result is shown as follows.

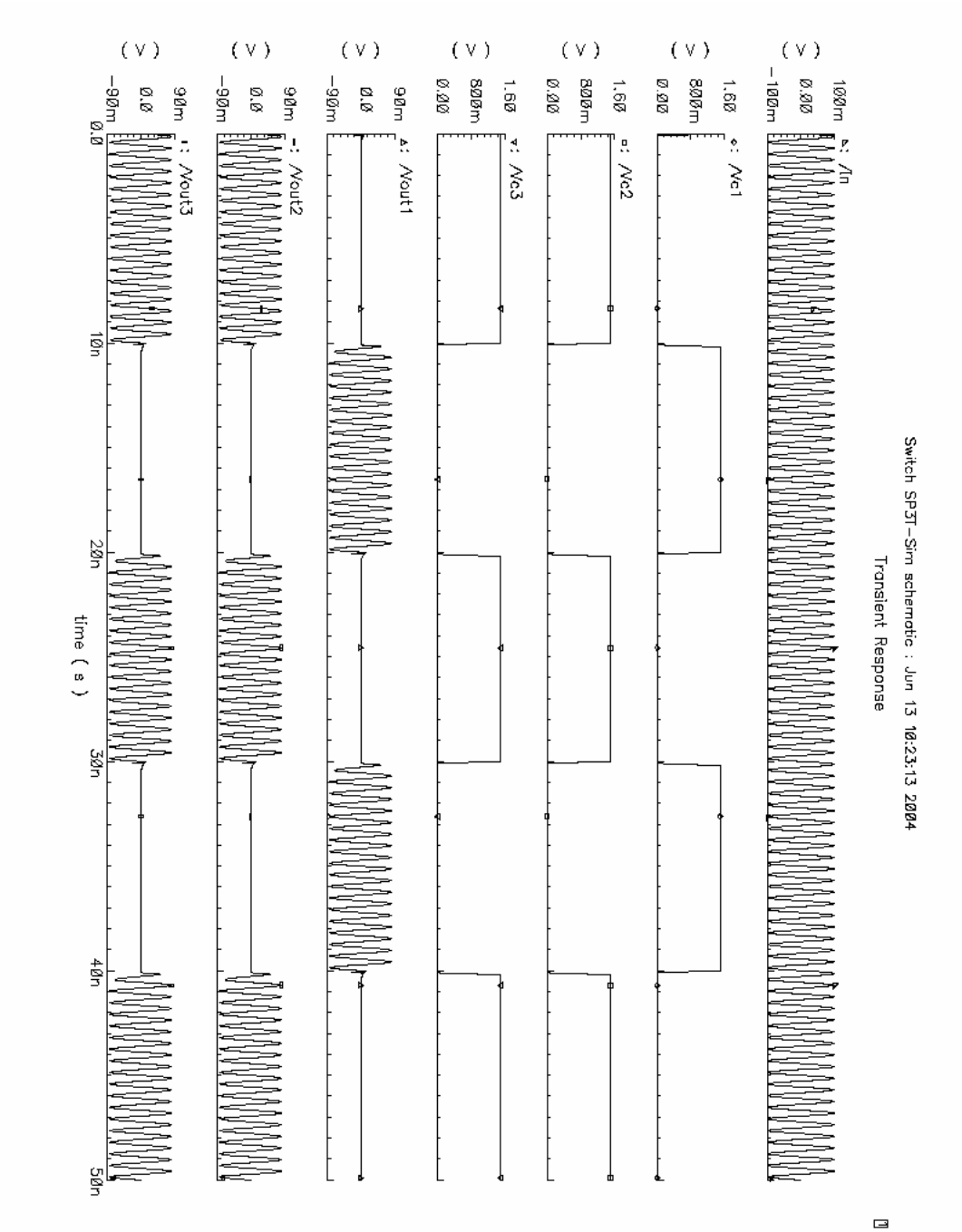


Fig. 16 Transient simulation of the switch.

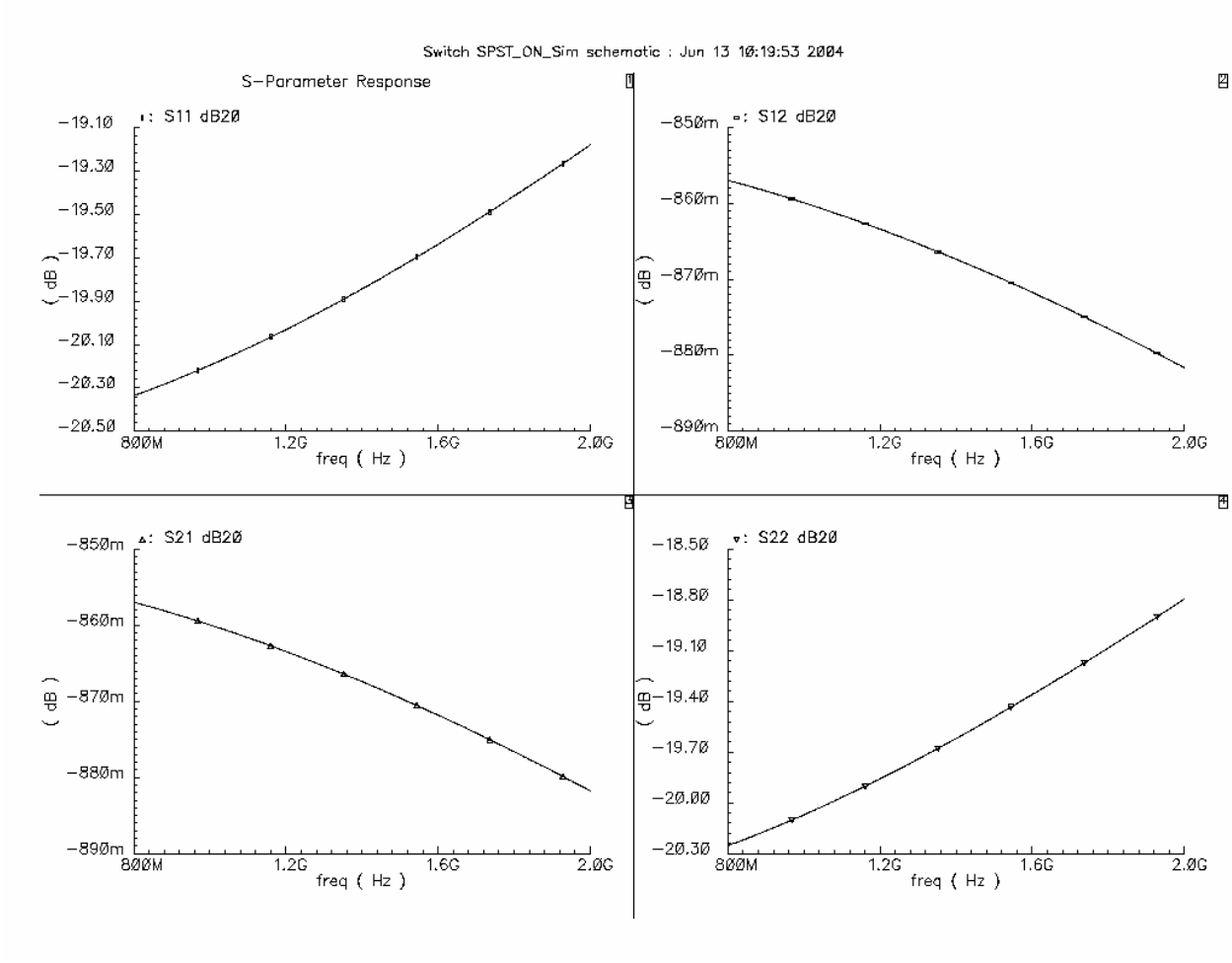


Fig. 17 S-parameters of the switch.

CHAPTER FOUR: LNA DESIGN

4.1 Review of LNA Design

CMOS integrated LNA design is under active research. The design concerns for a given architecture include bias points, device size, power, matching, etc. Since the primary role of the LNA is to lower the overall noise figure of the entire receiver, noise optimization is widely addressed [19]–[25]. Contemporary methods usually fix one design variable, and optimize with respect to the remaining variables, but fail to give guidelines on how to find the optimum value for that fixed variable. Or some variable values can only be obtained by extensive simulation. For example, in [19], noise factor is related to gate over-drive voltage and power dissipation (P_D), and optimized by fixing either G_m or P_D. In the first method, no optimum G_m value is given. In the second method, device width can only be obtained by iterative simulation.

When deciding device size for a cascade structure, some people omit the noise influence of the cascading transistor, which introduces 40% extra noise power or 0.5 dB noise figure [20], to

obtain the width of the input transistor. No good methods are given for calculating the width of cascode transistor, except multiple simulations.

Linearity is also under heated discussion. When analyzing nonlinearity, people have two different points of view. One is that the nonlinearity mainly results from the first stage [26]. People backing this opinion regard that the first amplifier stage as a tranconductor, while the second amplifier stage produces a unity current gain. The other point of view believes that the linearity is limited by the second MOSFET, due to the gain preceeding it, as can be seen from the equation $\frac{1}{IIP3^2} = \frac{1}{IIP3^2_1} + \frac{A^2_1}{IIP3_2{}^2}$, where $IIP3_1$ and $IIP3_2$ are the input-referred third-order intercept points of the first and second stage respectively. If the gain of the first stage A_1 is greater then unity, it can be seen that the second stage plays a more important role than the first stage in $IIP3$. Therefore, in the cascode architecture, M2 contributes more to the linearity of the circuit, and should be designed for linearity optimization.

To resolve this argument and gain insight on this issue, we recur to Volterra-series approach [27], since Volterra series is the best approach for identifying the linearity limiting factors of a given transtor technology for weakly nonlinear applications including LNAs [28].

Based on the aforementioned observation, an optimization method, with respect to noise, gain and linearity, without any prefixed value or iterative simulation, is proposed. The following

section provides the overall optimization method. Section III do the noise analysis, Section IV and V discuss the gain and IIP3. Model selection for analysis is briefly discussed in Section VI. A design example is illustrated in Section VII, with the results compared to some reports in the literature. Section VIII concludes this paper.

The proposed method aims at a popular cascode structure with source inductively degenerated, shown in Fig. 18. Inductive source degeneration offers the possibility of achieving the best noise performance. Cascode structure can reduce the interaction of the tuned output with the tuned input, and reduce the effect of M1's gate-drain capacitance.

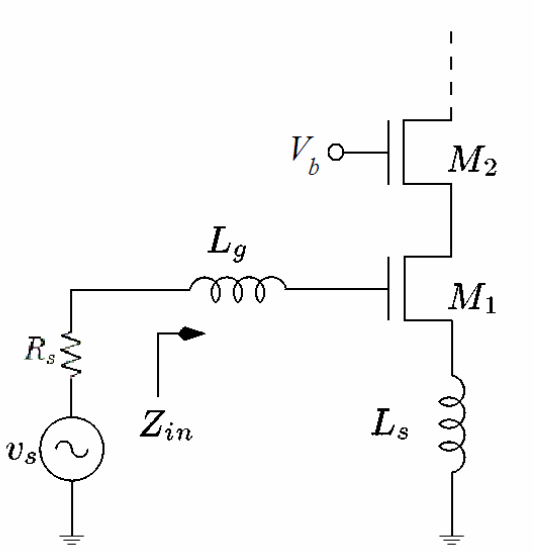


Fig. 18 LNA architecture.

Table 2 summaries a number of symbols used in the paper.

Table 2 Process and Design Parameters

Symbol	Parameter
W1, W2	Width of M1, M2
L	Transistor length
I_D	DC current flowing through M1 and M2
V_{GS}	DC gate-source voltage
V_{DS}	DC drain-source voltage
V_{BS}	DC bulk-source voltage
V_{G1}	DC gate voltage of M1
V_{D1}	DC drain voltage of M1
Z_{in}	Input impedance
g_m	Transconductance
C_{gs}	Gate-source capacitance
ω_T	Cut-off frequency
μ	Electron mobility
R_s	Source resistance
V_{TH}	Threshold voltage
V_{od}	$V_{GS} - V_{TH}$, over-drive voltage
g_{d0}	Output conductance at $V_{DS} = 0$
ω	Angular frequency of operation
R_l	Series resistance of the inductor L_g
R_g	Gate resistance
i_g	Gate noise current
i_d	Drain noise current
i_{out}	Output noise current
k	Boltzmann's constant
T	Absolute temperature

The aforementioned optimization method is used on TSMC 0.35 μm LOGIC, 3.3V/5V Silicide process. V_{DD} is set at 3.3V, and channel length 0.35 μm. The design specifications are 1.8 GHz, 8 mW.

4.2 Overall Method

By careful analysis, it is found that under power constraint condition, i.e., I_D is fixed, W_1 and W_2 are the only decisive elements for designing a LNA.

Generally, I_D is a function of V_{GS}, V_{DS}, V_{BS} and transistor width W, as in the form of $I_D = I_D\left(V_{GS}, V_{DS}, V_{BS}, W\right)$. For M1, it is obvious that

$$I_D = I_D\left(V_{G1}, V_{D1}, W_1\right); \tag{4.1}$$

for M2,

$$I_D = I_D\left(V_{GS2}, V_{DS2}, V_{BS2}, W_2\right) = I_D\left(V_b - V_{D1}, V_{DD} - V_{D1}, -V_{D1}, W_2\right) = I_D\left(V_{D1}, W_2\right). \tag{4.2}$$

Here, V_b is set to V_{DD} for better linearity, which will be explained in Section V. Once W_1 and W_2 are chosen, V_{G1}, V_{D1} can be solved from (1) and (2), and bias points are determined. There will be no need of lots of simulations for varies of bias points in order to find an optimum bias point as in [19], [20], [24]. Once bias points are decided, all the transistor small-signal parameters can be calculated, and other component values can be calculated.

So noise figure, gain and linearity can be related to only W_1 and W_2. The design problem is actually an optimization problem, i.e.

$$\text{minimize } NF(W_1, W_2),$$

$$\text{subject to } Z_{in} = 50\Omega,$$

$$\text{gain} \geq \text{minimum gain requirement},$$

$$\text{IIP3} \geq \text{minimum IIP3 requirement}.$$

4.3 Model Selection

The SPICE LEVEL 1 MOSFET model is convenient in analytical treatments of MOSFET circuits, but not accurate in the shot-channel region. The more precise and popular BSIM model, however, is too complicated to be practical for circuit analysis. A simple, yet accurate model is need for analytical treatment of the circuit. Several compact models are among the choices, including alpha-power law [29], [30], *n*th-power law [31], transregional model [32], alpha-power

law and transregional model coupled model [33]. References [32], [33] are still not convenient for back on envelope derivation. Output impedance cannot be obtained in [29], [30] because their drain currents are not related to V_{ds} explicitly. So [31] is chosen.

The drain current in the saturation region is $I_d = I_{DSAT}(1+\lambda V_{ds})$, where

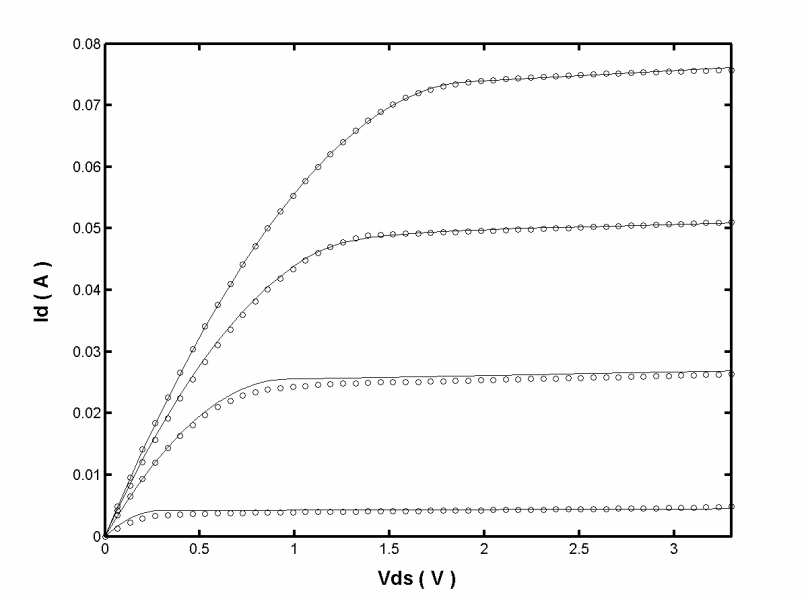
$I_{DSAT} = \frac{W}{L_{eff}} B\left(V_{gs} - V_{TH}\right)^n$, $V_{TH} = V_{T0} + \gamma\left(\sqrt{2\phi_F - V_{bs}} - \sqrt{2\phi_F}\right)$, $\lambda = \lambda_0 - \lambda V_{bs}$. Then g_m, g_{mb} and output resistance r_o can be expressed as the followings and will be used in later calculations.

$$g_m = n\frac{W}{L_{eff}} B\left(V_{gs} - V_{TH}\right)^{n-1}\left(1+\lambda V_{ds}\right),$$

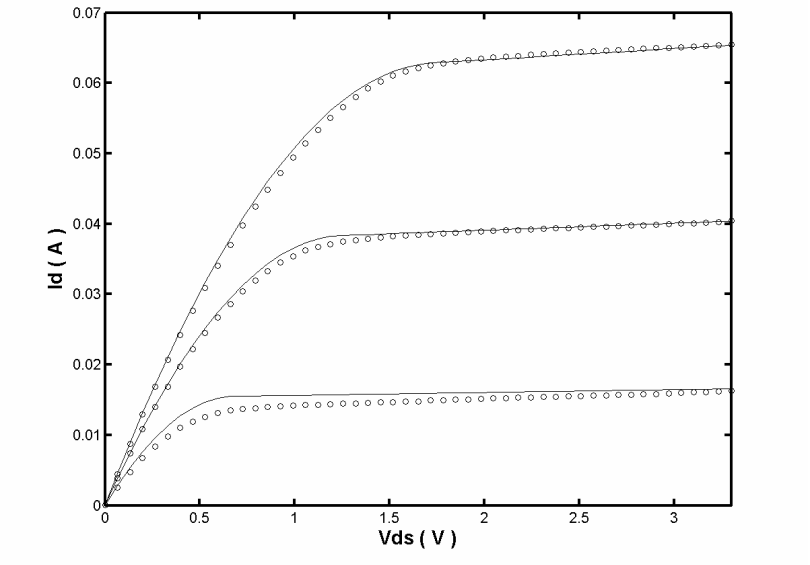
$$g_{mb} = \frac{\gamma}{2\sqrt{2\phi_F - V_{bs}}} g_m,$$

$$r_o = \frac{1}{\lambda \frac{W}{L_{eff}} B\left(V_{gs} - V_{TH}\right)^n}.$$

The *n*th-power law model parameters are first extracted. Fig. 19 shows good agreement between the BSIM3V3.02 model available and the *n*th-power law model.



(a)



(b)

Fig. 19 I_d - V_{ds} characteristics of BSIM3V3.02 model and *n*th-power law model. L = 0.35 μm, W = 150 μm. (a) V_b = 0 V (b) V_b = -2 V (circle: BSIM, line: *n*th-power law).

4.4 Noise Analysis

The small signal model for noise calculation is shown in Fig. 20. C_{gd} is neglected for simplicity. Anyhow, it can only bring 0.1 dB noise figure improvement when considered [34]. Instead, the channel resistance r_i [35], which is omitted in most of the analysis in literature, is included, because it brings shift to input impedance, working frequency, and noise figure [36]. g_{mb} is also included since it is found that g_{mb} can be as high as one third of g_m. It is also assumed that operating frequency is well below the transit frequency of the transistors.

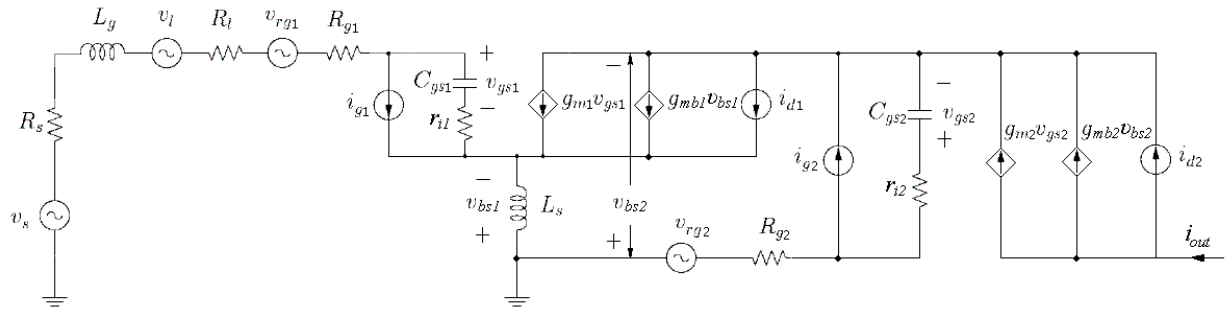


Fig. 20 Small signal model for noise calculation.

Five noise sources are considered: R_s, R_l, R_g, i_g, and i_d, where $R_g = \frac{R_{g\square}W}{3L}$, $R_{g\square}$ is the sheet resistance of the gate material, and $\overline{i^2_{gj}} = 4kT\delta g_{gj}$, $g_{gj} = \frac{\omega^2 C^2_{gsj}}{5g_{d0j}}$, $\delta = 4/3$, $\overline{i^2_{dj}} = 4kT\gamma g_{d0j}$, $j = 1$, 2, and i_d, i_g are correlated with the relation of $c = \frac{\overline{i_g \cdot i^*_d}}{\sqrt{\overline{i^2_g}}\sqrt{\overline{i^2_d}}}$, $c = 0.395i$; $\overline{v^2_s} = 4kTR_s$, $\overline{v^2_l} = 4kTR_l$, $\overline{v^2_{rg1}} = 4kTR_{g1}$, $\overline{v^2_{rg2}} = 4kTR_{g2}$ [37].

The input impedance of the circuit is given by $Z_{in} = R_g + R_l + \omega_{T1}L_s + j\omega\left(L_s + L_g\right) + \frac{1}{j\omega C_{gs1}}$, where $R_{g1} \propto W_1$ depending on layout [38]; $R_l = \frac{\omega L_g}{Q}$, Q is the quality factor of L_g, a parameter closely related to process. At the resonance,

$$\omega = \frac{1}{\sqrt{\left(L_s + L_g\right)C_{gs1}}}, \tag{4.3}$$

and impedance matching requires

$$R_s = Z_{in} = 50\Omega. \tag{4.4}$$

Note that $\omega_{T1} = \frac{g_{m1}(V_{G1}, V_{D1}, W_1)}{C_{gs1}(V_{G1}, V_{D1}, W_1)} = \frac{g_{m1}(W_1)}{C_{gs1}(W_1)}$, ω_{T1} is a sole function of W_1 and W_2. From (3) and (4), it is obvious that L_s, and L_g are functions of W_1 only. In other words, once W_1 is chosen, L_s and L_g can be calculated from (3) and (4).

The noise contributions of each noise component, R_s, R_l, R_{g1}, i_{g1}, i_{d1}, R_{g2}, i_{g2} and i_{d2}, are derived as

$$i_{out,R_s} = \frac{i_{n,R_s} g_{m1} g_{m2}}{2j\omega C_{gs1}\left(g_{m2} + j\omega C_{gs2}\right)} \tag{4.5}$$

$$i_{out,R_l} = \frac{\upsilon_l g_{m1} g_{m2}}{2j\omega R_s C_{gs1}\left(g_{m2} + j\omega C_{gs2}\right)} \tag{4.6}$$

$$i_{out,R_{g1}} = \frac{\upsilon_{rg1} g_{m1} g_{m2}}{2j\omega R_s C_{gs1}\left(g_{m2} + j\omega C_{gs2}\right)} \tag{4.7}$$

$$i_{out,i_{g1}} = \frac{-i_{g1} g_{m1} g_{m2}\left(R_s + R_l + R_{g1} + j\omega L_g + j\omega L_s\right)}{2j\omega R_s C_{gs1}\left(g_{m2} + j\omega C_{gs2}\right)} \tag{4.8}$$

$$i_{out,i_{d1}} = \frac{i_{d1} g_{m2}\left(2R_s - \omega_{T1} L_s\right)}{2R_s\left(g_{m2} + j\omega C_{gs2}\right)} \tag{4.9}$$

$$i_{out,R_{g2}} = 0 \tag{4.10}$$

$$i_{out,i_{g2}} = \frac{-i_{g2} g_{m2}}{g_{m2} + j\omega C_{gs2}} \tag{4.11}$$

$$i_{out,i_{d2}} = \frac{i_{d2} j\omega C_{gs2}}{g_{m2} + j\omega C_{gs2}} \tag{4.12}$$

Because i_{g1} and i_{d1} are correlated, their contribution to the power of output noise current should be calculated together as follows:

$$i_{out,i_{g1}+i_{d1}} = i_{out,i_{g1}} + i_{out,i_{d1}} \tag{4.13}$$

$$\overline{i^2_{out,i_{g1}+i_{d1}}} = i_{out,i_{g1}+i_{d1}} \cdot i^*_{out,i_{g1}+i_{d1}} \tag{4.14}$$

$$\overline{i^2_{out,i_{g1}+i_{d1}}} = \overline{i^2_{out,i_{g1}}} + \overline{i^2_{out,i_{d1}}} - \frac{\sqrt{\overline{i^2_{g1}}}\sqrt{\overline{i^2_{d1}}}\,|c|\, g_{m1} g^2_{m2}\left(R_s + R_l + R_{g1}\right)\left(2R_s - \omega_{T1} L_s\right)}{2\omega R^2_s C_{gs1}\left(g^2_{m2} + \omega^2 C^2_{gs2}\right)} \tag{4.15}$$

where the last term in (15) represents the output noise power due to the correlation. Treating i_{g2} and i_{d2} the same way yields

$$\overline{i^2_{out,i_{g2}+i_{d2}}} = \overline{i^2_{out,i_{g2}}} + \overline{i^2_{out,i_{d2}}} - \frac{2\sqrt{\overline{i^2_{g2}}}\sqrt{\overline{i^2_{d2}}}\,|c|\, g_{m2}\omega C_{gs2}}{g^2_{m2} + \omega^2 C^2_{gs2}} \tag{4.16}$$

The total power of the output noise current is then

$\overline{i^2_{out}} = \overline{i^2_{out,R_s}} + \overline{i^2_{out,R_l}} + \overline{i^2_{out,R_{g1}}} + \overline{i^2_{out,R_{g2}}} + \overline{i^2_{out,i_{g1}+i_{d1}}} + \overline{i^2_{out,i_{g2}+i_{d2}}}$. And the noise factor F is $\frac{\overline{i^2_{out}}}{\overline{i^2_{out,R_s}}}$.

From (5), (6), (7), (10), (15) and (16),

$$F = 1 + \frac{\left(\overline{\upsilon^2_l} + \overline{\upsilon^2_{rg1}}\right) g^2_{m1} g^2_{m2} + \overline{i^2_{g1}} g^2_{m1} g^2_{m2} \left[\left(R_s + R_l + R_{g1}\right)^2 + \omega^2 \left(L_g + L_s\right)^2\right]}{\overline{i^2_{n,R_s}} g^2_{m1} g^2_{m2} R^2_s}$$
$$+ \frac{\overline{i^2_{d1}} g^2_{m2} \omega^2 C^2_{gs1} \left(2R_s - \omega_{T1} L_s\right)^2 - 2\sqrt{\overline{i^2_{g1}}}\sqrt{\overline{i^2_{d1}}} \left|c\right| g_{m1} g^2_{m2} \omega C_{gs1} \left(R_s + R_l + R_{g1}\right)\left(2R_s - \omega_{T1} L_s\right)}{\overline{i^2_{n,R_s}} g^2_{m1} g^2_{m2} R^2_s}$$
$$+ \frac{4\overline{i^2_{g2}} g^2_{m2} \omega^2 R^2_s C^2_{gs1} + 4\overline{i^2_{d2}} \omega^4 R^2_s C^2_{gs1} C^2_{gs2} - 8\sqrt{\overline{i^2_{g2}}}\sqrt{\overline{i^2_{d2}}} \left|c\right| g_{m2} \omega^3 R^2_s C^2_{gs1} C_{gs2}}{\overline{i^2_{n,R_s}} g^2_{m1} g^2_{m2} R^2_s} \quad (4.17)$$

4.5 Gain Analysis

Assuming M2 produces a unity current gain, the output impedance of the LNA Z_{out} is approximately $\left[1 + \left(g_{m2} + g_{mb2}\right) r_{o2}\right] Z_{out1} + r_{o2}$, where Z_{out1} is the output impedance of M1, using the circuit in Fig. 21 [39].

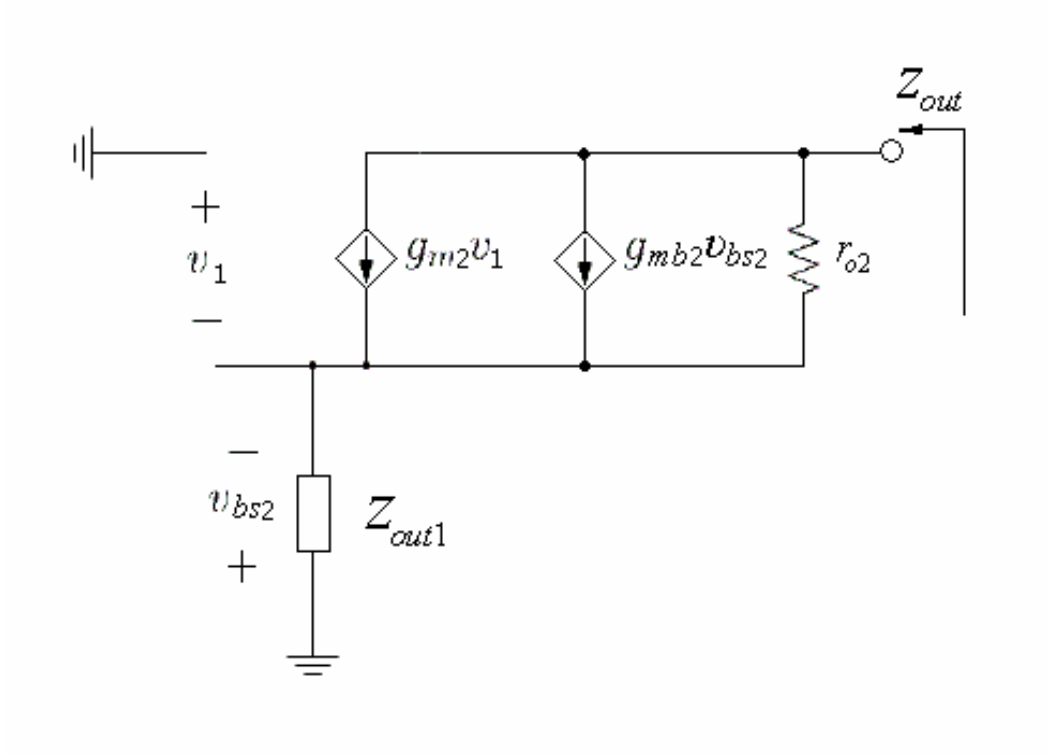


Fig. 21 Small signal equivalent circuit for calculating Z_{out}.

Z_{out1} is obtained using the circuit in Fig. 22 as

$$r_{o1}+\frac{\omega^2 L^2{}_s+\omega_{T1}r_{o1}L_s+g_{mb1}\omega^2 r_{o1}L^2{}_s}{R_s+R_l+R_g+r_{i1}}+\left(1+g_{mb1}r_{o1}\right)j\omega L_s\,.$$

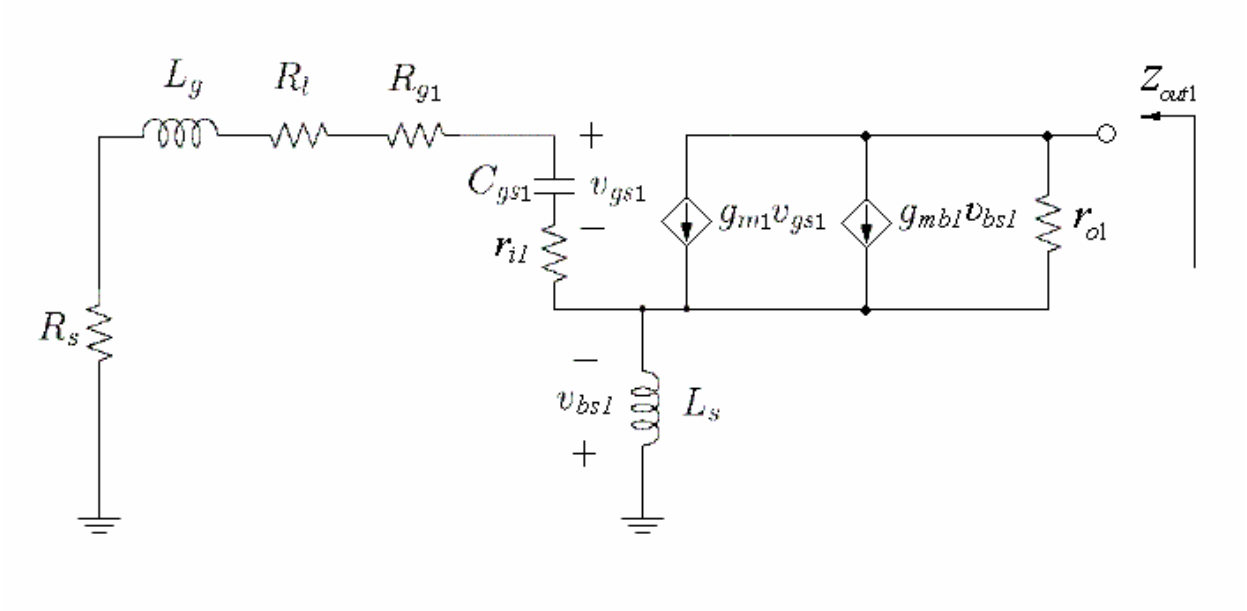


Fig. 22 Small signal equivalent circuit for calculating Z_{out1}.

Hence, Z_{out} can be written as $Z_{out} = R_{out} + jX_{out}$, where

$$R_{out} = \left[1+\left(g_{m2}+g_{mb2}\right)r_{o2}\right]\left(r_{o1}+\frac{\omega^2 L_s^2+\omega_{T1}r_{o1}L_s+g_{mb1}\omega^2 r_{o1}L_s^2}{R_s+R_l+R_{g1}+r_{i1}}\right)+r_{o2},$$

and $$X_{out} = \left[1+\left(g_{m2}+g_{mb2}\right)r_{o2}\right]\left(1+g_{mb1}r_{o1}\right)\omega L_s .$$

Matching Z_{out} to a 50 Ω load R_L using a high pass L network gives L_d and C_d:

$$L_d = \frac{R_p}{\omega\left(Q-Q_s\right)},$$

$$C_d = \frac{1}{\omega Q R_L},$$

where $Q_s = X_{out}/R_{out}$, $R_p = \left(Q_s^2 + 1\right) R_{out}$, $Q = \sqrt{R_p/R_L - 1}$.

Gain and IIP3 can also be related to W_1 and W_2. The transducer gain is

$$G_T = \frac{\left(\frac{i_{out1} Z^*_{out2}}{R_L + \frac{1}{j\omega C_d}} \right)^2 R_L}{\left(\frac{v_s}{2R_s} \right)^2 R_s},$$

where $i_{out1} = \frac{g_m r_{o1} v_x}{\left[1 + \left(g_{m1} + g_{mb1}\right) j\omega L_s\right] r_{o1} + j\omega L_s}$ is the incremental current flowing into the drain of M1, and $v_x = v_s - \frac{v_s}{2R_s}\left(j\omega L_g + R_l + R_g\right)$.

4.6 IIP3 Analysis

The large-signal equivalent circuit for the two transistors together with the source degeneration inductor is shown in Fig. 23.

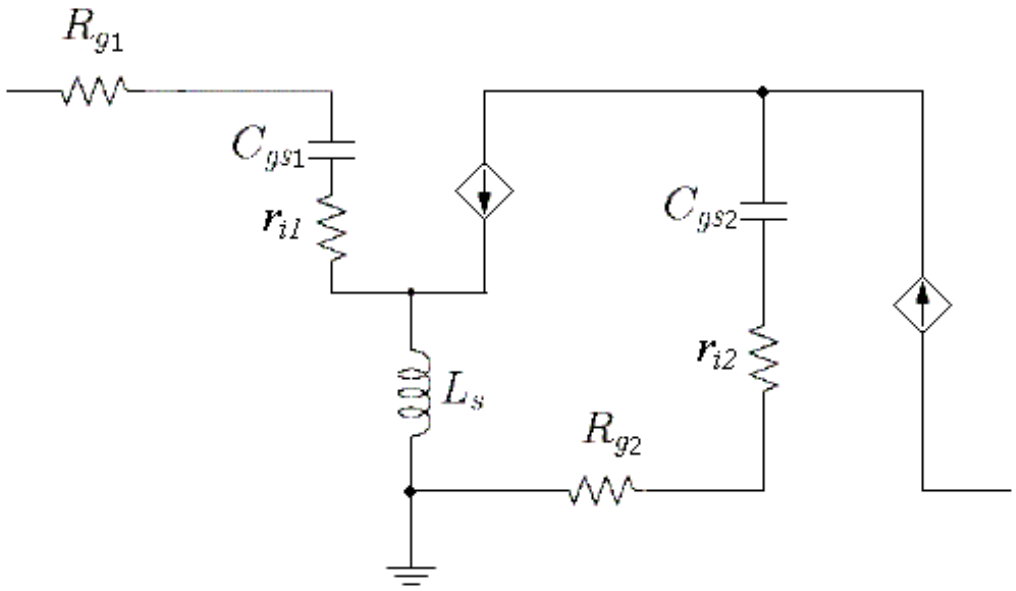


Fig. 23 Equivalent large-signal circuit for Volterra-series calculation.

It was first linearized at the operating bias. The resulting linear circuit was then solved using compacted modified nodal analysis (CMNA) [40], [41]

$$Y(s)\cdot\overrightarrow{H_1}(s)=\overrightarrow{I_1} \tag{4.18}$$

where $Y(s)$ is the CMNA admittance matrix at frequency $s(j\omega)$, $\overrightarrow{H_1}(s)$ is the vector of first-order Volterra kernel transforms of the node voltages, and $\vec{I}$ is the vector of the node excitations. The admittance matrix Y and the excitation vector I were obtained by applying the Kirchoff's current law at every circuit node. The unknowns are the node voltages. The unknown currents associated with zero impedance elements, such as voltage sources, were eliminated in advance. The circuit output and the voltages that control nonlinearities can be expressed as a linear combination of the elements of $\overrightarrow{H_1}(s)$. With $\overrightarrow{H_1}(s)$ solved, the same circuit was excited by the second-order nonlinear current sources $\overrightarrow{I_2}$, which were determined by the first-order voltages that control individual nonlinearities, and the second-order derivatives of all the $I-V$ nonlinearities. Every nonlinearity in the original circuit corresponds to a nonlinear current source in parallel with the corresponding linearized circuit element. The orientation of these current sources is the same as the orientation of the controlled current in the original nonlinear circuit. The node voltages under such an excitation are the second-order Volterra kernels $\overrightarrow{H_2}(s_1, s_2)$

$$Y(s_1+s_2)\cdot\overrightarrow{H_2}(s_1,s_2)=\overrightarrow{I_2}$$

where $Y(s_1+s_2)$ is the same CMNA admittance matrix used in (18), but evaluated at the frequency s_1+s_2.

In a similar manner, the third-order Volterra kernels $\overrightarrow{H_3}$ were solved as response to excitations specified in terms of the previously determined first- and second-order kernels

$$Y\left(s_1+s_2+s_3\right)\cdot\overrightarrow{H_3}\left(s_1+s_2+s_3\right)=\overrightarrow{I_3} \tag{4.19}$$

P_{out} versus P_{in}, the third-order input intercept (IIP_3) at which the first- and third-order signals have equal power, and the (power) gain can then be obtained from $\overrightarrow{H_3}$ and $\overrightarrow{H_1}$.

In the presence of a multi-tone input, the node voltages at each mixed frequency for each node can be expressed using the solved Volterra kernels. For a two-tone input $A\left(\cos\omega_1 t+\cos\omega_2 t\right)$, IIP_3 is obtained as [28], [41]

$$IIP_3=\frac{1}{6R_s}\cdot\frac{\left|H_3\left(j\omega_1,j\omega_1,-j\omega_2\right)\right|}{\left|H_1\left(j\omega_1\right)\right|},$$

where R_s is the source resistance.

Unfortunately, the IIP_3 expression is too complex to show and to provide any design insight. However, it is useful for prediction and optimization through mathematic software such as MATLAB.

4.7 Results and Discussion

Fig. 24–26 show the dependence of noise figure, gain and IIP3 on W_1 and W_2.

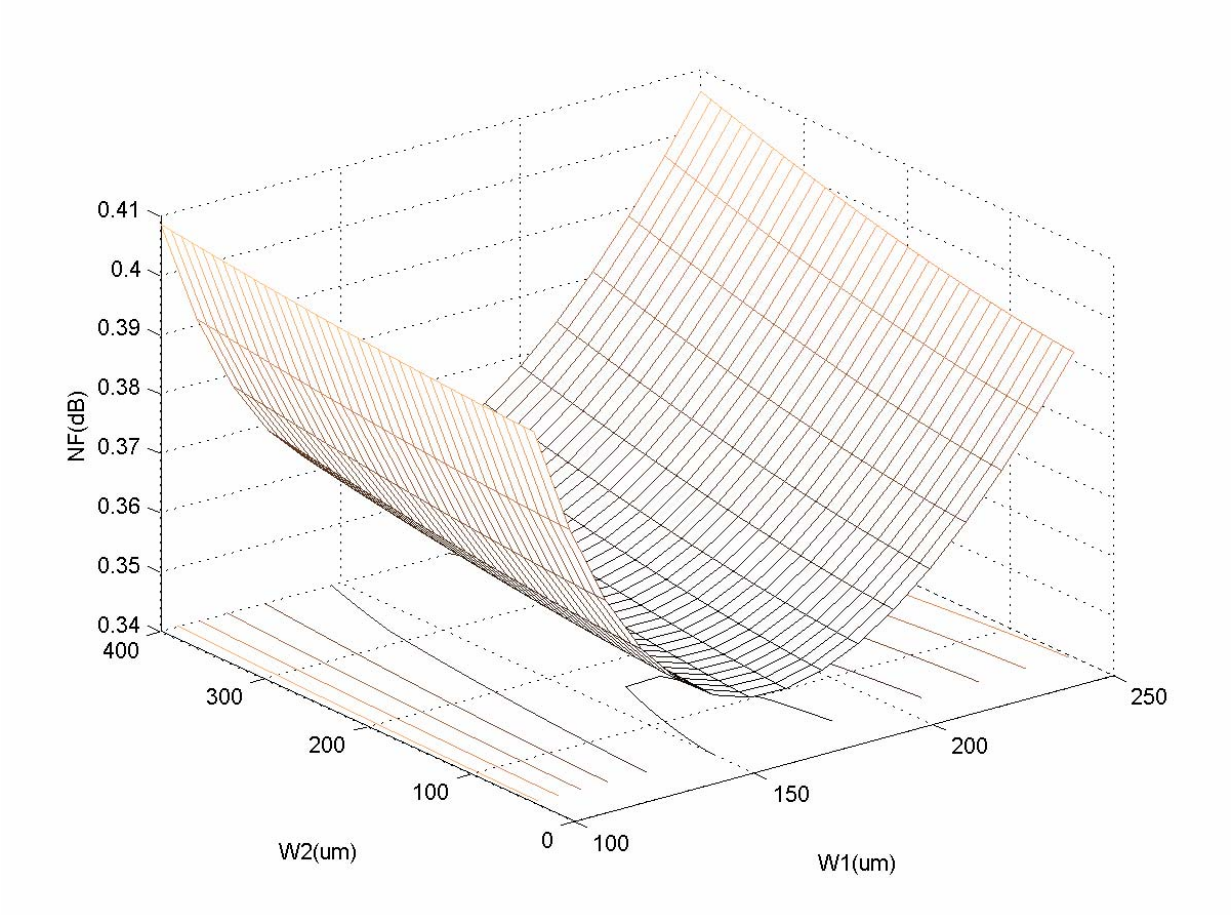


Fig. 24 Noise figure with respect to W_1 and W_2.

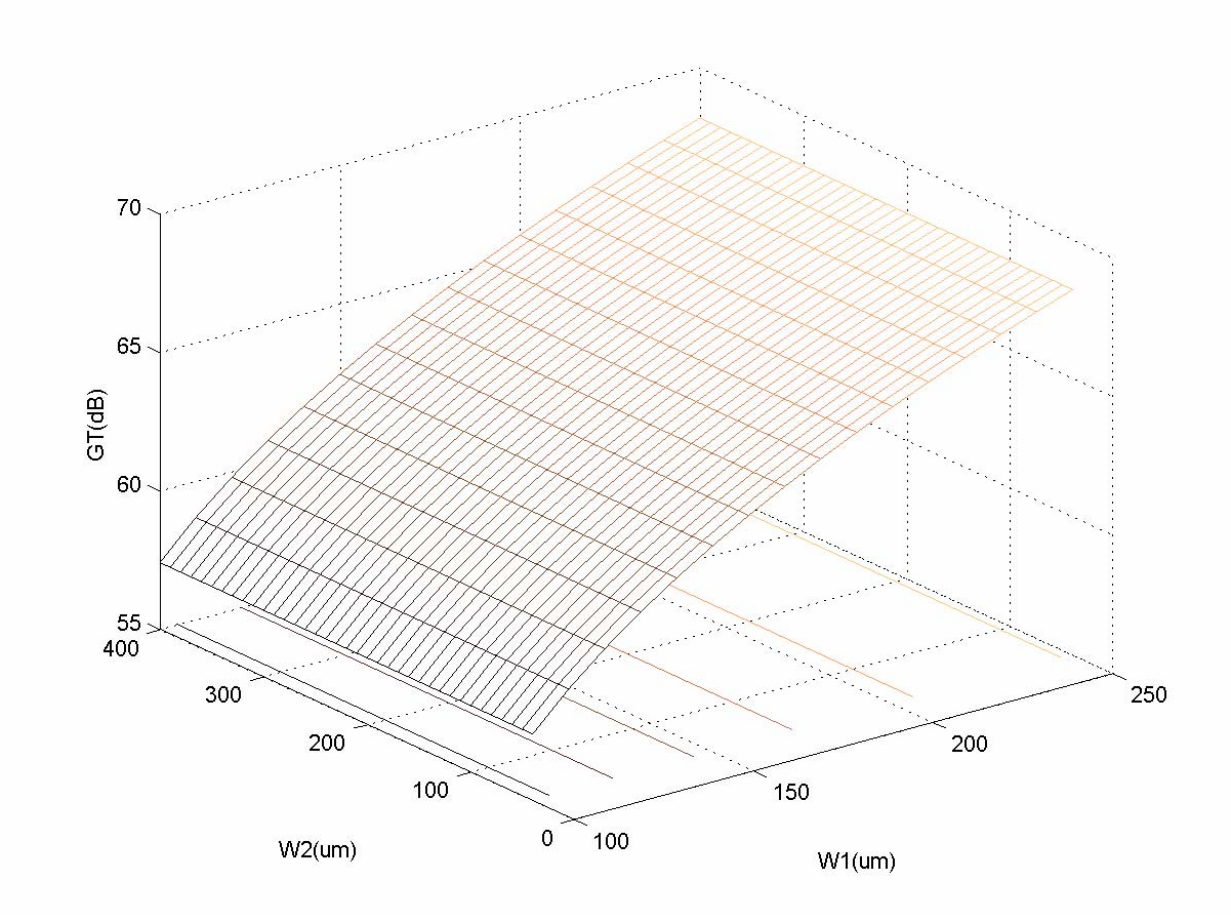


Fig. 25 Gain with respect to W_1 and W_2.

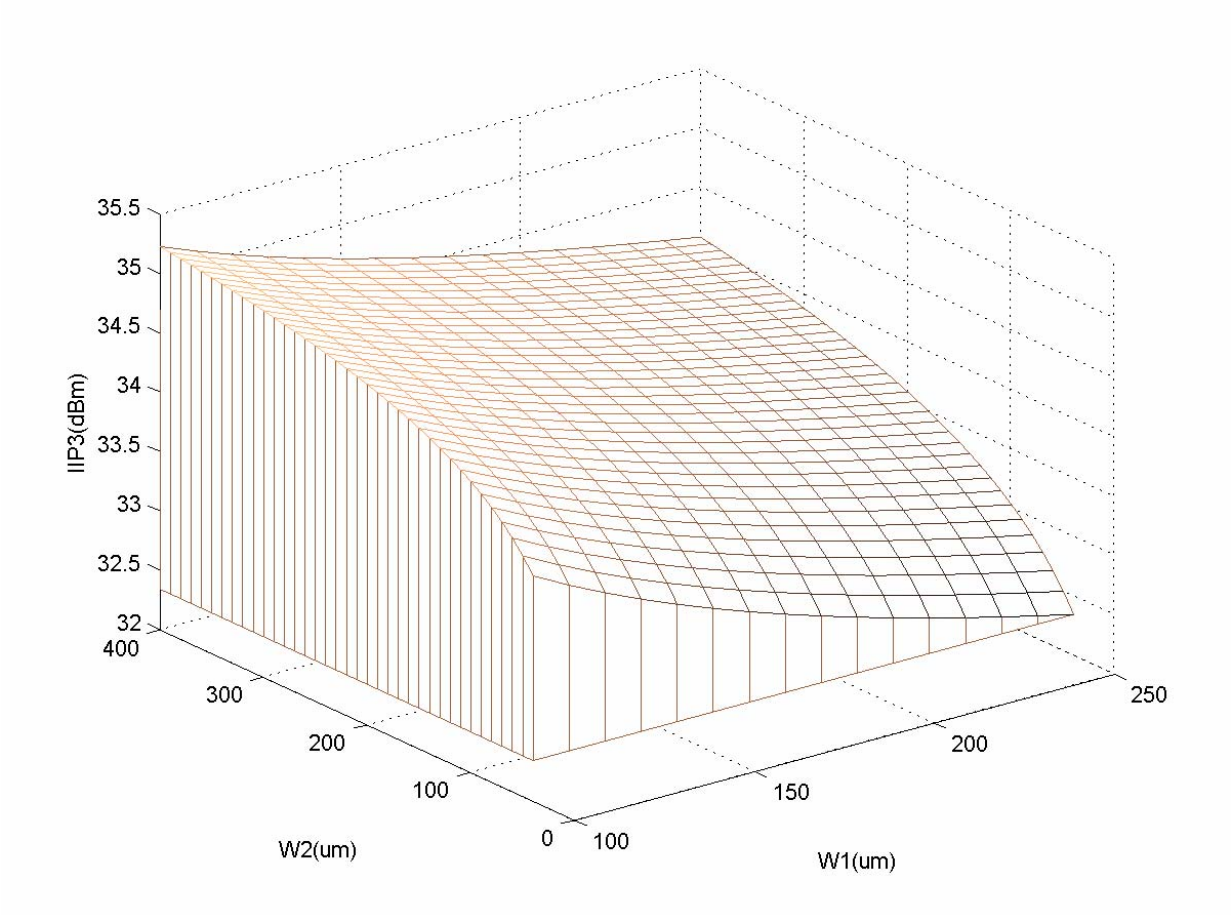


Fig. 26 IIP3 with respect to W_1 and W_2.

From the above three figures, it can be concluded that M1 contributes mainly to the noise and gain, while M2 to linearity.

To get an optimized device width for each transistor, it is straightforward to look at the contour graph of the noise figure, gain and IIP3, shown in Fig. 27. For the sake of easy implementation, both W_1 and W_2 are chosen as 146 μm.

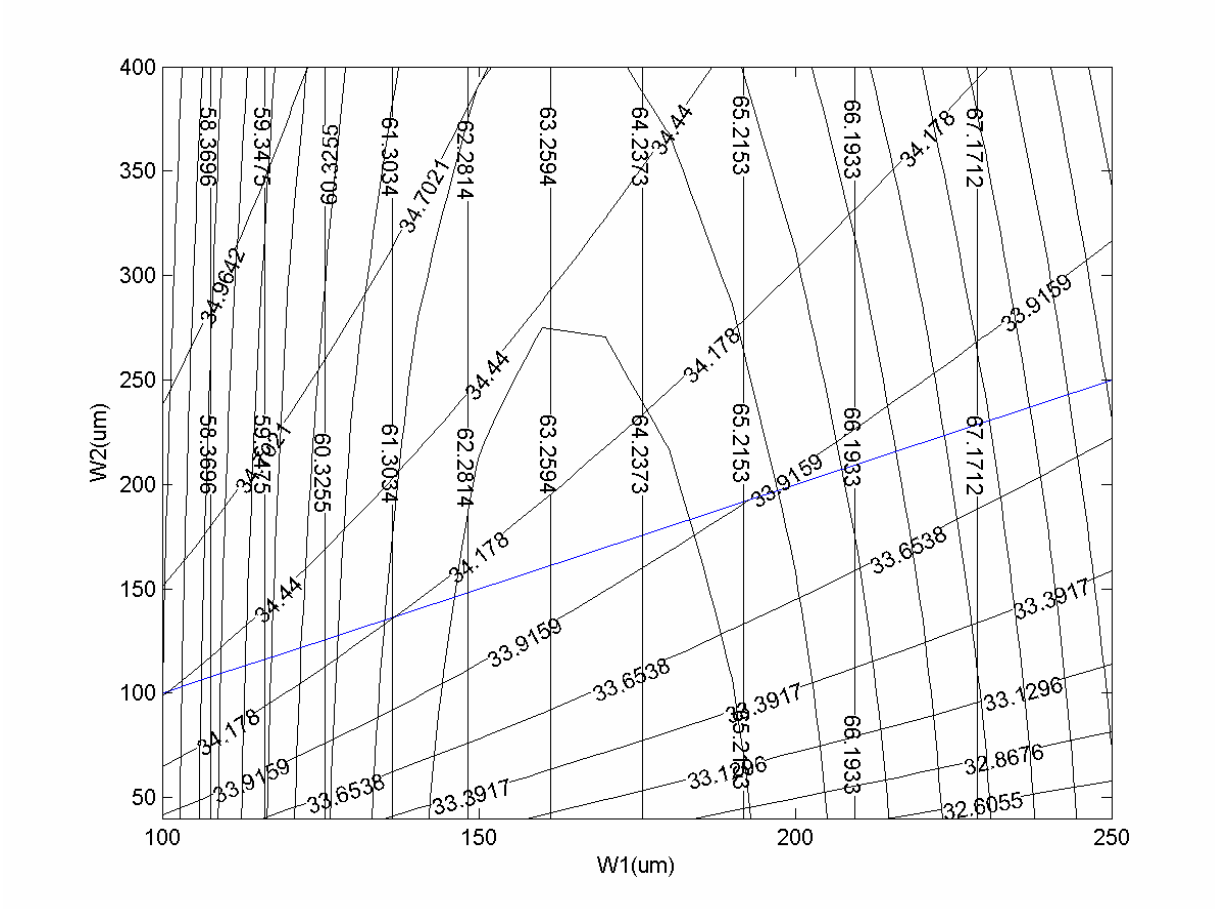
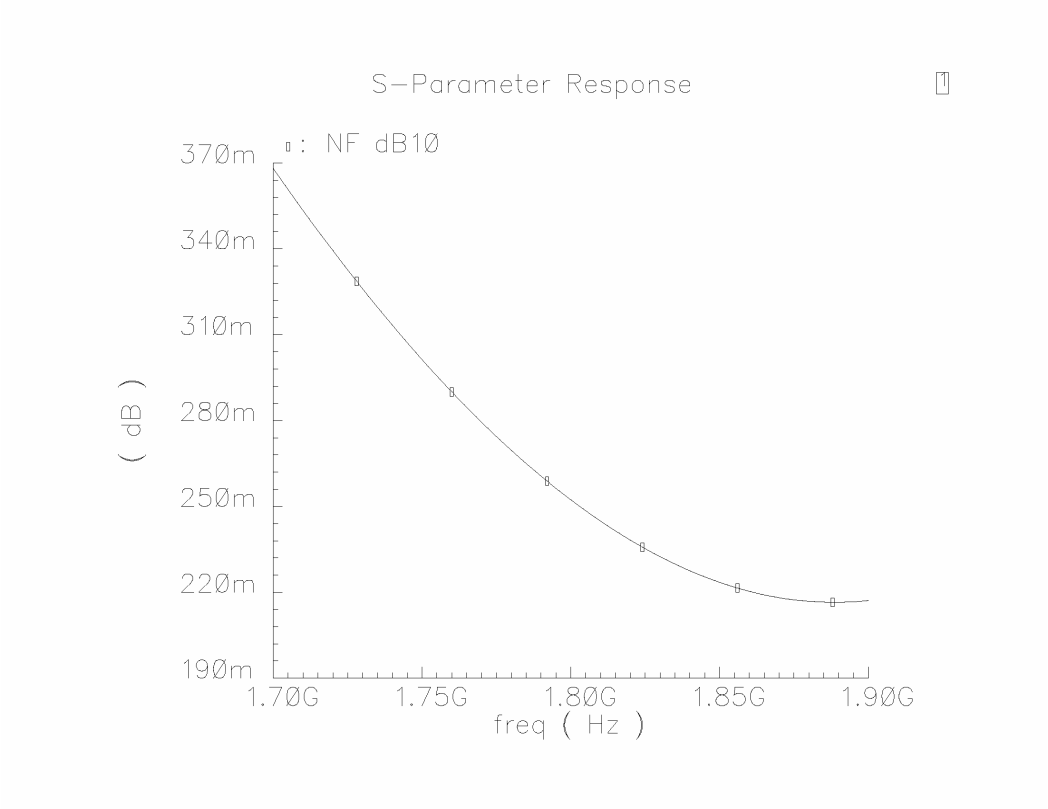


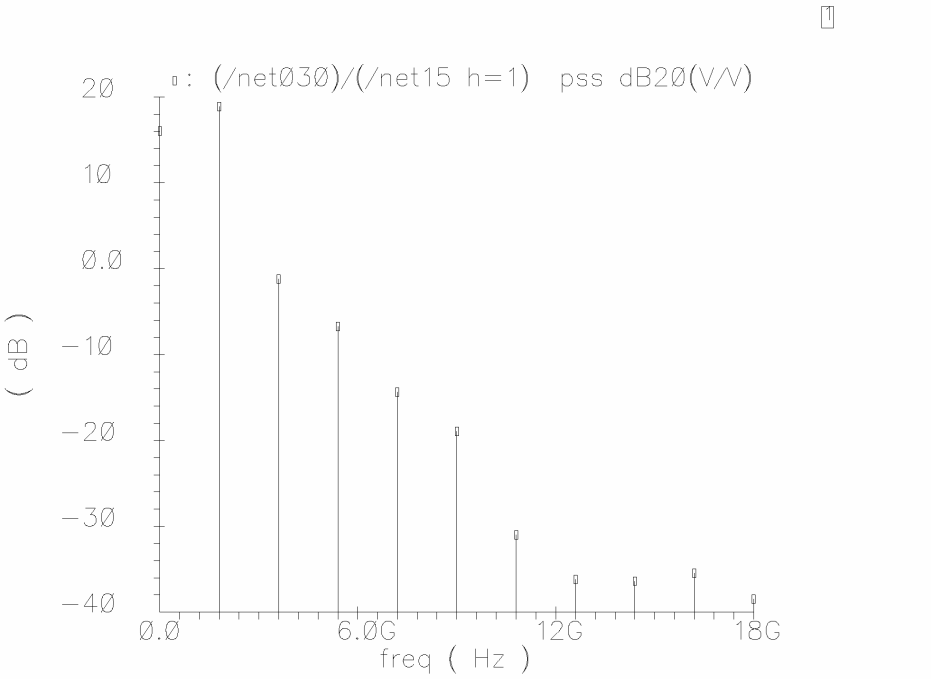
Fig. 27 Contour plot of noise figure, gain and IIP3.

The simulation results in Cadence Spectre are shown in Fig. 28. The noise figure and transducer gain is well matched between the predicted values and simulation results. The circuits S-

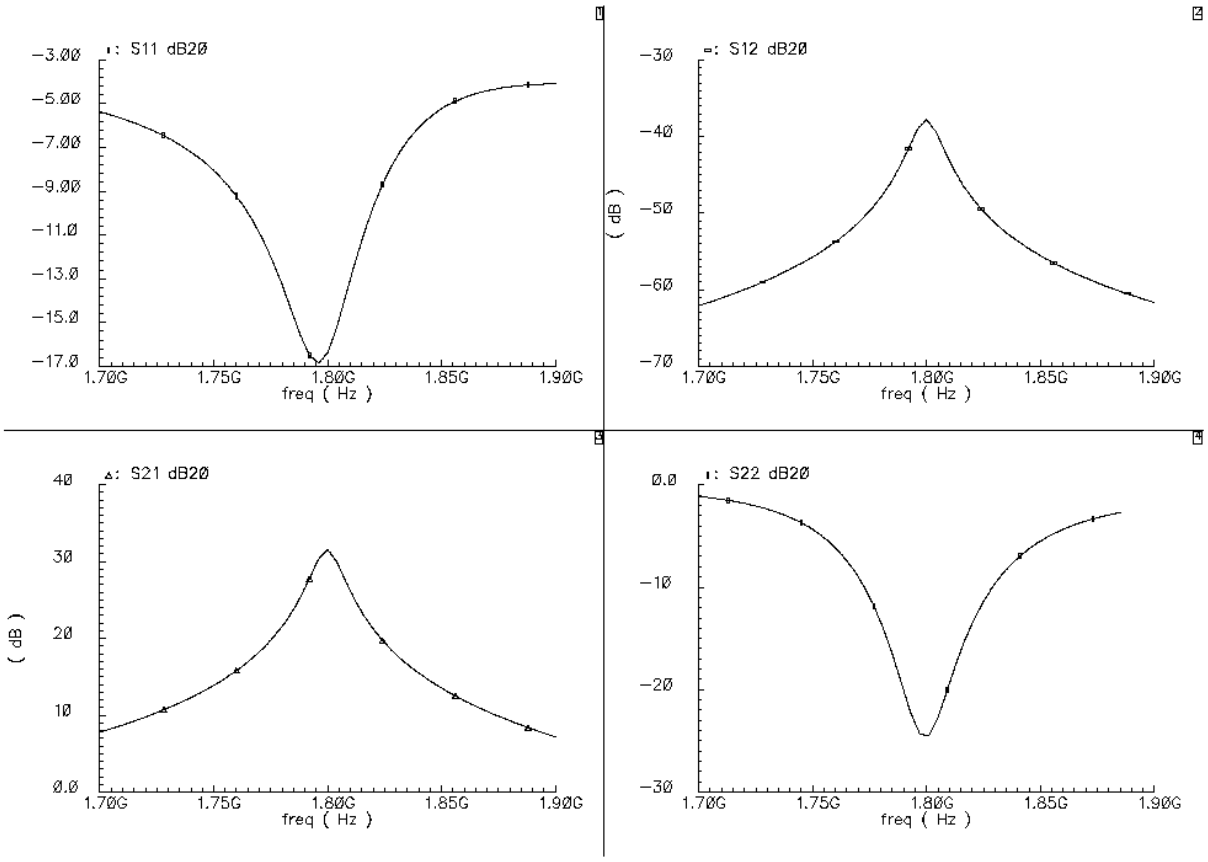
parameter performance is also very good. In Fig. 28(a), it can be seen that $NF_{\min}$ (around 0.22 dB) is not achieved at the desired frequency due to power matching instead of noise matching at the input port, but the noise sacrifice is pretty small.



(a)


: (/net030)/(/net15 h=1) pss dB20(V/V)
20
10
0.0
−10
−20
−30
−40
(dB)
0.0
6.0G
12G
18G
freq (Hz)

(b)



(c)

Fig. 28 Simulation results of (a) noise figure, (b) voltage gain, (c) S-parameters.

The design is compared with other designs reported in the literature in Table 3. For the sake of fairness, the designs compared are simulation results using cascade structure with source inductively degenerated and using CMOS technology. This work provides very good performance in terms of noise, gain and linearity, demonstrating the merit of the design method used in this work.

Table 3 Comparison of Recent LNA Reports

Author [ref.]	Gramegna *et al.* [42]	Park *et al.* [43]	Tinella *et al.* [24]	Yang *et al.* [44]	Guo *et al.* [24]	Youssef *et al.* [45]	This work
NF (dB)	0.9	>1.3	3	2.2	1.6	1.8	0.253
Input 1dB Compression Level (dBm)	-15	-17.8					
IIP3 (dBm)	-1.5		0	1.27		>-10	
OIP3 (dBm)	14			10.7			
Power (mW)	8.55	23.4	4.5	4.8	9	7.1	8
Frequency (GHz)	0.92	1.85	2.5	2.45	1.9	0.95	1.8
Technology	0.35 µm RF CMOS	0.35 µm CMOS	0.25 µm partially depleted SOI-CMOS	0.25 µm 5-metal CMOS	0.35 µm CMOS	0.6 µm AMS CMOS	TSMC 0.35 µm CMOS
Year	2001	2001	2001	2001	2002	2002	2004
Power Supply (V)	1.8	?	1	3.3	1.5	1.5	3.3
Architecture	Cascode, source L degenated	two stage	Cascode, source L degenated	Cascode, source L degenated	Cascode, source L degenated	Cascode, source L degenated	Cascode, source L degenated
S11 (dB)	-8.5	-24		-17		-40	-16.4
S21 (dB)	13.3	15	13.4	15	17.5	13	32
S12 (dB)				-24			-38
S22 (dB)	-27	-5		-23			-24.5

4.8 Conclusion

In a LNA design, bias point and device size are treated as independent variables. While device size tailoring is theoretically well researched, bias point is still obtained by extensive simulation. This work discusses a noise, gain, and linearity optimization under power constraint, with the independent design variables reduced to only device size. A noise, gain and linearity concurrent optimization method for an integrated cascode CMOS LNA under power constraint is demonstrated. Comparison between the result from this method and those from other methods show its superiority. It can easily be adapted to single-transistor and differential CMOS LNAs, as well as their bipolar counterparts.

CHAPTER FIVE: MIXER DESIGN

5.1 Introduction

Study in linearity of mixer is a strong interest more recently. At high frequencies, and particularly with narrowband circuits, it is more common to characterize the distortion produced by a circuit in terms of a compression point or an intercept point. Therefore, third-order intercept point (IP3) and –1 dB compression point becomes two important figures to represent the linearity of a mixer. In recent years, the power consumption has also become a critical design concern driven by the emergence of biosensor or mobile applications. As system designers strive to integrate multiple-systems on-chip, power consumption has become an equally important parameter that needs to be optimized along with area and other factors.

Based on aforementioned observations, a method is proposed for the power optimization of CMOS Gilbert cell which is quite popular between designers, and the method is easily extensible to single-balanced active mixers. The relationships between the power consumption of Gilbert cell and the linearity and other main factors are described. In investigating these relationships,

qualitative models in mixers have been developed whose predictions agree very well with sophisticated simulations. This chapter is organized as follows: in Section 5.2 principles and theory analysis for the Gilbert cell and discussion on the power consumption strategy is provided. In Section 5.3 predictions and simulations are compared. Finally, the research is summarized.

5.2 The Gilbert Cell and Theory Analysis

A widely used active mixer in CMOS designs is the Gilbert cell, shown in Fig. 29, because of its reasonable conversion gain, good rejection at the RF and LO ports and fully differential structure.

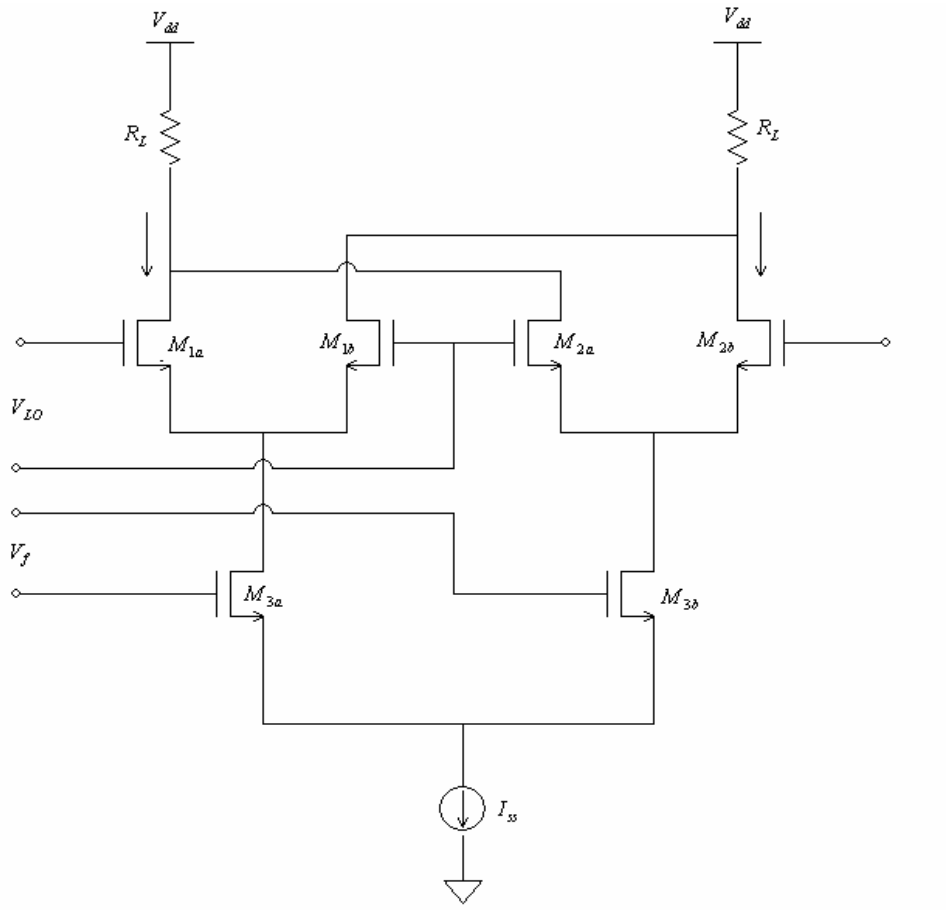


Fig. 29 CMOS Gilbert cell.

It has three differential pairs: two for switch stage and one for transconductance stage. Therefore, it is reasonable for the differential pair, shown in Fig. 30, to be studied carefully at first.

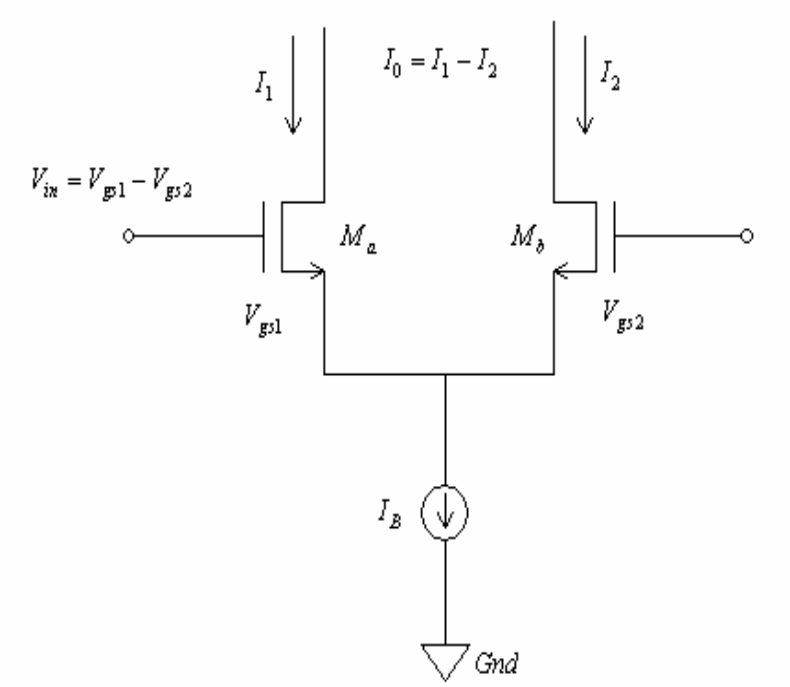


Fig. 30 Differential pair.

The simple square-law MOSFET model for large signal characteristics analysis is not accurate for modern short-channel technologies, and a better approximation for the I-V relation of a MOS transistor is given in [46].

$$I = K \frac{(V_{gs} - V_{th})^2}{1 + \theta (V_{gs} - V_{th})} \tag{5.1}$$

The large-signal behavior of the switching pair is described by

$$I_o = K\frac{(V_{gs1}-V_{th})^2}{1+\theta(V_{gs1}-V_{th})} - K\frac{(V_{gs2}-V_{th})^2}{1+\theta(V_{gs2}-V_{th})} \tag{5.2}$$

$$V_{in} = V_{gs1} - V_{gs2} \tag{5.3}$$

$$I_B = K\frac{(V_{gs1}-V_{th})^2}{1+\theta(V_{gs1}-V_{th})} + K\frac{(V_{gs2}-V_{th})^2}{1+\theta(V_{gs2}-V_{th})} \tag{5.4}$$

Combining (5.2), (5.3) and (5.4), the following equation for the differential pair is obtained:

$$V_{in} = f(I_o) = \frac{\theta^2}{K}I_o + \sqrt{(\frac{\theta^2}{2K}(I_B+I_o))^2 + \frac{2\theta^2}{K}(I_B+I_o))} - \sqrt{(\frac{\theta^2}{2K}(I_B-I_o))^2 + \frac{2\theta^2}{K}(I_B-I_o)} \tag{5.5}$$

Taylor series are usually used for weakly nonlinear behavior analysis because it is simple. We can write differential pair output signal I_0 as a function of the input V_{in} as follows:

$$I_o = f^{-1}(V_{in}) = c_1V_{in} + c_3V_{in}^3 + c_5V_{in}^5 + ... \tag{5.6}$$

By combining (5.5) and (5.6), the following results can be achieved:

$$c_1 = (\frac{\theta^2 I_B}{8} + \frac{K}{2})\sqrt{\frac{I_B}{K}(\frac{\theta^2 I_B}{K}+8)} - (1+\frac{\theta^2 I_B}{8K})\theta I_B \cong \sqrt{2KI_B}\,|_{\theta\to 0} \tag{5.7}$$

$$c_3 = \theta\frac{4\theta^3c_1^3 - 20\theta^2Kc_1^2 + 32\theta K^2c_1 - 16K^3}{32\theta^2KI_B + 4\theta^4I_B^2 + 32\theta Kc_1} \cong -\frac{K^{\frac{3}{2}}}{2\sqrt{2I_B}}\,|_{\theta\to 0} \tag{5.8}$$

Assuming that the commutating MOSFETs act as perfect switches, the main contribution of distortion for the mixer is from the input MOSFETs. The input MOSFETs transconductance can be modeled as weak nonlinear. The IIP3 of Gilbert cell given in (5.5) has been used as a linearity criterion in many previous reports:

$$IIP_3 = dB_{20}\sqrt{\frac{4}{3}\frac{c_1}{c_3}} \cong dB_{20}\sqrt{\frac{16I_{ss}}{3K_3}} \tag{5.9}$$

A more accurate expression can be achieved by instituting the coefficients c_1 and c_3 with (5.7) and (5.8). The model is accurate only when I_{ss} is large so that a large input V_{in} is permitted with linearity and the large-signal model is a good selection then. In fact, the model is inaccurate when I_{ss} is small, however, because it does not consider the input nonlinear impedance components, gate-source capacitance (C_{gs}) and feedback component through gate-drain capacitance (C_{gd}) and the non-linearity of the transconductance of the transistors for low current density. Also, in many works, such as [47], [48], small-signal model is employed to analyze the linearity of transistors. We can suggest two tail current tradeoff I_{ss1} and I_{ss2}. There are three regions, at the third region, $I_{ss} \geq I_{ss2}$, the transistor model used for equation (5.9) is accurate for high current density. At the first region, $I_{ss} \leq I_{ss1}$, the small-signal model is accurate for small current density. At the second region, $I_{ss2} \geq I_{ss} \geq I_{ss1}$, we can use the linear evaluation method to calculate IIP3.

The suggested small-signal model is shown in Fig. 31 and employed to calculate the IIP3 when $I_{ss} \leq I_{ss1}$.

$$IIP_3 = dB_{20}\sqrt{\frac{16}{3}\frac{(1+\beta)^2\sqrt{I_{ss}/2K_3}(1+\theta\sqrt{I_{ss}/2K_3})^4(2+\theta\sqrt{I_{ss}/2K_3})}{\theta(1+\theta(2+\theta\sqrt{I_{ss}/2K_3}))}} \tag{5.10}$$

where K_3 is the K parameter of M_a or M_b, β is an intermediate parameter:

$$\beta = (Z_g + Z_s)C_{gs}s + (Z_g + Z_s)C_{gd}s\frac{g_m + g_{ds}}{C_{gd}s + g_{ds}} \tag{5.11}$$

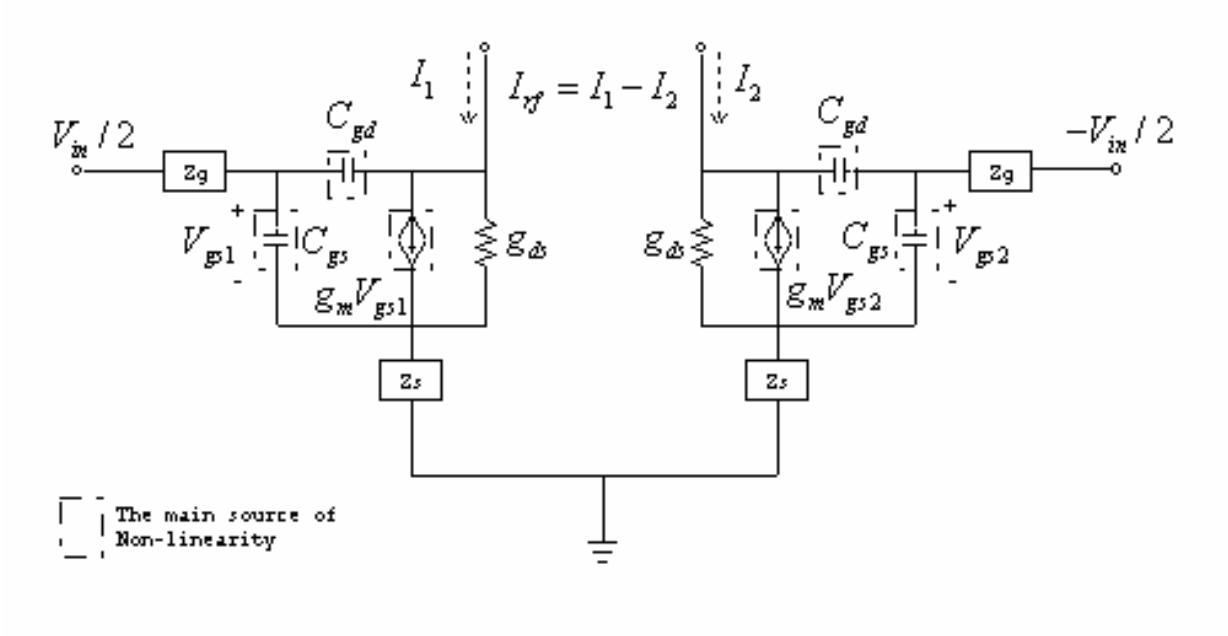


Fig. 31 Small-signal model of transconductance stage.

The conversion gain of the Gilbert cell in transconductance of differential pairs is

$$g_c = \alpha \cdot g_{m3} \cdot R_L \tag{5.12}$$

An estimate α can be obtained by approximating the driver stage output current with a straight line [49]

$$\alpha \cong \frac{2}{\pi} \frac{(1+\sqrt{1+\frac{8K_{1,2}}{\theta^2 I_{ss}}})\frac{\theta}{4K_{1,2}} I_{ss}/V_0}{\arcsin[(1+\sqrt{1+\frac{8K_{1,2}}{\theta^2 I_{ss}}})\frac{\theta}{4K_{1,2}} I_{ss}/V_0]} \tag{5.13}$$

5.3 Simulation Results

To validate the theory, the TSMC 0.35-μm process BSIM3V3 models are used for the linearity of Gilbert cell study. The output load is R_L = 300 Ω, input LO power is V_0 = 0.6 V. The input reference impedance is 50 Ω. The IIP3 of the mixer is simulated using SPECTRE-RF periodic steady-state (PSS) analysis and periodic AC (PAC) analysis. Two tones with equal size are traditionally used to test the IIP3 of a design. A new test method using unequally sized test tones has been described and discussed in [50], it is more accurate and fast. We use this method to test the IIP3 of our design for more sophisticated simulation. The predicted (computed numerically) and simulated values for the IIP3 are shown in Fig. 32, in which fairly good agreement is observed. For getting a good linearity performance and also power consumption, the I_{ss2} can be selected as tail current supply. Fig. 33 shows the relationship between noise figure and tail current. The conversion gain is also simulated using SPECTRE-RF, it increases with the increasing tail current at the first regions, and the second region is the optimal tail current region where the conversion gain is constant. Due to the degeneration of the conversion gain of

switching pairs as discussed previously and the subtracting nature of the third-order harmonic, a reduction of the conversion gain will appear in the third region, as shown in Fig. 34.

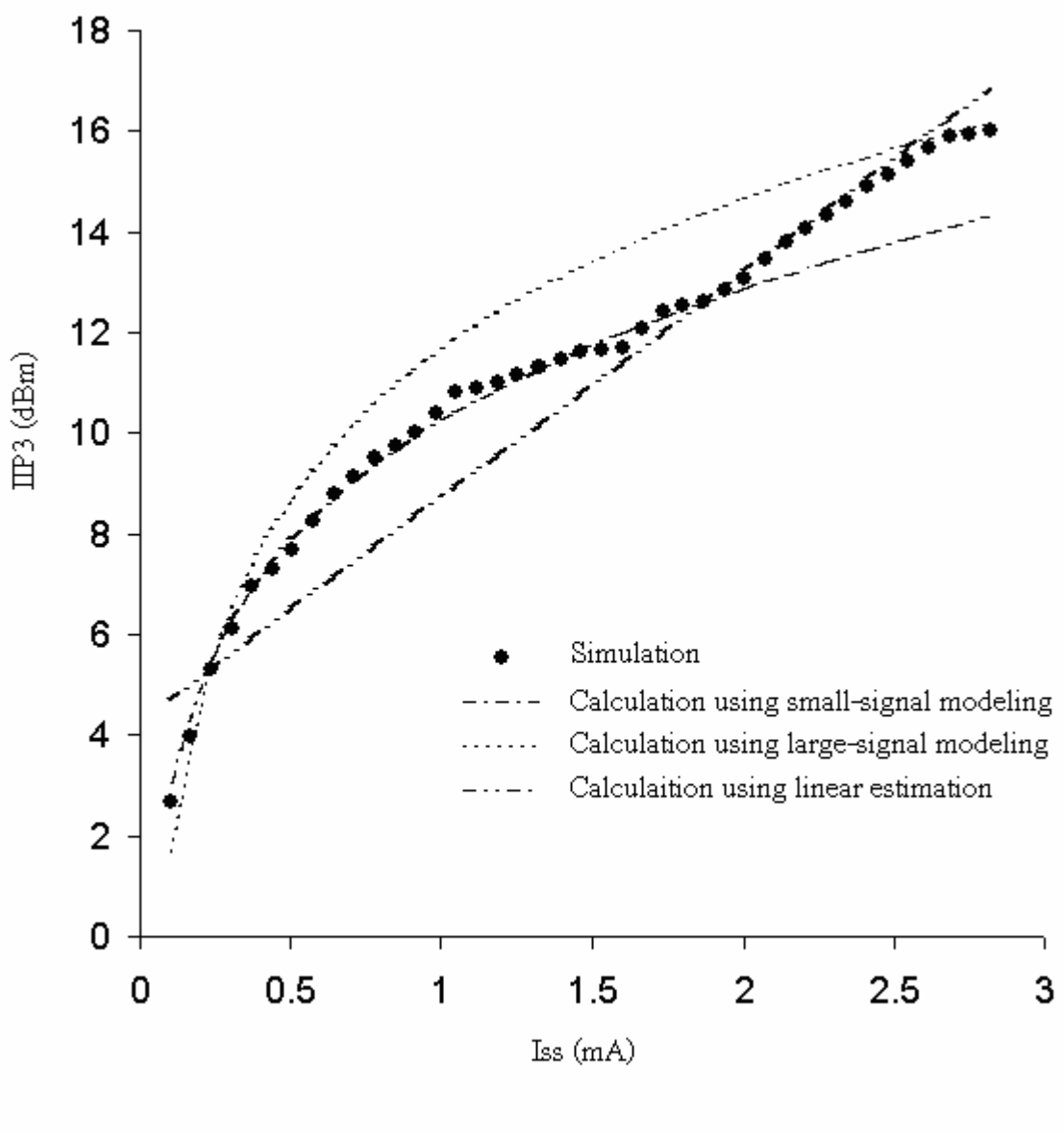


Fig. 32 Simulated relationship between IIP3 and tail current I_{ss} by TSMC 0.35-μm process.

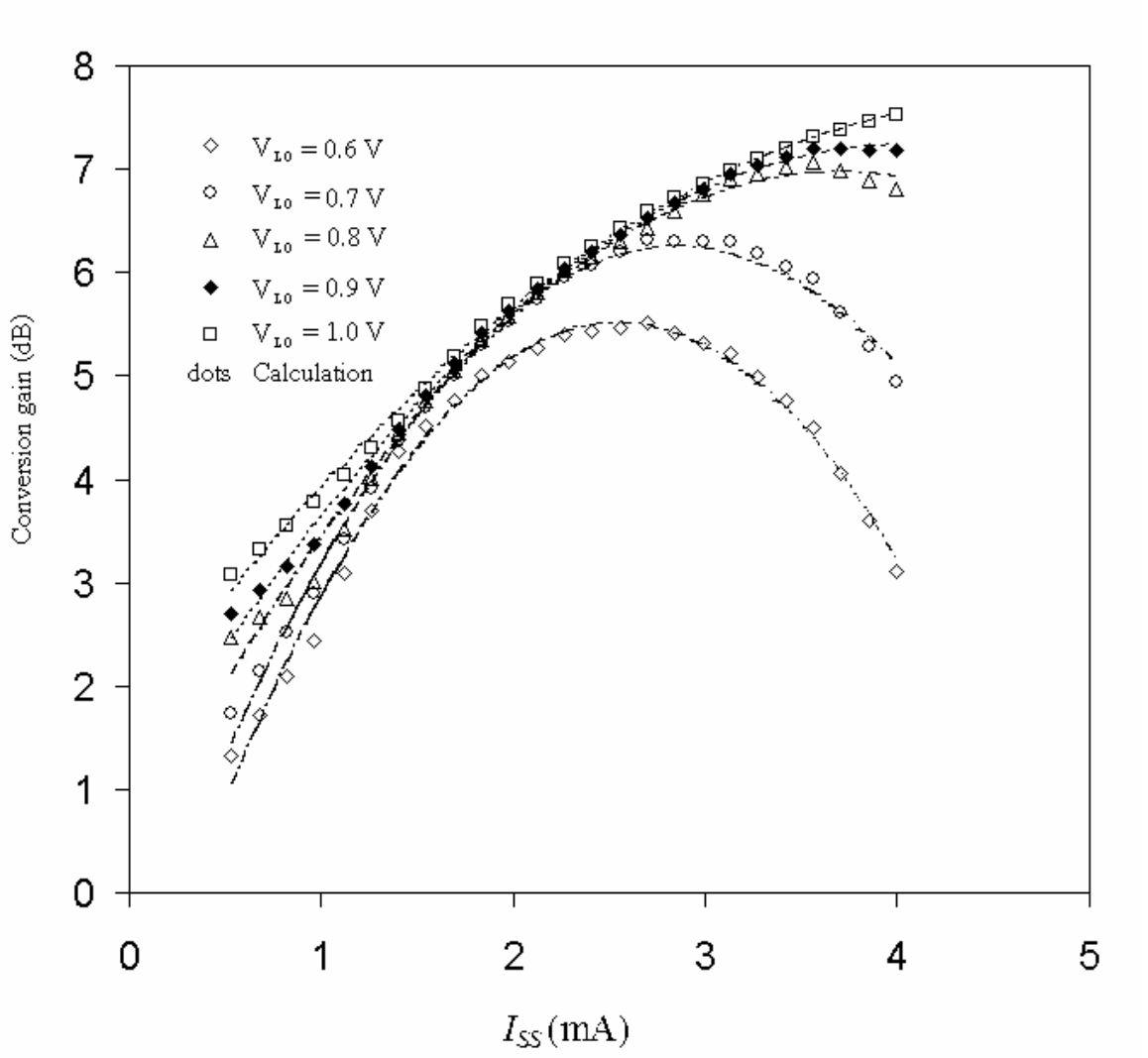


Fig. 33 Simulated conversion gain.

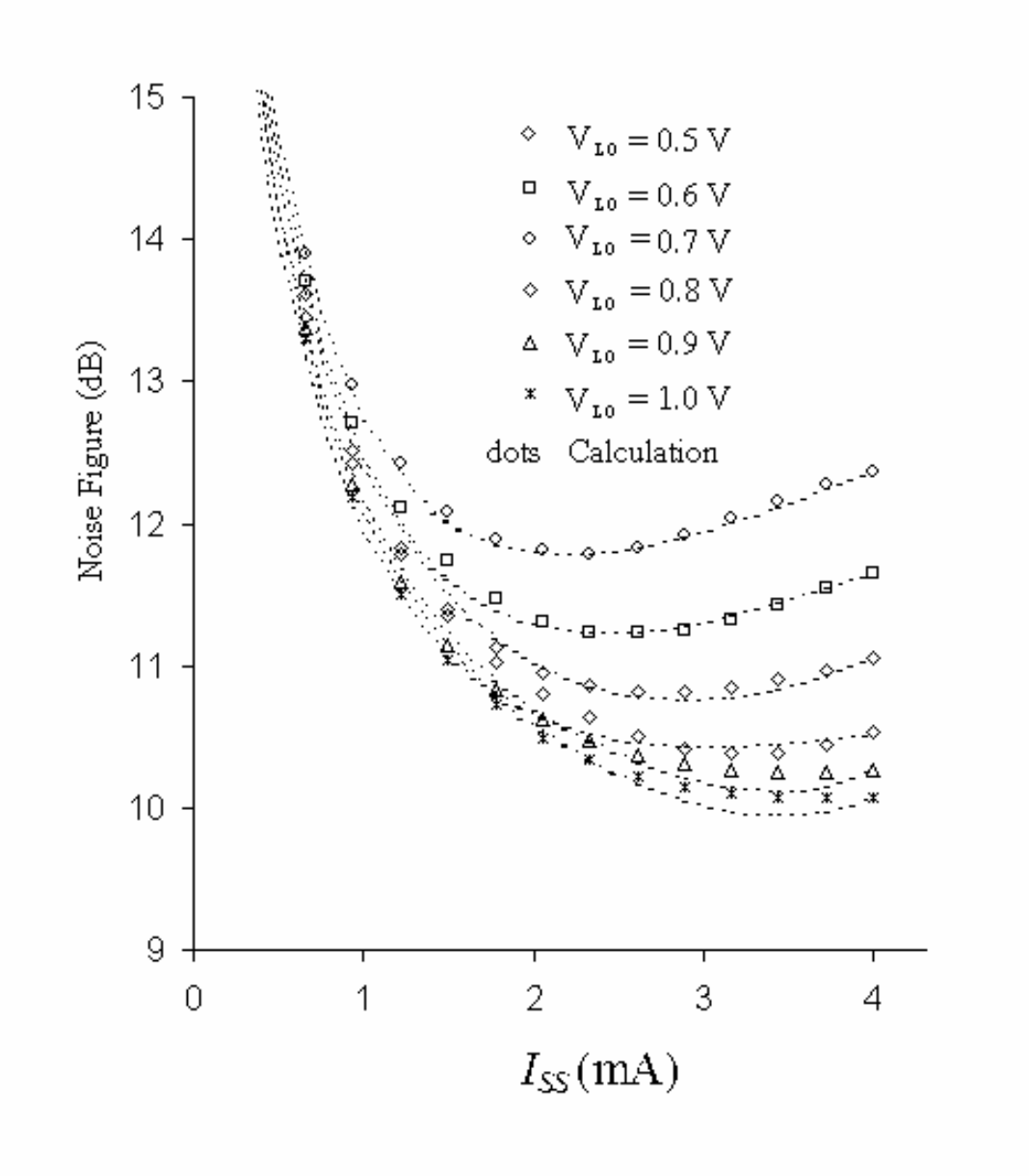


Fig. 34 Simulated SSB NF versus I_{SS} with different LO input amplitude.

Linearity can also be improved by increasing the gate overdrive voltage. The transconductance stage transistor can be operated in strong inversion if a sufficient overdrive is obtained [51].

An expression for P_{IIP3} is [48]:

$$P_{IIP3}\left(V_{od}\right)=\frac{8}{3}\frac{\upsilon_{sat}L}{\mu_1 R_S}V_{od}\left(1+\frac{\mu_1 V_{od}}{4\upsilon_{sat}L}\right)\left(1+\frac{\mu_1 V_{od}}{2\upsilon_{sat}L}\right)^2 \tag{5.14}$$

From (20), linearity can be improved by increasing the gate overdrive. However. Ihe large overdrive leaves little voltage headroom under 3.3 V supply to ensure the transconductance stage stays in the saturation region. Increasing the gate overdrive will also increase the power consumption which is unfavorable for low power application. A moderate conversion gain is necessary to reduce the noise contribution of the IF or baseband amplifier to the overall noise figure of the mixer.

The noise figure of a mixer is dominated by the current switch stage and is higher than that of a low-noise amplifier. The input transistor contributes 2-3 dB to the overall noise figure [52]. Common-gate and common-source input stages do not make too much difference in the noise contribution. A small gate overdrive voltage of the switch requires smaller LO power to turn the switches on and off effectively. This reduces the LO power and makes the switches more ideal.

Non-ideal switching, such as when the switches arc not completely turned on and off, reduces the conversion gain and increases the noise figure [53].

To validate the theory, the mixer is simulated using Cadence Spectre-RF. The BS1M3V3 MOS model parameters for the TSMC 0.35 urn CMOS process are used.

Fig. 35 illustrates *IIP*3 of the mixer simulated at LO power of -25 dBm. *IIP*3 at -3.7 dB is obtained.

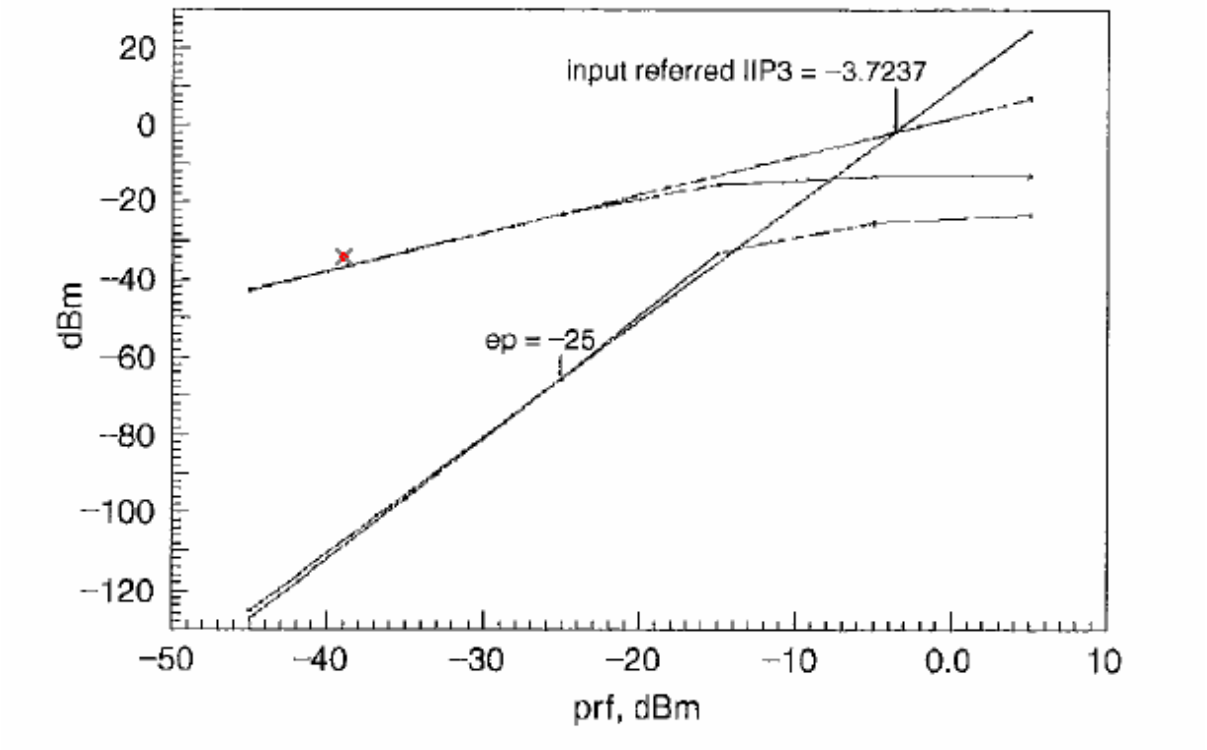


Fig. 35 Mixer *IIP*3 simulation.

Table 4 summarizes the mixer performance.

Table 4 Summary of Mixer Performance

Mixer performance	Value
Supply voltage	3.3V
Frequency	1.8 GHz
NF (SSB)	8.2 dB
IP3 (input)	-12dBm
1dB compression point	-21dBm
Conversion gain	7 dB
Technology	0.35μm CMOS

CHAPTER SIX: GATE-OXIDE BREAKDOWN ON DEVICE AND CIRCUIT PERFORMANCE

6.1 Introduction

Gate oxide breakdown (BD) has been studied extensively. Many papers investigated the defect generation leading to breakdown and the nature of the conduction after breakdown. Recently, researches on the impact of MOSFET gate oxide breakdown on circuits have been reported [3]–[6]. In [6] it was demonstrated that digital circuits would remain functional beyond the first gate oxide hard breakdown, and an equivalent circuit was proposed describing the gate current in an nMOSFET after gate oxide breakdown. On one hand, RF circuits are sensitive to the parameters of their components; therefore BD is reckoned to have severe impact on the performance of the circuits due to impedance mismatch and gain reduction [7]. On the other hand, big transistors are used in RF circuits; one small spot of BD path [8], [9] through the gate may not cause too much characteristic change. So it is worth investigating the performance of RF circuits after device BD.

6.2 Experiments

The devices used in this work are fabricated with 0.16 μm CMOS technology with channel length L = 0.16 μm and channel width W = 10 μm. The oxide thickness t_{ox} is 24 Å. The devices are tested with Cascade Probe Station, Agilent 4156B Precision Semiconductor Parameter Analyzer, and Agilent 8510C Network Analyzer.

The oxide breakdown voltage is first determined from the Voltage Ramp Test (VRT). After VRT the stress condition is then set at constant gate voltage V_G = 4.5 V and constant drain voltage V_D = 2 V with the source and the substrate grounded. High V_{GS} is set to get a fast and easy-to-observe breakdown occurrence. Because MOSFET devices are usually working in the saturation region in analog and RF circuits, the gate oxide breakdown is more likely to occur than under conventional TDDB conditions because of acceleration caused by hot-hole injection. High V_{DS} is also used in the stress in order to mimic the circuit operation condition and embody this effect. The stress automatically stops to avoid further damage to the oxide when the gate current meets a threshold of 1 mA, S-parameters are then measured and the BSIM3V3 model is extracted. Comparison between fresh and stressed I_G - V_G curves confirming the occurrence of hard breakdown are shown in Fig. 36. The gate current is described very well by exponential voltage dependence [54].

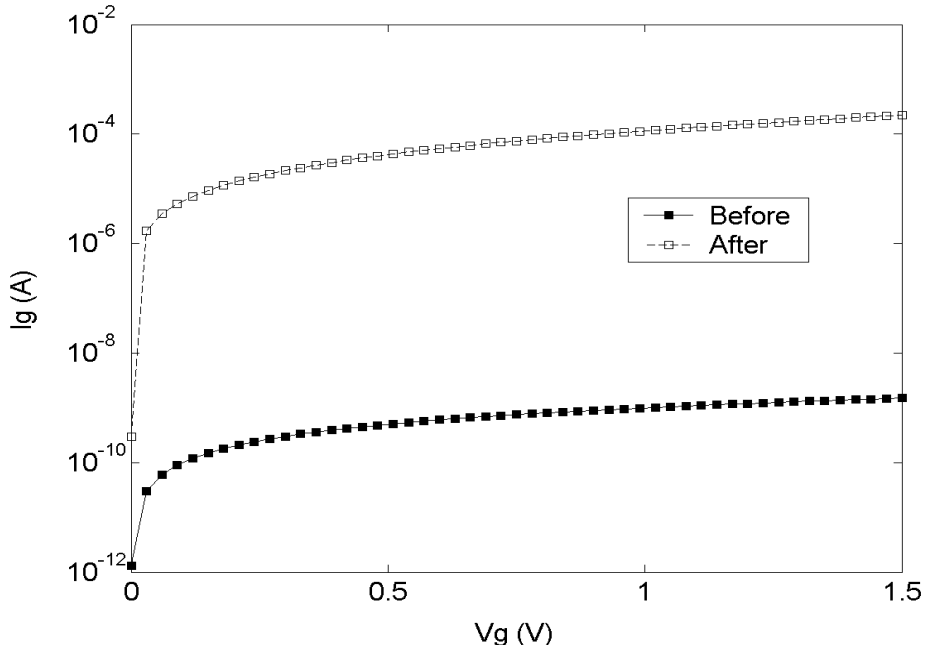


Fig. 36 I_g-V_g characteristics before and after device breakdown.

6.3 Equivalent Circuit Model of a MOSFET after Gate Oxide Breakdown

In [6] post-breakdown nMOSFET gate characteristics were explained by the position of a constant-size breakdown path, and a post-breakdown MOSFET equivalent circuit was proposed to split the original MOSFET into two transistors (represented by level-1 model) and add a breakdown path resistor between them.

When evaluating their results, several issues were identified: 1) Level-1 model is a little bit obsolete; 2) Transistor has a size limit, otherwise punch-through will occur. So simulator cannot handle the breakdown position from 0 to the whole channel length; 3) The two new transistors bring two more diffusion regions, which do not exist in the real post-breakdown transistor.

Based on the aforementioned observations, a modified equivalent circuit, which aims at RF applications, is proposed and shown in Fig. 37.

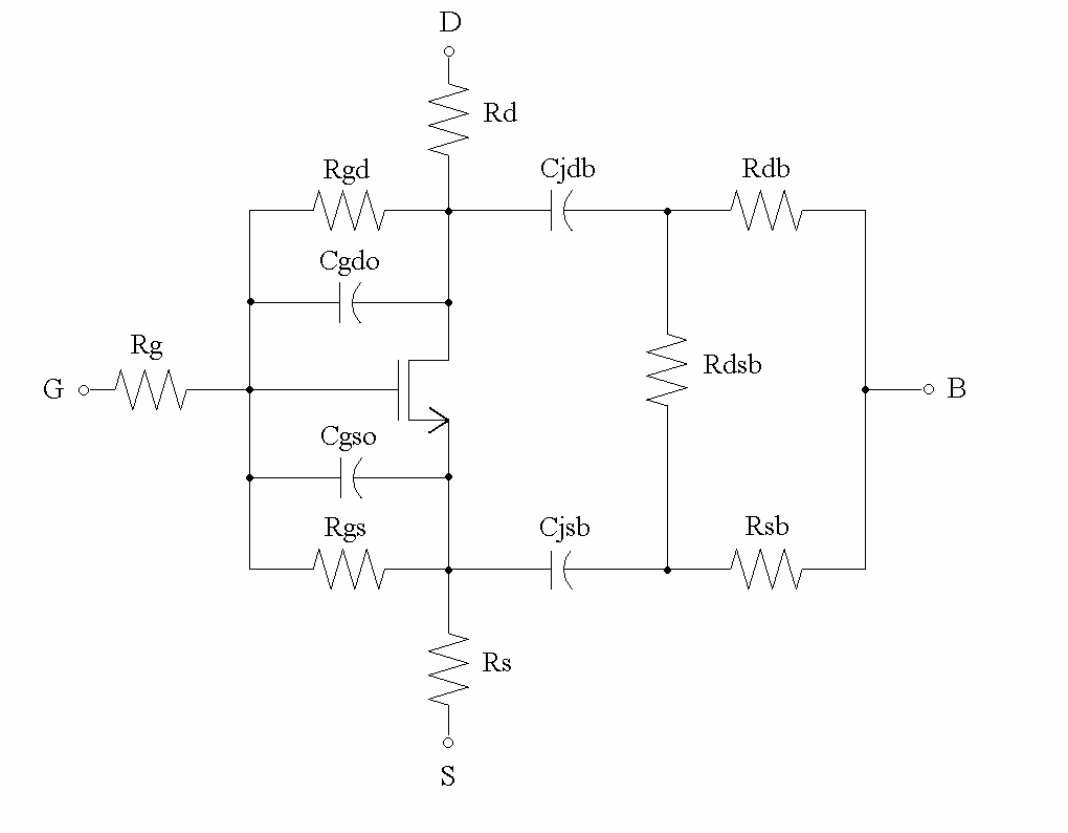


Fig. 37 Equivalent RF circuit after gate-oxide breakdown.

The equivalent circuit includes the intrinsic transistor, the terminal resistances (Rg, Rd, Rs), the substrate resistances (Rdb, Rsb, Rdsb), the overlap resistances (Cgdo, Cgso), the junction capacitances (Cjdb, Cjsb), and the two inter-terminal resistances (Rgd, Rgs). Rg and the RC substrate network are included for more accurate RF modeling [55]–[57]. When either Rgd or Rgs is large enough, the modified equivalent circuit leads to the gate-to-source or gate-to-drain extension breakdown. With different values of Rgd and Rgs representing the conducting path from gate to drain, from gate to source, or from gate to both drain and source [58], the gate-to-channel or gate-to-extension breakdown [59]–[61] can be distinguished and modeled. In this paper, breakdown occurs at about 0.15 μm from the source of the devices tested.

The validity of the present equivalent RF circuit is verified by measured and simulated results for fresh devices before oxide breakdown as well as for those results after breakdown as shown in Fig. 38 and Fig. 39, where W = 10 μm, L = 0.16 μm, tox = 2.4 nm, VT = 0.4 V, Rg = 85.4 Ω, Rd = Rs = 12.14 Ω, Rgd = 6.88 kΩ, Rgs = 23 kΩ, Cgdo = Cgso = 15.3 fF, Cjdb = Cjsb = 7 fF, Rdsb = 80 kΩ and Rdb = Rsb = 49.37 Ω are used for simulation. The model is then used to determine how the gate oxide breakdown affects RF circuit performance.

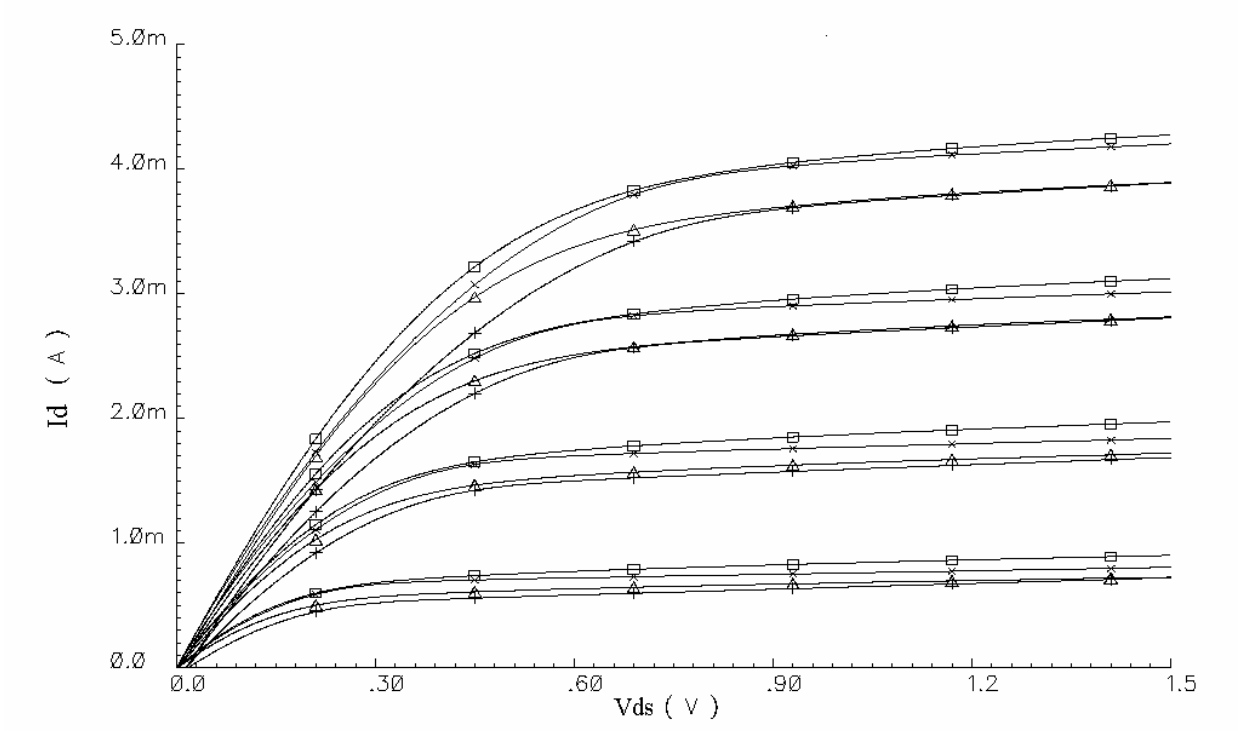


Fig. 38 I-V curves (square tick: fresh measurement, triangle tick: post-BD measurement, x-mark tick: simulation for fresh device, plus-sign tick: simulation for post-BD device).

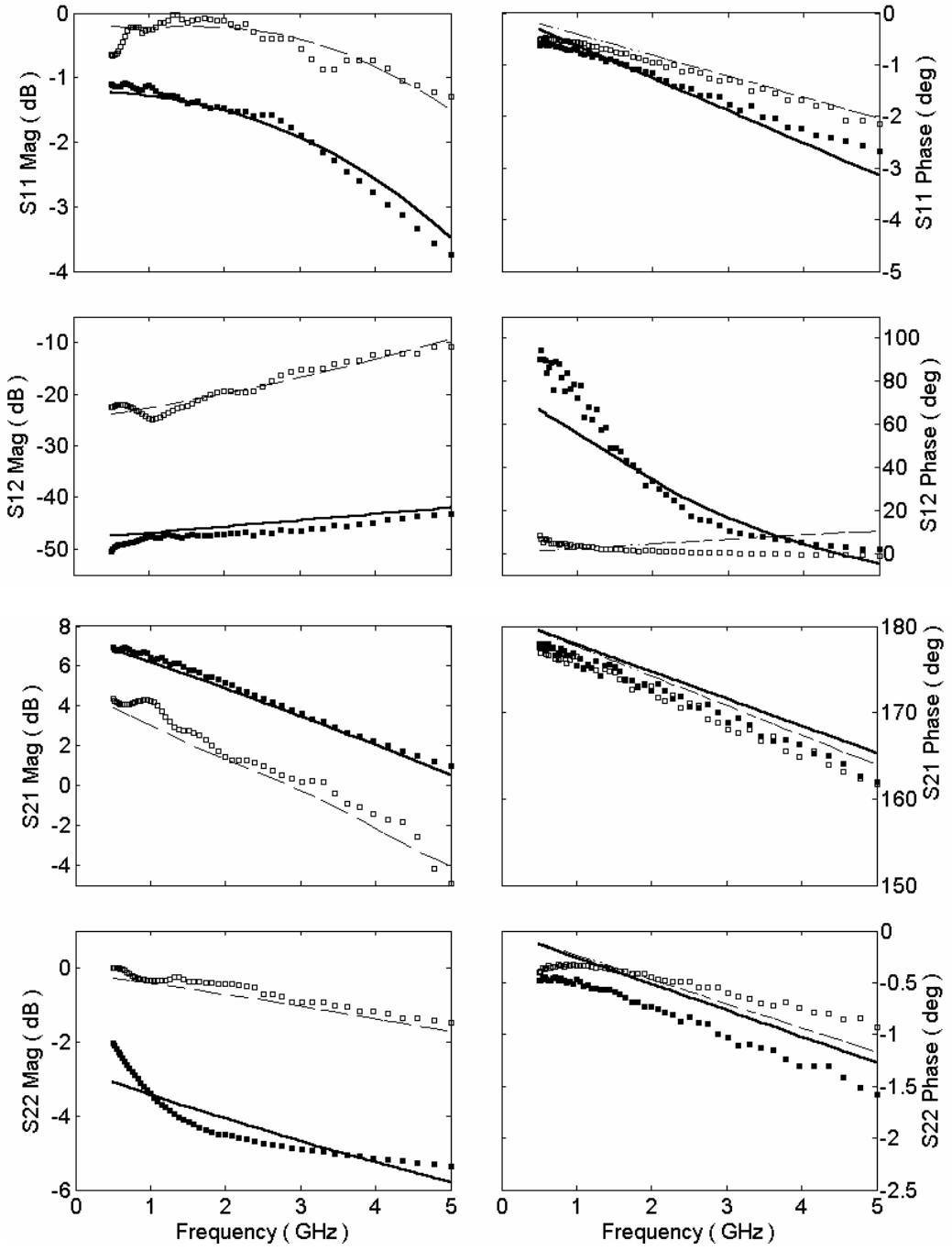


Fig. 39 S-parameters degrade after device breakdown (solid squares: fresh measurement, empty squares: post-BD measurement, thick lines: simulation for fresh device, thin lines: simulation for post-BD device).

6.4 Device Performance Degradation

It is clear from Fig. 39 that S-parameters degrade significantly after breakdown. After BD either a gate-to-channel or a gate-to-extension resistive path is formed. This changes the input impedance at the gate as evidenced by S11; another connection between the gate and the drain other than the original capacitive path, which explains the significant degradation of S12; and the change of the output impedance at the drain, which related to change of S22. The degradation of S21 is consistent with the decrease of gm as in Fig. 40.

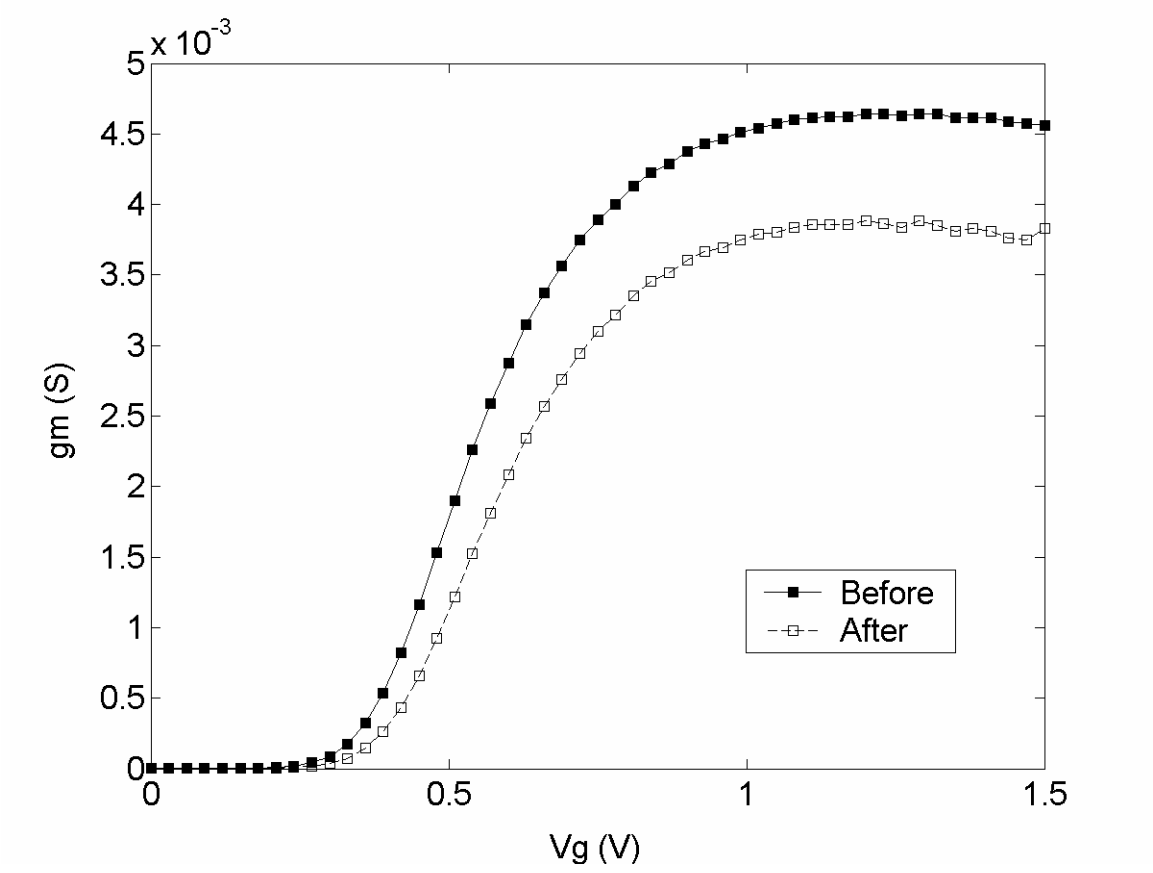


Fig. 40 Transconductance (V_D = 1.5 V) degrades after device breakdown.

The measurement results are similar to the report in [62] that nMOSFET S-parameters degrade due to hot carrier (HC) effects. Yet there exists difference in the significance of S-parameters degradation. Here, S12 changes most, while in [62] S21 and S22 change more than S11 and S12. The difference lies in the fact that in HC stressing, the damage of interface states and charge trapping is more likely to appear near the drain end, and there is parasitic drain series resistance increase [58], [63], [64] in NMOS, thus more impact is brought on the parameters related to

output. After BD the damage is a conduction path inside the gate. The isolation between the gate and the drain is broken, thus the reverse transmission S12 suffers most.

6.5 Circuit Performance Analysis

The above equivalent RF circuit after gate oxide breakdown is plugged into the Cadence Spectre simulation of an LNA. Fig. 41 shows a narrow band LNA designed at 1.8 GHz. A cascode structure is used to minimize the Miller effect and increase the gain. Source inductive degeneration is adopted to improve linearity. The inductance at the drain of the cascode device creates a resonant load with the input capacitance of the following mixer stage. Both the input device M1 and the cascode device M2 are composed of 20 fingers with each being 10 μm wide.

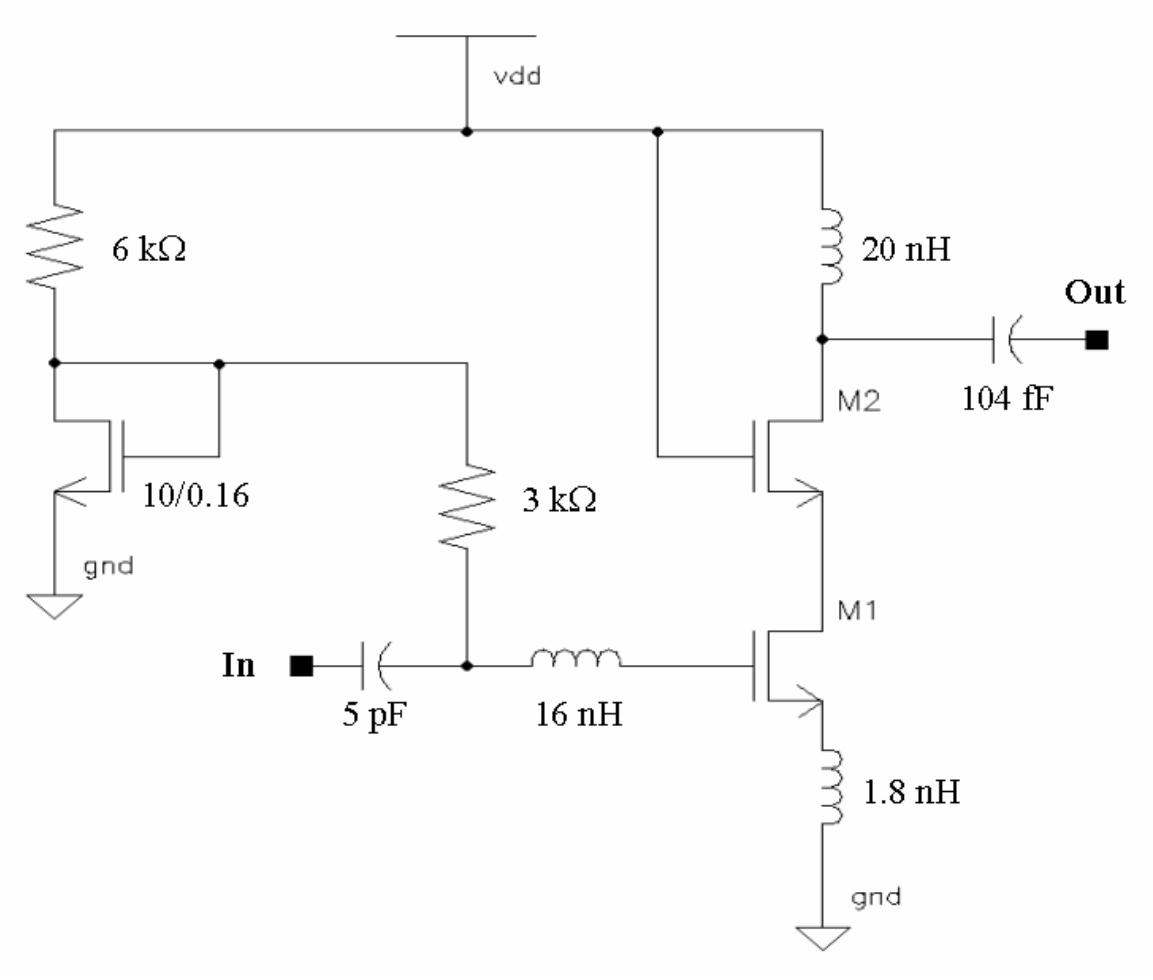


Fig. 41 Schematic of LNA.

It is worth mentioning that not all fingers experience breakdown simultaneously. The condition where only one finger of the input device breaks is first investigated. It can be seen in Fig. 42 that all S-parameter curves drift towards higher frequency and most of these curves change drastically. At 1.8 GHz S11 changes from –19.24 to –6.19 dB, a 68 % reduction; S21 diminishes from 30.59 to 23.47 dB and S22 changes from –17.9 to –6.37 dB. S12 changes only slightly.

Obviously, the circuit can no longer meet the usual –15 dB requirements of S11 and S22 after one finger of M1 breakdowns. From Fig. 43 and 44, the equivalent noise resistance of the circuit jumps from 5 to 18 Ω, and the noise figure changes from 0.54 to 1.81 dB at 1.8 GHz. Even after BD, the noise figure can still meet the general requirement of 2 dB.

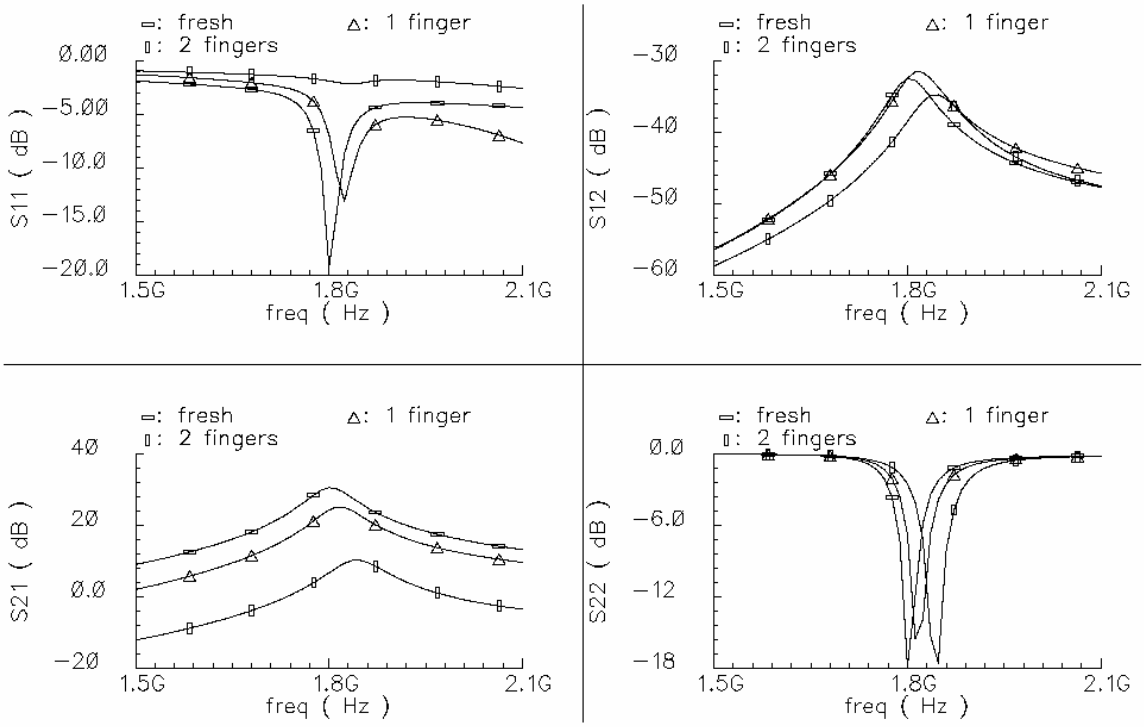


Fig. 42 Circuit S-parameters change before and after one or two fingers of M1 breakdown.

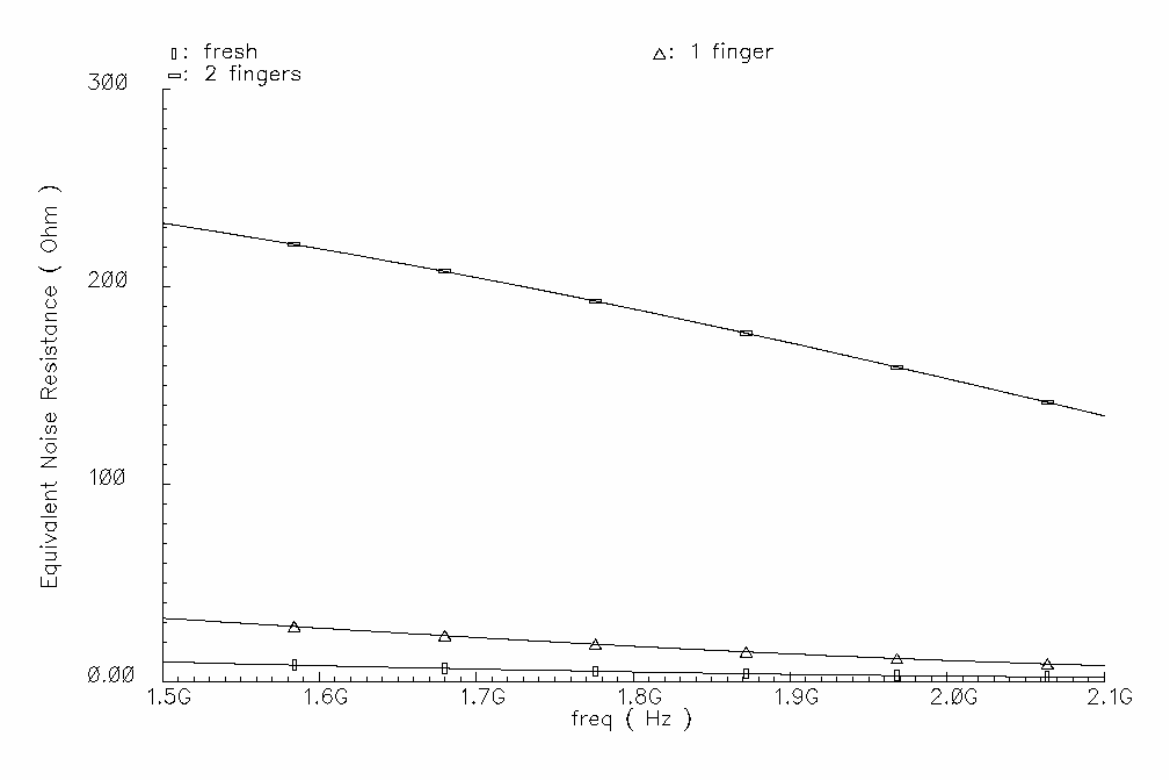


Fig. 43 Change of the equivalent noise resistance before and after up to two fingers of M1 breakdown.

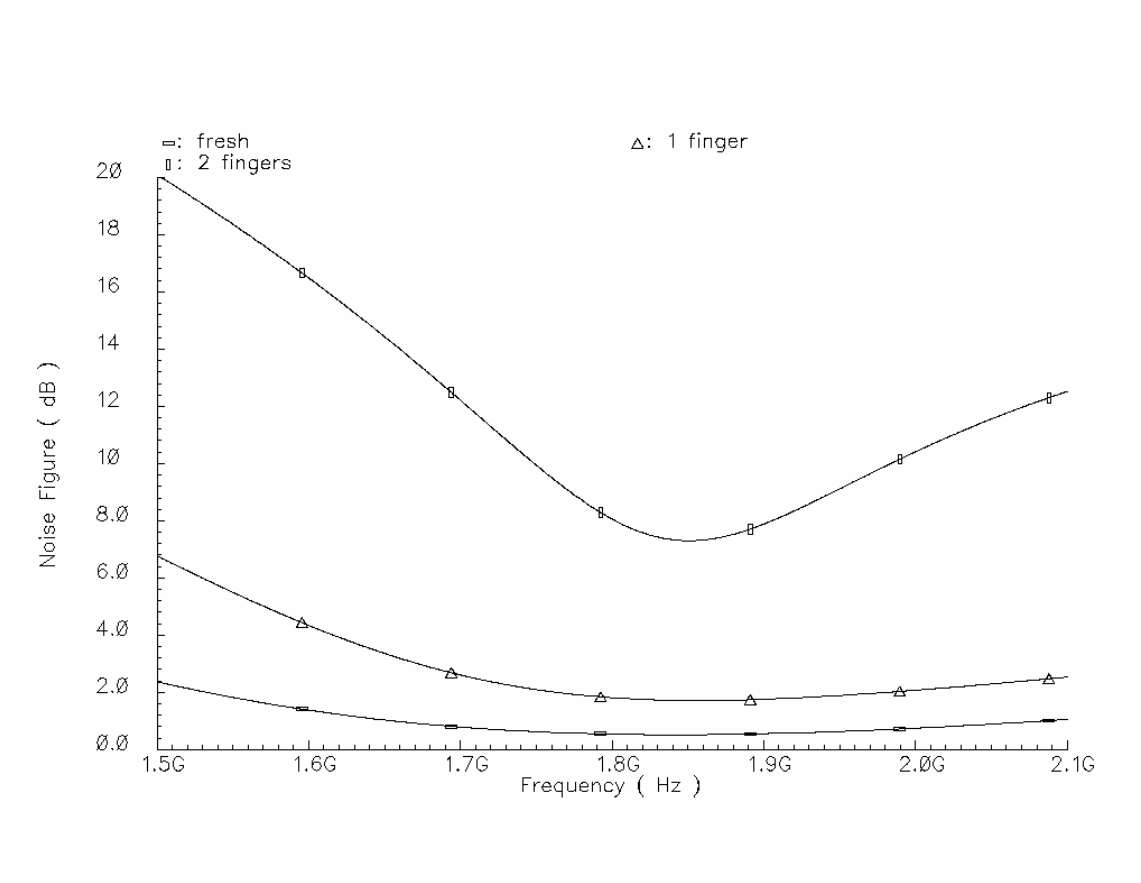


Fig. 44 Change of the noise figure before and after up to two fingers of 1 breakdown.

To explore other probable impacts of different numbers of BD fingers and different BD locations, several other simulations are done. Fig. 42–44 also show S-parameters, equivalent noise resistances, and noise figures of the LNA after up to two fingers of M1 break down. These figures of merits degrade more drastically after 2 fingers of M1 break.

The circuit performance degradation can be explained by the following. After BD a leakage path exists across the gate oxide [7]. This adds another noise source to the transistor, thus degrades the NF. Also the drastical increase in gate current significantly increases the real part of the complex input impedance. The immediate impact of such a change is to destroy the impedance matching condition, which is critical for LNA performance. Thus, circuit S-parameters degrade significantly, or even become unacceptable.

However, the breakdown of the cascode device is found not so crucial to the operation of the LNA. Table 5 and 6 list S-parameters and noise figures after several fingers of the cascode device break, while none or one finger of the input device breaking down at the same time. No matter whether none or one finger of the input device breaks, the breakdown of one or several fingers of the cascode device does not bring more significant damage to the LNA functionality. The main function of M2 is to provide better isolation between input and output ports rather than to provide significant gain. Besides, added noise at the first stage, M1, is more critical than latter stages, M2, to the overall noise performance. So breakdown of M2 has less severe effect than M1 on the LNA performance.

Table 5 S-parameters in Decible with None or One Finger of the Input Device Breaks down

Number of breakdown fingers of M2	None finger of M1 breaks down			1 finger of M1 breaks down		
	S11	S21	S22	S11	S21	S22
0	-19.24	30.59	-17.9	-6.19	23.47	-6.37
1	-20.43	30.36	-17.89	-6.18	22.95	-6.21
2	-20.31	30.14	-17.15	-5.82	22.56	-6.18
3	-20.56	29.87	-16.77	-5.64	22.11	-5.95
4	-20.05	29.60	-15.39	-5.54	21.65	-5.49
5	-19.25	29.43	-15.10			
6	-17.95	29.22	-14.16			

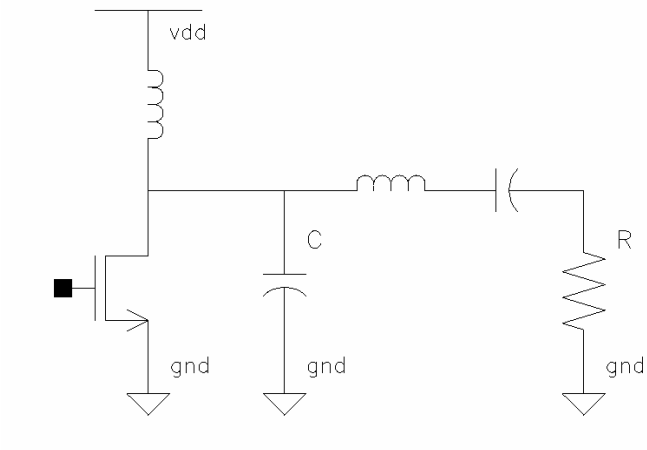
Table 6 Noise Figure with None or One Finger of the Input Device Breaks down

Number of breakdown fingers of M2	0	1	2	3	4
None finger of M1 breaks down	0.540	0.542	0.543	0.545	0.545
1 finger of M1 breaks down	1.81	1.831	1.845	1.864	

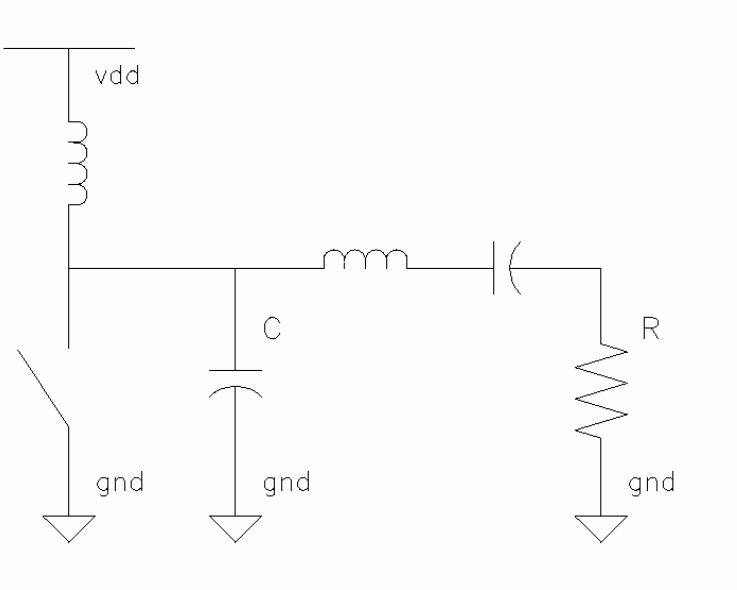
6.6 Effect of gate oxide breakdown on PA

6.6.1 Introduction

High efficiency in power amplifiers is always pursued. The class-E power amplifier, shown in Fig. 45, first devised by Sokal [65] and further analyzed in [66]–[68] has shown enormous potential in the area of high efficiency power amplifiers. The superior efficiency of the class-E power amplifier is due to its ability to displace the current and voltage waveforms of the switch with respect to time in order to allow minimum overlap, thereby reducing the power loss across the switch. This is done by reducing the drain voltage of the transistor to zero prior to the transistor's turning on.



(a)



(b)

Fig. 45 (a) Standard single transistor Class-E power amplifier. (b) Equivalent circuit used to estimate ideal operation with the MOSFET replaced by an ideal switch. The circuit can be thought of as having two states of operation, the "off" state and the "on" state. In the first stage, the switch is open, symbolizing the transistor being turned off (i.e. not providing any current). In this stage, the current from the choke inductor plus the current from the LCR circuit is fed into the capacitor, thereby leading to a buildup of voltage across the shunt capacitor switch combination. The current buildup within the shunt capacitor is discharged through the switch when the switch is closed during the "on" stage.

Nonetheless, the exceedingly high electric fields existing within power amplifier transistors during its operation can easily exceed the breakdown voltages in modern sub-micron technologies. It is known that the portion of the gate oxide near the drain ruptures most frequently in power amplifiers due to the exceedingly high drain voltages [23]. For example, the standard class-E power amplifier [65] is known to suffer from a maximum drain voltage of

$3.57\times V_{DD}$, therefore making this type of power amplifier a prime candidate for oxide breakdown in the gate to drain region.

Meanwhile, an equivalent RF circuit model [69] has been proposed to investigate the effect of gate oxide breakdown on RF circuit performance. This paper adopts the equivalent model to analytically model the amplifier in post-breakdown operation.

6.6.2 Analysis on Performance of Class-E Power Amplifier after Gate Oxide Breakdown

As mentioned earlier, the switch transistor is exposed to large voltage stresses during the "off" stage of the RF cycle. Over time, this voltage stress can lead to destruction of the oxide region between the gate and the drain of the MOSFET used as the amplifying device. However, all fingers in a multi-finger device, such as those frequently used in RF/Analog applications, usually will not break down all at once. Typically each finger will break down in its own time. This allows one to measure the level of breakdown by analyzing how many fingers have deteriorated.

For the breakdown effects on circuit operation to be analyzed, the original MOSFET in Fig. 45 is replaced with the post-oxide breakdown RF circuit model and is shown below in Fig. 46. All of the external parameters surrounding the MOSFET were calculated using the generated parameters in the BSIM3v3 model file obtained from the tested transistor and the BSIM3v3 equations given in [70]. After multiple simulations of the proposed class-E circuit, it was found

that the only parameter that made a significant contribution to the output of this circuit was the R_{gd} resistance. R_d and R_s were included in the MOSFET "on" and "off" resistance values and R_g is bound with R_{gd}. For this reason, Fig. 46 only displays the R_{gd} resistance parameter.

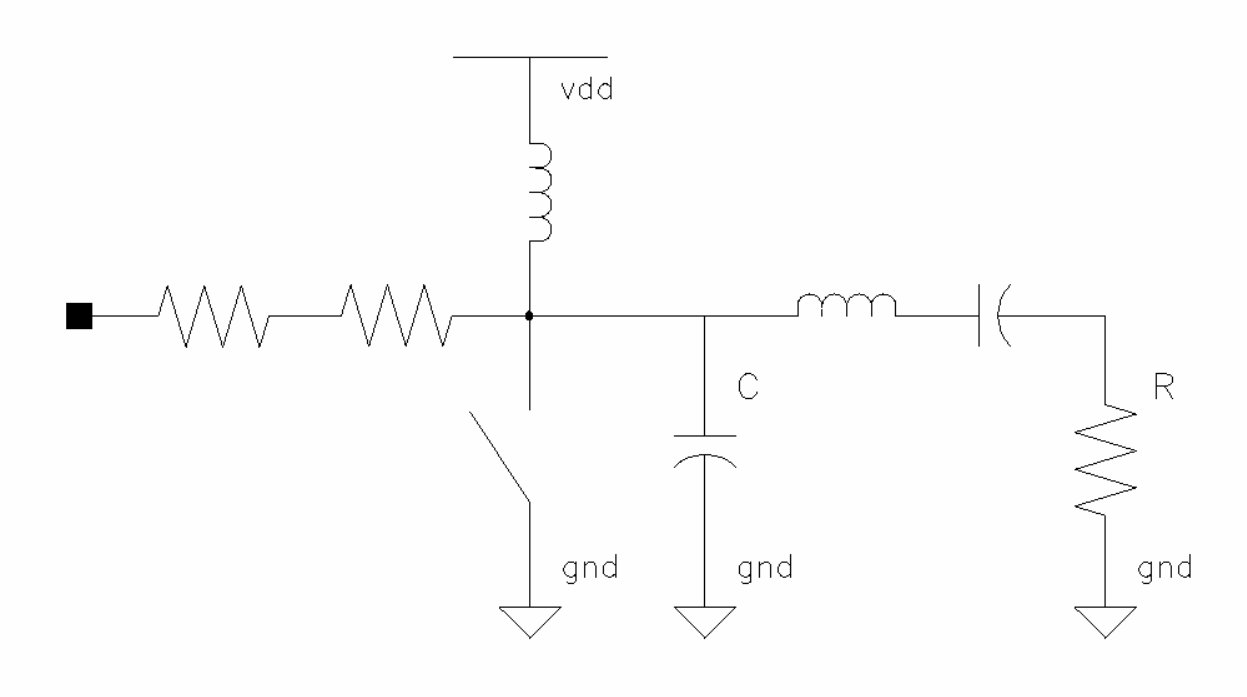


Fig. 46 The revised class-E power amplifier.

The method used to analyze the breakdown effects on the circuit operation analytically is similar to that employed by [57], [58]. The analysis presented here makes the following assumptions:

(1) The output capacitance of the transistor is independent of the switch voltage.

(2) The current fall time from the "on" to "off" state is ignored.

(3) The signal at the gate of the transistor is a square wave with a 50% duty cycle.

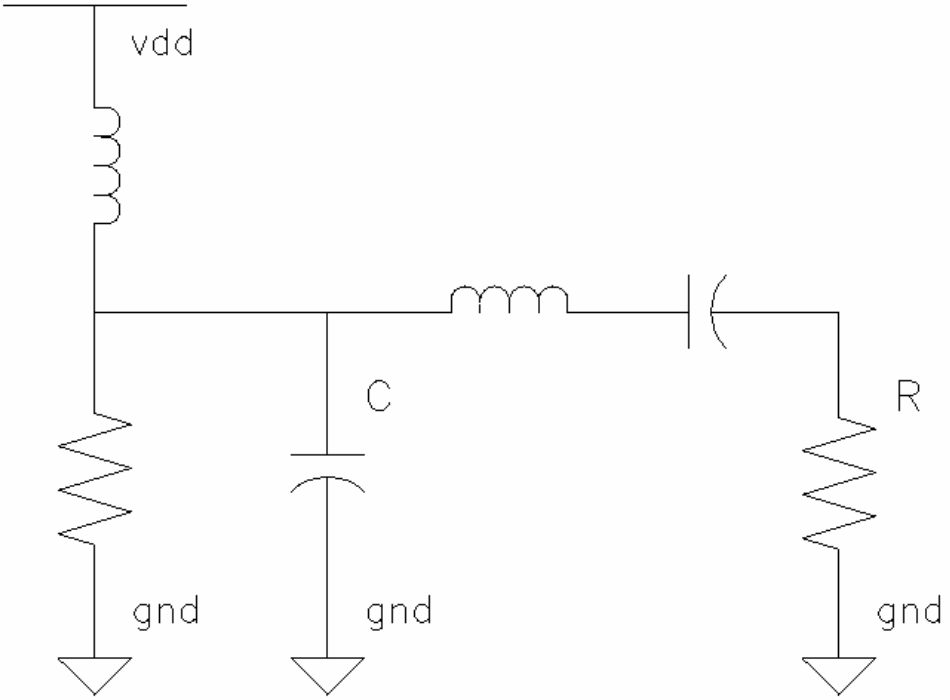
(4) The "on" and "off" resistances are both constant.

(5) The Q factor of the load is large enough to only allow sinusoidal output current to pass, thus providing an output current of

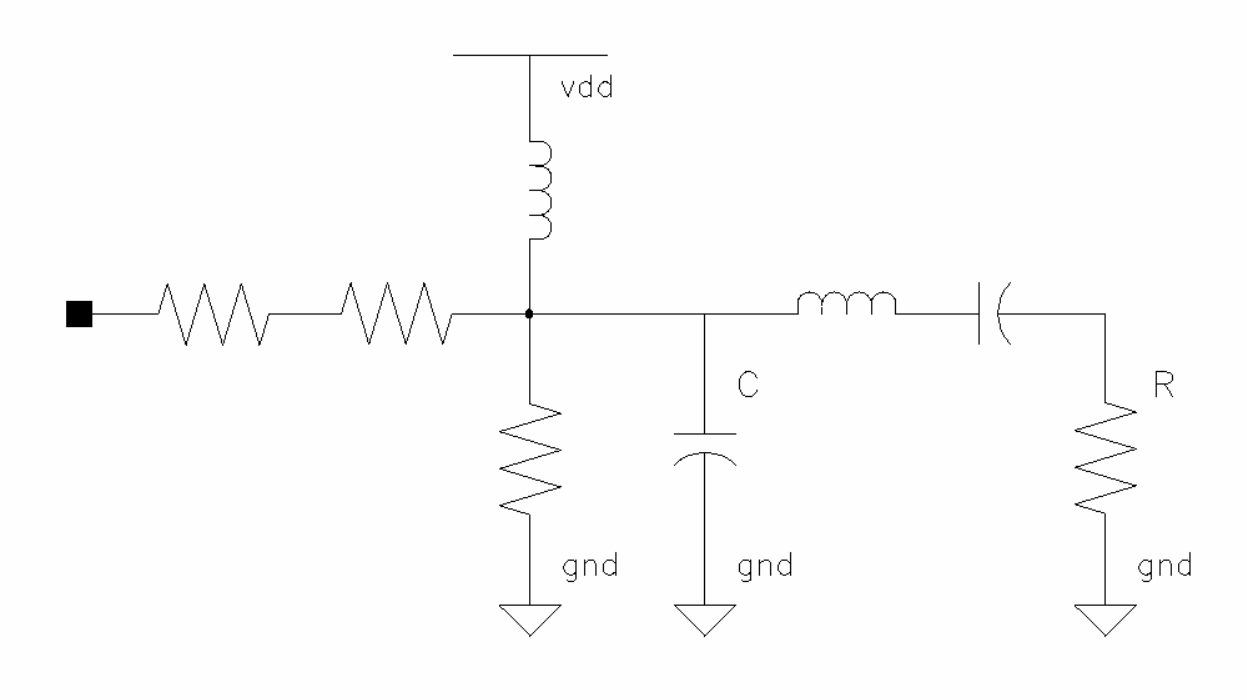
$$i_0 = I_0 \cdot \sin(\omega_c \cdot t + \phi_0) \tag{6.1}$$

where I_o is the amplitude of the output current and ϕ_0 is the initial phase of i_0.

For analysis purposes, the circuit operation cycle is divided into two states, the "off" state and the "on" state. The equivalent circuits used to analyze these states are displayed below as Figs. 47(a) and 47(b). The "off" state ranges between $0 < \omega_c \cdot t \le \pi$, and the "on" state $\pi < \omega_c \cdot t \le 2\pi$.



(a)



(b)

Fig. 47 The equivalent circuit for (a) the "off" state. (b) the "on" state.

During the "off" state, the voltage at the gate of transistor is zero, therefore allowing R_{gd} to act like a link between the drain node of the transistor and ground as noted in Fig 47(a). Summing the currents at the drain node gives

$$i_L = i_d + i_o \tag{6.2}$$

Noting that

$$i_{doff} = i_c + i_R = C_d \cdot \frac{dv_d}{dt} + \frac{v_d}{R} \tag{6.3}$$

and

$$V_{dd} - v_d = L_1 \cdot \frac{di_L}{dt} \tag{6.4}$$

where $R = R_{gd} + R_g$, equations (3) and (4) can be combined with (2) to produce

$$\frac{d^2 i_{Loff}}{dt^2} + p_{off} \cdot \frac{di_{Loff}}{dt} + q \cdot i_{Loff} = q \cdot \left(i_0 + \frac{V_{DD}}{R} \right) \tag{6.5}$$

where

$$p_{off} = \frac{1}{R \cdot C_d} \tag{6.6}$$

$$q = \frac{1}{L_1 \cdot C_d} \tag{6.7}$$

Solving (5) results in

$$i_{Loff} = e^{\alpha \cdot t} \cdot (C_1 \cdot \cos(\beta \cdot t) + C_2 \cdot \sin(\beta \cdot t)) + C_3 \cdot \cos(\omega_c \cdot t + \phi_0) + C_4 \cdot \sin(\omega_c \cdot t + \phi_0) + V_{DD}/R \tag{6.8}$$

where

$$\alpha = \frac{-p_{off}}{2} \tag{6.9}$$

$$\beta = \frac{\sqrt{4 \cdot q - p_{off}{}^2}}{2}$$

$$C_3 = \frac{\begin{vmatrix} 0 & p_{off} \cdot \omega_c \\ I_0 \cdot q & q - \omega_c{}^2 \end{vmatrix}}{\begin{vmatrix} q - \omega_c{}^2 & p_{off} \cdot \omega_c \\ - p_{off} \cdot \omega_c & q - \omega_c{}^2 \end{vmatrix}} \tag{6.10}$$

$$C_4 = \frac{\begin{vmatrix} q - \omega_c{}^2 & 0 \\ - p_{off} \cdot \omega_c & I_0 \cdot q \end{vmatrix}}{\begin{vmatrix} q - \omega_c{}^2 & p_{off} \cdot \omega_c \\ - p_{off} \cdot \omega_c & q - \omega_c{}^2 \end{vmatrix}} \tag{6.11}$$

Placing (8) back into (4) yields the drain voltage equation for the "off" cycle

$$v_{doff} = e^{\alpha t} \cdot ((\alpha \cdot C_1 + \beta \cdot C_2) \cdot \cos(\beta \cdot t) + (\alpha \cdot C_2 - \beta \cdot C_1) \cdot \sin(\beta \cdot t)) + L_1 \cdot C_3 \cdot \omega_c \cdot \sin(\omega_c \cdot t + \phi_0) - L_1 \cdot C_4 \cdot \omega_c \cdot \cos(\omega_c \cdot t + \phi_0) + V_{DD} \tag{6.12}$$

During the "on" state, a voltage is applied to the gate node of the MOSFET, therefore turning it "on" and allowing it to conduct current through the channel. The charge built up in C_d immediately flows into the transistor, thereby increasing the drain current steadily. From Fig. 47(b), it can be noted that R_{gd} can cause more current to leak through the channel, thus increasing the drain current and drain "on" voltage, which in turn leads to greater power loss through the transistor. For this interval, the drain current can be expressed as

$$i_{don} = i_c + i_R + i_{Ron} = C_d \cdot \frac{dv_d}{dt} + \frac{v_d}{R_{//}} - \frac{V_g}{R} \tag{6.13}$$

where $R_{//} = R_{on} \,//\, R$.

Combining (13), (4) and (2) gives

$$\frac{d^2 i_{Lon}}{dt^2} + p_{on} \cdot \frac{di_{Lon}}{dt} + q \cdot i_{Lon} = q \cdot \left(i_0 + \frac{V_{DD}}{R_{//}} - \frac{V_g}{R} \right) \tag{6.14}$$

where

$$p_{on} = \frac{1}{R_{//} \cdot C_d} \tag{6.15}$$

Solving (14) results in

$$i_{Lon} = C_5 e^{r_3 t} + C_6 e^{r_4 t} + C_7 \cos(\omega_c t + \phi_0) + C_8 \sin(\omega_c t + \phi_0) + V_{DD} / R_{//} - V_g / R \tag{6.16}$$

where

$$r_{3,4} = \frac{-p_{on} \pm \sqrt{{p_{on}}^2 - 4 \cdot q}}{2} \tag{6.17}$$

$$C_7 = \frac{\begin{vmatrix} 0 & p_{on} \cdot \omega_c \\ I_0 \cdot q & q - {\omega_c}^2 \end{vmatrix}}{\begin{vmatrix} q - {\omega_c}^2 & p_{on} \cdot \omega_c \\ -p_{on} \cdot \omega_c & q - {\omega_c}^2 \end{vmatrix}} \tag{6.18}$$

$$C_8 = \frac{\begin{vmatrix} q - \omega_c^{\,2} & 0 \\ -p_{on}\cdot\omega_c & I_0\cdot q \end{vmatrix}}{\begin{vmatrix} q - \omega_c^{\,2} & p_{on}\cdot\omega_c \\ -p_{on}\cdot\omega_c & q - \omega_c^{\,2} \end{vmatrix}} \tag{6.19}$$

Placing (16) back into (4) yields

$$v_{don} = -L_1\cdot C_5\cdot r_3\cdot e^{r_3\cdot t} - L_1\cdot C_6\cdot r_4\cdot e^{r_4\cdot t} + L_1\cdot C_7\cdot\omega_c\cdot\sin(\omega_c\cdot t+\phi_0) - L_1\cdot C_8\cdot\omega_c\cdot\cos(\omega_c\cdot t+\phi_0) + V_{DD} \tag{6.20}$$

From equations (12) and (20), the unknowns are found to be C_1, C_2, C_5, C_6, I_0, ϕ_0. In order to estimate values for these constants, the following conditions are employed

$$i_{Lon}\left(\frac{2\pi}{\omega_c}\right) = i_{Loff}(0) \tag{6.21}$$

$$i_{Lon}\left(\frac{\pi}{\omega_c}\right) = i_{Loff}\left(\frac{\pi}{\omega_c}\right) \tag{6.22}$$

$$v_{don}\left(\frac{2\pi}{\omega_c}\right) = v_{doff}(0) \tag{6.23}$$

$$v_{don}\left(\frac{\pi}{\omega_c}\right) = v_{doff}\left(\frac{\pi}{\omega_c}\right) \tag{6.24}$$

$$\left.\frac{dv_d(t)}{dt}\right|_{t=\pi/\omega_c} = 0 \tag{6.25}$$

$$\frac{V_{dd}}{T}\int_0^T i_L(t)dt + \frac{1}{T}\int_{T/2}^T V_g \cdot \frac{V_g - v_{don}(t)}{R}dt = P_{out} + \frac{1}{T}\left(\int_{T/2}^T \frac{v_{don}(t)^2}{R_{on}}dt + \int_0^{T/2}\frac{v_{doff}(t)^2}{R}dt + \int_{T/2}^T \frac{(V_g - v_{don}(t))^2}{R}dt\right) \quad (6.26)$$

Using the above listed boundary conditions, the unknown coefficients can be solved for numerically. Finally, the output power and efficiency can be calculated by

$$P_{out} = \frac{{I_0}^2 \cdot R_L}{2} \quad (6.27)$$

and

$$\eta_d = \frac{1}{(1 + \frac{P_{DS}+P_{BD}}{P_{out}})} \quad (6.28)$$

where P_{DS} is the power dissipated through the channel resistance and P_{BD} is the power dissipated through the breakdown resistance.

The effects of oxide breakdown on PA operation due to the number of fingers experiencing high voltage levels are analyzed. The R_{gd} value used in this circuit depends on the number of fingers that have suffered from oxide breakdown effects. The width of the MOSFET can be thought of as 700 parallel 10 μm fingers. Since each finger is in parallel with its neighbors, its corresponding R_{gd} is also in parallel with its neighbors. Therefore, assuming the experimentally

found value of 1 kΩ is a standard R_{gd} value found to exist with each broken down finger, it can be shown that

$$R_{BD} = \frac{1k\Omega}{N} \tag{6.29}$$

where N = the number of fingers that have suffered from oxide breakdown.

The circuit was first simulated using a fresh transistor model file. The value of R_{gd} was set to an extremely high value to represent an infinite resistance across the oxide layer. The circuit was designed to supply 0.25 Watts of output power at an operating frequency of 950 MHz with a 0.9 V power supply. A finite dc-feed inductor [71] was used instead of an RF choke to help provide some relief on the load resistance and supply voltage. The transient waveforms created at the drain of the MOSFET are displayed in Fig. 48.

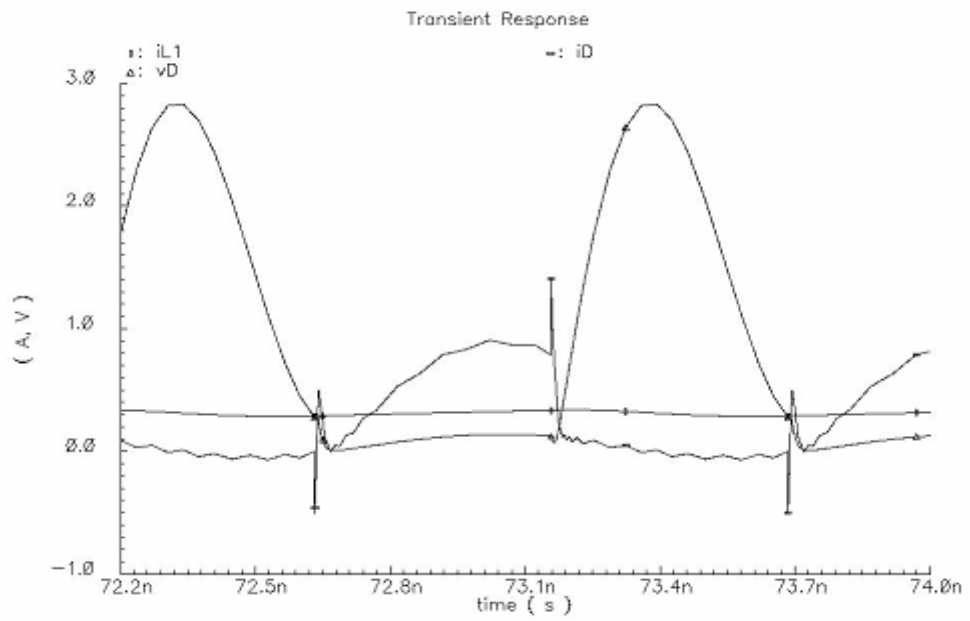


Fig. 48 $v_{D\min}$, i_D and i_L transient waveforms.

When the power amplifier was simulated using the fresh transistor model files with no breakdown effects included, a drain efficiency (η) of 90% was achieved at the fundamental. After the equivalent RF circuit model and the experimentally generated breakdown model files were applied, the drain efficiency at the fundamental dropped to 51% with 100 fingers affected by oxide breakdown. Fig. 49 depicts a comparison between the simulated pre-breakdown and post-breakdown drain efficiency values for various frequencies, whereas Fig. 50 displays the decline in drain efficiency with respect to the number of fingers suffering from oxide breakdown. The drain efficiency decreases rapidly with respect to number of breakdown occurrence.

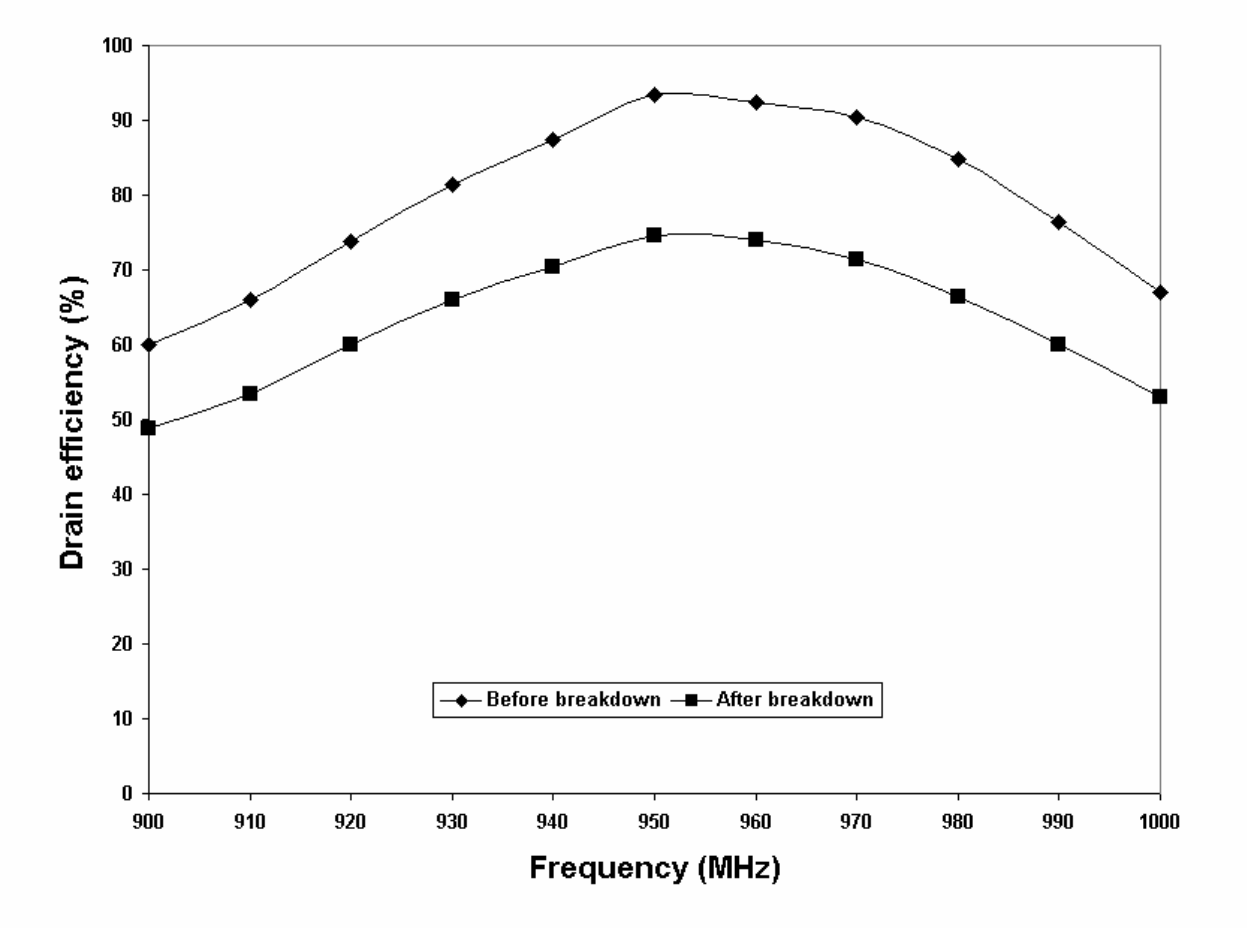


Fig. 49 Drain efficiency versus operation frequency.

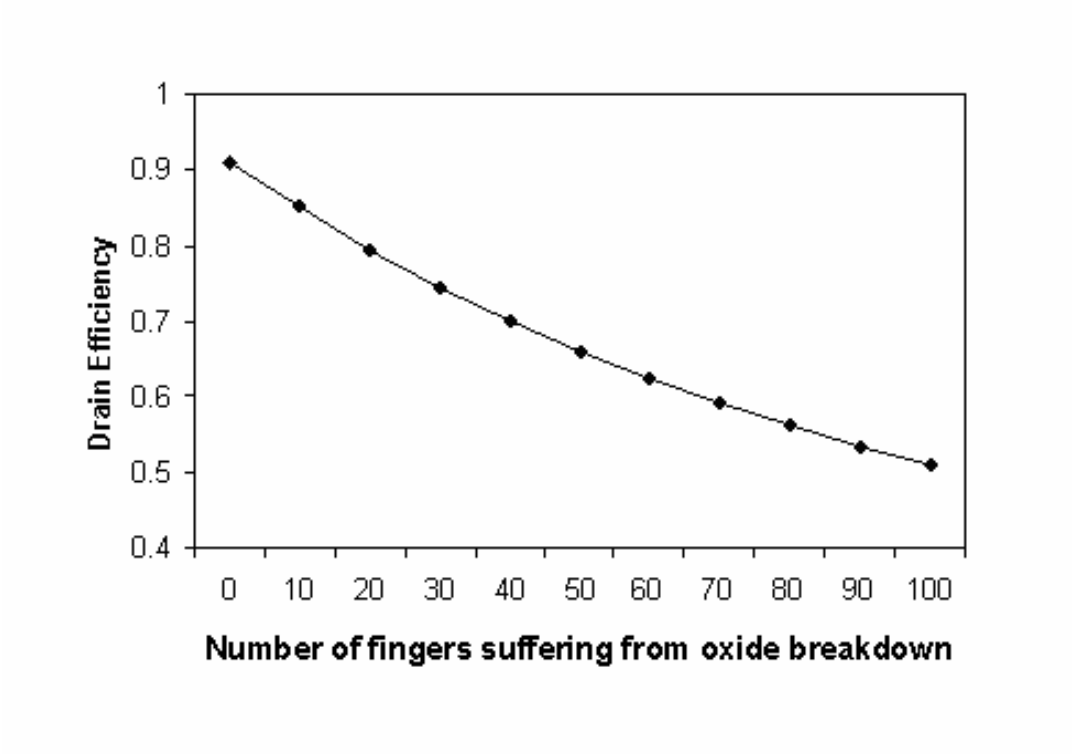
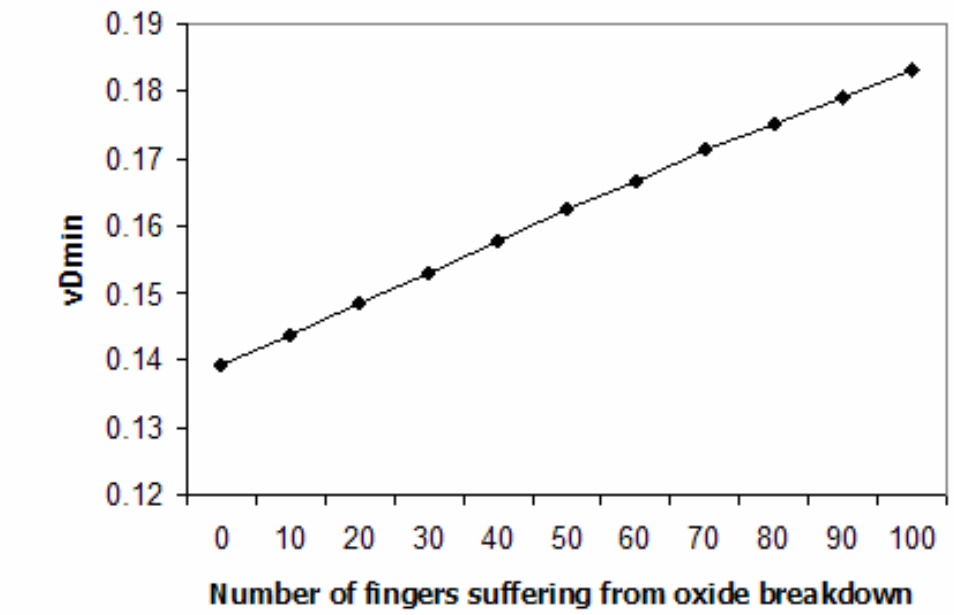


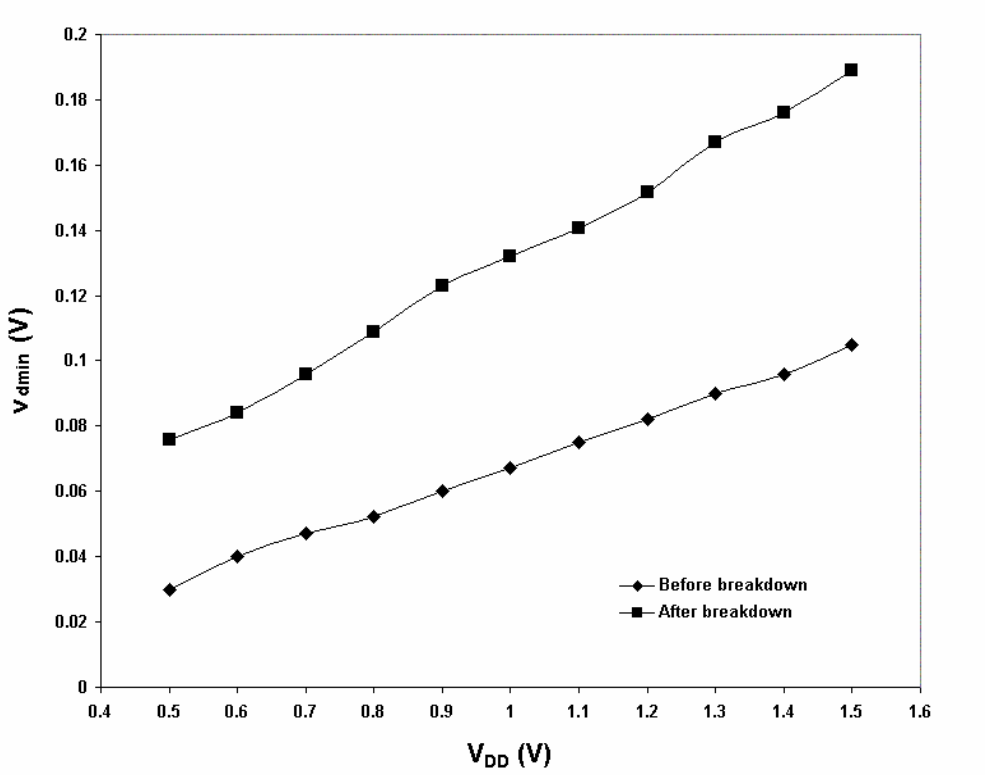
Fig. 50 Drain efficiency decline versus the number of fingers suffering from oxide breakdown.

One of the main contributors to power loss in a switching mode PA takes place when the nonzero switch voltage and the nonzero switch current overlap, thereby dissipating power through the transistor. As noted in [72], as technology scales down, the "on" resistance across the transistor tends to become a greater problem. In Fig. 51(a), the minimum voltage across the transistor when the transistor is in its conducting stage is displayed versus various values of degraded fingers. As can be noted from the figure, $V_{d\min}$ increases dramatically with an increase in oxide breakdown, thereby causing more power to be dissipated through the transistor. Fig. 51(b) shows the minimum drain voltage across the transistor for various supply voltages. One

can also take note that the drain current increases severely in direct proportion to how many fingers have been degraded. Fig. 52 shows a drain current transient plot of a fresh transistor compared to that of on suffering from 100 degraded fingers. From the figure, it can be found that close to a 3 mA difference exists between the drain current of the fresh transistor in comparison to that of the degraded transistor for the entire "on" state. Fig. 53(a) displays how an increase in the number of fingers affected by oxide breakdown leads to an increase in the degradation of the output power, whereas Fig. 53(b) shows output power consistently decreases at different supply voltages.



(a)



(b)

Fig. 51 Minimum drain voltage (v_D during the "on" state) versus (a) number of degraded fingers, and (b) power supply.

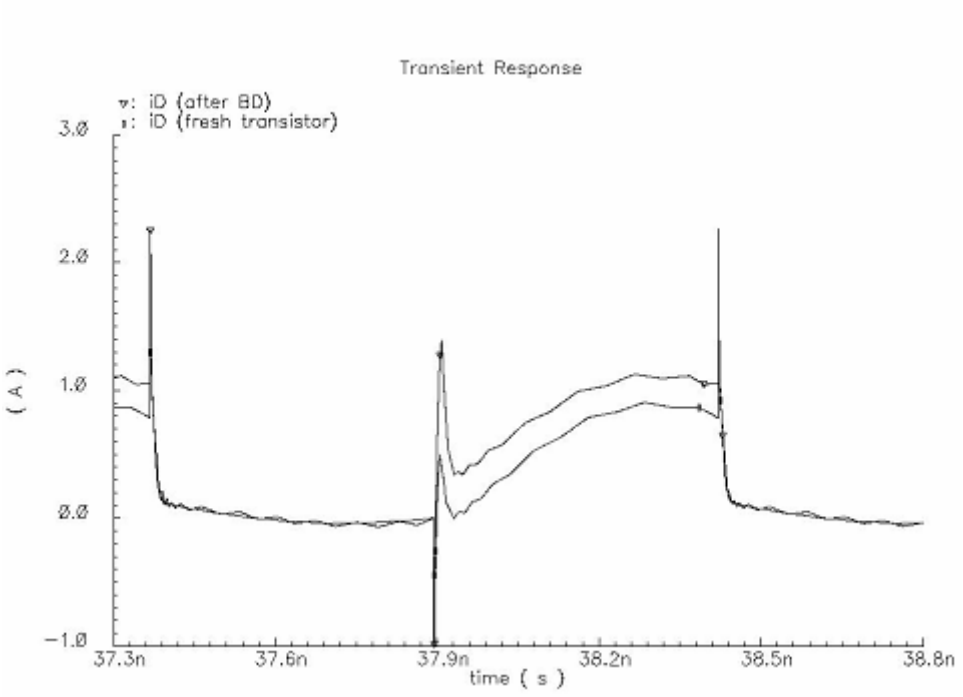
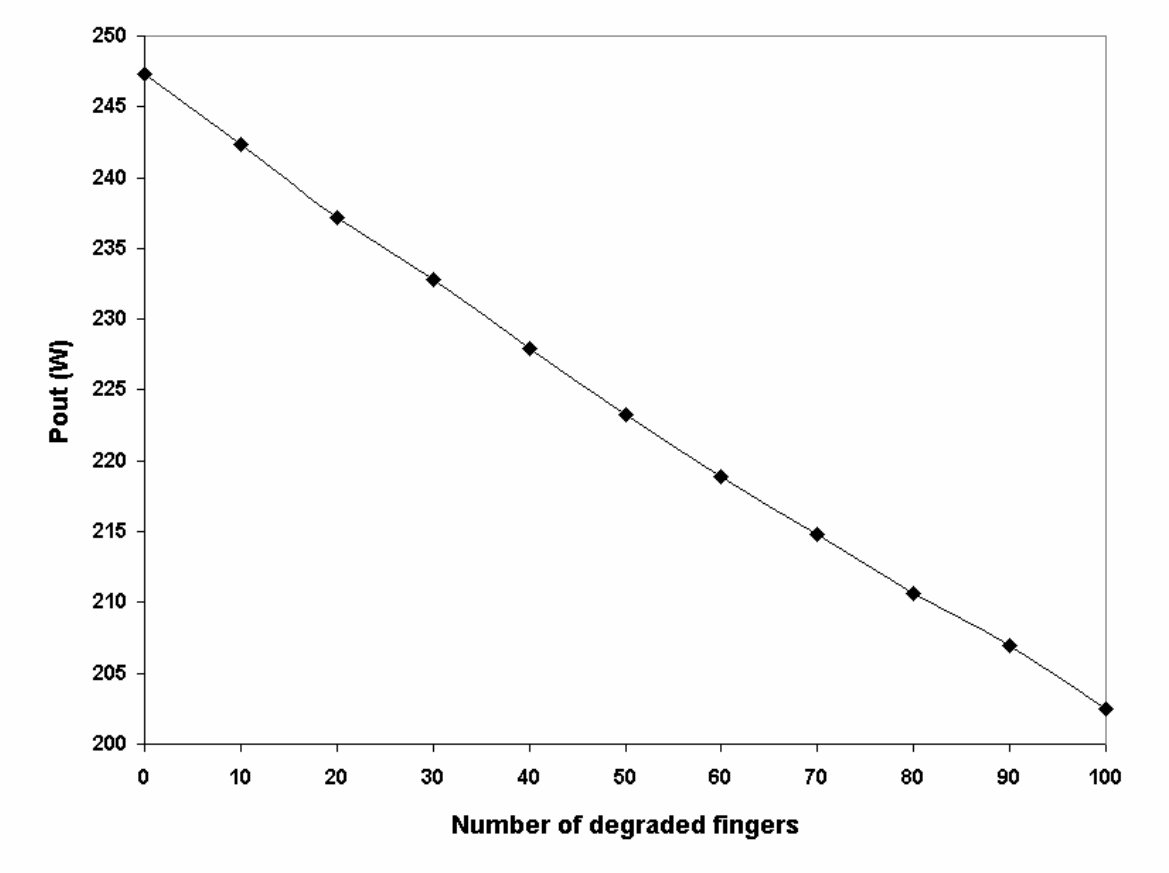
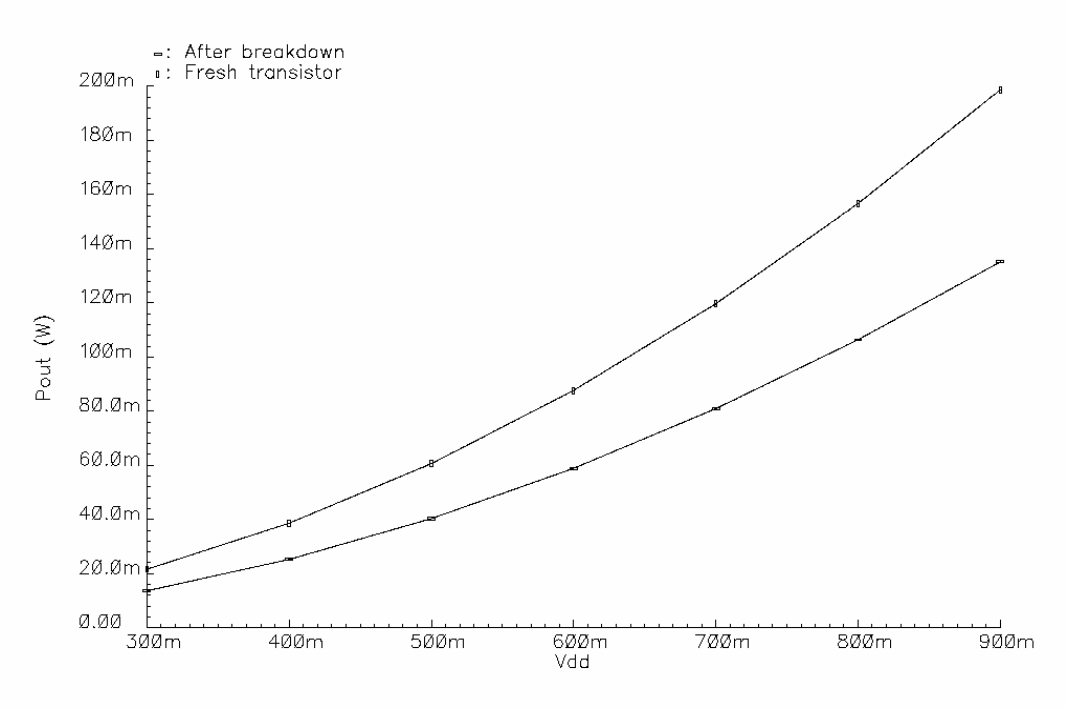


Fig. 52 Drain current from a fresh transistor versus that of a transistor suffering from 100 degraded fingers.


250
245
240
235
230
225
220
215
210
205
200
Pout (W)
0
10
20
30
40
50
60
70
80
90
100
Number of degraded fingers

(a)



(b)

Fig. 53 Output power versus (a) number of degraded fingers, and (b) power supply.

6.6.3 Conclusion

A new circuit model was proposed in order to take into account the effects oxide breakdown has on the operation of a class-E power amplifier. Analytical equations have been derived for the new circuit model to describe the operation of the circuit under various degrees of degradation.

It was shown that as the number of fingers affected by oxide breakdown increases the output power and drain efficiency of the class-E power amplifier diminishes.

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