2016

Electrical Parasitic Bandwidth Limitations of Oxide-Free Lithographic Vertical-Cavity Surface-Emitting Lasers

Xu Yang
University of Central Florida

ELECTRICAL PARASITIC BANDWIDTH LIMITATIONS OF OXIDE-FREE LITHOGRAPHIC VERTICAL-CAVITY SURFACE-EMITTING LASERS

by

XU YANG
B.S. Tsinghua University, 2008
M.Sc. Tsinghua University, 2010

A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy
in the College of Optics and Photonics
at the University of Central Florida
Orlando, Florida

Summer Term
2016

Major Professor: Dennis G. Deppe

ABSTRACT

In the past several decades, oxide-confined vertical-cavity surface-emitting lasers (VCSELs) have made success in competition with etched-post-type VCSELs and proton implanted VCSELs, and become the most popular optical sources in short-reach data communications. In the commercial oxide VCSEL technology, an oxide aperture is created inside resonant cavity in realizing good mode and current confinement, however, high electrical resistance comes along with forming the oxide aperture and the electrical parasitic bandwidth becomes the main limitation in modulation speed. Other drawbacks exist in oxide VCSELs, including difficulty in control of small aperture size, large internal stress and high thermal resistance.

To overcome the disadvantages, oxide-free lithographic VCSELs have been proposed and demonstrated. In this report, electrical bandwidths of oxide-free lithographic VCSELs have been studied along with their general lasing properties. Due to the new ways of fabricating the aperture, record low resistances have been achieved in oxide-free lithographic VCSELs with various sizes, while high slope efficiencies and high output powers have been maintained. High speed simulation has been performed showing the very low differential resistances will benefit much to the electrical parasitic bandwidths, and are expected to produce higher modulation speed. A bottom emitting structure has been proposed and analyzed, showing reduction in both mirror resistance and capacitance will further improve the modulation speed. The total 3-dB modulation bandwidth is expected to be 50-77 GHz, much higher than the bandwidth reached in existing oxide VCSELs.

Lithographic VCSELs also show superior lasing characteristics, including record low thermal resistance and record high output power. The maximum power exceeds 19 mW in a 6 μm device and over 50 % power conversion efficiency has been achieved. A maximum single mode

operation power of 5 mW has been observed from a 1 μm diameter VCSEL. High temperature stress testing has been performed showing lithographic VCSELs can operate more reliably than oxide VCSELs under extreme operating conditions. Lithographic VCSEL with low electrical resistance, single-mode operation, high efficiency, and high power will be a strong candidate as the optical source in high speed data communications, as well as other applications such as high power VCSEL arrays and optical sensing.

This report starts with a historical review on different VCSEL types in Chapter 1, and an introduction of the working principles of lithographic VCSELs in Chapter 2. The lasing characteristics of lithographic VCSELs with different sizes is shown in Chapter 3. Thermal effects and reliability issues are discussed in Chapter 4. Top- or bottom-emitting lithographic VCSELs with very low differential resistance for high speed modulation will be studied in Chapter 5.

To my parents Yong Yang and Cai Fang

ACKNOWLEDGMENT

First of all, I would like to thank to my advisor, Dr. Dennis G. Deppe for letting me join his group and doing research on the lithographic VCSELs. Without his guidance in the past six years, I wouldn't have gained so many experiences in design, fabrication and characterizing of semiconductor devices. The ways of doing scientific research and solving problems that I have learned will greatly benefit with my future research career and life.

I would also like to thank my committee members, Dr. Sasan Fathpour, Dr. Shin-Tson Wu, and Dr. Xun Gong, for their discussion and advice with great patience during the candidacy exam, proposal exam and dissertation defense.

Many thanks to all the group members, including former members Dr. Guowei Zhao, Dr. Sabine Freisem, Dr. Yu Zhang, Dr. Xiaohang Liu, and Yansong Zhang, and current group members, Mingxin Li, Jeremy Leshin, Jason Leshin, James Beadsworth, Nicholas Cox and Meng Xun. Guowei and Yu trained me with the device fabrication and testing skills. I enjoyed discussing and solving problems with all of you and I will remember the days we worked together.

Last but not least, I would like to thank my parents, Yong Yang and Cai Fang, who have brought me life and are always willing to give me support during difficult times. Also thanks to all my friends in Orlando for the wonderful days.

TABLE OF CONTENT

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBRIVATIONS

BCB	Benzocyclobutene
CW	Continuous Wave
DBR	Distributed Bragg Reflector
DHCBR	Depleted Heterojunction Current Blocking Region
DQE	Differential Quantum Efficiency
LPE	Liquid-Phase Epitaxy
MBE	Molecular Beam Epitaxy
PCE	Power Conversion Efficiency
RT	Room Temperature
RTA	Rapid Thermal Annealing
VCSEL	Vertical-Cavity Surface-Emitting Laser

CHAPTER 1 : INTRODUCTION

1.1 Introduction and applications of VCSELs

Vertical-cavity surface-emitting lasers (VCSELs) have been studied and developed for decades since the concept was firstly proposed in 1978, and they are one of the major categories optoelectronics devices manufactured today. Different from traditional edge-emitting semiconductor lasers which need to be cleaved to make light emitted from the edge, emission in VCSELs is in the vertical direction, which enables their on-wafer testing and precisely two-dimensional arrange. In addition, the circular beam shape and small divergent angle improve the coupling efficiency between lasers and optical fibers. There are other unique features of VCSELs, including low power consumption, high-speed modulation, low cost and small packaging capability, single longitudinal mode operation, and continuous wavelength tuning with electromechanical system.[1] Finally, VCSELs can be manufactured on a small wafer with high volume density and low cost, making them ideal for mass production. The cumulative sales of VCSELs during the past 20 years are estimated to have been about 1 billion units [2].

VCSELs are now widely used in high speed data communications, high power laser systems and optical sensing [3-5]. In their major application, data communications, VCSELs with modulation speed ranging from 1 to 30 Gb/s are placed in a fiber optic transceiver. The data is transformed into optical signals, and are transmitted between routers, switches, or storage area network servers. There are other applications such as biological tissue analysis, illumination source for optical mouse and cell phone thumb trackpads, chip scale atomic clock and laser printers. [6]

1.2 Historical review of the VCSEL structure

The VCSEL structure designs have been keeping revolving ever since its invention. Typically, VCSEL have an optical resonant cavity of a multiple of half-wavelength thickness which contains several quantum wells as the active region, enclosed by two distributed Bragg reflector (DBR) mirrors with high reflectivity. The quantum wells are placed at the antinodes of the standing-wave optical field. The top and bottom mirrors usually have a reflectivity larger than 98% to ensure a low threshold. Several major historical structures, Iga-type, etched-post-type, proton-implantation-type and oxide-confined-type VCSELs will be discussed next in Chapter 1. Different from the four historical structures, the major content of this report, non-oxide all-lithographic VCSELs, will be introduced and studied in the next a few chapters.

VCSEL was first proposed and demonstrated in 1979 by Soda, Iga, Kitahara and Suematsu [7] (Figure 1-1(a)). The first VCSEL was grown by liquid-phase epitaxy (LPE) technique using GaInAsP/InP material system. It was driven with 400 ns current pulse worked at a temperature of 77K, with a threshold current density J_{th} of $11kA/cm^2$. An optical output power of 7 mW was obtained.

The primary concern in VCSEL design is to have the carrier and photons well-confined in the cavity. The first VCSEL only used a full planar ring electrode structure (Figure 1-1). The current was easily spread out other than focus into the active region, so the lateral carrier confinement was poor, resulting in the heavy loss of injection current. The structure also did not provide good optical confinement in the lateral direction. In addition to that, the optical field got heavy loss in the metal/dielectric mirror, which results in a low efficiency.

There were further works from this group, including the first VCSEL arrays [8], single devices with thresholds $I_{th} = 4.5mA$ (77K, CW) and 6mA (300K, pulsed) [9], and the first VCSEL working in CW at room temperature [10]. However, due to the poor current and optical confinement, the differential quantum efficiency and the output power were limited (η=9.3% and max power=1.6 mW for CW under room temperature).

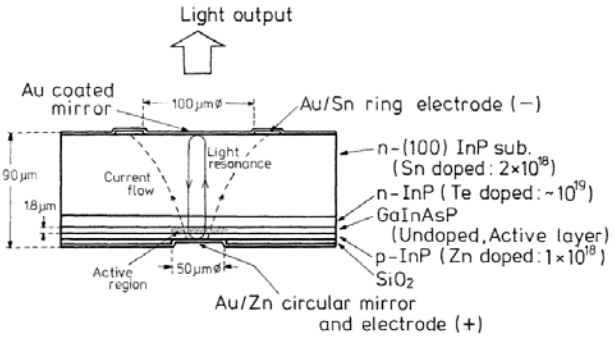


Figure 1-1 Structure of the first VCSEL structures designed by Iga [7]

The structure of etched-post-type VCSELs is illustrated in Figure 1-2. In their process, p metal squares were deposited on the surface using photolithography firstly. Then with the metal squares working as an etch mask, the top DBR mirror were etched off through reactive-ion etching. The etching stopped right above the active layer. The optical confinement was made by index guiding, due to the refractive index between the mesa and air, and the electrical confinement was achieved by the geometry of the etched mesa [11]. Typically, VCSELs with this structure can have low thresholds (190μA, pulsed) [12], because the mesa can be etched into very small size (~5μm), but the optical mode of the emission is multiple, due to the waveguide effect of the large index step between semiconductor mesa and air. The main drawbacks is the strong scattering loss due to the roughness of the etched surface, making a low differential quantum efficiency (4-5%) and a low maximum CW output power (140μW). [11]

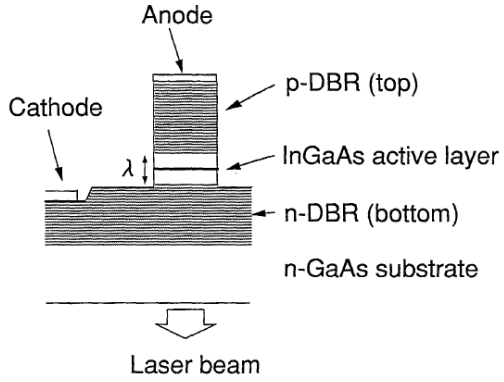


Figure 1-2 Illustration of the etched-post-type VCSELs [11]

The proton implanted VCSEL, illustrated in Figure 1-3, is fabricated by the implantation of the proton ions into the upper DBRs. The implantation creates defects in the crystal and making semiconductor semi-insulating, which enable the confinement of the current [13]. Optical mode confinement in this device is the thermal lensing effect and gain-guide, which are not very effective ways, and thus will increase the optical loss and decrease the differential quantum efficiency. Also because of the large-sized device, normally larger than 10 μm in diameter, the proton implanted VCSELs have higher thresholds, typically greater than 1 mA.

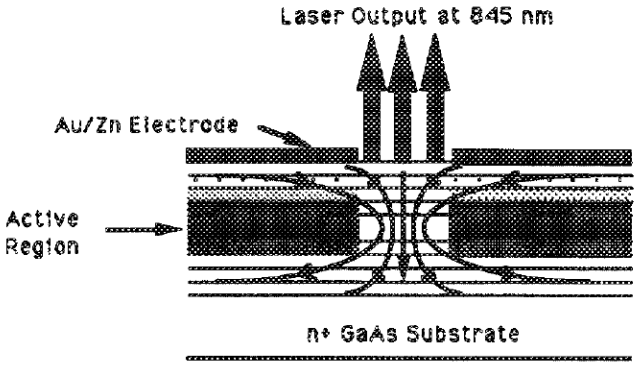


Figure 1-3 Structure of the proton implanted VCSELs [12]

The VCSEL performance was greatly improved by introduce of the method by using a thin oxide aperture buried inside an epitaxial structure, showing in Figure 1-4 [14]. The devices were fabricated by first defining 30- or 60-μm-diameter dots on p-side GaAs surface by photolithography and selective etching. After removing the photoresist from the GaAs mesas, the exposed AlAs layer is oxidized in a furnace at 475°C by reaction with water supplied by a flow of nitrogen bubbled through de-ionized water heated to a temperature of 95°C [14]. Because the oxide layer has high electrical resistance, current will flow through the oxide-defined aperture region, giving good electrical confinement. Also because of the step of refractive index between the AlAs and Al_xO_y, the photons will be confined inside the aperture, giving good optical confinement. This configuration will give a very low threshold current, which can be as low as 8.7 μA for a 3-μm device, corresponding to a threshold current density of $97A/cm^2$ [15], and a high wall plug efficiency ~50%. It is the most popular design and dominate the existing commercial VCSEL technologies.

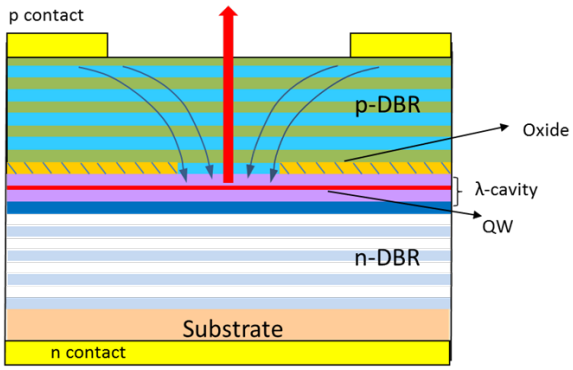


Figure 1-4 Structure of the oxide-confined VCSELs

Although the oxide-confined VCSELs show superior performance over the etched-post type and the proton-implanted type, they contain several drawbacks. First, the size of the aperture

formed in the oxidization process cannot be accurately controlled, especially when making small-sized device on a large wafer. Second, because of the difference in the thermal expansion coefficient between the oxide and the semiconductor, the oxide-aperture will creates stress in the device and reduce its reliability. Third, the oxide material Al_xO_y has a low thermal conductivity of 0.7 W/mK, while GaAs and AlAs have thermal conductivity of ~50 W/mK [16]. The low thermal conductivity will limit the spreading of the heat generated by the working device and reduce the output power and modulation bandwidth. In order to further improve the performance of VCSELs, a new design is required.

1.3 Requirement for high speed communication application

VCSELs are mainly used for high speed data communications. There are Ethernet standards proposed to reach data transmission speeds of 40 Gb/s and 100 Gb/s, which require for optical source with higher modulation capability. The requirements include several aspects. First, VCSELs devices need to show good lasing performance, including low threshold and low operating voltage, which will produce low power consumption, as well as high output photon density, giving high intrinsic modulation bandwidth. Second, small sized devices are preferred since they have less capacitance and higher bias current density. Third, single-transverse mode VCSELs will offer advantages when compared with multi-mode VCSELs, since all the driven current will be injected only into the single mode, lower operating current is required gives lower power consumption. Finally, high reliable VCSELs are needed to operate for 10 years at ambient temperature from 0 to 70 °C. These are key issues when considering high speed application, and will be discussed in the following chapters.

1.4 Content of this work

In this work, the working principles of all-epitaxial lithographically-defined VCSELs will be discussed in Chapter 2. The lasing characteristics of lithographic VCSELs with different sizes will be shown in Chapter 3. Thermal effects and reliability issues will be discussed in Chapter 4, including VCSELs working under extreme operating conditions. Electrical parasitic bandwidth of lithographic VCSELs with very low differential resistance will be studied in Chapter 5.

CHAPTER 2 : DESIGN OF OXIDE-FREE LITHOGRAPHIC VCSELs

2.1 Introduction to oxide-free lithographic VCSELs

VCSELs based on oxide-confinement have shown good characteristics in threshold, output power, slope efficiency, and have been widely manufactured. Despite their success, oxide-confined VCSELs have limitations in aperture size control, thermal expansion and high thermal resistance caused by the oxide layer. To overcome these disadvantages coming from the oxide-confined structures, oxide-free lithographically-defined VCSELs have been demonstrated [17] [18]. The key of this approach is to replace the oxide layer by an intra-cavity phase-shifting mesa to eliminate strain and provide controlled device size while keeping a low optical loss. Because the oxide layer served as a heat barrier, removal of this layer will help the heat spreading in the vertical direction and thus reduce the thermal resistance. Internal stress comes with the lattice mismatch between oxide and semiconductor can be eliminated. Also the size of the device can be accurately controlled through photolithography.

The schematic structure is illustrated in Figure 2-1. The growth of the all-epitaxial structure starts with the n-type DBR mirrors and multiple numbers of quantum wells inside the 1-λ cavity spacer. The whole structure needs two growth steps and a process is required in between. The first growth step stops at the first quarter wavelength of the top p-type DBR mirrors. Then then wafer is taken out of the MBE system and the phase shifting mesas with sizes varied from 1 μm to 20 μm are defined by photolithography and formed through wet etching. Next, the sample is reloaded into MBE system and then top p-type DBR mirrors are grown. The metal contacts on the p-side are then formed by thermal evaporation and a lift-off process. After isolation of each individual

devices through photolithography and wet etching, the n-side metal contacts are then deposited. Finally, the contacts are annealed at the Rapid Thermal Annealing (RTA) system to make metal contacts with low electrical resistance.

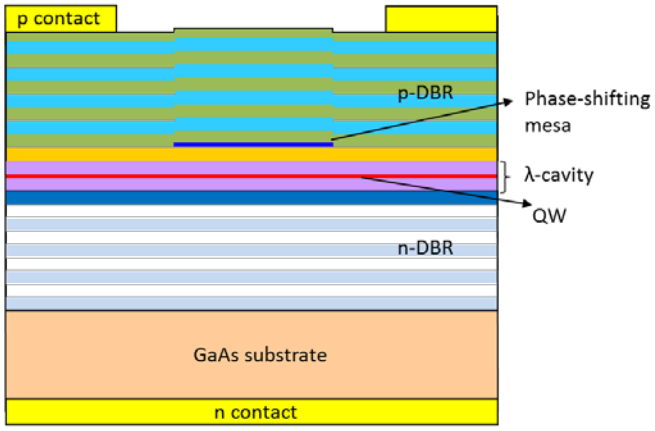


Figure 2-1 Schematic illustration of an all-epitaxial lithographically-defined VCSEL

2.2 Confinement in lithographic VCSELs

The optical confinement in all lithographic VCSELs is illustrated in Figure 2-2 [19], and it has been achieved through a resonant wavelength shift due to phase-shifting mesas, which can be analyzed as follows. The diameter of the mesa is W and the optical mode size is W_0. Due to the etched mesa, there would be a difference in the cavity length which is L at the on-mesa region (r<W/2) and L' at the off-mesa region (r>W/2). $\varepsilon(0) = \varepsilon_r(0)\varepsilon_0$, where ε_0 is the permittivity of free space. If the resonance condition is met and standing wave is formed in an F-P cavity, only discrete value of the vertical component of the wave vectors are allowed:

$$k_{z,A} = \pi m_z / (\sqrt{\varepsilon_r(0)} L) \qquad (2.1)$$

for the on-mesa region, and

$$k_{z,WG} = \pi m_z / (\sqrt{\varepsilon_r(0)} L') \quad (2.\ 2)$$

for the off-mesa region, where $m_z = 1,2,3$ ....

The mesa height will result in a difference from L to L', and thus make the resonance slightly shifted in the two different regions. The eigenmodes in a waveguide with cylindrical symmetry can be described by the Bessel function, so the transverse component of the wave vector can be described as:

$$k_{\rho,A} = 4.810 / (\sqrt{\varepsilon_r(0)} \omega_0) \quad (2.\ 3)$$

where the factor 4.810 comes from the lowest order Bessel function.

From Maxwell's equations, the wave vector in the vacuum:

$$k_0 = \frac{\omega}{c} = \sqrt{\frac{4.810^2}{\varepsilon_r(0)\omega_0^{\ 2}} + k_{z,A}^{\ 2}} = \sqrt{k_{\rho,WG}^{\ 2} + k_{z,WG}^{\ 2}} \quad (2.\ 4)$$

Since L>L' and $k_{z,A} > k_{z,WG}$, for equivalent m_z values, there will always exist a range of ω_0, where $k_{\rho,WG}$ is imaginary. Under such conditions, the electrical field in the off-mesa region becomes evanescent and the optical mode is confined in the on-mesa region. [19] Thus, the condition for the lowest order of the confined eigenmode can be given as:

$$\omega_{0,confined} \geq \frac{4.810}{\sqrt{\varepsilon_r(0)}} \frac{1}{\sqrt{k_{z,WG}^{\ 2} - k_{z,A}^{\ 2}}} \quad (2.\ 5)$$

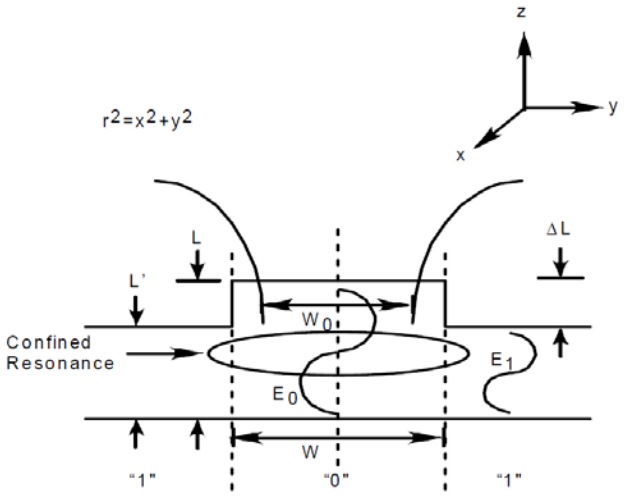


Figure 2-2 Mode confine mechanism in lithographic VCSELs [19]

Through this analysis, a higher mesa profile will give more resonance shift, and will make the optical mode more confined in the mesa area, however, there would be more scattering loss due to the mode mismatch between the two regions. On the other hand, if the mesa height is too thin, scattering loss due to the mode mismatch will be reduced, however, optical mode will get less confined and the lasing efficiency will be degraded. In general, a phase-shifting mesa designed with proper height, as well as a smooth regrowth surface and a uniform shape are all required to reduce the scattering loss and ensure good device performance.

The current confinement has been achieved through a proprietary scheme, and can be examined by measuring the current vs. voltage characteristics of two test structures, one of which has a planar region with on-mesa structure, and the other has a planar region with off-mesa structure. Isolated from other devices through photolithography and wet etching, the two test structures have 120 μm × 80 μm in dimension. Figure 2-3 shows the current versus voltage characteristics measured either through (a) planar on-mesa region, or (b) planar off-mesa region. The results show that the forward voltage is increased from ~1.3 V in region (a) to 3.3 V in region

(b). The operating voltage of the lithographic VCSEL is typically below 3 V, so the difference in forward voltage is sufficient to make current confinement in the active region.

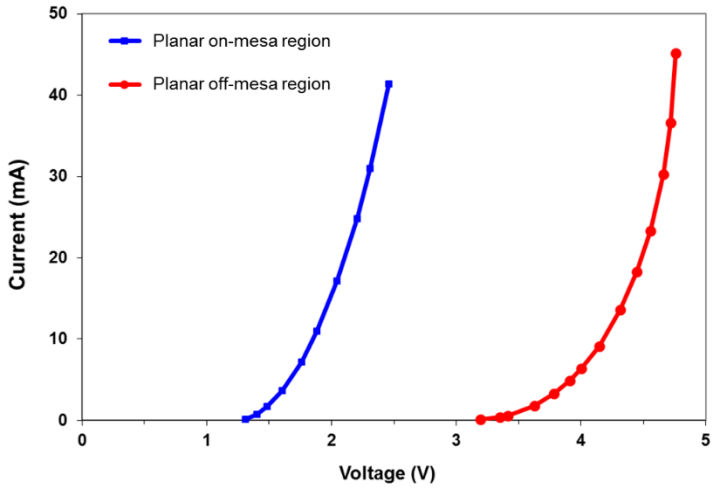


Figure 2-3 Current versus voltage characteristics measured either through a) planar on-mesa region, or b) planar off-mesa region

2.3 DBR mirror reflectivity and doping design

The structure of a VCSEL contains two distributed Bragg reflector (DBR) mirrors with high reflectivity to ensure low threshold. The design of the DBR mirrors will greatly affect the electrical resistance and optical efficiency of the VCSEL. The basic structure of a DBR mirror contains periodical structure formed by two materials with different refractive index. Consider light is incident from a material with a refractive index of n_1, reflected by a DBR mirror formed by two materials with refractive indices of n_2 and n_3, and passing through to a material with refractive index of n_4. If each layer is a quarter-wave film ($n_2h_2 = n_3h_3 = \lambda_0 / 4$, where λ_0 is the wavelength in vacuum) and the DBR contains N periodical structures, the reflectivity at normal incidence can be expressed by [20]:

$$R_{2N} = \left(\frac{1 - \frac{n_4}{n_1}\left(\frac{n_2}{n_3}\right)^{2N}}{1 + \frac{n_4}{n_1}\left(\frac{n_2}{n_3}\right)^{2N}} \right)^2 \qquad (2.\ 6)$$

Although it is easy to get a high reflectivity (>99.99%) using binary AlAs/GaAs, it cannot be directly applied to VCSEL owing to the following reasons. Generally, it requires a large refractive index contrast of the two materials, or more mirror pairs, to get a high reflectivity, however, it will introduce high electrical resistance comes from the energy barriers at the heterointerfaces, leading to an operating voltage that can be as high as 5V [21]. Although lower resistance can be obtained by using heavily doped DBR mirrors, it does so at the penalty of adding free-carrier absorption, and thus will increase threshold current and degrade efficiency and output power. In summary, there is always a tradeoff between optical loss and electrical resistance.

In order to reduce resistance in DBR mirror and operating voltage of VCSELs, while keeping a low optical loss, several techniques have been utilized, including putting graded layers or delta doping at heterointerfaces, as well as using selective doping depending on nodes or antinodes of optical field. The continuous grading of the heterointerfaces in the DBR mirror eliminated the energy-band discontinuities, thus improving carrier transport and result in a reduction in the series resistance and threshold voltage.[22] The threshold voltage had been greatly reduced from 4-5V in VCSELs without grading layers, to 2.1-3.4 V in various-sized devices with graded layers[23] [24]. Another example with continuous grading layers gave 1.47 V threshold voltage [25].

The purpose of adding grading layers is to flatten the band discontinuity. From Poisson's law, constant space charge creates parabolic band bending, so by compensating a parabolic grade

with constant space-charge regions, a flat valence band can be theoretically generated. Based on parabolic grading layers, threshold voltage <2V has been achieved by M.G. Peters et al [21][26] and E.F. Shubert et al[27].

Another solution of reducing the resistance is using delta-doping at the heterointerfaces of p-side DBR mirror [28]. Due to the band gap difference in the band structure, AlAs has a lower valence band-edge than GaAs. By putting a very thin heavily doping layer at the AlAs/GaAs heterointerfaces, the valence band-edge of AlAs is shifted upward, thus depletion of carriers at the heterointerfaces are relaxed and local resistance can be reduced. Tunneling current is also increased due to the reduced potential barrier. A DBR mirror with heavy doping everywhere will not work because of the high free-carrier absorption, however, in the case of delta-doping, since the carrier density is only locally increased, excess free carrier absorption can be minimal [29].

Referring to the methods of flattening band discontinuity and reducing resistance of the p-side DBR mirror, a simulation based on solving 1-D Poisson equation is performed and described as follows. First, we consider a simple heterointerface at x=1000 Å between GaAs and AlAs both with $5 \times 10^{17} cm^{-3}$ p-type doping (Figure 2-5 a) b)). A potential barrier exist at the interface and a region with depleted carrier density will produce high resistance. Second, grading layers with 2% step increment in Al content in $Al_xGa_{1-x}As$ and 5Å thickness for each layer have been inserted at the heterointerface (Figure 2-5 c) d)). The potential barrier drops significantly. Next, by adding a delta-doping spike with donors at the GaAs/2%AlGaAs interface where a peak appears, and a delta-doping spike with acceptors at the 98%AlGaAs/AlAs interface where a valley exist, the diagram of the valence band gets more flattened and the carriers distribute more evenly (Figure 2-5 e) f)). The delta doping is a monolayer with a doping level of $5 \times 10^{19} cm^{-3}$.Finally, the results

have been improved by increasing the doping levels from $5 \times 10^{17} cm^{-3}$ to $8 \times 10^{17} cm^{-3}$ in the grading layers (Figure 2-5 g) h)). In conclusion, the band discontinuity at the heterointerface between GaAs and AlAs has been greatly eliminated, leading to a carrier distribution without depletion. In DBR designs, graded layers and delta doping layers will be placed wherever high band discontinuity exists, together with selective doping to keep low optical loss and low electrical resistance simultaneously.

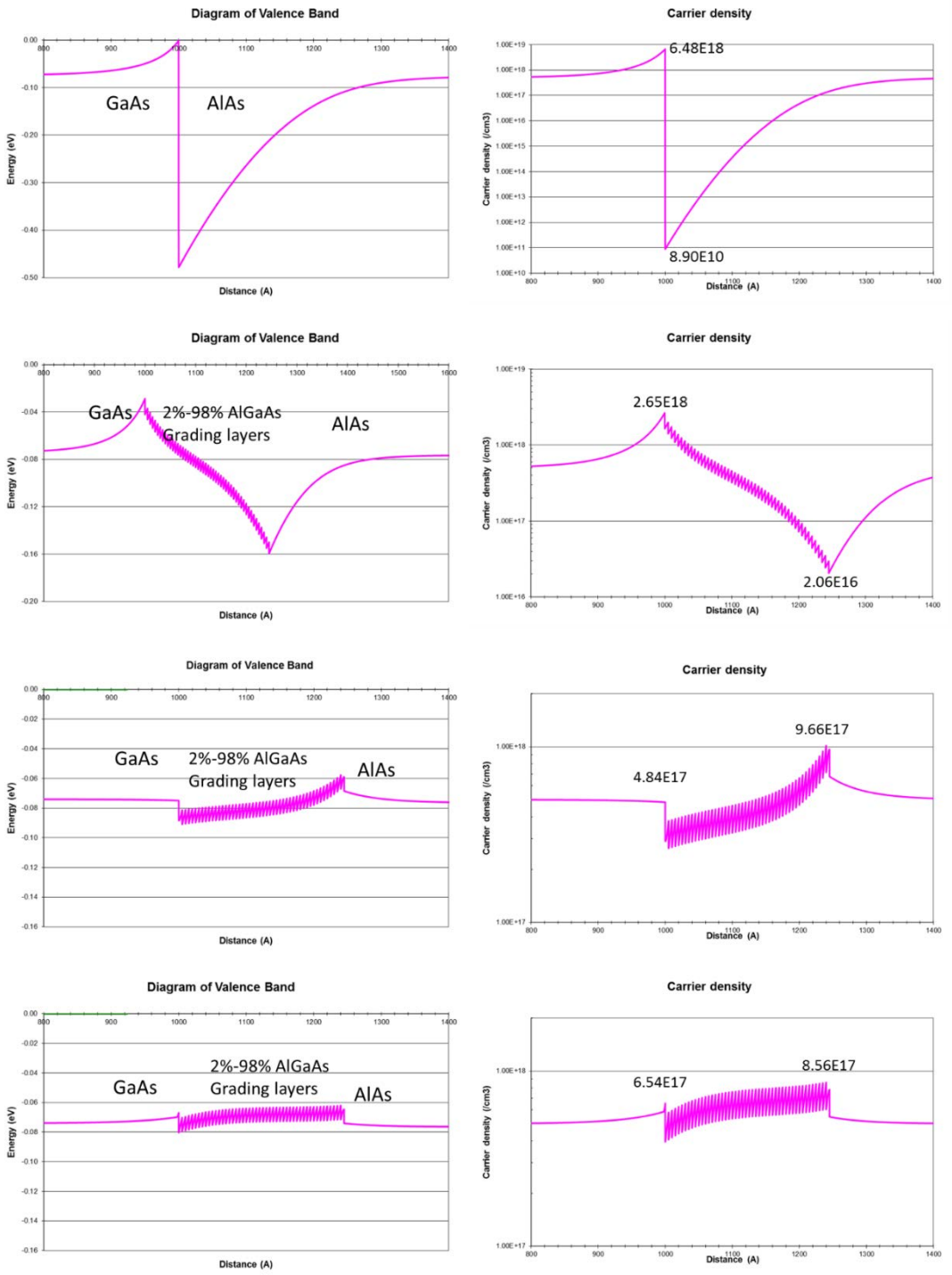


Figure 2-4 Diagram of the valence band and carrier density distribution of: a) b) GaAs/AlAs, c) d) with 245Å grading layers, e) f) with delta doping and grading layers, g) h) increased doping in grading layers

The reflectivity, transmission, and absorption can be simulated through Maxwell's Equations and transfer matrix. Here is an example of a DBR mirror designed with a center wavelength of 985 nm. Composed with GaAs/AlAs as the high/low refractive index material, the DBR mirror contains $Al_xGa_{1-x}As$ grading layers between GaAs and AlAs with a total thickness of 250 Å. The optical loss due to the doped carriers have also been taken into consideration. The reflectivity vs. wavelength is shown in Figure 2-6. It gives a peak reflectivity R=99.920%, a transmission T= 0.012% and an absorption a transmission A= 0.068% at 985nm for the n mirror, and a peak reflectivity R=98.565%, a transmission T= 1.196% and an absorption a transmission A= 0.240% for the p mirror. Figure 2-7 gives the total reflectivity of the cavity, showing a cavity resonance at 985 nm.

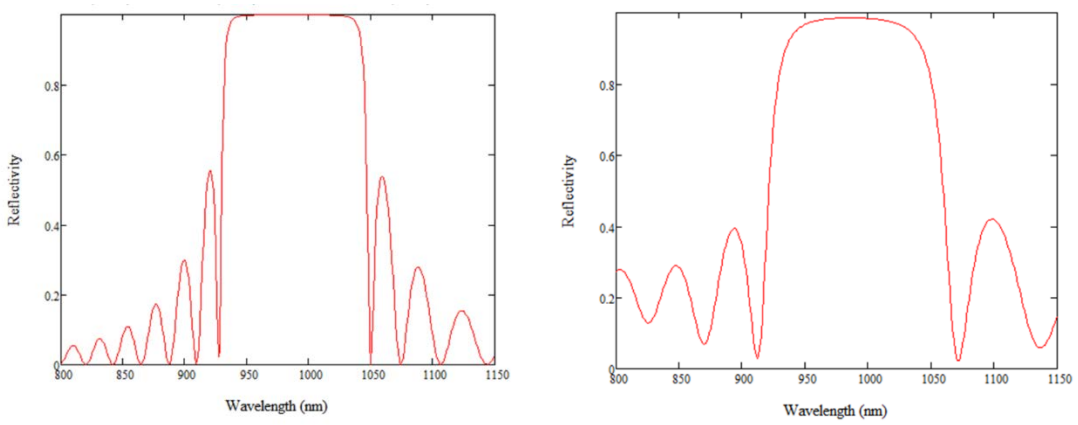


Figure 2-5 Reflectivity as a function of wavelength of n (left) and p-DBR (right) mirror designed at 985nm

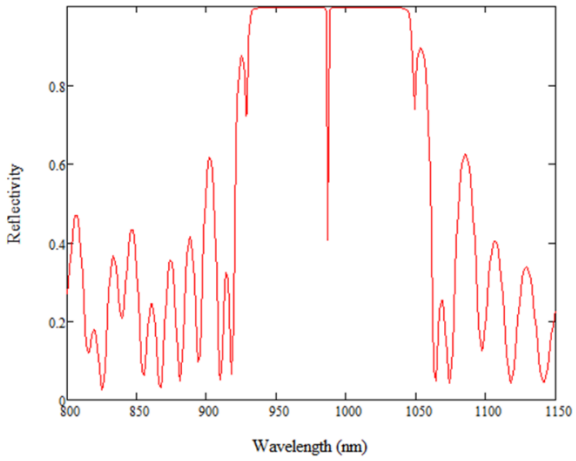


Figure 2-6 Reflectivity of a VCSEL cavity designed at 985nm.

2.4 Summary

In this chapter, all-epitaxial lithographically-defined VCSELs have been introduced. By replacing the oxide layer with an intra-cavity phase-shifting mesa, lithographic VCSELs are designed to overcome the disadvantages in oxide-confined VCSELs. Design principles including mesa height, DBR mirror reflectivity and electrical resistance, have been analyzed. To ensure the high efficiency, low series resistance and operating voltage, DBR mirrors should be well designed, including selective doping, graded layers and delta doping to ensure high electrical conductivity while keeping a low optical loss.

CHAPTER 3 : LITHOGRAPHIC VCSELS WITH HIGH EFFICIENCY, HIGH POWER AND SCALING PROPERTIES

Based on the design principles discussed in Chapter 2, lithographic VCSELs have been grown in MBE and processed. Lasing characteristics will be presented in this chapter, including record high output power and over 50% of power conversion efficiency in single devices. The high power and power conversion efficiency are mostly due to the low electrical resistance, low junction temperature and high crystal quality in the all-epitaxial lithographically-defined process.

In the applications such as long-distance communications, optical sensing and VCSEL arrays, a stable single-transverse mode of the laser source can be a crucial aspect, which can be achieved through making small VCSELs, because of the increased mode spacing in small devices. While in oxide VCSELs, the very small oxide aperture cannot be uniformly formed, since the oxidation rate is highly related to the Al content. While in lithographic VCSELs, problems can be solved in process base on photolithography and wet etching. Device with size 1-3 μm can be produced repeatedly. Single mode operation has been realized in lithographic VCSELs sized below 2.5 μm.

3.1 Experimental results of 6 and 4 μm VCSEL devices

The structures of 975nm lithographic VCSELs have been described in Chapter 2, using internal mesas instead of oxide apertures for confinement. The epitaxial growth has been optimized, and the doping profiles and reflectivity of both mirrors have been well-designed to produce high optical quality and low electrical resistance. By removing the oxide and using AlAs in both upper and lower mirrors, thermal resistance has be greatly reduced. Cavity resonance and quantum well

peak emission wavelength have been well-designed to ensure good align in elevated operating temperature. The processing of device fabrication has also been optimized, including metal contact pattern design, UV photolithography, metal deposition and lift-off, device isolation using wet-etching, and rapid thermal annealing. The devices are mounted on a probe station for characterizing.

Figure 3-1 shows a 6 μm lithographic VCSEL operating at continuous-wave (CW) under room temperature. The maximum power exceeds 19 mW under a bias of 30 mA, and to our knowledge is the record high value for CW/RT operated VCSELs with comparable sizes. Other lasing characteristics including a maximum differential quantum efficiency of 79 %, a differential series resistance of 71 Ω, a maximum power conversion efficiency (PCE) over 50%, match or exceed the most commercial available and laboratory demonstrated oxide VCSELs [30].

Figure 3-2 shows the lasing characteristics of a 4 μm lithographic VCSEL, including a maximum power conversion efficiency exceed 50 %, a differential quantum efficiency close to 80 %, a maximum output power more than 13 mW and a differential resistance of 111 Ω [30]. In addition to the optimized growth and processing steps, the high output and power conversion efficiency are due to the high efficiency, low resistance and low junction temperature benefiting from lithographic design, which be discussed in the next a few chapters.

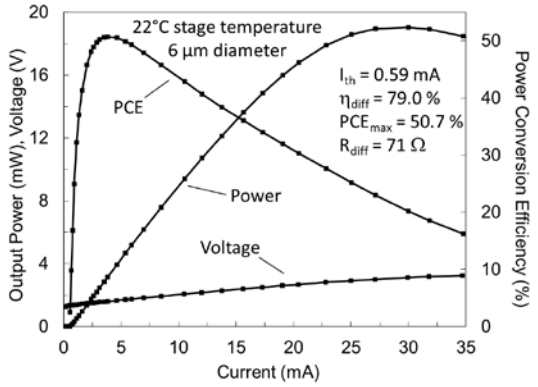


Figure 3-1 Voltage, power and PCE vs. current of a 6 µm lithographic VCSEL under CW/RT operation.

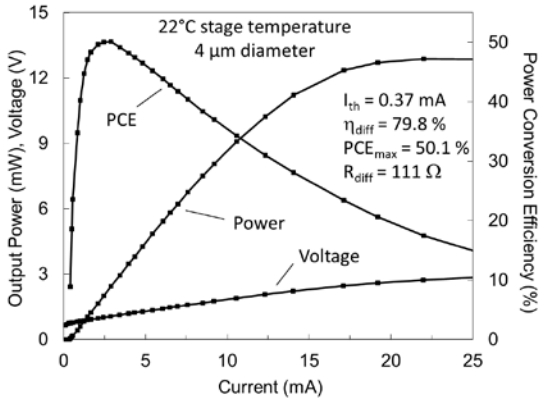


Figure 3-2 Voltage, power and PCE vs. current of a 4 µm lithographic VCSEL under CW/RT operation.

3.2 Capability of making small VCSEL devices and experimental results

Oxide VCSELs have achieved great success and becomes the most available commercial VCSEL devices, however, due to the lack of control in the oxidation process, they have difficulty in achieving high uniformity for small sizes. Slight variation in Al content will make great difference in oxidization rate. Different from the oxide VCSEL design, device size of lithographic VCSELs can be accurately controlled into sub-micron through photolithography. Therefore, the

improved technology can enter a size regime not easily achieved through oxide VCSELs. One of the benefits of making very small VCSELs is single mode operation, as a result of the reduced size of lateral optical mode, and can be useful to applications such as optical sensing and VCSEL arrays. Other benefits including high power density, are also important in getting high intrinsic speed for high speed communications.

The lasing characteristics of lithographic VCSELs size below 3 μm will be shown in this section. Figure 3-3 shows the RT/CW lasing characteristics of a 2 μm lithographic VCSEL. With a low threshold current of 0.30 mA, and a maximum differential quantum efficiency of 73%, this device produces a 7.97 mW maximum power under 13mA injection, and a maximum wall-plug efficiency of 46%.[31]

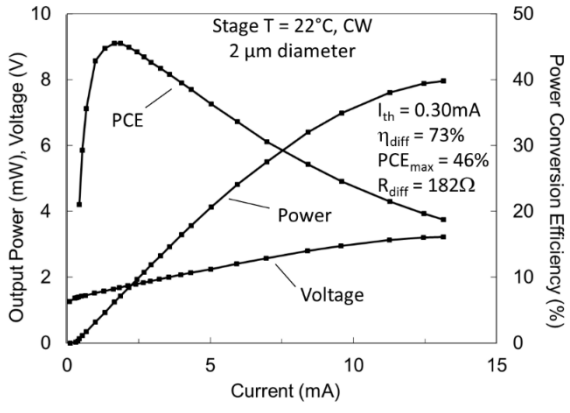


Figure 3-3 Voltage, power and PCE vs. current of a 2 μm lithographic VCSEL under CW/RT operation.

The output vs. current of small devices with size vary from 1 to 3 μm tested under CW, room temperature, are shown in Figure 3-4. The maximum powers have reached 5.00, 7.34, 7.97, 8.74, and 11.61 mW in 1, 1.5, 2, 2.5, and 3 μm devices, respectively, which to our knowledge are the highest reported in VCSELs with comparable sizes under CW/RT operation. [31]

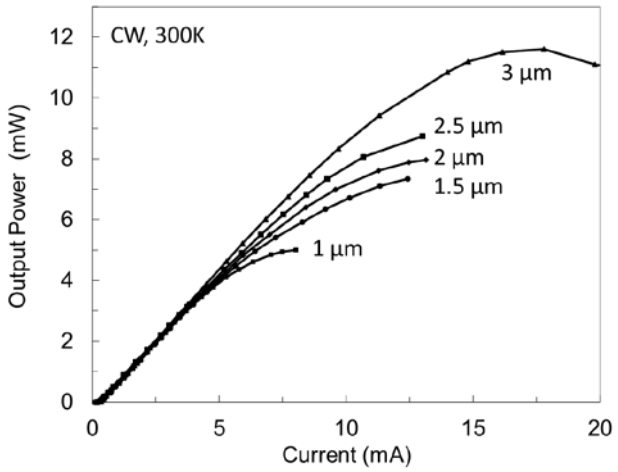


Figure 3-4 L-I curves of the 1, 1.5, 2, 2.5, 3 μm lithographic VCSELs under CW/RT operation.

3.3 Efficiency, wavelength and mode separation affected by size

In this section, lasing characteristics affected by device size, such as slope efficiency, wavelength and spectral mode separation, will be analyzed. Table 3-1 lists the lasing characteristics, including threshold currents, maximum power, differential quantum efficiency (D.Q.E.), power conversion efficiency (P.C.E.) and voltage at 10 kA/cm^2.

Table 3-1. Lasing characteristics for 1 to 6 μm lithographic VCSELs.

Device Size (μm)	I_{th} (mA)	$P_{\max}$ (mW)	D.Q.E	P.C.E.	Voltage at $10kA/cm^2$ (V)
1	0.33	5.00	79.7%	37.4%	1.273
1.5	0.31	7.34	76.8%	42.0%	1.315
2	0.30	7.97	73.4%	45.5%	1.381
2.5	0.28	8.74	79.8%	47.2%	1.410
3	0.32	11.61	76.0%	49.0%	1.413
4	0.37	12.87	79.8%	50.1%	1.490
5	0.47	15.89	78.9%	49.4%	1.520
6	0.59	19.05	79.0%	50.7%	1.551

Figure. 3-5 shows the lasing wavelength just above threshold and the differential quantum efficiency for lithographic VCSELs with different sizes. Despite of the device variation across the wafer, the slope efficiency generally increases in a smaller device, as a result of better overlapping between the optical mode and path of electrical current in smaller devices. The maximum power conversion efficiency, is 37%, 42%, 46%, 47%, and 49% for the 1, 1.5, 2, 2.5, and 3 μm devices, respectively. The lasing wavelengths just above threshold have also been recorded, showing a blue shift as the device size reduces, consistent with the more confined optical mode.[32]

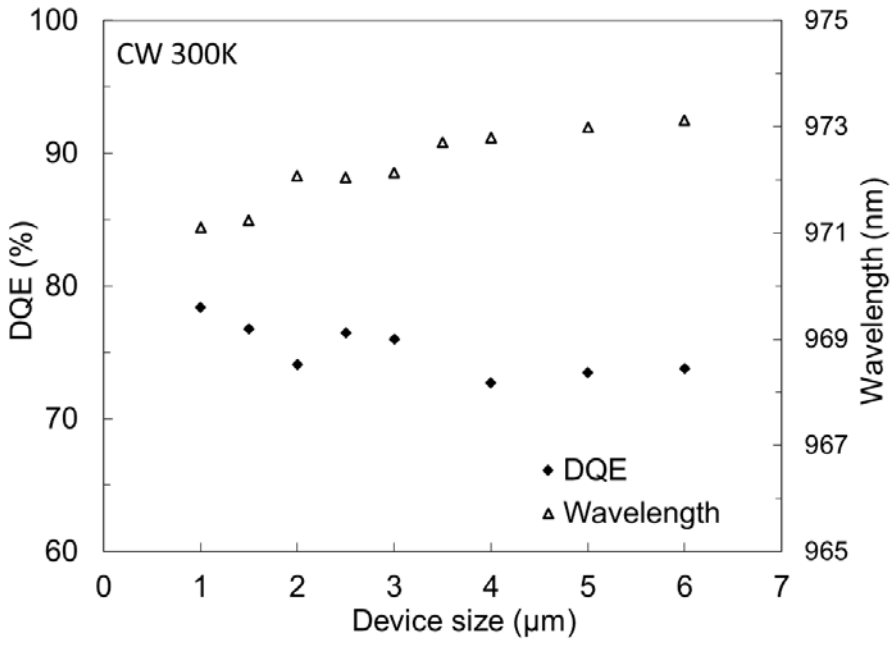


Figure 3-5 Differential quantum efficiency vs. device size and the lasing wavelength just above threshold vs. device size.

Multiple transverse modes exist in VCCELs with large size or in small VCSELs with high bias current. Mode separations between the fundamental and the second higher order for devices of different size have been plotted in Figure 3-6, showing a trend of increased separation as device becomes smaller. This is due to the increased optical confinement in the lateral direction. The

mode size is estimated to be 3.9 μm in the 1.5 μm device through an assumption of optical mode in the form of Bessel function. An abrupt step has been observed when size reduces from 3 μm to 2.5 μm, which appears to be a transverse resonance cavity effect. There is also a drop of differential quantum efficiency and a peak in wavelength for the 2 μm size relative to the other sizes in Figure 3-5. [32]

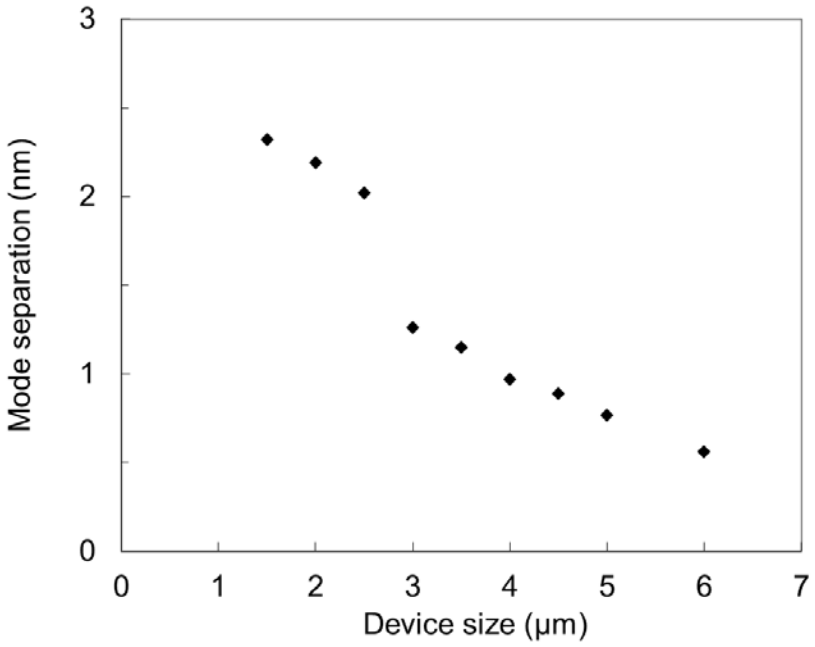


Figure 3-6 Wavelength separation of the first 2 order transverse modes for lithographic VCSELs of different size.

3.4 Single mode operation in small VCSELs

As shown in Figure 3-6, when the VCSEL size is made smaller, the spacing between different transverse modes will be increased. For a limited optical gain linewidth, only one mode will get lased and will make the device operate with single transverse mode, which is the case in device below 2.5 μm diameter. Figure 3-7 are the spectral characteristics of a 2 μm VCSEL under

different bias levels. Only single transverse mode of the lowest order with 2 polarizations have been observed under 4 mA bias current. It is already producing 3.3 mW single mode operation at 4 mA. The second order transverse mode can barely be detected at 7.0 mA, approximately 23 times of the lasing threshold. For the 1 μm device, showing in Figure 3-8, it maintains its single mode operation until thermal rollover, which corresponds to a maximum 5 mW output. The single mode operation features will enable the applications in high speed data communication with low power consumption, optical sensing and VCSEL arrays for reduced mode interfering and improved beam quality.[31]

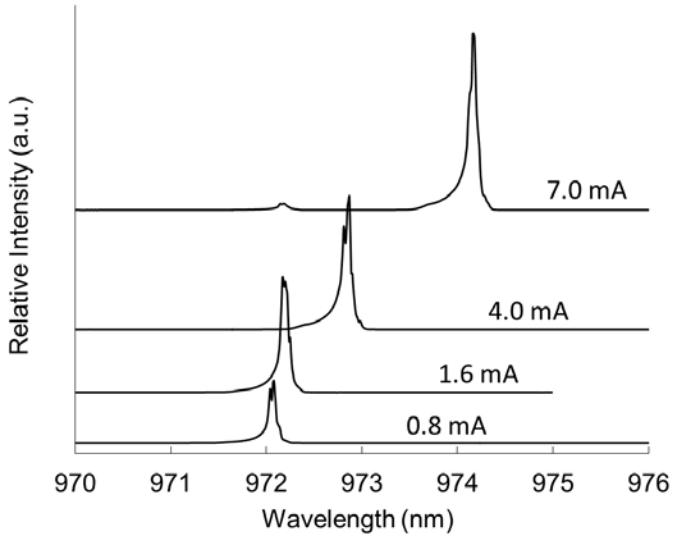


Figure 3-7 Spectra of a 2μm device, showing single transverse mode with 2 polarizations when driving is below 4.0 mA

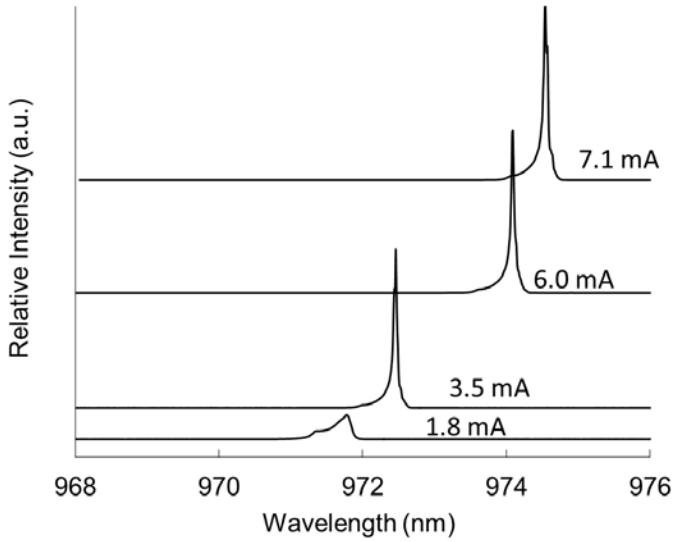


Figure 3-8 Spectra of a 1μm device, showing single transverse mode with 2 polarizations

3.5 Summary

Lithographic VCSELs with small size have been demonstrated and can produce high output power with high efficiency. Small device can be accurately defined through photolithography. Single transverse mode operation with high output power has been obtained in lithographic VCSELs with size below 2.5 μm. The high output and power conversion efficiency are due to the low operating voltage and low junction temperature benefiting from lithographic design, and will be discussed in the next chapter.

CHAPTER 4 : LITHOGRAPHIC VCSELS WITH LOW THERMAL RESISTANCE AND HIGH RELIABILITY

4.1 Introduction of thermal effects and reliability of VCSELs

Thermal effect is an important issue affecting VCSEL performance. As the driven current flows through the reflector and active region, part of the energy will be dissipated inside the device and the temperature will rise because of the ohmic heating and free carrier absorption. The output will get lower and thermal rollover will appear, and eventually make a device stop lasing.

The heating will degrade the performance of the device due to the following reasons. First, there will be a mode mismatch between gain peak and cavity resonance in a heated device. A laser device will get the largest optical gain and thus obtain a good lasing mode when the resonant wavelength of the F-P cavity matches with the peak of the gain. At an elevated temperature, due to the thermal expansion of the crystal, the resonant wavelength of the F-P cavity will shift to a longer wavelength. The peak in the gain spectrum will also shift to a longer wavelength due to the decreased bandgap energy of the quantum well, since a crystal with larger lattice constant corresponds a narrower bandgap. However, the shift speed for spectrum (~ 0.27 nm/°C) is much faster than resonant wavelength shift of the F-P cavity (~ 0.07 nm/°C). As a result, the device needs to be pumped harder to maintain the same amount of gain. Second, the Fermi distribution broads as the temperature increases, which means more carriers will stays at the high energy states. However, the carriers at lower energy states give more optical gain than these at higher energy states, so the optical gain will be reduced. Third, carrier can be more easily thermonically ejected out of the quantum wells as temperature elevates, making a loss in the recombination carriers. Finally, the non-radiative recombination will increase rapidly with temperature, due to the

interaction between photons and phonons. All the effects will give a reduction in optical gain and the limit the laser output. [33] In this chapter, data will be presented showing a much lower thermal resistance, as well as lower junction temperature in lithographic VCSELs than oxide, which are the key properties for lithographic VCSELs in achieving high output.

Reliability is another important issue in VCSEL application. A VCSEL device will degraded and eventually fail as a result of the growth of crystal defect, caused by internal stress. This degradation process will be accelerated if device is operated at a high injection and a high junction temperature. The early oxide VCSELs had lifetimes of a few hours, due to the high stress caused by the shrinks of oxide in oxidation process using pure AlAs. Strain could be greatly reduced by using $Al_{0.98}Ga_{0.02}As$ instead of AlAs to form the aperture, but still there are defects and strain at the interface between oxide and semiconductor, limiting the reliability of oxide VCSELs operating at several conditions [34]. In lithographic VCSELs, internal stress and junction temperature have been greatly reduced by eliminating the oxide from the structure, and thus are expected to work more reliable than oxide VCSELs.

4.2 All-epitaxial lithographically-defined VCSELs with low thermal resistance

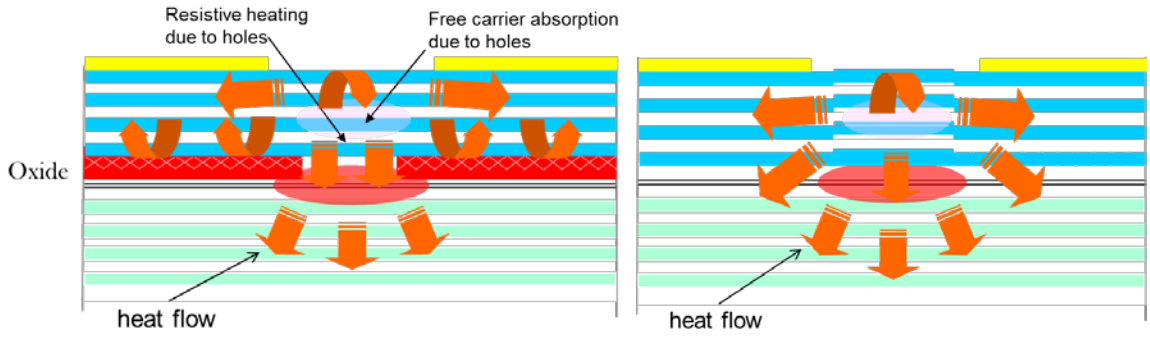
4.2.1 Analysis on thermal resistance

Thermal resistance describes the efficiency of heat flow that affecting the internal temperature, and it is defined as the ratio of temperature rise over the increased in the dissipated power:

$$R_{th} = \frac{\Delta T}{\Delta P_{diss}} \qquad (4.1)$$

Lower thermal resistance, i.e. higher thermal conductivity, gives lower internal temperature, later thermal roll-over of light output, and thus increased maximum output powers, which are important properties affecting the device modulation speed.

In oxide-confined VCSELs, an oxide layer Al_xO_y is used in order to get a good current and optical modes confinement. However, the Al_xO_y has a very low thermal conductivity, ~0.7W/mK, compared with semiconductors, 20-50W/mK. The difference in the thermal conductivities of materials will make big difference in heat flow of the two kinds of devices, illustrating in Figure 4-1. In VCSEL structures, due to the greater effective mass of holes than electrons, the dominant heat is generated from the electrical resistance due to current crowding in the p-side mirror above the active region, as well as from the free carrier absorption due to holes in the p-side mirror. In oxide VCSELs, owing to the low thermal conductivity of the Al_xO_ylayer, the heat flow is blocked or forced through the aperture, producing a very high internal temperature (Figure 4.1(a)). On the other hand, by eliminating the oxide layer in lithographic VCSELs, the heat generated can be spread out much more efficiently (Figure 4.1(b)), which enable lithographic VCSELs to be driven at higher bias levels.



a) b)

Figure 4-1 Heat flow in a) oxide-confined VCSEL and b) lithographic VCSEL.

4.2.2 Thermal resistance measurement of VCSELs

From equation (4.1), in order to get the thermal resistance, the temperature change inside the device and the corresponding dissipated energy need to be identified. Typically, the change of temperature inside a device is hard to measure directly, while the wavelength shift can be easily measured, thermal resistance can then be determined by:

$$R_{th} = \frac{\Delta T}{\Delta P_{diss}} = \frac{\Delta\lambda / \Delta P_{diss}}{\Delta T / \Delta\lambda} \qquad (4.2)$$

where the dissipated power can be get by extracting the output optical power from the input electrical power, the wavelength shift, $\Delta\lambda$, can be measured on a spectrometer, and the ratio $\Delta\lambda / \Delta T \approx 0.07 nm / K$, is used as the wavelength shift dependence on temperature[35]. So the temperature change can be obtained from the value of the wavelength shift. Finally, thermal resistance R_{th} can be got from the linear regression of ΔT and ΔP_{diss}.

We then measured the thermal resistance of 850 nm lithographic VCSELs from three different wafers. The schematic diagram of the growth structures are illustrated in Figure 4-2, which shows the different locations that AlAs is placed in three lithographic VCSELs. The AlAs is located either in structure A: The low index layers of the n-DBR, or in structure B: All low index layers of n-DBR layers except the one that adjacent to the cavity spacer, and all low index layers of p-DBR layers except the one that adjacent to the cavity spacer, or in structure C: All low index layers of n-DBR layers, and all low index layers of the p-DBR except the one that adjacent to the cavity spacer. The thermal resistances given on the Figure are measured from 6 μm devices.[36]

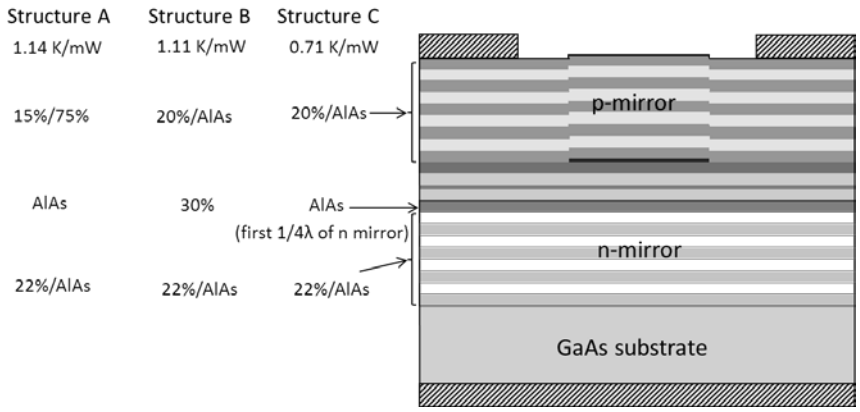


Figure 4-2 Three structure of the lithographic VCSELs with AlAs at different layers

The results of the devices with mesa sizes varied from 3 μm to 20 μm are plotted in Figure 4-3. For comparison, a 6 μm commercial 850 nm oxide-confined VCSEL was also measured by the same experiment setup. The outcome shows the lithographic VCSEL structure with lowest thermal resistance is about 1/3 or 1/4 of the value in oxide VCSEL with the same size. Also the difference of the three lithographic VCSELs indicates that the greater the amount of AlAs in DBRs, the lower the thermal resistance will be obtained from a device, which can be explained by tracking the thermal resistivity (cm·K/W) of the materials in Figure 4-4 [37]. The binary crystal GaAs (x=0) and AlAs (x=1) at two ends of the axis have the lower resistivity than that in between (0<x<1). The third atom in AlGaAs will cause more phonon scattering than the binary crystal structure of GaAs or AlAs, and thus will make the heat more difficult to spread out, making a higher thermal resistivity. Structure C has the most amount of AlAs and has the lowest thermal resistance values, which, to the best of our knowledge, are the lowest values that have ever been measured in 8xx nm mode-confined p-up VCSELs. [36]

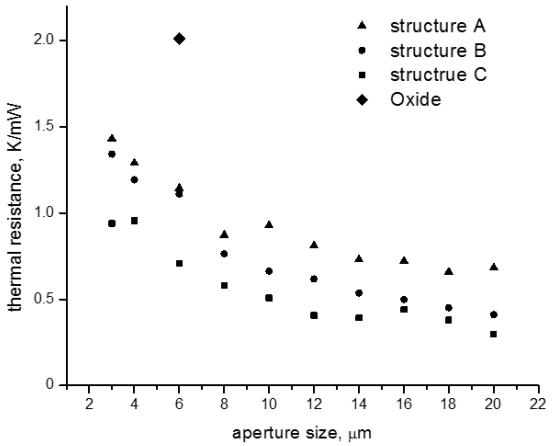


Figure 4-3 Thermal resistances of 3 - 20 μm lithographic VCSELs and a 6 μm commercial oxide VCSEL.

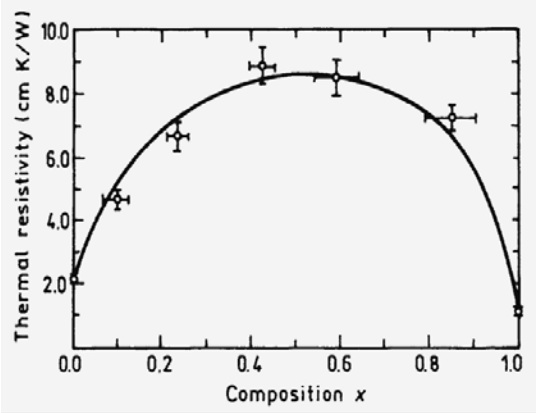


Figure 4-4 Thermal resistivity of $Al_xGa_{1-x}As$ as a function of Al fraction [37].

Here we make a comparison between the thermal resistances of lithographic and oxide VCSELs (Figure 4-5). In addition to the measured results in Figure 4-3, another lithographic VCSEL working at 980nm [38] and several oxide [39-41] [43] [45-49], proton implanted [42], and etched post [44] VCSELs mentioned in literatures have been plotted. To reach a low thermal resistance, many devices, as described in [39-44], have used copper-plate heat sink to help heat spread out, thus to increase the total thermal conductivity. On the contrary, there were no additional heat sink when measuring the lithographic VCSELs, still they reached the lowest record.

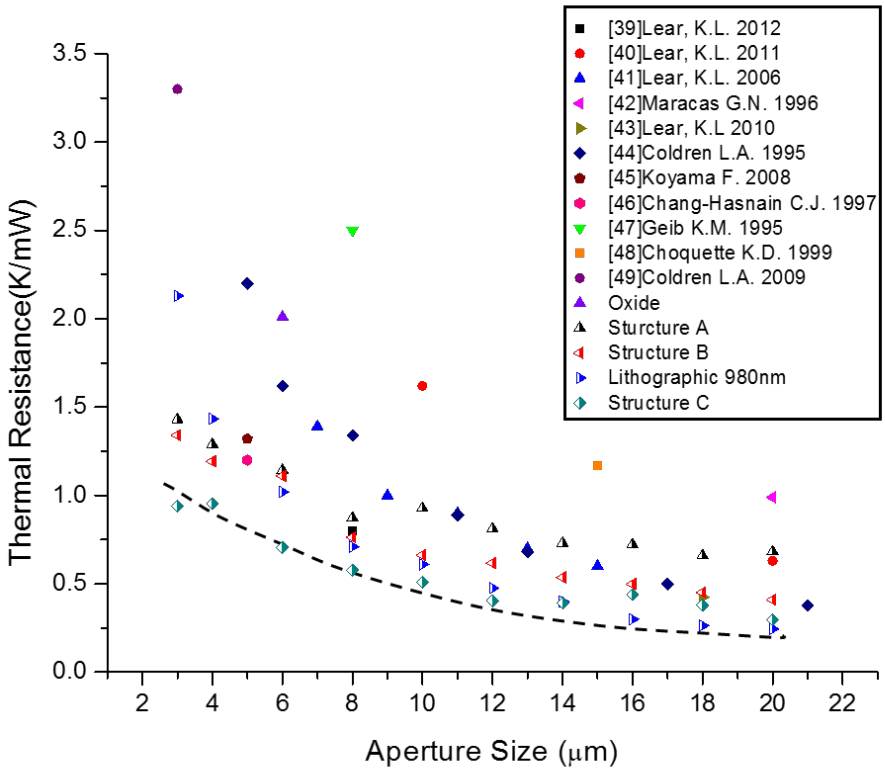


Figure 4-5 Comparison of thermal resistances between lithographic VCSELs and other types of VCSELs in literature

To make a comparison of the heat flow efficiency in different sized devices, we can make a plot of $\frac{1}{R_{th} \cdot A} = \frac{\Delta P_{diss}}{\Delta T \cdot A}$, which represents the increased dissipated power per unit raised temperature per unit area. In Figure 4-6, it can be inferred that heat dissipate more effectively per unit area in small device than in large devices, and can be explained from the illustration diagram of heat flow showing in Figure 4-7. Due to the small volume of optical mode and narrower current path, in a unit area of active region, the heat have more chance to spread laterally than in large devices, enabling the small sized device to be operated at a high current density before thermal rollover, and thus produce a high power density.

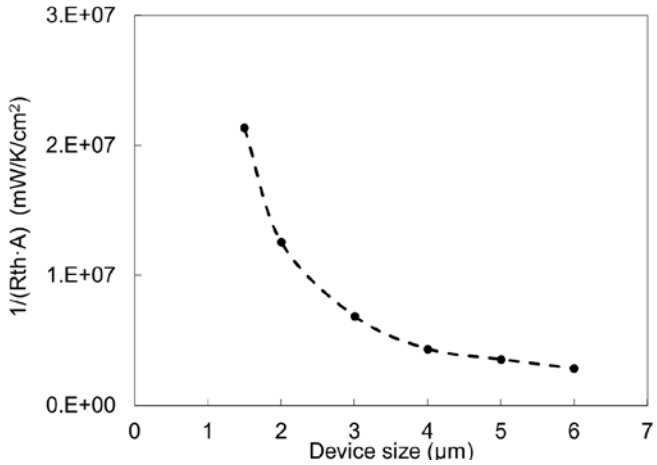


Figure 4-6 Plot of $1/(R_{th} \cdot A)$ in devices with different sizes. Higher values in small devices indicates more effective heat flow.

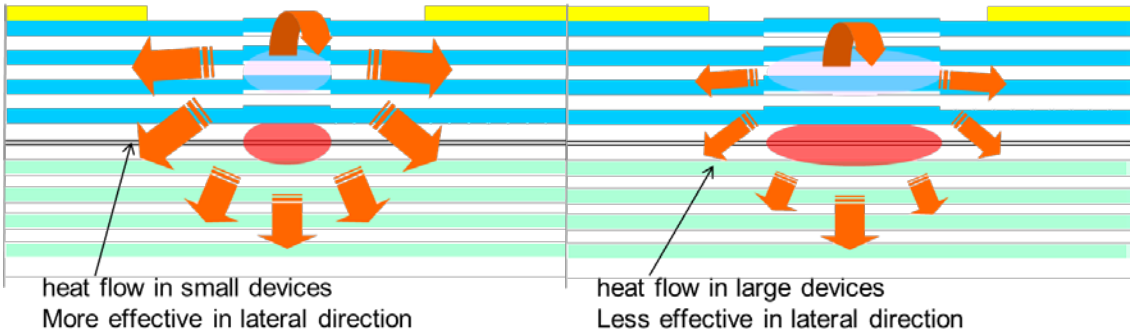


Figure 4-7 Heat spreading diagram in small and large lithographic VCSELs.

4.3 Low junction temperature and high driven level in lithographic VCSELs

The very low thermal resistance will benefit the VCSEL devices in having a postponed thermal rollover, and thus giving a higher output. Figure 4-8 shows the rollover current density for lithographic VCSELs with different sizes and two oxide VCSELs which are commercially available. The lithographic VCSELs are designed at 975 nm while the oxide VCSELs at 850 nm, so the comparison is not direct, but still insightful. In the last section, 850 nm lithographic VCSELs have shown a low thermal resistance, about 1/2 to /1/4 of the value in oxide VCSELs. Here the

rollover current density of 975 nm lithographic VCSELs are compared with 850 nm oxide with otherwise similar operating conditions. There is a trend of increasing current density when thermal rollover as device size goes down, which means small devices can be driven with a higher bias level, consist with the analysis in Figure 4-7. For example, the thermal rollover current density is 102, 167, 318 kA/cm^2 in 6, 4, 2 μm lithographic VCSEL, respectively. On the other hand, oxide VCSEL show a much lower rollover current density, 33, 127 kA/cm^2 in 7.5, 3 μm device, respectively. [30] The results difference are due to the internal junction temperature difference of the two kinds of VCSELs. The capability of higher operating bias levels consist with their higher output powers in lithographic VCSELs as presented in the former chapter, and this current density will enable high intrinsic speed in VCSELs.

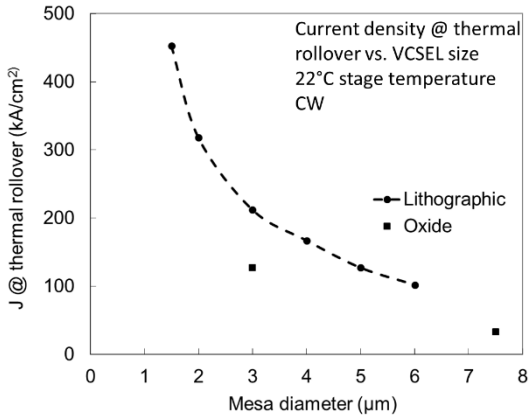


Figure 4-8 Thermal rollover current density of 1.5 to 6 μm lithographic VCSELs, and two oxide VCSELs, measured under similar operating conditions

The operating junction temperature between two kinds of VCSELs have also been compared as shown in Figure 4-9, by fixing the current density to be 50 kA/cm^2 for all devices. The temperature is determined by the measured resonance wavelength shift, and the cavity shift due to change of refractive index. The elevated junction temperature from stage temperature in

lithographic VCSELs is approximately one half as in oxide VCSELs. The 7.5 μm oxide VCSEL measured stopped lasing at this current density due to its high junction temperature. [30]

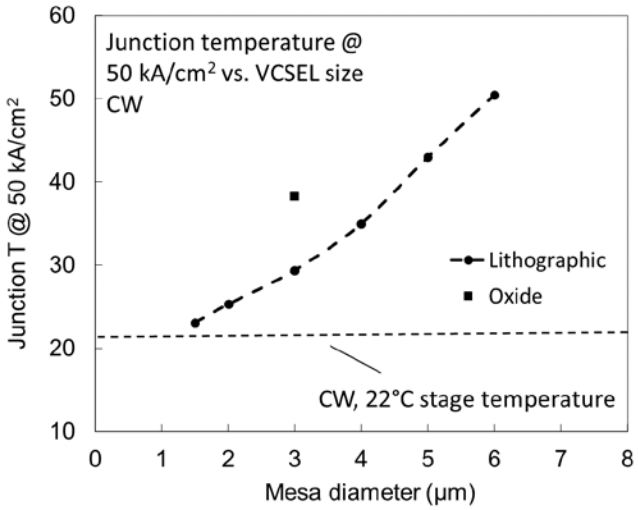


Figure 4-9 Internal junction temperature in VCSELs of different size, fixing bias current density to be 50 kA/cm^2.

The lower junction temperature in smaller devices also indicates reliability will improve in devices with reduced size under a given modulation speed. In lithographic VCSELs, the reduced active region size gives a lower junction temperature, and will reduce the strain caused by expansion. But in oxide VCSELs, the very small aperture size will cause reliability issues because of the strain and defect around the oxide aperture. Therefore lithographic VCSELs with very small size promise much higher reliability than oxide VCSELs and will be discussed next.[30]

4.4 Lithographic VCSELs with high reliability under extreme operating conditions

4.4.1 Theory and discussion of device reliability

A VCSEL device will degraded and eventually fail as a result of the growth of crystal defect, which are caused by internal stress. This degradation process will be accelerated if device

is operated at a high injection and a high junction temperature. The early oxide VCSELs had lifetimes of a few hours, due to the high stress caused by the shrinks of oxide in oxidation process using pure AlAs. Strain could be greatly reduced by using $Al_{0.98}Ga_{0.02}As$ instead of AlAs to form the aperture, but still there are defects and strain at the interface between oxide and semiconductor, limiting the reliability of oxide VCSELs operating at several conditions [49]. In lithographic VCSELs, internal stress and junction temperature have been greatly reduced by eliminating the oxide from the structure, and thus are expected to work more reliable than oxide VCSELs.

There is a well-known dependence of VCSEL reliability that express the expected failure time t_f to be: [50-54]

$$t_f = AJ^{-N} \exp[E_a / (kT_j)] \qquad (5.1)$$

where A is a scaling factor, J is the operated current density, E_a is the activation energy, k is the Boltzmann constant, T_j is the junction temperature, and N is the current acceleration factor. The junction temperature in the exponential term will mostly affect on the failing lifetime.

The heat flow and thermal resistance of the lithographic VCSELs in contrast with oxide VCSELs have been discussed in the former section. Here we make a comparison in thermal resistance, as well as junction temperature rise between small size lithographic VCSELs and a 3 μm oxide VCSEL in Figure 4-10. Thermal resistance measured from a 3 μm lithographic VCSEL, which will be used for reliability test, is 2.06 K/mW, much lower than the measured thermal resistance of 3.61 K/mW in an oxide VCSEL with the same size. The temperature rise above stage is 7.4 °C under a current density of 50 kA/cm^2, and is approximately one half of the value, 16.3°C

in oxide. The junction temperature difference will be much larger if device operated under an extreme conditions such as high stage temperature and high injections. [55]

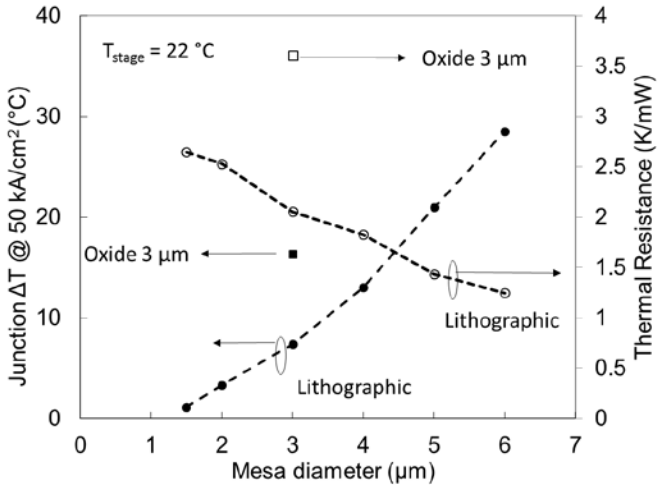
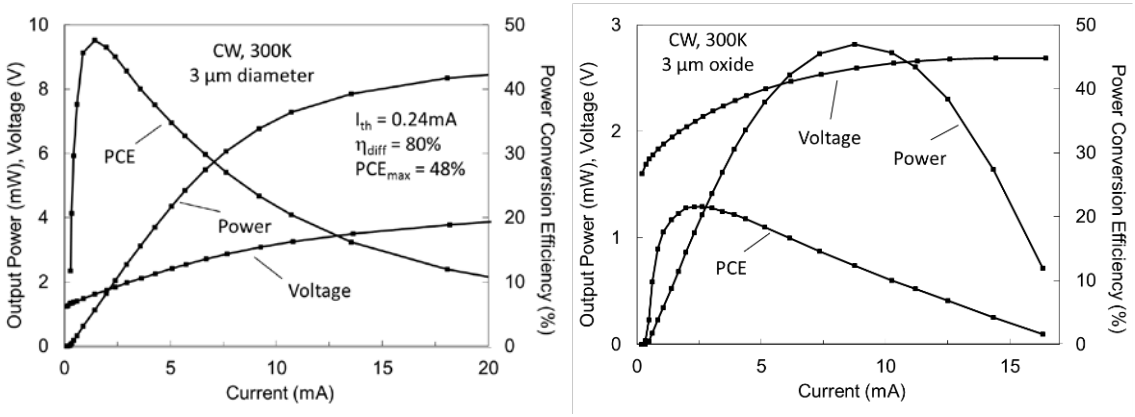


Figure 4-10 A comparison in thermal resistance, as well as junction temperature rise under a current density of 50 kA/cm^2 between small size lithographic VCSELs and a 3 µm oxide VCSEL

4.4.2 Characteristics of tested devices and stress test results

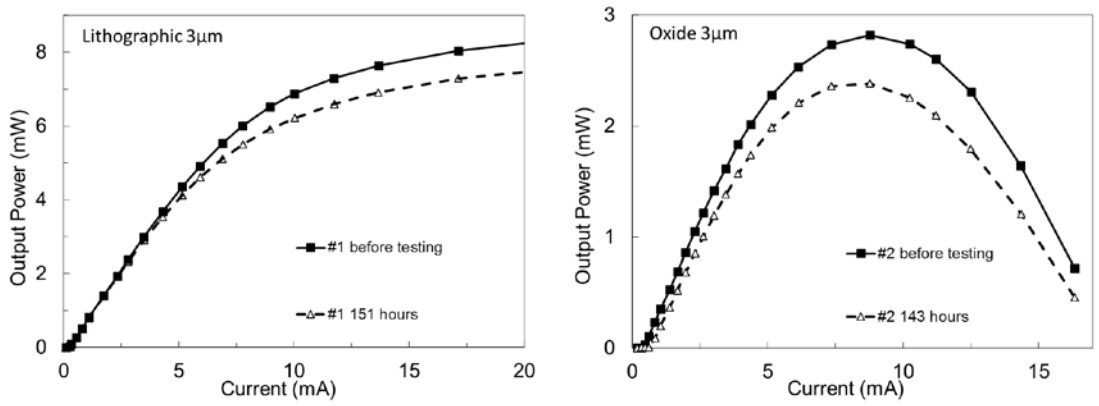
Figure 4-11 (a) gives the L-I-V characteristics from one of the three 3 µm lithographic VCSELs used for stress test, along with the power conversion efficiency vs. current. It has a threshold of 0.24 mA, a maximum power of 8.6 mW, a maximum differential quantum efficiency of 80%, and a maximum wall-plug efficiency of 48%. The other two lithographic VCSELs have similar characteristics. The two 3 µm oxide VCSELs tested for comparison were purchased from a leading VCSEL vendor and one of their lasing characteristics is shown in Figure 4-11(b). [55]



(a) *(b)*

Figure 4-11 Lasing characteristics of 3 µm VCSELs used in the stress test: (a) lithographic (b) oxide.

VCSELs have been developed as a mature product and it may take years before noticeable degradation may be observed under low bias and room temperature, so in our experiment an extreme operating conditions of 140 kA/cm^2 driving current density and 150 °C stage temperature were used, to accelerate the device degradation and shorten the experiment time. To watch the degradation process, L-I-V curves were measured under room temperature after running the stress test for a certain time, by intermittently cooling the stage and device. The light vs. current of the 3 µm lithographic VCSEL before and after a 151 hours operation is shown in Figure 4-12 (a), as well as the 3 µm oxide VCSEL before and after 143 hours operated under the same condition is shown in Figure 4-12(b). Significantly less degradation has been observed in the lithographic VCSEL.[55]



(a) *(b)*

Figure 4-12 Light vs. current before and after the stress test. (a) 3 μm lithographic VCSEL before and after 151 hours test, and (b) 3 μm oxide VCSEL before and after 143 hours test.

Figure 4-13 shows the factor of the power measured during test normalized to the value measured initially, in which the lithographic in solid curves and oxide in dashed curves behave differently. The two oxide VCSELs shows a continuous degradation in the output by tracking of the test time, while the output power of lithographic VCSELs only shows initial drops, and become much more stable in the longer run. [55]

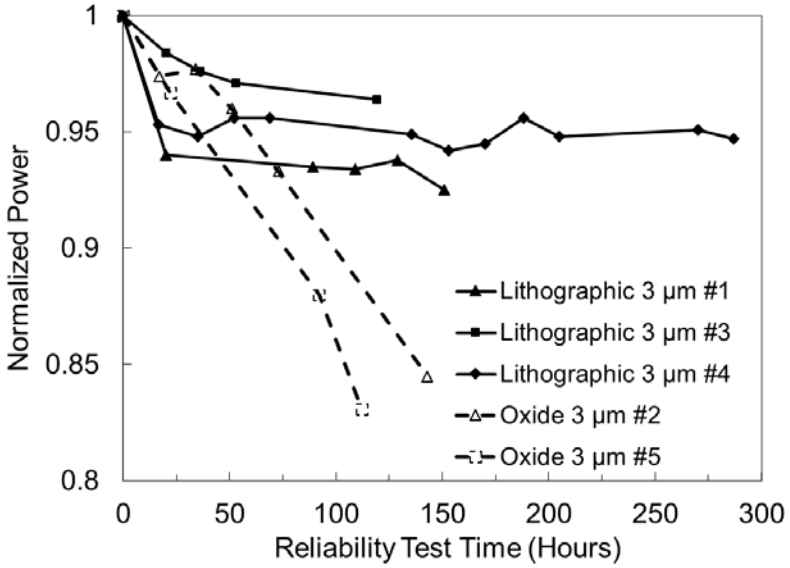


Figure 4-13 Power normalized to initial value track with stress test time

Although device reliability is affected by several factors, junction temperature is believed to be the most important in making the difference under this stress test. The junction temperature measured in lithographic VCSELs is about 185 °C, and in oxide VCSELs is about ~ 255 °C under the condition of 140 kA/cm^2 current density and 150 °C stage temperature. Other factors, including reduced strain by removing the oxide aperture, will also improve the reliability of lithographic VCSELs. For the oxide VCSELs, much higher junction temperature leads to more internal stress, which will accelerate the degradation and shorten the lifetime.[55]

4.5 Summary

In this chapter, the thermal related issues in VCSELs have been studied. By elimination of the oxide layer with high thermal resistivity, lithographic VCSELs surpass oxide VCSELs in their thermal conductivities, and has been experimentally proved. Record low thermal resistances have been reached in lithographic VCSELs even in absence of any heat sink. High temperature stress testing shows lithographic VCSELs can operate more reliably than oxide VCSELs for extreme operating conditions. The high reliability makes it a strong candidate for applications in harsh operating conditions such as integration into silicon electronics and high speed optical interconnects.

CHAPTER 5 : ELECTRICAL PARASITIC ANALYSIS OF LITHOGRAPHIC VCSELS

5.1 VCSEL application in high speed modulation.

One of the major VCSEL applications is in high speed data communication. In the application areas such as computing systems, data centers and short reach data communication networks, VCSELs with direct modulation and multimode fibers serve as the base components. There are 40/100 Gigabit Ethernet standard proposed for the next generation of high speed Ethernet, requiring optical source with higher modulation speeds.

The low power consumption and high speed modulation capability makes VCSEL an ideal optical source for the next generation data transmission. Circular beam profile with small divergence angle improves the efficiency in coupling optical signal into multimode fibers. Recently, the improved oxide-confined VCSELs with data rates ranging from 25 Gbps to 55 Gbps have been reported [56-58], which dominate high modulation speed records of laser diodes. However, several limitations still exist that set limitation for higher speeds, directly coming from the requirement of oxide aperture with in the laser cavity. The first is the elevated junction temperature at high injection currents due to high thermal resistance, limiting the maximum output power and intrinsic speeds. The second is the unrepeatable in the oxidation process to achieve small devices to get single mode operation and high photon density, which are important in getting low power consumption and high intrinsic speeds. The last is the requirement for current to pass through the heterojunctions in the oxide aperture, giving high serial resistances and limiting modulation bandwidth. In this chapter, data will presented with record low differential resistance

in lithographic VCSELs, showing its potential capability in high speed modulation through simulation.

5.2 Theory of high speed modulation

When a laser device is driven by a radio frequency electrical source, there are two major limitations to degrade the laser performance. One is the intrinsic laser properties, which are determined by the carrier combination and photon generation speeds. The other is the extrinsic parasitic elements including capacitance and resistance in the circuit. Since the extrinsic parasitics are the main limitation in current oxide VCSELs, a detailed analysis will be discussed next.

Figure 5-1 shows an equivalent circuit model commonly used for analyzing the parasitic modulation [59]. The capacitance and resistance in the circuit work as a low-pass RC-filter, so that not all the modulation current will flow through the laser junction. The parasitic transfer function is defined as:

$$H_{para}(\omega) = \frac{current\ flow\ into\ active\ region}{modulation\ current} = \frac{i_j(\omega)}{i_s(\omega)}$$

With higher modulation frequency, less current $i_j(\omega)$ from $i_s(\omega)$ will flow through laser junction, and thus produce less laser output. The parasitic elements affecting bandwidth includes: C_p, the capacitance due to the metal contact pads, C_m, the capacitance due to oxide or current blocking region, R_m, the mirror resistance including p-mirror where holes are the main charge carriers and the n-mirror where electrons are the main charge carriers, and R_j, the resistance next to the active region. Figure 5-2 shows the four elements inside an oxide VCSEL[60] or lithographic VCSEL structure. In the oxide VCSEL, capacitance C_m is a combination of the multiple

capacitances of the oxide layers (C_{ox}), and the capacitance formed by the depleted layers inside (C_{diff}) or outside (C_{dep}) the oxide aperture. In lithographic VCSELs, there is a capacitance formed by depleted heterojunction current blocking regions (C_{DHCBR}), similar to C_m in oxide VCSELs. By analyzing the circuit, the parasitic response can be expressed as:

$$H_{para}(\omega) = \frac{\dfrac{1}{C_p R_m C_{DHCBR} R_j}}{-\omega^2 + i\omega \dfrac{C_{DHCBR} R_j + C_p R_m + C_p R_j}{C_p R_m C_{DHCBR} R_j} + \dfrac{1}{C_p R_m C_{DHCBR} R_j}} \tag{5.1}$$

In order to get high electrical modulation bandwidth, all the four parameters, C_p, C_m or C_{DHCBR}, R_m, and R_j need to be optimized.

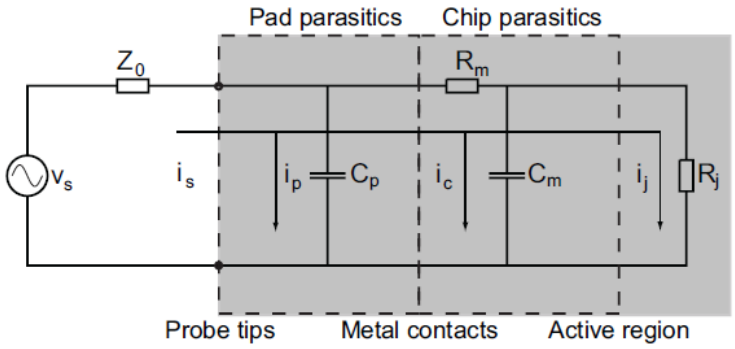


Figure 5-1 Equivalent circuit model for electrical modulation bandwidth analysis.[59]

5.3 Experiment results of lithographic VCSELs with low differential resistance

To minimizing the pad capacitance C_p, metal contacts need to be designed with reduced pad areas, increased spacing between metal pads, and use spacing material with low dielectric constant, such as Benzocyclobutene (BCB). Considering the dimension of the lithographic VCSEL devices and possible metal contacts, the optimized pad capacitance is estimated to be 33 fF.

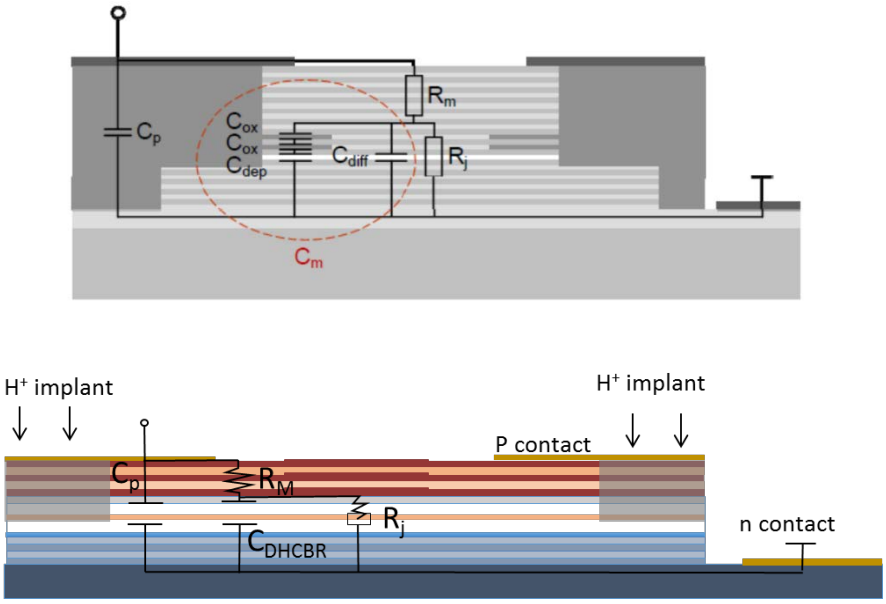


Figure 5-2. Equivalent circuit model in oxide [60] and lithographic VCSEL structures.

To minimizing the capacitance C_{DHCBR}, proton implantation is applied to reduce the effective area contributing to the capacitance. Also the thick current blocking layers (~160 nm) will help produce less capacitance. The C_{DHCBR} is estimated to be 128 fF in 6 μm device and 106 fF in 4 μm device. The capacitance can be reduced in small sized devices due to the reduced areas.

The electrical differential resistance, composed by mirror and junction resistances, is the major limitation to the parasitic response, and thus needs to be well-designed. As discussed in Chapter 2, graded layers have been placed at GaAs/AlAs interfaces in DBR mirrors and selective doping profile has been designed to produce low electrical resistance while keeping a low optical loss. Lithographic VCSELs sized from 1 to 6 μm with optimized structures have been measured. Figure 5-3 (a) (b) shows the L-I-V curves of a 6 μm and a 3 μm devices. With slope efficiency exceed 60%, measured maximum power is 17.2 mW for the 6 μm device, and 8.7 mW for the 3

μm device. Differential resistances and operating voltages are record low values for both VCSEL sizes. The differential resistance is 43 Ω for the 6 μm VCSEL and 78 Ω for the 3 μm VCSEL.

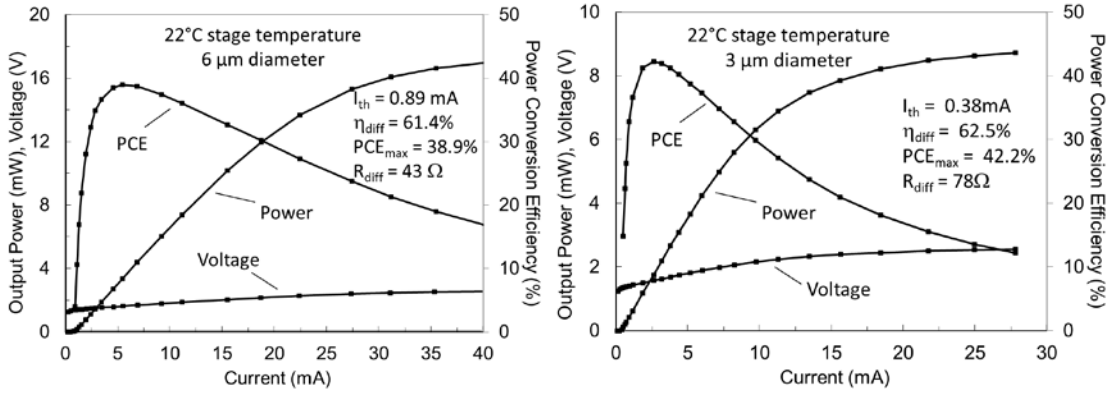


Figure 5-3 Lasing characteristics of 6 μm and 3 μm lithographic VCSELs with record low differential resistances.

Figure 5-4 shows differential resistances of lithographic VCSELs, as well as the lowest values in oxide VCSELs with comparable sizes designed for high speed [61-64]. It is shown that with optimized mirror and cavity design, much lower differential resistance can be reached in lithographic VCSELs than in oxide, especially in small sized devices. The differential resistance in VCSEL is composed by mirror resistance and aperture resistance. For oxide VCSELs, the aperture resistance is mainly set by the holes that flow from p DBR mirrors through the aperture into the active region. It is difficult to get low resistance since oxide aperture must be formed by $Al_xGa_{1-x}As$ with high Al content. Through removing the oxide layer, lithographic VCSELs do not have this limitations, and therefore much lower resistance can be obtained [65].

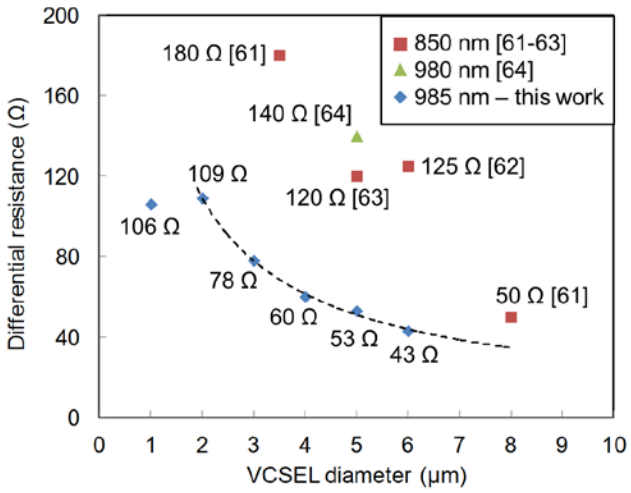


Figure 5-4 Comparison of differential resistances of lithographic VCSELs, as well as the best reported high speed oxide VCSELs.

In the meantime of getting lower differential resistance, the corresponding differential quantum efficiencies of lithographic VCSELs in Figure 5-5, are still higher than the oxide. This is because that these oxide VCSELs, designed for high speed, must have p-DBR mirrors to be heavily doped to control the overall resistance, which in turn brings excess free carrier absorption and degrades the optical efficiencies. In lithographic VCSELs, low resistance can be obtained without introducing too much carrier absorption to sacrifice efficiency. The efficiency of 1 μm VCSEL shows a descent value, as well as in the resistance trend, which are likely to be influenced by the leaking current due to electrical contact. Higher efficiency is expected in the small device once the leakage problem is solved.

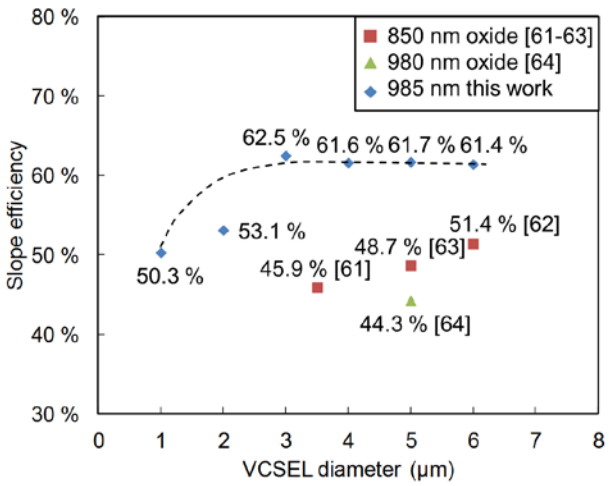


Figure 5-5 Comparison of the slope efficiency vs. device size in lithographic and oxide VCSELs.

5.4 Simulation of top-emitting high-speed lithographic VCSELs

The modulation speed of a VCSEL is determined both by intrinsic and parasitic response. To get low differential resistance is the key to get high parasitic response, so it is essential to do an estimation with the low differential resistance values obtained in lithographic VCSELs.

Based on the optimized metal configuration and measured differential resistance, modulation responses of 2 to 6 μm devices due to parasitic are plot out in Figure 5-6. The parameters used in the simulation are listed in Table 6-1.The 3 dB frequencies are 116 GHz, 89 GHz, 70 GHz, 50 GHz and 39 GHz for the 6 μm, 5 μm, 4 μm, 3 μm and 2 μm lithographic VCSELs, respectively. Although smaller devices have less capacitance due to the depleted heterojunction current blocking region, the parasitic bandwidths in smaller devices are lower, mostly due to the increased junction resistance R_j and mirror resistance R_m coming from the size reduction. The higher differential resistances in oxide VCSELs will give more limitations to their modulation

bandwidths. The overall high speed characteristics need to be determined by combining intrinsic and parasitic response.

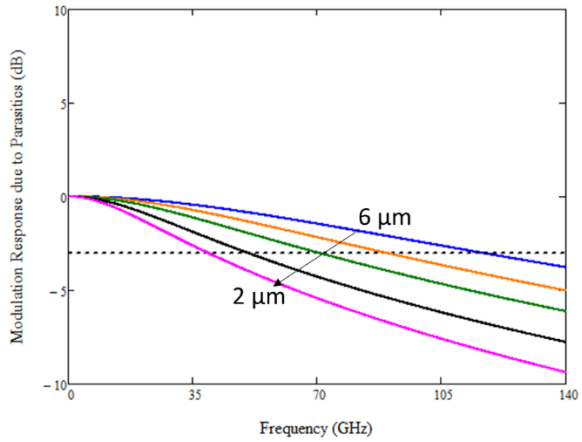


Figure 5-6 Simulation of modulation responses of 2 to 6 µm lithographic VCSELs due to electrical parasitics

Table 5-1 Parameters used in the simulation of modulation due to parasitics, and the corresponding 3dB frequency.

Device Size (µm)	$R_{diff}(\Omega)$ $(R_j + R_m)$	$R_j(\Omega)$	$R_m(\Omega)$	$C_p(fF)$	$C_{DHCBR}(fF)$	$f_{3dB}(GHz)$
2	109	51	58	33	83	39
3	78	37	41	33	95	50
4	60	23	37	33	106	70
5	53	15	38	33	117	89
6	43	10	33	33	128	116

Due to the high differential resistance in oxide-confined VCSELs, the electrical parasitic response usually plays a major role in limiting the bandwidth [66-67]. While in the lithographic VCSELs with low differential resistances, especially in 4-6 µm devices, the bandwidth will be mostly limited by the intrinsic other than the parasitic. The intrinsic modulation response have been simulated based on the laser rate equations, and the total response have been calculated by

combining intrinsic and parasitic response. Figure 5-7 shows the simulated total modulation response of the 6 μm device under four driving currents, giving a 3 dB bandwidth of 3 GHz, 26 GHz, 42 GHz, 56 GHz, respectively. Figure 5-8 shows the simulated modulation response of the 4 μm device under four driving currents, giving a 3 dB bandwidth of 10 GHz, 31 GHz, 51 GHz, 61 GHz, respectively. The expected modulation bandwidths are higher to the oxide-confined VCSELs designed for high speed. The overall modulation speed is still limited by the parasitic in devices sized below 3 μm, but already showing great improvement than the bandwidth of 25-30 GHz reached in the best reported high speed oxide VCSELs.

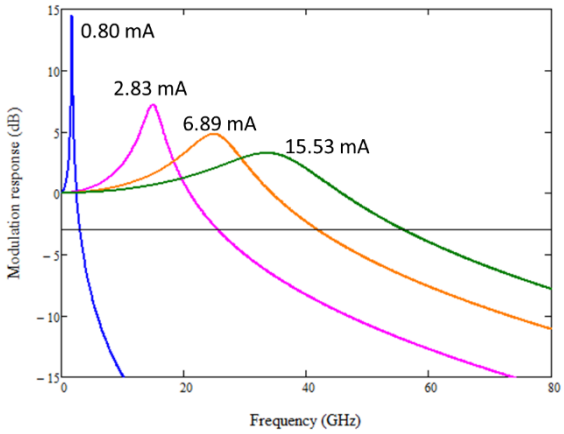


Figure 5-7 Simulation of total modulation response of a 6 um under driving current levels of 0.80, 2.83, 6.89 and 15.53 mA, giving 3 dB bandwidths of 3, 26, 42, 56 GHz, respectively.

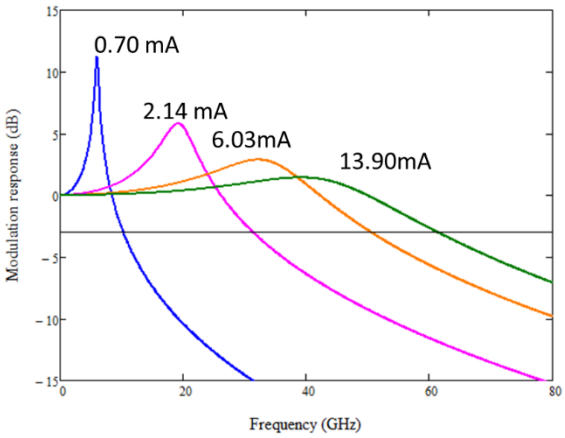


Figure 5-8 Simulation of total modulation response of a 4 um under driving current levels of 0.70, 2.14, 6.03 and 13.90 mA, giving 3 dB bandwidth of 10, 31, 51, 61 GHz respectively.

5.5 Bottom emitting VCSELs designed to improve parasitic response

The key to get higher parasitic modulation speed is to optimize the resistance and capacitance. The top emitting structure showing in Figure 5-2 can be further improved. In this section, a bottom emitting structure will be presented and analyzed, showing a reduction both in resistance and capacitance, and is expected to produce higher modulation bandwidth than the top emitting design.

The structure of a bottom emitter is illustrated in Figure 5-9. Different from the top emitters showing in Figure 5-2, the metal layer deposited on the p side will work as part of the p DBR mirror and an anti-reflection coating is deposited on the n side to make light emit from the bottom side. Proton implantation is also used to reduce the capacitance. Through this design, there would be less mirror resistance and less free carrier absorption, due to the more uniform current injection and the reduction of number of p mirror pairs. Also it is getting less area contributing to the C_{DHCBR}, making a reduction to the capacitance as well. All these aspects will help to improve the parasitic modulation bandwidth.

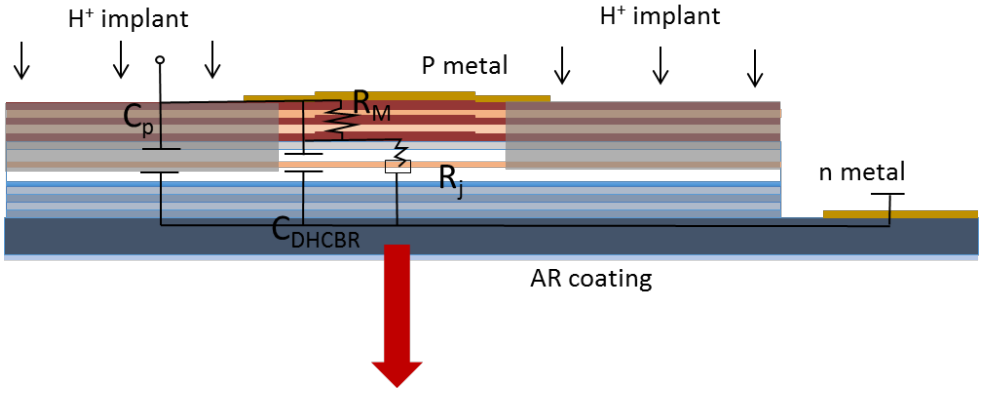


Figure 5-9 Illustration diagram of bottom-emitting structures of lithographic VCSELs for high speed modulation

By coating a gold layer on top of the p-DBR mirror, high reflectivity can be reached with fewer number of mirror pairs due to the increased difference of refractivie index [68-69]. Figure 5-10 are the simulation results showing that a GaAs/AlAs DBR mirror with graded interfaces needs 13 pairs to get R=98.56% at 990 nm, while a hybrid mirror with gold on top only requires 9 pairs of GaAs/AlAs to get R=99.58%. Since the electrons have much higher mobility than holes in $Al_xGa_{1-x}As$, the total mirror resistance is mainly coming from p mirror resistance. By reducing the number of mirror pairs in p-DBR can effectively lower the mirror resistance, as well as free carrier absorption. Also the lateral distance for the holes to reach device region is shortened from the top emitting design, thus a more uniform current flow injection would be formed and mirror resistance can be further reduced.

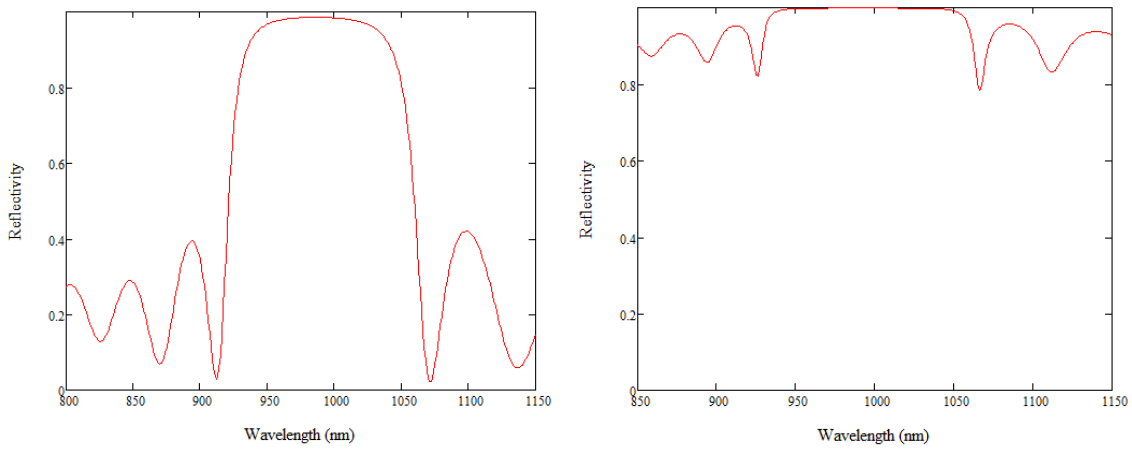
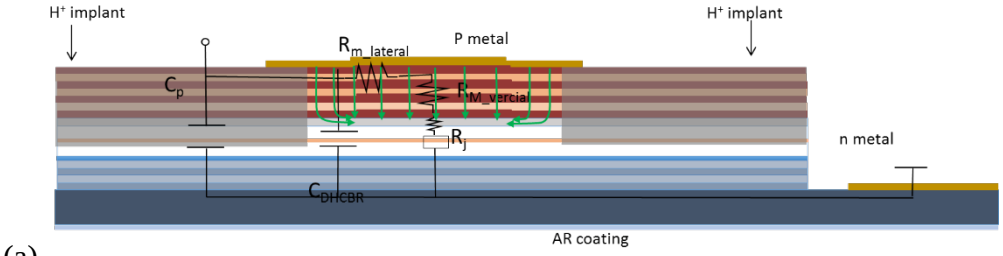
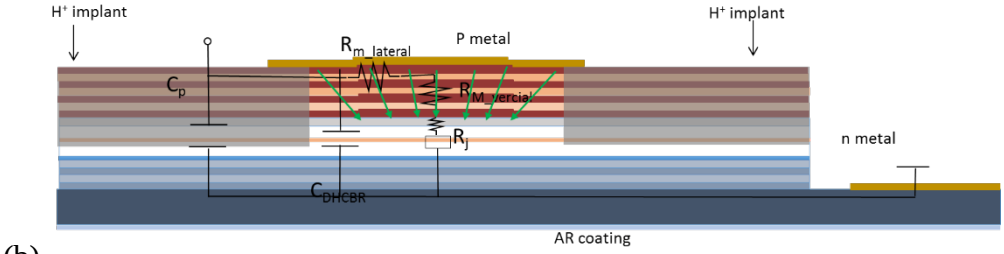


Figure 5-10 Reflectivity of 13 pairs of GaAs/AlAs mirrors for top emitters (R=98.56%, left), or a hybrid mirror contains 9 pairs of GaAs/AlAs and gold coating for bottom emitters (R=99.58%, right)

The analysis below is performed to get an estimation of the resistance of p mirror with reduced number of pairs. The total mirror resistance is divided into two parts, the lateral and vertical. For the vertical resistance, two current flow diagram showing in Figure 5-11 are considered, either through the largest possible cross section in (a), or through a constantly shrinking cross section (b). Current flow with a larger cross section will produce a lower resistance, however, the current needs to be confined to the device area before entering the laser junction to ensure high efficiency. So the two current flow diagram sets the minimum and maximum vertical resistance, and the actual current flow will be an intermediate case.



(a)



(b)

Figure 5-11 Two different current flow diagram setting (a) the minimum vertical resistance and (b) the maximum vertical resistance

By calculating the hole concentration inside p-DBR mirrors, resistance can be estimated using equation $R_m = \sum \frac{R_{sheet,i}}{A_i} = \sum \frac{d_i}{e \cdot \mu_{h,i} \cdot p_i \cdot A_i}$, in which $R_{sheet,i}$,in the unit of $\Omega \cdot cm^2$, is the sheet resistance of the i-th layer, A_i is the cross section area, d_i is the vertical thickness, $\mu_{h,i}$ is the hole mobility, and p_i is the hole concentration of the i-th layer. The p mirror resistances of different sized device under two different current flow diagram are listed in Table 6-2 as $R_{m\_\min}$ corresponds to Figure 5-11(a) and $R_{m\_\max}$ corresponds to Figure 5-11(b).

Table 5-2 Vertical and lateral resistance, junction resistance, and capacitance estimation from the bottom-emitting design.

Device Size (μm)	$R_{m\_min}(\Omega)$	$R_{m\_max}(\Omega)$	$R_{m\_lateral}(\Omega)$	$R_j(\Omega)$	$C_{DHCBR}(fF)$
2	20	76	15	46	20
3	15	41	12	25	25
4	11	26	10	16	29
5	9	18	8	10	34
6	7	13	7	7	39

The junction resistances listed in Table 5-2 are calculated using $R_m = \frac{\sum R_{sheet,i}}{A} = \frac{1}{A}\sum \frac{d_i}{e \cdot \mu_{h,i} \cdot p_i}$, where A is the area of device. The lateral resistances are set by the carriers flow from the edge of implanted region to the mesa, estimated by $R_{Lateral} = \frac{1}{q \cdot \mu_p \cdot p \cdot 2\pi\Delta t}\int_{r_1}^{r_2} \frac{dr}{r} = \frac{1}{q \cdot \mu_p \cdot p \cdot 2\pi\Delta t}\ln(\frac{r_2}{r_1})$, where Δt is the vertical thickness of the current spreading layers, and r_1 ,r_2 are the radii of mesa and implanted regions, separately. The capacitance due to the depleted heterojunction current blocking regions are much lower than the top emitters listed in Table 5-1, owing to the reduced ring area between mesa and implanted region.

The parasitic modulation response has been simulated with the $R_{m\_\min}$ or $R_{m\_\max}$ from the two current flow diagrams, showing in Figure 5-12. The 3-dB parasitic bandwidth is 83, 129, 179, 248, 315 GHz for device sized from 2 to 6 μm, separately, using current flow in Figure 5-11(b) that sets the $R_{m\_\min}$, and is 55, 94, 139, 199, 255 GHz, using current flow in Figure 5-11(a) that sets the $R_{m\_\max}$. Compared with top emitter results showing in Table 5-1, the improved

modulation speed are due to the lower resistances as a benefit from reduced number of p-mirror pairs, as well as the lower capacitance due to the area reduction in current blocking regions.

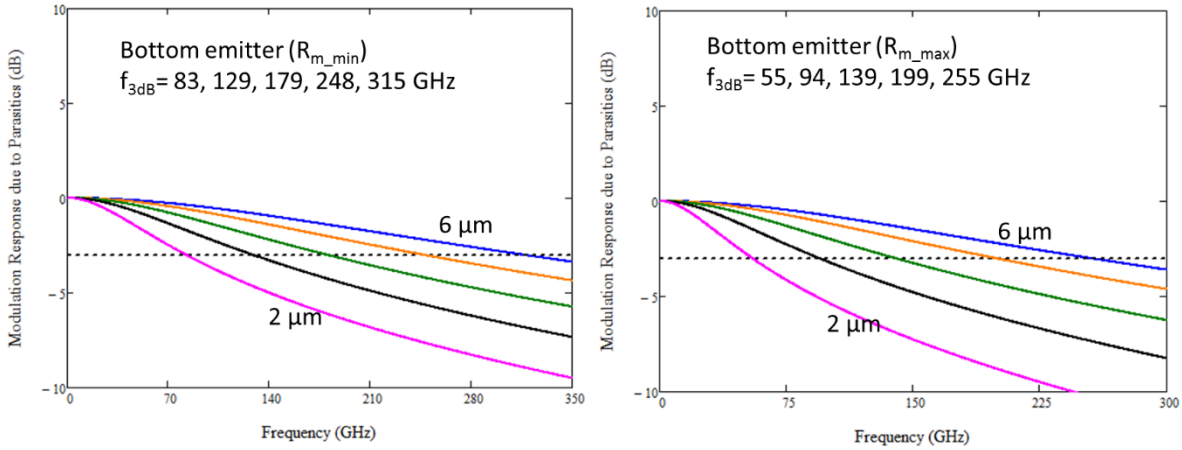


Figure 5-12 Simulation of parasitic modulation response of bottom emitters using R_{m_min} (left), and R_{m_max} (right).

The intrinsic model has been studied in Mingxin Li's dissertation [70] and the differential gain and photon density are calculated based on the photon number and slope efficiency from our experimental results. The total modulation responses for different sizes, including the intrinsic and parasitic, are then calculated. Figure 5-13 gives a 3 µm device as an example, showing the maximum 3-dB modulation bandwidth under 11.29 mA increase from 60.2 GHz using top-emitting design into 73.4 GHz using bottom-emitting design. The overall modulation bandwidths of top and bottom emitters are listed in Table 5-3.

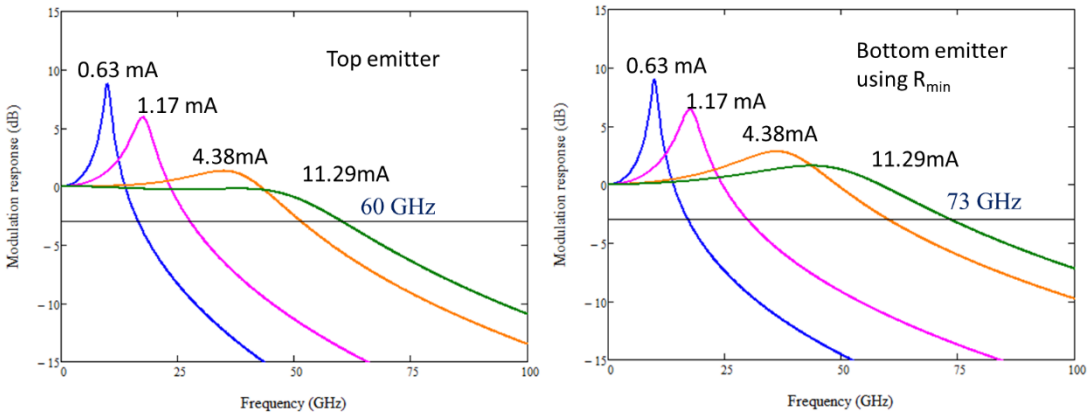


Figure 5-13 Simulation of total modulation response of 3 μm top emitter (left) or bottom emitter (right) using $R_{m\_\min}$.

Table 5-3 3-dB bandwidth of overall modulation response in top emitter and bottom emitters using $R_{m\_\max}$ or $R_{m\_\min}$ as p mirror resistance

Device (μm)	Current in getting max bandwidth (mA)	Top emitter (GHz)	Bottom emitter with $R_{m\_\max}$ (GHz)	Bottom emitter with $R_{m\_\min}$ (GHz)
2	7.52	54.2	67.6	77.7
3	11.29	60.2	69.6	73.4
4	13.90	60.6	67.7	69.8
5	17.89	57.5	62.7	63.5
6	22.45	56.1	59.5	60.0

5.6 Summary

From the new methods of defining aperture in lithographic VCSEL structures, record low differential resistance has been achieved while higher slope efficiency and higher output power has been maintained. High speed simulation has been made, showing the very low differential resistance will benefit much to the modulation response due to parasitic, and is expected to produce

modulation bandwidths of 54-61 GHz in 2-6 μm devices, respectively. Modulation bandwidth can be further improved to 60-78 GHz in 2-6 μm devices, respectively, by using a bottom emitting design with reduced resistance and capacitance.

CHAPTER 6 : CONCLUSION AND FUTURE WORKS

In this report, oxide-free lithographic VCSELs have been introduced and the lasing characteristics of devices have been presented. An intra-cavity phase shifting mesa is applied in lithographic VCSELs. By eliminating the oxide layer, lithographic VCSELs have reached the record low thermal resistance without any heatsink and record high output power. The maximum power in a 6 μm device exceeds 19 mW. Over 50 % power conversion efficiency has been achieved. In the smallest 1 μm VCSEL, a maximum power of 5 mW with single mode operation has been observed. The uniformity and reproducibility are realized through eliminating the oxidation process and using a lithographic design. These size VCSELs with high efficiency, high power can be applied in high power VCSEL arrays based on single mode VCSELs, high speed interconnects, and optical sensing.

A stress test with extreme operating conditions has been performed showing lithographic VCSELs have higher reliability than oxide VCSELs, mostly due to the much lower junction temperature, and reduced internal strain in the oxide-free structure. In applications with harsh operating conditions such as for integration into silicon electronics, lithographic VCSELs can have better reliability. The low junction temperature and small sizes can be useful for a range of applications in high speed optical interconnects and high power arrays, as well as applications such as sensors that require single mode operation.

Due to the new ways of fabricating the aperture, record low resistance has been achieved while higher slope efficiency and higher output power have been maintained. High speed simulation shows the very low differential resistance will benefit much to the parasitic modulation response, and is expected to produce high modulation bandwidths. A bottom emitting structure

has been proposed and analyzed, showing reduction in both mirror resistance and capacitance will further improve the modulation speed.

Future works includes optimizing of epitaxial structures and device packaging, as well as making high speed lithographic VCSELs with very low differential resistances. Another future work is to make dense-packed high-power 2-D VCSEL arrays based on the optimized single device.

REFERENCE

[1] Koyama, F. "Recent advances of VCSEL photonics." Journal of Lightwave Technology 24, no. 12 (2006): 4502-4513.

[2] Tatum, J. A. "Evolution of VCSELs." In SPIE OPTO, pp. 90010C. International Society for Optics and Photonics, 2014.

[3] Huffaker, D. L., D. G. Deppe, K. Kumar, and T. J. Rogers. "Native−oxide defined ring contact for low threshold vertical−cavity lasers." Applied Physics Letters 65, no. 1 (1994): 97-99.

[4] Blokhin, S. A., J. A. Lott, A. Mutig, G. Fiol, N. N. Ledentsov, M. V. Maximov, A. M. Nadtochiy, V. A. Shchukin, and D. Bimberg. "Oxide-confined 850 nm VCSELs operating at bit rates up to 40 Gbit/s." Electronics Letters 45, no. 10 (2009).

[5] Westbergh, P., Gustavsson, J. S., Kögel, B., Haglund, Å., Larsson, A., Mutig, A., ... & Joel, A. "40 Gbit/s error-free operation of oxide-confined 850 nm VCSEL." Electronics Letters 46, no. 14 (2010).

[6] Szweda, R. "Vcsel Applications Diversify as Technology Matures." III-Vs Review 19, no. 1 (2006): 34-38.

[7] Soda, H., Iga, K. I., Kitahara, C., & Suematsu, Y. "Gainasp/Inp Surface Emitting Injection Lasers." Japanese Journal of Applied Physics 18, (1979): 2329.

[8] Uchiyama, S. and K. Iga. "Two-Dimensional Array of Gainasp/Inp Surface-Emitting Lasers." Electronics Letters 21, no. 4 (1985): 162-164.

[9] Iga, K., Kinoshita, S. and Koyama, F. "Microcavity Gaalas/Gaas Surface-Emitting Laser with Ith=6mA." Electronics Letters 23, no. 3 (1987): 134-136.

[10] Koyama, F., S. Kinoshita and K. Iga. "Room-Temperature Continuous Wave Lasing Characteristics of a Gaas Vertical Cavity Surface-Emitting Laser." Applied Physics Letters 55, no. 3 (1989): 221-222.

[11] Geels, RS, SW Corzine, JW Scott, DB Young and LA Coldren. "Low Threshold Planarized Vertical-Cavity Surface Emitting Lasers." IEEE Photonics Technology Letters 2, no. 4 (1990): 234-236.

[12] Numai, T., Kawakami, T., Yoshikawa, T., Sugimoto, M., Sugimoto, Y., Yokoyama, H., Kasahara, K. and Asakawa, K., "Record Low Threshold Current in Microcavity Surface-Emitting Laser." Japanese journal of applied physics 32, no. 10B (1993): L1533-L1534.

[13] Tell, B, YH Lee, KF Brown-Goebeler, JL Jewell, RE Leibenguth, MT Asom, G Livescu, L Luther and VD Mattera. "High-Power Cw Vertical-Cavity Top Surface-Emitting Gaas Quantum Well Lasers." Applied physics letters 57, no. 18 (1990): 1855-1857.

[14] Huffaker, DL, DG Deppe, K Kumar and TJ Rogers. "Native-Oxide Defined Ring Contact for Low Threshold Vertical-Cavity Lasers." Applied Physics Letters 65, no. 1 (1994): 97-99.

[15] Yang, GM, MH MacDougal and PD Dapkus. "Ultralow Threshold Current Vertical-Cavity Surface-Emitting Lasers Obtained with Selective Oxidation." Electronics Letters 31, no. 11 (1995): 886-888.

[16] Lee, H. K., Y. M. Song, Y. T. Lee, and J. S. Yu. "Thermal analysis of asymmetric intracavity-contacted oxide-aperture VCSELs for efficient heat dissipation." Solid-State Electronics 53, no. 10 (2009): 1086-1091.

[17] Demir, A., Zhao, G., & Deppe, D. G.,"Lithographic lasers with low thermal resistance." Electronics letters 46, no. 16 (2010): 1147-1149.

[18] Lu, D, J Ahn and DG Deppe. "All-Epitaxial Current-and Mode-Confined AlGaAs/GaAs VCSEL." *Electronics Letters* 40, no. 21 (2004): 1336-1337.

[19] Deppe, DG, T-H Oh and DL Huffaker. "Eigenmode Confinement in the Dielectrically Apertured Fabry-Perot Microcavity [VCSEL]." Photonics Technology Letters, IEEE 9, no. 6 (1997): 713-715.

[20] Born, M., & Wolf, E. Principles of Optics: Electromagnetic Theory of Propagation, Interference and Diffraction of Light: CUP Archive, 1999.

[21] Peters, MG, BJ Thibeault, DB Young, JW Scott, FH Peters, AC Gossard and LA Coldren. "Band-Gap Engineered Digital Alloy Interfaces for Lower Resistance Vertical-Cavity Surface-Emitting Lasers." Applied physics letters 63, no. 25 (1993): 3411-3413.

[22] Zhou, P., Cheng, J., Schaus, C. F., Sun, S. Z., Zheng, K., Armour, E., ... & Vawter, G. A. "Low Series Resistance High-Efficiency Gaas/Algaas Vertical-Cavity Surface-Emitting Lasers with Continuously Graded Mirrors Grown by Mocvd." Photonics Technology Letters, IEEE 3, no. 7 (1991): 591-593.

[23] Chang-Hasnain, CJ, CE Zah, G Hasnain, JP Harbison, LT Florez, NG Stoffel and TP Lee. "Effect of Operating Electric Power on the Dynamic Behavior of Quantum Well Vertical-Cavity Surface-Emitting Lasers." Applied physics letters 58, no. 12 (1991): 1247-1249.

[24]Orenstein, M, AC Von Lehmen, C Chang-Hasnain, NG Stoffel, JP Harbison and LT Florez. "Matrix Addressable Vertical Cavity Surface Emitting Laser Array." Electronics letters 27, no. 5 (1991): 437-438.

[25] Lear, KL, RP Schneider, KD Choquette, SP Kilcoyne, JJ Figiel and JC Zolper. "Vertical Cavity Surface Emitting Lasers with 21% Efficiency by Metalorganic Vapor Phase Epitaxy." Photonics Technology Letters, IEEE 6, no. 9 (1994): 1053-1055.

[26] Peters, MG, DB Young, FH Peters, JW Scott, BJ Thibeault and LA Coldren. "17.3% Peak Wall Plug Efficiency Vertical-Cavity Surface-Emitting Lasers Using Lower Barrier Mirrors." Photonics Technology Letters, IEEE 6, no. 1 (1994): 31-33.

[27] Schubert, EF, LW Tu, GJ Zydzik, RF Kopf, A Benvenuti and MR Pinto. "Elimination of Heterojunction Band Discontinuities by Modulation Doping." Applied physics letters 60, no. 4 (1992): 466-468.

[28] Reiner, G, E Zeeb, B Moller, M Ries and KJ Ebeling. "Optimization of Planar Be-Doped Ingaas Vcsel's with Two-Sided Output." *Photonics Technology Letters, IEEE* 7, no. 7 (1995): 730-732.

[29] Kojima, K, RA Morgan, T Mullally, GD Guth, MW Focht, RE Leibenguth and MT Asom. "Reduction of P-Doped Mirror Electrical Resistance of GaAs/AlGaAs Vertical-Cavity Surface-Emitting Lasers by Delta Doping." Electronics Letters 29, no. 20 (1993): 1771-1772.

[30] Yang, X., M. Li, G. Zhao, Y. Zhang, S. Freisem, and D. G. Deppe. "Oxide-free vertical-cavity surface-emitting lasers with low junction temperature and high drive level." Electronics Letters 50, no. 20 (2014): 1474-1475.

[31] Yang, X., M. Li, G. Zhao, Y. Zhang, S. Freisem, and D. G. Deppe. "Small-sized lithographic single-mode VCSELs with high-power conversion efficiency." In SPIE OPTO, pp. 93810R-93810R. International Society for Optics and Photonics, 2015.

[32] Yang, X., M. Li, G. Zhao, S. Freisem, and D. G. Deppe "Small oxide-free vertical-cavity surface-emitting lasers with high efficiency and high power." Electronics Letters 50, no. 24 (2014): 1864-1866.

[33] Sale, T. E., “Vertical cavity surface emitting lasers,” PP 258-264, Wiley, 1995

[34] Herrick, R.W., Lim, S.F., Deng, H., Deng, Q., Dudley, J.J., Keever, M.R., Oh, T.H., Li, M.Y., Tashima, M., Hodge, L.A. and Zhang, X., "Highly reliable oxide VCSELs manufactured at HP/Agilent Technologies." In Symposium on Integrated Optoelectronics, pp. 14-19. International Society for Optics and Photonics, 2000.

[35] Al-Omari, A. N., G. P. Carey, S. Hallstein, J. P. Watson, G. Dang, and K. L. Lear. "Low thermal resistance high-speed top-emitting 980-nm VCSELs." IEEE Photonics Technology Letters 18, no. 11 (2006): 1225-1227.

[36] Zhao, G., Yang, X., Zhang, Y., Li, M., Deppe, D.G., Cao, C., Thorp, J., Thiagarajan, P. and McElhinnery, M., "Record Low Thermal Resistance of Mode-Confined Vcsels Using Alas/Algaas DBRs." In CLEO: Science and Innovations: Optical Society of America, 2013.

[37] Afromowitz, M. A. "Thermal conductivity of Ga1− xAlxAs alloys." Journal of Applied Physics 44, no. 3 (1973): 1292-1294.

[38] Demir, A, G Zhao and DG Deppe. "Lithographic Lasers with Low Thermal Resistance." Electronics letters 46, no. 16 (2010): 1147-1149.

[39] Al-Omari, AN, MS Alias, A Ababneh and KL Lear. "Improved Performance of Top-Emitting Oxide-Confined Polyimide-Planarized 980 Nm VCSELs with Copper-Plated Heat Sinks." Journal of Physics D: Applied Physics 45, no. 50 (2012): 505101.

[40] Al-Omari, AN and KL Lear. "Fabrication and Performance of Bottom-Emitting Flip-Chip Bonded 980 Nm Vertical-Cavity Lasers with Copper-and Indium-Plated Heat-Sinks." Semiconductor Science and Technology 26, no. 12 (2011): 125020.

[41] Al-Omari, AN, GP Carey, S Hallstein, JP Watson, G Dang and KL Lear. "Low Thermal Resistance High-Speed Top-Emitting 980-Nm Vcsels." Photonics Technology Letters, IEEE 18, no. 11 (2006): 1225-1227.

[42] Mathine, DL, H Nejad, DR Allee, R Droopad and GN Maracas. "Reduction of the Thermal Impedance of Vertical-Cavity Surface-Emitting Lasers after Integration with Copper Substrates." Applied physics letters 69, no. 4 (1996): 463-464.

[43] Safaisini, R., Joseph, J. R., and Lear, K. L. "Scalable High-Cw-Power High-Speed 980-Nm Vcsel Arrays." Quantum Electronics, IEEE Journal of 46, no. 11 (2010): 1590-1596.

[44] Wipiejewski, T, DB Young, MG Peters, BJ Thibeault and LA Coldren. "Improved Performance of Vertical-Cavity Surface-Emitting Laser Diodes with Au-Plated Heat Spreading Layer." Electronics Letters 31, no. 4 (1995): 279-281.

[45] Miyamoto, T., Nishina, T., Kashihara, Y., Ishida, S. and Koyama, F. "Thermal Resistance Reduction of Vertical-Cavity Surface-Emitting Lasers by Thickness-Modulated Distributed Bragg Reflector." Japanese Journal of Applied Physics 47, (2008): 6772.

[46] Lascola, K. M., W. Yuen, and C. J. Chang-Hasnain. "Structural dependence of the thermal resistance of vertical cavity surface emitting lasers." In Vertical-Cavity Lasers, Technologies for a Global Information Infrastructure, WDM Components Technology, Advanced Semiconductor Lasers and Applications, Gallium Nitride Materials, Processing, and Devi, pp. 79-80. IEEE, 1997.

[47] Lear, KL, KD Choquette, RP Schneider Jr, SP Kilcoyne and KM Geib. "Selectively Oxidised Vertical Cavity Surface Emitting Lasers with 50% Power Conversion Efficiency." Electronics Letters 31, no. 3 (1995): 208-209.

[48] Pu, R., Wilmsen, C.W., Geib, K.M. and Choquette, K.D. "Thermal resistance of VCSELs bonded to integrated circuits." IEEE Photonics Technology Letters 11, no. 12 (1999): 1554-1556.

[49] Chang, Y.C. and Coldren, L.A. "Efficient, High-Data-Rate, Tapered Oxide-Aperture Vertical-Cavity Surface-Emitting Lasers." Selected Topics in Quantum Electronics, IEEE Journal of 15, no. 3 (2009): 704-715.

[50] Guenter, J. K., Hawthorne III, R. A., Granville, D. N., Hibbs-Brenner, M. K., & Morgan, R. A. “Reliability of proton-implanted VCSELs for data communications.” Photonics West, 1996, International Society for Optics and Photonics.

[51] Hawthorne, R.A., Guenter, J.K., Granville, D.N., Hibbs-Brenner, M.K. and Morgan, R.A., "Reliability study of 850 nm VCSELs for data communications." In Proceedings of International Reliability Physics Symposium. 1996.

[52] Hawkins, B.M., Hawthorne, R.A., Guenter, J.K., Tatum, J.A. and Biard, J.R. "Reliability of various size oxide aperture VCSELs." In Electronic Components and Technology Conference, 2002. Proceedings. 52nd, pp. 540-550. IEEE, 2002.

[53] Herrick, R.W. "Oxide VCSEL reliability qualification at Agilent Technologies." In Symposium on Integrated Optoelectronic Devices, pp. 130-141. International Society for Optics and Photonics, 2002.

[54] Lowes, T.D. "VCSEL reliability research at Gore Photonics." In Symposium on Integrated Optoelectronic Devices, pp. 121-129. International Society for Optics and Photonics, 2002.

[55] Yang, X., Zhao, G., Li, M. and Deppe, D.G "Stress test of lithographic vertical-cavity surface-emitting lasers under extreme operating conditions." Electronics Letters 51, no. 16 (2015): 1279-1280.

[56] Kuchta, D. M., A. V. Rylyakov, C. L. Schow, J. E. Proesel, C. Baks, C. Kocot, L. Graham et al. "A 55Gb/s directly modulated 850nm VCSEL-based optical link." In Photonics Conference (IPC), vol. 2, pp. 1-2. 2012.

[57] P. Westbergh et al., “High-speed 850 nm VCSELs with 28 GHz modulation bandwidth operating error-free up to 44 Gbit/s”, Electronics Letters 48 (18), pp. 1145-1147 (2012).

[58] Li, N., Xie, C., Luo, W., Helms, C.J., Wang, L., Liu, C., Sun, Q., Huang, S., Lei, C., Jackson, K.P. and Carson, R.F, “Emcore’s 1 Gb/s to 25 Gb/s VCSELs”, Proc. SPIE vol. 8276, pp. 03-1 to 03-10 (2012).

[59] Chang, Y.C. and Coldren, L.A. "Efficient, high-data-rate, tapered oxide-aperture vertical-cavity surface-emitting lasers." IEEE Journal of Selected Topics in Quantum Electronics 15, no. 3 (2009): 704-715.

[60] Ou, Y., Gustavsson, J.S., Westbergh, P., Haglund, A., Larsson, A. and Joel, A., "Impedance characteristics and parasitic speed limitations of high-speed 850-nm VCSELs." IEEE Photonics Technology Letters 21, no. 24 (2009): 1840-1842.

[61] Haglund, E., Westbergh, P., Gustavsson, J.S., Haglund, E.P., Larsson, A., Geen, M. and Joel, A. "30 GHz bandwidth 850 nm VCSEL with sub-100 fJ/bit energy dissipation at 25–50 Gbit/s." Electronics Letters 51, no. 14 (2015): 1096-1098.

[62] Kuchta, D.M., Rylyakov, A.V., Schow, C.L., Proesel, J.E., Baks, C.W., Westbergh, P., Gustavsson, J.S. and Larsson, A., "A 50 Gb/s NRZ modulated 850 nm VCSEL transmitter operating error free to 90 C." Journal of Lightwave Technology 33, no. 4 (2015): 802-810.

[63] D. M. Kuchta, A. V. Rylyakov, F. E. Doany, C. L. Schow, J. E. Proesel, C. W. Baks, P. Westbergh, J. S. Gustavsson, and A. Larsson, "A 71-Gb/s NRZ Modulated 850-nm VCSEL-Based Optical Link," IEEE Photonics Technology Letters, Vol. 27, No. 6 (2015).

[64] Moser, P., J. A. Lott, P. Wolf, G. Larisch, H. Li, and D. Bimberg. "Error-free 46 Gbit/s operation of oxide-confined 980 nm VCSELs at 85 C." Electronics Letters 50, no. 19 (2014): 1369-1371.

[65] Li, M., X. Yang, N. Cox, J. Beadsworth and D.G. Deppe. "Record Low Differential Resistance Using Lithographic VCSELs." In CLEO: QELS_Fundamental Science, pp. JTh2A-49. Optical Society of America, 2016.

[66] Larsson, A., P. Westbergh, J. Gustavsson and Å. Haglund. "High-speed low-current-density 850 nm VCSELs." In OPTO, pp. 761505-761505. International Society for Optics and Photonics, 2010.

[67] Westbergh, P., High speed vertical cavity surface emitting lasers for short reach communication. Chalmers University of Technology, 2011.

[68] Lu, C.Y., S.L. Chuang, A. Mutig and D. Bimberg. "Metal-cavity surface-emitting microlaser with hybrid metal-DBR reflectors." Optics letters 36, no. 13 (2011): 2447-2449.

[69] Deng, H., Q. Deng, and D. G. Deppe. "Very small oxide-confined vertical-cavity surface-emitting lasers with a bulk active region." Applied physics letters 70, no. 6 (1997): 741-743.

[70] Li, M. Intrinsic Modulation Response Modeling and Analysis for Lithographic Vertical-Cavity Surface-Emitting Lasers. University of Central Florida, 2016.