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Design And Characterization Of High Temperature Packaging For Wide-bandgap Semiconductor Devices

Brian Grummel
University of Central Florida

DESIGN AND CHARACTERIZATION OF HIGH-TEMPERATURE PACKAGING FOR WIDE-BANDGAP SEMICONDUCTOR DEVICES

by

BRIAN J. GRUMMEL
B.S.E.E. University of Central Florida, 2007
M.S.E.E. University of Central Florida, 2008

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ABSTRACT

Advances in wide-bandgap semiconductor devices have increased the allowable operating temperature of power electronic systems. High-temperature devices can benefit applications such as renewable energy, electric vehicles, and space-based power electronics that currently require bulky cooling systems for silicon power devices. Cooling systems can typically be reduced in size or removed by adopting wide-bandgap semiconductor devices, such as silicon carbide. However, to do this, semiconductor device packaging with high reliability at high temperatures is necessary. Transient liquid phase (TLP) die-attach has shown in literature to be a promising bonding technique for this packaging need. In this work TLP has been comprehensively investigated and characterized to assess its viability for high-temperature power electronics applications. The reliability and durability of TLP die-attach was extensively investigated utilizing electrical resistivity measurement as an indicator of material diffusion in gold-indium TLP samples. Criteria of ensuring diffusive stability were also developed. Samples were fabricated by material deposition on glass substrates with variant Au–In compositions but identical barrier layers. They were stressed with thermal cycling to simulate their operating conditions then characterized and compared. Excess indium content in the die-attach was shown to have poor reliability due to material diffusion through barrier layers while samples containing suitable indium content proved reliable throughout the thermal cycling process. This was confirmed by electrical resistivity measurement, EDS, FIB, and SEM characterization. Thermal and mechanical characterization of TLP die-attached samples was also performed to gain a newfound understanding of the relationship between TLP design parameters and die-attach properties. Samples with a SiC diode chip TLP bonded to a copper metalized silicon nitride

substrate were made using several different values of fabrication parameters such as gold and indium thickness, Au–In ratio, and bonding pressure. The TLP bonds were then characterized for die-attach voiding, shear strength, and thermal impedance. It was found that TLP die-attach offers high average shear force strength of 22.0 kgf and a low average thermal impedance of 0.35 K/W from the device junction to the substrate. The influence of various fabrication parameters on the bond characteristics were also compared, providing information necessary for implementing TLP die-attach into power electronic modules for high-temperature applications. The outcome of the investigation on TLP bonding techniques was incorporated into a new power module design utilizing TLP bonding. A full half-bridge inverter power module for low-power space applications has been designed and analyzed with extensive finite element thermo-mechanical modeling. In summary, TLP die-attach has investigated to confirm its reliability and to understand how to design effective TLP bonds, this information has been used to design a new high-temperature power electronic module.

This dissertation is dedicated to my family.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

AC.....Alternating Current

AES.....Auger Electron Spectroscopy

AlN.....Aluminum Nitride

DBC .....Direct Bonded Copper

DC.....Direct Current

EDS.....Energy Dispersive Spectroscopy

IGBT .....Insulated Gate Bipolar Transistor

JBS .....Junction-Barrier Schottky

MOSFET.....Metal-Oxide-Semiconductor Field Effect Transistor

MPS.....Merged PiN Schottky

RF.....Radio Frequency

SEM .....Scanning Electron Microscope

Si_3N_4.....Silicon Nitride

SiC.....Silicon Carbide

SLID.....Solid Liquid Inter-Diffusion

TLP .....Transient Liquid Phase

WBG .....Wide-Bandgap

LIST OF VARIABLES

χ_{In} .....Atomic Fraction of Indium

ρ_{bond} .....Bonding Pressure

$D_{\%}$ .....Die-Attach Percentage

V_F .....Forward Voltage

λ_0 .....Mean Free Path

ρ_T .....Resistivity, Total

t_{In} .....Thickness, Indium

Z_{th} .....Thermal Impedance

τ_{sh} .....Ultimate Die Shear Strength

τ_{shf} .....Ultimate Die Shear Force

CHAPTER 1: INTRODUCTION

1.1 Motivation

Wide-bandgap power semiconductor devices, such as silicon carbide (SiC) diodes and MOSFETs, are now beginning to enter the power electronics marketplace which allow for improved power electronics performance. These wide-bandgap devices differ from silicon devices because of a wider energy bandgap which reduces the intrinsic carrier concentration and increases dielectric strength. These traits allow for lower power losses, higher efficiency, higher thermal conductivity, and much higher temperature operation capabilities than silicon [1–3]. Higher temperature capability is a critical improvement, with it there is increased potential for high-temperature applications that were previously impractical due to the low heat tolerance of silicon devices which must operate below 175 °C. A low temperature constraint requires the use of large cooling systems and bulky packaging modules for keeping the devices and critical packaging components cool so that they may operate reliability. Even still, they typically have short module life spans when operating in extreme environments where even possible. Wide-bandgap devices, however, demonstrate high-temperature capability with prolonged 500 °C operation demonstrated [3].

The benefits of these devices will allow for new applications of power electronics in a variety of applications. Exploration into deeper, higher-temperature down-hole well locations is now possible in the energy industry due to increasing access to difficult-to-reach natural resources. Geothermal energy will become more feasible to harness also, as it has been difficult to capture to date because it is inherently in the highest-temperature locations within the earth's

crust [4]. Overall system efficiency can increase in renewable energy power conversion and in electric vehicles by allowing for device operation at higher temperatures and reducing the power electronics' cooling systems to simple passive cooling methods. Wide-bandgap devices can also extend space exploration possibilities by reducing the need for warming and cooling boxes to house sensitive electronic components on satellites [5], [6].

Advanced packaging techniques are required, however, to implement high-temperature wide-bandgap devices into these and other applications. To transition to new packaging and allow the temperature to rise, the packaging must evolve using advanced packaging techniques to utilize wide-bandgap devices' full temperature range. Standard packaging technology is designed for silicon device temperatures and thus confines high-temperature device capabilities. Die-attach technology, which bonds the semiconductor device to a metalized substrate, is a critical need in the development of any new advanced packaging.

To achieve this, transient liquid phase (TLP) bonding is promising for die-attach due to its high-temperature capability equal to those of wide-bandgap devices [7–10]. There are many advantages of TLP bonding over alternative high-temperature die-attach techniques (e.g., brazing and silver sintering paste) including low thermal resistance due to its micrometer scale thickness and high thermal conductivity, lead-free capability, high mechanical strength, low mechanical stresses, and a simple bonding procedure with no binders to remove. TLP bonding die-attach and modern wide-bandgap power modules must be further investigated before major advances in packaging reliability, system reliability, and power electronic system size reduction becomes a reality.

1.2 Statement of Benefit

This work is unique because it advances TLP die-attach research and understanding to assist wide-bandgap semiconductor devices, such as SiC, for their inclusion into high-temperature applications such as electric vehicles and renewable energy. This is primarily accomplished by the first known comparison and assessment of important TLP design parameters. This is unlike from any other previously done TLP analysis because a critical analysis of the fabrication of TLP die-attach bonds has been done and compares the fabrication parameters used in their design. This analysis is then used to realize dependencies and relationships of the success and failure of the bonds to their design to draw conclusions on creating better TLP bonds. This information will be invaluable to research and industry in the high-temperature packaging field by providing a greater understanding of how to design TLP bonds aside from already known information such as which materials can be used to create them.

Most TLP investigation prior to this one in the growing field of electronic packaging has amounted to "proof of concept" works in which the authors design and create a TLP bond then present a single characterization proving only that a bond was created. This leaves the reader to know only that a TLP bond was made but little more, and without any detailed knowledge of what contributed to the success or failure of the bond. This work highlights the design process as well as the characterization of several completed bonds in multiple designs to give a strong understanding of the role of important fabrication parameters. This is done by creating several bonds using the same design process with variation of only important parameters that are under inspection. Each of the design parameters are characterized for that particular parameter's importance to the design process and it is learned and shown how each of them affects TLP die-attach properties. This analysis has never before been seen.

Previous works typically used only one of a multitude of different characterization techniques, which again leaves the reader confused as to which bonds are actually of higher quality. In this work, several characterization of each design parameter are done so that the importance of each design parameter is known both mechanically and thermally through the use of scanning acoustic microscopy (C-SAM) for voiding analysis, die shear testing to measure shear strength, and peak junction temperature measurement for thermal impedance characterization. This work also performs several reliability inspections of TLP die-attach unlike any work prior. This includes a unique detection of unwanted diffusion within the bond in response to degradation using measurement of electrical resistivity. The durability of TLP thermal properties are investigated as well for the first known time.

TLP die-attach is in need of a refocus to lead it to implementation in high-temperature packaging and unleash wide-bandgap devices into important high-temperature applications. This work advances TLP die-attach past proof of concept work with a roadmap to design refinement and application.

1.3 Wide-Bandgap Semiconductors

Wideband-gap semiconductors are defined by having a wider gap between the conduction and valence bands in the energy band diagram of the material than silicon. This typically results in more favorable material and device properties such as a lower intrinsic carrier concentration, higher dielectric voltage strength, and higher electron saturation velocity. This causes higher temperature operation ability, higher breakdown voltage, lower on-resistance, and faster switching for the devices created within them, which have the same basic structures as silicon such as diodes, MOSFETs, and IGBTs.

There are several wide-bandgap semiconductor materials that can be used for devices and among them SiC is the most well developed for power device. SiC devices have been in production for decades with improvement demonstrated in the early 1990s by North Carolina State University researchers who went on to found today's preeminent SiC substrate and device manufacturer Cree, Inc. (who supplied this project with SiC devices) [11]. It took many years for the devices to show reliability after initial proof-of-concept demonstrations but they improved in the mid-2000s with continuous high-temperature operation of first MESFETs then later diodes and MOSFETs. Development delays were rooted in substrate improvement to create pure single crystal substrates without micro-pipes or stacking faults which made devices unreliable. Eventually, low current power diodes were released in 2001 by Infineon to much fanfare and a decade later SiC MOSFETs entered the marketplace in January 2011 by Cree [12], [13].

There remain many other wide-bandgap materials which feature several key differences in material and device property from traditional silicon devices. Those properties are detailed in this section.

1.3.1 Material

There are a several wide-bandgap semiconductor materials each with unique properties making some better for certain application, some less. Table 1.1 gives a succinct overview of the material properties of each major wide-bandgap material. It contains promising new materials, current ones, and past technologies such as germanium, the first semiconductor prototype ever produced [14]. Gallium arsenide (GaAs) may be the most common wide-bandgap device material in use today owing to its high electron mobility μ_n which allows for very high switching speeds. This makes it very useful for high frequency communications such as mobile phones and

other communication industries. There are several different material properties each having distinct changes on the operation of a device built in that material [15].

Table 1.1 – Wide-Bandgap Semiconductor Properties

Material	Bandgap, E_g (eV)	Intrinsic Carrier Con., $n_{i,\ 300K}$ (cm^{-3})	Perm., ε_r	Electron Mobility, μ_n (cm^2/Vs)	Field Strength, E_c (MV/cm)	Elec. Sat. Velocity, v_s (10^7 cm/s)	Thermal Cond., λ (W/cm-K)	Bandgap Type
Si	1.1	1.5E10	11.8	1350	0.3	1.0	1.5	I
SiC (4H)	3.26	8.2E-9	10	~700	2.0	2.0	4.5	I
GaAs	1.4	1.8E6	12.8	8500	0.4	2.0	0.5	D
GaP	2.3	7.7E-1	11.1	350	1.3	1.4	0.8	I
InN	1.86	~1E3	9.6	3000	1.0	2.5	-	D
GaN	3.39	1.9E-10	9.0	900	3.3	2.5	1.3	D
C	5.45	1.6E-27	5.5	1900	5.6	2.7	20	I
BN	6.0	1.6E-31	7.1	5	10	1.0	13	I
AlN	6.1	~1E-31	8.7	110	11.7	1.8	2.5	D
Ge	0.66	2.4E13	16.0	3900	0.1	0.5	0.6	I

1.3.2 Bandgap

The bandgap E_g describes the separation of the valance and the conduction band in the semiconductor energy band diagram. For an electron-hole pair of free carriers to be created, an electron must cross the bandgap from the valance band E_v to the state of higher energy the conduction band E_c. The bandgap is described in electron volts as the amount of energy that an electron must gain to cross the energy bandgap. This energy commonly arrives thermally, thus for a wider bandgap at an equal temperature fewer electron hole pairs will be formed and there will be fewer mobile charge carriers formed in the semiconductor. These are intrinsic carriers which are described in the next section.

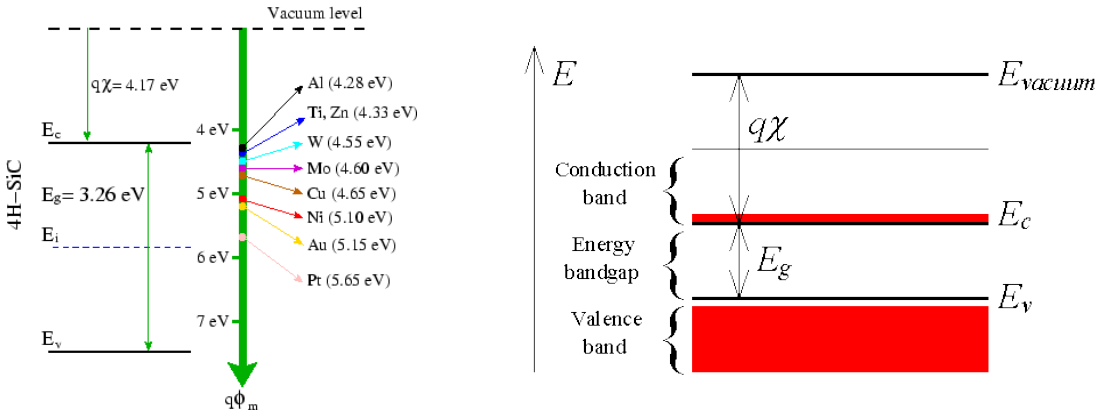

Figure 1.1 – Energy band diagram of 4H-SiC material

Bandgap may be described as direct or indirect. This corresponds to the valence and conduction bands versus the wave number k by taking the energy band diagram into the third dimension. Regardless of E_V or E_C vs. k, the bandgap is measured typically from the lowest energy of E_C to the highest magnitude of E_V, if these points happen to be at the same wave number then the material is known to have a direct bandgap and the electrons and hole transfer

more directly at the same wave number. These materials have lower carrier lifetimes leading to faster devices [16]. Direct bandgap semiconductors also emit energy as a photon thus releasing light when electrons cross the bandgap. Silicon and SiC are both indirect bandgap semiconductors thus alternative wide-bandgap semiconductors are needed in the area of lasers and optics [17].

1.3.3 Intrinsic Carrier Concentration

Intrinsic carrier concentration n_i is the average amount of electron hole pairs in an unbiased semiconductor per unit volume. It is a function of E_g and temperature by

$$n_i = \overline{N_c N_v} \exp\left(\frac{-E_g}{2kT}\right) \left(\frac{1}{cm^3}\right), \tag{1.1}$$

where

$$N_c = 2\left(\frac{2\pi m_e^* kT}{h^2}\right)^{\frac{3}{2}} \tag{1.2}$$

and

$$N_v = 2\left(\frac{2\pi m_h^* kT}{h^2}\right)^{\frac{3}{2}} \tag{1.3}$$

in which m_e* and m_h* are the effective mass of an electron and hole, respectively [16]. It can be assumed m_e*=m_h* for simplification, thus,

$$n_i = 2\left(\frac{m^* kT}{2\pi h^2}\right)^{\frac{3}{2}} \exp\left(\frac{-E_g}{2kT}\right) \left(\frac{1}{cm^3}\right). \tag{1.4}$$

It can be seen in Table 1.1 that as the bandgap increases, n_i begins to reduce drastically, which is desirable. SiC carrier concentration is observed to be 18 orders of magnitude lower than silicon at n_i = 8.2E-9 cm^{-3}. A few electron volts have a dramatic impact on its value in silicon and SiC because n_i has an exponential relationship to E_g [18]. Carrier concentration is dependent on also temperature, as defined by (1.4), thus devices become ineffective at higher temperatures because of excess free carriers. SiC maintains n_i much lower than silicon up to very high temperatures, within the range of most high-temperature electronic applications, as seen in Figure 1.2 [19]. This constraint limits silicon device operation to 125 °C before the intrinsic carriers dominate, but SiC devices have been demonstrated to constant operation at 500 °C [3].

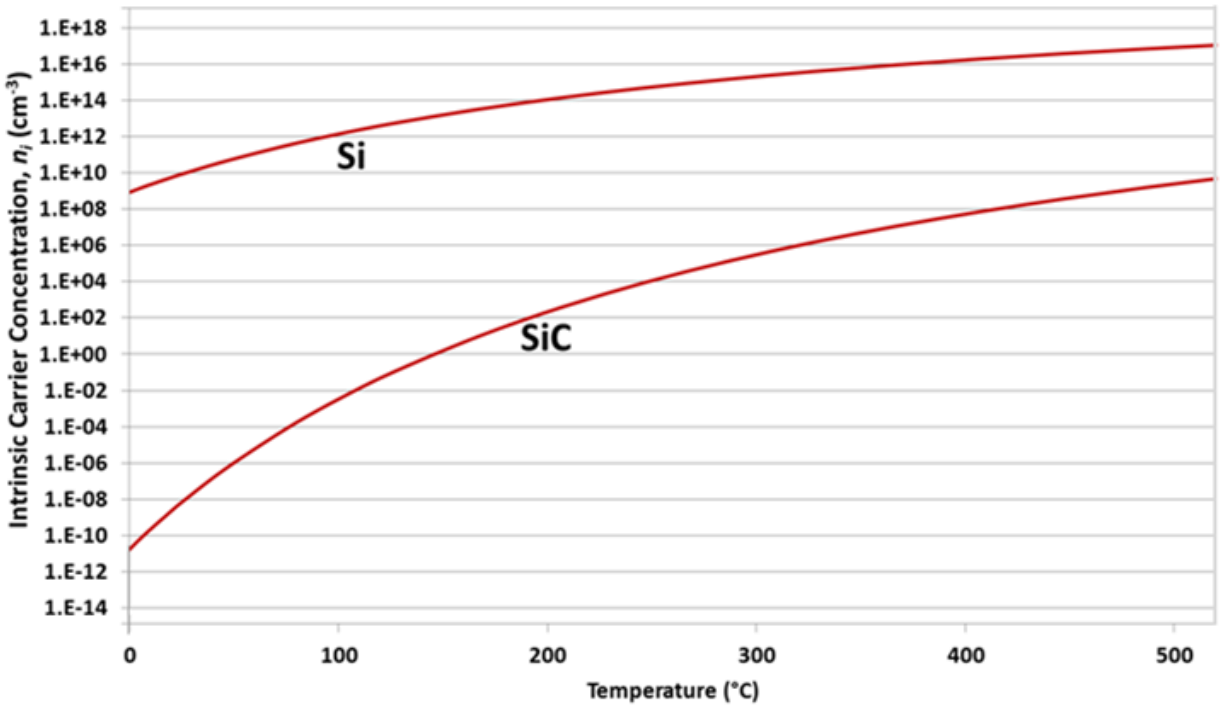

Figure 1.2 – Intrinsic carrier concentration versus temperature in silicon and SiC material

1.3.4 High-Temperature Capability

Lower intrinsic carrier concentrations in wide-bandgap materials facilitate higher temperature operation. Lower n_i equates to fewer minority carriers in devices which often contribute to loss due to increased body currents and also can trigger BJT latch-up within the device. These losses increase with temperature until operation is no longer possible, however with a lower n_i, peak temperature increases several hundred of degrees Celsius, depending on device type and failure mechanism.

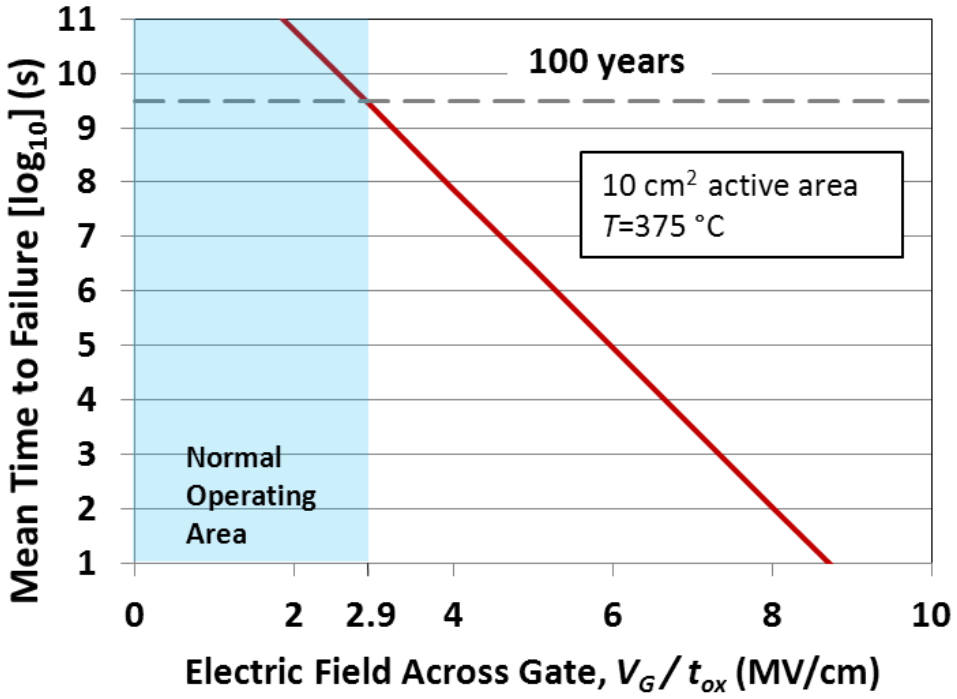

Figure 1.3 – SiC oxide reliability shown by mean time to failure (MTTF)

Poor reliability of the gate oxide has been one of the principal impediments to the implementation of WBG devices, specifically SiC, at high temperature. SiC has the benefit over other WBG materials of the capability to grow native SiO_2 on the surface. However, it has a lower conduction band offset than Si–SiO_2, also the effective barrier height of this junction is reported to lower with temperature and increase leakage. Altogether, SiC devices were not

thought to be reliable over 250 °C [20]. This understanding has changed with new experimental data of increased oxide quality on SiC showing that gate oxides can withstand 375 °C for 100 years at up to 2.9 MV/cm of field across it as shown in Figure 1.3 [21].

1.3.5 Electric Field Strength

A material's dialectic, or electric field, strength E_C is the greatest determinant of its voltage blocking capability. For silicon, E_C = 0.3 MV/cm and in SiC E_C is an order of magnitude higher at 3.18 MV/cm [22]. This is due to the dependence of E_C on the bandgap as described by

$$E_c = 1.02 \times 10^7 \ \frac{\bar{q}}{\epsilon} N_B^{1/8} E_g^{3/4}. \tag{1.5}$$

This relationship is presented in Figure 1.4 showing increasing E_C with E_g for multiple wide-bandgap semiconductor materials [23]. Increased electric field strength directly relates to the breakdown voltage of a device fabricated in it.

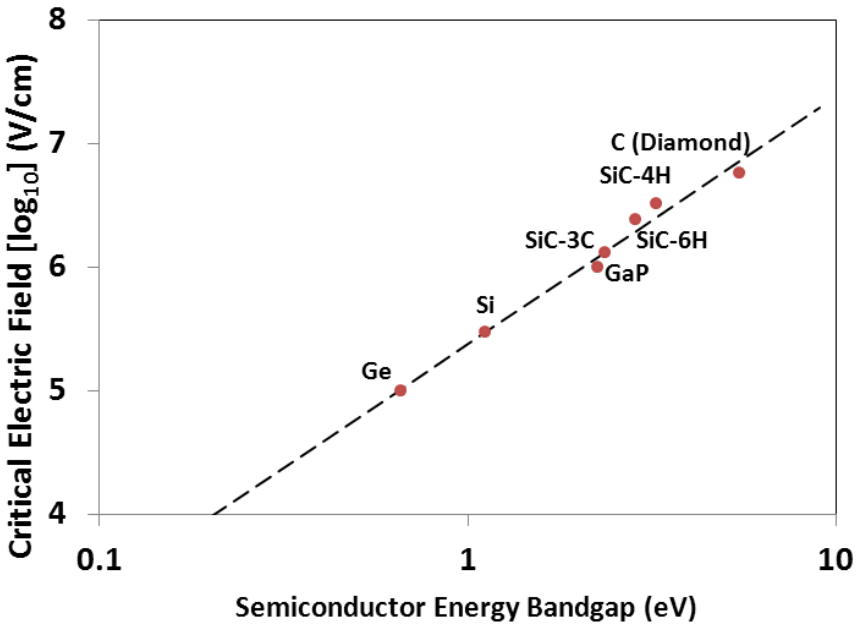

Figure 1.4 – Relationship of electric field strength to energy bandgap in semiconductor materials [23]

1.3.6 Breakdown Voltage

The breakdown voltage V_{BV}, or blocking voltage, is the voltage up to which a device blocking junction will block the in reverse bias, preventing current flow in the opposing direction or when off. This is typically a PN junction as in MOSFETs, IGBTs, and JBS diodes, however it maybe a metal semiconductor junction as in a Schottky or JBS rectifier. The breakdown is determined by two important factors; one is a static material property, the E_C, the other is a design dimension, the background doping concentration N_A of the drift region, as seen in Figure 1.5 [24]. A depletion region predominantly forms in the lightly doped drift region as voltage is applied to the junction, more so than in the N or P well where the inversion channel is formed. Lower N_A causes a greater depletion region width leading to a lower voltage gradient ($^{dV}/_{dx}$). This gradient must be higher than the E_C or the device will no longer block current. There is a direct relationship between blocking voltage and doping concentration in non-punch through devices as shown in Figure 1.6. Devices with higher rated blocking voltages have wider more lightly doped drift regions. Because wide-bandgap materials have much higher E_C, they may have much higher V_{BV} across a thinner drift region than silicon [1].

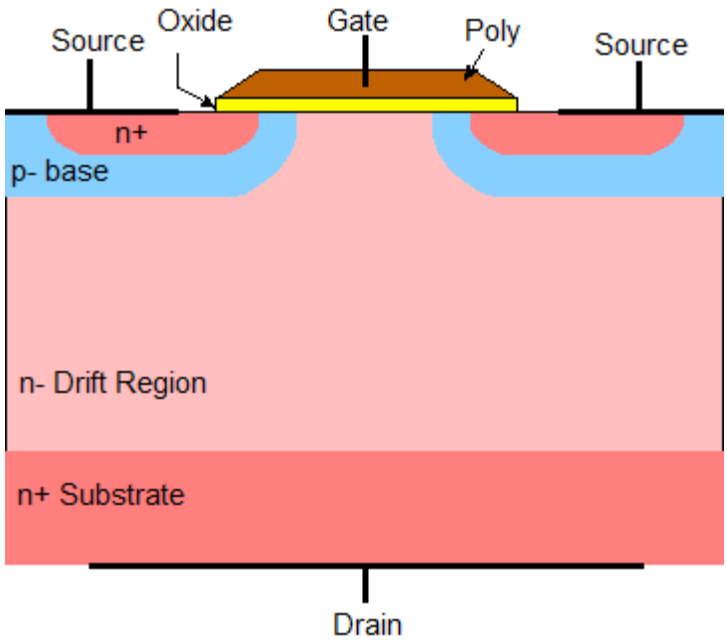

Figure 1.5 – DMOS device structure [24]

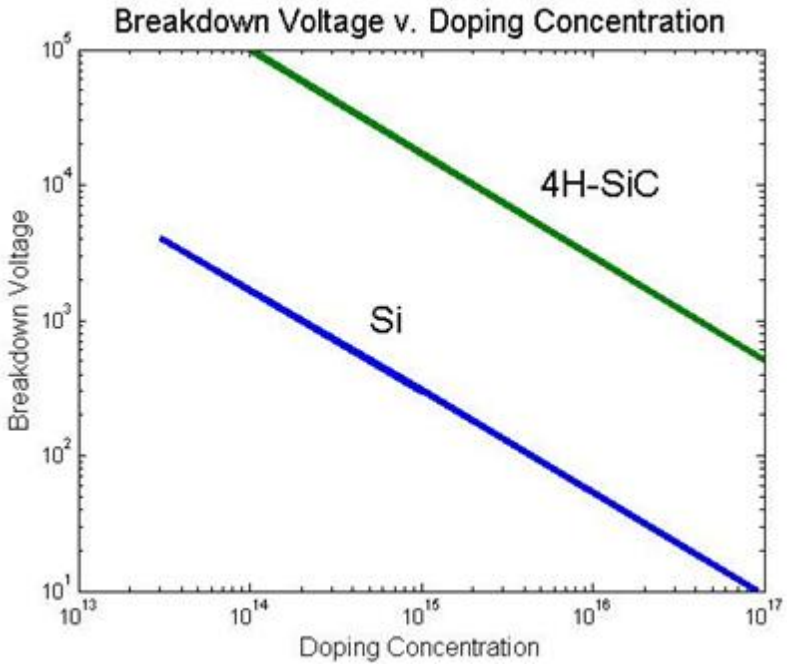

Figure 1.6 – Breakdown voltage versus doping concentration in silicon and SiC materials [1]

1.3.7 Specific On Resistance

High electric field strength is a great advantage to specific on resistance $SpR_{DS,on}$ of wide-bandgap devices as well. $SpR_{DS,on}$ is the resistance, normalized by area, through an on state device at a certain gate voltage. The high electric field strength allows for manipulation of the two primary design dimensions that determine $SpR_{DS,on}$: N_A and the drift region width. Decreasing N_A to increase V_{BV} also increases $SpR_{DS,on}$. However, since E_C is higher in wide-bandgap material, N_A may be increased with much higher V_{BV} than silicon devices. This is because greater depletion doping keeps the region thinner with an equal or higher breakdown voltage. Thus the drift region may be designed much thinner which causes a reduction in $SpR_{DS,on}$ since majority carriers pass through a shorter distance from drain to source. Similar to Figure 1.6, the $SpR_{DS,on}$ is linked to N_A as seen in Figure 1.7 [25]. SiC devices have shown $R_{DS,on}$ up to 200 X smaller for comparable silicon devices with the same V_{BV} [26].

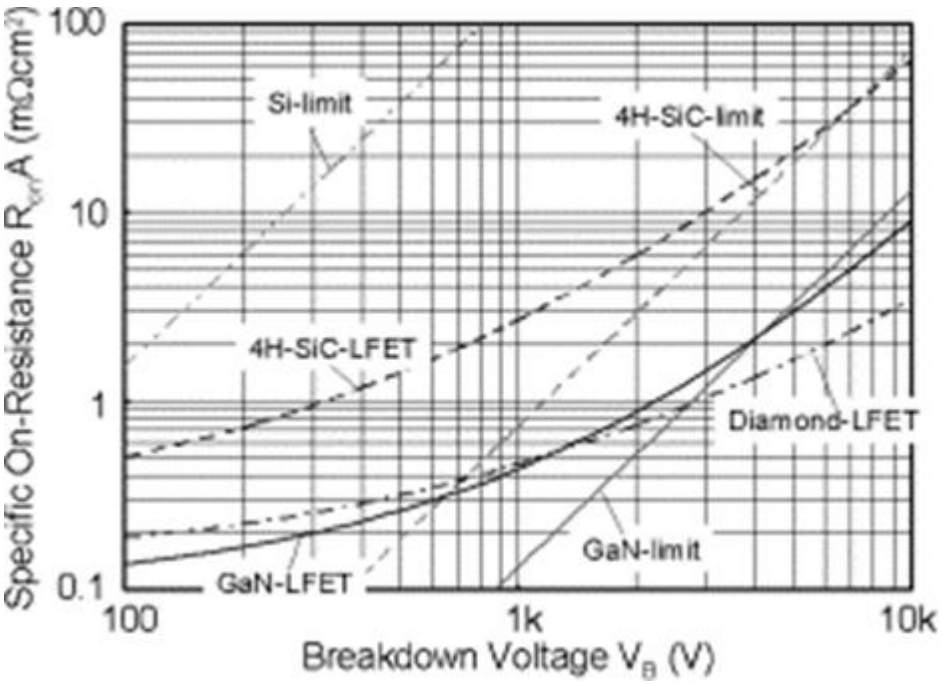

Figure 1.7 – Specific on-resistance of semiconductors vs. breakdown voltage [25]

1.3.8 Mobility

Electron mobility μ_n also varies in wide-bandgap material from silicon. It is lower in some wide-bandgap semiconductors, including SiC, which is a disadvantage unlike so many other wide-bandgap material properties. The lower mobility in SiC and GaN does raise $SpR_{DS,on}$ for comparably designed silicon devices, however the effect is largely neutralized because in actual devices the $SpR_{DS,on}$ is lower by the shortened drift region. This makes bipolar devices less practical in SiC because of the decreased mobility of the minority carriers in addition to the already low $R_{DS,on}$ of single carrier devices [16]. SiC suffers less from mobility degeneracy at high doping concentrations, however, where it is actually higher than silicon for $N_D > 3\text{E}17$ [1].

1.4 High-Temperature Power Electronic Applications

There are several applications for power electronics that must endure high temperatures that can be enhanced by wide-bandgap devices and new packaging. All power electronics are inherently associated with high temperatures because the high currents and voltages they operate at in conjunction with their higher on-resistances create a great deal of heat loss which must be removed from the device. This is difficult for some applications however due to a high ambient temperature around the system such as in space applications or because the cooling system required to keep the devices cool is a large hindrance to overall system performance such as in an electric vehicle.

The benefits of these devices will allow for new applications of power electronics in a variety of fields. Exploration into deeper, higher-temperature well locations is now possible in the energy industry due to increasing access to difficult-to-reach natural resources. Geothermal energy will become more feasible to harness also, as it has been difficult to capture to date

because it is inherently in the highest-temperature locations within the earth's crust [4]. Overall system efficiency can increase in renewable energy power conversion and in electric vehicles by allowing for device operation at higher temperatures and reducing the power electronics' cooling systems to simple passive cooling methods. Wide-bandgap devices can also extend space exploration possibilities by reducing the need for warming and cooling boxes to house sensitive electronic components on satellites [5], [6].

1.4.1 High Power, High Ambient Temperature Limitation

Some power electronics are required to operate in harsh environments which have no ambient environment available to base a cooling system in that can keep silicon devices below their 175 °C rating. Eqn. (1.6) shows the maximum power loss P_{loss} of a device based on $T_{j,max}$ of the device, the ambient temperature of the cooling environment T_{amb}, and the total thermal resistance from device to ambient $R_{\theta JA}$ by [27]

$$P_{loss} = \frac{T_{j,max} - T_{amb}}{R_{\theta JA}}, \tag{1.6}$$

which gives $T_{j,max}$ as a function of T_{amb} by,

$$T_{j,max} = P_{loss} \cdot R_{\theta JA} + T_{amb}. \tag{1.7}$$

This suggests that T_{amb} cannot exceed a device's maximum temperature rating nor can it approach it without considering the temperature rise due to P_{loss}. This type of situation is excellent to employ wide-bandgap devices such as underground energy exploration, geothermal

energy, or oil well logging. Space based electronics also lack a cool ambient environment which inhibits satellites' ability to house sensitive electronic components.

1.4.2 Down-Hole Energy Extraction

Geothermal energy is a very promising energy source which only requires very high underground temperatures and has been aided in development by oil well drilling. It is a stable renewable energy supply that does not fluctuate in weather and has the potential to provide over 10 % of the country's total energy demands with 100 GW of capacity. The process of geothermal energy harvesting is simple. Instead of traditional energy production techniques where a heat source is created to heat water to drive steam through turbines which create energy; the heat source is natural underground heat present within the earth where temperatures reach thousands of degrees Celsius. There is enough geothermal energy to heat water to the required temperatures of 250–300 °C if one digs up to 10 km down anywhere in the United States [28].

To harness this energy, two wells are dug, one is the injection well which pumps water down into the earth, the second well is the production well from which the heated water rises into turbines which produce electricity [29]. This simple system has been advanced in recent years to enhanced geothermal systems (EGS) in which the heated rocks in the ground are intentionally cracked and fractured. This creates more surface area on them to more efficiently heat water pumped in to produce steam. New geothermal systems are typically closed systems where the extracted hot water is pumped back down to keep output water temperatures high and water consumption down, as seen in an EGS well is shown in Figure 1.8. Temperature typically need to be 250 °C or higher, depending on depth, for geothermal plants to be practical with higher temperatures at shallow depths best. The western United States is largely more practical than the

eastern region, along with areas near tectonic fault lines or historic volcanic areas. However with the advent of more durable high-temperature devices and packaging this would no longer be a prerequisite [30].

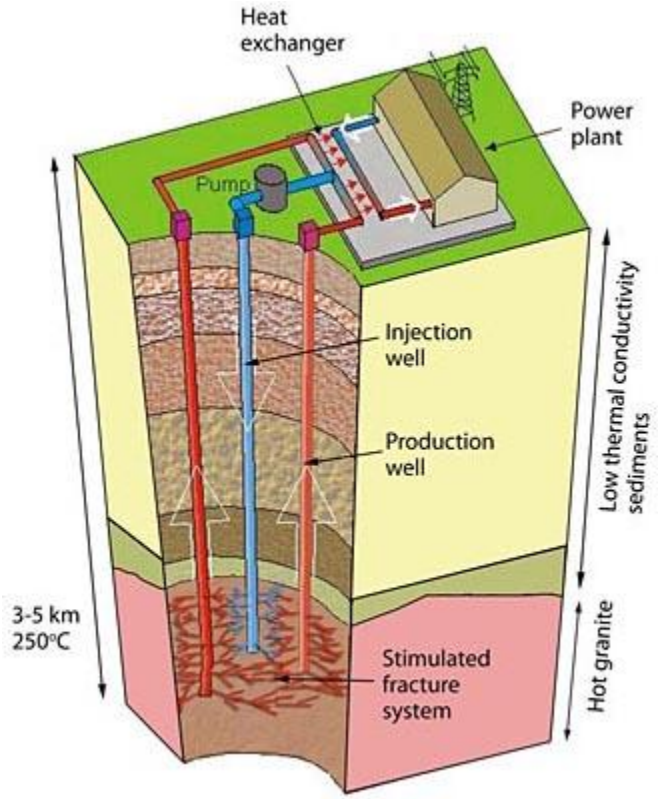

Figure 1.8 – Diagram of EGS geothermal plant and well [29]

Underground rock formations must be well characterized for geothermal extraction and well digging, and also to properly asses the area's capability for geothermal energy. This is similar in the oil industry, in a process known as oil well logging. This is where the opportunity for high-temperature devices and packaging are greatest. Many sensors are required which draw a sizable power supply to operate in these extreme temperatures for extended periods of time to characterize wells. Electronics are required during the drilling of the wells also. Although oil

wells do need to be in high-temperature rock formations, as required for geothermal, newly tapped oil wells are typically in higher and higher temperature locations since oil in shallow low temperature locations is being depleted. Increased temperature capability of oil discovery and collection would be very beneficial.

Currently, most electronics are protected by Dewar flasks that provide a heat shielded environment around electronic though the use of a vacuum for a fixed period of time. They have a maximum temperature of 400 °C and can protect electronics at 300 °C for 4-12 hours before failure or a return to the surface. There are currently no long term monitoring sensors to operate continuously in all parts of wells [31]. Silicon-On-Insulator (SOI) is a common high-temperature resilient fabrication and design technique with silicon electronics that has been necessary for existing higher temperature technologies. SOI incorporates a buried insulator, such as SiO_2, to block the increased leakage current that rises with temperature, however it does not match SiC and other wide-bandgap semiconductor's capabilities.

1.4.3 Reduced Cooling Capacity Systems

A need to reduce overall system size and weight can be accomplished by reducing the cooling system mass. Transportation vehicles of all kinds, such as hybrid-electric automobiles and airplanes, are relatively small working environment for high density high power electronics which make cooling a challenge. Also, transportation power electronics must be physically carried by the vehicle thus the weight of the electronics and the cooling system is a factor in overall system efficiency. There are two cooling loops in some hybrid vehicles, one for the engine and a separate loop just for active cooling electronics. By reducing the cooling system or removing it in favor of passive cooling the load can be lightened considerably [27].

1.4.4 Higher Efficiency Systems

Most renewable power electronic systems require all efficiency and power system capital cost savings possible. Wide-bandgap devices in high-temperature packaging are attractive for this reason because they offer the efficiency improvements of SiC and the reduced system capital cost of high-temperature ability by not utilizing a cooling system. Unlike high-temperature environment applications or those with reduced cooling capability, renewable energies often are able to have a cooling system easily installed. However, they are competing fiercely in the marketplace with existing energy sources as they develop and would benefit by shedding a potentially sizable cooling system considering the large amount of power electronics required to perform a host of energy conditioning tasks in converting their variable DC power into grid-ready 120 V AC. By removing their cooling system this will reduce the high initial capital costs that currently plague renewable energies, as seen in

Figure 1.9, [32]. This would likely also reduce operations and maintenance costs and further increasing the competitiveness of renewable energies.

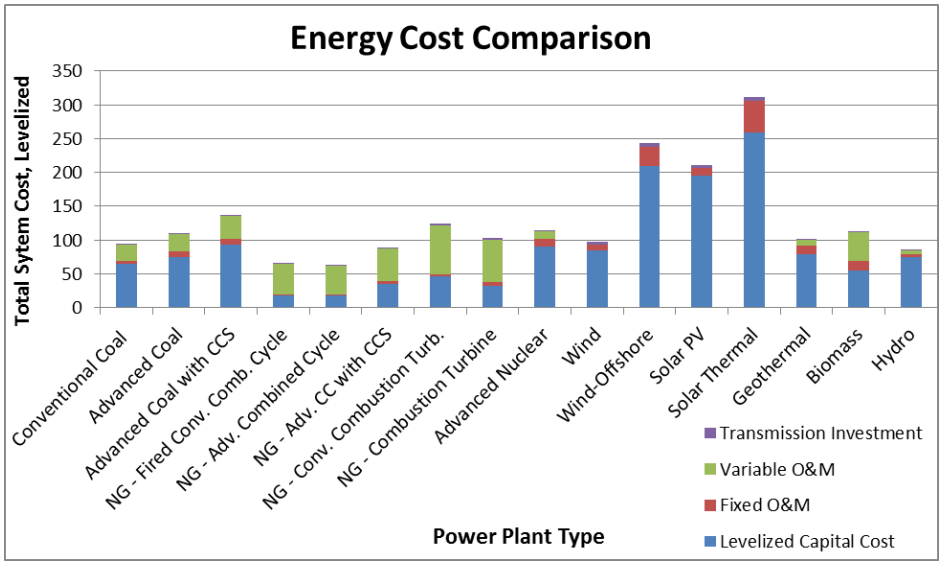

Figure 1.9 – Comparison of normalized energy costs for multiple sources as a culmination of capital costs, operations, maintenance, and transmission [32].

CHAPTER 2:
REVIEW OF HIGH-TEMPERATURE PACKAGING PRIOR ART

This work strives for advancement in the field of high-temperature power packaging. A focus of prior work in the field is on large conventional half-bridge power modules containing only a few high-current, high-powered devices which are still the primarily power module used today. With SiC device beginning to enter the marketplace, these modules typically contain silicon devices and are built for the low temperature range of silicon electronics (< 150 °C). Another packaging focus has been for high-temperature transportation applications, and other demanding environments which are also discussed, but not always used for high-power devices. This packaging employs other high-temperature die-attach materials that prelude TLP bonding along with high-temperature silicon devices.

2.1 Conventional Power Module

The conventional power module contains two switching devices, typically IGBTs, and two anti-parallel diodes to form a half-bridge circuit. Although the circuitry is simple, the packaging design is not because it must withstand large temperature changes over its lifecycle and allow for the removal of large amounts of energy losses with a high thermal conductivity design.

The insulated gate bipolar transistor (IGBT) power module is an extremely popular component in power applications. There is currently an industry standard design for the half-bridge power module with silicon IGBT devices as the switching device and freewheeling anti-parallel diodes seen in Figure 2.1. The design became common in the early 1990s as the IGBT

became more popular in the market place [33]. The IGBT can be used in much greater power densities than the MOSFET at low frequencies due to its low conduction losses.

The half-bridge design is designed to produce a sinusoidal output wave with an inductive load from a DC supply voltage. It is useful for motor control applications and it is typically found in trains, electric vehicles, and other traction devices. These fields are expected to grow for the foreseeable future with rising demand for electric powered transportation due to its environmentally friendly potential. This places an added importance on packaging design. The circuit is also used in high voltage power transmission and can be used to produce a DC voltage output in a buck or boost convert.

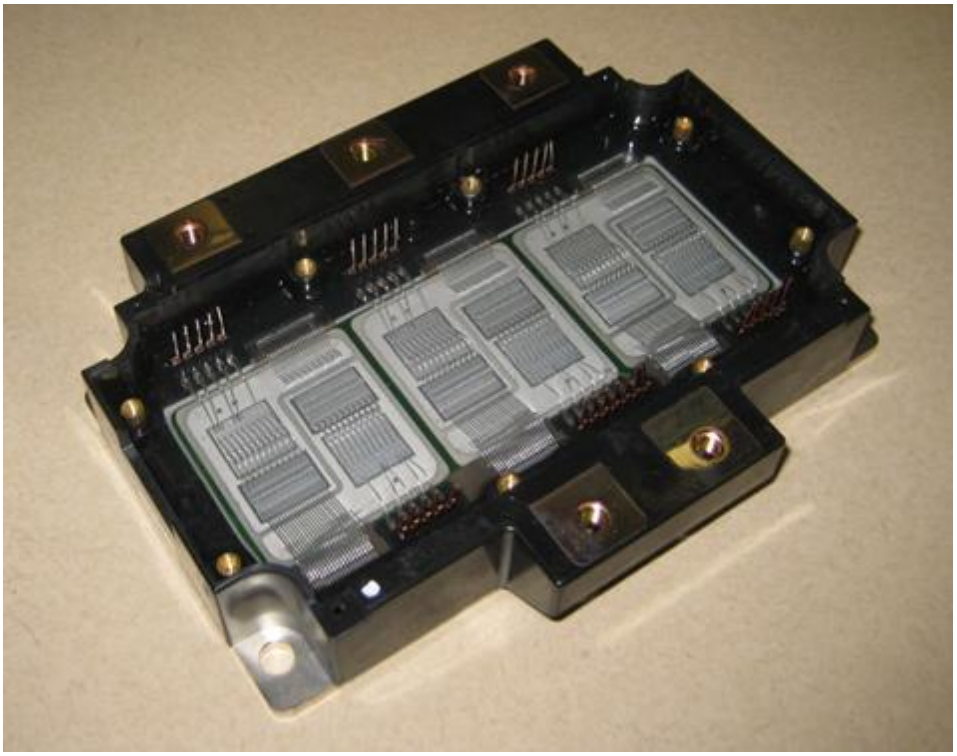

Figure 2.1 – Conventional IGBT power module

2.1.1 Half-Bridge Circuit Design and Operation

A common half-bridge circuit consists of a high and low side switch with freewheeling diodes and is seen in Figure 2.2. In motor control operation and DC to AC voltage inversion the output voltage will be sinusoidal. The device switching frequency is orders of magnitude higher than the output frequency thus each switch cycle is only infinitesimally different from the previous with an approximately constant output current. A switch cycle is seen in Figure 2.3, where a switch and its opposite rectifier are in conjunction. As the high side IGBT switch turns on, the output current I_L transfers from the low side diode to the high side IGBT. As the diode approaches I_L = 0 A, the diode suffers reverse recovery current and causes additional strain on the transistor at IGBT turn on as a current spike. The IGBT current and the diode blocking voltage stabilize as excess charge carriers diminish within the diode. The IGBT current, which is the output current of the circuit at this time, rises over this time period infinitesimally due to the higher DC bus voltage of the transistor input charging the inductive load by $\frac{di}{dt} = \frac{v\ t}{L}$. When the IGBT turns off, excess carriers exit it while its blocking voltage rises, exactly similar to the diode. This again leads to switching power loss in the device and system. The system is again

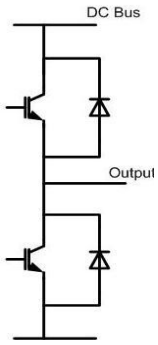

Figure 2.2 – Half-bridge circuit diagram

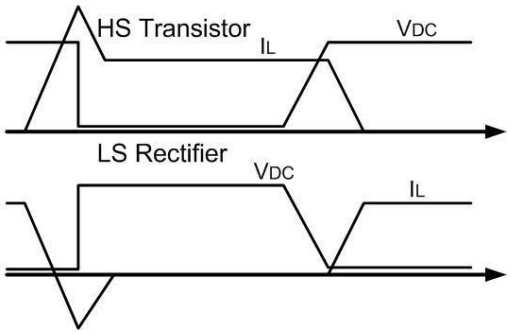

Figure 2.3 – Half-bridge switching waveform [34]

in discharging state at I_L = 0 A in the switch where the current is actually lowering by $\frac{-di}{dt} = \frac{v\ t}{L}$ as in the beginning of the waveform figure [34].

The gate control of the module is pulse width modulated (PWM) for a sinusoidal output or a more constant duty cycle corresponding to a single DC output voltage depending on the application. On times of the devices must adjust dynamically since the output current I_L is always slightly fluctuating due the charging or discharging of the load. This is why the switching frequency is much higher than the output frequency. Both the IGBT and p-*i*-n diodes are dominated by switching losses, therefore the circuit is bound by a reasonable operating frequency which is typically around 20 kHz [1]. These switching losses produce heat which dominates packaging designs for these power circuits leading to robust thermal consideration examined at in the following section.

The half-bridge may be modified without freewheeling diodes in which an inductive DC motor is connected to the high voltage DC, parallel to the high side switch. The low-side switch acts as a drive switch MOSFET and when it is switched on the current will flow through the motor and voltage source. The high side switch acts as a freewheeling switch when the drive switch is off to allow the inductive motor current to flow through the freewheeling switch and back to the motor [35].

The half-bridge circuit configuration can also be expanded to serve a similar role for three phase current, where three identical half-bridges are placed in parallel on the DC bus to produce three AC voltages of the same frequency and amplitude but each 120 degrees out of phase. This circuit configuration and module topography is seen in Figure 2.4.

In CHAPTER 1 it is seen that wide-bandgap semiconductors can improve circuit performance. There are much few minority carriers in bipolar devices due to the lower intrinsic

carrier concentration of SiC, nearly eliminating minority charge reverse recovery [36]. Also, the lower $SpR_{DS,on}$ makes it possible to use unipolar SiC MOSFETs instead of bipolar IGBTs. This leads to much lower conduction and switching losses compared to silicon IGBTs.

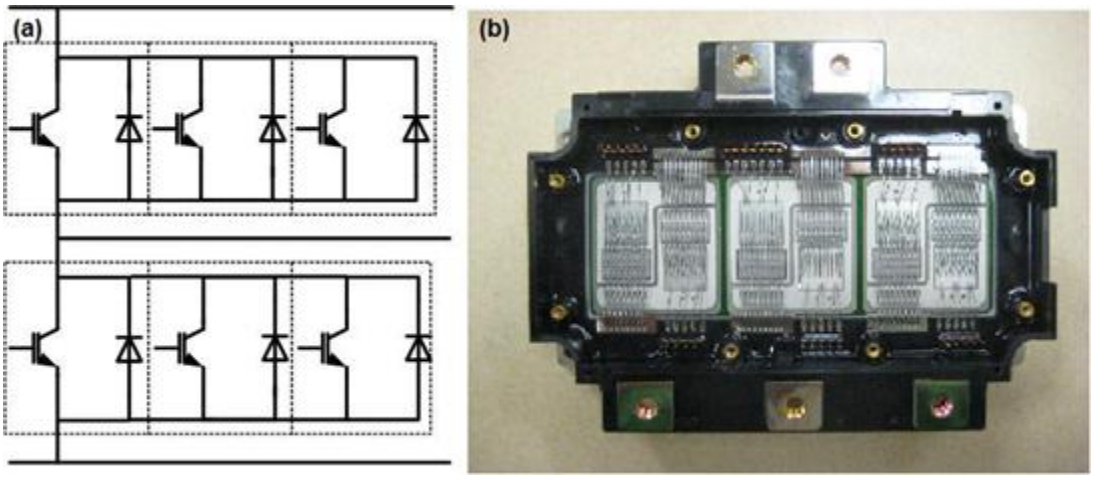

Figure 2.4 – Three phase half-bridge circuit diagram and module

2.1.2 Conventional Power Module Design

Construction of conventional modules has remained similar for over two decades, indifferent to the exact circuit configuration or the number of phases or switches. The cross sectional view is seen in Figure 2.5 [37]. There are many components of the module for both electrical and thermo-mechanical reasons. The design is robust and its fabrication begins with the placement of direct bonded copper (DBC) substrate. DBC is a sandwich structure of a ceramic material with copper layer on either side, aluminum nitride (AlN) is a common ceramic insulator because of its high thermal conductivity although aluminum oxide may also be used because of their lower cost. Silicon nitride (Si_3N_4) is also a less common option which features higher strength and allows for the insertion of conducting copper vias through the ceramic. Power semiconductor devices are then soldered to the top side of the DBC typically with tin-lead solder.

The DBC is then soldered to a heat spreader or baseplate with a lower melting point solder so as not to reflow the die-attach solder material. The DBC and baseplate are then attached to a semi-heat resistant, plastic enclosure which typically has rigid power interconnects built into it extruding from the plastic while the copper baseplate is still exposed. Wirebonding or ribbon attachment is then done to connect the DBC traces to the top-side device pads, typically gate, collector, and anode connections, and also the traces to the power interconnects. After which, the plastic enclosure is filled with a silicone based encapsulant gel for protection from debris, dielectric insulation, and additional thermal conductance from the devices [38]. This process makes for large modules with a mass upwards of 3 kg primarily due to the thick plastic packaging and the thick copper baseplate, none of which is necessary but for thermo-mechanical ruggedness.

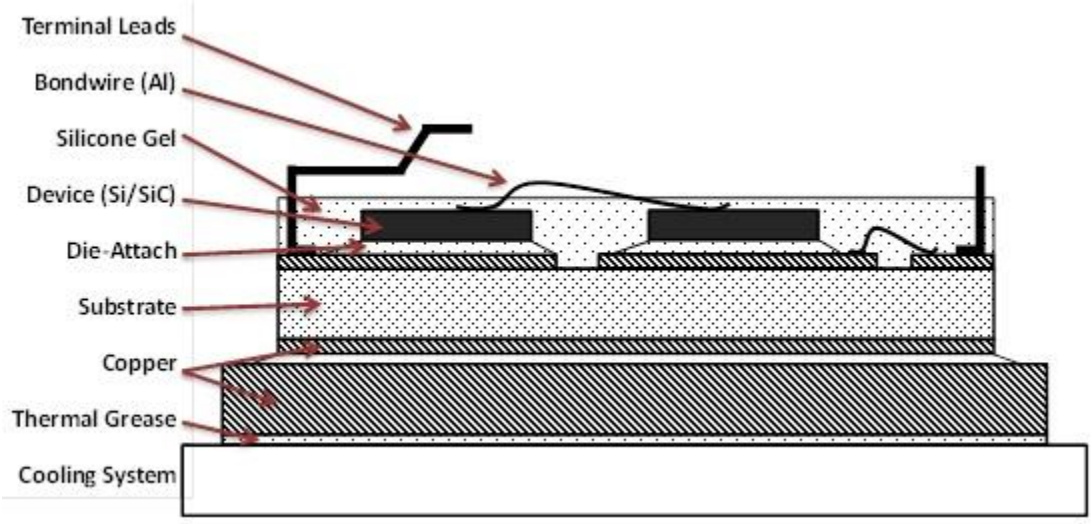

Figure 2.5 – Conventional power module cross section [38]

2.1.3 Power Module Thermal Design Considerations

The power module is designed to bridge the need for electrical, thermal, and mechanical demands. Design methodology dictates that once electrical connection demands are met, thermo-mechanics dominate leading to a large form factor. This is because when the module is in use, devices can produce over 270 W of power loss per device at 10 kHz with 114 W from conduction and an additional 164 W from switching losses, these amounts only increase with faster switching [39]. A fundamental design goal of the modules is to remove the power loss to keep $T_{j,max}$ of the device below the 175 °C silicon device limit. Also, power loss leads to mechanical stress from material expansion because materials expand with higher temperatures as determined by their coefficient of thermal expansion (CTE).

Each material has two primary steady state thermal performance characteristics: CTE and thermal conductivity. These properties are listed for each common power module material in Table 2.1 and are carefully considered in module design.

Table 2.1 – Thermal Properties of Traditional Power Module Materials

Material	CTE (µm/m-K)	Conductivity (W/m-K)
Copper	16.4	385
Aluminum	24	210
Silicon	3.0	124
SnPb40 Solder	24	50
Aluminum Nitride	4.5	83
Thermal Grease	–	0.75

2.1.3.1 Coefficient of Thermal Expansion

CTE is the rate at which a material expands in response to heat. Typically ceramics and non-ductile material have low CTE, although some metals also have a low CTE. Every material has a CTE and it is measured in parts per million per Kelvin (µm/m/K). This is an important

material property because two joined materials that do not expand identically when heated will inflict force and stress on each other until a failure occurs. This process is the basis of nearly every single mechanical failure type in power modules. Larger CTE mismatches between joined materials cause larger stress per Kelvin.

Silicon and SiC have relatively low CTEs compared to most metals at 3.0 μm/m/K and 3.6 μm/m/K, respectively. Therefore this low CTE is the benchmark for every other material CTE to be used in any power module because the devices cannot be removed. Every material should have as similar CTE to silicon or SiC as possible to avoid large CTE mismatch. Unfortunately, some common materials of conventional modules do not have low CTEs and cause stress. This can often be because of price or complication of changing the module manufacture process. It may be because the other material has a low thermal resistance which is also desirable.

2.1.3.2 Thermal Resistance and Specific Heat Capacity

Thermal conductivity k is a measure of a material's ability to transfer heat power efficiently and is the reciprocal of thermal resistivity ρ_{th}. Lower resistivity imposed on heat flow causes a lower thermal gradient across it and lower peak temperature. Thermal resistance is exactly similar to electrical resistance except for heat flow instead of current. Therefore, like CTE, each material should have as low of thermal resistivity as possible.

Electrical capacitance is emulated by thermal capacitance, or specific heat capacity c_p. This property is most important when considering switching; heat capacity resists temperature change like a capacitor and maintains temperature after the device is turned off. The effect of these two thermal properties is seen in Figure 2.6 which gives a thermal model of a power module with heat resistance and specific heat capacity of each material. They are in series with

each other where voltage is analogous to temperature and heat power flow to current [40]. Improving thermal performance reduces module temperature which also decreases CTE expansion, therefore reducing stress can be achieve through temperature reduction or improved CTE matching.

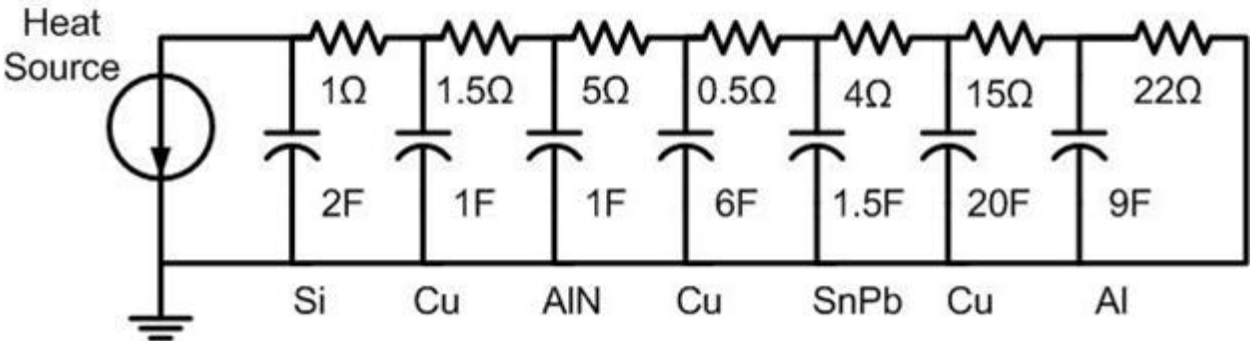

Figure 2.6 – Electro-thermal equivalent circuit model [40]

2.1.4 Power Module Reliability Issues

Power modules endure a great deal of thermo-mechanical stress from the CTE mismatches causing several types of failures and reliability degradation issues. Figure 2.7 displays the relationship between the average amount of module usage cycles before failure and the rise in $T_{j,max}$ during each cycle [41]. Module reliability is commonly expressed this way because a change in temperature brings about a proportionate amount of stress depending on CTE. A smaller ΔT each cycle produces less stress, thus identical modules should operate more cycles on average with a lower ΔT than with a greater ΔT. More importantly, since power modules are used heavily in traction devices there is a great deal of thermal cycling because of the constant starting and stopping of vehicles. Constant thermal cycling leads to several reoccurring reliability issues including die cracking, DBC delamination, and wirebond failure.

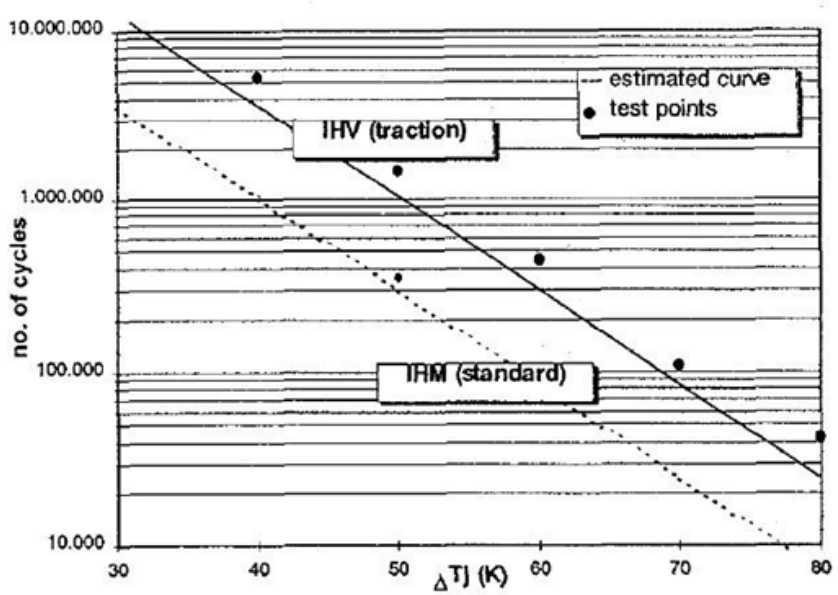

Figure 2.7 – Module cycles to failure vs. temperature rise reliability [41]

2.1.4.1 Direct Bonded Copper Delamination

There is good adhesion between DBC and AlN, the highest thermal conductivity ceramic insulator. This is achieved by oxidizing copper which forms a copper oxide bond layer and then annealing the oxidized surface upon AlN at 1070 °C [38]. This bond combats the 11.9 µm/m/K CTE mismatch between the two, however, give enough thermal cycles it will eventually fail. When doing so, DBC lifts off the ceramic substrate and curls causing solder and devices to break off. If the devices do remain after copper delamination, it will cause the heat flow to bottleneck into whatever contact remains between the copper and ceramic, raising the effective thermal resistance several orders of magnitude. This will lead to a huge temperature rise in $T_{j,max}$, solder, and wirebonds which quickly leads to device burnout or causes another interface to succumb to CTE stress failure [42].

2.1.4.2 Die Cracking of Device

Conventional tin–lead solder (SnPb40) is sandwiched between silicon and copper which have CTE differences with the solder of 21 µm/m/K and 7.6 µm/m/K, respectively. Because of this, it is a common reliability issue point. This sometimes results in the solder itself cracking, as seen in Figure 2.8, or in the die itself cracking or breaking [43]. This sort of failure is less common than others due to the ductile nature of tin-lead solder.

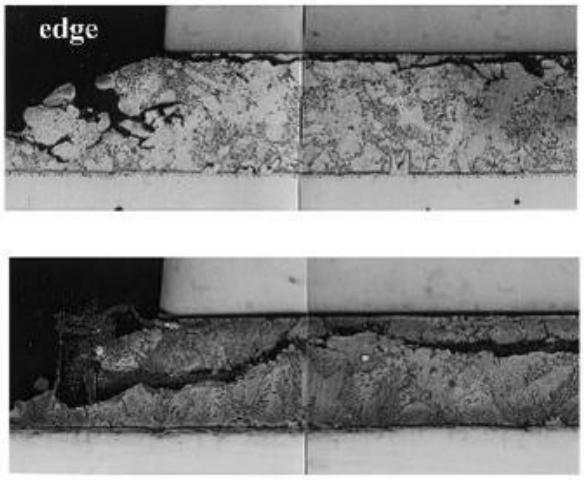

Figure 2.8 – SEM cross section of solder cracking failure [43]

2.1.4.3 Wirebond Issues

Semiconductor wirebonding is the cause of 70 % of IGBT power module failures. Their problems cause two common types of failures, one is liftoff due to CTE mismatch. There is no ductile buffer between silicon die and aluminum wirebonds direction upon it leaving a 21 µm/m/K CTE mismatched interface, a difference matched within the module only by the more ductile solder and silicon interface [44]. This wirebond connection is also the interface that experiences the highest temperature rise since it is directly at $T_{j,max}$, leading to the greatest expansion of those materials which leads to even higher CTE stress [45].

The other concern for wirebonds is inductance, their mutual inductance and high current acts upon other wirebonds within the module which causes non-uniform current sharing between devices. There is already concern of reverse recovery currents from power diodes and IGBTs in play. The addition of parasitic inductance has the potential to destroy the devices by further exceeding their current ratings. This phenomenon is especially true on the devices further from the center of the module because there is likely to be a balance of electromagnetic forces acting on the inner wires. Outer wires, however, are not typically as inductively balanced thus they are more prone to burnout [46]. This phenomenon is seen in a graph of the transient currents of parallel devices in a module in Figure 2.9 [37]. The lower numbered devices are on the periphery of the module while the higher numbered devices are in the center. It is seen that for several dozen microseconds the current can be at severe imbalance with some devices 100 % higher than the steady state current and others 66 % below it, easily pushing some devices above their current ratings.

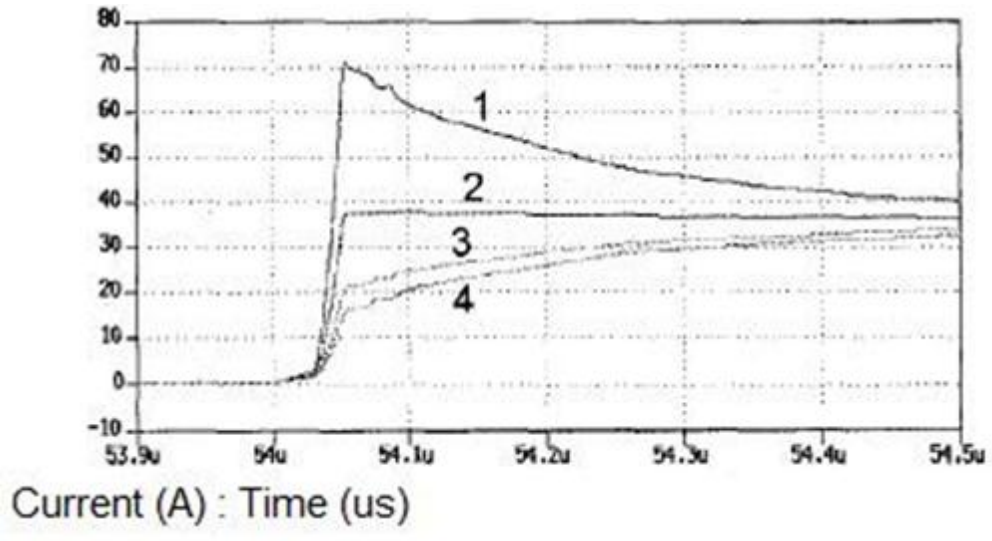

Figure 2.9 – Non-uniform current in parallel devices within power module [37]

2.2 Advanced Power Module Designs

There are many ideas and designs in power module packaging which attempt to introduce new high-temperature wide-bandgap semiconductors into modules while also attempting to address traditional problems with current modules.

2.2.1 Press Pack Module

A press pack consists of a mechanical spring connection to one side of a die's electrical connections, they are otherwise similar to conventional modules, which makes them a modest manufacturing change from wirebonding, one can be seen in Figure 2.10 [47]. The substitution of the wirebond is advantageous due to the increase in cooling capability from the potentially robust metal electrical contact on the spring. There is also less inductance and CTE mismatch since there is no wirebond on the die, therefore there is no rigid Si–Al interface to reduce reliability. The notion of the press pack module has been around as long as the semiconductor era dating back to 1969 with a Westinghouse design [48].

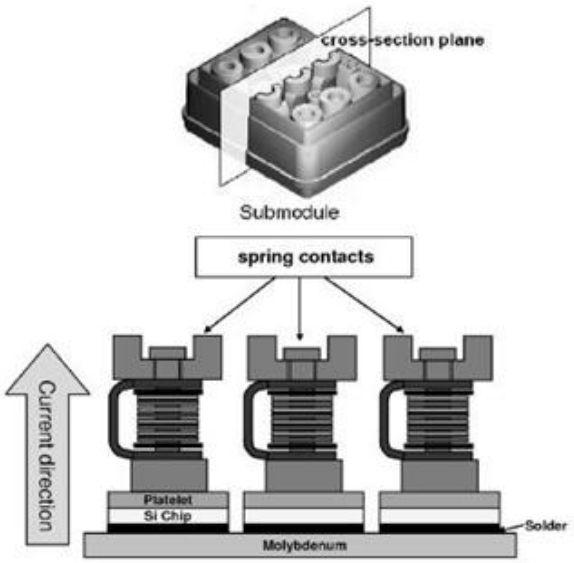

Figure 2.10 – Standard press pack module design cross section [47]

ABB Corporation of Zurich, Switzerland has developed a solder-less 1000 A, 4.5 kV package seen Figure 2.11 [49]. This press pack uses no solder at all, which is not characteristic of all press packs but simplifies manufacture. This is possible due to the holding pressure of the device by press pins, the lack of solder is a point of merit according to ABB. Also coming from ABB is the conceptualized design seen in Figure 2.12 which is a design for a larger module composed of smaller modules similar to Figure 2.11 [50]. Press packs have their advantages over traditional modules however they do share the fundamental problem of a large form factor due to the required pressure system, this new system likely also bring in new mechanical reliability issues.

Figure 2.11 – ABB press pack sub-module [49]

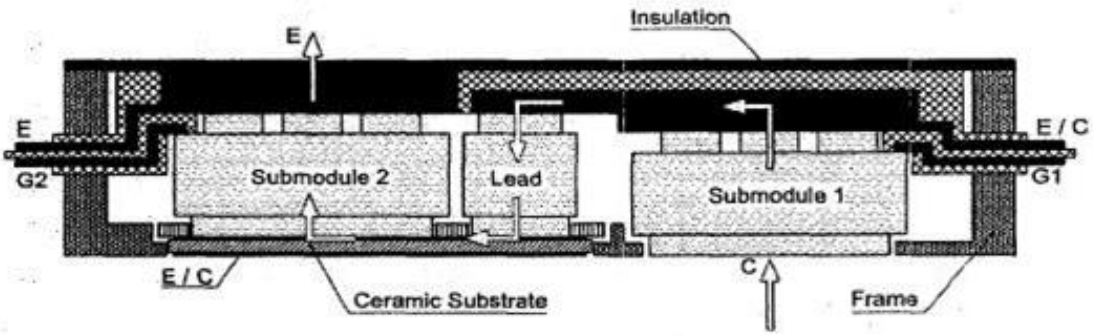

Figure 2.12 – ABB system module conceptualization [50]

2.2.2 Alstom Transit Module

Alstom Corporation is a conglomerate of power electronics businesses that deal in transportation, power services, and power generation. They have a variety of designs for all aspects of train transportation including power module designs, one of which is seen in Figure 2.13 [51–53]. The module does not consider encapsulation or junction termination, this make other modules able to carry a higher blocking voltage than the Alstom design. There is no mention of the electrical material which, if copper, which would severely limit the temperature usage due to CTE stress.

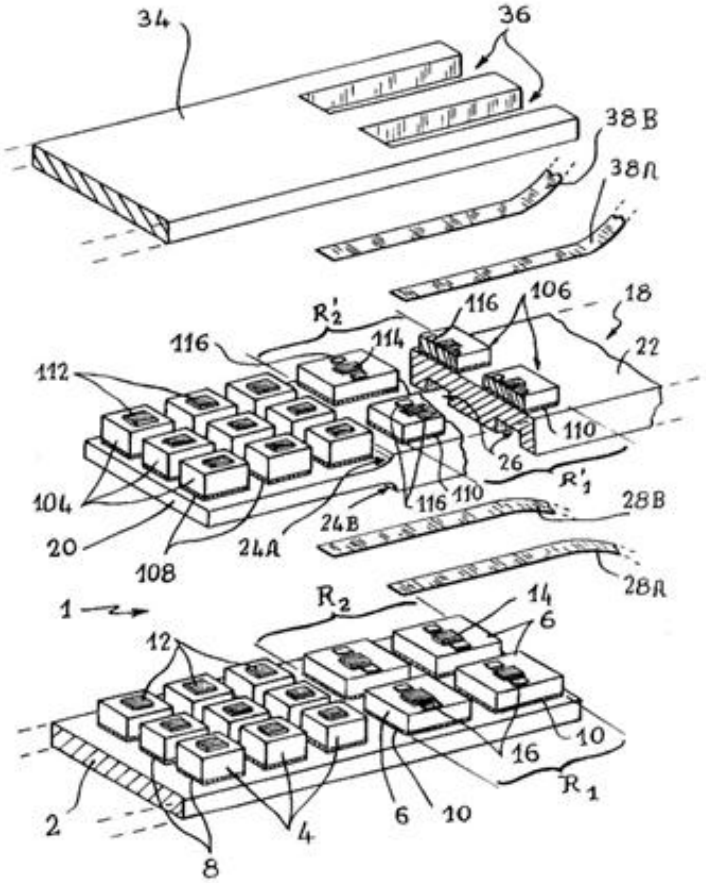

Figure 2.13 – Alstom double lead frame module design [53]

2.2.3 Semikron and Powerex Modules

Powerex and Semikron are leading power module manufactures offering a variety of traditional modules with various circuit configurations. Their latest developments have been the introduction of new solder-less packages [54]. This is accomplished by the use of silver based epoxy or nano-sinter paste described later. They add an ease of manufacture while also raising the thermal rating of these new modules to 175 °C from the 125 °C to 150 °C range. Their modules which do not utilize the nano-silver sintered paste have begun using ribbon connections between the chips for improvement over wirebonds. Manufactures have also begun separating the module connection terminals by separating the input and output and moving them from the module face to the sides so that they may mount a control module atop them [49], [55].

2.2.4 Arkansas Power Electronics International Hybrid Module

Arkansas Power Electronics International (APEI) is a packaging company associated with the University of Arkansas who has worked to design new power modules for use to 300 °C [56–59]. Their modules are advanced by the inclusion of the gate driver circuitry within the module housing which is a traditional high-temperature semi-hermetic case with experimental encapsulation that does not adequately hold up to the 300°C environment, the module can be seen in Figure 2.14. They have demonstrated a working module at 300 °C in a high-temperature ambient environment, however the power devices still rely on wirebonds. Thus this package has a small chance of exceeding previous benchmarks in terms of reliability.

Figure 2.14 – APEI hybrid module design [57]

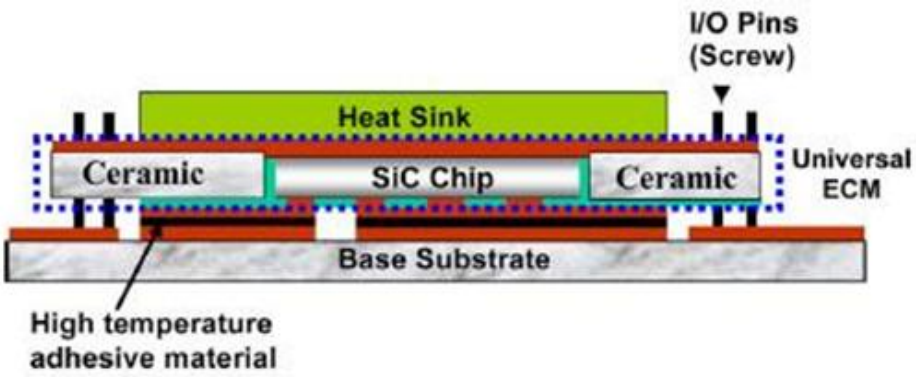

Figure 2.15 – CPES double-sided cooling module design [60]

2.2.5 Double Sided Power Module

A double sided cooling module as seen in Figure 2.15 has been proposed and built by the Center for Power Electronics Systems [60]. CPES is group of several universities funded by the National Science Foundation that does work in packaging and thermal characterization [61].

Their power module places devices inside of a ceramic layer with glass filler areas to seal the SiC chips in place [62]. Interconnect layers are then sputtered upon the ceramic and etched for electrical connections. This module is promising because it puts consideration into thermal stress physics and materials along with form factor. It also employs high-temperature materials such as nano-silver for electrical connections to allow for operation to 300°C.

2.3 Electronic Cooling Systems

In order to constrain the temperature of power modules – conventional and others – for device performance and long term package reliability, they are connected to a cooling system which dissipates the device heat loss or attempts to overcome environmental module heating. These systems are either passive in which there is no moving components or active in which there is dynamic system to more vigorously lower module temperature [27]. All cooling systems must eventually terminate to an uncontrolled ambient temperature environment.

2.3.1 Passive Cooling

Passive cooling is the simplest of cooling technique and does not involve the use of moving parts. It is typically used for lower power loss conditions (< 5 W/cm^2) or may be used when a higher junction temperature $T_{j,max}$ is acceptable. The most common of all electronic cooling is the passive heat sink, seen in Figure 2.16, which is a conductive solid mass that has extruding fins to dissipate heat effectively through natural air convection. They are typically mounted with a low thermal impedance path between sink and devices in order to absorb heat loss. The sink then rises in temperature and dissipates that heat to the ambient air surrounding it.

The effectiveness of the sink is increased with additional fins, longer fins, and higher thermal conductivity metal.

It is not necessary to use a heat sink for passive cooling however. It is also possible with very little material and structural design but rather by strategic placement of electronic devices in common surface mount technology in a means that allows for acceptable natural convection but without the use of a heat sink. This is often done in electronic “racks” in which circuit boards are placed vertically as opposed to horizontally to allow for the heated air surrounding the devices to rise unimpeded by the board [27].

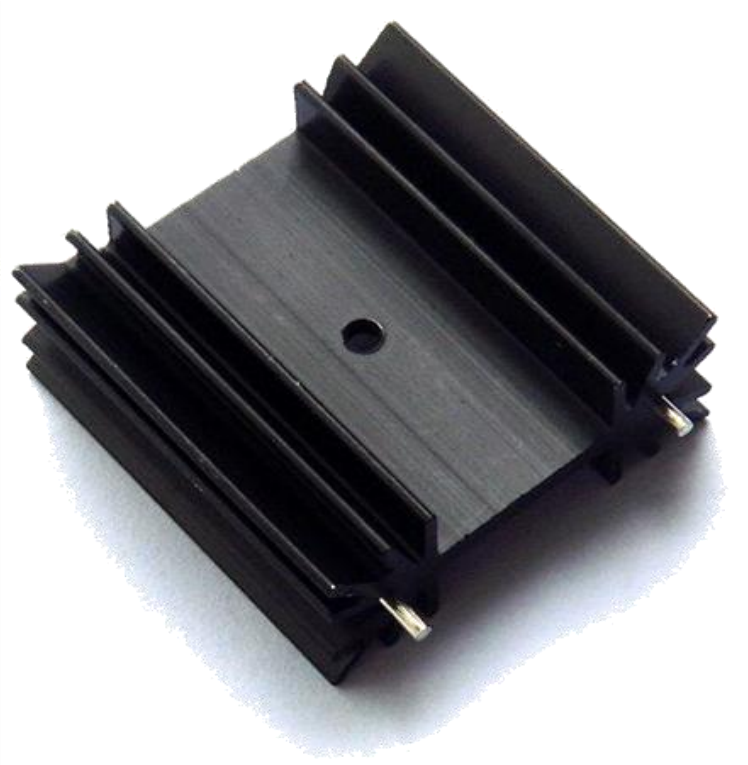

Figure 2.16 – Conventional heat sink for passive air cooling

Dialectic fluids may also be utilized for passive cooling by means of submerging thermally sensitive components to utilize a higher thermal conductivity and conductive heat transfer capability of liquid as opposed to air. This technique is often gravity assisted by the

buoyancy of the lighter, heated fluid which then rises away from the electronics until it cools and lowers to near the heat source again creating a continuous loop, all the while acting passively [63]. This is also called a thermosiphon.

2.3.2 Active Cooling

More complex cooling systems which are able to dissipate higher power loads (>10 W/cm^2) are known as active cooling systems and are defined by requiring actively functioning component for operation to increase heat removal. The most common of these for power electronic modules is a forced liquid cooling loop. This entails a coldplate which a power module is attached to, typically metal and has piping throughout it to run fluid through. Fluid is pumped through the coldplate to a larger heat exchanger, possibly a passive heat sink and back through the coldplate in a closed loop. This allows for the liquid to remove the heat loss faster by conduction to a heat sink much larger than can be directly attached to the module. The heat sink may also make use of an active cooling system such as forced air cooling. This cooling, also common in computer hardware, features a simple fan blowing air onto the heat sink to quicken convective cooling. In Figure 2.17 and Figure 2.18 the insertion of an active cooling system within a hybrid vehicle can be seen [64].

Typically the power loss of power electronic modules necessitates active cooling. When they do not, such as often with SiC, the space and design considerations of the power components still require its use as when they are imbedded within motor housing because the ambient and be a distance from the electronics.

Active cooling systems also lower system reliability because they feature parts that must operate as opposed to passive cooling, thus they may occasionally break which then may cause

damage to the electronic components as well. Therefore it is advantageous to make use of simple passive cooling systems whenever possible.

Figure 2.17 – Ford Focus power electronics with cooling system

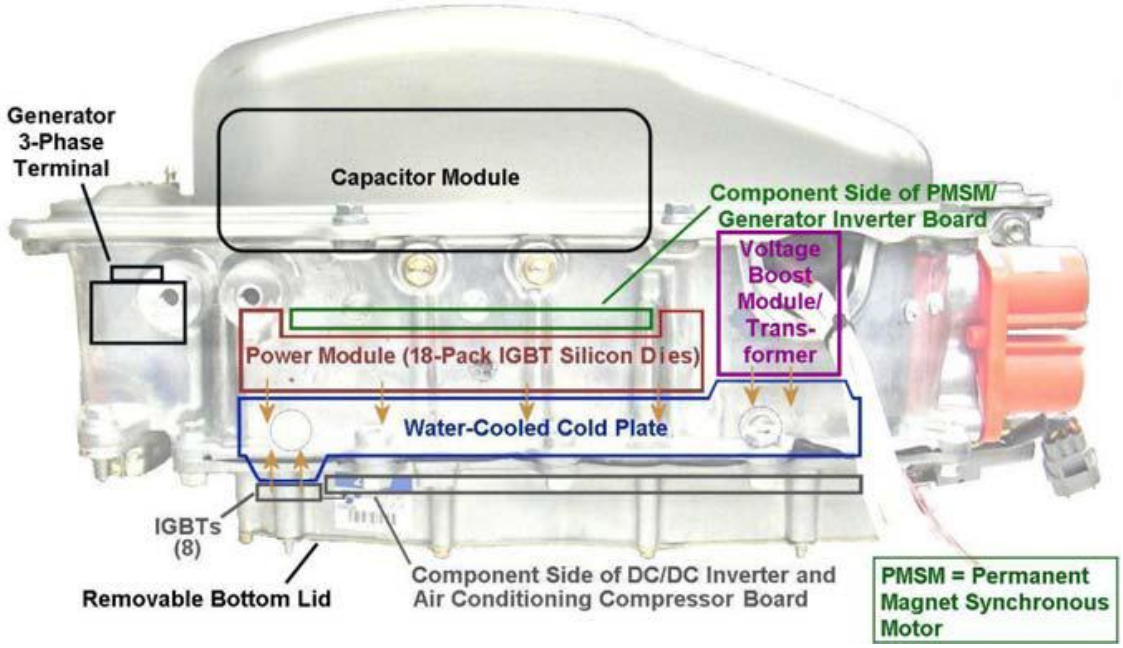

Figure 2.18 – Toyota Prius power electronics module with active cooling plate [64]

2.4 High-Temperature Die-Attach

TLP bonding is one of many types of electronic die-attaches each with its own advantages and applications. It fits in with a progression of advancing among die-attaches that have raised temperature thresholds and improved quality. Currently there several types of die-attaches which, although are not best for wide-bandgap power devices, are important to understand and are discussed in this high-temperature die-attach prior art review

2.4.1 Solders and Brazes

The traditional die-attach for power semiconductor devices is solder [65]. Solders are characterized by typically being a eutectic multi-metal system that melts below 450 °C thus acting like pure conductive elements with advantageous mechanical properties Brazes are typically off eutectics and melt above 450 °C and higher. There are countless varieties of solders and brazes featuring many different material combinations which have different effects on the properties of them. The most common solder is tin-lead, of which, the high-tin eutectic solder SnPb37 is the most typical form which contains 63 % tin and 37 % lead. It has a melting point of 183 °C which allows for the devices and package to operate up to the traditional silicon device temperature limit of 150 °C [8]. Tin-lead is a common solder due to the history of using low melting tin as a solder, however tin suffered from the phenomenon of short circuit causing “tin whiskers”. It was found that by adding at least 3 % of palladium to the tin solved this problem although tin-lead solder had been used for non-electronic needs since Roman times [66], [67]. Higher ratios of tin are sometimes used to improve wetting, typically in non-electronic settings, and high palladium compounds are more common to increase the melting temperature to well over 200 °C. Also, lead increases ductility in compounds which increases reliability in solder.

High lead content solders have become less prevalent however due to environmental regulations such as Restriction of Hazardous Substances Directive (RoHS) in Europe and Electronic Waste Recycling Act (EWRA) in the United States banning toxic materials in electronics such as lead which cause health problems. There does remain a demand for popular tin-lead solder with many exemptions of the environmental regulations for military applications.

The preference for non-lead containing solders has contributed to diversification of other eutectic solders which typically have higher liquidus and solidus temperatures benefiting power device packaging needs. Gold, aluminum, silver, and zinc alloys all exists for high-temperature soldering with gold being the most common. Gold-tin (AuSn20), gold-silicon (AuSi3), gold-antimony (AuSb25), and gold-germanium (AuGe12) solders each have re-melting temperatures exceeding 280 °C while other solders exists with filler materials of nickel, indium, and cadmium also with high-temperature capability. Each of these solders however carries the disadvantage of needing be heated to above its extreme melting temperature and held for fabrication, also most of these materials are very brittle and do not have good long term reliability [8]. Furthermore, some even outgas toxic fumes and are volatile during reflow [65]. All compositions of solder are typically available in paste form which typically contains a flux material that inhibits oxidation during reflow or are available in pre-cut solid sheets known as preforms which are typically sized and shaped to fit the exact need of that device.

Table 2.2 – Common High-Temperature Solder and Braze Materials

Material	Melting Point (°C)	Thermal Conductivity (W/m-K)	CTE (µm/m-K)
SnPb37	183	50.9	24.7
SnPb95	312	36.0	28.7
AuSn20	280	280	16.0
AuSi3	363	363	12.0
AuGe12	356	44.0	13.0
AuIn19	487	28.0	14.7

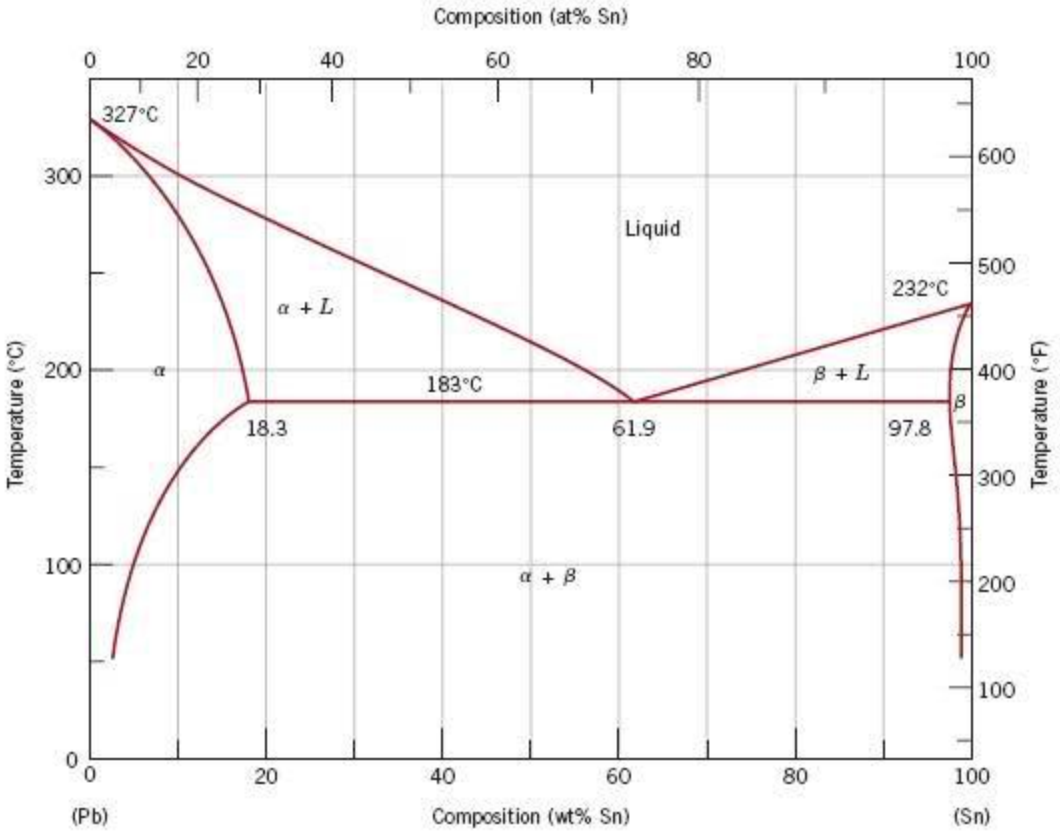

Figure 2.19 – Tin-lead (Sn-Pb) phase diagram

2.4.2 Conductive Pastes

Conductive pastes are a less conventional die-attach from traditional solders that rely on metallic constituents providing electrical and thermal conduction. Pastes also contain organic or inorganic binder epoxies or glass in addition to metal particles. Most pastes rely on silver or possibly nickel as the electrical conductor since it has the highest known electrical conductivity (419 W/m-K) and thermal conductivity (64.5E6 $\Omega^{-1}m^{-1}$) [68] amongst all metals. But large quantities are not required of them, therefore they are more economically feasible than in a solder [69–71]. The silver particles are suspended within a binder and create electrical pathways through the die-attach but they are not fused together, they simply touch. Their density within the composite is enhanced typically by a "burnout" of the binder which makes conduction feasible.

This burnout for both silver-glass and epoxies typically takes hours and may require vacuum storage also which greatly increases fabrication time and difficulty [72]. This process can also require extremely high firing temperatures up to 400 °C [73]. The advantage of these epoxies is that they are typically low cost and the simplicity of applying them that may not require heating and some yield higher operational temperatures that solders. Also, if die stress is an issue, a highly elastic epoxy can relive this with a tradeoff of thermal and electrical conductivity. There are numerous disadvantages aside from long, high-temperature processing including low thermal and electrical conductivity (even though they contain silver), lower shear strength compared to solder by an order of magnitude, and high CTE which increase package stress [8], [73].

2.4.3 Silver Sinter Paste

The most promising high-temperature die-attach technique aside from TLP bonding is that of nano-scale silver sintering. Silver sintering is a derivation of silver epoxy and silver glass die-attach however it is processed at a higher temperature so that the silver particles sinter together as opposed to simply touching while being suspended in an epoxy. Ideally there are no other constituents remaining after sinter bonding aside from silver, therefore it differs from silver glass in which silver particles sinter but they remain in lead borate glass [72]. It was conceived in its modern form by Schwarzbauer *et al.* based on the principle of diffusion welding [74–76]. In their experiments micron scale diameter silver pieces were suspended in an organic solvent and dispended at a thickness of 20–30 µm upon a gold or silver coated surface then heated at 250 °C to remove the organic binder. A device die was then placed upon it, also silver or gold coated, with 40 MPa of force for approximately 2 min to yield good shear strength results of

approximately 100 MPa [77]. Since only silver should remain in the joint after binder drying or burnout the re-melt temperature is theoretically that of silver (962 °C) [68].

This epoxy-less approach to sintering was advanced further by the use of nano-particles instead of micro particles for the development of trace lines [78–80] before applying it again to die-attach but without the need for large bonding pressures [81–86]. This is possible because with the smaller silver particles than in epoxies there are more points of contact between them and there is a higher density of silver. Since there are more contact points they can be sintered together more securely similar to silver-glass however without the need for the borate glass, only silver. Thus only an organic binder is necessary solely for the deposition process. This is then burnt out during a low temperature (~150 °C [87]) reflow that also induces some silver sintering which maintains the silver nanoparticles cohesion in the absence of the binder prior to die-attach. The silver sintering process is depicted in Figure 2.20. After the binder is gone, the die to be bonded is placed atop the silver and heated again with little to no pressure at a heat typically near 300 °C to complete the bond although many still utilize pressure at this stage to increase die-attach ultimate shear strength.

This bonding process has many advantages since it is primarily pure silver when complete thus it has a very low resistivity of less than 4.0 μΩ–cm, nearly to that of pure silver (< 2.0 μΩ–cm) and less than a third of traditional Sn-Pb solder or even high-temperature AuSn20 solder [82]. However, similar to silver-epoxy die-attach, the bonding process can still take many minutes, upward of half-an hour which is incompatible with high volume production. Also, the low density of the nano structure, compared to solid die-attaches, is unfavorable to thermal behavior which is seen in Figure 2.21 [8]. Lower die-shear strength values than is required for high reliability applications have been reported also unless pressure is still applied during

sintering which negates a theoretical advantage of nano-sintering [87]. This may be a due to the binder materials not fully exiting the composite; this would also cause an issue of outgassing later during the life cycle.

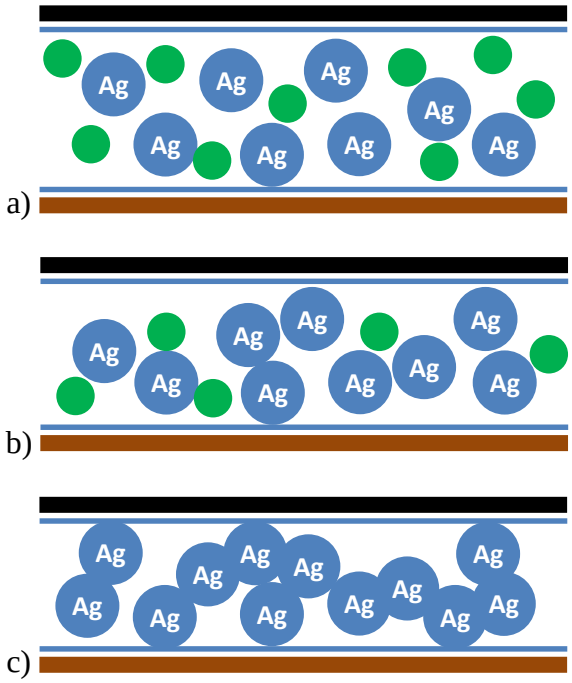

Figure 2.20 – Silver sinter die-attach with silver sinter paste in which organic binders (green) evaporate and burnout with heat, leaving silver particles (blue) to sinter together and to silver material layers.

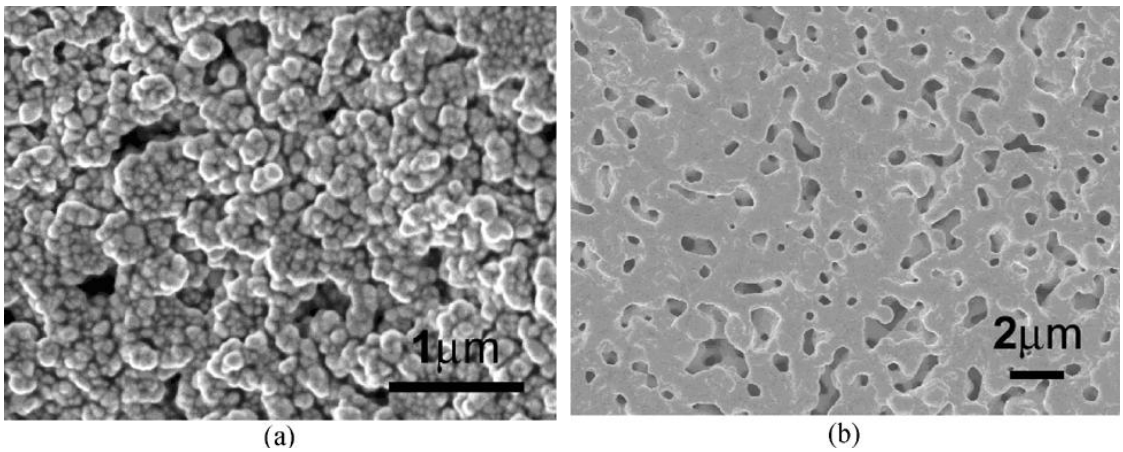

Figure 2.21 – Surface morphology of nano-silver paste before and after high-pressure sinter [82]

Figure 2.22 – Silver sinter paste fabrication process [81]

2.5 Summary

There have been decades of work associated with improving the packaging surrounding silicon devices. Modules have been designed and improved to deal with increased power loss due to increases is silicon device power. However with the opportunity of utilizing wide-bandgap devices in power electronics, packaging prior art is largely insufficient, especially to utilize them to their full advantages in the most ambition applications. New die-attach materials and module design are still required.

CHAPTER 3:
INTRODUCTION TO TRANSIENT LIQUID PHASE DIE-ATTACH

The focus of this work is on a novel die-attach technique known as transient liquid phase bonding, or TLP bonding, also less commonly referred to as solid liquid interdiffusion, or SLID. TLP bonding is capable of withstanding high temperatures while providing excellent strength and is a leading choice for advanced SiC packaging.

3.1 TLP Bonding Process Overview

TLP die-attach is the use of a TLP reaction to form a bond between a semiconductor and substrate. A TLP reaction is shown in the Figure 3.1 process overview and again in Figure 3.2. During the reaction, a highly diffusive material with a low melting temperature (the interlayer) melts and diffuses within minutes into a solid material with a significantly higher melting temperature (the base layer). Once the interlayer has completely diffused into the base, one new homogeneous solid material remains that has a melting temperature above both the original interlayer melting temperature and the reflow processing temperature [88–90]. The TLP reaction occurs at a fixed reflow temperature that is hot enough to melt the interlayer but not the base material. This process is known as isothermal solidification, in which the materials become solid during a constant-temperature process. It is important to perform this process in an inert or reducing atmosphere due the possibility of oxidation of the materials, some of which are highly susceptible to oxidation. Flux is not an option for TLP die-attach because its residue would remain in the joint.

To utilize a TLP reaction as a die-attach bond, the base and interlayer materials are deposited onto two different items (e.g., semiconductor and substrate) and then compressed together and heated. The reaction of the TLP materials adhered to the semiconductor and substrate bonds them together. There are several differences from TLP die-attach from familiar soldering techniques and are summarized in Table 3.1 many are also mentioned in the advantages section of this chapter [91].

Table 3.1 – Comparison of Select Solder and TLP Die-Attach Properties

Property	Solder	TLP Die-Attach
Metal System	No material system change	Formation of one or several material phases, elimination of pure interlayer
Reflow Temperature	Slow ramp up and down; above re-melt temperature	Constant temperature; below re-melt temperature
Bond Thickness	~50–100 µm	< 15 µm
Re-melt Temperature	Below reflow temperature	Significantly higher than reflow temperature
Rework Possibility	Yes, with drawbacks	Very limited, irreversible metal system phase changes
Oxidation Prevention	Flux typically necessary	Inert or reducing environment
Device and Substrate Surface Roughness	Flexible to many heights	Limited due to small liquid interlayer thickness and volume
Thermal Cycling Effect	Some, evolution of bond properties	Limited, high durability, thermodynamically stable

Some information from Ref. [92]

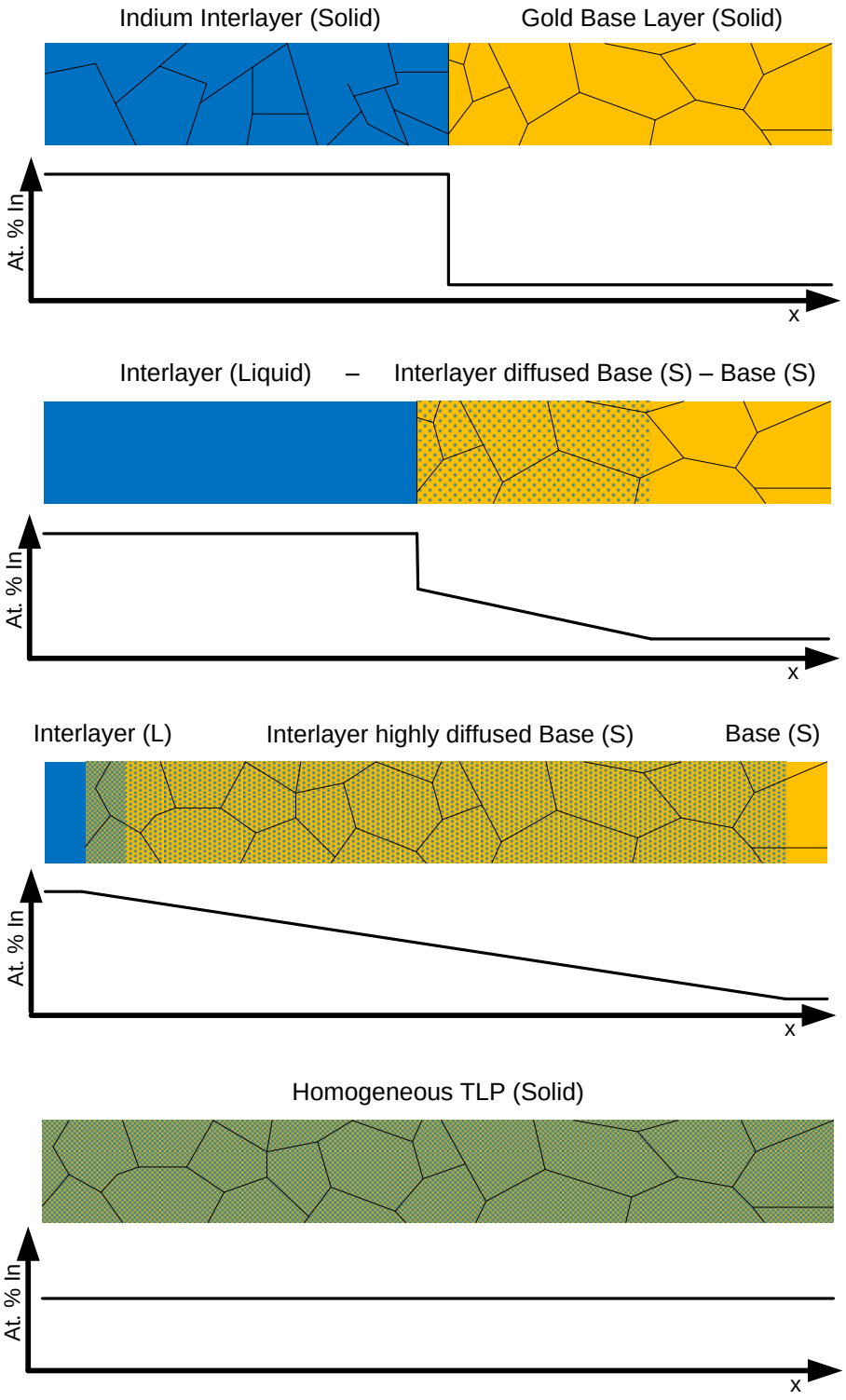

Figure 3.1 – Transient liquid phase (TLP) reaction illustration in which a highly diffusive interlayer diffuses into the high melting temperature base material, indium and gold, respectively, in this work. The In composition is plotted as it diffuses through the sample until complete. This composition solidifies into one homogenous composition while the reflow temperature is constant below the base melting point.

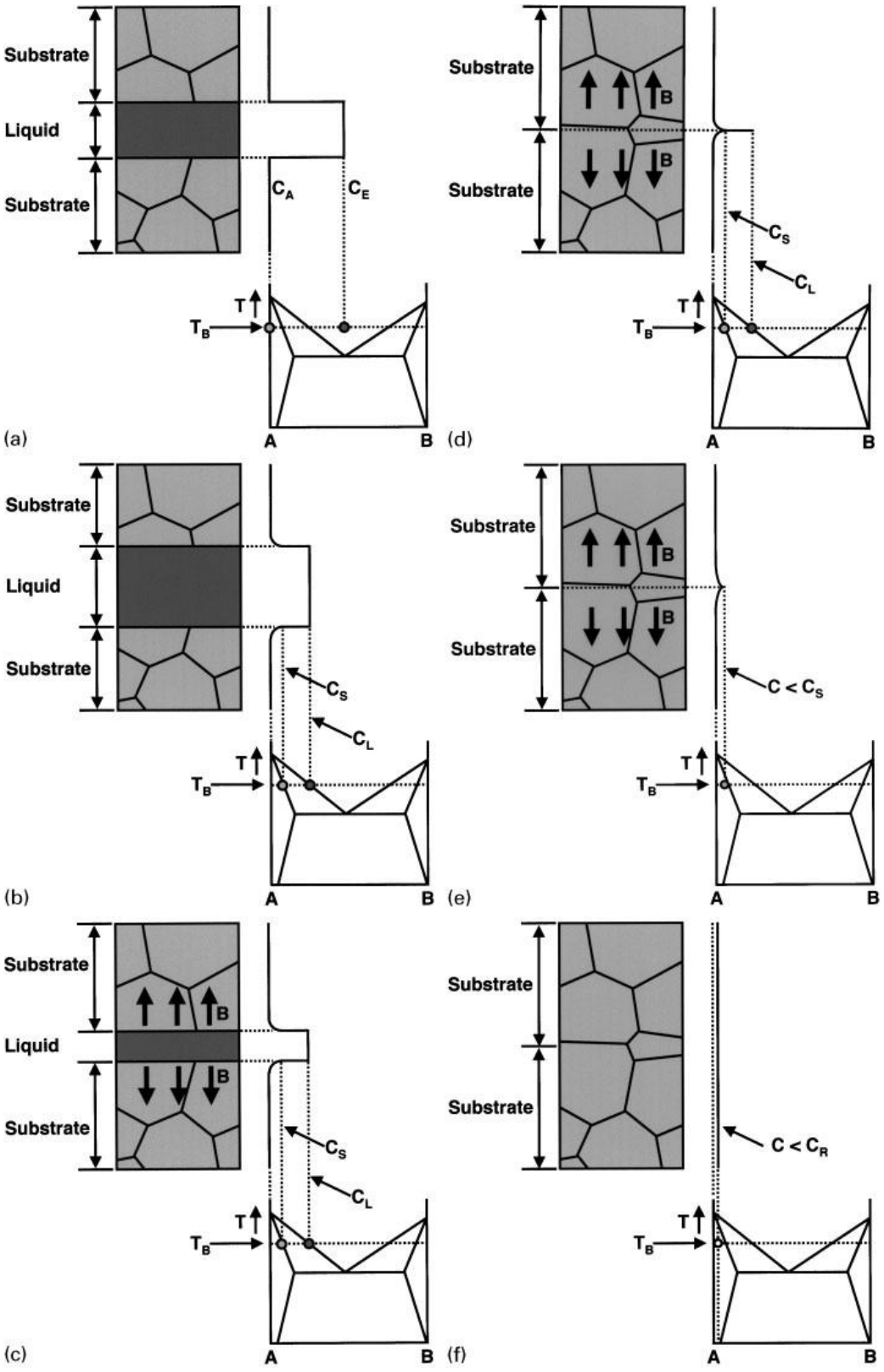

Figure 3.2 – TLP reaction process by Gale *et al.* with the associated material phase of the two materials during the reaction until they are fully homogenized after isothermal solidification [88].

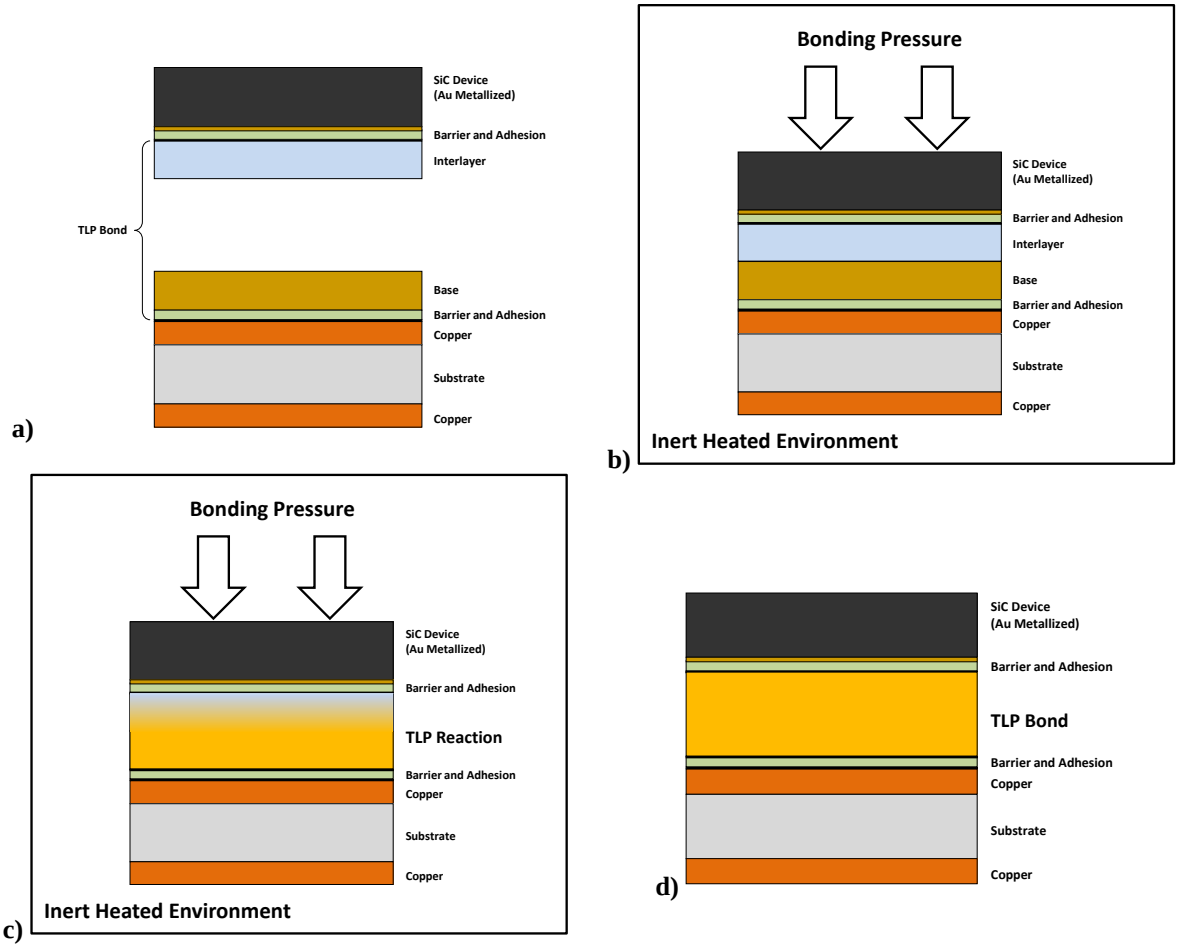

Figure 3.3 – TLP die-attach bonding process in which SiC device and copper metallized silicon nitride substrate are bonded in which the necessary TLP material are applied, the components are compressed in an inert heated environment, and they become bonded together.

3.2 Material System Requirements

3.2.1 Material Diffusion Overview

The compatibility of materials for TLP die-attach is highly dependent on their diffusivity into other materials. Materials used must be either selectively diffusive, selectively receptive to diffusion, or wholly inhibitive to diffusion to act in the TLP system as an interlayer, base layer, or barrier layer, respectively.

Material diffusion is the migration associated with mass transport through a medium and it is the described by the diffusion rate D of one material into another [93]. It is defined by the simple equation involving the distance d a diffusant travels over a period of time t,

$$D = \frac{d^2}{4t}. \tag{3.1}$$

The diffusion rate is unique for any two materials and is also a function of several factors such as temperature and material homogeneity thus it is also described by the Arrhenius relationship

$$D = D_0 \exp\ -\frac{E_A}{kT}\ , \tag{3.2}$$

using the diffusion coefficient D_0, activation energy E_A, and the temperature T, it is typically expressed in the units cm^2/s [94]. The diffusion rates of highlighted material pairs are shown in Figure 3.4. If both materials are in perfect atomic lattices their diffusion is described as lattice diffusion which is the slowest type of diffusion. If the materials are defected or amorphous it lowers E_A and diffusion is short circuited and accelerated along grain boundaries which is known

as grain boundary diffusion δD_{GB} which is highly common in electronics because it involves so many freshly deposited thin films which are amorphous. Long, a high-temperature annealing increases grain size in thin films and reduces the grain boundary width δ between them slowing diffusion through the film. Because diffusion is dependent on so many factors unique to the exact circumstances of each scenario it is sometimes estimated based on melting temperatures and film thickness [95]. Diffusion can be detected by a change in electrical resistivity in certain circumstances, this concept is explained and utilized in CHAPTER 6 [96].

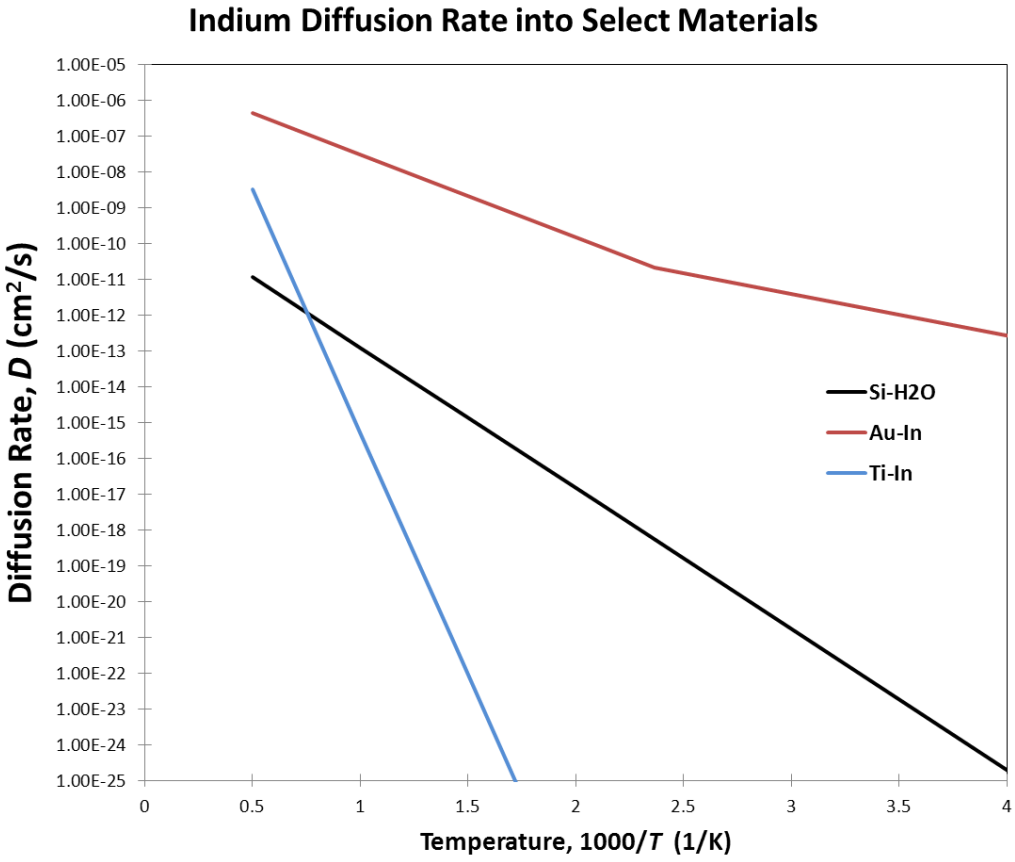

Figure 3.4 – Select diffusion rates of indium into thin films

3.2.2 Base and Interlayer

In order for create a TLP bond the two primary component materials, interlayer and base, must be chosen carefully. The individual properties of the materials matters along with the properties of the new homogenous material formed when isothermal solidification is complete. The interlayer should have a low melting temperature to reduce TLP reflow temperature which is slightly above the interlayer melting point. It should also be highly diffusive, specifically into the chosen base material so that the TLP interaction occurs quickly, on the order of minutes or seconds. If possible, the interlayer should have a low vapor pressure – which is often not associated with diffusive materials – to ease fabrication by not contaminating deposition systems. The base material should have as high of melting temperature as possible to increase the final re-melt temperature and maximum operating temperature. Most importantly, the final homogenous material created by the TLP reaction and the associated phases of the resultant material system should have favorable properties for die-attach. This includes high strength, ductility, high thermal conductivity to remove heat losses, and a high re-melting temperature. The materials ideally should not create a eutectic if possible because it is not necessary like a braze and will only lower the operating temperature. Also, the new TLP material should be stable because the diffusive interlayer can pose many system problems alone, but should be stable after fully diffusing into the base material. The final TLP material should not continue to be highly diffusive (this is investigated in CHAPTER 6).

3.2.3 Gold–Indium System

Among potential base–interlayer pairs, Au–In is a promising combination exhibiting very favorable properties. It has been shown to perform TLP bonding well [97–103] and the pair's

diffusion properties are well examined [103–111] thus it is an excellent material pair to bring TLP characterization to the next level of understanding in this work.

The Au–In binary system has been investigated by Okamoto to show many stable compounds and phases in the phase diagram shown in Figure 3.5 [7], [112]. The highest In content compound is $AuIn_2$ and has been shown to form quickly even at room temperatures [113]. The compound AuIn occurs at atomic mass fraction 0.5 for both materials and there is a notable eutectic point at 0.553 at.% In with a melting point of 496 °C [112]. Both of these compounds appear to be strong with no brittleness, which is often feared of line compounds such as these. Between the gold-rich (Au) phase and the AuIn compound there are numerous phases with the lowest eutectic point at 450 °C. This region of the phase diagram is less meaningful due to the expense of gold making it difficult to have TLP compound with a high gold content.

The diffusion of indium into gold is atypical in that it relies on a temperature dependent activation energy. This phenomenon is also seen in the Cu–Sn system and it is believed to be caused by the lack of grain boundary diffusion at some temperature ranges [114]. The diffusion coefficient and activation energy (from Eqn. (3.2)) of Au–In interdiffusion according to Zhang *et al.* [103] is

$$D_0 = 6.43\ 10^{-6}\frac{cm^2}{s}, \qquad E_A = 0.46\ eV, \qquad T > 150\ °C$$

$$D_0 = 1.20\ 10^{-8}\frac{cm^2}{s}, \qquad E_A = 0.23\ eV, \qquad T \leq 150\ °C.$$

Liu and Chuang report an activation energy of 0.41 eV when working in the 250–300 °C range which closely approximates Zhang's value [104]. Also, Bjøntegaard *et al*. reports E_A = 0.23 eV for Au–In when working at T < 50 °C which matches Zhang [105]. From Bjøntegaard the

diffusion coefficient can also be derived to be 1.5×10^{-9} $cm^2/s > D_0 > 0.5296 \cdot 10^{-9}$ cm^2/s depending on the grain size in the gold film by assuming a $AuIn_2$ density of 11.31 g/cm^3 from the weighted average densities of gold and indium. This diffusion coefficient range confirms the reported Au–In diffusion rate since it is within one order of magnitude of Zhang, $D_0 = 1.2\times10^{-8}$ cm^2/s, and may differ only due to experimental and measurement differences. Regardless, these diffusion rate magnitudes are incredibly fast, especially for metal–metal diffusion, making this an excellent choice for TLP. The Au–In interdiffusion rate is plotted against temperature in Figure 3.4. At a bonding temperature of 200 °C (473 K) the diffusion rate is 8.1×10^{-11} cm^2/s and for a gold layer thickness of 1.0 µm (the thickest used in CHAPTER 5 and 6 experimental work), the total diffusion time required to perform TLP is calculated from Eqn. (3.1) to be only 30.8 s and would still occur in only 5 min at an order of magnitude slower.

The work of Saw and Siekhaus gives the density of $AuIn_2$ to be 10.266 g/cm^3 [115] which follows the rule of mixtures since it lies between that of indium (7.3 g/cm^3) and gold (19.32 g/cm^3) [116]. The CTE of $AuIn_2$ is reported to be lower than both gold (14.1 µm/m/K) and In (33.0 µm/m/K) at 11.4 µm/m/K [115]. This is a promising value amongst the lowest of all potential high-temperature die-attach materials, lower than all Au–Sn, Au–Si, and Au–Ge solders (12.0–17.5 µm/m/K) and even lower than high-lead SnPb85 solder (27.2 µm/m/K) [117].

Furthermore, the line compounds of gold-indium are relatively ductile according to Humpston which can greatly increase their reliability [118]. The system shows excellent durability in this work which indicates high reliability.

Table 3.2 – Select Material Diffusion Properties

Base	Interlayer	D_0 $\frac{cm^2}{s}$	E_A (eV)	*D(200 °C)*	Ref.
Si	Dry O_2	2.144E-9	1.23		[94]
Si	Wet H_2O	1.072E-9	0.78	5.28e-18	[94]
Si	In	1.443	3.565	1.562e-38	[94]
Au	In	6.43e-6	0.46	8.11e-11	[103]
Ti	In	0.02	2.695	3.95e-31	[119]
Sb	In	1.8e-11	0.311	8.77e-15	[120]
Pt	In	0.037	0.961	2.15e-12	Derived [121]

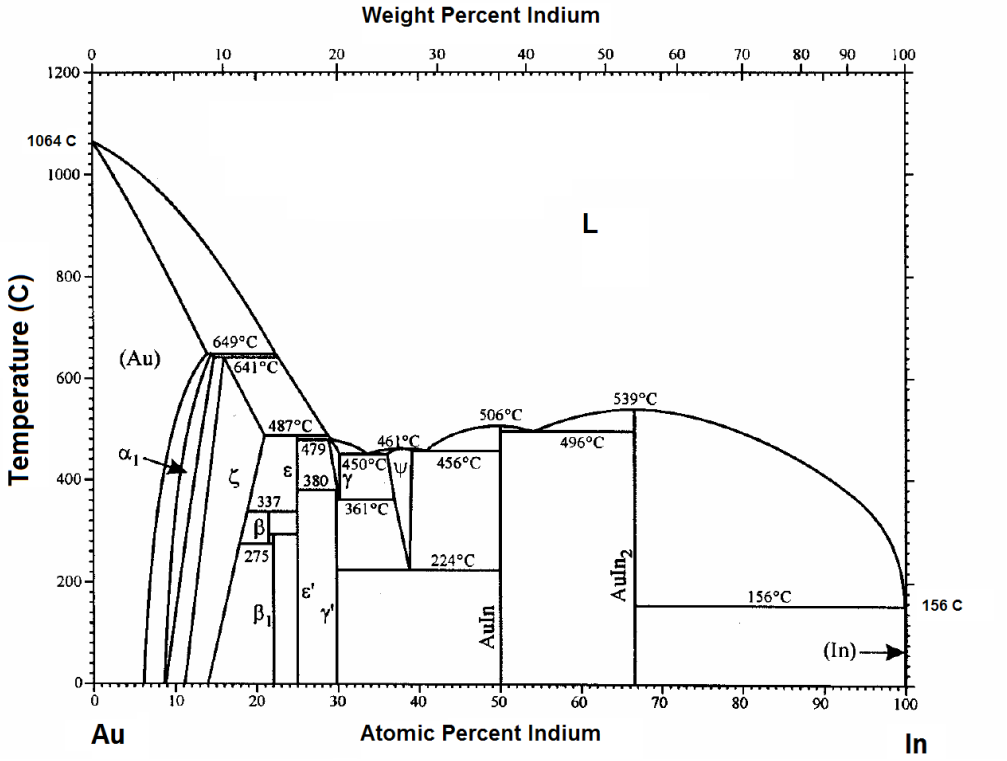

Figure 3.5 – Gold–indium binary system phase diagram [7]

3.2.4 Additional Base–Interlayer Pairs

Many other combinations of base and interlayers exist for TLP die-attach besides Au–In. Indium as well as tin are the two most common interlayers used because of their low melting temperature which coincides with acceptable device processing temperatures and are also diffusive into other materials which may be used as base layers. Gallium has been investigated in the past as an interlayer and was one of the first ever conceived as such by Harman in preliminary TLP research but has never been investigated more seriously likely due to its extremely low melting temperature (29.8 °C) [122]. Other materials such as magnesium, aluminum, and antimony have been also used but their melting temperatures exceeding 1000 °C are not tolerable for even an expanded packaging fabrication process for SiC devices, therefore indium and tin remain most common for die-attach TLP [89].

The three most common base metals for TLP have emerged as gold, silver, and copper resulting in six highly common TLP pairs with interlayers indium and tin for pairs: Au–In, Au–Sn [123–126], Ag–In [101], [109], [127–132], Ag–Sn [92], [133], [134], Cu–Sn [92], [135–142], and Cu–In [143–145]. These have been investigated because of their stable compounds with the interlayers along with fast diffusion rates and chemical stability. Copper is emerging as the most popular base with new research because of its low expense and familiarity amongst packaging materials but it suffers from oxidation issues [92]. Silver is attractive because of its high ductility, nearing that of gold, however it is expensive but without the same oxidation advantages as gold [146]. And gold, as mention in the previous section, is expensive as well but has the highest know ductility of any metal thus it can withstand stress well and is oxidation resistant to ease fabrication difficulties and storage costs [147]. The copper TLP system phase diagrams are shown in Figure 3.6 and Figure 3.7 which contain few eutectic points.

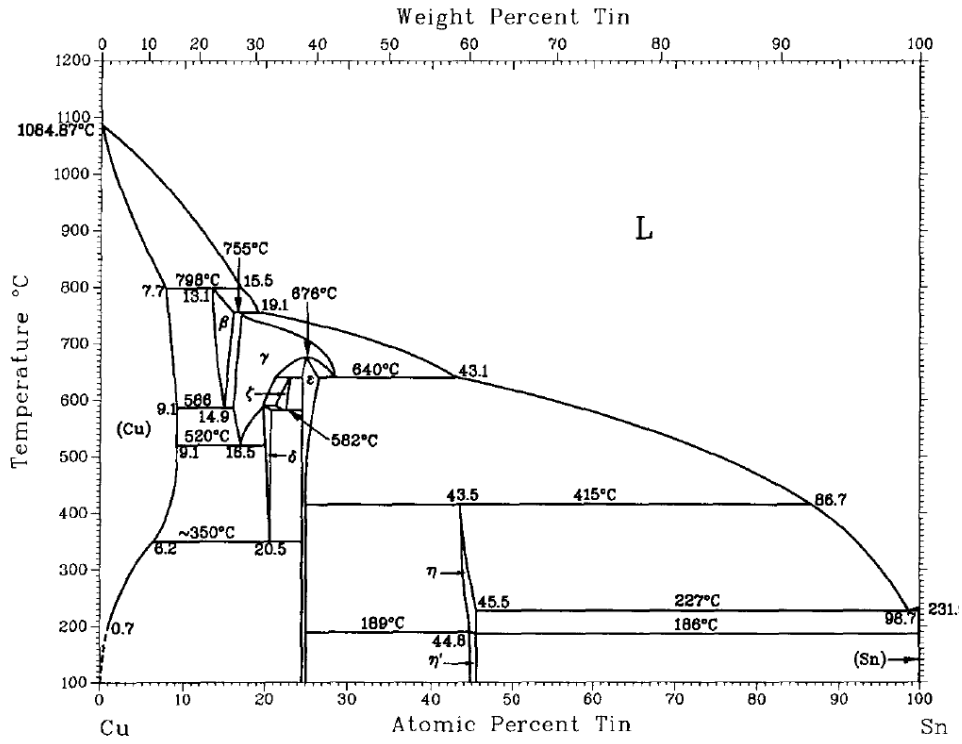

Figure 3.6 – Copper–tin (Cu–Sn) phase diagram [142]

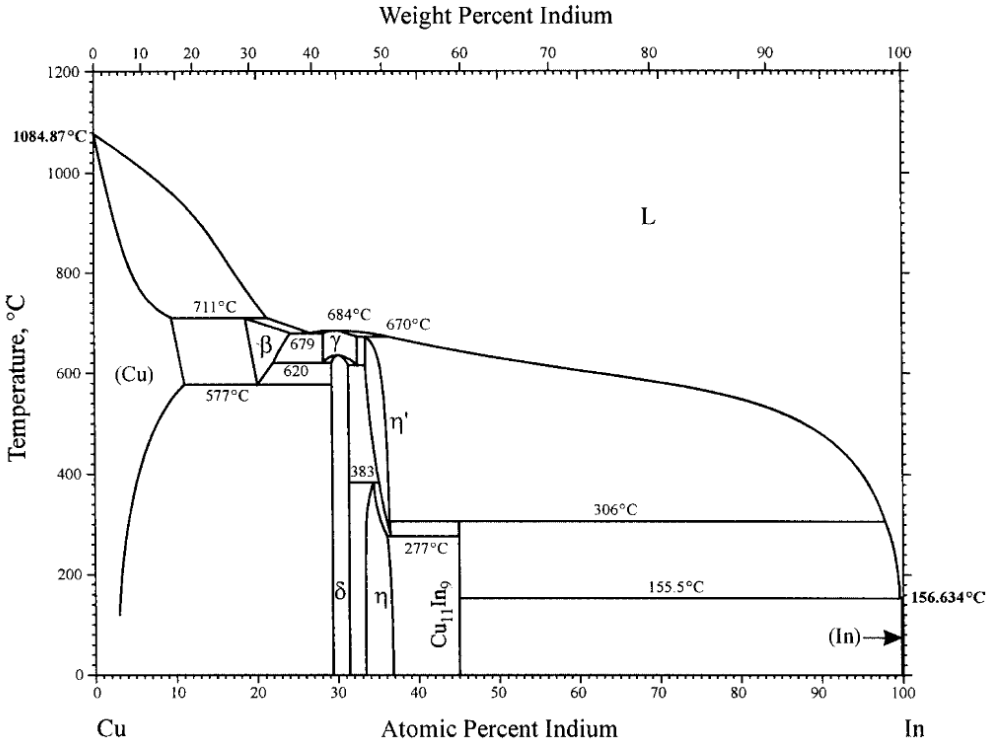

Figure 3.7 – Copper–indium (Cu–In) phase diagram [145]

3.2.5 Barrier Layers

Ancillary layers such as barrier layers are also necessary for TLP die-attach. Because the interlayer is intentionally diffusive into the base layer, it is problematic because it may diffuse into other packaging materials as well and degrade them or change their properties thus a good barrier layer is strongly necessary. Additional sacrificially barrier layers may be also required to avoid forming unwanted intermetallics with the barrier layer and the base or interlayer. Also, adhesive layers can typically be beneficial in all layer deposition, especially for die-attach to increase the shear strength and a thus is preferred in TLP bonding applications.

To protect the other package materials a barrier layer that will contain the base and interlayer from leaving the TLP composite is used. Titanium is a common barrier layer material used for decades for this task and works well for TLP also. Newly formed binary metallic phases typically have lower diffusion rates after isothermal solidification is complete, therefore the greatest attention for the barrier is paid to the diffusion of the interlayer [109]. The rates of the two most common TLP interlayer materials, indium and tin, have been investigated for their diffusivity into titanium and the rates are exceptional. While $D = 8.1\times10^{-11}$ cm^2/s in the Au–In system at 200 °C, diffusion in the Ti-In system is between 3.95×10^{-31} cm^2/s < $D_{Ti\text{-}In}$ < 1.48×10^{-35} cm^2/s, a full +20 X lower magnitude diffusivity than in Au–In [119], [148]. In the Ti-Sn system, D varies between 1.46×10^{-36} cm^2/s and 2.1×10^{-36} cm^2/s at 200 °C, also exceptional, thus Ti appears to be an excellent barrier layer for most TLP systems [149], [150].

For an intermediary layer, platinum has been applied in our work atop the titanium to prevent Au–Ti brittle intermetallics from forming [151], [152]. This layer may be diffused into by indium or tin but this has not shown to be a inhibition to TLP die-attach and therefor can be used in thin layers compared to the thicker base and interlayer (>30 nm) [121]. Tungsten and

TiW have also been shown to give good adhesion of metal thin films to each other and should only improve the shear strength of the bond as well [153].

3.3 Advantages and Limitations of TLP Die-Attach

3.3.1 Advantages

The unique nature of TLP bonding brings with it many advantages for use as a semiconductor die-attach. First and foremost, it has a high operating temperature and wide temperature range which allows for the full range of wide-bandgap semiconductor device operation.

Another unique advantage of TLP is the low processing temperature. Au–In TLP has an operation range up to about 500 °C while the reflow temperature is only around 200 °C. This shields the other components from excessive temperature during reflow which can cause unnecessary mechanical CTE stress or potentially cause unwanted dopant diffusion (although this is a small concern for SiC which requires much higher diffusion temperatures). This low processing temperature also reduces the peak stresses on the die-attach later during normal operation because the temperature at which the die-attach is under no stress, the zero-stress temperature, is lowered. Typically with braze and solder, the zero-stress temperature is at the melting temperature because that is the point when the die-attach becomes solid after reflow and is uncompressed by the adjoined semiconductor or substrate. However as the system continues cooling, the substrate, its metallization, the die, and the die-attach all typically contract at different rates due to un-matching CTEs which impose stress on the die-attach and the peak stress occurs at the lowest operating temperature, typically room temperature. With TLP bonding, because the interlayer melts and solidifies at a much lower temperature than highest

reaches of the operating temperature range, the peak stresses during the temperature cycling of normal operation are significantly reduced which increases reliability and life span.

TLP bonding has also shown outstanding durability – typically an indicator of reliability – with high die-shear strength and force. Die-attach strength is typically compared to Military Standard (MIL-STD) 883, section 2019.8 dictating the minimum shear strength or force of die-attach – depending on die size – in electronics for military consumption which states that the die must withstand 2.5 kgf of shear force before fracturing or 6.08 MPa of shear strength for smaller die. Reported values of TLP die-attach shear force often exceed value by orders of magnitude, regularly exceeding 50 kgf of force with some exceeding 100 kgf of force (the test limit in the reporting work) [125]. This work shows values of up to 57.8 kgf of die shear force along with excellent strength values (§5.5).

Lastly, TLP die-attach can be incredibly thin while maintaining the prior advantages. It is only necessary to have a few microns of interlayer, base, and barrier layers which reduces thermal impedance to negligible levels. This is very useful in the many high power applications TLP die-attach is attractive for.

3.3.2 Limitations

There are some drawbacks associated with TLP die-attach which tempers its quick acceptance into the packaging industry. Two of the largest inhibitions are cost and fabrication complexity. As detailed in the TLP overview section (§3.1), creating a TLP bond is not as simple as solder or braze preforms which can typically be assembled in air then simply ran through a multi-zone reflow furnace. TLP requires the intricate deposition of at least the base material on one component or possible both. It also requires care in ensuring that the interlayer is shielded

from air before reflow in an inert or reducing atmosphere because it is typically prone to oxidation. Pressure must also be applied to the die to break the capillary action of the interlayer or a protective oxidation barrier atop it. Furthermore, several base–interlayer pairs previously investigated involve expensive base layers, less expensive options must be found to work nearly as well for greater packaging integration. Finally, because TLP is typically very thin compared to solder, the surfaces involved must be very planar and without any debris. This is rarely an issue for devices but ceramic substrates must be kept in a more controlled environment than current standards.

CHAPTER 4: OBJECTIVES

The objective of this dissertation is to address needs in the development of SiC and other wide-bandgap power devices. After surveying this field it has been observed that one of the greatest impediments to achieving the integration of SiC devices at high temperatures – one of their major advantages – is insufficient packaging. This has caused an infusion of electrical engineers into packaging design to develop new packages and packaging techniques that will not limit wide-bandgap devices within them. At the premier power device conference in the world, the International Symposium of Power Semiconductor Devices (ISPSD), a packaging section was recently added shortly after wide-bandgap devices began to be more widely discussed. This section has been the fastest growing of the event because of how pertinent this need has become.

This study investigates, develops, and characterizes SiC device packaging with a focus on transient liquid phase (TLP) die-attach for high-temperatures which gives full temperature capability to the devices. Literature has shown that TLP die-attach is by far the most promising technique for securing and interfacing power devices across all temperatures. However TLP has yielded mostly proof-of-concept papers thus far with almost no detailed comparative analysis of different design structures and fabrication routines. This work strives to design a unique TLP die-attach which will greatly enhance existing packaging temperature capability while gaining an understanding of the effect of important design parameters on the electrical, thermal, and mechanical properties.

4.1 Investigation of Thermal and Mechanical Properties of TLP Die-Attach

This work strives to extensively characterizes thermal and mechanical properties of TLP die-attach. Detailed characterization is necessary for the understanding of TLP die-attach, and currently there is very little published on comparative analysis of variant TLP structures or fabrication. In order to refine the TLP bonding process, this work analyzes the effect of multiple design and processing parameters on several TLP bond properties such as their durability, bond quality, thermal resistance, and bond strength.

4.2 Resistive, Diffusive, and Thermal Analysis of TLP Reliability and Durability

The durability of TLP die-attach in response to thermal cycling is also analyzed in order to give an indication of its reliability in normal operation. This has been done by unique means never before utilized for durability analysis in which the occurrence of undesirable material diffusion within a TLP bonds is detected by a shift in the electrical resistivity of the material thin film system. The thermal impedance durability of TLP die-attach is also investigated to see whether there is a breakdown of its superior thermal conductivity with degradation.

4.3 Design and Simulation of High-Temperature Power Electronic Module

This study also investigates the use of the TLP die-attach in a newly designed high-temperature half-bridge module with SiC devices capable of reaching the limits their temperature range. This module incorporates other packaging features beneficial to SiC devices such as having a double-sided cooling design to even more efficiently remove the device heat loss. Also the module will be devoid of wirebonds which are a typical power module failure point and also introduce parasitic inductance into the system which becomes much more problematic when

utilizing the module at much higher switching frequencies that the SiC devices are capable. This module is fully designed and thermo-mechanically modeled using finite element analysis to gauge its durability against thermo-mechanical stresses.

CHAPTER 5: INVESTIGATION OF THERMAL AND MECHANICAL PROPERTIES OF TLP DIE-ATTACH

Thermal and mechanical characteristics of Au–In transient liquid phase (TLP) die-attach are examined for SiC devices in this chapter. Samples with SiC diodes TLP bonded to copper metalized silicon nitride substrates were made using several different values for such fabrication properties as gold and indium thickness, Au–In ratio, and bonding pressure. The samples were then characterized for die-attach voiding, shear strength, and thermal impedance. It was found that the Au–In TLP bonded samples offer high average ultimate shear force of 22.0 kgf and a low average thermal impedance of 0.35 K/W from the device junction through the substrate. It was also discovered that some of the fabrication properties have a greater influence on the bond characteristics than others [154]. The results are believed to be informative of all TLP die-attach and not exclusive to Au–In TLP.

5.1 TLP Fabrication Parameters

In Au–In TLP die-attach, indium is the interlayer and diffuses into the gold base during reflow. There are many choices to consider regarding the design parameters of these materials. The total Au–In TLP thickness is comprised of the gold thickness t_{Au} and indium thickness t_{In}. Indium thickness is assumed to be the most influential on bond quality of the three thicknesses because there is a theoretical minimum and maximum indium thickness for the bond [103]. Indium may completely diffuse away before TLP bonding can begin if t_{In} is too thin, because it begins to diffuse with gold instantaneously upon deposition. If the indium is too thick, it may seep out from the bonding interface due to pressure during reflow.

The ratio of indium to gold thickness, best expressed as the atomic fraction of indium χ_{In} in the TLP bond, is also investigated. This ratio determines the re-melting temperature and phase of the Au–In composition, as shown in the Figure 5.1 phase diagram. Additionally, indium diffusion reliability and TLP electrical resistivity are shown to have a strong dependence on χ_{In} [154]. However, it is unknown whether χ_{In} affects TLP thermo-mechanical characteristics.

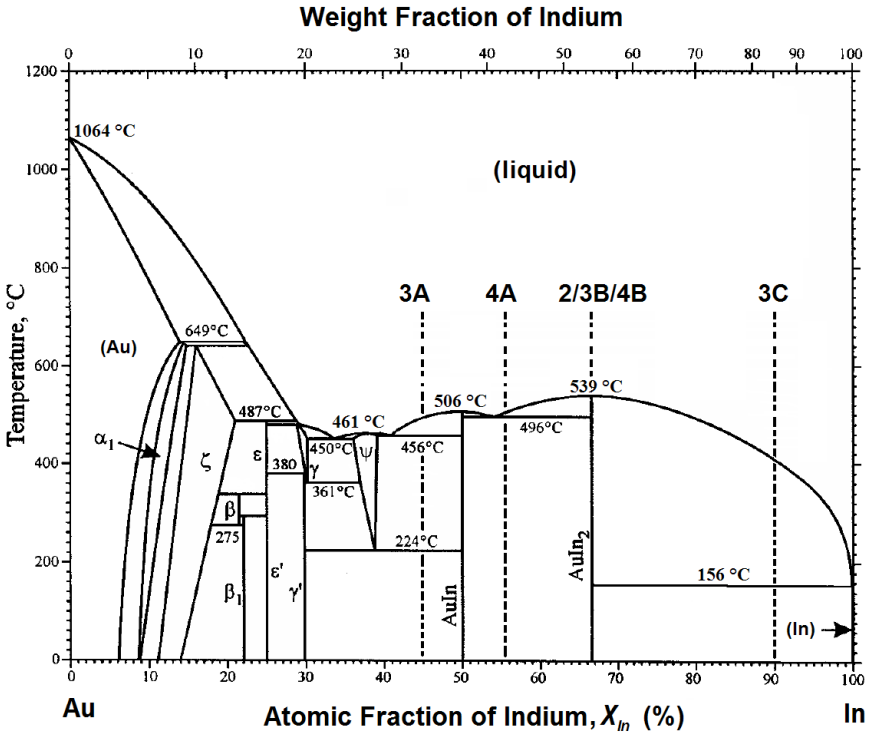

Figure 5.1 – Binary phase diagram of the gold-indium (Au–In) system with TLP diffusive reliability test sample concentrations denoted from Table 5.1 [7]

Bonding pressure ρ_{bond} during reflow is also an important fabrication property. It must induce a quality bond by breaking the surface tension on the molten interlayer during reflow to establish sufficient contact with the base layer. However, if the pressure is too high, the compressed semiconductor die may crack, or indium may be forced out from the die-attach and

seep out (this can also be due to t_{In} being too thick). The three fabrication parameters, t_{In}, χ_{In}, and ρ_{bond}, are examined in this work.

5.2 Sample Fabrication Process

To study the effects of t_{In}, χ_{In}, and ρ_{bond} on TLP die-attach, 25 samples of varying fabrication parameter values were built and characterized. This sample size was sufficient to study how variations in each fabrication parameter affect bond quality and thermal behavior. The sample structures are summarized in Table 5.1 and diagrammed in Figure 5.3. Within the samples, t_{In} ranges in value from 1.26 µm to 4.5 µm, χ_{In} from 0.45 to 0.9, and ρ_{bond} from 0.8 MPa to 5.56 MPa. Each sample was created from a 4 mm by 8 mm SiC JBS diode that was TLP bonded to a 10 mm by 13 mm silicon nitride (Si_3N_4) substrate, with 7 mm by 10 mm of copper metallization.

Due to their higher strength and thermal conductivity than more common alumina and aluminum nitride substrates, these Si_3N_4 substrates are promising for use in specialty environments in which wide-bandgap devices and TLP die-attach are good candidates. They also show excellent adhesion to copper metallization due to a unique active metal brazing process that strongly bonds copper and Si_3N_4 [155]. The high strength of Si_3N_4 also permits the fabrication of copper vias through the ceramic, allowing for more advanced substrate designs and improved voltage isolation for high-voltage SiC power devices [156].

Sample fabrication began by depositing 47 nm of tungsten for adhesion, followed by 150 nm of titanium as a diffusion barrier and 30 nm of platinum, which prevents brittle Au–Ti intermetallics from forming, on to the SiC devices and substrates [151], [153]. The design of the barrier layers was constant for each sample; however, the gold and indium thicknesses varied

depending on the TLP structure of each sample. A gold base layer was sputtered on top of the barrier layers on the copper of the Si_3N_4 substrates, with the thickness being dependent on χ_{In} and t_{In} of the sample. On the SiC devices, barrier layers were followed by an e-beam deposition of an indium interlayer and then 50 nm of gold as an oxidation barrier before removing samples from the e-beam system vacuum. This thin gold layer breaks apart during reflow to allow the indium to diffuse into the gold base layer and is accounted for in χ_{In} calculations [3], [9].

Substrates and devices were then paired to yield the pre-calculated χ_{In} value of each sample. The samples were then inserted into a spring-loaded, custom-designed stainless-steel TLP pressure applicator that applied pressure at specified ρ_{bond} values. The mount was loaded into a 200 °C oven, which was purged of nitrogen, and pumped to a weak vacuum of 1.44 kPa for 15 min. This procedure allowed ample time for the TLP reaction to complete before removing the mount and sample from the furnace to air cool. The reflow time exceeded the thermal time constant for the pressure mount and TLP samples in addition to the diffusion time constant for each of the samples.

The completed samples featuring a SiC diode TLP bonded to a Si_3N_4 substrate are shown in Figure 5.3. The samples were then thermo-mechanically characterized for their die-attach percentage, shear strength, and thermal impedance characteristics.

Table 5.1 – TLP Sample Fabrication Properties for Mechanical Characterization

Sample Set	Thickness (μm)		Atomic Fraction of Indium, χ_{In}	Bonding Pressure, ρ_{bond} (MPa)
	Indium, t_{In}	Gold, t_{Au}		
2 .	3.0	1.07	0.65	0.80
3-A	1.261	1.0	0.45	0.80
3-B	3.087	1.0	0.67	0.80
3-C	3.087	0.223	0.90	0.80
4-A	4.5	2.36	0.55	1.455, 3.02, 5.76
4-B	4.5	1.458	0.67	1.455, 3.02, 5.76

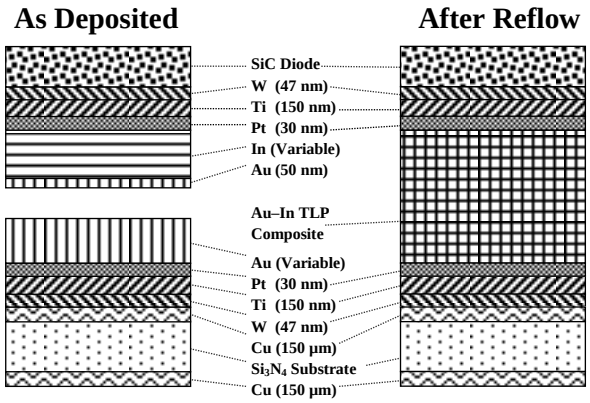

Figure 5.2 – Material stack of a TLP die-attach sample joining a SiC power semiconductor diode to a copper metallized silicon nitride substrate before and after TLP bonding reaction.

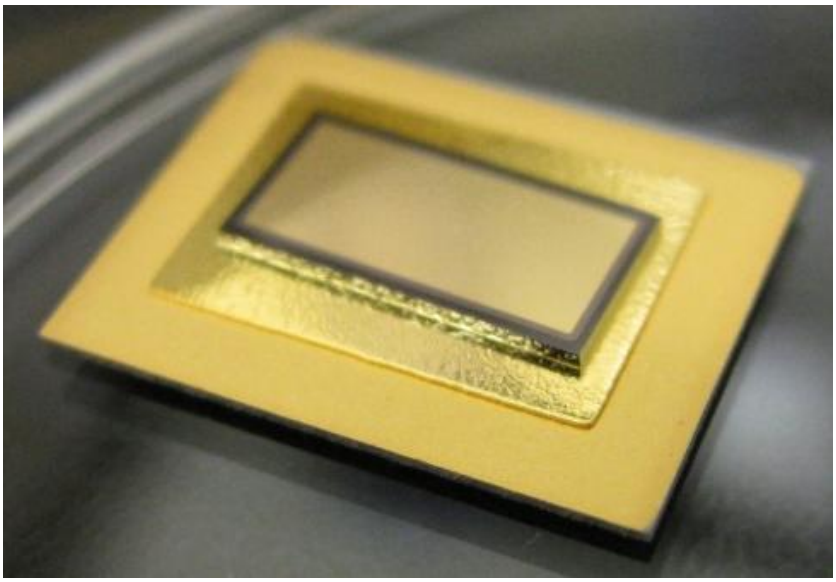

Figure 5.3 – Fully constructed TLP sample featuring a SiC diode and silicon nitride substrate bonded by gold-indium (Au–In) TLP die-attach for thermo-mechanical characterization.

5.3 Die-Attach Percentage

The samples were first inspected by non-destructive scanning acoustic microscopy (C-SAM) to measure the die-attach voiding, which was generally evenly dispersed below the die. The percentage of total die-attach area that is well bonded and has no voids, denoted by the dark area in Figure 5.4, is called "die-attach percentage" $D_{\%}$ and its value is defined as

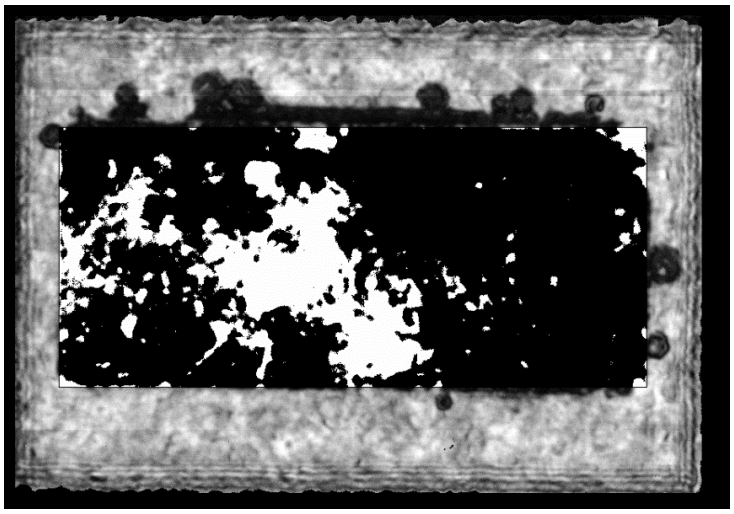

Figure 5.4 – TLP die-attach C-SAM image showing a typical voiding pattern beneath the die in which voids occur evenly distributed.

$$D_{\%} = \frac{\text{Area TLP Bonded}}{\text{Total Possible Bonding Area}}, \tag{5.1}$$

which was measured for each sample. The influence of each TLP fabrication parameter on $D_{\%}$ was then assessed.

Bonding pressure is confirmed to have a significant effect on $D_{\%}$, as shown in the plot of $D_{\%}$ versus ρ_{bond} in Figure 5.5. This correlation is likely due to the need for sufficient contact between the base and interlayer during bonding, for which higher pressure provides. Die-attach percentages are lowest at the lowest bonding pressure. $D_{\%}$ increases with higher values of ρ_{bond} when $\rho_{bond} < 3$ MPa. For $\rho_{bond} > 3$ MPa, $D_{\%}$ increases with ρ_{bond} much more gradually and nearly plateaus. For samples with $t_{In} = 4.5$ µm, to remove the effect of indium thickness on $D_{\%}$, there is similar indication that die-attach percentage increases with bonding pressure.

Indium thickness has a strong correlation with $D_{\%}$, with thicker t_{In} values yielding greater die-attach percentages, as shown in Figure 5.6a. When $D_{\%}$ versus t_{In} is plotted and the data are grouped by ρ_{bond} values, the influence of t_{In} on $D_{\%}$ is isolated from pressure effects. This

observation is shown in Figure 5.6b and confirms the conclusion that increased t_{In} improves die-attach. According to these data, $D_{\%}$ increases linearly with t_{In} for bonding pressures below 1.5 MPa. For ρ_{bond} > 1.5 MPa, the effects of t_{In} and ρ_{bond} are combined for even higher die-attach percentages. Note that in Figure 5.6b, ρ_{bond} and t_{In} appear to exceed thresholds when $\rho_{bond} \geq$ 3.0 MPa and t_{In} > 3.0 µm, likely due to breaking of the sacrificial 50 nm gold capping layer used during fabrication. Bonding with the highest die-attach percentages is achieved at these highest pressures and thicknesses.

Conversely, there appears to be no correlation between the atomic fraction of indium and die-attach percentage, although χ_{In} is shown to be of great importance in diffusive durability in CHAPTER 6. By isolating the effect of χ_{In} on die-attach percentage from the other fabrication properties, it is found that χ_{In} has no effect on $D_{\%}$ in Au–In TLP, shown in Figure 5.7.

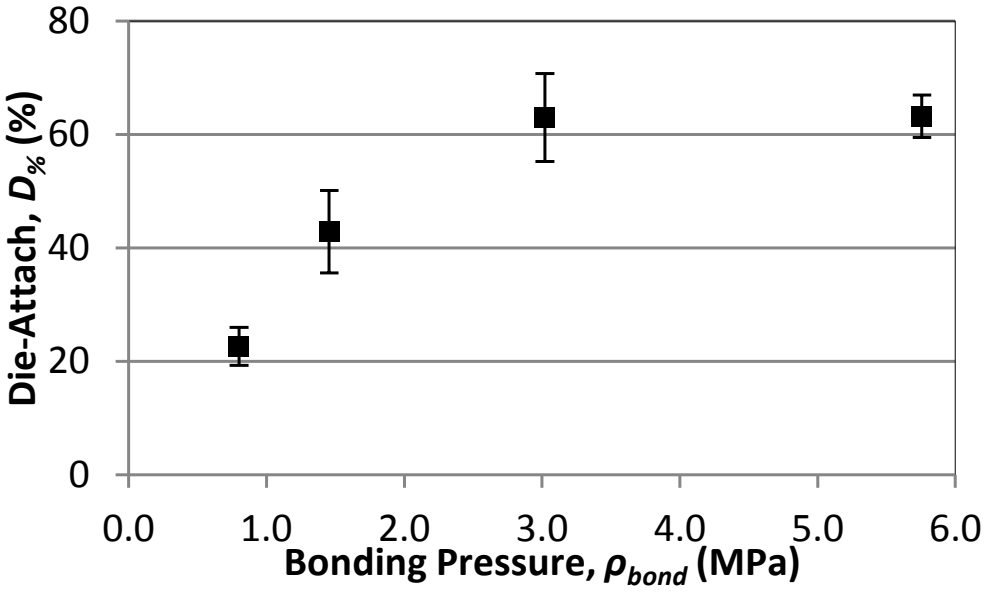

Figure 5.5 – Die-attach percentage of TLP samples indicating a strong correlation to the fabrication bonding pressure. (Error bars indicate one standard deviation.)

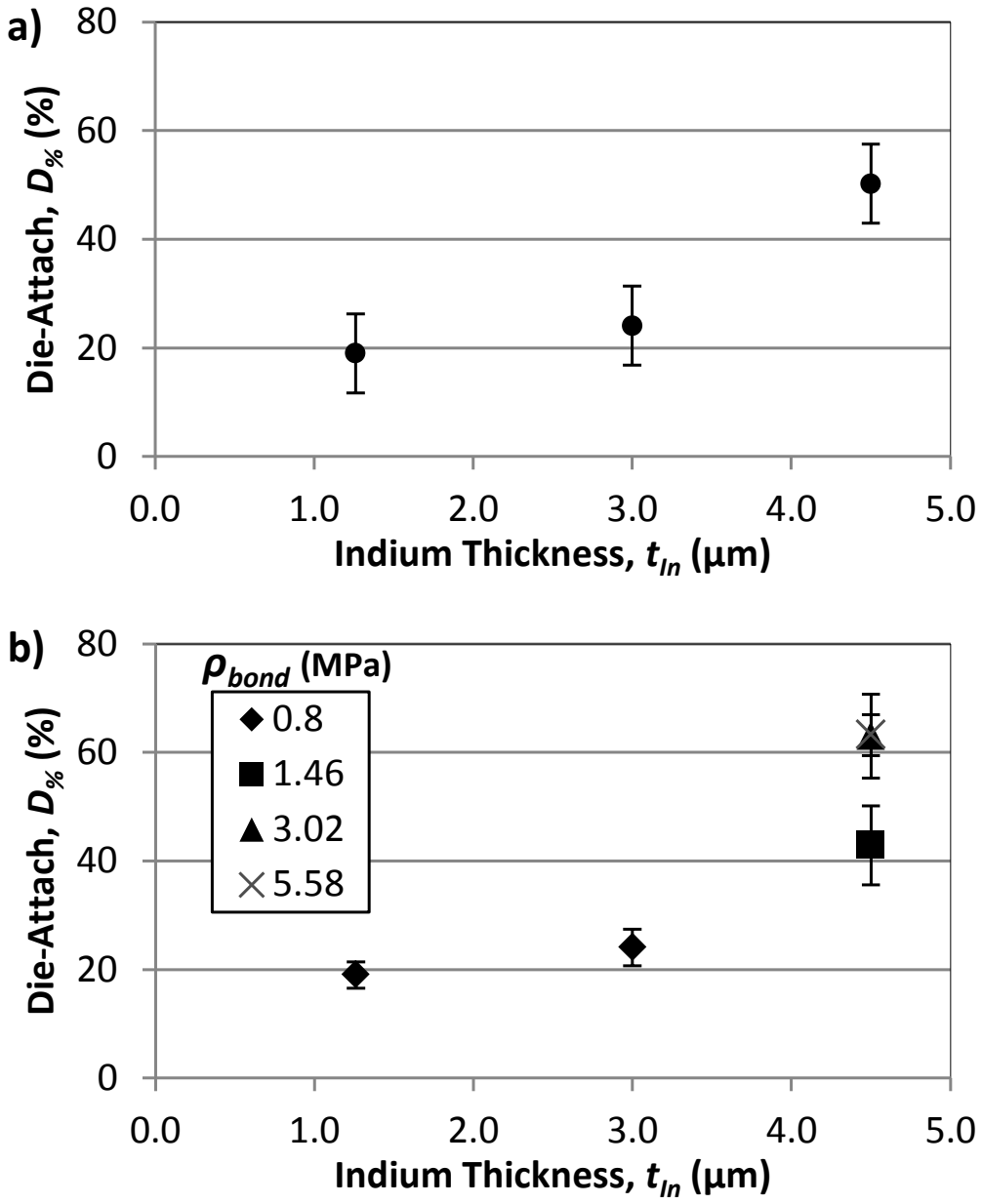

Figure 5.6 – Die-attach percentage of TLP samples showing a positive correlation to thicker indium interlayers. Fabrication bonding pressure is indicated in data of lower plot (b).

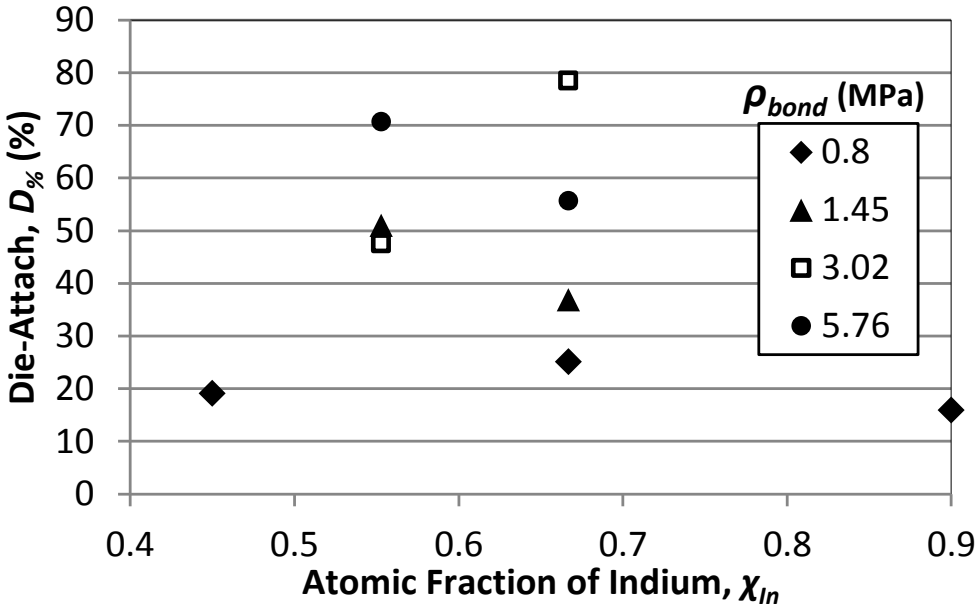

Figure 5.7 – Die-attach percentage data plotted against the atomic fraction of indium showing no correlation of the two properties in the TLP bonds. The samples are segregated by bonding pressure to separate its influence from the indium fraction.

5.4 Thermal Impedance

The junction-to-baseplate thermal impedance Z_{th} was also measured to quantify the effects of the fabrication properties on thermal performance. Z_{th} is defined as the impedance from the average peak junction temperature T_{junc} of the device through the SiC, die-attach, substrate, and thermal grease to a copper baseplate at a fixed temperature. A diagram of Z_{th} is shown in Figure 5.8. Thermal impedance was measured by extrapolating T_{junc} from the temperature dependent forward voltage drop V_F of the SiC diodes in response to a 100 ms 60 W power pulse, at which time the sample is in thermal steady state [157]. The known temperature and power values for each sample were then used to derive Z_{th}. Each sample was mounted to a temperature controlled baseplate with thermal grease using two mounting brackets applied with 0.45 N·m of torque on opposite sides of the sample, as shown in Figure 5.9. This procedure ensured that all results were comparable and unaffected by the

measurement procedure and that the only variations in impedance values were caused by differences in the TLP die-attach layer.

Thermal results are best analyzed as a plot of Z_{th} versus $D_{\%}$, with a fabrication parameter's values being identified of each sample data point, one parameter at a time (i.e., t_{In}, χ_{In}, ρ_{bond}). This plotting technique is necessary because Z_{th} is a function of die-attach percentage expressed by either

$$Z_{th} = \frac{t_{TLP}}{k\ A}\ e^{c_1\ 1-D_{\%}} \tag{5.2}$$

or

$$Z_{th} = \frac{t_{TLP}}{k\ A} + c_2\ \ 1 - D_{\%} \quad , \tag{5.3}$$

depending on the voiding pattern, where k is thermal conductivity, t_{TLP} is the composite TLP material thickness, A is the die-attach area, and c is a constant [158]. To understand each fabrication parameter's effect on thermal behavior, both the value of the parameter and $D_{\%}$ data must be plotted to see a relationship. Additionally, data are plotted versus $D_{\%}$ and grouped by the parameter value because the $D_{\%}$ value is unique for each sample. The average value of Z_{th} is 0.35 K/W. Some samples record higher Z_{th} values than predicted by die-attach percentage in which Z_{th} > 0.5 K/W. These samples show die-attach voiding more concentrated in the center of the die area than typical of the other samples explaining their large thermal impedance.

A subtle correlation of thermal impedance to die-attach percentage is shown across all samples, regardless of any fabrication parameters in Figure 5.10. This correlation is expected, given (5.2) and (5.3), in which higher $D_{\%}$ values result in lower Z_{th} values. A close look at the

data with t_{In} values identified in Figure 5.11 provides an understanding of the influence of both t_{In} and $D_{\%}$ on thermal impedance. It is observed that thicker t_{In} values yield higher thermal impedance for approximately equal die-attach percentages. There is a more exaggerated correlation of falling Z_{th} with rising $D_{\%}$ within each t_{In} value.

No relationship between ρ_{bond} or χ_{In} and thermal impedance was observed. Because ρ_{bond} does not describe the design of a constructed TLP bond but only a fabrication process step, its effect is believed to be confined to influencing $D_{\%}$. Thus, for two samples of equal $D_{\%}$ value, Z_{th} is independent of ρ_{bond}. The lack of correlation of Z_{th} with χ_{In} establishes that the atomic fraction of indium in Au–In TLP material does not greatly affect its thermal conductivity or that the TLP layer is so thin that any variation of conductivity is negligible.

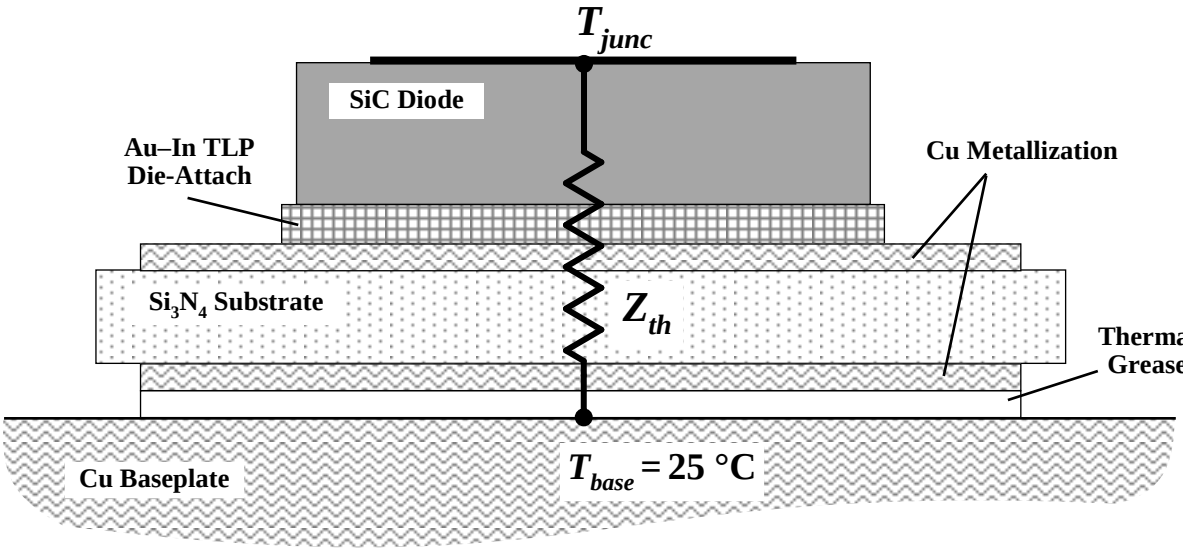

Figure 5.8 – Diagram of thermal impedance Z_{th} from the peak junction temperature T_{junc} through the device, TLP die-attach, metallized substrate, and thermal grease to the fixed temperature baseplate T_{base}. Junction temperature is derived from the measured diode forward voltage drop V_F which is a function of junction temperature.

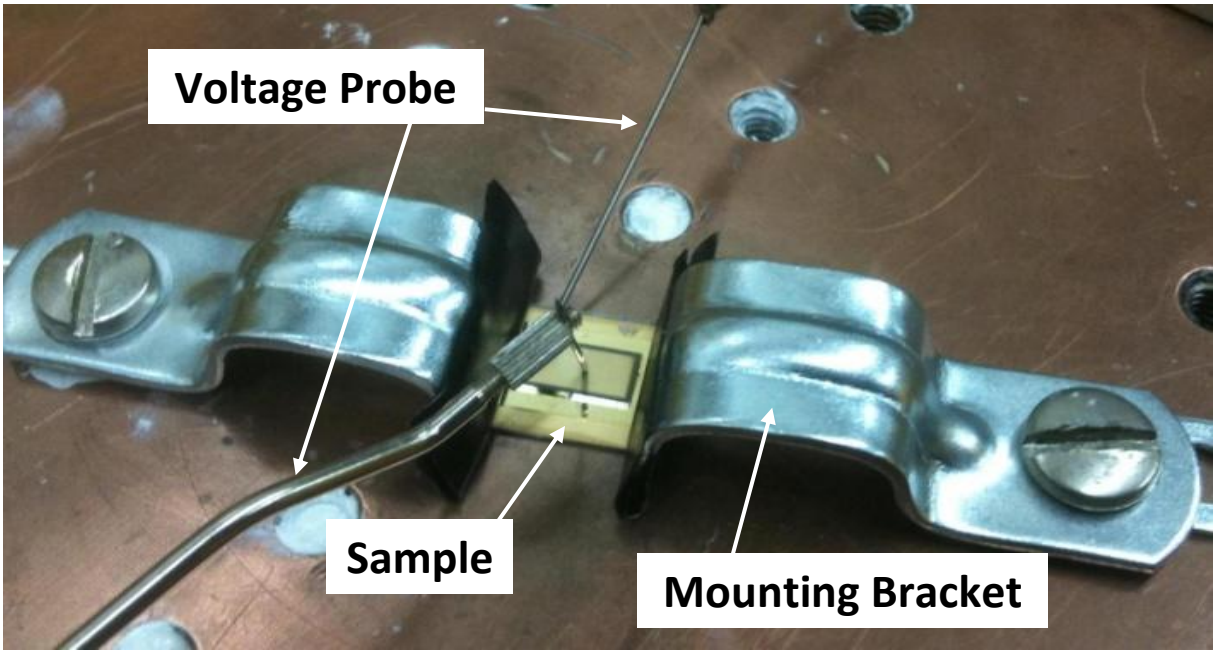

Figure 5.9 – Thermal impedance mounting for characterization of a sample on a cooling baseplate held by two mounting brackets for mounting pressure uniformity. The forward voltage drop is measured through two probing needles and used to extrapolate the peak junction temperature in the SiC diode in response to a heating power pulse during a unique customizable procedure.

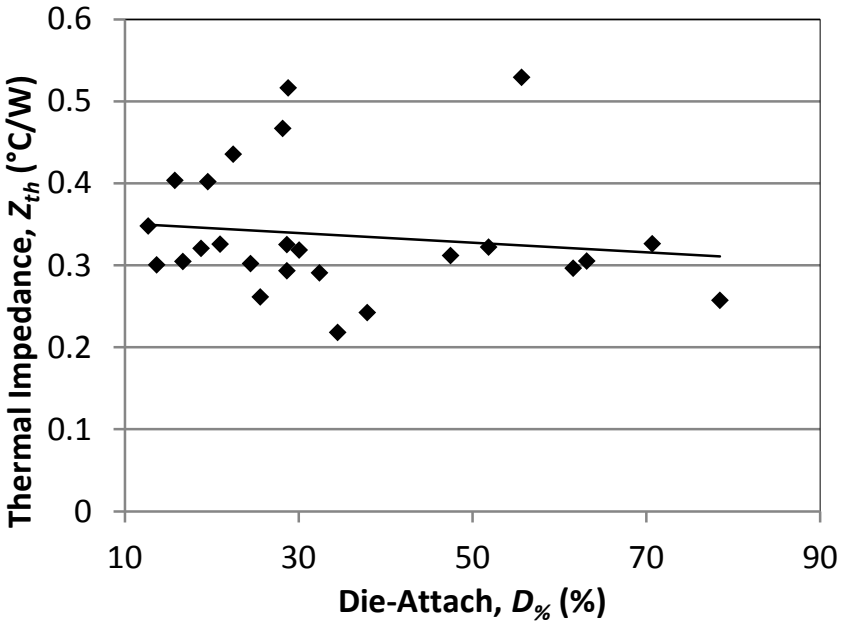

Figure 5.10 – Thermal impedance of each TLP sample plotted against die-attach percentage comparison showing a subtle increase of impedance with decreasing die-attach area percentage.

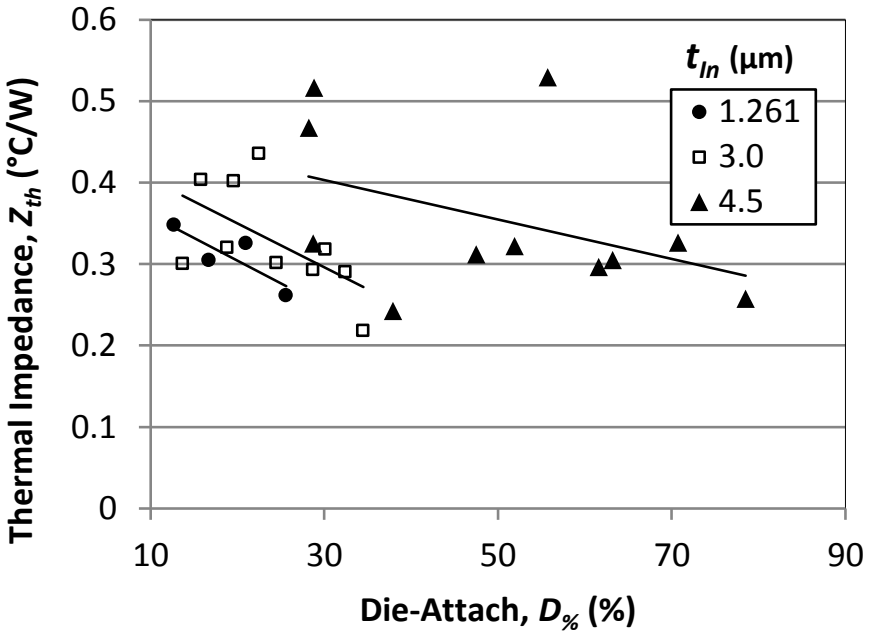

Figure 5.11 – Thermal impedance of each TLP sample plotted against die-attach percentage comparison segregated by indium thickness with linear trends of each thickness shown, indicating lower thermal impedance with thinner indium interlayer independent of die-attach.

5.5 Shear Strength and Force

Most samples were subject to destructive ultimate shear strength τ_{sh} measurement after $D_{\%}$ and Z_{th} characterization. It measures die-attach durability and is a strong indicator of high-temperature reliability and capability. Shear force τ_{shf} data – the force applied to the die perpendicular to the die-attach plane necessary to cause rupture – are plotted versus $D_{\%}$ because it is a function of $D_{\%}$, similar to thermal impedance results. A relationship between τ_{shf} and $D_{\%}$ is seen in Figure 5.12 where higher $D_{\%}$ values lead to greater shear force, as expected. For shear strength data there is no relationship to $D_{\%}$, however voiding does cause stress concentration in

It is customary for electronics packaging literature to use the term "shear strength" for both strength and force values of this property, although the terminology is incorrect. This is due to military standard MIL-STD-883, dictating the requirements of die shear durability, using the term for both pressure and force for given die sizes without deviating from the term "strength" even when larger die sizes are measured in force, independent of die area (which is most common in power devices, is which this work deals). In this work, the author attempts to delineate between the two terms and use them correctly. The term force is used independent of area when literature would use "strength" and the term strength is use for the actual ultimate shear strength of the die-attach, using area and force data.

the die-attach which affect shear strength. When data is isolated according to the fabrication parameter values, additional unexpected relations to τ_{shf} and τ_{sh} are seen.

Indium thickness was expected to have the greatest effect on τ_{shf}, however its influence is small. There is no apparent effect on shear force between different indium thicknesses when $t_{In} \leq 3.0$ µm. However, for $t_{In} = 4.5$ µm, $D_{\%}$ values are higher although the shear force of the samples are approximately equal, indicating that a thicker interlayer reduces τ_{shf} in TLP die-attach. This observation is confirmed with shear strength observation in Figure 5.13 in which thicker indium layers decrease the shear values, which are independent of $D_{\%}$ and area. This is due to greater indium thickness increasing leverage on the substrate–TLP interface which amplifies the shear force and causes rupture at lower strength values.

Furthermore, different χ_{In} values had no effect on shear force durability contrary to Jellison [159] who indicated that there is a negative correlation of shear force with higher indium content in the Au–In system. This relationship was not observed in this work.

Also, bonding pressure unexpectedly does have an impact on τ_{shf}. As shown in Figure 5.14, lower pressure values have greater shear force durability for similar $D_{\%}$ values than samples bonded at higher pressures. This is notable because bonding pressure is a fabrication *process* property as opposed to t_{In} and χ_{In} which describe the *design* of the completed samples and were assumed to have a greater effect on the shear force which they did not. This effect is more clearly seen in Figure 5.15 in which strength data are plotted versus ρ_{bond} and τ_{sh} decreases with increased pressure. A potential explanation for this observation may be that higher bonding pressure increases expansion of the ductile copper metallization on the substrates during reflow heating, which then causes additional stress on the die-attach and reduces τ_{shf} and τ_{sh}.

All shear force values measured exceed the United States Military Standard (MIL-STD) requirement of withstanding 2.5 kgf of force or 6.08 MPA of strength on die-attach [160]. The average ultimate shear force recorded is 22.02 kgf. Most samples exceeded this requirement by several orders of magnitude even amongst those with lower die-attach percentages. The requirement for die-attach to exceed 6.08 MPa of shear strength is used to judge these samples also, although only this rule only is intended for devices below 4.13 mm^2 in area and these samples are 24 mm^2 in area. Regardless, all but one sample passes, with the average τ_{sh} value being and incredible 22.0 MPa.

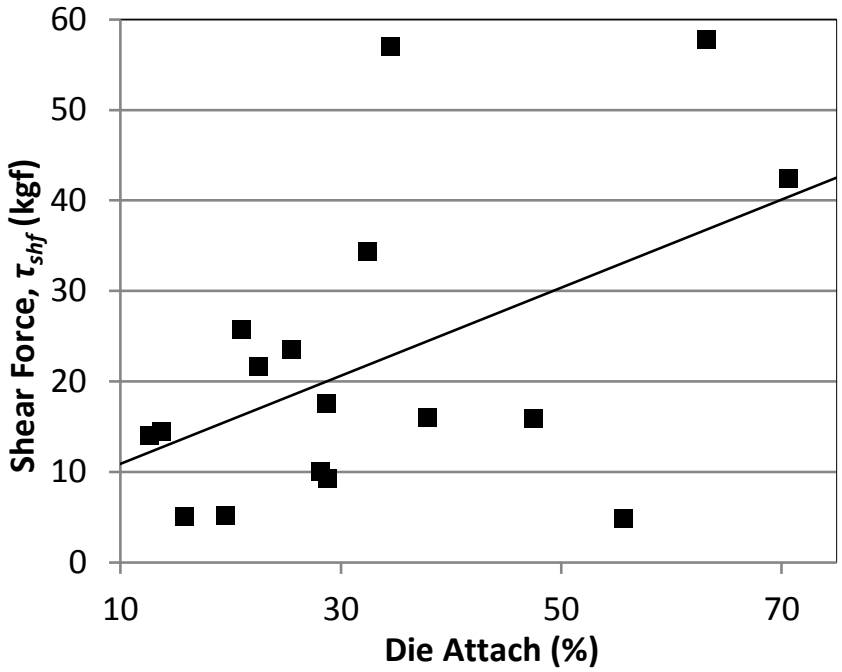

Figure 5.12 – Dependence of TLP die-attach ultimate shear force on die-attach percentage

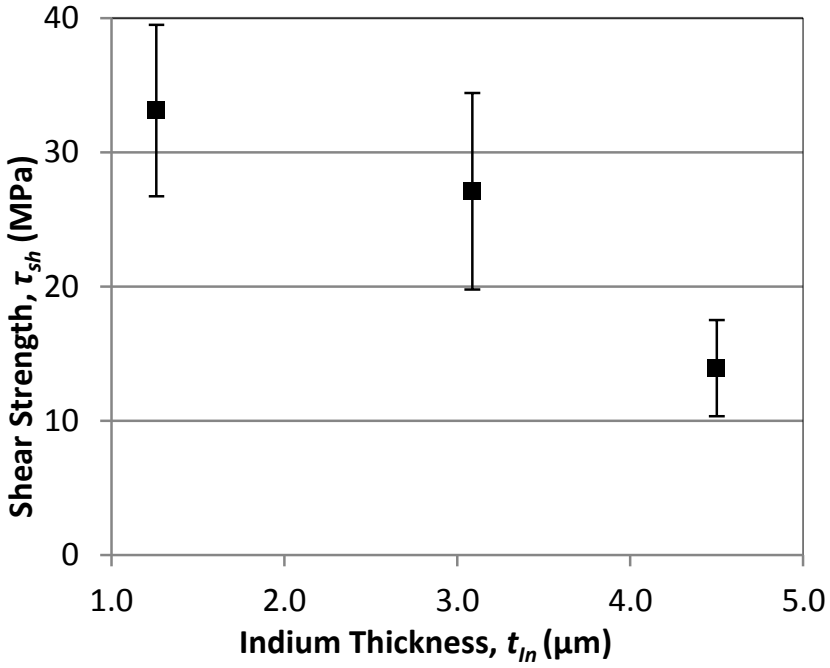

Figure 5.13 – Dependence of TLP die-attach ultimate shear strength on indium thickness.

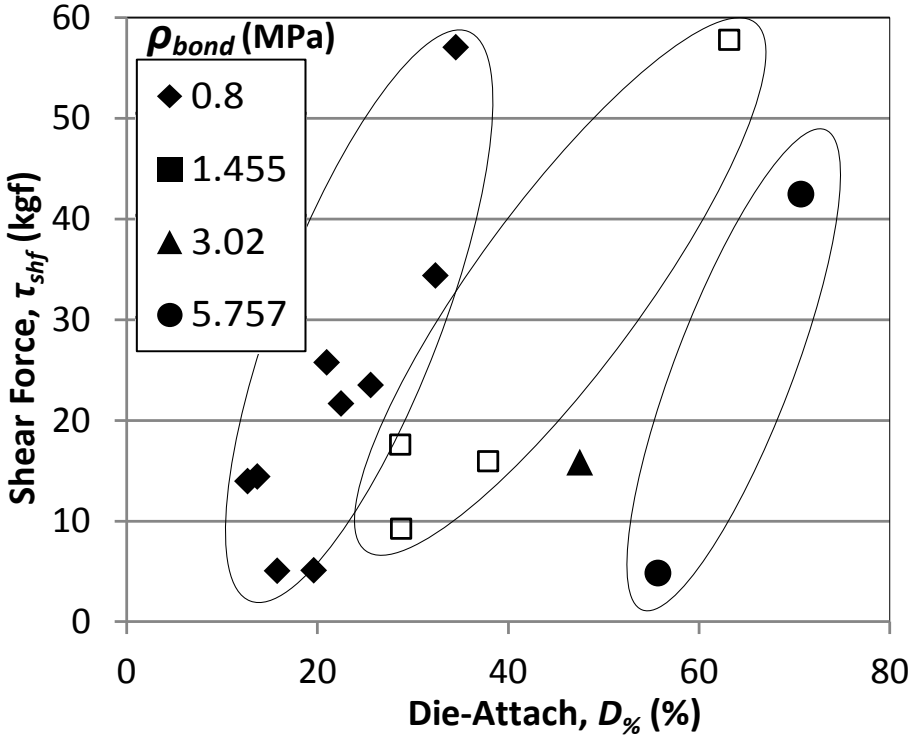

Figure 5.14 – TLP die-attach sample ultimate shear force data plotted against die-attach percentage identified by samples' bonding pressure. Results show higher pressure bonded samples require higher die-attach percentage for comparable strength.

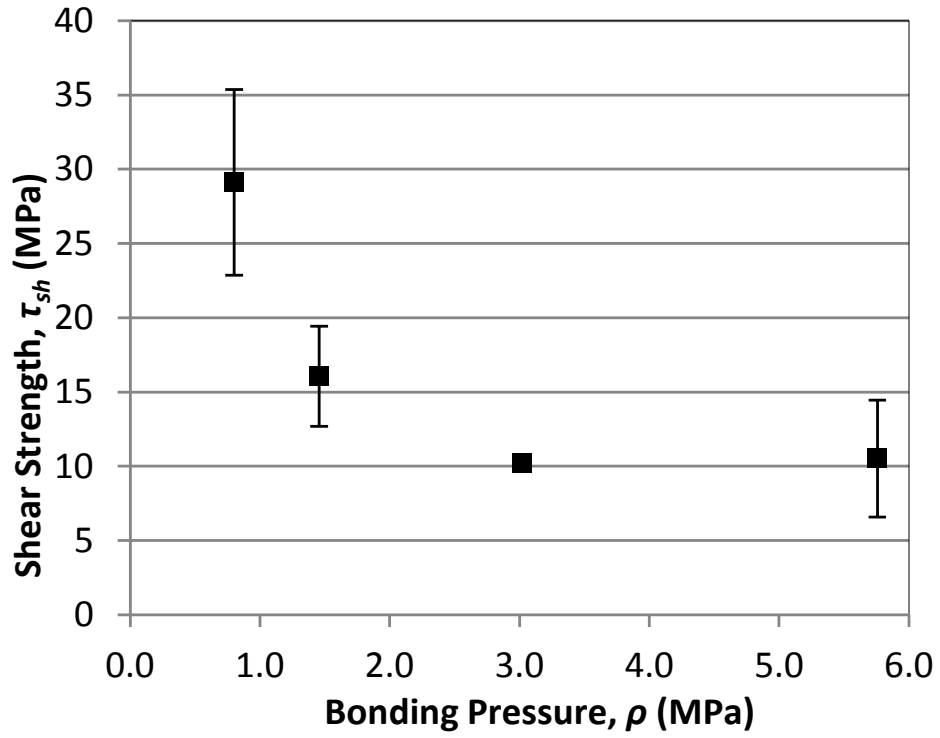

Figure 5.15 – TLP die-attach sample ultimate shear strength versus bonding pressure, showing decreasing strength with increased pressure.

5.6 Thermo- Mechanical Investigation Summary

To achieve quality TLP bonding, interlayer thickness, bonding pressure, and the atomic fraction of interlayer must be carefully considered. The effects of these design properties on the resulting thermo-mechanical TLP bond characteristics have been presented and are summarized in Table 5.2. The fabricated samples have undesirable die-attach percentages but excellent thermal impedances and die shear strengths. More importantly, the results of the data give strong indications of which TLP die-attach characteristics are influenced by the fabrication parameters.

TLP bonding pressure is shown to have a large effect on die-attach percentage and, interestingly, shear strength but not thermal impedance with increasing pressure also increasing die-attach percentage but a tradeoff of decreasing shear strength. The thickness of the indium interlayer has a strong effect on die-attach percentage and thermal impedance, but an

unanticipated weak influence on shear strength where thicker interlayer decreases shear strength and increase thermal impedance but increase the die-attach percentage. Die-attach percentage of the bond, as anticipated, is a major factor for the shear strength and thermal impedance of the bonded samples. Finally, the atomic fraction of In within the Au–In compound does not show any discernible effects on the die-attach percentage, shear strength, or thermal impedance of the samples, although it is shown to have an important effect on the material diffusion reliability.

These suggest that TLP die-attach for wide-bandgap power devices is an attractive option for high-temperature and extreme-environment power electronics.

Table 5.2 – Correlation of TLP Fabrication Parameters with Results

Char. Property → **Fabrication Param. ↓**	**Die-Attach Percentage, $D_{\%}$**	**Shear Strength, τ_{sh}**	**Thermal Impedance, Z_{th}**
Bonding Pressure, ρ_{bond}	Strong	Inverse	None
Indium Thickness, t_{In}	Strong	Strong	Strong
Atomic Fraction of Indium, χ_{In}	None	None	None
Die-Attach Percentage, $D_{\%}$	—	Strong	Strong

Summary of the correlations between the fabrication parameters (bonding pressure indium thickness, and atomic fraction of indium) and the characteristics of the completed bonds (die-attach percentage, shear strength, and thermal impedance) observed in results.

CHAPTER 6:
RELIABILITY AND DURABILITY STUDY OF TLP DIE-ATTACH

The material reliability of gold-indium (Au–In) TLP bonding is investigated utilizing electrical resistivity measurement as an indicator of material diffusion. Representative TLP samples, featuring a TLP reaction, were fabricated by material deposition on glass substrates with multiple Au–In compositions but identical barrier layers for reliability investigation. The samples were annealed at 200 °C and then degraded with thermal cycling. Samples containing high indium content are shown to have poor reliability due to material diffusion through barrier layers while samples containing suitable gold content proved reliable through electrical resistivity measurement, EDS, FIB, and SEM characterization [154].

In this chapter, Au–In TLP samples featuring a TLP reaction have been studied to better understand TLP bonding for high-temperature die-attach. Test samples similar to a TLP bonds with varying Au–In ratios and thicknesses were fabricated, temperature cycled, and characterized for their material reliability during the packaging life cycle. Detrimental material diffusion and electrical resistivity degradation in the TLP materials were investigated in particular.

6.1 TLP Diffusion Experiment

Due to its unique bonding method, TLP die-attach is in need of additional reliability testing beyond traditional approaches to ensure its sustained reliability. Packaging die-attach reliability is often judged by characterization methods such as die-shear strength, voiding percentage, die or solder cracking, or thermal resistance. These characterizations are typically used in tandem with a degradation system such as thermal cycling or high-temperature annealing

to stress the die-attach. Together they have shown to be effective means of judging the reliability of die-attaches and can be used for TLP bonds as well [100], [101]. However, since TLP die-attach contains a highly diffusive interlayer material (e.g., In, Sn, etc.) that is required to fuse with a higher melting temperature material, additional testing is necessary to ensure its reliability. In particular, interlayer atoms may continue to diffuse after the TLP joint is complete and if so, they could reach the semiconductor device where they will cause electrical performance problems or other issues in the package or device.

This can be avoided through TLP structural design. To study it, test samples with gold and indium materials that undergo a TLP reaction are created and are designed to observe for material diffusion while emulating TLP die-attach bonds. Although the test samples feature a TLP reaction they were not constructed through TLP bonding. The samples were created to have the die-attach materials of interest deposited along with their barrier layers on glass slides to electrically isolate them for characterization.

Typically TLP die-attach is investigated by TLP bonding a semiconductor to a metallized substrate, as they are in power modules, however this is an ineffective design to detect for possible TLP material diffusion. The TLP materials exist in the samples, shown in Figure 6.1, exactly as if they had been TLP bonded together but without the semiconductor device and substrate to affect the resistivity. This design also electrically isolates the materials for a unique diffusion characterization technique using electrical resistivity measurement to detect for diffusion which has been confirmed through traditional material characterization techniques afterward. This characterization method was also done for the following reasons:

1) Creating fully bonded samples and evaluating the material diffusion would require destructive cross sectioning of the samples for material characterization by energy-

dispersive X-ray spectroscopy (EDS/EDX) or similar methods. This would not allow for consistent evaluation of each sample throughout thermal cycling which is preferable for accurate results.

2) Material characterization such as EDS would involve time-consuming breaks throughout degradation and would affect results by allowing additional diffusion during characterization down times.

3) The technique of equating electrical resistivity change to material diffusion detection can be done only when the TLP materials are electrically isolated. This is impossible when deposited upon a semiconductor device or metalized substrate.

By creating the TLP samples on glass substrates these problems were avoided and they were able to be non-destructively inspected for material diffusion. Furthermore, by designing the samples as having an accessible top surface it was possible to utilize EDS characterization to confirm the resistivity based diffusion results.

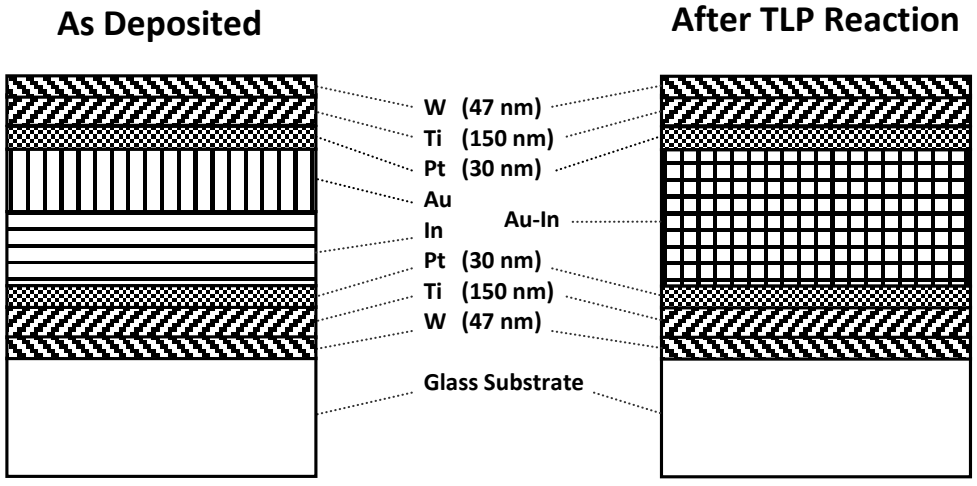

Figure 6.1 – Material stack of TLP samples fabricated in this chapter emulating actual TLP bonds as they are before and after reflow. Gold and indium layer thicknesses vary by sample to create different material ratios seen in Table 6.1.

Table 6.1 – TLP Sample Design Parameters

Sample	t_{In} (µm)	t_{Au} (µm)	wt.% In	χ_{In}	Note
TLP-A	1.261	1.0	0.323	0.45	High Au
TLP-B	3.087	1.0	0.538	0.67	($AuIn_2$)
TLP-C	3.087	0.223	0.84	0.90	High In

6.2 Diffusion Detection through Electrical Resistivity

Material diffusion within a thin film multilayer, like TLP die-attach, is detectable through electrical resistivity measurement parallel to the film surface using a four-point probe. Diffusion is observable as an increase in the measured total resistivity which occurs due to a breakdown of the classical parallel resistor model. This model is similar to common resistors acting in parallel. In it, each thin film sheet resistance acts in parallel to each other to create a total sheet resistance of the thin film multilayer which is easily used to determine the total film stack resistivity ρ_T. When the multilayer resistivity is dictated by this parallel resistor model, as is typical, the conducting electrons of the electrical current each generally stay in a single material layer as they propagate. In this circumstance, the film stack resistivity is described by

$$\frac{1}{\rho_T} = \frac{1}{t_{total}} \sum_{i=1}^{n} \frac{1}{\rho_i} t_i. \tag{6.1}$$

When a small amount of material diffusion occurs between the thin films it causes increased scattering at the material film interfaces which slightly raises the electrical resistivity because it disrupts the conducting electrons [96], [161–164]. However, if material diffusion continues until it becomes excessive, the electrons no longer stay in their original film layer and the films no longer act as parallel resistors with independent sheet resistances. Instead the total resistivity of the multilayer becomes an average of all of the thin film resistivities proportional to

their thickness and the electrons move between the material layers but with greater resistance. The total multilayer resistivity after excessive diffusion has occurred is described by

$$\rho_T = \frac{1}{t_{total}} \sum_{i=1}^{n} \rho_i t_i. \tag{6.2}$$

The total film stack resistivity ρ_T increases greatly as this breakdown occurs, indicating a material reliability breakdown of the thin film multilayer also due to diffusion between the thin films. Regardless of the state of the multilayer, (6.1) or (6.2), the total resistivity will still dictate the sheet resistance as measured by a four-point probe. Thus, monitoring the TLP samples for changes in ρ_T will indicate material diffusion causing a breakdown of the parallel resistor model. This effect is summarized in Table 6.2.

Table 6.2 – Summation of Diffusion Effects on Total Resistivity in a Multi-Layer Thin Film

Magnitude of Diffusion	Effective Resistivity Equation	Sheet Resistance Interaction
Non-Diffused	$\frac{1}{\rho_T} = \frac{1}{t_{total}} \sum_{i=1}^{n} \frac{1}{\alpha\rho_i} t_i, \ \alpha = 1$	Parallel
Interfacial Diffusion	$\frac{1}{\rho_T} = \frac{1}{t_{total}} \sum_{i=1}^{n} \frac{1}{\alpha\rho_i} t_i, \ \alpha > 1$	Parallel
Lattice or Grain Boundary Diffusion	$\rho_T = \frac{1}{t_{total}} \sum_{i=1} \alpha\rho_i t_i, \ \alpha > 0$	Average

When the samples are fabricated the material thin films are well delineated and ρ_T is dictated by (6.1), as shown in Figure 6.2. If there is unwanted diffusion of the indium interlayer from the TLP area into the other thin films, the parallel resistor model breaks down and ρ_T rises

as dictated by Eqn. (6.2). This observation method is utilized on the glass slide samples in this work to detect for diffusion.

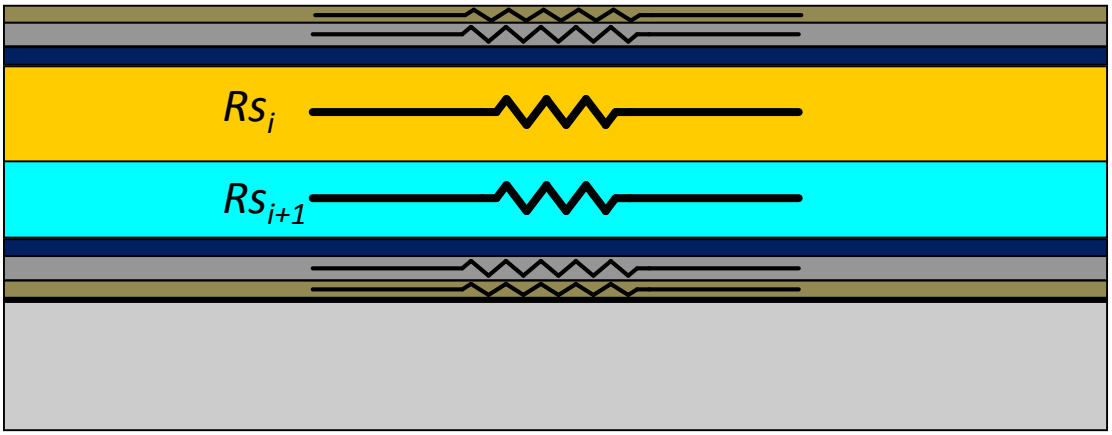

Figure 6.2 – Representation of parallel sheet resistances in a thin film structure whose total effective resistivity changes in the presence of material diffusion between them.

6.3 Diffusion Sample Fabrication

Au–In TLP material samples of varying Au–In thickness and ratio parameters were fabricated in three different designs emulating TLP die-attach samples from thermo-mechanical characterization in CHAPTER 5 to investigate for diffusive reliability. An example of a traditional TLP die-attach bonding a semiconductor device to a substrate can be seen in Figure 5.3. The thickness of the TLP indium interlayer and the gold base layer were adjusted along with the ratio of the two which has a major influence on the resultant bonding compound including its material phase. The barrier layers tungsten, titanium, and platinum were used to aid film adhesion, to serve as a diffusion barrier, and as a buffer to avoid harmful Au–Ti intermetallics, respectively [151], [153]. These design aspects may curtail any possible diffusion in the Au–In design and will be informational in other TLP material pairs as well.

In Figure 6.3, the samples fabricated for this work are shown. Each sample consists of a single indium layer of thickness 1.0 μm or 3.06 μm and a single gold layer of thickness 0.22 μm or 1.0 μm. These two layers were deposited between two identical barrier layers on each side of the Au–In composite, consistent for all three sample structures. The barrier layer stack consists of 47 nm of tungsten applied directly to a glass substrate, followed by 150 nm of titanium, and then 30 nm of platinum adjacent to the gold and indium TLP materials. Following the gold and indium depositions, the barrier layers were again applied but in reverse order. The resultant samples' structure and composition are summarized in Table 6.1.

After all depositions were completed, the samples were then annealed at 200 °C for 10 min under vacuum to achieve the Au–In TLP reaction depicted in Figure 3.1 and Figure 3.3, after which there were no longer separate gold or indium layers but only a combined Au–In layer. Sample TLP-A has a high gold content Au–In composition while Sample TLP-B was designed to be entirely $AuIn_2$ compound, and Sample TLP-C has a high indium content. The sample compositions are identified within the Au–In phase diagram of Figure 6.4 [7].

After fabrication, the samples were subjected to uniform thermal cycling in air to simulate the high-temperature conditions of device operation for reliability characterization, depicted in Figure 6.5. The thermal cycles consisted of a ramp between 25 °C and 200 °C at a rate of 20 °C/min with a dwell at 25 °C and 200 °C for 5 min each for a total cycle of approximately 30 minutes.

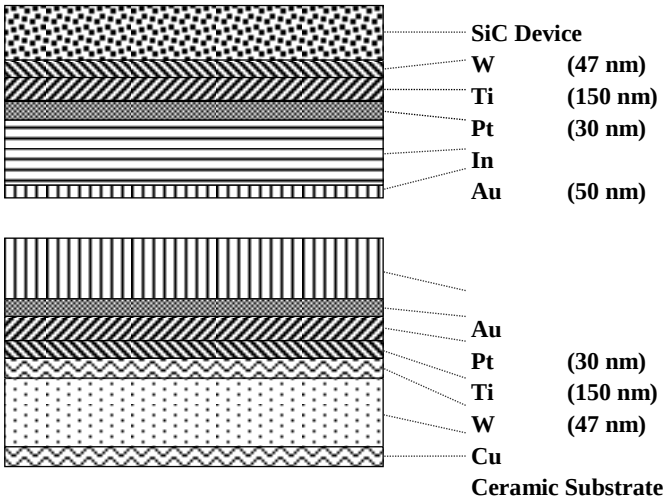

Figure 6.3 – Material stack of a TLP bond attaching a SiC power semiconductor device to a metalized substrate which this diffusion reliability work is designed to emulate

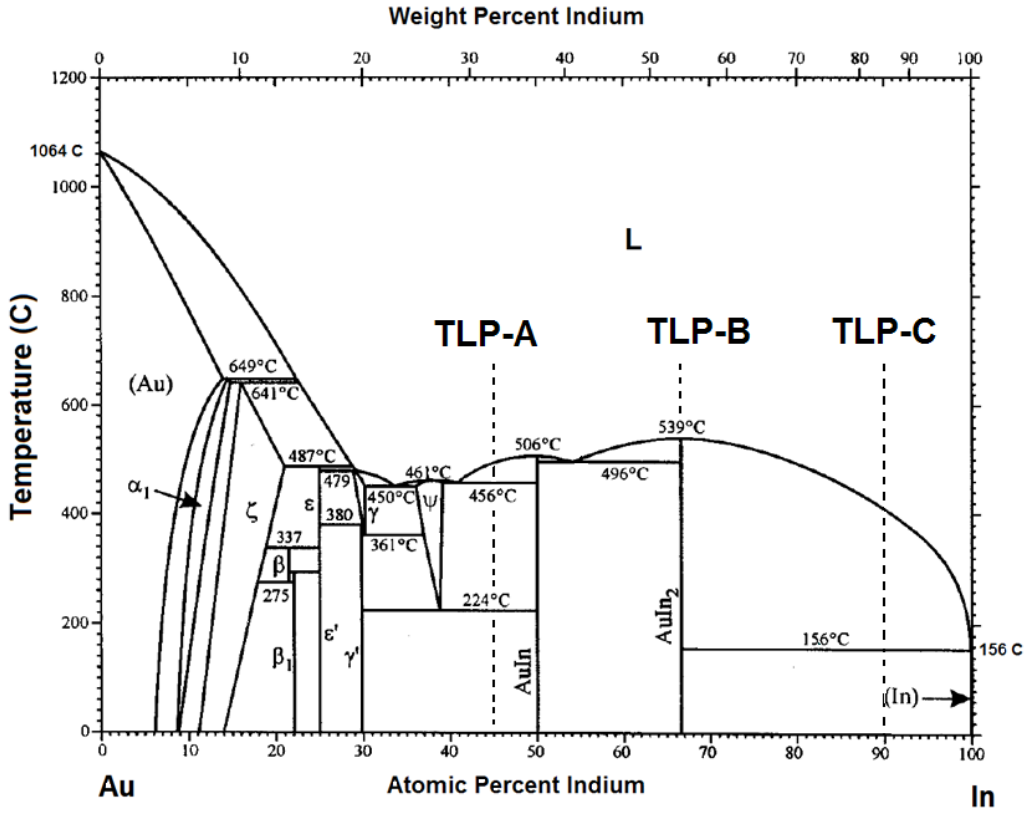

Figure 6.4 – Binary phase diagram of the gold-indium (Au–In) system with three test sample concentrations denoted at indium atomic fractions of 0.45, 0.67, and 0.90 within Samples TLP-A, B, and C, respectively [7].

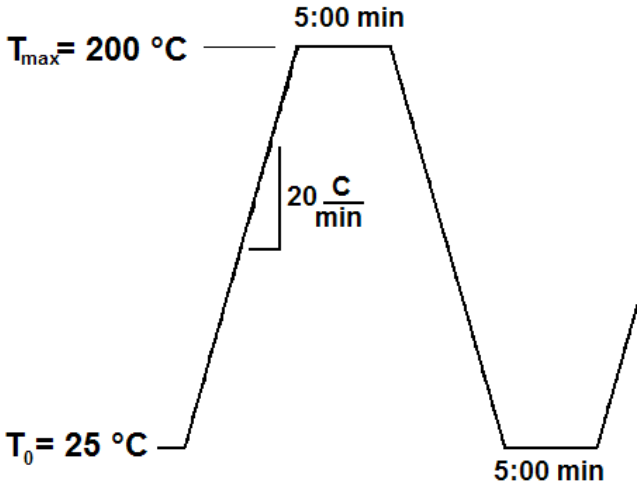

Figure 6.5 – Representation of thermal cycles used to degrade samples and analyze durability and reliability.

6.4 Diffusion and Electrical Resistivity Results

Electrical resistivity of the samples was measured initially after fabrication and throughout thermal cycling. Resistivity measurements were taken using a four-point probe at five constant locations uniformly distributed over the sample surface. Each location was measured using both a 10.0 mA and a 9.00 mA probe current during each characterization. All measurements for each particular sample were then averaged to create a mean resistivity ρ value. Initially, the high gold concentration sample, TLP-A, had an average resistivity of $\rho_{TLP\text{-}A}$=38.9 μΩ-cm as Samples TLP-B and TLP-C held lower resistivity values of $\rho_{TLP\text{-}B}$=14.07 μΩ-cm and $\rho_{TLP\text{-}A}$=14.36 μΩ-cm.

The resistivities of the samples, and of all thin films, differ from the bulk resistivity of the same material due to many factors, not only interdiffusion. Film thickness, grain size, and the material interfaces all increase the resistivity in metallic thin films and their effects were calculated within the samples.

The Fuchs-Sondheimer (FS) effect *h* describes how film thickness affects resistivity. When film thickness is of the same magnitude as the conducting electrons' mean free path λ_0, the interference of conducting electrons with the films' termination planes increases significantly. This causes a reduced effective λ_0 and an increased resistivity. This effect is described by

$$h = \frac{\rho}{\rho_0} = \left[1 - \frac{3}{2k}\left(1-p\right)\int_1^{\infty}\left(\frac{1}{x^3} - \frac{1}{x^5}\right)\frac{1-e^{-kx}}{1-p\,e^{-kx}}\,dx\right]^{-1}, \qquad (6.3)$$

which simplifies to

$$\frac{\rho}{\rho_0} = \begin{cases} 1 + \frac{3}{8k}\left(1-p\right), & k \geq 1 \\ \frac{4}{3k}\frac{1}{1+2p}\frac{1}{\ln\frac{1}{k}}, & k \ll 1 \end{cases}, \qquad (6.4)$$

in which $k = t/\lambda_0$, ratio of film thickness *t* to the electron mean free path λ_0 of the material and variable *p* is the specularity factor, an unknown value which describes the behavior of electrons at the film interface [165], [166].

The average grain size of a thin film also affects resistivity as described by the Mayadas-Shatzkes (MS) *m* effect which relates the average grain size *g* of a thin film to an increase in resistivity. As grain size decreases, resistivity increases because of increased scattering due to the interference of small grains and larger λ_0 values. This relationship is described by

$$m = \frac{\rho}{\rho_0} = \left[1 - \frac{3}{2}\alpha + 3\alpha^2 - 3\alpha^3 \ln\left(1+\frac{1}{\alpha}\right)\right]^{-1} \qquad (6.5)$$

or for extreme values of α, (6.5) simplifies as

$$\frac{\rho}{\rho_0} = \begin{matrix} 1 + \frac{3}{2}\alpha, & \alpha \ll 1 \\ \frac{4}{3}\alpha, & \alpha \gg 1 \end{matrix}, \tag{6.6}$$

where

$$\alpha = \frac{\lambda_0}{g}\frac{R}{1-R}. \tag{6.7}$$

In Equ. (6.7), α is expressed in terms of a reflection coefficient R intrinsic to the amorphous material describing the electrons' exit from the material grains [167].

The variables p and g are known only through direct measurement of each film in isolation which is impossible when sandwiched within a film stack. For this reason, it is necessary to approximate for comparison to the measured results. R values for each material are taken from literature [168–172], grain size is evaluated as $g = t/2$ for room temperature deposition [41], and a standard assumption of $p = 0.2$ is used for the specularity factor [173]. The modified barrier layer resistivities are shown in Table 6.3.

The resistivity of each material layer then allows for the calculation of the resistivity of the isolated Au–In TLP layer ρ_{Au-In} from the measured total material stack resistivity $\rho_{T,mes}$ given by

$$\frac{1}{Rs_{total}} = \frac{1}{R_{s,Au-In}} + \frac{1}{R_{s,W}} + \frac{1}{R_{s,W}} + \frac{1}{R_{s,Pt}} + \frac{1}{R_{s,Pt}} + \frac{1}{R_{s,Ti}} + \frac{1}{R_{s,Ti}}, \tag{6.8}$$

or

$$\rho_{T,mes} = t_{stack}\left(\frac{t_{Au-In}}{\rho_{Au-In}} + 2\,\frac{t_W}{\rho_W} + 2\,\frac{t_{Pt}}{\rho_{Pt}} + 2\,\frac{t_{Ti}}{\rho_{Ti}}\right)^{-1}, \tag{6.9}$$

where R_S is the sheet resistance of each layer or total sheet resistance as $\rho_i = R_{s,i}t_i$. The resistivity of the Au–In TLP layer ρ_{Au-In} in each of the samples is then calculated by accounting for Fuchs-Sondheimer and Mayadas-Shatzkes resistivity modulation with the results of $\rho_{TLP\text{-}A}$=39.98 μΩ-cm, $\rho_{TLP\text{-}B}$=13.2 μΩ-cm, and $\rho_{TLP\text{-}C}$=13.3 μΩ-cm.

It should be noted that the pure $AuIn_2$ resistivity of 13.2 μΩ-cm from TLP-B compares excellently with a deviation of only 0.43 μΩ-cm from Seyffert *et al*. who directly measures pure $AuIn_2$ without need for extrapolation from a material stack, indicating that $AuIn_2$ compound was formed during TLP-B fabrication as designed [164]. The much larger resistivity of TLP-A is also agreeable since the Au–In TLP composition is composed of AuIn and other high gold content phases shown in [133] to have resistivities as high as 51 μΩ-cm.

Although these agreeable resistivity values are promising, the primary reason for measuring the initial resistivity values of the samples is to establish a baseline for comparison during degradation.

The resistivity will not change due to a change of the film thicknesses because that is rigid and completely eliminating all grain boundary scattering effects will result in only an approximately 5 % resistivity change which may occur due to Au–In crystallization during thermal cycling. Conversely, the effect of material interdiffusion may occur and has shown to cause large changes in thin film resistivities and therefore will be more evident.

Through 100 thermal cycles, there is negligible change in resistivity of Samples TLP-A and TLP-B with the higher gold concentrations while TLP-C, with a higher concentration of indium, shows a large increase in resistivity indicating degradation of the Au–In TLP bond. After only 200 thermal cycles, the resistivity of TLP-C has increased by 79 % to ρ_C = 25.66 μΩ-cm and by 95 % after 600 cycles to ρ_C = 28.04 μΩ-cm. Over the same period of 600 cycles, TLP-A

rises only 4.04 % and TLP-B just 4.54 %, indicating little change within the TLP bond. The increase in the sample resistivities due to degradation is plotted in Figure 6.6.

The large resistivity increase in TLP-C is due to the breakdown of the classical parallel resistivity model described previously in (1). As indium atoms exit the Au–In layer, they increase interface scattering between thin films which then causes the films to stop acting as independent resistors in parallel but as a single resistor with a weighted average resistivity based on film thicknesses as in (2). In sample TLP-C, the high resistivity titanium layer with ρ_{Ti} = 55.4 μΩ-cm increases the measured resistivity due to this effect occurring in addition to each individual layer's resistivity rising due to scattering. From this, it is concluded that unacceptable levels of material diffusion are occurring in TLP-C.

Visual observation of the samples shows there is a noticeable change in the color of the TLP-C surface in response to the thermal cycling. The observed color changes from a brown color due to the exterior tungsten layer to a blue-gray color indicative of stronger indium presence. The color of the samples TLP-A and TLP-B remains consistently brown with a slight increase in darkness, which is more evident in TLP-A, however there is nothing to visually suggest mass indium diffusion toward the surface.

Table 6.3 – Effective Resistivities and Calculation Properties of TLP Material Layers

Material	Bulk Resistivity, ρ_{bulk} (μΩ-cm)	Thickness, *t*	Reflection coefficient, *R*	Grain size, *g (est.)*	Mean Free Path, λ_0	Fuchs-Sondheimer Factor, *h*	Mayadas-Shatzkes Factor, *m*	Effective Resistivity, ρ_{eff} (μΩ-cm)
W	5.65	47 nm	0.65 [36]	23.5 nm	8.9 nm	1.097	2.515	15.59
Ti	55.4	150 nm	0.17 [37]	75 nm	0.98 nm	1.002	1.004	55.73
Pt	10.6	30 nm	0.8 [38]	15 nm	7.4 nm	1.08	3.684	42.17
Au	2.2	—	0.7 [39]	—	38.1 nm	—	—	—
In	8.4	—	0.26 [40]	—	6.4 nm	—	—	—
AuIn (A)		2.26 μm	—	1 μm	—			39.975
$AuIn_2$ (B)		4.09 μm	—	1 μm	27.6 nm	1.004	1.01	13.205
Au–In (C)		3.31 um	—	1 μm	—			13.299

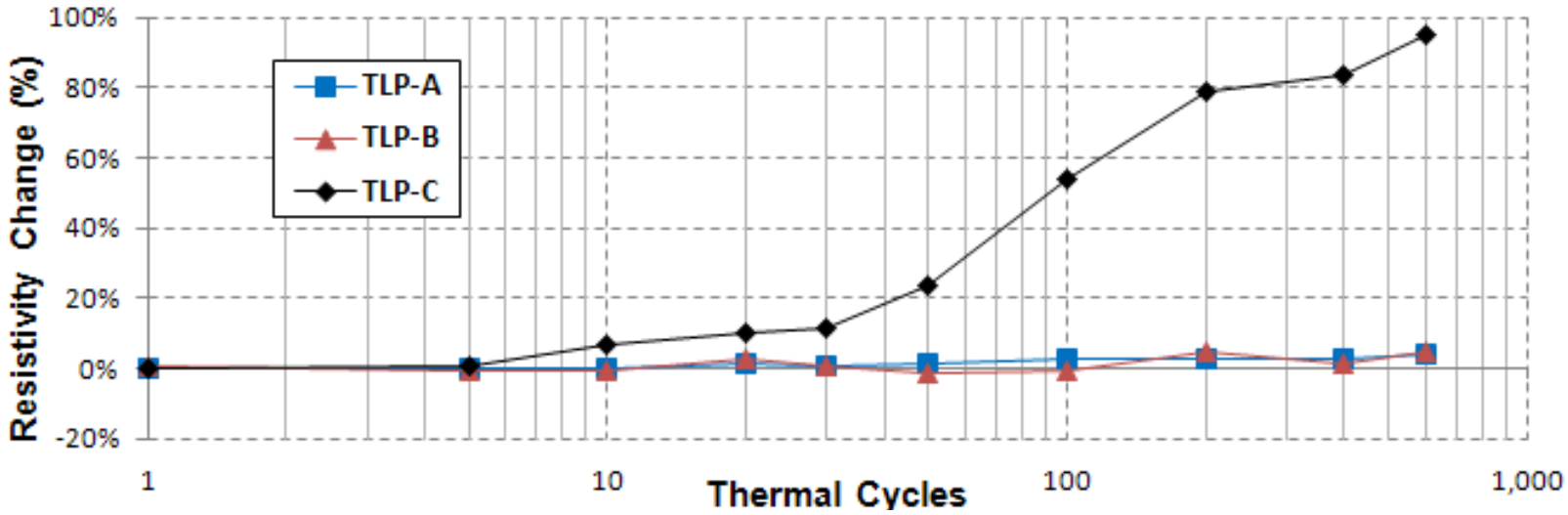

Figure 6.6 – Measurement of resistivity change in Samples TLP-A, B, and C versus thermal cycling degradation showing excellent durability in higher gold concentration Samples TLP-A and B whereas Sample TLP-C, containing excessive indium, exudes poor durability with increasing resistivity, indicating diffusion.

6.5 Surface EDS Characterization

Indium diffusion due to thermal cycling observed from resistivity characterization results in Sample TLP-C and the diffusive stability of samples TLP-A and B is confirmed through EDS characterization taken through the sample's surface normal to the surface plane. EDS is the only material characterization technique with a probing depth capable of sampling below the 227 nm thick barrier layers in this manner. Samples were characterized prior to degradation and after 400 thermal cycles when diffusion is clearly indicated through the resistivity testing. EDS results in Figure 6.7 confirm a sizable migration of indium towards the sample surface in TLP-C.

Samples TLP-A and B show a slight increase in indium detection but settle at an approximately equal intensity of indium detected which likely corresponds to the $AuIn_2$ phase. It has been shown by Wronkowska *et al.* that similarly constructed Au–In films with a high gold content still form large quantities of $AuIn_2$ compound along with the high gold rich phases as expected, particularly γ phase (Au_9In_4), thus the presence of $AuIn_2$ is anticipated in both samples [133]. Conversely, in sample TLP-C although the indium intensity is predictably higher before thermal cycling than in other samples, the intensity still increases over 90 % with cycling, detailed in Table 6.4. This is an unfeasible increase given the diminishing detection ability of the EDS with depth without detrimental diffusion. Therefore, indium atoms must be penetrating the barrier layers [93].

Figure 6.8 shows a focused ion beam (FIB) cut cross section scanning electron microscope (SEM) image of sample TLP-A showing the presence of multiple Au–In phases. The SEM data indicate that the lighter colored portion near the sample surface is $AuIn_2$, whereas the darker portions are likely γ phase (Au_9In_4).

Table 6.4 – Concentration of Indium at Sample Surfaces

Sample	In Intensity (arb. units)		Increase
	Initial	400 Cycles	(arb. Units)
TLP-A	12.53	17.60	5.07
TLP-B	9.71	17.17	7.46
TLP-C	19.71	37.60	17.89

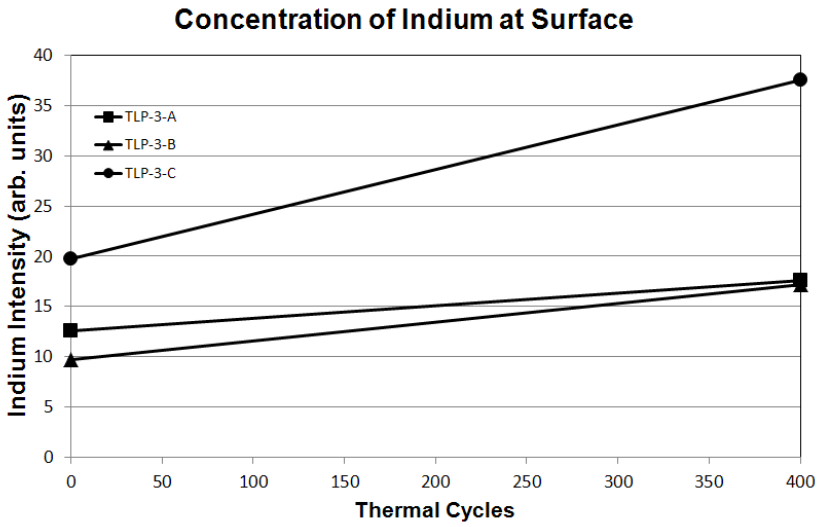

Figure 6.7 – EDS surface characterization of TLP samples showing stability in Samples TLP-A and B and detrimental indium diffusion towards the sample surface through Pt/Ti/W barrier layers.

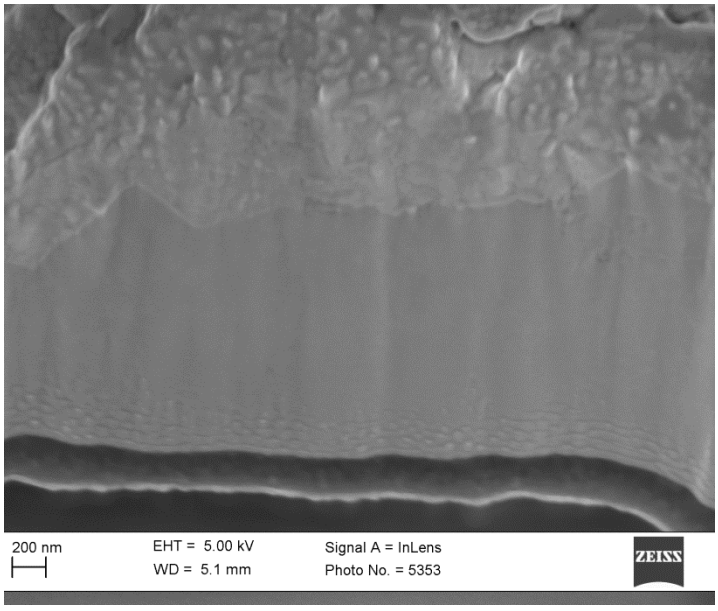

Figure 6.8 – FIB cross section SEM image of Sample TLP-A showing multiple phases present and EDS characterization indicating $AuIn_2$ compound near the surface.

6.6 Thermal Impedance Durability

Reliability and durability of the thermal impedance of TLP die-attach was also investigated through the use of select samples fabricated primarily for mechanical characterization as discussed in CHAPTER 5, Section 5.4 and in Table 5.1, Set 2. In die-attach, a degradation of the bonding material will cause an increase of the transient and steady state thermal impedance when measured from the attached device [174], [175]. The thermal impedance of three TLP samples was monitored while being subjected to thermal cycling degradation; Z_{th} is described by Figure 5.8. The results of Z_{th} as calculated from 15 A, ~60 W power pulses through the attached SiC diodes of lengths 10, 50 and 100 ms are shown in Figure 6.9, 9, and 10 (the power value to determine each Z_{th} value is not approximated in the results, it is precisely measured from each diode's forward voltage drop V_T, it was approximately P = 60 W in each test). Monitoring Z_{th} in TLP die-attach measures an important aspect of its durability and gives an indication of its reliability.

Measured data in the samples shows excellent resilience to cycling. Initial Z_{th} values vary due to the indicated $D_{\%}$ value of each of the three samples, however Z_{th} modulation is likely independent of die-attach value. Therefore, the stability, or lack thereof, of Z_{th} is most important of which, two of the three samples show such Z_{th} stability with the third showing a modest increase with added cycles. In a typical degrading die-attach there is a slight increase in resistance until an exponential rise in resistance occurs indicating die-attach breakdown. This is due to the compounding degradation effects of voiding occurring along with a decrease in the thermal conductivity of the remaining die-attach materials. In power cycling there is a third compounding effect of Z_{th} increasing the peak temperature even further. What is seen in the TLP results below is a *decrease* in Z_{th} which does not indicate degradation of the die-attach but an

enhancement of it. This is likely due to further annealing of the TLP materials past what was necessary for the initial bonding. This effect is similar to what others have seen with improvement of TLP mechanical properties with some thermal cycling or no degradation at all [136]. Also, there is no observance of thermal runaway which would indicate a finite lifetime of TLP die-attach, therefore TLP Z_{th} can presumably be deemed durable for operation under 200 °C and likely much higher up to approximately its re-melting temperature.

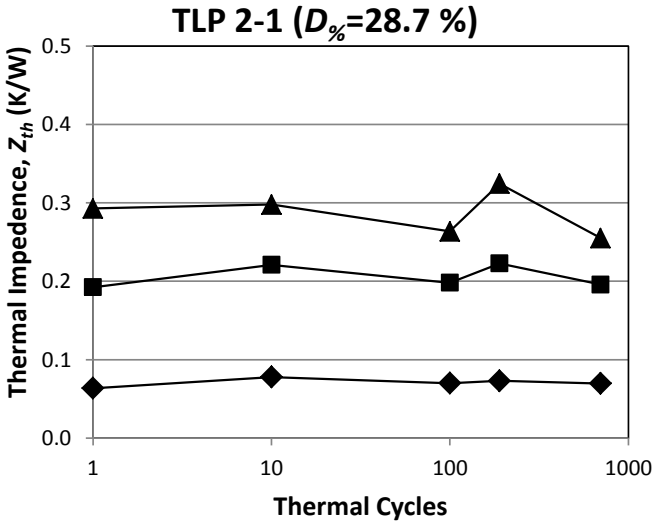

Figure 6.9 – Thermal impedance durability in response to thermal cycling degradation of sample TLP 2-1.

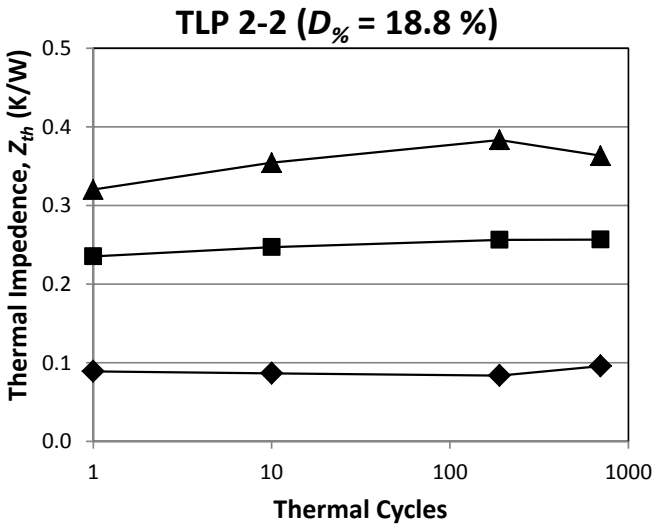

Figure 6.10 – Thermal impedance durability in response to thermal cycling degradation of sample TLP 2-2.

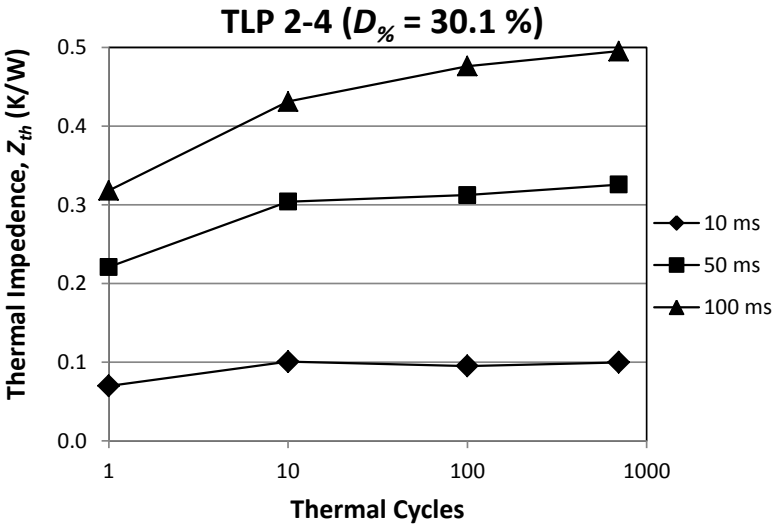

Figure 6.11 – Thermal impedance durability in response to thermal cycling degradation of sample TLP 2-4.

6.7 TLP Reliability and Durability Summary

The reliability of various Au–In TLP formations was investigated through the use of test structures for the application of TLP bonding in high-temperature environments. Samples TLP-A and TLP-B, containing atomic fractions of indium 0.553 and 0.667 ($AuIn_2$), respectively, show excellent electrical and diffusive durability with thermal cycling. Sample TLP-C, with 0.9 atomic fraction of In, was shown to have poor electrical durability due to the diffusion of indium atoms out of the Au–In TLP material pair and into the diffusion barrier which will affect the electrical properties of a power device. Furthermore, an inspection of the thermal impedance durability of TLP die-attach indicated promising results for reliable operation with no thermal runaway effects. A small but discernible shift in thermal and diffusive properties of the TLP composite with annealing indicates that they are functionally graded materials after reflow, prior to long term annealing, although this is does not indicate that a TLP bond is unreliable prior to complete homogenization [176].

By utilizing a TLP design in sample TLP-C in which the highly diffusive indium interlayer was not designed to completely form into Au–In phases – which occur at indium atomic fractions greater than 0.667, the $AuIn_2$ line compound – durability and reliability was jeopardized. It is concluded that TLP designs for power semiconductor bonding applications should not contain a higher content of interlayer material than will completely form into compounds with the base material or there will be an excess of inherently diffusive interlayer material which will affect device performance over time. It is also shown that, although the TLP bonds contain highly diffusive indium atoms, they are stable when designed properly within the Au–In phases and are not expected to pose reliability concerns for TLP bonded devices.

CHAPTER 7: DESIGN AND MODELING OF POWER ELECTRONIC MODULE BASED ON TLP DIE-ATTACH

A novel power electronic module for TLP die-attach implementation has been designed after having thoroughly characterized the bonding techniques and investigating its reliability and durability. The module has been fully designed and simulated and fabrication difficulty concerns have been addressed.

7.1 Design Concept

The new power module is intended for high and low-temperature space-based operation for use in satellite low power delivery electronics which aligns perfectly with TLP die-attach capabilities. The circuit of the module is a half-bridge inverter featuring four SiC power MOSFETs, two switches in parallel on both the high and low sides for redundancy to increase reliability and module operational lifetime. The MOSFETs are provided by Cree Inc. in die form and have a blocking voltage of 1200 V with a peak pulsed current of 85 A, although they will not be used in continuous operation over 10 A at elevated temperatures. No separate anti-parallel diodes are included, the module utilizes the body diodes of the MOSFETs which are capable of handling the current demands of the MOSFETs because the body diodes are also in parallel which assists in current conduction. The simple circuit design can be seen in Figure 7.1. Design goals of the module also include having no wirebonds, double-sided cooling capability, small form factor, low voltage, high reliability, and high thermal conductivity.

Figure 7.2 and Figure 7.3 show the fully designed module. It features four silicon nitride substrates 0.32 mm thick measuring 37 mm long by 40 mm wide with copper metallization

0.15 mm thick active metal brazed to them and extruding 15 mm outward as connection pins to account for the majority of the module. Due to the high strength of silicon nitride it is possible to design copper vias though the substrate in order to have a more sophisticated design. The TLP module traces route away from the devices for voltage isolation and through vias to the five connection pins. The pins include a high and low side voltage bus, two gate connection pins, and the output. Both the "top" and "bottom" of the modules features two substrates with metallization; within these sets; one substrate is TLP bonded to the devices and electrically connects pins to the devices. The other substrate of the set primarily insulates the exterior of the module from the electronics so that it can be adheres to a mount apparatus and also it incorporates additional copper where possible to spread the stress of copper expansion over the substrate and increase reliability. Additionally, a boron nitride filled ceramic adhesive is injected in-plane with the devices to secure the top and bottom substrate sets together. This material offers high-temperature capability of over 850 °C and a CTE very similar to that of SiC at 3.6 μm/m/K and is produced by Aremco. The thermal properties are unreported but are likely poor as are other ceramic adhesive, although it is not in a thermal sensitive location of the module being out of the direct thermal path between the die and substrate faces. Thus, its agreeable CTE makes it a good material for the adhesive material needed with its other properties acceptable for the role.

The Au–In TLP structure of the module is seen in Figure 7.4, featuring a 2.648 μm of TLP material which originates as 2.0 μm of indium and 0.648 μm of gold to form $AuIn_2$ during reflow. This indium atomic fraction of 0.667 is chosen due to previous results indicating its diffusive reliability with the least material cost, as opposed to higher gold fractions, there are also no discernible thermal of mechanical tradeoffs. The 2.0 μm indium interlayer thickness is a

balance of the tradeoffs between increasing die-attach percentage with added thickness and decreasing shear strength and thermal resistance. The die-attach is to be compressed with 3.0 MPa of bonding pressure which is the best compromise of pressure value between increasing die-attach percentage with higher pressure but lower shear strength effects.

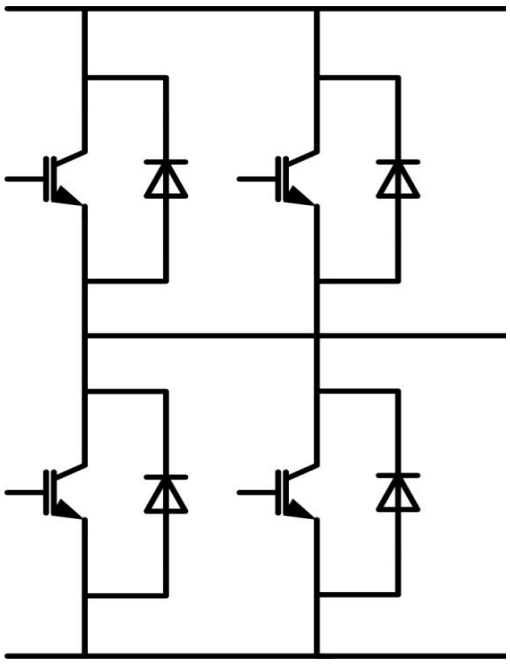

Figure 7.1 – Half-bridge circuit design of high-temperature TLP power module featuring four SiC power MOSFETs

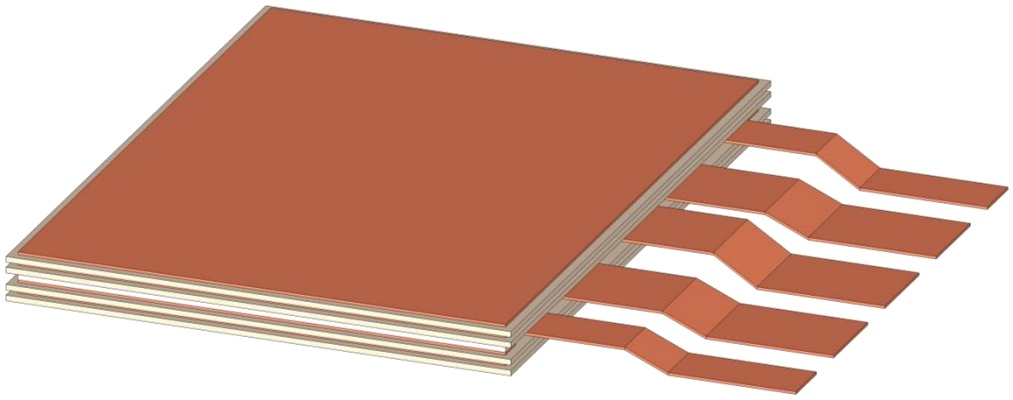

Figure 7.2 – TLP power module design model

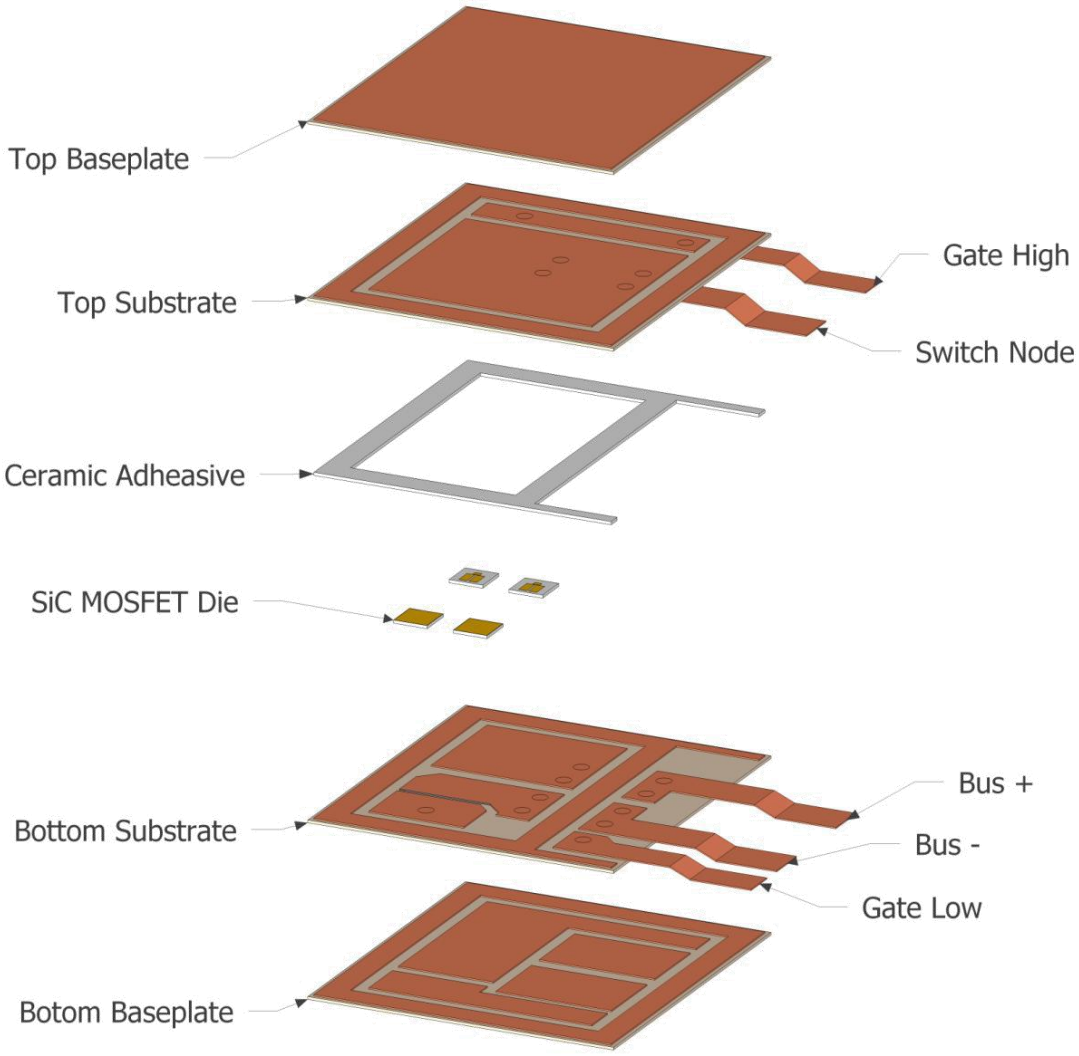

Figure 7.3 – TLP power module exploded view showing all internal components

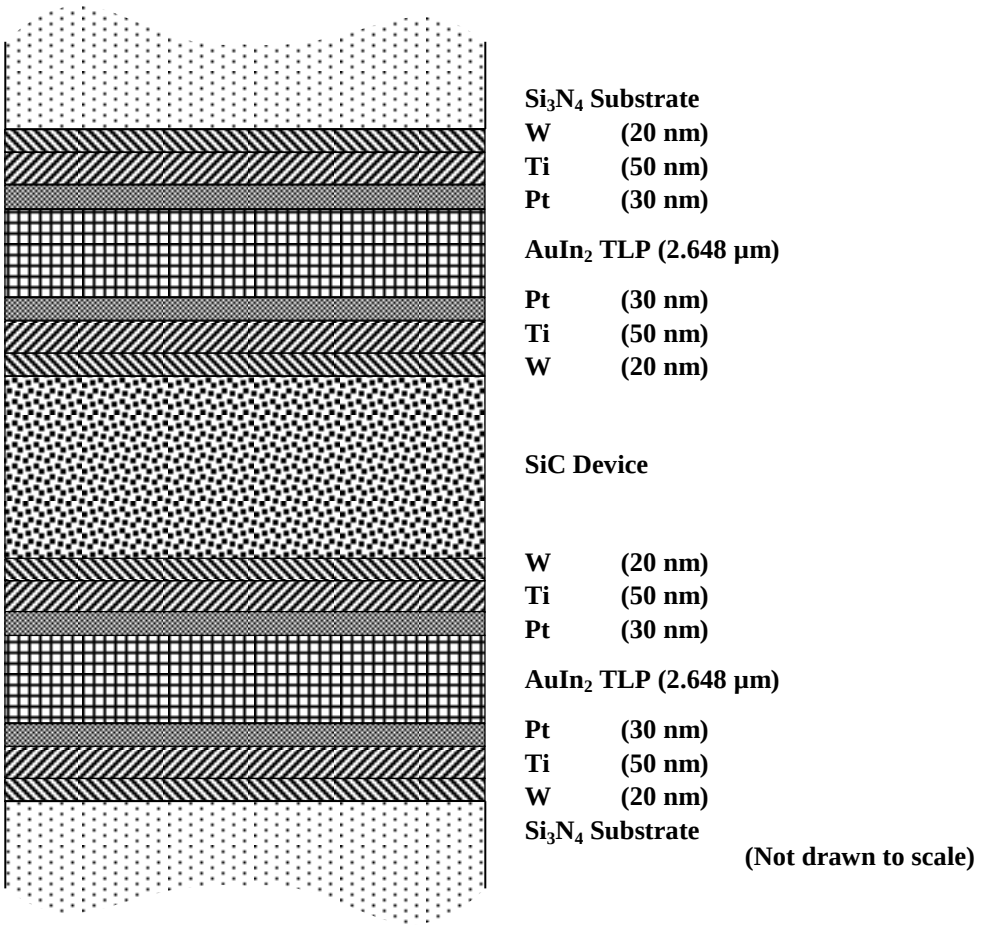

Figure 7.4 – Material stack of a TLP die-attach in new module design surrounding SiC die between substrates

7.2 Finite Element Analysis

7.2.1 Temperature and Thermal Resistance

The TLP power module has been thermally and electrically simulated to assess its capability in the intended space environment including high and low temperature operation. Given the die area, the manufacturer supplied $R_{DS,on}(T)$ data, and a continuous operation current of I_d = 10 A, the power loss per device is approximately 60 W in steady state, which will yield the largest ΔT and thus the highest CTE related mechanical stresses. For these power conditions and the material properties of the module components in the designed geometry the temperature rise in the devices is ΔT = 18.6 °C. This equates to a thermal resistance of R_{th} = 0.31 K/W with double sided cooling; the temperature gradient is identified in Figure 7.5. The majority of the heat flux is through the drain connection due to the larger contact area compared to the source-gate face, however this is a small impediment since R_{th} is much smaller than any reported commercially available device package thermal resistance value.

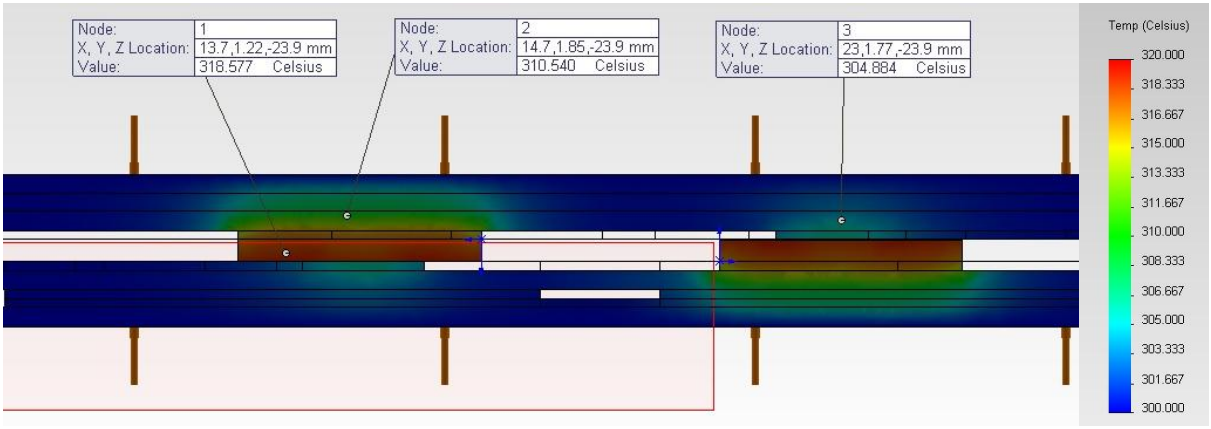

Figure 7.5 – Thermal simulation of TLP power module given normal operating conditions in 300 °C ambient.

7.2.2 Thermo-Mechanical Stress

With the extreme temperatures the TLP module is capable of there is potential for substantial mechanical CTE stress which tests the durability of the module and dictates its long term reliability. The low thermal resistance of the package in conjunction with the moderate device power loss levels reduces this issue to a small degree, however the extreme ambient temperatures it is subject to leads to potentially destructive CTE stress levels which test the ultimate strengths of the module and materials.

In mechanical stress simulation at 400 °C, representing the upper temperature limits of intended intermittent module operation, the stress magnitudes are extreme. The peak stress level in the module is $\sigma_{T,max}$ = 567 MPa occurring in the silicon nitride substrate near the copper vias, this is below the ceramic's flexural strength of 850 MPa. An extremely small volume of the module is subjected to these extreme stresses however; 1 % of total module volume is subjected to above 419 MPa of stress at 400 °C with 60 W of power loss per device. Von Mises stress levels within the copper metallization exceed its rated tensile strength of 220 MPa in 41 % of total copper volume and has an average stress level of 179 MPa. This however does not guarantee rupture since the stresses are internal and if the module is not subjected to exceedingly rapid and repetitive temperature change the damage of this stress condition can be avoided. 400 °C stresses are shown in Figure 7.6. Stress levels at -100 °C are also high with a peak stress of $\sigma_{T,min}$ = 850 MPa and 1 % of total module volume is subjected to stress above 628 MPa which, again, does not exceed silicon nitride capabilities. Copper stress levels are increased also from T_{max} stresses, as is seen in Figure 7.7 where stress peaks are near the vias through the ceramic substrate. No mechanical simulations can prove or disprove module reliability, but only give an indication of its durability which this module shows.

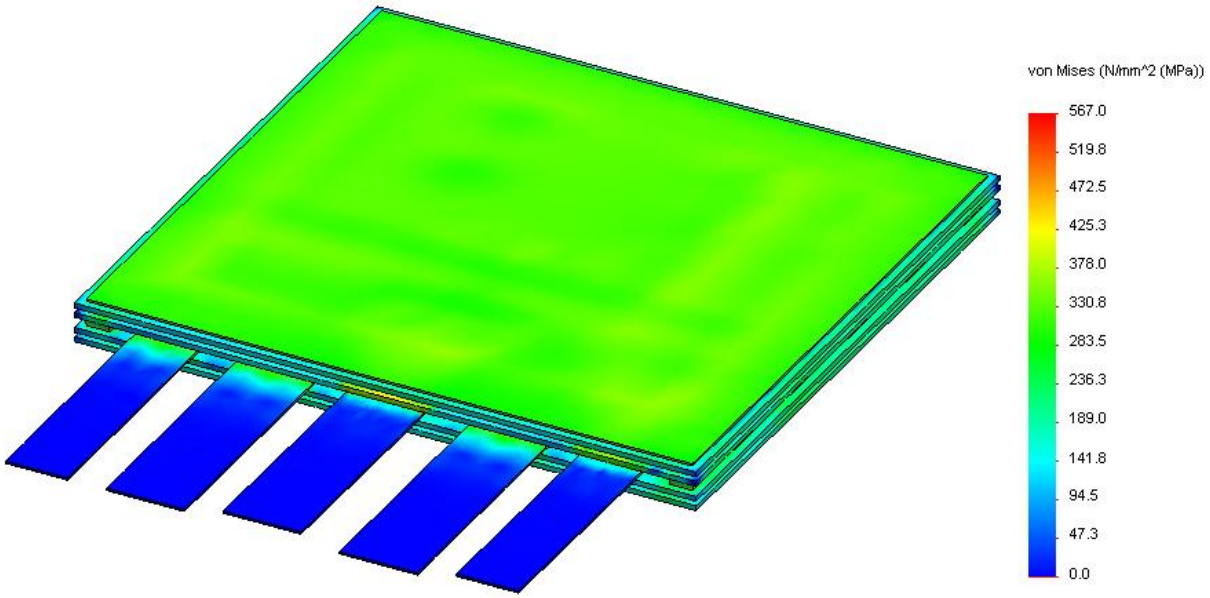

Figure 7.6 – Mechanical stress simulation of TLP module at 400 °C ambient temperature in operation.

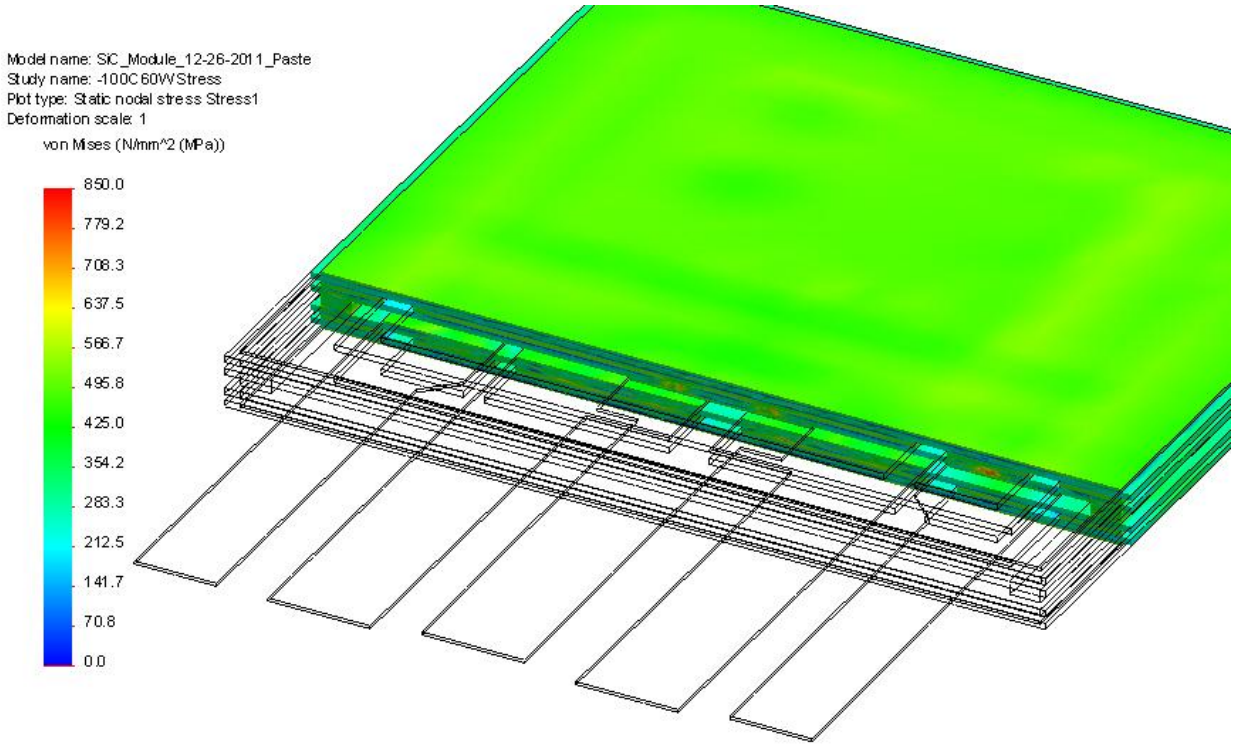

Figure 7.7 – Mechanical stress simulation of TLP module at -100 °C with sectioned view of internal stress levels.

7.3 Module Fabrication Approach

In order to account for a meticulous design of the TLP module, the fabrication of the module must be precisely planned due to small feature sizes. The primary location of concern is upon the MOSFET gate-source die face where the two connection pads are separated by only 70 μm and will cause device and module failure if there in a short circuit or arcing between them. Because of this, there is difficulty in TLP bonding the devices to the silicon nitride substrates which needs to be considered in three ways: substrate design, TLP material deposition, and module assembly.

7.3.1 Substrate Design

Since the gate and source pads of the device are separated by only 70 μm the substrate metallization pads also must be similarly close, however this is much thinner than any substrate manufacturer rates their minimum spacing dimensions. The need to apply a metallic paste between metallization and substrate for the active metal brazing process of silicon nitride increase this gap dimension due to natural seepage from under the copper layer outward. Working with the manufacturer Kyocera, this gap spacing between copper pads has been reduced from the standard minimum width of 1.0 mm to 700 μm in which the metallic paste directly touching the substrate is separated by only 300 μm. This gap spacing requires that the entirety of both the gate and source pads cannot be 100 % metallized and bonded to the substrate since the substrate gap is wider than the device gap, however this is not a considerable issue. As seen in Figure 7.9, the excess gap spacing on the substrate can be placed primarily over the much larger source pad while the majority of the gate pad area can still be TLP bonded to the copper, the

source pad bonding area will be reduced also, but it is much smaller percentage of total potential area and will not significantly reduce reliability or durability.

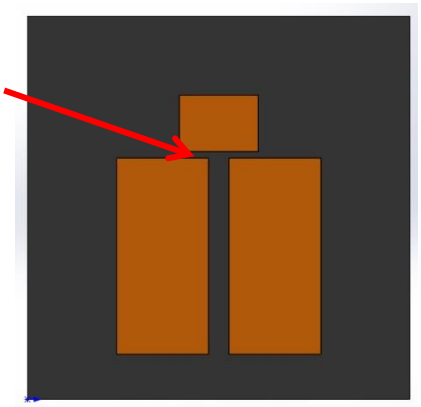

Figure 7.8 – SiC MOSFET model showing 70 µm gap between source and gate pads

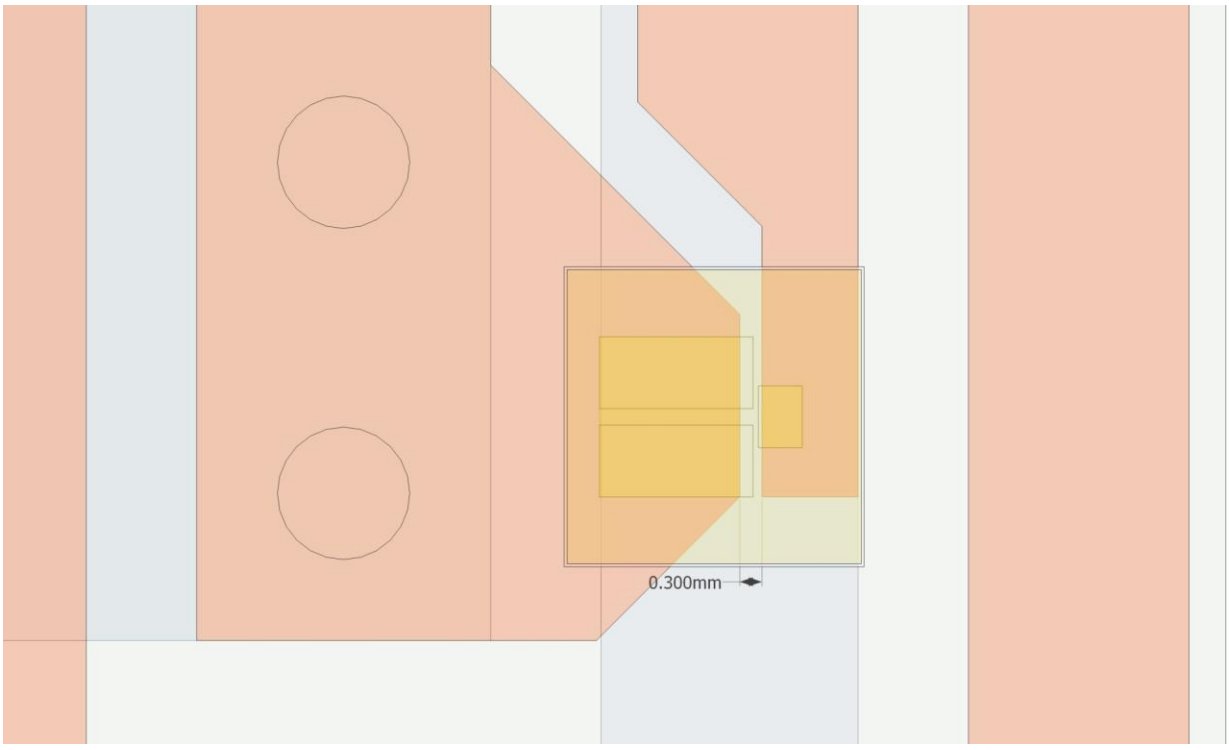

Figure 7.9 – Modeled gap width between source and gate pad upon the MOSFET devices overlaid upon the specialty copper metallization traces

7.3.2 TLP Material Deposition

In order to precisely define the location of materials for TLP die-attach on both the devices and substrates numerous deposition masks are necessary which isolate the materials to only where desired. These masks protect against metals short circuiting the gate and source on both the devices and substrates and also hold the substrates and masks in place while they are inside of the electron beam and sputtering systems. For both the devices and substrates there are two types of masks, one to horizontally restrain the components, as seen in Figure 7.10, and another to vertically restrain them while also having precise cutouts to define the material deposition locations, shown in Figure 7.11. The masks align in sets and are designed to fit with preexisting planetary holders of common deposition systems.

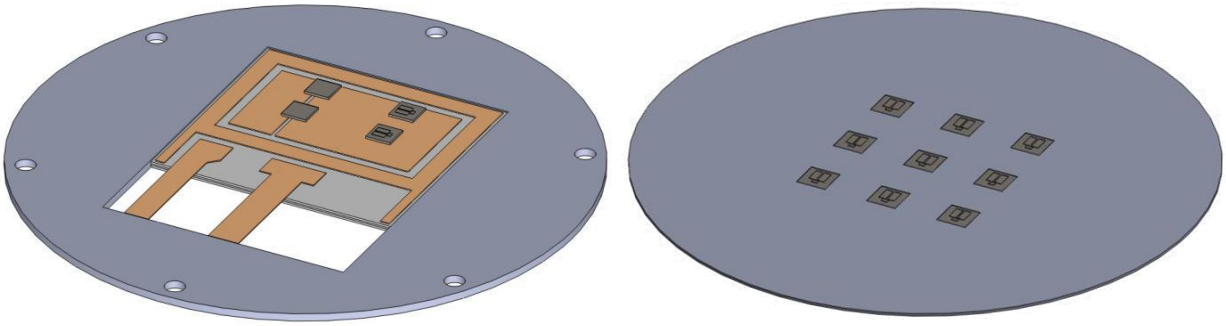

Figure 7.10 – Deposition masks for holding MOSFET devices and substrates within deposition systems

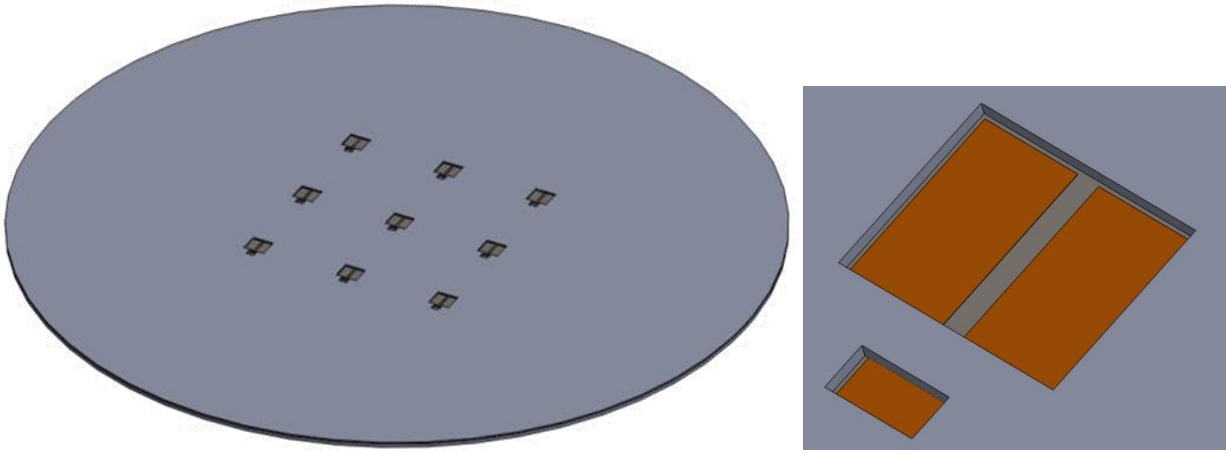

Figure 7.11 – Deposition masks allowing for deposition of material only on MOSFET gate and source pads without short circuiting passivation areas.

7.3.3 Module Assembly

A final step in fabricating the TLP module and accounting for the fine device dimensions involved is the assembly of the module which requires precise placement and alignments of all four devices and substrates during TLP reflow. This process requires the either the use of an assembly jig and alignment system or a die bonder which picks and places devices onto substrates for bonding. To allow for use of an inert oven for reflow an assembly jig has been designed as seen in Figure 7.12. The holder jig itself principally constrains the substrates and aligns with additional alignment mask which position the MOSFET devices on the bottom substrate set to align with the previously deposited TLP materials. These masks are constructed in graphite due to its low emissivity and specific heat capacity.

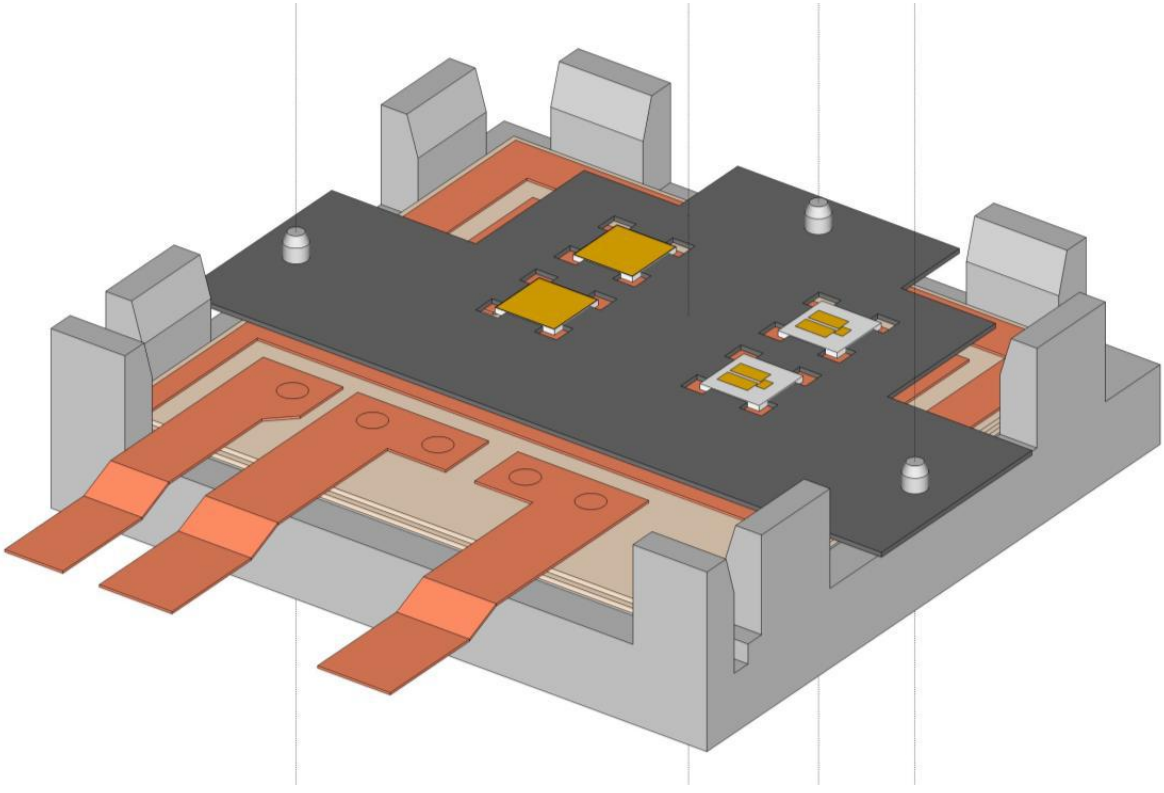

Figure 7.12 – Assembly jig designed to constrain module components during fabrication and align TLP bonds and device terminal pads.

7.4 Module Design Summary

A TLP power electronic module has been designed to achieve optimal performance in a space-based environment by utilizing TLP die-attach and also incorporating other advantageous design features to achieve its wide temperature range goals. Several aspects of its difficult fabrication have been contemplated and solutions were discussed such as fine feature sizes, specifying TLP material deposition locations, and precise assemble alignment. The module has been thermally and mechanically simulated to assess its durability in the extremes of its intended environmental conditions and appears viable still. However, it is necessary for others to fabricate the designed TLP module to observe its reliability and operational viability in its intended extreme conditions.

CHAPTER 8: CONCLUSION AND FUTURE WORK

8.1 Summary and Conclusion

In summary, a lack of high-temperature packaging is becoming a bottleneck to wide-bandgap power device capabilities, SiC in particular. Prior art in the field does not satisfy the requirements of current high-temperature application needs such as in energy and transportation and this problem will only become a larger with the ongoing expansion of these key technology applications in conjunction with an explosion of SiC devices. TLP die-attach is one of the most promising techniques to alleviate this restriction by featuring packaging capabilities exceeding 450 °C with high reliability, low thermal resistance due to its micrometer scale thickness, high thermal conductivity, lead-free capability, high mechanical strength, low mechanical stresses, and a simple, fast bonding procedure with no organic binders to remove.

In this dissertation, comprehensive mechanical characterization was performed in which key TLP die-attach design parameters were analyzed for their effect on pertinent bond properties, advancing TLP understand past the constant proof-of-concept works which dominate the current research field. Important relationships between parameters (bonding pressure, interlayer thickness, and atomic fraction of interlayer) and bond properties (die-attach area, thermal impedance, and shear strength) were observed for the first time.

Unique reliability and degradation research was also performed for the first time which associated electrical resistivity measurement of thin film structures, like TLP, to instant detection of detrimental material diffusion within the material layers. This was used to learn that properly designed TLP structures are incredibly durable, as confirmed though traditional material detection metrology. It was also learned what design requirements produce electrically and

diffusively reliable bonds. Furthermore, the thermal conductivity of TLP die-attach was investigated for the first time, which also showed promising results, indicating a thermally durable and reliable die-attach technique in extreme temperature ranges.

Finally, this TLP characterization and reliability information was used to inform the design of a new high-temperature power electronic module featuring TLP die-attach which also features SiC devices, double-sided cooling capability, small form factor, low voltage, high reliability, high thermal conductivity, and a wirebond-less design to best capitalize on the advantages of TLP die-attach and SiC devices. This power module has been fully designed and simulated both thermally and mechanically to investigate its viability in extreme temperature environments in terms of CTE stress acting on it, for which it appears totally capable.

8.2 Future Work

Future work is available for additional TLP die-attach research. This present work focused on gold-indium TLP for reasons explained previously and consistency among electrical, mechanical, thermal, and diffusive research performed. This reliability investigation, mechanical characterization, and module design could also be continued with additional TLP material systems such as the now popular copper-sin or silver-tin, copper-indium, or others. Those results would confirm or negates the conclusions reached here and also gain new understanding of the interaction of those base and interlayer materials.

Additional material science research is needed on the resultant TLP compounds created by TLP both in this work and in additional material pairs, material phases such as $AuIn_2$, Au_9In_4, CuIn, etc. are not fully characterized for their coefficient of thermal expansion, thermal conductivity and specific heat capacity, ductility, and stress-strain curve information which are

all necessary to fully utilize TLP die-attach commercially in the future. Also, long term TLP die-attach degradation monitoring is need to completely understand its reliability which has been heavy suggested by the durability information gained by this work. Finally, the TLP power module designed and simulated here can be brought to fruition by fabricating multiple copies of it and investigating its operating characteristics and reliability.

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