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RF Circuit Designs for Reliability and Process Variability Resilience

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RF CIRCUIT DESIGNS FOR RELIABILITY AND PROCESS VARIABILITY RESILIENCE

by

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ABSTRACT

CMOS devices are scaled down and beyond pose significant process variability and reliability issues. Negative biased temperature instability (NBTI) and hot carrier injection (HCI) are well-known aging phenomena that degrade transistor and circuit performance. Yield analysis and optimization, which takes into account the manufacturing tolerances, model uncertainties, variations in the process parameters, and aging factors are known as indispensable components of the circuit design procedure. Process variability issues become more predominant as the feature size decreases. With these insights provided, reliability and variability evaluations on typical RF circuits and possible compensation techniques are highly desirable.

In this work, a class F power amplifier was designed and evaluated using TSMC 0.18 μm RF technology. The PA's output power and power-added efficiency were evaluated using the ADS simulation. Physical insight of transistor operation in the RF circuit environment was examined using the Sentaurus mixed-mode device and circuit simulation. The hot electron effect and device self-heating degraded the output power and power-added efficiency of the power amplifier, especially when both the input transistor and output transistor suffered high impact ionization rates and lattice heating.

RF power amplifier adaptive body bias compensation technique was used for output power and power-added efficiency resilient to process, supply voltage, and temperature variations. The adaptive body biasing scheme used a current source for PVT sensing to provide resilience through the threshold voltage adjustment to maintain power amplifier performance over a wide range of variability. The resilient

body biasing design improved the robustness of the power amplifier in output power and power-added efficiency over process, supply voltage, and temperature variations.

Process variation and aging effect were studied on a RF mixer. The mixer compensation using a process invariant current source was evaluated. Mixer parameters such as conversion gain, noise figure, and output power before and after compensation over a wide range of variability were examined. Analytical equations were derived for physical insight. ADS and Monte-Carlo simulation results showed that the use of invariant current source improved the robustness of the mixer performance against process variations and device aging.

Finally, Semiconductor process variation and reliability aging effect on CMOS VCO performance was studied. A technique to mitigate the effect of process variations on the performances of nano-scale CMOS LC-VCO was presented. The LC-VCO compensation used a process invariant current source. VCO parameters such as phase noise and core power before and after compensation over a wide range of variability were examined. ADS and Monte-Carlo simulation results showed that the use of invariant current source improved the robustness of the VCO performance against process variations and device aging.

To my family.

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LIST OF ACRONYMS AND ABBREVIATIONS

ADS	Advanced Design System
ASIC	Application Specific Integrated Circuits
BD	Breakdown
BTI	Bias Temperature Instability
CDMA	Code Division Multiple Access
CHE	Channel Hot Electron
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
FET	Field Effect Transistor
HC	Hot Carrier
HCI	Hot Carrier Injection
HCD	Hot Carrier Degradation
HF	High Frequency
IC	Integrated Circuit
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LNA	Low Noise Amplifier
MC	Monte Carlo
MOS	Metal Oxide Semiconductor

MOSFET	MOS Field Effect Transistor
NBTI	Negative Bias Temperature Instability
NF	Noise Figure or Noise Factor
NMOSFET	N-type MOS Field Effect Transistor
OPAMP	Operation Amplifier
PA	Power Amplifier
PAE	Power Added Efficiency
PBTI	Positive Bias Temperature Instability
PMOSFET	P-type MOS Field Effect Transistor
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
SBD	Soft Breakdown
SH	Self-Heating
SNR	Signal-to-Noise Ratio
SOC	System on Chip
SOI	Silicon-on- Insulator
STD	Standard Deviation
TDDB	Time Dependent Dielectric Breakdown
μ_n	Mobility of N-Type MOS Field Effect Transistor
VLSI	Very-Large-Scale Integration
V_{DD}	DC Supply Voltage
V_T	Threshold Voltage

CHAPTER ONE: INTRODUCTION

1.1 Motivation

Advances in process technologies and circuit design techniques, along with sophisticated RF design kits, have made CMOS technology the platform of choice for wireless designs. With the rapid growth of IC industry, CMOS RFICs are widely used in wireless communication systems, like mobile phone and TV, Bluetooth, WLAN, wireless sensing system, etc. Using RF CMOS to fabricate highly integrated single-chip solutions enables products that are smaller, more affordable, more power efficient and have a longer range than previously possible. Due to aggressive scaling in device dimensions for improving speed and functionality, CMOS transistors in the deep sub-micrometer to nanometer regime has resulted in major reliability issues including gate oxide breakdown and channel hot electron degradation, NBTI, and variability.

Most of RF circuits are vulnerable to the reliability issues. They suffer from different reliability problems since they have different operation schemes and different structures. It is very urgent to study why they are suffer from the reliability and variability issues. Nowadays, there have not been any universal rules developed on the relationship between RF circuits and susceptible reliability issues yet. Each RF circuits should be studied individually according to its unique features.

Power amplifier, mixers and oscillator are essential parts in RF transceivers. Power amplifier is the last one before antenna in a transmitter and serves to amplifier the power to be transmitted. Mixers are used to yield both, a sum and a difference frequency at a single output port when two distinct input frequencies are inserted into the other two ports. Oscillators are used to provide signal

sources for frequency conversion and carrier generation. It is of great significance to keep them working stably over variations of temperature, process, voltage supply, and other stress and degradation conditions.

1.2 Goal of research

This work is mainly focused on solving issues listed below:

1. Principle and theoretical study of typical reliability issues and verification by device and circuit level simulations.
2. Circuit design and chip implementation of RF PA, mixer, oscillator circuits.
3. Reliability analysis based on experimental results on class F PA.
4. Propose and compare possible compensation circuits, such as adaptive body biasing circuits, a process invariant current source, etc.
5. Monte-Carlo simulation to demonstrate variability issues and compensation effects of adaptive body biasing circuit.

1.3 Results outline

To summarize, chapter two gives an overview of current reliability and variability issues remained in RF circuits design. The author evaluated hot electron and oxide stress effects on Class F PA by experiments, details are shown in chapter three. Adaptive body biasing technique to minimize PVT variations of RF class AB power amplifier is evaluated, verified with analytical equations, this is described in chapter four. Chapter five examined Process variations and reliability on mixer using a process invariant current source, and supported by analytical equations. A robust, adaptive design technique to reduce PVT variation effects on RF oscillator circuits is developed in chapter six. Chapter seven is the final conclusion and future work.

CHAPTER TWO: RF CIRCUITS AND RELIABILITY ISSUES OVERVIEW

2.1 Oxide Breakdown

Oxide Breakdown [1] is defined as the destruction of the oxide layer (usually silicon dioxide or SiO2) in a semiconductor device. Oxide layers are used in many parts of the semiconductor device: such as the dielectric layer in capacitors; the gate oxide between the metal and the semiconductor in MOS transistors; the inter-layer dielectric to isolate conductors from each other, etc. Oxide breakdown is also considered as ‘oxide rupture’ or ’oxide punch-through’.

In the modern world with the dimensions reductions of the transistor, one of the reliability issues called Oxide breakdown has been concerned by the industry. While the other features of the device are scaled down, the oxide thickness must be reduced. Oxides become more vulnerable to the gate to source and drain to source voltages when they get thinner. Right now the thinnest oxide layers in the world are already less than 30 angstroms thick. An oxide layer can break down easily at once at 8-11 MV per cm of thickness.

There are several classifications of the oxide breakdown base on different kinds of definition.

The first type is Early-life dielectric breakdown. Early-life dielectric breakdown refers to the breakdown happens in the early device life, such as within the first 1-2 years of the normal operation. Early life dielectric breakdown is mainly because of the presence of weak spots within the dielectric layer arising from its poor processing or uneven growth. These weak spots or dielectric defects could be caused by: 1) radiation damage; 2) contamination, wherein particles or impurities are trapped on the silicon prior to oxidation; 3) the presence of mobile sodium (Na) ions in the oxide; and 4) crystalline defects

The second type is Time-dependent dielectric breakdown (TDDB). Time-dependent dielectric breakdown refers to the breakdown happens after a longer use of time, such as 6-10 years, usually considers as the “wear-out stage”. However the mechanism is the same as the early-life breakdown.

The last type is EOS/ESD-induced dielectric breakdown. The third classification is self-explanatory, which is merely to gate oxide destruction due to the application of excessive voltage or current to the device.

Gate oxide breakdown could also divide into soft breakdown and hard breakdown. When breakdown just happens, it could be considered as the soft breakdown, and when breakdown happens in a long time it could be considered as hard breakdown. Usually soft breakdown does not degrade the device performance a lot, but hard breakdown could usually damage the device. As Figure 1 shows, in (a) first the traps start to form in the gate oxide, but they do not overlap and conduct; in (b) as more and more traps are created, then the traps start to overlap and conduction path is created, as soon as the conduction path is created, the soft breakdown happens. After soft breakdown happens, in (c), the traps are overlapping, at this time thermal damage was happen. Because conduction leads to heat, and heat leads to thermal damage. And finally in (d), hard breakdown happens, because the silicon in the breakdown spots melts and oxygen is released.

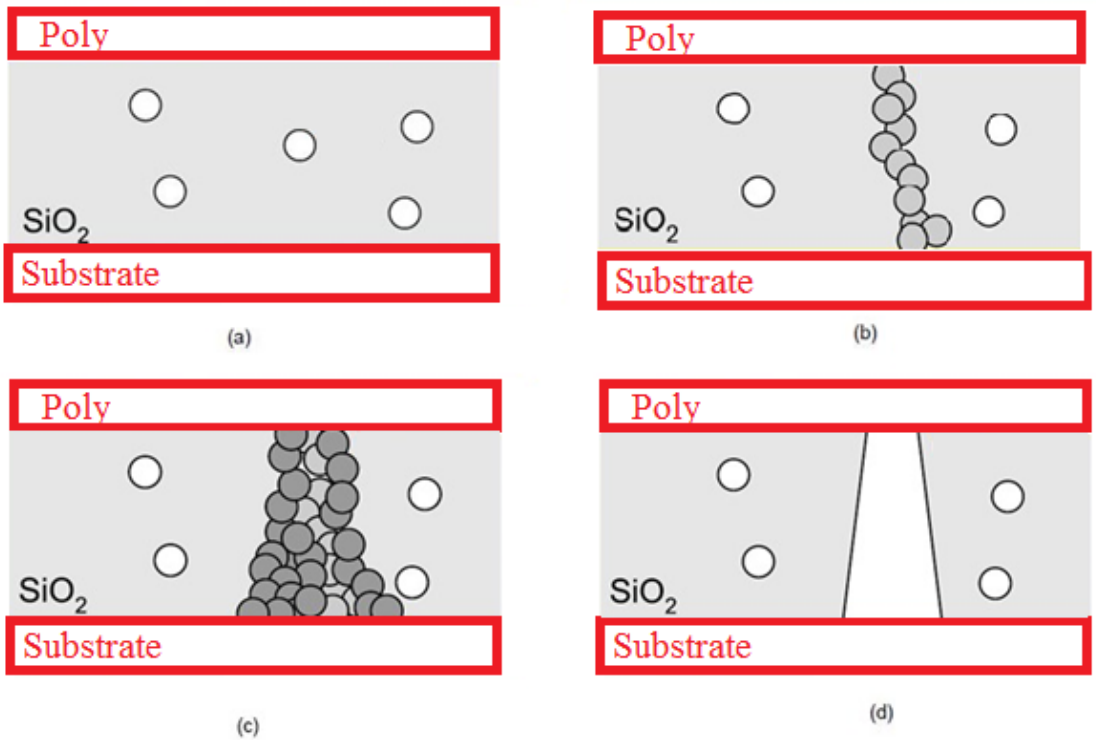


Figure 1 Traps in the gate oxide when soft hard and hard breakdown happen

Figure 2 is a picture of after-breakdown from Emission Microscopy (EMMI).[2] Light regions are the areas of gate oxide breakdown where the Silicon has melted. After a hard breakdown, usually silicon in the breakdown spots melts, oxygen is released, and silicon filament is formed from gate to substrate. Typically, not only the gate oxide is ruptured after hard breakdown, but also the Si substrate channel is severely damaged by gate oxide BD-induced thermal effect. In some cases, a direct short in the channel between source and drain is observed from TEM in HBD MOSFETs.

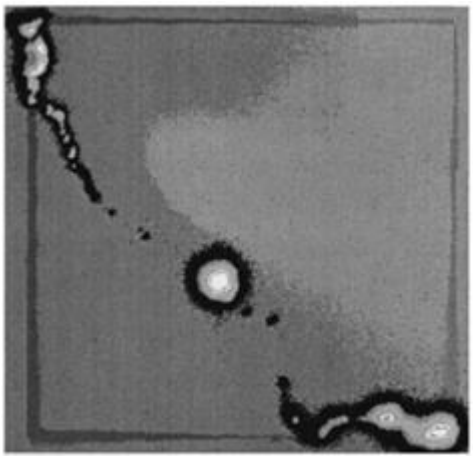


Figure 2 EMMI image of the gate after breakdown.

2.2 Hot Carrier Effect

Hot carrier effect is one of the most significant reliability problems of advanced MOSFETs devices. Hot carrier refers to either holes or electrons that have gained very high kinetic energy after being accelerated by a strong electric field in areas of high field intensities within a semiconductor device. Hot carrier usually injects into the gate oxide or substrate layers because of the high electrical field. A path of traps and charges will be created which will degrade the semiconductor device performance. Hot carries effects refers to device degradation or instability caused by hot carrier injection. There are four types of hot electron injection mechanisms. The first type is the channel hot electron injection. Channel hot electron injection happens when both the gate voltage and drain voltage are higher than the source voltage, with $V_D \approx V_G$. Due to the high gate voltage, channel carriers sometimes are driven to the gate oxide before they reach the drain side. The second type is the substrate hot electron injection. Substrate hot electron injection usually happens when the substrate bias is very high such as, $|V_B| >> 0$. Substrate field drives the carriers to the Si-SiO_2 interface under this condition. In the process the carriers gain a lot of kinetic energy from the high electrical field so that they could go into the surface depletion region. In the end, they overcome the surface energy barrier and inject into the gate oxide. The third type is the drain avalanche hot carrier injection.

The drain avalanche hot carrier (DAHC) injection is shown in Fig. 3. This is the worst device degradation under normal operating temperature. This happens when a high voltage applied at the drain at the condition of ($V_D > V_G$) the channel carriers will accelerate into the drain's depletion region. The results show that the worst effects happen when $V_D = 2V_G$. This acceleration of channel carriers creates dislodged electron-hole pairs. The phenomenon is known as impact ionization, some electron-hole pairs gain enough energy to overcome the electric potential barrier between the gate oxide and the silicon substrate. Then some of the electron and carriers inject into the gate oxide layer as well as the substrate layer where they are sometimes trapped. Hot carriers can be trapped at the Si-SiO_2 interface or within the oxide itself, creating a space charge which will increase over time as more charges are trapped. These trapped charges change some of the device characteristics, for example the threshold voltage (V_{th}) and mobility. Injected carriers will not become gate current in the gate oxide. Meanwhile, most of the holes from the electron-hole pairs generated by impact ionization flow back to the substrate, comprising a large portion of the substrate's current. The forth type is the secondary generated hot electron injection. Secondary generated hot electron injection involves the generation of hot carriers from impact ionization involving a secondary carrier which was created by an earlier incident of impact ionization. This happens when a high voltage applied at the drain side or $V_D > V_G$. The back bias results in a field which tends to drive the hot carriers generated by the secondary carries to the surface region and get enough kinetic energy to overcome the surface energy barrier.

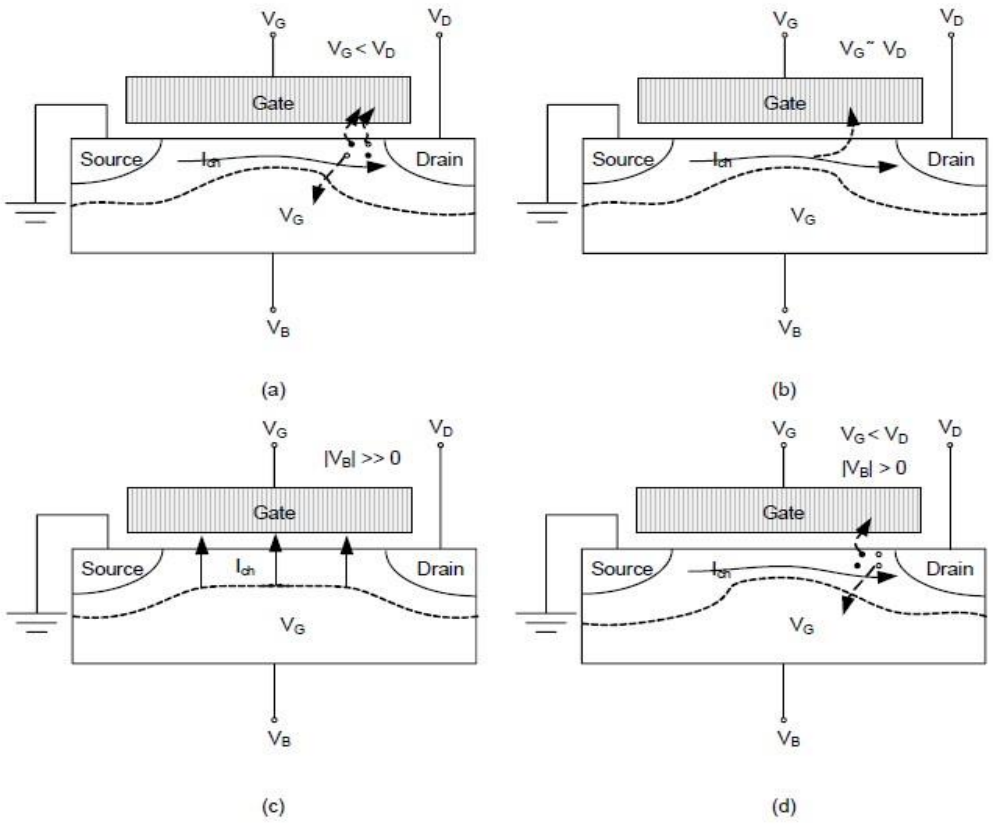


Figure 3 Mechanisms of Hot Carrier Effects

2.3 Variability Issues

As the characteristic dimensions of device becomes smaller and smaller, it becomes harder and harder to precisely control the physical dimensions and dopant levels during the fabrication process. As a result, these growing uncertainties lead to more and more statistic variations in circuit performance and behaviors from designed circuit. Traditionally, designers tend to think in a deterministic way, while with these variability issues become too big to ignore, designers got more problem to solve. As shown in Figure 4, initially, process variation has been treated mainly as die to die variation, that is the difference originated from different die environments, but devices from the same die share the same properties. With the device size shrinks, intra-die variations have become the main concern for design since it will cause local

mismatch even if chips are cut from the same die.

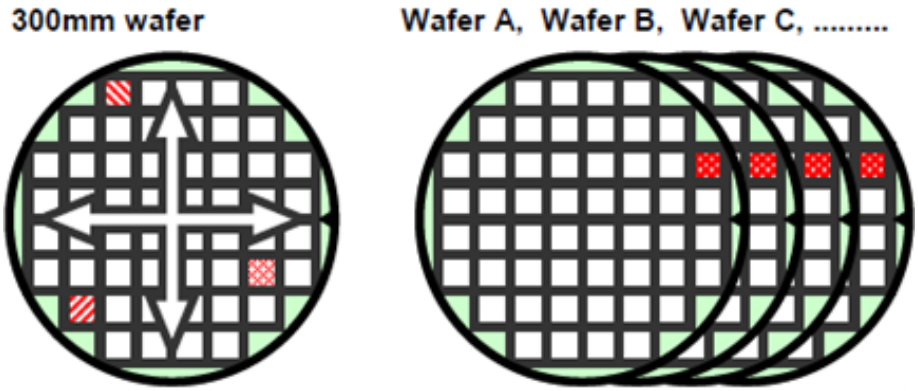


Figure 4 Variability issue inside and among dies.

The major sources of process variability include random dopant fluctuations (RDF), line-edge and line-width roughness (LER and LWR) and oxide thickness and interface roughness etc [3].

Random dopant fluctuations results from the random fluctuations in the number and location of the dopant atoms in the channel of a transistor and is a major source of process variability in advanced CMOS technology. As the number of dopant atoms in the channel decreases with scaled dimensions, the impact of the variation associated with the atoms increases. The major effect of random dopant fluctuations is introducing threshold voltage shift and mismatch. The impact of process variability due to dopant variation on threshold voltage mismatch derived from the overall number variation of the total depletion charge is given by [4]:

$$\delta V_T = \left(\frac{\sqrt[4]{4q^3\varepsilon_{si}\emptyset_B}}{2}\right)\left(\frac{\sqrt[4]{N_{CH}}}{\sqrt{W_{eff}L_{eff}}}\right)\left(\frac{T_{ox}}{\varepsilon_{ox}}\right) \quad (1)$$

where q is the electron charge, ε_{si}, ε_{ox} are the permittivity of the silicon and SiO_2, $\emptyset_B$ is the built-in potential of S/D-to-channel PN junction of MOFETs, N_{CH} is the channel doping concentration, L_{eff} is the effective channel length and W_{eff} is the effective channel width. The threshold voltage variation is inversely proportional to the square root of the active device area. As a result of scaling down technology, dopant variation is significantly increased in the process variability for scaled CMOS technology beyond 90-nm regime. As an example, it is estimated that the random dopant fluctuation

contributes over 60% to the threshold voltage mismatch in sub-90-nm MOSFETs [5].

The second major source of process variability is line-edge and line-width roughness that causes the critical dimension variation and is due to the tolerances inherent to materials and tools used in the lithography process. The edge roughness remains typically on the order of 5nm almost independent of the type of lithography used in production [6]. Line-edge and line-width roughness does not scale accordingly as the technology scaling, becoming an increasingly larger fraction of the gate length. LER and LWR will result in the increases in the subthreshold current [7] and the degradation in the threshold voltage (V_T) characteristics [8]. The variation effect due to LER and RDF are statistically independent and can be modeled independently [9]. The scaling of the MOSFETs to deep submicrometer involves aggressive reduction in the gate oxide thickness. When the oxide thickness is equivalent to only a few silicon atomic layers, the atomic scale interface roughness steps between Si-SiO_2 and SiO_2-polysilicon gate will result in significant oxide thickness variation (OTV) within the gate region. Asenov et al. [10] show that intrinsic threshold voltage fluctuations induced by local oxide thickness variations become comparable to voltage fluctuations introduced by RDF for conventional MOS devices with dimensions of 30nm and below. A V_{TH} fluctuation of about 30 mV is produced due to gate oxide thickness fluctuation by interface roughness for an MOSFET with L=W=30nm.

CHAPTER THREE: EVALUATION OF ELECTRICAL STRESS EFFECT ON CLASS F PA

3.1 RF Power Amplifiers Fundamentals

Power amplifiers can be categorized into different types (A, AB, B, C, D, E, F) distinguished primarily by bias conditions and conduction angle. For the four classic classes A. AB, B and C, the input signal overdrive is relatively small and the device is operated more as a current source. Class A, AB, B, and C may be studied with a single model as in Figure 5.

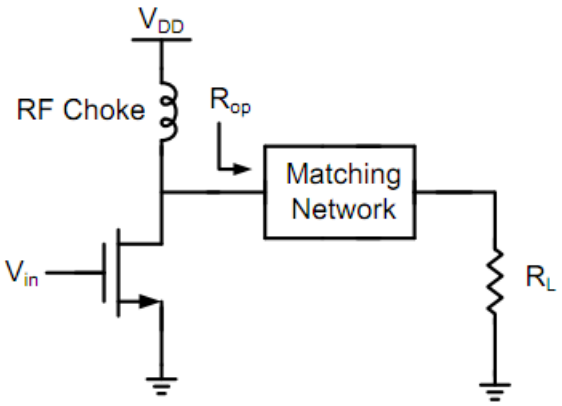


Figure 5 General power amplifier model

In this general model, the resistor RL represents the load. The RF choke feeds DC power to the drain. The RF choke is assumed large enough so that the current through it is substantially constant. The matching network formed with LC tank is used to optimize gain. The drain voltage of the output transistor swings between ground and 2VDD depending on the input power level.

The current and voltage waveforms of class A, AB, B and C power amplifiers are shown in Fig. 3.5. Class A power amplifier is operated in full input and output range which provides good linearity at the cost of low efficiency. For class AB, B and C, the gate bias voltage is decreased 20 to reduce the conduction angle for higher efficiency as illustrated in Figure 6. The maximum efficiency for class A is 50%. With a smaller conduction angle, the power efficiency of class AB can reach up to 78.5%. For class C, as the conduction angle shrinks to zero, the efficiency can reach 100%

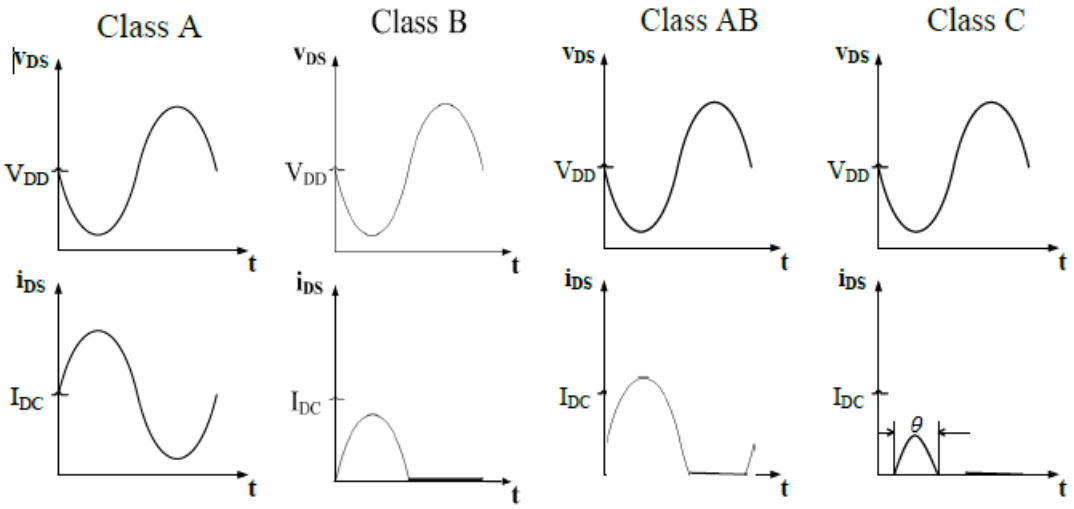


Figure 6 Current and voltage waveforms of class A, AB, B and C power amplifiers.

For class D, E and F power amplifiers, the transistor is used as a switch. The current and voltage waveforms for class D, E and F power amplifiers are shown in Figure 7. Since there is either zero voltage across it or zero current across it, the transistor dissipates no power and the theoretical efficiency is 100%.

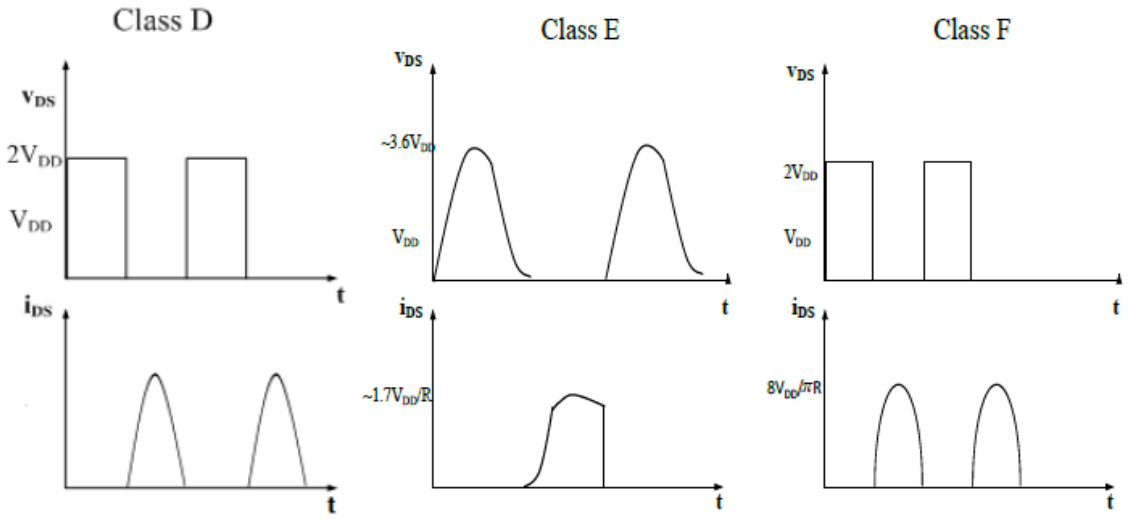


Figure 7 Current and voltage waveforms of class D, E and F power amplifiers.

3.2 Class E PA Reliability Issues

The advance in CMOS technology for high frequency applications has made it a natural choice for integrated, low cost RF power amplifiers (PAs) for wireless communications ICs. Depending on its applications, the power transistor can be used as a current source (class A, B, and C mode) or a switch (class D, E, and F mode). Switching-type amplifiers achieve high power efficiency [11] and are desirable for portable communication systems such as cell phones, global position systems, and wireless local area networks. The tradeoff between linearity and efficiency in power amplifiers has been investigated extensively. To linearly amplify the modulated signals, the PAs typically operate in a back-off power region at the expense of efficiency. However, polar modulation transmitter architecture [12], where a phase modulated signal with constant envelope is amplified by a non-linear (switching type) PA, has the potential to enhance the efficiency while achieving high linearity.

Due to aggressive scaling in device dimensions for improving speed and functionality, CMOS transistors in the nanometer regime continue to endure major reliability issues such as channel hot electron degradation [13] and gate oxide breakdown [14]. In the past 10 years, numerous papers on the stress effect on digital and RF circuits have been published [15-18]. For example, the gate oxide stress decreases the static noise margin of 6-transistor SRAM cells [15]. Hot electron increases the noise figure of the low-noise amplifier [19], and the phase noise of the voltage-controlled oscillator [20].

In this work, a class F power amplifier is designed. Its RF performances before and after layout are analyzed. The design of the class F power amplifier, the Cadence layout and post layout simulation results are presented. The physical insight of the device behavior in the class F PA operation environment is illustrated.

3.3 Design of Class F PA

The Class F RF power amplifiers utilize multiple harmonic resonators in the output network to shape the drain-source voltage. The drain current flows when the drain-source voltage is low, and the drain-source voltage is high where the drain current is zero. This reduces the transistor switching loss and increases the drain efficiency of the class F PA. In class F amplifiers with odd harmonics, the drain-source voltage contains only odd harmonics and the drain current contains only even harmonics. Thus, the input impedance of the load network represents an open circuit at odd harmonics and a short circuit at even harmonics. The V_{DS} of class F PA with odd harmonics can be written as

$$V_{DS} = V_{DD} - V_m \cos(\omega_0 t) + \sum_{n=3,5,7,\ldots}^{\infty} V_{mn} \cos(n\omega_0 t) \quad (2)$$

were V_{DD} is the supply voltage, V_m is the fundamental component of drain voltage, V_{mn} is the amplitude of n-th harmonic of V_{DS}, and ω_0 is the angular frequency at the operating point.

The drain current i_D is given by

$$i_{DS} = I_{DD} + I_m \cos(\omega_0 t) + \sum_{n=2,4,6,\ldots}^{\infty} I_{mn} \cos(n\omega_0 t) \quad (3)$$

where I_{DD} is the DC current from V_{DD}, I_m is the fundamental component of drain current, I_{mn} is the amplitude of n-th harmonic of i_{DS}. No real power is generated at harmonics because there is either no current or no voltage present at each harmonic frequency. In class F amplifiers with even harmonics, on the other hand, the drain-source voltage contains only even harmonics and the drain current contains only odd harmonics.

In this work, the PA is designed with third hamonic peaking. The detail of class F PA design can be referred in [11]. The load network consists of a parallel LC resonant circuit tuned to the operating frequency f_0 and a parallel resonant circuit tuned to the third harmonic $3f_0$. The two resonant circuits

are connected in series. The ac power is delivered to the load resistor. Figure 8 shows the schematic view of the PA with a class-F output stage. The output of the input stage transistor is connected to the gate of the output stage transistor by a coupling capacitor C_1. The circuit is tuned and simulated using ADS software [21].

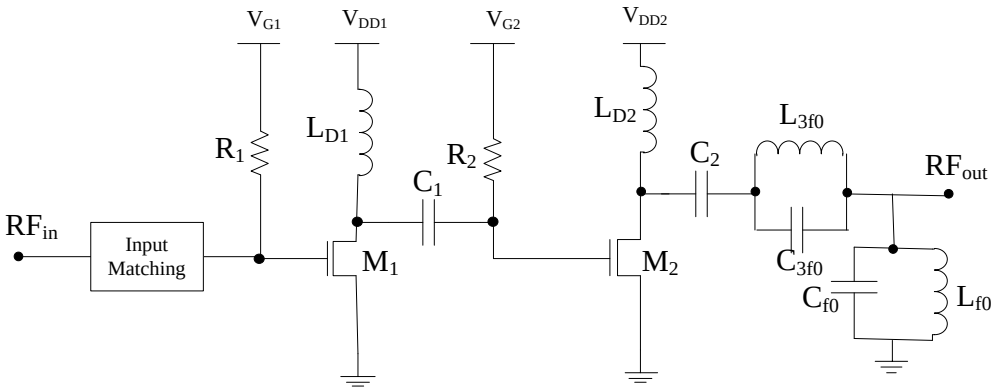


Figure 8 Schematic of class F power amplifier.

The class F power amplifier has been laid out using Cadence Virtuoso software, followed by Calibre DRC for design rule checking and LVS for layout versus schematic verification. A silicon chip layout of 726×950 μm^2 is displayed in Figure 9. In this figure spiral inductors, capacitors, transistors, GSG RF input and output pads, biasing and supply voltage DC pads are shown. The layout (interconnection) parasitic effects are extracted using ADS Momentum EM simulation to generate s-parameters. These s-parameters implicitly account for interconnect resistive, capacitive, and inductive behaviors. The extracted interconnect parasitic effects (s-parameter boxes) are then added to the original ADS circuit simulation for post-layout simulation. The post-layout simulation results are shown in Figure 10 and 11. The layout parasitic effect decreases the output power and power-added efficiency of the amplifier, as expected. Parasitic resistance introduces additional power loss in the circuit which reduces the power efficiency. Layout interconnections are very important for CMOS RFIC parasitic effects [22]. To reduce layout parasitic effects, we adjust inductors, capacitors, and transistors location and orientation in our design.

The simulated output current and voltage versus time, output power and power-added efficiency versus input power are as shown in Figure 10 and 11, respectively. In Figure 8 the line with triangles represents the pre-layout simulation results and the line with squares represents the post-layout simulation results. As seen in Figure 8 the output power increases with input power and reaches saturated output power at about 17.5 dBm. The post layout parasitics decrease the output power at a given input power. The power-added efficiency (≡ (RF output power - RF input power)/total DC power dissipation) increases with input power, reaches its peak value, and then decreases with input power. The power-added efficiency starts to decrease after reaching its peak because of the gain reaching a compression point, resulting in the output power no longer increasing. The maximum power-added efficiency approaches 32%, drops to 29.5% after post-layout simulation. Note that the power-added efficiency is lower than the drain efficiency because of additional power dissipation in the input stage.

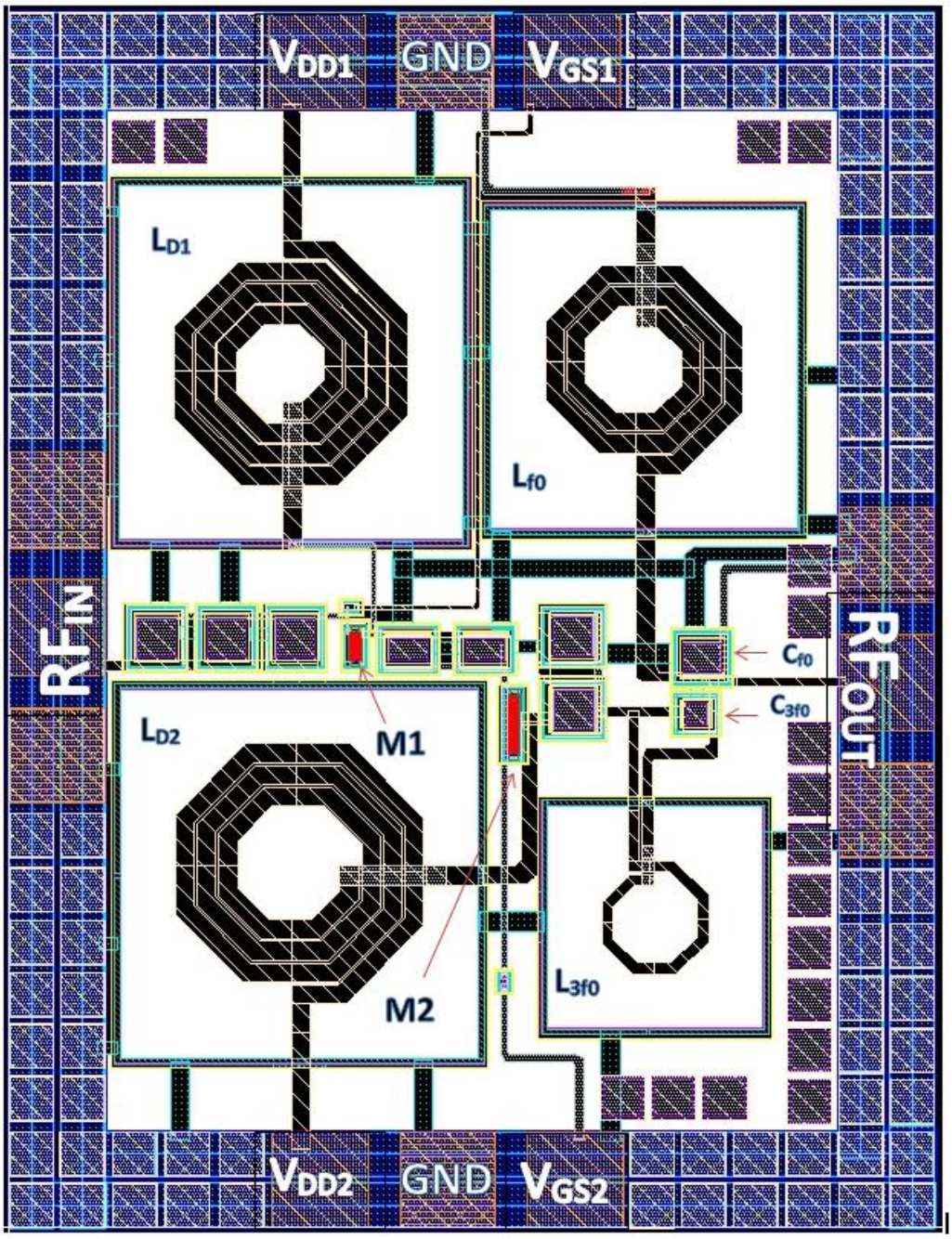
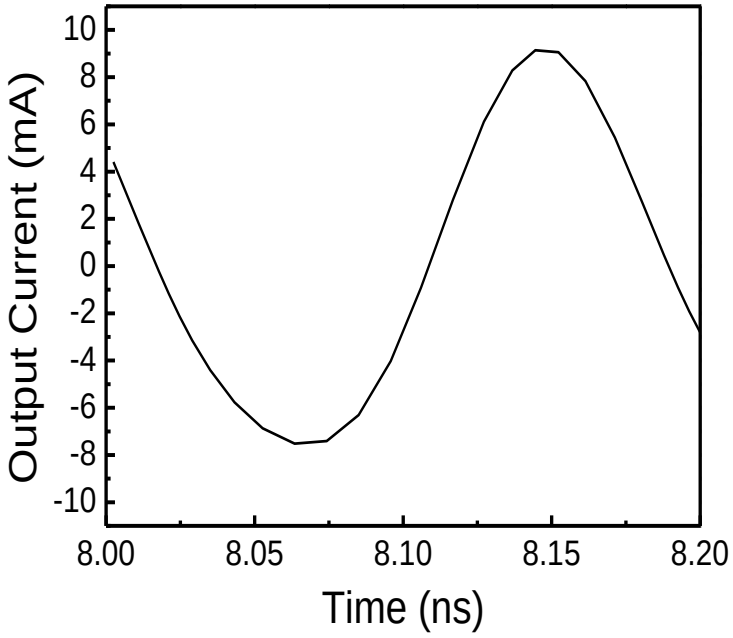
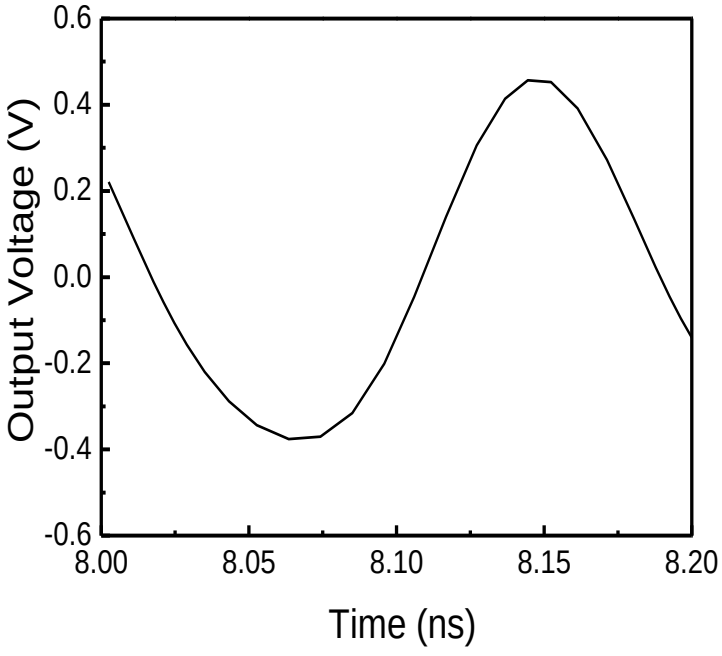


Figure 9 Layout view of the class F power amplifier.

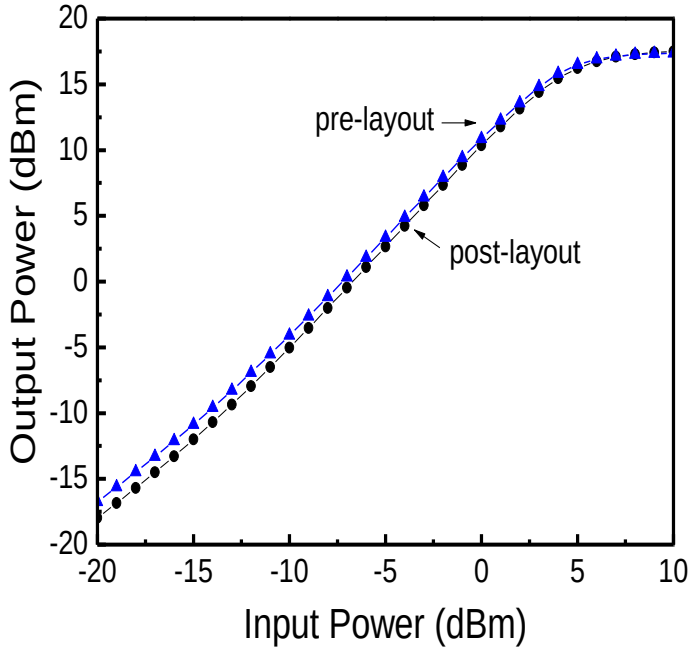


(a)

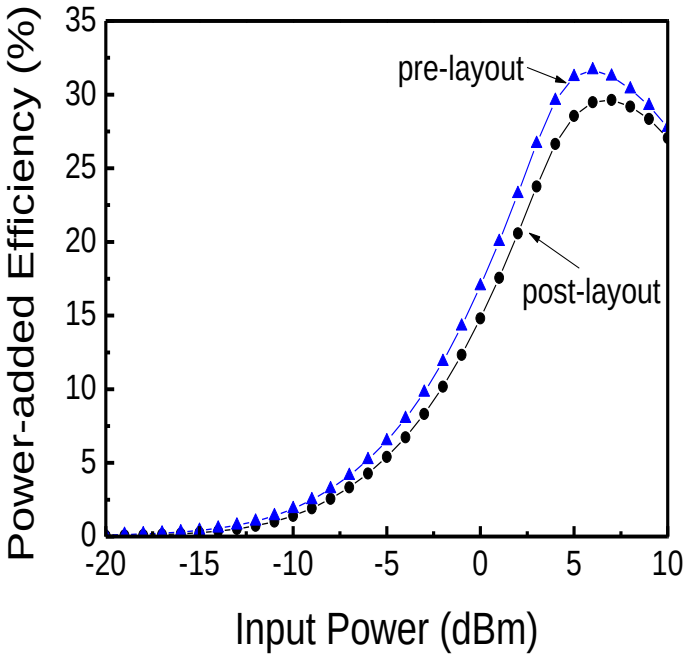


(b)

Figure 10 (a) Output current versus time (b) Output voltage versus time.



(a)



(b)

Figure 11 (a) Output power and power gain versus input power. (b) Power-added efficiency versus input power.

3.4 Mixed Mode Simulation

To evaluate the physical insight of hot electron effect in RF operation, the mixed-mode simulation of Sentaurus TCAD software is used [23]. The mixed-mode device and circuit simualation allows one to evaluate the device physical insight under the real circuit opreation condition. In Sentaurus simulation, physical equations such as Poisson's and continuity equations for drift-diffusion transport are implemented. The Shockley-Read-Hall carrier recombination, Auger recombination, and impact ionization models are also used. The impact ionization van Overstraetende Man model [24] assumes the impact ionization coefficient to be a function of the local field. To account for lattice heating, Thermodynamic, Thermode, RecGenHeat, and AnalyticTEP models in Sentaurus are used. The thermodynamic model extends the drift-diffusion approach to account for electrothermal effects. A Thermode is a boundary where the Dirichlet boundary condition is set for the lattice. RecGenHeat includes generation-recombination heat sources. AnalyticTEP gives analytical expression for thermoelectric power. The ambinet temperature is at 300 K. Figure 12 and 13 show the gate-source voltage and drain-source voltage of the input transistor M1 and the output transistor M2 from Sentaurus simulation. It is clear from Figure 12 and 13 that the output transistor has much larger V_{GS} and V_{DS} swings than those of the input transistor. When the gate-source voltage is above the threshold voltage and the drain-source voltage is very high, the transistor is under high electric field stress. Sufficient high field may trigger device avalanche and hot carrier injection.

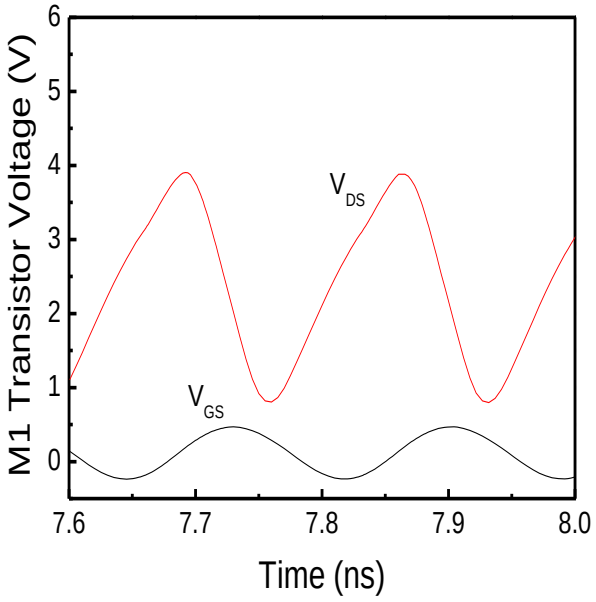


Figure 12 Drain-source and gate-source voltage of the input transistor M1.

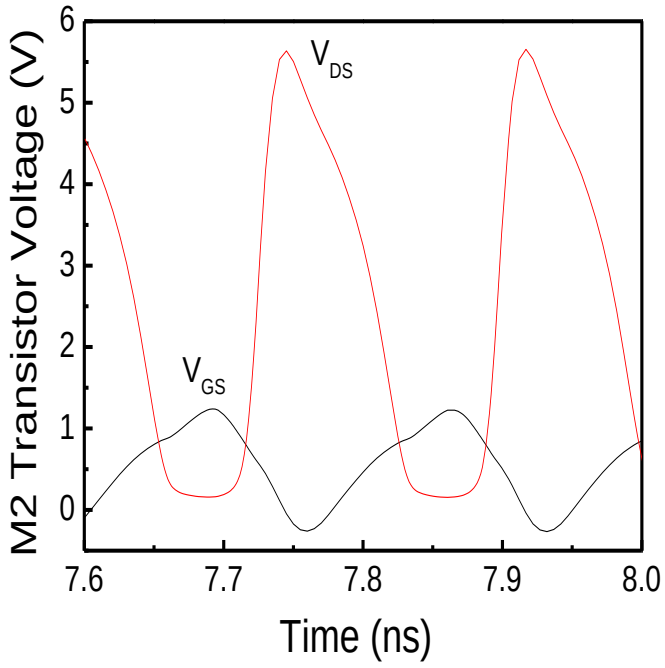


Figure 13 Drain-source and gate-source voltage of the output transistor M2.

Figure 14 shows impact ionization rates for the input and output transistor transistors of the PA at high V_{DS}. The supply voltage in Sentarus simulation is set at V_{DD} = 3.3 V. As seen in Figure 14 the

I.I. rates at the peak of output voltage waveform from M2 (left plot) are much higher than those in M1 (right plot). High impact ionization rates (2×10^{30} /cm^3/s) at the drain of M2 transistor suggest large hot electron injection into the gate of the M2 near the drain edge. Hot electron effects result in the MOS transistor performance degradation [25]. Figure 15 shows the lattice temperature of M1 and M2. The maximum lattice temperature at the drain of M2 increases to about 320 K, while the lattice temperature of M1 is virtually the same from source to drain. The current density in M2 is higher than that in M1 due to larger gate-source voltage and drain-source voltage simultaneously (data not shown here). High curernt density and high drain voltage produce self-heating and high lattice temperature near the drain edge.

From the reliability point of view, the output stage transistor of the class F power amplifier is more vulnerable to channel hot electron effect and gate oxide stress. It is clear from Fig. 13 that the peak drain-gate voltage of the second stage transistor is above 5.6 V due to larger V_{DS} and V_{GS} which provides high voltage stress between the drain and gate oxide. For example, the electric field of a 4-nm oxide thickness at 5.6 V voltage stress can approach 14 MV/cm, a precursor for gate-drain oxide breakdown. Note that the drain stress voltage can further increase when the supply voltage V_{DD} increases.

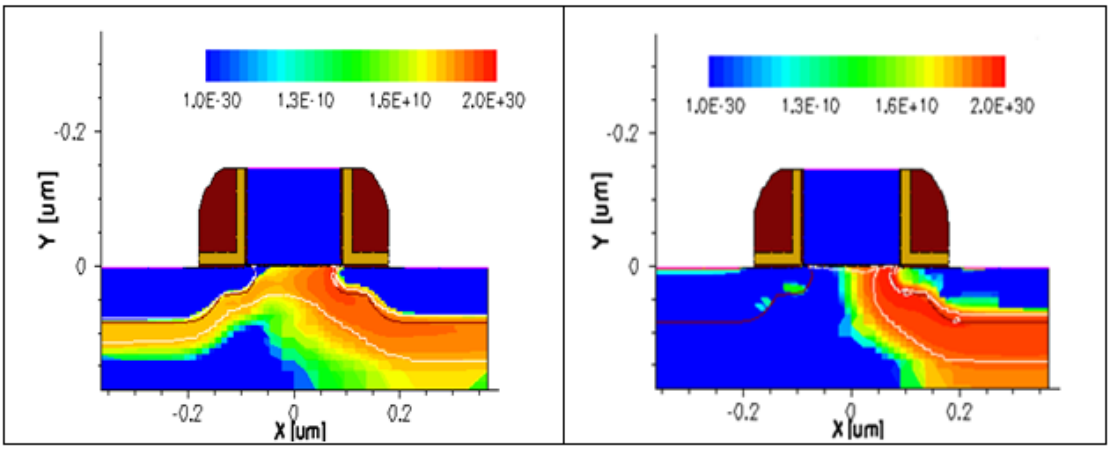


Figure 14 Impact ionization rates of the input stage (left plot) and output stage (right plot) transistors.

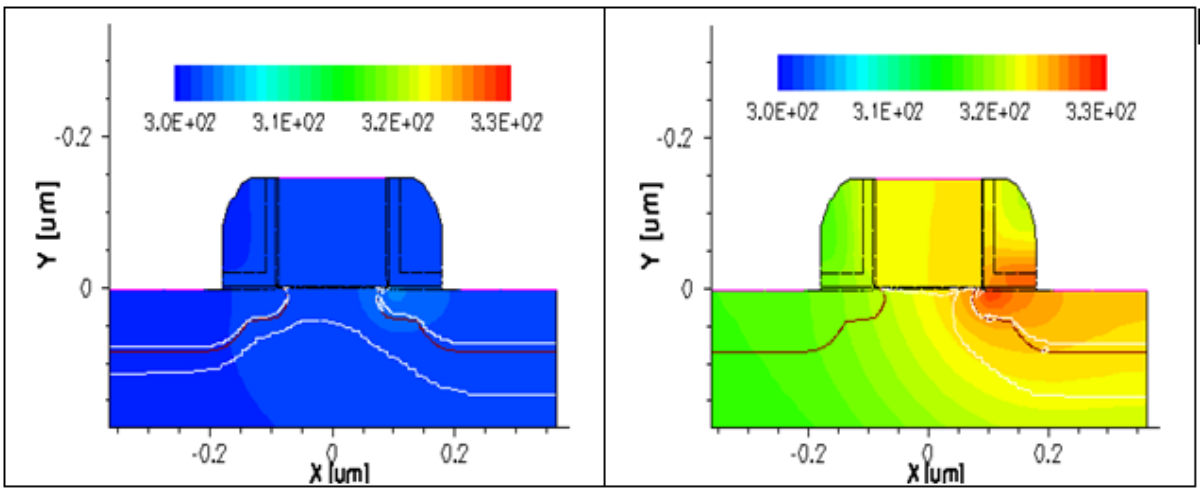


Figure 15 Lattice temperature of the input stage (left plot) and output stage (right plot) transistors.

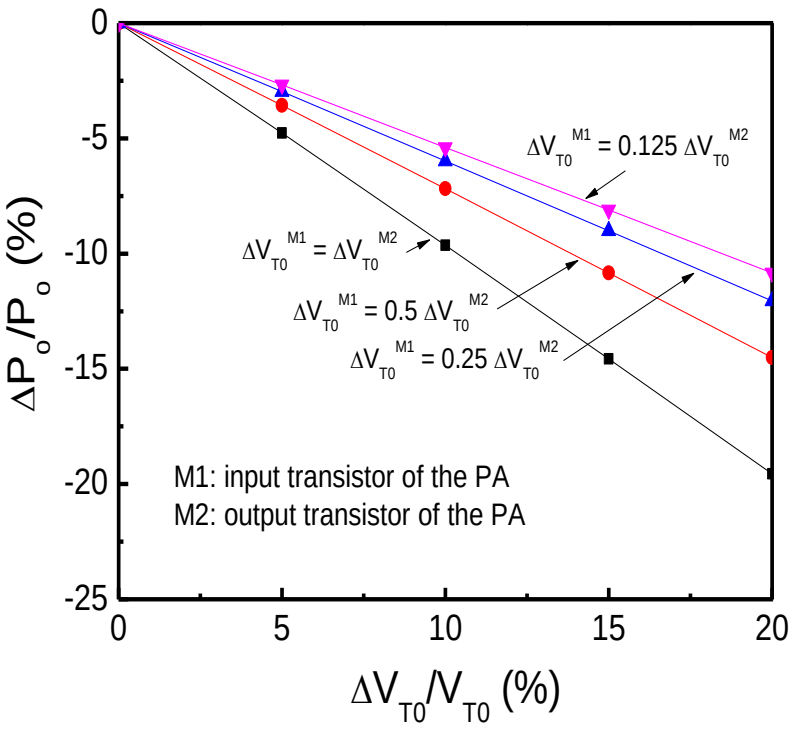
The oxide under high voltage stress may experience some kind of soft breakdown before hard breakdown [26]. Soft breakdown increases the gate leakage current noise due to formulation of random defects and conducting path within the oxide [27]. Soft breakdown effect may be modeled using nonlinear current sources [19], while the hard breakdown can be realized by using breakdown resistances [28]. In general, oxide breakdown decreases the output power and power efficiency of power amplifiers [29].

3.5 RF Stress Simulation

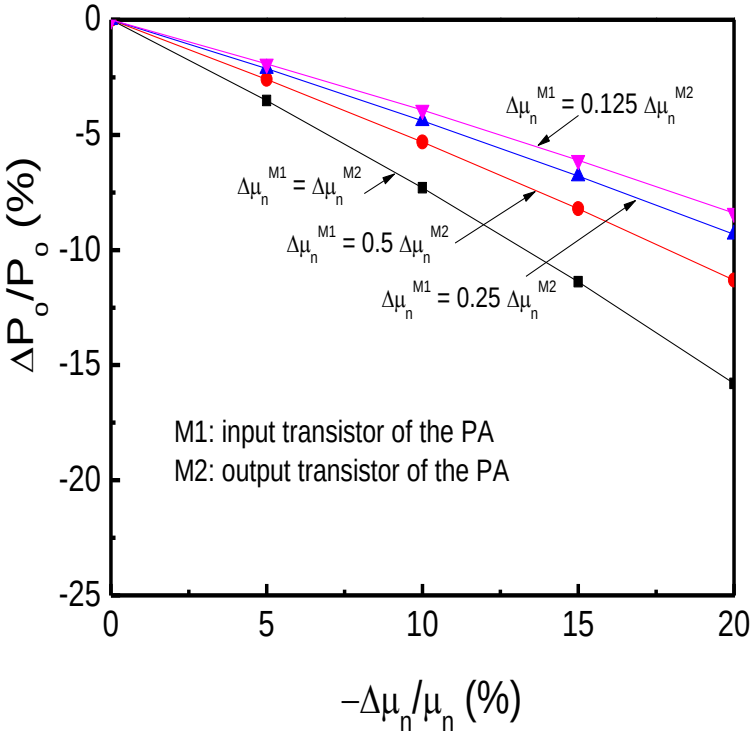
Hot electron injection originates from energetic electrons or holes in the channel entering oxide layer produce oxide trap charge and interface states, which in turn increase the transistor threshold voltage and decreases the effective channel electron mobility. The output power and power-added efficiency versus threshold voltage shift and mobility degradation are depicted in Figs. 16 and 17, respectively. In general, the threshold voltage shift accumulates over time ($\Delta V_T \propto t^n$). To account for different degrees of hot electron stress effects on M1 and M2 over a period of time, the shift of threshold voltage in M1 is modeled differently than that in M2. For example, ΔV_{T0} in M1 could be set to 1/8, ¼, ½, and $1\times\Delta V_{T0}$ of M2. As seen in Fig. 16(a) the largest output power degradation occurs

when $\Delta V_{T0}^{M1} = \Delta V_{T0}^{M2}$. This is because the output of the first stage transistor M1 drives the second stage transistor M2 for output power. When the input transistor's driving current drops, the overall output power of the PA decreases. Similar characteristics are observed for the output power versus electron mobility shift. The output power decreases when the electron mobility decreases. The worst case of degradation occurs when $\Delta\mu_n^{M1} = \Delta\mu_n^{M2}$ as shown in Fig. 16(b).

Furthermore, the normalized power-added efficiency versus normalized threshold voltage shift and mobility degradation has been examined. The simulation results are shown in Fig. 17. The power-added efficiency decreases with the increase in threshold voltage and the decrease in electron mobility. Again, the worst case of degradation occurs when $\Delta V_{T0}^{M1} = \Delta V_{T0}^{M2}$ and $\Delta\mu_n^{M1} = \Delta\mu_n^{M2}$. To reduce hot electron degradation effects on power amplifier performance, the cascode transistor topology may be used to reduce electron field on the drain edge of MOS transistors.

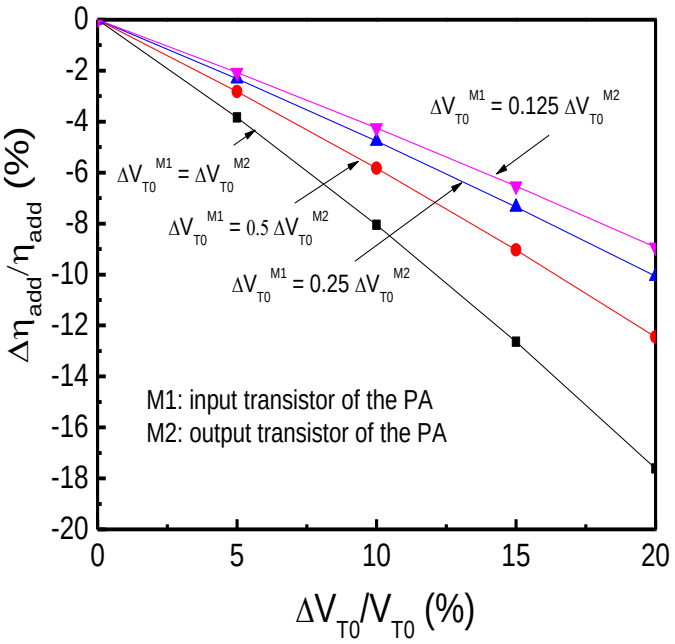


(a)

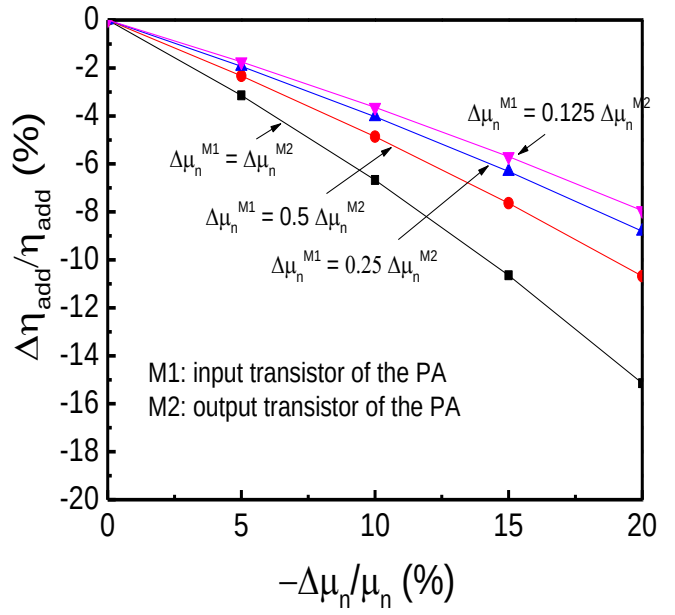


(b)

Figure 16 Normalized output power versus (a) threshold voltage and (b) mobility shift



(a)

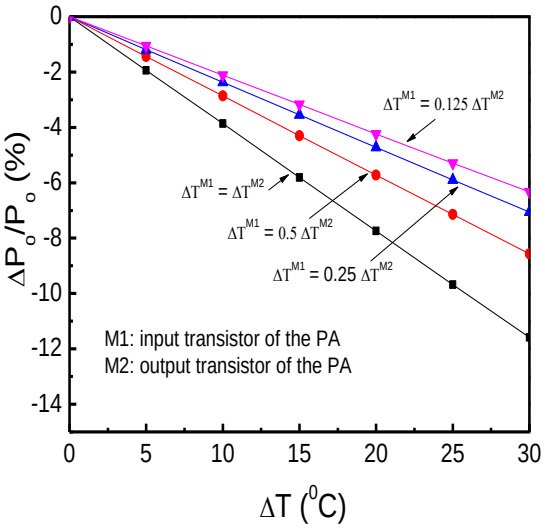


(b)

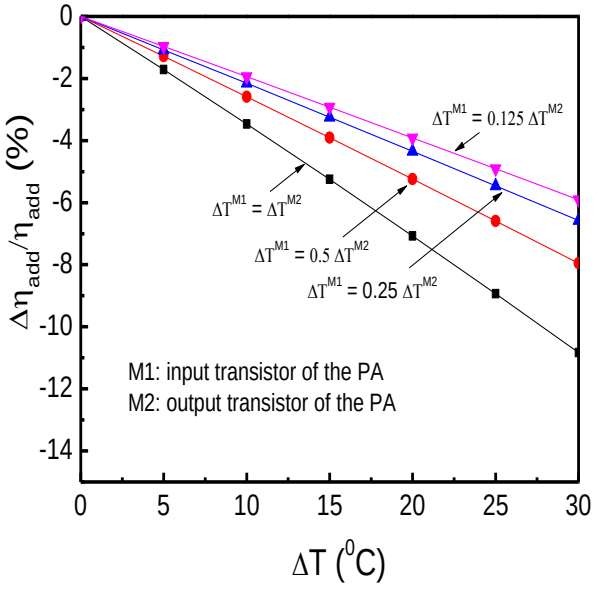
Figure 17 Normalized power-added efficiency versus (a) threshold voltage and (b) mobility shift.

High drain current and high drain-source voltage result in large power dissipation, which causes device self-heating. The transistor temperature rise ΔT in M2 is generally larger than that in M1 due

to larger dc current and ac power flowing through the output transistor M2. To account for a wide range of temperature rise, ΔT^{M1} = 1/8, ¼, ½, and 1×ΔT^{M2} are simulated. Both the output power and power-added efficiency decrease with increasing temperature resulting from device self-heating as shown in Fig. 18.



(a)



(b)

Figure 18 Normalized (a) output power and (b) power-added efficiency versus temperature rise.

3.6 Summary

A class F power amplifier at 5.8 GHz has been designed and analyzed. Its pre-layout and post-layout performances are compared. Post-layout parasitic effect decreases the output power and power-added efficiency. Physical insight of hot electron impact ionization and device self-heating has been examined using mixed-mode device and circuit simulation to mimic the class F PA operating environment. The output transistor has larger impact ionization rates and self-heating due to larger power dissipation and higher drain electric field than those of the input transistor. Hot electron effect increases the threshold voltage and decreases the electron mobility of the n-channel transistor, which in turn decreases the output power and power-added efficiency of the power amplifier, as evidenced by the RF circuit simulation results. The device self-heating also reduces the output power and power-added efficiency of the PA.

CHAPTER FOUR: POWER AMPLIFIER RESILIENT DESIGN FOR PROCESS, VOLTAGE AND TEMPERATURE VARIATIONS

This chapter is about a robust adaptive design technique to reduce PVT variation effects on RF circuits. The adaptive body biasing scheme uses a current source for PVT sensing to provide resilience through the threshold voltage adjustment to maintain power amplifier performance over a wide range of variability. This adaptive body biasing technique is used to minimize PVT variations of RF class AB power amplifier.

4.1 Current Source Design

An on-chip variability sensor using current source is proposed to detect process, supply voltage, and temperature variations or even reliability degradation stemming from hot electron effect. The PVT variations yield a control signal from the designed current source. In Fig. 1 the current-source circuit is made of n-channel transistors M1, M2 and M3. The transistors M1 and M2 have the same width and length and two times width of transistor M3. On the right branch in Figure 19, a resistor R is used to set a control voltage VCtrl. The reference current Iref is dependent on the PVT fluctuations.

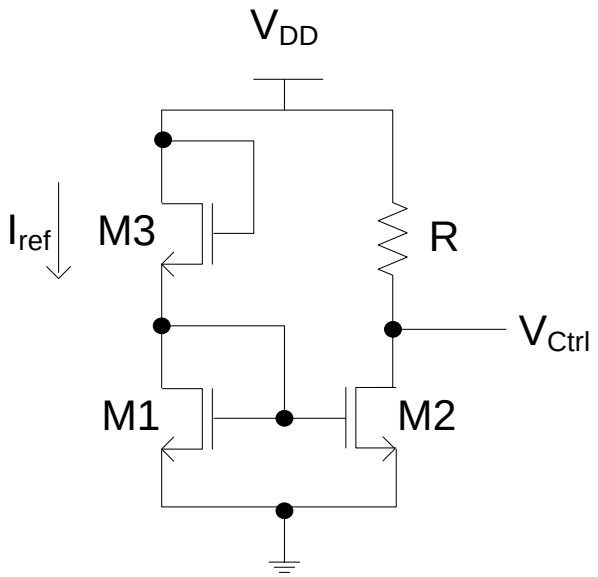


Figure 19 Current-source circuit schematic.

The Kirchhoff's current law to solve for VCtrl is given by

$$V_{Ctrl} = V_{DD} - I_{ref} R \tag{4}$$

and I_{ref} is the reference current and can be obtained as [30]

$$Iref = \frac{(V_{DD} - V_{T1} - V_{T3})^2}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}}\right)^2} \tag{5}$$

where V_T is the threshold voltage, L is the channel length, W is the channel width, and Kn is the transconductance factor ($Kn = \mu_n \varepsilon_{ox}/t_{ox}$). Subscripts 1 and 3 represent the transistors M1 and M3, respectively.

The V_{Ctrl} shift because of supply voltage variation is derived using (1 and 2)

$$\frac{\partial V_{Ctrl}}{\partial V_{DD}} = 1 - \frac{2R(V_{DD} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}}\right)^2} \quad (6)$$

The V_{Ctrl} shift due to mobility fluctuation is given by

$$\frac{\partial V_{Ctrl}}{\partial \mu_n} = -\frac{\varepsilon_{ox} R}{t_{ox}} \frac{(V_{DD} - V_{T1} - V_{T3})^2}{\left(\sqrt{\frac{2L_1}{W_1}} + \sqrt{\frac{2L_3}{W_3}}\right)^2} \quad (7)$$

Furthermore, the V_{Ctrl} shift resulting from fluctuation of the threshold voltage from M1 or M3 is

$$\frac{\partial V_{Ctrl}}{\partial V_{T1,3}} = 2R \frac{(V_{DD} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}}\right)^2} \quad (8)$$

Combing (6)–(8) yields the overall V_{Ctrl} variation as follows:

$$\Delta V_{Ctrl} = \left[1 - \frac{2R(V_{DD} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{KP_n W_1}} + \sqrt{\frac{2L_3}{KP_n W_3}}\right)^2}\right] \Delta V_{DD} - \left[\frac{\varepsilon_{ox} R}{t_{ox}} \frac{(V_{DD} - V_{T1} - V_{T3})^2}{\left(\sqrt{\frac{2L_1}{KP_n W_1}} + \sqrt{\frac{2L_3}{KP_n W_3}}\right)^2}\right] \Delta \mu_n + \left[2R \frac{(V_{DD} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{KP_n W_1}} + \sqrt{\frac{2L_3}{KP_n W_3}}\right)^2}\right] \Delta V_{T1} + \left[2R \frac{(V_{DD} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{KP_n W_1}} + \sqrt{\frac{2L_3}{KP_n W_3}}\right)^2}\right] \Delta V_{T3} \quad (9)$$

4.2 Tuning for Variability

The sensitivity of the class AB PA is evaluated in Figure 20. The PVT variations change behaviors of the PA and also degrade the performance. In the simulation, the PVT variations are given to the PA circuit. Adaptive body biasing is used to find a range of body biasing voltage (V_{ABB}) to compensate each variation. V_{Ctrl} signal is efficiently transformed to an optimal body bias signal for power amplifier application. From a range of V_{ABB}, an operational amplifier is used as a voltage shifter and amplifier to adjust the V_{Ctrl} to meet a required V_{ABB} (see Figure 20). Choosing appropriate size of resistor R1 and R2 using (10) provides a matched V_{ABB} for PA. For example, for a reference voltage (V_{ref}) of 0.4 V, R1 and R2 can be designed at 500 Ω and 1500 Ω, respectively.

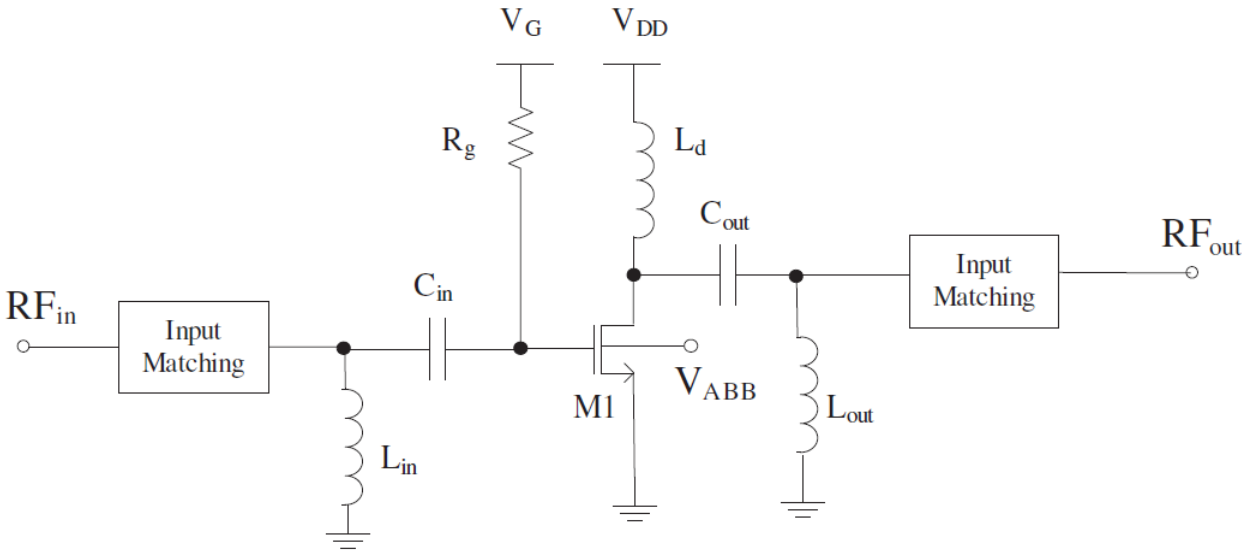


Figure 20 A class AB PA with adaptive body biasing.

$$V_{ABB} = \frac{R2}{R1}(V_{Ctrl} - V_{ref}) \qquad (10)$$

Due to the body effect, the threshold voltage of the power amplifier transistor is described by the following expression

$$V_T = V_{T0} + \gamma(\sqrt{2\phi F - V_{ABB}} - \sqrt{2\phi_F}) \quad (11)$$

where γ is the body effect factor and ϕ_F represents the Fermipotential. The threshold voltage shift of the PA transistor is modeled by the fluctuation of V_{T0} and V_{ABB} as

$$\Delta V_T = \frac{\partial V_T}{\partial V_{T0}}\Delta V_{T0} + \frac{\partial V_T}{\partial V_{ABB}}\Delta V_{ABB} = \Delta V_{T0} - \frac{\gamma}{2\sqrt{2\phi_F - V_{ABB}}}\Delta V_{ABB} \quad (12)$$

From (10) the VABB shift is given by

$$\Delta V_{ABB} = \frac{\partial V_{ABB}}{\partial V_{Ctrl}}\Delta V_{Ctrl} = \frac{R_2}{R_1}\Delta V_{Ctrl} \quad (13)$$

Thus, the threshold voltage shift of the power amplifier input transistor due to PVT variations are summed as

$$\Delta V_T = \Delta V_{T0} - \frac{\gamma R_2}{2R_1\sqrt{2\phi_F - V_{ABB}}}\left\{\left[1 - \frac{2R(V_{DD} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}}\right)^2}\right]\Delta V_{DD} - \left[\frac{\varepsilon_{ox} R}{t_{ox}}\frac{(V_{DD} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}}\right)^2}\right]\Delta\mu_n\right\}$$
$$+\left\{\left[2R\frac{(V_{DD} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}}\right)^2}\right]\Delta V_{T1} + \left[2R\frac{(V_{DD} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}}\right)^2}\right]\Delta V_{T3}\right\} \quad (14)$$

The drain current fluctuation subjects to key transistor parametric drifts $\Delta\mu_n$, ΔV_{GS} and ΔV_T can be modeled as

$$\Delta I_D = \frac{\partial I_D}{\partial \mu_n}\Delta\mu_n + \frac{\partial I_D}{\partial V_{GS}}\Delta V_{GS} + \frac{\partial I_D}{\partial V_T}\Delta V_T \quad (15)$$

Assume the V_{GS} shift is proportional to the fluctuation of V_{DD}.

$$\Delta V_{GS} = \alpha \Delta V_{DD} \quad (16)$$

where a is a fitting parameter. Using (14)–(16) the fluctuation of drain current normalized to its fresh current is expressed as follows:

$$\Delta V_T = \frac{\Delta \mu_n}{\mu_n} + \frac{2\alpha \Delta V_{DD}}{V_{GS} - V_T} - \frac{2}{V_{GS} - V_T} \left(\Delta V_{T0} - \frac{\gamma R_2}{2R_1 \sqrt{2\phi_F - V_{ABB}}} \left\{ \left[1 - \frac{2R(V_{DD} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}} \right)^2} \right] \Delta V_{DD} - \left[\frac{\varepsilon_{ox} R}{t_{ox}} \frac{(V_{DD} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}} \right)^2} \right] \Delta \mu_n \right\} \right) + \left[2R \frac{(V_{DD} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}} \right)^2} \right] \Delta V_{T1} + \left[2R \frac{(V_{DD} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}} \right)^2} \right] \Delta V_{T3} \quad (17)$$

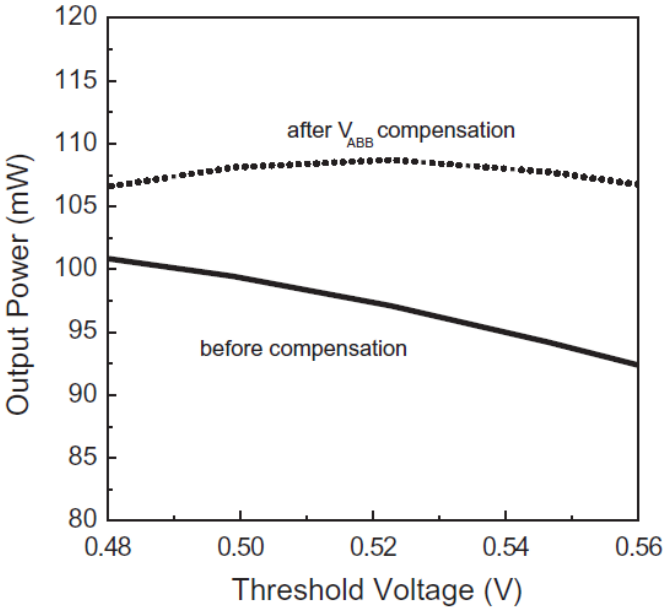
In the above equation the terms beyond ΔV_{T0} represent the VDD, mobility, and threshold voltage compensation effects. To normalized output power degradation is related to the normalized drain current degradation as follows [18]:

$$\frac{\Delta Po}{Po} \approx \frac{\Delta I_D}{I_D} \quad (18)$$

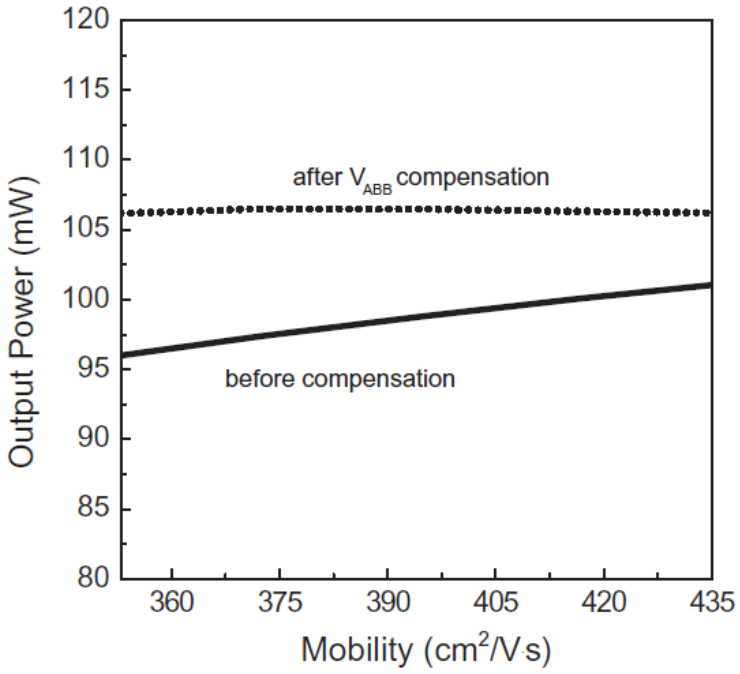
4.3 Compensated Results

The power amplifier with the current source compensation technique is compared with the PA without compensation using ADS simulation. For the process variation effect, the output power is evaluated against threshold voltage and mobility variations as shown in Figure 21 (a) and (b). It is clear from Figure 21 (a) and (b) that the power amplifier with adaptive body bias is more robust against threshold voltage variation (see Figure 21 (a)) and mobility fluctuation (Figure 21 (b)). For the process variation effect, the output power of the PA has also been evaluated using different

process corner models due to inter-die variations. The simulation result of the fast–fast, slow–slow, and nominal–nominal models is shown in Figure 22.



(a)



(b)

Figure 21 (a) Output power versus threshold voltage shift. (b)Output power versus mobility variation

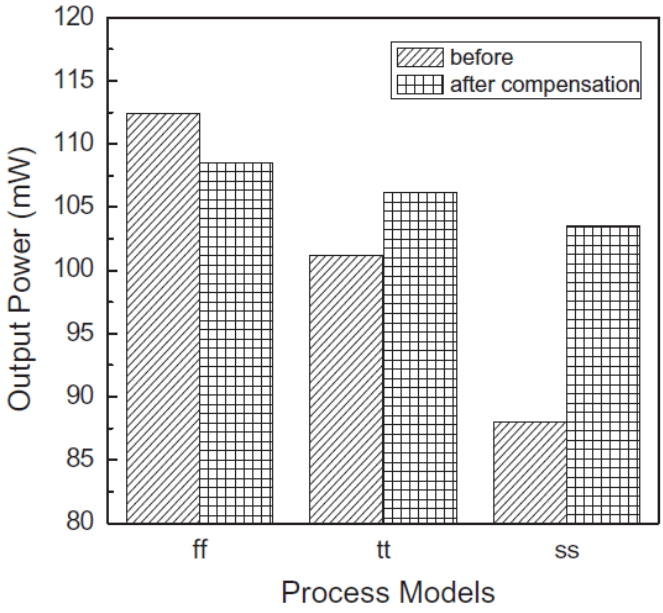


Figure 22 Output power versus process corner models.

Clearly, the PA using the adaptive body bias compensation exhibits better stability against process variation effect. Figure 23 and 24 show the output power of the power amplifier versus temperature variation and supply voltage change, respectively. As seen in Figs. 23 and 24 the output power of the PA using the adaptive body bias compensation technique demonstrates less sensitivity over temperature and VDD variations.

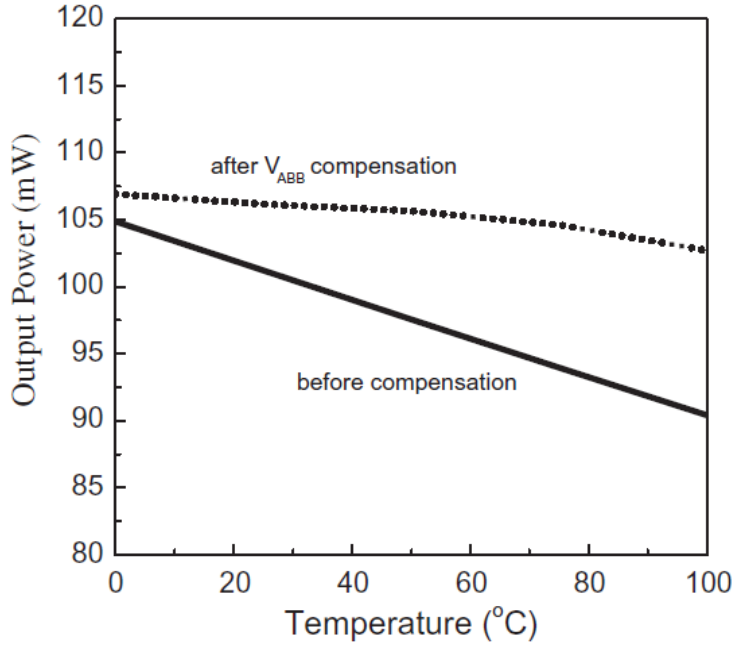


Figure 23 Output power versus temperature.

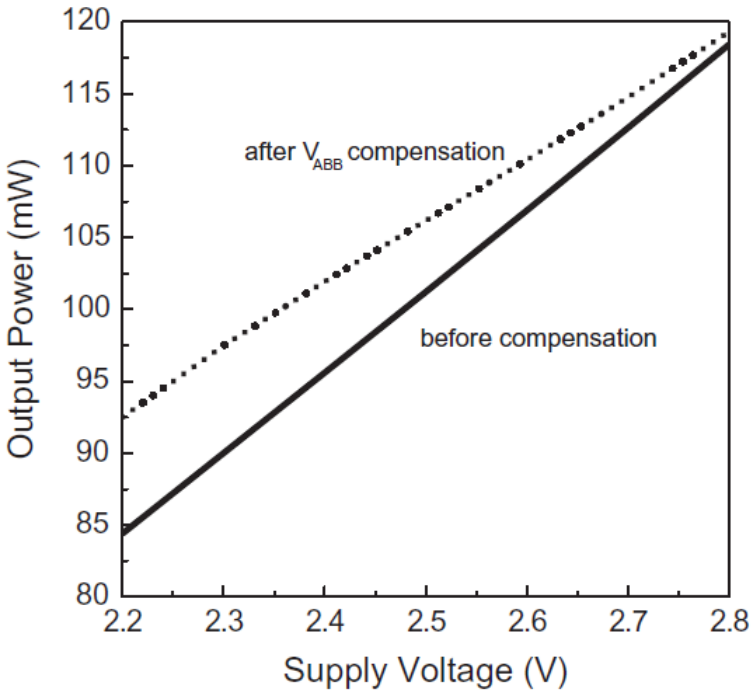


Figure 24 Output power versus supply voltage.

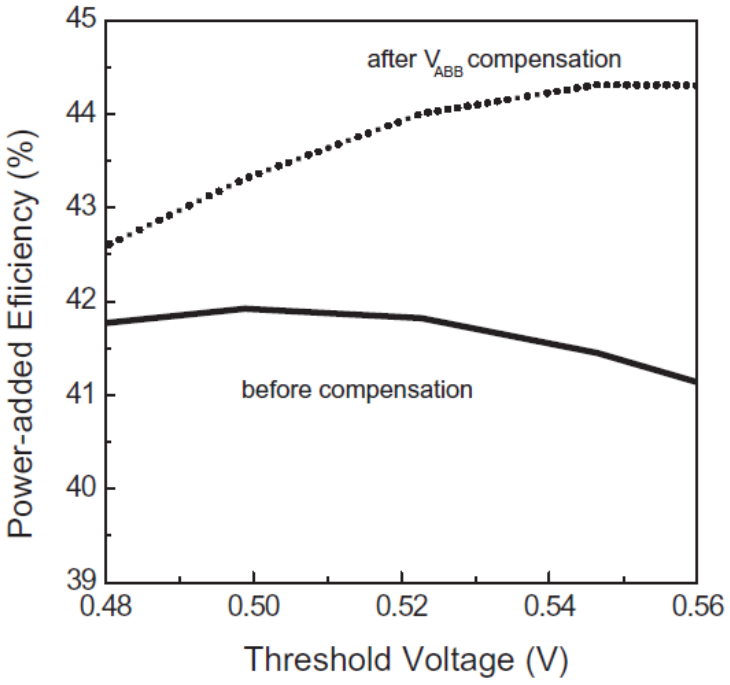


Figure 25 Power-added efficiency as a function of threshold voltage.

In addition, the power-added efficiency of the power amplifier with or without adaptive body bias compensation is examined against semiconductor process variations effects. Figure 25 and 26 display the improvement of power-added efficiency of the PA with ABB compensation over that without adaptive body bias for the threshold voltage shift (see Figure 25) and mobility variation (see Figure 26).

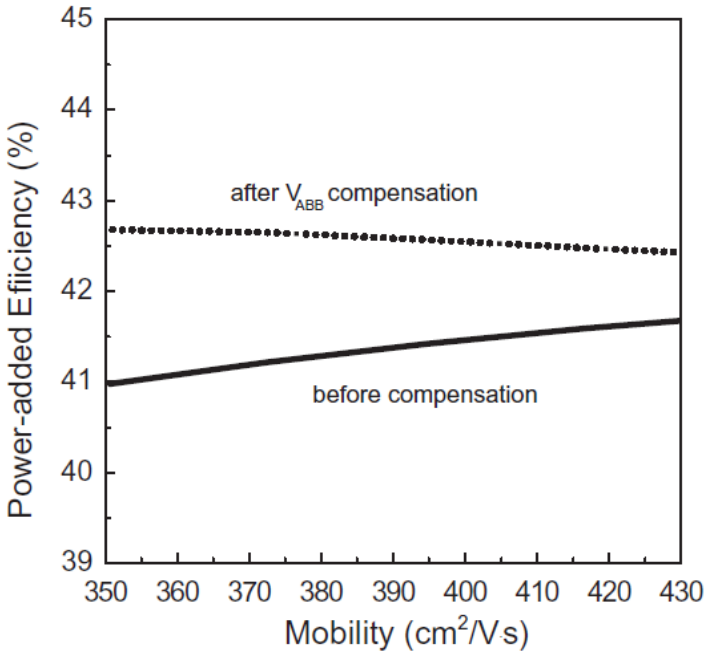


Figure 26 Power-added efficiency as a function of mobility.

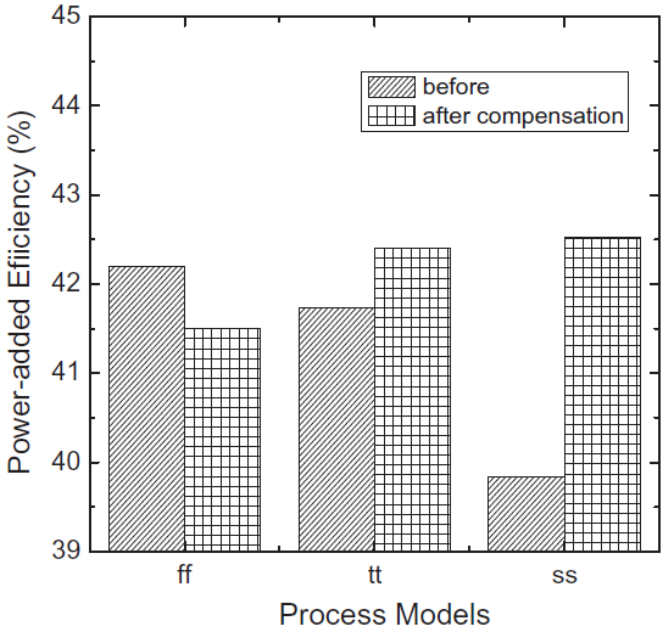


Figure 27 Power-added efficiency vs process corner models.

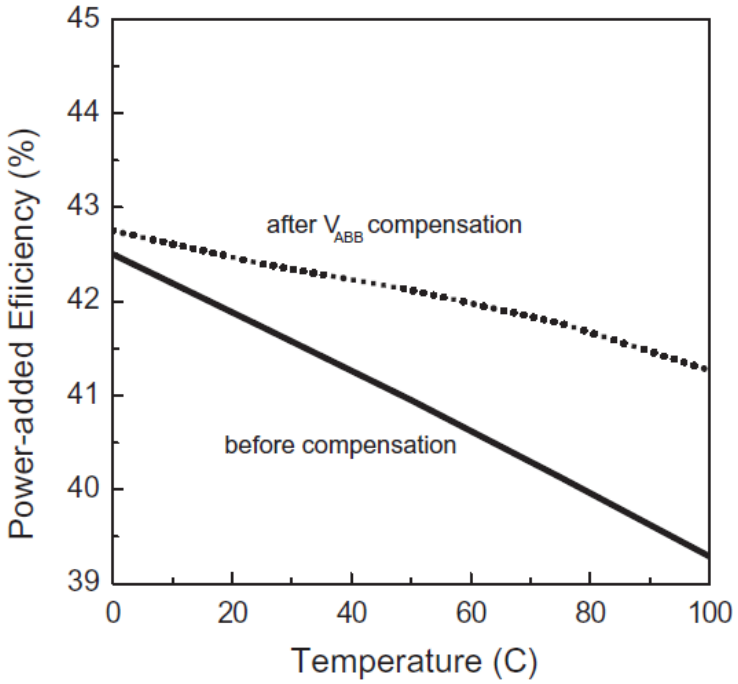


Figure 28 Power-added efficiency versus temperature.

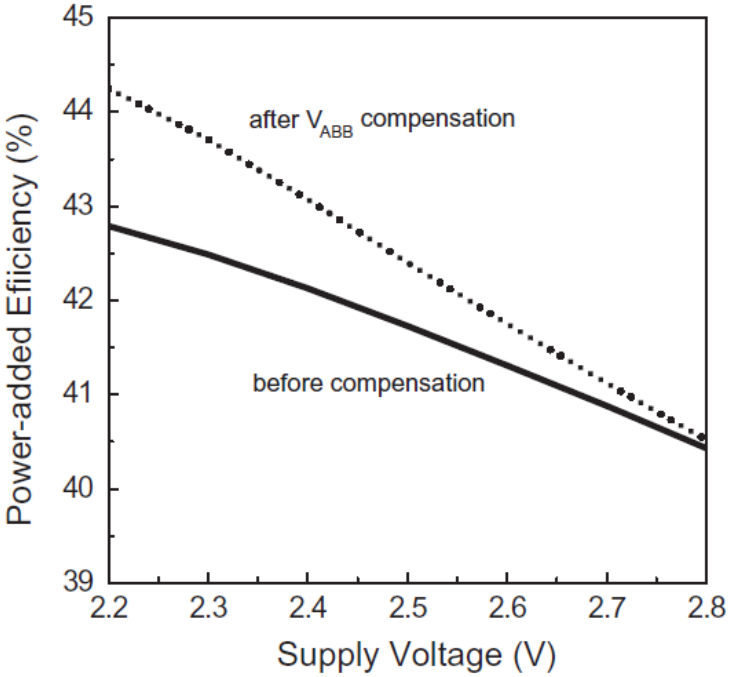


Figure 29 Power-added efficiency versus supply voltage.

For the process corner models the power-added efficiency of the PA with ABB compensation shows less process sensitivity, as evidenced by the plot in Figure 27. Then, the power-added efficiency is

compared against temperature and supply voltage variations. The power-added efficiency is getter better for the PA with ABB compensation as shown in Figure 28 and 29

4.4 Summary

In this work, the PVT compensation of power amplifier using a current-source as an on-chip sensor has been presented. The adaptive body bias design using current sensing makes the output power and power-added efficiency much less sensitive to process, supply voltage, and temperature variations, predicted by derived analytical equations and verified by ADS circuit simulation results.

CHAPTER FIVE: PROCESS VARIATION STUDY ON RF MIXER

5.1 Process Variations

To gain better speed and further reduce coat, silicon CMOS are scaled down to 22 nm [31] and beyond. The well-known reliability mechanisms such as gate oxide breakdown (GOB), hot carrier injection (HCI), and negative bias temperature instability (NBTI) remain very important for the design of digital and RF circuits.

HCI is associated with hot carrier get trapped in gate oxide which is deteriorated by high lateral field induced impact ionization (I.I.), while GOB is related to field -induced oxide traps or defects due to oxide vertical scaling. NBTI occurs due to a build-up of positive charges occurs either at the Si/SiO2 interface or in the oxide layer of p-channel MOSFETs under negative gate bias at higher temperatures. The reaction-diffusion model [32] illustrates the holes in the inversion layer of pMOSFETs react with the Si-H bonds at the SiO2/Si interface. The hydrogen species diffuse away from the interface toward the polysilicon gate. This causes the threshold voltage shift of p-MOSFETs.

Originally, process variations were considered in die to die variations. However, with transistors progress into nanoscale regime, intra die variations are posing the major design challenge as technology node scales. Fluctuations with intrinsic device parameters that result from process uncertainties have substantially affected the device characteristics. For state-of-the-art nano-scale circuits and systems, device variation and uncertainty of signal propagation time between dies and inside die have become crucial in the variation of system timing and the determination of clock speed. Yield analysis and optimization, which takes into account the

manufacturing tolerances, model uncertainties, variations in the process parameters, and aging factors are known as indispensable components of the circuit design procedure.

5.2 Mixer Circuit Design

An idealized mixer is shown in Figure 30. An RF mixer is an active or passive device that converts a signal from one frequency to another. It can either modulate or demodulate a signal. It has three signal connections, which are called ports. These three ports are the radio frequency (RF) input, the local oscillator (LO) input, and the intermediate frequency (IF) output.

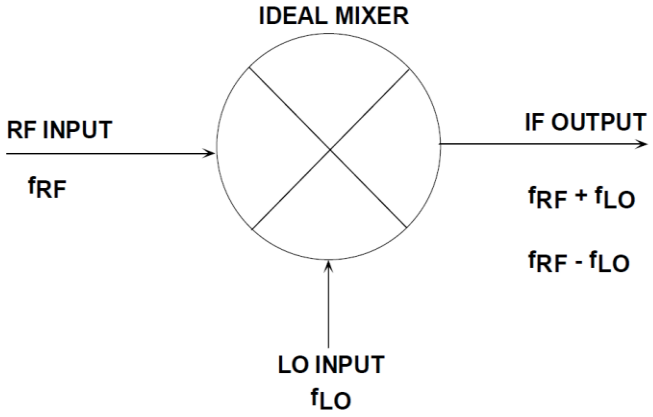


Figure 30 The mixing process.

A mixer takes an RF input signal at a frequency f_{RF}, mixes it with a LO signal at a frequency f_{LO}, and produces an IF output signal that consists of the sum and difference frequencies, $f_{RF} \pm f_{LO}$. The user provides a bandpass filter that follows the mixer and selects the sum ($f_{RF} + f_{LO}$) or difference ($f_{RF} - f_{LO}$) frequency.

A mixer is characterized by evaluating its various performance metrics such as noise figure and conversion gain. Noise figure is the ratio of input SNR at RF port to the output SNR at IF port. This parameter impacts receiver's sensitivity. Conversion gain is the ratio of desired IF output to the input RF input signal value. Conversion gain can be either calculated as Voltage or Power. When the

mixer's input impedance equals the load impedance and when it is equal to the source impedance, the voltage and power conversion gain are the same in decibels.

In this work, the reliability and process variability on the double-balance Gilbert RF mixer has been examined. Here, the most widely used double-balance Gilbert structure in Figure 31 is used to evaluate the process variations and aging effects on RF mixer performance. In this figure positive and negative RF input signals are applied to transistors M1 and M2. Local oscillator (LO) signals are applied to switching transistors M3, M4, M5, and M6. The transistor M7 provides the bias current. RF and LO multiplication produces the output signal at intermediate frequency (IF).

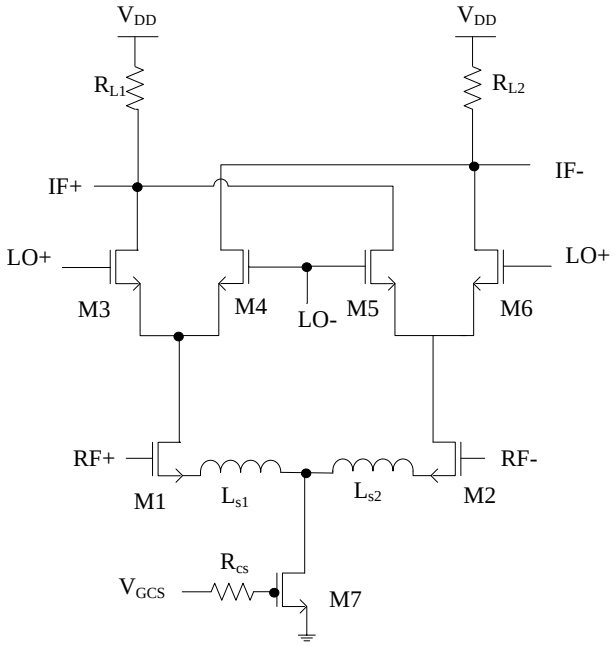


Figure 31 Schematic of a double-balance Gilbert RF mixer

The conversion gain (CG) of the mixer can be derived as

$$CG = \frac{2}{\pi}\left(\frac{R_L}{R_S + \frac{1}{g_m}}\right) \quad (19)$$

where R_L is the load resistance, R_S is the inductor resistance, and g_m is the transconductance. The noise figure (NF) of the mixer is given by

$$NF = 10\log_{10}(F) \tag{20}$$

where F is the flicker noise derive as

$$F = \frac{\pi^2}{4}\left(1 + \frac{2\gamma}{g_m R_S} + \frac{2}{{g_m}^2 R_L R_S}\right) \tag{21}$$

and γ is the noise factor.

The sensitivity of the Gilbert cell mixer can be examined. The process variation and the aging effect may degrade the mixer performance. The conversion gain variation is modeled by the fluctuation of g_m and bias current drift as

$$\Delta CG = \frac{\partial CG}{\partial g_m}\Delta g_m = \frac{\partial CG}{\partial g_m}\left(\frac{\partial g_m}{\partial V_T}\frac{\partial V_T}{\partial I_{bias}} + \frac{\partial g_m}{\partial \mu_n}\frac{\partial \mu_n}{\partial I_{bias}}\right)\Delta I_{bias} \tag{22}$$

where un is the mobility and VT is the threshold voltage.

Expanding the partial derivatives in (22) the conversion gain variation can be written as

$$\Delta CG = \frac{2}{\pi g_m^2}\frac{R_L}{(R_S + \frac{1}{g_m})^2}\left\{\frac{I_{bias}}{(V_{GSM1} - V_T)^2}\frac{L}{\mu_n C_{ox} W_{CS}(V_{GSCS} - V_T)} + \frac{I_{bias}}{\mu_n (V_{GSM1} - V_T)}\frac{2L}{C_{ox} W_{CS}(V_{GSCS} - V_T)}\right\}\Delta I_{bias} \tag{23}$$

where C_{ox} is the oxide capacitance per unit area, L is the channel length and W is the channel length of the current source transistor, V_{GSM1} is the gate-source voltage to the RF transistor, and V_{GSCS} is the gate-source voltage to the current source transistor.

Similarly, the noise figure shift is derived as

$$\Delta F = \frac{\partial F}{\partial g_m}\Delta g_m = \frac{\partial F}{\partial g_m}\left(\frac{\partial g_m}{\partial V_T}\frac{\partial V_T}{\partial I_{bias}} + \frac{\partial g_m}{\partial \mu_n}\frac{\partial \mu_n}{\partial I_{bias}}\right)\Delta I_{bias}$$

$$= \left\{\frac{\pi^2}{4}\left(\frac{-2\gamma}{{g_m}^2 R_S} - \frac{1}{{g_m}^3 R_L R_S}\right)\right\}\left\{\frac{I_{bias}}{(V_{GSM} - V_T)^2}\frac{L}{\mu_n C_{ox} W_{CS}(V_{GSCS} - V_T)} + \frac{I_{bias}}{\mu_n (V_{GSM} - V_T)}\frac{2L}{C_{ox} W_{CS}(V_{GSCS} - V_T)}\right\}\Delta I_{bias} \tag{24}$$

Eqs. (23) and (24) account for process variations and aging effect of the mixer.

5.3 Invariant Current Source

It is clear from (22) to (24) that the mixer performance is dependent on the drain current of current source. To maintain the mixer performance, the drain current of M7 has to be kept stable. Thus, process invariant current source circuit shown in Figure 32 is employed. In Figure 32 drain currents of M8 and M9 are designed the same. Changes in M8 and M10 drain currents are negatively correlated to remain a stable bias current ($I_{D8} + I_{D10}$). For example, if the process variation increases the threshold voltage, but decreases the drain current of M8, the gate voltage of M10 increases ($V_{G10} = V_{DD} – I_{D9}R$). Thus, the drain current of M10 increases to compensate the loss of I_{D8}.

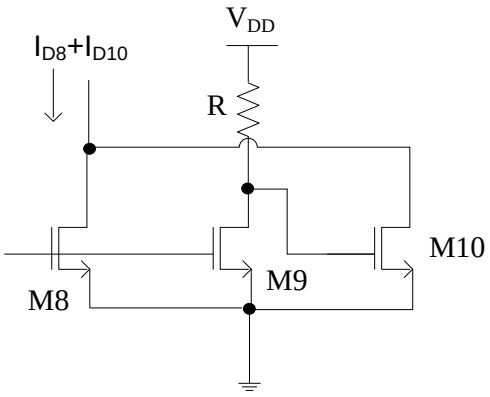


Figure 32 Process insensitive current source.

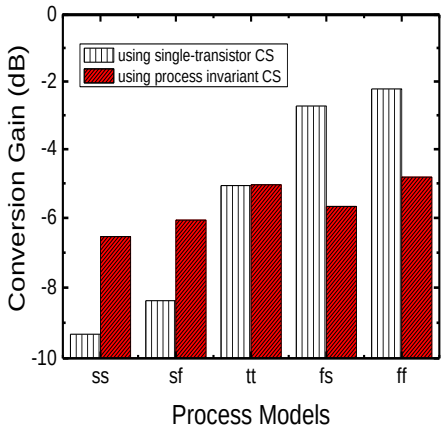
5.4 Simulation Results

ADS simulation is used to compare the mixer performance using the single transistor current source versus process invariant curernt source. The RF mixer is operated at 900 MHz with an intermediate frequency of 200 MHz. In the circuit design, CMOS 0.18 µm mixed-signal technology node is used. R_{L1} is 210 Ω and R_{L2} is 190 Ω. The transistor channel width of M3 to M6 is 200 µm. The channel widths of M1 and M2 are 190 and 210 µm, respectively. L_{s1} and L_{s2} are chosen at 2 nH.

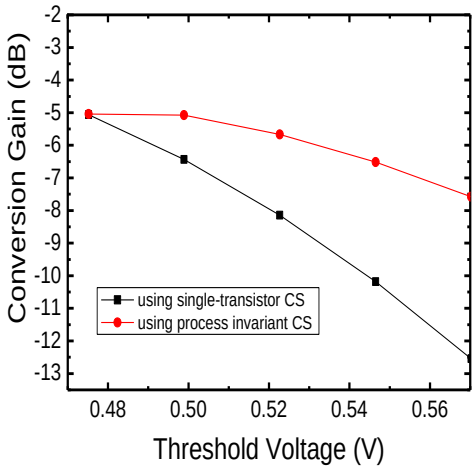
The width of M7 is 250 μm. The gate resistor size of the current source is 400 Ω. The mixer sets the gate biasing voltage at the current source at 0.62 V. In the current source, the transistor M8 and M9 match each other as 100 μm. The width of M10 is 600 μm. The supply voltage V_{DD} is 1.8 V.

For the process variation effect, the conversion gain of the mixer is evaluated using different process corner models due to inter-die variations. The simulation result of the fast-fast, slow-slow, slow-fast, fast-slow, and normal-normal models is shown in Figure 33(a). It is clear from Figure 33(a) that the mixer with the invariant current source shows robust conversion gain against different process variations.

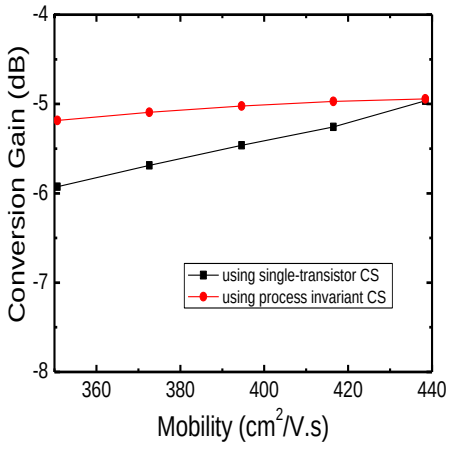
The conversion gain is also evaluated using different threshold voltage and mobility degradations resulting from aging (hot carrier effect) as shown in Figure 33(b) and 33(c). The hot-carrier injection increases the threshold voltage, but decreases the electron mobility. The conversion gain decreases with an increased threshold voltage or decreased mobility due to reduced transconductance. Again, the mixer with process invariant current source exhibits more robust performance againt threshold voltage increase and mobility degradation.



(a)



(b)



(c)

Figure 33 (a) Conversion gain predicted by different process models. (b) Conversion gain versus threshold voltage. (c) Conversion gain versus electron mobility

In addition, the noise figure of the mixer using the process invariant current source is compared with that using the single transistor current source. The noise figure versus different process models is displayed in Figure 34 (a). It is clear from Figure 34(a) that the noise figure is more stable over different corner models for the mixer using the current invariant current source. The noise figure also shows less threshold voltage and mobility sensitivity as evidenced in Figure 34(b) and 34(c). In Figure 34(b) and 35(c) the noise figure increases with increased threshold voltage and decreased mobility due to reduced drain current and transconductance in the mixer.

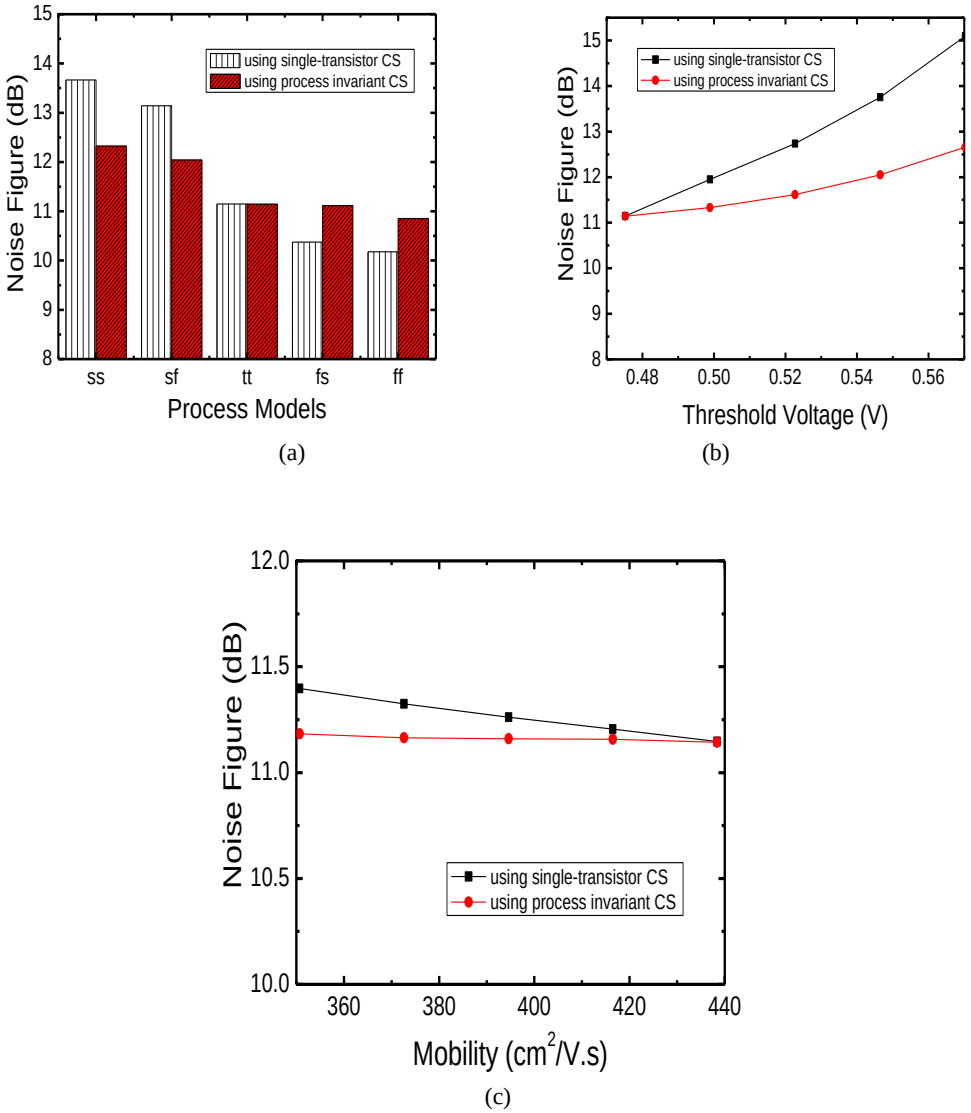


Figure 34(a) Noise figure predicted using different process models. (b) Noise figure versus threshold voltage. (c) Noise figure versus electron mobility

The output power of the mixer has been evaluated using different process corner models as well. As shown in Figure 35 (a) the output power of the mixer using the process invariant current source demonstrates robust performance against process variations. In Figure 35(b) and 35(c) the output power decreases with increased threshold voltage and decreased mobility due to reduced drain current in the mixer. The output power in Figure 35(b) and 35(c) also shows less sensitivity against aging effect which increases the threshold voltage and decreases the electron mobility.

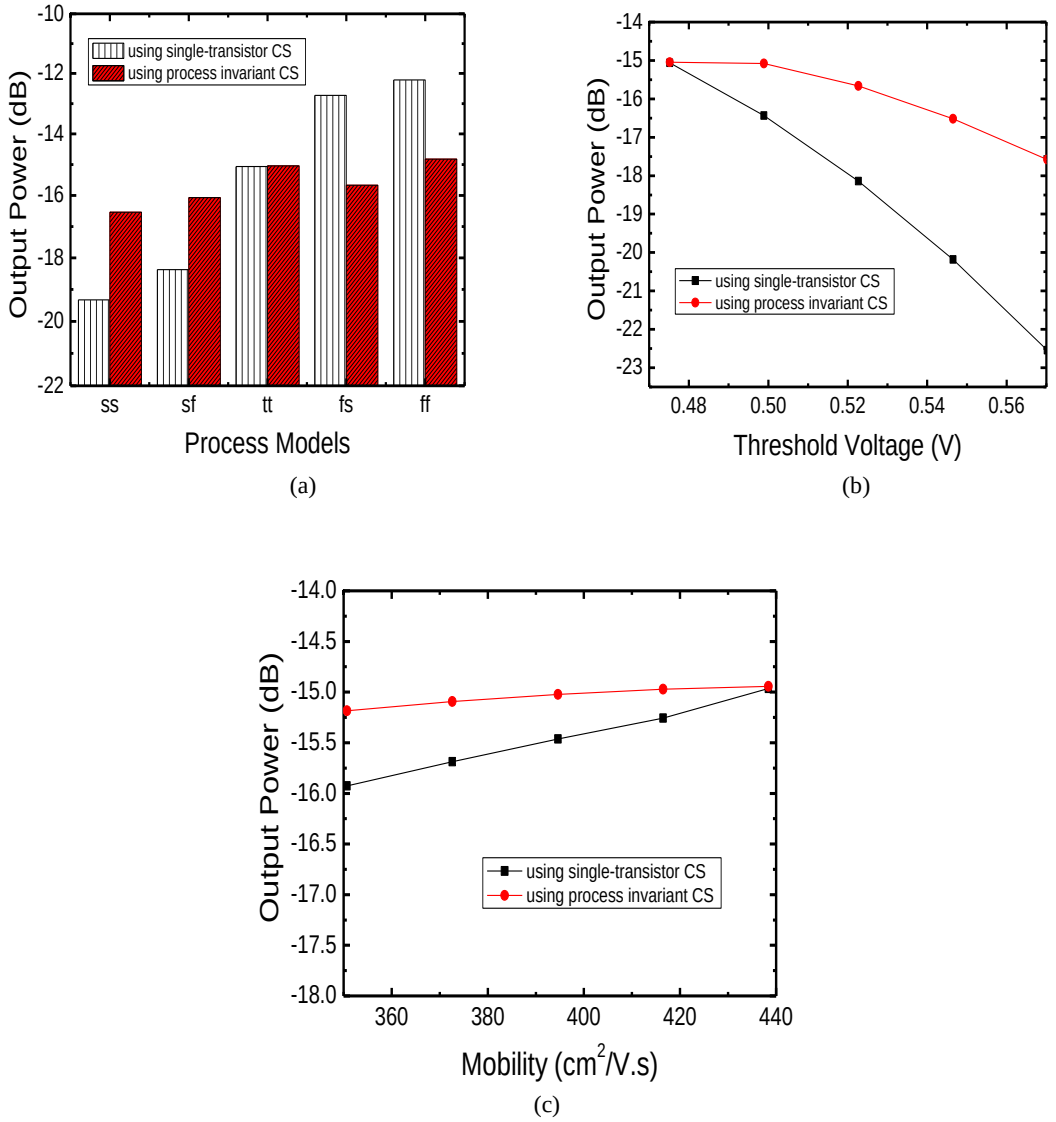


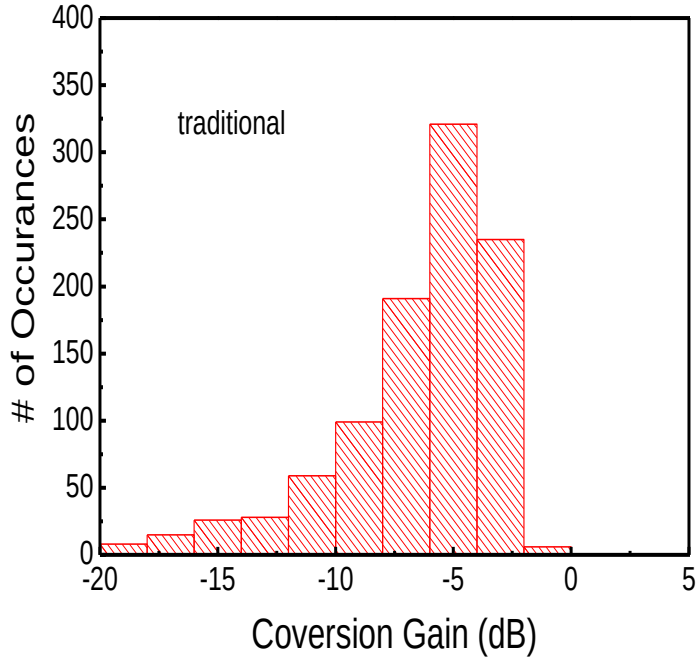
Figure 35(a) Predicted mixer out power using different process models. (b) Output power versus threshold voltage. (c) Output versus electron mobility.

5.5 Monte Carlo Simulation

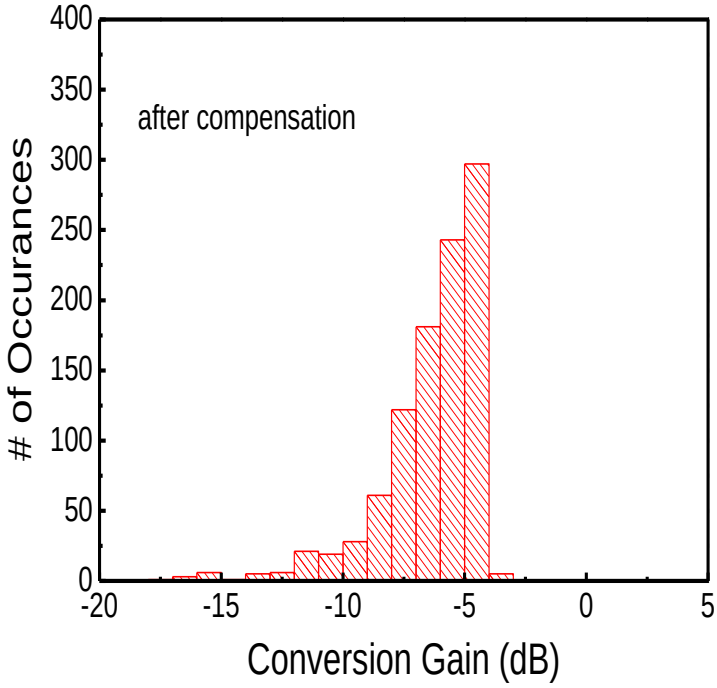
Monte Carlo analysis is associated with simulating the design over a given number of trials. In each trial the yield variables have values that distribute randomly with specified probability distribution functions. To further examine the process variation and compensation results on RF mixer, Monte Carlo (MC) circuit simulation has been performed. In ADS the Monte Carlo simulation assumes statistical variations (Gaussian distribution) of transistor model parameters such as the threshold voltage, mobility, and oxide thickness.

Monte Carlo simulation obtains the overall performance variation by randomly varying network parameter values according to statistical distributions. Monte Carlo yield analysis methods have been widely utilized as an efficient approach to estimate yield. It performs a series of trials from randomly generating yield variable values according to statistical-distribution specifications. Simulation is performed and results evaluated against stated performance specifications.

In the Monte-Carlo simulation a sample size of 1000 runs is adopted. Figure 36 (a) and 36 (b) display the histograms of conversion gain using single transistor current source (traditional) and using the process invariant current source (after compensation). For the mixer using the traditional current source, the mean value of conversion gain is -6.608 dB and its standard deviation is 3.18%. When the process invariant current source is applied, the mean value of conversion gain changes to -6.324 dB and its standard deviation reduces to 2.08%.



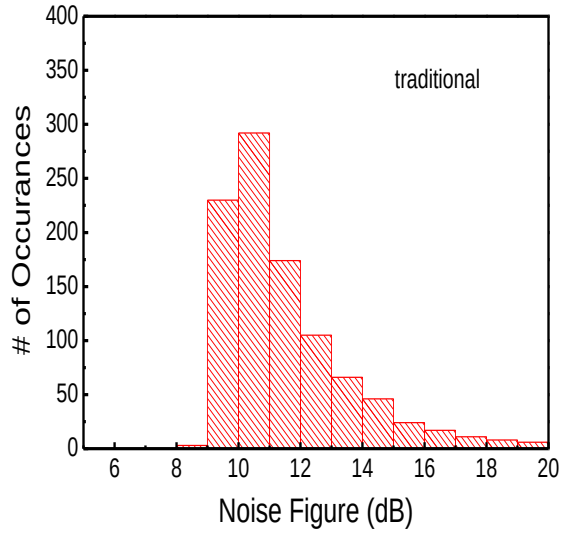
(a)



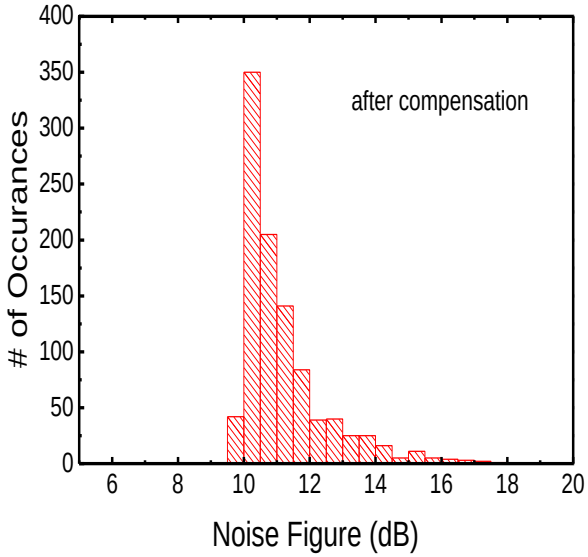
(b)

Figure 36 (a) Conversion gain statistical distribution without compensation (b) Conversion gain statistical distribution after process compensation effect

The noise figure after 1000 runs of Monte-Carlo simulation is diaplyed in Figure 37(a) and 37(b). For the mixer using the traditional current source, the mean value of noise figure is 11.667 dB and its standard deviation is 2.49%. When the process invariant current source is applied, the mean value of noise figure changes to11.159 dB and its standard deviation reduces to 1.29%. Clearly, the mixer using the proces invariant current source shows better stability against statistics process variations.



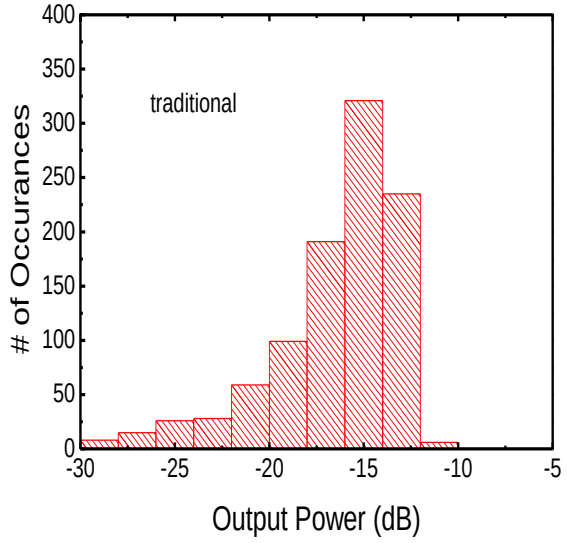
(a)



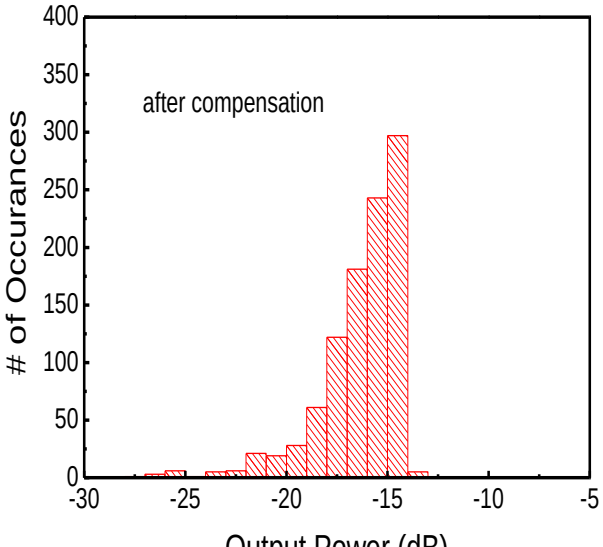
(b)

Figure 37 (a) Noise figure statistical distribution without current compensation (b) Noise figure statistical distribution after process compensation effect

In addition, the output power of the mixer is examined in Monte-Carlo simulation. Figure 38(a) and 38(b) demonstrates an improvement of output power for the mixer using the process invariant current source over that using the traditional current source. In Figure 38 the mean value of output power changes from -16.608 dB to -16.324 dB and its standard derivation reduces from 3.81% to 2.08% once the process invariant current source is used.



(a)



(b)

Figure 38 (a) Output power statistical distribution without current compensation (b) Output power statistical distribution after process compensation effect

5.6 Summary

Process variations and hot electron reliability on the mixer performance have been evaluated using different process models and key model parameters such as threshold voltage and mobility. The conversion gain, noise figure, and output power show robust performance for the mixer using the process invariant current source compared to that using the traditional single transistor current source. Monte-Carlo simulation demonstrates that the standard deviation of conversion gain reduces from 3.18% to 2.08%, the standard derivation of noise figure changes from 2.49% to 1.29%, the standard derivation of output power decreases from 3.81% to 2.08%, while their relative mean values remain the same.

CHAPTER SIX: PROCESS VARIATION STUDY ON CMOS VOLTAGE CONTROL OSCILLATOR

6.1 Process Variability Details

Statistical variability (SV), which is mainly caused by the discrete nature of charge and the granularity of matter, is one of the crucial limitations of device scaling. Process variability comes from random dopant fluctuation (RDF), line edge roughness (LER), and poly gate granularity (PGG). Inside each device, there are many regions needs to be doped specifically according to the device design. With device size becomes smaller, the average number of dopant atoms becomes less and less. It is extremely difficult to control the accuracy of the dopant amount, resulting fluctuations of dopants between devices. RDF [33] remains the dominant source of statistical variability and is mainly caused by silicon dopant fluctuations during fabrication process. It becomes more severe as device size shrinks. LER, is a random deviation of line edges from gate definition. It is notoriously difficult to scale with line width due to the molecular structure of photo-resist. Study shows that in bulk MOSFETs beyond gate lengths of 20nm it can overtake RDD in becoming the dominant IPF source [34]. PGG is basically attributed to gate dielectric thickness variations which contribute to threshold voltage variations; it is also caused by faster diffusion speed along the gate oxide grain boundaries which leads to uneven doping. High density of defect states along the boundaries of gate grains can cause Fermi level pinning, as a result, surface potential fluctuates within the MOSFET channel, which also contributes variation of threshold voltage and other device parameters as part of the effects of PGG. All the above mentioned process variations cause fluctuation of threshold voltage, mobility, and oxide thickness, which in turn affect the device and circuit performance. Furthermore, reliability issue could widen the standard derivation of process variation in Gaussian distribution [35].

6.1.1 Related Work

There have been numerous papers on reliability and process variability and their impacts on circuit performances published recently. To illustrate, NBTI is a major contributor to CMOS ring oscillator propagation delay [36]. GOB reduces the static noise margin of the SRAM cell[37]. Hot electron effect increases noise figure of low noise amplifier [38], decreases the output power and power efficiency of power amplifier [39], and increases phase noise of cross-coupled oscillator [40]. For process variability, random-dopant-induced variability was studied by Li et al. in nano-scale device cutoff frequency and CMOS inverter gate delay [41]. Hansson and Alvandpour demonstrated that the delay variation in the master-slave flip flops is 2.7 times larger than the delay variation in a 5-stage inverter chain [42]. Rao et al. described a on-chip technique to measure local random variation of FET current which is completely digital [43]. Mukhopadhyay et al. presented that large variability and asymmetry in threshold-voltage distribution significantly increase leakage spread and degrade stability of fully depleted SOI SRAM cell due to random dopant fluctuation [44].

What's more, to provide solutions of process variation, Didac Gómez [45] presented a circuit compensation technique to analyze and reduce temperature and process variation effects on low noise amplifiers and mixers. Han et al. [46] addressed a post-manufacturing self-tuning technique that aims to compensate for multi-parameter variations. However, the effects of aging and process variations on RF oscillator and the circuit technique to reduce variability effect on oscillator have not been well studied. Liu and Yuan [47] developed an adaptive body bias technique for power amplifier resilient to reliability aging and process variations.

6.2 Oscillator Circuit Design

Both the fabrication process-induced fluctuation and time-dependent degradation cause the MOSFET model parameter to drift. The threshold voltage and mobility are the two most significant model parameters that suffer from process uncertainty and reliability degradations. Here, the most widely used LC-VCO structure in Figure 39 is used to evaluate the process variations and aging effects on RF VCO performance. The LC-VCO is one of the most important building blocks in the implementation of a single radio chip in today's various wireless communication systems. LC-VCO is commonly used in CMOS radio frequency integrated circuits because of their good phase noise characteristics and their ease of implementation.

The architecture of LC-VCO uses a cross-coupled pair of NMOS transistors.

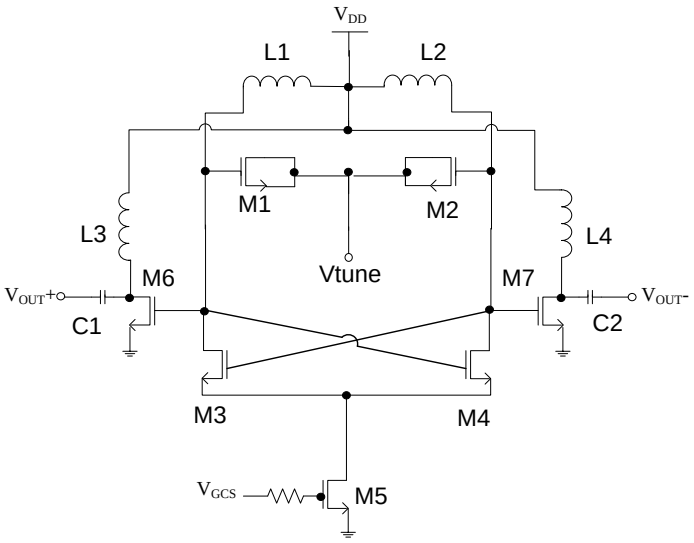


Figure 39 Schematic of a LC-VCO

Transistor M1 and M2 are used as capacitors. The drain and source terminal are connected to each other and a tuning voltage is applied to that connection. Transistor M3 and M4 are a NMOS cross-coupled pair of the VCO. The transistor M5 provides the bias current. Transistor M6 and M7 are used as a buffer and they produces the output signal

There are many important parameters used to show the performance of the VCO. Phase noise and power consumption are chosen to evaluate the performance of LC-VCO in this paper. Normally, phase noise (L) is characterized by the ratio of phase noise power compared to the signal power. In general, larger signal can be achieved by increasing the core current at the cost of larger power consumption. The output voltage swing of LC oscillator is limited by the saturation conditions of the cross-coupled transistors. When this saturation condition is met, a further increase of the core current will have no effect.

The phase noise of the VCO can be derived as

$$L = \frac{4FkTR}{V_o^{\,2}}\left(\frac{\omega_o}{2Q\omega_m}\right)^2 \qquad (25)$$

where F is the noise factor, k is the Boltzman constant, ω_o is the carrier center frequency, ω_m is the carrier offset frequency, T is temperature, R is output resistor, Q is the resonator and Vo is the output voltage. The noise factor (F) of the VCO is given by

$$F = 2 + \frac{8\gamma RI_{bias}}{\pi V_o} + \frac{8\gamma g_m R}{9} \qquad (26)$$

where γ is the noise factor of single transistor and g_m is the transconductance.

The sensitivity of the LC-VCO can be examined. The process variation and the aging effect may degrade the VCO performance. The Phase noise variation is modeled by the fluctuation of g_m and bias current drift as

$$\Delta F = \frac{\partial F}{\partial g_m}\Delta g_m = \frac{\partial F}{\partial g_m}\left(\frac{\partial g_m}{\partial V_T}\frac{\partial V_T}{\partial I_{bias}} + \frac{\partial g_m}{\partial \mu_n}\frac{\partial \mu_n}{\partial I_{bias}}\right)\Delta I_{bias} \qquad (27)$$

where u_n is the mobility and V_T is the threshold voltage.

Expanding the partial derivatives in (27) the phase noise variation can be written as

$$\Delta F = \frac{\gamma 8R}{9}\left\{\frac{I_{bias}}{(V_{GSOSC}-V_T)^2}\frac{L}{\mu_n C_{ox} W_{CS}(V_{GSCS}-V_T)}+\frac{I_{bias}}{\mu_n(V_{GSOSC}-V_T)}\frac{2L}{C_{ox}W_{CS}(V_{GSCS}-V_T)}+\frac{9}{\pi V_o}\right\} * \Delta I_{bias} \quad (28)$$

where C_{ox} is the oxide capacitance per unit area, L is the channel length and W is the channel length of the current source transistor, V_{GSOSC} is the gate-source voltage to the cross coupled transistor, and V_{GSCS} is the gate-source voltage to the current source transistor.

Eq. (28) accounts for process variations and aging effect of the mixer.

6.3 Invariant Current Source

It is clear from (28) that the VCO performance is dependent on the drain current of current source. To maintain the mixer performance, the drain current of M5 has to be kept stable. Thus, process invariant current source circuit shown in Figure 40 is employed. In Figure 40 drain currents of M8 and M9 are designed the same. Changes in M8 and M10 drain currents are negatively correlated to remain a stable bias current (I_{D8} + I_{D10}). For example, if the process variation increases the threshold voltage, but decreases the drain current of M8, the gate voltage of M10 increases (V_{G10} = V_{DD} – I_{D9}R). Thus, the drain current of M10 increases to compensate the loss of I_{D8}.

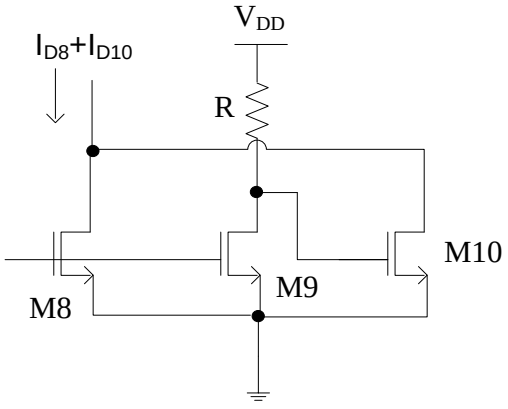


Figure 40 Process insensitive current source

6.4 Simulation Results

ADS simulation is used to compare the VCO performance using the single transistor current source versus process invariant current source. The RF VCO is operated at 2.4 GHz. The output spectrum is shown in Figure 41. The output spectrum of the VCO is very peaked near the oscillation frequency (2.4GHz).

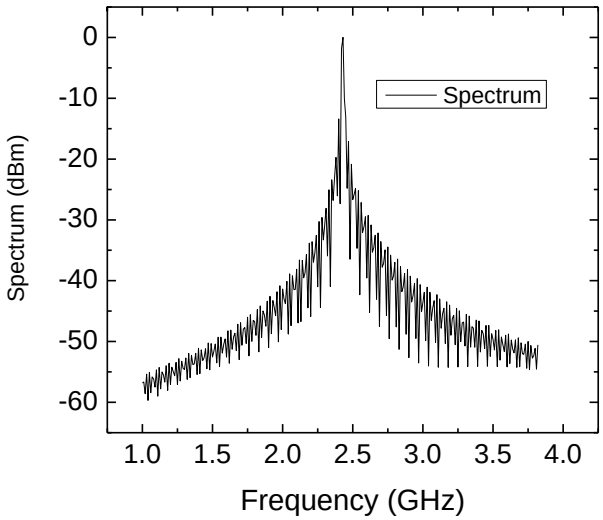
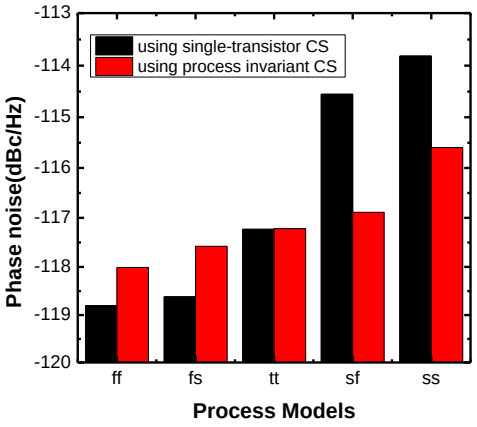


Figure 41 The output spectrum

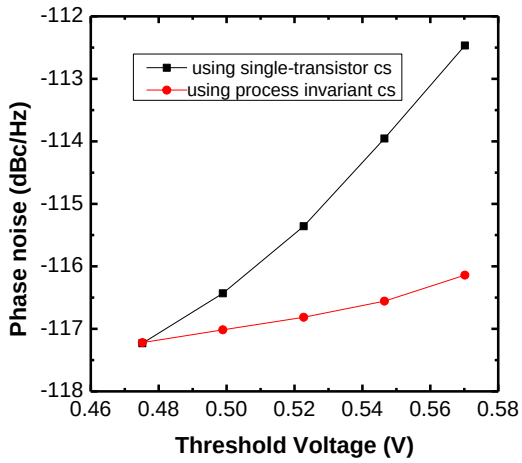
In the circuit design, CMOS 0.18 µm mixed-signal technology node is used. L1 to L4 are chosen at 2nH. The transistor channel widths of M1 and M2 are 696 µm. The channel widths of M3 and M4 are 128 µm. The channel width of M5 is 300 µm. The channel widths of M6 and M7 are 48 µm. The gate resistor size of the current source is 200 Ω. The mixer sets the gate biasing voltage at the current source at 0.9 V. In the current source, the transistor M8 and M9 match each other as 100 µm. The width of M10 is 600 µm. The supply voltage V_{DD} is 1.8 V. The tuning voltage is 0.5 V.

For the process variation effect, the phase noise of the VCO is evaluated at 1MHz offset frequency using different process corner models and variable resistance due to inter-die variations. One naming convention for process corner models is using two-word designators, where the first word refers to the N-channel MOSFET (NMOS) corner, and the second word refers to the P channel (PMOS) corner. In this naming convention, three corner models exist: typical, fast and slow. Fast and slow corners exhibit carrier mobilities that are higher and lower than normal, respectively. The simulation result of the (ff), (ss), (sf), (fs), and (tt) is shown in Figure 42(a). It is clear from Figure 42(a) that the VCO with the invariant current source shows robust phase noise against different process variations.

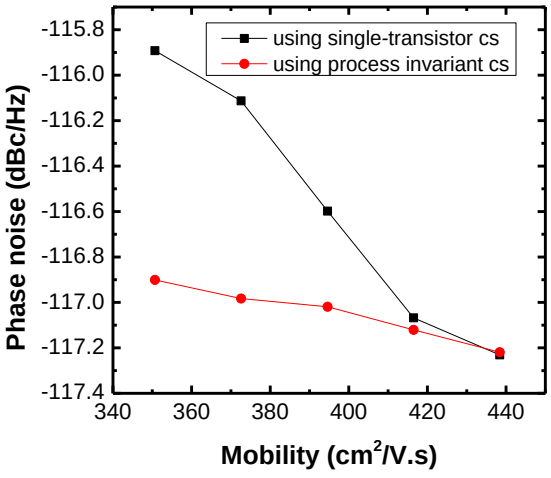
The phase noise gain is also evaluated using different threshold voltage and mobility degradations resulting from aging (hot carrier effect) as shown in Figs. 42(b) and 42(c). The hot-carrier injection increases the threshold voltage, but decreases the electron mobility. The phase noise increases with an increased threshold voltage or decreased mobility due to reduced transconductance. Again, the VCO with process invariant current source exhibits more robust performance against threshold voltage increase and mobility degradation.



(a)



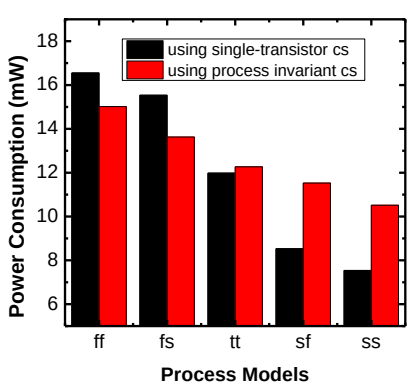
(b)



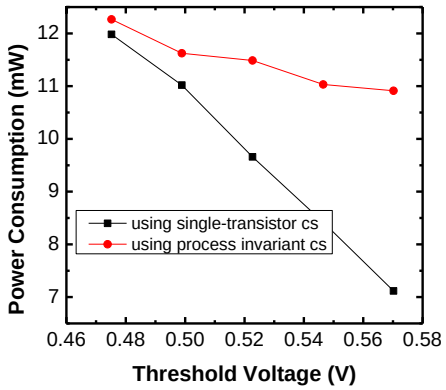
(c)

Figure 42 (a) Phase noise by different process models (b) Phase noise versus threshold voltage (c) Phase noise versus electron mobility

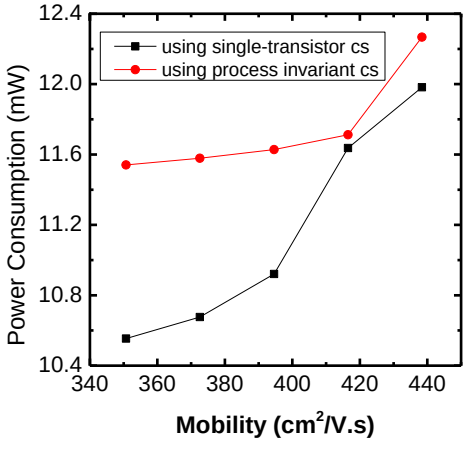
In addition, the power consumption of the VCO using the process invariant current source is compared with that using the single transistor current source. The power consumption versus different process models is displayed in Figure 43 (a). It is clear from Figure 43(a) that the power consumption is more stable over different corner models for the mixer using the current invariant current source. The power consumption also shows less threshold voltage and mobility sensitivity as evidenced in Figure 43(b) and 43(c). In Figure 43(b) and 43(c) the power consumption decreases with increased threshold voltage and decreased mobility due to reduced drain current and transconductance in the VCO.



(a)



(b)



(c)

Figure 43 (a) Power consumption predicted using different process models (b) Power consumption versus threshold voltage (c) Power consumption versus electron mobility

6.5 Monte Carlo Simulation

To further examine the process variation and reliability impact on RF LC-VCO, Monte-Carlo (MC) circuit simulation has been performed. In ADS the Monte-Carlo simulation assumes statistical variations (Gaussian distribution) of transistor model parameters such as the threshold voltage, mobility, and oxide thickness. In the Monte-Carlo simulation a sample size of 1000 runs is adopted. Figure 44 (a) and 44 (b) display the histograms of phase noise using single transistor current source (traditional) and using the process invariant current source (after compensation). For the mixer using the traditional current source, the mean value of phase noise is -117.06 dBc/Hz and its standard deviation is 1.48%. When the process invariant current source is applied, the mean value of phase noise changes to -117.29 dBc/Hz and its standard deviation reduces to 0.34%.

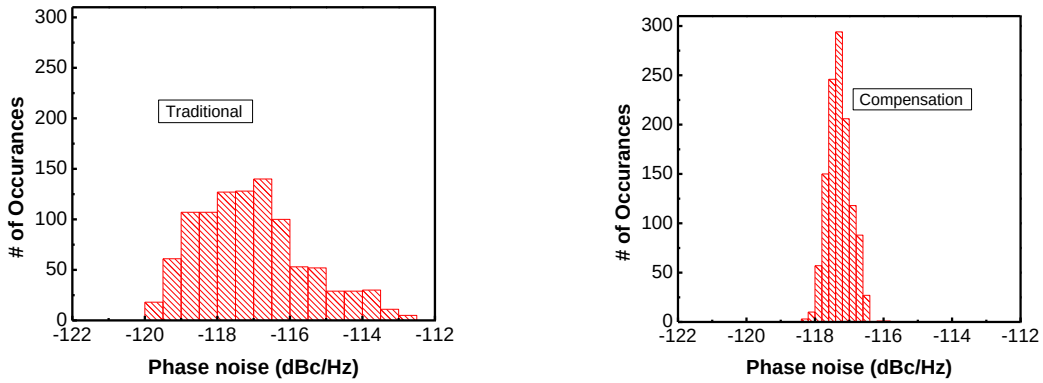


Figure 44 (a) Phase noise statistical distribution without compensation (b) Phase noise statistical distribution after process compensation effect

6.6 Summary

Semiconductor process variations and hot electron reliability on the LC-VCO performance have been evaluated using different process models and key model parameters such as threshold voltage and mobility. The phase noise and power consumption show robust performance for the VCO using the process invariant current source compared to that using the traditional single transistor current source. Monte-Carlo simulation demonstrates that the standard deviation of phase noise reduces from 1.48% to 0.34% while their relative mean values remain the same.

CHAPTERSEVEN：CONCLUSIONS

7.1 Accomplishments

In this work, a class F power amplifier at 5.8 GHz was designed and analyzed. Its pre-layout and post-layout performances were compared. Post-layout parasitic effect decreases the output power and power-added efficiency. Physical insight of hot electron impact ionization and device self-heating was examined using mixed-mode device and circuit simulation to mimic the class F PA operating environment. The output transistor had larger impact ionization rates and self-heating due to larger power dissipation and higher drain electric field than those of the input transistor. Hot electron effect increased the threshold voltage and decreased the electron mobility of the n-channel transistor, which in turn decreased the output power and power-added efficiency of the power amplifier, as evidenced by the RF circuit simulation results. The device self-heating also reduced the output power and power-added efficiency of the PA.

The PVT compensation of power amplifier using a current-source as an on-chip sensor was presented. The adaptive body bias design using current sensing made the output power and power-added efficiency much less sensitive to process, supply voltage, and temperature variations, predicted by derived analytical equations and verified by ADS circuit simulation results.

Process variations and hot electron reliability on the mixer performance were evaluated using different process models and key model parameters such as threshold voltage and mobility. The conversion gain, noise figure, and output power showed robust performance for the mixer using the process invariant current source compared to that using the traditional single transistor current source. Monte-Carlo simulation demonstrated that the standard deviation of conversion gain reduced from 3.18% to 2.08%, the standard derivation of noise figure changed from 2.49% to 1.29%, the standard deviation of output power decreased from 3.81% to 2.08%, while their

relative mean values remained the same.

Semiconductor process variations and hot electron reliability on the LC-VCO performance was evaluated using different process models and key model parameters such as threshold voltage and mobility. The phase noise and power consumption showed robust performance for the VCO using the process invariant current source compared to that using the traditional single transistor current source. Monte-Carlo simulation demonstrated that the standard deviation of phase noise reduced from 1.48% to 0.34% while their relative mean values remained the same.

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