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Work Function Extraction of Indium Tin Oxide Used As Transparent Gate Electrode For MOSFET.

Shraddha Nehate
University of Central Florida

WORK FUNCTION EXTRACTION OF INDIUM TIN OXIDE USED AS TRANSPARENT GATE ELECTRODE FOR MOSFET

by

SHRADDHA DHANRAJ NEHATE
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ABSTRACT

Recent commercialization has peaked interest in transparent conducting oxides being implemented in display technology. Indium Tin Oxide (ITO) is a popular transparent conducting oxide which has been utilized as high work function electrode in liquid crystal displays, solar cells, gas sensors and heat reflecting films. Indium Tin Oxide films exhibit excellent transmission characteristics in the visible and infrared spectrum while maintaining high electrical conductivity. High work function electrodes are used to inject holes into organic materials. In majority applications the ITO work function has an impact on the device performance as it affects the energy barrier height at the hetero-junction interface. Hence, the work function of ITO is of critical importance.

In this thesis, the work function of ITO is extracted successfully from a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device for the first time. Two MOSFET devices are fabricated using a four level mask under exact same conditions. Aluminum metal is used as a drain and source contact for both MOSFETs. One of the MOSFET has aluminum gate contact and transparent conducting ITO is used as gate contact for the second MOSFET. From the threshold voltage equation of both the fabricated MOSFETs, work function of ITO is extracted. Further optical transmission studies of ITO performed in the visible spectra are also reported in this study.

This thesis is dedicated to my family. To my mother and grandmother who have shaped my personality in a unique way. To my father who influences me in the best way and has taught me to never give up. To my little brother who constantly motivates me to do better.

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CHAPTER 1: INTRODUCTION

1.1 Motivation

Transparent and conductive films of cadmium oxide (CdO) and Indium Tin Oxide (ITO) were first reported in 1970, and since then the interest in characteristics of these materials have rapidly increased. Non-stoichiometric and doped films of oxides of tin, indium, zinc and cadmium are known to exhibit metallic conductivity and high transmittance [1]. Tin doped Indium Oxide have found found their applications in mechanical, electrical and optical technologies due to their transmittance and conductivity as high as 95% and $10^4\Omega^{-1}cm^{-1}$ respectively

In intrinsic stoichiometric materials, it is difficult to obtain high optical transparency as well as high electrical conductivity. Electron degeneracy is created in a wide bandgap Indium Tin Oxide by converting them to non-stoichiometric composition.These favorable properties along with the transmittance and conductance have made ITO one of the most commonly used Transparent Conducting Oxide (TCO).

Uses of ITO traditionally range from opto-electronic devices [2][3], antistatic coatings for instruments [4], liquid crystal displays [5][6], transparent heating elements to transparent electrodes for display devices [7]. ITO has been used recently for solar cells, LED and photo diodes, photo transistors and lasers as a transparent contact. Emerging technology demands greater understanding of optical, electrical and structural properties of ITO.

ITO thin films can be deposited by various techniques such as RF and DC sputtering [8][9], pulsed laser deposition [10], evaporation [11], chemical vapor deposition [12] and sol-gel deposition techniques [13].

1.2 Aims and Objective

The primary objective of this work was to extract the work function of ITO film deposited as a metal gate for a Metal Oxide Semiconductor Field Effect Transistor (MOSFET). The first step was to fabricate a MOSFET using four level mask. Next a series of experiments were performed to obtain transparent and conductive films of ITO using RF Sputtering. The main goal was to measure the threshold voltage and then calculate work function on completing the entire MOSFET fabrication.

1.3 Layout of Thesis

In this thesis, literature review of ITO is presented in Chapter 2 followed by the deposition techniques used. Chapter 3 describes the operating principle and characteristics of MOSFET. All steps followed to fabricate MOSFETs are described in Chapter 4. Chapter 5 includes results followed by conclusion in Chapter 6.

CHAPTER 2: LITERATURE REVIEW

2.1 Properties of ITO

ITO is an n-type wide band gap semiconductor with high free carrier density and thus exhibits low electrical resistivity. The structure and composition defines the unique properties of ITO. ITO is fundamentally formed due to substitutional doping of indium oxide (In_2O_3) by tin (Sn). Sn replaces the In^{3+} atoms to form cubic bixbyte structure of indium oxide as shown in Figure 2.1. The oxygen anions are positioned at the six corners whereas each cation rests at center of the cube. Major influence in the structural properties of ITO is caused due to two remaining corners of oxygen vacancies. These oxygen vacancies play an important role in the defect chemistry of ITO. These vacancies are at opposite vertexes.

A free electron is achieved when Sn^{4+} replaces an In^{3+} cation. Sn then forms an interstitial bond with oxygen and occurs as SnO or SnO_2 - depending on the valency of +2 or +4 respectively. This valency state has an immediate effect on the conductivity of ITO. +2 valence state implies that a hole is created which acts as trap to reduce conductivity. On the other hand, predominance of SnO_2 implies Sn^{4+} acts as a n-type donor releasing electrons to increase the conductivity of ITO. Hence the non-stoichiometric ITO containing substitutional Sn and oxygen vacancies is represented as $In_{2-x}Sn_xO_{3-2x}$.

The doping level is crucial for electrical properties. With increasing tin concentration the carrier concentration increases until it reaches saturation. Beyond this point the carrier concentration drops.Tin doping of typically 8-10% produces degenrative ITO corresponding to highest carrier concentration and hence lowest resistivity[14]. Beyond this, high tin doping results in neutral Sn:O bonds which do not contribute to electrical conductivity and may also distort the ITO lattice

structure. The grain size of polycrystalline ITO depends on process parameters such as deposition rate and substrate temperature during the deposition process.

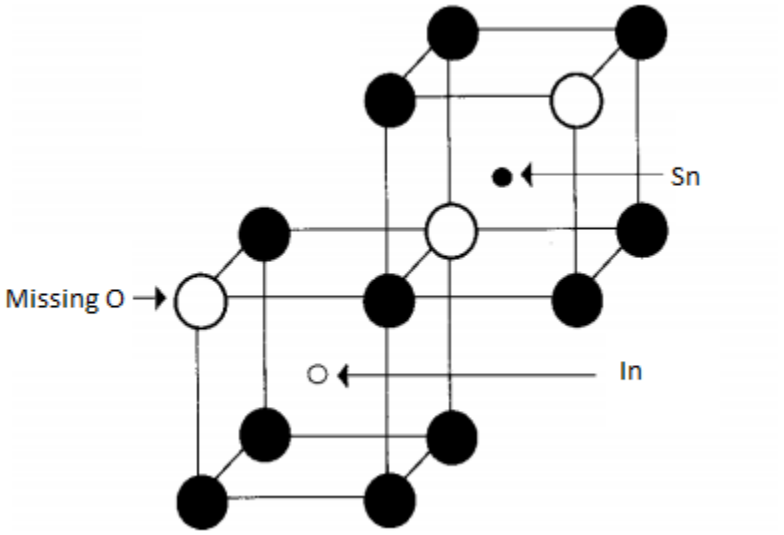

Figure 2.1: Cubic Bixbyite structure of ITO formed by replacing In atom with Sn

Literature reports that the direct optical bandgap of ITO ranges between 3.5 to 4.06 eV [15][16]. Being a wide bandgap semiconductor ITO models high transmittance. The fundamental absorption edge of ITO lies in the ultraviolet region of radiation. With increase in carrier concentration, absorption edge is found to shift towards shorter wavelengths. Figure 2.2 shows the parabolic band structure of ITO. Fermi level is positioned at the middle of undoped In_2O_3. Donor states are formed just below the conduction band when In_2O_3 is doped with Sn. If the doping density is increased these eventually combine with the conduction band. This combining takes place at a critical density of $2.3x10^{19}\ cm^{-3}$ [14]. Conductivity of ITO increases if the the density of Sn atoms increase beyond the critical value. However, if carrier concentration goes beyond the critical density, valence band and conduction band merge resulting in reduction of the bandgap.

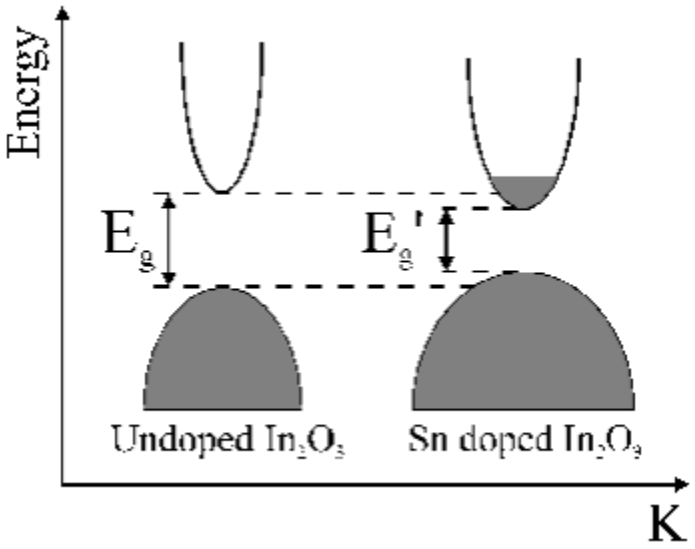

Figure 2.2: Energy Band diagram

The fluctuation of electrical and optical properties of ITO under heat treatment has become crucially significant for its applications. For applications which demand high optically transmitting ITO, it is possible to achieve transmission as high as 91% while retaining conductivity of $1.2x10^3(\Omega cm)^{-1}$. For the use as an infrared mirror, it is possible to control wavelength at which ITO becomes highly refelective, for use in solar cells the location of fermi level can be changed through heat treatments thus regulating the band diagram at interfaces [17].

2.2 ITO Deposition Techniques

Several techniques have been studied and developed to fabricate transparent conducting oxides. Some factors which govern the choice of technique used for depositing ITO are quality and reproducibility of films, homogeneity, cost and availability, as well as drawbacks of each approach. Since the choice of deposition technique influences electrical, optical, morphological and structural

properties, it is certain that each deposition technique will yield films with characteristics different from each other. Thus it is only convenient to use a deposition technique which produces films relevant to properties required for intended application. ITO has been prepared by several techniques as discussed in section 1.1. Sputtering has been by far the most extensively used method for ITO deposition. Sputtering along with other ITO deposition techniques will be discussed briefly in this section.

2.2.1 Sputtering

Sputtering illustrates the knocking of an individual or cluster of atoms from the target material using accelerated ions which are generated by excited plasma. These target atoms or molecules from the eroded material are condensed onto the substrate. Sputtering can be further classified into reactive and magnetron sputtering. A chemical reaction alters the precursor material when the atoms or molecules are transferred from the target to top of the substrate. Various techniques are used to accelerate the plasma ions in sputtering process by DC field, DC field in combination with a magnet, using radio frequency and by ion beams. Depending on the process used, they are named as DC magnetron sputtering and Reactive RF sputtering. RF sputtered ITO films have been reported with transmission of 95%, resistivity of $4X10^{-4}\ \Omega cm$ and Hall mobility of $12cm^2V^{-1}s^{-1}$ [18]. Transmission electron microscopy and electron diffraction studies of RF Sputtered ITO films exhibit amorphous structure due to crystallographic defects. Post annealing ITO films between $200 - 500\,^{\circ}\mathrm{C}$ in vacuum not only improves the crystallinity of films but also enhances the optical and electrical properties [19].

2.2.2 Thermal Evaporation

Thermal Evaporation of ITO involves heating the target material to sufficiently high temperature to vaporize it by means of resistive heating or ion beam. The vapors are condensed on the substrate. Transparent and heat reflecting ITO thin films of $0.4\mu m$ have been deposited using reactive electron beam evaporation displaying 90% transmittance and resistivity of $3x10^{-4}\Omega cm$ in oxygen atmosphere [20].

2.2.3 Spray Pyrolysis

Spray pyrolysis refers to a method of spraying a solution on a heated substrate where the constituents react to form a compound which gets deposited as a thin film. This is one of the famous techniques for coating owing to its low cost and high mass production. The solution droplets generated on the hot substrate can be produced by pressure, nebulizer or ultrasonic methods. To coat ITO thin film on a substrate, the process is employed using alcoholic solution of anhydrous tin chloride $InCl_3$ and tin chloride $SnCl_4.5H_2O$. The spraying takes place in a furnace at $400\,^{\circ}\mathrm{C}$. Nitrogen acts as a carrier gas in this process. Substrate temperature is a critical factor controlling the coating quality. Spray Pyrolysis technique have been able to produce 420nm thin films of ITO with resistivity of $1x10^{-3}\Omega cm$ and transmission greater than 90% [21].

2.2.4 Sol-gel Processing

Sol-gel process defines the evolution of liquid solution towards the formation of a gel-like state . This gel-like structure incorporates morphologies of both discrete particles as well as continuous polymer network. It is a low temperature multi-level processing technique. Low temperature processing allows the use of volatile components and avoid formation of undesired phases. The sol-gel process takes place in three steps : preparation of sol, spray coating on the substrate and then annealing to achieve crystallized thin film coatings. Compared to conventional thin films processing techniques, sol-gel requires less number of equipments and is a cost effective process [22].

2.2.5 Screen Printing

Screen printing technique is implemented in applications such as anti-reflection coatings for solar cell, liquid crystal displays which require relatively thick layer of ITO. Typically the thickness of ITO deposited using Screen Printing Technology can be within range of 10 to 30um. The thick films of ITO are annealed after deposition at higher temperature up to $400\,^{\circ}\mathrm{C}$ to achieve crystallized film. Screen Printing Technique yield films with resistivity comparable to other techniques but transmission has been recorded to be low.

2.3 Work Function Extraction of ITO

Literature reports work function extraction of ITO on glass and silicon. However the work function extraction of ITO from a MOSFET device is successfully achieved in this study for the first time. For a $300A^{\circ}$ ITO film coated on borosilicate glass, the work function is reported to be 4.4 - 4.5eV which is measured in Ultra-high Vacuum (UHV) using ultraviolet photoelectron spectroscopy [23].

CHAPTER 3: MOSFET

3.1 What is MOSFET?

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a special type of Field Effect Transistor (FET) that works as a switching device by electronically varying the channel width carrying charge carriers. MOSFETs can be found at the core of integrated circuit and can be designed and fabricated in a single chip due to their small sizes. The MOSFET is a four terminal device with its terminals being source(S), drain(D), gate(G) and body(B). Commonly the source and the body terminals are connected, thus making the MOSFET look like a three terminal device like FET. MOSFET can be fabricated using metal or polysilicon for gate contact.

MOSFETs can be broadly classified into two types n-channel and p-channel MOSFET depending on the doping of substrate as compared to the source and drain regions. If two highly doped n-regions of source and drain are diffused into a lightly doped p-type substrate the MOSFET is called n-channel MOSFET or NMOS. If the source and drain regions doped with p-type impurity are diffused into a n-type substrate then it forms a p-channel MOSFET or PMOS. The symbols for NMOS and PMOS are shown in the Figures 3.1 and 3.2 respectively. The source and drain regions are connected through the metallic contacts linked by n-channel or p-channel depending on the type of MOSFET used. The gate region is connected to a metal contact surface but it remains isolated from the channel and the substrate through a thin layer of silicon dioxide (SiO_2) dielectric.

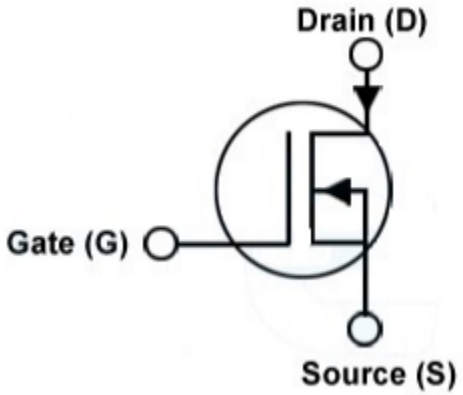

Figure 3.1: NMOS Symbol

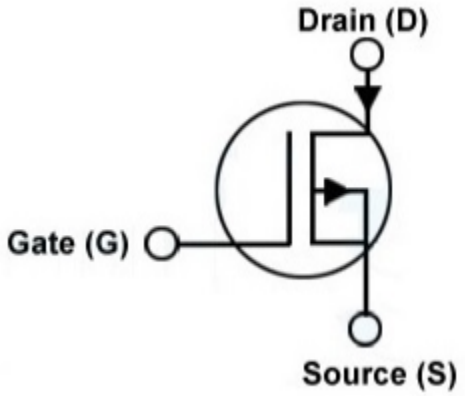

Figure 3.2: PMOS Symbol

3.2 Operating Principle

To understand the working principle of MOSFET, consider the cross section of NMOS shown in Figure 3.3 [24]. In a p-silicon substrate, two n+ regions are formed for source and drain by diffusion. There exists a thin layer of dielectric SiO_2 in between the gate electrode. 'L' is the conducting channel length and 'W' represents the channel width.

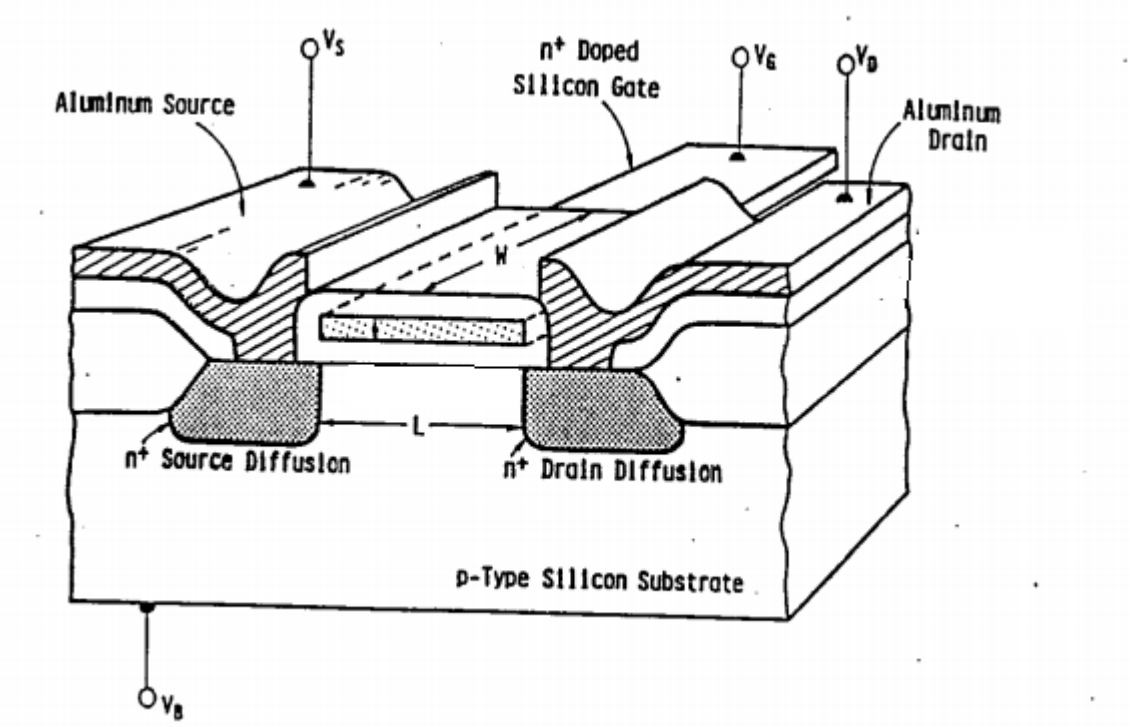

Figure 3.3: N-channel MOSFET Cross Section

The voltage applied to gate electrode controls the current flowing through drain-source channel. When no voltage is applied to gate, there is no conduction present between the n-channel and hence no current flows through the device. This state is called as the OFF state of MOSFET.

Consider what happens when suppose first negative gate voltage is applied with respect to the

substrate. This signifies a negative charge on metal and positive charge at the substrate. The excess positive charge will reside as holes at the semiconductor surface. Due to accumulation of positive charge at the semiconductor surface, the surface is more p-type than the bulk silicon and hence the semiconductor surface is said to be in accumulation mode.

Next consider positive charge is applied to the gate metal. In this situation electric field in the semiconductor is directed away from the surface. Application of positive gate voltage results in repulsion of holes at the $Si - SiO_2$ interface. Hence the surface is depleted of positive charges leaving behind excess of negative charges.There exists a depletion region extending from the semiconductor surface to into the bulk.

As the gate voltage V_G continues to increase, the electrons are attracted at the Si substrate where they are pinned and the holes are swept into the substrate.Eventually the surface of semiconductor becomes strongly n-type due to presence of electrons. The channel has conductivity opposite to that of the substrate and is called as inversion layer.These electrons constitute a drain current. The MOSFET device is considered to be in the ON state now as there exists a channel of electrons between the source and drain. Thus application of positive gate voltage causes an electric field to appear in the substrate, this field causes the mobile charge concentration at the semiconductor surface to vary. The gate voltage required to produce the inversion layer is called as threshold voltage V_T of the MOSFET [25].

Consider a device where source and drain are p-type and the substrate is a n-type . In this case a negative gate voltage large enough to induce a p-type inversion layer at the surface of Si will create flow of holes from source to drain. Such a device is termed as p-channel MOSFET. The current flow between source and drain can be controlled by modulating threshold voltage [26]. For both the types of devices, when gate voltage falls below the threshold voltage, the channel formed between the source and drain regions is lost and MOSFET enters OFF state. Thus, the MOSFET

acts as a switching device.

Energy band diagram identifies the barrier between the metal and semiconductor. Figure 3.4 [27] shows flat-band energy diagram of aluminum metal, silicon dioxide and silicon.

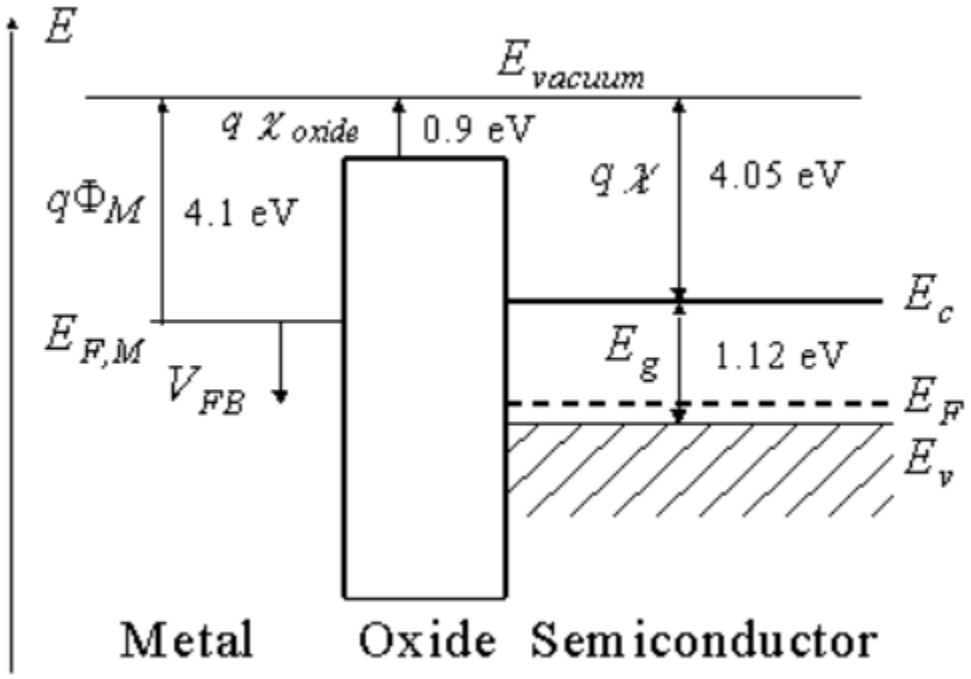

Figure 3.4: Flatband energy diagram of MOS structure consisting of aluminum metal, silicon dioxide and silicon

3.3 I-V Characteristics of MOSFET

In this section, we will discuss about the current-voltage characteristics of MOSFET and its operating regions namely cut-off, linear and saturation region. Consider the transistor is an NMOS device in which the current carrying channel consists of electrons. In contrast, a PMOS device has a current carrying channel of holes induced by a negative gate voltage. The threshold voltage of

MOSFET is given by:

$V_T = -\phi_{ms} + 2\phi_f - \frac{Q_i}{C_i} + \frac{Q_d}{C_i}$ [28].

The key parameters determining V_T are gate oxide thickness, substrate doping,and gate metal.

The threshold voltage equation shows that V_T is a function of dielectric capacitance C_i. Dielectric capacitance is inversely proportional to the gate oxide thickness [29]. Hence we can conclude that $V_T \alpha$ Oxide thickness (d). The thinner the gate oxide, larger fraction of gate voltage will be appearing across the semiconductor which will lower the threshold voltage.

Another principal parameter affecting threshold voltage is the gate metal. In the equation above, $\phi_{ms} = \phi_m - \phi_s$ Where ϕ_m is the work function of gate metal and ϕ_s is the work function of silicon substrate. This implies by changing the gate metal of MOSFETs, the work function will vary and so threshold voltage can be varied too. Ion implantation is another parameter affecting V_T. Depletion charge Q_d of the MOSFET can be controlled by ion implantation for the drain and source regions, hence the threshold voltage can be controlled by ion implantation.

As shown in Figure 3.4, the MOSFET has three regions of operations.When the gate voltage V_g is less than the threshold voltage defined in the equation above, no inversion layer is formed and hence drain current is zero. This segment of characteristics that coincides with the drain voltage axis V_{DS} is called as cut-off as seen in Figure 3.4. In the cut-off region, the structure between the drain and source forms two back to back junction diodes so the current for any voltage V_{DS} is zero.

For the linear and saturation regions of MOSFET, gate voltage greater than threshold voltage induces an inversion layer at the semiconductor surface by capacitor action. If drain voltage V_{DS} is zero, lateral electric field required for the flow of current along the channel is absent and thus I_D is zero. On application of V_{DS} the drain current starts to flow. This region of MOSFET operation is known as linear region. This process continues as V_D is increased, causing increase in I_D until

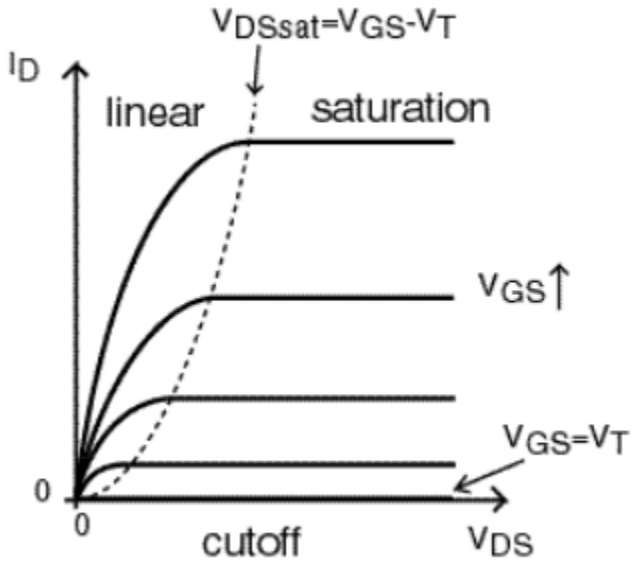

Figure 3.5: I-V Characteristics of MOSFET

the point is reached where increase of V_D culminates in pinch-off at the drain end where electron density in the channel has become zero. The value of drain voltage at which pinch-off occurs is called as saturation voltage (V_{DSat}). At this point the linear region terminates.

When the MOSFET is ON implying V_G is greater than V_T and drain voltage V_D is greater than V_{DSat} the device is said to enter saturation region. Increasing V_G results in increase in channel density, but after pinch-off the current remains constant.

CHAPTER 4: METHODOLOGY

For work function extraction of Indium Tin Oxide, two sets of MOSFET were fabricated simultaneously under same process conditions. Aluminum was used for source and drain metal contacts. One of the MOSFETs had aluminum as gate metal and the other MOSFET employed Indium Tin Oxide as gate contact metal. This chapter describes comprehensive details of the steps used in fabricating both MOSFETs.

4.1 Type of Silicon Used

A p-type 3" diameter silicon wafer was used to fabricate MOSFETs. The wafer was cut into 4 equal pie shaped pieces. Two out of four pieces were used to fabricate different MOSFETs, one with Aluminum gate contact and the other with ITO gate contact. The silicon wafer specifications are mentioned in the table below.

bbb

Table 4.1: Silicon Specifications

Type	p
Thickness	500-550μ
Resistivity	1-10 ohm-cm
Orientation	100

4.2 Cleaning Procedure

The p type silicon substrates were initially scrubbed with Alconox detergent and then rinsed using De-ionized(DI) water. This ensures removal of bulk contaminants on the silicon surface. Silicon

samples are cleaned to remove particulate matter on the surface as well as traces of ionic, organic and particulate impurities. The samples were then treated with trichloroethane (TCE) to remove any possible contamination left. This was followed by treating the samples with acetone to remove any residue of TCE, methanol to remove any residue of acetone and finally DI water. There is always some native oxide present on the samples which will add to the parasitic capacitance value. Hence, the samples are dipped in Buffer Oxide Etch (BOE) for 10 seconds, rinsed with DI water and blow dried with N_2 gun.

4.3 Initial Field Oxide Formation

The field oxide of silicon is fundamentally grown for masking pattern of drain and source wells. Thick layer of $4500A^\circ$ or more should be grown in order for the field oxide to act as a mask for confined phosphorus diffusion. Wet oxidation was performed at $1100\,^\circ\mathrm{C}$ for 45 minutes in Model MB-71H of *Thermco Mini-Brute furnace* shown in Figure A.1. Nitrogen pressure was maintained at 5 psi at a flow rate of 1. Nitrogen is introduced inside the furnace through steam bubbler. The steam bubbler was maintained at $98\,^\circ\mathrm{C}$.

The wafers were then loaded onto a quartz boat and the boat is fed at the mouth of furnace. The quartz boat is then slowly pushed to the center of furnace where the temperature is maximum. The push time and pull time for quartz boat was 3 minutes each in order to avoid thermal shock to silicon samples.

Figure 4.1: Silicon Substrate Cross Section after Gate Oxidation

Figure 4.1 shows the silicon substrate after initial field oxidation. After oxidation of 45 minutes, the samples were removed from the furnace and the wafer color was noted to be violet. Violet colors corresponds to $4700A^\circ$ thickness according to the silicon dioxide color chart.

4.4 Mask Level One-Negative Photoresist Process

The first level mask was used to make wells for source and drain. Phosphorous deposition needs to be confined to the drain and source region, first level mask will create wells cutting through the layer of oxide reaching the top surface of silicon. Figure 4.2 shows the level one mask design. Negative photoresist (PR) NR9-1500 was spin coated by high speed whirling of silicon samples. The substrate was coated with the mentioned PR onto a spinner for 30 seconds at the speed of 3000 rpm.

On evenly coating the PR on top of the substrate, the wafer was then baked inside a Blue M oven kept at $150\,^\circ\mathrm{C}$ for 1 minute. This process of heating for 1 minute after application of PR to the substrate is called as Soft Baking. Soft baking ensures maximum adhesion of resist to substrate and residual solvents and components are removed by evaporation. Next the wafers were loaded in *Karl Suss Mask Aligner MJB3* model for ultra violet exposure. Figure A.3 shows the *Karl Suss*

Mask Aligner MJB3. Mask alignment is one of the most important steps in photolithography. A mask is a glass plate with patterned emulsion of metal film on one side. The mask was loaded into mask aligner, the substrate were placed onto the chuck one at a time and on hard contact of mask and substrate, the substrate was exposed to UV light for a duration of 10 seconds.

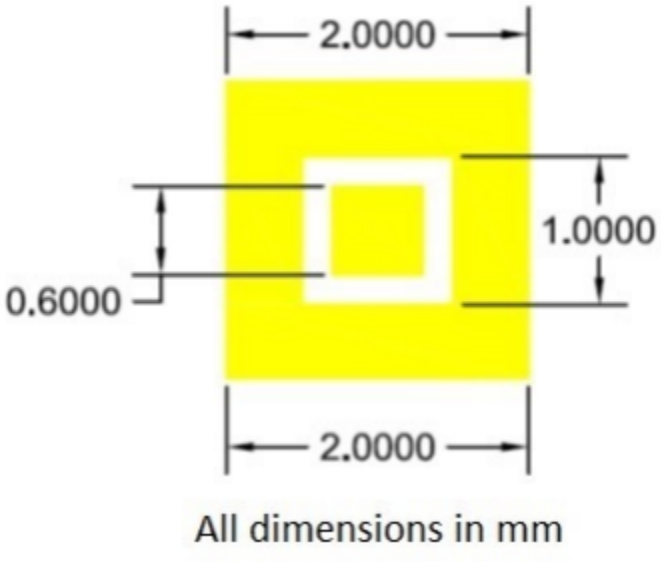

Figure 4.2: Level One Mask Design

After UV exposure the wafers were again heated in another oven maintained at $100\,^{\circ}\mathrm{C}$ for 1 minute. This step is called as post exposure baking. Next the PR was developed in a petri dish containing RD6 PR developer for 30 seconds and then rinsed with DI water and dried by nitrogen spray gun. Developing PR ensures that PR is removed from the areas unexposed to the UV light and remain only in the areas which were exposed to UV light.It in critical to check under microscope if PR has been developed properly.

The final step of photolithogrpahy is hard baking. The wafers were heated at $150\,^{\circ}\mathrm{C}$ for 3 minutes in an oven. After hard baking the wafers were now ready for drain and source well oxide etch.

4.5 Drain and Source Well Oxide Etch

In the photolithography stages, required pattern was obtained on the substrate. Next step was to open windows through the layer of silicon dioxide to reach the top of silicon surface. Buffer Oxide Etch (BOE 6:1) was used to etch through silicon dioxide. BOE is a mixture of 40% ammonium fluoride and hydrofluoric acid in the ratio 6:1. BOE does not attack photo resist and is preferred for patterned etching of oxides. BOE used has an etching rate of $900A^\circ$. The field oxide was around $4700A^\circ$ and thus it took around 5 minutes to etch the oxide and reach silicon top surface. Figure 4.3 shows the substrate cross section after oxide etch. Once the etching was completed, the PR was stripped from the wafers by rinsing with acetone.

Figure 4.3: Substrate Cross Section after First Mask And Oxide Etch

4.6 Phosphorous Predeposition and Drive In

Source and drain wells need to be diffused with phosphorus, which is a n-type dopant. For predeposition step, the samples were loaded onto a quartz boat facing phosphorous sources. The quartz boat was fed into furnace with push and pull times of 1 minute each. Phosphorous predeposition occurs at $950\,^\circ\mathrm{C}$ at a nitrogen pressure of 5 psi and flowrate of 4 sccm in the flowmeter. The wafers were kept inside the furnace for 15 minutes. Figure A.2 shows the furnace used for phosphorus dif-

fusion. The predeposition step ensures the deposition of n-type dopant into drain and source wells. The control wafer was checked for majority carriers and sheet resistance. These dopants however needed to be further driven inside the silicon substrate, which was achieved through Drive-In step.

The drive in step was basically wet oxidation in a furnace at $1100\,^{\circ}\mathrm{C}$, 5 psi nitrogen pressure, flowrate of 1 sccm on flowmeter at bubbler temperature $98\,^{\circ}\mathrm{C}$. The push and pull times were 3 minutes each and the samples were retained inside the furnace for 20 minutes. Figure 4.4 shows the substrate cross section after phosphorus diffusion and drive in. An oxide thickness of approximately $3500A^{\circ}$ was formed on the substrates during drive in.

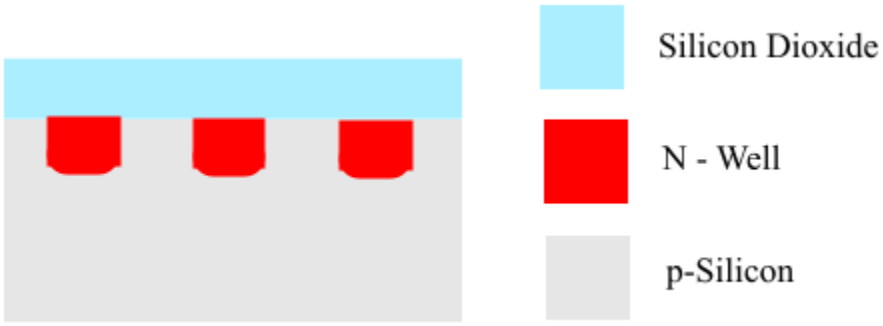

Figure 4.4: Substrate Cross Section after Phosphorus Pre-Deposition and Drive-in

4.7 Mask Level Two-Negative Photoresist process

The second level mask shown in Figure 4.5 was used to create window in the PR for via hole etching. Second level mask photolithography process was carried out in the similar manner to that of first level masking. The substrate was spun coated with negative PR as before and then soft baked at $150\,^{\circ}\mathrm{C}$ for 1 minute. The second level mask was aligned precisely on the top of first level on the substrates in Karl Suss Mask Aligner. After UV exposure, the substrates were

baked at $100\,^{\circ}\mathrm{C}$ for 1 minute. The PR was developed in RD6 developer and examined under the microscope. Further the substrates were hard baked at $150\,^{\circ}\mathrm{C}$ for 3 minutes.

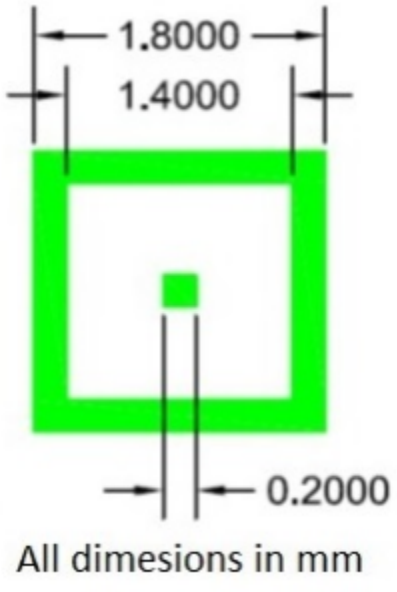

Figure 4.5: Level Two Mask Design

4.8 Via Hole Oxide Etch for Contact Windows

The via hole oxide etch was performed to reach the n-wells of source and drain regions. This process is similar to the field oxide etch. Total etch time for the via hole oxide etch was calculated to be 4 minutes to etch thickness of $3500A^\circ$ which was formed in the drive in step. Once clean edges were achieved, PR was striped with acetone, followed by methanol and DI water. Figure 4.6 shows the silicon substrate cross section after via hole oxide etch.

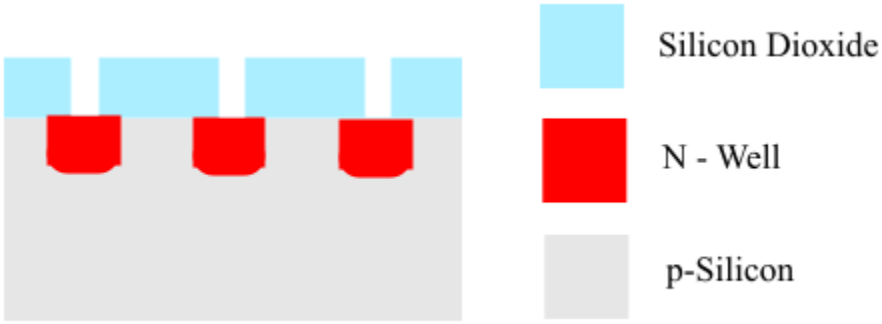

Figure 4.6: Substrate Cross Section after Second Mask and Via Hole Oxide Etch

4.9 Source and Drain Contact Metallization

After creating the via holes, metal contacts needs to be deposited for the drain and source regions. Aluminum was used as contact material for source and drain regions. Figure 4.7 shows aluminum deposited on the silicon substrate. An aluminum wire of approximately 1.5cm long was thermally evaporated at pressure of $2x10^{-5}$ Torr.

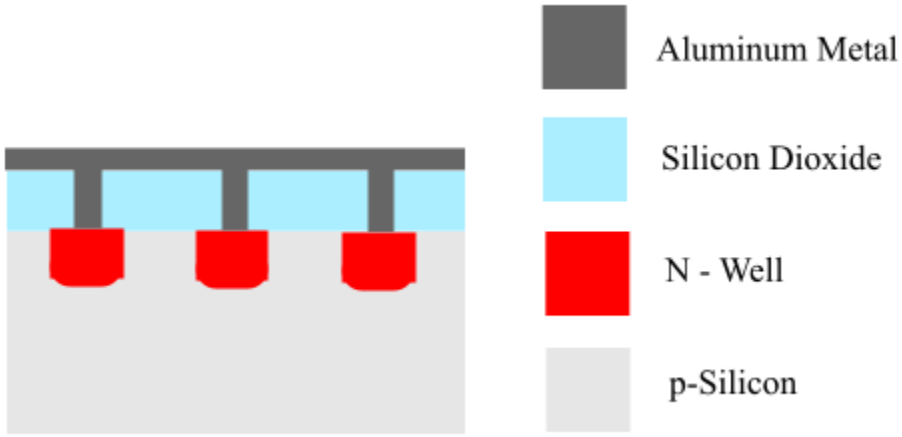

Figure 4.7: Substrate Cross Section after Aluminum Thermal Evaporation

4.10 Mask Level Three-Positive Photoresist process

The aluminum metal that was deposited in the previous stage needs to be patterned, which was achieved through third level mask shown in Figure 4.8. Positive photolithography was used for third level mask. The PR used was Shipley 1813. On coating the samples with positive PR, the samples were spun at 3000 rpm for 30 seconds. The samples were then soft baked at $100\,^{\circ}\mathrm{C}$ for 3 minutes. Third level mask was then accurately aligned with the previous levels on the substrates in *Karl Suss Mask Aligner*. The substrate was then exposed to UV light for 10 seconds to imprint

the mask onto sample. The PR was developed in Shipley CD-26 developer solution for 30 seconds and then rinsed with DI water. The mask pattern was checked under microscope to ensure all the PR was removed before it was hard baked in an oven at $100\,^{\circ}\mathrm{C}$ for 10 minutes.

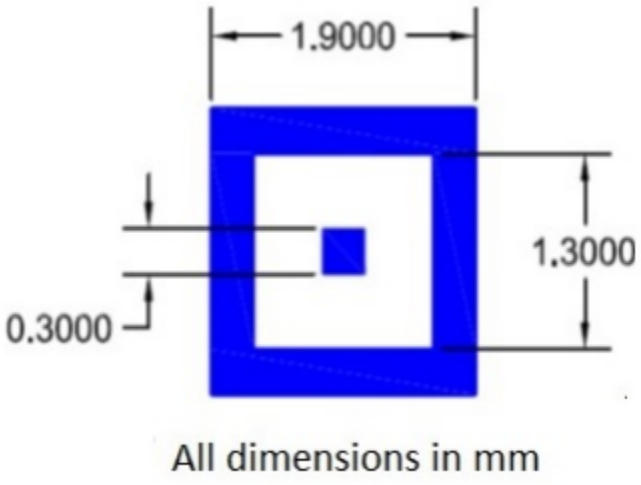

Figure 4.8: Level Three Mask Design

4.11 Source and Drain Contact Patterning

Source and Drain aluminum metal contact was patterned through process of etching. Aluminum etch solution which is composed of 16 parts of phosphoric acid, 1 part of acetic acid, 1 part of nitric acid, and 20 parts of DI water was used at $35\,^{\circ}\mathrm{C}$ to etch aluminum. The etcing process was continued till the time all the aluminum was visibly removed from the areas which were not protected by the PR. The time can vary depending on the metal thickness. When all the unprotected aluminum was etched, the PR was stripped using acetone,methanol, rinsed with DI water and dried with N_2 gas. Figure 4.9 shows silicon cross section of patterned aluminum for drain and source contacts.

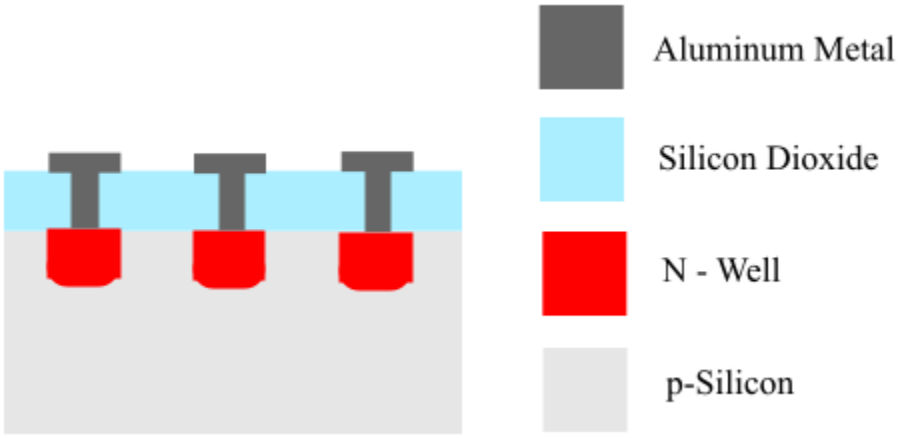

Figure 4.9: Substrate Cross Section after Source and Drain Contact Patterning

4.12 ITO Gate MOSFET Fabrication

The four level mask is specifically designed to deposit gate electrode of a different metal than the gate electrode of source and drain. All the above steps till source and drain contact patterning were followed for fabricating both the samples. Next ITO was to be deposited on the substrate as a gate metal for one of the MOSFETs. The next sections define how ITO was sputtered using mask level four.

4.12.1 Mask Level Four for Lift Off-Negative Photoresist process

Indium Tin Oxide that was used as the gate contact is composed of 90% In_2O_3 and 10% SnO_2 in weight. The level four mask shown in the Figure 4.10 was performed using negative photolithography with NR9-1500 PR. The substrate was spun coated with this PR at 3000 rpm for 30 seconds.

With PR on it, the sample was soft baked inside an oven at $150\,^{\circ}\mathrm{C}$ for 1 minute. In Mask aligner, the fourth level mask was aligned with all the previous levels accurately and then the sample was

exposed to UV light for 10 seconds.

The sample was inserted into another oven maintained at $100\,^{\circ}\mathrm{C}$ for 1 minute for post exposure baking. Now the PR was ready to be developed. The sample was dropped in a petri dish containing RD6 developer solution for 30 seconds and then rinsed with DI water. The sample was checked for proper PR developing and then hard baked in an oven at $150\,^{\circ}\mathrm{C}$ for 1 minute. The PR was going to be lifted off and hence hard baking was performed only for a minute.

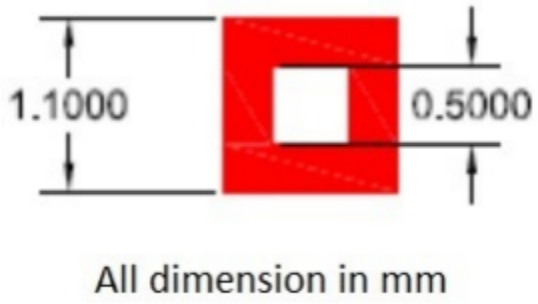

Figure 4.10: Level Four Mask Design

4.12.2 ITO Sputtering for Gate Contact

The gate oxide, in this case ITO was to be deposited next for gate contacts. As discussed previously ITO can be deposited using several techniques. In this study, ITO was deposited on the substrate using Radio Frequency (RF) magnetron sputtering. The target used for sputtering process was 2" in diameter.

ITO deposition was performed in a AJA Six Gun Sputtering system at a pressure of 4 milli-Torr and RF current of 100 W. The argon flowrate was kept constant at 25 sccm in the flowmeter. Sputtering

was implemented for about 30 minutes which resulted in an ITO film on the substrate of thickness equal to $1500A^\circ$ shown in Figure 4.11. The ITO thickness was measured using *Veeco Dektat 150 Profilometer* shown in Figure A.5.

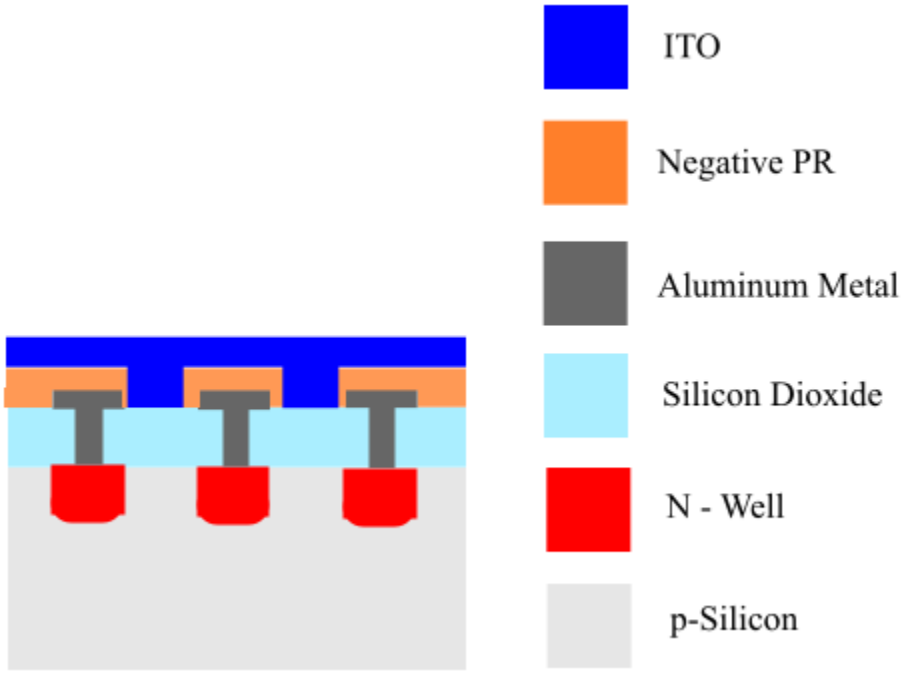

Figure 4.11: Substrate Cross Section After ITO Sputtering

4.12.3 Gate Patterning of ITO by Lift off

After ITO was sputtered on the substrate, next step was to lift off the PR and pattern ITO only to be confined to the gate region. Even though hard baking was performed for only 1 minute, prolonged high temperature exposure of substrate during sputtering increased the adhesiveness of PR. For lifting off process, the sample was immersed in concentrated sulfuric acid (H_2SO_4) which dissolves the PR and leaves ITO only confined to gate metal contact. Figure 4.12 shows the final cross section of ITO gate electrode MOSFET.

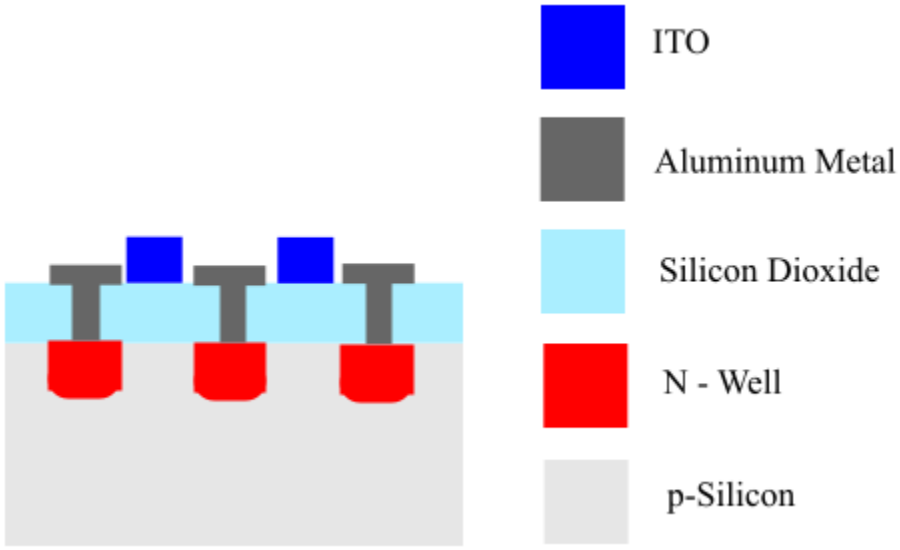

Figure 4.12: Cross Section of ITO Gate Contact MOSFET

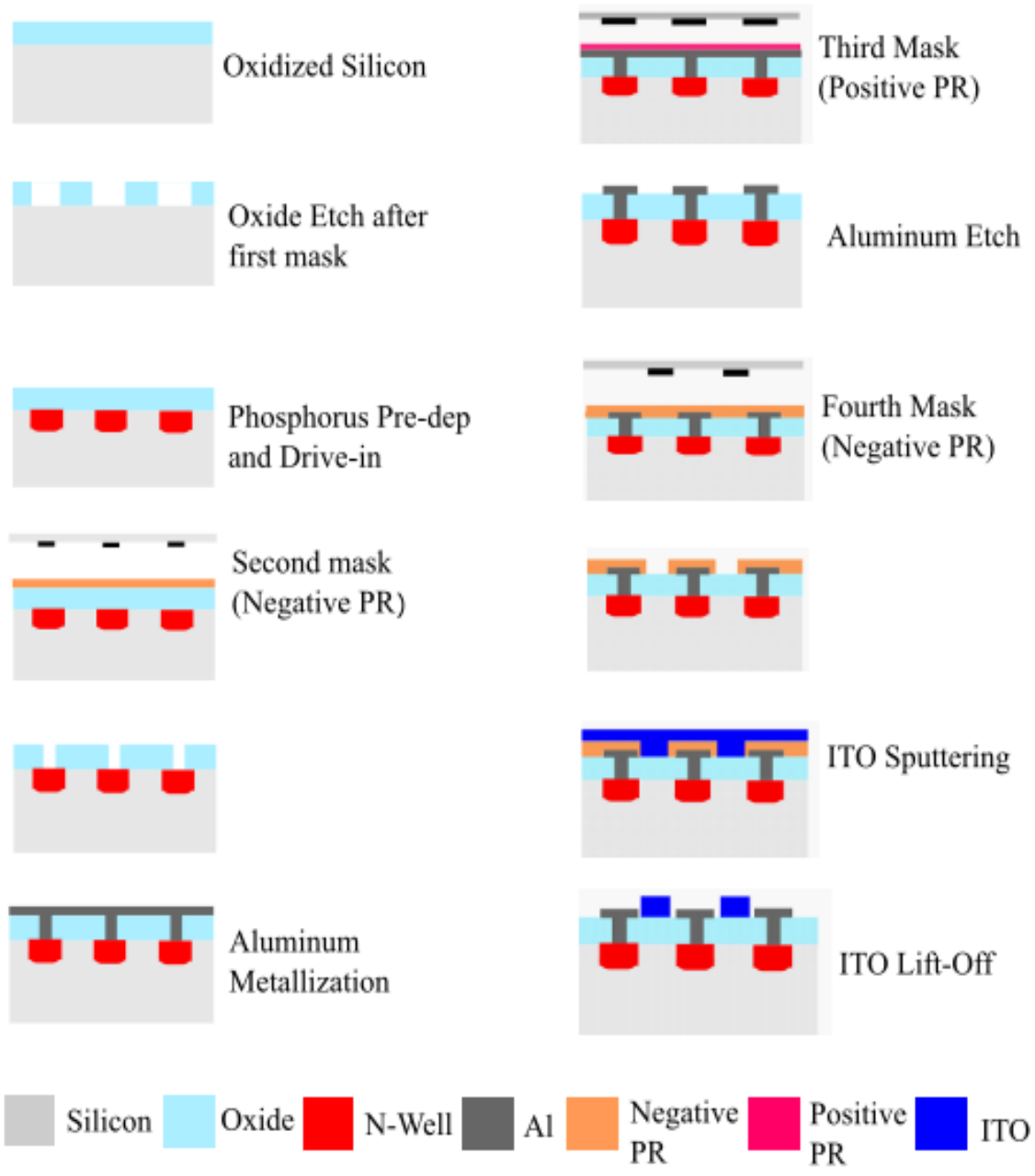

Figure 4.13: Fabrication Steps of ITO Gate MOSFET

4.13 Al Gate MOSFET Fabrication Steps

All the steps until source and drain contact patterning were followed for the sample which was to have aluminum as gate contact. Next using the fourth level mask, the sample was coated with aluminum gate metal. So now we had two substrates, one with aluminum gate metal and the other with ITO gate metal. Both the devices have aluminum source and drain contact regions which we have already discussed in the previous sections. In this section, we will discuss the metallization procedure for the device with aluminum as gate contact.

4.13.1 Mask Level Four-Negative Photoresist process

After patterning the source and drain contacts, negative photoresist process was followed in the exact same manner as that of mask level three. Spin coating negative PR, soft-bake, UV-exposure, post exposure bake, developing the film and hard bake. Figure 4.14 shows the substrate cross section after UV exposure and PR developing.

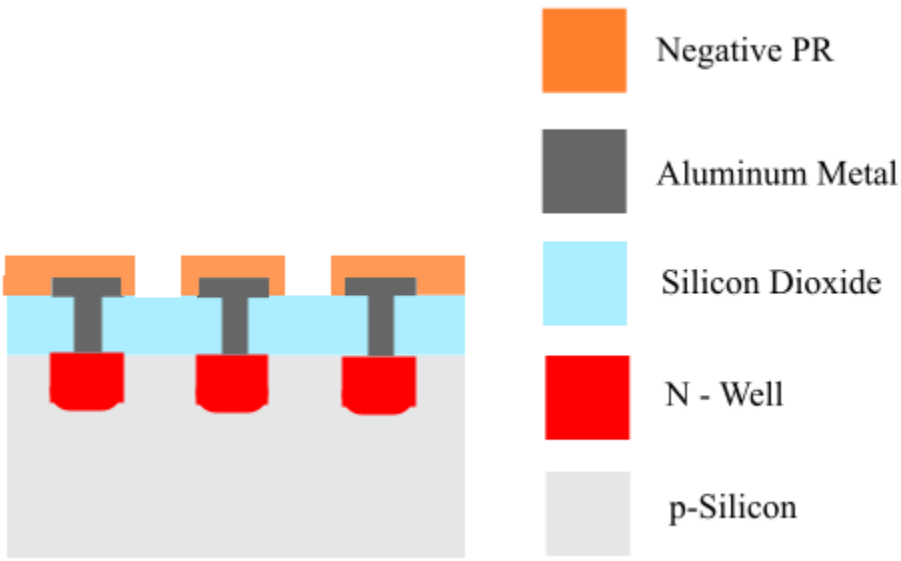

Figure 4.14: Mask Level Four after UV Exposure and PR Developing

4.13.2 Aluminum Deposition for Gate Contact

After hard bake, aluminum was deposited on the top of PR using thermal evaporation similar to as discussed in section 4.1.9. The substrate cross section after aluminum thermal evaporation is shown in Figure 4.15.

4.13.3 Gate Patterning of Aluminum by Lift-Off

In this final step, lift-off process was used to remove deposited aluminum from regions other than the gate electrode. The negative PR below the aluminum was striped using Sonicator. The substrate was immersed in acetone and placed in a petri dish. The petri dish is placed on a bath of water. Ultrasonic vibrations lifted off the PR producing the gate electrodes with clear edges. Figure 4.16 shows final cross section of aluminum gate electrode MOSFET.

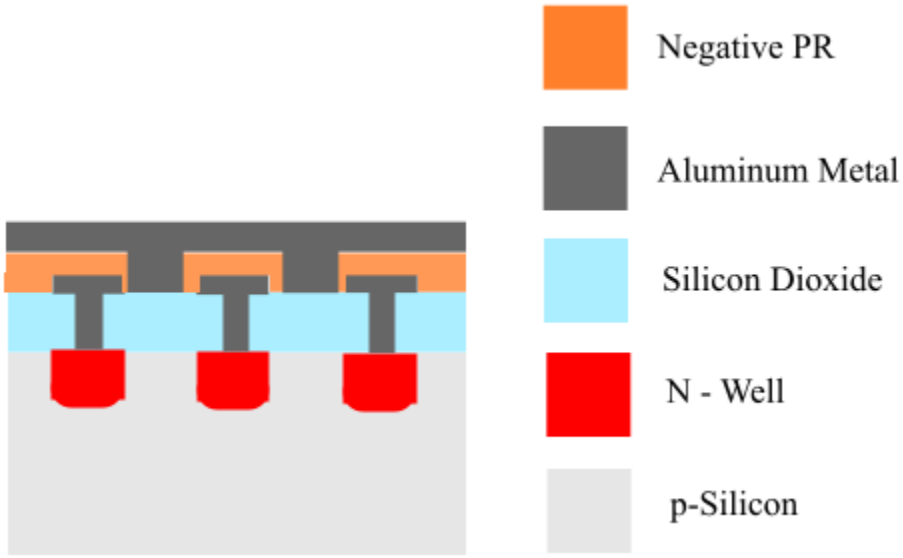

Figure 4.15: Cross Section of MOSFET of Al Deposition by Thermal Evaporation

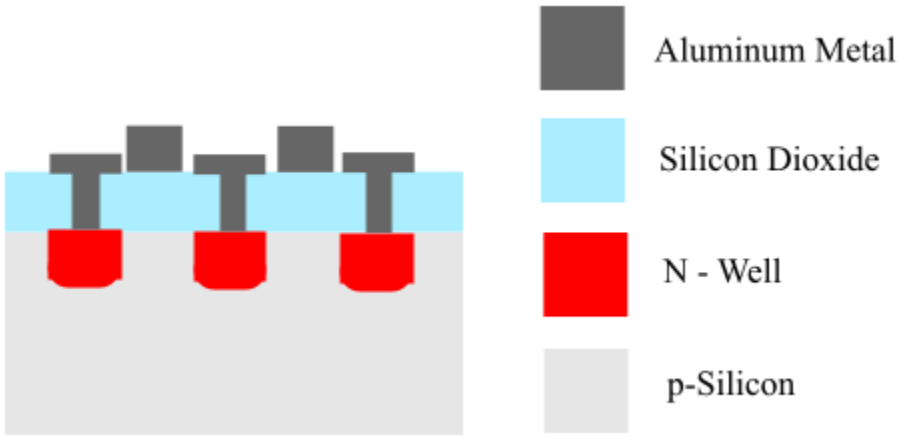

Figure 4.16: Cross Section of Aluminum Gate Contact MOSFET

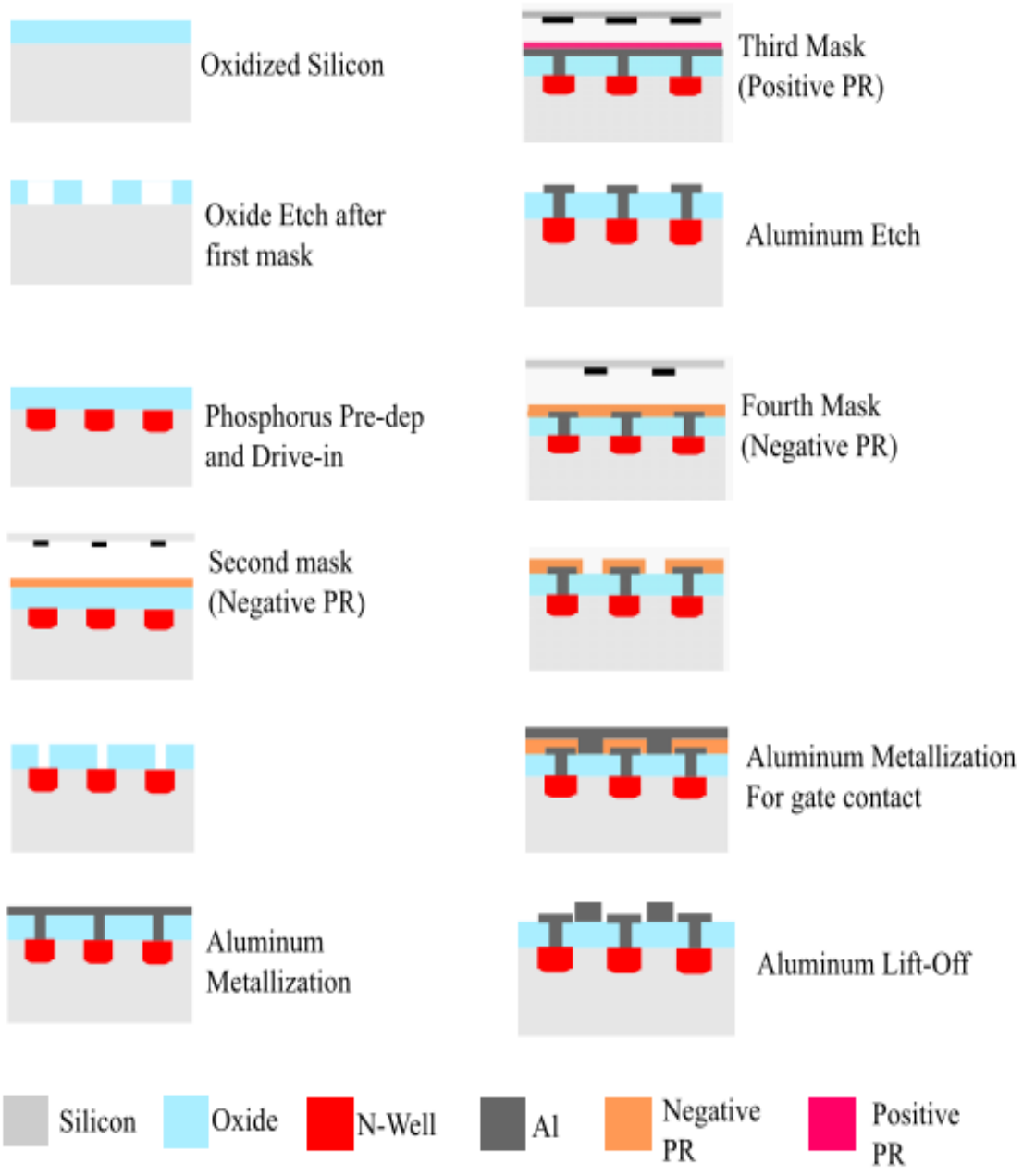

Figure 4.17: Fabrication Steps of Aluminum Gate MOSFET

CHAPTER 5: RESULTS

5.1 ITO MOSFET I-V Characteristics

The IV characteristics of ITO gate MOSFET is shown in figure 5.1. The graph shows relation between drain source voltage V_{DS} and drain current I_D at different values of gate source voltage V_{GS}. All the curves were documented using Tektronix 576 curve tracer.

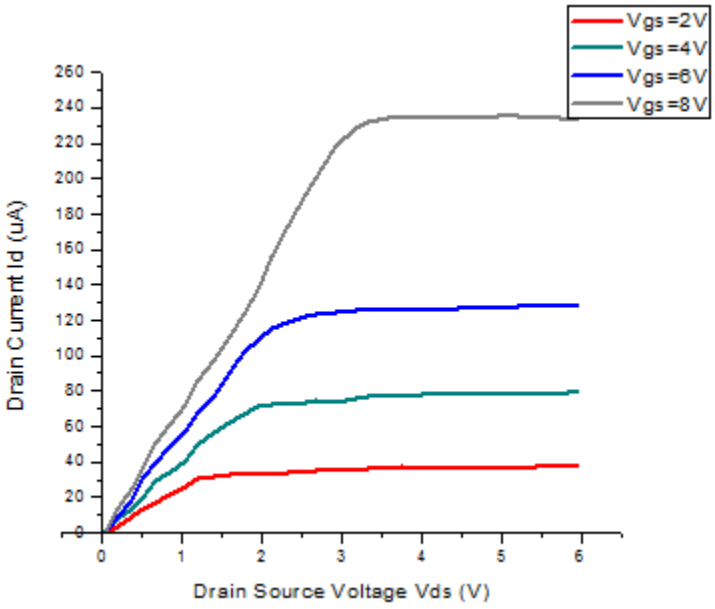

Figure 5.1: ITO Gate MOSFET V_{ds} vs. I_d Characteristics

5.2 ITO MOSFET Threshold Voltage

The gate source vs square root of drain current graph is derived from the IV characteristics of ITO gate based MOSFET.The graph of gate source voltage V_{GS} vs. $sqrt(I_D)$ shown in figure 5.2, the threshold voltage of ITO gate based MOSFET was found to be 2.4V.

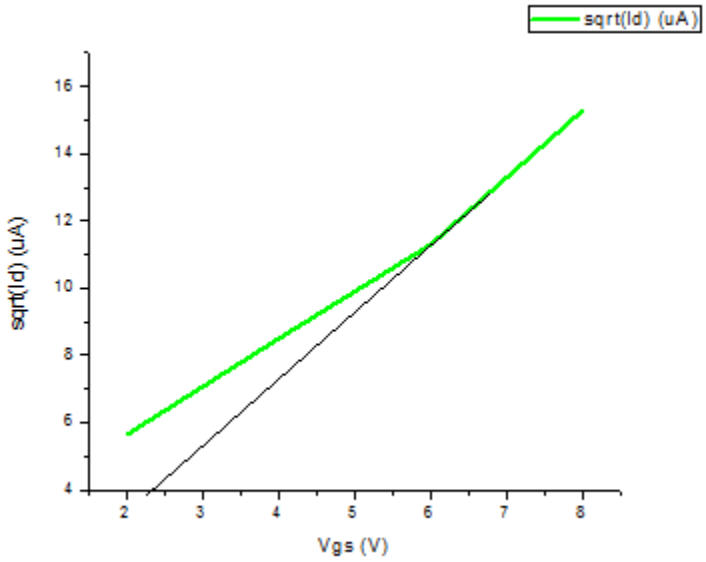

Figure 5.2: ITO Gate MOSFET V_{gs} vs. $sqrt(I_d)$ Characteristics

5.3 Aluminum MOSFET I-V Characteristics

The IV characteristics of aluminum gate MOSFET is shown in Figure 5.1. The graph shows relation between drain source voltage V_{DS} and drain current I_D at different values of gate source voltage V_{GS}. All the curves were documented using *Tektronix 576 curve tracer*.

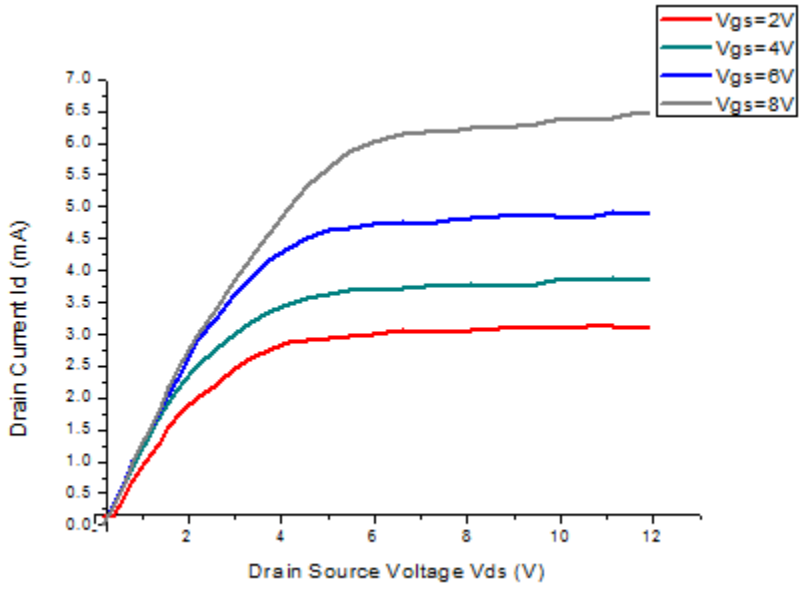

Figure 5.3: Aluminum Gate MOSFET V_{ds} vs. I_d Characteristics

5.4 Aluminum MOSFET Threshold Voltage

The gate source vs square root of drain current graph is derived from the IV characteristics of aluminum gate based MOSFET. The graph of gate source voltage V_{GS} vs. $sqrt(I_D)$ shown in Figure 5.3, the threshold voltage of aluminum gate based MOSFET was found to be 2.2V.

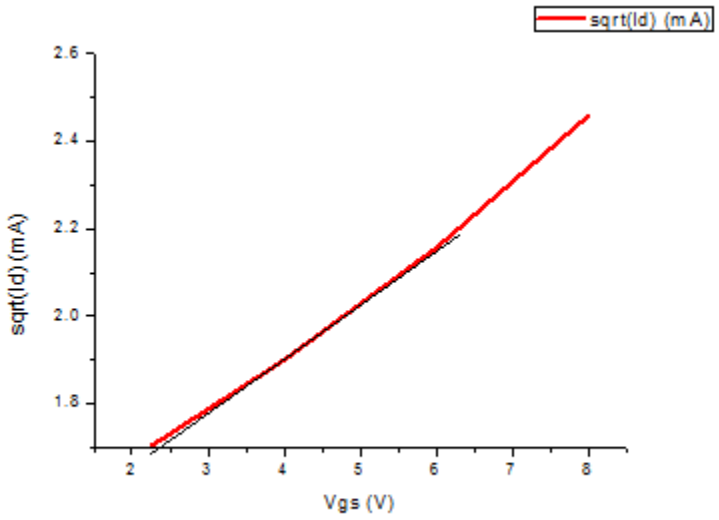

Figure 5.4: Aluminum Gate MOSFET V_{gs} vs $sqrt(I_d)$ Characteristics

5.5 Work Function Calculation of ITO

We have the threshold voltage of both the MOSFET devices from the graphs shown in figures 5.2 and 5.4.

The threshold voltage equation for aluminum gate MOSFET is given by the following equation:

$$V_{T1} = - \phi_{ms1} + 2\phi_f - \frac{Q_i}{C_i} + \frac{Q_d}{C_i}$$

The threshold voltage equation for ITO gate MOSFET is given by the following equation:

$$V_{T2} = - \phi_{ms2} + 2\phi_f - \frac{Q_i}{C_i} + \frac{Q_d}{C_i}$$

Since both the MOSFETs are fabricated under exact same conditions both the devices have the same built in voltage ϕ_f, interface trapped charges Q_i, and dielectric capacitance C_i.

Subtracting V_{T2} from V_{T1}, we get

$V_{T1} - V_{T2} = -\phi_{ms1} + \phi_{ms2}$

ϕ_{ms1} = 0.88 [30] where ϕ_{ms1} is the work function difference between aluminum on p-type silicon corresponding to the doping concentration in substrate.

2.2 - 2.4 = -0.88 + ϕ_{ms2}

ϕ_{ms2} = 0.68

ϕ_{m2} - ϕ_s = 0.68

ϕ_{m2} = 4.73 eV

Thus the work function of ITO calculated from the fabricated MOSFET is found to be 4.73 eV. This fits in the wide range of ITO work function values reported in literature 4.2 - 5.0 eV [31][32][33]. Figure 5.5 shows the Flatband energy diagram of MOS structure consisting of ITO metal, silicon dioxide and silicon.

On the same samples of aluminum gate MOSFET and ITO gate MOSFET, other devices were tested as well. The following table provides the work function of few other ITO gate based devices.

Table 5.1: Work Function of ITO Extracted from devices

Device Number	Threshold Voltage (V)	Work Function of ITO (eV)
Device 1	2.4	4.73
Device 2	2.2.5	4.62
Device 3	2.72	4.41
Device 4	2.9	4.19

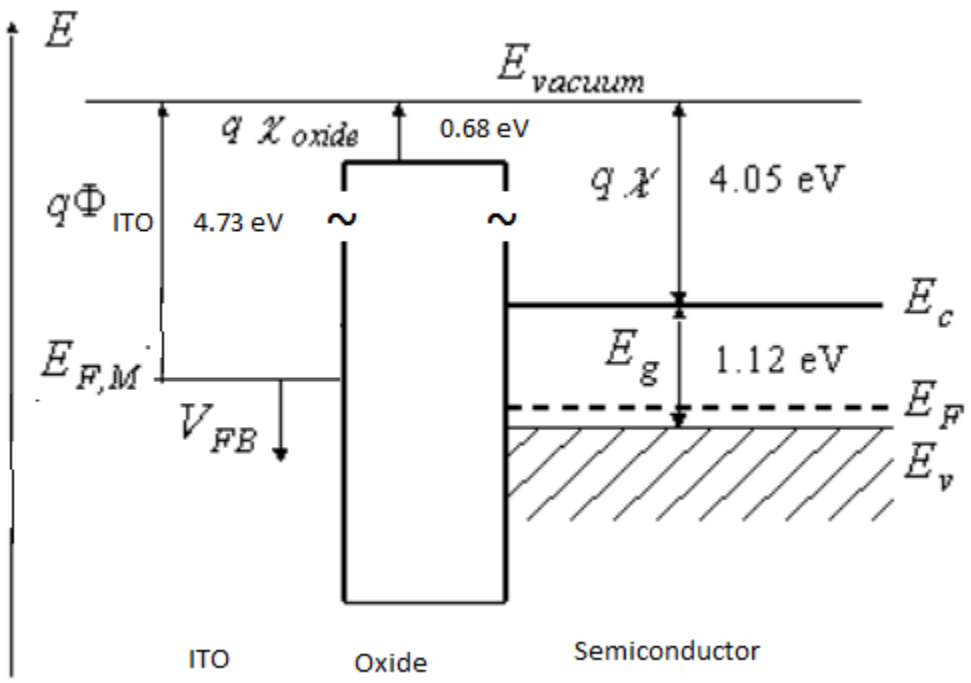

Figure 5.5: Flatband energy diagram of MOS structure consisting of ITO metal, silicon dioxide and silicon

5.6 ITO Transmission Property

The optical transmission value of ITO was measured using *Cary UV-Visible Spectrophotometer* shown in Figure A.4. Figure 5.5 shows the optical transmission spectra of ITO film over the spectral range from 400nm to 800nm. The optical transmisison value of ITO films deposited was found to be 90%.

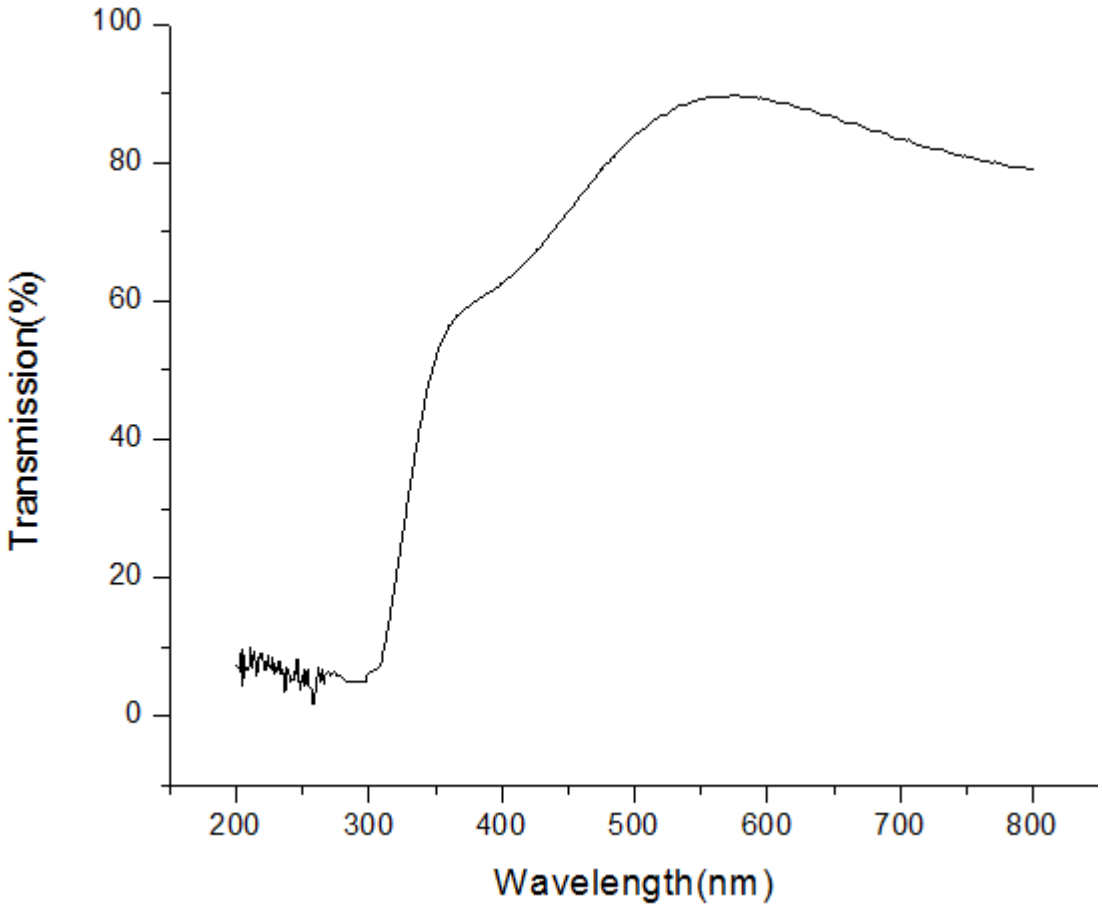

Figure 5.6: ITO Optical Transmission

CHAPTER 6: CONCLUSION

In order to investigate the work function of Indium Tin Oxide (ITO), a series of technological steps were developed and utilized during this course of study. This is the first time that work function of ITO has been extracted from measurements of a MOSFET device. Two Metal Oxide Semiconductor Field Effect Transistor (MOSFET) were fabricated using a four level mask with aluminum and ITO gate electrode respectively. Both the MOSFETs were processed under exact same conditions.

The first level of mask was used to create n-well for phosphorus impurity doping into p-silicon. Via holes were created using the second level mask. Oxide etching for source and drain contacts was achieved using third level mask. Following the photolithography process, aluminum was thermally evaporated on one of the MOSFETs to form gate contact. This aluminum was then confined only to the gate region by adopting fourth level mask for lift-off. Similarly ITO was patterned as the gate contact for another MOSFET. Lift-off was used to pattern ITO using the fourth mask. ITO was successfully fabricated on the MOSFET using Radio Frequency sputtering technique.

On completing the fabrication process, threshold voltage was measured from the I-V characteristics for both Aluminum and ITO gate based MOSFET. Using the threshold voltage equation, the work function of ITO was calculated to be 4.73 eV which is comparable to the work function values reported in literature.

APPENDIX A: FABRICATION MACHINES AND INSTRUMENTS USED

Figure A.1: Oxidation Furnace

Figure A.2: Phosphorus Diffusion Furnace

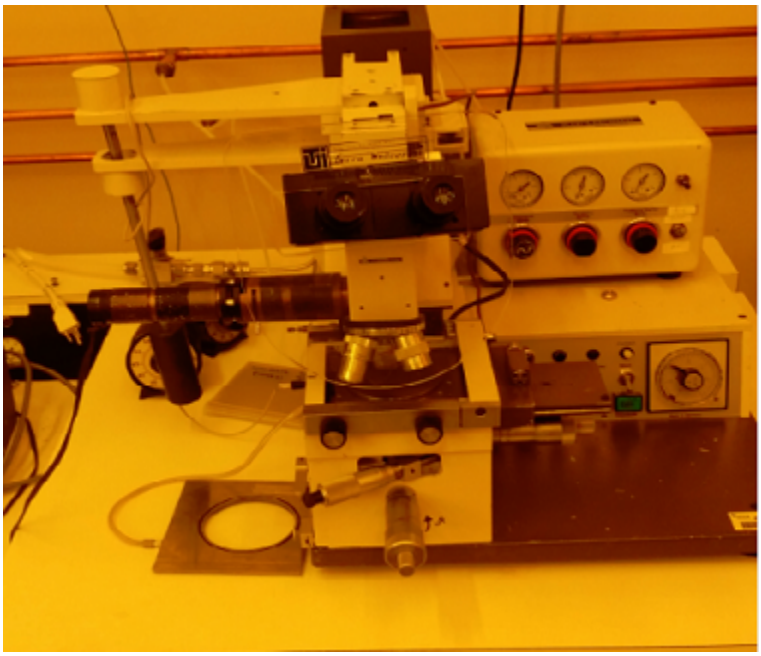

Figure A.3: Karl Suss Mask Aligner

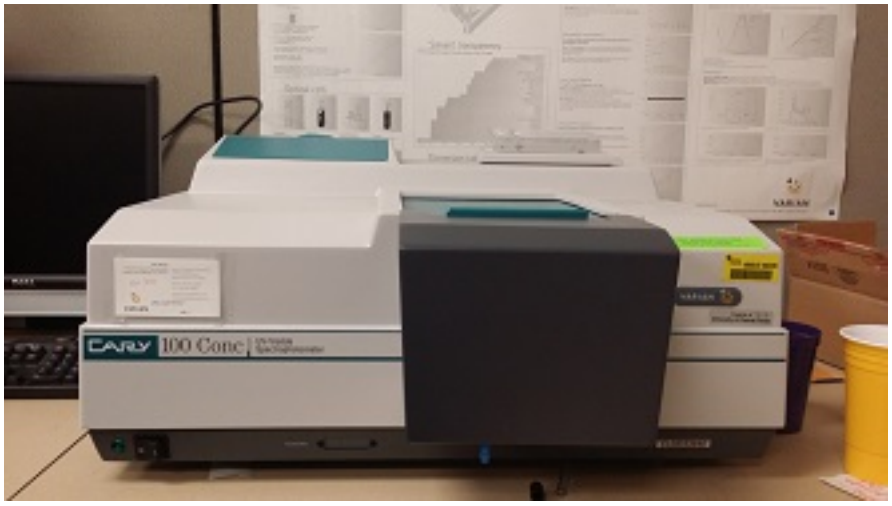

Figure A.4: Cary UV Visible Spectrophotometer

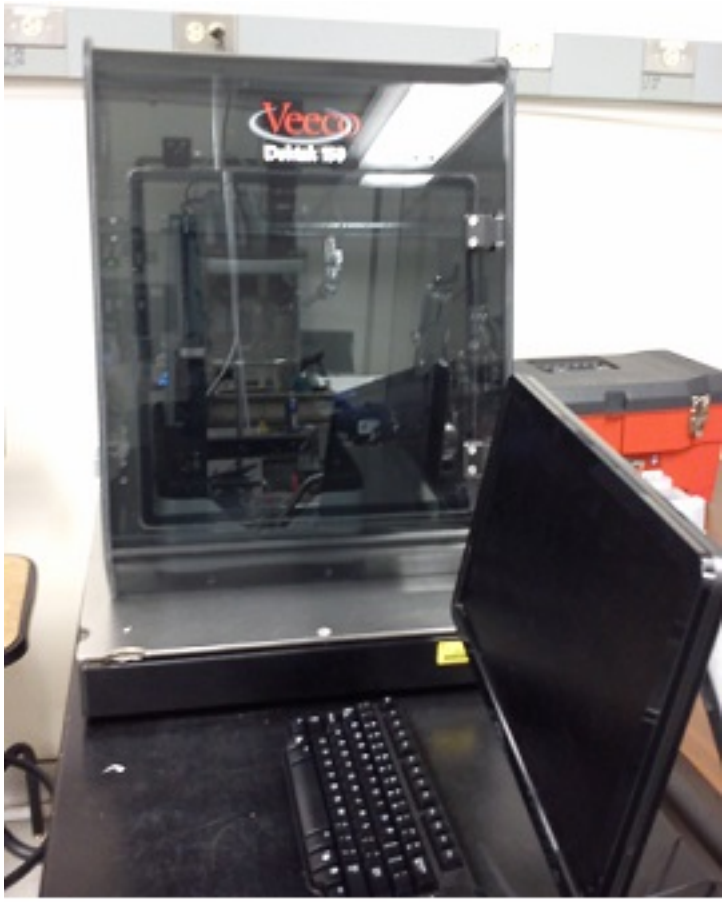

Figure A.5: Dektat 150 Profilometer

APPENDIX B: MASK STRUCTURE

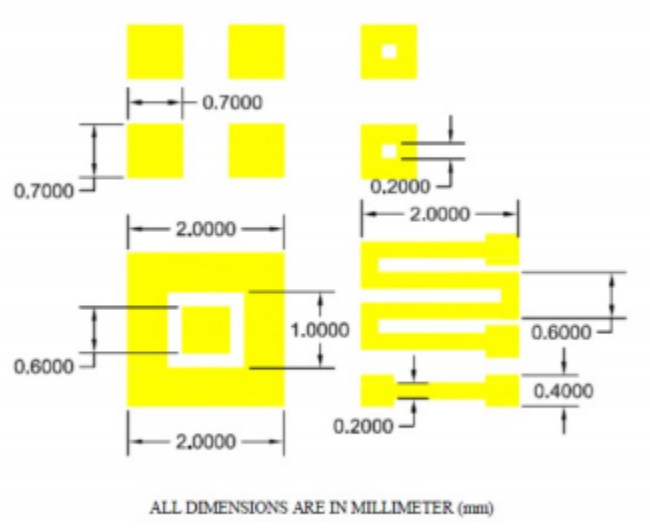

Figure B.1: Level One Mask

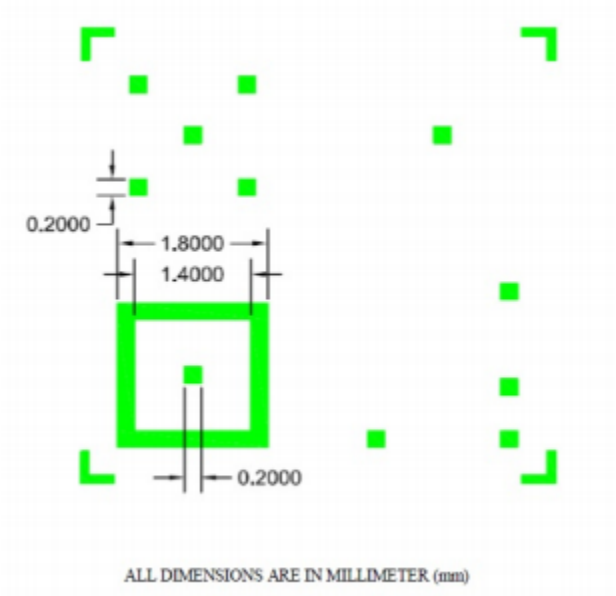

Figure B.2: Level Two Mask

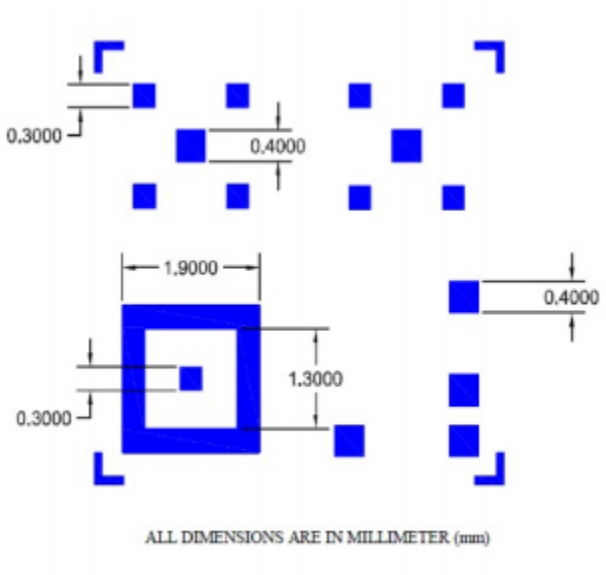

Figure B.3: Level Three Mask

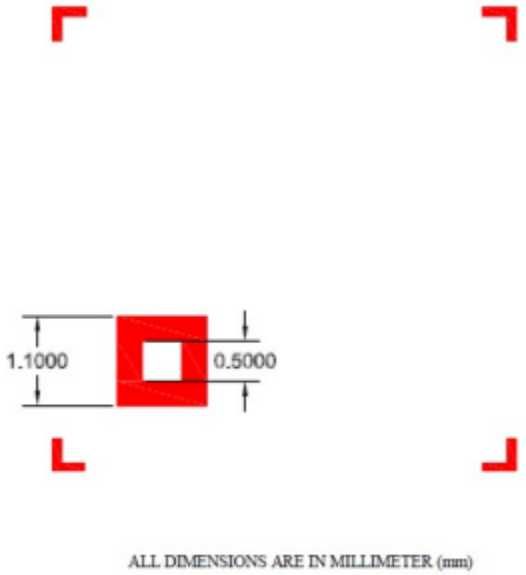

Figure B.4: Level Four Mask

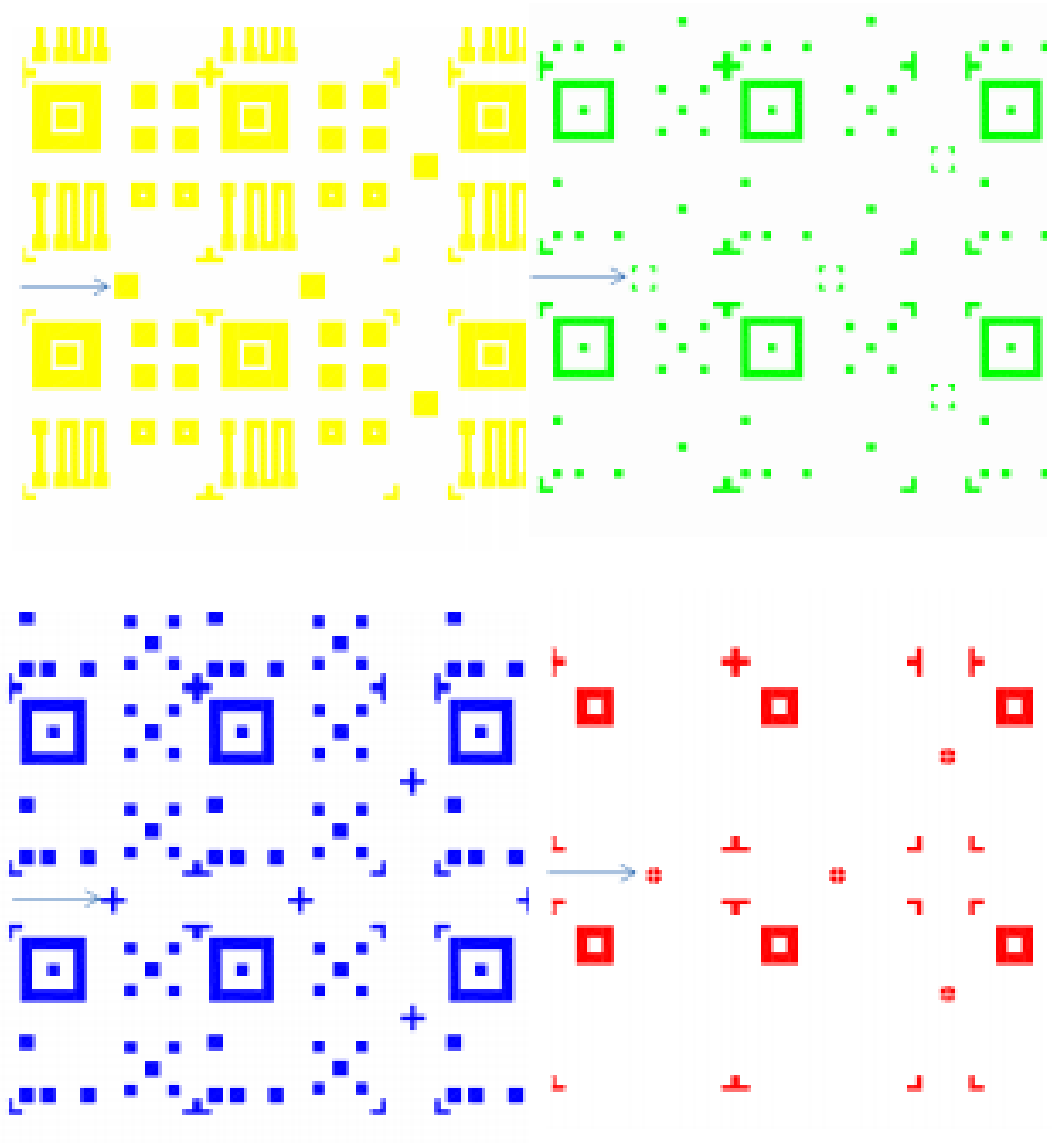

Figure B.5: All Levels of Mask

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