2010

Highly Integrated Dc-dc Converters

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HIGHLY INTEGRATED DC-DC CONVERTERS

by

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A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy
in the School of Electrical Engineering and Computer Science
in the College of Engineering and Computer Science
at the University of Central Florida
Orlando, Florida

Spring Term 2010

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ABSTRACT

A monolithically integrated smart rectifier has been presented first in this work. The smart rectifier, which integrates a power MOSFET, gate driver and control circuitry, operates in a self-synchronized fashion based on its drain-source voltage, and does not need external control input. The analysis, simulation, and design considerations are described in detail. A 5V, 5-μm CMOS process was used to fabricate the prototype. Experimental results show that the proposed rectifier functions as expected in the design. Since no dead-time control needs to be used to switch the sync-FET and ctrl-FET, it is expected that the body diode losses can be reduced substantially, compared to the conventional synchronous rectifier. The proposed self-synchronized rectifier (SSR) can be operated at high frequencies and maintains high efficiency over a wide load range.

As an example of the smart rectifier's application in isolated DC-DC converter, a synchronous flyback converter with SSR is analyzed, designed and tested. Experimental results show that the operating frequency could be as high as 4MHz and the efficiency could be improved by more than 10% compared to that when a hyper fast diode rectifier is used.

Based on a new current-source gate driver scheme, an integrated gate driver for buck converter is also developed in this work by using a 0.35μm CMOS process with optional high voltage (50V) power MOSFET. The integrated gate driver consists both the current-source driver for high-side power MOSFET and low-power driver for low-side power

MOSFET. Compared with the conventional gate driver circuit, the current-source gate driver can recovery some gate charging energy and reduce switching loss. So the current-source driver (CSD) can be used to improve the efficiency performance in high frequency power converters.

This work also presents a new implementation of a power supply in package (PSiP) 5MHz buck converter, which is different from all the prior-of-art PSiP solutions by using a high-Q bondwire inductor. The high-Q bondwire inductor can be manufactured by applying ferrite epoxy to the common bondwire during standard IC packaging process, so the new implementation of PSiP is expected to be a cost-effective way of power supply integration.

ACKNOWLEDGMENTS

First, I would like to express my sincere appreciation to my advisor, Dr. Z. John Shen, for his guidance, advice and continuous support throughout this work. His enthusiasm for exploring new ideas within the area of power electronics has made my graduate study here a rewarding experience. I am grateful for the opportunity to work with him and appreciate all the help from him.

I would like to thank Dr. Xu Cheng for his help on this work. I still remember the time we worked together to run the DRC and LVS checks using our eyes before the tape-out of one of our designs.

I gratefully thank Dr. Issa Batarseh, Dr. Jiann S. Yuan, Dr. Osama Abdel-Rahman, and Dr. Kalpathy B. Sundaram for their very constructive suggestions on my thesis work as members of my advisory committee. Special thank goes to Dr. Osama Abdel-Rahman for his invaluable help with some of this work.

I would also like to acknowledge my fellow student and scholars at Power Semiconductor Research Lab (PSRL). The friendship, the enlightening discussions, and the enjoyable atmosphere make the stay at PSRL a very pleasant and rewarding experience. Special thanks are due to Mi Dong, Brain Grummel, Dr. Lina Guo, Jian Lu, Matt Landowshi, Karthik Padmanabhan, Patrick Shea, Shan Sun, Xuexing Wang, Yali

Xiong, Boyi Yang. I also would like to express my appreciation to Karthik Padmanabhan for his proof reading of this thesis.

My heartfelt appreciation goes to my family for their understanding and constant support during my study years. Especially, I would especially like to thank my wife for her love, encouragement, and best support.

Some of the thesis work was done in collaboration with Dr.Yan-fei Liu, Dr. Zhiliang Zhang, and Jizhen Fu from Queen's University, Canada. I would like to thank all of them for the delightful discussions.

The IC fabrication work in this thesis has been done through MOSIS and IMEC of Europractice IC service. Special thanks are extended to the supporting people from MOSIS and IMEC.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1: INTRODUCTION

1.1 Background and Prior-art

Physical feature sizes of Integrated Circuits (IC) continue to scale down as IC fabrication technology advances. Thanks to the shrinking in geometry size, more transistors and new functions are integrated into today's GHz-class microprocessors. At the same time, the current consumption of the microprocessors increases significantly due to the increasing number of integrated transistors, higher operating frequency, and more functions. The power consumption of the microprocessor, therefore, increases dramatically in spite of the decreasing of the core voltage. According to the international technology roadmap for semiconductors (ITRS) published by the Semiconductor Industry Association (SIA), microprocessors will be operating at less than 1V, drawing up to 200A in the near future[1].

Voltage regulator modules (VRM) and voltage regulator down (VRD) are responsible for delivering power to multiple-processor and a single processor, respectively, as stated in Intel's VRD/VRM design guidelines[2]. The primary performance requirements for VRM/VRD are accurate voltage regulation and fast transient response to load variation. At the same time, in today's battery powered, portable electronic system, the requirements for smaller volume, lighter weight, and longer battery life become more important than ever. To meet these requirements, DC-DC converters must have high efficiency, high power density (or high integration), and high switching frequency (in

MHz range). Formidable technological challenges exist in designing of power supplies for today's and future's advanced application systems.

Power MOSFETs are the most critical component and fundamental building block of high performance power supplies. Power MOSFET structure, as illustrated in Fig. 1.1, consists of a gate voltage controlled channel and an integral body diode which is in anti-

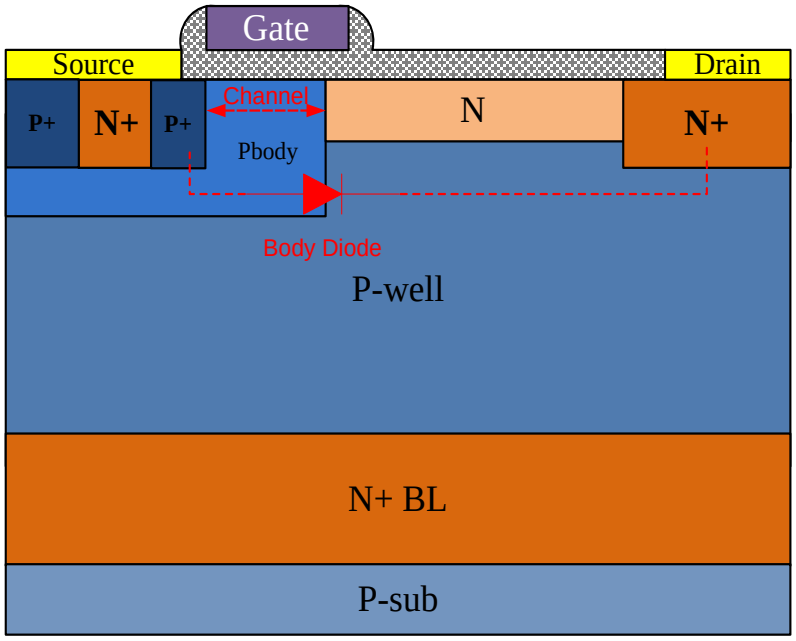


Figure 1.1 A typical power MOSFET structure with the inherent body diode

parallel to the channel. The body diode is inherent to the structure of the MOSFET and turns on whenever the voltage polarity across it is reversed during typical switching operation. Power MOSFETs form the fundamental building blocks of switching mode power converters and act as active power switches or synchronous rectifiers.

Synchronous buck converter has been predominantly employed in high performance, low-voltage and high-current power converters, like VRM or VRD, to efficiently provide power to computer system and portable/hand-held devices. A typical synchronous buck converter is shown in Fig. 1.2, where power MOSFETs are used as main control switch (ctrl-FET) and synchronous rectifier (sync-FET).

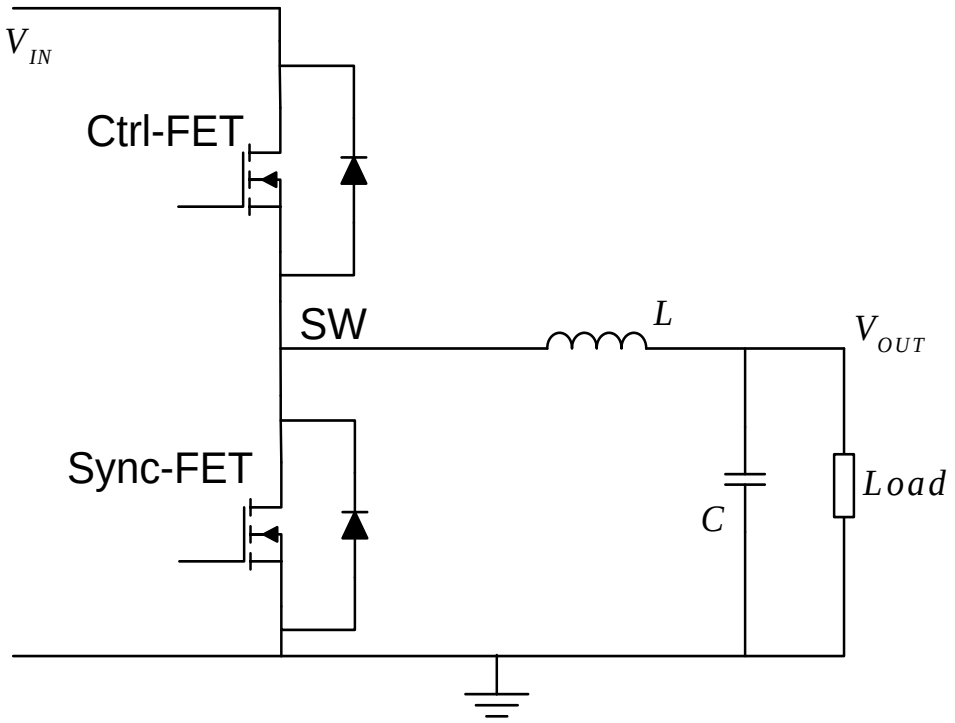


Figure 1.2 A typical synchronous buck converter

A time interval, so called “dead time”, has to be inserted between two gate driving signals to prevent shoot through in a synchronous buck converter. Shoot-through is defined as the condition when both MOSFETs are either fully or partially turned on, providing a path for current to “shoot through” from VIN to GND[3]. Shoot through, if allowed to occur, reduces system efficiency, causes power MOSFET heating and even

thermal shutdown. Dead time is a time period where neither switch conducts, which is a new feature of the newer integrated circuits that are designed specifically for synchronous rectification applications. During the deadtime, because both MOSFETs keep off, so the inductor current has to flow through the body diode of the synchronous rectifier (sync-FET), which causes power loss and degrades the overall efficiency of the system.

1.1.1 Body Diode Power Loss in Synchronous Rectifiers

The corresponding switching waveforms of the synchronous buck converter is shown in Fig. 1.3. From the waveforms, it can be seen that the body diode of the sync-FET turns

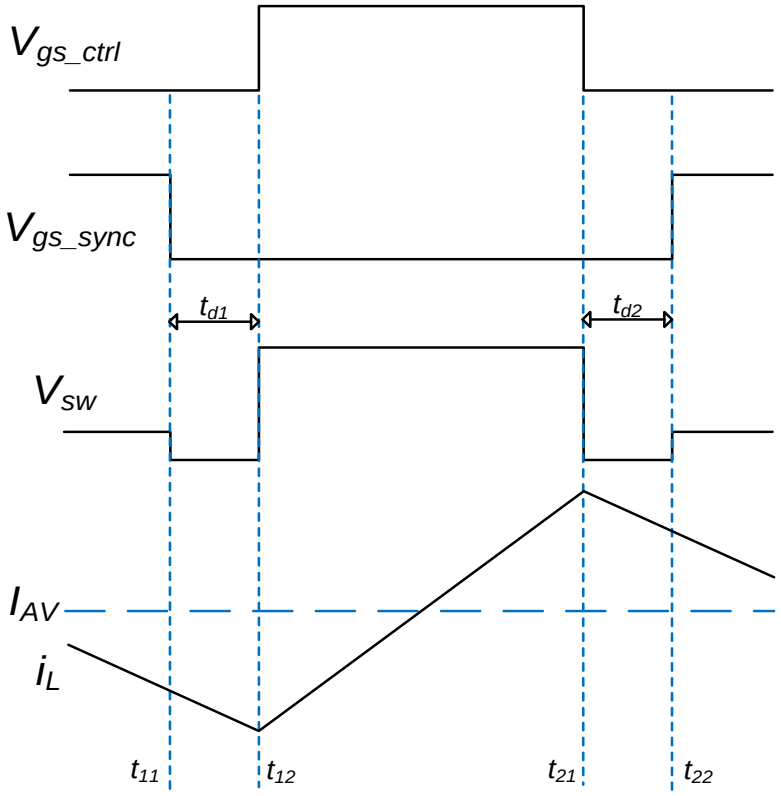


Figure 1.3 Switching waveforms of a typical synchronous buck converter

on twice during deadtime interval of t_{d1} and t_{d2} in every switching cycle, which degrades the system efficiency by both conduction loss and reverse recovery loss. During deadtime t_{d1}, the body diode conduction loss can be calculated by

$$\begin{aligned} P_{cond-t_{d1}} &= \frac{1}{T_{sw}} \cdot \int_{t_{11}}^{t_{12}} V_F \cdot \frac{V_{OUT} + V_F}{L} \cdot t \cdot dt \\ &= V_F \cdot f_{sw} \cdot (I_{AV} - \frac{V_{IN} - V_{OUT}}{2L} \cdot D \cdot T_{sw} + \frac{V_{OUT} + V_F}{2L} \cdot t_{d1}) \cdot t_{d1} \end{aligned} \tag{1-1}$$

where T_{sw} is the period of the switching cycle, D is the duty circle, f_{sw} is the switching frequency, V_F is the forward voltage drop of the body diode, I_{AV} is the average inductor current, which equals to output current I_{OUT}, V_{IN} and V_{OUT} are input and output voltage, respectively.

And at time t_{12}, ctrl-FET turns ON, body diode begins reverse recovery, which cause power loss

$$P_{rev-t_{d1}} = \frac{1}{T_{sw}} \cdot \int_{t_{12}}^{t_{12}+t_{rr}} V_{IN} \cdot i_{rr}(t) \cdot dt = V_{IN} \cdot f_{sw} \cdot Q_{rr} \tag{1-2}$$

where $i_{rr}(t)$ is the transient reverse recovery current, t_{rr} is the reverse recovery time, and Q_{rr} is the reverse recovery charge, which is the stored excess carriers when the body diode is conduction under forward bias condition.

During deadtime t_{d2}, the body diode conduction loss can be calculated by

$$P_{cond-t_{d2}} = \frac{1}{T_{sw}} \cdot \int_{t_{21}}^{t_{22}} V_F \cdot \frac{V_{OUT} + V_F}{L} \cdot t \cdot dt$$
$$= V_F \cdot f_{sw} \cdot (I_{AV} + \frac{V_{IN} - V_{OUT}}{2L} \cdot D \cdot T_{sw} - \frac{V_{OUT} + V_F}{2L} \cdot t_{d2}) \cdot t_{d2} \quad (1\text{-}3)$$

At time t_{22}, sync-FET turns on, body diode is still forward biased (but the biasing voltage becomes $V_{DS\text{-}sync}$) and hence there is no reverse recovery loss. The total power loss caused by diode conduction, therefore, can be calculated as (by assuming $t_{d1} = t_{d2} = t_d$)

$$P_{diode} = P_{cond-t_{d1}} + P_{cond-t_{d2}} + P_{rev-t_{d1}} = 2V_F \cdot f_{sw} \cdot I_{OUT} \cdot t_d + V_{IN} \cdot f_{sw} \cdot Q_{rr} \quad (1\text{-}4)$$

The above analysis is for continuous conduction mode (CCM), for discontinuous conduction mode (DCM), the body diode loss is only conduction loss which occurs only during deadtime t_{d2}.

From equation (1-4), it can be concluded that the diode related power loss increases dramatically for longer deadtime, higher switching frequency, and higher output current. Another interesting conclusion is that the higher the input voltage, the more reverse recovery loss.

Given the fact that MOSFET conduction and switching losses have been reduced substantially in the past years [4]-[6], the body diode loss will contribute to a substantial portion of the total losses in the future due to the large forward voltage drop and poor reverse recovery characteristics of the PN junction diode. For example, in [7], over 3.5% improvement of efficiency is reported for a synchronous buck converter by just eliminating unnecessary body diode conduction. Because body diode related power

losses during dead time are proportional to switching frequency, the body diode power loss will present a fundamental technical barrier for meeting performance and efficiency requirement of future DC/DC converters as they migrate into higher switching frequency ranges [8]-[9].

Various prior-art approaches have been proposed to address the body diode loss issue during dead time interval from both device and circuit points of view. From device standpoint, people have tried to control carriers lifetime profile [10] or to add additional Schottky diode in parallel with the body diode[11]-[15]. Control of carrier lifetime reduce reverse recovery loss but have no effect on the conduction loss. Additional Schottky diode will suppress the body diode turn on, so it reduces the body diode related losses significantly. However, it is limited by the increased cost and also by the die size (when it is integrated) or parasitic resistance and inductance (when it is co-packaged or externally connected).

It is important to realize that a fixed very short dead time is impractical since the dead time required to avoid shoot through usually depends on circuit input, load condition, power MOSFET parameter, other circuit components parameters, and even the temperature. Therefore, many circuit techniques, including adaptive deadtime control, have been proposed to keep the deadtime as short as possible[16]-[23] to maximize system efficiency. Some proposed algorithm[19]-[23], however, require fairly complex additional hardware, and therefore increase the overall size and cost of the power converters. Hence, the less complicated, adaptive/predictive deadtime control schemes

have been commonly implemented[24]-[26]. More simplified circuit techniques, if possible, are still at a premium to address the body diode conduction.

1.1.2 Synchronous Rectifier in Isolated Power Converters

When synchronous rectification technique is used in isolated converter to improve system efficiency, there are some specific issues that need to be solved[27]. Flyback converter, the isolated version of buck-boost converter, has been widely used in power applications under 200W due to the advantages of less component counts, low cost, compact profile, step up and down functions, and isolation between input and output [28]-[31]. Here, we take flyback DC-DC converter as an example to explain the existing problems and some solutions when synchronous rectifiers are used.

Recently, high frequency flyback converters are being considered for VRM application to overcome the low duty cycle limitation encountered in the buck VRM topology [32][33] since the flyback topology uses a transformer to step down the voltage, and is thus not limited by the low duty cycle issue. In low-output-voltage flyback converters, it is necessary to use MOSFET as secondary synchronous rectifiers (SR) to meet the high efficiency requirement [34]-[36]. However, the synchronous rectifier MOSFET (Sync-FET) requires a control signal and gate driver circuit for proper switching timing control, which must be in synchronization with respect to the control power MOSFET on the primary side of the transformer. This presents a design and implementation challenge in terms of system complexity, performance, and overall cost.

According to how the gate driving signal is generated, the synchronous rectifiers in existing flyback converter can be classified into two types: the self-driven synchronous rectifier (SDSR) and external-driven synchronous rectifier (EDSR) The SDSR approach, as shown in Fig.1.4, realizes synchronized switching by simply connecting an additional

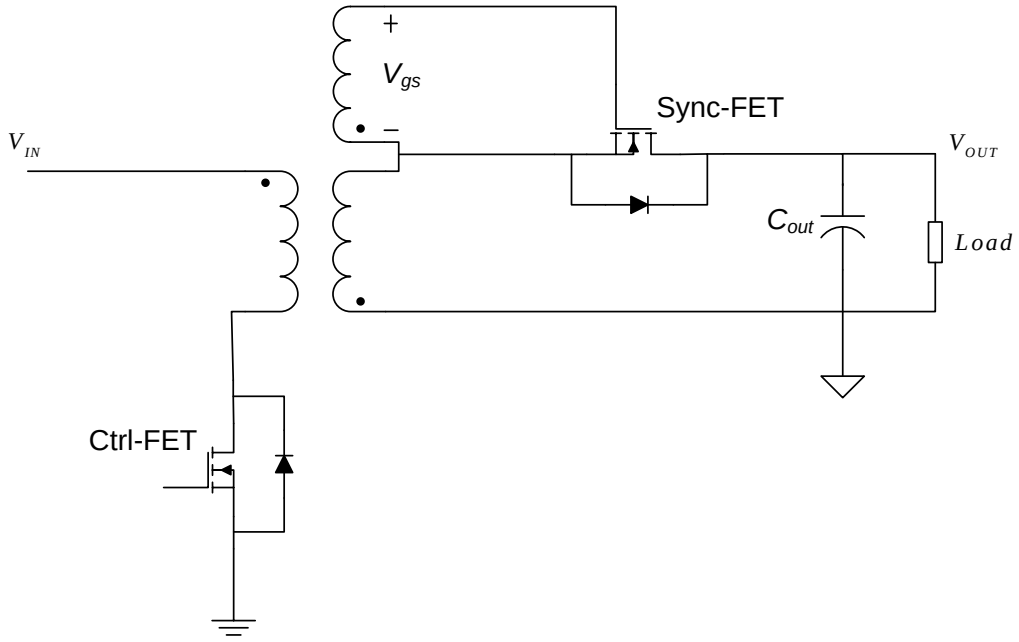


Figure 1.4 SDSR driving topology

winding in the transformer to the gate and source of the sync-FET [37][38]. Although very simple in operation principle, SDSR does not offer sufficiently precise control timing to fully utilize the Sync-FET [39]. The parasitic body diode of the Sync-FET conducts the load current during a significant portion of the total rectifier on-time, resulting in low system efficiency, particularly at very high switching frequencies. Furthermore, SDSR does not allow DCM operation and consequently lead to low

efficiency at light load conditions because current is still circulating all the time after the primary side switch is turned off.

The EDSR approach, as shown in Fig. 1.5, can be used to overcome the limitations of SDSR to a certain extent by using break-before-make control scheme. Usually, the

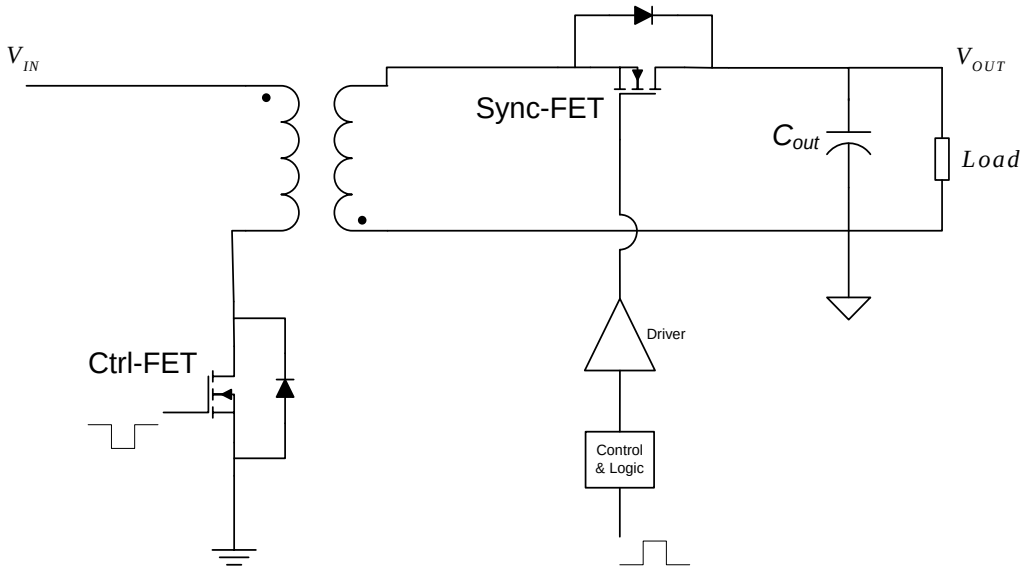


Figure 1.5 EDSR driving topology

control signal in this approach comes from the primary side directly without isolation or through a pulse transformer or opto-isolator[40][41]. Similarly, deadtime is also used in these topologies to avoid the switch in primary side and the switch in secondary side from conduction simultaneously. Therefore, as in other synchronous converters, the same issue with regards to minimizing the deadtime remains because system efficiency is very

sensitive to the deadtime[42]. Also, in these topologies, DCM operation is still not available, which degrades the system efficiency the same way as it does in SDSR.

The sync-FET can also be controlled by sensing the secondary current through a current transformer [43]-[45]or voltage drop of the sync-FET.[46]-[49]. However, those circuits are mostly implemented in discrete form and do not offer sufficient precision in timing due to the influence of the parasitic elements. It is therefore advantageous to find a integrated, less-complicated way to realize synchronous rectifier in isolated converters.

1.1.3 Current-Source Gate Driver

Switching power supply operates at ever increasing high frequency in order to reduce the size of the passive components in hand-held/portable applications and to meet the requirements for fast dynamic response and low output voltage ripple in computing electronics[50]-[52].

However, as the switching frequency increases, the switching loss and gate drive loss also increase dramatically since both of the losses are proportional to switching frequency. These two frequency-dependent loss components become dominant in the total loss of a high frequency power converter system, which significantly degrades the overall efficiency and increases the heat removal cost. Switching loss is also proportional to the switching time, while switching time is mainly decided by the gate driver design for a given power MOSFET. Conventional gate driver circuit usually charges and discharges the gate capacitance of the power MOSFET through active switches. The charging and discharging current have high peak value but fast drop down rate. So the

switching time is relatively long. Therefore, further increase in the switching frequency necessitates a new gate driver scheme to reduce both the gate driver loss and switching loss.

Fig. 1.6 presents a simplified conventional lossy gate driver circuit, where MOSFET S_1-S_4 compose the simplified drive circuit to drive main MOSFET M_1. There are 3 main

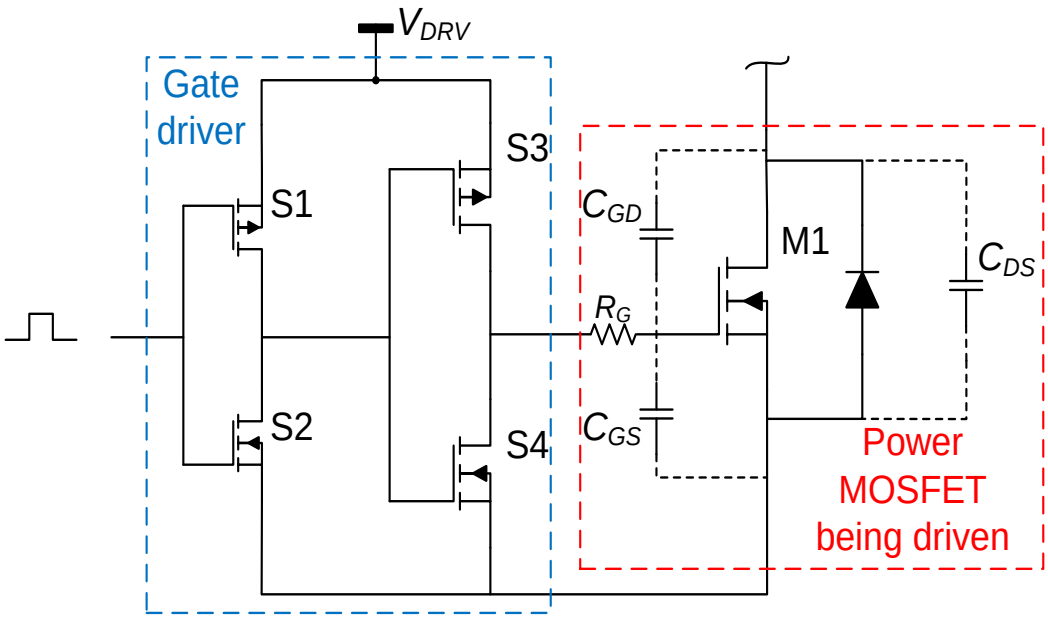


Figure 1.6 Simplified converntional gate driver

parasitic capacitors also illustrated in Fig. 1.6 for the main MOSFET M_1: C_{GS}, C_{GD}, *and* C_{DS}, which represent the gate-source capacitor, gate-drain capacitor, and drain-source capacitor, respectively. All of these capacitors are non-linear, which means their capacitance values vary with the bias conditions. In a power MOSFET datasheet, three different capacitors, i.e. C_{iss}, C_{oss}, C_{rss} are usually specified. C_{iss} and C_{oss} refer to input capacitor (when drain and source are shorted) and output capacitor (when gate and source

are shorted), respectively, while C_{rss} means reverse transfer capacitor (or miller capacitor). The analysis and calculation of MOSFET power loss will based on these three capacitance from MOSFET datasheet. The relationship between these two groups of capacitance is given by

$$C_{iss} = C_{GS} + C_{GD} \tag{1-1}$$

$$C_{oss} = C_{GD} + C_{DS} \tag{1-2}$$

$$C_{rss} = C_{GD} \tag{1-3}$$

The most important power losses in the conventional driver circuit can be classified as the power used to charge and discharge all the output capacitance of switch S_1-S_4, the power dissipated when charging and discharging all the input capacitance of switch S_1-S_4, and the power dissipated when charging and discharging the input capacitance of the main power MOSFET M_1. The first two power losses are caused by the driver circuit itself, which are targeted low in conventional driver circuit design. Power MOSFET M_1 usually needs to handle high current, which requires low $R_{ds\text{-}on}$ to lower power loss. Low $R_{ds\text{-}on}$ means large silicon area and high parasitic capacitance in most cases. Therefore, the third item (the power required to turn on/off the power MOSFET M_1) is the dominant power loss for driving a power MOSFET. In [53], the investigation discovers that the power required to turn on/off the power MOSFET M_1 accounts for 66.7% of the total power loss in the driver circuit. In this work, we mainly consider the third loss item. The power loss due to charging the input capacitor of M_1 is given as

$$P_{DRV} = \frac{1}{T_{SW}} \cdot \int_0^{t_{chg}} V_{DRV} \cdot i_G(t) \cdot dt = V_{DRV} \cdot f_{SW} \cdot Q_G \quad (1\text{-}4)$$

where V_{DRV} is the gate drive voltage. $i_G(t)$ is the transient gate charging current. t_{chg} is the time to charge the gate capacitance. Q_G is the gate charge when the gate capacitors are charged to V_{DRV}. Interestingly, the gate resistance R_G have no effect on gate driving loss. Based on this equation, several approaches have already been proposed to reduce the gate drive loss.

From device point of view, small gate capacitor means less gate charge, so by optimization of device structure or fabrication process technology (like doping profile), the gate driving power loss can be reduced [7][54]-[57]. Once a power MOSFET in the market is chosen for a specific application, some circuit techniques can be used to further reduce the gate drive power loss.

Since $Q_G \propto V_{DRV} \cdot C_{iss}$, it can be inferred that gate drive loss is approximately proportional to the square of driving voltage from the equation (1-4). So decreasing the gate driving voltage will reduce the gate loss significantly. However, the conduction loss may increase due to the increased $R_{ds\text{-}on}$. Based on this observation, some circuit techniques, like low-swing gate driver [58]-[60] were proposed to try to find a optimum driving voltage which can obtain a good trade-off between gate drive loss and conduction loss and improve the system efficiency.

In conventional gate driver circuit, half of the gate driving energy is stored in the gate capacitors during charging and dissipated when the gate capacitor is discharged. Some

resonant gate driver circuits have been proposed to recover part of the energy loss. In [61], a resonant gate driver is proposed with extra L-C tank to reduce the gate drive loss. The main drawback of [61] is that the inductor current is continuous, which means there is always a circulating current flowing in the driver circuits. So the driver circuit generate some extra conduction loss. Another resonant gate driver is proposed in [62], in which the inductor current is discontinuous. No inductor current is present except during the on/off transition of the main MOSFET. So the conduction loss in driver circuit is reduced. However, since the inductor current starts from zero to charge and discharge the gate of the main MOSFET, the switching transition becomes longer, the switching loss increases. Combining both [61] and [62], a current source gate driver[63] is proposed, in which, the inductor current is discontinuous, but it rises before turning the main MOSFET on/off, so the conduction loss in driver circuit is minimized and a quick turn-on and turn-off transition is obtained at the same time. In addition, it is capable of clamping the main MOSFET gate to the gate driving power supply during the on time and to ground during the off time. The ground-clamping is particularly important to avoid undesired false triggering of the main MOSFET, i.e. *Cdv/dt* immunity [64]-[66].

1.1.4 Power Supply in Package

The evolution of mobile electronic devices such as PDAs, smart cell phones, and digital audio/video recorder/players has been driving the increasing demand for power supply miniaturization or integration. Apart from the saved board space and reduced board mounting height, the power supply integration is also advantageous for the improved

performance and system efficiency due to the reduction in unwanted parasitic components, e.g. inductance and resistance [67]-[69].

Power supply on chip (PwrSoC), which is an advanced technology to incorporate multiple components into a single semiconductor substrate, is believed to be the ultimate level of power system integration. Some PwrSoC implementations have already been demonstrated in literature [70]-[72]. In these work, although very high switching frequencies have been used to reduce passive components size, inductors and capacitors usually still consume a large portion of the silicon area. There is no cost effective way been found to make the PwrSoC actually enter the power supply market. So far, there are only a few "near" PwrSoC devices which are so called power supply in package (PSiP). PSiP integrates all active devices and passive components into a single package, providing an attractive and practical solution because of the significant improvement in performance and reduction in board space, parts count, and time-to-market[73]-[75].

However, the development of PSiP is seriously hindered by a few major technical barriers including integration of magnetic passive components. Magnetics integration is thought as an enabling technology for power supply integration [76]. The main challenge is to find a cost effective means of integrating inductors and transformers with adequate performance in terms of inductance, dc series resistance, saturation current, coupling coefficient, and Q factor. Current research work on integrated magnetics has predominantly focused on utilizing MEMS (micro-electro-mechanical-system) micromachining technology as a post-processing step after the completion of the CMOS chip containing all power switching devices and control circuitry [77]-[83].

Sophisticated MEMS technology allows sequential deposition and patterning of numerous layers of conductor, insulator, perm alloy or ferrite thin films to form desirable inductor and transformer structures. However, the high dc resistance and poor Q factor (typically 3 to 8) of the MEMS inductors/transformers severely limit the current handling capability and efficiency. More critically, the large increase of fabrication complexity and cost associated with the MEMS post-processing approach raises questions on its feasibility to facilitate large scale commercialization of the power system integration concept into the extremely cost-sensitive power supply market.

In reality, almost all PSiP products available in market only have control, drive and power MOSFET assembled with passive components in a single surface mount package

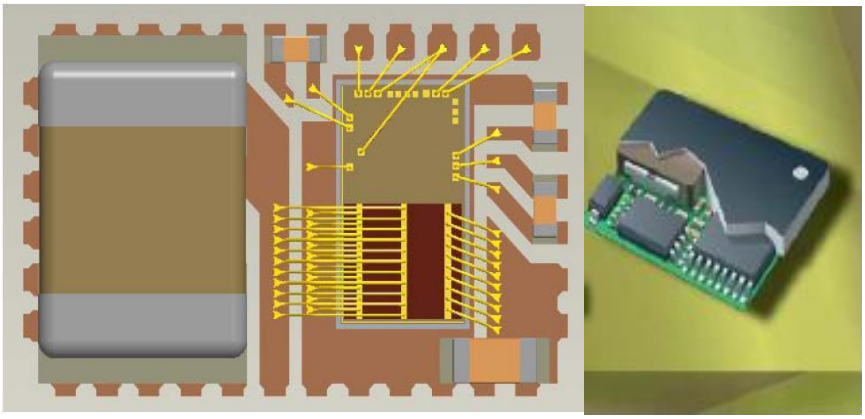


Figure 1.7 PSiP products in market: inside and package

[84]. Usually in PSip, the silicon dice of active devices and passive components are connected with each other through mixed-mode inter-connection, which adopts surface mounting technology (SMT) and bondwires [85][86]. The package and the inside of the PSiP are illustrated in Fig. 1.7. It is very clear that this type of PSiP is only a co-package

of few active dice and passive components, and hence they usually can not use standard package process.

1.2 Research Objectives

The main purpose of this dissertation work is to address some issues mentioned in the previous section, i.e. the body diode power loss in synchronous rectifiers, the synchronous rectification technique in flyback converter, new gate driver in high frequency power converters, and power supply integration, for today's high frequency, high performance, and high integration switching power converters.

The first objective is to develop a monolithically integrated, smart synchronous MOSFET with significantly reduced body diode power loss without employing an additional Schottky diode. More specifically, we propose to investigate a smart auxiliary circuit approach to enable the synchronous MOSFET to operate in a self-synchronized fashion without requiring complex "dead time" or "break-before-make" control, but in the meantime offer a very low conduction loss. The smart rectifier, which integrates a power MOSFET, its driving circuit, and control logic, operates in a self-synchronized fashion similar to a simple diode. We verify the concept with extensive circuit simulation and a prototype device fabricated with AMIS 0.5μm CMOS technology through MOSIS services.

When synchronous rectification technique is used in isolated converters, synchronization of the switching timing of the two power MOSFETs on different sides of the transformer becomes complicated. The second objective of this work is to propose and demonstrate a

new way to simply implement a synchronous flyback converter by using the newly developed monolithic self-synchronized rectifier.

The third research objective is to develop a gate driver chip for a buck converter. The chip, which integrates gate drivers for both high-side and low-side power MOSFETs, is expected to reduce the gate drive loss in high frequency power converters by using some new gate drive techniques.

Another research objective is to demonstrate a package level integration of a monolithic buck converter in a cost-effective way by using high performance bondwire inductors.

1.3 Dissertation Outline

There are six chapters in this dissertation. In this chapter, the research background, the existing issues, and the prior-of-art solutions are presented. At the end of this chapter, the research objectives and the dissertation outline are given.

Chapter 2 describes the development of the self-synchronized rectifier, which includes brief introduction to the process technology and EDA tools used in the development, circuit design and simulation results, design considerations, layout design and experimental verification.

In chapter 3, we propose and demonstrate a new way to implement the high frequency synchronous flyback converter by using the novel self-synchronized smart rectifiers developed in chapter 2. We have discussed the existing schemes to realize synchronous rectification in flyback converter first. In chapter 3, the flyback converter with the smart

rectifier is designed, analyzed and simulated. We then demonstrate the new implementation through an experiment. The experimental results and explanation are also presented.

An integrated gate driver circuit, which includes gate drivers for both low-side and high-side power MOSFETs, is developed using high voltage (50V) isolated process technology in chapter 4. High-side driver is designed based on a concept of current source gate driver. A brief introduction is first given to the current source gate drive circuit. The whole procedure of the development including circuit design, simulation, layout, and package are presented in detail.

In chapter 5, we present a cost-effective way to realize power supply in package (PSiP) by using high-Q, high inductance bondwire inductor with ferrite epoxy coating. The prior-of-art techniques used in power supply integration has been briefly reviewed. In chapter 5, a introduction to the new bondwire inductor is given first. Then a synchronous buck converter is designed and implemented to demonstrate the new PSiP concept. Experimental results also are presented and discussed.

The dissertation work is summarized and concluded in last chapter. Some possible future work is also pointed out in the last chapter.

CHAPTER 2: SELF-SYNCHRONIZED RECTIFIER (SSR)

Power MOSFETs have been widely used as synchronous rectifiers in essentially all low voltage dc power supplies to improve the power converter's efficiency because of its low conduction voltage drop in comparison with regular P/N junction diode rectifiers [34][35][87][88]. However, as mentioned in chapter 1, the conduction of the body diode during deadtime results in both conduction loss and reverse recovery loss, which degrades the system efficiency considerably in high frequency power converters. The majority of the existing approaches to address deadtime control, unfortunately, suffer from the increased complexity and cost.

In this chapter, an integrated, high-speed self-synchronized rectifier (SSR) is designed, simulated, and fabricated, which offers remarkably simplified circuit design and reduced body diode power loss without employing an additional Schottky diode. The smart rectifier integrates a main low-voltage power MOSFET and a simple control circuitry that does not need external control signal input. High-speed and high-efficiency operation in the whole load range can be ensured by innovative control circuit. It is suitable for applications in both isolated and non-isolated DC-DC converters.

AMIS C5 process is used in the development of the SSR prototype. C5 is a 5V, 0.5-μm mixed signal CMOS process, but the minimum channel length is 0.6 μm. Double poly, 13.5 nm gate oxide thickness are used in the process. There are 2 or 3 metal layers available. To have good shielding protection for some critical paths, 3 layers of metal is used in our SSR prototype.

Virtuoso® Front to Back Design Environment v5.1.41 from Cadence™ is used for schematic input. Accurate circuit simulations have been performed with Spectre simulator in Analog Artist. Assura® is used for design rule check (DRC) and layout versus schematic (LVS) comparison during back-end layout physical design.

2.1 Concept of the Self-Synchronized Rectifier

Fig. 2.1 depicts the implementation of synchronous rectification technique in a conventional buck converter using an externally controlled synchronous rectifier. A PWM/PFM controller IC controls both high side MOSFET (Ctrl-FET) and low side

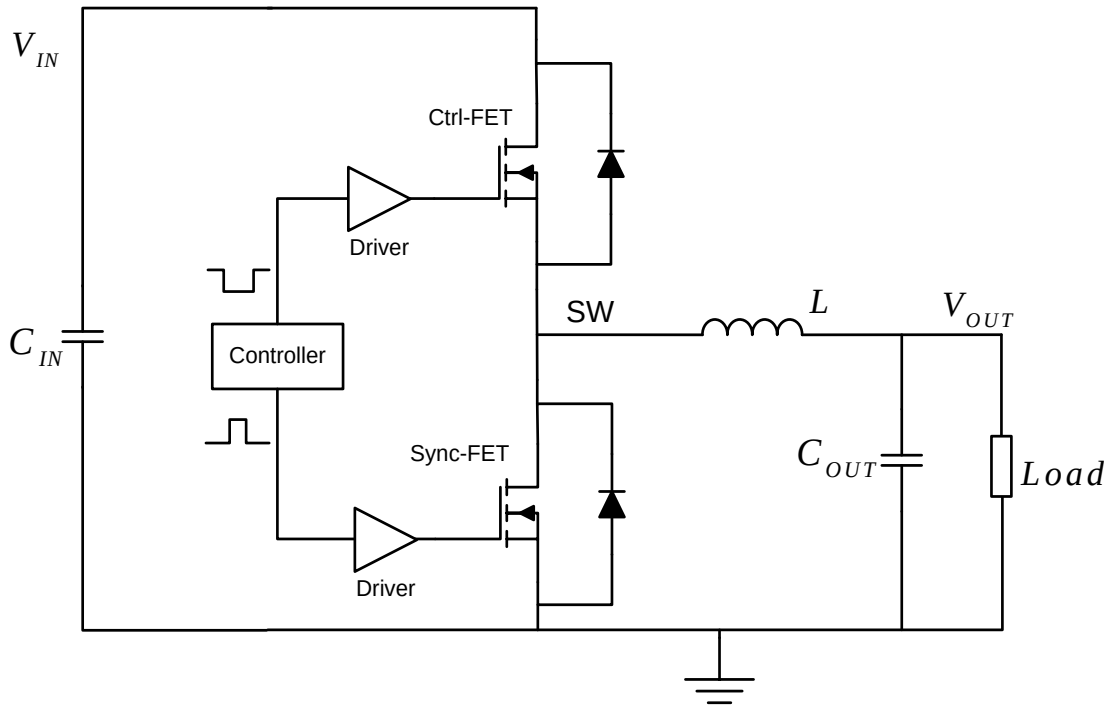


Figure 2.1 Conventional synchronous buck converter

MOSFET (Sync-FET). The logic signals (with deadtime) generated by the controller control both power MOSFETs through gate drivers. When the high-side MOSFET switch turns on, the inductor current rise linearly. When the Ctrl-FET is turned off, the low-side synchronous rectifier turns on to provide a current path for the inductor current to ramp down. In this topology, the dead time has to be generated inside the controller, and body diode of sync-FET conducts current during the dead time.

The concept of the smart self-synchronized rectifier is shown in Fig. 2.2. The self-synchronized rectifier consists of a synchronous MOSFET and an auxiliary control circuit to minimize body diode conduction during the deadtime and simplify the PWM/PFM control IC design. The core of the auxiliary circuit is a high-speed comparator which senses V_{DS} of the sync-FET and generates a control signal accordingly to switch the Sync-FET. When the Ctrl-FET is on, the Sync-FET is off and has a V_{DS} close to the input voltage V_{in} (e.g. 12V). The voltage comparator therefore outputs a logic "0" signal and keeps the Sync-FET off. When the Ctrl-FET turns off, the inductor current will start to freewheel through the body diode of the Sync-FET, and V_{DS} of the sync-FET becomes negative. A negative V_{DS} triggers the output of the voltage comparator to logic "1", and turns on the Sync-FET to carry the inductor current through its MOS channel. The smart rectifier doesn't need any external control signals. It automatically adapt to the switching operation of the Ctrl-FET. The Sync-FET only turns on after the Ctrl-FET turns off and it will turn off before the Ctrl-FET turns on completely. So the "break-before-make" control is automatically realized and no extra dead-time control circuit is needed. Since no dead-time control needs to be used to switch the Sync-FET and Ctrl-

FET synchronously, it is expected that the body diode losses can be reduced substantially comparing with the conventional synchronous rectifier.

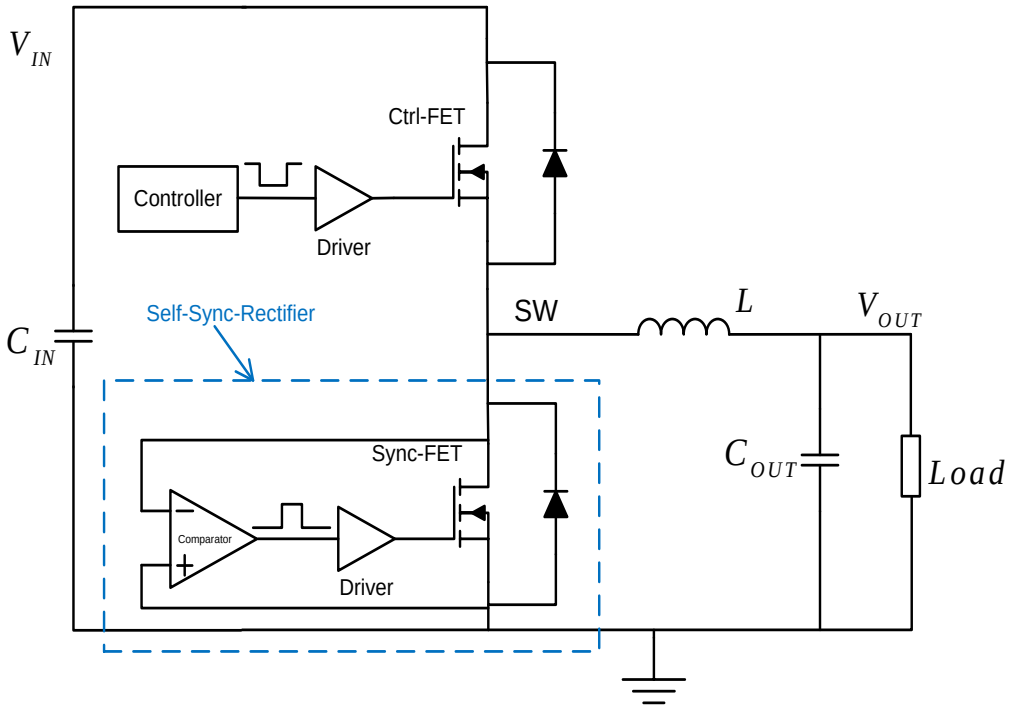


Figure 2.2 Concept of the proposed self-synchronous rectifier

A similar concept has been studied in [89]-[93]. However, the main objectives of the work in [89]-[93] are only to propose a simple control scheme to emulate power MOSFET switch as an ideal diode rectifier. Body diode conduction and the related power loss were not addressed. Furthermore, all the proposed schemes, only being tested in very low frequency (less than 110 kHz or DC) and over-simplified circuits, have not been experimentally verified in actual high frequency power converters and hence many important design considerations and possible issues were not pointed out.

The smart rectifier concept has also been implemented in some products [94]-[97]. All of these products can only work at low frequency due to fundamental design issues. The reported highest operating frequency is below 500 kHz[96]. Furthermore, they potentially suffer from high gate driving loss and switching loss at light load condition and hence low overall efficiency.

2.2 Design of the Self-Synchronized Rectifier

The block diagram of the proposed self-synchronous rectifier is shown in Fig. 2.3. The whole system consists of the following main blocks: current source, comparator, POR (Power On Reset), control and logic, and gate driver.The POR block offers some basic

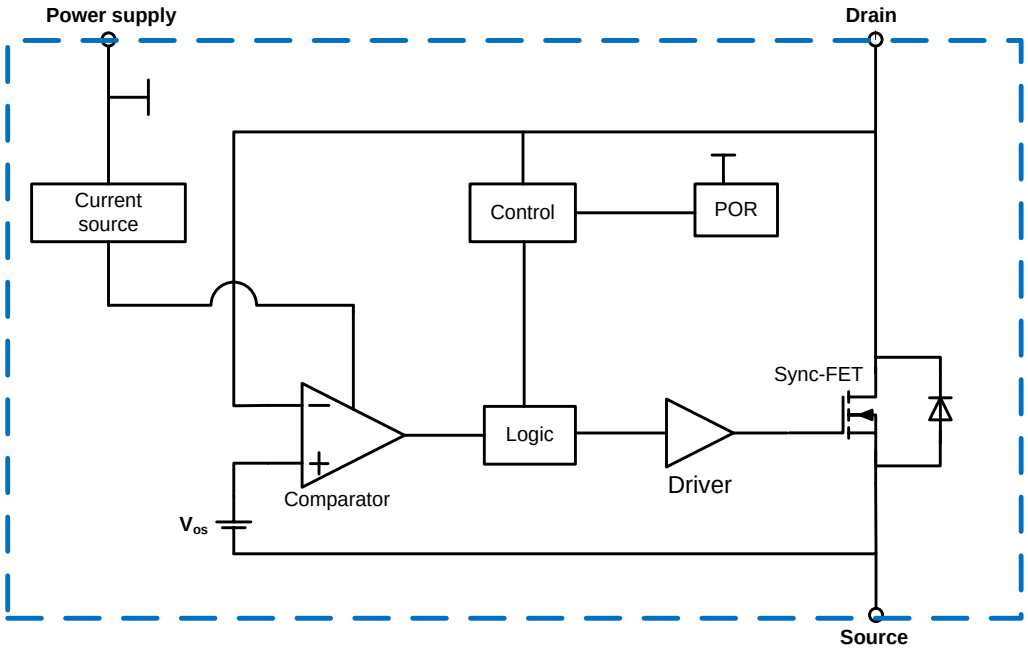


Figure 2.3 Block diagram of the proposed self-synchronous rectifier

protection function to ensure the gate of sync-FET is connected to ground if the power supply is below the normal operating voltage. The current source provides accurate current bias for the voltage comparator. The voltage comparator and control function blocks in our design have distinct features and will be discussed in detail.

2.2.1 Power On Reset (POR)

The POR block works like a UVLO (Under Voltage Lock Out), which generates a reset

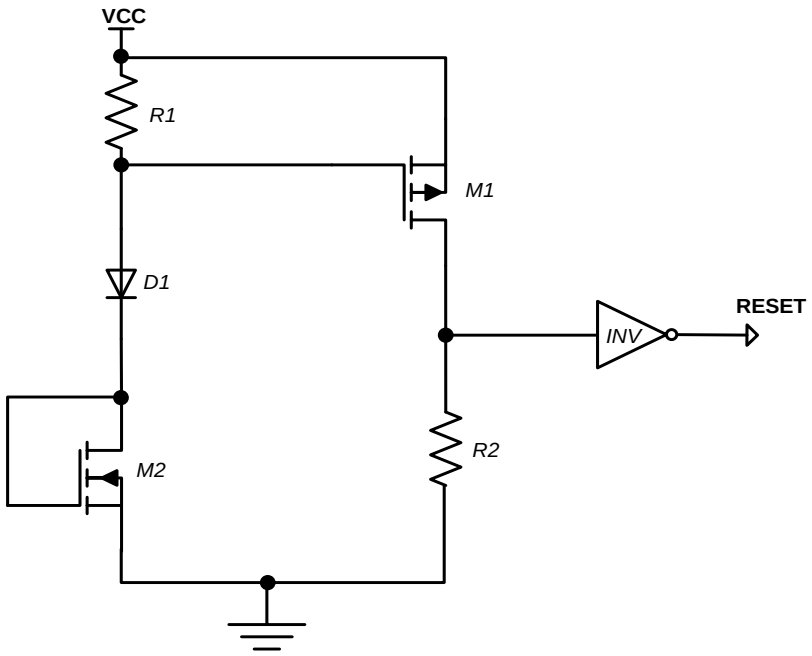


Figure 2.4 Power on reset

signal to ensure the Sync-FET stays off during the power on/off stage. When the power supply, V_{CC}, ramps to above 2V, the reset signal turns to low level (inactive). The control circuit starts to function normally. Only a rough UVLO is needed here, so a very simple

circuit structure, as shown in Fig.2.4, is used. The simulation results is presented in Fig.2.5.

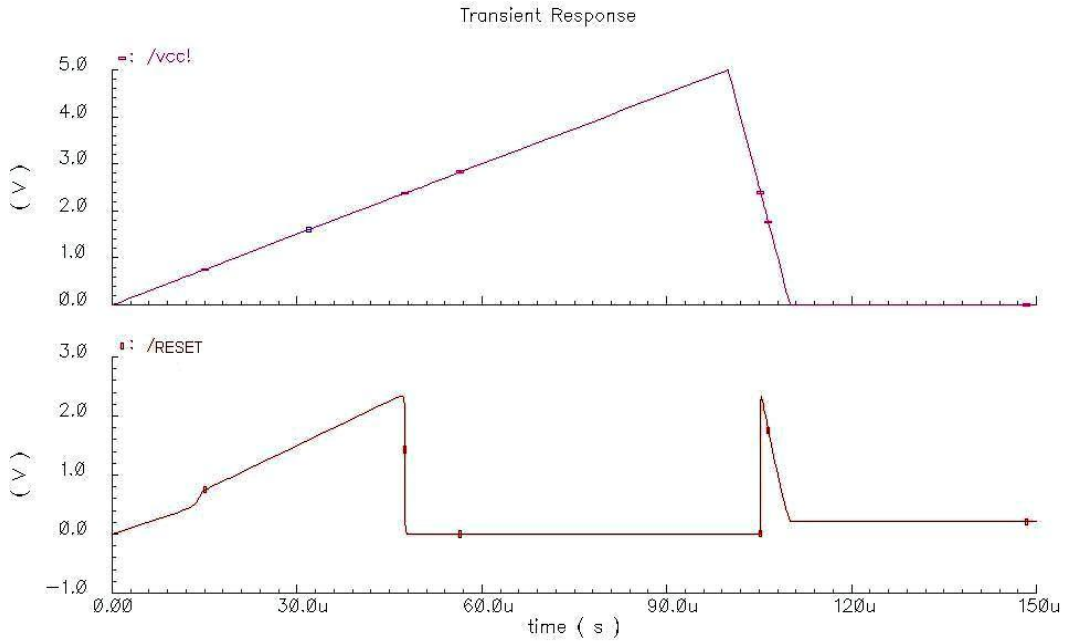


Figure 2.5 Simulated transient response of the POR (typical)

2.2.2 Current Source

This block generates a steady current source bias for the high speed comparator. A self-biased current source structure, including start up circuit as shown in Fig. 2.6, is used. The current generated from this circuit, I_{CS}, is expressed as below,

$$I_{CS} = \frac{V_{gs-M5}}{R} \tag{2-1}$$

where $V_{GS\text{-}M5}$ can be find from the following equation as long as M_5 is operating in saturation mode.

$$\frac{V_{GS-M5}}{R} = \mu_N \cdot C_{ox} \cdot \frac{W}{2L}(V_{GS-M5} - V_{th})^2 \tag{2-2}$$

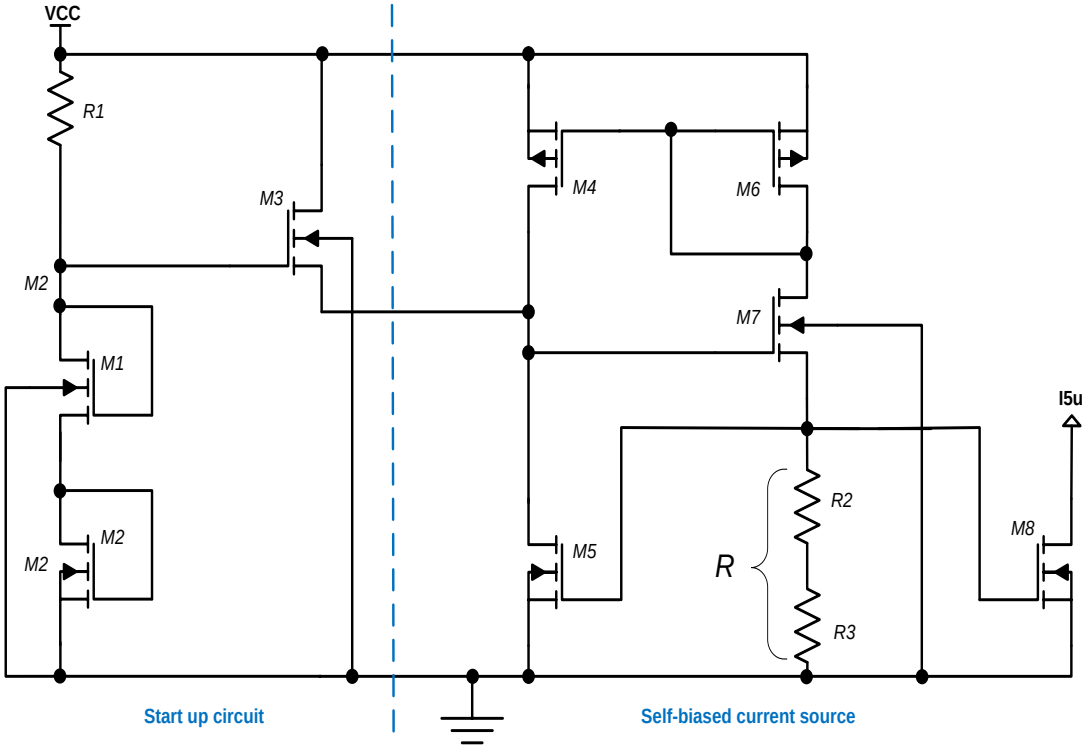


Figure 2.6 Current source circuit

So obviously, the current source is power supply independent. By appropriate selection of R, the temperature coefficient (TC) of V_{gs} and R may cancel each other, so a temperature independent current source can be obtained. In this work, both poly resistor (R_2, negative TC) and Nwell resistor (R_3, positive TC) are used. The design value of the output current

is 5 uA with typical model, $Vcc = 5V$ and $Temp = 27°C$. Typical simulation results are shown in Fig. 2.7 and Fig. 2.8.

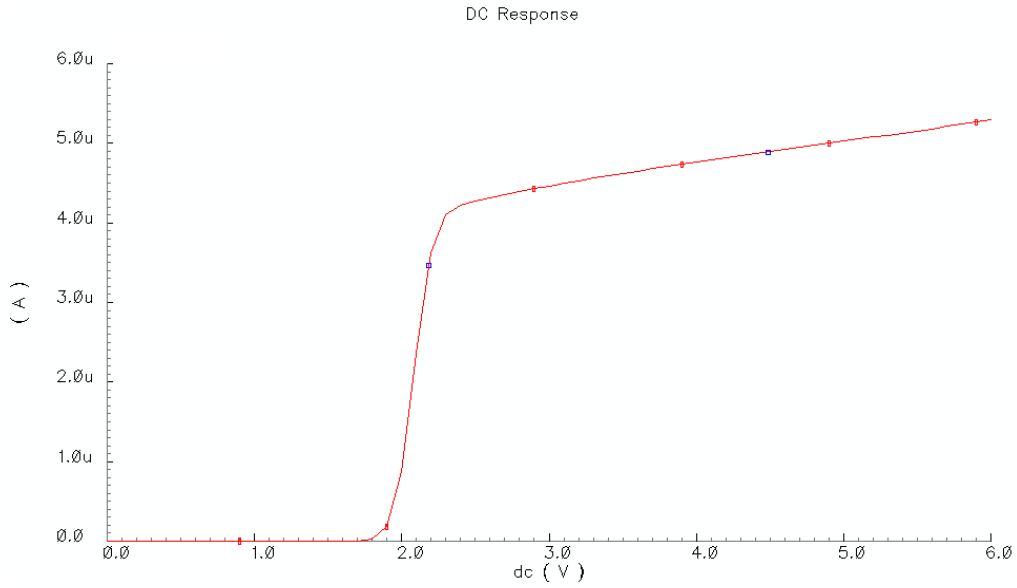


Figure 2.7 Current source power supply dependence (typ.)

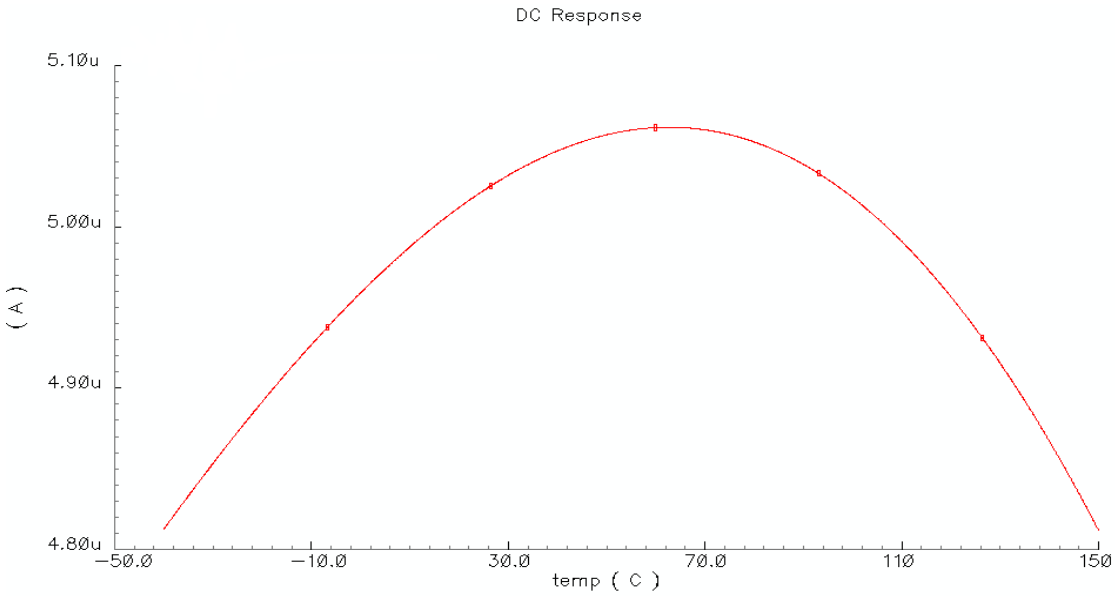


Figure 2.8 Current source temperature dependence (typ.l)

2.2.3 Comparator

The voltage comparator is the most critical function block of the self-synchronous rectifier. Propagation delay and input offset voltage are the two most important parameters for its design. A high-speed comparator can minimize the time during which the body diode conducts current and therefore reduce the diode power loss. Offset voltage (V_{OS}) is a measure of the accuracy of a voltage comparator. A large offset voltage may falsely trigger the voltage comparator. A low offset voltage leads to high accuracy, but may inadvertently degrade the dynamic response time. This is because a low offset voltage usually means large device size (which results in large parasitic capacitance) for good matching while a fast dynamic response time needs small parasitic capacitance to minimize the delay time. As shown in the simulated transient response waveform in Fig. 2.4, the propagation delay of the voltage comparator is approximately 10 ns in our final design.

A. Offset voltage polarity selection

If an ideal voltage comparator is used, zero-crossing V_{DS} detection should be realized in the self-synchronized rectifier. However, non-zero input offset voltage is the mostly likely case for the non-ideal nature of practical voltage comparators. V_{OS} serves as the reference or threshold voltage of the voltage comparator, and directly affects the timing of the sync-FET switching action. The overall efficiency performance of the converter will also be affected by the offset voltage.

For instance, if a small positive offset voltage of a few mV shows up in the voltage comparator as in [97][98], that is, the reference voltage is slightly higher than ground, as

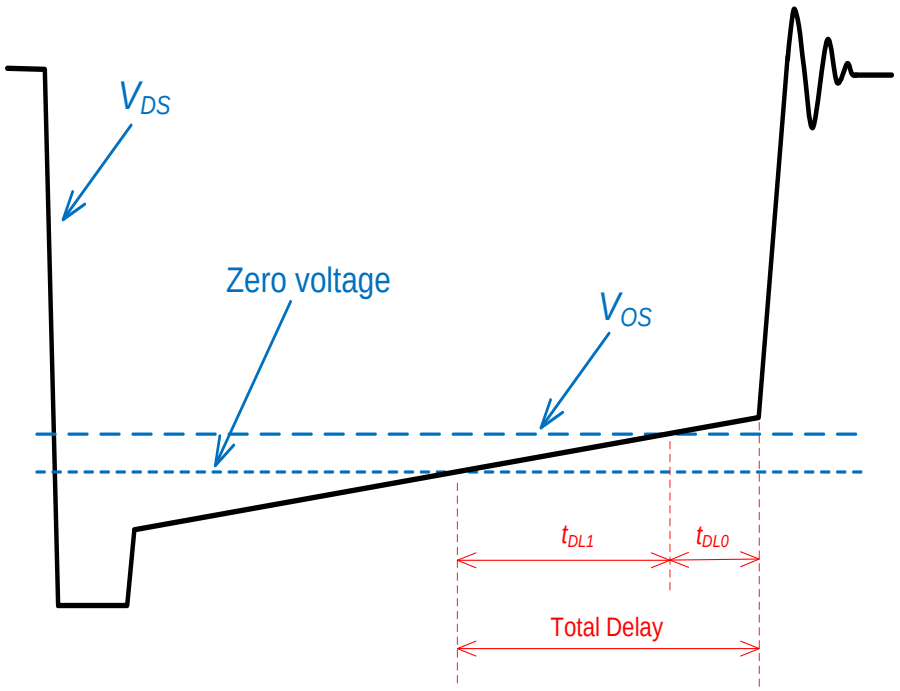


Figure 2.9 V_{DS} waveform of the sync-FET for $V_{OS} > 0$

shown in Fig. 2.9, the positive V_{OS} causes an much larger turn-off delay of the sync-FET when the ctrl-FET starts to turn on. The total delay, is the sum of t_{dl0} and t_{dl1}, where t_{dl0} is the propagation delay of the whole control circuitry including delay from comparator and driver, while t_{dl1} is the delay caused by the use of positive V_{OS}. The large turn-off delay limits the operating frequency range that this approach can be applied. Furthermore, the sync-FET has to conduct a large amount of reverse current (i.e. from drain to source), which means, in heavy load or continuous conduction mode (CCM), shoot-through may happen; and in light load, reverse inductor current may occur. Shoot-through current

flows from power supply to ground through $R_{DS\text{-}ON}$ of ctrl-FET and sync-FET, generates heat and lowers the overall efficiency. Reverse inductor current pushes current back into the circuit unnecessarily, wasting power and discharging output capacitor.

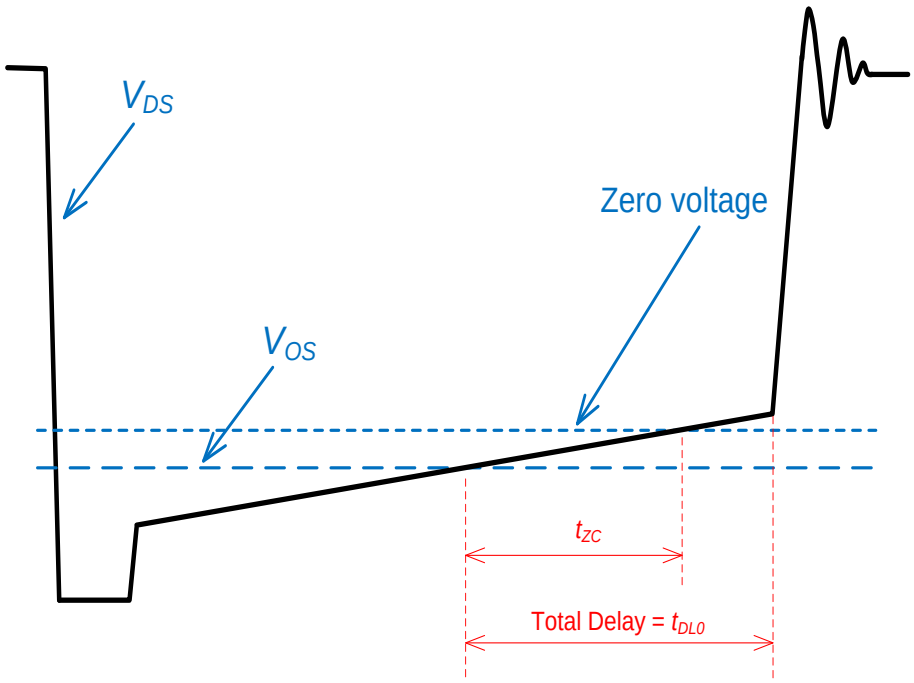


Figure 2.10 V_{DS} waveform of the sync-FET for $V_{OS} < 0$

On the other hand, a small negative offset voltage, as shown in Fig. 2.10, can be used to minimize the turn-off delay and improve the shoot-through problem associated with a positive offset voltage. In this case, the total turn-off delay of sync-FET equals to the propagation delay of the whole control circuitry, t_{DL0}. And if t_{DL0} is less than t_{zc} , which is the time interval from V_{DS} cross V_{OS} (the reference voltage of the comparator) to V_{DS} cross zero, sync-FET will be turned off prematurely and hence there would be no shoot

through at all. So negative offset in the voltage comparator tends to be more power efficient than a positive offset

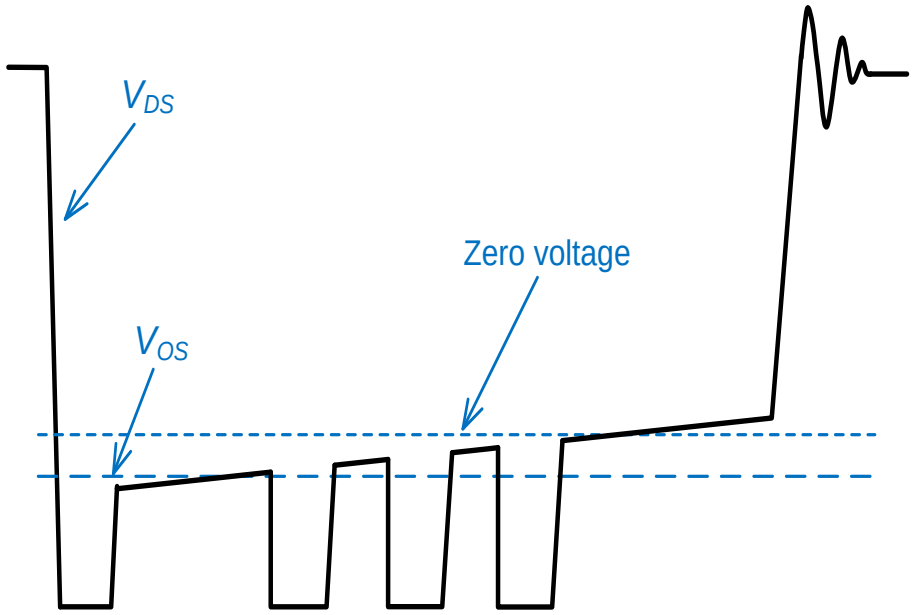


Figure 2.11 V_{DS} waveform with oscillation for $V_{OS} < 0$ under light load

However, negative offset may cause oscillation under light load condition as shown in Fig. 2.11. Under light load conditions, the inductor current becomes very small, and V_{DS}, (the product of $R_{DS\text{-}ON}$ and inductor current) may rise above V_{OS} very soon after sync-FET turns on. If this happens, the voltage comparator output will switch from high to low, and turn off the sync-FET. However, this would force the inductor current to flow through the body diode, and bring V_{DS} again to below V_{OS}. The sync-FET will turn on again if that happens.. Once sync-FET turns on, the voltage comparator output will switch again. So the oscillation occurs until the inductor current reaches zero. The oscillation results in repetitive on and off of the Sync-FET and a large gate drive and switching power loss.

In this work, we propose to use a small negative offset voltage combined with a new control logic to ensure the Sync-FET only turns on once in each switching cycle to avoid the oscillation and minimize non-necessary gate drive and switching loss at light load condition.

B. Circuit design

Voltage comparator is designed based on the consideration of negative offset voltage,

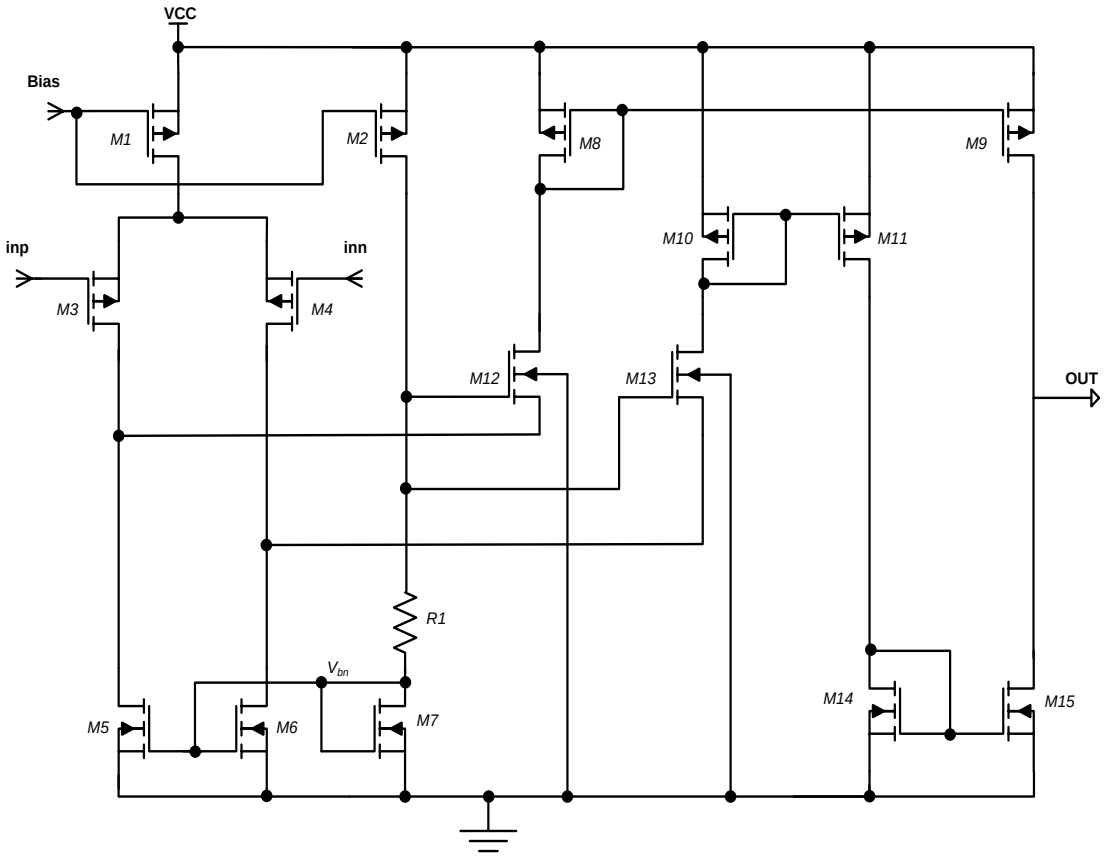


Figure 2.12 Schematic of the voltage comparator

minimized delay, and the input common-mode range (ICMR). The simplified final circuit of the voltage comparator is shown in Fig. 2.12.

The input common-mode voltage needs to go below zero. Therefore PMOS differential pair input stage and folded cascode structure are used. In this circuit, assume M_3-M_7 in saturation operating region, the low ICMR can be expressed as

$$ICMR_{LOW} = V_{bn} - V_{THN} - |V_{THP}| \tag{2-3}$$

where Vbn is the bias voltage at the gate of M_5-M_7, V_{THN} and V_{THP} are the threshold

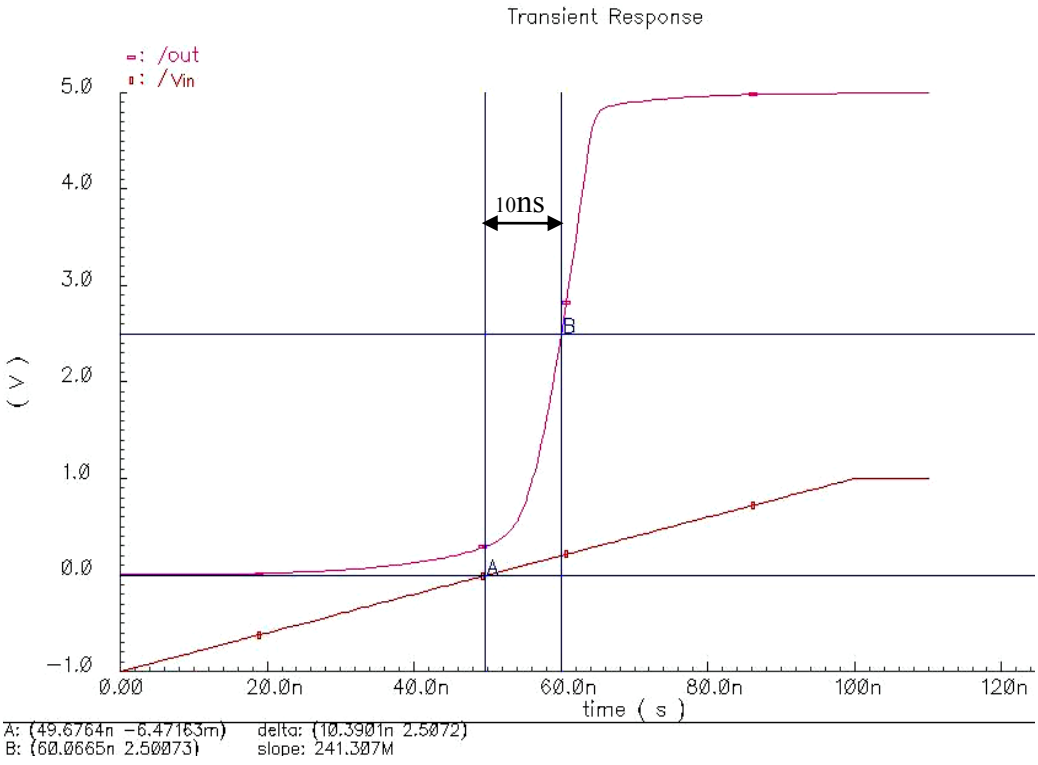


Figure 2.13 Propagation delay simulation for the voltage comparator (typ.)

voltage of NMOS and PMOS, respectively. So by proper setting up bias voltage , the ICMR can be met.

The delay of the circuit is mainly generated by bias current charging and discharging the node capacitors. In this circuit we try to reduce propagation delay by using relatively high bias current (typical total bias current is around 240 μA) and small device sizes. The typical delay is around 10 ns as shown in Fig. 2.13.

The offset voltage of the voltage comparator generally comes from two main sources:

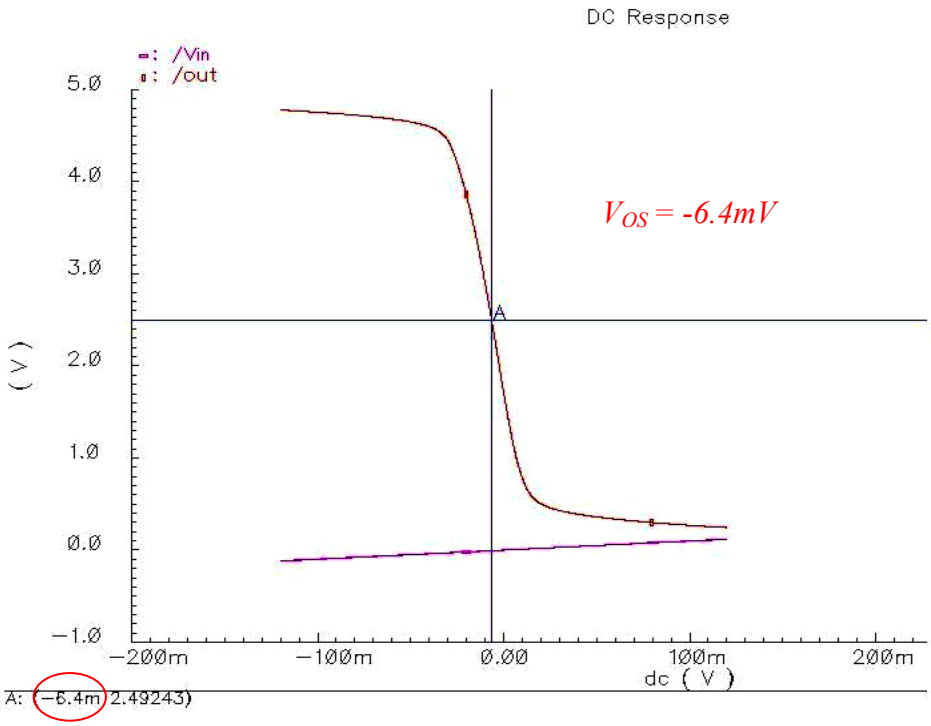


Figure 2.14 Voltage comparator offset voltage simulation

circuit design and fabrication mismatch. Circuit design may introduce an intrinsic or system offset voltage due to designated devices sizes and/or circuit structures. Nevertheless this part of the offset voltage can be controlled. In our design, we introduce a negative offset (around -6.4 mV as shown in Fig. 2.14). Offset caused by fabrication mismatch usually can not be directly controlled by the circuit designer. Yet a good layout design can help to minimize it. Statistical data from process technology shows that the MOSFET V_{TH} mismatch can be approximately calculated by [99]

$$\Delta V_{TH} = \frac{0.1 \cdot t_{ox}}{\sqrt{W \cdot L}} mV \tag{2-4}$$

where t_{ox} is the thickness of oxide layer and expressed in angstroms, W and L are MOSFET channel width and length, respectively, and in microns. If we substitute the device size and process parameter for our design: $t_{ox} = 135$, $W = 30$, and $L = 3$, we can get the V_{TH} mismatch is around 1.42mV. Therefore the -6.4mV should be negative enough to ensure the negative offset voltage in the final silicon chip to prove our concept.

2.2.4 Control Logic

Fig. 2.15 shows the detail of the proposed control logic. The control circuit is mainly composed of a mono-stable circuit and a D-type flip-flop. The mono-stable circuit input is tied to the drain of the sync-FET, and triggered at the falling edge of V_{DS}. The D-type flip-flop is designed with Set and Reset features. Its data input port is connected to ground, and its clock signal is tied to the output of the voltage comparator to be triggered at the falling edge.

In every switching cycle, when the ctrl-FET turns off, V_{DS} of the sync-FET drops below zero. The mono-stable output sets the D flip-flop to high level. The voltage comparator output then can turn on the sync-FET. Under very light load conditions, the comparator output goes to low once V_{DS} goes above V_{OS}. The comparator output serves as a clock

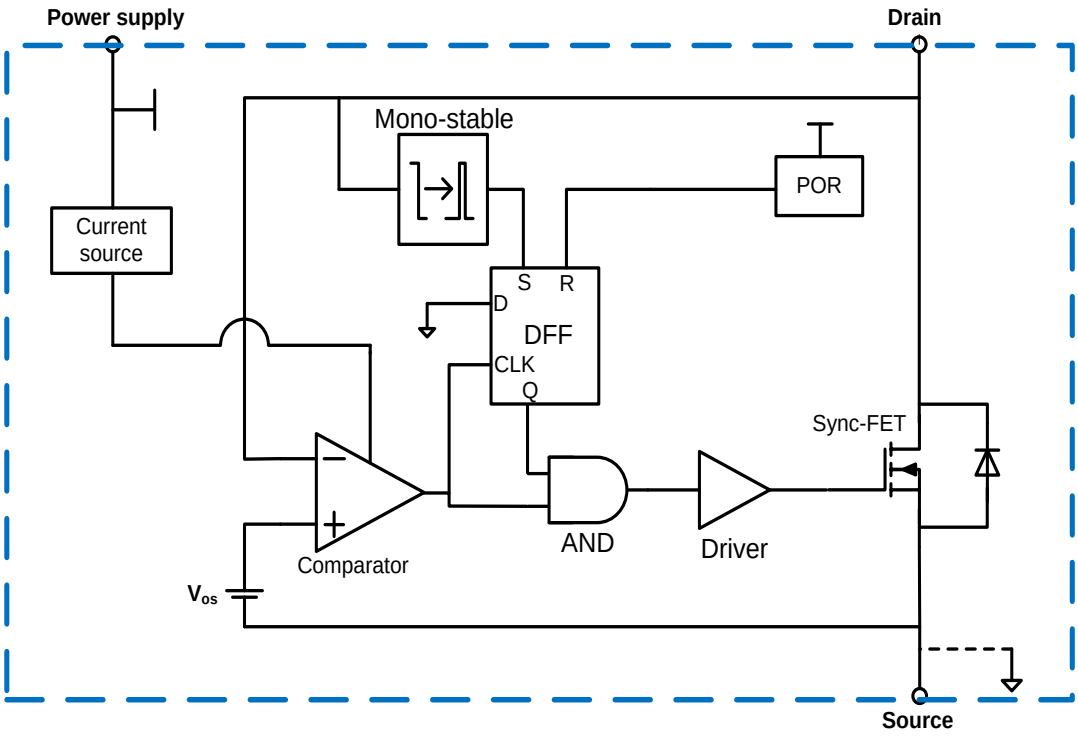


Figure 2.15 Detailed block diagram of the proposed SSR with the ONE-SHOT control

signal for the D flip-flop and the falling edge will make Q become zero. The low level Q signal will keep the sync-FET off no matter what the comparator output is until the next switching cycle. The repetitive switching ON/OFF of sync-FET at light loads is thus avoided. Fig. 2.16 and 2.17 show the circuit simulation result without and with the

proposed ONE-SHOT logic control. It is shown that there is only one pulse to turn on the sync-FET in every switching cycle with the control logic.

One drawback of this control logic is that a very small inductor current will be forced to

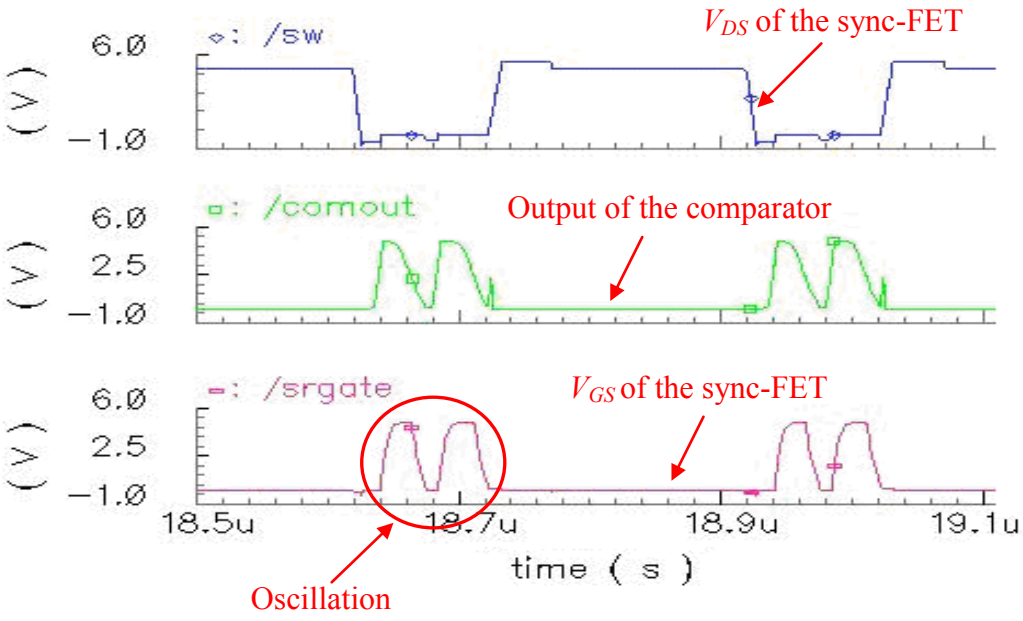


Figure 2.16 Simulation results for $V_{OS} < 0$ without the ONE-SHOT control

flow through the body diode after sync-FET turns off. This may introduce some power loss. But compared to the total gate driving loss and switching loss, this diode loss is relatively small because the current level is very low.

Estimation of the load current when oscillation happens is complicated because it depends on not only comparator design, power MOSFET, but also operating conditions of the buck converter. However, we can assume an extreme case as example, where the

product of peak inductor current and $R_{DS\text{-}ON}$ is equal to $|V_{OS}|$, then the light load current to trigger oscillation can be roughly estimated as below

$$I_{trigger} = \frac{|V_{OS}|}{R_{DS-ON}} - \frac{V_O}{2 \cdot L} \cdot (1 - D) \cdot T \tag{2-5}$$

where V_O is the output voltage of the buck converter, L is inductance value of the inductor in the buck converter, D is duty cycle, T is the period of the switching cycle.

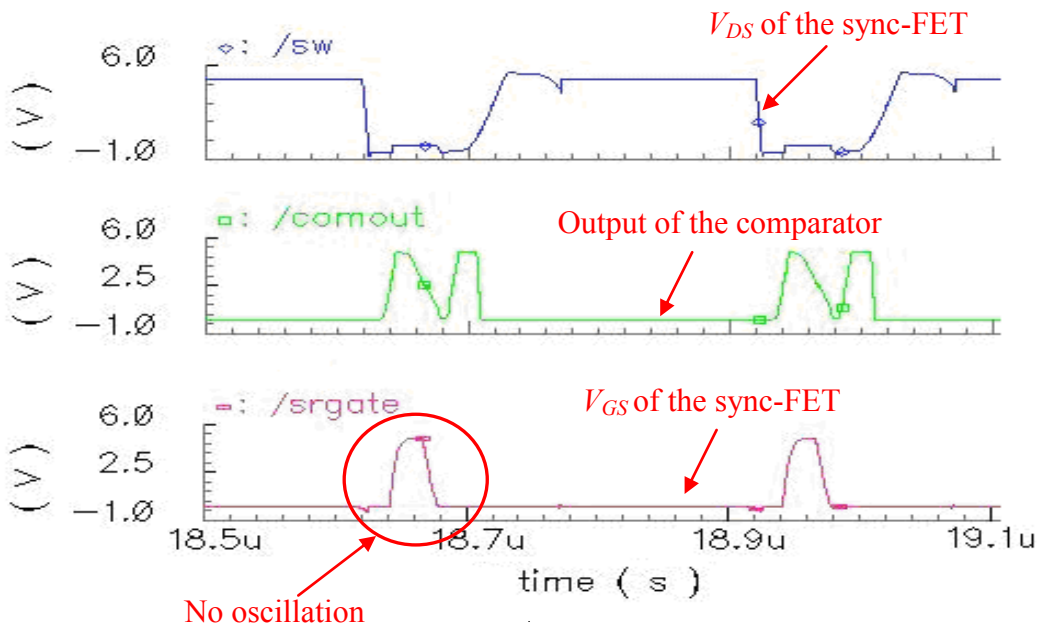


Figure 2.17 Simulation results for $V_{OS} < 0$ with the ONE-SHOT control

2.2.5 Gate Driver Design

The main consideration for gate driver of the power MOSFET is the propagation delay. A simple tapered inverter chain is used as the driving circuit. The tapering coefficient is 3 and 6 stages are used. Less than 10 ns of delay is achieved typically.

2.2.6 Physical Design

The proposed self-synchronized rectifier is designed using an AMIS C5 process. Special attention has been paid to the physical design to minimize the offset voltage variation of

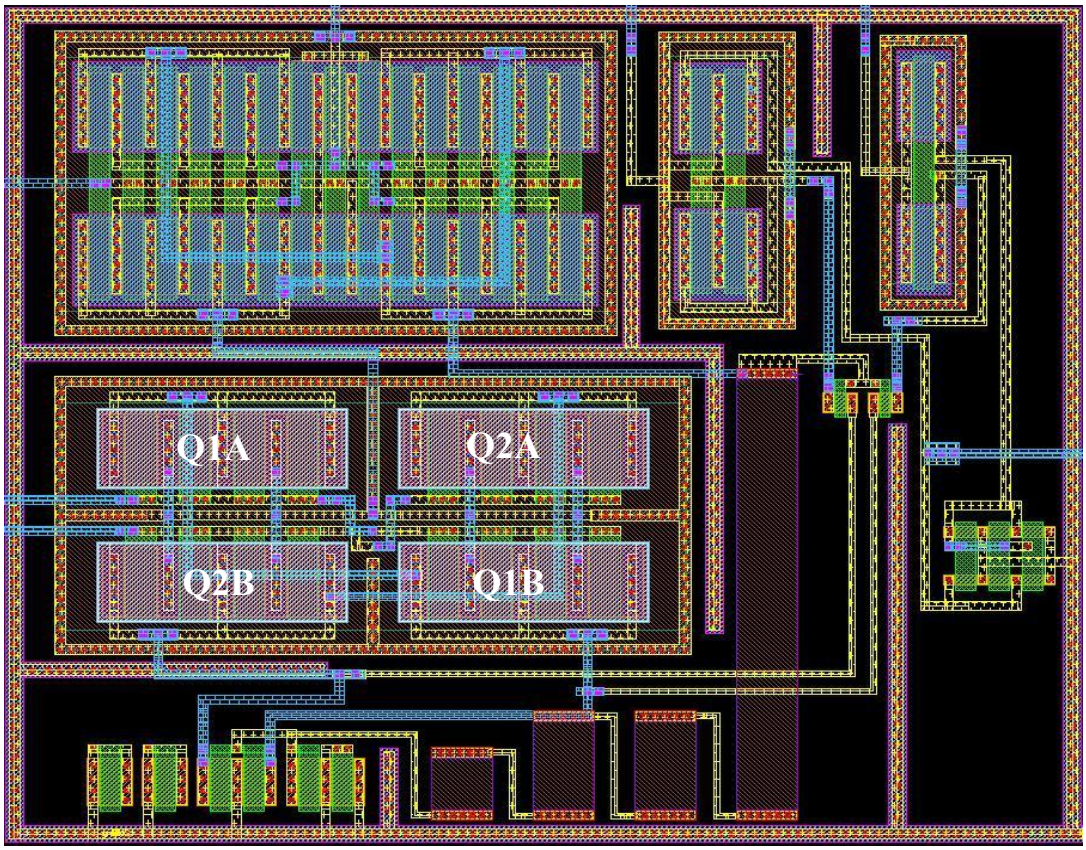


Figure 2.18 Layout of the voltage comparator

the voltage comparator. We have adopted a split layout strategy in which each of the input pair of the voltage comparator is split in half. The final layout of the comparator is shown in Fig. 2.18. It is worth noting that each input transistor is placed with half on the

upper left (or upper right) corner and the other half on the lower right (or lower left) corner in the layout.

In the top level design, the Kalvin probe path is used to sense V_{DS} of the sync-FET. Metal

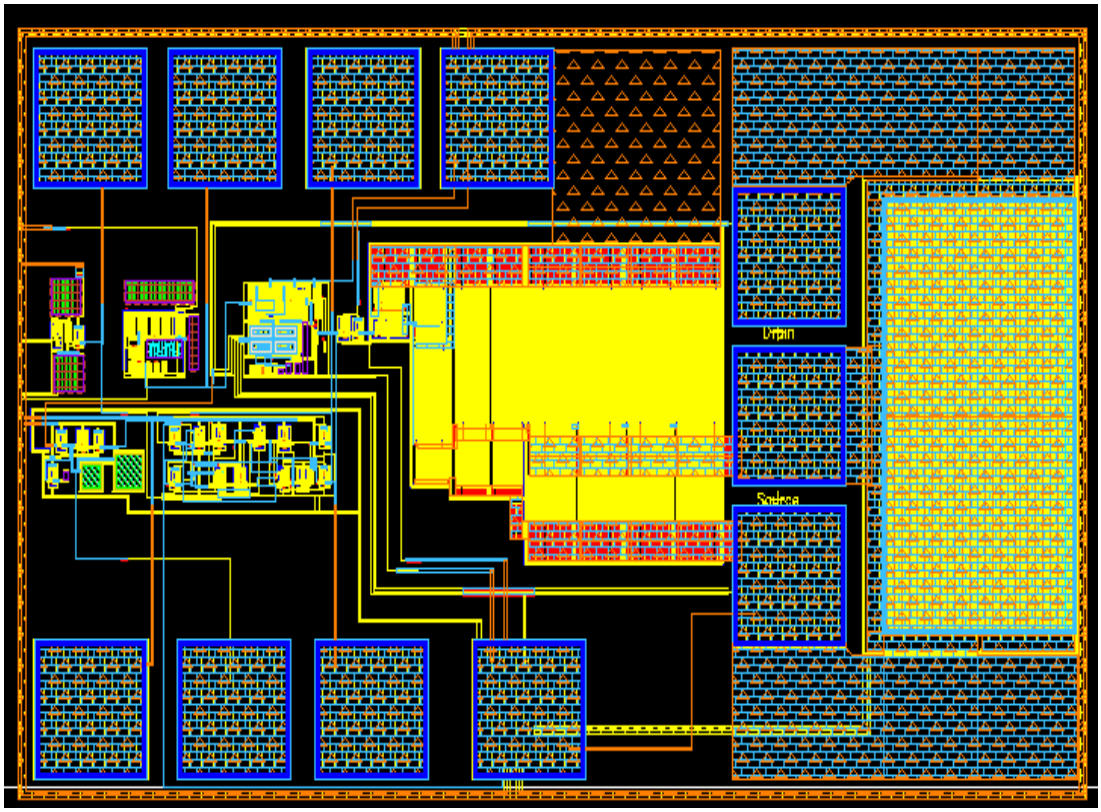


Figure 2.19 Top layout view

shield has been added along the whole route of the sensing wires. The two metal path connected from drain and source to comparator input terminals also have to be routed to have equal length and width. The top layout result is presented in Fig. 2.19. The total die size is 1.29×0.72 mm^2.

2.3 Experimental Results

Our design was successfully fabricated with the AMIS C5 0.5-μm CMOS process through MOSIS. Fig. 2.20 shows the die photo of the fabricated smart rectifier. In addition to the external drain and source pads, several internal probe pads are designed

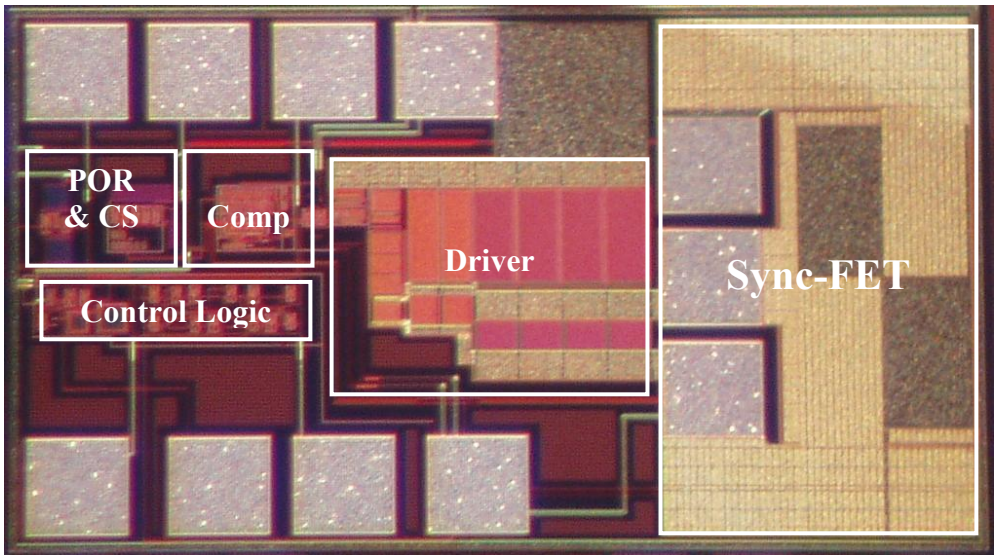


Figure 2.20 Photo of the self-synchronized rectifier chip

onto the chip to allow us to test the function of each individual block.

All the testing work has been performed by using wafer probe station with no package. Since there are no standard ESD protection devices available in the process design kit, only very basic diodes to ground and to power supply paths are provided for static charge discharging. Actually, there is no any guarantee that the ESD events can be protected in this case. Therefore, some measures have to be taken during the testing procedure. For

instance, all the probes have to contact with ground before contact with the pads on the die. Testing results are summarized in the following sub sections.

2.3.1 Testing of the Main Functional Blocks

A. POR block

Fig.2.21 and 2.22 show the measured waveforms of the UVLO (Under Voltage Lock

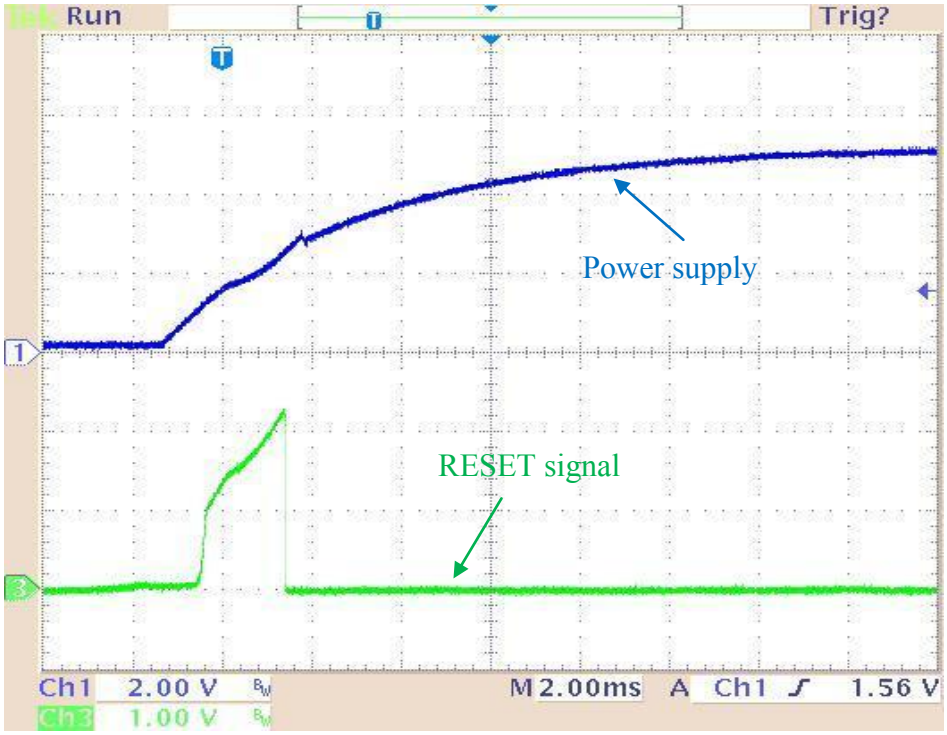


Figure 2.21 UVLO at Power-up transient

Out) function of the POR block during power up and down operation, respectively. Channel 1 is the voltage ramp waveform of the power supply. Channel 3 is the reset

signal of POR. It is shown that the reset signal becomes active when the power supply voltage decreases below about 2V, and inactive when the power supply increases above 2V. The testing results match simulation results very well.

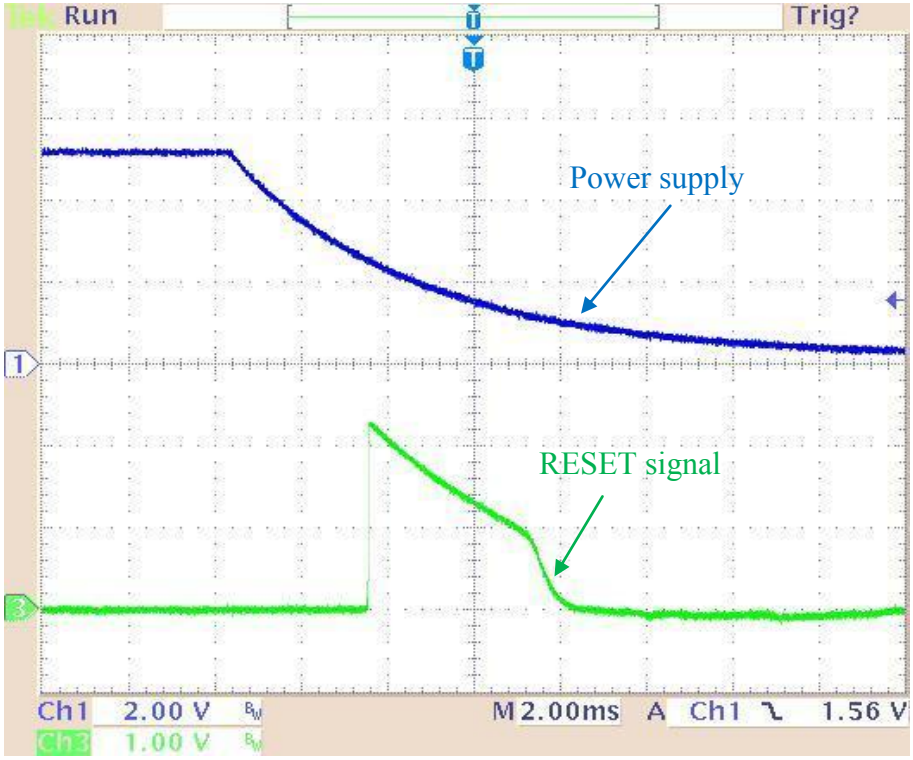


Figure 2.22 UVLO at Power-down transient

B. Current source block

Fig. 2.23 shows the measured characteristics of the current source on two different chips. The design target is 5μA output current source at 5V power supply voltage. The testing results are very close to it.

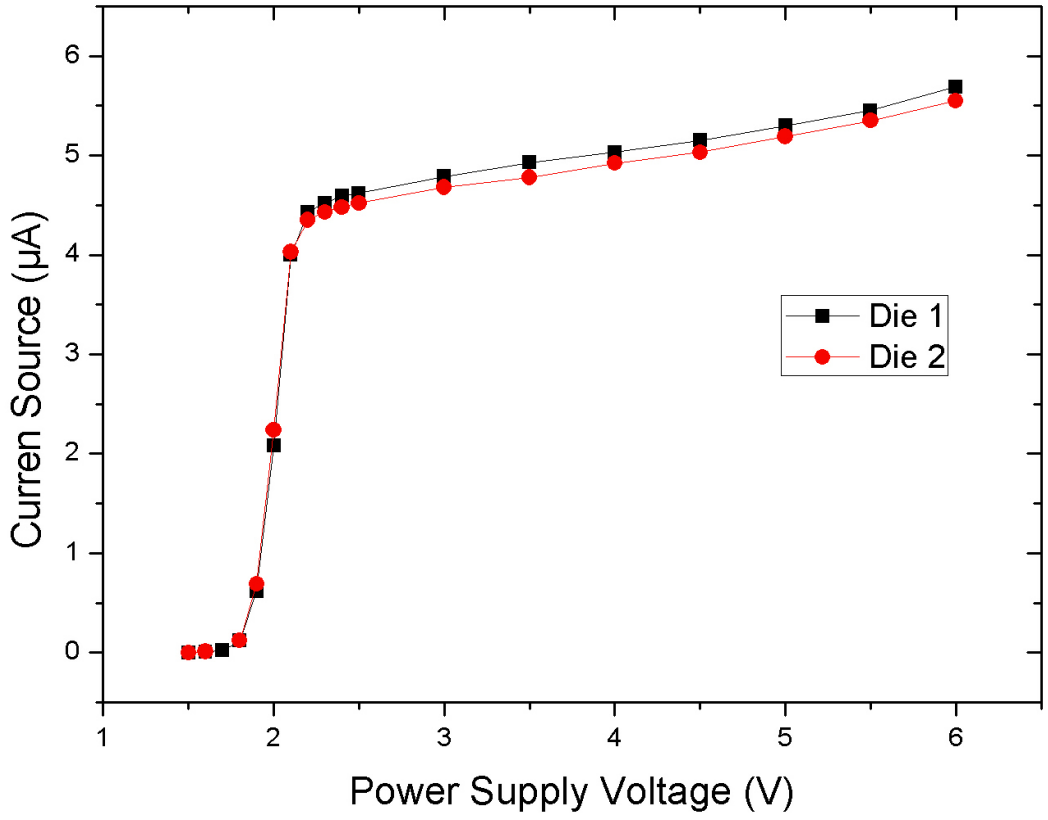


Figure 2.23 Current source testing results

C. Comparator testing

The comparator offset voltage was tested based on the open-loop configuration in Fig. 2.24. A dc power supply was connected to the inverting input terminal, which sweeps from negative to positive. The offset is the inverting input voltage when the output is $V_{cc}/2$. Fig. 2.25 demonstrates the measured transfer characteristics of the voltage comparator. The offset voltage is found to be around -13 mV, which is good for us to verify the operation of the proposed self-synchronized rectifier.

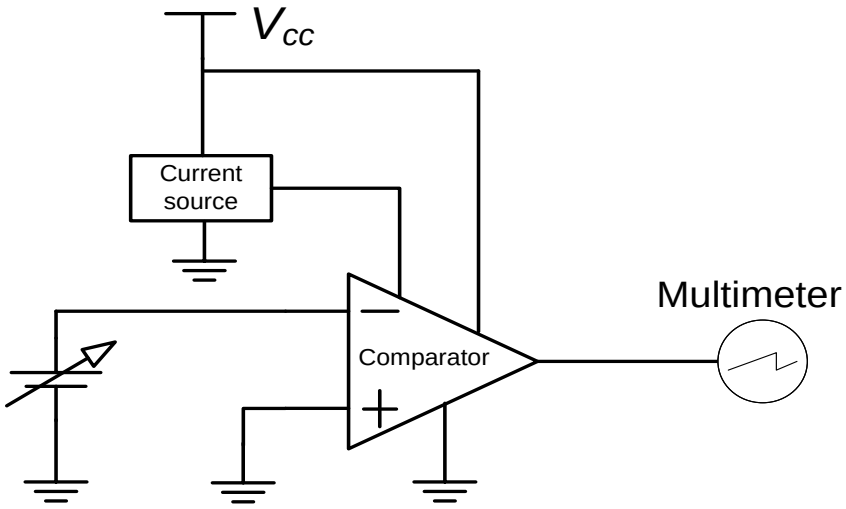


Figure 2.24 Comparator offset voltage testing setup

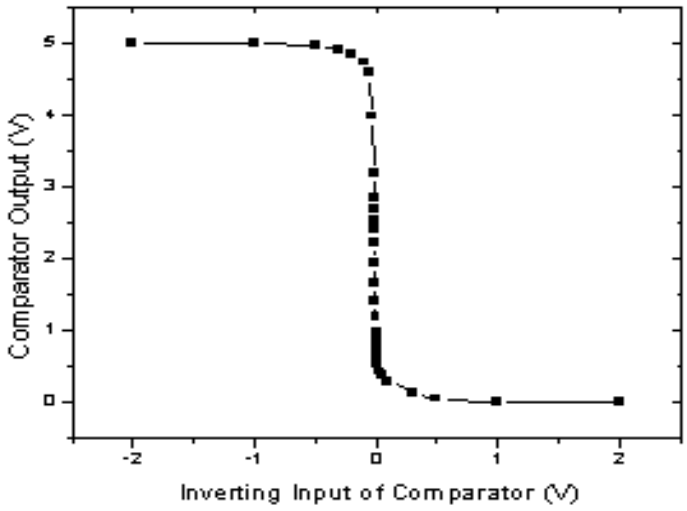


Figure 2.25 Comparator DC transfer characteristics

2.3.2 Testing of System Level Function

A buck converter shown in Fig. 2.26 is designed onto a monolithic IC chip to verify the operation of the self-synchronized rectifier design. All the devices inside the green

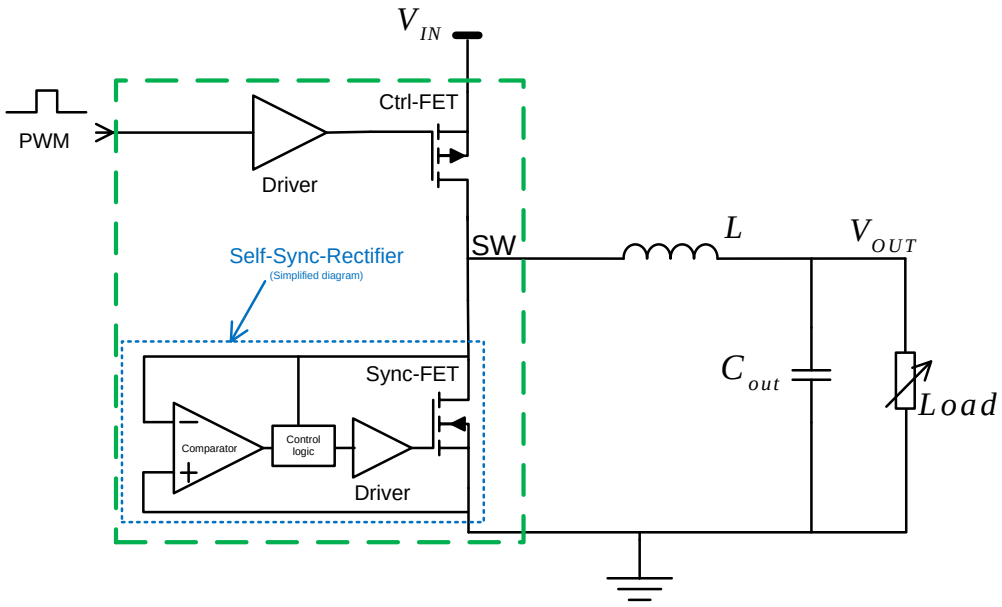
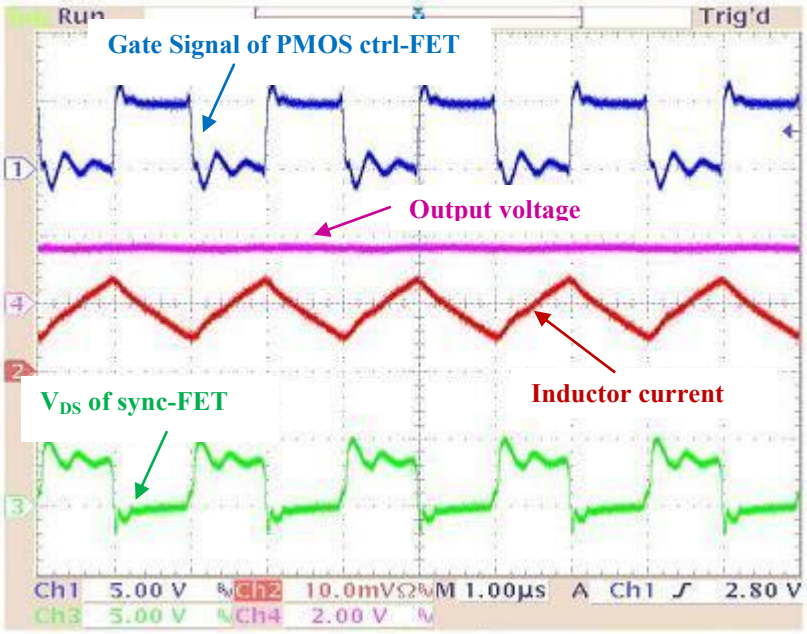
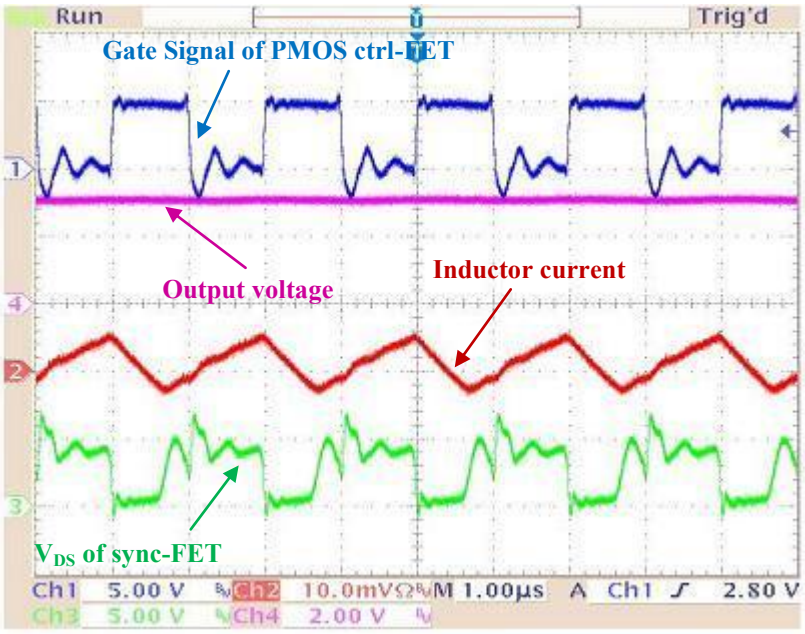


Figure 2.26 Simple buck converter testing circuit

dashed line box are integrated into one single chip. A pulse function generator is used to provide the input PWM control signal for the p-channel ctrl-FET. With $V_{IN} = 5V$ and input control signal duty cycle of 0.5, the measured waveforms are provided in Fig. 2.27 and Fig.2.28. With the adjustable resistor load, the system is tested in both heavy load of 120mA and light load of 40mA. PMOS (ctrl-FET) gate signal, inductor current, V_{DS} of the NMOS (sync-FET), and output voltage are shown in channel 1 to channel 4, respectively. No oscillation is observed in the waveform of V_{DS} even when the load current decreases into very light condition.



(a) Heavy load of 120mA



(b) Light load of 40mA

Figure 2.27 Measured switching waveforms of the buck converter at 500KHz

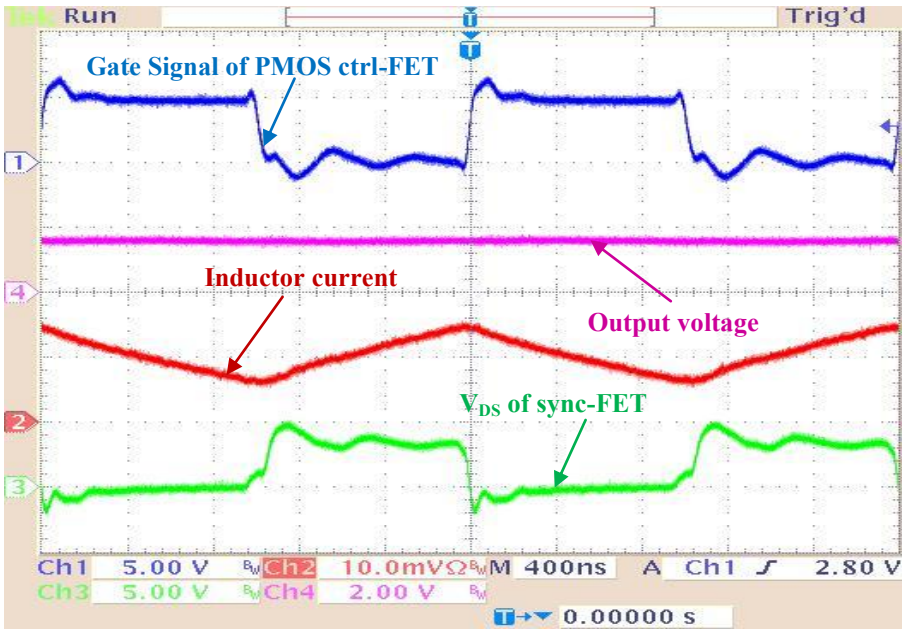


Figure 2.28 Measured switching waveforms of the buck converter at 1MHz

2.4 Summary

A monolithic self-synchronized rectifier (SSR) for DC/DC converter applications is presented in this paper. The analysis, simulation, design considerations, and fabrication of the SSR are described in detail. Actual application in a integrated buck converter has also been presented. Experimental results show that the SSR functions as designed. Compared to the prior work on smart rectifier concept [84]-[92], this work combines the following advantages.

1) Monolithic: Power MOSFET, driver circuit, control circuit and necessary protection circuit are all integrated in a single chip, which substantially reduces the components count and parasitic components. So smaller mounting area and better control accuracy can be achieved.

2) High speed: it can be operated in MHz range because of the use of negative threshold voltage and small propagation delay in comparator and driver design. Higher operating frequency is helpful to reduce the size of passive components in power converters.

3) High efficiency over a large range of load current. At very light load, it still maintains high-efficiency operation due to the elimination of the possible oscillation, diode emulation, and the DCM operation.

A comparison with some commercial products in the market is given in Table 2.1.

Table 2.1 Coparasion to the similar comercial products

	NIS6111 BERS™ IC (Better Efficiency Rectifier System)	IR1167 SmartRectifier™ Control IC	Self-Synchronous Rectifier (This work)
Integration	Co-packaged	Control IC and MOSFET separated	Monolithic
Switching frequency	Below 100KHz	Below 500KHz	Above 2MHz
Pin count	5	8(controller only)	3

CHAPTER 3: MEGAHERTZ SYNCHRONOUS FLYBACK CONVERTER

Isolated DC-DC converters are widely used as power supply in low-output-voltage applications where secondary-side synchronous rectification is usually required to improve system efficiency. However, as pointed out in chapter 1, the generation of a precise control and driving signal for the gate of the synchronous rectifier MOSFET has been a design challenge in terms of performance, system complexity, and cost. In this chapter, we propose and demonstrate a new way to implement a synchronous flyback converter by using the monolithic self-synchronized rectifier (SSR) [100]. The use of the SSR considerably simplifies converter design, improves system efficiency, and enables an operating frequency up to 4MHz. A demonstration board with 3.6V/100mA output was built and tested. Modeling analysis and ,measurement results are also discussed.

3.1 Proposed Flyback DC-DC Converter with the SSR

The proposed synchronous flyback converter is depicted in Fig. 3.1. The sync-FET in the secondary side of a conventional synchronous flyback converter is just simply replaced by the SSR chip in this implementation. The circuit shown in the dashed box is the subcircuit of the monolithic SSR as described in Chapter 2. It is basically a 3-terminal device. The real drain-source voltage drop, V_{DSs}, through the sync-FET switch is sensed to compare with a reference voltage V_{os} (<0) to decide the switching action of the SSR. The power supply pin, V_{CC}, could be biased in following ways:

1) Connecting V_{CC} pin to an auxiliary winding in secondary side. In this way, the isolation between primary side and secondary side and proper voltage for normal and safe operation of the SSR can be achieved.
2) Connecting V_{CC} pin to the same power supply in primary side (in case there's no isolation needed), to a bootstrap circuit in secondary side, or to the output voltage. In all these possible connections, the power supply voltage for the SSR chip has to be in the safe range for normal operation of the SSR.

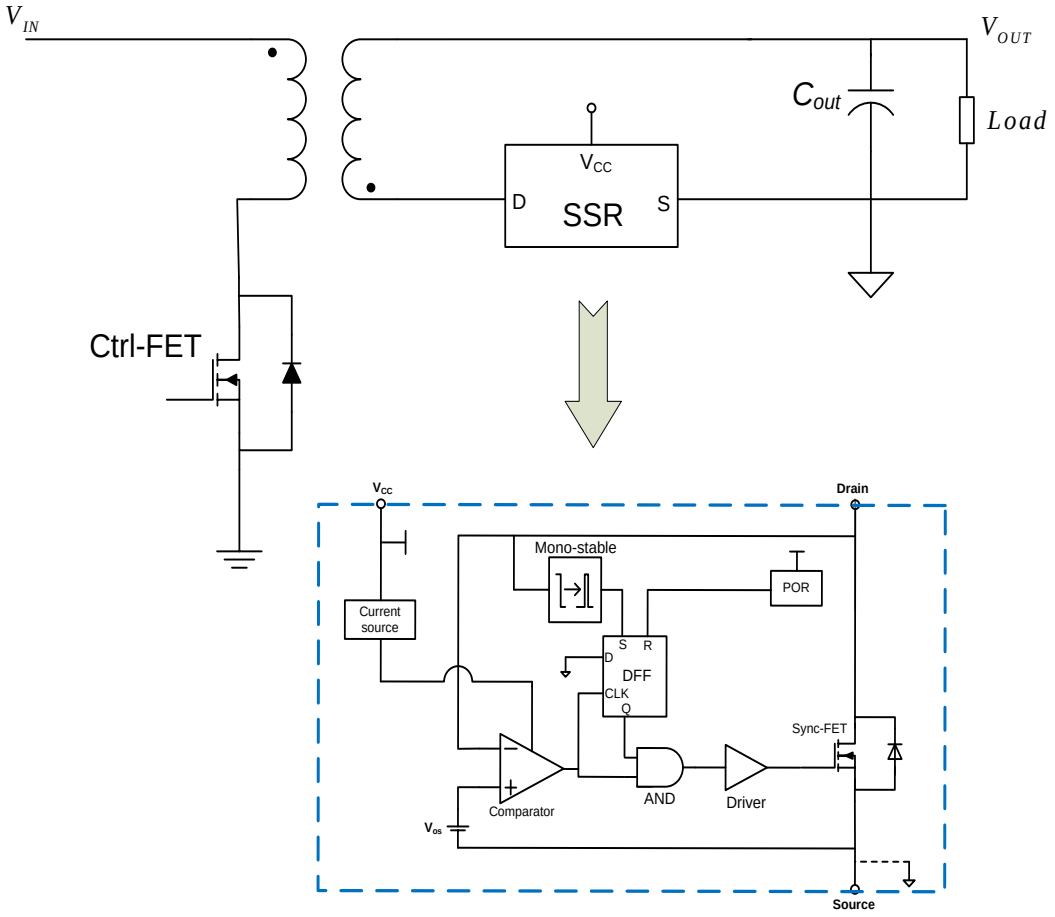


Figure 3.1 Proposed synchronous flyback converter with the SSR

3.2 Operation of the Proposed Synchronous Flyback Converter

To verify the operation of the proposed flyback converter, extensive accurate time-

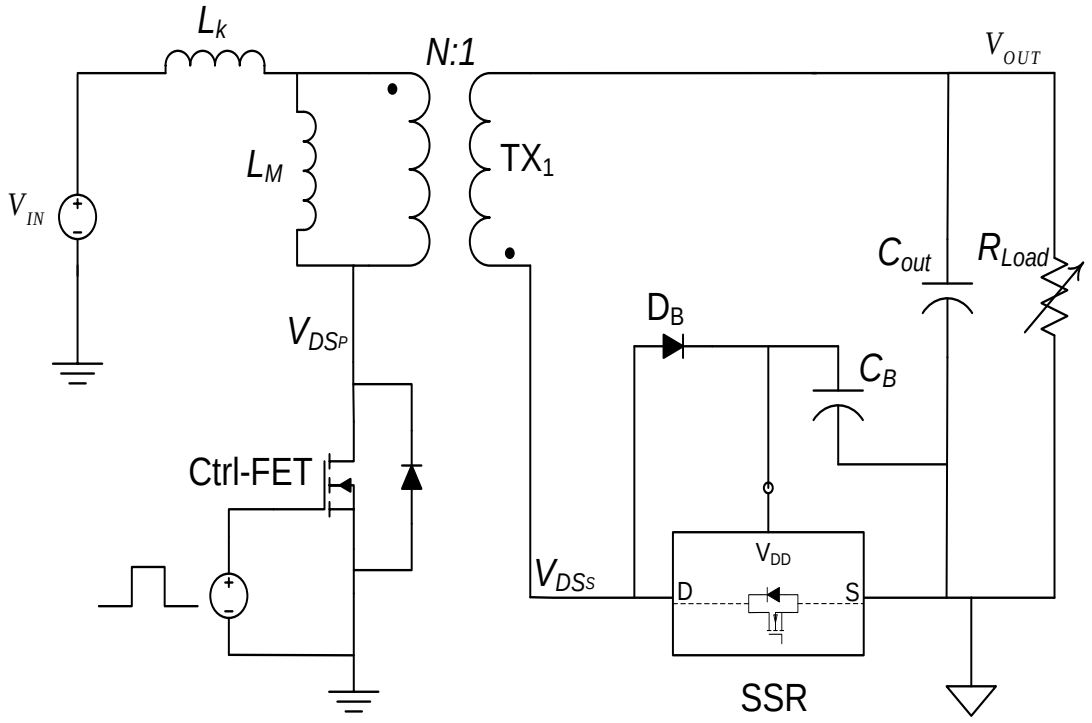


Figure 3.2 Circuit setup for simulations in Cadence

domain simulations have been performed in Cadence, the full-custom IC design environment, in which the monolithic smart rectifier was designed. The functional schematic used for simulation is presented in Fig. 3.2. The transformer is modeled by a leakage inductor L_k, a magnetic inductor L_M, and an ideal transformer TX_1 with a turns ratio of *N:1*. By the variation of the load resistor, the converter could be operated in both continuous-conduction-mode (CCM) and discontinuous-conduction-mode (DCM). At 18V input, 3.6V output, and 2MHz switching frequency, the simulation results are

presented in Fig. 3.3 (CCM) and Fig. 3.4 (DCM). The description of the circuit operation is given as follows.

In CCM operation, when the switch in the primary side, ctrl-FET, turns on, the SSR

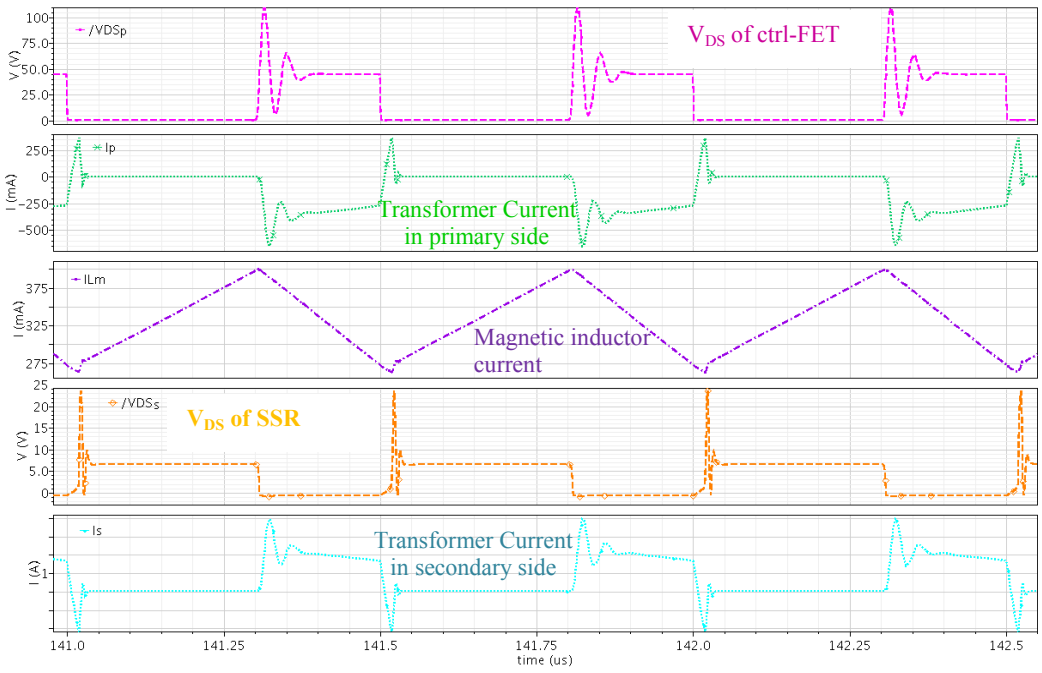


Figure 3.3 CCM Simulation

automatically becomes off. There is no current in both sides of the ideal transformer. The voltage drop across the magnetic inductor is close to V_{in}, so the current increases linearly and flows through ctrl-FET. The voltage drop across the secondary winding is V_{in}/N with reversed polarity, where N is the turns ratio from primary side to secondary side. Therefore, the voltage V_{DSS} of SSR can be written as.

$$V_{DSs} = V_{OUT} + \frac{V_{IN}}{N} = \frac{V_{IN}}{N} \cdot \frac{1}{1-D} \tag{3-1}$$

where D is the duty cycle of the control signal for the primary side switch, while V_{IN} and V_{OUT} are input and output voltage, respectively.

When the switch, ctrl-FET, turns off, the SSR is automatically turned on, so current flows in both sides of the ideal transformer. The voltage appearing across the secondary side

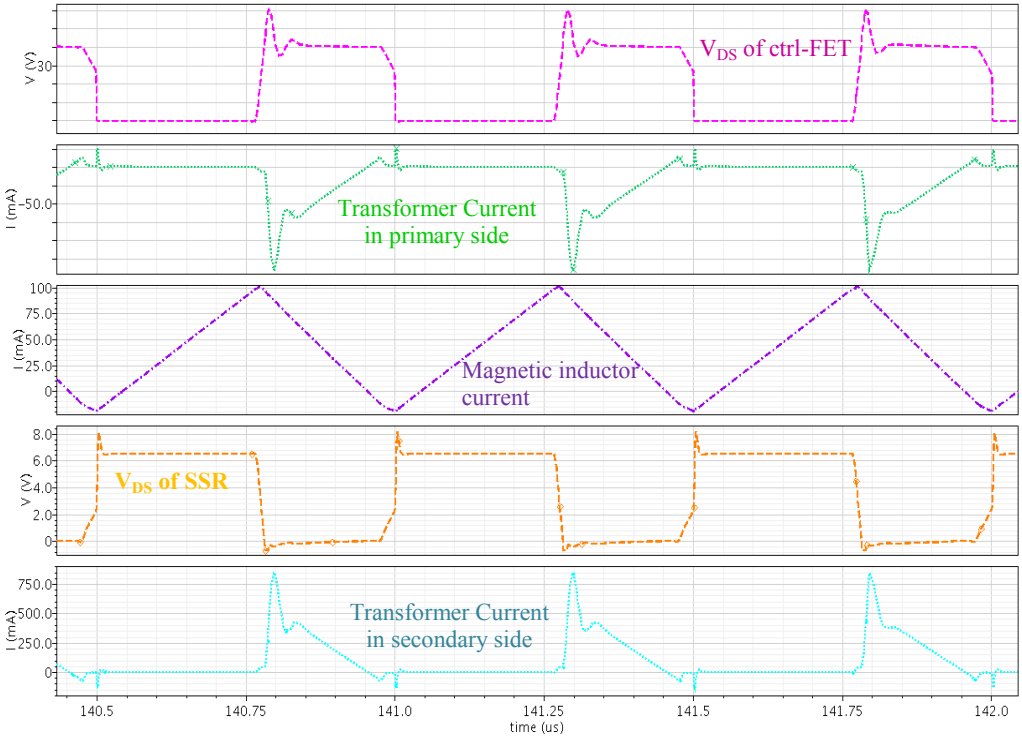


Figure 3.4 DCM Simulation results

winding is close to V_{out} (neglecting the SSR voltage drop). This voltage reflects to the primary side (and appearing across the magnetic inductor) as $N \cdot Vout$ with the reversed

polarity. Because the magnetic inductor has an constant reversed voltage drop, its current linearly decreases and circulates through primary side of the ideal transformer, which also induces current in secondary side. The voltage drop across the primary side switch, ctrl-FET, is given as

$$V_{DS_p} = V_{IN} + N \cdot V_{OUT} = V_{IN} \cdot \frac{1}{1-D} \tag{3-2}$$

Equations (3-1) and (3-2) can be used to determine the voltage ratings of the switches in both sides so that proper devices can be chosen accordingly. The peak current in primary side and secondary side to determine the current rating of the power switches are also given below

$$I_{pk-pri} = I_{AV} + \frac{\Delta I_L}{2} = \frac{I_{LOAD}}{N} \cdot \frac{1}{1-D} + \frac{V_{IN}}{2L_M} \cdot D \cdot T_{SW} \tag{3-3}$$

$$I_{pk-\sec} = N \cdot (I_{AV} + \frac{\Delta I_L}{2}) = I_{LOAD} \cdot \frac{1}{1-D} + \frac{N \cdot V_{IN}}{2L_M} \cdot D \cdot T_{SW} \tag{3-4}$$

where I_{AV} is the average magnetizing inductor. ΔI_L is the peak-to-peak current ripple of the magnetizing inductor. I_{LOAD} is the load current, T_{SW} is the switching period.

Under light load conditions, the secondary side current decrease to zero before primary side switch turns on. If SDSR is used, or if EDSR is used but control signal comes from primary side, there would be circulating current in the secondary side, which results in some energy transferred from output capacitor to secondary winding. With the use of the

SSR, before the current decreases to zero, the voltage drop across the sync-FET will trigger the comparator to turn off the secondary switch and thus no reverse current. However, the turning-off of the sync-FET before the current decreases to zero will force the very small current to flow through the body diode, which will trigger the turn-on of the sync-FET again. The repetitive on/off of the sync-FET increases gate driving loss and switching loss and therefore lowers the system efficiency. Fortunately, this would be suppressed by the one-shot control logic in the SSR.

During the switching transient, due to the existences of the transformer leakage inductance L_k and MOSFET output capacitor *Coss* (neglecting stray inductance and resistance), the turning-off of ctrl-FET or sync-FET will cause resonant oscillation in the L-C tanks of primary or secondary side, respectively. The resonance results in high spike in voltage and current waveforms, which actually increases the voltage and current stress in power switches. The resonant angular frequency ω_r and characteristic impedance z_r can be simply given as

$$\omega_r = \frac{1}{\sqrt{L_k C_{OSS}}} \tag{3-5}$$

$$z_r = \sqrt{\frac{L_k}{Coss}} \tag{3-6}$$

Compared to the prior topologies on the control of synchronous rectifier in flyback converters, the SSR solution has the following advantages. First, monolithic integration reduces parasitic components and overall converter size. Second, the DCM operation can

be easily realized. Third, the capability for high switching frequency allows further reduces the volume of passive components.

3.3 Experimental Results

We have designed and built a synchronous flyback converter with the monolithic SSR IC. which is a very simple design and only used to demonstrate the operation of the new flyback converter at high frequencies. To use the SSR IC, its safe operating area (SOA) has to be considered in the design. For example, the maximum voltage applied to the SSR, which can be calculated from equation (3-1), has to be less than the breakdown voltage given in the design rule file from the IC foundry (7V in this case). The final input and output parameters for the flyback converter are listed in Table 1.

Table 3.1 Design specification for the prototype flyback converter

Symbol	Description	Value
Vin	Input voltage	10~18V
Vout	Output voltage	2.8~4.2V
Iout	Output current	10~200mA
	Typical output	3.6/100mA

The demonstration board designed is shown in Fig.3.5. The transformer used in this design is C1453 from Coilcraft, which has a turns ratio of 6 from primary side to secondary side, magnetic inductance of 50uH, and lekage inductance of 1.1uH. With the use of this transformer, the typical duty cycle would be greater than 50%. The voltage

stress for the primary side MOSFET can be calculated from (2). A 80V MOSFET, FDS3812, from Fairchild is used in the design. Real parameters from these datasheets are used in the simulation presented in Section III. The monolithic SSR IC is packaged with a DIP-24 but only 3 pins being used. To show the real performances and operation of the proposed converter, there is no snubber circuit or clamp circuit. An over-voltage protection (OVP) circuit is used to prevent output voltage from over-voltage in the testing. To have a comparison, a DR and the SSR can replace each other as rectifier in the design. The rectifier diode used in the comparison is a Fairchild hyperfast diode, PHRP1560. The list of the main components used in the demo board is show in Table 3.2. Experimental results are summarized as follows.

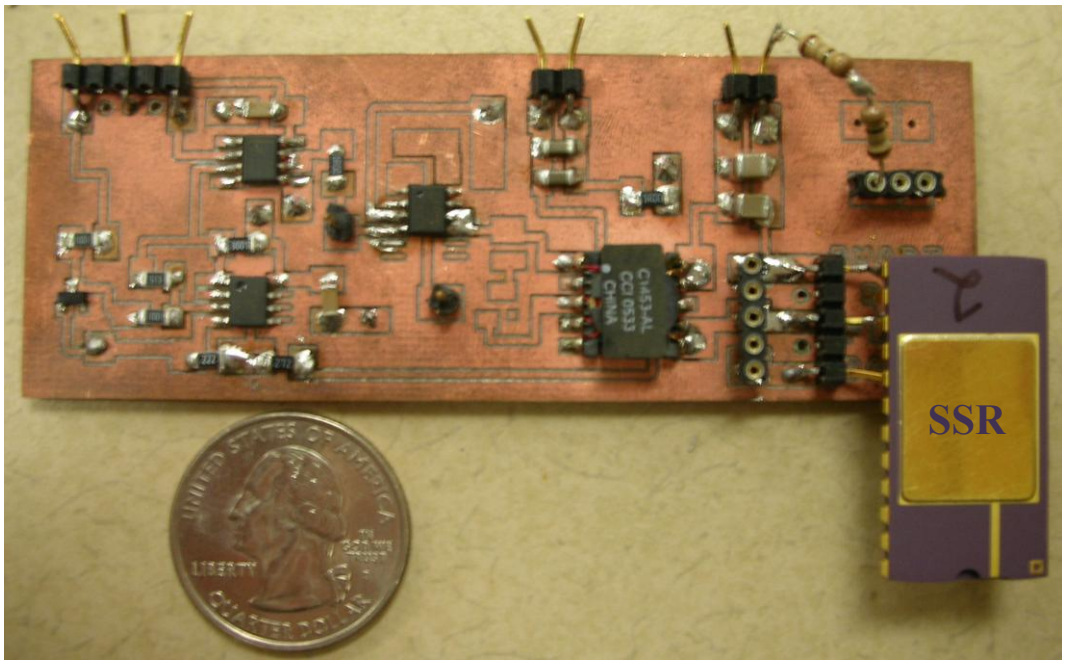


Figure 3.5 Prototype of the proposed flyback converter with the SSR

Table 3.2 Components list for the prototype flyback converter

Component	Manufacturer part #
Transformer	C1453
Ctrl-FET	FDS3812
Driver	UCC37322
Comparator (for OVP)	LM393A
Hyperfast diode rectifier (DR)	PHRP1560

Fig. 3.6-8 shows the V_{DS} waveforms of the primary side ctrl-FET switch and the secondary side SSR at 1MHz, 2MHz, and 4MHz operating frequency. The waveforms show that the SSR works normally even at 4MHz, which is the highest operating frequency observed in lab testing. The main limitation to the increase of the switching frequency comes from the parasitic components and the safe operating area (SOA) of the ctrl-FET and the SSR. After primary side switch turns off (and SSR turns on), the primary side leakage inductance and the output capacitor C_{oss} of ctrl-FET compose a resonant tank. The ringing can be seen on the V_{DSp} waveform. On the SSR waveforms, the ringing of the leakage inductance and the equivalent capacitor between drain and source terminals of the SSR can also be seen on V_{DSs} waveform.

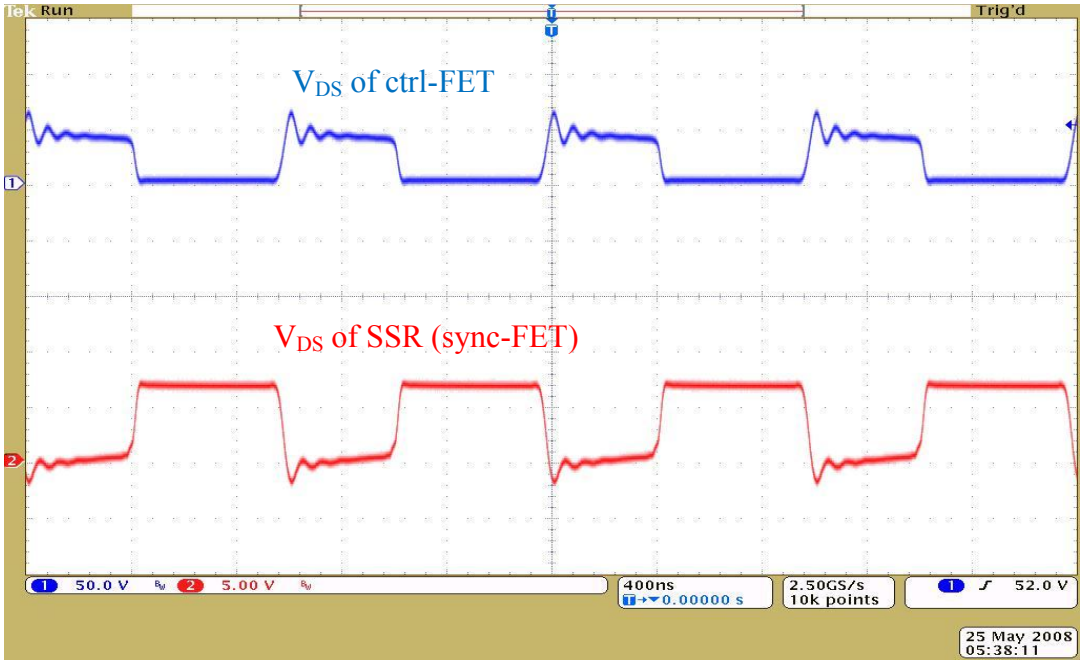


Figure 3.6 Operating waveforms at 1MHz

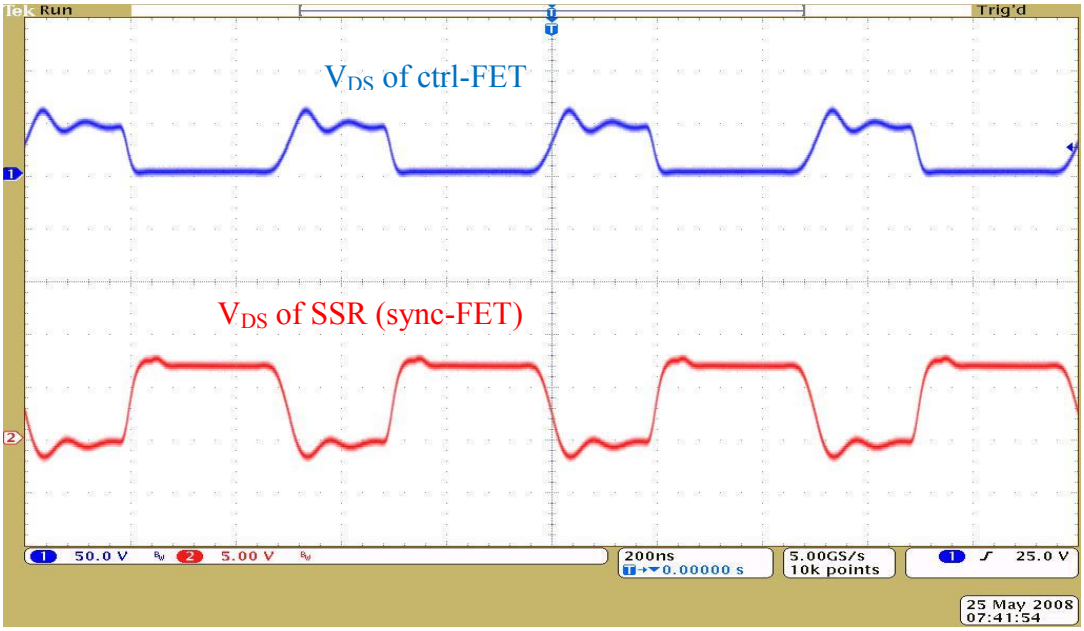


Figure 3.7 Operating waveforms at 2MHz

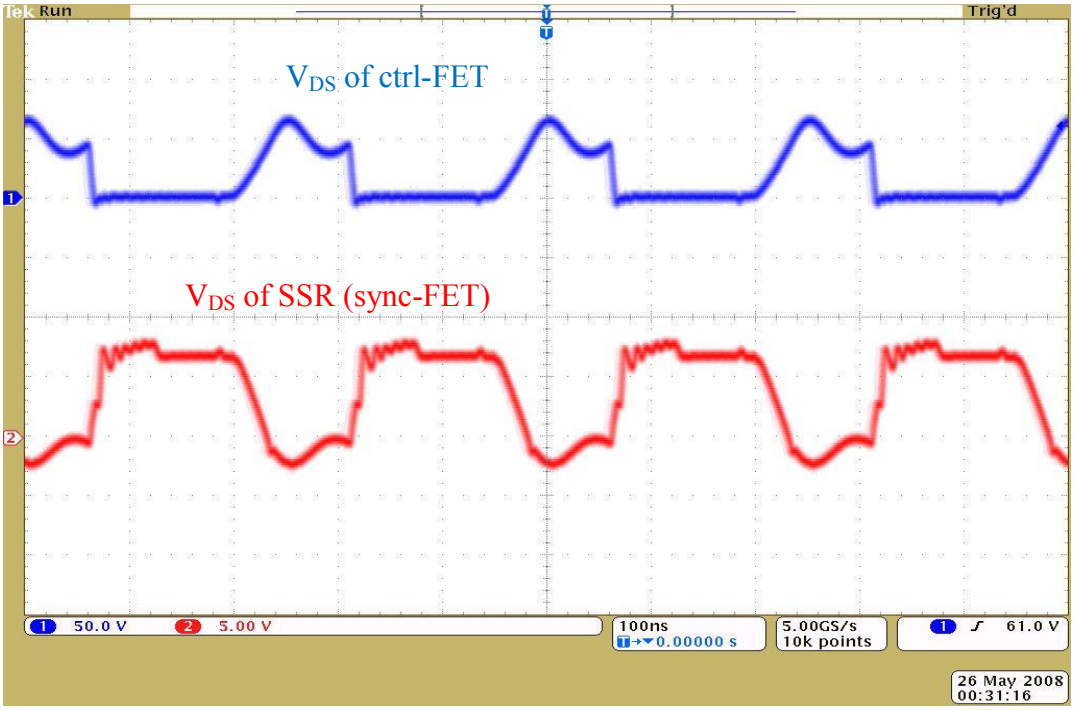


Figure 3.8 Operating waveforms at 4MHz

The efficiency performance of the prototype flyback converter has also been investigated. Fairchild hyperfast diode PHRP1560 was used to replace the SSR as a diode rectifier (DR) in the secondary side of the demonstration board. The efficiency when SSR is used was compared to that when DR is used. The testing was done with the typical output, i.e. 3.6V/100mA.

Fig. 3.9 presents the measured efficiency versus input voltage of the prototype flyback converter at the switching frequency of 1MHz. The results show that at high input voltage, SSR efficiency higher than DR efficiency. Vise versus. This is because at low

input voltage, the duty circle become very low, which means the conducting time of the SSR is very short. So the efficiency improvement from low conduction voltage drop may be outweighed by the increase in switching loss in high operating frequency when the SSR was used.

The measured efficiency versus switching frequency when input voltage is 18V are given in Fig. 3.10, which shows that by using the SSR, system efficiency could be improved by

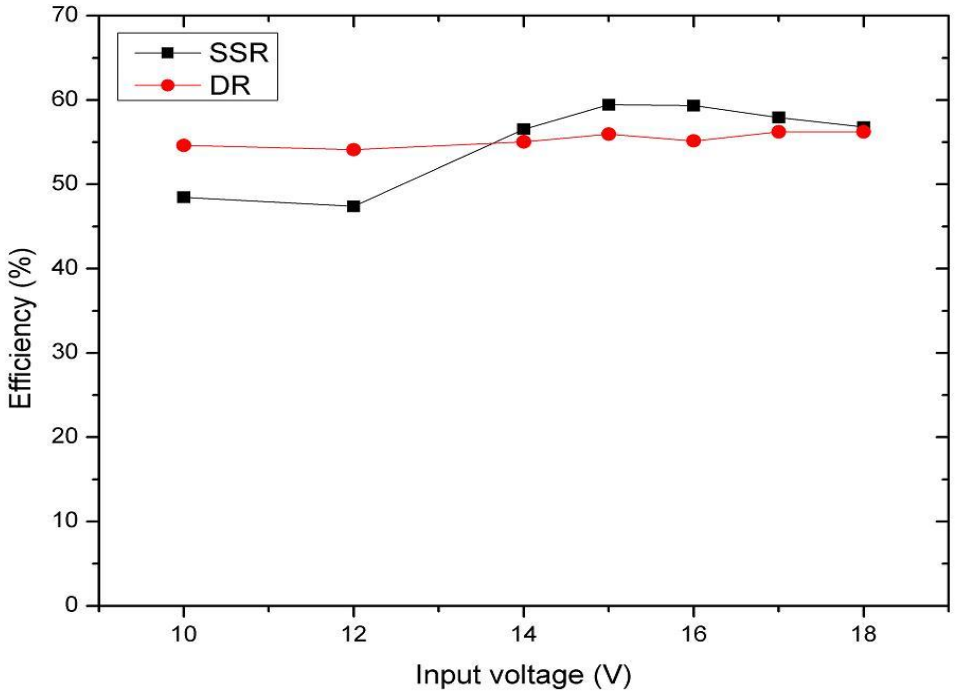


Figure 3.9 Measured efficiency vs. input voltage

up to more than 10%. For very low frequency, the flyback converter operates in DCM mode. For the same output power, a flyback converter works under DCM usually have a much lower efficiency than its CCM counterpart [101]. With the increase of the

frequency, switching loss dominant, the efficiency close to each other for both SSR and DR.

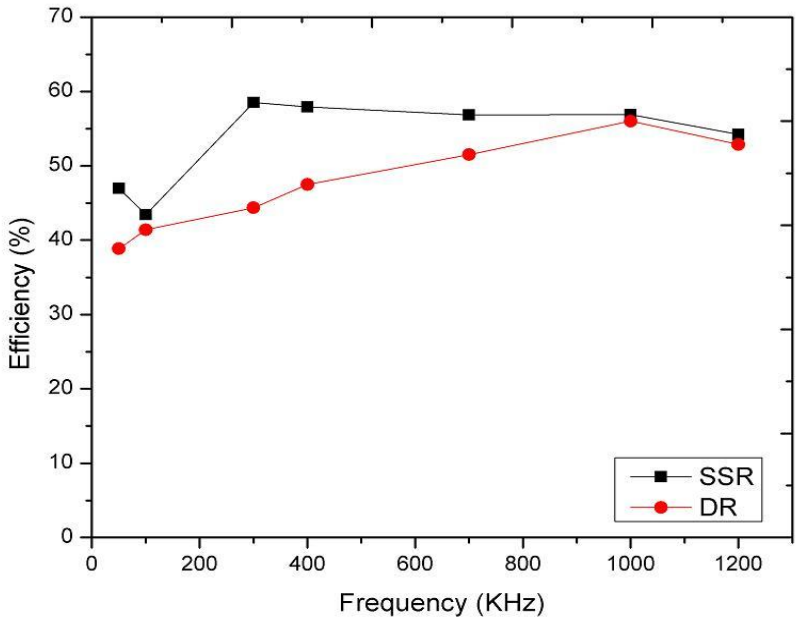


Figure 3.10 Measured efficiency vs. switching frequency

It should be mentioned that the efficiency for the prototyped flyback converter is relatively low for both SSR and DR cases. First reason for this is because the very high $R_{DS\text{-}ON}$ of the sync-FET, which is around 650 mΩ. The $R_{DS\text{-}ON}$ is limited by the available die size in the SSR design and the CMOS process itself. So it is expected to have higher efficiency by reduce $R_{DS\text{-}ON}$. Secondly, the 3.6V/100mA application can not take full advantage of the synchronous rectification technique, which would be most beneficial to efficiency improvement in low-output-voltage and high-output-current applications. The reason why 3.6/100mA application is chosen is also limited by $R_{DS\text{-}ON}$. The voltage drop

across the SSR will be very high if high current is flowing through. Finally, the demo board, which is used just for the demonstration of the new scheme to realize synchronous rectification in flyback converter, is not optimized for efficiency performance. Since there are no any clamp or snubber circuits, large current and voltage spikes degrade the system efficiency.

3.4 Summary

In this chapter, we experimentally investigate the new scheme for synchronous flyback DC-DC converters with the use of the monolithically integrated self-synchronized rectifier developed in Chapter 2. The self-synchronized rectifier (SSR) prototype IC, considerably simplifies converter design, improves system efficiency, and enables high operating frequencies up to 4MHz. A flyback DC-DC converter with 3.6V/100mA output was built and tested by use of the SSR IC. Modeling analysis and experimental results are also discussed in detail. Compared to the prior art secondary control methods, the new SSR solution has the advantages of monolithic integration to minimize parasitic components and converter size, automated DCM operation, and MHz switching frequency capability to reduce the size of passive components.

CHAPTER 4: INTEGRATED GATE DRIVER FOR BUCK CONVERTER

In this chapter, a current source gate driver (CSD) scheme [63] is studied in detail to develop an integrated gate driver for buck converters. The integrated gate driver is developed by using a high voltage, isolated semiconductor process technology. Specific considerations in circuit design, layout, and package are discussed in detail for the integrated high voltage gate driver.

The process technology used for this work is ONSemiconductor's I3T50. I3T50 is a 0.35-μm mixed signal CMOS process with 50V high voltage power devices available. All the devices are built in n-type epitaxial layer above p-type substrate. Single poly, 7 nm gate oxide thickness is used in the process. There are 4 layers metal available for standard process, at the same time 3- or 5-layer of metal are optional. To reduce cost, the design is made with only 3 metal layers.

Virtuoso® Front to Back Design Environment v5.1.41 from Cadence™ is used for schematic input. Circuit simulations are done with Spectre MMSIM 6.0 simulator in Analog Artist. Layout physical design is verified by Caliber® DRC and LVS tools from Mentor Graphic®.

4.1 Introduction to the Current Source Gate Driver

The concept of the current source gate driver (CSD) circuit is illustrated in Fig. 4.1. The circuit consists of four small driving MOSFETs (i.e. S_1-S_4), their drivers, and a very small inductor. It should be noticed that in order to simplify the drivers design, S_1 and S_2 are

PMOS switches and S_3 and S_4 are NMOS switches. The current in the inductor is controlled to make it discontinuous so as to minimize conduction loss caused by circulating current in the driver. The operation waveforms of the current source driver (CSD) are given in Figure 4.2. Waveforms, v_{gs1}-v_{gs4}, represent the gate driving signal of MOSFETs S_1-S_4. The operation of the CSD circuit is described as follows.

t_0-t_1: Before t_0 , S_4 is on and S_1-S_3 are all off, so gate of M_1 is clamped to its source

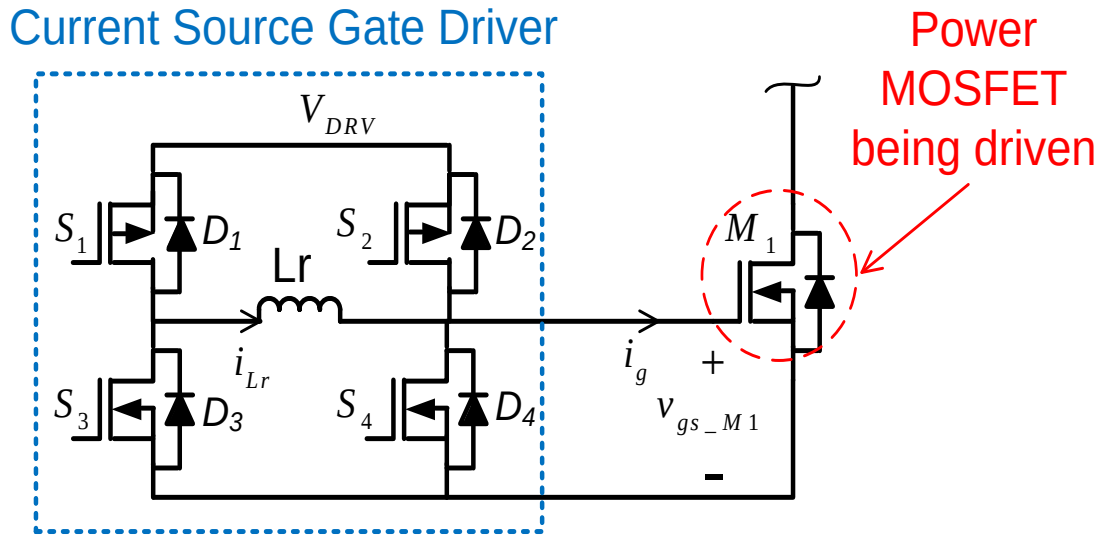


Figure 4.1 Schematic diagram of the current source driver (CSD)

potential to keep M_1 off. At t_0, S_1 is turned on, so V_{DRV} is applied across inductor Lr. Inductor current increases linearly. So in this period, energy is stored in the inductor to prepare to charge the gate capacitor of M_1. Current flows in this path: S1 → Lr → S4.

t_1-t_2: At t_1, S_4 turns off. The current flowing in the inductor start to charge the gate capacitor. So in this period, the gate capacitor is charged to turn on M_1. Current flows in this path: S1 → Lr → gate of M1.

t_2-t_3: At t_2, the gate is charged to V_{DRV} , M_1 is completely on and S_1 turns off. Also at this moment, S_2 turns on (D_2 may turn on in the transition) and D_3 turns on. So the energy stored in the inductor is returned to the line in this period. Current flows in this path: D3 → Lr → S2 (D2).

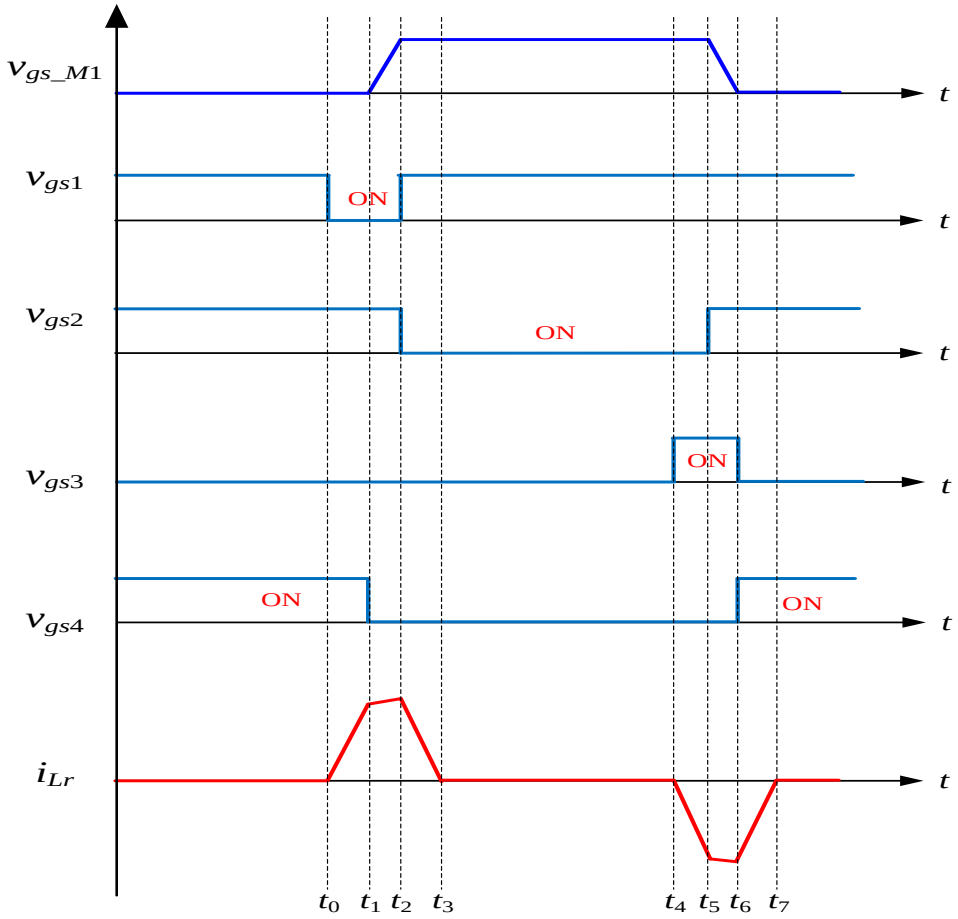


Figure 4.2 Waveforms of the CSD circuit

t_3-t_4: S_2 is on to make sure the gate of M_1 is clamped to V_{DRV} to keep M_1 on. D1 and S2 are on, so inductor current equals zero. No circulating current during this period.

t_4-t_5: At t_4, S3 turns on, voltage applied to the inductor become VDRV again but with reversed polarity, so inductor current begins to linearly increases. So in this period, energy is stored in the inductor to prepare to discharge the gate capacitor of M_1. Current flows in this path: S2 → Lr →S3.

t_5-t_6: At t_5 , S_2 turns off. Inductor current starts to discharge the gate of M1. So in this period, the gate capacitor is charged to turn off M1. Current flows in this path: gate of M1 → Lr → S3.

t_6-t_7: At t_6 , gate capacitance of M1 is completely discharged, so M1 turns off and S3 turns off. S4 turns on (D4 turns on during the transition) and D1 turns on. So in the period, the gate discharging energy is returned to the line. Current flows in this way: S4 (D4) → Lr → D1.

After t_7, S4 is kept on to clamp gate of M1. D3 and S4 are on, so there is no voltage drop across the inductor. No circulating current in the circuit until next M1 turn-on process starts.

So the new current source driver circuit has the following 4 advantages when compared to the previously proposed gate driving solutions.

1) Part of the gate charging energy is recovered during the discharging process.
2) No circulating current during the steady ON/OFF state. So the power loss in driving circuit itself is reduced.
3) Charging and discharging currents are adjustable (by changing inductance value or the length of time intervals of t_0-t_1 and t_4-t_5). So quick turn-on and turn-off

transition time can be achieved. Therefore, the power MOSFET switching loss can be reduced.

4) The ability to actively clamp the power MOSFET gate to gate driving power supply during the on time and to ground during the off time so as to avoid unwanted triggering of the power MOSFET, i.e. *dv/dt* immunity.

4.2 Integrated Gate Driver for Synchronous Buck Converter

Fig. 4.3 illustrates a system level block diagram of a buck converter, where the Gate Driver Chip is the integrated driving circuit that we are going to develop in this chapter. The PWM signal is processed by CPLD module to get proper control signals CT_1-CT_6, which are the input signals for the integrated gate driver. Outputs (HSG and LSG) of the

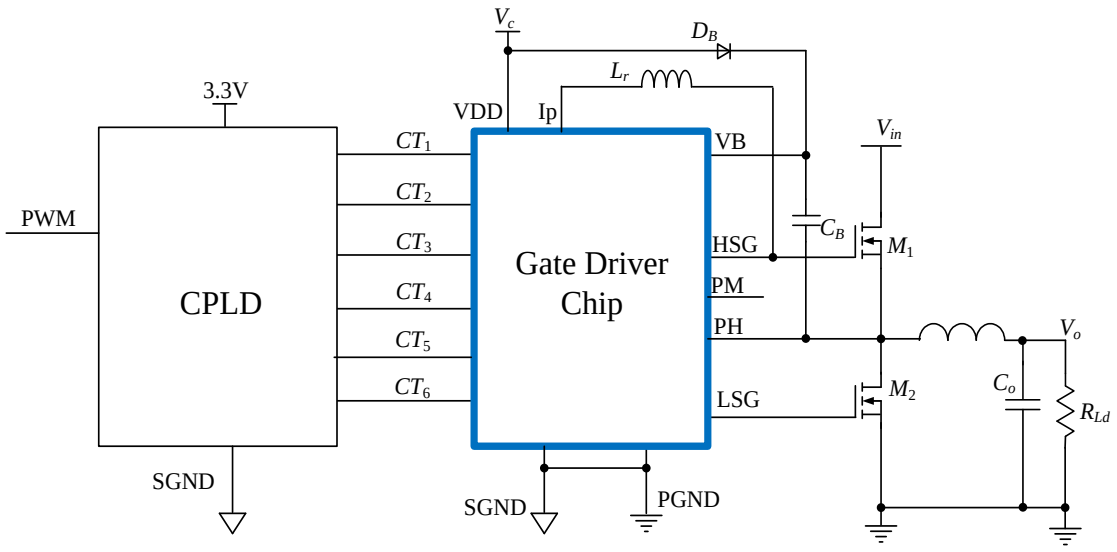


Figure 4.3 System level block diagram of a buck converter

driver chip are connected to the gates of high-side MOSFET M_1 and low-side MOSFET M_2 in the power stage of the buck converter.

The simplified block diagram of the integrated gate driver circuit for a synchronous buck converter is shown in Figure 4.4, where we integrate necessary level shifting circuits and the driver circuits for high-side MOSFET and low-side MOSFET. The inductor L_r will be

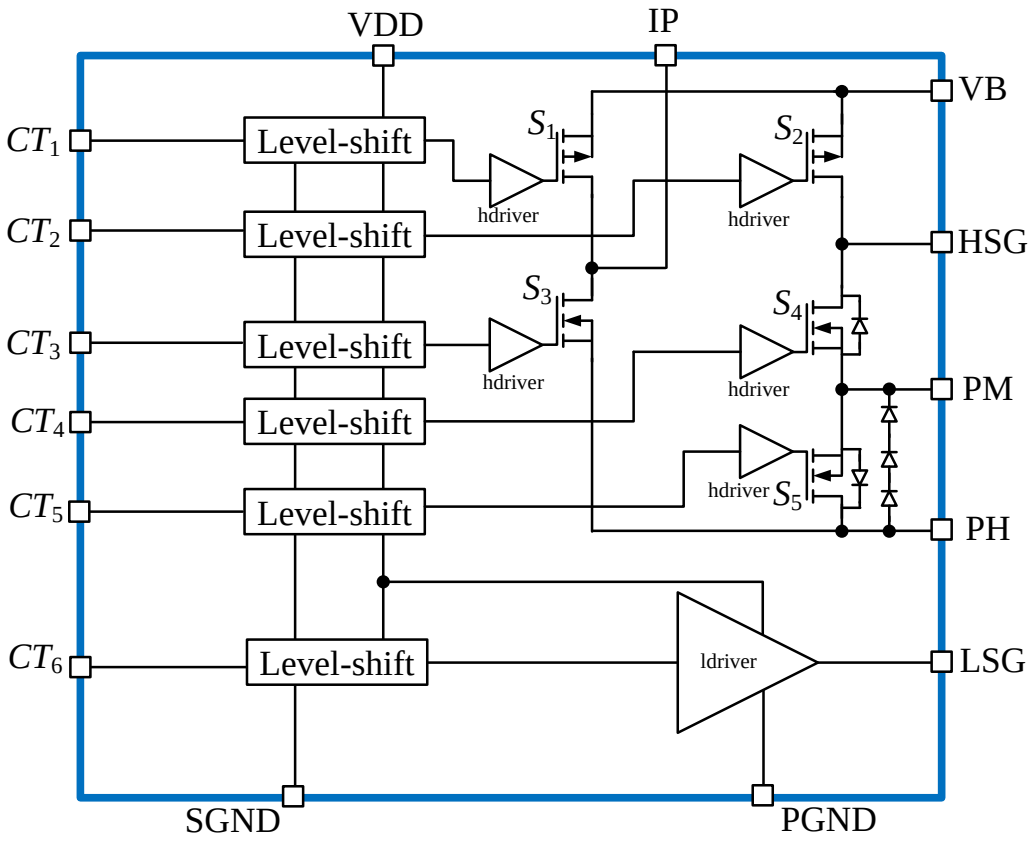


Figure 4.4 Simplified block diagram of the integrated gate driver

an external component. Because low-side MOSFET is almost ZVS turn-on, the switching loss in high-side MOSFET is dominant in buck converter. The driver for the high-side MOSFET employs the CSD circuit, while the low-side MOSFET driver still uses the conventional driver circuit to simplify the circuit design. The main design specification is given in Table 4.1.

Table 4.1 CSD chip main design specifications

Parameter	Symbol	Test conditions	Typical
VDD power supply	V_{DD}		5~12V
Bootstrap voltage	V_B		17~24V
Input signal (CT1-CT6) High level			3.3V
Switch turn-on resistance	$R_{DS\text{-}ON}$	S1-S3	250mΩ
Switch turn-on resistance	$R_{DS\text{-}ON}$	S4,S5	125 mΩ
Rise/fall time of driver for S1-S5 output	t_{FS},t_{RS}	C_{Load}=3nF	8ns
Source/sink current of driver for S1-S5 output	I_{src},I_{snk}		2A
Rise time of driver for M2	t_{RS}	C_{Load}=3nF	8ns
Fall time of driver for M2	t_{FS}	C_{Load}=3nF	4ns
Source current of driver for M2	I_{src}		2A
Sink current of driver for M2	I_{snk}		4A

4.3 Circuit Design

The schematic top level gate driver chip is presented in Fig. 4.5, where all ESD protection circuit is removed for circuit readability.

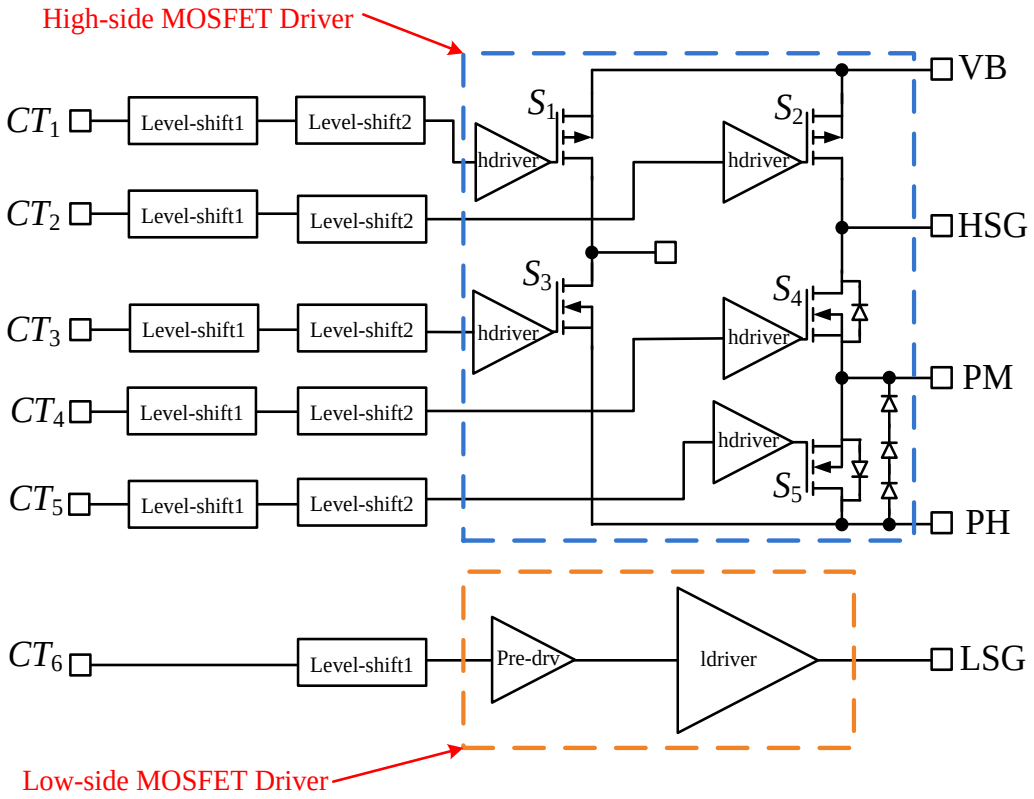


Figure 4.5 Schematic of the top level CSD chip

The level shift circuits are necessary based on two reasons. First, all the input signals (CT_1-CT_6) generated by CPLD module use 3.3V power supply while the power supply used in the CSD chip is in 5-12V range. Second, some circuits also have to use floating ground in the CSD chip. In this design, the level shifting function is decomposed into two functional blocks. The first one, as shown in Fig. 4.6, performs the high level shift of the

input signals from 3.3V to chip power supply V_{DD}. The second one, as shown in Fig. 4.7, is used to shift the signal ground to floating ground and also shift high level from V_{DD}. to bootstrap voltage source V_B for the control signals of switches S_1-S_5.

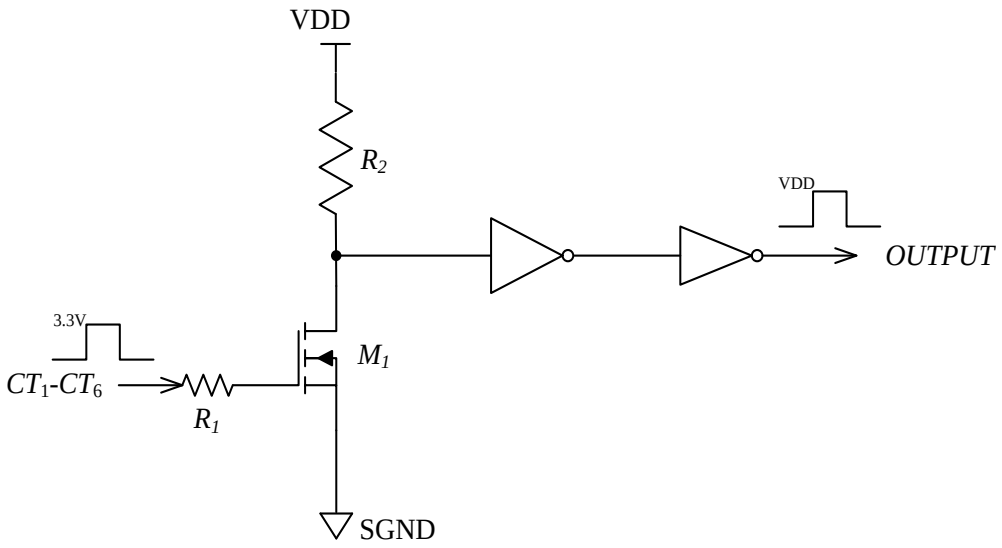


Figure 4.6 1st Level shifter

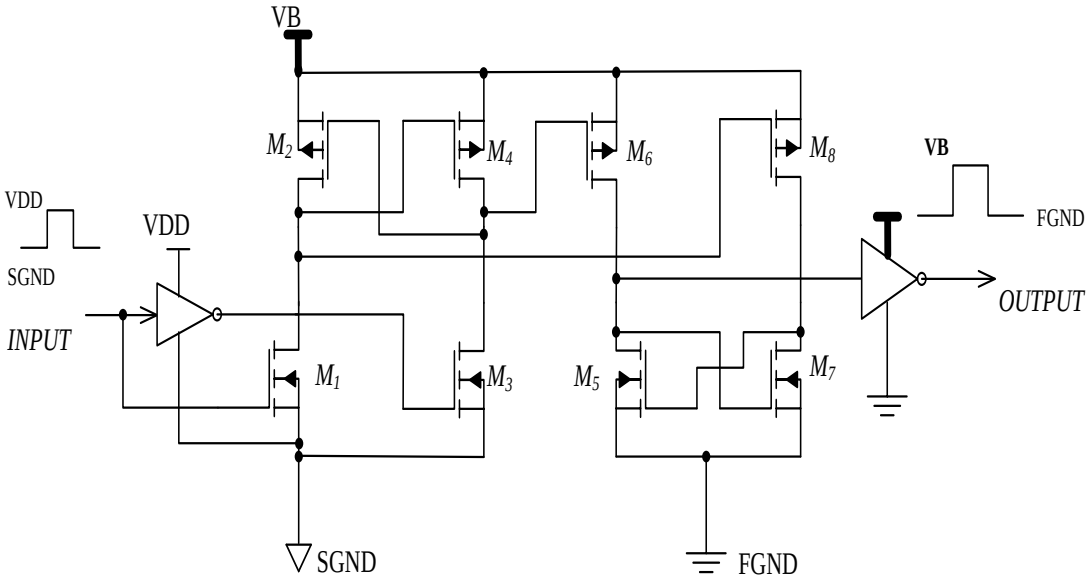


Figure 4.7 2nd level shifter

In the first level shifter, it is all CMOS devices because all the voltages are low voltage. R_1 is used for ESD to protection gate of the NMOS. R_2 is used as pull-up resistor. In the second one, M1-M4 are used to shift high level from *VDD* to *VB*, and M5-M8 are used to shift low level from *SGND* to *FGND*.

Tapering inverter chain is widely used as gate driver for its simplification of circuit design. Usually, the design of the tapering inverter chain driver follows the following equation

$$A^N = \frac{C_g}{C_i} \tag{4-1}$$

where N is the number of inverters in the chain; A is the tapering coefficient, i.e. the width ratio between n th stage and $(n-1)$ th stage; C_i is the total capacitance at the input node of the chain; C_g is the capacitance at the output node, which is dominated by the gate capacitance of the power MOSFET being driven. Basically, the design of the driver is to decide the value of N and A. To get minimized propagation delay from input to output, [102] suggest the following equation should be used to decide N and A

$$A = e \tag{4-2}$$

$$N = \ln \frac{C_g}{C_i} \tag{4-3}$$

Usually, using the values obtained from (4-2) and (4-3) will result in too many stages of inverters, which causes the power loss in driver circuit increase [103][104]. In the CSD chip design here, both power loss and propagation delay are considered.

The low side MOSFET driver includes two block: a *pre_drv* block and a *ldriver* block. The p*re_drv* block is a simple inverter chain with $A = 5$ and $N = 4$. The *ldriver* block is shown in Fig. 4.8. The circuit can be seen as a 3-stage inverter chain. The P/NMOS in the last stage are driven by two separated inverters so to reduce short-circuit loss in last stage because the devices in last stage is very big. BJT devices are used in parallel with P/NMOS in the output stage to boost the charging and discharging current at Miller plateau.

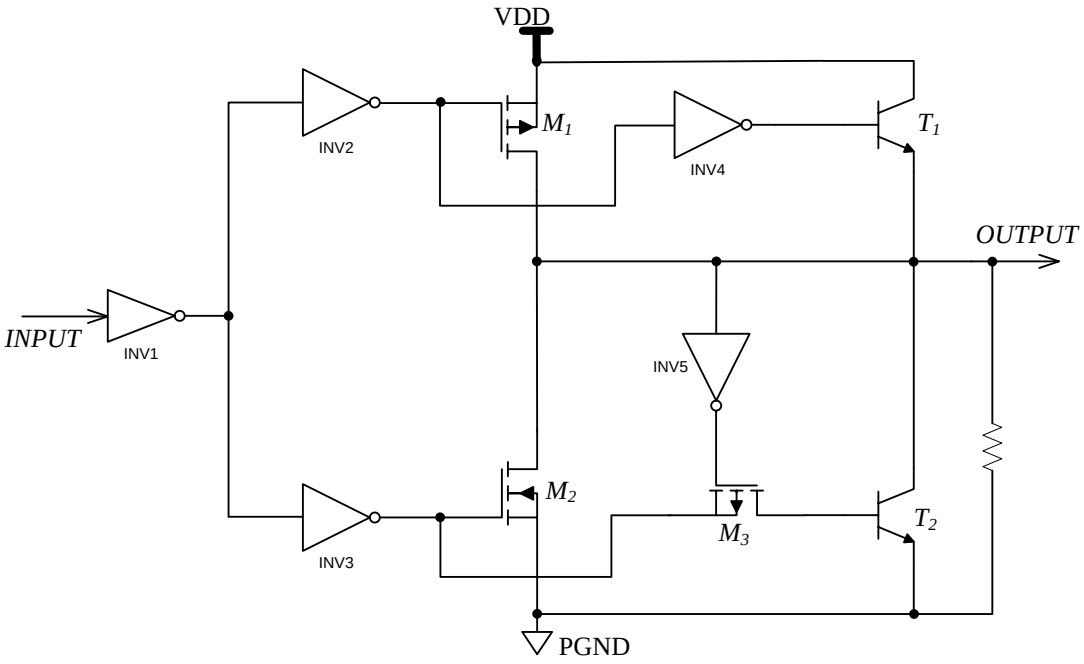


Figure 4.8 Driver for low-side MOSFET

The high-side MOSFET driver, which includes 3 diodes in series, 5 switches and their driver blocks (called “hdriver”), is a little different from the CSD circuit in [63]. The 3

diodes in parallel with switch S_5 are added to make the high-side MOSFET turn off quickly and completely but with no effect on the turn-on transient.

Fig. 4.9 shows schematic of the *hdriver* block, the driver for MOSFET switches, which

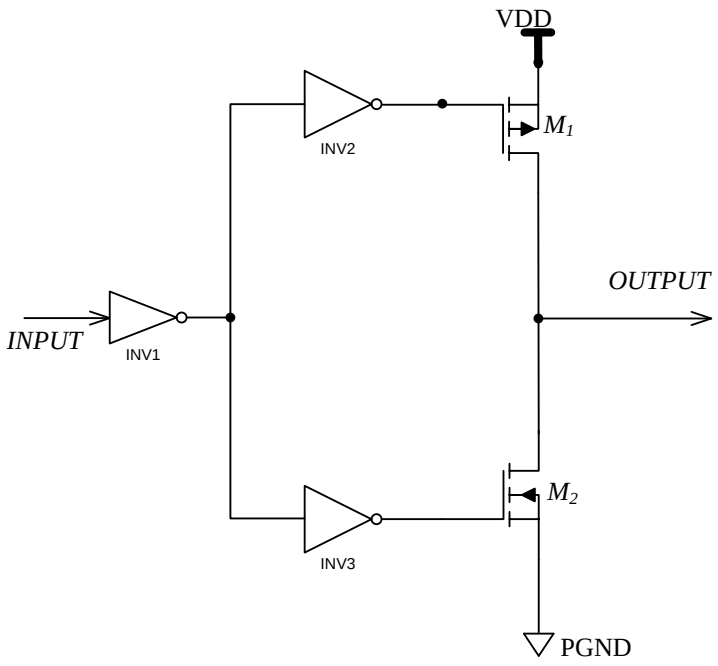


Figure 4.9 Driver for MOSFET switches in high-side driver

also includes 3 stages of inverter. For the same reason, the output stage P/N MOS are driven separately by two different inverters. Because the switch S_1-S_5 are smaller than the external low-side power MOSFET, the sizes of the devices in *hdriver* are smaller than those in *ldriver* and no BJTs are used.

The MOSFET switches are designed just to meet the on-resistance specification. The on-resistance of a MOSFET operating in linear region can be written as

$$R_{DS-ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})} \tag{4-4}$$

Where μ_n is the mobility of electrons in silicon, and C_{ox} is the gate-oxide capacitance per unit area. *W* and *L* are channel width and length, respectively. V_{TH} is the threshold voltage of the MOSFET. V_{GS} is the gate drive voltage. Thus, by choosing suitable width (length of power MOSFET usually is fixed), we can get the desired R_{DS-ON} at the given driving voltage.

Extensive simulations were done in Cadence to ensure the function and performance of the designed circuit. The simulation results versus specifications are summarized in Table 4.2.

Table 4.2 CSD chip design resuts vs. specifications

Parameter	Symbol	Test conditions	Spec.	Sims.
VDD power supply	V_{DD}		5~12V	
Bootstrap voltage	V_B		17~24V	
Input signal (CT1-CT6) High level			3.3V	
Switch turn-on resistance	$R_{DS\text{-}ON}$	S1-S3	250mΩ	213mΩ
Switch turn-on resistance	$R_{DS\text{-}ON}$	S4,S5	125mΩ	110mΩ
Output rise/fall time of S1-S5 driver	t_{FS},t_{RS}	C_{Load}=3nF	8ns	8ns
Output source/sink current of S1-S5 driver	I_{src},I_{snk}		2A	1.4A
Driver for M2 rise time	t_{RS}	C_{Load}=3nF	8ns	8ns
Driver for M2 rise time	t_{FS}	C_{Load}=3nF	4ns	4ns
Driver for M2 source current	I_{src}		2A	1.5A
Driver for M2 sink current	I_{snk}		4A	2.6A

The simulation results meet all of the performance specifications. Driver peak source/sink current is not critical, because all the rise/fall times meet the specs.

4.4 Physical Design and Package

For the layout of this design, matching is not a strict requirement. The most important consideration is to avoid parasitic devices from turning on or affecting the normal circuit operation. Other main considerations in the layout design include ESD protection, metal electro-migration, and latch-up.

For reliability concern during wirebonding, all the pads are designed with all 3 metal layers inter-connected by an array of vias during layout design. The pad position and related blocks layout must consider the feasibility in packaging.

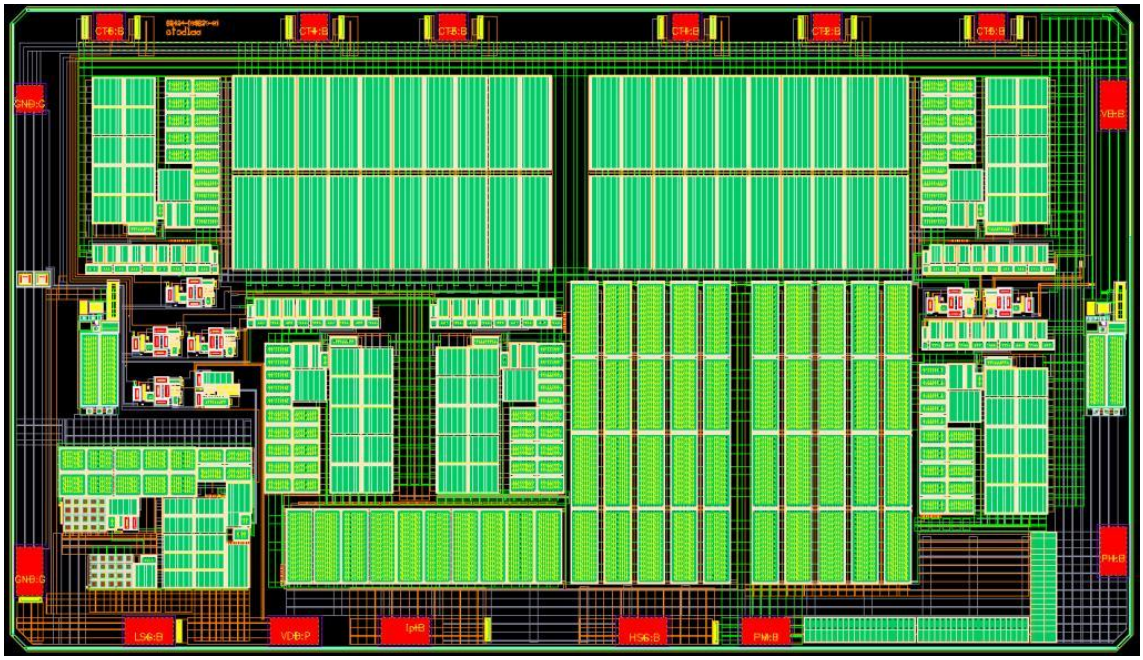


Figure 4.10 Layout of the CSD chip

The final whole chip layout is shown in Figure 4.10. Total 16 layers of mask are used in the design. Only 3 metal layers are used in the design to reduce cost. The total die size is $4098.25\mu\text{m} \times 2347.55\mu\text{m} = 9.62\ \text{mm}^2$.

The pin count of the gate driver chip is 15. We chose CSOIC16 as the package for the driver chip. Hence, one of the pins will be left no connection. The bonding diagram shown in Fig. 4.11 is manually generated to guide the bonding work. Because some of the pads in the chip will conduct high switching current, to reduce parasitic resistance and inductance, those pads are connected to the package with double bonding wires in

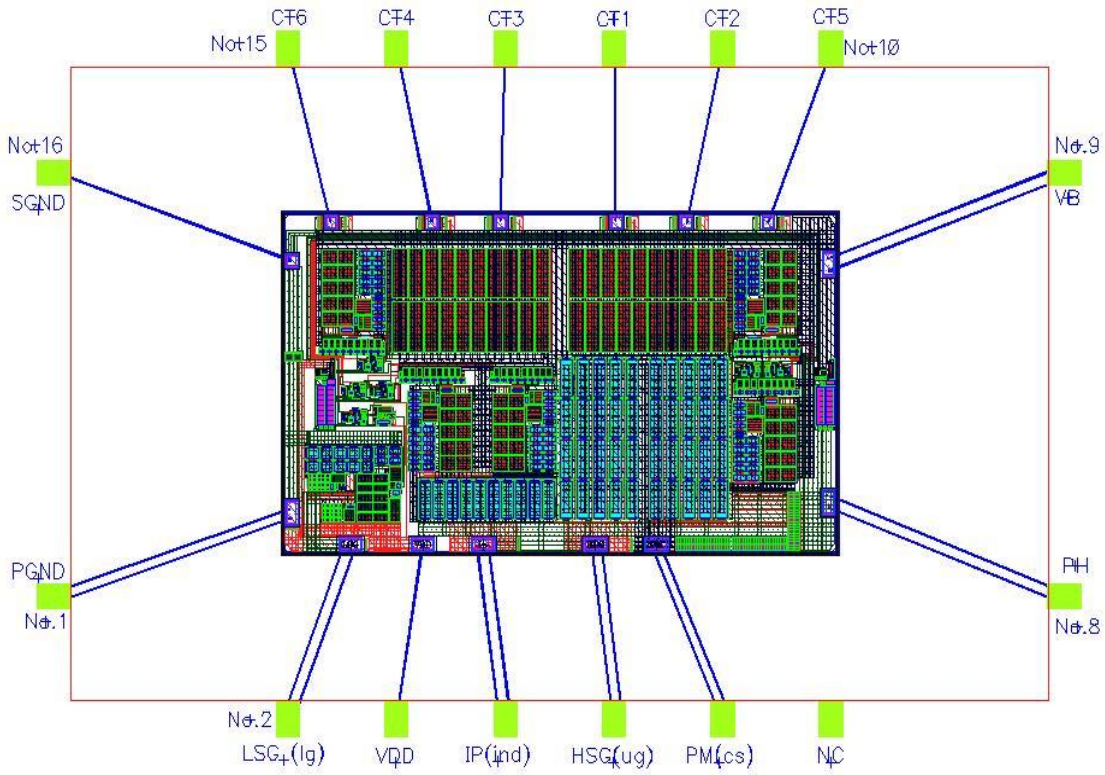


Figure 4.11 CSD chip bonding diagram

parallel.

The pinouts are shown in Fig. 4.12 and pin description is listed in Table 4.3.

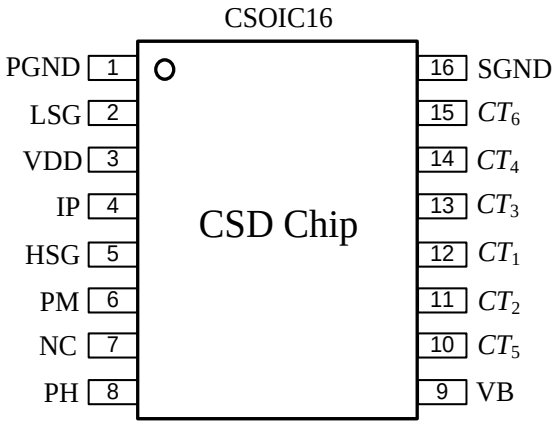


Figure 4.12 CSD chip pinouts

Table 4.3 Package pin desicription

Pin #	*Symbol*	*Description*
1	PGND	Power ground
2	LSG	Low-side gate drive
3	VDD	Power supply
4	IP	Inductor connection pin
5	HSG	High-side gate drive
6	PM	Switch S4/S5 common source pin
7	NC	No connection
8	PH	Phase node
9	VB	Bootstrap voltage
10	CT5	Switch S5 gate signal
11	CT2	Switch S2 gate signal
12	CT1	Switch S1 gate signal
13	CT3	Switch S3 gate signal
14	CT4	Switch S4 gate signal
15	CT6	Switch S6 gate signal
16	SGND	Signal ground

4.5 Summary

An integrated gate driver for a buck DC-DC converter has been developed. The gate driver chip includes drivers for both high-side power MOSFET and low-side power

MOSFET of a buck converter. To simplify circuit design but not to sacrifice too much performance, high side driver uses the new current source drive scheme, while low side driver still uses a conventional drive circuit but optimized for both delay and power consumption. Design considerations, circuit analysis, layout design are presented in detail. A package style is also properly selected to facilitate testing work.

CHAPTER 5: POWER SUPPLY IN PACKAGE

Power supply in package (PSiP) that integrates all active and passive components into a single package using low cost semiconductor manufacturing processes will provide an attractive solution with significant improvement in performance and reduction in board space, parts count, and time-to-market. As mentioned in Chapter 1, the integration of magnetic passive components is one of the major technical barriers in PSiP development. The magnetic components made from MEMS and LTCC technologies are limited by high cost and low performance [71]-[78][105].

In this chapter, we propose and investigate a new approach of forming in-package power supply by utilizing gold or aluminum bondwires with ferrite epoxy glob cores as inductors. All the active power devices, driver circuitry, and necessary control logic were designed and fabricated with a standard 0.5μm CMOS process. The bondwire inductor is made by adding ferrite epoxy composite glob coating to the bondwires during the IC packaging process to increase the bondwire inductance and thus increase Q factor. A 2.2V/120mA prototype PSiP buck converter was built to operate at frequencies up to 5MHz. Multi-turn bondwires with and without ferrite epoxy glob cores are used as the filter inductor in the buck converter. The power level of the prototype buck converter is scalable by scaling of the active power switches. Analysis, experimental results, and discussion are presented in this work.

5.1 Concept

Wirebonding has been commonly used in nearly all power IC packages. Bondwires naturally show some inductive characteristics with the inductance value of few nH depending on the length, loop height, and diameter of the bondwires. To increase the inductance, it was proposed to add ferrite epoxy composite glob cores to the bondwires[106]. Fig. 5.1 shows the concept of the bondwire with ferrite epoxy coating.

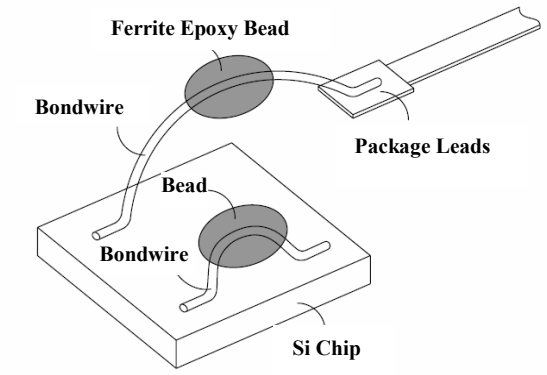


Figure 5.1 Concept of single bondwire with ferrite epoxy beads

Modeling and experimental results of bondwire inductors with ferrite epoxy were reported in [107]-[109]. With the use of ferrite epoxy, the bondwire inductance can be increased by up to 5 times. To further increase the inductance, multi-turn bondwire inductors, as shown in Fig. 5.2, have also been investigated [110]. It is similar to conventional coil inductor, in which the coupling effect between each turn boosts the inductance value. However, the conventional coil inductor is formed by winding a conductor (usually a solid copper wire) around a core, while multi-turn bondwire

inductor is formed by on chip metal traces and bondwires with ferrite epoxy glob. Unlike conventional ferrite ceramics, ferrite epoxy materials are essentially ceramic magnetic powders mixed with a polymer binder, and can be dried or cured at temperatures less than 200oC. These materials combine appropriate magnetic properties with a high resistivity and high manufacturability. The ferrite epoxy glob cores can be formed on the bondwires during the PSiP or PSoC packaging process using high precision robotic tools similar to the commonly used electronic assembly equipment such as solder paste dispensers.

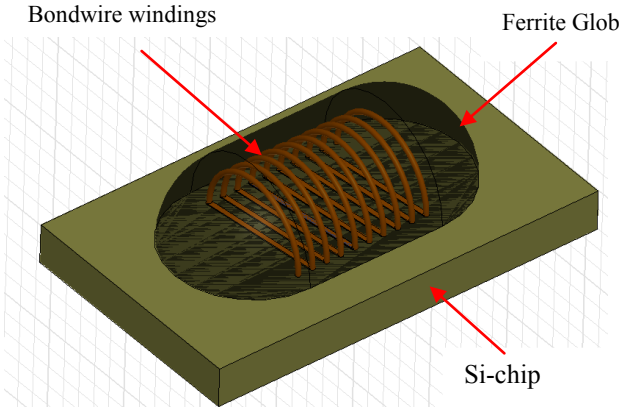


Figure 5.2 Concept of coupled on-chip multi-turn bondwire inductor

The purpose of this work is to demonstrate a proof-of-concept PSiP buck converter based on the bondwire inductor concept. Fig. 5.3 depicts a two-phase, 5V-to-2.5V buck converter using bondwire inductors as filters and a monolithic power IC on a package substrate (PCB in this case).

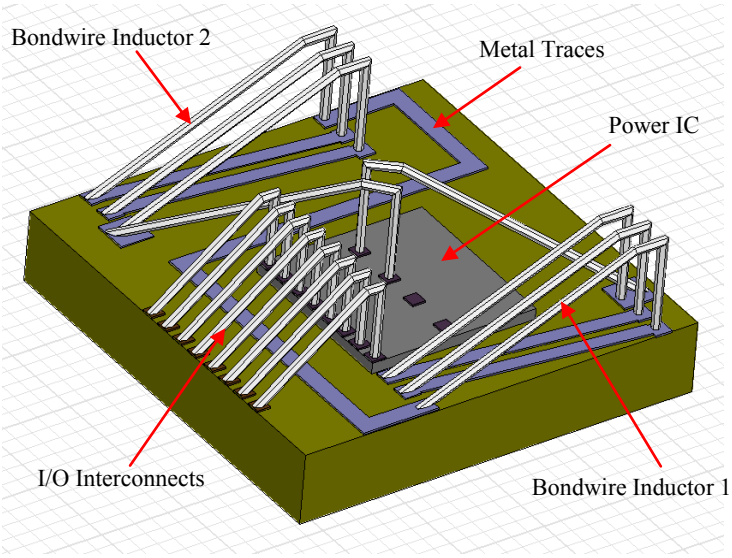


Figure 5.3 Conceptual drawing of the PSiP buck converter

The power IC chip, as shown in Fig. 5.4, integrates all active power switches, gate drivers, and logic circuits. It was designed and fabricated with a standard 0.5 µm CMOS process (the AMIS C5 process) through the MOSIS foundry service. To simplify the design of the gate driver stage, PMOS was used as the high side power switch (the controlFET). NMOS was used for the low side power switch (the SyncFET) to minimize the silicon real estate. Although the AMIS C5 process offers 20V extended drain MOSFET options, it is essentially a 5V digital CMOS process that is not optimized for power applications. The specific RDSON of both its 20V extended-drain NMOS and PMOS are much higher than those of a typical BCDMOS power IC process. This constraint will limit the achievable efficiency of the prototype buck converter but otherwise will not affect the basic operation of the circuit. The NMOS low side switch has a channel length of 5µm and a channel width of 50 mm while the PMOS high side switch has a channel length of 3 µm and a channel width of 100 mm. Both gate drivers

simply use the tapered inverter chain structure to optimize delay and sufficient source and sink current to charge and discharge the gate capacitors of the power MOSFETs. The control logic block basically generates two out-of-phase PWM signals for the high- and low-side power switches from the external PWM input signal. To focus on the goal of evaluating the basic converter operation with the bondwire inductors, the power IC converter was purposely designed for open-loop operation without any feedback circuit. The electrical parameters of the key elements of the power IC are summarized in Table 5.1.

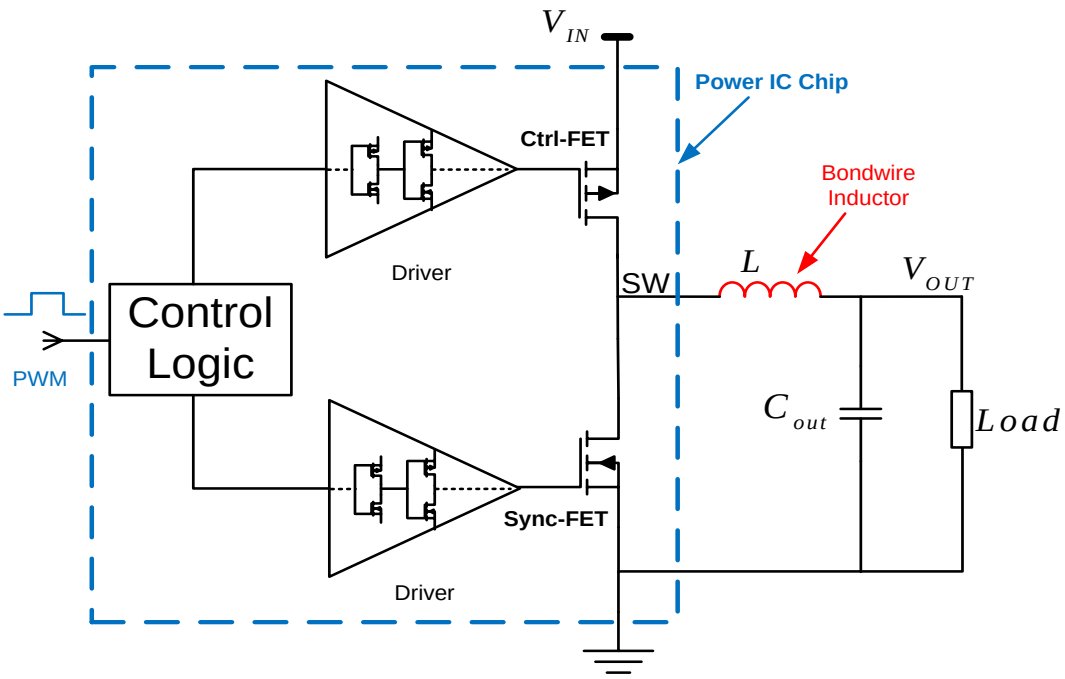


Figure 5.4 Schematic diagram of the buck PSiP

Table 5.1 Driver and power MOSFET design results

High Side PMOS $R_{ds\text{-}on}$ @V_{gs}=5V	0.72 Ω
Low Side NMOS $R_{ds\text{-}on}$ @V_{gs}=5V	0.63 Ω
High side Driver propagation delay	3 ns
Low side Driver propagation delay	5 ns

5.2 Prototype of the PSiP Buck Converter and Experimental Results

The final implementation of the PSiP converter before and after applying the ferrite

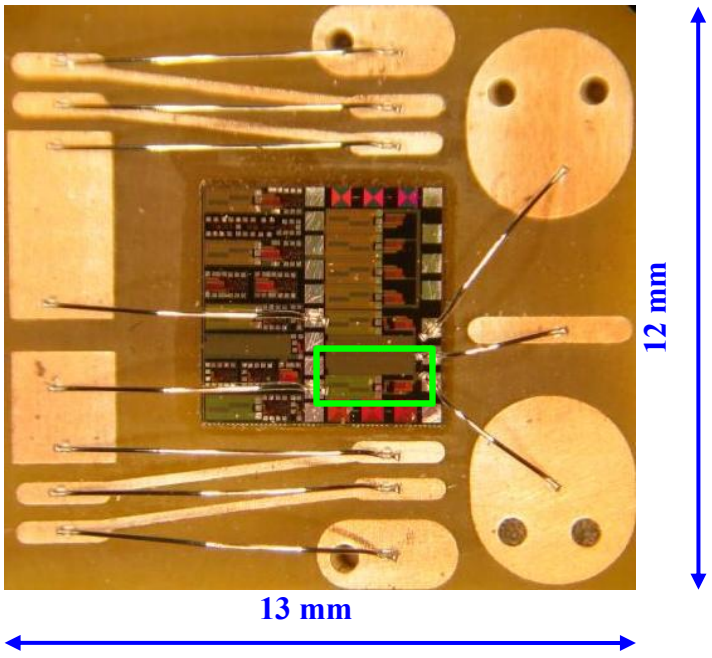


Figure 5.5 The buck PSiP before ferrite epoxy coating

epoxy glob cores are shown in Figs. 5.5 and 5.6 respectively. The multi-project silicon chip shown has a die size of 5 ×5 mm^2, but the actual chip area for the buck converter is

only 2.5×1.5 mm^2. (the green boxes in Fig. 5.5 and 5.6) Due to the limitation of the manual wirebond machine used in this experiment, the pads size and spacing between bondwires are relatively large. While the total size of the PSiP buck converter in its current form is 13 ×12 mm^2, it is expected to be reduced to 5 × 5 mm^2 by using a dedicated silicon die and finer pitch wirebond machine. Three-turn bondwire inductors were used as the filter inductor in the PSiP buck converter which demonstrated an inductance of 150 nH and 450 nH without and with the ferrite epoxy glob cores respectively.

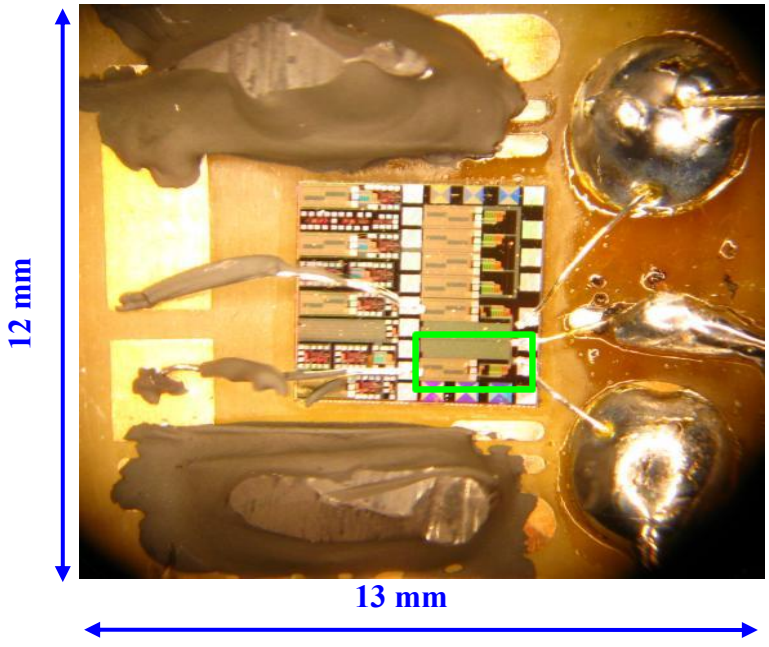


Figure 5.6 The buck PSiP after ferrite epoxy coating

Figs. 5.7 and 5.8 show the switching waveforms of the PSiP buck converter without and with the ferrite epoxy glob core respectively. The testing conditions were as the following: Input voltage V_{IN} = 5 V and switching frequency f_{SW} = 5 MHz. It is observed

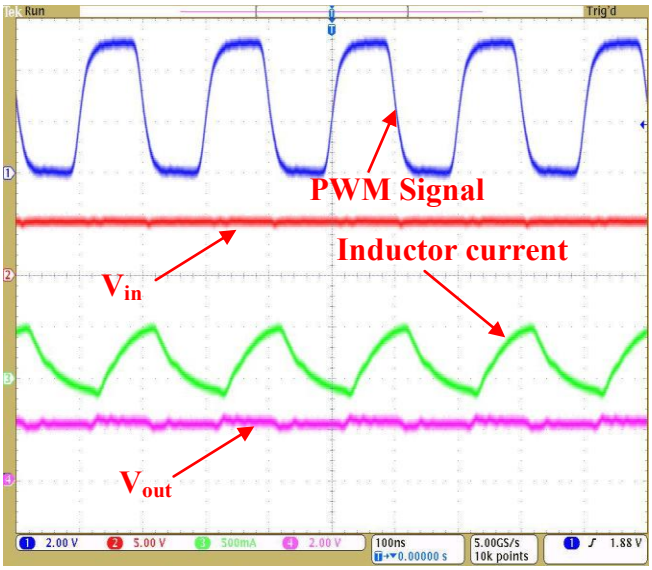


Figure 5.7 Operating waveforms of the PSiP without ferrite epoxy coating

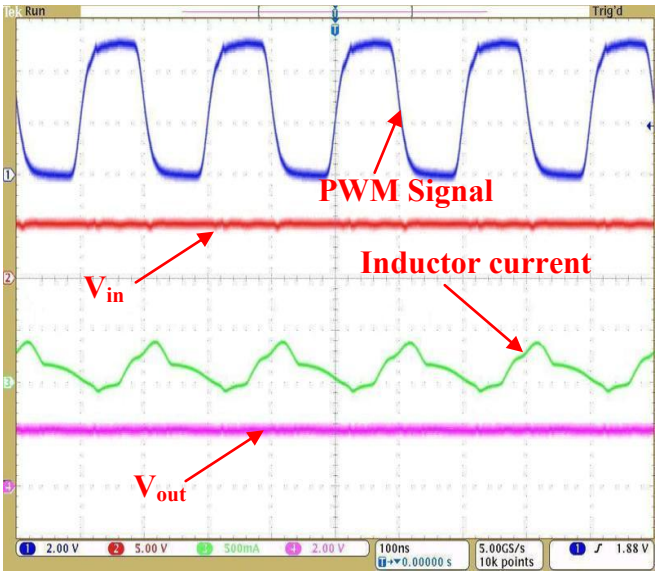


Figure 5.8 Operating waveforms of the PSiP with ferrite epoxy coating

that the converter operated in DCM and the peak to peak inductor current ripple decreases approximately 35% with the utilization of ferrite epoxy glob cores. With the use of ferrite epoxy, the inductor ripple current and output voltage ripple decreases, so the efficient increases.

5.3 Discussion

A. Increase the output power and improve the overall efficiency of the PSiP

The output voltage and current of the PSiP buck converter is 2.2V and 120 mA respectively. The measured efficiency is about 52% which is low. Since the bondwire inductor shows very high saturation current and low DCR [109], the low efficiency is attributed to the power MOSFET losses. As discussed earlier, the specific RDSON of the power MOSFET in the AMIS C5 5V digital CMOS process is very high, and subsequently limits the achievable converter efficiency. The lack of reverse current blocking function in DCM operation and the less than optimal dead time control in the power IC also partially contributed to the low efficiency. It is expected that the efficiency can be significantly improved with the adoption of more advanced power IC fabrication processes and IC design optimization. Nevertheless, the prototype buck converter reported in this letter did serve its purpose of demonstrating the basic operation with in-package bondwire inductors at a frequency up to 5 MHz.

B. Inductance value selection for the PSiP

The selection of inductance value in buck converter is a tradeoff between efficiency and transient response. A larger value of inductance offers greater output current capability,

reduced inductor ripple current, low output voltage ripple, and hence a higher system efficiency. However, the transient response will degrade as a penalty if larger inductance value is used because inductor current changes very slowly. Generally, selecting an inductance to have the peak-peak current ripple of 20~40% of the average current gives a good balance between efficiency and transient response. If take the ratio of current ripple to average current as a design input to design a buck power converter, the inductance value can be expressed as

$$L = \frac{V_{in} \cdot D \cdot (1 - D)}{I_O \cdot RR \cdot f_{sw}} \tag{5-1}$$

where V_{in} is the input voltage, I_o is the output current, f_{sw} is the switching frequency, D is the duty cycle, RR is the ratio of inductor ripple current over average inductor current.

In the PSiP buck converter prototype, the bondwire inductance is around 150 nH and 450 nH without and with ferrite epoxy core respectively, which is relatively small and causes the system operating in DCM and gives rise to high current ripple. Bondwire inductance values can be considerably increased with the use of fine pitch wirebonding machine [111] In addition, by adopting some system topology, such as multiphase technology, the ripple current could be reduced even with the same inductance value.

C. The non-linear inductor current waveform of the PSiP

In the presented experimental results, the inductor current waveforms show some non-linearity, which can be explained as the following. The slope of the inductor current in the PSiP buck converter can be approximated as the following expressions.

$$Rise\_slope = \frac{V_{in} - R_{ON-P} \cdot i_L - V_o}{L} \tag{5-2}$$

$$Fall\_slope = -\frac{R_{ON-N} \cdot i_L + V_o}{L} \tag{5-3}$$

where V_{in} and V_o are input and output voltage, respectively; $R_{ON\text{-}P}$ and $R_{ON\text{-}N}$ are the on-resistance of the high side PMOS and low side NMOS, respectively; i_L is the inductor current, and L is the inductance of the inductor. Usually, in practical buck converter, $R_{ON\text{-}P}$ and $R_{ON\text{-}N}$ are very small, so the product of the on-resistance and the inductor current can be neglected. Therefore, the slope is almost constant and the inductor current is linear. In our demonstration unit, $R_{ON\text{-}P}$ and $R_{ON\text{-}N}$ are much larger because of the limitations of the 5V digital CMOS process and silicon real estate, introducing considerable nonlinearity of the inductor current.

D.The integration of capacitors in PSiP

The integration of input and output capacitors is still a major challenge for any PSiP development. On-chip capacitors are not a practical solution yet due to the large silicon real estate they consume. The highest integrated capacitance per unit area reported so far is 400nF/mm^2 for TiN/Al_2O_3 MIM capacitors [112]. In the experiment we report here, surface-mount ceramic capacitors are used for the input and output ports and mounted on the backside of the PCB substrate.

5.4 Summary

In this chapter, a power supply in package (PSiP) prototype, which contains the power IC of a buck converter and bondwire inductor, is presented. The power IC containing all switching devices, driver circuitry, and control logic was designed and fabricated with a standard 0.5 μm CMOS process. Multi-turn bondwires with and without ferrite epoxy glob cores are used as the filter inductor in the buck converter. Although with a relatively low efficiency due to the CMOS fabrication process limitation, the PSiP buck converter prototype demonstrated basic operation with an output voltage and current of 2.2V and 120mA, and switching frequencies up to 5MHz. The power level of the prototype buck converter is scalable by increasing the size of the active power switches.

CHAPTER 6: CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

High power density and high efficiency are two basic requirements for the power supplies in hand-held or battery-powered electronic devices. Increasing the switching frequency is one of the most effective way to reduce the volume of power converters by reducing the sizes of passive components. However, power loss in the converters also increases significantly due to increased switching frequency. In this work, various integration of new topologies and control techniques have been investigated to address the demand for high switching frequency, high efficiency, and high power density DC-DC converters.

6.1.1. Self-Synchronized Rectifier

The concept of self-synchronized rectifier (SSR) has been proposed in this work to mitigate the body diode conduction issue in conventional synchronous rectification technique, which is one of the most popular techniques used in power converters for today's electronic devices. Analysis, design considerations, circuit simulation and layout design have been done. A prototype with the negative offset voltage, high speed comparator and the novel one-shot control has been fabricated in a 5V, 0.5-μm mixed signal CMOS process. Experimental results for the block performance parameters and functions matches the simulation results. The prototype SSR IC was also tested in a monolithic buck converter. It works well under both heavy load and light load conditions. The possible oscillation (the repetitive turning on/off of the sync-FET in one switching

cycle) is eliminated under light load condition. The SSR can be used in high switching frequency (higher than 1MHz) power converters.

6.1.2. MHz Synchronous Flyback Converter

A MHz synchronous flyback DC-DC converter using the SSR has been analyzed, designed, and simulated. Based on the modeling work, experimental demonstration has also been performed with a 3.6V/100mA flyback converter. By using the SSR, the design of flyback DC/DC converters was significantly simplified. The 3.6v/100mA flyback converter can also be operated at high frequency (higher than 4MHz), which is helpful to reduce the board space. Compared to a flyback converter using diode rectifier, the one using the SSR have efficiency improvement up to more than 10%.

6.1.3. Integrated Gate Driver for Buck Converter

An integrated gate driver for buck converter has also been presented in this work to address the ever increasing dynamic power loss (gate driving loss plus switching loss) in high frequency power converters. The monolithic gate driver integrates both the driver for high-side power MOSFET and the one for low-side power MOSFET of a buck converter. To simplify the circuit design, the high-side MOSFET driver employs the current source gate driving (CSD) scheme and the low-side one use the conventional gate driver but with design considerations on both delay and power loss. A 0.35-μm mixed signal CMOS process with optional 50V high voltage power devices was used for the fabrication of the chip. Simulation results show that the CSD chip is able to provide fast

switching transient less than 8 ns. The design, simulation, layout, and packaging consideration are discussed in detail in this thesis.

6.1.4. Power Supply in Package (PSiP) Integration

PSiP integration of a buck DC-DC converter has been demonstrated in a cost effective way. The PSiP buck converter operates at a frequency of 5MHz with 2.2V/120mA output. All the active devices, including power MOSFETs, drivers, and logic circuit, are integrated into a single silicon chip by using a 0.5- μm CMOS process technology. Multi-turn bondwire with ferrite epoxy core was used as the output filter inductor, which has been proved to have high inductance, low DCR (and thus high Q), high saturation current. Since the bondwire magnetic integration can be made during standard IC packaging process, it is believed to open enormous possibilities for realizing cost-effective, high current, high efficiency PSiP.

6.2 Future Work

Some possible future work is outlined here for the topics in this thesis work.

6.2.1. Self-Synchronized Rectifier

The proposed self-synchronized rectifier (SSR) features high speed comparator with negative input offset voltage and one-shot control method. Because the offset voltage plays an important role in the SSR, it would be better to have it externally programmable or adaptive to load conditions.

In addition, the possibility to integrate a power supply for the SSR would be very advantageous since the SSR would be more like an ideal diode with only two terminals by doing this. However, an relatively large capacitor may need to be integrated for the power supply integration.

To better demonstrate the advantage of the SSR, low $R_{DS\text{-}ON}$ power MOSFET from a power IC process technology needs to be used in the SSR. In this way, the output power level can be increased and the overall system efficiency can also be improved.

6.2.2. MHz Synchronous Flyback Converter

The use of a power IC process technology for the SSR fabrication would also be beneficial to the demonstration of the synchronous flyback converter.

And if the SSR can be packaged in a small package with reduced parasitic inductance and resistance, the switching frequency can be pushed to higher. Therefore the passive components size can be reduced further.

6.2.3. Integrated Gate Driver for Buck Converter

Currently, the integrated gate driver has been developed with an external inductor. A very promising future work is to integrate the inductor into the package or onto the chip since the inductance required in the current source gate driver is relatively small (in the range of only few tens of nH).

Another future work is to integrate the CPLD function (which is used in the system level testing to generate gate control signals for the power MOSFETs) into the driver. So the

only input signal would be PWM pulse input. Furthermore, the controller may also be integrated with the driver to reduce component counts and board space.

6.2.4. Power Supply in Package (PSiP)

The buck converter chip can be made with a power IC process to reduce the $R_{DS\text{-}ON}$ of the power MOSFET. Then the output power level, overall efficiency will be improved. The inductor current will also become more linear.

If the multi-turn bondwire inductor can be made on the silicon chip with on-chip metal traces, it would be more attractive because the whole power supply system will be demonstrated in a very small area.

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