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HIGH TEMPERATURE PACKAGING FOR WIDE BANDGAP SEMICONDUCTOR DEVICES

by

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ABSTRACT

Currently, wide bandgap semiconductor devices feature increased efficiency, higher current handling capabilities, and higher reverse blocking voltages than silicon devices while recent fabrication advances have them drawing near to the marketplace. However these new semiconductors are in need of new packaging that will allow for their application in several important uses including hybrid electrical vehicles, new and existing energy sources, and increased efficiency in multiple new and existing technologies. Also, current power module designs for silicon devices are rife with problems that must be enhanced to improve reliability. This thesis introduces new packaging that is thermally resilient and has reduced mechanical stress from temperature rise that also provides increased circuit lifetime and greater reliability for continued use to 300°C which is within operation ratings of these new semiconductors. The new module is also without problematic wirebonds that lead to a majority of traditional module failures which also introduce parasitic inductance and increase thermal resistance. Resultantly, the module also features a severely reduced form factor in mass and volume.

This thesis and the work put into it dedicated to those serving at

home and abroad striving to grant and protect freedom for all.

ACKNOWLEDGEMENTS

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CHAPTER 1   INTRODUCTION

The landscape of the power semiconductor industry like its partner semiconductor industries is dominated by silicon semiconductors. For decades silicon has provided as an increasingly inexpensive, reliable semiconductor material that has by and large provided functionality for whatever application has been conceived of it. Silicon's achievements of functionality were hypothesized by almost no one, and it has been almost fully utilized. However the impending fate of silicon is foreshadowed by examples of many tools that have also been fully exploited by man's resourcefulness. Just as clay, stone, and sod met their fundamental limits in providing safe, sturdy housing, it is now built with concrete, brick, and steel. Just as the horse and ox had their fundamental limits of strength and speed, cars and trains are now used for travel and shipping. And just as Gutenberg's block type printing press transformed the world in just a few short years, even it met its fundamental limits of speed and clarity and now instant color laser printing is in almost every desiring office across the world.

The writing is on the wall for silicon's future in the power semiconductor device field as silicon's fundamental limits of on-state resistance and voltage blocking capabilities and various other characteristics become more of a glass ceiling rather than a barrier. Soon the transition will be made to a new age of wide bandgap power semiconductor with a wide array of advantages that will lend to faster, more powerful devices. However, work must be done to harbor in these new technologies; they must be fully integrated into the fields that they will best serve which carries significant challenges to incorporate them into new environments.

In order to contribute to this effort of facilitating wide bandgap semiconductors into the industry and to make use of some of their intrinsic advantages like their increased operating

temperature the Power Semiconductor Research Lab, part of the Florida Power Electronics Center, in conjunction with the National Institute of Standards and Technology is developing packaging for a half bridge power rectifier using silicon carbide device technology.

There are several advantages of wide bandgap semiconductor, like silicon carbide, that will be nurtured in the developed packaging. Wide bandgap semiconductors have shown extreme resilience to high temperature operation, the package in development will allow the enclosed devices to operate at much higher junction temperatures than currently available packaging. This will be done with the use of new encapsulation and solder materials that allow for a 300° C device operating temperature that also have similar coefficients of thermal expansion that do not create excessive stress within the package from increased temperature rise leading to fewer failures thus greater reliability. The package will also be designed without wirebonds to high current terminals to reduce the package inductance and lower thermal resistance; this will be effective in making use of the high switching speeds possible with wide bandgap semiconductor devices. Notable also, the package will have a much smaller form factor with up to a 66% decrease in mass and volume, this will make the package easier to implement and also in conjunction with the material considerations reduce the thermal resistance of the package from junction to ambient. The lower thermal resistance is aided furthermore by the lack of wirebonds, the package's soldered connections on both sides of the devices provide effective double-sided cooling in this low profile package, increasing its advantages.

1.1   New Module Motivation

There are great deals of advantages that lie with wide bandgap (WBG) semiconductors, many of which will require a reconsideration of standard packaging to fully extract these

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advantages. Simultaneously, current power semiconductor packaging is somewhat archaic and has been slow or ignorant in adjusting to problems with even today's silicon device operation (Chapter 2: Review of Prior Art). This combination of old problems and new potentials makes for an exciting opportunity to step into the conversation with some fresh ideas and new strategies of implementing new packaging designs. Not to mention, the growth of need for high temperature electronics in a variety of fields either due to high working temperatures or lack of cooling options also increases the need for new modules.

1.1.1   High Temperature Electronics Environments

There is an existent and growing field for electronic circuits and devices to work at elevated temperatures, in which WBG semiconductors, in particular silicon carbide (SiC) have shown a great resilience to handling (1). The need for electronics high operating temperatures is the result of two primary situations, either the need for greater power delivery or a higher temperature environment. Equation 1.1 shows the maximum power of a device based on the maximum junction temperature ($T_{j,max}$), the ambient temperature or case temperature (T_C), and the thermal resistance ($R_{\theta JC}$) of the package to the case (2).

$$P_{max} = \frac{T_{j,max} - T_C}{R_{\theta JC}} \tag{1.1}$$

$$T_{j,max} = P_{max} \cdot R_{\theta JC} + T_C \tag{1.2}$$

It is rarely one variable of the equation that dictates the need for high temperatures operation; it may be that $R_{\theta JC}$ is fixed and the power level must be increased, doing so would inevitably raise $T_{j,max}$. It is also possible that if the circuit were constrained by a high thermal resistance with a similar power input then the $T_{j,max}$ would again rise. The max junction temperature could possibly be pinned by the ambient environment, if the temperature in which the devices or circuit

are to operate is above the rated junction temperature then there is virtually no solution to reliability problems, unfortunately this is often related to packaging.

1.1.2   Energy Generation Packaging Applications

The energy industry has always been a large part of the power semiconductors industry and has been a driving force for research and improvement within it. This research has shown that there are several components of WBG semiconductors that make them so appealing to the industry (3). However, the temperature dealings of WBG are especially attractive because of their temperature limits, the increased $T_{j,max}$ can be of great use for power stations for running their devices at greater power densities. In a decentralized power grid, as the future likely holds, generation systems will have less cooling capabilities and need greater power density to maintain a small form factor to be attractive for consumers as they may very well be attached to one's home or business (4).

Both old and cutting edge facets of energy production are looking for an operational temperature range boost. Oil and geothermal energy exploration and harvesting require extremely harsh and hot surrounding environments for electronics below the earth's surface. Referred to as down-hole applications, necessary electronics must go down below with a burrowing rig deep below the earth's surface and face temperatures upwards of 200°C ambient temperatures for oil drilling, which can lead to much greater junction temperatures on the power devices, to operate machinery for the digging of wells. It is believed that current silicon on insulator (SOI) technology can make the logic circuitry feasible however even it too will need a redesign for the packaging to hold up over time (5). This logic circuitry will be necessary as hopefully down-hole operations shift toward geothermal energy solutions due to its great

potential as a clean renewable energy (6). This will pose even greater challenges for the packaging and electronics due to the greater temperatures (>300° C) and the need to have even more reliable electronics because unlike oil drilling the measured temperature will be more critical as the temperature is the primary reason for the down-hole operations so that it may vaporize water sent below earth to run turbines above ground like conventional energy, thus the higher the temperature below the more lucrative, unlike oil drilling where the high temperatures are avoided if possible (7).

1.1.3   Automotive / Aerospace Packaging Applications

Aerospace and automotive fields can also put great strain on their electronics, not only due to increased power demands and the increased working environment temperature on the devices, but also due to the lack of adequate cooling and the need to reduce the cooling system size and weight. Both automobiles and airplanes are relatively small working environment for high density high power electronics especially compared to trains or marine ships where similar power inversion takes place, this small workspace makes cooling more of a challenge, and in both cases the reduction or possible removal of the cooling system can lighten the load considerably. This is especially enticing considering not only the initial cost savings but since cars and planes propel themselves it makes them much more efficient to perform their primary goals with a lesser weight (8). This is more than an upgrade for some systems, in particular for the Lockheed F-35 fighter aircraft which is designed to be as small and agile as possible; a bulky liquid heat exchanger is infeasible, the fuel, as with many aircrafts, is used as the ambient cooling fluid on the heat sink. This leaves the jet with severely limited flight lengths as well as

minimum fuel levels even to land. It has been reported that the fuel must sometimes even be chilled before takeoff to perform flights (9).

As mentioned the primary goal of removing the cooling system for automotive systems is to raise the efficiency of hybrid electric systems. This is an incredibly fertile electrical engineering field for work as research goes into having a car able to go approximately 40 or more miles on one charge primarily to get people to and from work. However, as work is not quite there yet this efficiency gain can be a huge step forward towards this millage goal (10).

1.2 Fundamental Advantages of Wide Bandgap Semiconductor Materials

It is important not only to find uses for the new WBG semiconductors, but to also understand what their properties are, how they work, and what advantages they carry in addition to the higher temperature operation. It is important to note that there are a variety of WBG semiconductors with a variety of different properties, some better in certain aspects than silicon, some less advantageous than others. Table 1.1 gives a succinct overview of the material properties of each of the major WBG materials that have been seen in recent research. The table contains not only promising new materials but current and past technologies such as Germanium (Ge) which can be seen to not be a wide but a narrow bandgap material (11). There are several different fundamental material properties each having distinct changes on the operation of a device built on that material. Let us examine more closely some of these properties giving special attention to SiC as it not only appears currently be the most promising in terms of material properties but also one of the nearest to advance to market. This material is also of most interest to this project's sponsor the National Institute of Standards and Technology (NIST) (12).

Table 1.1 – Wide Bandgap Semiconductor Properties

Material	E_g (eV)	n_i (cm^{-3})	ε_r	μ_n (cm^2/V-s)	E_c (MV/cm)	V_{sat} (10^7 cm/s)	λ (W/cm-K)	Direct/ Indirect
Si	1.1	1.5E10	11.8	1350	0.3	1.0	1.5	I
Ge	0.66	2.4E13	16.0	3900	0.1	0.5	0.6	I
GaAs	1.4	1.8E6	12.8	8500	0.4	2.0	0.5	D
GaP	2.3	7.7E-1	11.1	350	1.3	1.4	0.8	I
InN	1.86	~1E3	9.6	3000	1.0	2.5	-	D
GaN	3.39	1.9E-10	9.0	900	3.3	2.5	1.3	D
4H-SiC	3.26	8.2E-9	10	~700	2.0	2.0	4.5	I
C	5.45	1.6E-27	5.5	1900	5.6	2.7	20	I
BN	6.0	1.6E-31	7.1	5	10	1.0	13	I
AlN	6.1	~1E-31	8.7	110	11.7	1.8	2.5	D

1.2.1 Bandgap

The bandgap (E_g) is the predominate property dictating the thermal resilience of the semiconductor. The bandgap describes the separation of the valance and the conduction band in the traditional semiconductor band diagram. For an electron to become a free carrier it must cross the bandgap from the valance band to the state of higher energy the conduction band. The bandgap is described in energy, electron volts (eV), as the amount of energy that an electron must gain to cross the bandgap. This energy commonly comes from thermal energy, and thus for a wider bandgap at an equal temperature fewer electron hole pairs will be formed and there will be less undesired mobile charge carriers formed in the semiconductor.

Semiconductors may also have a direct or indirect bandgap. This corresponds to the valence and conduction bands versus the wave number or vector (k) by taking the energy band diagram into the third dimension. Regardless of E_V or E_C vs. k the bandgap is measured typically from the lowest energy of E_C to the highest E_V, if these points happen to be at the same wave vector, k, then the material is known to have a direct bandgap and the electrons and hole transfer more quickly at the same wave vector thus these materials will have lower carrier lifetimes leading to faster devices (13). What is also very important to note as it is a great advantage of this direct bandgap is that electrons emit their energy as a photon thus releasing light; Si and SiC are both indirect bandgap semiconductors thus alternative WBG semiconductors are needed in the area of lasers and optics (14).

1.2.2 Intrinsic Carrier Concentration

The intrinsic carrier concentration, n_i, is the average number of electron hole pairs in a given semiconductor per unit volume at equilibrium. It is a function of E_g by

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$$n_i = \sqrt{N_c N_v} \exp\left(-E_g\big/2kT\right) 1\big/cm^3 \tag{1.3}$$

where

$$N_c = 2\left(\frac{2\pi m_e^* kT}{h^2}\right)^{3/2} \tag{1.4}$$

and

$$N_v = 2\left(\frac{2\pi m_h^* kT}{h^2}\right)^{3/2} \tag{1.5}$$

where m_e^* and m_h^* are the effective mass of an electron and hole, respectively (13). It can be assumed $m_e^* = m_h^*$ for simplification, thus,

$$n_i = 2\left(\frac{m^* kT}{2\pi h^2}\right)^{3/2} \exp\left(-E_g\big/2kT\right) 1\big/cm^3 \tag{1.6}$$

It can be seen in the table that as the bandgap increases the carrier concentration begins to reduce drastically as desired. The values given are for room temperature where silicon is relatively high however SiC is observed to be over 18 orders of magnitude lower! Because it is an exponential relationship a few electron volts have a dramatic impact thus the large change between silicon and SiC but not so much between Si and Ge (15). The intrinsic carrier concentration is dependent on temperature which is what causes devices to become ineffective at higher temperatures; however as seen in Fig. 1.1, SiC and other WBG materials the intrinsic carrier concentration remain lower than silicon up to very high temperatures, within the range of most currently desired high temperature electronics (16).

1.2.3   Electric Field Strength

A material's electric field strength (E_{crit}) is the greatest determinant of its voltage blocking capability. Silicon has an $E_{crit}(Si) = 3e07$ V/cm, SiC has $E_{crit}(SiC) = 2e08$ V/cm, nearly an

order of magnitude higher. SiC has one of the lower critical electric fields of WBG materials with some ranging as high as $E_{crit} = 3.3e08$ V/cm (17).

1.2.4 Breakdown Voltage

The breakdown voltage (BDV) is the voltage up to which that a device will block across the blocking junction, preventing current flow without destroying the device. This is typically a PN junction as in MOSFETs, IGBTs, and JBS diodes, however it maybe a metal semiconductor junction as in a Schottky rectifier. The breakdown is determined by two important factors; one is a static material property, the E_{crit}, the other is a design dimension, the background doping concentration (N_A) of the drift region as seen in Fig. 1.2 (18). As voltage is applied to the junction the depletion region expands over the drift region more so than the n or p well where the inversion channel is primarily formed due to the lower doping concentration. The lower N_A is, the greater the width of depletion region, this leads to a lower voltage gradient ($^{dV}/_{dx}$) this gradient must be higher than the E_{crit} or the device will fail. Because when it is assumed the device has a sufficiently long drift region to avoid punch through materials have a direct relationship between blocking voltage and doping concentration as seen in Fig 1.3. Thus higher rated BDV devices have longer and more lightly doped drift regions. Because WBG materials have much higher E_{crit} they may have a much higher BDV without stretching out the drift region as far which has a low N_A (19).
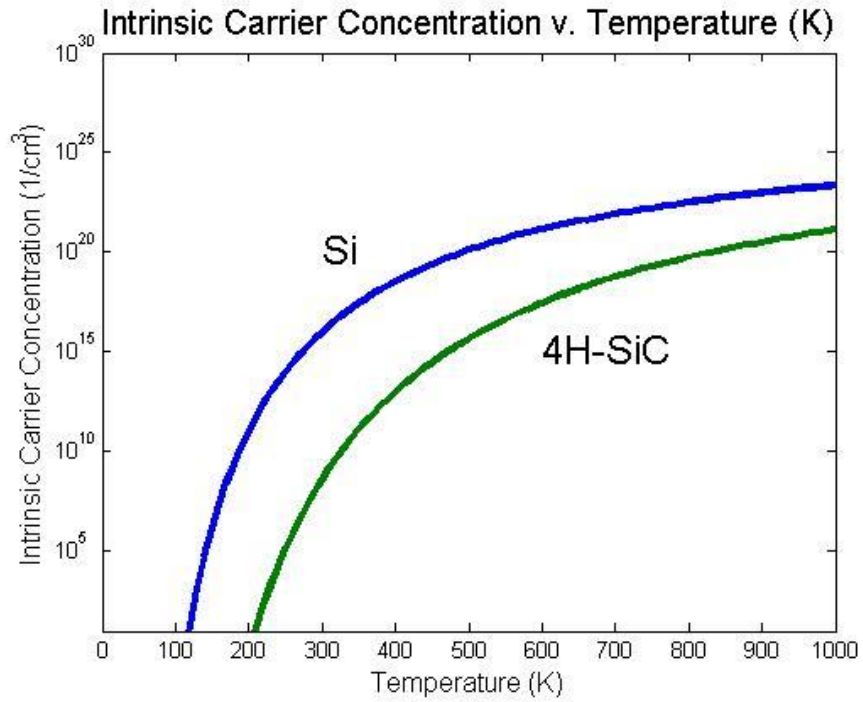
Figure 1.1 - Intrinsic Carrier Concentration v. Temperature in Si and SiC [16]
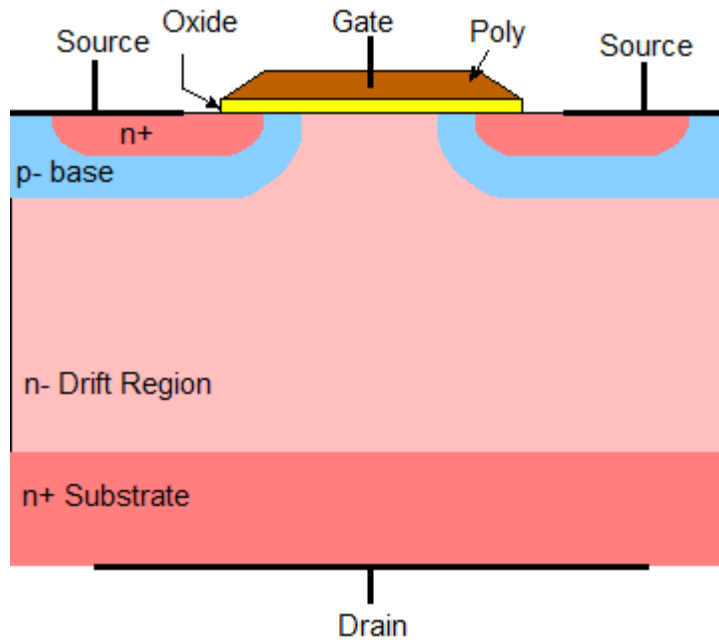
Figure 1.2 - Typical DMOS Device Structure [18]

1.2.5   Specific On Resistance

This high electric field strength is of great advantage to the specific on resistance ($SpR_{DS,ON}$) of the WBG devices as well. $SpR_{DS,ON}$ is the resistance through a semiconductor device at a certain gate voltage divided by the device active area. The high electric field strength allows for manipulation of two design dimensions that determine the $SpR_{DS,ON}$, N_A and the drift region width. Lowering N_A to increase BDV also increases the $SpR_{DS,ON}$, thus now that the E_{crit} is higher, N_A may be higher with a much higher blocking voltages than with Si, because the greater N_A keeps the depletion region thinner with equal or higher BDV thus the drift region may be much thinner which leads to reduction in $SpR_{DS,ON}$ as the majority carriers must pass through a shorter distance from drain to source. Similar to Fig. 1.3 the $SpR_{DS,ON}$ is linked to N_A as seen in Fig. 1.4 (20). SiC devices have shown to have $R_{DS,ON}$ up to 200 times smaller for comparable Si devices with the same blocking voltage (21).
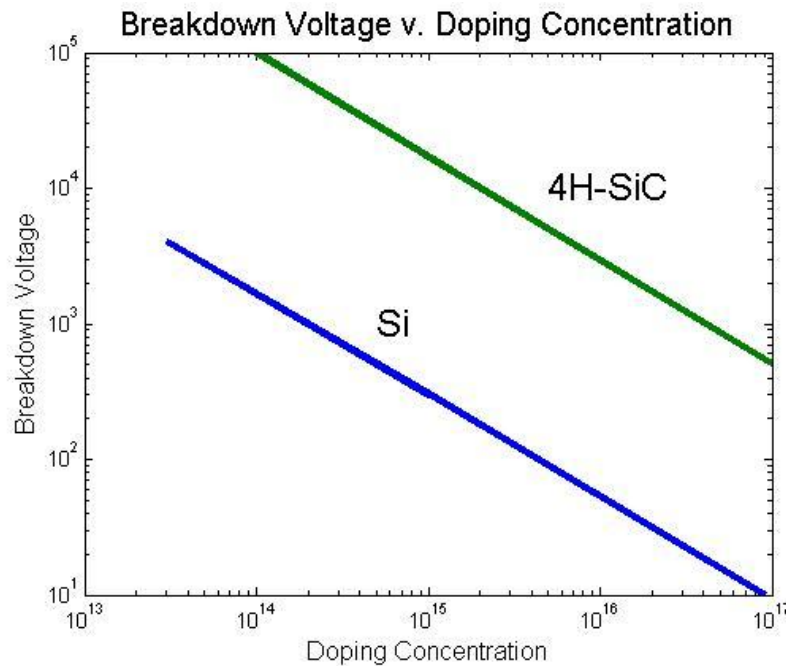
Figure   1.3   -   Breakdown   Voltage   versus   Doping Concentration in Si and SiC [19]

1.2.6 Mobility

Mobility (μ) is also changed in WBG material from Si. It is actually lower in some semiconductors, a negative unlike so many other WBG material properties; however it is negated by other advantages. The lower mobility in SiC and GaN does raise $SpR_{DS,ON}$ however, because the $SpR_{DS,ON}$ is already lower by the shortened drift region the effect is slightly neutralized except that is does make is slightly less practical for bipolar operation because of the further decreased mobility of the minority carriers (13).

While the decrease mobility of SiC does hold true over the entire temperature range, SiC suffers less from degeneracy cases at high doping concentrations where it is actually higher than Si above $N_D \leq 3e017$ (19).
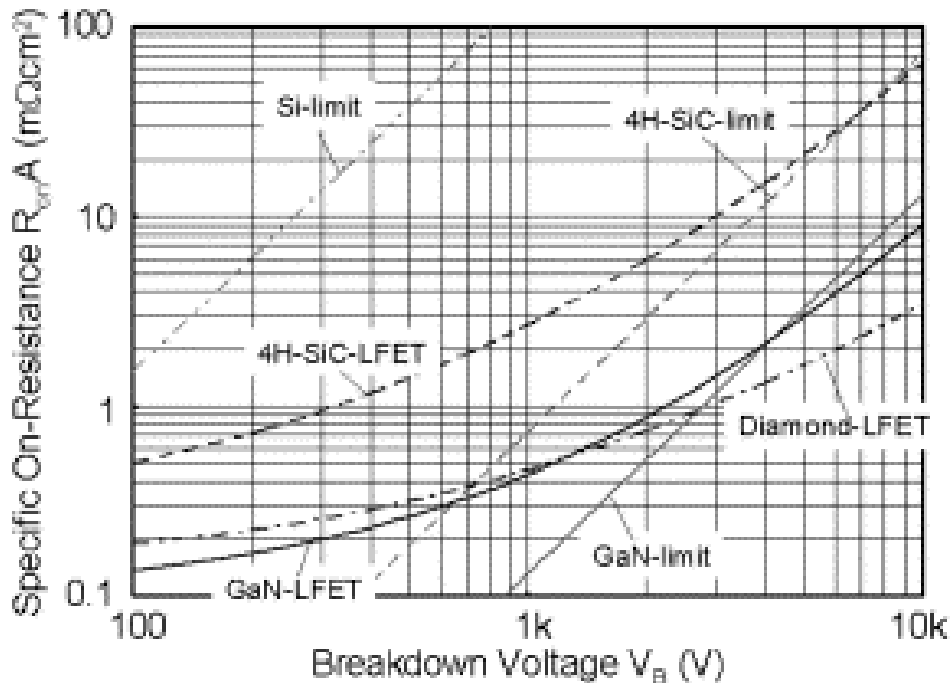
Figure 1.4 - Specific On-Resistance of Semiconductors v. Breakdown Voltage [20]

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CHAPTER 2   REVIEW OF PRIOR ART

The insulated gate bipolar transistor (IGBT) power module is an extremely popular component in power applications. There is currently an industry standard design for the half bridge power module with Si IGBT devices as the switching device with anti-parallel, freewheeling diodes. The design became popular in the early 1990s as the IGBT became more popular in the market place (22). The IGBT can be used in much greater power densities than the metal oxide semiconductor field effect transistor (MOSFET) at low frequencies due to its lower conduction loss, the module is seen in Fig. 2.1.

The half bridge design is designed to produce a sinusoidal output wave with an inductive load from a DC supply voltage. This makes it most useful for motor control applications where it is typically found in use such as in trains, electric vehicles, and other traction devices. As mentioned, since these fields are expected to grow for the foreseeable future due to the growing demand for electric powered transportation due to its environmentally friendly potential, it places an added importance on the design. The circuit is also used in high voltage power transmission; the circuit can simply be used to produce a static voltage output instead of sinusoidal and used in power delivery (23).

2.1   Enclosed Half Bridge Circuit Design and Operation

The common half bridge design can be seen in Fig. 2.2, it consists of a high side and low side switch with freewheeling diodes. In motor control operation and DC to AC voltage inversion the output voltage will ultimately be AC or sinusoidal, here the switching frequency is orders of magnitude higher than the output frequency thus a single switch cycle is nearly identical to that of operation for a DC output. The switch cycle can be seen in Fig. 2.3, where the

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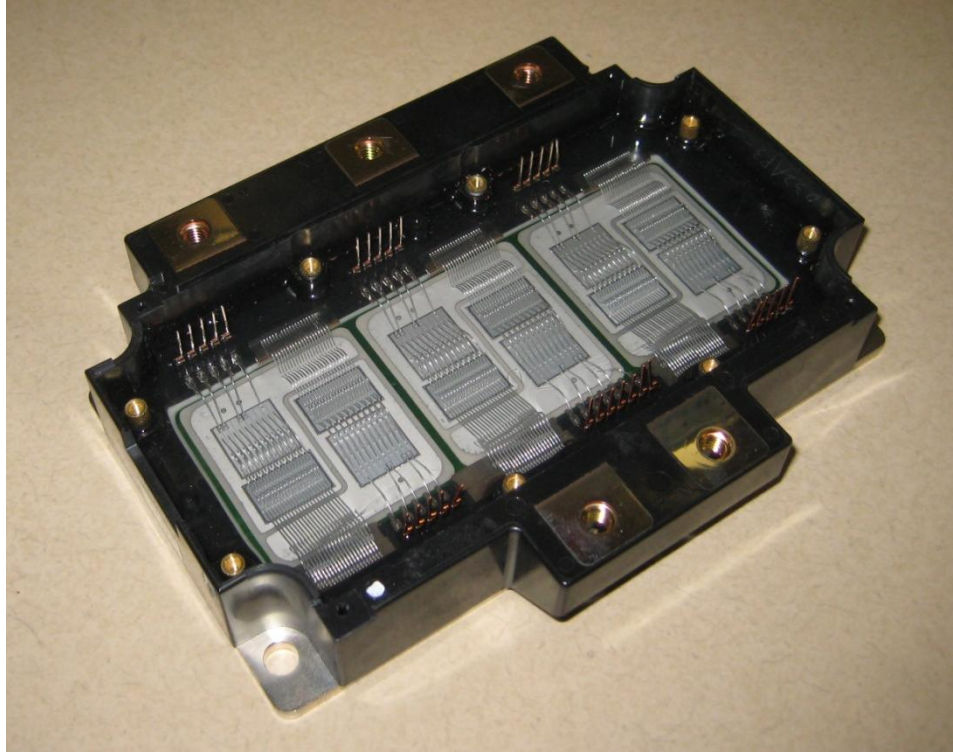
Figure 2.1 – Photograph of Traditional IGBT Power Module

switch and rectifier corresponding to the waveform are in conjunction with the opposing device from Fig. 2.2. As the high side switch turns on the output current (I_L) transfers from the low side diode to the IGBT, then as the diode approaches $I_L=0\ A$ the diode suffers reverse recovery current as seen in the current spike of the waveform, causing additional strain on the transistor. Once the excess charge carriers have been removed from the diode the IGBT current and the diode blocking voltage stabilizes. Over this period the IGBT current, which is the output current of the circuit at this time, is being raised infinitesimally due to the higher DC bus voltage of the transistor input. As the switch turns off, similar to the diode before, excess carriers exit the IGBT, this time while the blocking voltage rises; this again leads to switching power loss in the device and system. Once $I_L=0\ A$ in the switch the system is again in discharging state as in the beginning of the waveform figure where the current is actually going lower infinitesimally. The

control of the module will be either pulse width modulation (PWM) for a sinusoidal output or a static ratio corresponding to a single DC output voltage for the gates. Since the output current I_L is always changing slightly the on times of the devices must correspond to the output, it is also why the switching frequency is much higher than the output frequency. There is also to consider that both the IGBT and p-*i*-n diodes are dominated by switching losses, this is seen in the reverse recovery and the loss stemming from the rising blocking voltage with continuing current in the IGBT, therefore the circuit is bound by a reasonable operating frequency which is typically around 20 kHz (19) (23). These switching losses also produce heat leading to the robust thermal consideration to be looked at shortly, which dominate most all packaging designs for these power circuits.

The half bridge may also simply be modified; in some motor control application, a DC motor is connected to a high voltage DC and a half bridge circuit without freewheeling diodes. The low side switch is noted as the drive switch or MOSFET and when switched on, the current will flow back to the battery or voltage source to close the circuit. When the drive circuit is switched off the high side MOSFET is switched on as a freewheeling switch to allow the motor induced current to flow back to the motor (24). The half bridge circuit configuration can also be
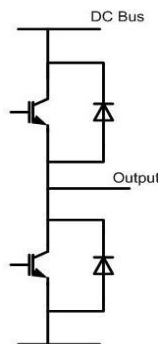
Figure 2.2 – Half Bridge Circuit Diagram   Figure 2.3 – Operation Switching Waveform [19]
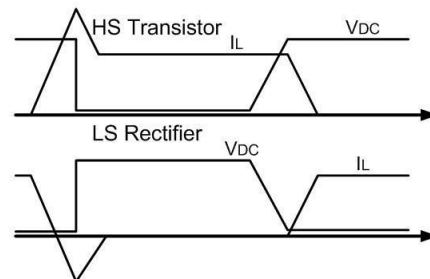
expanded to serve a similar role for three phase current, where three identical half bridges are placed in parallel with gate control to produce three AC voltages of the same frequency and amplitude but each 120 degrees out of phase. The circuit configuration and module topography can be seen in Figure 2.4.

Fortunately, in chapter 1 it is seen what the advantages of WBG semiconductors can do to improve device performance. Due to the lower intrinsic carrier concentration of SiC, there are much few minority carriers in unipolar devices, such as diodes, thus they have much less excess minority charge carriers than Si devices. If this concept is added to SiC JBS diodes then the switching loss of the diode can be almost entirely eliminated (25). In fact, SiC diodes have already been reported in working modules (26). Also, the lower $SpR_{DS,ON}$ makes it feasible to use SiC MOSFET (a unipolar device) instead of bipolar IGBTs. This leads first to lower conduction losses in the device, then again, the lesser minority charges will lead again to lower switching losses compared to Si IGBTs.
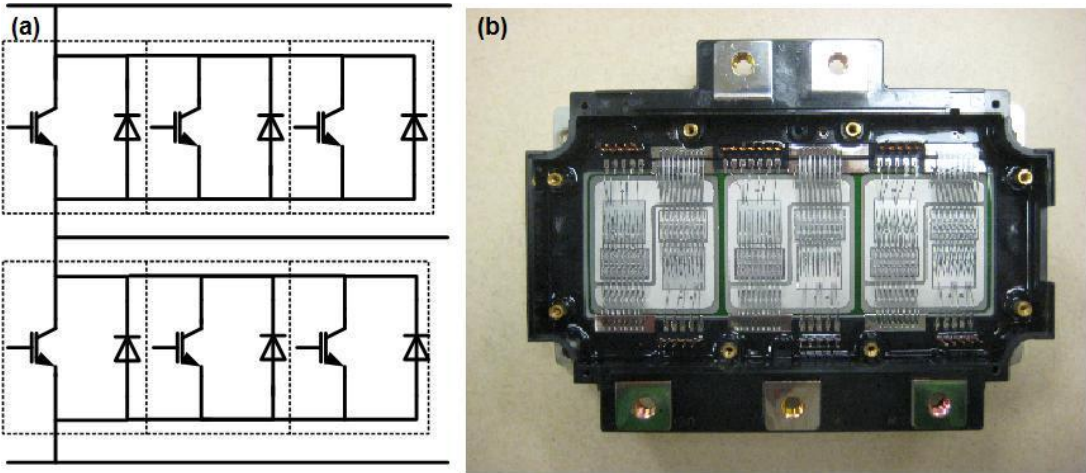
Figure 2.4 - Three Phase Half Bridge Circuit Diagram and Photograph

2.2   Traditional Power Module Design

Regardless of the exact circuit configuration or the number of phases or switches in each phase, the cross sectional view of the module has remained similar for nearly two decades which is where to find the greatest potential for improvements. There are a great deal of components within the module most of which are for more than simply the electrical connections. The typical cross sectional view of the power module is seen in Figure 2.5 (27). The design is robust and its construction begins with the placement of direct bonded copper (DBC) substrate. DBC is a sandwich structure of a ceramic with copper layer on either side, aluminum nitride (AlN) is the most preferable ceramic insulator because of its high thermal conductivity although aluminum oxide or silicon nitride may also be used because of their lower cost. The DBC structure is then cleaned and the power semiconductor devices are soldered to the top side of the DBC typically with a tin-lead solder. The DBC is then soldered to the heat spreader or baseplate with a lower melting point solder so as not to reflow the die attach solder material. This DBC structure is then firmly attached to the semi-heat resistant plastic enclosure which typically has the outer power
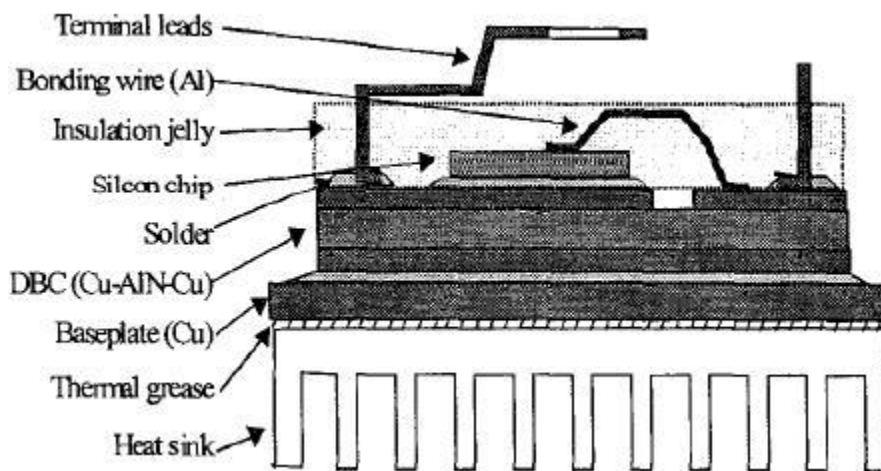
Figure 2.5 - Traditional Power Module Cross Section [27]

interconnects built into it. The device wire bonding or ribbon attachment is then done to connect the DBC traces to the power interconnects before or after placing it in the plastic packaging. Once the DBC and package are together and the devices are wirebonded it then is typically filled with a silicone based encapsulant gel for device protection, dielectric protection, and additional thermal conductance from the devices (28). This typically makes for a very large module with a mass upwards of 3 kg due primarily to the thick plastic packaging and the thick copper baseplate, none of which is necessary but for thermal and mechanical ruggedness.

2.3   Power Module Thermal Design Considerations

The power module is designed to bridge the need for electrical, thermal, and mechanical considerations. Design methodology dictates that once electrical credence has been paid thermo mechanics dominate the design leading to its large form factor. This is because when the module is in use the devices can be producing over 270W of power loss per device at a 10 kHz operating frequency with 114 W from conduction and an additional 164 W from switching losses (29). This immense amount of power manifests itself in the form of heat and thus the fundamental design goal is established, to remove the heat to keep $T_{j,max}$ of the device below 175° C. Also important is that because materials expand with temperature rise this large power can lead to mechanical stress from the material expansion.

Table 2.1 – Thermal Properties of Traditional Power Module Materials

Material	CTE (µm/m-K)	Conductivity (W/m-K)
Copper	16.4	385
Aluminum	24	210
Silicon	3.0	124
SnPb40 Solder	24	50
Aluminum Nitride	4.5	83
Thermal Grease		0.75

There are two primary characteristics of each material in terms of its thermal performance: coefficient of thermal expansion (CTE) and thermal conductivity. Each of materials within the typical power module featured in Table 2.1 with their applicable thermal properties. These characteristics are not functions of each other and both must be carefully considered in the module design.

2.3.1 *Coefficient of Thermal Expansion*

Every material has a CTE measured in parts per million per degree Celsius (ppm/C), it is the rate at which a material expands in response to heat, typically ceramics and non-ductile material have lower CTE, although some metals also have a low CTE. This is an important property because two joined materials that do not expand identically when heated will inflict stress on each other until a break occurs. It is this phenomenon that is the basis of nearly every single mechanical failure type in power modules.

The larger the CTE mismatch between joined materials the larger the stress per degree Celsius. It is also important to note that the CTE of Si (3.0 ppm/°C) or SiC (3.8 ppm/°C) because devices are typically fabricated in one of the two materials and are the only items that cannot be replaced from the module package. Therefore this low CTE is the benchmark for every other material CTE to be used in any power module. Since large CTE mismatch is bad, then ultimately every material should have as similar CTE to Si or SiC as possible. Unfortunately, some of the materials do not have low CTEs as desired, this often can be because of price of material or complication of changing the manufacture of the modules, but also it may be because the other material has a lower thermal resistance which is also important.

2.3.2 Thermal Resistance and Capacitance

Thermal conductivity is a measure of the rate at which heat passes through a material, it is the reciprocal of thermal resistance. The lower the resistance the material imposes on heat flow the less heating that material will incur upon itself. Therefore, like CTE each material should also have as low of thermal resistance as possible. Ideally if the total thermal resistance from the device to the heat sink were zero then although the device may be producing power loss of some magnitude there would still be $\Delta T=0°$, if that was the case then there would be no thermal expansion. The thermal resistance is exactly similar to electrical resistance only for heat flow, thermal capacitance, or specific heat capacity, is similar to electrical capacitance. This property is most important when considering switching; it is the heat capacity that holds the temperature up momentarily instead of it draining out instantly like a capacitor. Figure 2.6 gives and accurate thermal model of a power module with heat resistance and specific heat capacity of each material which are in series with each other where voltage is analogous to temperature and heat power flow to current (30).
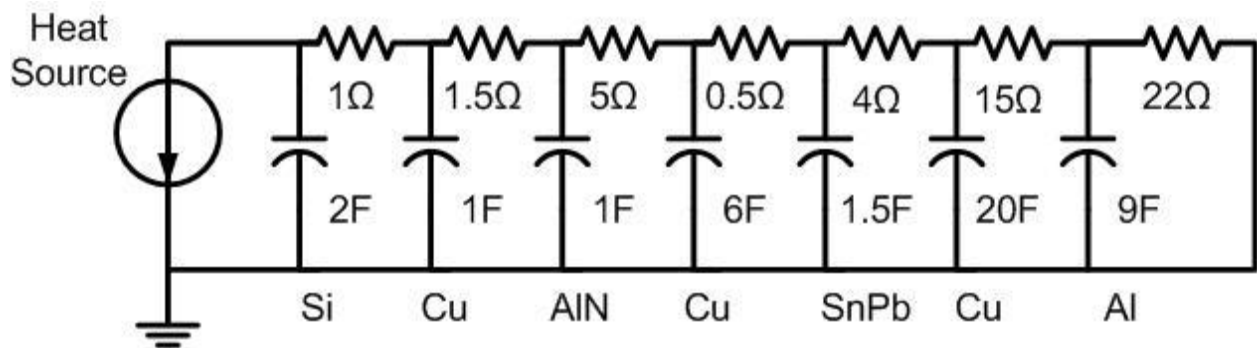
Figure 2.6 - Electro Thermal Equivalent Circuit Model [31]

2.4   Traditional Module Reliability Issues

Power modules endure a great deal of thermo-mechanical stress from the CTE mismatches within causing several types of failures and reliability degradations. Figure 2.7 displays the relationship of number of usage cycles and the total change in $T_{j,max}$ before failure (31). Reliability of a module is commonly expressed in cycles to failure vs. temperature change because change in temperature brings about a proportionate amount of stress depending on CTE due to thermal expansion. Measuring them in this manner is somewhat similar to aggregating all of the stress that has ever been placed on the module since its first use; a smaller ΔT each use produces less stress, thus and identical modules should operate more cycles with a smaller ΔT than the same with a greater ΔT. More importantly since power modules are used heavily in traction devices there is a great deal of thermal cycling involved in the field because of the
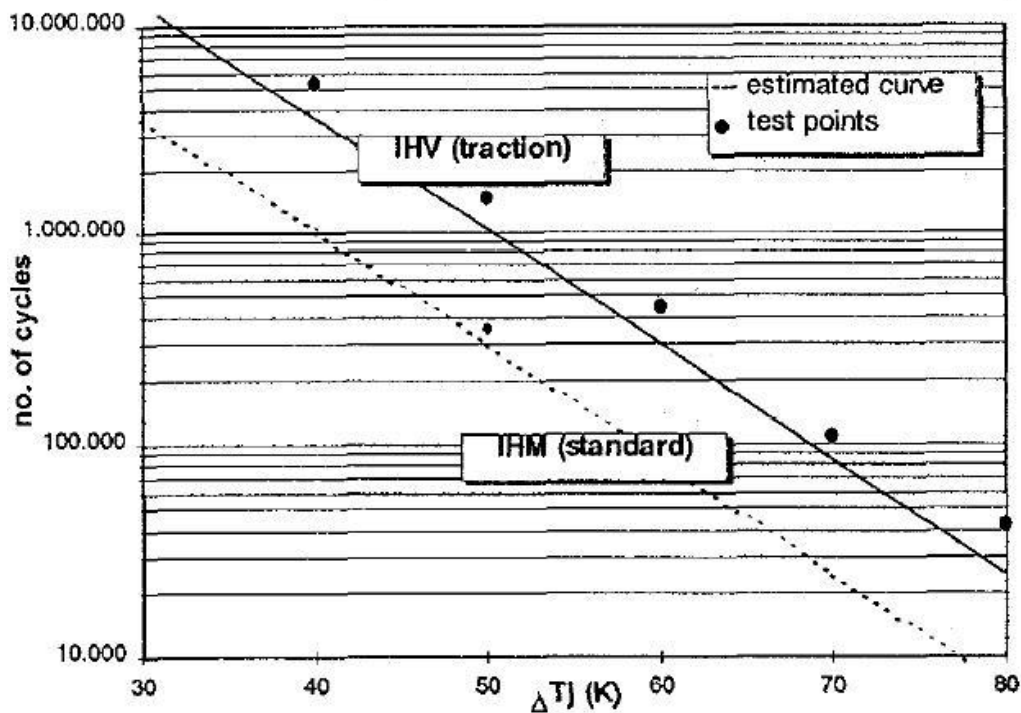
Figure 2.7 – Usage Cycles to Failure v. Temperature Rise Reliability Graph [31]

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constant starting and stopping of automobiles and other vehicles. All of this thermal cycling leads to several reoccurring reliability and failure issues.

2.4.1   Die Cracking of Device

Because typical tin lead solder (SnPb40) is sandwiched in between silicon and copper that have CTE mismatches of 20 ppm/°C and 10 ppm/°C respectively with the solder it becomes an easy target to relive some of the thermal stress in the package, this sometimes result in the solder itself cracking, as seen in Fig. 2.8, or in the device die itself cracking or breaking or breaking away from the solder (32). This sort of failure is somewhat less common due to the ductile properties of the solder.

2.4.2   Direct Bonded Copper Delamination

DBC exhibits good adhesion between the copper and the ceramic do to a copper oxide
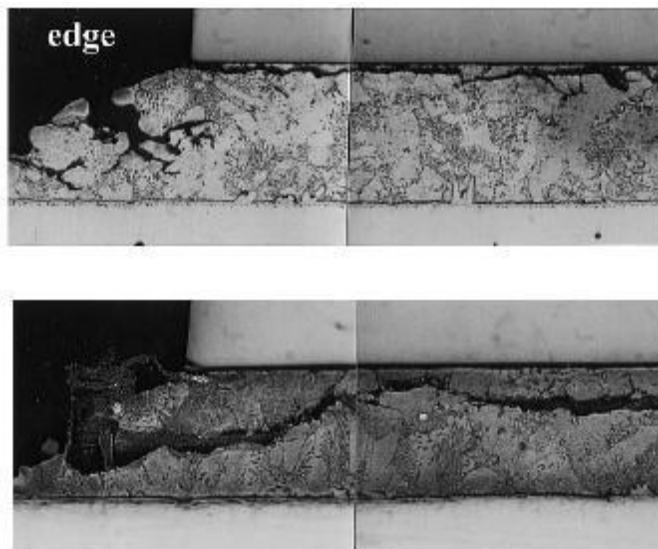
Figure 2.8 – SEM Cross Section of Solder Cracking Failure [32]

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bond layer that is formed by oxidizing the copper then annealing the oxidized copper surface to the ceramic at 1070°C (28). This is necessary to combat the 11.9 ppm/°C CTE mismatch between copper and AlN, the highest thermal conductivity ceramic insulator. If this adhesion fails it causes the DBC to liftoff of the ceramic substrate after several thermal cycles. When doing so, the copper layer may curl causing the solder to instantly break off. Or if the devices do maintain after copper delamination, it will cause the heat flow to bottle neck into whatever contact remains between the copper and ceramic, raising the effective thermal resistance several orders of magnitude. This will lead to a huge temperature rise at $T_{j,max}$, the solder, and wirebonds immediately leading to either device burnout where the die melts or causes another interface to succumb to CTE mismatch (33).

2.4.3   Wirebond Issues

The semiconductor die/wirebond interface is the cause of 80% of IGBT power module failures. Their problems cause two types of failures. One being the common CTE mismatch:
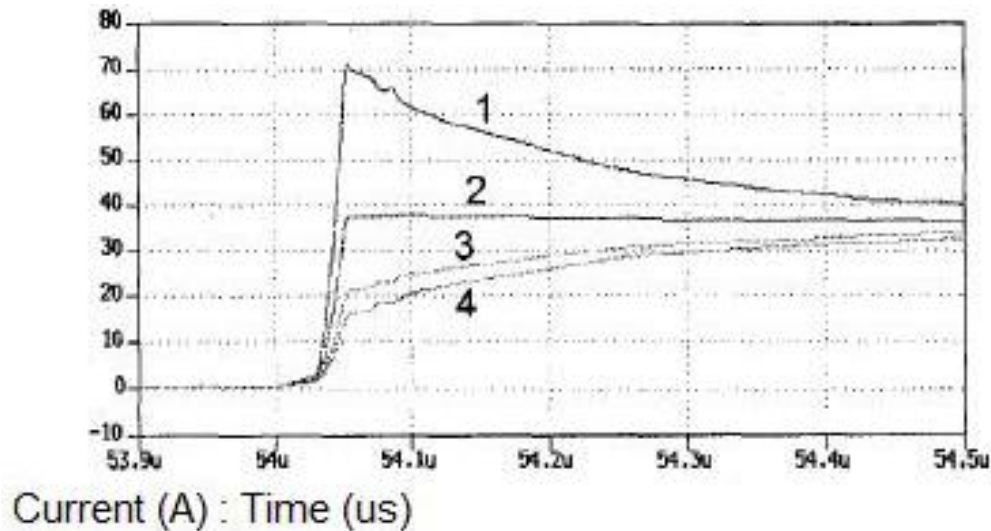
Figure 2.9 - Non-Uniform Current in Parallel Devices within Power Module [27]

liftoff; there is no ductile buffer between the Al wirebonds and the Si surface leaving only the 21 ppm/°C CTE mismatch between the two materials, a difference matched within the module only by the more ductile solder and Si interface (34). This wirebond connection is also the interface that experiences the highest temperature rise, leading to the most expansion of those materials which in turn leads to even more stress (35).

The other concern for the wirebonds is their mutual inductance. Their high power, linear current causes some inductance on other wirebonds within the module that can cause additional current within some devices. There is already the concern of reverse recovery currents from the power diodes inducing additional current in the IGBTs. The addition of parasitic inductance has the potential to destroy the devices by exceeding their current ratings with every switch. This phenomenon is especially true on the devices further from the center because there is likely to be a balance of the electromagnetic force acting on the inner wires, however the outer wires are not typically as inductively balanced and thus they are more prone to burnout (36). This phenomenon is seen in Fig. 2.9, a graph of the transient currents of devices in a module. The lower numbered devices are in the extremities of the module while the lower numbered modules are in the center area. It is seen that for several dozen microseconds the current can be at severe imbalance with some devices 100% higher than the steady state current and other 66% below it, easily pushing devices temporarily above their current rating.

2.5   Advancing Module Designs

There are ideas and designs currently being investigated in power module packaging also looking to introduce new high temperature WBG semiconductors into modules while also looking to address traditional problems with current modules.

2.5.1   ABB's Press Pack Module

The notion of the press pack module has been around as long as the semiconductor era dating back to 1969 with a Westinghouse design (37). What a press pack, Fig. 2.10, consists of is the use of a mechanical spring connection to one side of a die's electrical connections (38). Besides that point they are otherwise similar to preexisting modules, which also makes them a less drastic, less costly manufacturing jump. The substitution of the wirebond is advantageous due to the increase in cooling capability from the potentially robust metal contact on the spring; also the potential for less inductance, as well as the lack of CTE mismatch as there is no solder on the top contact therefore there is no rigid Si/Al interface to induce failure. Also admirable of the press pack design is that it has the ability to circumvent chip failure due to the springs constant contact with the device even if it fails unlike wirebonds that allow for an open circuit at
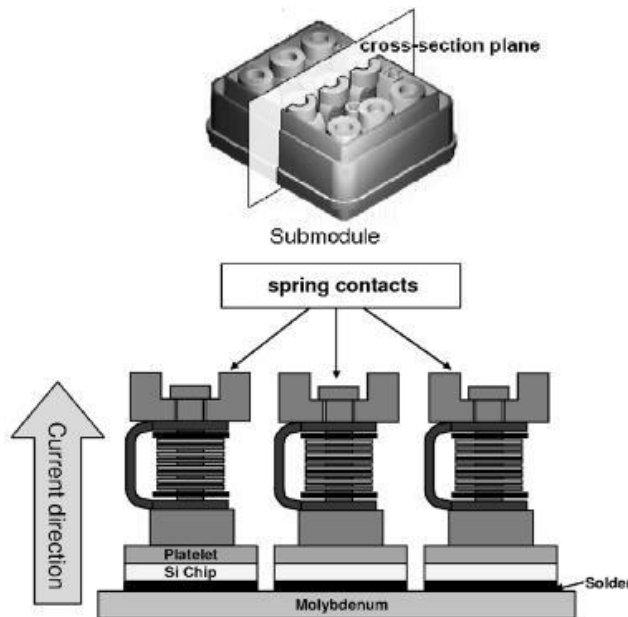
Figure 2.10 – Standard Press Pack Module Design Cross Section [38]

Figure 2.11 - ABB Press Pack Sub-Module Photograph [38]

failure. When the devices fail to short circuit if several modules are in series with each other current may continue to pass thought the module as the expense of resistance temporarily until replaced, this is utilized primarily when used for power conditioning when dozens of modules may be used in series.

Some of the latest work conducted on press pack modules has occurred at ABB Corporation in Zurich, Switzerland. They have developed a solder-less 1000A/4.5kV package seen Fig. 2.11. This press pack uses no solder at all which is not characteristic of all press packs however is possible due to the holding pressure of the pins; the lack of solder is also a point of merit according to ABB due to the supposed simplified manufacture. Also coming from ABB is the conceptualized design seen in Fig. 2.12 which is a design for a larger module composed of
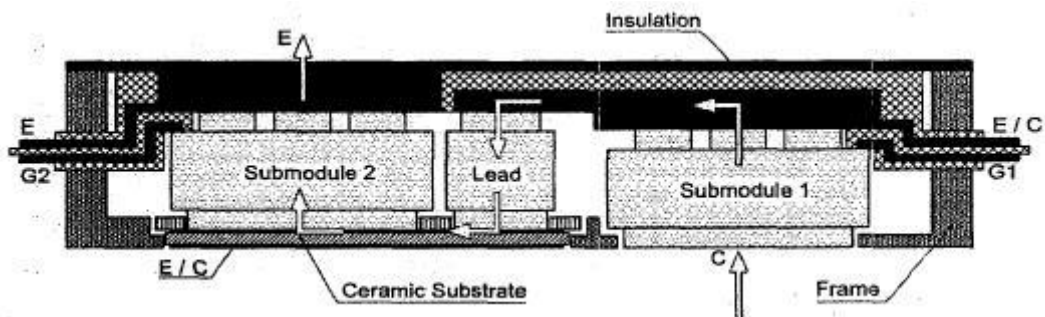
Figure 2.12 - ABB Module Conceptualization [39]

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smaller modules similar to Fig. 2.13 (39). Press packs have their advantages over traditional modules which dominate the market however they do share the fundamental problem of a larger form factor due to the inherent mechanical system, this new system may also bring in new reliability issues.

2.5.2   Alstom's Transit Module

The Alstom Corporation is a conglomerate of various business components that all work in some way in the power electronics field with branches dealing in transportation, power services, and power generation. They are headquartered in France near Paris and have approximately 80,000 employees. It is easy to see how they may be interested in the power module field however they do have some power module ideas that constitutes a few of their American patents; they have a variety of patents for all aspects of train transportation from signs to seats and some power module designs (40) (41) They happen to have one module design that is the most similar found to the PSRL design, the Alstom design is seen in Fig. 2.13 (42). The dual lead frame design does share resemblance to the PSRL module, seen in Fig. 5.1, with a similar design vision however the Alstom device circuit does not share the same design considerations. The new module comprises of components that make it superior to Alstom's module including encapsulation and junction termination considerations. These components make the PSRL module fundamentally able to carry a higher blocking voltage than the Alstom design. Also while the PSRL module is designed specifically for high temperature operation which this module does not consider, there is no mention of the electrical material which may or may not be copper which would severely limit the temperature usage due to mechanical package stress. There are few specific advantages of this design over previous modules named within the
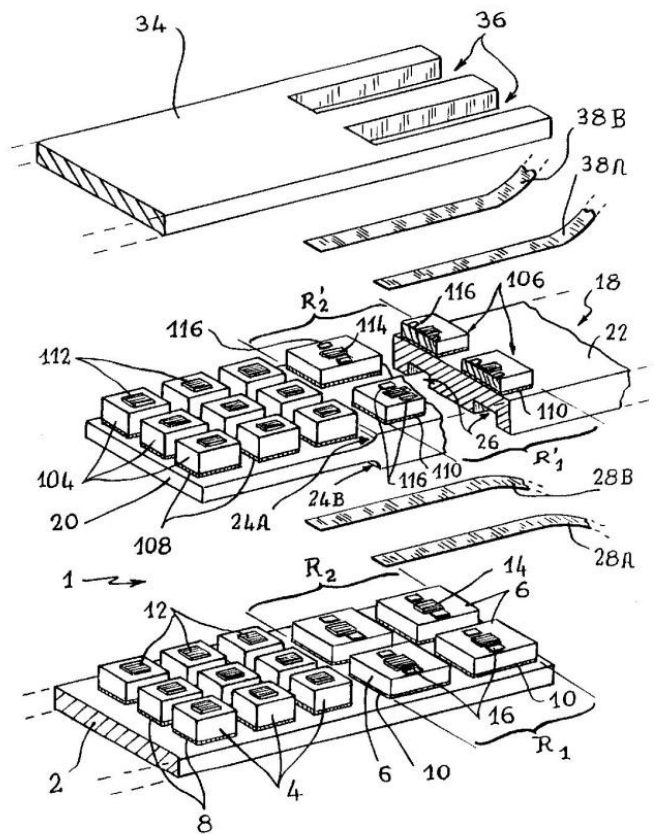
Figure 2.13 – Alstom Double Lead Frame Module Design [42]

design patent giving rise to questions about the intended advantages. This package is similar to the PSRL package however it does not give any noted additional benefits above that of press packs besides smaller form factor (37).

2.5.3   Semikron and Powerex Modules

Powerex and Semikron are leading power module companies offering a variety of traditional power modules with different circuit configurations. Their latest developments have been the introduction of new solderless packages (43). This is accomplished by the use of silver based epoxy or nano-sinter paste, it adds an ease of manufacture while also raising the thermal

rating of these new modules to 175°C from the 125°C to 150°C range. This thermal rise is accomplished due to removal of the low melting point of soft solders that pin all modules using it below 186°C. The modules that are not utilizing the nano-silver sintered paste have also begun to use ribbon connections between the chips for an improvement over wirebonds. Manufactures have also begun the separation of the module connection terminals by separating the input and output connections and moving them from the module face to the sides so that they may mount the control module atop them (44) (45). While the leading power module companies may have ideas in research they have demonstrated nothing as ambitious as the PSRL module.

2.5.4   Arkansas Power Electronics International's Hybrid Module

A group associated with the University of Arkansas called Arkansas Power Electronics International (APEI) has published a variety of papers dealing with the creation of a new power

Figure 2.14 – APEI's Hybrid Module Design [49]

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module for use to 300°C (46) (47) (48). They have a more advanced module than traditional designs by the inclusion of the gate driver circuitry within the module housing. The housing is a traditional high temperature semi-hermetic case with experimental encapsulation that does not adequately hold up to the 300°C environment, the module can be seen in Fig. 2.14 (49). It is excellent that APEI has demonstrated a working module at 300°C in high temperature ambient environments however it is clear to see that power devices are still in the antiquated old packaging complete with wirebonds, this package has a smaller chance of exceeding previous benchmarks in terms of reliability with bond wires as it has.

2.5.5   *Center for Power Electronics Systems' Double Sided Design*

The Center for Power Electronics Systems (CPES) is group based out of several universities funded by the National Science Foundation (NSF). CPES has done work in packaging and thermal characterization with much of this work being done in association with Virginia Polytechnic Institute and State University (50). They have proposed and built prototypes of a double sided cooling module as seen in Fig. 2.15 (51). It features power devices
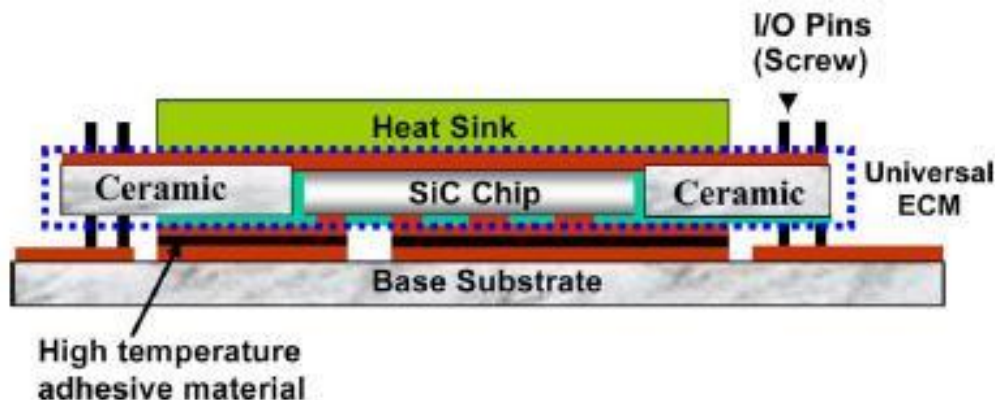
Figure 2.15 - CPES Double-Sided Cooling Module Design [51]

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inside of a ceramic layer with glass filler areas to seal SiC chips in place (52). Interconnect layers are then sputtered and etched for connections. This module is promising because it puts consideration into form factor and thermal stress physics and materials; it also employs high temperature materials such as nano-silver for electrical connections to allow for reliability to 300°C. This is some of the most promising packaging designs in discussion with several similarities to the PSRL module, and will continue to emulate the PSRL module as isolation is added to affix the proposed two heat sinks.

CHAPTER 3   NEW MODULE DESIGN CONCEPT

The objective of this project is to introduce a hybrid power module packaging concept that allows 300°C operation to leverage recent advances in SiC and other WBG semiconductor materials. What is proposed is a new power module architecture based on the use of double metal lead frames, direct lead frame-to-chip bonding, and high temperature encapsulation. A half-bridge circuit, comprised of two active SiC switches and two anti-parallel SiC diodes, is used as the specific design goal. The half-bridge circuit is the most basic building block in power electronics, which can be used in various combinations in electric vehicle motor drive inverters, power supply DC-DC converters, uninterruptible power supply DC/AC inverters, and many other applications. Nevertheless, the proposed module construction concept can be easily adapted to other circuit configurations such as three-phase inverters or even RF power circuits.

It is seen in previous chapters that there are a variety of both old problems and new potential for some new ideas for the next generation of power semiconductors. It is within the
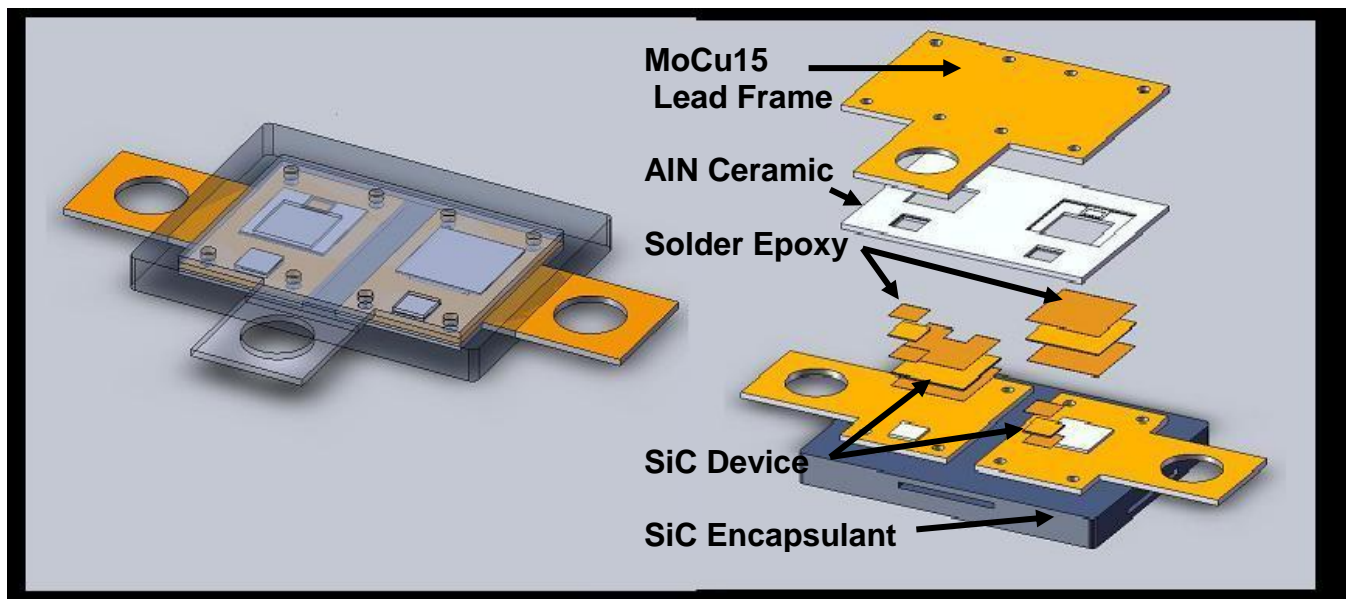
Figure 3.1 – Exploded View of PSRL Power Module Design Concept

project's goal is to learn from these problem areas to fully develop a half bridge circuit module with certain features that will give it a marked improvement over the standard power module design and a with more ambition than other SiC packaging designs in development. The initial design prototype can be seen in Fig. 3.1, it is simple with only four material layers from the SiC device to the exterior of the package. The fundamental goal of the module is to provide much improved long-term reliability for high-temperature applications. The module is the embodiment of five major design goals.

3.1   Coefficient of Thermal Expansion Matching Materials

As materials react to heat their volume changes according to their CTE, most often they expand in heat and contract in cooling. When two materials with different CTEs are bonded together as in previous Si IGBT power modules they will induce stress on each other with heating, which leads to most all power module failures over time (34). Traditional power modules use a great deal of copper, both in the DBC but also the baseplate, however copper's large CTE (16.4 ppm/°C) causes stress on other portions of the module leading to failure. It is the goal of this project to focus material selection on materials with CTEs closely resembling the low CTE of SiC (~3.8 ppm/°C). All materials much nearly match SiC because it is the one truly necessary material within the module that cannot be replaced for an alternative.

3.2   High Heat Capability Materials

SiC transistors have shown resilience up to 500°C for extended periods of time at constant operation (1), Si as a semiconductor does not stand up well to heat as its intrinsic carrier concentration goes to $n_i = 1e16 \ cm^{-3}$ at 300°C making it useless for use as a device (53).

Allowing devices in traditional packages to reach 300°C is also infeasible due to the CTE mismatch stress, once low CTE materials are chosen then the materials will be able to handle high temperature in terms of package stress. However the materials independent of the module will also be chosen in terms of independent temperature resilience such as melting point and oxidation while also staving off degradation for extended time periods at 300°C.

3.3   Removal of Wirebonds

Wirebonds provide a range of drawbacks for power semiconductors. Their failure mechanisms related to thermal cycling and their poor CTE matching is well documented (34) (35). They also induce undesirable inductance into the system dampening switching frequency for future high frequency goals associated with SiC packaging (27) (54). The module package design will be devoid of wirebonds on all drain, source, anode, and cathode connections for these reasons. Without them the package will carry less parasitic inductance than current module designs and is capable of half the thermal resistance. The removal of wirebonds makes way for a CTE matching material plate to serve as the electrical connection to and from the device.

3.4   Double-Sided Cooling Design

This wirebond-less design allows for a coveted double-sided cooling design that allows heat to be removed from both sides of the package. Because wirebonds are very thin and are typically surrounded by a moderately high thermal resistance silica gel they do an inadequate job of removing heat from the device, thus the need for such an elaborate low thermal resistance path the on the opposite side of the device from the wirebonds directly to the only cooling face of the

module (28). The new package is thermally symmetric on both sides of the device thus allowing for improved heat removal from the device.

3.5   Low Profile Package

The replacement of wirebonds with a CTE matching electrical connection to the devices allows for double-sided cooling in conjunction with the use of high temperature capable materials, including the SiC devices, severely lessens the need for the elaborate heat path provided on one side of traditional modules. Without this bulky baseplate and DBC the form factor of the new module is approximately a 10 fold mass reduction from traditional modules which can weigh up to 3kg and up to a 5 fold volume reduction.

CHAPTER 4   SELECTION OF PACKAGING MATERIALS

The goals of the new power module design hinge on the inclusion of high temperature materials that significantly ease the CTE stress on the package. Some potential materials are well known while others are not. Some have been in use in electronics and high temperature packaging before due to their CTE matching characteristics yet one can look at using them in new ways. There are also extremely promising new materials that have not yet found their way into power module construction.

As seen in Fig. 4.1 there are 4 primary materials involved in the new module package, they include: device material, lead frame material, die attach material, and encapsulant material. These four basic materials will make up the entire power module opposed the traditional design which contains potentially ten different material components including the aluminum wirebonds, silica gel encapsulant, aluminum terminal leads, silicon devices, plastic encasement, soft solder, copper and ceramic DBC, low temperature soft solder, and copper baseplate. Table 4.1-4 diagrams the material information for potential use in the new power module.

4.1   Selection of Die Attach Materials

There are a variety of solder materials for the die-attach procedure for the new module design. Solders have the mechanical property important to them know as shear strength, it is their ability to hold under force described as

$$\tau = \frac{F}{A} \tag{4.1}$$

it is an important measure of the solder's ability to handle mechanical force applied to it such as from CTE mismatch.
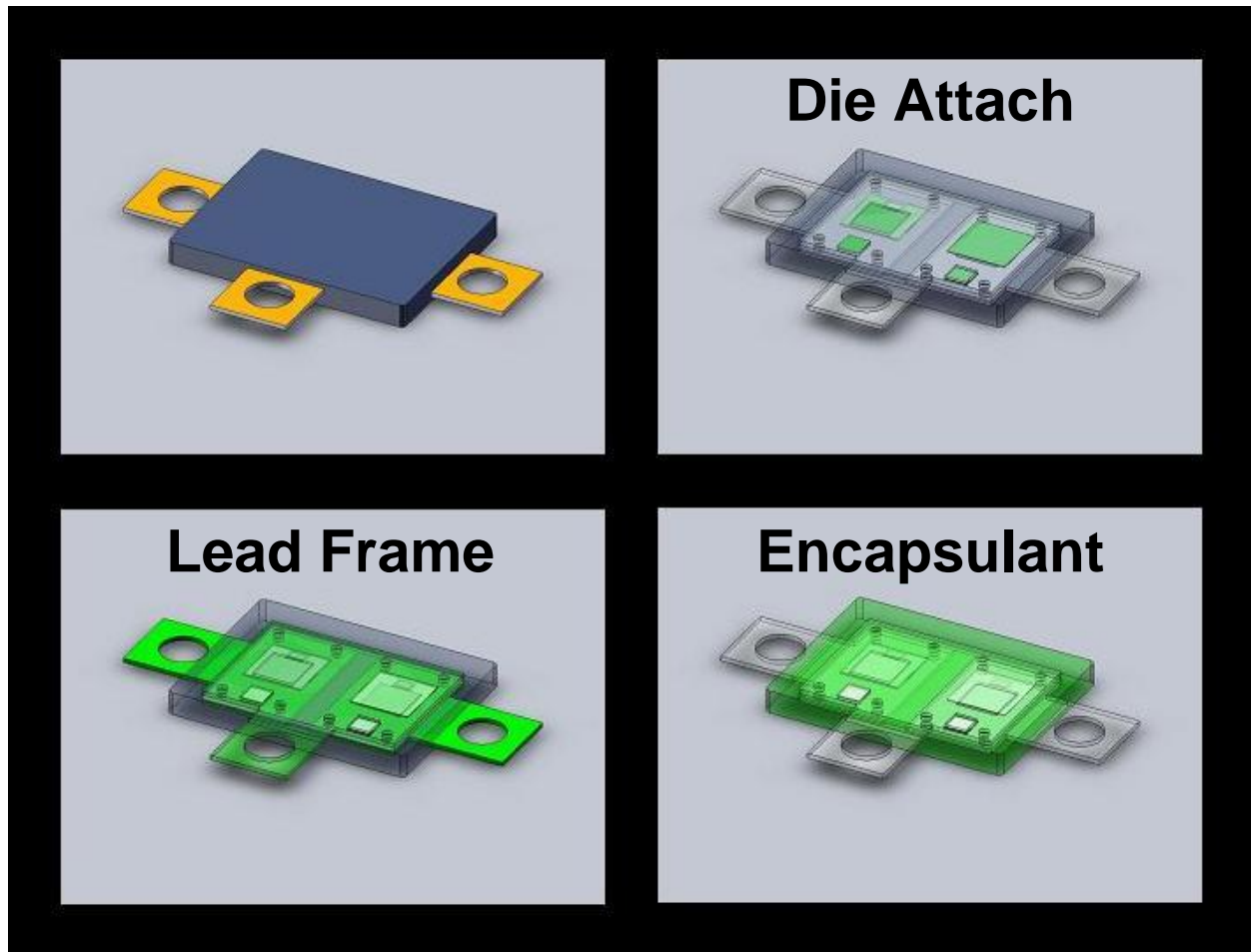
Figure 4.1 – View of Material Components within the PSRL Power Module

As seen, traditional soft solders (SnPb40, SnPb37, etc.) have a melting point far too (Solidus: 183°C) low to make use of the advantages of SiC therefore they must be replaced (55). The module's design goals require usage up to 300°C which means that the melting point must obviously exceed this value by a safe margin. Three extremely viable choices for solder rise above the rest thus far. One such solder is nanoTach, developed by Virginia Polytechnic Institute and State University, now distributed by BNE Tech, it is advertised as having a low processing temperature similar to a phase sintering process (also in development) in which the materials are sintered for a period of time with applied pressure to produce a high temperature product that

will perform up to the base material's melting temperature, in this case up to that of silver at 961°C (56) (57) (58) (59). It is attractive because of the high thermal conductivity (est. 240 W/m-k) however it is rather expensive for experimental testing ($20/gm). Also the high CTE would provide no gain over soft solders. The Aremco PyroDuct 597-A, is somewhat similar to the nanoTach, with unfortunately less desirable properties such as lower thermal conductivity and lower bonding shear strength, however it has a 2.3 ppm/°C CTE gain on the nanoTach at 17.3 ppm/°C and is considerably less expensive at ~$2/gm (60).

Gold-Germanium solder (AuGe12) has also distinguished itself as an alternative for high temperature die-attachment. It is a more traditional solder/braze that simply must be heated to the melting temperature to wet to the brazing surface. It is adequately priced for its gains and boasts a huge jump in bonding shear strength over all competitors. It has a higher CTE than SiC at 13.0 ppm/°C, but it is lower than the silver based epoxies and nano-particle choices and lower than traditional soft solders, showing a 8.6 ppm/°C improvement over traditional packaging and thus a 39.8% decrease in CTE mismatch (61). The largest drawback for the AuGe12 solder at this time is the difficult processing opposed to the silver particle solders making it difficult to use in non-industrial settings. This however is a small issue for industrial soldering as it is processing is similar to tin-lead solder only with higher temperatures involved (62).

4.2   Selection of Lead Frame Materials

Much like high temperature solders there are a variety of options for use of the electrical connections. Typically copper is used for both the DBC and the baseplate because it is so commercially available lowering the cost, but also the strong bond it forms with ceramics, also it is used for the baseplate because it acts as an excellent heat spreader it has an astounding 385

W/m-K thermal conductivity which is only comparable with pure silver (419 W/m-K) and pure carbon, diamond (2000 W/m-K) (63).

Carbon composites are interesting because they have such a high potential thermal conductivity infusing even some carbon into another material will make it much more thermally viable while also tuning their CTE which is in fact even more important. Synthetic crystalline carbon has a CTE of 1.18 ppm/°C which can be mixed into a higher CTE material melt, like copper, to reduce the alloy's CTE, this is the case for the composite materials from Plansee Corp. (64). These cutting edge materials, although expensive, can provide the best possible materials of any kind for thermo mechanical application.

Molybdenum is anther material that the electronics field has had its eye on for some time because it offers a good CTE match for SiC (4.8 ppm/°C). It is typically combined with copper in a laminate structure for baseplate applications to reduce the CTE (65). It can also be produced as an alloy for an additional cost. The alloy has advantages over pure molybdenum in that it raises it electrical conductivity because of the high value of copper's, while also making it easier to deposit film upon due to molybdenum's poor wetting characteristics, with only an acceptable rise in CTE (66). This highly thermal conductive material can also have nickel deposited on it to improve the wetting and adhesion of the solder materials.

4.3   Selection of Encapsulant Materials

The encapsulation material must be electrically insulating with the stated 300°C thermal limit minimum, it must also carry the highest thermal conductivity possible as it will be part of the short thermal conduction path to a potential heat sink from the devices. There are many attractive hydraulic setting ceramic materials due to their similar CTEs to the SiC power

semiconductors, also these materials have extremely high temperature limits as is expected of ceramics. They also carry a much higher thermal conductivity than a traditional encapsulant, Epoxy Cresol Novolac (ECN) which is the material that traditionally houses semiconductor die in single die housing such as TO-220 packaging and BGAs. It is used in one of the most similar manners as the PSRL module's encapsulant. It has a glass transition temperature of 165°C thus it could not work for in high temperature environments, however comparison reveals an extremely low thermal conductivity for this industry wide material when brought against the many alternatives (67). The Aremco Cermabond 865 is an AlN based adhesive ceramic with a high dielectric strength; it carries a great deal of potential to the module to provide as an insulating layer due to it adhesive nature. Cotronics Corporation also features a variety of high temperature epoxies with a range exceeding 300°C, these are non-ceramic based and thus they have a high viscosity excellent for potting (68).

Table 4.1 – Solder Material Properties

Material	Supplier	Base Material	Max Temperature (°C)	Electrical Conductivity (S/m)	Thermal Cond. (W/m-k)	CTE (ppm/k)	Bonding Shear (MPa)
SnPb40	Various	Sn	183	6.67E+06	49	21.6	52
PyroDuct 597A	**Aremco**	**Ag**	**650**	**5.00E+05**	**9.09**	**17.3**	**8.3**
PyroDuct 598A	Aremco	Ni	538	2.00E+04	2.57	11.7	
nanoTach	NBE Tech	Ag	961	3.80E+05	240e	19.6e	20-40
Duralco	Cotronics	Ag	343	5.00E+04	7.20		
XH9680-16	Namics	Ag		2.00E+05			
AuGe12	**Indium Corp**	**Au**	**356**	**6.63E+06**	**44.00**	**13.0**	**185**
PbInAg 92.5/5/2.5	Indium Corp	Pb	300	3.23E+06	25.00	25.0	
WS487 (AuIn19)	Williams Advanced	Au	487	4.88E+06	28.00	14.7	

Table 4.2 – Lead Frame Material Properties

Material	Supplier	Max Temp (°C)	Electrical Cond. (S/m)	Thermal Cond. (W/m-k)	CTE (ppm/K)	Density (g/cc)	Young's Modulus (GPa)	Poisson's Ratio
Copper		1083	5.88E+07	385.0	16.80	8.96	110	0.343
Diamond		4027	2.17E+01	2000.0	1.18	3.51	700	0.200
Molybdenum Copper (MoCu15)	Eagle Alloys	2617	1.87E+07	138.0	5.30	10.22	329	0.310
Copper Diamond Composite		1083	5.88E+07	210.0	17.8	8.96	110	0.343
Tungsten		3370	1.77E+07	163.3	4.40	19.30	400	0.280
Tungsten Copper (WCu10)	BAM	1083	1.56E+07	175.0	5.90	17.00		0.290
Tungsten Alloy (Ni/W/Cu 3.5/95/1.5)	CMW Inc.	1200	5.80E+06	137.0	4.43	18.00	310	0.280
Molybdenum Copper (MoCu15)	**CMW Inc.**	**1080**	**1.62E+07**	**140.0**	**6.50**	**9.92**	**248**	**0.325**
Copper Diamond Composite	Plansee	1020	1.11E+07	470.0	6.70	5.50	255	0.280
Aluminum Diamond Composite	Plansee	700	6.67E+06	440.0	7.00	3.00	220	0.270
Silver Diamond Composite	Plansee	990	1.18E+07	550.0	5.80	6.10	275	0.340

Table 4.3 – Encapsulant Material Properties

Material	Supplier	Base Material	Max Temperature (°C)	Electrical Conductivity (S/m)	Thermal Cond. (W/m-k)	CTE (μm/m-°C)
Epoxy Cresol Novolac		SiO2	165		0.67	18-65
Cermacast 575N	Aremco	Al2O3	1650	1.0E-07	28.00	
Cermacast 646N	Aremco	ZrO2	1650	1.0E-07	2.00	
Cermacast 673N	Aremco	SiC	1750	1.0E-07	36.00	
Cermabond 865	Aremco	AlN	1650		136.40	2.70
Durapot 863	**Cotronics**	**Polymer**	**343**	**1.0E-12**	**1.30**	**34.00**
Duralco 4460	Cotronics	Polymer	260	1.0E-11	0.58	64.00
VECTRA S135 LCP	Ticona	Glass	350	1.0E-13		
VECTRA E130i LCP	Ticona	Glass	300	1.0E-11		
EPM-2482	NuSil	Si	260	1.0E-12		

Table 4.4 – Semiconductor Device Material Properties

Material	Max Temperature (°C)	Electrical Conductivity (Undoped) (S/m)	Thermal Cond. (W/m-k)	CTE (μm/m-°C)	Density (g/cc)	Young's Modulus (GPa)	Poisson's Ratio
Silicon	150	1.00E+04	124	3.61	2.33	112.4	0.280
Silicon Carbide	600	1.00E+05	250	3.80	3.21	440.0	0.183

CHAPTER 5   FINITE ELEMENT MODELING

Modeling data has been compiled simultaneously for two module designs to coincide with experimental data. The full power module design has been designed and simulated along with a simplified module consisting of a single power diode, two lead frames, an adhesive layer, and the encapsulant. Simulation work has been done with a variety of programs for both thermal and mechanical simulations of the module. Thermal simulations have been done in Saber® Software by Synopsys and COMSOL® software; thermal and mechanical simulations have been done thus far in Ansys® and primarily COSMOS® by Solidworks Corp.

COMSOL, Ansys, and COSMOS are finite element analysis (FEA) design and simulation tools, they use a 3-D model of the module and solve various thermal and mechanical equations at each node of a mesh determined by the user, a range of node densities are possible with the trade off of longer simulation time for less robust results and the possibility of a non-converging simulation typically yielding no results. Saber is a spice modeler; it discretizes
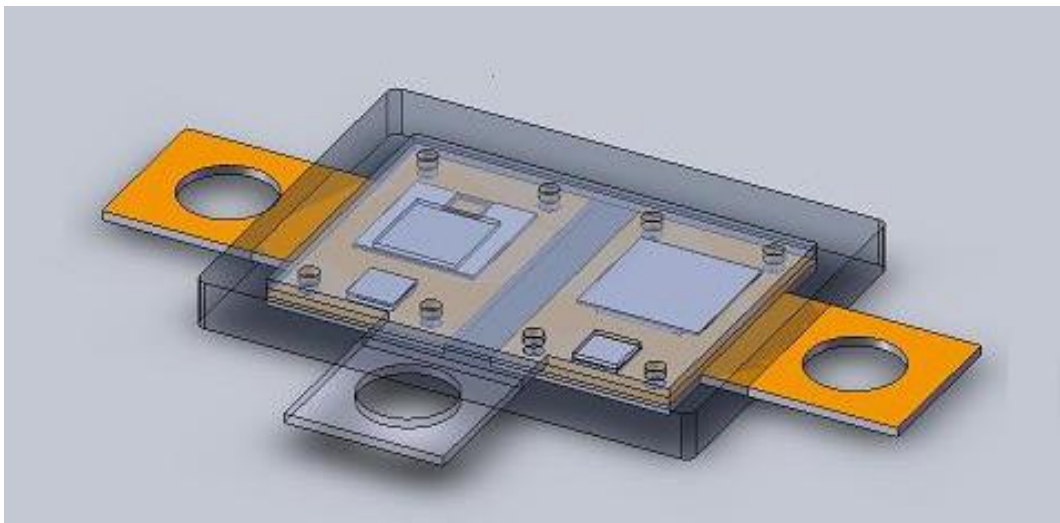
Figure 5.1 – Transparent Design of PSRL Half Bridge Power Module

elements of the design into an equivalent circuit model as is possible with thermal characteristics, as seen previously in Fig. 2.7. All simulators revealed applicable results however some were used in an evaluative process and were not heavily relied upon to produce results.

5.1   Module Design Methodology

The modeled design of the half bridge power module can be seen in Fig 5.1 it is complete with three lead frames for the three nodes of a half bridge circuit. It has soldered interfaces on each side of each of the 4 devices within the package, 2 SiC MOSFETs and 2 SiC JBS diodes, although the actual devices within the SiC substrate modeled is irrelevant at this point, only the power loss emitting from them. The model is also built with an insulating layer separating the lead frames from each other and to practically provide as an adhesive layer to provide greater strength to the package. It can also be seen on the lead frames that they are designed with a standoff or mesa from the planar face of the lead frame to connect to the anode of the diode and the source of the MOSFET. These are designed with considerations for junction termination, or junction termination extensions (JTE), and voltage blocking capabilities. The more precise connections allowable by use of the standoffs eliminates the entire face of the device die being connected to the lead frame which would undermine device JTE by shorting the edges of the die to the lead frame which are not typically designed to block a high voltage over the entire top plane of the device. Typically just the anode and not the entire face of the device is at the blocked voltage which can be connected to precisely by use of wirebonds or the designed standoff. Also the standoff allows for greater separation from the gate node on the face of the MOSFET die, an additional connection will be made to the precise gate node later however it is not yet fully considered in the simulation because it does not have great impact on the thermal or

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mechanical properties of the package, the gate connection technique will be largely excluded from this paper's discussion.

The holes seen through the lead frames also come with a two distinct purposes. One necessary purpose of the holes is as a manufacturing alignment system. The alignment of the holes will ensure alignment between the output frame and high side frame and low side frame. More than simply visually aligning the frames, the holes can also be used as a means of securing the frames into a manufacturing mold (as was done), temporary securing pins may be placed through the alignment holes during solder reflow and/or adhesive insertion to give the unfinished module or prototype greater mechanical strength until the module is complete and fully secure.

After the module is complete the alignment holes will serve a purpose of provided mechanical strength then too by the allowance of encapsulant to flow through the holes during construction. The addition of encapsulant though the lead frames gives additional tensile and compressive strength between the lead frames. (The complete designs of the module complete with dimensions may be seen in Appendix A.)

An additional module has been simulated for manufacturing consideration, comparison, and design. The simplified module, Fig. 5.2, is the first phase of construction. It has been simulated so that the results may be compared against each other before continuing on to full module construction. It consists of a diode chip in the sandwich structure similar to the full module design, with two lead frames consisting of the anode and cathode connections. It is also modeled with an adhesive layer between the plates to add mechanical strength. A single diode is used so that the total power loss in the system by the diode can be precisely calculated and measured during simulation, while the junction temperature, $T_{j,max}$, may also be measured during experiment because of the temperature dependence on the operation of the device (69) (70).
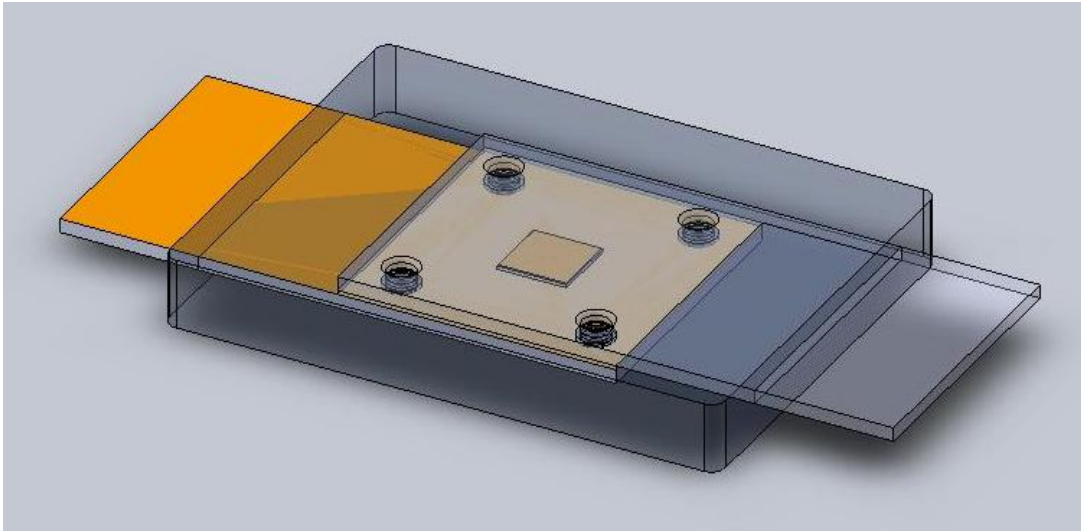
Figure 5.2 – Transparent Design of Single Device Module

For the simulations the material data of materials which has been purchased to prototype the single device module to be discussed in the following chapter was used, but also to maintain a level of comparability across all simulations. The materials simulated as a default for module design are SiC devices, MoCu15 for the lead frame, Cermacast 673N for the encapsulant, Cermabond 865 as an adhesive insulator, and AuGe12 solder. The applicable material properties for thermal and mechanical simulation for each of these particular materials are listed in Tables 4.1-4.

5.2 Thermal Modeling and Discussion

5.2.1 *Saber Thermal Circuit Modeling*

As previously mentioned, Saber Simulator by Synopsys is a circuit based simulator. In order for Saber to compute any thermal output properties it must derive a thermal circuit model similar to Fig. 2.7 or have one input. The model has been derived by breaking the thermal path

into volumetric nodes, and computing an effective thermal resistance and heat capacity of that node. This model building style, done by use of the user created program *mod_test_1*, is used by precedence set by NIST in doing identical thermal simulations on DBC substrates with single or multiple chips. The thermal simulation will assume one chip so that the results may be compared to the Single device module design. The model creator program, *mod_test_1*, inputs the thermal resistance, specific heat capacity, density, and thickness of each material layer (not node). The thicknesses are used to then create 5 nodes of as portions of that material stack, similar to that of Fig. 5.3. These 5 nodes will then have thermal resistances and heat capacitance, C, as determined by the proportional makeup of the material layers comprising of the node. The thermal resistances of the layers and portions of the partial layers within the node summate to create a node resistance, the heat capacities are found by Eqn. 5.1 which takes in the specific heat capacity, C_p; density, ρ; and the effective volume of the material layer, V_{eff}.

$$\frac{1}{C_{node}} = \frac{1}{C_{layer\ 1}} + \frac{1}{C_{layer\ 2}} + \cdots + \frac{1}{C_{layer\ n}}$$ (5.1)

where

$$C_{layer} = C_p \cdot \rho \cdot V_{eff}$$ (5.2)

This particular model assumes that the module is also placed on a heat sink which has 3 additional nodes within it going to a tunable depth. The heat spreading angle though the material layers was fixed throughout the structure and was assumed to be 45° in disagreement with the heat spread angle, α, being a function of the thermal conductivities, k, of the material layers by
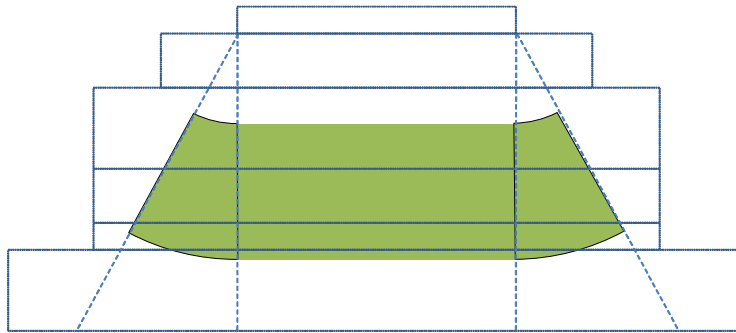
Figure 5.3 – Cross Section of Saber Simulator Nodal Calculation Method

$$\alpha = \tan^{-1}\frac{k_1}{k_2} \tag{5.3}$$

However, this model using a uniform $\alpha=45°$ has shown agreeable results (71).

The *mod_test_1* had one particular drawback in that it could only produce a single-sided heat path; the equivalent circuit model could not be added in parallel to make a double sided heat path due to the DBC design initial assumption, thus the results were post processed to account for this effect. Also due to this alteration a Single device, single-sided cooling module model was built for results comparison and simulation validation in COSMOS. The effective thermal model of the Saber model built for COSMOS can be seen in Fig. 5.4.
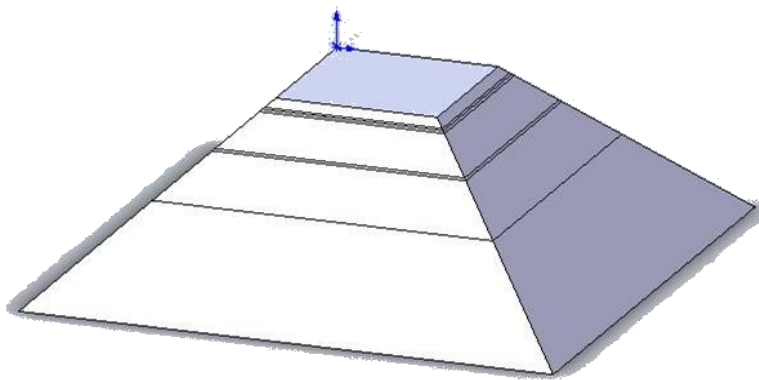
Figure 5.4 - COSMOS Model Design of Equivalent Saber Circuit

The results were compared through a combination of steady state and transient power input comparisons. For all simulations a steady state or transient power input, Q, is applied directly to the SiC device and the fixed temperature of 25°C is assigned to the heat sink base as the reference point. Because the Saber does all simulation in a transient evaluation the COSMOS simulations are done as transient chip heating although they do agree with a simplified steady state simulation. The entire structure is assumed to be at 25°C at $t=0$. Also, because the exact temperature values cannot be extracted from each point in Saber as is possible with COSMOS the average value of the SiC temperature is used for comparison for both simulators as opposed to the peak temperature of the device. The response of the single-sided cooling module from Fig. 5.4 can be seen in the results of Fig. 5.5 for the transient responds of a steady state 500W input distributed evenly throughout the SiC device.
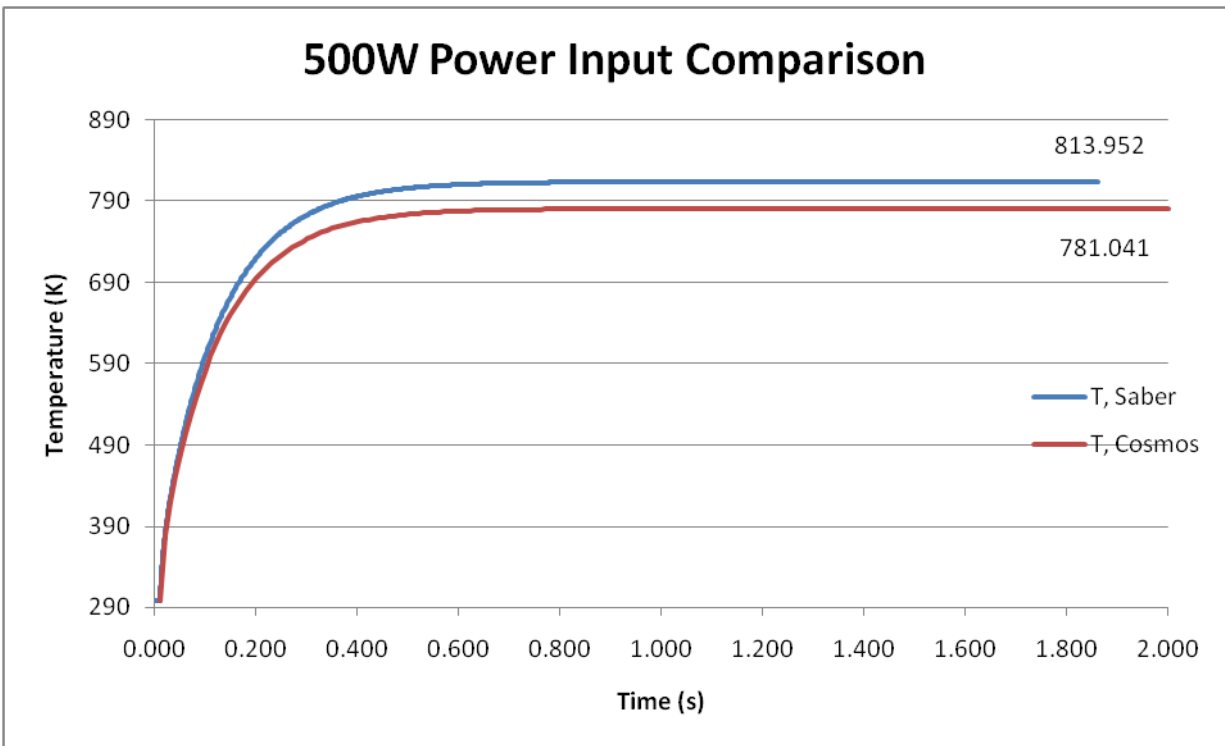
Figure 5.5 - Saber vs. COSMOS Steady State Heating Comparison at Steady 500W

The two chip heating curves do not match unfortunately as they should due to the identical system input properties and power, the two systems have identical layer properties and thicknesses with matching power inputs and base temperatures and an and initial steady state temperature. The heating plot of $0 \leq t \leq 2s$ has two distinct regions, the heating phase, and the steady state temperature portion. The chip temperature in the heating portion is combination of the thermal capacitance and thermal resistance while the once the temperature plateaus the capacitance does not alter the temperature and the temperature is solely determined by the thermal resistance to the ambient temperature and the power input by Eqn. 1.1.

The steady state temperatures in the two simulations for $Q = 500W$ are $T_{chip}(Saber) = 813.94°C$ and $T_{chip}(COMSOL) = 781.04°C$. This equates to thermal resistances, $R_{\theta~JH}$, of 1.03 K/W and 0.966 K/W for Saber and COSMOS respectively. These differences in temperature reflects a difference of $\Delta T=32.91°C$ and a thermal resistance difference of $\Delta R_{\theta JH}=0.0658~K/W$, this value equates to a 6.85% error, η, between the two simulated thermal resistances. Subsequent testing reveals a similar error figure for a variety of input powers as seen in Table 5.1 where the thermal resistance error is compared for multiple input powers. It is seen that once the power reaches the moderate value of 50W, $Q > 50W$, η is steady at ~6.7%.

In the heating phase thermal capacitance should play a vital role in the temperature of the device, however very little effects are seen from the heating capacitance possibly due to the high power of the simulations. With equal or no capacitance the thermal resistance is directly related to the temperature rise by

$$\eta = \frac{\Delta R_{\theta JH}}{R_{\theta JH}} = \frac{\Delta T(t)}{T_{rise}(t)}$$ (5.4)

at high power at all time instances. It is seen throughout this heating phase that the error remains close to 6.85% as $\eta(t = 0.1s) = 0.0596$ and $\eta(t = 0.3s) = 0.0674$. Thermal capacitances

should have a greater bearing on the temperature at lower powers. This is exemplified in Fig. 5.6 where the heating phase for $Q=18W$ reveals that the temperature of the COSMOS model rises above Saber model for $0 \leq t \leq 0.26s$ due to the capacitance of the Saber model being higher as the temperatures reach steady state and the Saber model reveals a greater temperature as is the case for every simulation, visible in Table 5.1.

Table 5.1 – Simulation Comparison Temperature Rise and Error Calculation

| Input Power | Steady State Temp. | | ΔT | Error, η |
| | Saber | COSMOS | | |
(W)	(K)	(K)	(K)	
18	316.4	315.9	0.48	0.027
50	349.6	346.5	3.10	0.063
100	401.1	394.8	6.38	0.065
150	452.7	443.1	9.60	0.065
200	504.5	491.5	12.98	0.067
300	607.6	588.1	19.52	0.067
400	710.8	684.8	26.03	0.067
500	814.0	781.0	32.91	0.067

The capacitive effects can be magnified even greater in a fully transient thermal analysis. Fig. 5.7 displays a 300W power input for 20ms, the capacitance of the materials greatly alters the temperature of the device with time, leading to transient thermal resistance of devices (72). Although the input properties of the devices are the same the transient effects of the devices are vastly different with the Saber simulation calculating a much larger effective capacitance on the device than the COSMOS model. For both simulations T_{max} occurs at $t = 30ms$ where $T_{max}(COSMOS) = 397.1°C$ and $T_{max}(Saber) = 379.1°C$. This is an astonishing $\Delta T = 18°C$ leading to error of 22.2%. The disparities of capacitances are seen in Fig.5.7 by the large ΔT throughout heating and the much larger cooling gradient again in the COSMOS simulation than in the Saber, thus a much lower capacitance in the COSMOS file than Saber.

It must be determined whether Saber is giving an incorrectly large capacitance or whether COSMOS is giving an incorrectly small capacitance. The layers of the materials act in series in

conductivity and capacitance, the equation for which was given in Eqn. 5.1. Investigating the nodal capacitance in Saber as computed by the *mod_test_1* file used at NIST reveals an incorrect nodal capacitance calculation. Here the capacitance is computed as a proportion of the density specific heat capacity product relative to the volume contribution to the node, this is incorrect as it should be computed as in Eqn. 5.1 as the material layers are still in series within the node. Not doing so will result in an inflated capacitance since a smaller capacitance would not dominate as correct in the series calculation. This is required because in the transient of temperature or voltage the lowest capacitance between two points would cause the greatest instantaneous impedance to the temperature path along with the other material capacitances which should also lower the total capacitance thus a low capacitance caused by a material layer should not be averaged out into a node which would neglect this effect.

The incorrect heat capacitances would be fixable however it would not cause an agreement with the thermal resistance disparity in the simulations. It also casts doubt on the accuracy of the thermal resistance measurement in Saber. This and the lack of robustness of the simulator due to its circuit based fundamental design make it a poor choice for continuation in this project. There is also the difficulty in adding a double-sided cooling equivalent circuit along with the simulator being devoid of any mechanical simulation properties. COSMOS not only has all of these thing but most importantly the linkage of the point specific heating data to the thermal expansion of the materials, leading to the point specific mechanical stress data that will be made use of later. These deficiencies lead us to the suspension of use of Saber and the continuation of use of COSMOS for thermal and mechanical simulation.
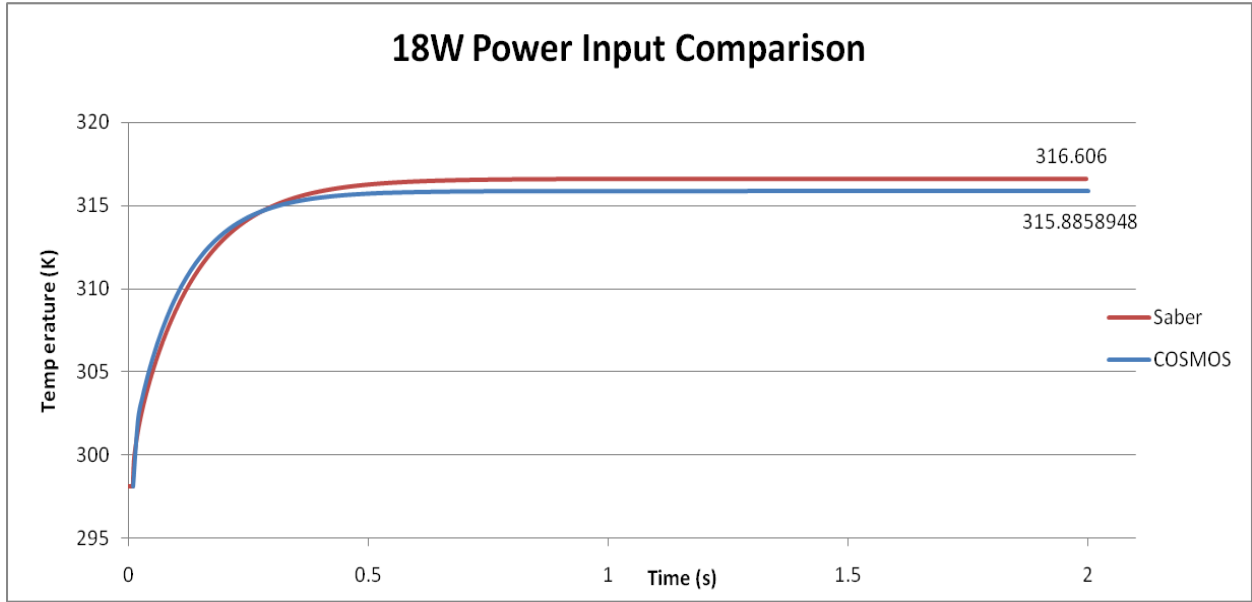
Figure 5.6 - Saber vs. COSMOS Steady State Heating Comparison at 18W
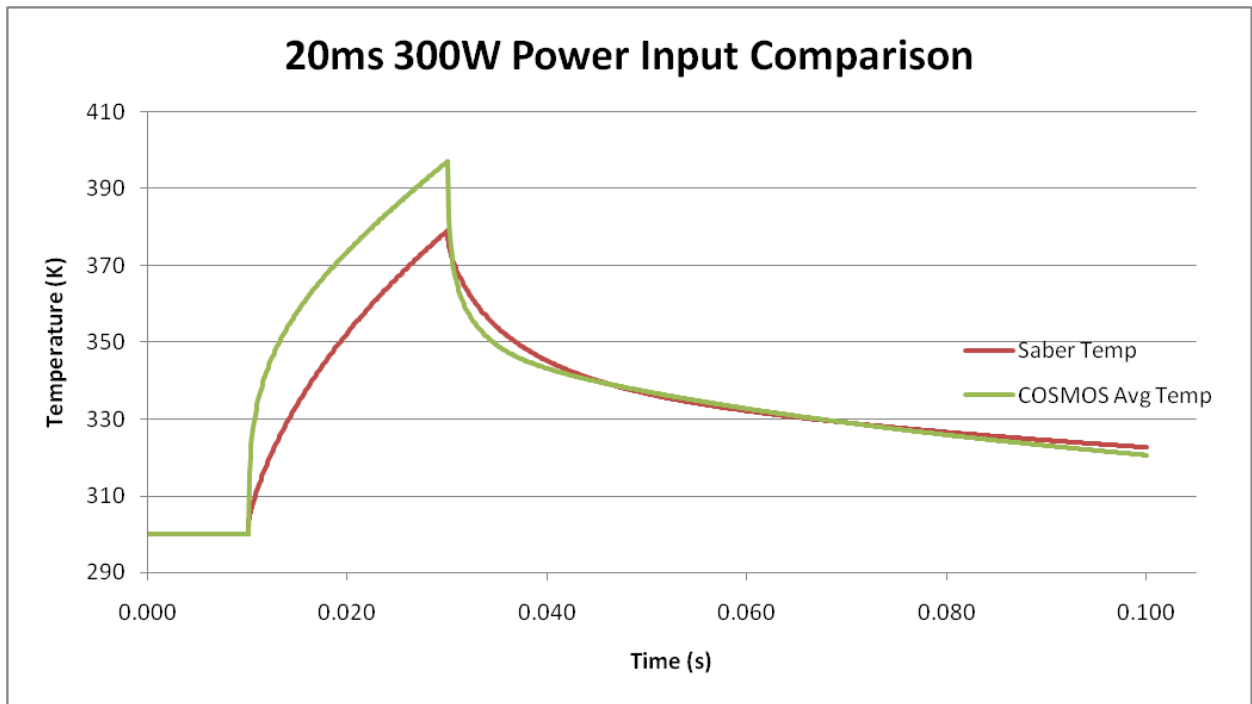
Figure 5.7 - Saber vs. COSMOS Transient Heating Comparison

5.2.2 COSMOS Thermal Modeling

The single device module has under gone extensive thermal simulations from steady state and transient power inputs, Q. The single device module is a simplified module, the concept for which is primarily one of ease of construction it however has allowed for additional thermal testing as well. The precise module being assembled currently is shown in Fig. 5.8 in the mesh used to simulate the module it has a total volume of 6.396 cm^3 and carries 95964 nodes of calculation. This module is simulated without the lead frame standoffs discussed earlier due to the difficulty in manufacturing thus the single device model should serve as a principal match to the testable module.

The module is seen in Fig. 5.9 with *Q=100W*, the module has double-sided cooling and shows *$T_{j,max}$=48.7°C*, for a temperature rise of *T_{rise}=23.7°C*, this equates to a package resistance of *$R_{\theta JC}$(Double-Sided)=0.237 K/W*. This value should remain independent of input power which it does as the thermal resistance of the double-sided cooling package is steady to *Q=500W*. If single-sided cooling is employed, only one face then is set at a fixed temperature and in the

Figure 5.8 – Meshed View of Single Device Module Design
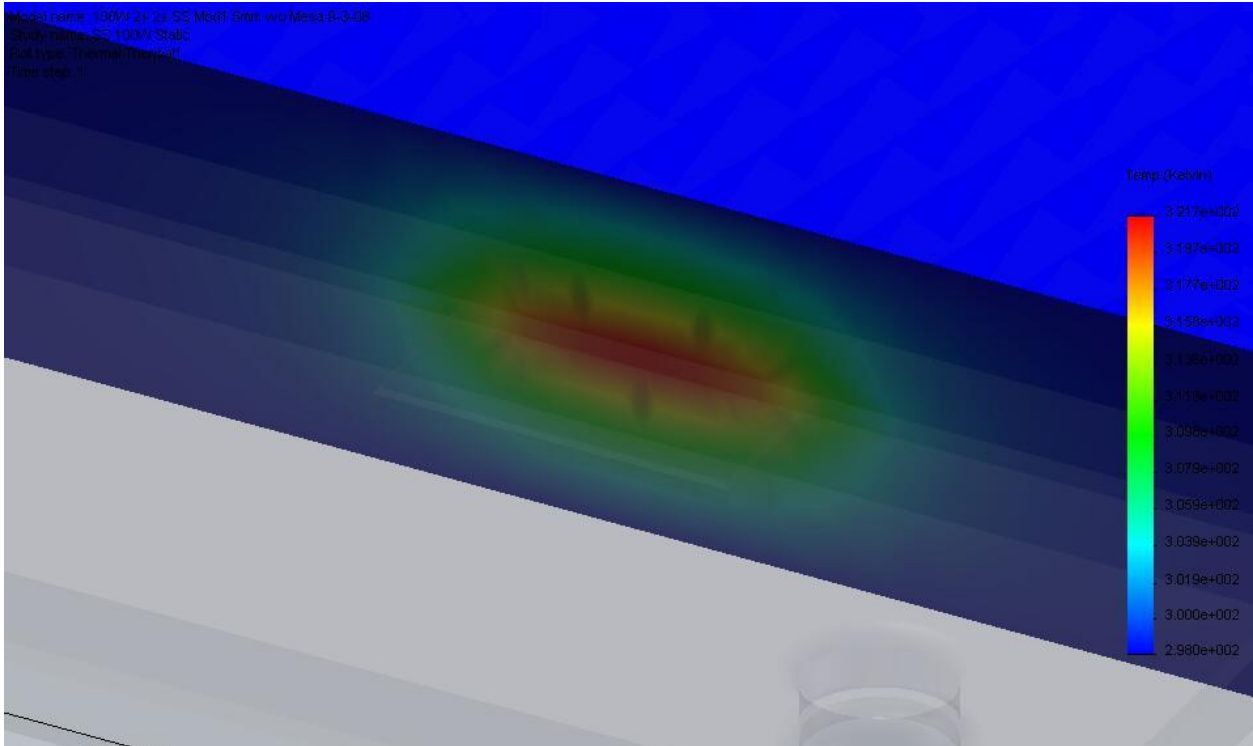
Figure 5.9 – Heating of Single Device Module, 100W Loss, Double-Sided Cooling

simulation the other faces are thermally isolated – although in an experiment they would be subject to unavoidable convective cooling, this however is negligible for comparison. When the single-sided cooling module is subject to the same power input the thermal resistance goes up as expected but only slightly to $R_{\theta JC}(S\text{-}S)=0.301$ K/W this is surprising only a 21.4% thermal resistance increase over the use of double-sided cooling, as a result there is only a 21.4% decrease in temperature for a double-sided cooled module. This equates to a double-sided cooled single device package being able to dissipate 30.5% more power from a device than the single-sided cooling. The single sided device package may dissipate 1.48 kW of power loss before reaching a junction temperature of 300°C; the double-sided may dissipate 1.93 kW before reaching the same temperature.

The heat flux within the package can help explain why there is only a 21.4% decrease in thermal resistance for double the cooling area. Figures 5.11 & 12 show the heat flux vector fields
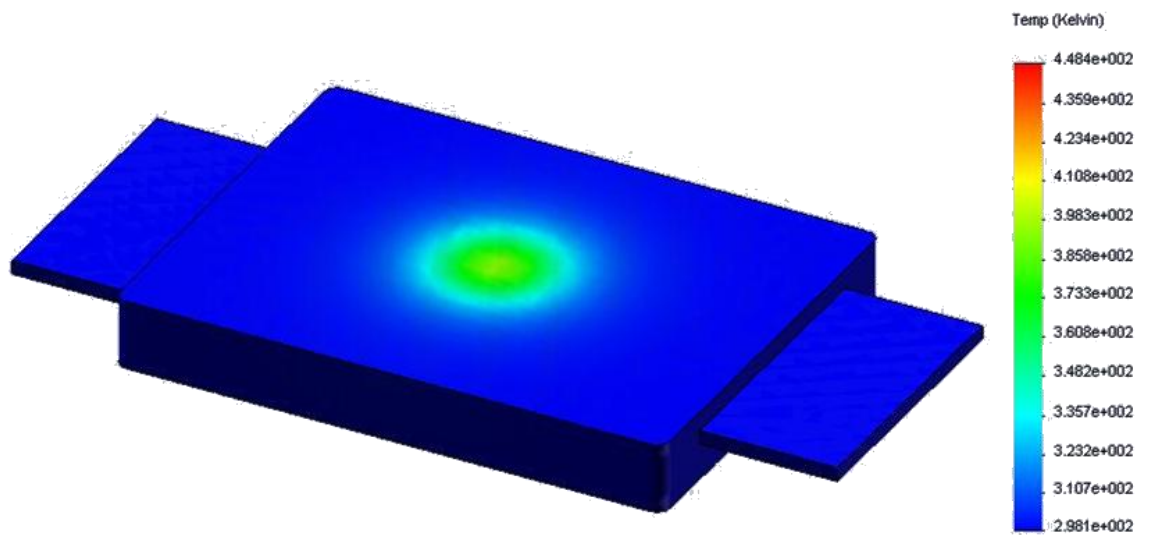
Figure 5.10 – Heating of Single Device Module, 100W Loss, Single-Sided Cooling

of the double and single-sided packages respectively. It can be seen in the double-sided package

the heat flows from the device to the heat dissipating sides nearly entirely in the $\pm z$ directions, in

the fringe areas of the device the magnitude of the heat flux is very low compared to in the single

sided module with only 6.42E5 W/m². In the single sided module the flux at the same point 5mm

from the chip center along the lead frame is 1.62E6 W/m², this is an 149% increase in heat flux,

it is also seen in the figure that there is a focused direction of the heat flux, that is moving heat

from the top side of the package towards the heat absorbing low side where it can be dissipated.

This heat flux is no doubt aided by the use of the high thermal conductivity lead frames other

than wirebonds or thin copper layers on DBC.

If the single device module is simulated with standoffs of 0.5 mm as the full module has

at $Q=100W$ there is a temperature rise of $T_{rise}=44.9°C$, thus a thermal resistance of $R_{\theta JC}(S-S)=0.449$ K/W for single-sided cooling. For double-sided cooling there is a rise of $T_{rise}=36.1°C$,

thus $R_{\theta JC}(D-S)=0.361$ K/W.
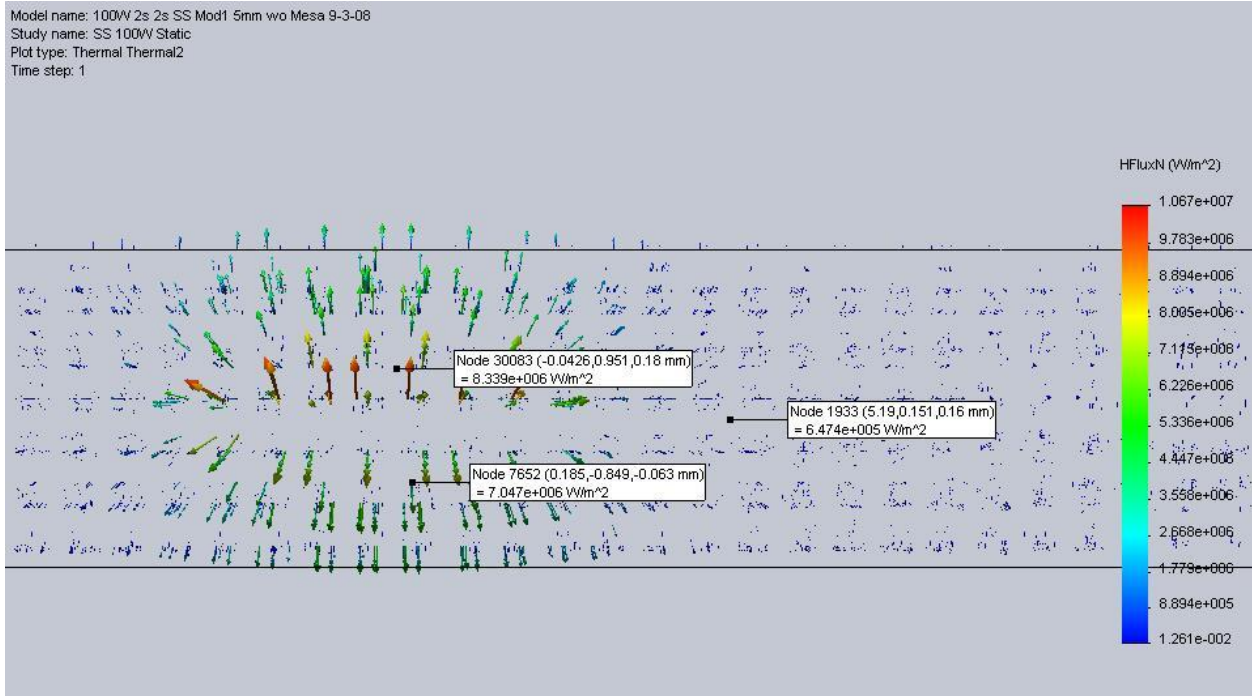
Figure 5.11 – Heat Flux within Single Device Module with Double-Sided Cooling
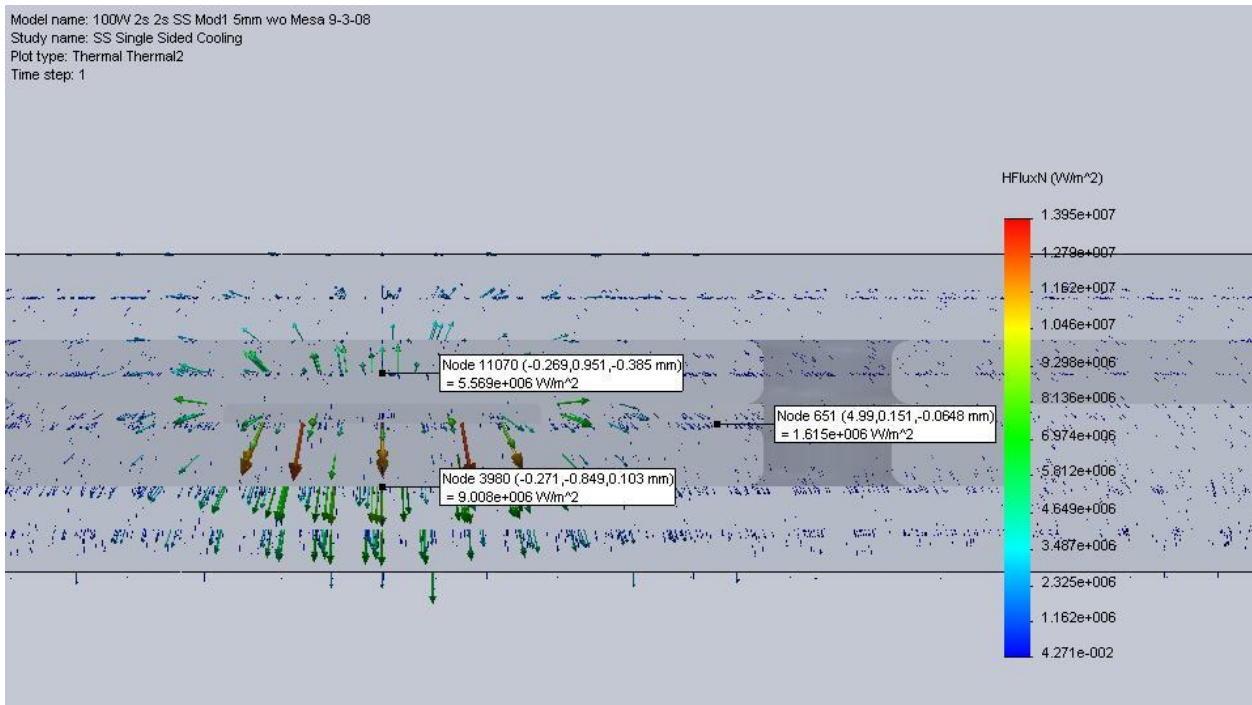
Figure 5.12 – Heat Flux within Single Device Module with Single-Sided Cooling
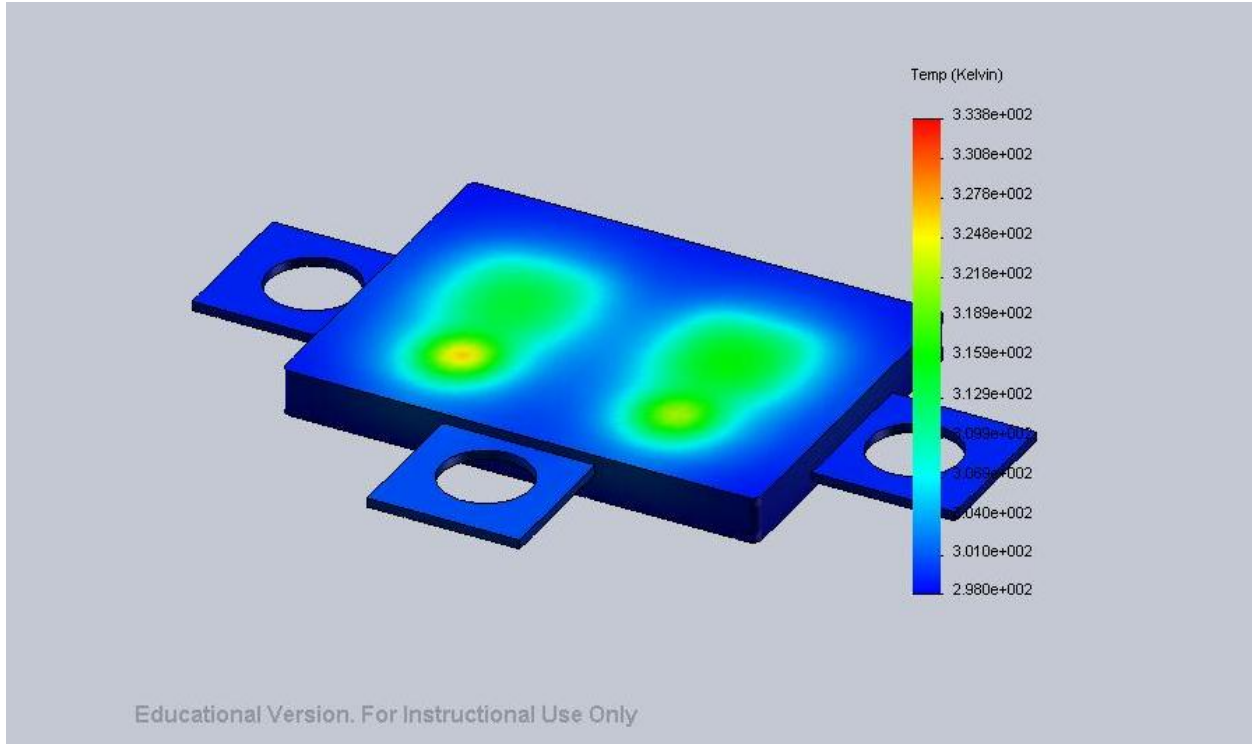
Figure 5.13 – Heating of Full Module, 1 kW Loss, Single-Sided Cooling

The half bridge or final module design can be seen simulated in Fig. 5.13 with single sided cooling and the re-inclusion of the 0.5 mm standoffs from the lead frames to the devices for electrical connections with edge termination consideration. The module has power inputs $Q_Q = 100W$ and $Q_d = 0.694Q_Q = 69.44W$ for the transistor and diode powers respectively. The power loss factor of 0.694 for the diode relative to the transistor is based on a calculation of the switching and conduction power loss of the half bridge circuit switching at $f = 10kHz$, where

$$P_{Q,cond,loss} = \overline{I_Q}V_Q + |I_Q|^2_{rms}r_{DS,on} \tag{5.5}$$

$$P_{Q,sw,loss} = \frac{fI_{max}V_{max}}{\pi} \tag{5.6}$$

where $r_{DS,on} = 4.55 \ m\Omega$ in the 1.6 kV SiC MOSFET (29) (73). For the Si IGBT device the diode factor drops to 0.175 due to the greater losses in the IGBT than the SiC MOS.

For $Q_Q=100W$, with single sided cooling $T_{j,max}=60.8°C$, thus $T_{rise}=35.8°C$, in the diode and $T_{j,max}=61.5°C$ in the transistor. For a similar power input with double-sided cooling $T_{rise}=26.0°C$ these values equate to thermal resistances of $R_{\vartheta JC}(S-S) = 0.358\ K/W$ and $R_{\vartheta JC}(D-S) = 0.26\ K/W$. However as stated when the peak power of 100W is entering the transistor only 69.44W is entering the diode at the same time; this equates to thermal resistances of $R_{\vartheta JC}(S-S) = 0.516\ K/W$ and $R_{\vartheta JC}(D-S) = 0.374\ K/W$. If the thermal resistance is taken in this fashion there is a 13.0% increase in the single sided thermal resistance and only a 3.5% increase in the double-sided resistance. It is expected to increase in this transition from single device to full module, the double-sided module does not gain much resistance because although there are now 4 devices within the module creating power loss as seen with the short heat flux path the power loss of the additional devices does little to impede the power flow. In the single-sided device where the heat exiting the top side of the devices must traverse the
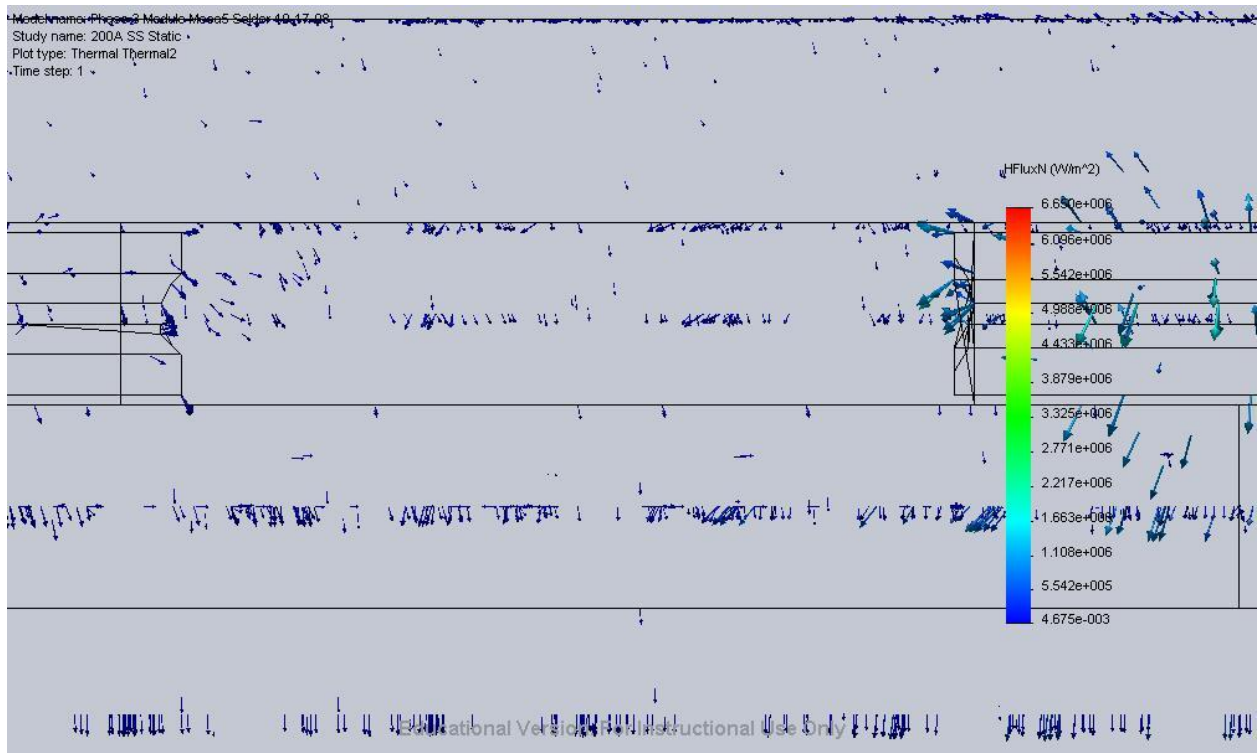
Figure 5.14 – Heat Flux of Full Module, 1 kW Loss, Single-Sided Cooling

module to reach the lower plate the heat flux paths will impede each other. It is seen in Fig. 5.14 between two devices that the resultant heat flux is directed primarily in the $-z$ direction, towards the cooling plate because the fluxes away from the device laterally cancel.

5.3   Mechanical Modeling and Discussion

The mechanical stresses on the package can come from three origins to create the internal forces. The package may be externally compressed or pulled by the external leads or on the SiC encapsulant, this may happen unintentionally altogether similar to a short circuit test where the package is dropped or it may happen when the package is mounted and the mounting apparatus inflicts stress on the package. The other two stresses that are most critical in electronic packaging are related to the heating of the device and packaging, the stress coming from the thermal expansion of the device materials related to their CTEs. If two materials bonded to each other have different thermal coefficients then they will induce stress on each other, the larger the coefficient difference the more stress, or the more heating the larger the stress. This heating is induced by one or both of two means; it may be the device heating that is caused by the power loss of the devices. This is the heating that causes current ratings on devices and the need to know the package thermal resistance. The heating may also come from the ambient, even if the device heating is low due to efficient devices or low power usage, the stresses are the same for a given temperature at an interface. The stresses of the chip heating, as will be shown, are centered primarily on the devices. When the entire package is heated uniformly the stresses are more evenly distributed although it will be shown the peak stresses are similar.
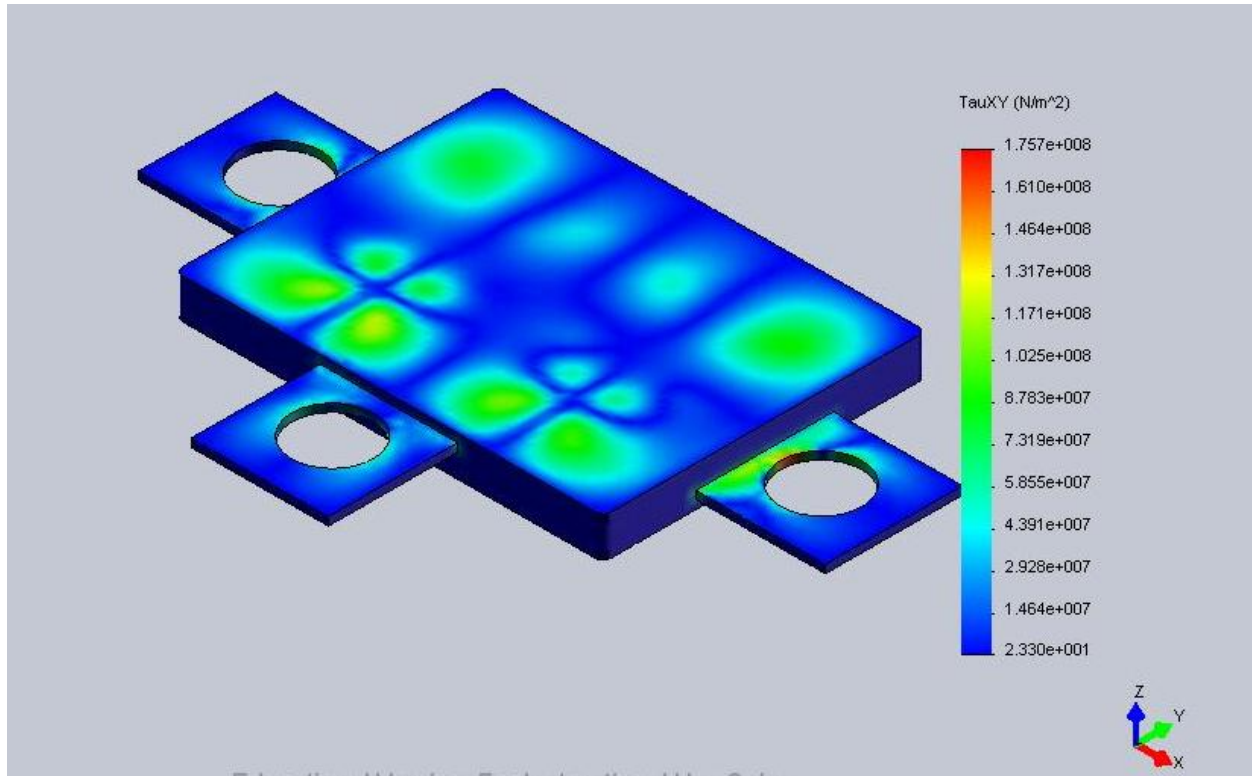
Figure 5.15 – Shear Stresses within Full Module with 300°C Devices

To verify the stresses on the package will not lead to its failure due to chip heating power loss is applied to the package. For the single-sided cooling arrangement the thermal resistance for the peak power input is $R_{\vartheta JC}(S-S) = 0.358\ K/W$ thus to obtain $T_{j,max} = 300°C$ from a 25.0°C baseplate $Q_Q = 768W$ thus $Q_d = 533.3W$ is needed. Figure 5.15 shows the module's shear stresses that will predict if the shear stresses will overcome the ultimate shear strength of the solder which is 183 MPa for the AuGe12 solder. For all mechanical stress simulations the zero stress benchmark has been set at 25°C, any heating above this will cause stresses in the package. It is seen that the maximum shear forces present in the module when affixed at the three terminal to a rigid body is 175 MPa therefore it can be concluded that the module can handle the CTE stresses of $T_{j,max}$=300°C operation. The module is actually more secure than that since the highest shear stress acting on a solder piece is 61.9 MPa and 114 MPa on a device which can be

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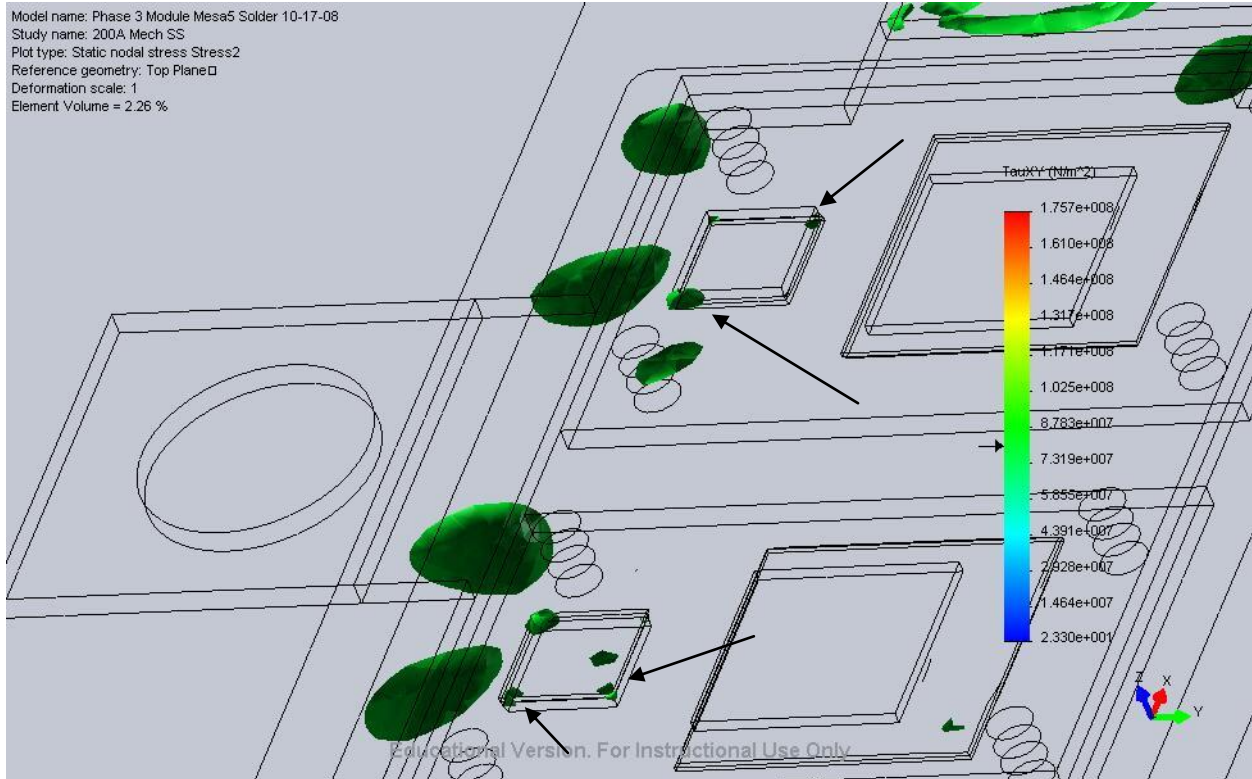
Figure 5.16 – Isolated Shear Stresses >100 MPa within Full Module

seen in the stress isolation image of Fig. 5.16 where only stresses above 100 MPa can be seen. It is visible that the greatest stresses of interest are formed at the corners within the chip in agreement with traditional packaging stress distribution (74). For the double-sided cooling setup $Q_Q = 1058W$ for $T_{j,max} = 300°C$, here the peak stresses are also below 185 MPa at $\tau_{xy,shear} = 146.3\ MPa$ and again the stress is similar the single-sided with peak shear stress on solder and SiC devices being 63.03 MPa and 91.7 MPa, respectively. For both the greatest magnitude of stress is placed on the mounting holes where it is assumed to be fixed in position.

If the module is uniformly heated to 300°C then the stresses will be placed differently than due to chip heating, the greatest stresses occur still on the mounting holes only with much greater magnitude, $\tau_{xy,shear} = 1.03\ GPa$, this can be seen in Fig. 5.17. The stresses for the single and double-sided cooling modules are nearly equal with stresses of 114.9 MPa on the

solder and 184.9 on the devices. If the restraint scenario is altered to allow the high side and low side lead frames to be attached in a manner that does not rigidly restrain the module so as to compress the frame in heating the forces drop drastically to similar to that of only chip heating as seen previous. In this scenario the peak shear stresses on the solder and devices are 69.9 MPa and 62.0 MPa respectively for the single-sided module and the double-sided cooled module again.
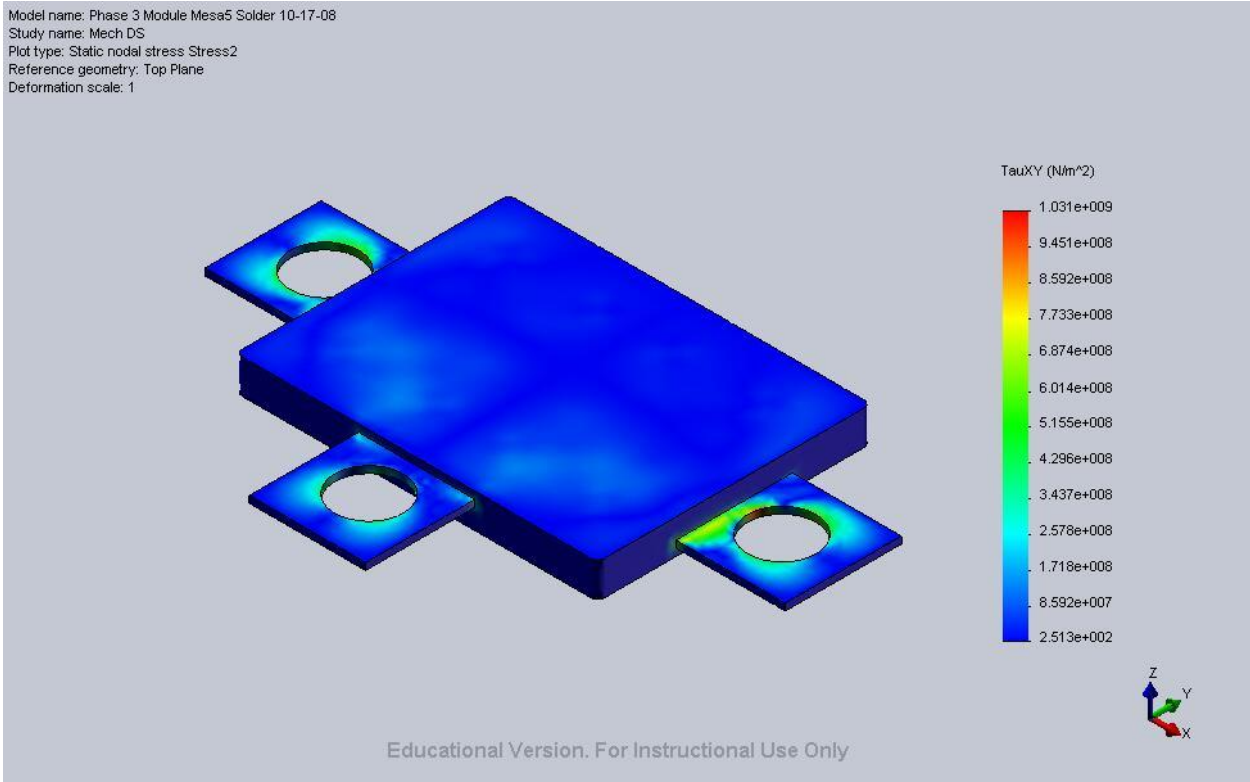
Figure 5.17 - Shear Stresses within Full Module with 300°C Ambient Temperature

CHAPTER 6   EXPERIMENTAL WORK AND RESULTS

6.1   Module Construction Process

Currently constructed and tested is the simplified single device module, receiving data and feedback for continued construction of modules. The single device module has been designed, simulated, constructed, and tested for a variety of reasons, rather than first attempting construction on the full module design when a great deal of information can be derived from the single device module. The primary reason for the intermediate prototyping step is the extreme cost of SiC devices specifically the non-commercially available transistors, obtaining a necessary amount to complete a fully functional package designing and constructing only a full module would require several devices, each failure of a package would lie to rest four devices, including two of the elusive SiC MOSFETs. The boldness of the module design makes for an arduous path to commercialization although the benefits are substantial over the current options. Also even with low cost devices available, there are great difficulties in the construction of the full module that are unnecessary obstructions to significant initial data that can be had from the single device module. Due to the great temperature dependence of diodes the temperature $T_{j,max}$ can easily be measured along with the power loss of the device. Thus all important parameters can be extracted with great certainty from the single device module containing a Schottky diode.

6.1.1   Material Research

The module has been constructed primarily in the Power Semiconductor Research Lab with the assistance of the Advanced Materials Processing and Analysis Center (AMPAC) clean room and processing labs at the University of Central Florida in Orlando, Florida. This is where

most of the characterization has occurred also; some characterization has also occurred at NIST in Gaithersburg, Maryland and will continue to be done there in the future.

The first step of module construction was the allocation of materials that had qualities matching the design goals of the project, primarily low CTE and high thermal conductivity. The material properties of potential materials along with suppliers of the material are captured in Tables 4.1-4. Although for some materials there are several good candidates decision were made on which to purchase based on manufacturability and cost. As mentioned the primary modules have in them MoCu15 lead frames from Plansee Corporation with a gold coating for solder wetting and adhesion. The adhesive layer surrounding the devices is the Cermabond 865 with AlN filler from Aremco, the encapsulant is the Cermacast 673N with SiC filler which is also from Aremco. And the devices are crystalline SiC which have been acquired from SemiSouth Laboratories and Cree. Also a purchase of pure molybdenum from Eagle Alloys for alternative lead frames has been made along with Cermacast 575 which has an alumina (Al_2O_3) base and Cermacast 646N with a zirconium (ZrO_2) base for the encapsulant all ceramic, both from Aremco. From Cotronics, which serves a very similar product line to Aremco, is the Durapot 863 which is a polymer with an opaque visual consistency. For the die attach material Aremco's PyroDuct 597A was also ordered which is a silver based epoxy with a high heat resistance. The devices came in three forms, the PSRL received 30 2x2mm and 8 5x5mm prototype devices from SemiSouth Laboratories which have been used in all modules, also the PSRL received ten sample 2.5x2.5mm JBS diodes and 5 fully certified working JBS diodes. All of these materials have been ordered to inspect their manufacturability and to build a multitude of single device modules for comparisons of materials although the leading module material candidates are known due to their known properties.

6.1.2   Soldering Mount and Encapsulant Mold Construction

As the module materials were incoming it was necessary to facilitate the manufacture of the modules. Two necessary tools had to be customized for the module they included a soldering mounting apparatus and an encapsulant mold seen in Fig. 6.1, both of which were second renditions of their designs. The soldering module is used to align the top and bottom lead frame pieces using the alignment holes seen in Fig. 5.2. The standoff seen is to offset and raise the top lead frame so that it will be planar with the solder layer atop the diode when it is place on the solder-diode-solder-bottom lead frame stack. It has a displacement of 1.25 mm to account for this stack height, when the five layers are placed on it as seen in Fig. 6.2 it has a 3 gram weight placed on it to apply brazing pressure when the solder wets. For modules utilizing the PyroDuct, silver epoxy, for solder the mount is also used as it still works effectively in aligning the lead frames. The hole at the end of the mount along with the bottom contours on either side are in place for usage inside of a tube furnace where the AuGe12 solder was reflowed. The first version
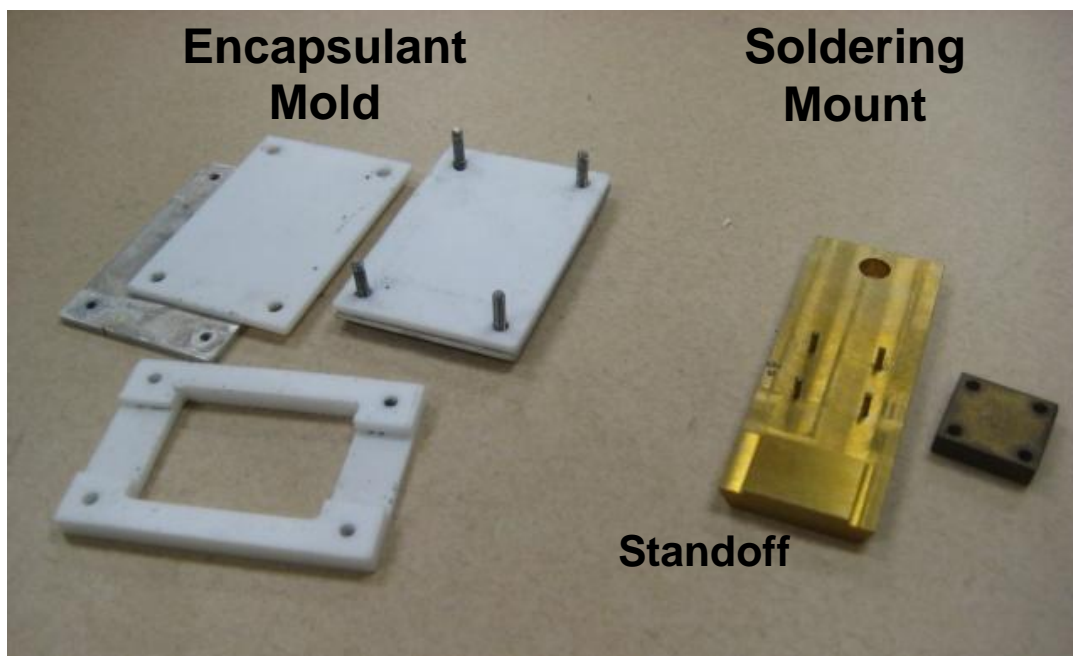
Figure 6.1 - Phase One Module Encapsulation Mold and Soldering Mount
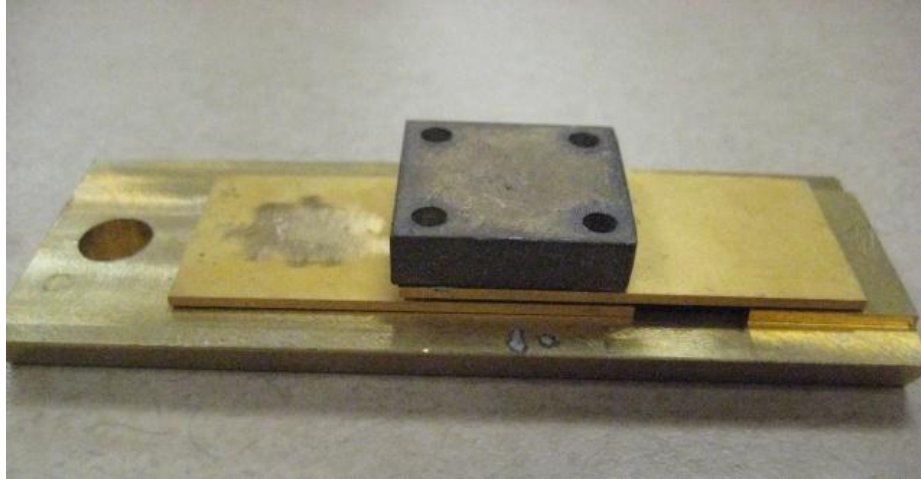
Figure 6.2 - Soldering Mount with Lead Frames and Weight

of the mount did not have a standoff, making it very impractical when the space was confined to

the inside of a tube. Both the first and second mounts are made of brass. The mold is used for the

encapsulation of the device. It is made of Teflon and also consists of a top and bottom flat piece

along with two near identical aluminum pieces to make a five layer mold stack. The aluminum

pieces have screw holes to tighten the mold together with the use of four screws. The original

mold design was purely aluminum giving it two large drawbacks; encapsulant materials had the

ability to easily adhere to it even with a generous amount of silicon spray pre-treated to it, also

its rigid material put pressure on the module in its intermediate stages before the use of the

strengthening encapsulant. If the lead frame modules were not exactly aligned during soldering

then they would be broken or useless in trying to put them in the aluminum mold, the Teflon

allows for greater flexibility which also makes for a more enclosed design when tightened.

6.1.3   Module Die Attach Process

The soldering process has been one of the most trying procedures of the project. The first

soldering began initially with the use of pure molybdenum lead frames and the silver epoxy as a

visual conception creation, this however proved to be very difficult as molybdenum wets very little to solders (66). However a solder joint was formed by abrading the molybdenum with a grinding tool to increase adhesion.

Upon the reception of the MoCu15 frames and diodes the 2 and 5 mm diodes were used to create functioning modules using silver epoxy as the solder. AuGe12 solder was used extensively in attempts to solder the devices together however great difficulty was encountered in both dealing with oxidation of the gold at high temperatures and finding literature on the rare solder. Wetting tests in a tube furnace in an argon environment after a short buffered 25% hydro-fluoric etch to remove the native oxides of the lead frames, solder, and diodes which also have Au contacts eventually produced desirable results in wetting, although a module has not yet been produced with the AuGe12 material. The liquidous and solidus melting point of the AuGe12 is 356°C thus it is suggested to ramp the soldering temperature to 400-430°C.

During the soldering process difficulties in encapsulating the temporarily joined modules due to soldering breaking along with speculation in the presence of trapped air bubbles due to the low viscosity of the SiC encapsulant led to the use of the adhesive which could be added simultaneously during the soldering using the silver epoxy which would provide a strong layer between the frames in parallel with the device. This worked effectively in providing a strong module even before encapsulation in the SiC ceramic. The AlN along with the PyroDuct required a two hour room temperature setting period and then a 93°C two hour heating period to cure, it was also suggested that additional heating would improve resistance qualities for both.

6.1.4   Module Encapsulation Process

The encapsulation procedure went relatively smoothly throughout, once a module was ready to be encapsulated. The joined frames were placed in the mold with the lower planar mold piece set and a portion of encapsulant in the mold. Additional encapsulant was then poured over the frames until the mold was full. Additional Teflon pieces were then placed so as to no leave voids to allow the liquid encapsulant to drain out. The remaining mold pieces were then placed and the screws tightened to secure the module and the mold was vibrated to increase the viscosity of the encapsulant and to remove air from the lead frames and device. The mold was then placed in a vacuum chamber and the air pressure was quickly cycled to remove air bubbles from the module. The ceramic encapsulants were left to dry for 24 hours exceeding the 8 hour minimum drying time before a 2 hour minimum 93°C bake in air. The Durapot epoxy had a similar bake at 121.1°C after a 2 hour setting period. The ceramics including the adhesives became very rigid during the bake and changed very little visually. The epoxy changed very little during the setting until its bake where its viscosity dropped before beginning to harden into a rigid encapsulant. The encapsulants were tested to observe their performance at high temperature and to ensure that the binders had been burned out of the ceramic modules. Figures 6.3 and 4 show the finished modules of the SiC and the Durapot encapsulants. The SiC showed no signs of temperature degradation initially however as can be seen in Fig. 6.4 that CTE problems of the Durapot quickly foiled it as it went from a smooth opaque color to black with large thermal cracking, it was not further considered for module construction due to the problems encountered at 300°C. The alumina encapsulant appearing white in color reacted similarly to the SiC however the zirconium based material remained to be extremely brittle after baking.
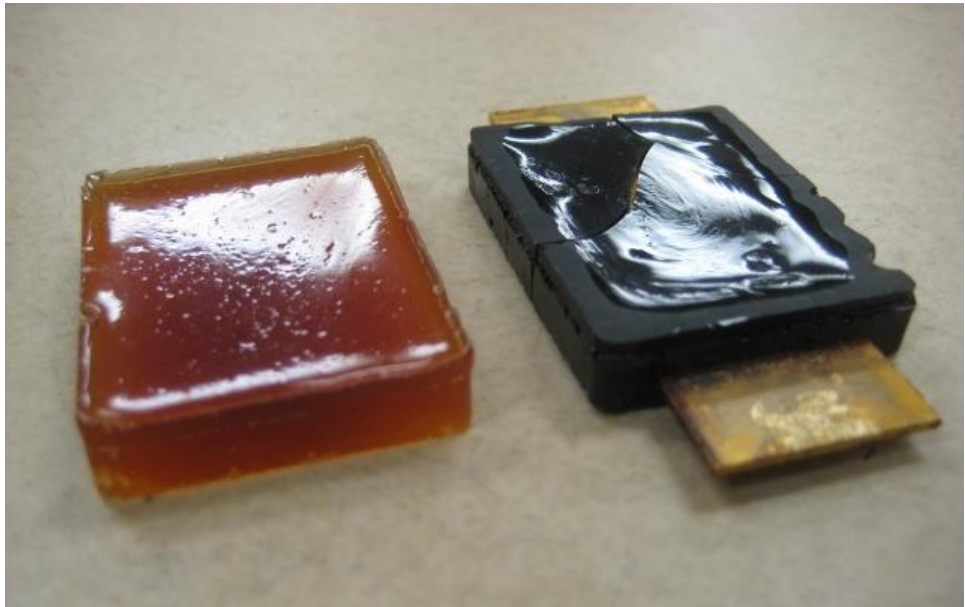
Figure 6.3 - Module A-4 with SiC Based Encapsulant

Figure 6.4 - Module 1 with Durapot Epoxy Encapsulant, Post 300°C Stress

6.2   Experimental Results and Discussion

6.2.1   Module Resistance

The resistance of the modules is taken by comparing the packaged electrical data and comparing it to the device electrical characteristics the die packaged. Modules are labeled by the device they have enclosed within them, thus module A-1 has enclosed 5 mm SemiSouth Diode A-1. Unfortunately due to the lack of reliable diodes at the time of manufacture it can be seen in Fig. 6.6 Module A-4 has a greater V_T before packaging, the primary manufacturing process that can be attributed to this is the 2 hour 93°C bake which certainly should not affect the use of any device. Module A-10 shows comparatively a much greater reliability in Fig. 6.7 although there is still a shift in the I-V curve. It is very peculiar that in both modules there is an encouraging shift in the diode performance as there should be an increase in package resistance however there is virtual negative resistance which is impossible in both cases.

6.2.2   High Temperature Module Operation Verification

To ensure that the modules correctly operate as expected at high temperatures the modules were characterized at the goal temperature of 300°C. It is possible for modules to withstand high temperatures without operating at the elevated temperatures to later operate again at lower temperatures because as materials expand from they may temporarily induce an open circuit but still allow for the device to be connected again by contact as the material contract because the devices themselves have one of the lowest CTEs (SiC, 3.8 ppm/K). The single device module however does not suffer from such negative effects as both modules tested, A-4 and A-10, fully operate as projected up to 300°C (Fig 6.5). Confirmation of the high temperature operation is a major proof of concept for additional project work continuing on. The modules are
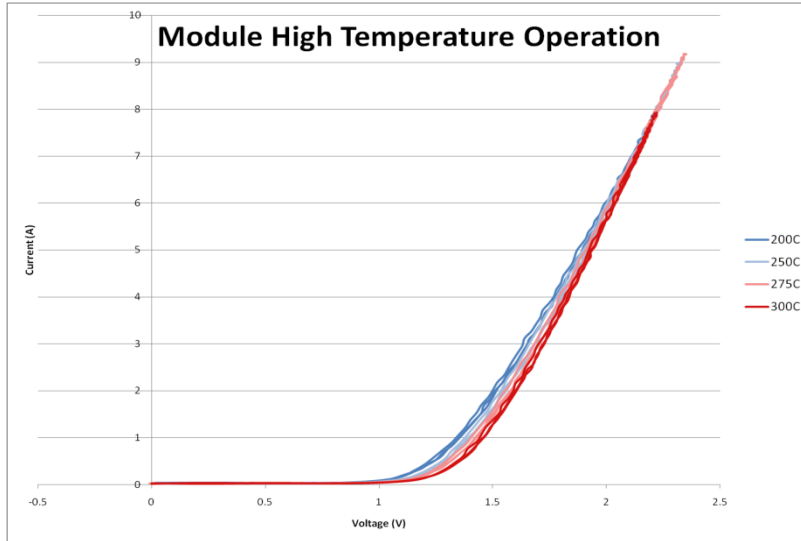
Figure 6.5 – Module A-10, High Temperature Operation Verification Graph

also tested for reliance to high temperatures, Section 6.2.4, High Temperature Reliability, and also pass.

6.2.3   Device Temperature Calibration

In order to decipher the thermal resistance of the single device module a temperature-current-voltage relationship must be established. This relationship is defined simply in the forward voltage (V_F) equation of a Schottky rectifier

$$V_F = \frac{kT}{q} ln \left(\frac{J_F}{J_S}\right) + \left(R_{drift} + R_{subs}\right)J_F \qquad (6.1)$$

However, this relationship can also be defined by a calibration of the diode as can be done of any temperature sensitive device property (70). The calibration method is not only possible but necessary for the PSRL module calibration at this time due to the lack of knowledge about the specific devices packaged and the demonstrated inconsistencies it would be better to not rely on a theoretical value. As can be seen in the equation the forward voltage will increase depending on the junction temperature regardless of how this heating comes about, therefore what has been

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done is the module was heated to 300°C and the voltage was pulsed so as not to induce conductive heating and the IV curve was extracted. The results of the temperature calibration of module A-10 can be seen in Fig. 6.8, with similar results for module A-4. These results are troubling however as the result should look far more similar to that of Fig. 6.9 in which a JBS diode is characterized and simulated over temperature variation (75). As can be seen, the diodes in use which are supposed to be Schottky diodes have an extreme temperature resistance which point to P-*i*-N diode behavior. This lends to the conclusion that the metallization did not induce a Schottky contact and all that was left of the JBS diode which is a merge of a Schottky and p-n diode was the p-n barrier. This unfortunate setback shall delay the determination of the thermal resistance of the single device module until new prototypes can be built.

The 5mm SemiSouth A-10 diode demonstrates a temperature dependence of $\frac{\Delta V}{\Delta T}\Big|_{I=10A}(5mm) = -0.352\ \frac{mV}{K}$ while a properly functioning JBS diode for NIST exhibits a temperature dependence of $\frac{\Delta V}{\Delta T}\Big|_{I=10A}(NIST) = 90.7\ \frac{mV}{K}$ derived from the IV temperature curves. The proper diode temperature dependence allows for the calculation of the thermal resistance by use of a baseplate, as the base temperature, diode current, and voltage may all be measure *in situ* while power is being introduced into the diode. While the current is fixed the V_F may be measured to derive the corresponding temperature from the $\frac{\Delta V}{\Delta T}$ relationship. For a fixed power loss in the module the temperature will reach a steady state determined by the thermal resistance of the module. With the use of an oscilloscope this may also be done transiently (70).
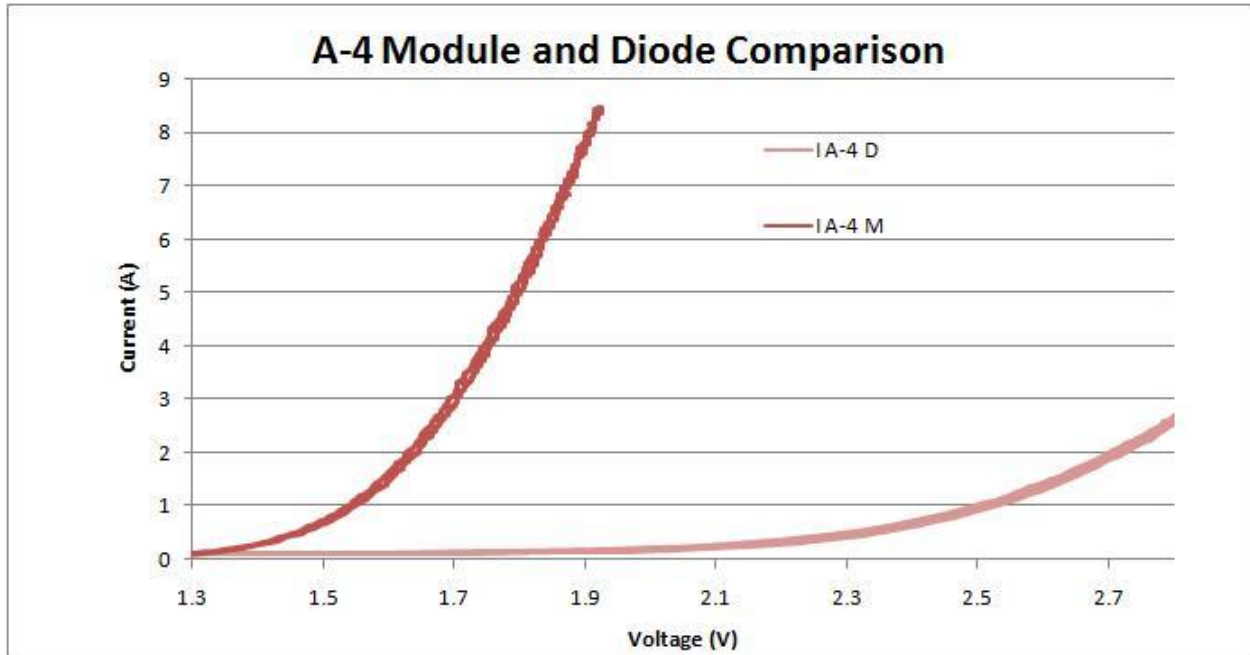
Figure 6.6 - Module A-4 Device and Module Comparison
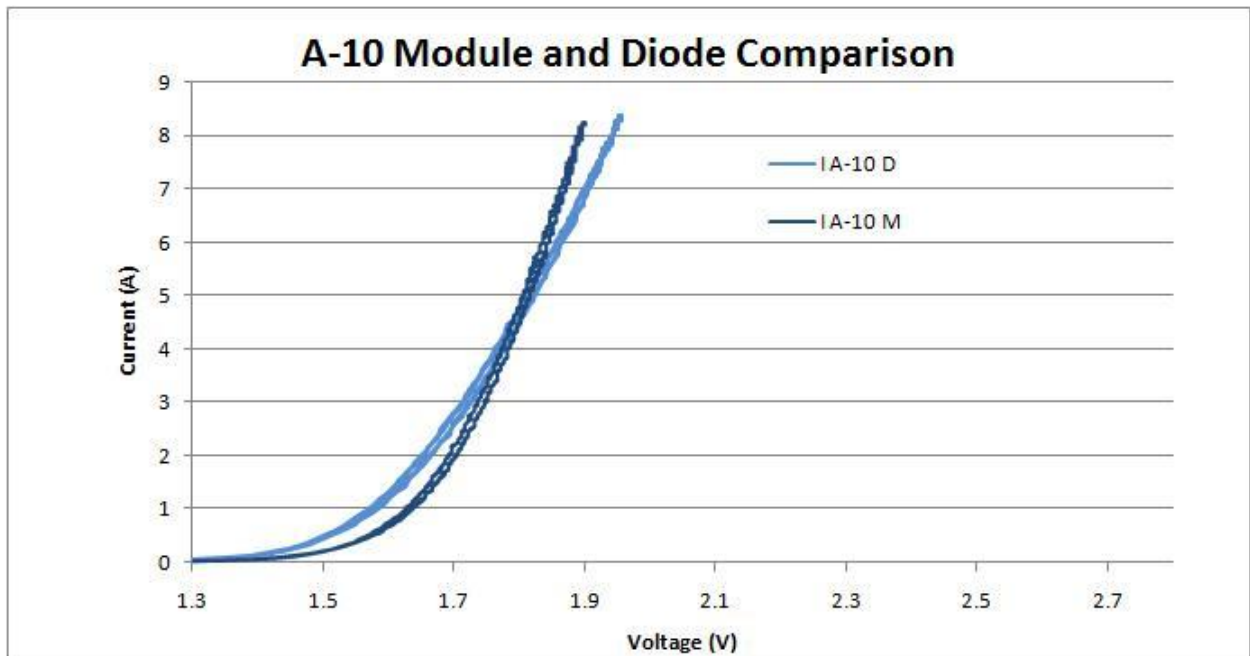
Figure 6.7 - Module A-10 Device and Module Comparison
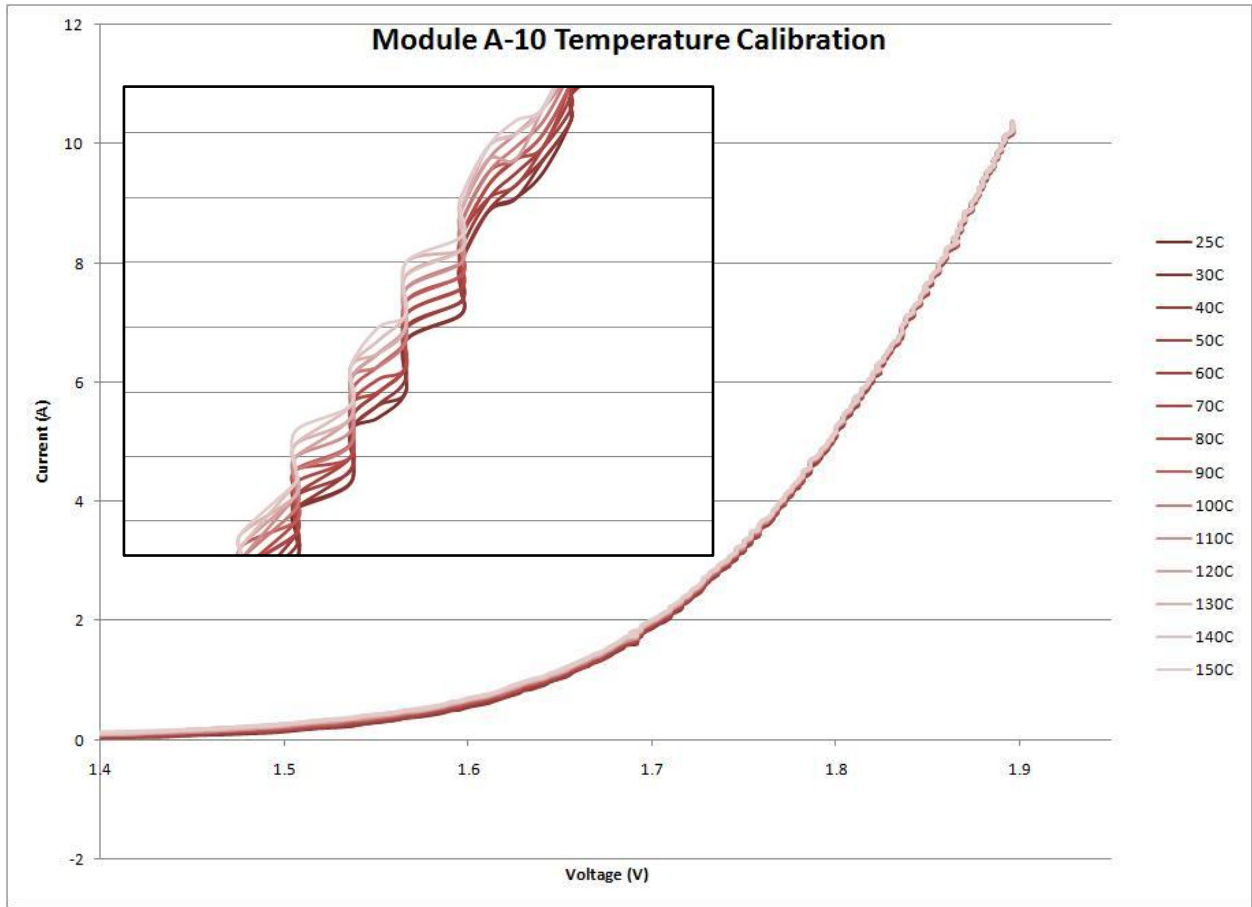
Figure 6.8 - Module A-10 Temperature Resilient Calibration Testing
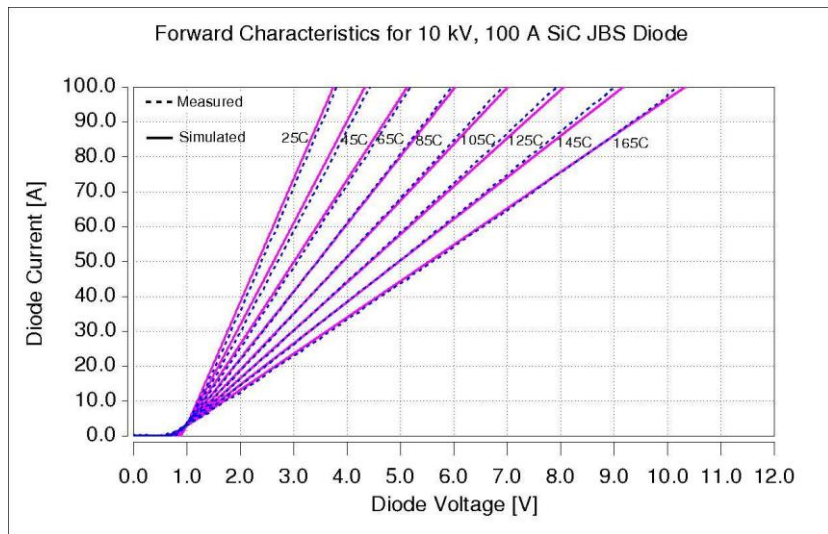
Figure 6.9 - Correct JBS Diode Temperature Dependence [70]

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6.2.4   High Temperature Reliability

The single device module was subjected to reliability testing to ensure the packaging continued operation while experiencing prolonged elevated temperatures. A module (A-10) was baked at 250°C for 100 hours and verified that the continued stress from the elevated temperatures did not induce failure. The IV curves of the module can be seen in Fig. 6.10 after verification of operation after 0, 50, and 100 hours of thermal-mechanical stress. The module is seen to withstand the stress very well with little degradation and no failure. The module may either degrade due to increased resistance in the solder or the lead frames or it may fail due to shear stresses breaking the solder, neither of which happened to the module, it performed excellently.
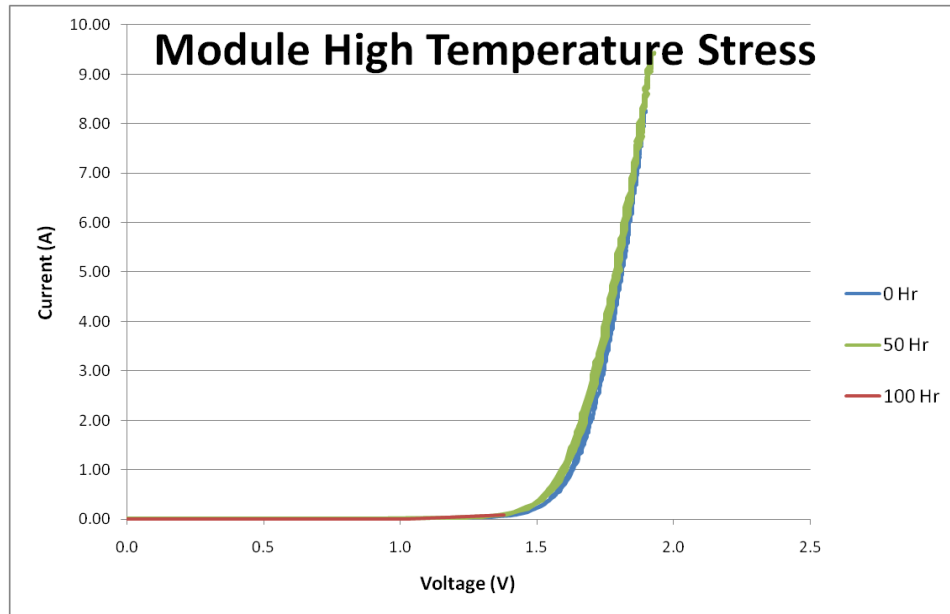
Figure 6.10 – Module A-10 High Temperature Reliability Stress Results

6.2.5   Inductance

The inductance of the modules has been tested with and without devices with the results compared to the traditional module design. The inductance of traditional power modules is problematic due to the minor loss of switching speed but also the induced current crowding in the devices on the extremities of the module causing burn-out (27). By simulation this inductance is shown to be $L_{module} = 40 - 55nH$, a portion of which is contributed by the bond wires and the terminal connections of the module, the total module inductance is broken into $L_{bond\ wire} = 10 - 15nH$ and $L_{terminal} = 30 - 40nH$ at $f = 20kHz$, which is an approximate maximum switching frequency of traditional modules. The inductance of a traditional power module, as seen previously in Fig. 2.1, can be compared by measuring the inductance over one of the anti-parallel diodes from the low side voltage DC terminal to the output node of the half bridge circuit without biasing the IGBT, this will apply current solely over one diode along with its terminal connections and bond wires. This inductance is equivalent to the inductance of the single device module; all inductances may also are taken at *f=20 kHz* to compare with simulated values.

Table 6.1 – Inductance Testing Results Comparison

	Traditional Module (Modeling)	Traditional Module (Measured)	PSRL Module, No Device (Measured)	PSRL Module (Measured)
Parasitic Inductance	40-55nH	45nH	1.1nH	3.2nH

The inductances were measured with an Agilent LCR meter using an HP current source bias. In order to measure the inductance over a device they must be biased on therefore the modules were biased using a current of *I=5 A*. By measurement of the modules it is shown that

the simulation is correct as seen in Table 6.1. The traditional power module measures to be *L=45nH* at 20 kHz, however as predicted the PSRL design module lowers this parasitic inductance by an average of 92.8% to an average of *L=3.2nH*, where module A-4 recorded an inductance of 3.4nH and A-10 an inductance of 3.0nH. This is a 10 fold measured reduction in the parasitic inductance of the module. Also measured was a control module of the PSRL packaging that does not contain a device which has an inductance of 1.1nH. This severe inductance reduction is a great accomplishment to the project which boasts this feat as a primary project goal.

CHAPTER 7   FUTURE WORK

There is still much work to be continued on the high temperature packaging projects, it is a variety of designing, modeling and simulating, and construction and characterizing. This work must be continued on the single device module in operation but also work must be advanced to the construction of the final module design.

In the continued design of the module ideas must be fitted to the module to allow for the intelligent connection to the gate nodes on the surface of the SiC MOSFETs as this has not yet been considered is the model. The gate will be low current thus it may be possible to use a ribbon or wirebond to make this connection if the reliability is shown to fit with the rest of the module. In press pack modules where there is also no wirebonds and a large source connection the gate connections are typically made by use of a specified press pin however this connection could not work the new module. Additional research into abstract connection types must continue on.

It is also necessary to add to the simulation results with data to predict and agree with inductance testing that has taken place. It is necessary to improve the design and also investigate potentially different methods of shaping layers to improve their electromagnetic design. Electrical simulations must also be performed in order to better approximate and specify the power loss of the system and potential power output, this can then be used to determined the efficiency, these two simulations can be cascaded for power loss at different operating powers and frequencies.

This power loss calculation can be used to improve the thermal and mechanical stress simulations. Better approximated power loss calculations will lead to more accurate specification of the power generation along with the magnitude in each chip. All of this data for the electrical, thermal, and stress will then be done transiently to extract how the module will operate in

transience which is necessary due to the switching of the devices and the sporadic usage nature of the module as a whole. Parameters such as the transient thermal resistance will then be extracted from the model.

For the current and subsequent single device modules thermal cycling test may be conducted, this can take week and months for robust result of the module's ability to handle the power cycling along with tests to deduce when the module may fail. Power cycling will also be performed where the heating of the module occurs from the devices which induce different stresses that are accurate of most module operation. And without question the most important continuation of the project is the building of the final module design and confirm its correct operation along with the performing all previous testing upon it to fully and correctly characterize it for predictable usage.

APPENDIX A: PSRL POWER MODULE DESIGN

53

40

5   4   3   2   1

83

7.10

19

21

⌀10

30

4.80

⌀2

3

		UNLESS OTHERWISE SPECIFIED:		NAME	DATE	High Side Lead Frame
		DIMENSIONS ARE IN INCHES TOLERANCES: FRACTIONAL ± ANGULAR: MACH ± BEND ± TWO PLACE DECIMAL ± THREE PLACE DECIMAL ±	DRAWN			
			CHECKED			TITLE:
			ENG APPR.			
			MFG APPR.			
		INTERPRET GEOMETRIC TOLERANCING PER:	Q.A.			
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APPLICATION		DO NOT SCALE DRAWING				SCALE: 2:1	WEIGHT:	SHEET 1 OF 1

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Ø10

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9

43

4.80

UNLESS OTHERWISE SPECIFIED:

DIMENSIONS ARE IN INCHES
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Output Lead Frame

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5   4   3   2   1

85

	NAME	DATE
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Q.A.		
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AIN Adhesive

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SIZE	DWG. NO.		REV
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SiC Encapsulant

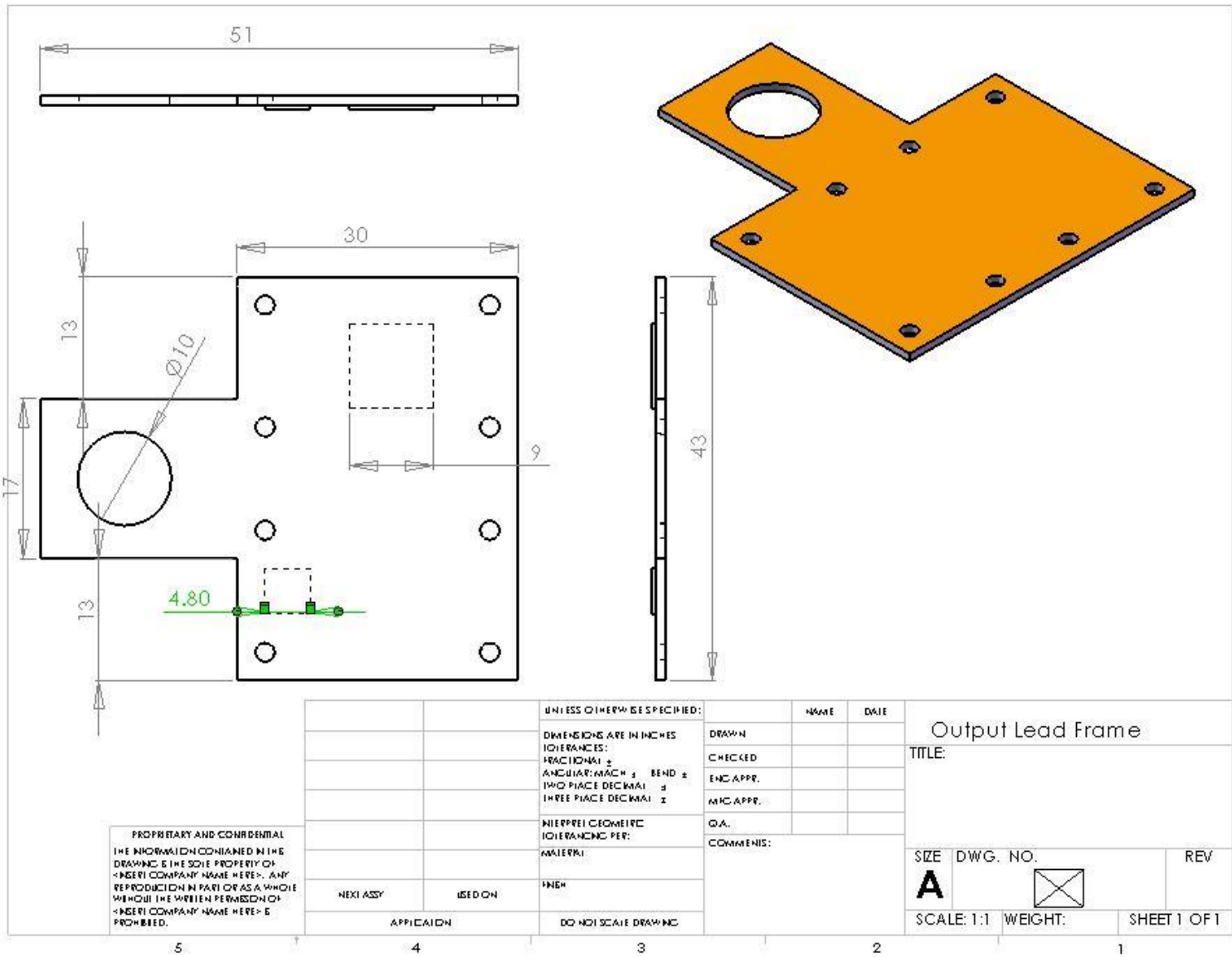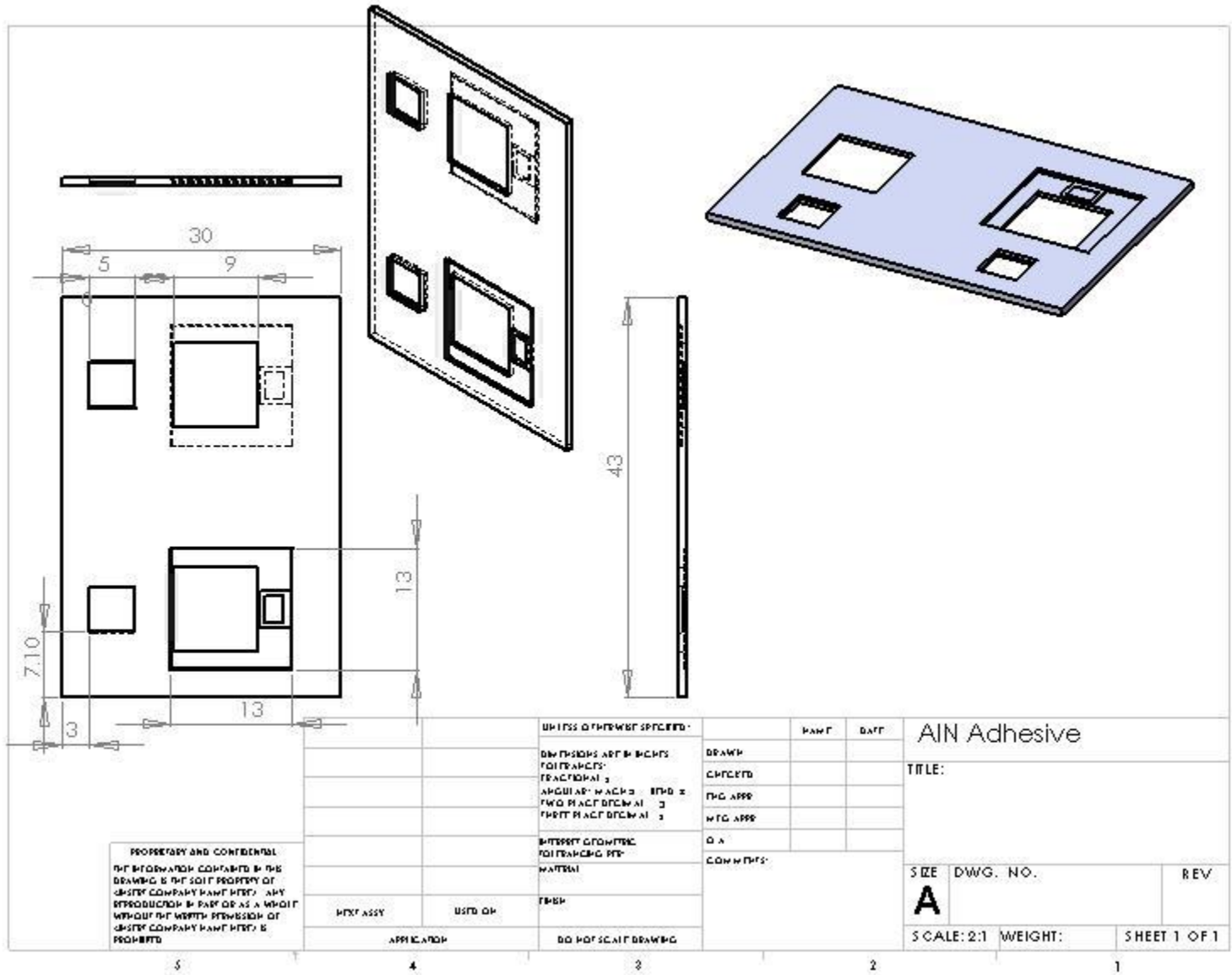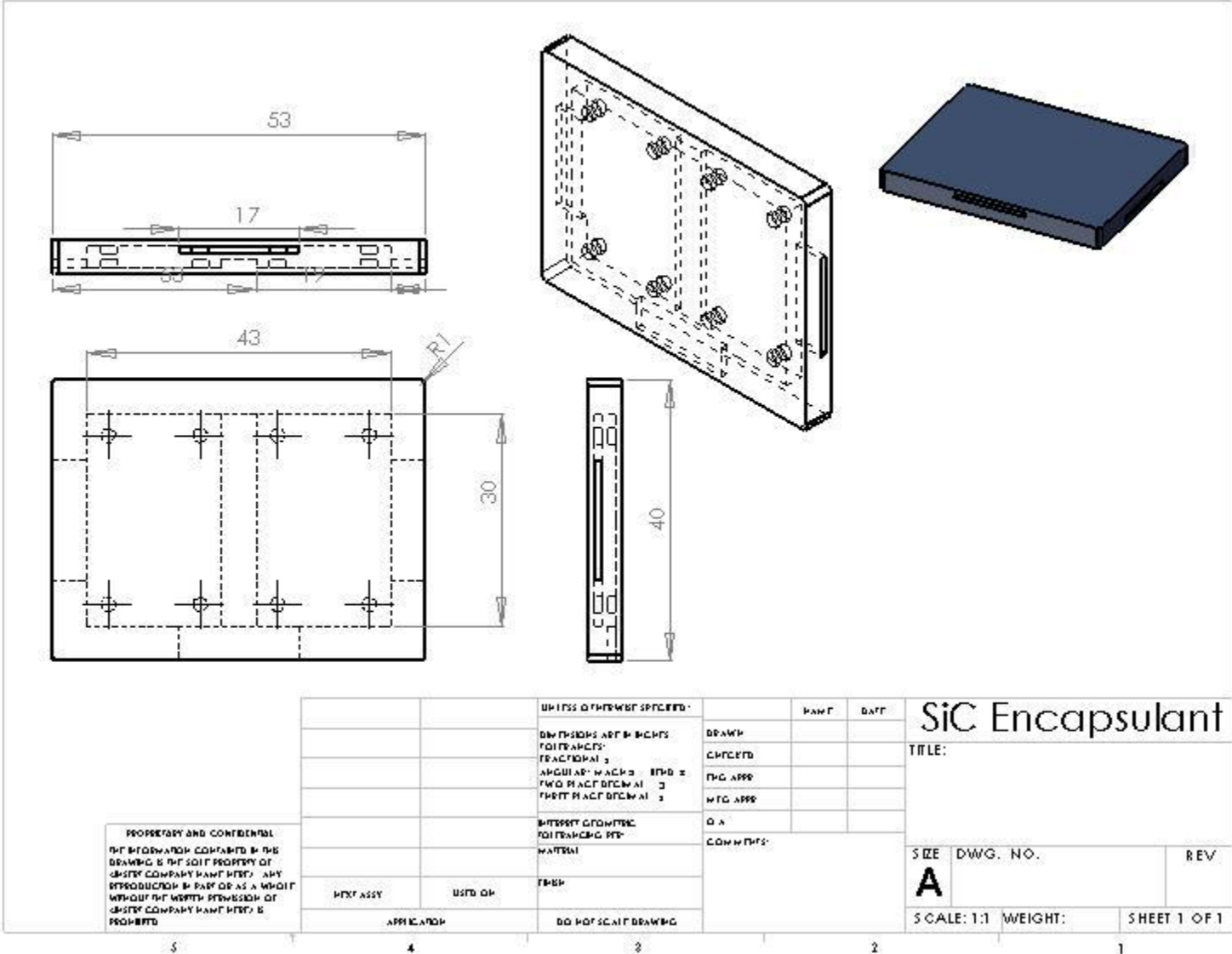|				UNLESS OTHERWISE SPECIFIED:		NAME	DATE	SiC Encapsulant
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APPENDIX B: THESIS DEFENSE PRESENTATION SLIDES

UNIVERSITY OF CENTRAL FLORIDA

HIGH TEMPERATURE PACKAGING FOR WIDE BANDGAP SEMICONDUCTOR DEVICES

November 5, 2008

M.S. Thesis Defense

Brian Grummel

SCHOOL OF ELECTRICAL ENGINEERING & COMPUTER SCIENCE

Outline

- Motivation
- Review of Prior Art
- Objectives
- New Packaging Concept
- Selection of Packaging Materials
- Modeling Results and Discussion
- Experimental Results and Discussion
- Future Work

UCF Stands For Opportunity

SCHOOL OF ELECTRICAL ENGINEERING & COMPUTER SCIENCE

Motivation: Power Modules

- Feature High Power Half-Bridge Circuit
- IGBT or MOSFET, Si PiN or SiC JBS Diodes

UCF Stands For Opportunity

SCHOOL OF ELECTRICAL ENGINEERING & COMPUTER SCIENCE

Power Modules
Current Applications

High Voltage DC Power Transmission

Traction Applications

UCF Stands For Opportunity

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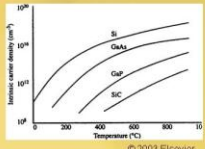
Motivation

- Current module design suffers from several problems that limit their ratings and induce reliability problems.
- New wide bandgap semiconductors increase potentials for semiconductor usage that are infeasible with current modules.
- Currently unexploited markets in part due to packaging constraints.

UCF Stands For Opportunity

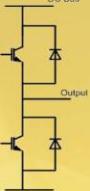SCHOOL OF ELECTRICAL ENGINEERING & COMPUTER SCIENCE

Project Motivation
Wide Bandgap Semiconductor Advantages

- Great temperature resilience due to low intrinsic carrier concentration

$$\uparrow E_g \rightarrow \downarrow n_i \rightarrow \downarrow I_r(T)$$

- High thermal conductivity reduced hot spots of thermal runaway

$$n_i = \sqrt{N_c N_v} \exp\left(-E_g \Big/ 2kT\right) \frac{1}{cm^3}$$

© 2003 Elsevier

Material	E_g	n_i	ε_r	μ_n	E_c	V_{sat}	λ	Direct/
	(eV)	(cm⁻³)		(cm²/V·s)	(MV/cm)	(10⁷ cm/s)	(W/cm²K)	Indirect
Si	1.1	1.5e10	11.8	1350	0.3	1.0	1.5	I
GaAs	1.4	1.8e6	12.8	8500	0.4	2.0	0.5	D
InN	1.86	~1e3	9.6	3000	1.0	2.5	-	D
GaN	3.39	1.9e-10	9.0	900	3.3	2.5	1.3	D
4H-SiC	3.26	8.2e-9	10	~700	2.0	2.0	4.5	I

Elasser, Ahmed and T. Paul Chow. "Silicon Carbide Benefits and Advantages for Power Electronic Circuits and Systems." 90, no 6, pp. 969-986 (June 2002).

UCF Stands For Opportunity

SCHOOL OF ELECTRICAL ENGINEERING & COMPUTER SCIENCE

Project Motivation

High Temperature Electronics Environments

- **Energy Exploration**
  - High Ambient Temperature Environments
    - Down-Hole Environments
      - Geothermal
      - Oil Well Excavation
    - 200-300°C Ambient Temperatures
    - Used in Conjunction with SOI Technology
- **Automotive/Aerospace**
  - Limited Cooling Systems Possibilities
  - Seeking System Efficiency Increases
    - Reduce weight by shrinking cooling system

Thermal Resistance

$$P_{max} = \frac{T_{j,max} - T_C}{R_{\theta JC}}$$

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Prior Art

Classical Power Module Design

- Terminal Leads
- Bonding Wire
- Encapsulant
- Semiconductor
- Solder
- DBC (Cu/AlN/Cu)
- Baseplate (Cu)
- Thermal Grease
- Heat Sink

Xing, Lee K. "Extraction of parasitics within wire-bond IGBT modules." Applied Power Electronics Conference and Exposition, 1998. APEC. 1998. 497-503.

UCF — Stands For Opportunity — SCHOOL OF ELECTRICAL ENGINEERING & COMPUTER SCIENCE

Prior Art

Module Design Considerations

Need to Provide Low Thermal Resistance Rugged Package

- Thermal Stability
- Cost, Ease of Manufacture
- Coefficient of Thermal Expansion
- Junction to Case Thermal Resistance
- Consistent Electrical Characteristics
- Mechanical Stability

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Prior Art

Module Design Considerations

Material	CTE (µm/m-K)	Conductivity (W/m-K)
Copper	16.4	385
Aluminum	24	210
Silicon	3.5	124
SnPb40 Solder	24	50
Aluminum Nitride	4.5	83
Thermal Grease		0.75

CTE mismatch leads to interface shear stress with temperature rise

Thermal Heat Flow to Heat Sink

Thermal Circuit Model

Van Godbold, C., "Novel designs in power modules," IAS '95., pp.911-915.
Yun, Chan-Su, et al. "Thermal component model for electrothermal analysis of IGBT module systems." Advanced Packaging, IEEE Transactions 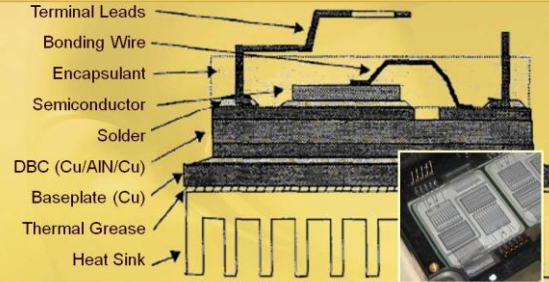on [see also Components, Packaging and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on] 26.3 (2001): 401-406.

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Prior Art

Classic Module Failure Modes

- **Die Cracking**
- **Solder Cracking**
- **Device Burnout**
- **Wirebond Liftoff**
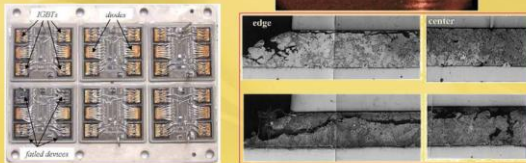
Schutze, T., Berg, "Further improvements in the reliability of IGBT modules," Industry Applications Conference, 1998. Morozumi, A., et al. "Reliability of power cycling for IGBT power semiconductor modules." IAS Annual Meeting. Conference Record of the 2001 IEEE. Chicago: IEEE Press, 2001.

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Prior Art

Classic Module Failure Modes

- **Wirebond Issues**
  - Liftoff
    - ~80% of Package Failures
    - >20 ppm/K CTE mismatch interface
  - Inductance
    - Contribute to 40-55 nH Package Inductance
    - Induces >100% Steady State Current
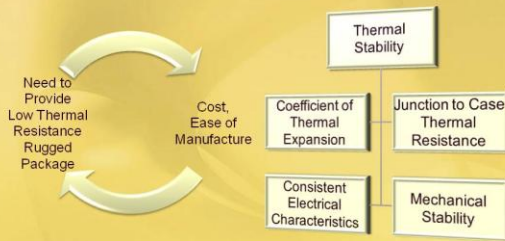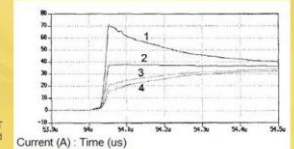

Wuchen Wu "Thermal stress related packaging failure in power IGBT modules." ISPSD '95
Xing, Lee K. "Extraction of parasitics within wire-bond IGBT modules." Applied Power Electronics Conference and Exposition, 1998. APEC. 1998. 497-503.

Current (A) : Time (us)

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Advancing Module Designs
ABB Press Pack Modules

- Can achieve short circuit in failure
- Spring Contact Connection
  - Solderless
- Pseudo Double-Sided Cooling
- 1000A/4.5kV Sub-Module
  - Full module comprised of multiple sub-modules
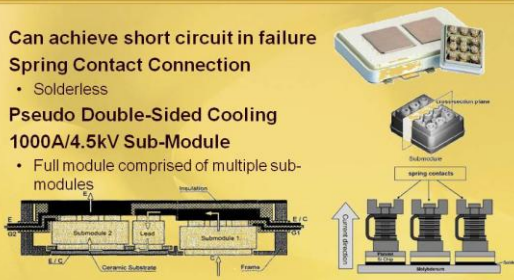
Gunturi, Satish. "On the Operation of a Press Pack IGBT Module Under Short Circuit Operation." IEEE Transactions on Advanced Packaging 29.3 (2006).

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Advancing Module Designs
Center for Power Electronics Systems (CPES)

- Planar Packaging
- Double-Sided Cooling
- High Temperature Nano-Silver Sinter Paste for Soldering
- 300°C Goal Temperature
  - Thermal and Mechanical Designing
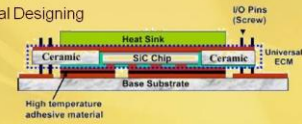
Yin, Jian, Zhenxian Liang and J.D. van Wyk. "High temperature embedded power module." Applied Power Electronics Conference and Exposition, 2005. APEC 2005. Twentieth Annual IEEE. n.d. 357 - 361.

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Advancing Module Designs
Arkansas Power Electronic International

- Fundamental Classical Design
  - Wirebonds Still Present
  - High Temperature Hermetic Casing
- Pbln (310°C) Solder
- Experimental Encapsulation
  - Not yet working correctly
- Hybrid Module
  - Includes Gate Drivers, SOI?
- 300°C Goal Temperature

Hornberger, J.M., et al. "A Fully Integrated 300°C, 4 kW, 3-Phase, SiC Motor Drive Module." Power Electronics Specialists Conference, 2007. PESC 2007. IEEE. 2007.

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Advancing Module Designs
SEMIKRON

- MiniSKiiP IPM
  - Intelligent Power Module
- Press Pack / Press Pin Connection
  - Nano-Sinter Silver Paste
- Hybrid Module
  - Includes Gate Drivers, SOI
- Improved Ratings
  - 175°C Temperature Rating From 125°C
  - $R_{\theta TC}$=0.95 K/W From 1.45 K/W
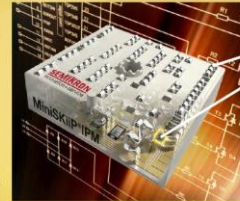
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Outline

- Motivation
- Review of Prior Art
- Objectives
- New Packaging Concept
- Selection of Packaging Materials
- Modeling Results and Discussion
- Experimental Results and Discussion
- Future Work

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Objective

To investigate a new high temperature power packaging concept for wide bandgap semiconductors with thermal and mechanical modeling and experimental methods.

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New Power Module Design Concept

- **CTE Matching Materials**
  - SiC = 3.8 ppm/K
- **High Heat Capable Materials**
  - 300° C Package Rating
- **Removal of Wirebonds**
- **Double Sided Cooling**
  - Reduce Thermal Resistance
- **Low Profile Design**
  - <1kg, ~0.1 x 5 x 3 cm

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Design Concept:
Module Exploded View

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Selection of Packaging Materials

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Selection of Solder Materials

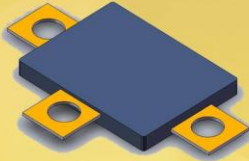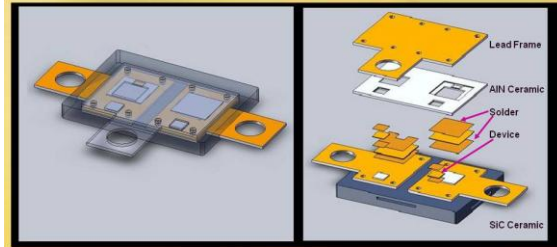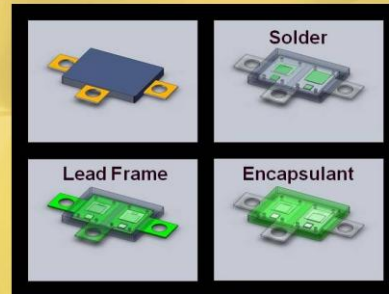| Material	Supplier	Base Material	Max Temperature (° C)	Electrical Conductivity (S/m)	Thermal Cond.(K) (W/m-k)	CTE (ppm/k)	Bonding Shear (MPa)	Young's Modulus (GPa)
SnPb40	Various	Sn	183	6.67E+06	49	21.6	52	
PyroDuct 597A	Aremco	Ag	650	5.00E+05	9.09	17.3	8.3	
PyroDuct 598A	Aremco	Ni	538	2.00E+04	2.57	11.7		
nanoTach	NBE Tech	Ag	961	3.80E+05	240e	~19.6	20-40	9
Duralco	Cotronics	Ag	343	5.00E+04	7.20			
XH9680-16	Namics	Ag		2.00E+05				
AuGe12	Indium Corp	Au	356	6.63E+06	44.00	13.0	105	
PbInAg 92.5/5/2.5	Indium Corp	Pb	300	3.23E+06	25.00	25.0		
WS497 (AuIn19)	Williams Advanced	Au	487	4.88E+06	28.00	14.7		

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Selection of Lead Frame Materials

Material	Supplier	Max Temp (°C)	Thermal Cond. (W/m-k)	CTE (ppm/K)	Electrical Cond. (S/m)	Density (g/cc)	Young's Modulus (GPa)	Poisson's Ratio
Copper		1083	385.0	16.80	5.88E+07	8.96	110	0.343
Diamond		4027	2000.0	1.18	2.17E+01	3.51	700	0.200
Molybdenum Copper (MoCu15)	Eagle Alloys	2617	138.0	5.30	1.87E+07	10.22	329	0.310
Copper Diamond Composite*		1083	210.0	17.8	5.88E+07	8.96	110	0.343
Tungsten		3370	163.3	4.40	1.77E+07	19.30	400	0.280
Tungsten Copper (WCu10)*	BAM	1083	175.0	5.90	1.56E+07	17.00		0.290
Tungsten Alloy (Ni/W/Cu 3.5/95/1.5)**	CMW Inc.	1200	137.0	4.43	5.80E+06	18.00	310	0.280
Copper Diamond Composite**	Plansee	1020	470.0	6.70	1.11E+07	5.50	255	0.280

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Slide 1: Selection of Encapsulant Materials

Material	Base Material	Supplier	Max Temperature	Thermal Cond.	CTE	Electrical Conductivity
			(°C)	(W/m-k)	(µm/m-°C)	(S/m)
Epoxy Cresol Novolac	SiO2		165	0.67		18-65
Cermacast 575N*	Al2O3	Aremco	1650	28.00		1.0E-07
Cermacast 646N*	ZrO2	Aremco	1650	2.00		1.0E-07
Cermacast 673N*	SiC	Aremco	1750	36.00		1.0E-07
Cermabond 865	AlN	Aremco	1650	136.40	2.70	
Duralpot 863**	Polymer	Cotronics	343	1.30	34.00	1.0E-12
Duralco 4460*	Polymer	Cotronics	260	0.58	64.00	1.0E-11
VECTRA S135 LCP**	Glass	Ticona	350			1.0E-13
VECTRA E130i LCP**	Glass	Ticona	300			1.0E-11
EPM-2482**	Si	NuSil	260			1.0E-12

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Slide 2: Outline

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Slide 3: Introduction to Modeling Tools

- COSMOSWorks by SolidWorks
- Full 3D FEA modeler and simulator
- Able to simulate conductive and convective heat transfer
- Link simulations to derive stress from power input and temperature rise

3DS SolidWorks

COSMOSWorks
Design Validation Made Simple

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Slide 4: Modeling Result: Thermal Resistance of Single Die Power Module

Double-Sided Cooling

$T_{amb} = 25°C$
$Q_{in} = 100W$
$T_{max} = 48.7°C$

$$\therefore R_{\theta C}(D-S) = \frac{T_{max} - T_{case}}{Q_{in}} = \frac{(48.7-25)C}{100W} = 0.237 \frac{K}{W}$$

Single-Sided Cooling

$T_{amb} = 25°C$
$Q_{in} = 100W$
$T_{max} = 55.1°C$

$$\therefore R_{\theta C}(S-S) = \frac{T_{max} - T_{case}}{Q_{in}} = \frac{(55.1-25)C}{100W} = 0.301 \frac{K}{W}$$

Module	Thermal R
SEMIKRON	$R_{JC} = 0.95$ K/W
Double-Sided	$R_{JC} = 0.237$ K/W
Single-Sided	$R_{JC} = 0.301$ K/W

75.1% and 68.3% Decrease in thermal resistance below current state of the art Power Modules. ($R_{JC} = 0.95$ K/W)

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Slide 5: Modeling Result: Temperature Distribution for Single Die Power Module
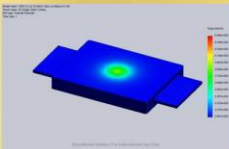
Single-Sided Cooling

$R_{\theta C}(S-S) = 0.301 \frac{K}{W}$

$Q(T_{J,max} = 300°C) = 1.48kW$

Double-Sided Cooling

$R_{\theta C}(D-S) = 0.237 \frac{K}{W}$

$Q(T_{J,max} = 300°C) = 1.93kW$

$$\%Increase, R_{\theta C}(D \rightarrow S) = \frac{0.301 - 0.237}{0.237} = 27\%$$

- Only a 27% increase in thermal resistance with half the cooling surface. (Why? Flux)
  - Double Sided Module can dissipate 30.5% more power at same $T_{J,max}$

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Slide 6: Modeling Result: Heat Flux Distribution of Single Die Power Module
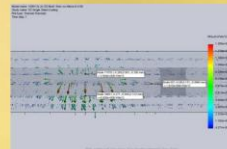
Single-Sided Cooling

$\phi_{Qs-s}(d = 1cm) = 1.615 \cdot 10^5 \frac{W}{m^2}$
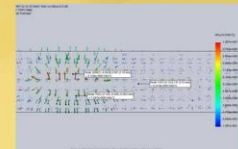
Double-Sided Cooling

$\phi_{QD-s}(d = 1cm) = 6.474 \cdot 10^5 \frac{W}{m^2}$

Heat flux around the periphery of the device is ~3X higher in the single-sided module

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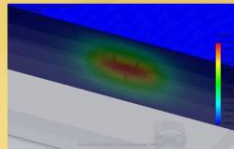## Modeling Result: Temperature Distribution for Half-Bridge Module

$Q=100W$, $T_{case}=25°$ C

Modeling Result: Thermal Resistance of Half-Bridge Module

Module	Thermal Resistance	Decrease in Thermal Resistance from Classic Module
Classic Module	R_{JC}=1.45 K/W	--
SEMIKRON	R_{JC}=0.95 K/W	34.5%
Single-Cooling Half Bridge	R_{JC}=0.516 K/W	64.6%
Double-Cooling Half Bridge	R_{JC}=0.374 K/W	74.2%

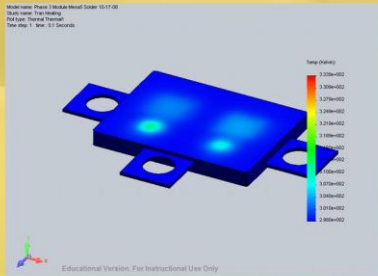## Modeling Result: Sheer Stress Analysis for Half-Bridge Module

- Bonding Shear Strength - AuGe12=185 Mpa
- Peak Stress will occur from greatest expansion→ Highest Temperature

$T_{amb}=25°C$

$T_{max}=300°C$

$R_{\theta JC}(S-S) = \dfrac{T_{max}-T_{case}}{Q_{TRAN}} = 0.358\,K/W$

$\Rightarrow Q_{TRAN}=768W$

$\Rightarrow Q_{Diode}=0.694 Q_{TRAN}=533.3W$

Peak Shear Stress

$\tau_{Shear}(T=300°C)=175MPa < 185MPa$

Modeling Result: Sheer Stress Analysis for Half-Bridge Module

- Applicable Stresses Much Lower

$\tau_{Shear,Max}(Solder)=61.9MPa$

$\tau_{Shear,Max}(Diode)=114MPa$

- Device Stresses Identical for ambient temperature rise to 300° C
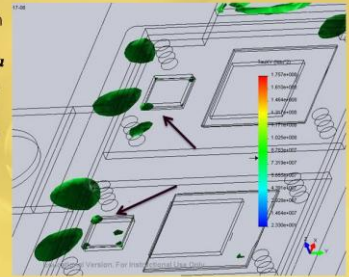
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Experimental Prototypes: Single Die Power Module

- Durapot Encapsulant
  - CTE Crack at 300° C
- Cermacast 673N
  - a-SiC Cermaic

Electrical Measurement at 300C

Module A-10 Temperature Calibration

Experimental Data
250°C Ambient Stress Test

Mod A-4
- Shows degradation at 50 hr mark before failure <100 hr
- Construction evident to be of lower quality to A-10 before test

Mod A-10
- Great reliance to constant high ambient temperature

Module A-4 | Module A-10

Experimental Data
250°C Ambient Stress Test

Mod A-4
- Shows degradation at 50 hr mark before failure <100 hr
- Construction evident to be of lower quality to A-10 before test

Mod A-10
- Great reliance to constant high ambient temperature

Module A-4 | Module A-10

Experimental Data
Inductance Test

- *f=20 kHz, simulate operation frequency*
- Biased Devices On @ I$_c$=5 A
- Control Module – Phase One Mod w/o Device

Classic Module
- Tested single Diode to Match Phase One Module Condition
- Experimental Data fits Simulation precisely
- Inductance contributed from terminals and wirebonds

Phase One Modules
- 92.8% decrease in parasitic inductance!
- Both Module Results Concur

	Traditional (Modeling)	Traditional (Measured)	New Module Package D only No	New Module Average (Measured)
Parasitic Inductance	40-55nH	45nH	1.1nH	3.2nH

Xing, Lee K. "Extraction of parasitics within wire-bond IGBT modules." Applied Power Electronics Conference and Exposition, 1998. APEC. 1998. 497-503.

Outline

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Future Work

- Must continue to implement new designs of the module to fully implement gate control of transistor devices and improve thermal resistance.
- Will perform simulations to enhance robustness of expected results and to further predict module performance.
- Construct additional single device modules and half-bridge modules to perform additional experimental testing and further prove proof of concept.

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