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University of Central Florida

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**ON-CHIP ELECTRO-STATIC DISCHARGE (ESD) PROTECTION
FOR RADIO-FREQUENCY INTEGRATED CIRCUITS**

by

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A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy
in the School of Electrical Engineering and Computer Science
in the College of Engineering and Computer Science
at the University of Central Florida
Orlando, Florida

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2013

Major Professor: Juin J. Liou

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ABSTRACT

Electrostatic Discharge (ESD) phenomenon is a common phenomenon in daily life and it could damage the integrated circuit throughout the whole cycle of product from the manufacturing. Several ESD stress models and test methods have been used to reproduce ESD events and characterize ESD protection device's performance. The basic ESD stress models are: Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM). On-chip ESD protection devices are widely used to discharge ESD current and limit the overstress voltage under different ESD events. Some effective ESD protection devices were reported for low speed circuit applications such as analog ICs or digital ICs in CMOS process. On the contrast, only a few ESD protection devices available for radio frequency integrated circuits (RF ICs). ESD protection for RF ICs is more challenging than traditional low speed CMOS ESD protection design because of the facts that: (1) Process limitation: High-performance RF ICs are typically fabricated in compound semiconductor process such as GaAs pHEMT and SiGe HBT process. And some proved effective ESD devices (e.g. SCR) are not able to be fabricated in those processes due to process limitation. Moreover, compound semiconductor process has lower thermal conductivity which will worsen its ESD damage immunity. (2) Parasitic capacitance limitation: Even for RF CMOS process, the inherent parasitic capacitance of ESD protection devices is a big concern. Therefore, this dissertation will contribute on ESD protection designs for RF ICs in all the major processes including GaAs pHEMT, SiGe BiCMOS and standard CMOS.

The ESD protection for RF ICs in GaAs pHEMT process is very difficult, and the typical HBM protection level is below 1-kV HBM level. The first part of our work is to analyze pHEMT's snapback, post-snapback saturation and thermal failure under ESD stress using TLP-like Sentaurus TCAD simulation. The snapback is caused by virtual bipolar transistor due to large electron-hole pairs impacted near drain region. Post-snapback saturation is caused by temperature-induced mobility degradation due to III-V compound semiconductor materials' poor thermal conductivity. And thermal failure is found to be caused by hot spot located in pHEMT's InGaAs layer. Understanding of these physical mechanisms is critical to design effective ESD protection device in GaAs pHEMT process.

Several novel ESD protection devices were designed in 0.5um GaAs pHEMT process. The multi-gate pHEMT based ESD protection devices in both enhancement-mode and depletion-mode were reported and characterized then. Due to the multiple current paths available in the multi-gate pHEMT, the new ESD protection clamp showed significantly improved ESD performances over the conventional single-gate pHEMT ESD clamp, including higher current discharge capability, lower on-state resistance, and smaller voltage transient. We proposed another further enhanced ESD protection clamp based on a novel drain-less, multi-gate pHEMT in a 0.5um GaAs pHEMT technology. Based on Barth 4002 TLP measurement results, the ESD protection devices proposed in this chapter can improve the ESD level from 1-kV (0.6 A It^2) to up to 8-kV ($> 5.2 \text{ A It}^2$) under HBM.

Then we optimized SiGe-based silicon controlled rectifiers (SiGe SCR) in SiGe BiCMOS process. SiGe SCR is considered a good candidate ESD protection device in this process. But the possible slow turn-on issue under CDM ESD events is the major concern. In order to optimize the turn-on performance of SiGe SCR against CDM ESD, the Barth 4012 very fast TLP (vfTLP) and vfTLP-like TCAD simulation were used for characterization and analysis. It was demonstrated that a SiGe SCR implemented with a P PLUG layer and minimal PNP base width can supply the smallest peak voltage and fastest response time which is resulted from the fact that the impact ionization region and effective base width in the SiGe SCR were reduced due to the presence of the P PLUG layer. This work demonstrated a practical approach for designing optimum ESD protection solutions for the low-voltage/radio frequency integrated circuits in SiGe BiCMOS process.

In the end, we optimized SCRs in standard silicon-based CMOS process to supply protection for high speed/radio-frequency ICs. SCR is again considered the best for its excellent current handling ability. But the parasitic capacitance of SCRs needs to be reduced to limit SCR's impact to RF performance. We proposed a novel SCR-based ESD structure and characterize it experimentally for the design of effective ESD protection in high-frequency CMOS based integrated circuits. The proposed SCR-based ESD protection device showed a much lower parasitic capacitance and better ESD performance than the conventional SCR and a low-capacitance SCR reported in the literature. The physics underlying the low capacitance was explained by measurements using HP 4284 capacitance meter.

Throughout the dissertation work, all the measurements are mainly conducted using Barth 4002 transmission line pulsing (TLP) and Barth 4012 very fast transmission line pulsing (vfTLP) testers. All the simulation was performed using Sentaurus TCAD tool from Synopsys.

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It is impossible for me to finish this dissertation without the help and support of a number of people.

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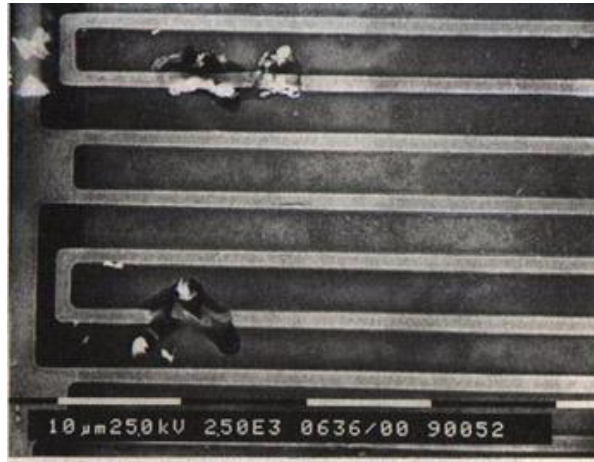
CHAPTER 1 INTRODUCTION OF ESD IN INTEGRATED CIRCUITS

Electrostatic discharge (ESD) has been one of the most important design concerns to integrated circuits (ICs) for many years.[1-10] This reliability threaten exists in all kinds of fabrication processes including mainstream silicon-based complementary metal–oxide–semiconductor (CMOS) process and other compound semiconductor processes such as GaAs or GaN pseudomorphic high electron mobility transistor (pHEMT) process, and silicon-germanium heterojunction bipolar transistor (SiGe HBT) process. Static charge is an unbalanced electrical charge at rest. In semiconductor fabrication environment, the static charge could be induced by human, machine or by semiconductor device itself. Static charge is common in semiconductor devices and components. The move of static charge from one surface to another surface causes ESD phenomenon in ICs. When ESD happens, the large transient voltage and current could damages or destroys gate oxide, metallization, and junctions. Figure 1.1 (a) shows the ESD damage in IC components. It is reported that ESD damage accounts for over 37% return failure, and it is the most important reason for product reliability.

In order to protect ICs against ESD-introduced damage, some on-chip ESD protection devices were designed in CMOS, pHEMT, and SiGe HBT process. The ESD protection structures for low speed/ low frequency circuits are fairly mature and the typical ESD failure level is above 2-kV under Human Body Model. However, effective ESD protection for radio frequency is still missing: [9, 11, 12]

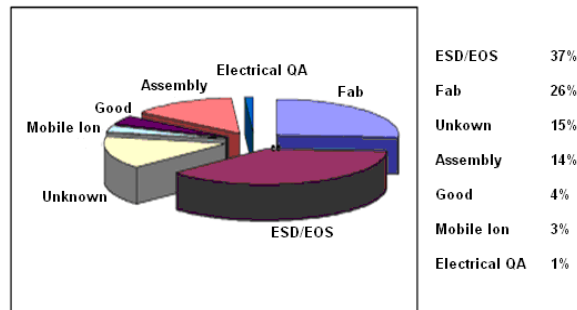
- i. The existing ESD protection is mainly for CMOS process. There are basically no effective ESD protection structures in compound semiconductor process such as GaAs pHEMT and SiGe HBT process. Compound semiconductor process is mainly for high performance RF/Microwave circuits and they are generally vulnerable under ESD events because of the inherent low thermal conductivity of compound materials like GaAs and AlGaAs. The available ESD level is only about 1kV HBM with widely used stacked schottky diode-based ESD protection solution.
- ii. Even though there are already some ESD protection solutions for RF ICs in CMOS process. The existing ESD protection design in CMOS process inherently introduces fairly large parasitic capacitance which is not suitable to protect RF ICs against ESD.

Therefore, there has been a growing demand for the availability of robust ESD protection solutions for radio frequency integrated circuits (RFIC's). This dissertation will mainly focus on design and simulation of ESD devices in compound semiconductor processes (GaAs pHEMT, and SiGe HBT) for RF/Microwave ICs. And also a novel ESD protection device in CMOS process was proposed in the very end of this dissertation.



(a)

Customer Return Failure Statistics



ESD is one of the leading causes of microchip failure during manufacture as well as field and consumer use

Data from National Semiconductor Corporation

(b)

Figure 1.1 (a) Electro-Static Discharge (ESD) damage in Integrated Circuits (IC) (b) Statistics of ESD failure

1.1 ESD Models and Test Setup

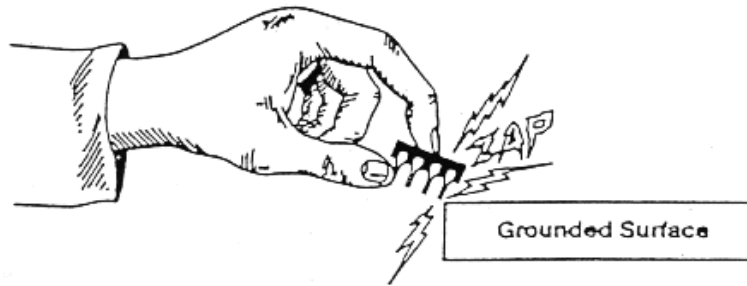
ESD events are very common in IC components. Based on their different origins and impact to ICs, ESD events are classified by three different models: Human Body

Model (HBM), Machine Model (MM), and Charged Device Model (CDM). Figure 1.2 (a) (b) and (c) present the discharge conditions for HBM, MM, and CDM respectively.

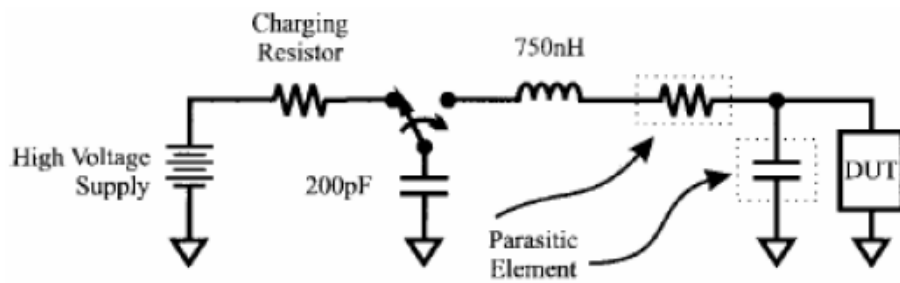
HBM is the most commonly used ESD model during reliability test, and it is the mandatory requirement for any IC components. When a human is charged with static and touches uncharged IC components, the unbalanced static could be quickly transferred into ICs and flow into grounded pin. This process lasts only hundreds of nano-seconds and the peak voltage could be as high as several amperes. Such high transient current could easily destroy IC if there is no proper protection circuit. The HBM test standard was documented in MIL-STD-883, there the equivalent capacitor (C_{esd}) is 100 pF, the equivalent resistor (R_{esd}) is 1500 Ohm.

The MM simulates a machine discharging accumulated static charge through an IC component to ground. It comprises a series RC network of a 200-pF capacitor, and nominal series resistance of less than 1 ohm. Because of the extremely small value of resistance, the static discharges much faster than HBM event. Therefore, the transient current level is much higher than HBM ESD event, and the discharge current pulse is faster than HBM. The CDM describes charging/discharging events that occur in IC components and semiconductor itself. One of many examples is a device sliding down a shipping tube and hitting a metal grounded surface. The CDM addresses the possibility that a charge may reside on a lead frame or package (e.g., from shipping) and discharge through a pin that subsequently is grounded, causing damage to sensitive devices in the path. The discharge current is limited only by the parasitic impedance and capacitance

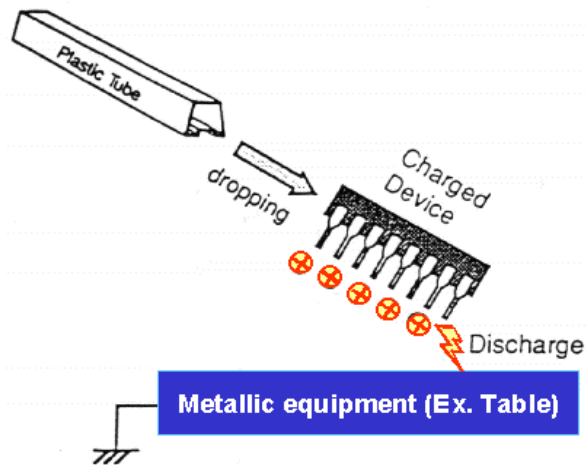
of the device. Therefore, the discharge current pulse is even faster and more severe than both MM and HBM.



(a)



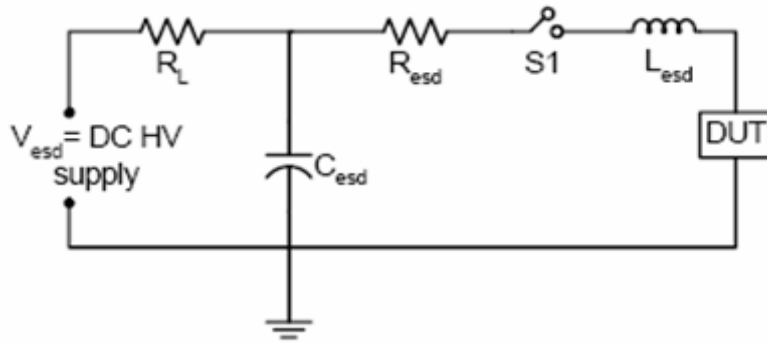
(b)



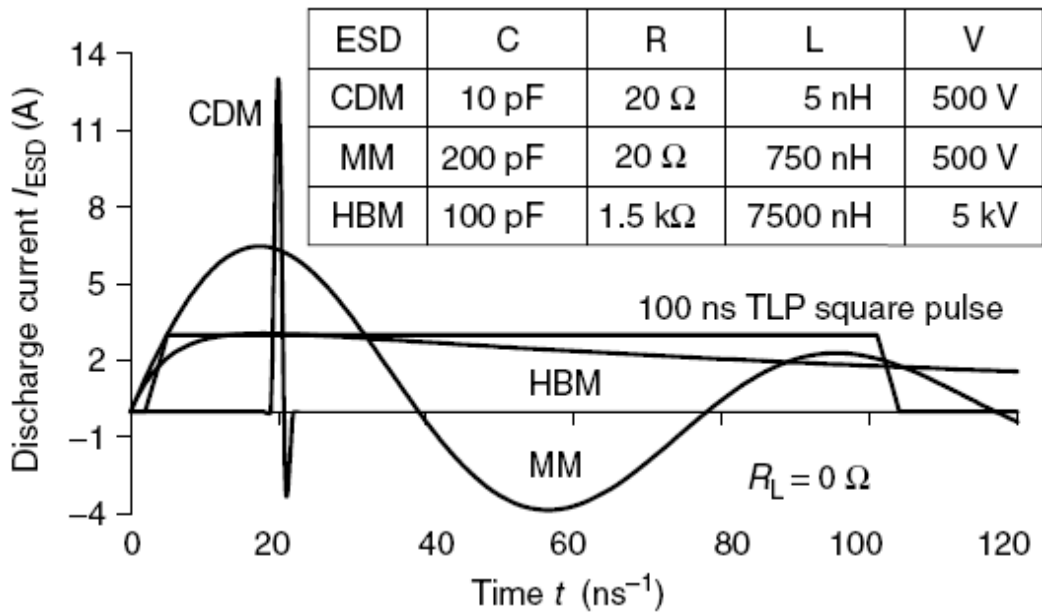
(c)

Figure 1.2 Discharge condition for (a) Human-Body Model (HBM) (b) Machine Model (MM) (c) Charged Device Model (CDM)

The equivalent circuit for ESD event is described in Figure 1.3 (a). All the three abovementioned ESD models (HBM, MM and CDM) can be represented using this equivalent circuit Figure 1.3 (a), and the three models were distinguished by different values of resistance, capacitance and inductance in Figure 1.3 (b). The different current waveforms of HBM, MM and CDM result from different RLC values. If the oscillation frequency $\omega = 1/\sqrt{LC}$ exceeds the damping coefficient $\alpha = R/2L$, including the load resistance, the discharge is an oscillation as observed for the MM and CDM with low resistive loads. Otherwise it is a periodically damped, like the HBM.



(a)

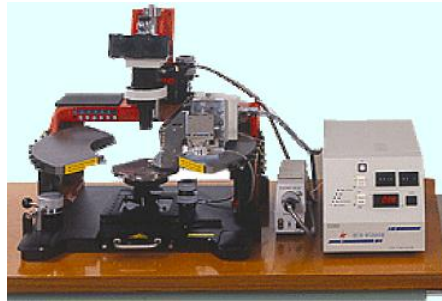


(b)

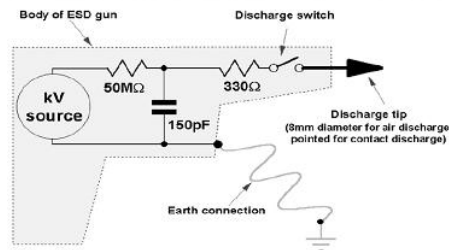
Figure 1.3 (a) RLC equivalent circuit for ESD models (b) Discharge current waveform of ESD models in Figure 1.2

All the above introduced ESD models are tested in a destructive way to check the failure level of an ESD sensitive device. Figure 1.4 (a) is the transient HBM tester to check ESD device's failure under wafer level and Figure 1.4 (b) is the ESD gun to check ESD device's failure under system level. However, these destructive test methods can not supply enough insights of the possible failure analysis. To overcome this

disadvantage, a testing method called Transmission Line Pulse (TLP) was first introduced by Tim Maloney to mimic HBM ESD events. See Figure 1.5 (a), the principle of TLP measurements is that a transmission line cable is used to generate the stable square waveforms and then discharge into an IC component to simulate ESD stress. The TLP pulse has around 100ns width and 10ns rise time. Figure 1.5 (b) shows the most popular Barth 4002 TLP system used nowadays. More recently, the very fast Transmission Line Pulse (vfTLP) system was developed to represent CDM events. vfTLP test system has similar concept of generating square waveform by transmission line cable, but it has much narrow pulse width (1~5ns) and shorter rise time (0.1~0.5ns). Figure 1.5 (c) shows the photo of Barth 4012 vfTLP system. In this dissertation, both TLP and vfTLP will be used to characterize ESD protection devices.

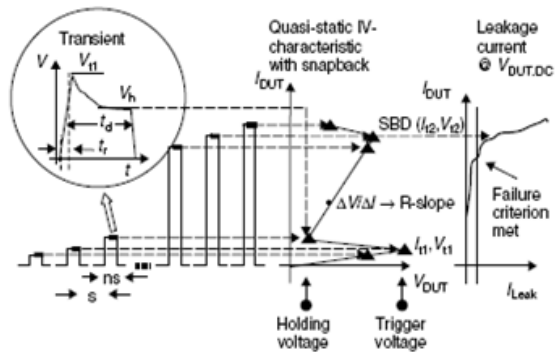


(a)



(b)

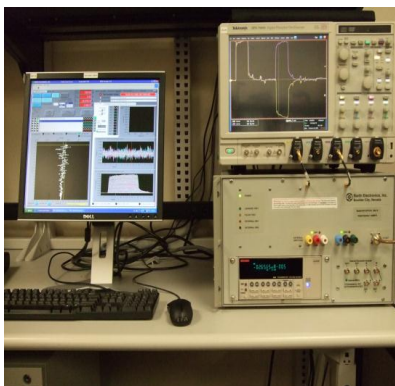
Figure 1.4 (a) Wafer-level transient HBM tester from Hanwa HED W5000M (b) System-level ESD-gun from Schaffner/Teseq



(a)



(b)



(c)

Figure 1.5 (a) Mechanism of Transmission Line Pulse (TLP) Measurement for ESD protection devices (b) Barth 4002 TLP measurement system for HBM ESD model (c) Barth 4012 TLP measurement system for CDM ESD model

1.2 On-Chip ESD Protection Strategy

In order to protect internal circuits against possible ESD-introduced damage, on-chip ESD protection network was built as Figure 1.6. This protection network has five protection units: (1) Input pad to ground “Vss” protection (2) Input pad to power rail “Vdd” (3) Output pad to ground “Vss” protection (4) Output pad to power rail “Vdd” (5) Power rail “Vdd” to ground “Vss”. The core of every protection unit is controllable ESD protection device. This protection device should keep in “OFF” state under normal operation condition of internal circuits and turn “ON” to effectively discharge current under ESD events. This on-chip ESD protection network is a common strategy for all the major process including CMOS, GaAs pHEMT and SiGe HBT.

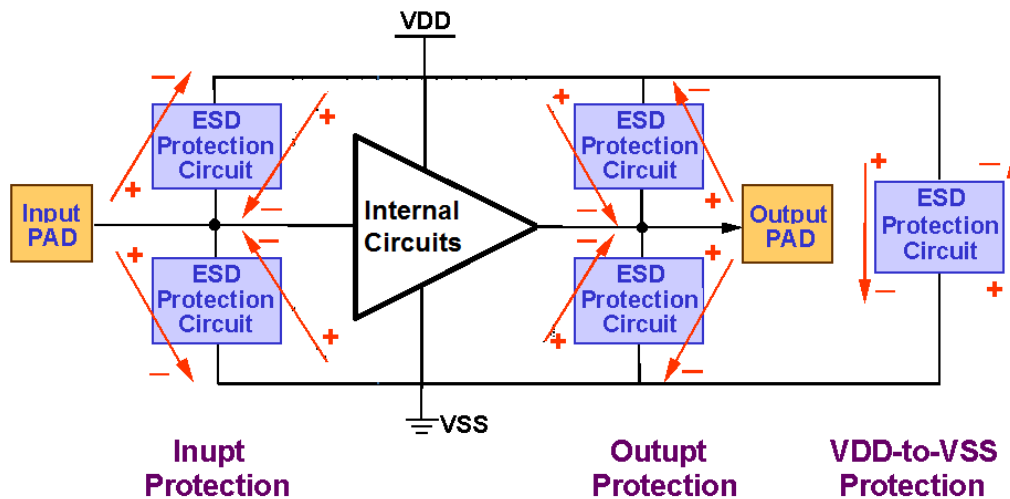


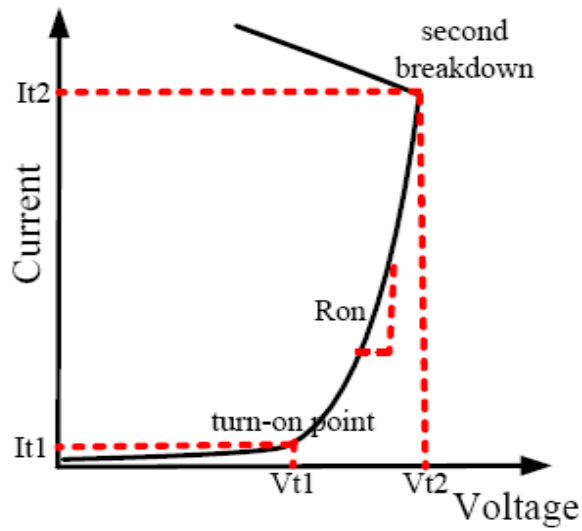
Figure 1.6 On-chip ESD protection network

1.2.1 Two Types of ESD Protection Devices

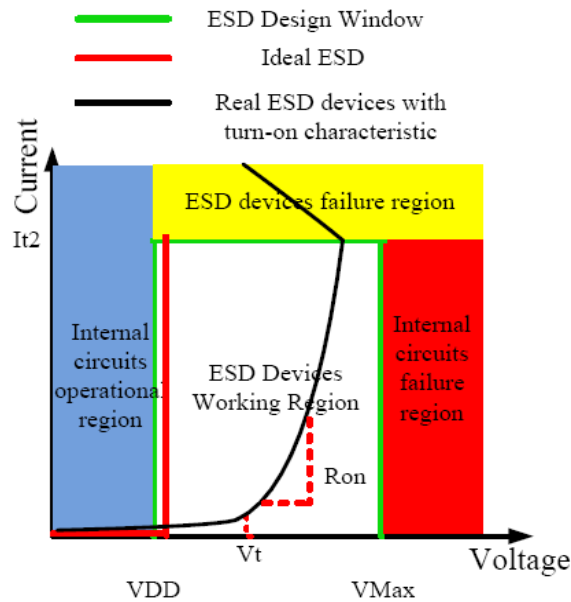
There are mainly two types of on-chip ESD protection devices available: (1) ESD protection device with turn-on characteristics (Figure 1.7). (2) ESD protection device

with snapback characteristics (Figure 1.8). Both types of ESD protection devices will be discussed in this dissertation.

For turn-on characteristics ESD device in Figure 1.7 (a), it has a threshold point (V_{t1} , I_{t1}). When applied voltage is below V_{t1} , ESD protection device works at high-impedance state and the current is negligible. Beyond the turn-on voltage V_{t1} , a low-impedance path will exhibit to discharge ESD current. As the current further increases, ESD device will be damaged at second breakdown point (V_{t2} , V_{t1}). The ESD design window for this type of ESD devices was plotted in Figure 1.7 (b) Different colors are used to differentiate three regions: the internal circuit operation region (blue), internal circuit's failure region (red) and ESD devices failure region (yellow). The ESD design window is surrounded by the three regions and highlighted by solid green lines. A good ESD turn-on characteristics protection device should have its I-V characteristics located in this ESD design window. Silicon diode chain in CMOS process and Schottky diode chain in GaAs pHEMT process are the examples for turn-on characteristics ESD device.



(a)

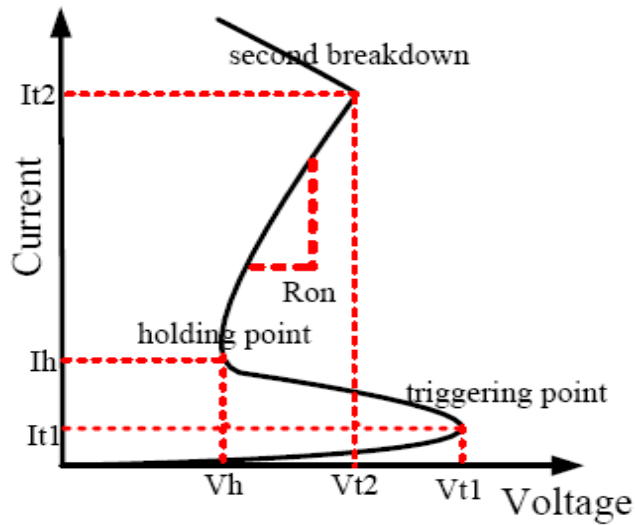


(b)

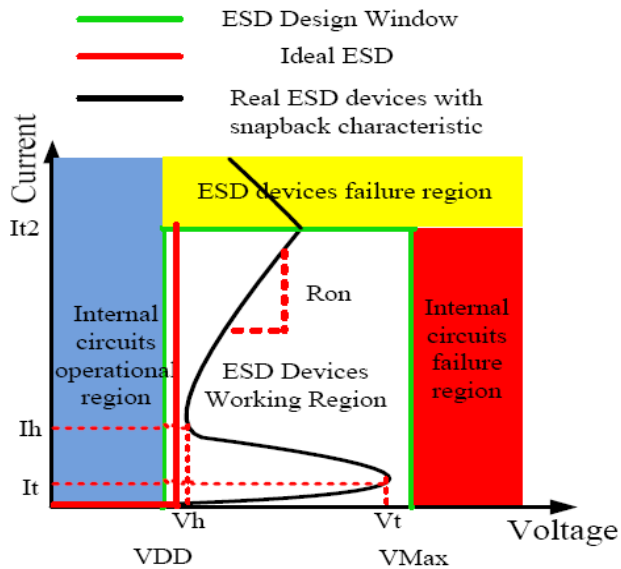
Figure 1.7 ESD protection devices with turn-on characteristics (a) typical I-V curve (b) design window

Figure 1.8 (a) shows the I-V curve of ESD devices with snapback characteristics. This type of ESD devices has similar characteristics before trigger point (V_{t1} , I_{t1}). After the ESD device reaches turn-on voltage V_{t1} , it will be driven into the snapback region

with low clamping voltage and low impedance discharge path. As the current further increases, ESD device will be damaged at second breakdown point (V_{t2} , V_{t1}). The similar ESD design window for this type of ESD devices was plotted in Figure 1.8Figure 1.7 (b). A good ESD snapback characteristics protection device should have its I-V characteristics located in this ESD design window. The examples for snapback characteristics ESD device include externally-triggered active clamp in GaAs pHEMT process and silicon controlled rectifier in CMOS process.



(a)



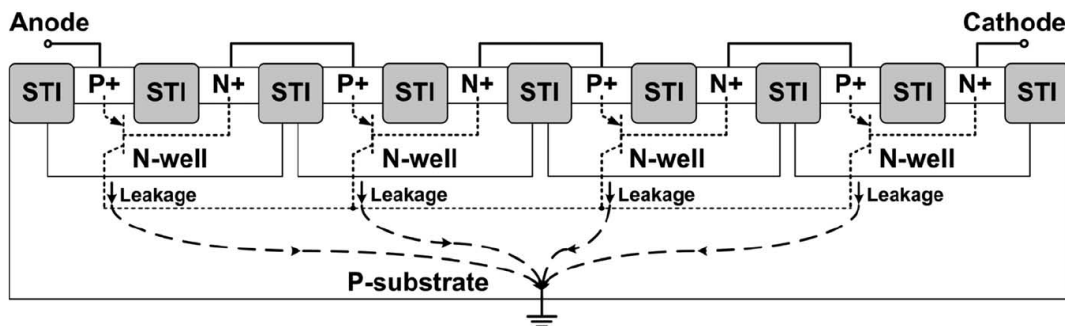
(b)

Figure 1.8 ESD protection devices with snapback characteristics (a) typical I-V curve (b) design window

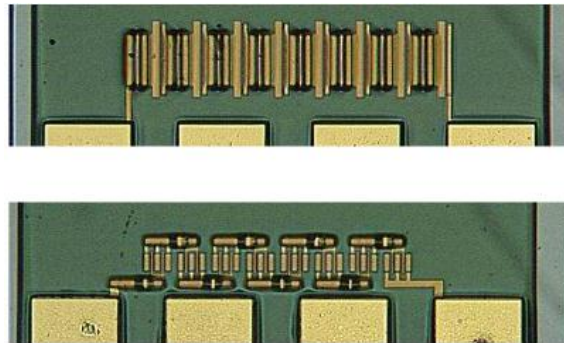
1.2.2 Typical on-Chip ESD Protection Devices for RF ICs

Diode chain is simple and widely used as ESD protection devices for RF ICs in both CMOS process and GaAs pHEMT process as shown in Figure 1.9. Diode chain

could be used to protect low voltage I/O pins, or combined with power supply clamps to provide rail-based ESD protection. The main advantage of diode chain is that it has fairly low parasitic capacitance because the parasitic capacitance of each diode is put in series configuration. The possible drawbacks of diode chain are high on-state resistance and poor leakage current in “OFF” state. There are a lot research papers on optimization of diode chain including limit on-state resistance and decrease leakage current.



(a)



(b)

Figure 1.9 (a) Conventional diode chain in CMOS process (b) Schottky diode chain in GaAs pHEMT process

Externally-triggered ESD clamp shown in Figure 1.10 is a more advanced protection circuit for RF ICs in GaAs pHEMT process. Because of its relatively higher ESD current handling ability, the externally-triggered ESD clamp is a more favorable

protection device in GaAs pHEMT process. The trigger voltage of ESD clamp could be flexibly adjusted by changing the number and orientation of the trigger diodes. Externally-triggered ESD clamp has been investigated in several papers, and the reported failure current level is 0.6A, roughly 1-kV HBM ESD level.

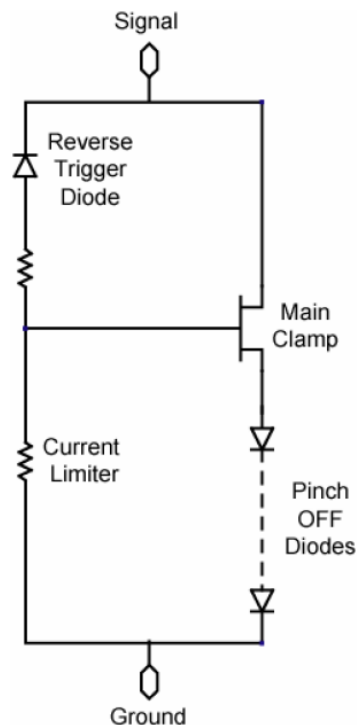
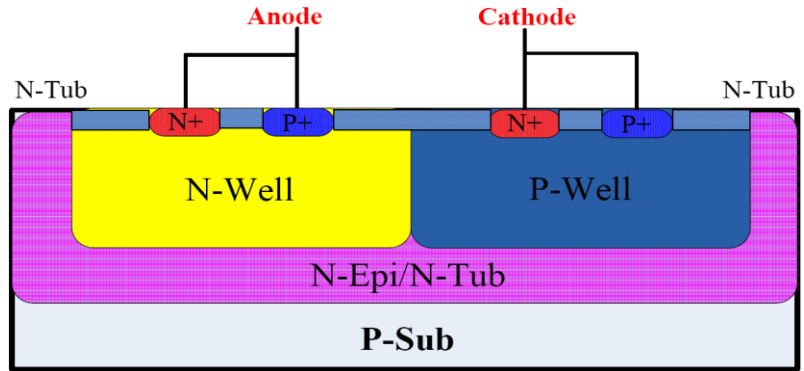


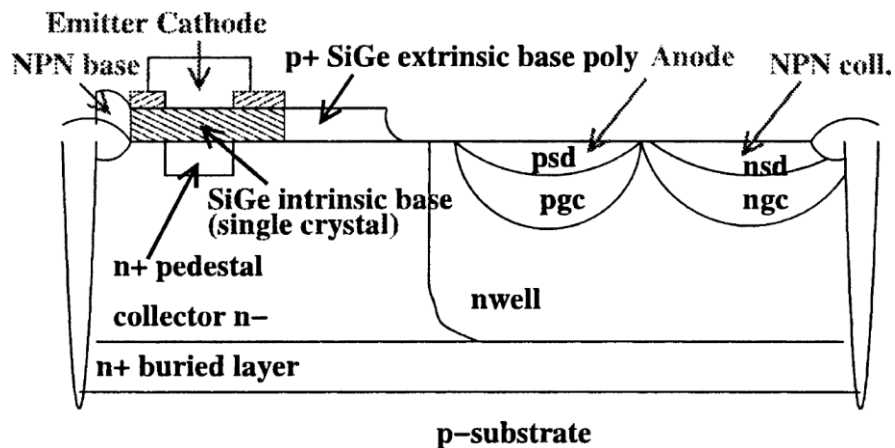
Figure 1.10 Externally-triggered ESD clamp in GaAs pHEMT process

Silicon controlled rectifier (SCR) in Figure 1.11 is another ESD protection device. When SCR is turned on, both parasitic PNP transistor and NPN transistor conduct due to its double injection modulation effect. SCR has much higher current handling ability than any other ESD devices, which makes it a great candidate of ESD devices. However, there are several disadvantages of using SCR as ESD protection devices: (1) SCR is not possible to be fabricated in GaAs pHEMT process because only N-type is available in

such a process. (2) larger trigger voltage (3) small holding voltage and latchup risk (4) slow turn-on speed with large overshoot voltage. Both lateral SCR (see Figure 1.11(a)) in CMOS process and vertical SCR (see Figure 1.11 (b)) in SiGe BiCMOS process are provided here. Vertical SCR is considered to have faster turn-on speed due to high efficiency (high-Beta) of vertical NPN heterojunction transistor, and it will be further optimized in o in SiGe BiCMOS process.



(a)

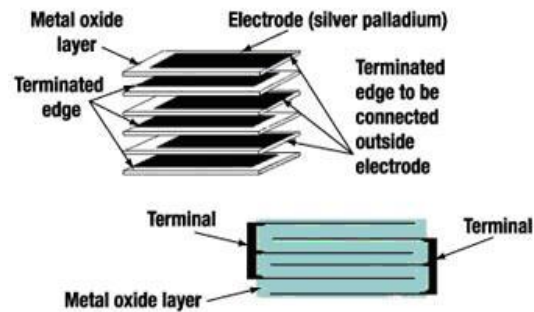


(b)

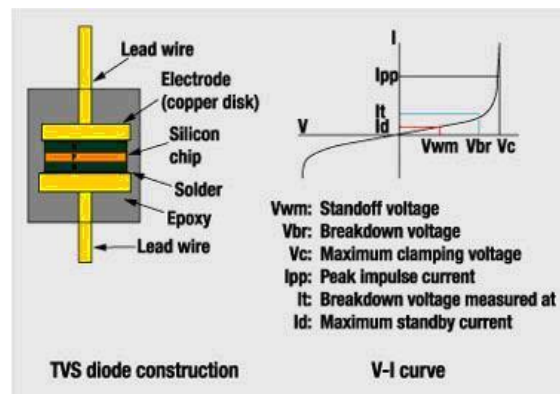
Figure 1.11 Cross section of (a) Lateral SCR in CMOS process (b) Vertical SCR in SiGe BiCMOS process

1.3 Off-Chip ESD Protection Strategy

In addition to the on-chip ESD protection method discussed in the above section, the protection method could also be realized by connecting off-chip ESD protection cells with to-be-protected ICs on PCB board level. For today's electronic products, both on-chip and off-chip ESD protections are required to satisfy the application requirements. There are mainly three reasons why off-chip is necessary: (1) Nowadays, on-chip ESD protection is often sacrificed in favor of chip performance. According to ESD Association, tomorrow's ICs will not need to maintain existing 2-kV HBM protection level. And a proposal has been discussed to lower on-chip ESD target by more than half. To the view of system level, since on-chip ESD protection is reduced, more off-chip ESD is needed to guarantee the overall ESD level. (2) In future high speed / high frequency application, a mix of off-chip and on-chip might be important to reduce the capacitance loading effect caused by ESD protection devices. (3) In several present and future technologies, on-chip ESD protection is not quite possible due to the material perspective such as magnetic recording devices such as magneto-resistor (MR) heads and giant magneto-resistor (GMR) heads. Figure 1.12 presents the two main off-chip ESD protection devices: Multi-Layer Varistor (MLV) and Transient Voltage Suppressor (TVS).



(a)



(b)

Figure 1.12 Off-Chip ESD protection structures (a) Multi-Layer Varistor (MLV) (b) Transient Voltage Suppressor (TVS)

1.4 Summary

As semiconductor fabrication technology continues to advance, ESD induced reliability issue is becoming more and more challenging due to the shrink of device size, and lower breakdown voltage. In order to reduce IC failure caused by ESD damage, on-chip ESD protection devices are widely used to discharge ESD current and limit the overstress voltage under different ESD events. There are only a few ESD protection devices available for RF ICs, and RF ESD design is more challenging than traditional

low speed CMOS ESD protection design. This chapter introduces ESD phenomena fundamentals, ESD models, ESD test methods and different types of ESD device's characteristics. And also, we introduced three on-chip ESD protection devices available in existing literature: (1) diode and diode chain (2) externally triggered ESD clamp (3) SCR. Finally, off-chip ESD protection is also briefly introduced.

CHAPTER 2 UNDERSTANDING OF GAAS PHEMT OPERATION UNDER ESD EVENTS USING TECHNOLOGY COMPUTER AIDED DESIGN (TCAD) SIMULATION

2.1 Introduction of Technology Computer Aided Design (TCAD)

Technology computer aided design (TCAD) simulation tool has been serviced in development of semiconductor devices for over 30 years. The history of commercial TCAD began with the formation of the company Technology Modeling Associates (TMA) in 1979. The software was a result of research performed at Stanford University. The Stanford TCAD software programs were evolved into a 2-D process simulator called “SUPREM4”. Then, TMA's versions of these programs were developed into “TSUPREM4” and “MEDICI”. Silvaco later licensed these programs from Stanford University too and offered a commercial alternative (ATHENA and ATLAS. The third major TCAD vendor was integrated Systems Engineering (ISE). Their equivalent product offerings were DIOS and DESSIS. Finally, Synopsys acquired TMA (Avanti) and ISE and dominates more than 80% of the market share using its TCAD simulation tool called “Sentaurus TCAD”

Typically, TCAD tool consists of process simulator and device simulator. Process simulator calculates the device structure based on given fabrication steps (e.g. lithography, Ion Implantation, Temperature). Then the simulated device structure will be input to device simulator to generate mesh and solve a set of fundamental semiconductor equations for every grid point. These equations include Poisson's equation, continuity equations. Figure 2.1 shows the TCAD simulation framework of

Sentaurus TCAD. The process simulation was performed in TS4 and then imported into Sentaurus Device to do mesh and device simulation.

As a device-level physics-based simulation tool, TCAD is more advantageous over circuit-level simulator (e.g. SPICE) when analyzing ESD device. The reason is that ESD device will need to operate under high-current/-voltage condition when discharging ESD current. Accordingly, the simulation tool must be able to calculate ESD device's operation under such high-current/-voltage condition. However, the models used in SPICE are typically unable to support such condition. On the contrast, TCAD simulation can calculate device's behavior under any high-current/voltage condition, because TCAD simulation is based on fundamental semiconductor equations not on mathematic fitting as SPICE. In a word, TCAD simulation is more favorable for ESD device simulation because it is a more "physics-based" simulator.

It is worthy to note that we don't necessarily need the I-V curve simulated from TCAD simulation is exactly fitted with the measured I-V curves when analyzing ESD devices. In most case, we only anticipate to gain the physical understanding of device inside, such as impact ionization, mobility and so on. To understand those, we only want to get the correct tendency matching between TCAD simulation and measurement results. This requirement looks "loosened", but it is the only feasible goal when we are not able to get the detailed fabrication condition of a specific process. This chapter will give an example of using TCAD simulation to analyze ESD device in GaAs pHEMT process.

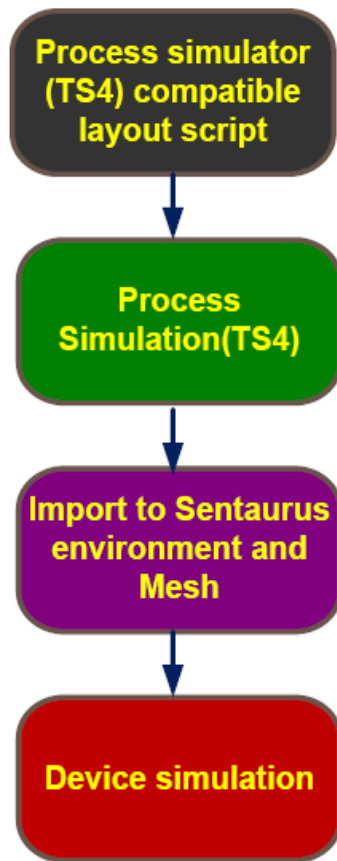


Figure 2.1 TCAD simulation framework in Sentaurus

2.2 “TLP-like” Simulation Setup

Figure 2.2 (a) shows the setup of Barth 4002 TLP measurement system, which generates human body model-like pulses with a 100-nsec pulse width and 10-nsec rise time. Figure 2.2 (b) is the existing DC-like simulation setup using Sentaurus TCAD. Figure 2.2 (c) shows the proposed TLP-like simulation setup. The $50\text{-}\Omega$ resistor R_d is to imitate $50\text{-}\Omega$ characteristic impedance of Barth 4002 TLP system.

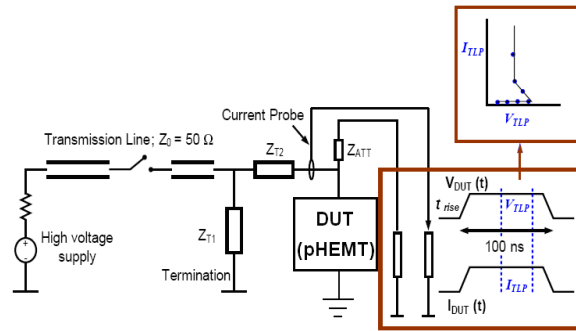
Technically, DC-like simulation setup is used to analyze ESD device's performance. In DC-like simulation setup, ramped voltages are directly applied to terminals of ESD devices, and the lattice temperature module is turned off. This simulation setup takes less time and is accurate enough when device is under low-power condition. However, DC-like simulation setups has 2 inherent disadvantages:

- i. DC-like simulation can not simulate the dynamic time effects. While dynamic times effects are important for both TLP measurement and real-world ESD events. For instance, DC-like simulation can never reflect TLP pulse width/rise time's impact on the simulation result, although the rise time is reported to be important to ESD device's triggering mechanism.
- ii. DC-like simulation can not easily integrate temperature effect, because temperature simulation is strongly related to dynamic time effect. As well known, generated or dissipated heat, which is time-dependent, directly affects the temperature simulation.

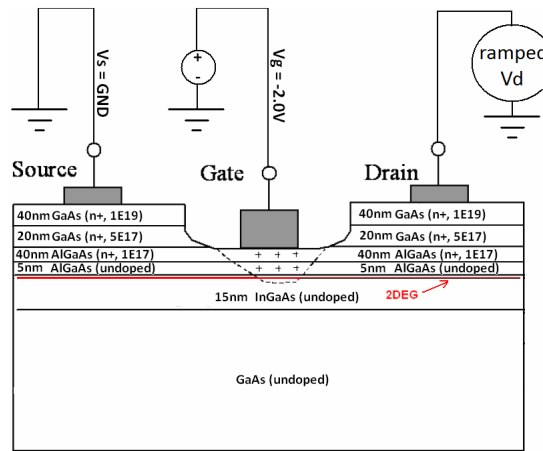
The 2 disadvantages of DC-like simulation hurt the simulation accuracy, because both TLP measurement and real-world ESD event are affected by dynamic time effect and temperature effect. TLP-like simulation setup is proposed in this paper to overcome this problem. Respectively, it has 2 essential advantages over DC-like simulation:

- i. TLP-like simulation setup simulates TLP pulses directly, and the dynamic time effect has been reflected.
- ii. TLP-like simulation setup can integrate temperature effect in the simulation.

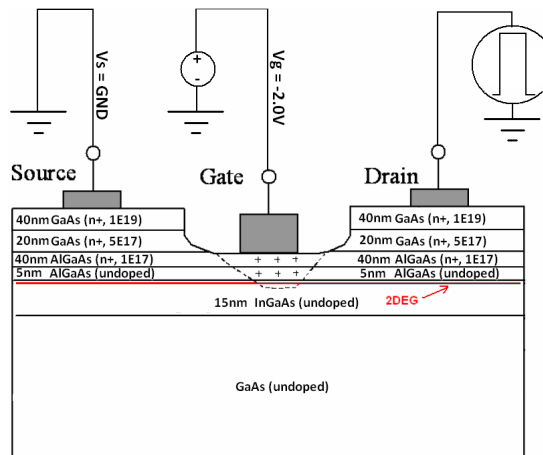
Although the TLP-like simulation setup is not perfect to include the transmission line model in Barth 4002 TLP system, this setup is good enough for ESD application. Therefore, we will perform TLP-like simulation to analyze pHEMT ESD clamps. Figure 2.3 shows the simulated voltages/currents vs. time waveforms of the pHEMT and the data extraction method. We can clearly see that, after the trigger point, the voltage waveform decreases, which is consistent with the TLP measurement results. And the data in TLP I-V curves is derived by averaging the voltages and currents in a time window between 70%~90% of the transient waveform. This time window is exactly the same as the TLP measurement setup.



(a)



(b)



(c)

Figure 2.2 (a) Measurement setup using Barth 4002 TLP (b) DC-like simulation setup (c) TLP-like simulation setup

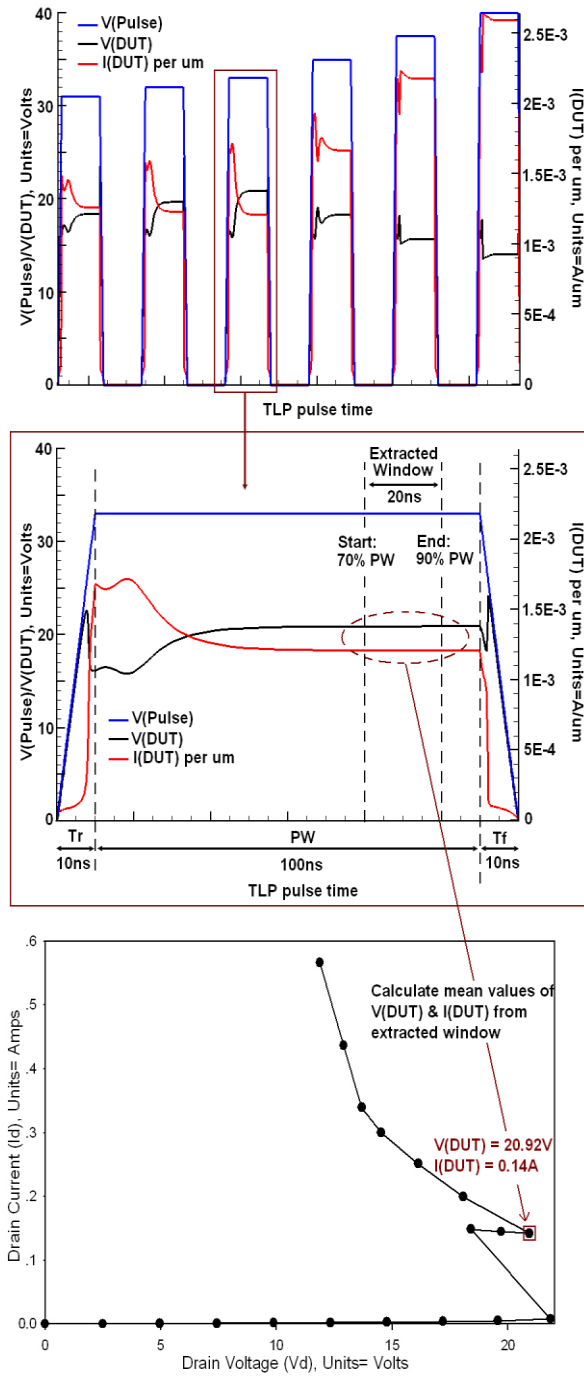
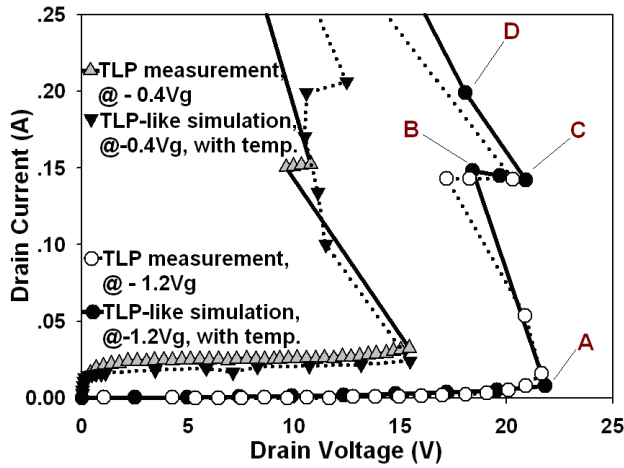


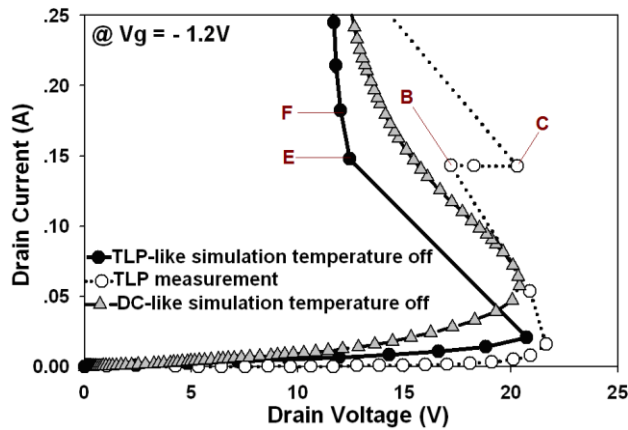
Figure 2.3 Data extraction method of TLP-like simulation

With TLP-like TCAD simulation setup, Figure 2.4 (a) compares the TLP I-V curves of the PHEMT under different gate biases conditions in simulation and measurements.

Both measurement data and TLP-like simulations which include thermal effect are depicted. Good agreement is found between simulation and data. Snapback (points A to B) and post-snapback saturation (points B to C) behaviors are clearly illustrated. It should be noted that the device failed beyond point C. In contrast, the DC-like simulation in Figure 2.4 (b) predicts no post-snapback saturation due to its inability to incorporate temperature induced effects in the high current transient ESD regime. Figure 2.4 (b) further demonstrates that without including the temperature effect, the TLP-like simulation is quite accurate in the pre-snapback region but inaccurate in the post-snapback operation.



(a)



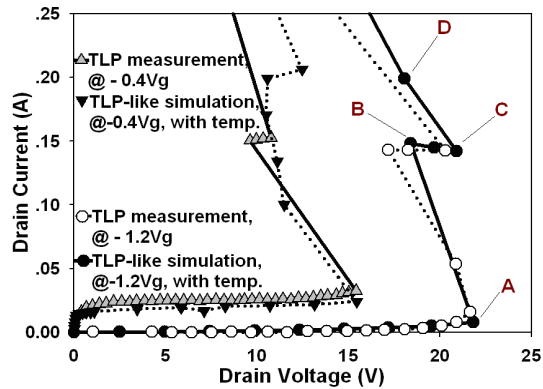
(b)

Figure 2.4 (a) Comparison of the measured and TLP-like simulated I-V curves, with the snapback (points A to B) and post-snapback saturation (points B to C) indicated. In both measurement and TLP-like simulation, square pulses with a 10 ns rise time and 100 ns pulse width were applied. (b) Comparison of PHEMT's I-V curves obtained from TLP measurement, DC-like simulation, and TLP-like simulation without including the electro-thermal simulation module.

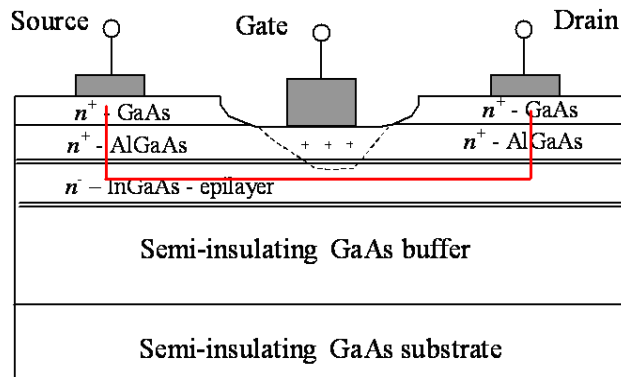
2.3 Snapback Behavior

Snapback is an I-V phenomenon that the device voltage decreases as device current increases. Snapback is widely seen in ESD devices. For example, the snapback in Silicon

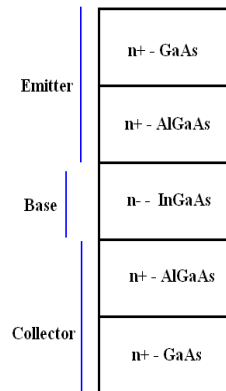
MOS devices subjected to an ESD stress is attributed to the parasitic bipolar transistor. Similarly, snapback behavior is also found in pHEMT-based ESD clamps (see Figure 2.5 (a)). The traditional bipolar-based snapback rationale in Silicon CMOS process cannot directly apply to the pHEMT because of the absence of a physical parasitic BJT imbedded in the pHEMT. However, we will prove that there is a parasitic virtual bipolar transistor under high ESD stress. Figure 2.5 (b) and (c) show the device cross section view and equivalent BJT-like structure along current path. The virtual p-type BJT base is formed by the generated holes from heavy impact ionization.



(a)



(b)



(c)

Figure 2.5 Snapback mechanism of 0.5um depletion mode pHEMT (a) Comparison of the measured and TLP-like simulated I-V curves (b) device cross section and current path (c) equivalent BJT-like structure

When the PHEMT is subject to a TLP pulse, the holes and electrons generated by the impact ionization are driven towards the source and drain, respectively, as a result of the lateral electric field due to the elevated drain voltage. Figure 2.6 shows that the TLP-like simulated hole density near the AlGaAs/InGaAs interface under the gate increases significantly in the post snapback regime (from A to B). This in turn forms a virtual base region for the parasitic BJT. As the hole density in this base region increases, the potential in the InGaAs layer rises. This lowers the potential barrier to the electrons in the AlGaAs layer, as demonstrated in Figure 2.6 by the conduction band energies on the source side before and after snapback. This allows the injection of holes from the InGaAs base to the AlGaAs emitter, and a large number of electrons injected in the opposite direction. The virtual bipolar current conduction reduces the voltage between the drain and source, resulting in the observed snapback behavior.

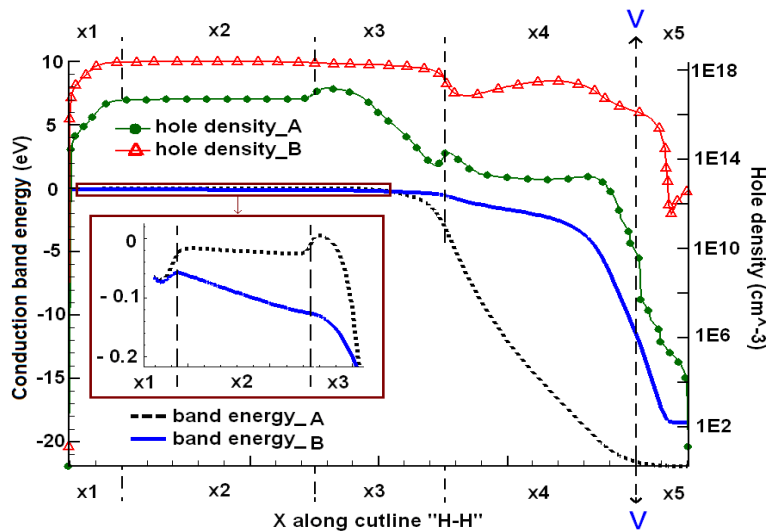
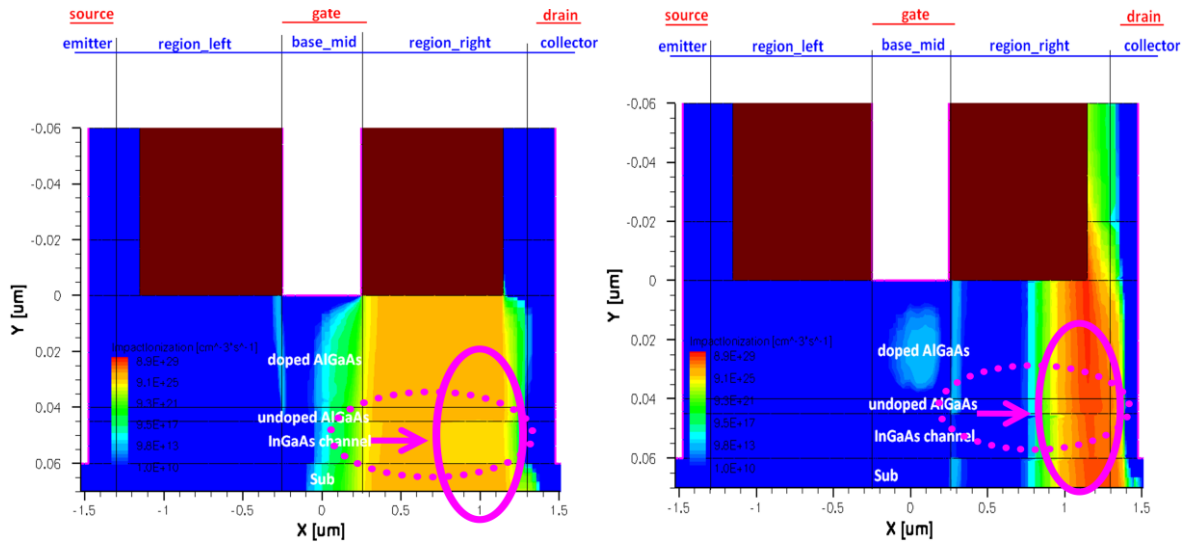
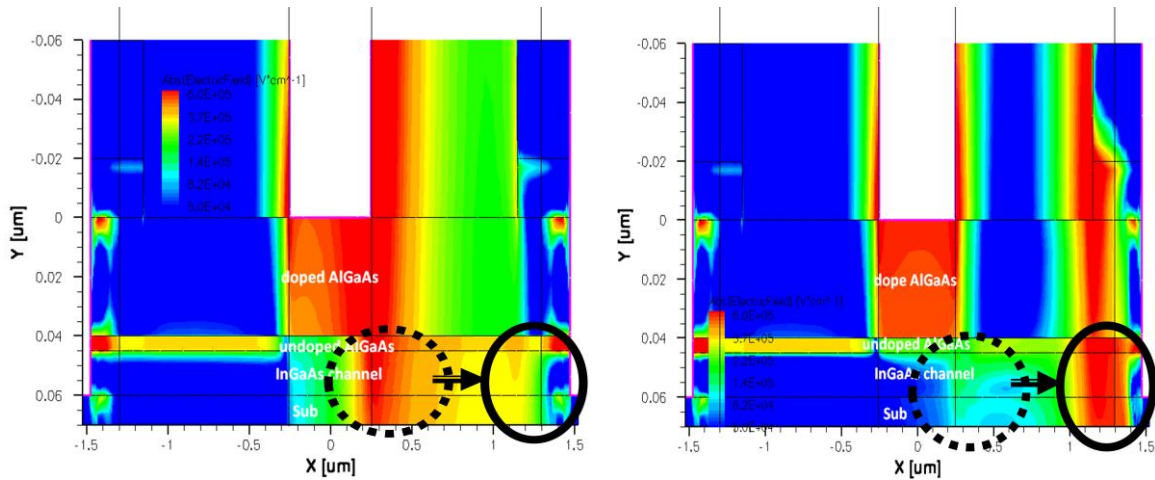


Figure 2.6 Simulated hole densities and conduction band energies along the horizontal line (H-H) at onset of snapback (“A”) and post snapback (“B”). The insert is the zoom-in of the band energies in regions x1, x2, and x3.

To provide better insights, Figure 2.7 shows the simulated impact ionization rate and electric field in the pHEMT at snapback onset point and post snapback point. Both high impact ionization region and high electric field is shifted away from virtual BJT's base/collector junction region towards collector region as current increases. This further verifies the virtual bipolar effect. This is analogous to the kirk effect phenomenon in bipolar devices.



(a)



(b)

Figure 2.7 Kirk effect found in pHEMT device under TLP-like ESD stress (a) Impact ionization region shift from point “A” to point “B” (b) Electric field region shift from point “A” to point “B”

2.4 Post-snapback Saturation Behavior

Beyond snapback, there is a unique current saturation region observed prior to failure (see Figure 2.8 (a)). This region is named post-snapback saturation region in

order to make it different to the saturation in traditional region. It will be proved that post-snapback saturation is caused by “temperature-induced velocity saturation”. Diagram flow for this hypothesis is shown in Figure 2.8 (b). As well known, electron current density is proportional to the product of “electron mobility” “electric field” and “electron density”. ($J_n = q * \mu * E * n$). So, whether post-snapback saturation exists depends on calculated values of “electron mobility”, “electric field” and “electron density” in TCAD simulation.

In Figure 2.8 (b), lattice temperature module is turned off. Therefore, increase of power density can not raise the lattice temperature during TCAD simulation. We select 2 points (point “E” and “F”) from simulated I-V curve without temperature effect in Figure 2.4 (b). Physical process from point “E” to “F” is:

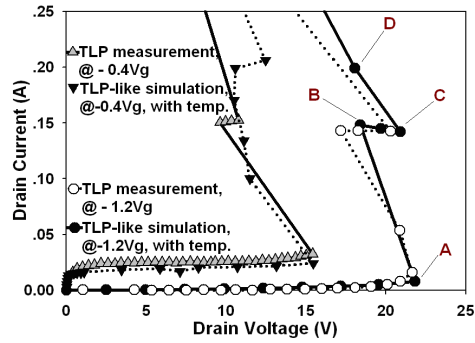
- i. Electric field increases heavily. Because increased TLP-like voltage stress raises pHEMT’s voltage “Vd” and current “Id” heavily.
- ii. Electron mobility decreases as the electric field increases, which is consistent with traditional theory.
- iii. Electron density is nearly the same because the fact that almost all the electrons have been depleted.
- iv. Since electron current density equals the product of “electric field”, “electron mobility” and “electron density”, we can not see “second saturation” if temperature module is turned off.

In Figure 2.8 (c), lattice temperature module is turned on, thus increase of power density surely raises the lattice temperature during TCAD simulation. Similarly, we also

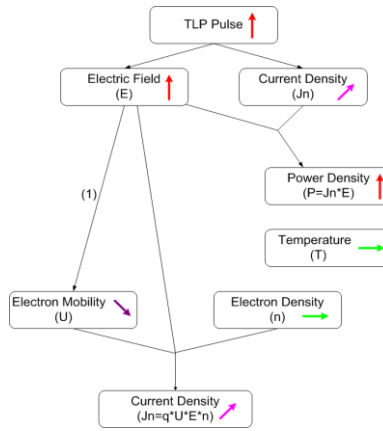
select 2 points (point “B” and “C”) from simulated I-V curve with temperature module in

Figure 2.4 (a). Physical process from point “B” to “C” is:

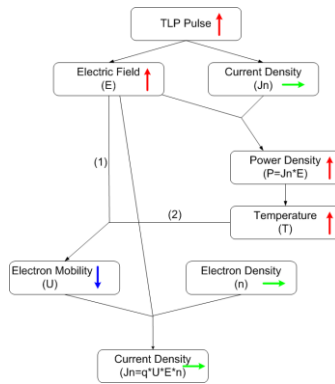
- i. Electric field increases heavily. Because increased TLP-like voltage stress raises pHEMT’s voltage “ V_d ” and current “ I_d ” heavily.
- ii. Electron mobility decreases heavily because of 2 reasons: increased electric field and increased lattice temperature. Mobility here drops more heavily.
- iii. Electron density is nearly the same because the fact that almost all the electrons have been depleted.
- iv. As a result, since electron current density equals the product of “electric field”, “electron mobility” and “electron density”, we can anticipate “second saturation” if temperature module is turned on.



(a)



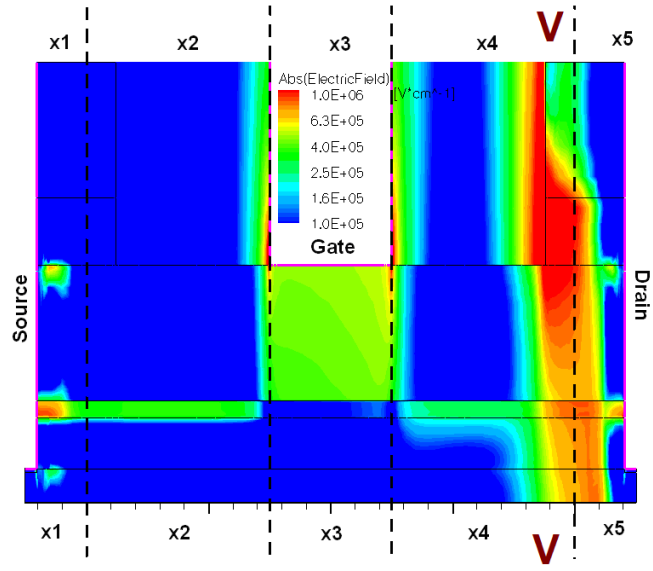
(b)



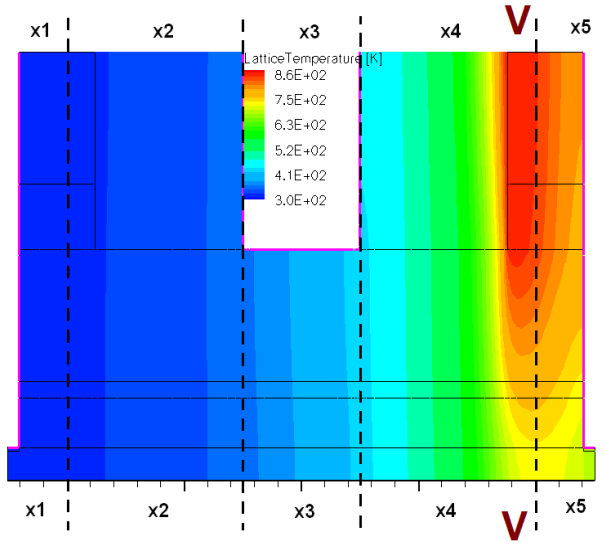
(c)

Figure 2.8 Post snapback saturation mechanism of 0.5um depletion mode pHEMT (a) Comparison of the measured and TLP-like simulated I-V curves (b) explanation of TCAD calculation with lattice temperature module "OFF" (c) explanation of TCAD calculation with lattice temperature module "ON"

Figure 2.9 shows electric field contour and lattice temperature contour in post-snapback saturation region. In the marked region, electric field and lattice temperature is high. Electron velocity is found to saturate in this region. Therefore, we selected a vertical cutline “V-V” in this marked region, and simulated the average electric field (E), average electron mobility (μ), average electron density (n) and average electron current density (Jn) along cutline “V-V”. Electron mobility is plotted in Figure 2.10. Here, electron mobility is found to decrease with the increase of temperature and electric field. With temperature module turned on in simulation, mobility decreases more dramatically.

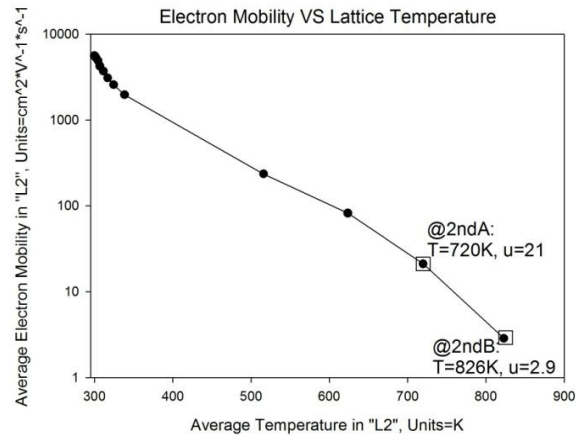


(a)

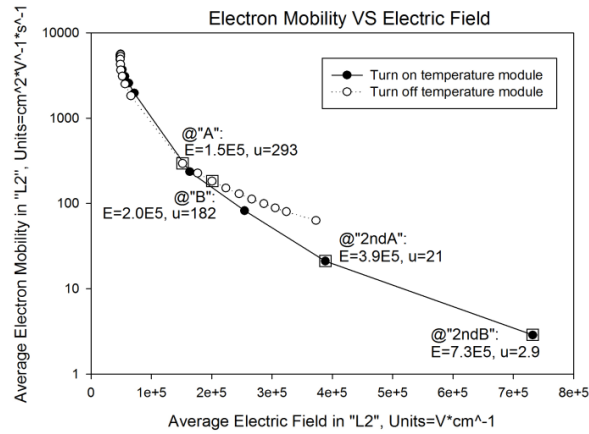


(b)

Figure 2.9 TCAD Simulated (a) electric field (b) temperature contour in post-snapback saturation region



(a)



(b)

Figure 2.10 Simulated mobility degradation (a) with temperature increased (b) with electric field increased

Table 2.1 further lists the simulated parameters of PHEMT, which were obtained by averaging the data along the V-V line near the drain junction of the PHEMT device (Figure 2.9) at points A, B, C, and D in Figure 2.8 (a). Note that prior to the virtual BJT formation, at point A the drift current accounts for over 90% of the total current, which indicates FET action. After the virtual BJT turns on at point B, the diffusion current accounts for over 75% of total current, which indicates the existence of BJT action. From

points B to C, the electron and hole densities remain constant, the electric field continues to increase with the increase in drain voltage, but this is offset by the decrease in the mobility due to increasing temperature (Table 2.1). Because of this electrical-thermal interacting effect, the diffusion current also saturates. This is the result of electron and hole densities being constant, as the effects of temperature increase and mobility decrease offset each other. Saturation of both the drift and diffusion currents makes the total current constant.

Table 2.1 Simulated PHEMT parameters at points A, B, C, and D, where $|E|$ is the electric field, J_n and J_p are the electron and hole current densities, n and p are the electron and hole densities, and μ_n and μ_p are the electron and hole mobility.

Parameter	A	B	C	D
Temp (K)	317	787	826	908
$ E $ (V/cm)	7.2E4	5.3E5	8.0E5	7.8E5
J_n (A/cm ²)	4.23E4	5.92E5	5.78E5	6.76E5
J_{n_diffu} (A/cm ²)	2.82E3	5.36E5	5.36E5	4.79E5
J_{n_drift} (A/cm ²)	3.95E4	4.23E4	4.23E4	1.94E5
μ_n (cm ² /(V·s))	2.7E3	8.33	2.38	1.89
n (cm ⁻³)	3.53E18	3.22E18	3.27E18	4.03E18
J_p (A/cm ²)	1.07E3	1.13E5	1.13E5	2.28E5
J_{p_diffu} (A/cm ²)	56.4	2.82E3	5.64E3	1.16E5
J_{p_drift} (A/cm ²)	1.01E3	1.10E5	1.07E5	1.12E5
μ_p (cm ² /(V·s))	2.0E3	41.0	36.1	31.6
p (cm ⁻³)	3.64E8	1.13E16	1.14E16	2.38E16
J_{total} (A/cm ²)	4.34E4	7.05E5	6.91E5	9.04E5

2.5 Thermal Failure Behavior

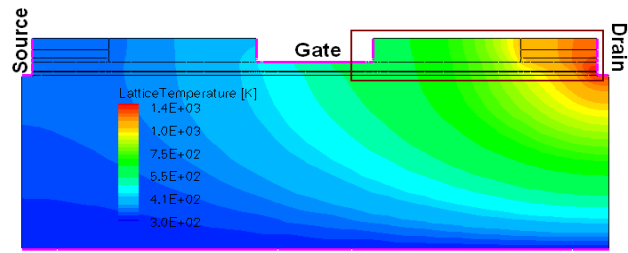
See Figure 2.4 (a), from points C to D, the decrease of the voltage drop and the increase of current in simulation are due to significant conductivity modulation. At the same time, the device has entered the intrinsic generation region due to the very high temperature, where increase of both electron and hole densities is considerable and uncontrollable. This is an unstable region leading to a catastrophic hot spot and device failure. In measurements, there is no point D, as the PHEMT fails immediately after point C. The failure can be correlated to TLP measurements which also indicate an irreversible damage after the post-snapback saturation. We will prove the thermal failure behavior using TCAD simulation and scanning electron microscope (SEM) failure analysis.

pHEMT has complex layers, each layer has different melting point. (see Table 2.2) In order to find the hot spot location, we set failure criteria in TCAD simulation using melting point as the limitation point. If temperature in any material layers of pHEMT exceeds the melting point, simulation stops and hot spot location is reported.

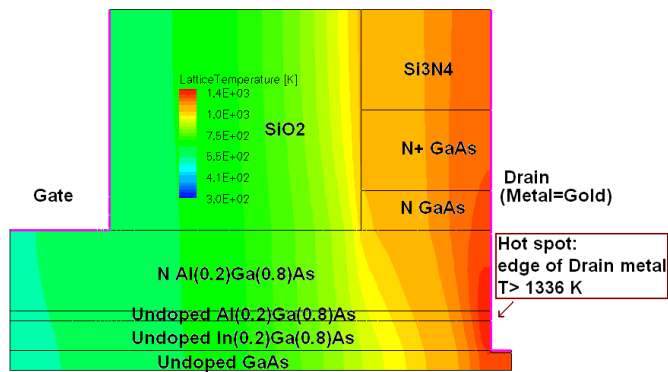
Table 2.2 Melting temperatures in pHEMT

Materials in pHEMT	Melting Point (K)
GaAs	1511
SiO ₂	1873
Si ₃ N ₄	2173
AlGaAs	1523
InGaAs	1373
Gold (Drain Metal)	1336

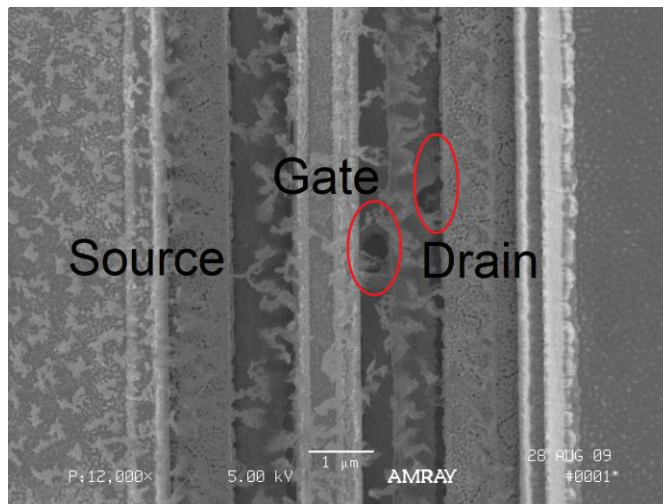
In Figure 2.11 (a) and (b), we plot the temperature contour at point “D” indicated in Figure 2.4 (a). And also hot spot is targeted by SEM in Figure 2.11 (c). Simulation result and FA result correlate each other well. We can see that hot spot is located on the edge of “Drain” metal (Gold). Temperature of the interface of gold and pHEMT device exceeds gold’s melting point 1336K first. Since melting points of gold and InGaAs layer are almost the same. In practice, damage may happen in both materials together.



(a)



(b)



(c)

Figure 2.11 Hot spot in TLP-like simulation (a) Zoom out (b)(c) zoom in (c) Failure analysis using SEM

2.6 Summary

In this chapter, thorough understanding of pHEMT's snapback, post-snapback saturation and thermal failure has been explained via TLP-like numerical simulation, TLP system and SEM inspection. Snapback was found resulted from the virtual parasitic bipolar transistor formed due to the large number of electrons and holes generated near the drain region by impact ionization. Post-snapback saturation was caused by the significant electrical-thermal interaction in the III-V compound semiconductor due to the material's poor thermal conductivity. Thermal failure is caused by hot spot located in pHEMT's InGaAs channel. Understanding these physical mechanisms is critical to the design of ESD protection solutions in GaAs- and GaN-based PHEMT technologies.

CHAPTER 3 DESIGN AND OPTIMIZATION OF ESD PROTECTION DEVICES FOR GAAS PHEMT PROCESS

3.1 Introduction and Prior Arts

Electrostatic discharge (ESD) induced failure is a major concern for the pseudomorphic high electron mobility transistor (pHEMT) based integrated circuits [13, 14]. This reliability issue is further worsened by the inherent low thermal conductivity of compound materials like GaAs and AlGaAs. Nowadays, there has been a growing demand for the availability of robust ESD protection solutions for radio frequency integrated circuits (RFIC's) fabricated in the pHEMT process. Typically, stacked schottky diodes are used as ESD protection in GaAs pHEMT process. However, this approach could consume a huge layout area and has poor leakage current as well as large on-state resistance. Therefore, ESD shunting apparatus with external trigger unit was proposed as an effective protection scheme in GaAs pHEMT process (see Figure 3.1). Single-gate pHEMT clamps are recently used for developing pHEMT-based ESD protection structures [15], but the current conducting capability of such a device is quite limited due to the self-heating and current saturation mechanisms [16].

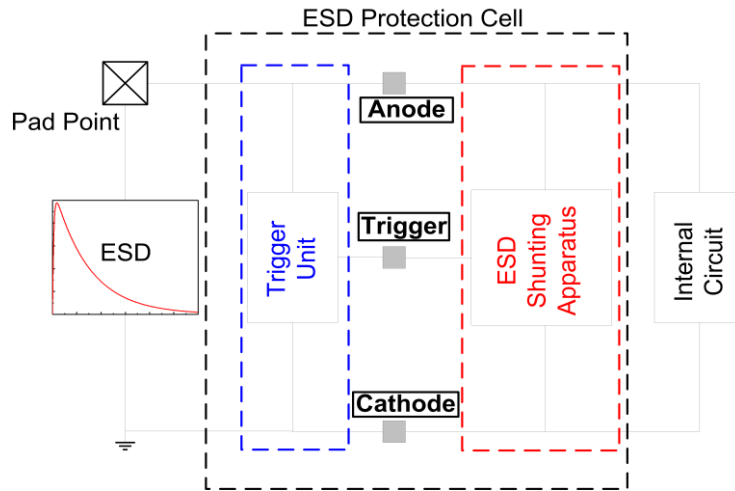


Figure 3.1 ESD protection structure with trigger unit in pHEMT process

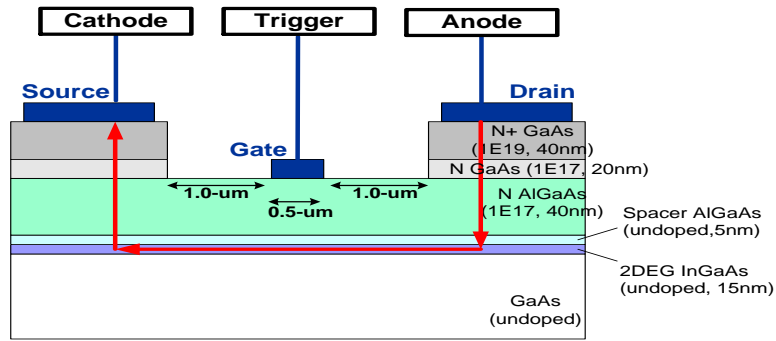
3.2 A Novel Enhancement-Mode Dual-gate ESD Protection Design

This section reports a new multi-gate pHEMT which can be used as an effective device in protecting GaAs-based IC's against ESD threats. With approximately the same layout area and parasitic capacitance, the proposed ESD protection device can carry a current three times higher than the conventional single-gate pHEMT device. Moreover, the new device possesses a very low on-state resistance, fast turn-on speed, low parasitic capacitance normalized to failure current, and flexibility to adjust the trigger voltage for fulfilling different ESD protection design requirements.

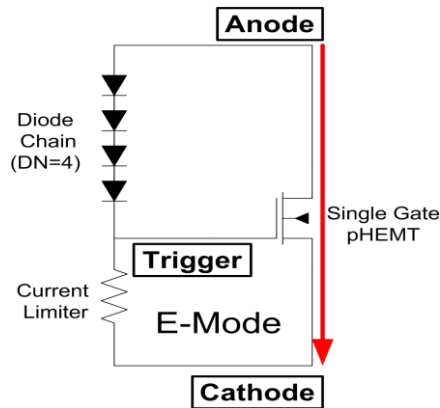
3.2.1 Device Structure

Figure 3.2 (a) and (b) show the cross section view of a conventional enhancement-mode, single-gate, GaAs pHEMT and schematic of ESD clamp built based on such a device, respectively. The ESD clamp consists of a diode chain and a resistor (i.e., current limiter) to control the triggering of the pHEMT. Under the normal operation condition,

the diode chain (see Figure 3.2 (b)) is not turned on, potential at the trigger terminal is low, pHEMT is off, and current flow between the anode and cathode is negligibly small. Under the ESD condition, a stress voltage at the anode larger than the blocking voltage of the diode string first turns on the diodes and then forces a current through the resistor. This raises the potential at the trigger terminal, reduces the depletion region underneath the gate, exposes the 2DEG, and consequently allows for ESD current discharge between the anode and cathode via the 2DEG channel (indicated by the red line in Figure 3.2). Such an ESD clamp is considered a better protection design than the Schottky diode-based clamp [15, 17], but its robustness is still relatively poor due to the fact that there is only one current path (via the 2DEG channel) in the single-gate pHEMT.



(a)

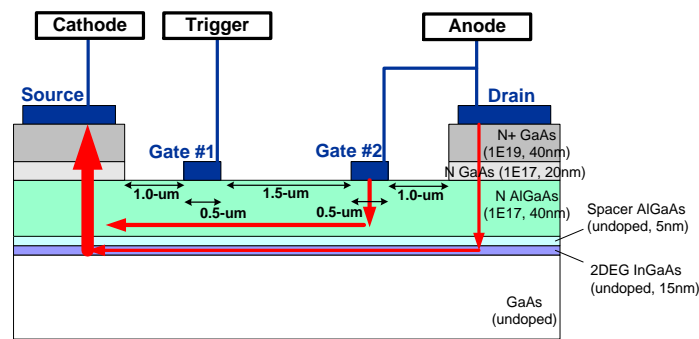


(b)

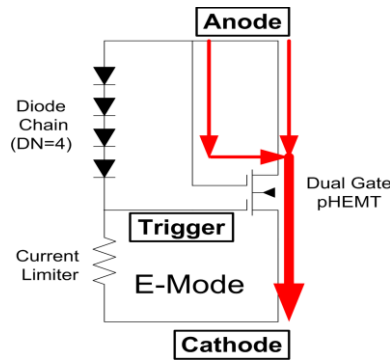
Figure 3.2 (a) Cross section view of single-gate pHEMT with the red line denotes the current path, and (b) ESD clamp built using the single-gate pHEMT and diode chain

Figure 3.3 (a) and (b) show the cross section view of the proposed enhancement-mode, dual-gate, GaAs pHEMT and schematic of its ESD clamp, respectively. Gate #1 in the dual-gate pHEMT is the same as the gate in the single-gate pHEMT. The new feature in this device is a second gate Gate #2 connected to the anode (Figure 3.3 (a)). A similar concept was reported by Lin et al. [7] aiming at reducing pHEMT's parasitic capacitance. Our work below will show that the intrinsic advantages of such a device are actually the relatively high failure current and low on-state resistance, rather than the small capacitance. Under a sufficiently large ESD stress voltage, the Schottky junction

underneath Gate #2 will conduct. This forms a second current discharge path from Gate #2 through the AlGaAs layer to the source (see Figure 3.3 (b)), in addition to the 2DEG current path created by Gate #1. The added current path reduces the on-state resistance and increases the robustness of the dual-gate ESD clamp. More detailed explanations for the mechanisms of two current conducting paths will be given in the next section.



(a)



(b)

Figure 3.3 (a) Cross section view of proposed dual-gate pHEMT with the two red lines denote the two current paths, and (b) ESD clamp built using the dual-gate pHEMT and diode chain

3.2.2 Measurements and Discussion

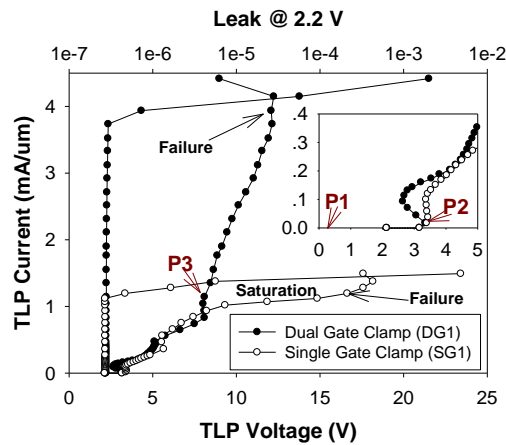
Single- and dual-gate pHEMT clamps were fabricated in a 0.5-um pHEMT process at WIN Semiconductor. A triggering unit consisting of 4-diode chain and a current

limiter was incorporated in both clamps. Diode area was $62 \times 53 \text{ } \mu\text{m}^2$, the current limiter resistor area was $40 \times 20 \text{ } \mu\text{m}^2$, and the single- and dual-gate pHEMT each had 20 fingers and areas of $116 \times 106 \text{ } \mu\text{m}^2$ and $135 \times 106 \text{ } \mu\text{m}^2$, respectively. For the GaAs technology used, the smallest size available for the dual-gate device was $24 \times 3 \text{ } \mu\text{m}^2$.

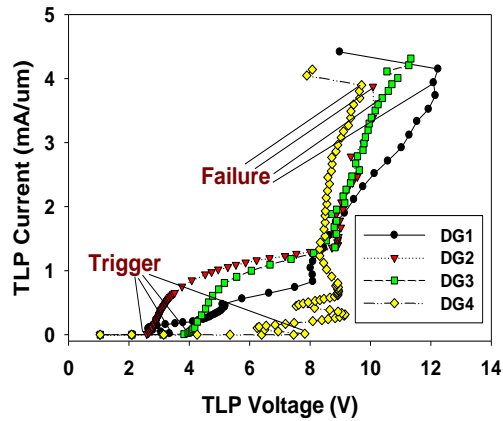
ESD measurements were carried out using the Barth 4002 transmission line pulse (TLP) tester which generates HBM-like pulses having a 10 ns rise time and 100 ns width. Post-stress leakage current was measured at a voltage of 2.2 V. This voltage is the pHEMT normal operating voltage of 2.0 V, plus 10% dynamic voltage margin. In addition, the Hanwa HED-W5000M on-wafer HBM tester was used to accurately assess the ESD clamps' robustness.

Figure 3.4 (a) compares the TLP current density (current per width, y-axis) vs. voltage (bottom x-axis) and leakage current (top x-axis) curves of the single- and dual-gate ESD clamps. Clearly, the dual-gate clamp possesses a smaller on-state resistance and higher failure current than its single-gate counterpart. The failure current densities (failure current I_{t2} per width) of the single- and dual-gate devices are $1.15 \text{ mA}/\mu\text{m}$ and $3.8 \text{ mA}/\mu\text{m}$, respectively. The insert in Figure 3.4 (a) shows the TLP I-V curves near the triggering point. Note that the trigger voltage depends on the number of diodes in the diode chain, and this voltage can be adjusted by altering diode number and diode polarity. The trigger voltage of about 3.2 V observed in Figure 3.4 (a) resulted from the use of a 4-diode string. It is noticed that the resistance of both single-gate and dual-gate clamps changes at around 5 V. This can be attributed to a positive feedback due to the electron-hole pair generation near the drain junction and the turn-on of embedded

parasitic lateral bipolar transistor (BJT) [16]. Figure 3.4 (b) shows the TLP I-V characteristics of DG pHEMT's having 4 different diode strings. While the trigger voltage depends on the diode number, the failure current is insensitive to such a factor. Table 3.1 summarizes the measured trigger voltage as a function of diode number and polarity.



(a)



(b)

Figure 3.4 (a) Current-voltage characteristics (the two curves on the right-hand side) and leakage currents (the two curves on the left-hand side) of single- and dual-gate clamps having a 4-diode string obtained from the TLP tester, and (b) TLP results of DG pHEMT's having different diode number and polarity (see DG1, DG2, DG3, DG4 in Table 3.1)

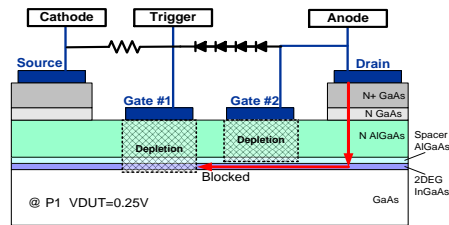
Table 3.1 Trigger Voltage Dependency on Diode Connection for E-mode pHEMT ESD clamp

Dual-gate clamp	Diode Polarity	Diode Number	Trigger Voltage of Single-Gate pHEMT	Trigger Voltage of Dual-Gate pHEMT
DG1	Forward	4	3.2 V	3.2 V
DG2	Forward	3	-	2.5 V
DG3	Forward	5	-	4.1 V
DG4	Reverse	1	7.5 V	7.5 V

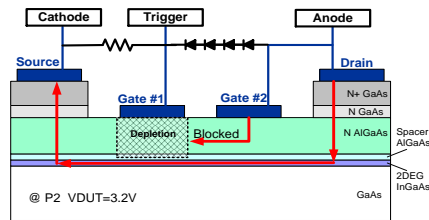
Of another important phenomenon found in Figure 3.4 is that the I-V curves of single- and dual-gate clamps have almost the same slopes when the voltage is less than 8 V. Beyond this, the single gate clamp enters the saturation region caused by temperature induced mobility degradation [16], whereas the dual-gate clamp exhibits a steeper curve stemming from the turn-on of the second current path.

The different current conduction mechanisms can be explained in more details below using physical reasoning and TCAD simulation results. When the stress voltage is equal to the threshold voltage of the pHEMT, 0.25 V, the 2DEG underneath Gate #2 is unblocked but underneath Gate #1 is still obscured by the depletion region because of the blockade of 4-diode chain (see schematic in Figure 3.5 (a) and simulated electron density in Figure 3.6 (a)). The Schottky diode of Gate #2 is also off at this time. When the stress voltage is increased to 3.2 V, the clamp trigger voltage, the Schottky diode begins to turn on but its current path from the Schottky contact to the source via AlGaAs layer is still blocked by the depletion region associated with Gate #1 (see schematic in Figure 3.5 (b) and simulated electron density in Figure 3.6 (b)). The 2DEG underneath Gate #1 is unveiled at this time because the diode chain is conducting. So there is one

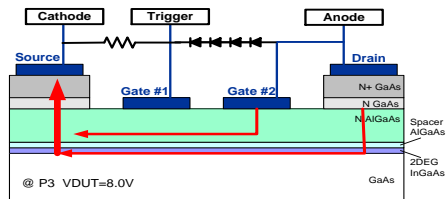
current conducting path between the anode and cathode via the 2DEG channel (see Figure 3.5(b) and Figure 3.6 (b)). As the stress voltage at the anode reaches 8 V, where the slope of I-V curve of DG1 is increased sharply, the depletion region associated with Gate #1 also vanishes, and the second current path associated with the Schottky diode is formed (see Figure 3.5 (c) and Figure 3.6 (c)). As a result, two current conducting paths exist in the dual-gate pHEMT when the stress voltage is larger than 8 V, giving rise to a smaller on-state resistance and larger failure current.



(a)

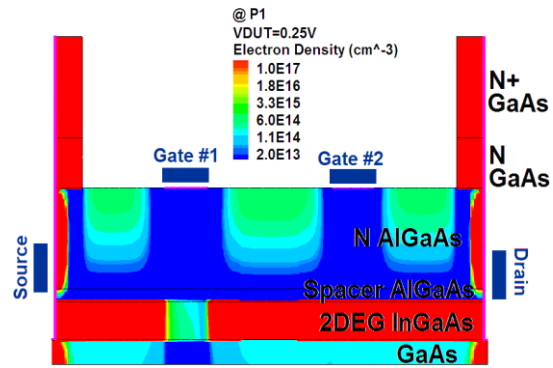


(b)

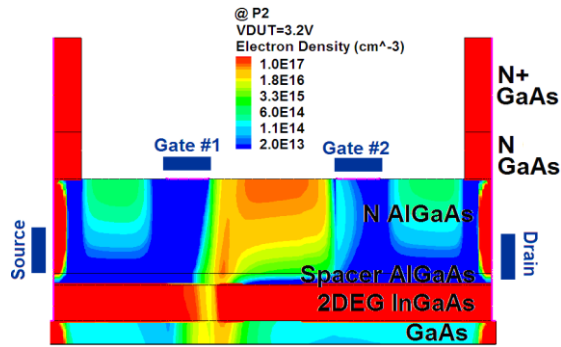


(c)

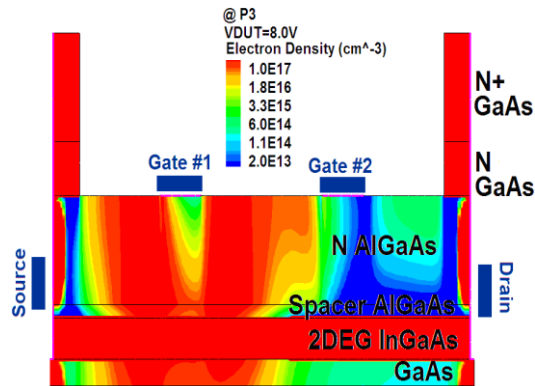
Figure 3.5 Depletion regions and current paths in the dual-gate pHEMT at a stress voltage of (a) 0.25 V and (b) 3.2 V (c) 8.0V



(a)



(b)



(c)

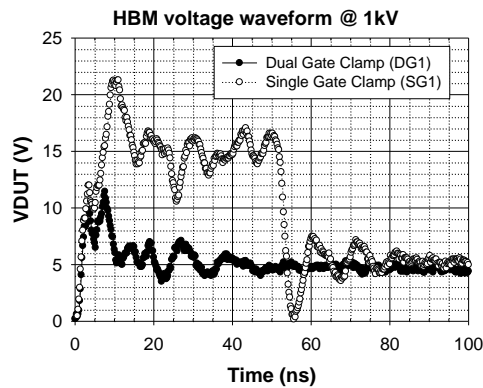
Figure 3.6 Simulated electron densities in the dual-gate pHEMT at a stress voltage of (a) 0.25 V, (b) 3.2 V, and (c) 8.0 V

The robustness of the two ESD clamps was further verified using the Hanwa HED-W5000M on-wafer HBM tester. The single-gate clamp can survive up to a 2 kV HBM zap, whereas the new dual-gate clamp can pass 8 kV HBM zap. These results are consistent with the trend found in Figure 3.4, but they are not exactly equal to the HBM passing voltages obtained by the conventional estimate of multiplying the TLP failure currents to 1,500 ohm human body resistance due to the different setup and calibration issues.

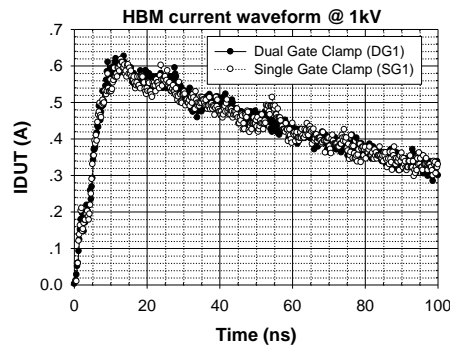
Figure 3.5 presents the voltage/current waveforms of the two clamps zapped at 1 kV obtained from the on-wafer HBM tester. The max clamping voltage of single-gate clamp SG1 is 22 V, which is similar to data reported in [15] for a single-gate pHEMT fabricated in a comparable GaAs technology. The lower max clamping voltage of 12 V of the dual-gate clamp DG1 reduces the likelihood of damages to the core circuit. The reason SG1 has a much higher clamping voltage than DG1 is because SG1 enters the saturation at 8 V while at the same voltage DG1 continues its linear I-V characteristics (see Figure 3.4), thus giving rise to a small voltage drop in DG1.

Another interesting characteristic found in Figure 3.7(a) is that the voltage vs. time waveform of the single-gate clamp SG1 suddenly drops at 55 ns while the dual-gate clamp DG1 does not. This observation can be explained below. As shown in Figure 3.4(a), SG1 enters the current saturation region when the current is higher than about 0.5 mA/um (i.e., equivalent to 0.5 A). The saturation results from the flow of discharging current being limiting to the 2DEG channel and mobility degradation due to thermal effect [4]. Below this current level, SG1 does not saturate and operates in a

region where the clamping voltage drops considerable when the current decreases. This is fairly consistent with the results given in Figure 3.7(b), which show that SG1 carries a current of more than 0.5 A before 55 ns, thus resulting in a large clamping voltage. After 55 ns, the current in SG1 is smaller than 0.5 A and the clamping voltage suddenly drops. For DG1, the saturation region does not exist, and the clamping voltage vs. time waveform is fairly constant (see Figure 3.7(a)). It is worth pointing out that the quasi-static nature of TLP I-V curves in Figure 3.4(a) cannot be used to fully explain the voltage and current transients in Figure 3.7(a) and (b).



(a)

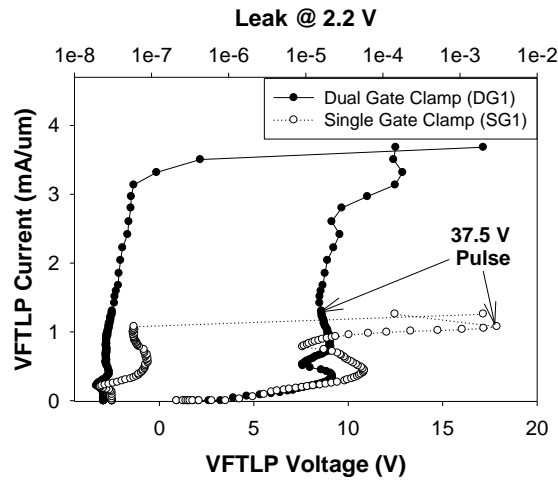


(b)

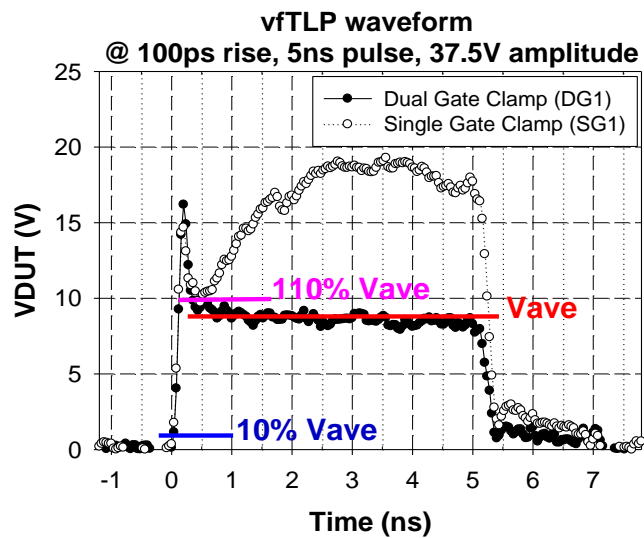
Figure 3.7 (a) Voltage (b) current waveforms of the two clamps subject to 1 kV HBM stress obtained from on-wafer HBM tester

For charged device model (CDM) ESD applications, the ESD protection devices have to be triggered sufficiently fast and possess a relatively low overshoot voltage. To investigate this, the pHEMT clamps were characterized using the Barth 4012 very-fast TLP (VF-TLP) tester which produces very fast and short pulses with a 100 ps rise time and 5 ns pulse width. Figure 3.8 (a) shows the VF-TLP I-V curves of SG1 and DG1, and Figure 3.8 (b) shows the voltage vs. time waveforms of the two devices measured using a VF-TLP pulse with an amplitude of 37.5 V. Note that the failure currents obtained from the VF-TLP measurement are quite similar to those from the TLP measurements. Our failure analysis revealed that the ESD-induced damages took place near the corner of the gate/N-AlGaAs interface, suggesting that the failure is field rather than thermal related. Moreover, it was found that the single-gate ESD clamp SG1 failed at a VF-TLP pulse amplitude of 38 V, while the dual-gate clamp DG1 survived up to 94 V. We selected a stress voltage of 37.5 V to observe the voltage transients since neither DG1 nor SG1 was damaged and the ESD stress phenomenon was pronounced at such a stress condition. It can be seen that both SG1 and DG1 have similar turn-on speeds and overshoot voltages. As such, for structures being protected and sensitive to overshoots, the ESD capabilities of SG1 and DG1 can be very similar. On the other hand, the dual-gate clamp has the advantage over the single-gate clamp of a much lower voltage after triggering. Specifically, after 0.5 ns, the transient voltage waveform of SG1 rises up again to a plateau region, while the voltage waveform of DG1 is kept at a fairly constant level (see Figure 3.8(b)). This phenomenon can be explained as follows. Following the voltage overshoot, a large current in SG1 is forced to flow in the narrow 2DEG InGaAs channel

(see Figure 3.2(a)), resulting in an increase in the lattice temperature and consequently a decrease in the electron mobility. This in turn increases the resistance and hence the voltage drop in SG1 [16]. In contrast, for DG1, the creation of the additional current path in the AlGaAs layer owing to the presence of second gate keeps the resistance and voltage drop in such a device relatively constant. This makes the dual-gate clamp a highly attractive candidate for CDM ESD protection at the input pin where the ESD-induced damage is caused mostly from high voltage CDM transient. The turn-on time is defined as the time it takes from 10% V_{ave} to 110% V_{ave} , where V_{ave} for DG1 is a constant voltage calculated by averaging the voltages between 25% and 75% time periods. The values of V_{ave} , 10% V_{ave} , and 110% V_{ave} of DG1 are indicated in Figure 3.8(b). For SG1, since the voltage rises again after 0.5 ns, V_{ave} is chosen as the nadir voltage at 0.5 ns.



(a)



(b)

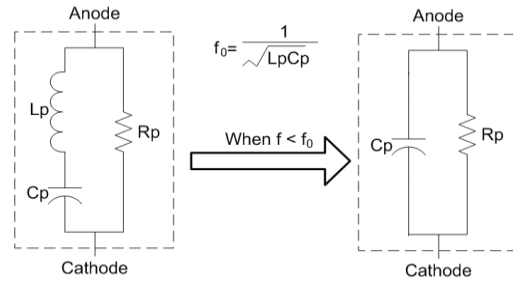
Figure 3.8 Current-voltage characteristics (the two curves on the right-hand side) and leakage currents (the two curves on the left-hand side) of SG1 and DG1 subject to VFTLP stresses, and (b) transient voltage waveforms of SG1 and DG1 subject to a VFTLP stress voltage of 37.5 V. Different Vave points for DG1 are also indicated.

Finally, we measured the S-parameters of the two clamps biased at 0 V using Agilent E8364C PNA Microwave Network Analyzer to determine the parasitic capacitances at different frequencies. Figure 3.9 (a) shows the ESD clamp's equivalent

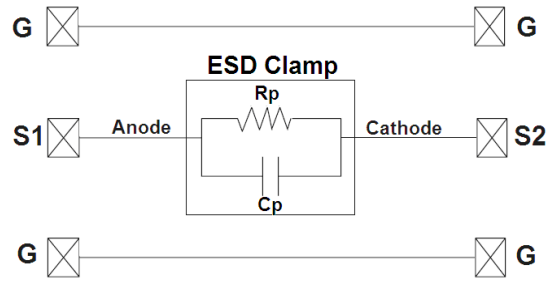
RLC circuit consisting of a capacitor C_p , resistor R_p , and inductor L_p and its simplified RC model. In most cases, an ESD clamp is operating under frequencies lower than the resonant frequency f_0 , and the RLC model can be reduced to the RC model under such an operation. Figure 3.9 (b) presents the ESD clamp's ground-signal-ground layout for S-parameter measurement, and Figure 3.9 (c) is the equation relating the capacitance to the S parameters based on the simplified RC model [18]. Figure 3.10 (a) and (b) plot the capacitances normalized to the layout area ($cap/area$) and to the TLP failure current (cap/It_2), respectively. The $cap/area$ results of SG1 and DG1 are very similar, whereas DG1 shows advantageous over SG1 when cap/It_2 is considered. When frequencies are higher than 8.5 GHz, both SG1 and DG1 exceed their resonate frequencies, and the devices turn from capacitive into inductive, causing the capacitance to drop sharply after this frequency.

The normalized capacitance of the single gate pHEMT clamp reported in [15] was about 0.06 fF/ μm^2 at 2 GHz, while both the single-gate/dual-gate pHEMT clamps in this paper have a normalized capacitance of about 0.1 fF/ μm^2 at the same frequency. The difference is due mainly to the different processes used. Considering its superb failure current level, the proposed dual-gate clamp is still highly attractive for RF ESD applications since further trade-off can be made between the parasitic capacitance and failure current.

Table 3.2 summarizes the ESD performances of SG1 and DG1 pHEMT-based clamps.



(a)



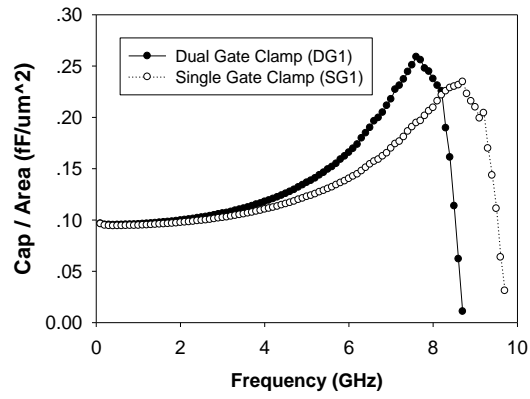
(b)

$$Y_{21} = \frac{-2S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{21}S_{12}}$$

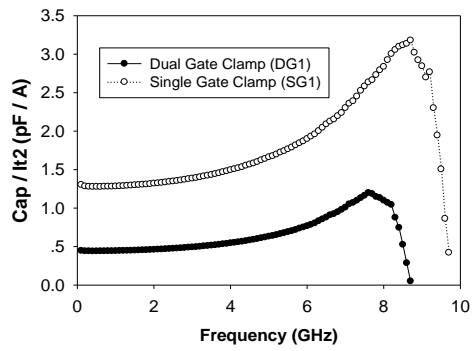
$$C_p = \frac{\text{Im}[Y_{21}]}{2\pi f}$$

(c)

Figure 3.9 (a) RLC model and simplified RC model (b) ground-signal-ground layout and (c) capacitance equation for the pHEMT ESD clamp



(a)



(b)

Figure 3.10 Measured parasitic capacitances vs. frequency of two clamps normalized to (a) area and (b) TLP failure current

Table 3.2 Summary of ESD figure of merits (FOMs) for single-gate clamp (SG1) and dual-gate clamp (DG1)

ESD FOMs	SG1	DG1
pHEMT Area (um ²)	116 x 106	135 X 106
Triggering Diode Area (um ²)	62 x 53	62 x 53
Current Limiter Resistor Area (um ²)	40 x 20	40 x 20
Failure Current I _{t2} (A)	1.15	3.80
Passing HBM (V)	2K	> 8K
Cap @ 5.2GHz (pF)	1.95	2.47
Cap / Area @ 5.2GHz (fF/um ²)	0.125	0.140
Cap / It2 @ 5.2GHz (pF/A)	1.70	0.65
On-state Resistance before failure (Ω)	14.0	3.07
Turn-on Time (ns)	0.48	0.48
Leakage Current (A)	2.7E-7	2.7E-7

The proposed dual-gate clamp can readily be used as a power clamp for a pHEMT-based LNA with $V_{dd} = 2\text{ V}$ and $V_{ss} = 0$, as the proposed ESD clamp has a trigger voltage of 3.2 V and a superb failure current. The device can also be used as an ESD protection device at the I/O pin, but the trigger voltage and parasitic capacitance will need to be optimized according to the I/O requirements.

3.3 A Novel Depletion-Mode Dual-gate ESD Protection Design

Section 3.2 presented a novel E-mode dual-gate ESD clamp in GaAs pHEMT process. This clamp has shown much better ESD protection ability than traditionally used stacked Schottky diode chain and single-gate pHEMT clamp. However, this E-mode ESD clamp can not be directly applied to depletion mode-only GaAs pHEMT process because lack of E-mode HEMT there. And this novel Dual-Gate pHEMT ESD

protection approach has not been experimentally evaluated in D-Mode technology yet. We are still using either stacked diode chain-based or Single-Gate clamp-based D-Mode ESD protection circuit with very limited ESD current handling ability. [15] On the contrast, A robust ESD protection solution in D-Mode HEMT technology is highly in demand because a lot of RF switch and RF power amplifiers are built in D-Mode only HEMT technology. [19] In this section we investigate and analyze the effectiveness of multi-gate D-mode pHEMT-based ESD protection circuits. Transmission line pulsing (TLP) measurement result shows that Dual-Gate D-Mode pHEMT ESD circuit has very attractive ESD discharge ability (failure current “ I_{t2} ” ~ 1.2 A, ~ 1.75 kV Human Body Model ESD level) and flexibility to adjust the trigger voltage for fulfilling different ESD protection design requirements.

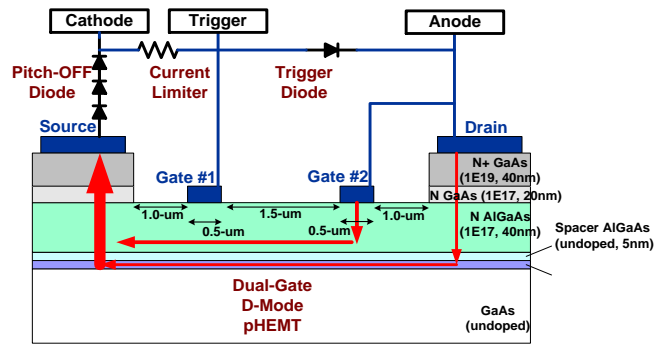
3.3.1 Device Structure

Figure 3.11 (a), and (b) show the cross section view of the proposed Depletion-Mode Dual-Gate GaAs pHEMT and schematic of ESD circuit built based on such a device. The ESD clamp consists of a trigger diode and a resistor (i.e., current limiter) to control the triggering of the pHEMT. Gate #1 in the dual-gate pHEMT is connected to the “trigger” terminal and Gate #2 is connected to the anode. And also note that several diodes (see “Pinch-OFF Diode” in the figure) are connected in series with main Dual-Gate D-Mode HEMT to turn it off since D-Mode HEMT is a normally “ON” device. The series “Pinch-OFF Diode” also helps in limiting the leakage through the protection circuits. Under the normal operation condition, the “Trigger Diode” is not turned on,

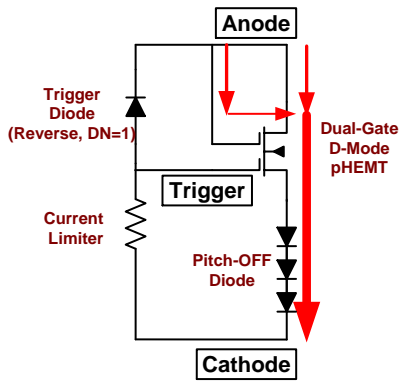
potential at the “Trigger” terminal is low, pHEMT is off, and current flow between the anode and cathode is negligibly small.

Under a sufficiently large ESD condition, a stress voltage at the anode larger than the blocking voltage of the diode string first turns on the diodes and then forces a current through the resistor. This raises the potential at the trigger terminal, reduces the depletion region underneath the Gate #1 and Gate #2, exposes the 2DEG channel and the second N AlGaAs discharge path, which allows for ESD current discharge between the anode and cathode. More detailed explanations for the mechanisms of two current conducting paths will be given in the next section.

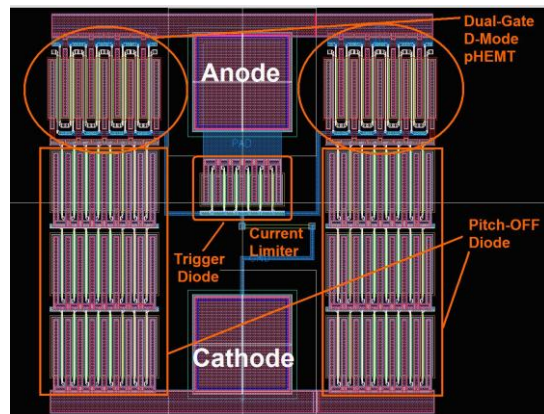
Figure 3.11 (c) presents the layout view of the Dual-Gate pHEMT. It was fabricated in a 0.5-um Depletion-Mode pHEMT technology at WIN Semiconductor. A triggering unit consisting of a reverse Schottky diode and a current limiter was incorporated in the circuit. Trigger diode area was 70x40 μm^2 , the current limiter resistor area was 64x5 μm^2 , Pitch-OFF diode area was 180x190 μm^2 , and the Dual-Gate pHEMT had 16 fingers and areas of 180x60 μm^2 . The total effective ESD cell area is 300 x 300 μm^2 including PADS area. Moreover, in real application we could further squeeze layout size by: (1) squeezing Trigger Diode area since it is just trigger unit and will not need large area to discharge ESD current (2) removing testing PADS structures.



(a)



(b)



(c)

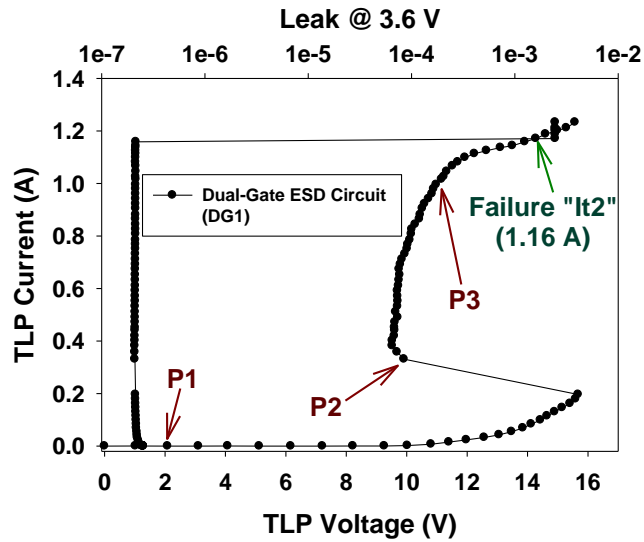
Figure 3.11 (a) Cross section view of proposed dual-gate ESD protection circuit in D-Mode pHEMT technology with the two red lines denote the two current paths, (b) Schematic view and (c) Layout view

3.3.2 Measurements and Discussion

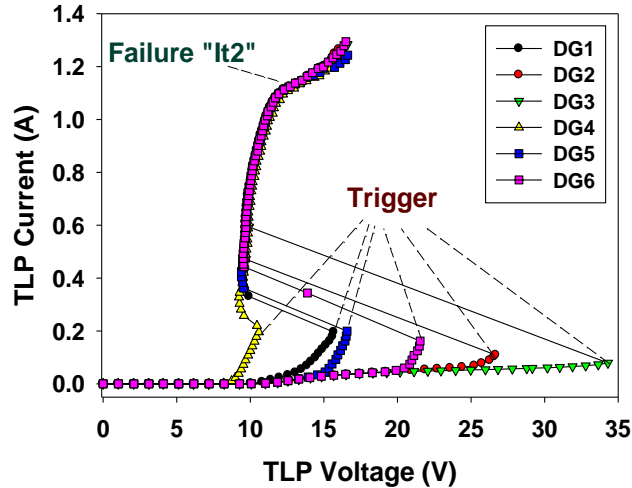
We performed HBM-like ESD measurements using the Barth 4002 transmission line pulse (TLP) tester which generates pulses having a 10 ns rise time and 100 ns width. Post-stress leakage current was measured at a voltage of 3.6 V. This voltage is the pHEMT normal operating voltage of 3.3 V, plus 10% dynamic voltage margin.

Figure 3.12 (a) presents the TLP current (y-axis) vs. voltage (bottom x-axis) and leakage current (top x-axis) curves of the Dual-Gate pHEMT ESD circuit. The failure current of the Dual-Gate device is 1.16 A, which can be directly correlated to HBM passing voltages by conventional estimate of multiplying the failure current to 1,500 ohm human body resistance. [20] Thus, it equals 1.75 kV HBM ESD level. We suspect the ESD damage happens in the series “Pitch-OFF” diode since “DG1” exhibits high on-state resistance prior to the failure, which is similar to stacked Schottky diode chain failure metrics. Table 3.3 compared TLP measurement results of the proposed Dual-Gate D-Mode HEMT ESD circuit with previously reported Single-Gate D-Mode clamp [15]. Clearly, the proposed Dual-Gate ESD circuit possesses a much higher failure current than its Single-Gate counterpart. And also the proposed Dual-Gate ESD circuit has better ESD level normalized to the pHEMT area (0.162 in “DG1” vs 0.12 in reported [15]). Note that the trigger voltage depends on the “Trigger Diode”, and this voltage can be adjusted by altering diode number and diode polarity. The trigger voltage of about 15.68 V observed in Figure 3.12 (a) resulted from the use of a reverse diode plus the 3 series Pitch OFF diodes. Figure 3.12(b) shows the TLP I-V characteristics of Dual-Gate pHEMT’s having 6 different Trigger Diode units. While the trigger voltage depends on

the diode number, the failure current is insensitive to such a factor. Table 3.4 summarizes the measured trigger voltage as a function of diode number and polarity.



(a)



(b)

Figure 3.12 (a) Current-voltage characteristics (on the right-hand side) and leakage currents (on the left-hand side) of dual-gate ESD protection circuit (DG1) having a reverse trigger diode from the TLP tester (b) TLP results of Dual-Gate ESD circuits having different trigger diode number and polarity (see DG1, DG2, DG3, DG4, DG5 and DG6 in Table 3.4)

Table 3.3 Comparing ESD Results of Proposed Dual-Gate ESD Circuit (DG1) and Single-Gate ESD Circuit [15]

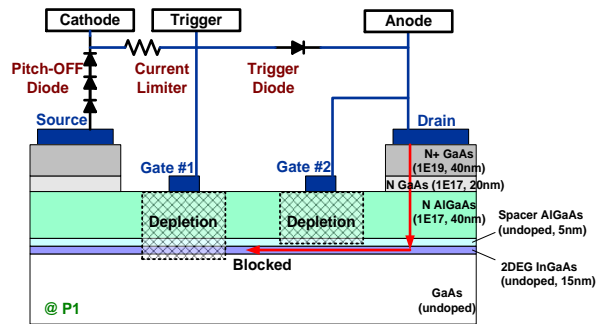
ESD FOMs	Dual-Gate “DG1”	Single Gate in [15]
Failure Current I_{t2} (A)	1.16	0.6
Equivalent HBM ESD Level (V)	1.75 kV	0.87 kV
HEMT Area (μm^2)	180 x 60	90 x 80
ESD / HEMT Area (V/ μm^2)	0.162	0.120

Table 3.4 Trigger voltage dependency on trigger diode number/ polarity for D-mode pHEMT ESD clamp

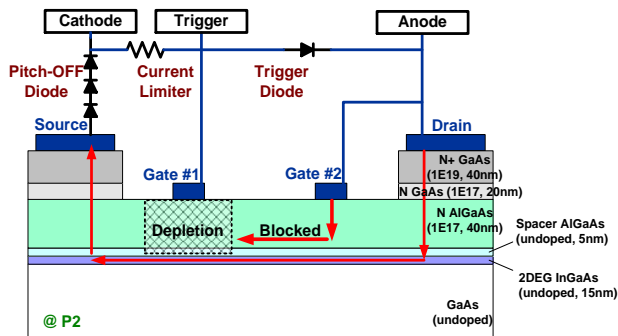
Dual-Gate Circuits	Diode Polarity	Diode Number	Trigger (V)	Failure “ I_{t2} ” (A)
DG1	Reverse	1	15.68	1.16
DG2	Reverse	2	26.67	1.17
DG3	Reverse	3	34.31	1.16
DG4	Forward	10	10.59	1.18
DG5	Forward	18	16.58	1.17
DG6	Forward	25	21.54	1.16

Referring to Figure 3.13, the different current conduction mechanisms can be explained in more details below using physical reasoning. When the stress voltage is at around 2V (“P1” in Figure 3.12 (a)), the 2DEG underneath Gate #2 is unblocked but underneath Gate #1 is still obscured by the depletion region because of the blockade of reverse “Trigger Diode” and “Pinch-OFF Diode” (see schematic in Figure 3.13(a) When the ESD stress increases (“P2” in Figure 3.12(a)), the clamp trigger voltage, the Schottky diode begins to turn on but its current path from the Schottky contact to the source via AlGaAs layer is still blocked by the depletion region associated with Gate #1 (see schematic in Figure 3.13(b)). The 2DEG underneath Gate #1 is unveiled at this time

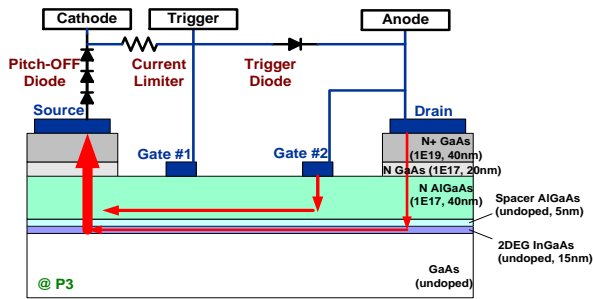
because the Trigger Diode is conducting. So there is only one current conducting path between the anode and cathode via the 2DEG channel (see Figure 3.13(b)). As the stress voltage further increases (“P3” in Figure 3.12 (a)), the depletion region associated with Gate #1 also vanishes, and the second current path associated with the Schottky diode is formed (see Figure 3.13(c)). As a result, we have two current conducting paths exist in the Dual-Gate pHEMT, which make the Dual-Gate D-Mode ESD circuit maintain much larger failure current.



(a)



(b)



(c)

Figure 3.13 Depletion regions and current paths in the dual-gate pHEMT at points (see Fig. 2) (a) "P1" (b) "P2" (c) "P3"

This section reports a new ESD protection structure consisting of a multi-gate pHEMT and trigger diodes in D-Mode only pHEMT technology. Due to the induced second current path in addition to 2DEG channel, the new ESD protection circuit showed improved ESD current discharge performances over the conventional Single-

Gate pHEMT ESD clamp. These results provided valuable information for the design of effective ESD protection solutions for D-Mode HEMT integrated circuits.

3.4 A Novel Drainless ESD Protection Design with Further Improved Robustness

Electrostatic discharge (ESD) induced failure is an important design concern for the GaAs pseudomorphic high electron mobility transistor (pHEMT) based integrated circuits due to the inherent low thermal conductivity of the compound material and fragility of the pHEMT structure [13]. As such, there is an urgent need for robust ESD protection solutions for radio frequency integrated circuits (RFIC's) built in the GaAs pHEMT process.

Traditionally, the stacked Schottky diode chain is widely used as an ESD protection component in GaAs pHEMT process. [17, 21] But this approach could consume a large footprint and give rise to a large on-state resistance as well as a large leakage current in the off state.[15] An ESD protection structure using a single-gate pHEMT clamp was proposed for the depletion mode (D-Mode) and enhancement mode (E-Mode) technologies [15, 22]. Such an ESD clamp is considered a better protection design than the Schottky diode-based clamp [15, 17, 22], but its robustness is still relatively poor due to the fact that there is only one current path (via the 2DEG channel) conducting the ESD current in the single-gate pHEMT, which consequently causes significant self-heating and current saturation [23]. More recently, a dual-gate pHEMT clamp was reported [24, 25] demonstrating an excellent ESD current handling ability because of the two current discharge paths imbedded in such a device. To further

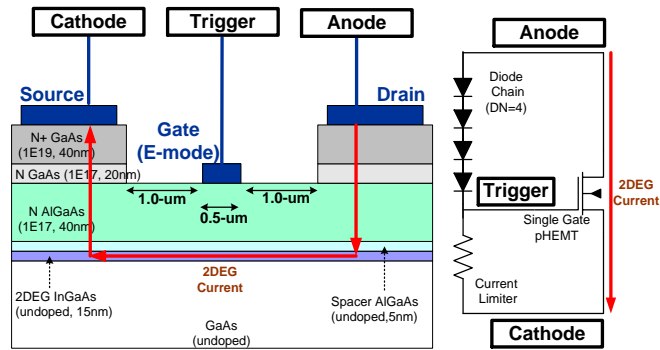
enhance the performance of the dual-gate pHEMT clamp, we will in this paper develop a new drain-less, multi-gate pHEMT for ESD protection applications. Transmission line pulsing (TLP) measurements will be carried out to illustrate the ESD performances of the new and existing pHEMT clamps.

3.4.1 Device Structure

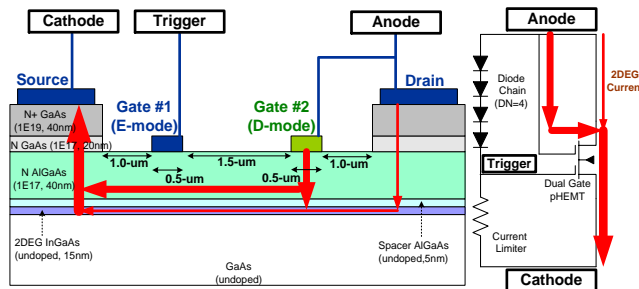
Figure 3.14 (a) shows the cross section view of a conventional E-mode, single-gate GaAs pHEMT and schematic of ESD clamp built based on such a device [15, 22]. The ESD clamp consists of a diode chain and a resistor (i.e., current limiter) to control the triggering of the pHEMT. Under the normal operation condition, the diode chain is not turned on, the potential at the trigger terminal is low, the pHEMT is off, and the current flow between the anode and cathode is negligibly small. Under the ESD condition, a stress voltage at the anode larger than the blocking voltage of the diode string first turns on the diodes and then forces a current through the resistor. This raises the potential at the trigger terminal, reduces the depletion region underneath the gate, exposes the 2DEG, and consequently allows for the ESD current to be discharged between the anode and cathode via the 2DEG channel (indicated by the red line in Figure 3.14(a)). Figure 3.14 (b) shows the cross section view of a recently reported dual-gate GaAs pHEMT and schematic of its ESD clamp [25]. Gate #1 in the dual-gate pHEMT is the same gate in the single-gate pHEMT, but the dual-gate pHEMT has a second gate, Gate #2, which is connected to the anode. Subjecting to a sufficiently large ESD stress voltage, the Schottky junction underneath Gate #2 will conduct. This forms a second current discharging path via the AlGaAs layer (see Figure 3.14 (b)), in addition to

the 2DEG current path created by Gate #1. The added current path reduces the on-state resistance and increases the robustness of the dual-gate pHEMT clamp.

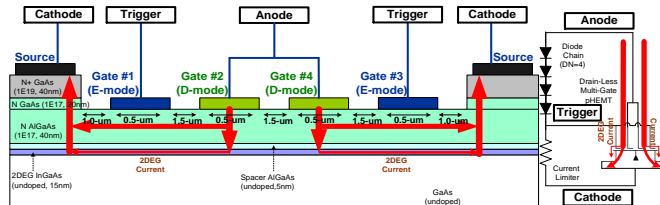
Figure 3.14 (c) shows the cross section view of the new drain-less, multi-gate pHEMT and schematic of its ESD clamp. This device differs from the dual-gate GaAs pHEMT in the following two aspects: (1) the drain region is removed due to the fact that the drain contributes minimally to the ESD current discharge while it does consume a considerable layout area [25], and (2) the structure is symmetrically mirrored, with two D-mode gates connected to the anode terminal, two E-mode gates connected to the trigger terminal, and two source contacts connected to the cathode terminal for better current distribution uniformity. Under a sufficiently large ESD stress voltage, the Schottky junction underneath the D-mode Gate #2 and Gate #4 will conduct. This forms a symmetrical current discharge path from Gate #2/Gate #4 to the source via the AlGaAs layer (see Figure 3.14 (c)), in addition to the 2DEG current path created by Gate #1/Gate #3. The added current path reduces the on-state resistance and increases the robustness of the dual-gate ESD clamp. The reason underlying the higher ESD robustness in the drainless multi-gate pHEMT clamp is that the conduction-inefficient “drain” in the conventional pHEMT is now replaced with a symmetrical, highly conductive channel in the AlGaAs layer created by the two D-mode gates, while the traditional current path via the 2DEG is still maintained (see Figure 3.14 (c)).



(a)



(b)



(c)

Figure 3.14 Cross section view and respective ESD clamp circuit for (a) single-gate pHEMT (b) dual-gate pHEMT (c) Drain-Less Multi-Gate pHEMT

3.4.2 Measurements and Discussion

Single-gate, dual-gate, and new drain-less multi-gate pHEMT clamps were fabricated in a 0.5- μm pHEMT process at WIN Semiconductor. A triggering unit consisting of 4-diode chain and a current limiter was incorporated in the clamps. Diode area was $62 \times 53 \mu\text{m}^2$, the current limiter resistor area was $40 \times 20 \mu\text{m}^2$, and the single-

gate, dual-gate, and proposed drainless multi-gate pHEMT each had 20 fingers and areas of $116 \times 10^6 \text{ um}^2$, $135 \times 10^6 \text{ um}^2$, and $175 \times 10^6 \text{ um}^2$, respectively. We performed HBM-like ESD measurements using the Barth 4002 transmission line pulse (TLP) tester which generates pulses having a 10 ns rise time and 100 ns width. Post-stress leakage current was measured at a voltage of 2.2 V. This voltage is the pHEMT normal operating voltage of 2.0 V, plus a 10% dynamic voltage margin.

Figure 3.15 presents the TLP current (y-axis) vs. voltage (bottom x-axis) and leakage current (top x-axis) curves of the single-gate, dual-gate and drain-less multi-gate ESD clamps. The measurement results were also summarized in Table 3.5. Clearly, the drain-less multi-gate pHEMT clamp has the highest failure current I_{t2} and equivalent HBM ESD level I_{t2} of 5.2 A and HBM passing voltage of 7.8 KV), followed by the dual-gate pHEMT clamp (I_{t2} of 2.0 A and HBM passing voltage of 3.0 KV), and the traditional single-gate pHEMT clamp has the lowest failure current handling ability of I_{t2} of 1.0 A. Moreover, the drain-less clamp also has the highest HBM passing level normalized by the pHEMT area (see Table 1). The trigger voltage of about 3.5 V was observed in Figure 3.15, resulting from the use of a 4-diode chain, and this voltage can be further adjusted by altering the diode number and diode polarity [25]. The proposed drainless multi-gate pHEMT clamp can readily be used as a power clamp for a pHEMT-based LNA with a supply voltage $V_{dd} = 2 \text{ V}$, as the ESD clamp has a trigger voltage of 3.5 V and a superb failure current.

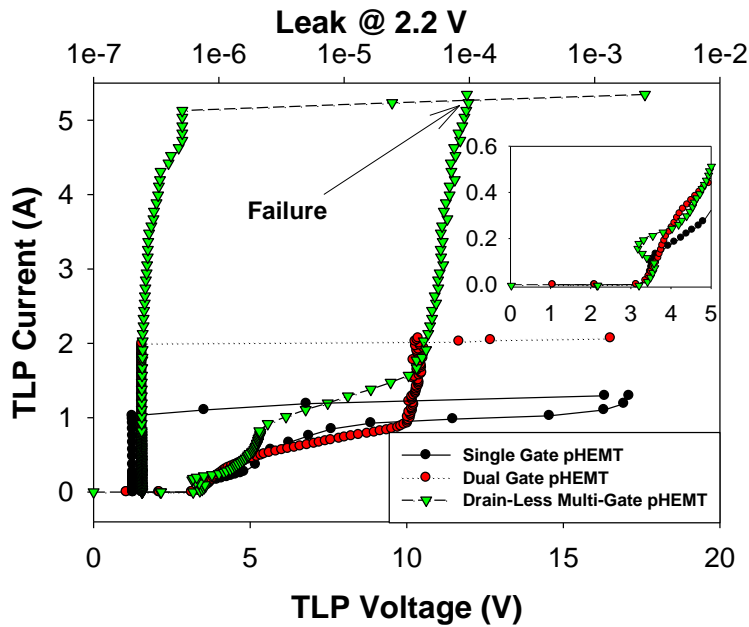


Figure 3.15 Current-voltage characteristics (the three curves on the right-hand side) and leakage currents (the three curves on the left-hand side) of single-gate pHEMT, clamp, dual-gate clamp, and drain-less multi-gate pHEMT clamp having a 4-diode chain obtained from the TLP tester

Table 3.5 Results of Single-Gate pHEMT, Dual-Gate pHEMT and Drain-Less Multi-Gate pHEMT ESD clamps

Device	Failure Current “ I_{f2} ” (A)	pHEMT Device Area (μm^2)	ESD/Area ($\text{V}/\mu\text{m}^2$)
Single Gate	1.1	116 x 106	0.1342
Dual Gate	2.0	136 x 106	0.2081
Four Gate	5.2	175 x 106	0.4205

Referring to Figure 3.16, the different current conduction mechanisms can be explained in more details below using physical reasoning. When the stress voltage is at around 2V (“P1” in Figure 3.15), the 2DEG channels underneath Gate #2/Gate #4 were unblocked but underneath Gate #1/Gate #3 are still obscured by the depletion region because of the blockade of diode chain (see schematic in Figure 3.14 (c). When the ESD stress increases (“P2” in Figure 3.15), the clamp trigger voltage, the Schottky diode

begins to turn on but its current path from D-mode Schottky gate contact (Gate #2 and Gate #4) to the source via AlGaAs layer is still blocked by the depletion region associated with Gate #1/Gate #3 (see schematic in Figure 3.16 (b)). The 2DEG underneath Gate #1/Gate #3 are unveiled at this time because the diode chain is conducting. So there is only one current conducting path between the anode and cathode via the 2DEG channel (see Figure 3.16 (b)). As the stress voltage further increases (“P3” in Figure 3.15), the depletion regions in N AlGaAs layer associated with Gate #1/Gate #3 also vanish, and the second current path associated with the Schottky diode are formed (see Figure 3.16 (c)). As a result, we have 4 symmetrical current conducting paths (2 symmetrical D-mode Schottky gate-N AlGaAs channel and 2 symmetrical 2DEG channel) exist in the proposed drainless multi-gate pHEMT, which make it maintain much larger failure current.

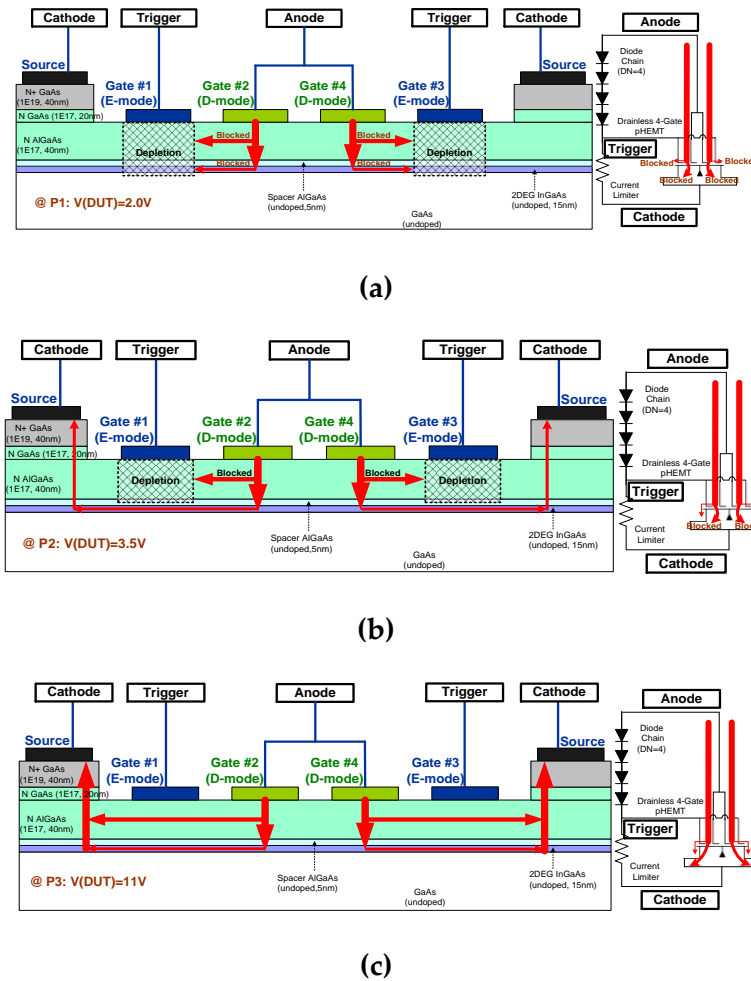


Figure 3.16 Depletion regions and current paths in the drainless multi-gate pHEMT ESD clamp at points (see Figure 3.15) (a) “P1” (b) “P2” (c) “P3”

A new ESD protection structure constructed by using a novel drain-less, multi-gate GaAs pHEMT and trigger diode chain was developed and characterized experimentally. Due to the symmetrically and highly conductive current path available in the novel pHEMT, in addition to the 2DEG channel existed in the traditional pHEMT, the new ESD protection solution showed significantly improved ESD performances over the conventional ones. These research results provided valuable information for the design of robust ESD protection solutions for pHEMT integrated circuits.

3.5 Summary

In this chapter, three novel ESD protection devices were designed and analyzed. The multi-gate pHEMT based ESD protection devices in both enhancement-mode and depletion-mode were reported and characterized. Due to the multiple current paths available in the multi-gate pHEMT, the new ESD protection clamp showed significantly improved ESD performances over the conventional single-gate pHEMT ESD clamp, including higher current discharge capability, lower on-state resistance, and smaller voltage transient. These results provided useful information for the design of effective ESD protection solutions for GaAs-based integrated circuits. Moreover, this chapter develops a further enhanced ESD protection clamp based on a novel drain-less, multi-gate pHEMT in a 0.5 μ m GaAs pHEMT technology. The three proposed ESD protection clamp can possess much higher current handling capability than the existing ESD protection devices such as Schottky diode chain and single-gate externally-triggered pHEMT clamp.

CHAPTER 4 DESIGN AND OPTIMIZATION OF ESD PROTECTION DESIGN FOR SiGe BiCMOS PROCESS

4.1 Introduction and Prior Arts

Silicon controlled rectifiers (SCRs) are increasingly used in the industry for Electrostatic Discharge (ESD) protection applications because of their high current handling capability[26] and low parasitic capacitance [27, 28]. In particular, these devices continue gaining importance for constructing ESD protection solutions for modern high-frequency integrated circuits such as those fabricated in a SiGe BiCMOS process [29].

ESD protection solutions for SiGe-based integrated circuits have been traditionally built primarily using low capacitance diodes. For applications in which the operating conditions do not allow for the use of up/down diodes due to voltage swing or noise considerations, Si-based low-voltage trigger SCR (LVTSCR) has also been considered [30, 31]. While the LVTSCR is generally robust, its response time is relatively slow. The response time for ESD device is defined at the time it takes the device to sink the intended current forced through it. LVTSCR's "slow" response performance leads to a considerable transient voltage overshoot that can severely limit the capability of this device to protect the MOS gates connected to the I/O pins during fast transient events, such as the Charged Device Model (CDM) event. In light of this, an improved SCR with a dummy gate structure has been also proposed to improve the response time and reduce parasitic capacitance [32].

In an effort to achieve a more robust protection clamp, SiGe SCRs characterized via transmission line pulsing (TLP) testing have been reported in the literature [2, 29, 33, 34]. These studies provided SiGe SCR's quasi-static I-V behaviors, which are applicable for the Human Body Model (HBM) ESD event. However, information pertinent to SiGe SCR's transient behaviors, such as the peak voltage and response time, has not been addressed. The transient behaviors are less critical for optimizing the protection device for HBM robustness, but gain importance for achieving CDM protection robustness. CDM is a fast ESD event having pulses with a 100 to 200 ps rise time and 1 to 2 ns width. More recently, the SiGe SCR's transient performance under the CDM stress was reported in [35], which offered initial guidelines for optimizing SiGe SCRs.

This chapter applies a systematic design methodology for SiGe BiCMOS SCR clamps based on ESD Technology Computer Aided (TCAD) analysis [36-42]. Very fast transmission line pulsing (vfTLP) measurements and TCAD simulations are conducted to obtain the underlying understanding on the optimization of several SiGe SCRs subject to the CDM ESD event and successful optimization results are demonstrated.

A conventional SiGe Silicon Controlled Rectifier (SCR1) [2] built in a 0.18-um SiGe BiCMOS process is shown in Figure 4.1, including its cross-section view and equivalent circuit. SCR1 consists of a P+/NW HV/P bipolar transistor T1, NW HV/P SiGe/N Poly bipolar transistor T2, NW HV resistor R1, and main capacitances C1 and C2. Note that there is an underneath buried oxide layer in this process and a deep trench surrounding this device. And also there is an additional highly-doped NXBA layer

between N+ and anode metal which helps a lot to reduce the contact resistance. On the contrast, no such highly-doped layer is available to P+ contact for SCR1 structure due to process limitation. Therefore some contact resistance effect might be expected here. Unlike T1, which is a Si homojunction bipolar transistor, T2 is a heterojunction bipolar transistor which turns on much faster than T1. In such a device, T1's base width D1 (i.e., 0.7 μm) is designed to be the minimum value allowed by the design rule of this process, the layout area is 208 μm^2 and the device width is 50 μm .

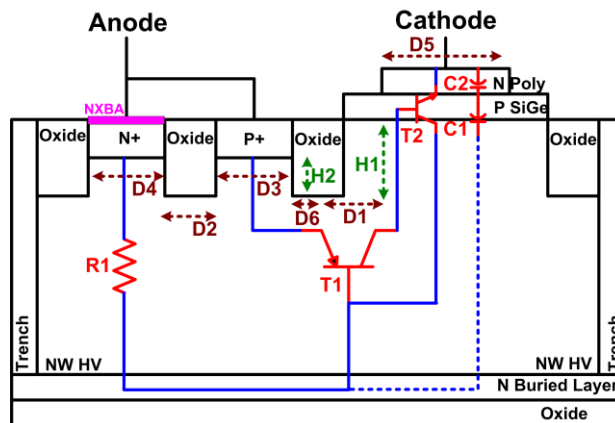


Figure 4.1 Cross-section views and equivalent circuits of conventional SiGe SCR (SCR1).

ESD measurements were carried out using the Barth 4012 very fast transmission line pulsing (vfTLP) tester. It generates CDM-like pulses with a 0.1 ns rise time and 5 ns width. [38, 39, 43]. Post-stress leakage currents were measured at a voltage of 3.6 V.

Figure 4.2 shows the transient voltage and current waveforms, respectively, under a vfTLP pulse which generates 570mA effective DUT (device under test) current level. Note that the 570mA effective vfTLP current level was used as a benchmark and corresponds to an arbitrary point in the snapback region of operation of the SCRs. (see Figure 4.3) It can be seen that the transient voltage waveform first rises to its overshoot

peak value (~ 24.61 V at around 0.1 ns) then falls to a relatively “flat” region (~ 1 ns). On the other hand, the current exhibits a plateau-like waveform between the turn-on and turn-off window. Based on these results, both the quasi-static method $V(\text{Quasi-Static})$ and peak voltage method $V(\text{Peak})$ can be used to extract the voltage data. For the quasi-static method, the data are extracted by averaging the voltage waveform in the $25\% \sim 75\%$ window, whereas the peak voltage method simply takes the peak transient voltage. On the other hand, only the quasi-static method is used in extracting the current data from the waveform since the overshoot is absent, and this extracted current data will be plotted versus extracted quasi-static voltage and peak voltage respectively in the followings.

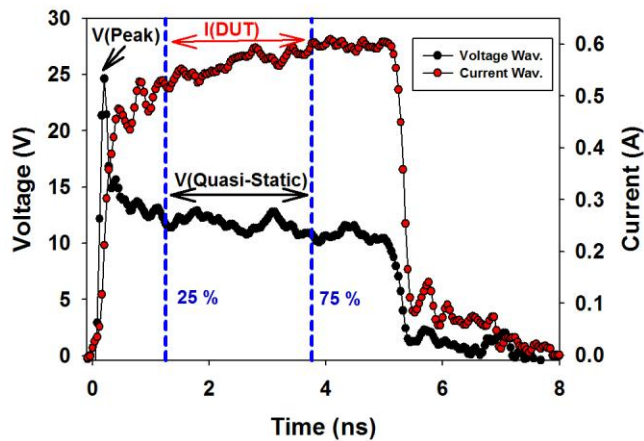


Figure 4.2 Measured transient waveforms for “SCR1” under Barth 4012 vFTLP with 5 ns pulse width, 0.1 ns rise time at 570 mA DUT current level stress: Voltage waveform (looking to left) and Current waveform (looking to right).

Figure 4.3 compares SCR1’s vFTLP current (y-axis) vs. voltage (bottom x-axis) and leakage current (top x-axis) curves using the quasi-static voltage and peak voltage methods. Clearly, the I-V curves of the two methods diverge soon after the device turns on at around 12.8 V. For example, at a current level of 570 mA, the quasi-static voltage is

11.62 V but a much higher peak voltage of 24.61 V. (see Figure 4.3) This phenomenon indicates that the commonly used quasi-static I-V method can overestimate ESD device's protection ability under fast ESD events such as the Charged Device Model (CDM). From the viewpoint of the quasi-static method, SCR1 looks good enough since the clamping voltage is below 13 V until it fails at 1.5 A. Based on the peak voltage method, this device in fact is poor because its peak voltage keeps on increasing to more than 25 V, a sufficiently large stress to damage the internal circuits intended to be protected (e.g. thin gate oxide).

In the following, we will study SiGe SCRs based on vFTLP measurements and TCAD simulations to gain the physical insights on the transient behaviors (peak voltage and response time) under the CDM event.

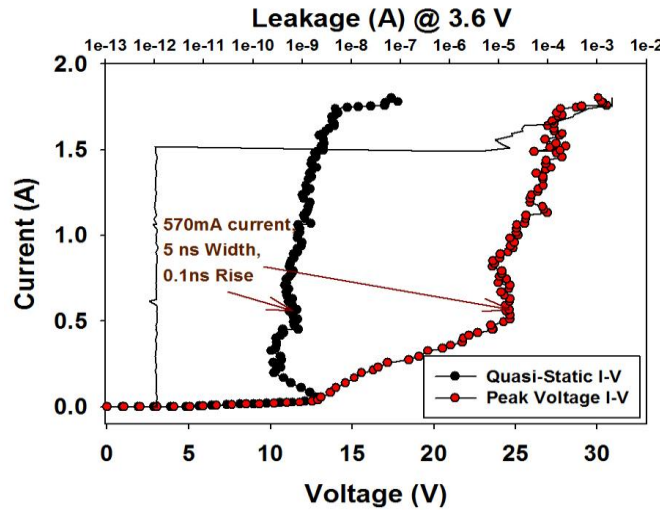


Figure 4.3 Measured I-V curve in Barth 4012 vFTLP for SiGe SCR1 using the quasi-static and peak voltage methods.

4.2 An Improved Vertical SCR-Based ESD Protection Design

4.2.1 Device Structure

Aiming at reducing the peak voltage, a new SiGe SCR with a P PLUG layer added was proposed and demonstrated recently [35]. For this specific process, a highly-doped PXBA layer was an associated layer of PPLUG and being automatically added between anode metal and N+ layer, which further reduces the contact resistance. The cross-section view and equivalent circuit of such a device is shown in Figure 4.4. Here we consider two different versions, called SCR2 and SCR3. They consist of a P PLUG/NW HV/P bipolar transistor T₃, NW-HV/P SiGe/N Poly bipolar transistor T₄, NW-HV resistor R₃, and main capacitances C₃ and C₄. For SCR2, the dimension D₁ is set to the minimum value of 0.7 μm , and D₁ is enlarged to 1.7 μm in SCR3. The areas are 208 μm^2 and 258 μm^2 for SCR2 and SCR3, respectively. Both devices have the same width of 50 μm .

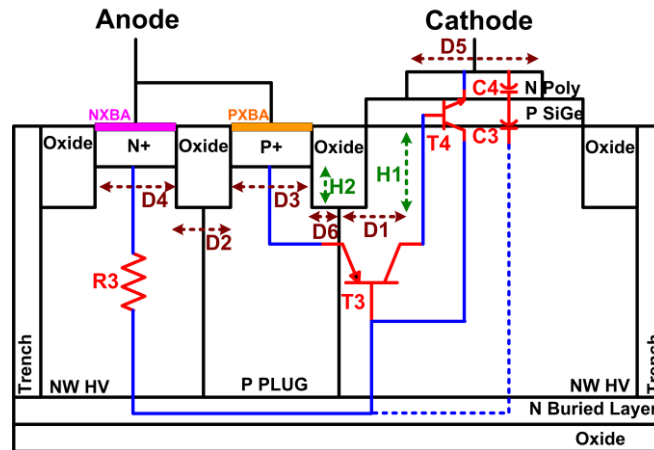


Figure 4.4 Cross-section views and equivalent circuits of proposed SiGe SCR with P PLUG (SCR2 and SCR3).

4.2.2 Measurements and Discussion

Figure 4.5(a) compares the transient voltage waveforms of SCR1, SCR2 and SCR3 under a 570mA effective current level v_{fTLP} stress. The results demonstrate that the presence of P PLUG can reduce the peak voltage, as SCR1 has the largest peak voltage of 24.61 V and SCR2 and SCR3 have smaller peak voltages of 13.91V and 15.65 V. PPLUG can also reduce the overshoot magnitude defined by difference of the peak voltage “V(Peak)” and averaged holding voltage “Vave” as SCR1 has 13.1V overshoot magnitude and SCR2 and SCR3 only have 11.0V, 12.7V respectively. It is noticed that SCR1 has the largest holding voltage “Vave” (averaged value between 25%~75% time window), which mainly come from contact resistance of anode metal and P+ in Figure 4.1. The metal/P+ contact resistance effect should not hurt our analysis of SiGe SCR under CDM condition since both measurement and simulation results show that turn-on speed indicators (peak voltage and overshoot magnitude) are not affected by contact resistance. The current waveforms of the three devices are given in Figure 4.5(b)

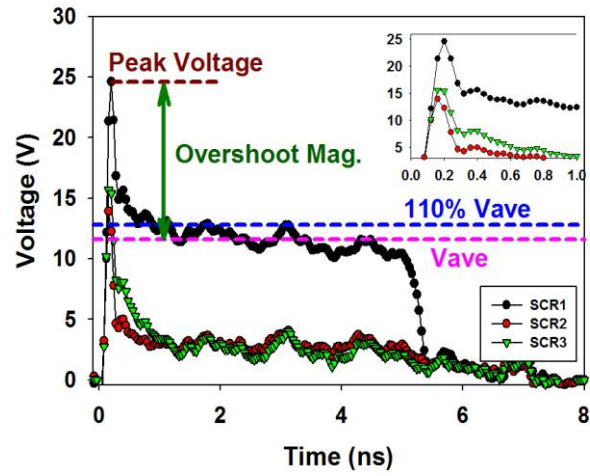
Shown in Figure 4.6 are the I-V curves of SCR1, SCR2 and SCR3 extracted using the peak voltage method. Consistent with the results in Figure 4.5 (a), SCR2 is clearly the most optimized ESD device in terms of the maximum voltage across it during v_{fTLP} stress. It is interesting that from Figure 4.6, after V_{t1} points, changes of I-V slopes around 0.5A can be observed on all three SCRs (around 15V for SCR2 and SCR3, and 25V for SCR1) under peak voltage extraction method. This slope-changing phenomenon confirms with the statement raised in [37, 44, 45] that turn-on time decrease with increased v_{fTLP} current level. The explanation is as follows: When v_{fTLP} current level is

lower than certain value (e.g. $<0.5\text{A}$, region “I”), the displacement current (dE/dt) is unable to sufficiently trigger the turn-on process at $\sim 0.1\text{ ns}$ time point therefore the peak voltage continues to increase (region “A” in Figure 4.6). While as the v_{TLP} current is greater (e.g. $>0.5\text{A}$, region “II”), the turn on process was triggered at 0.1 ns time period, which limits the peak voltage and exhibits a steeper I-V slope. This slope-changing phenomenon can not be observed by traditional quasi-static voltage extraction method because the traditional quasi-static method only takes data from 25%~75% time window when the device has already been turned on. The 570mA v_{TLP} current level mentioned above was intentionally selected from region II to better compare the turn-on performance of different versions of SiGe SCRs.

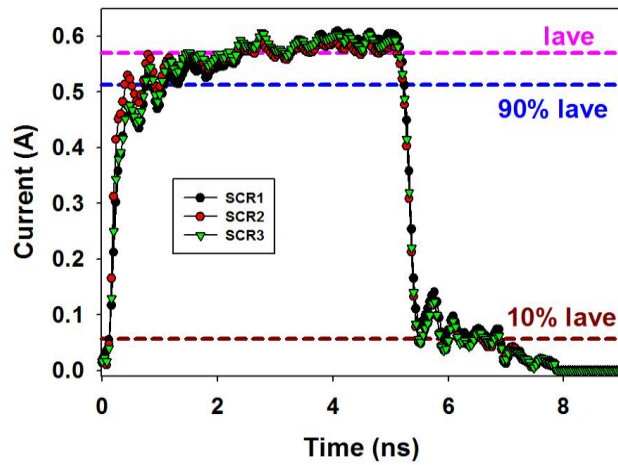
Another important figure of merit for the CDM event is the SCR’s turn-on response time, which can be extracted using both voltage vs. time waveforms and the current vs. time waveforms given in Fig. 5(a) and (b). As for voltage turn-on time method, response time is defined by the time from peak voltage to 110% averaged holding voltage “ V_{ave} ”. For all the three SiGe SCRs considered, the currents increase rapidly before 0.2 ns and then reach a fairly constant level. The time for ESD device to reach its steady-state current is called the current turn-on response time and is defined as the time it takes from 10% to 90% I_{ave} , where I_{ave} is the constant current calculated by averaging the currents between 25% and 75% time periods. The values of I_{ave} , 10% I_{ave} , and 90% I_{ave} for SCR1 are labeled in Fig. 5(b). For both voltage turn-on method and current turn-on method, SCR2 has smallest turn-on response time, SCR3 has the largest response time, and SCR1 has a value in between. For constructing an effective CDM ESD

protection solution, a small peak voltage and small response time are highly desirable. Thus, SCR2 with the P PLUG layer and minimum D1 is the most optimized device for such an application.

Table 4.1 summarized the dimensions and measured key parameters of the three SCR's under study using both very fast TLP (vfTLP) measurement and traditional TLP measurement. It is worthy to mention that both vfTLP / TLP measurements show exactly the same tendency for parameters such as trigger voltage, failure current, on-state resistance, and holding voltage. For this specific process, the trigger voltage, peak voltage of ESD protection device under CDM ESD event is targeted to be lower than 14 V, which is the gate oxide breakdown voltage in this process. The SiGe SCRs mentioned in this paper were fabricated in a dielectrically isolated SOI process, so there is inherent latch up immunity. And the quasi-static holding voltage is targeted to be larger than operation voltage "1.8V-Vdd" to further avoid latch up risk. At the same time, high failure current is favorable. Clearly, the SCR2 is the most optimized ESD device because of its all-around excellence in the parameters mentioned before. And as the fabrication technology further scales down (e.g. 90nm, 65nm), the proposed SCR2 will turns out to be more advantageous for its smaller overshoot/faster turn-on speed because in such advanced process, gate oxide is very thin and therefore more and more vulnerable under CDM stress. In the next section, we will conduct TCAD simulations to analyze and gain physical insights on the transient behaviors (peak voltage and response time) of the SCRs under the CDM event.



(a)



(b)

Figure 4.5 Comparison of measured transient (a) voltage waveforms and (b) current waveforms for SiGe SCRs (SCR1, SCR2 and SCR3) subject to 570mA effective DUT current level with 5 ns pulse width, 0.1 ns rise time by Barth 4012 vFTLP stress.

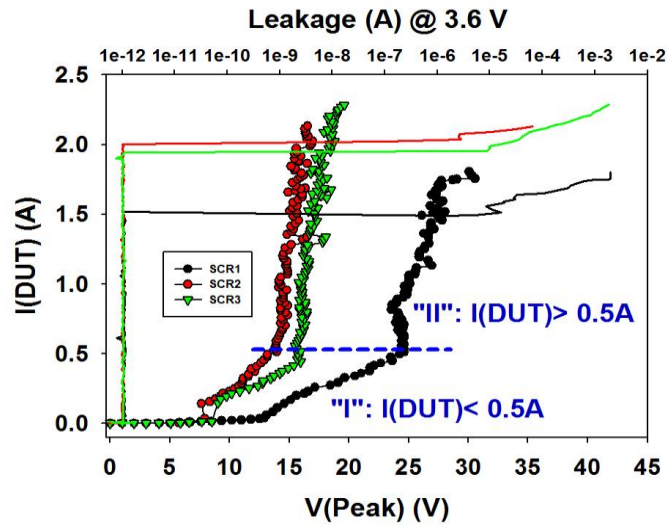


Figure 4.6 Comparison of I-V curves extracted using the peak voltage method for SCR1, SCR2 and SCR3.

Table 4.1 Summary of Dimensions and Measurement ESD Parameters.

Device	SCR1	SCR2	SCR3
Figs	Fig. 1	Fig. 4	Fig. 4
D1 (um)	0.7	0.7	1.7
D2 (um)	1.0	1.0	1.0
D3 (um)	0.7	0.7	0.7
D4 (um)	0.7	0.7	0.7
D5 (um)	0.35	0.35	0.35
D6 (um)	0.5	0.5	0.5
H1 (um)	0.5	0.5	0.5
H2 (um)	0.2	0.2	0.2
P PLUG Existence	N	Y	Y
Effective PNP Base Width (um)	1.9	1.2	2.2
Device Width (um)	50	50	50
Trigger (V)-vfTLP	12.77	6.33	8.16
Trigger (V)- TLP	12.33	7.1	8.03
Failure Current "I _{t2} " (A)-vfTLP	1.5	2.0	1.94
Failure Current "I _{t2} " (A)-TLP	0.7	1.5	1.4
On-State Resistance (Ohm)-vfTLP	18.49	8.44	9.01
On-State Resistance (Ohm)-TLP	21.31	3.25	3.61
Holding Voltage (V)-vfTLP	11.62	3.0	2.5
Holding Voltage (V)- TLP	8.0	3.0	3.0
Peak Voltage (V) @ 570mA	24.61	13.91	15.65
Overshoot Mag. (V) @ 570mA	13.1	11.0	12.7
Voltage Turn-On Time (ns)@570mA	0.96	0.5	1.02
Current Turn-On Time (ns)@570mA	0.63	0.27	0.64

The SiGe SCRs were simulated in Sentaurus TCAD software tool using the same doping densities listed in

Table 4.2. The TCAD simulation setup was calibrated by comparing DC-like I-V curves between simulation and measurements. We performed vfTLP-like simulations in

which voltage pulses with a 0.1 ns rise time, 5ns width and incremental amplitude were used. An effective resistor was also attached to the voltage pulse to mimic 50-Ohm transmission impedance of vTLP test system. In this TCAD simulation, important mechanisms including the Fermi statistics, Shockley-Read-Hall carrier recombination, Auger recombination, high-field saturation, lattice temperature, and avalanche model are accounted for.

Table 4.2 Doping Profile in TCAD Simulation.

Layer	Doping	Concentration (cm ⁻³)
P SiGe	Boron	1.2E17
N Poly	Arsenic	5E20
NW HV	Phosphorus	1E16
P PLUG	Boron	1E17
N Buried	Arsenic	1E19
N+	Arsenic	1E19
P+	Boron	1E19

The simulated voltage vs. time waveforms for SCR1, SCR2 and SCR3 are shown in Figure 4.7. All devices exhibit a peak voltage at ~ 0.1 ns before they settle down to a relatively constant value. Further, the results suggest that SCR1 has the largest peak voltage and SCR2 the smallest peak voltage. These TCAD simulation data are in excellent agreement with the measured data presented in the previous section except for the holding voltage, because the anode metal/P+ was set to be ideal contact in simulation hence SCR1 shows no higher holding voltage as seen in Figure 4.5(a). This discrepancy between simulation and measurements should not hurt the physical

understanding since peak voltage and overshoot magnitude turn out to be exactly the same tendency as measurements.

In Figure 4.8, we compare the impact ionization rates of the three SiGe SCRs at their respective peak voltage points (see “Peak @ SCR1”, “Peak @ SCR2”, and “Peak @ SCR3” in Figure 4.7. Based on this, we can suggest the following sequential events in the SCRs at the time of voltage peaking [37, 40]:

- i. As the voltage between the anode and cathode increases, a large number of hole-electron pairs are generated in the high impact ionization region (impact region) between the P+ and P SiGe regions;
- ii. Holes are injected toward the cathode to turn on the vertical NPN BJT (see T2 in Figure 4.1 and T4 in Figure 4.4) and electrons are injected toward the anode to turn on the PNP BJT (see T1 in Figure 4.1 and T3 in Figure 4.4);
- iii. When both the PNP and NPN BJT are turned on, a large current flows through the impact region; and
- iv. Voltage between the anode and cathode decreases.

In other words, the peak voltage is the voltage needed to generate the required impact ionization rate in the impact region to trigger the SCR. Figure 4.8(a)-(c) clearly show that the sizes of the impact ionization region of the SCRs are different, the SCR1 being the largest and SCR2 the smallest. Therefore, the reason SCR1 has the largest peak voltage is because the absence of the P PLUG layer induces a relatively large area of impact ionization region, and the voltage drop roughly equals the integration of electric

field along with ionization region. Therefore, larger-area impact ionization region means larger peak voltage needed to trigger the SCR device. On the other hand, For the SiGe SCRs with the P PLUG layer (SCR2 and SCR3) the impact ionization region is much smaller which in turn reduces the voltage required to generate the required impact ionization. Another factor that influences the area size of the impact ionization is the emitter injection efficiency of the PNP (T1). For SCR2 and SCR3 the presence of the heavily doped PPLUG region will result in a very high emitter injection efficiency factor. The reason is that the reduced base width of PNP transistor, which improves bipolar efficiency of PNP and eventually improved SCR's turn-on behavior. Whereas for SCR1 this factor is much lower due to the absence of the PPLUG.

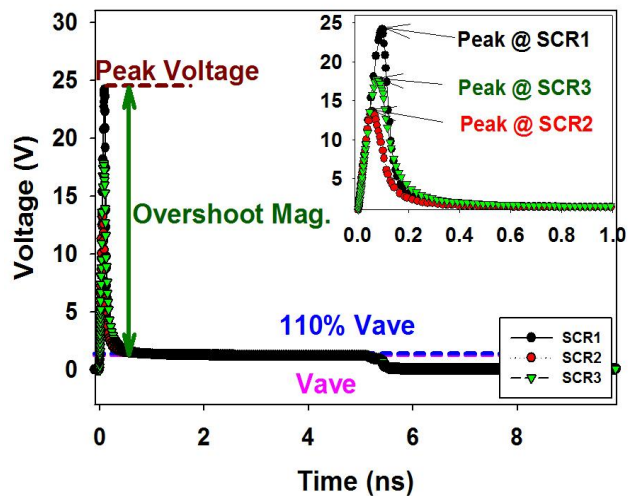
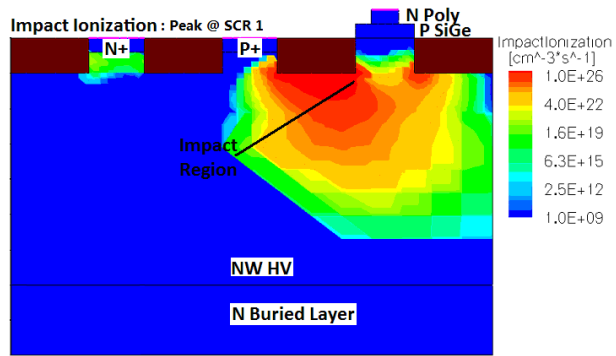
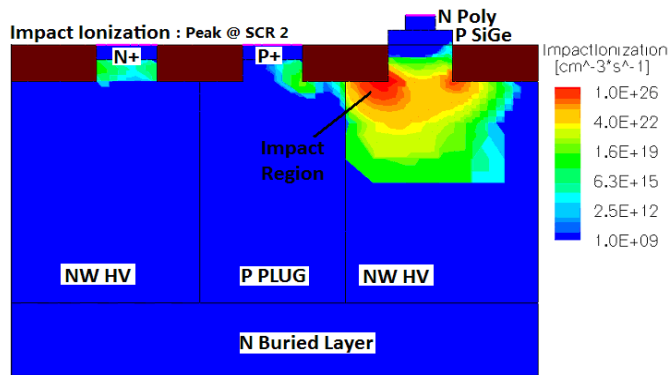


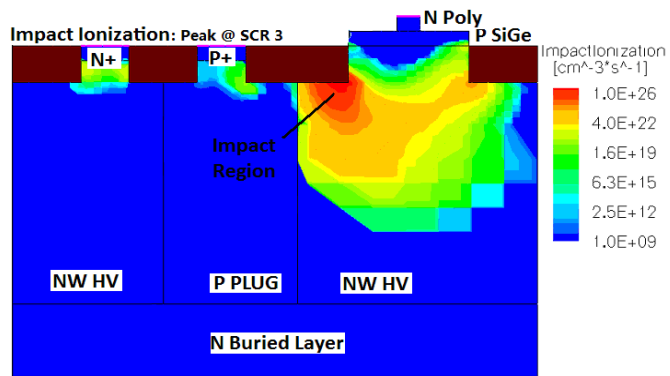
Figure 4.7 Comparison of simulated transient voltage waveforms for SiGe SCRs under 30V amplitude, 5 ns pulse width, 0.1ns rise pulse.



(a)



(b)



(c)

Figure 4.8 Simulated electron impact ionization contour at peak voltage points of (a) SCR1 (b) SCR2 and (c) SCR3.

Figure 4.9 compares the simulated current vs. time waveforms for SCR1, SCR2 and SCR3 subject to the same CDM stress as used in Figure 4.5. A similar trend is found

between the measured and simulated data; SCR2 has the smallest response time and SCR3 largest response time. To understand this, we simulated the hole current densities of the three SiGe SCRs at their respective turn-on points (see “SCR1_90%”, “SCR2_90%” and “SCR3_90%” in Figure 4.9), and the simulation results are given in Figure 4.10(a)-(c). The response time of SiGe SCR is mainly determined by the base transit time of the parasitic PNP homojunction transistor (T1 in Figure 4.1 and T3 in Figure 4.4) since the vertical NPN transistor (T2 and T4) are heterojunction transistors which turn on much faster than the homojunction counterpart [46]. Thus, a longer PNP base width will increase the base transit time and lead to a larger response time. The effective base widths in which the majority hole currents flow are different for the three SCRs. As indicated in Figs. 10 (a)-(c), SCR2 has the smallest effective base width of 1.2 μm and SCR3 has the largest effective base width of 2.2 μm . This provides a good explanation to the response times extracted from the measured and simulated results. Comparing the results of SCR1 and SCR2, which have the same D1 value, it can be concluded that the presence of the P PLUG layer reduces the effective PNP base width. To a smaller extent, the smaller D1 in SCR2, in comparison with that in SCR3, also plays a role in reducing the response time of the SiGe SCR.

Table 4.3 summarizes SiGe SCRs' transient parameters obtained from the measurements and TCAD simulations. The preceding analysis has suggested that a SiGe SCR having a combination of the P PLUG layer and minimal PNP base width D1 can offer an optimal protection capability against the CDM ESD event.

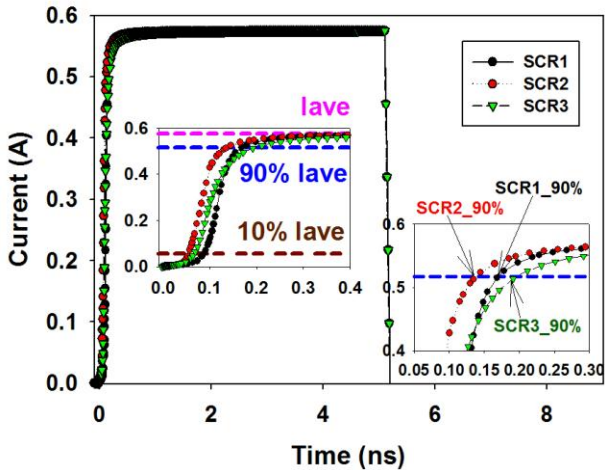
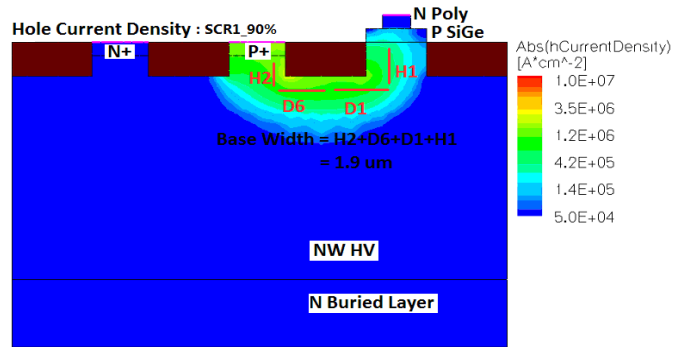
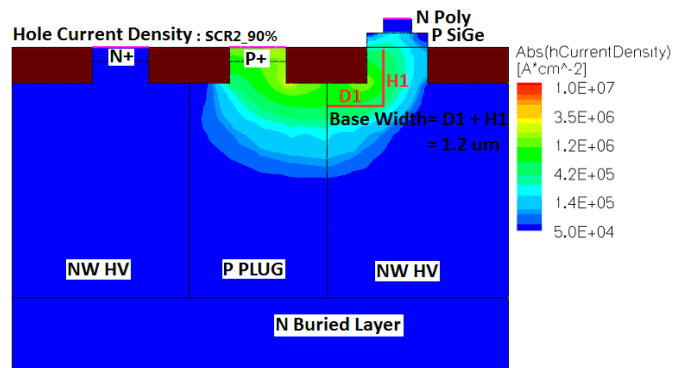


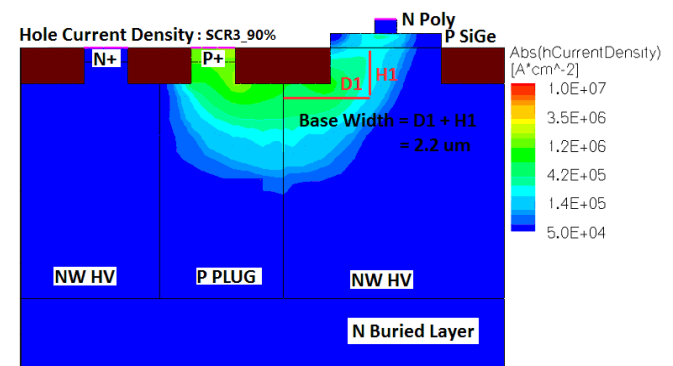
Figure 4.9 Comparison of simulated transient current waveforms for SiGe SCRs under 30V amplitude, 5 ns pulse width, 0.1ns rise pulse.



(a)



(b)



(c)

Figure 4.10 Simulated hole current density contours of (a) SCR1 (b) SCR2 and (c) SCR3.

Table 4.3 Summary of Transient Parameters Obtained from Measurement and Simulation under vFTLP Stress.

Device	SCR1	SCR2	SCR3
P PLUG Existence	N	Y	Y
Effective PNP Base Width (um)	1.9	1.2	2.2
Peak Voltage (V): Measured	24.61	13.91	15.65
Peak Voltage (V): Simulated	24.16	13.64	17.82
Overshoot Magnitude (V): Measured	13.1	11.0	12.7
Overshoot Magnitude (V): Simulated	22.88	12.36	16.49
Voltage Turn-On Response Time (ns): Measured	0.96	0.5	1.02
Voltage Turn-On Response Time (ns): Simulated	0.63	0.59	0.92
Current Turn-On Response Time (ns): Measured	0.63	0.27	0.64
Current Turn-On Response time (ns): Simulated	0.09	0.06	0.13

4.3 Summary

In this chapter, SiGe-based silicon controlled rectifiers (SiGe SCRs) fabricated in a 0.18-um BiCMOS process were analyzed using the very fast TLP and TCAD simulation. It was demonstrated that a SiGe SCR implemented with a P PLUG layer and minimal PNP base width can offer the smallest peak voltage and fastest response time. The improved performance mainly resulted from the fact that the impact ionization region and effective base width in the SiGe SCR were reduced due to the presence of the P PLUG layer. This work demonstrated a practical approach for designing optimum ESD protection solutions for the low-voltage/high-speed SiGe-based integrated circuits.

CHAPTER 5 DESIGN AND OPTIMIZATION OF ESD PROTECTION DESIGN FOR STANDARD RF CMOS PROCESS

5.1 Introduction and Prior Arts

In standard CMOS process, Electrostatic discharge (ESD) protection devices for radio frequency (RF) applications must hold very low parasitic capacitance to minimize degradation to RF functionality. This requirement imposes an important challenge to RF ESD design, as a low capacitance typically means a small device area and consequently a poor robustness of the ESD protection device. Diode chain has traditionally been used as ESD protection structures for RF integrated circuits (RF IC's) in CMOS process because of its relative simple makeup and low parasitic capacitance [30, 47]. But such a structure can have a large on-state resistance as well as a high leakage current [48]. A polysilicon silicon controlled rectifier (SCR) was reported in [31] for its low capacitance and good ESD robustness. This ESD clamp is considered a better protection solution than the diode chain, but it requires a modification to the polysilicon deposition process which limits its application in the standard CMOS process. An SCR with a waffle layout and small parasitic capacitance was also developed recently [49]. Nevertheless, this structure exhibited a relatively large turn-on time and large trigger voltage (close to 13 V), rendering it unsuitable for ESD protection of low-voltage CMOS applications.

In this chapter, a new SCR-based ESD protection clamp aimed for a very low parasitic capacitance is developed. The new device can be fabricated in a standard CMOS process without introducing extra processing steps. This clamp also provides a

relatively low trigger voltage for effectively protecting thin gate oxide as well as a relatively high holding voltage for latch-up immunity.

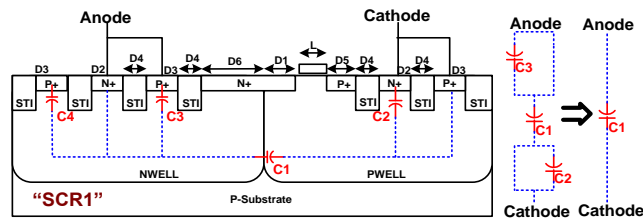
5.2 An Improved Low Parasitic Capacitance ESD Protection Design

5.2.1 Device Structure

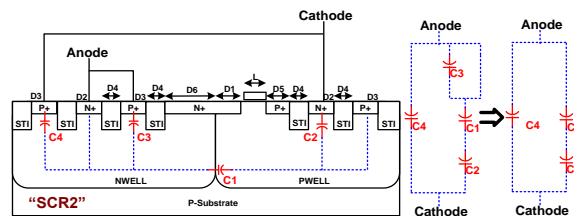
Figure 5.1 (a) and (b) show the cross-sectional views and equivalent junction capacitances of the conventional low-voltage SCR (Clamp1) and the proposed optimized SCR (Clamp2), respectively. These devices were fabricated in a 0.18- μm CMOS process and has the same layout area of $50 \times 10 \mu\text{m}^2$. It is important to note that the make-up of the two devices is identical, only the cathode terminal connections are different. Instead of connecting the cathode terminal to the P+ region in the P-Well region, as is conventionally done (see Figure 5.1 (a)), the cathode terminal of the new optimized SCR is connected to the P+ region in the N-Well region (see Figure 5.1 (b)). Because of this optimum configuration, the total capacitance of Clapm2 is equal to C_4 in parallel with C_1 in series with C_2 . On the other hand, the total capacitance in Clamp1 dominated by C_1 since C_2 , and C_3 were shortened.

The above mentioned capacitances are the various junction capacitances imbedded in Clamp1 and Clamp2 shown in Figure 5.1 (a) and (b). Since C_1 is the largest among these capacitances due to the large N-Well/P-Well junction area, Clamp2 has a lower capacitance than Clamp1. The capacitances of Clamp1 and Clamp2 at different anode-to-cathode voltages were measured using HP 4284 and are shown in Figure 5.1 (c). Notice that the capacitance of Clamp1 is larger than that of Clamp2 by a factor as

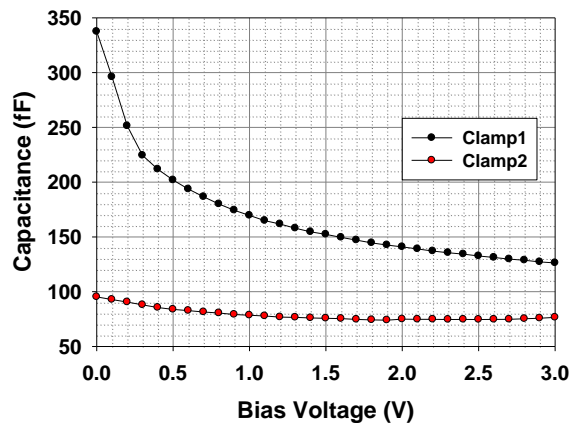
large as 3.4. The results also show that the capacitance values for both Clamp1 and Clamp2 decrease when the voltage is increased. The trend is consistent with the fact that dominating capacitance C_1 associated with the reverse biased N-Well/P-Well junction decreases with increasing reverse voltage [50].



(a)



(b)



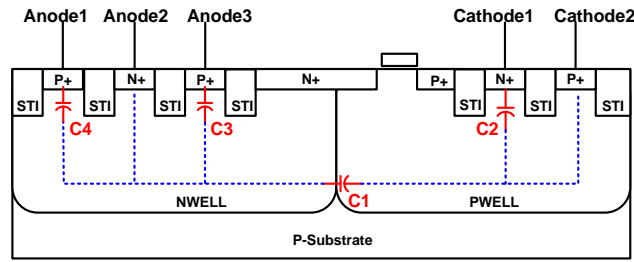
(c)

Figure 5.1 (a) Cross section and capacitance equivalent circuit of conventional-like SCR Clamp1, (b) cross section and capacitance equivalent circuit of new optimum SCR Clamp2, and (3) measured capacitances vs. Anode-Cathode voltage of Clamp1 and Clamp2.

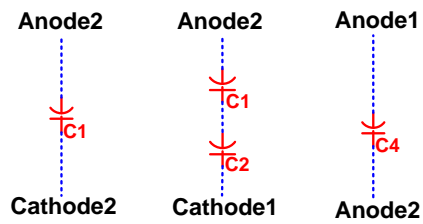
5.2.2 Measurements and Discussion

In order to analyze in more detail the overall parasitic capacitances of Clamp1 and Clamp2, the same SCR-based structure but with isolated anode and cathode terminals was fabricated as shown in Figure 5.2 (a). To isolate the various capacitances in the device, several isolated terminals (anode1, anode2, anode3, cathode1, and cathode2) were defined in the various N+ and P+ regions. The different pairings of these terminals allowed capturing the difference capacitances, as illustrated in the equivalent circuits in Figure 5.2 (b). For example, anode2-cathode2 pair yields C_1 . These different capacitances were measured and plotted in Figure 5.3.

The results confirm the earlier statement that the main blocking junction capacitance C_1 is the largest among all these capacitances. The parasitic capacitance of Clamp1 is about the same as the N-Well/P-Well capacitance C_1 , which is very large (335 fF at zero bias). In contrast, in the optimized Clamp2, the C_1 is in series with C_2 , thus resulting in a small value of $C_{1,2}$ (34 fF at zero bias). In addition, the capacitance of P+/N-Well junction C_4 is also small (60 fF at zero bias) because of the small junction area. Hence the parasitic capacitance of Clamp2 is simply the addition of C_4 and $C_{1,2}$ (see Figure 5.3), and Clamp2 exhibits a much lower capacitance than Clamp1 (94 fF versus 335 fF).



(a)



(b)

Figure 5.2 (a) SCR with isolated Anode and Cathode terminals and (b) equivalent capacitances for the pairings of Anode2-Cathode2, Anode2-Cathode1, and Anode1-Anode2.

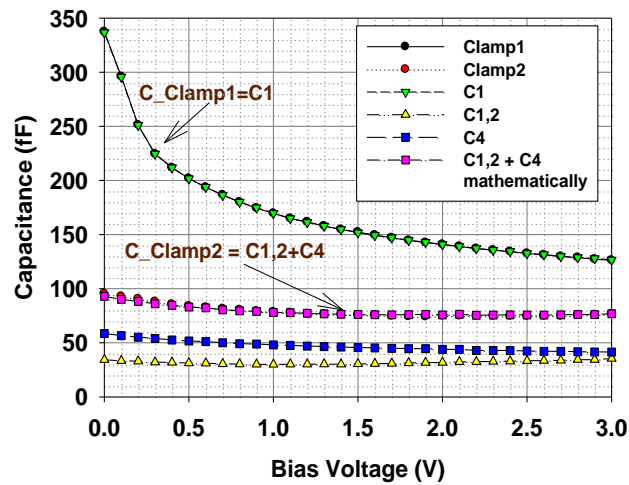


Figure 5.3 Comparison of capacitances obtained from different anode-cathode connections shown in Figure 5.2.

To investigate the ESD robustness of Clamp1 and Clamp2 under the human body model (HBM), transmission line pulsing (TLP) measurements were conducted. Post-stress leakage

currents were measured at 3.6 V, which is the maximum operating voltage of the technology under consideration. Figure 5.4 shows the measured TLP current (y-axis) vs. voltage (bottom x-axis) and leakage current (top x-axis) curves of Clamp1 and Clamp2. In the forward direction, Clamp2 has a smaller trigger voltage and higher failure current than Clamp1 (i.e., 8.1V in Clamp2 versus 10.5V in Clamp1, and 1.55A in Clamp2 versus 1.2A in Clamp1). These improved features are stemmed from the presence of the floating base of the N-Well/P-Well/N+ transistor in Clamp2. In the reverse direction, Clamp2 also possesses a smaller on-state resistance and higher failure current than Clamp1. This is owing to the different current conducting capabilities of the P-Well/N-Well diode in Clamp1 and the P+/N-Well diode in Clamp2.

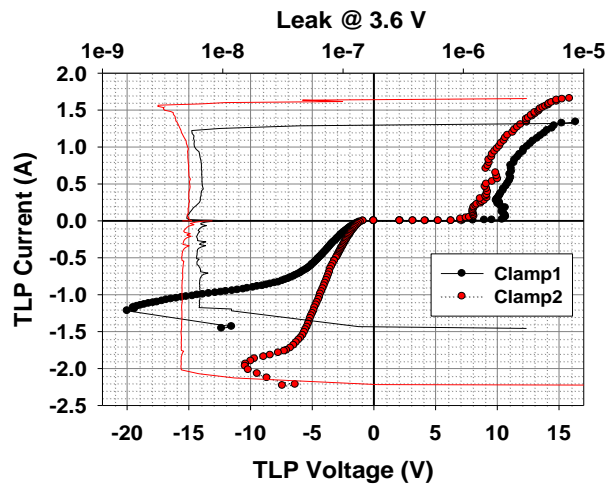


Figure 5.4 Bidirectional TLP current-voltage characteristics (red and black closed circles) and leakage currents (red and black solid lines) of Clamp1 and Clamp2.

Table 5.1 summarizes the characteristics of the two above-mentioned ESD devices (Clamp1 and Clamp2) as well as another low-capacitance clamp (Clamp3) reported previously [51]. Among the three devices, Clamp2 is the best candidate for RF ESD protection because of its all-around excellence in parasitic capacitance, current handling capability, trigger voltage, turn-on

time, and voltage overshoot. It should be pointed out that the turn-on time and voltage overshoot were measured using the very-fast TLP and are important parameters for a fast ESD event like the charge device model (CDM). The voltage overshoot is the peak voltage of ESD device in its turn-on transient, and the turn-on time is defined as the time from voltage overshoot point to 110% holding voltage point.

Table 5.1 Comparison of results of Clamp1, Clamp2, and Clamp3

Parameter	Clamp1	Clamp2	Clamp3 ^[51]
Device Area (μm^2)	50 x 10	50 x 10	45 x 20
Failure Current-Forward (A)	1.2	1.55	1.0
On-State Resistance-Forward (Ohm)	5.0	4.5	4.8
Trigger Voltage-Forward (V)	10.5	8.1	8.5
Failure Current-Reverse (A)	1.2	2.0	1.5
On-State Resistance-Reverse (Ohm)	13.0	2.0	2.5
Turn-On Time (ns) @ 1A	3.2	0.9	2.8
Voltage Overshoot (V) @ 1A	25	12	22
Capacitance @ 0V bias (fF)	335	94	95

5.3 Summary

A novel SCR-based ESD structure has been proposed and characterized experimentally for the design of effective ESD protection solutions in high-frequency CMOS-based integrated circuits. Such a new device showed a much lower parasitic capacitance and better ESD performance than the conventional SCR and a low-capacitance SCR reported in the literature. A theoretical analysis was also given to provide the physics underlying the low capacitance observed in the new ESD protection device.

CHAPTER 6 CONCLUSION

As semiconductor fabrication technology continues to advance, ESD induced reliability issue is becoming more and more challenging due to the shrink of device size, and lower breakdown voltage. In order to reduce IC failure caused by ESD damage, on-chip ESD protection devices are widely used to discharge ESD current and limit the overstress voltage under different ESD events. There are already some effective ESD protection devices reported for low speed circuits such as analog ICs or digital ICs in CMOS process. On the contrast, there are only a few ESD protection devices available for RF ICs. RF ESD design is way more challenging than traditional low speed CMOS ESD protection design because of the facts that: (1) High-performance RF ICs are typically fabricated in compound semiconductor process such as GaAs pHEMT and SiGe HBT process. And some proved effective ESD devices (e.g. SCR) are not able to be fabricated due to process limitation. (2) Compound semiconductor process has lower thermal conductivity which will worsen its ESD damage immunity. (3) Even for RF ICs fabricated in CMOS process, the inherent parasitic capacitance of ESD protection devices is a big concern. The dissertation begins with the introduction of ESD phenomena fundamentals, ESD models, ESD test methods and different types of ESD device's characteristics. For RF ICs, there are mainly three on-chip ESD protection devices available in existing literature: (1) diode and diode chain (2) externally triggered ESD clamp (3) SCR. However, each of them has its own shortcomings which will prevent them from being widely used as RF IC ESD protection. Diode chain has large layout area, large on-state resistance and poor leakage under "OFF" state. Externally

triggered in GaAs pHEMT process has only limited ESD protection level due to the fact that there is only one current path (via the 2DEG channel) conducting. SCR could be fabricated in SiGe BiCMOS process and standard CMOS process, but SCR is slow under CDM event and also SCR has fairly large parasitic capacitance. Motivated by the abovementioned design challenges of RF ESD design, this dissertation will systematically contribute on ESD protection design and analysis for RF ICs in different processes such as GaAs pHEMT, SiGe BiCMOS process, and standard CMOS process.

The ESD protection for RF ICs in GaAs pHEMT process is very difficult, and the typical HBM protection level is below 1-kV HBM level. The first part of our work is to analyze pHEMT's snapback, post-snapback saturation and thermal failure under ESD stress. In CHAPTER 2, we performed both TLP-like simulation in Sentaurus TCAD and Barth 4002 TLP measurements to understand the device physics behind them. The snapback is caused by virtual bipolar transistor due to large electron-hole pairs impacted near drain region. Post-snapback saturation is caused by temperature-induced mobility degradation due to III-V compound semiconductor materials' poor thermal conductivity. And thermal failure is found to be caused by hot spot located in pHEMT's InGaAs layer. Understanding of these physical mechanisms is critical to design effective ESD protection device in GaAs pHEMT process.

With these important device physics understood, several novel ESD protection devices were designed in CHAPTER 3. The multi-gate pHEMT based ESD protection devices in both enhancement-mode and depletion-mode were reported and characterized. Due to the multiple current paths available in the multi-gate pHEMT, the

new ESD protection clamp showed significantly improved ESD performances over the conventional single-gate pHEMT ESD clamp, including higher current discharge capability, lower on-state resistance, and smaller voltage transient. These results provided useful information for the design of effective ESD protection solutions for GaAs-based integrated circuits. Moreover, this chapter develops a further enhanced ESD protection clamp based on a novel drain-less, multi-gate pHEMT in a 0.5 μ m GaAs pHEMT technology. The proposed ESD protection clamp can possess a even higher current handling capability than the newly reported dual-gate pHEMT clamp under the human body model (HBM) ESD condition. Based on Barth 4002 TLP measurement results, the ESD protection devices proposed in this chapter can improve the ESD level from 1-kV (0.6 A It₂) to up to 8-kV (> 5.2 A It₂) under HBM.

SiGe BiCMOS process is another important compound semiconductor process for RF ICs. SiGe-based silicon controlled rectifier is considered a good candidate ESD protection device in this process. However, the SiGe SCR has the possible slow turn-on issue under CDM ESD events, which could prevent it from being the effective ESD protection devices. In order to optimize the turn-on performance of SiGe SCR against CDM ESD, the Barth 4012 very fast TLP (vfTLP) and vfTLP-like TCAD simulation were used for characterization and analysis in. It was demonstrated that a SiGe SCR implemented with a P PLUG layer and minimal PNP base width can supply the smallest peak voltage and fastest response time. The improved performance mainly resulted from the fact that the impact ionization region and effective base width in the SiGe SCR were reduced due to the presence of the P PLUG layer. This work demonstrated a

practical approach for designing optimum ESD protection solutions for the low-voltage/high-speed integrated circuits in SiGe BiCMOS process.

Finally we returned to standard silicon-based CMOS process to optimize ESD protection devices for RF ICs in CHAPTER 5. In CMOS process, there are already lots of ESD structures reported. Of those reported structures, SCR is again considered the best for its excellent current handling ability. However, the parasitic capacitance of SCRs need to reduced to limit SCR's impact to RF performance. Driven by this, we proposed a novel SCR-based ESD structure and characterize it experimentally for the design of effective ESD protection in high-frequency CMOS based integrated circuits. The proposed SCR-based ESD protection device showed a much lower parasitic capacitance and better ESD performance than the conventional SCR and a low-capacitance SCR reported in the literature. A theoretical analysis was also given to provide the physics underlying the low capacitance observed in the new ESD protection device.

The dissertation has systematically discussed ESD protection for RF ICs in all the major process including GaAs pHEMT process, SiGe BiCMOS process, and standard silicon-based CMOS process. Barth 4002 TLP, Barth 4012 vfTLP and Sentaurus TCAD tools were used for characterization and analysis. This dissertation supplies some useful information for effective ESD design for RF ICs.

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