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STUDY OF INGAAS LDMOS FOR POWER CONVERSION APPLICATIONS

by

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B.S. Shanghai Jiaotong University, 2003
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A thesis submitted in partial fulfillment of the requirements
for the degree of Master of Science
in the School of Electrical Engineering and Computer Science
in the College of Engineering and Computer Science
at the University of Central Florida
Orlando, Florida

Summer Term
2009

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ABSTRACT

In this work an n-channel $In_{0.65}Ga_{0.35}As$ LDMOS with Al_2O_3 as gate dielectric is investigated. Instead of using traditional Si process for LDMOS, we suggest $In_{0.65}Ga_{0.35}As$ as substitute material due to its higher electron mobility and its promising for power applications. The proposed 0.5-μm channel-length LDMOS cell is studied through device TCAD simulation tools. Due to different gate dielectric, comprehensive comparisons between $In_{0.65}Ga_{0.35}As$ LDMOS and Si LDMOS are made in two ways, structure with the same cross-sectional dimension, and structure with different thickness of gate dielectric to achieve the same gate capacitance. The on-resistance of the new device shows a big improvement with no degradation on breakdown voltage over traditional device. Also it is indicated from these comparisons that the figure of merit(FOM) Ron·Qg of $In_{0.65}Ga_{0.35}As$ LDMOS shows an average of 91.9% improvement to that of Si LDMOS. To further explore the benefit of using $In_{0.65}Ga_{0.35}As$ LDMOS as switch in power applications, DC-DC buck converter is utilized to observe the performance of LDMOS in terms of power efficiency. The LDMOS performance is experimented with operation frequency of the circuit sweeping in the range from 100 KHz to 100 MHz. It turns out InGaAs LDMOS is good candidate for power applications.

ACKNOWLEDGMENTS

I would like to express my gratitude to my advisor, Professor Jiann S. Yuan, for his warm, sincere, approachable support, patience, and encouragement throughout my graduate studies. He contributed many critical directions and suggestions to this work while offering freedom to pursue and manage my own research. His technical and editorial advice was essential to the completion of this dissertation and has taught me innumerable insights on the workings of academic research in general. The knowledge and the philosophy that he taught me will be the guide for my professional life.

My thanks also go to the members of my dissertation committee, Dr. Kalpathy B. Sundaram, Dr. Lee Chow for reading previous drafts of this dissertation and providing many valuable comments that improved the presentation and contents of this dissertation.

I am grateful to all my colleagues in the lab - Jun Ma, Yixin Yu, and Karan. In particular, I discussed lots of issues with Jun Ma about the design and simulation of LDMOS device. Yixin gave me precious advice on the macro model setup and simulation environment. I also obtained many helps from karan about the DC-DC power circuit simulations. We have collaborated in many issues, and I have learned many things from them.

Last, but not least, I would like to thank my wife Tieying Ma for her understanding and love during the past few years. Her support and encouragement was in the end what made this dissertation possible. My parents - Shaojiang Liu and Longnv

Wang, receive my deepest gratitude and love for their dedication and many years of support during my studies.

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LIST OF ACRONYMS/ABBREVIATIONS

AC	Alternating Current
ASIC	Application Specific Integrated Circuits
BV	Breakdown Voltage
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DUT	Device-Under-Test
EOS	Electrostatic Discharge
EOT	Effective Oxide Thickness
ESOA	Electrical Safe Operating Area
FOM	Figure of Merit
GTO	Gate Turn-Off thyristor
HF	High Frequency
HVIC	High Voltage Integrated Circuit
IC	Integrated Circuit
IGBT	Insulate Gated Bipolar Transistor
I-V	Current versus Voltage
LDMOS	Lateral Double-diffused MOSFET
MCT	MOS Controlled Thyristor
MOS	Metal Oxide Semiconductor
MOSFET	MOS Field Effect Transistor
NMOSFET	N-type MOS Field Effect Transistor
PE	Power Efficiency

PMOSFET   P-type MOS Field Effect Transistor

RESURF   Reduced SURface Field technology

RF   Radio Frequency

SH   Self-Heating

SOC   System on Chip

SOI   Silicon-on- Insulator

T-SOA   Thermal Safe Operating Area

VDMOS   Vertical Double-diffused MOSFET

VLSI   Very-Large-Scale Intergration

CHAPTER ONE: INTRODUCTION

1.1 Power Semiconductor

Semiconductor power devices and power circuit is extremely important in the microelectronic technology, its development has been hailed as the second electronic revolution. Contemporary development of semiconductor power devices can be traced back to 1952 when R.N.Hall [1] developed the first power semiconductor rectifier. In 1957, the invention of silicon thyristor by J.L.Moll and et al [2] marks the advent of the semiconductor devices to power electric field. Since then, with the new power semiconductor devices continue to emerge, forming the edge of a new subject of the power electronics. Electronics then began to follow two directions: in pursuit of a single component of the low-power, high - Integrated, high-frequency integrated circuits, micro-electronics technology at the core; another is in pursuit of great merit rate, a small drive current, high current density, and short switching time for high-power semiconductor devices on behalf of the power electronics.

The first generation of power in the fifties is mainly due to improve the device by the thyristor and its components. Silicon thyristor invented in 1957 by J.L.Moll, who, which are semi-controlled device, has the conduction current of 25A, blocking voltage of 300V. But it is too slow to shutdown, it can only work at low-frequency (typically less than 400 kHz), at the same time gate anode current can not be turn off and can only be controlled one-way.

Power transistors in sixties represent the second generation - power bipolar type transistors, such power device solves the non-controllable of the first generation, but they face large current drive and power consumption problems. At the same time as a result of power bipolar transistor minority charge storage in base charge neutral region, although its working frequency have greatly improved from thyristor, but is still relatively low, generally 1MHz or below.

The late seventies, with the development of micro-electronic technology and power electronic technology, high-frequency and fully controlled third generation power devices - field control power devices emerges. Field-controlled power device is used for small and medium-power application; the main product includes the power MOSFET, static induction transistor as well as the static induction thyristor and so on. Compared with bipolar-type power device, it has the merit of fast switching speed, high input impedance, no second breakdown, and simpler driver circuit. It has become the main strain in today's power device.

After eighties, the fourth-generation of power device comes up with a complex power control. There are two categories: the power MOSFET combined with bipolar power transistor and thyristor respectively. The former includes Insulated Gate Bipolar Transistor (IGBT) [3], MOS transistor (MGT) and so on. The later includes a static induction thyristor (SITH), MOS Gated thyrister (MCT) [4] and so on.

Based on the above developing stage and working principle, power devices can be divided into the following three categories: 1. traditional bipolar based power semiconductor devices; 2. MOSFET and modern power IC devices; 3. the large power

devices on the basis of the first two categories that are developed. Among them, the power MOS are mainly small and medium-power devices, mostly used in the field of consumer electronics. It has been more than three decades since possession development of power MOS transistors from its inception. Summed up its development path, we can see that it has been to the development into two directions: first, towards the traditional bipolar power devices, which have a great hope that the device achieves high breakdown electric pressure and low on-resistance. A typical device, such as: The GBT, MCT, etc.; the other direction is its self - body structure, improved materials and a very low resistance direction. In this area, there are work such as LDMOS, VDMOS performance optimization and the opening of SOI materials.

The development of power MOSFET promotes the development of power integrated circuits. Power IC is the combination of power semiconductor technology and microelectronic technology. Power integrated circuits currently used mainly for motor control (Motor control), electronic ballast (electrical ballast), flat-panel display driver (pannel display drive), switching power supply (switching power), automotive electronics and RF base station (RF base station) and etc. At present, there are major usage of two technologies, RESURF technology, and direct silicon bonding (SBD technology); the other is the smart power integrated circuits (SP workers C), it is the power electronic devices and control circuits, protection of electricity wire, drive circuit and sensor circuits such as multi-purpose single-chip integration, as compared with discrete components, it achieves a size reduction of a two-thirds and the cost drop of one third, alto the efficiency and reliability increases.

1.2 LDMOS

In 1971, Y. Tarui and etc. proposed a lateral MOS structure of double-diffusion [5]. In 1976, M. J. DeClerq And J. D. Plummer used this program to make the first LDMOS [6]. LDMOS technology is the use of double-diffusion, that is, in the same window implant boron and phosphate twice. The difference in depth of horizontal spread of two impurities through the junction determines the length of channel. LDMOS technology can easily achieve sub-micron channel length, and lithography is not restricted. Therefore, the transconductance gm, drain current Ids, maximum operating frequency and speed greatly improve than ordinary MOSFET.

LDMOS have a high resistance region between source and drain, known as the drift region. The existence of high resistance drift region gives higher breakdown voltage and reduced the parasitic capacitance of the source and drain, which will help improve the frequency characteristics. At the same time, drift region gives a buffer between the channel and drain, weakens the short-channel effect of LDMOS. Because of the majority of voltage drop in the drift region, so after the channel pinch-off, there is no channel length modulation effect. Increased voltage drop will not reduce the output resistance, channel area is not penetrated, so the breakdown voltage of LDMOS will not be affected by the channel length and doping level, which may carry out an independent design.

LDMOS is a voltage-controlled device with high input impedance and low driven power. It has good temperature characteristics, with negative temperature coefficient, excessive negative feedback will not form the localized current that lead to bipolar second breakdown. It also has wide safe work area (SOA), thus can prevent the effects of

heat dissipation, good thermal stability, and work temperature of 200 ℃. It is the majority carrier devices, with strong anti-radiation and do not have minority carrier storage effects, so it has fast switching speed. A number of LDMOS devices can work in parallel. LDMOS has high-gain, linear range, small intermodulation distortion, which is suitable for RF Applications. Due to high input impedance from gate control, current has the negative temperature coefficient, LDMOS completes multi-unit parallel to achieve low on-resistance of the high current work which the bipolar transistors do not have. Because multi-unit parallel, so it is easy to use the rest of the unit to achieve over-voltage, over current, over-temperature protection and many other features. The existence of drift region played a role in channel isolation, they weakened channel modulation. However, the LDMOS relatively large capacitance, smaller current density, and along with the increase in drain voltage, on-resistance and breakdown voltage trade-off restrict LDMOS in broader application fields.

Compared with the bipolar transistor, LDMOS has advantages in the following aspects. First is a higher gain. LDMOS maintains constant transconductance in case of a large range of current level, so it has a larger linear dynamic range. This indicates that to receive the same gain, LDMOS devices only need a smaller amplifier cascade, resulting in higher reliability and lower Costs.

Second is the thermal stability. LDMOS with the negative temperature coefficient, it can prevent the effects of heat dissipation, thus measures do not need temperature compensation.

Third is the frequency stability. The absence of diode nodes and the higher feedback capacitance corresponding to the input impedance make LDMOS more stable than the bipolar.

Lastly, LDMOS devices with lower power density lead to larger cooling area. And LDMOS devices do not need electrical isolation, thus the thermal resistance of LDMOS devices is lower compared to bipolar devices.

With the power capacity of the power semiconductor devices continue to increase and performance advancing, the scope of application continues to expand. In recent years, LDMOS is often used as switch in switching power supply circuits, display drivers, communication circuits, electronic ballasts, automotive electronic circuits, DC a DC Transform, DC one AC transform, fast switch transform, high-fidelity audio amplification, a variety of analog switches, high-speed core driven, following the circuit or Spiral-driven, a transistor logic and interface, motor control, automotive electronics, Energy efficient lighting, induction heating, RF communications and other fields. In addition, LDMOS devices are especially suitable for digital terrestrial TV, satisfy the need for the widest frequency range, high linearity and high service life applications.

Nowadays LDMOS device applied to the products includes main semiconductor manufacturers Freescale, Philips, Ericsson and so on. In which, Freescale account for 60% the global market, Philips accounted for 25% of the global market, other companies are actively competing for research and development [7].

1.3 Research Work

Under the guidance of Dr. Jiann S. Yuan, we carried out a series of studies, with emphasis on research of InGaAs LDMOS power devices in a variety of working conditions and the temperature change of the self-heating effect. That common Ⅲ-Ⅴ compound material InGaAs applied to LDMOS structure is novel in stead of silicon LDMOS, which will result in many interesting issues. In this work, the results can satisfy as a reference for the design of Ⅲ-Ⅴ compound LDMOS power devices.

Firstly, the possibility and advantages of using InGaAs as channel conducting material of LDMOS on InP substrate is discussed. There are recent trend in fabricating InGaAs MOSFET in terms of its high current handling capability. A couple of lab samples are available as reported recent years [8, 9]. Due to the similarity in the structure of MOSFET and LDMOS, we can easily assume the process availability of applying InGaAs to the LDMOS structure. Thus, the work proposes InGaAs LDMOS for the power application purpose, which is supposed to obtain the advantage of both LDMOS structure and InGaAs material.

Secondly, to satisfy LDMOS requirements of high-voltage, high current, low-resistance, important device structure parameters are introduced. The electrical properties of the device such as on-resistance, breakdown voltage, saturation current and their mutual influence on the main parameters of device structure are described, which includes the length of drift region, doping concentration, junction depth.

Thirdly, the typical current model of LDMOS is utilized to fully understand the mechanism of the device different from MOSFET. Also the high-voltage LDMOS capacitance is described for the benefit of transient analysis.

Fouthly, for LDMOS as switch in power application, research the effects of LDMOS FOM like Qgd. With the Qgd test bench, Qgd is extracted from mixed mode simulation of LDMOS test circuit.

Finally, to further prove the concept, DC-DC buck converter is utilized as sample to illustrate the performance of InGaAs LDMOS switch such as power efficiency. Both single high-side switch buck converter and synchronous buck converter is applied for the study of InGaAs LDMOS in power applications. Peer comparison with Si LDMOS is made for better observation.

After all, the work is pioneer in exploring new material for LDMOS. Basic device parameters are simulated with Silvaco TCAD tools. The parameters are compared with those of silicon LDMOS with the same structure dimension and doping level condition. The self-heating effect is investigated after that. Finally, the suitability of InGaAs LDMOS as switch in power applications is observed through simulation using DC-DC buck converter. It proves the superior especially in low on resistance thus low conduction loss in switching function. So InGaAs LDMOS is very promising candidate for future power application.

CHAPTER TWO: INGAAS LDMOS DEVICE DESIGN

2.1 LDMOS Material

Two material issues are introduced here. One is InGaAs instead of silicon for the LDMOS bulk. Another is high K material for gate insulation, which is commonly used for Ⅲ-Ⅴ compound material.

2.1.1 InGaAs for LDMOS

Indium gallium arsenide (InGaAs) is a semiconductor composed of indium, gallium and arsenic. It is used in high-power and high-frequency electronics because of its superior electron velocity with respect to the more common semiconductors silicon and gallium arsenide [10].

The optical and mechanical properties of InGaAs can be varied by changing the molecule fraction of In and Ga, $In_xGa_{1-x}As$. In Figure 1 [11], it shows the relationship between long cutoff wavelength and the lattice constant in InGaAs system. The InGaAs device is normally grown on an indium phosphide (InP) substrate.

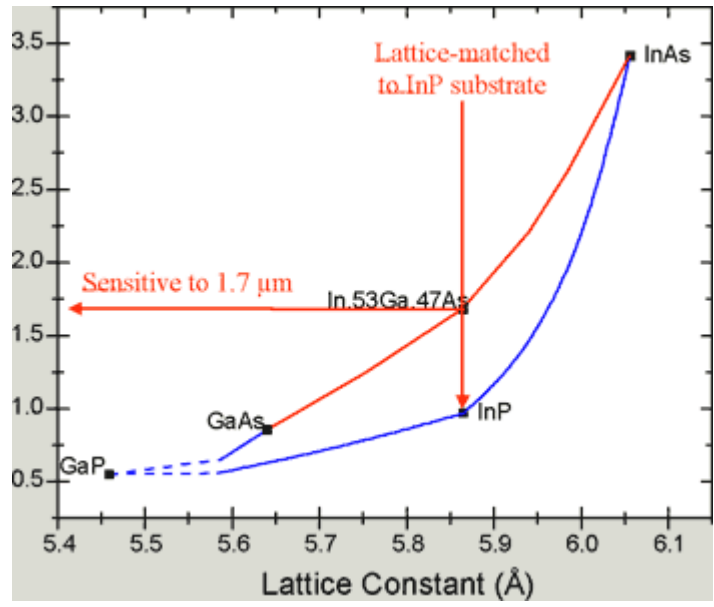Figure 1. Relationship between Cutoff Wavelength and Lattice Constant

In room temperature, the energy bandgap of InGaAs is much smaller than that of silicon, which leads to higher intrinsic charge density. Also the electron mobility of InGaAs is much higher than that of silicon, which usually makes higher current density. Detailed semiconductor property comparisons are provided in Table 1[12].

Table 1. Semiconductor Material Properties

	Si	GaAs	InGaAs	InP
ε	11.8	13.2	14.2	12.5
Eg(eV)	1.08	1.42	0.571	1.35
χ(eV)	4.17	4.07	4.13	4.4
Nc(per cc)	2.8E+19	4.35E+17	1.15E+17	5.68E+17
Nv(per cc)	1.04E+19	8.16E+18	8.12E+18	8.87E+18
ni(per cc)	1.45E+10	2.12E+6	1.56E+13	1.03E+7
Lifetime(el)	1E-7	1E-9	1	1
Lifetime(ho)	1E-7	2E-8	1	1
Vsatn(cm/s)	1E+7	7.7E+6	7.7E+6	1E+6
Vsatp(cm/s)	1E+7	7.7E+6	7.7E+6	1E+6
mun(cm^2/Vs)	1000	8000	N/A	4600
mup(cm^2/Vs)	500	400	N/A	150

Recently InGaAs/InP MOSFET lab sample has been reported [8, 9], which is said to provide record high performance in terms of current handling capability. Notice that there are a lot similarity in structure and process between MOSFET and LDMOS, thus InGaAs/InP LDMOS process is ready at least at lab research level. Future mature factory products are quite optimistic as long as high yield is reached and there is big application need for this.

2.1.2 High k Dielectric

The continuous downscaling of SiO_2 thickness was constrained by issues such as boron penetration in PMOSFET and high leakage current in NMOSFET. To overcome this constraint, new material -- high-k dielectric was proposed. Many candidates of possible high-k gate dielectrics have been suggested to replace SiO_2, as shown in Table 2 [13].

Table 2. Approximate k and bandgap for some of the possible dielectrics

Dielectric	κ	E_{gap}	Dielectric	κ	E_{gap}
SiO_2	3.9	8.9	La_2O_3	30	4.0
Si_3N_4	7	5.1	TiO_2	20-80	~3.5
Al_2O_3	9	8.7	HfO_2	25	5.7
Y_2O_3	15	5.6	ZrO_2	25	5.8
CeO_2	26	5.5	$HfSi_xO_y$	15-25	~6
Ta_2O_5	26	4.5	$ZrSi_xO_y$	15-25	~6

High-k dielectric, as its name suggests, has a higher dielectric constant than the conventional SiO_2. The higher dielectric constant enables the use of a thicker gate dielectric layer to suppress tunneling current while keeping gate capacitance constant at a given EOT. A set of successes have been achieved by using high-k gate dielectrics, such as uniform and controlled layer growth, gate leakage current reduction and integration into small area MOSFET devices.

A major problem introduced by high-k dielectric is the interface defects which will affect the channel electron mobility. For silicon, SiO_2 is a natural choice since it can be grown by simply thermal oxidation. High-k on silicon is more complicated from process point of view. For III-V compound material, there is no dramatic contrast in

process either SiOx or high-k dielectric, since SiO_2 is only natural for silicon. Thus the benefit brought by high-k is much larger than that of SiO_2 while they are similar difficulty for fabrication.

2.2 LDMOS Device Structure

LDMOS is the horizontal double-diffusive silicon MOS technology, that is, diffuse twice within the same window. The channel length is determined by the lateral spread depth difference of the two impurities. The technique implants the same source / drain region twice, one with larger concentration (typical dose of $10^{15}cm^{-2}$) and another implantation of the smaller concentration (typical dose of $10^{13}cm^{-2}$). Thermal annealing process is applied after implantation. Basically Boron has faster diffusion speed than Phosphor in the process. Thus it will form a channel with doping variance. With this technique, the channel length is fully determined by the implantation and thermal diffusion process, while not by the lithographic feature length of MOSFET.

Figure 2 is a common n-channel LDMOS device structure cross section view, in which gate shielding and STI (shallow trench isolation) is provided for higher breakdown voltage. The device active area is made directly through the well on silicon substrate, thus the process is CMOS compatible process.
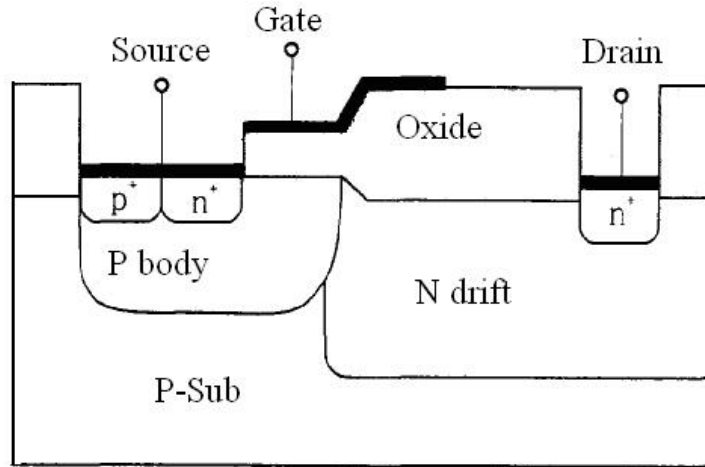
Figure 2. Cross Section of LDMOS

P-body formed in the channel of the LDMOS, it also share the same potential of the source contact. In order to improve the breakdown voltage, there is a high resistive region between source and drain, as the extension of VDMOS area, this layer is known as drift region. Drift region of LDMOS is the key to the design of such devices, the impurity concentration of drift region is low. Hence when high voltage is applied, due to the high resistive drift region, it can withstand higher voltage. The poly plate of LDMOS extends to the top of drift region to act as a field plate, which reduces the surface electric field strength of the drift region, improves the breakdown voltage. The role of the field plate is closely related to the length of plate [14]. At the same time, drift region between the channel and drain acts as buffer, weakens the short-channel effect of LDMOS. When Vds increases, the output resistance will reduce, n-channel will not easily punch through. Thus LDMOS breakdown voltage is not subject to the channel length and doping level of channel, which may carry out an independent design. LDMOS can easily achieve the 0.4-

2μm channel length, so the transconductance g_m, drain current I_{ds}, cutoff frequency f_T, and speed of the LDMOS increases largely than the general MOS.

2.3 Structure Design Issues

LDMOS drift region design is the most important and complex part. This part has significant influence on breakdown voltage, resistance, power consumption, device stability and reliability of LDMOS. Each parameter in the design of drift region will have an impact on device performance, and different process parameters have mutual influence between them. For example, by increasing the length of drift region to improve the breakdown voltage, but it will increase the chip area and the on-resistance. In addition, the voltage and resistance requirement for the concentration and the thickness of the drift region is contradictory. Higher breakdown voltage requires lightly-doped, thick and long drift region, while low on-resistance required heavily doped, thin and short drift region. So the design of LDMOS needs to balance between drift region doping concentration and length, maintaining certain breakdown voltage of the device and achieve the least on resistance.

The main parameters of the drift region include length of drift region L_d, substrate concentration N_{sub}, drift region junction depth t_{drift}. As a result of process determined, substrate concentration can be regarded as constant. The relationship trend of these design parameters to the performance of LDMOS is analyzed and discussed.

2.3.1 RESURF Technology

RESURF (Reduced Surface Field) [15] technology is popular in the design of high-voltage, low-resistance lateral device. The use of this technology can make high breakdown voltage devices, the principle of RESURF is shown in Figure 3.
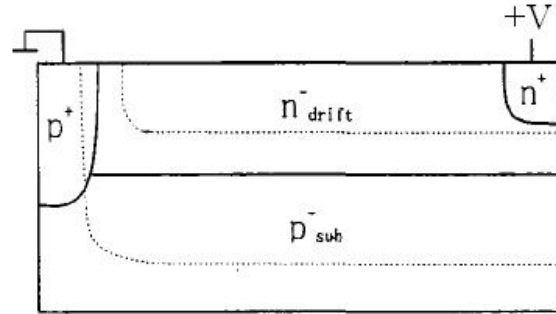
Figure 3. Depletion region distribution

To simplify the discussion, it is assumed that all regions in Figure 3 are uniformly doped. Take the lateral mutation junction p^+/n^-_{drift} and p^-_{sub}/n^-_{drift}, the former one is unilateral mutation node and therefore is breakdown earlier than the latter one. Its building electric field is

$$E = \sqrt{\frac{2 \cdot q \cdot N_{drift} \cdot V}{\varepsilon}} \qquad (2\text{-}1)$$

When the E-field reaches the critical field, the corresponding voltage is called breakdown voltage. The current increases dramatically due to the avalanche impact ionization process. That is E reaches E_c, V_R equals BV.

$$BV = \frac{\varepsilon \cdot E_C^2}{2 \cdot q \cdot N_{drift}} \tag{2-2}$$

For both of the junction of the device to reach breakdown voltage at same time, the thickness of thick drift region has to be reduced such that the drift region is fully depleted. Thus the electric field at the drift region is much more uniformly distributed than single junction and lead to lower peak electrical field as seen in Figure 4, which serves the purpose of enhanced breakdown voltage.
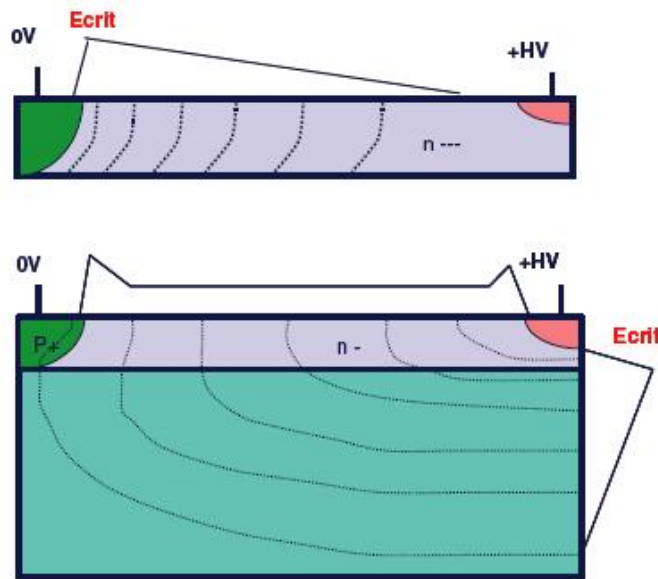

Figure 4. RESURF technology

To better improve the breakdown voltage and reduce resistance, M. M. De Souza and etc. put forward a double RESURF [16] technology. In addition to bottom p/n junction for RESURF, there is a top layer of p_{top}^- added. Due to the existence of p_{top}^- layer, doping concentration of n_{drift}^- can be further increased. So at the same time it can remain

the same breakdown voltage and lower on-resistance. Its schematic diagram is shown in Figure 5.
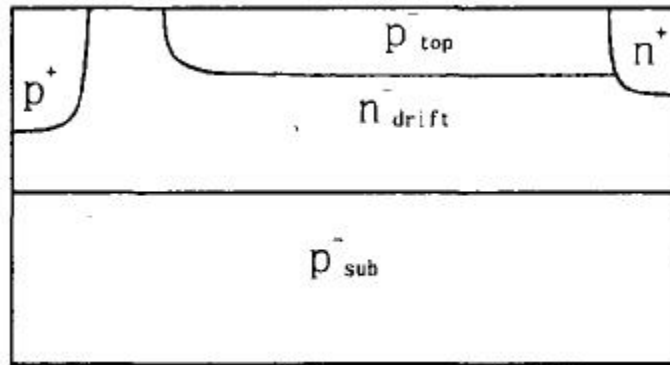
Figure 5. Double RESURF structure

2.2.2 Key Structure Parameters

When designing the device structure, several key parameters should be carefully considered. They are drift region length, drift region doping, gate insulator thickness, and channel related parameters. Even with different material, the trend of parameter optimization is similar for high BV and low Ron design purpose. The relationship between structure parameters and device performance is shown in the following for traditional LDMOS.

Figure 6. BV and Ron vs. drift length L_d

One representative relationship trend can be seen from the Figure 6. It is observed that both the on-resistance and breakdown voltage increases with the increase of length of drift region L_d. It is also observed that when the drift length r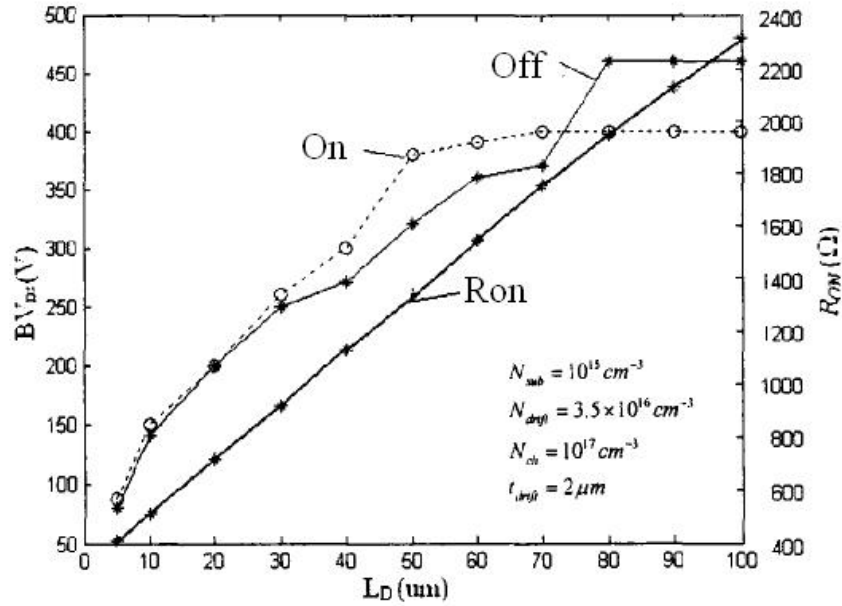eaches certain value, the on-state device and off-state breakdown voltage is no longer a function of drift length. This is mainly due to the reason that at small drift length L_d, the device breakdown voltage is determined by lateral dimension. The vertical breakdown voltage is larger than that of lateral breakdown voltage. Therefore the larger the length of drift region, the higher the lateral breakdown voltage so does the total breakdown voltage. When the length of drift region increases further to certain level, the lateral breakdown voltage surpasses the vertical breakdown voltage, so the device breakdown voltage is determined by the vertical voltage. The vertical dimension remains unchanged, so do the vertical breakdown voltage and the device breakdown voltage.
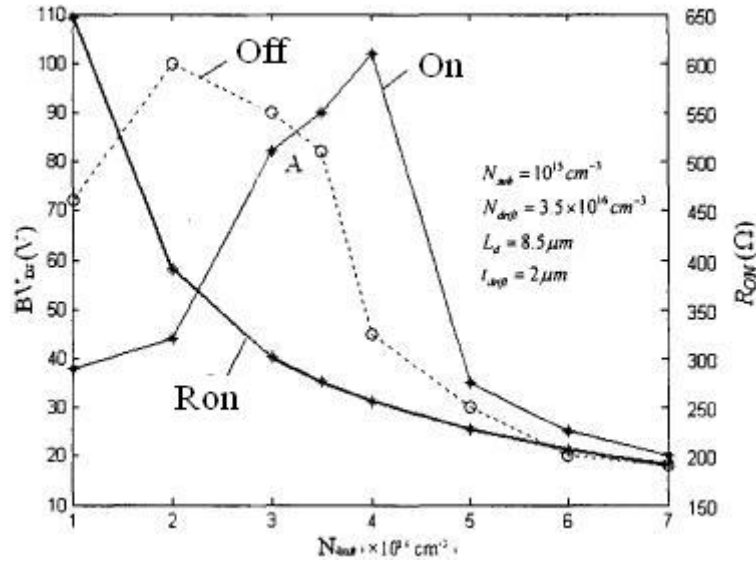
Figure 7. BV and Ron vs. drift region doping N_{drift}

Figure 7 is typical impact of drift region doping concentration on device breakdown voltage and on-resistance. As can be seen from the figure, the on-resistance reduces as the drift region doping concentration increases, which is quite reasonable. It is also observed that both the on-state and off-state breakdown voltage gradually increase to a peak, when the breakdown voltage starts to drop. There is optimal value of the drift region doping concentration for breakdown voltage. Neither too low nor too high drift region doping concentration is good. It is for that if the drift region doping concentration is too low, the drift region depletes too early. When the drain voltage increases, the electric field mainly concentrates in the drain side, which lead to breakdown there. If the drift region doping concentration is too high, it is easier to get to high impact ionization generation rate, which finally lead to avalanche breakdown.
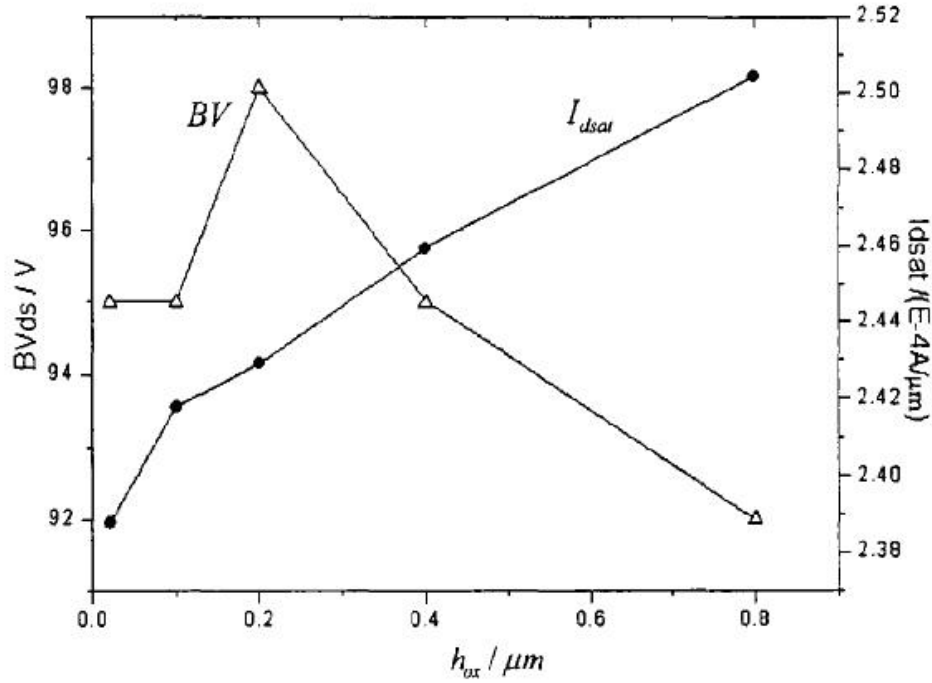
Figure 8. BV and I_{sat} vs. dielectric thickness h_{ox}

It is also worth to find out the relationship of saturation current and dielectric thickness. From the above Figure 8, it is seen that the device saturation current increases as the oxide layer thickness increases. Nearly linear relationship between them can be seen. This is due to that with h,, increasing, device surface electric field is reduced. The reduced surface electric field reduces the surface scattering, electron mobility can be improved, thereby increasing current. At the same time, with the fixed field plate length, the breakdown voltage first increase and then decrease with the increase of dielectric thickness. But the overall breakdown voltage swings in the range of only 6V. This shows that the breakdown voltage is less affected by changes in the thickness of oxide layer.

Last but not least, channel doping determines the threshold voltage. The design of channel doping concentration from the threshold voltage needs to be considered. The LDMOS channel is non-uniform doped due to the specific process, the source side is the biggest doping concentration. The device threshold voltage is determined by the highest doping concentration and therefore should be carefully considered.

2.4 InGaAs LDMOS Design

In this work, a typical InGaAs LDMOS structure is proposed. Figure 9 shows the schematic cross-sectional view of the device structure under investigation. This structure is not optimized for device performance since the main purpose here is to investigate the benefit for using InGaAs LDMOS instead of Si LDMOS in power applications. As traditional LDMOS device structure, an n doped $In_{0.65}Ga_{0.35}As$ drift region is deposit on p InP substrate. The overlap area of p body under the gate contact forms the n-channel current conducting path. To make the device doping profile and structure dimension representative, a typical doping profile is shown in Figure 9.
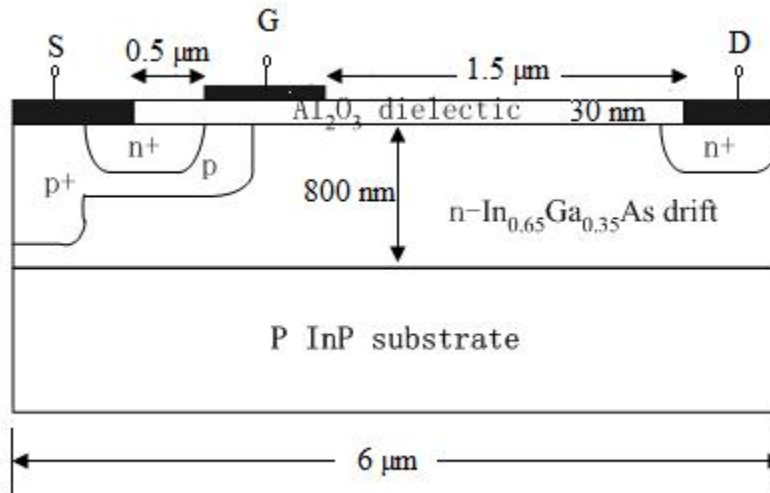
Figure 9. The design of $In_{0.65}Ga_{0.35}As$ LDMOS

Considered different gate dielectric, two cases are designed for comprehensive comparison. One case assumes the same gate dielectric thickness, while the other assumes the same gate capacitance. In the later case, gate dielectric thickness is adjusted to achieve the same gate capacitance as that of SiO_2.

2.5 Chapter Outline

InGaAs material is introduced. It has higher low field electron mobility than that of silicon, which will bring the benefit of large current handling capability for LDMOS. Also for comparison purpose, two design cases are proposed for fair comparison in the later chapter. Several structure dimension and doping parameters are highly relevant to the device performance, there typical relationship is briefly described by reference to silicon LDMOS, since the trend for the relationship is similar despite of material minor

difference. The content in this section provides information needed to build qualified

structure targeted for the special purpose in this work.

CHAPTER THREE: LDMOS ANALYSIS AND MODELING

3.1 LDMOS Physics

This chapter first introduced the basic model equations essential for the study of LDMOS device electric characteristics. These model equations compose the fundamentals for solving the simulation in today's TCAD tools. Then temperature effect is introduced. When considering the heating effect of the device, solve only the traditional basic semiconductor electric equation that has been the model of the device is not accurate any more for the device internal current voltage characteristics. It needs to consider the lattice temperature rise inside the device and its impact on current and voltage characteristics. It is that we need to solve the heat equation coupled with the semiconductor basic electric equation in order to get more accurate electric model of the current and voltage characteristics.

3.1.1 Basic Equations

When thermal effects are not considered, the basic semiconductor equations are poisson equation, electron and hole transport equation, and carrier continuity equation. These equations can be used to describe a unified set of flow distribution and transport situation in all regions of the semiconductor. And it can also be used to describe the distribution of electric potential and field distribution in various regions of the semiconductor. As shown in the following formula [l7]:

$$\frac{d^2V_i}{dx^x} = \frac{q}{\varepsilon}[p - n + N_D^+ - N_A^-] \tag{3-1}$$

$$J_n = q\mu_n nE + qD_n \frac{dn}{dx} \tag{3-2}$$

$$J_p = q\mu_p pE - qD_p \frac{dp}{dx} \tag{3-3}$$

$$\frac{\partial n}{\partial t} = \frac{d\,J_n/q}{dx} - R_n - G_n \tag{3-4}$$

$$\frac{\partial p}{\partial t} = -\frac{d\,J_p/q}{dx} - R_p + G_p \tag{3-5}$$

Among them, the Vi represents electrostatic potential, usually refers to intrinsic Fermi potential [18]; n and p represent the electron and hole concentrations; N_D^+ and N_A^- on behalf of donor and acceptor concentration; q on behalf of electronic charge; ε on behalf of the dielectric constant of semiconductor; Jn and Jp on behalf of electron and hole current density; t on behalf of time; Gn and Gp represent the electron and hole generation rate; Rn and Rp represent the electron and hole recombination rate; μ_n and μ_p represent the electron and hole mobility; Dn and Dp on behalf of electron and hole diffusion coefficient; E on behalf of electric field.

The equations here are described in one dimensional (x axis) format. Equation (3-1) is the Poisson equation, which relates the electrostatic potential to the charge density in a semiconductor. Equation (3-2) and (3-3) are the electron and hole drift-diffusion transport equation, where the drift term (the first) are caused by the electric field and the

second term is caused by the carrier concentration gradient. They are derived from Boltzman-Transport equation with some approximations. Equation (3-4) and (3-5) are carrier continuity equation indicating that the electronic (or hole) concentration changes with time, electronic (or hole) current density gradient (the first), the generation rate, and the recombination rate.

3.1.2 Self-heating Effect

When considering thermal effects, it is important to introduce a new state variable - the lattice temperature. To solve the lattice temperature, there is need for an independent equation excluding the Poisson equation and continuity equation - heat flow equation. In addition, as a result of introduction of lattice temperature, Poisson equation and the current equation will change. Electro-thermal model is taking into account both the semiconductor the basic equations and heat equation, that is, to solve it at the same time lattice heat equation, Poisson equation, the electron and hole transport equation, and the carrier continuity equation.

When the lattice temperature is not uniform in the space, the Fermi level changes with temperature, at this point Poisson equation changes to [18, 19]:

$$\frac{d^2(V_i - \theta)}{dx^x} = \frac{q}{\varepsilon}[p - n + N_D^+ - N_A^-] \qquad (3-6)$$

$$\theta = \chi + \frac{E_g}{2q} + \frac{kT}{2q}\ln(\frac{N_C}{N_V}) \qquad (3-7)$$

Here, θ represents the energy band structure parameters, χ for the electron affinity, T for the lattice temperature, N_C for the effective conduction band density of states, N_V is the effective valence band density of states, k is Boltzmann constant; Eg for the energy band gap.

The transport equation changes to the following form with electric field coupled with temperature field [20]:

$$J_n = q\mu_n nE + qD_n \frac{dn}{dx} + qnD_n^T \frac{dT}{dx} \tag{3-8}$$

$$J_p = q\mu_p pE - qD_p \frac{dp}{dx} - qpD_p^T \frac{dT}{dx} \tag{3-9}$$

Which, in addition to the drift term caused by the electric field (the first) and the diffusion term caused by carrier concentration gradient (the second), also taking into account the current caused by the lattice temperature gradient (third). The lattice temperature gradient is the source of heat generated current. D_n^T and D_p^T are the electron and hole thermal diffusion coefficient respectively.

Well-known heat conduction equation (or heat equation) as follows:

$$\rho \cdot c \cdot \frac{\partial T}{\partial t} = H + \vec{\nabla}(\lambda(T)\vec{\nabla}T) \tag{3-10}$$

T is the absolute temperature of the lattice, unit K; ρ representative the material quantity density, unit g/cm^3; c is the material specific heat, units $J/g \cdot K$; H represents the density of heat generated (that is, on behalf of the heat source), unit W/cm^3; λ is the

thermal conductivity of the material, unit W/cm·K. The formula shows the relationship between the lattice temperature and time under the influence of the heat source.

Recent years, the model equation for H in the electro-thermal model has been continuously developed. The model will differentiate considered whether or not the carrier energy balance equation is included [21-23]. Further information on heat transfer will not be described in the chapter as long as the major equations are provided for LDMOS device modeling and simulation.

3.2 Modeling of LDMOS

LDMOS is formed from double-diffused lateral channel. Impurities show an exponential change along the channel length direction and an n-drift region exists between the drain and channel. So the ordinary method of calculating MOS drain current [24] can not be directly applied in the LDMOS. The LDMOS channel current and drift region current are calculated in the following sections.

3.2.1 Channel Current

The LDMOS channel areas could be taken as an enhanced MOSFET transistor to derive the current equation. Several assumptions have to be made before calculation.

1. It is assumed to be a graded channel. That is the vertical electric field gradient is much smaller than the horizontal electric field gradient. Thus the channel can be processed using one dimensional method.

2. The channel doping concentration follows the following distribution [25]:

$$N(x) = N_0 \exp(-\frac{\alpha}{L}x) \qquad\qquad (3\text{-}11)$$

Where, N_0 is the boundary doping concentration; L is the channel length; α

is the fitting parameter, $\alpha = \ln[\dfrac{N_0}{N(L)}]$.

3. Neglect diffusion current, only count on drift current.

4. Assume the effect oxide charge density to be constant.

When Vds is small, the device is operation in linear region and it can be assumed that the voltage is linearly distributed along the channel.

$$V(x) = \frac{V_{ch}}{L}x \qquad\qquad (3\text{-}12)$$

Vch is channel voltage.

Due to that the channel is not uniformly doped, the depletion thickness under reversion layer is not the same along the channel. From Figure 10, $Q_G(x)$ is the gate charge density, $Q_n(x)$ is the carrier density in the inversion layer, and $Q_d(x)$ is the depletion charge density. Thus we have

$$Q_n(x) + Q_d(x) = Q_G(x) \qquad\qquad (3\text{-}13)$$

$$Q_G(x) = -C_{ox}[V_{GS} - V_{FB} - 2\phi_F - V(x)] \qquad\qquad (3\text{-}14)$$

$$Q_d(x) = -\sqrt{2q\varepsilon_0\varepsilon_{Si}N_A(x)[2\phi_F + V(x)]} \qquad\qquad (3\text{-}15)$$
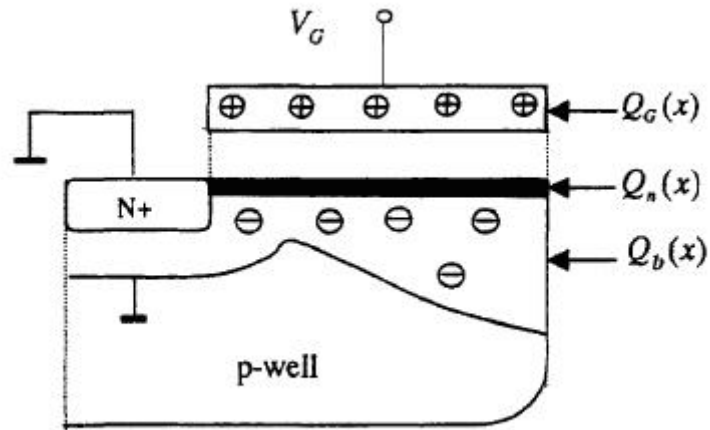
Figure 10. LDMOS channel charge

Bring equation (3-14) and (3-15) into equation (3-13), we get

$$Q_n(x) = -C_{ox}[V_{GS} - V_{FB} - 2\phi_F - V(x)] + \sqrt{2q\varepsilon_0\varepsilon_{Si}N_A(x)[2\phi_F + V(x)]} \qquad (3\text{-}16)$$

Given the mobility μ by appropriate mobility model [26, 27] considering lattice scattering and etc., channel current under strong inversion can be expressed as:

$$I_{ch} = -WQ_n(x)\frac{\mu E}{1 + E/E_{sat}} \qquad (3\text{-}17)$$

Esat is the electric field when carrier reaches saturation velocity.

3.2.2 Drift Region Current

Mainly the drift region is treated as a resistor to derive the current, even though the height of the resistor is changing with the applied drain voltage. In N-well drift region, there is a smaller depletion layer as part of the p_{sub}/n^-_{drift} junction. When the drain voltage is low, the depletion layer thickness is negligible. So the whole N-well drift region depth can be taken for conduction layer. With the increasing of drain voltage, the depletion layer boundary in the n-well drift region will further advance to the device surface, which leads to smaller current flowing area and increased drift region resistance.

Suppose the horizontal direction along the drift region is x axis and point from channel to drain, where the boundary of channel and drift region is x = 0. The average doping concentration for the drift region is

$$\overline{N_D} = \frac{1}{X_{jn}} \int_0^{X_{jn}} [N_A(x) - N_S] dy + N_S \tag{3-18}$$

X_{jn} is depth of the drift region; N_S is doping concentration of the substrate.

The depletion thickness in the drift region side of the p_{sub}/n^-_{drift} junction is written as h(x). Take the junction as abrupt junction, we get

$$h(x) = \sqrt{\frac{2\varepsilon_0\varepsilon_{Si}N_S}{qN_D(N_D + N_S)}[V(x) + V_{br}]} \tag{3-19}$$

Vbr is the p_{sub}/n^-_{drift} junction built-in potential.

The area S(x) the drain current flows through is:

$$S(x) = W_d[X_{jn} - h(x)] \tag{3-20}$$

Wd is the width of drift region.

So after choosing appropriate simplified mobility model considering lattice scattering, the drain current flowing through drift region is:

$$I_{drift} = S(x)q\overline{N_D} \frac{\mu E}{1 + E \big/ E_{sat}} \tag{3-21}$$

The full drain current takes the capacity of channel current and drift region current, that is the smaller one determines the current of LDMOS. For power application in this work, the device as switch operates with very low Vds and the current is mainly determined by formula (3-17) channel current.

3.2.3 Channel On-resistance

LDMOS on-resistance is an important parameter, the value of which is closely related with the maximum output power of LDMOS. LDMOS as a result of non-uniform channel doping, the complex and diverse high resistive drift region, therefore is hard to get the accurate analytic models [28-30].

Channel region is non-uniformly doped. Take into account LDMOS is operating in linear region when calculating on-resistance, so graded channel can be used as approximation, and drain-source voltage is also linear distribution [31, 32] along the channel.

$$I_{ch} = -WQ_n(x)\mu_{eff}\frac{dV}{dx} \qquad (3\text{-}22)$$

$$V(x) = \frac{x}{L}V_{ch} \qquad (3\text{-}23)$$

I_{ch} is the drain-source current; $Q_n(x)$ is carrier density in the inversion layer;

μ_{eff} is the effective mobility; L and W are the channel length and width; V_{ch} is the

channel voltage. Using the carrier continuity equation and some approximations, we can

get the current expression combining formula (3-22) and (3-23).

$$I_{ch} = \mu_{eff}C_{ox}\frac{W}{L}[V_{GS} - 2\phi_B - V_{FB} - \frac{2}{\alpha(e^{\frac{\alpha}{2}}-1)}\frac{qN_0x_{d0}}{C_{ox}}]V_{ch} \qquad (3\text{-}24)$$

$$x_{d0} = \sqrt{\frac{4\varepsilon_0\varepsilon_{Si}\phi_B}{qN_0}} \qquad (3\text{-}25)$$

Where, Vgs is the gate-source voltage; V_{FB} for Flat-band voltage; C_{ox} for gate

oxide capacitance. The linear channel resistance can simply be derived from Vch

divided by Ich, which is quite straightforward.

3.2.4 Drift Region On-resistance

The case of high resistance drift region is much more complicated than the

channel region. \Since the field plate has the bellowing carrier accumulation layer,

current from the channel flow through the accumulation region, diverge to the high

resistance layer and finally reach the drain area. That is the current flow through the

process of accumulation layer, the initial part is non-divergent, expands at the latter part,

and then flow parallel to the bottom in the main areas of high resistance region until reaching the drain. The drift region resistance can be written as

$$R_{drift} = R_{ac} + R_{sp} + R_{sh} + R_{cd} \qquad (3\text{-}26)$$

Rac is the resistance of accumulation region; Rsp is spreading resistance; Rsh is resistance of the non-uniform doping body; Rcd is resistance of the body below the corresponding drain.

3.3 Dynamic Characteristics of LDMOS

In the high-voltage drive circuit, LDMOS device as the output stage in circuit is used for the current/voltage conversion. So there are a lot of charging and discharging operations for LDMOS. Because of this, the modeling of LDMOS devices transient characteristics is essential. In the analysis of high-voltage drive circuit transient characteristics, LDMOS device capacitance effects must be taken into account. Only when the capacitance effect of LDMOS devices is accurately reproduced by the model, the circuit performance can be accurately assessed.

For high-voltage LDMOS devices, the charge-control theory is often used to analyze and calculate capacitance. At charge-control theory, current and voltage are not subject to control. The theory uses the controlled charge of different regions to establish equations that will present controlled charge as function of voltage [33, 34], which mainly include controlled charge between source and gate, source and drain charge, gate and drain. Here is a brief analysis of capacitance for the LDMOS.

For MOSFET, Cgs, Cgd, and Gdb are the main consideration for circuit design. There is similarity between LDMOS and MOSFET for the respective capacitor. But due to asymmetry of LDMOS, Cgs and Cgd do not follow the same trend of MOSFET. They are not equal anymore due to that source and drain can not be switched for LDMOS.

A brief description follows here. Gate/source capacitance Cgs consists of two parts: gate/channel capacitance and gate/source overlap capacitance. Gate/drain capacitance Cgd is composed of two parts: gate/channel capacitance and gate/drift overlap capacitance. Drain/source capacitance Cds is simply a p/n junction capacitance. Detailed model can be referred from that of MOSFET with specific attention to the drift region of LDMOS.

3.4 Chapter Outline

InGaAs LDMOS materials are introduced besides traditional Si LDMOS. They are Ⅲ-Ⅴ compound material for the bulk of LDMOS and high k dielectric for gate insulation. Then five basic semiconductor equations are described, which compose the basis for calculation and simulation of LDMOS device. Equations coupled with lattice temperature are important for more accurate calculation of the device. Finally the current model is derived, with on-resistance and parasitic capacitance analyzed. With this basis, it helps to get full picture of LDMOS and its unique advantage compared with traditional MOSFET and Si LDMOS. After all, the content in this chapter paves the way for further simulation and study of InGaAs LDMOS.
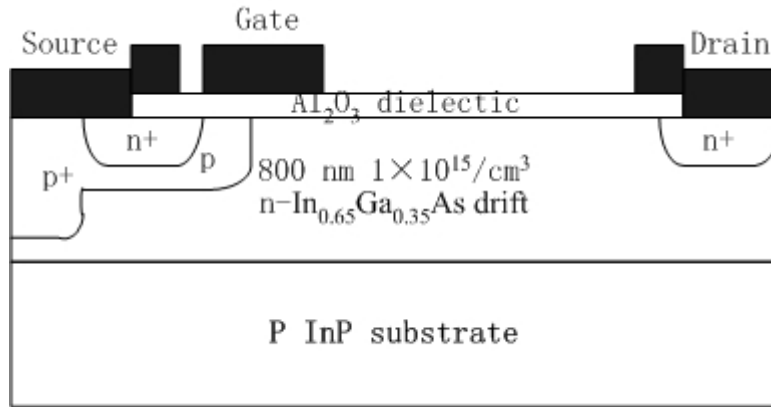
CHAPTER FOUR: INGAAS LDMOS PERFORMANCE

4.1 InGaAs LDMOS Performance

In this chapter, we investigate the performance of using $In_{0.65}Ga_{0.35}As$ as building material for LDMOS device. Its inherent high electron mobility leads to high current density and high cut-off frequency. Also good off-state breakdown voltage, low on-resistance and low on-state voltage drop are anticipated. For better illustration, performance improvements made by $In_{0.65}Ga_{0.35}As$ LDMOS are compared with Si LDMOS in the same structure and doping conditions.

4.1.1 Environment Setup

In recent years, great efforts have been given to the cross section optimizations [35-38] and 3-D layout refinements [39] in the LDMOS design. Figure 11 shows the schematic cross-sectional view of the device structure under investigation. As traditional LDMOS device structure, an n doped $In_{0.65}Ga_{0.35}As$ drift region is deposit on p InP substrate. The overlap area of p body under the gate contact forms the n-channel current conducting path. To make the device doping profile and structure dimension representative, a typical doping profile is shown in Figure 11. A 30 nm and 70 nm thick Al_2O_3 layer is chosen here as gate dielectric, similarly HfO_2 and HfAlO or other high-κ dielectrics could also be applied. The length of n-channel is set to a value of 0.5 μm. In the following device simulation, a Si LDMOS with 30 nm gate thickness is compared in FOM such as breakdown voltage, on-resistance Ron, gate charge Qg, and Ron·Qg. In the

37

following sections, 30 nm and 70 nm gate insulator thickness $In_{0.65}Ga_{0.35}As$ LDMOS is abbreviated as InGaAs LDMOS and InGaAs_Cg LDMOS, respectively. InGaAs_Cg LDMOS is the device with adjusted gate dielectric thickness to reach the same gate capacitance as Si LDMOS.


(a)
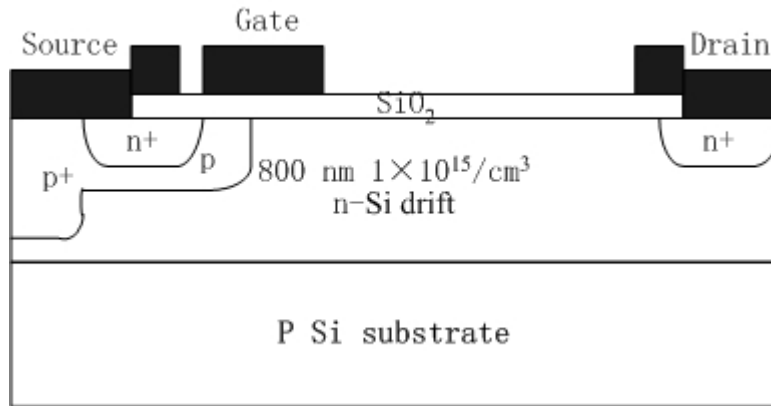
(b)

Figure 11. The cross-section structure of (a) $In_{0.65}Ga_{0.35}As$ LDMOS and (b) Si LDMOS

4.1.2 InGaAs LDMOS Performance

The device simulation is carried under the Silvaco 2D TCAD simulators [40]. In the simulation of snapback curve and output current characteristic, the default mobility models used are lattice temperature dependent with model parameters adjusted for In rich InGaAs. Self-heating effects are considered by using the thermodynamic model, and the substrate contact is set to reference temperature of 300K. Temperature dependent impact ionization models are used in these two simulations.
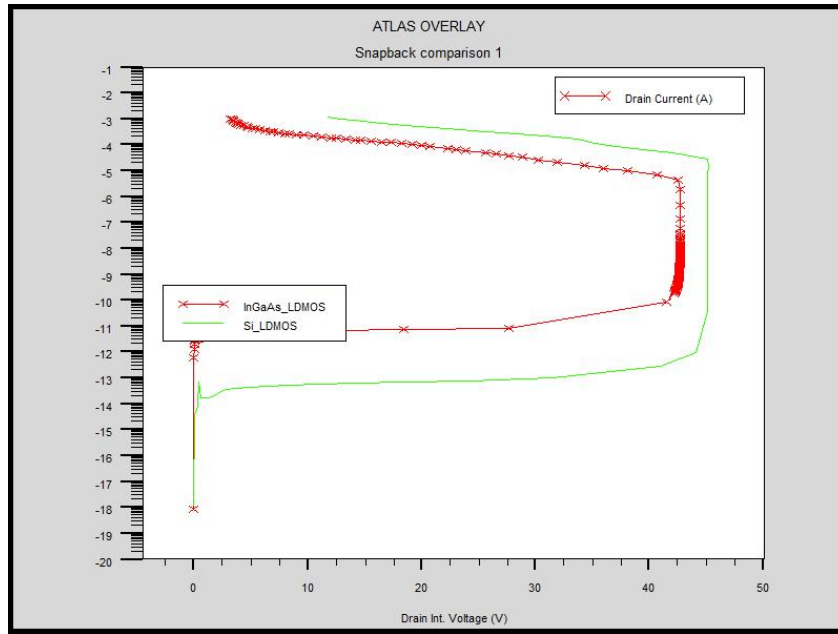
(a)
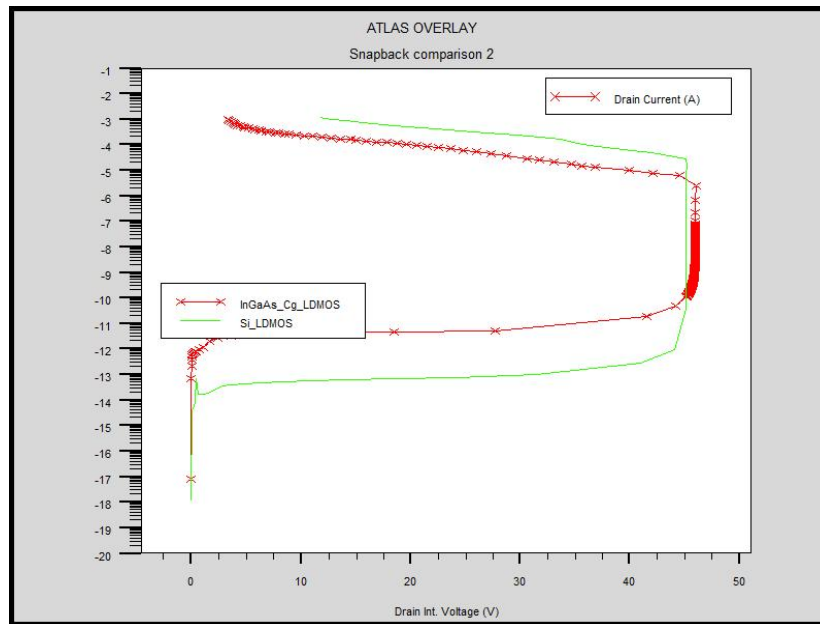
(b)

Figure 12. The comparison of snapback curve for In$_{0.65}$Ga$_{0.35}$As and Si LDMOS with (a) the same thickness of gate dielectric and (b) the same gate capacitance

Figure 12 shows the comparison of snapback curve for $In_{0.65}Ga_{0.35}As$ and Si device with the same gate dielectric thickness and the same gate capacitance. It is observed that the 47V breakdown voltage of Si LDMOS is higher than the 43V breakdown voltage of InGaAs LDMOS. But the 48V breakdown voltage of InGaAs_Cg LDMOS is a bit higher than that of Si LDMOS.
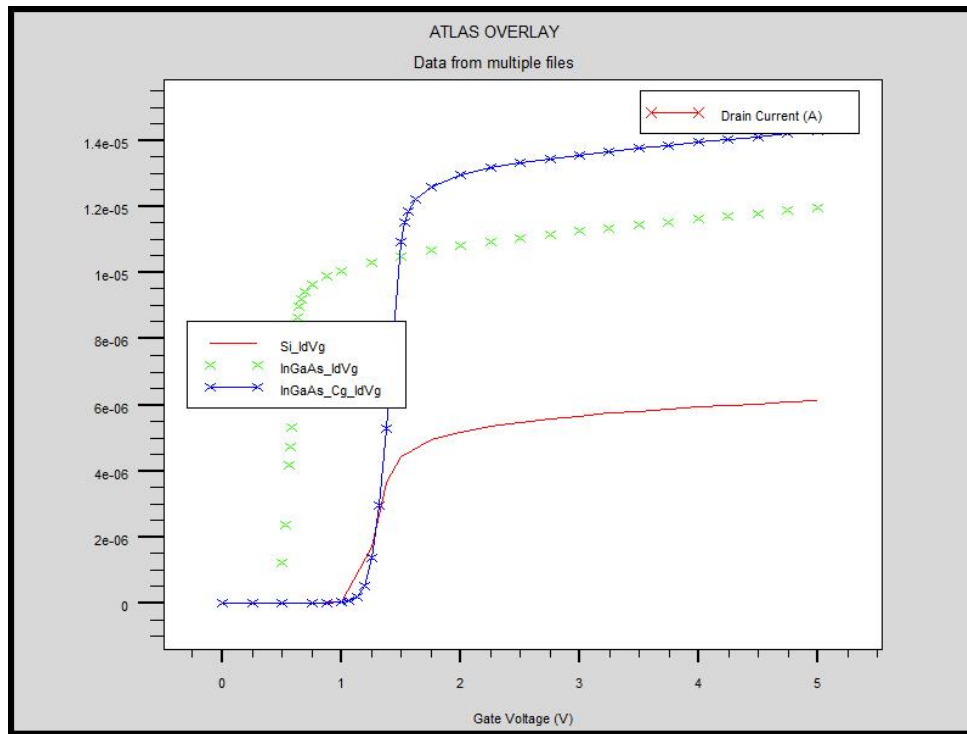

Figure 13. DC transfer characteristics for Si, InGaAs, and InGaAs_Cg LDMOS

The DC transfer characteristic curve is shown in Figure 13. It shows that the threshold voltage Vt of InGaAs LDMOS is smaller than that of Si LDMOS. Vt of MOSFET is related with several factors such as material affinity, bandgap, metal workfunction, gate dielectric, channel doping, drift doping, and etc. Using the Vt model

in MOSFET as an approximation, the smaller Vt in InGaAs LDMOS has two major

reasons: high k gate dielectric and lower band gap of $In_{0.65}Ga_{0.35}As$ compared to Si.
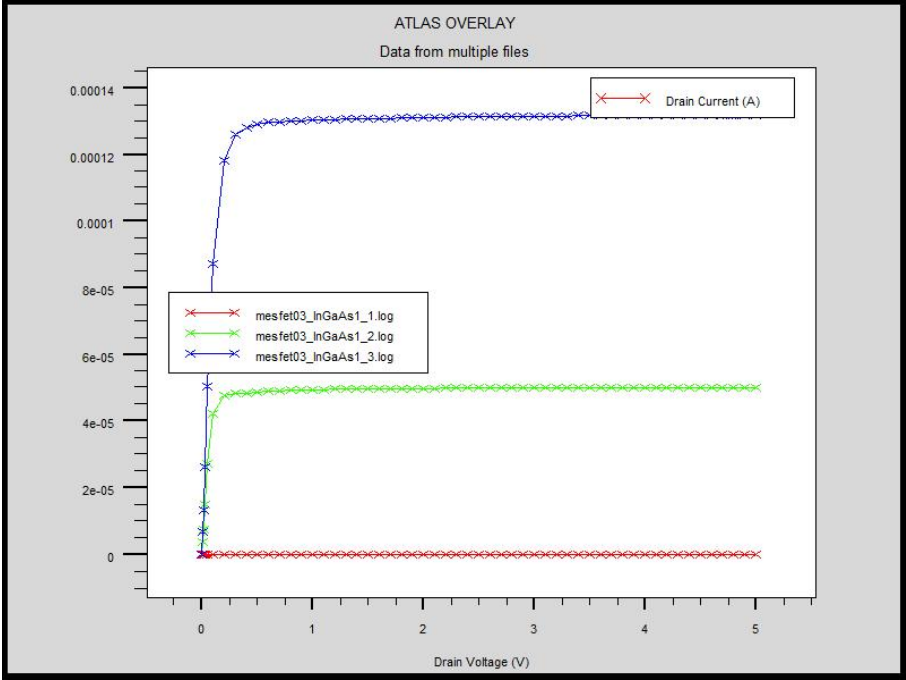
(a)
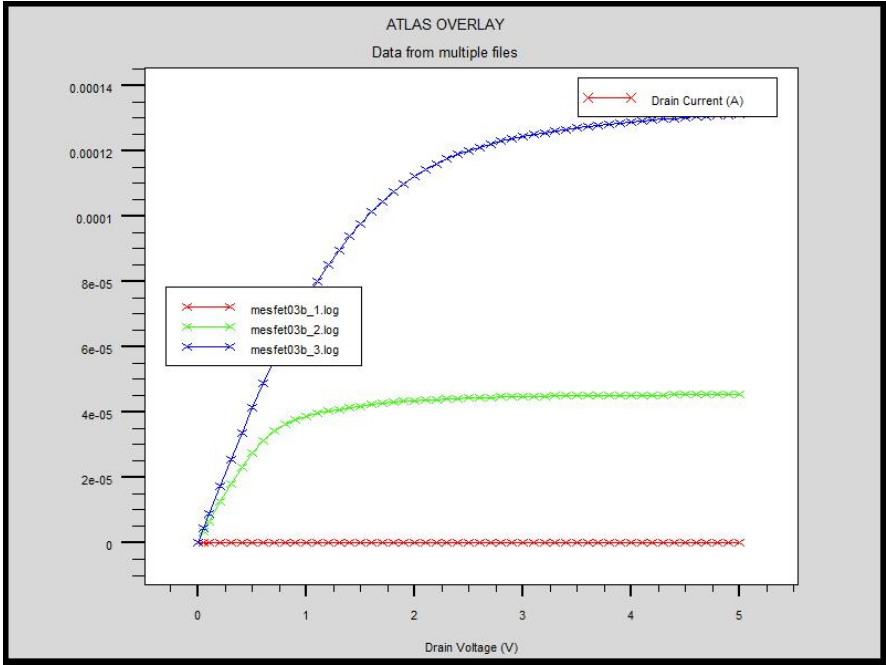
(b)

Figure 14. I-V characteristic of (a) InGaAs_Cg LDMOS and (b) Si LDMOS

Figure 14 shows the DC characteristic of the two devices with gate voltage from 1 to 3 V at a step of 1 V. The device has a channel length of 0.5 µm and a drift length of 2.5 µm. The rising of current density of the $In_{0.65}Ga_{0.35}As$ LDMOS in linear region is much larger than that of Si mainly due to much higher electron mobility. It is calculated from the DC curves that the on-resistance of Si, InGaAs, and InGaAs_Cg LDMOS with 30mm device width reaches 0.296Ω, 0.022Ω, and 0.024Ω, respectively. Consider the active FET area, the on-resistance is 36mΩ·mm2, 2.67mΩ·mm2, and 2.9mΩ·mm2, respectively. $In_{0.65}Ga_{0.35}As$ LDMOS shows much lower on-resistance than that of Si LDMO in both situations.

4.1.3 InGaAs LDMOS Gate Charge
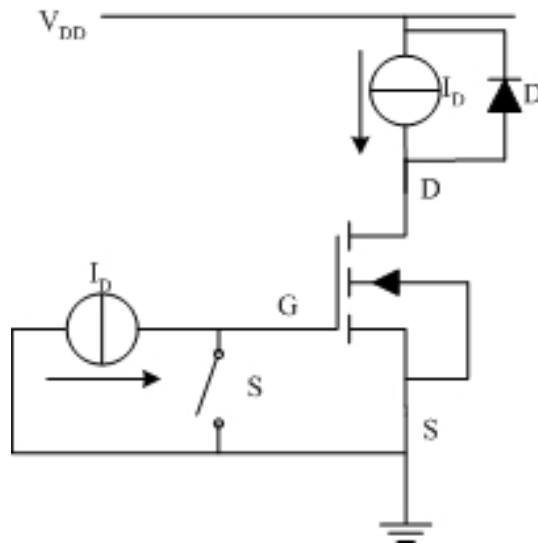

Figure 15. Gate charge Qg test bench circuit

The gate charge Qg investigated includes Qgs and Qgd. The principle of the test bench circuit used in mixed-mode simulation is shown in Figure 15. The initial circuit state comes with the switch 'S' closed. At time t0, the switch is open and the current 'ID'

is pumped into gate-source capacitor which raises the gate-source voltage Vgs(V[1] in Figure 16). At a certain point after threshold voltage, the gate current begins to charge the gate-drain capacitor. Then the drain voltage Vds(V[2] in Figure 16) begins to fall rapidly while Vgs remains the same. After Vds falls to Zero, the gate continues charging gate-source capacitor and give rise to Vgs. $Qg = Ig \times (t1-t0)$, where t1 is taken as the moment when Vgs arrives 5V or more to make sure that the switch is open sufficiently.
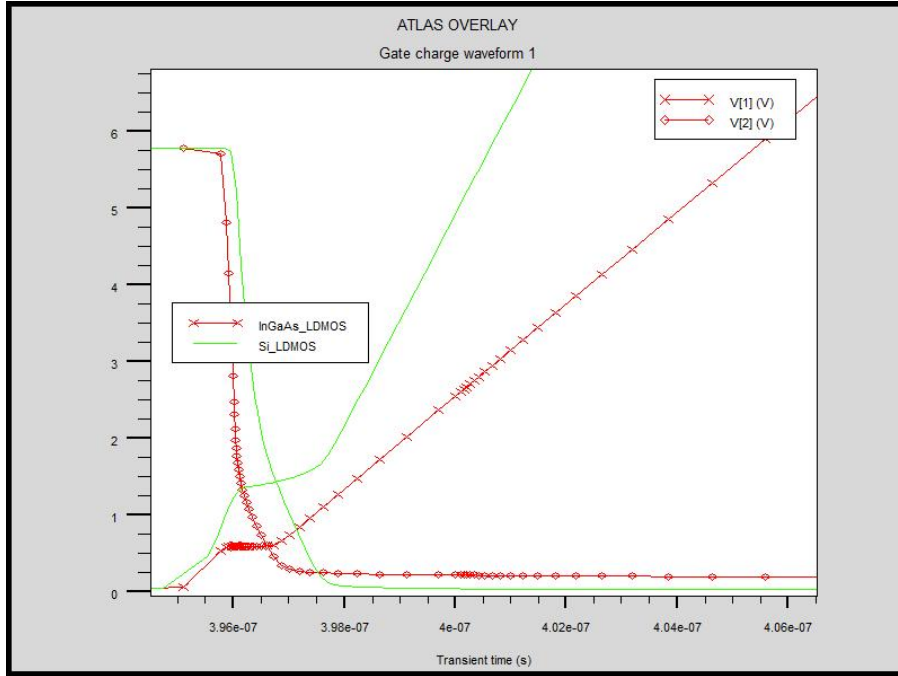
(a)
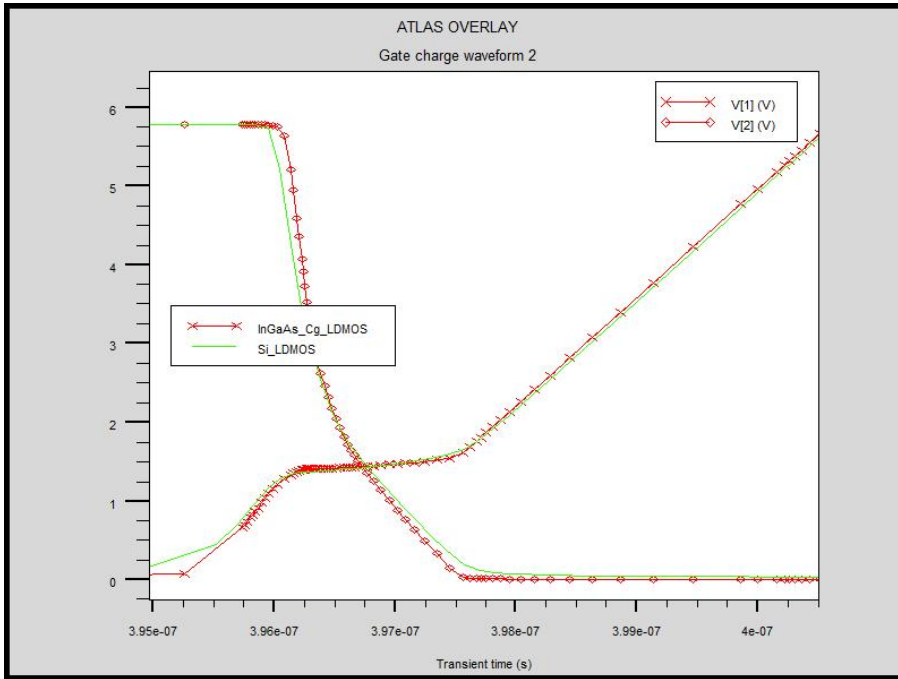
(b)

Figure 16. Gate charge Qg comparison between $In_{0.65}Ga_{0.35}As$ LDMOS and Si LDMOS with (a)

the same gate dielectric thickness and (b) the same gate capacitance

4.2 Performance Analysis

To get an insight into the avalanche breakdown which occurs in the parasitic diode, the electric field distribution is plotted in Figure 17. As can be seen, the maximum E-field in the In0.65Ga0.35As LDMOS occurs around the boundary of drain and drift region, it reaches 5.85×10^5 V/cm, 5.66×10^5 V/cm, 5.83×10^5 V/cm for Si, InGaAs, and InGaAs_Cg respectively.
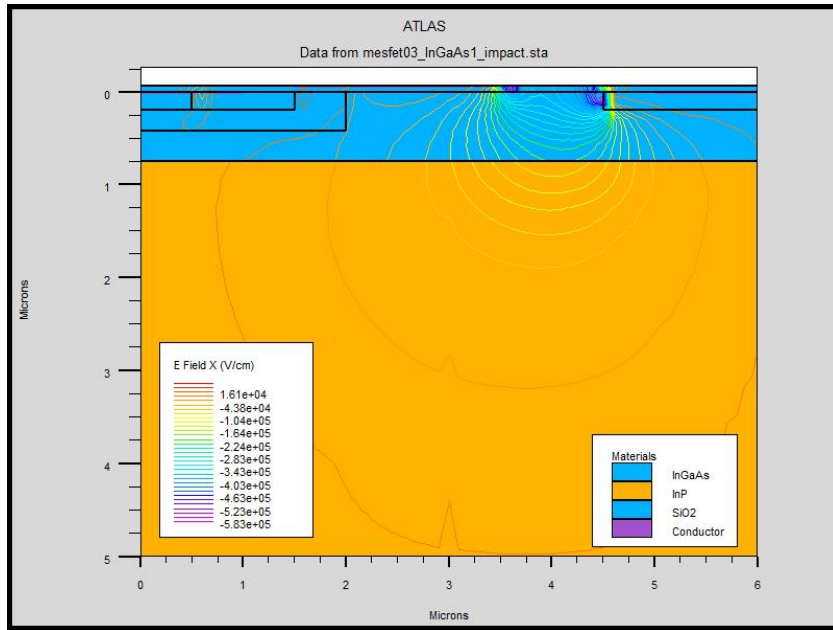
(a)
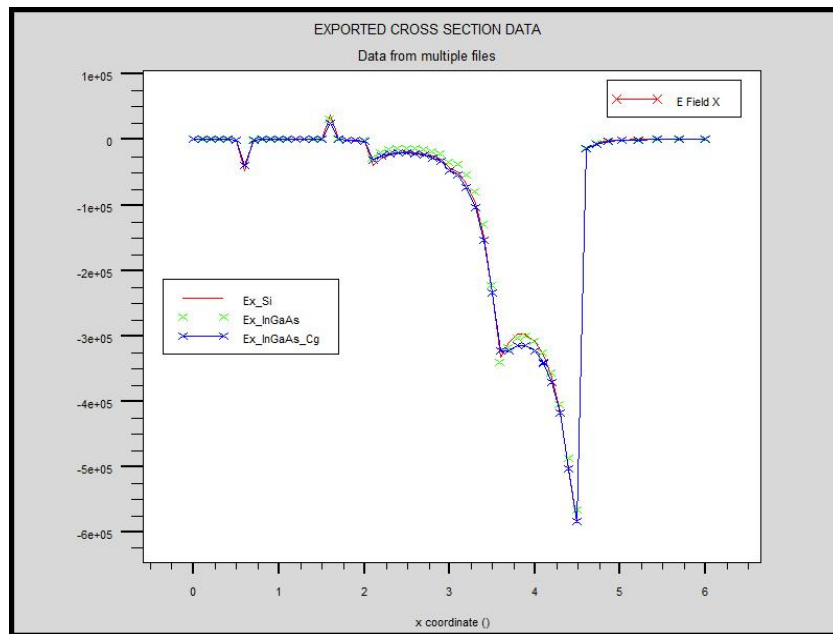
(b)

Figure 17. X-direction electrical field (a) 2-D distribution from InGaAs LDMOS (b) comparison

between different devices

A simple model of impact ionization rate α is a function of electric field ε:

$$\alpha = A \cdot e^{-B/\varepsilon} \qquad (1)$$

In the snapback simulation, comprehensive Selberherr's model[8] is included which relates α to the lattice temperature. Two-dimensional impact ionization generation rate is shown in Figure 18(a). The result is taken when breakdown current reaches 1×10-6 A/μm.
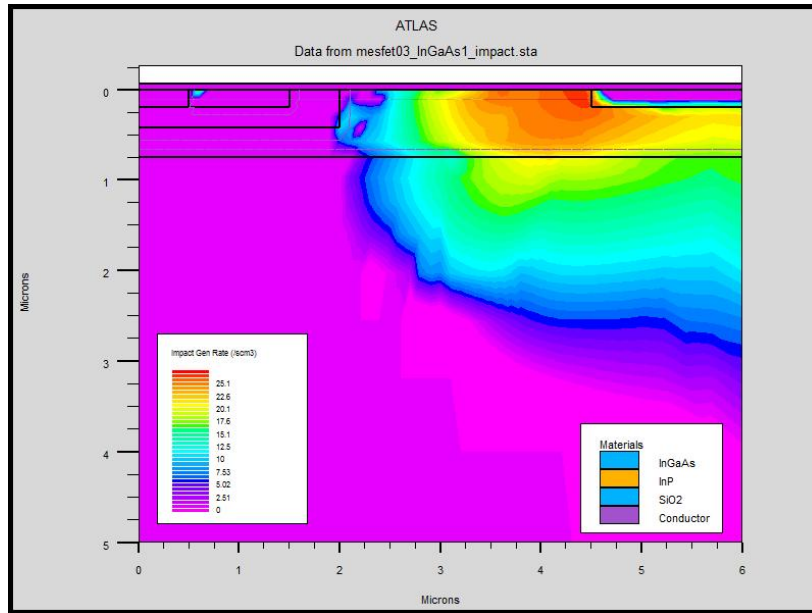
(a)
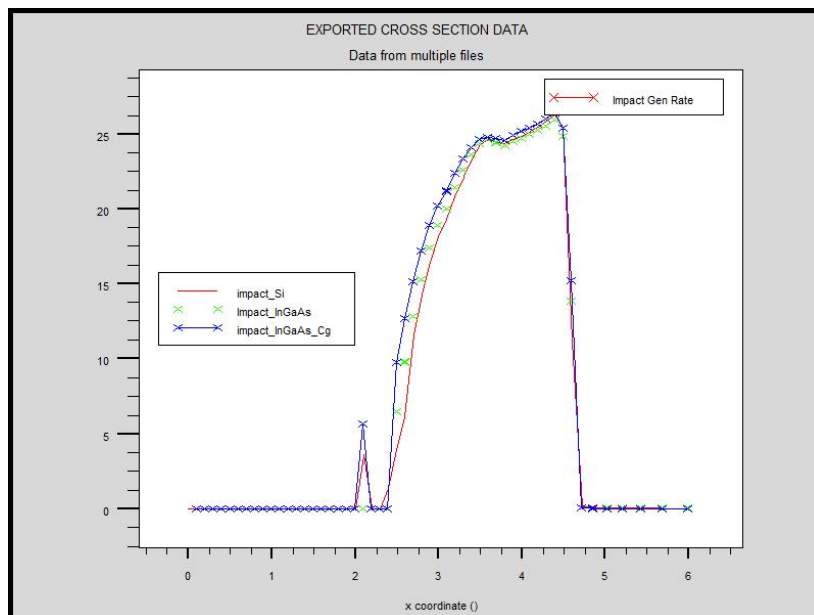
(b)

Figure 18. Impact ionization rate (a) 2-D distribution from InGaAs LDMOS (b) comparison

between different devices

Figure 18(b) shows the impact ionization rate for all 3 devices along the horizontal line 0.1 μm below the material-insulator interface. It shows a slightly bigger integral area of impact generation rate for InGaAs_Cg LDMOS. It partly helps the device to bear a higher breakdown voltage.

For a better understanding the FOM Ron×Qg from experiment, let us use the simple current model from MOSFET as estimation for on-resistance.

$$R_D \propto \frac{1}{\mu \cdot Cox \cdot \frac{W}{L} \cdot (V_{GS} - V_{th})} \tag{2}$$

Qg is rewritten as the following equation.

$$Q_g = I_D \times t = \int_{t_0}^{t_1} C_g \cdot \frac{dV}{dt} dt \propto Cox \cdot W \cdot L \int_{t_0}^{t_1} dV \tag{3}$$

here for rough estimation, Cgs and Cgd is assumed to equal to Cox·W·L. Combine equation (2) and (3), Ron×Qg can be calculated as:

$$R_{on} \times Q_g \propto \frac{L^2 \cdot \int_{t_0}^{t_1} dV}{\mu \cdot (V_{GS} - V_{th})} \tag{4}$$

Thus, FOM of device is proportional to the square of channel length and inverse to the carrier mobility. Thus the higher mobility helps Ron×Qg of In0.65Ga0.35As LDMOS to be smaller than that of Si LDMOS.

Finally, the following table listed the performance comparison between the work here and the work reported by others [41-43]. From the Table 3, we can see InGaAs LDMOS proves to be good candidate for power applications.

Table 3. Overall performace comparisons

	Si LDMOS	InGaAs LDMOS	InGaAs_Cg LDMOS	Toshiba Si LDMOS	HEMTs	Philips Si Trench MOSFET
FET area	0.12 mm^2	0.12 mm^2	0.12 mm^2	5.9 mm^2	2 mm^2	
BV(V)	40 V	40 V	40 V	35 V	>35 V	21 V
Vth(V)	1 V	1 V	1 V	1.5 V	7.4 V	
Rdson	$36 \text{ m}\Omega\text{-mm}^2$ @ Vgs=5	$2.67 \text{ m}\Omega\text{-mm}^2$ @ Vgs=5	$2.9 \text{ m}\Omega\text{-mm}^2$ @ Vgs=5	$12.2 \text{ m}\Omega\text{-mm}^2$ @ Vgs=7	$2.5 \text{ m}\Omega\text{-mm}^2$ @ Vgs=7	$5 \text{ m}\Omega\text{-mm2}$ @ Vgs=10
Qgd	0.84 nC/mm^2	1.5 nC/mm^2	0.84 nC/mm^2	0.82 nC/mm^2 @ Vdd=11	0.62 nC/mm^2 @ Vdd=11	3.6 nC/mm^2
FOM	$30.2 \text{ m}\Omega\text{nC/mm}^2$ @ Vgs=5	$4 \text{ m}\Omega\text{nC/mm}^2$ @ Vgs=5	$2.4 \text{ m}\Omega\text{nC/mm}^2$ @ Vgs=5	$10 \text{ m}\Omega\text{nC/mm}^2$ @ Vgs=7 Vds=11	$1.6 \text{ m}\Omega\text{nC/mm}^2$ @ Vgs=0 Vds=11	$18 \text{ m}\Omega\text{nC/mm}^2$ @ Vgs=10

4.3 Chapter Outline

In this chapter, we study the new $In_{0.65}Ga_{0.35}As$ LDMOS instead of traditional Si. The cross-sectional structure dimension and doping profile are described. Two situations of InGaAs LDMOS dimension are considered during the simulation using Silvaco TCAD tools, one with the same gate thickness as Si LDMOS and the other with the same gate capacitance as its Si peer. The key parameters of the novel devices are extracted and compared with Si LDMOS. The breakdown voltage, DC characteristics, on-resistance, gate charge, and FOMs are examined and discussed. Due to the specific material superior like electron mobility enhancement, the FOM of InGaAs LDMOS beats that of Si

LDMOS for an 87.9% improvement. Also it is found that the FOM of LDMOS is less relevant to the gate capacitance. At last, we believe that based on this work, InGaAs LDMOS and all other compound semiconductor LDMOS will be future choice of high performance devices in power applications.

CHAPTER FIVE: EVALUATION FOR POWER CIRCUIT

5.1 DC-DC Buck Converter

To evaluate the performance of LDMOS as a switch in power applications, LDMOS is placed in a simple DC-DC buck converter as example. A buck converter is a step-down DC to DC converter. Its design is similar to the step-up boost converter, and like the boost converter it is a switched-mode power supply that uses two switches (a transistor and a diode) and an inductor and a capacitor.
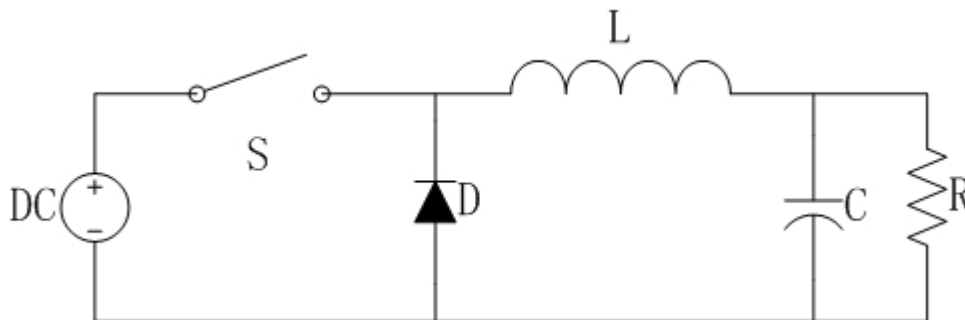
5.1.1 Circuit Scheme

Figure 19. Schematic of DC-DC buck converter

A simple buck converter schematic is shown in Figure 19. From the figure, there are switch and diode that control the current through the inductor. Thus by controlling the duty cycle D of the switch, the output voltage is D ratio of input voltage. There are CCM and DCM operation modes for the converter, which represents continuous or

discontinuous current conduction through the inductor. Normally CCM mode is the focus and the case in this work.
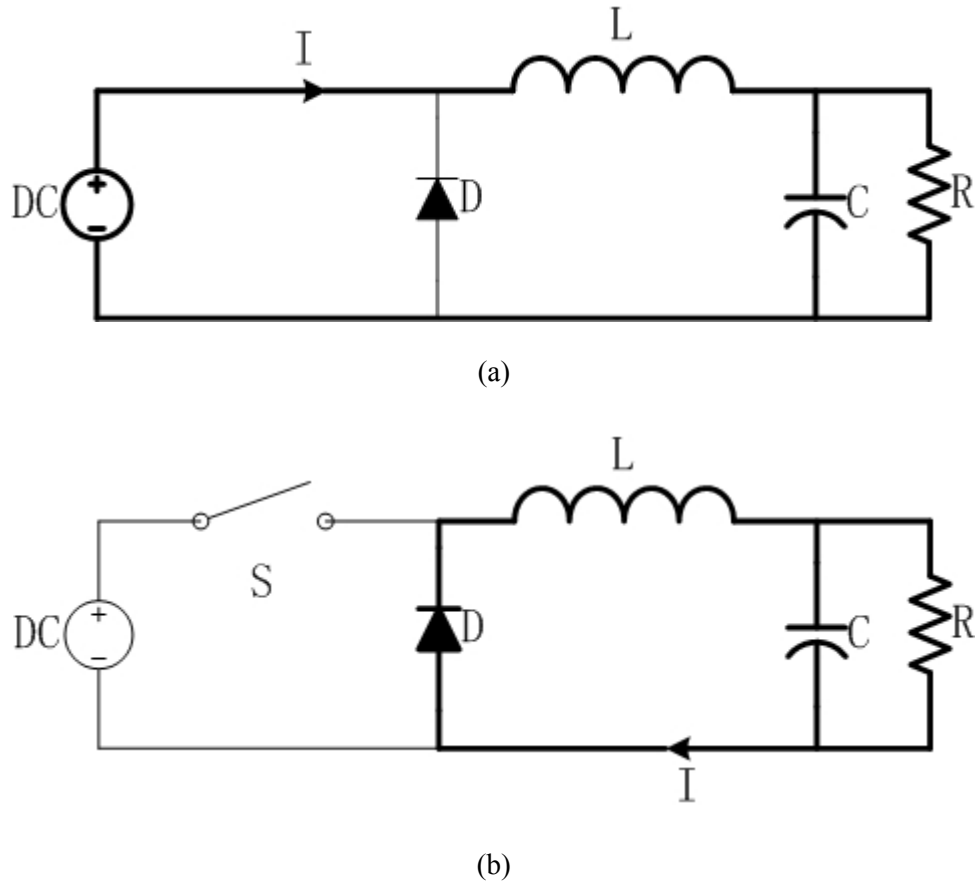

(a)

(b)

Figure 20. Current conduction path during (a) switch turn on; (b) switch turn off

A Buck converter operates in continuous mode if the current through the inductor (IL) never falls to zero during the commutation cycle. In this mode, the operating principle is described by the chronogram in Figure 20.

- When the switch pictured above is closed (On-state, top of figure 2), the voltage across the inductor is VL = Vi − Vo. The current through the inductor rises

linearly. As the diode is reverse-biased by the voltage source V, no current flows through it;

- When the switch is opened (off state, bottom of figure 2), the diode is forward biased. The voltage across the inductor is VL = − Vo (neglecting diode drop). The current IL decreases.

While switching between these two states, the steady state of different circuit components are shown in the Figure 21.

Figure 21. Periodic steady-state voltage and current of buck converter
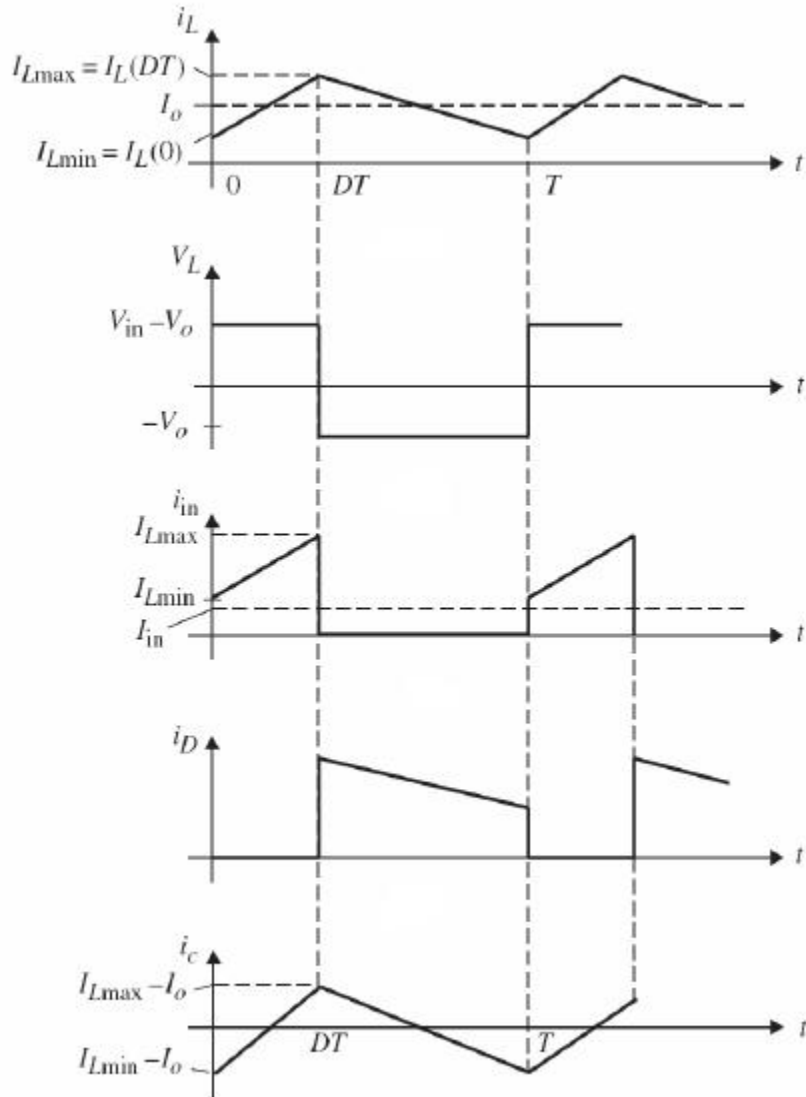
From top to bottom picture, it is waveform of inductor current, inductor voltage, switch current, diode current, and capacitor current, respectively. Under the periodic steady state condition, it is easy to deduct the step down ratio of voltage using the balance of inductor voltage.

$$(Vin - Vo) \cdot D \cdot T = -Vo \cdot (1 - D \cdot T) \qquad (5\text{-}1)$$

$$\frac{Vo}{Vin} = D \qquad\qquad (5\text{-}2)$$

The above result assumes an ideal switch, diode, and inductor. This simple buck converter is very popular in many power applications. Its switching frequency ranges from 20 KHz to 100 MHz nowadays.

5.1.2 Non-ideality induced Power Loss

There are several non-idealities existing in the circuit component, which will lead to different power loss. These non-idealities include output voltage ripple, on resistance of power MOSFET and power diode, and voltage drop across the switch and diode. The consequent power losses are divided into two categories: static power loss and dynamic power loss [44].
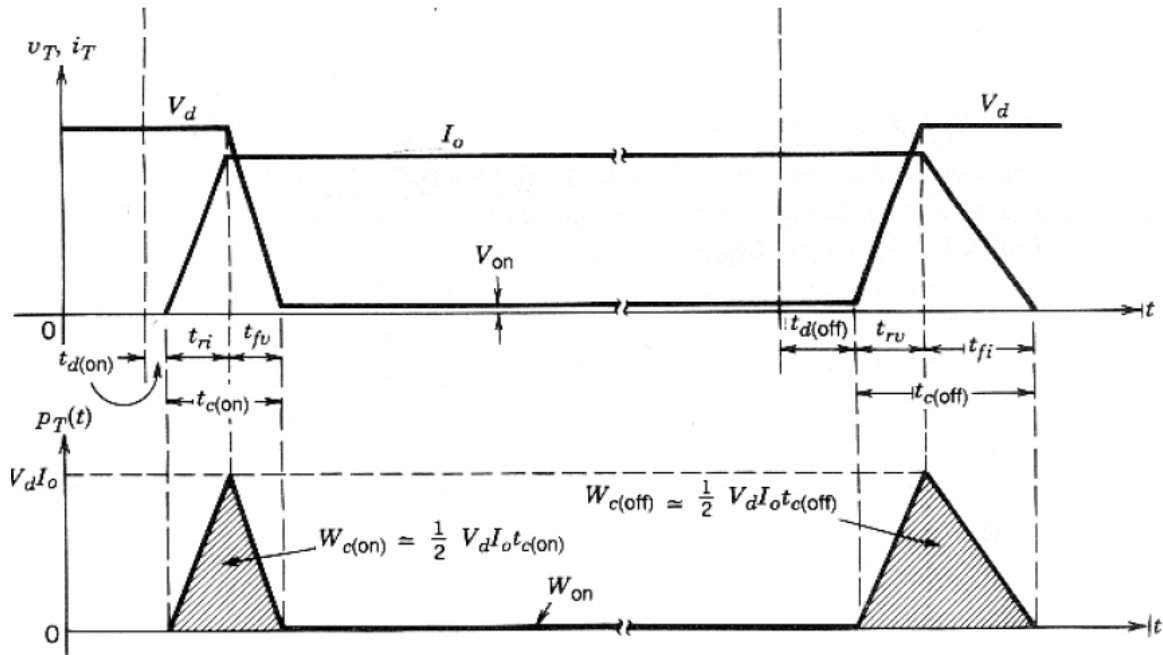

Figure 22. Power loss for the switch

According to Figure 22, the main static power loss is the conduction loss. When switch is on, there is current conducting through the device and small voltage drop across the switch at the same time. The power consumed during device on state is the conduction power loss, which is caused by the nonzero on-resistance of the switch.

$$P_{total} = P_{conduction} + P_{switching} \tag{5-3}$$

$$P_{conduction} = V_{ON} I_o \frac{t_{on}}{T_s} \tag{5-4}$$

The dynamic power loss usually refers to the switching loss of the device. This is large for switch under inductive load.

$$P_{swiching} = P_{S(on)} + P_{S(off)} \tag{5-5}$$

$$P_{S(on)} = \frac{V_d I_o t_{(on)} f_s}{2} \tag{5-6}$$

$$P_{S(off)} = \frac{V_d I_o t_{(off)} f_s}{2} \tag{5-7}$$

Another power loss is often omitted, which becomes significant in higher frequency. This is the gate drive power loss which occurs as a result of the power required to turn the switches on and off. Gate charge is a good indicator for such power loss, which is related with the energy required to charge and discharge the gate capacitance to turn gate between the threshold voltage and the on voltage. The optimum gate drive power loss device can be chosen from those devices with minimum gate charge and operating the device at low frequency.

$$P_{gate} = Q_G \cdot V_{GS} \cdot f_s \tag{5-8}$$

The major power losses are introduced here. They are good indicators whether InGaAs LDMOS is good candidate for power applications.

5.2 Power Efficiency of InGaAs LDMOS

InGaAs LDMOS will be the actual switch device run in mixed mode simulation to explore the performance of the device. Also Si LDMOS is put into simulation for peer comparison purpose. Two kinds of buck converter are considered in the following study: single switch (high-side switch) and synchronous buck converter (both high-side and low-side switch). For only high-side switch, the power efficiency is degraded by the power loss of low-side diode, so its efficiency is highly related with the duty cycle D of the switch control voltage.

5.2.1 High-side Switch Buck Converter

The following experiments are done under different switching frequency ranging from 100 kHz to 1 GHz, but with fixed duty cycle of 50%. With regarding to the component value, under the switching frequency of 1 MHz the inductance is 10μH and capacitor is 1μF. The output voltage should be around 5 V with input voltage of 10V. Figure 23 shows the transient waveform of output voltage and inductor current for buck converter operating at 1 MHz for InGaAs LDMOS case. After the initial unstable stage, the output voltage fluctuates around 5 V output range.
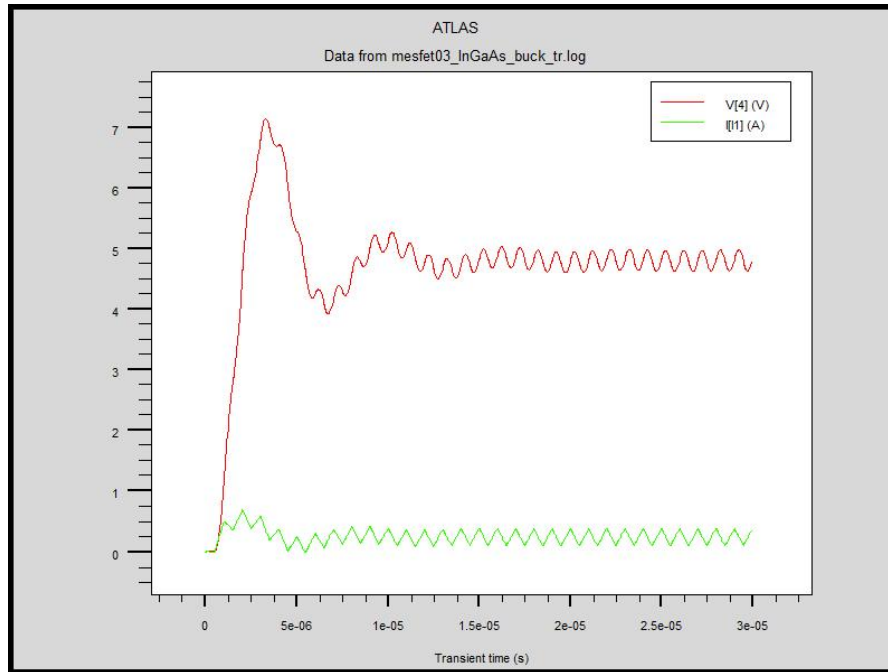
Figure 23. Output voltage and inductor current of InGaAs LDMOS switch buck converter

Further experiments are taken for switch under different frequency compared with conventional LDMOS. Figure 24 shows the similar case for Si LDMOS switch, which is very similar to that of InGaAs LDMOS with only minor difference.
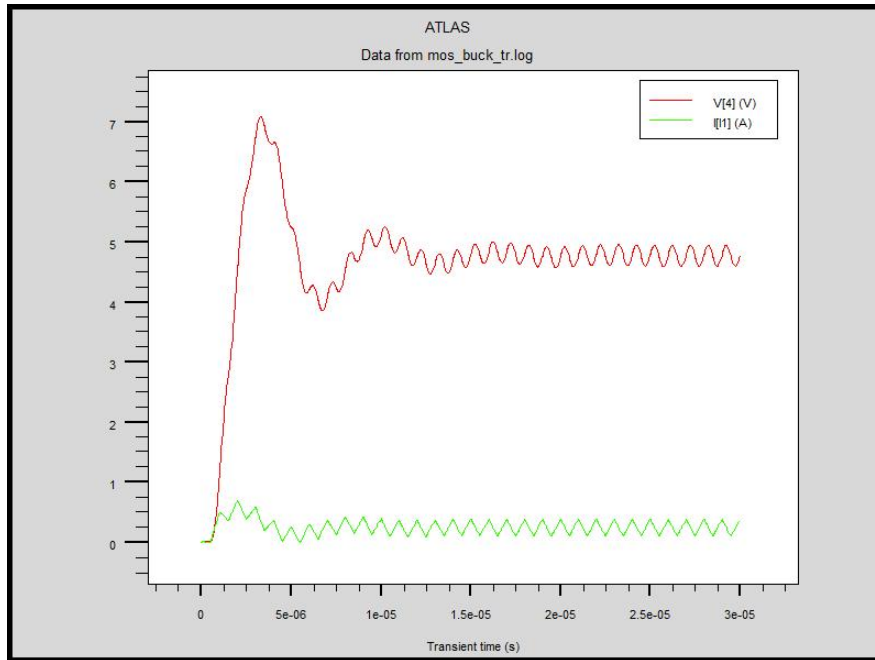
Figure 24. Output voltage and inductor current of Si LDMOS switch buck converter

Figure 25 shows the turn off process of InGaAs LDMOS switch, the overlap of the switch current and voltage drop is the source of turn off power loss.
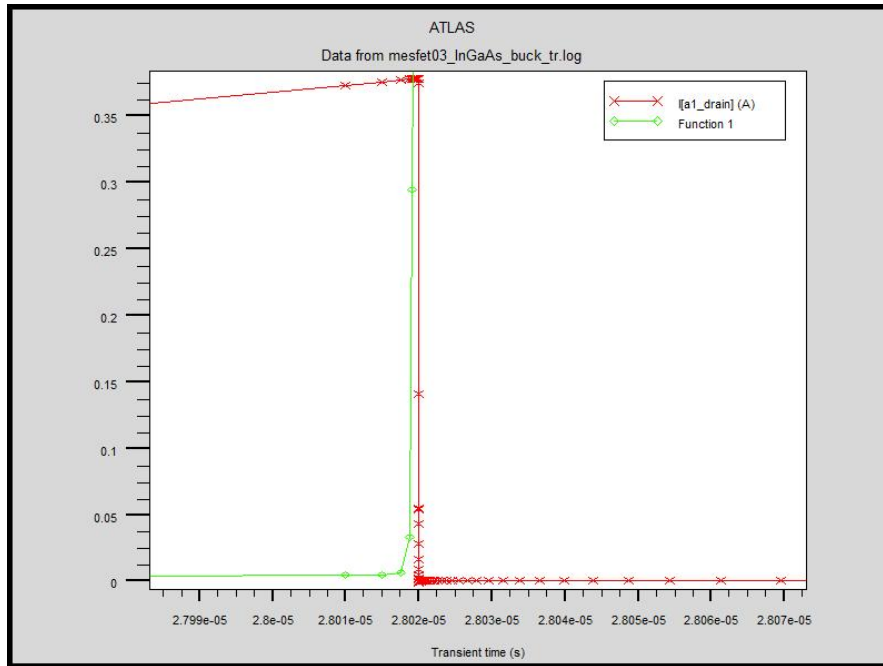
Figure 25. Turn off process of the switch

Figure 26 shows the turn on process of InGaAs LDMOS switch. The current first increase to the suggested level and the voltage begins to drop. This process incurs turn on power loss.
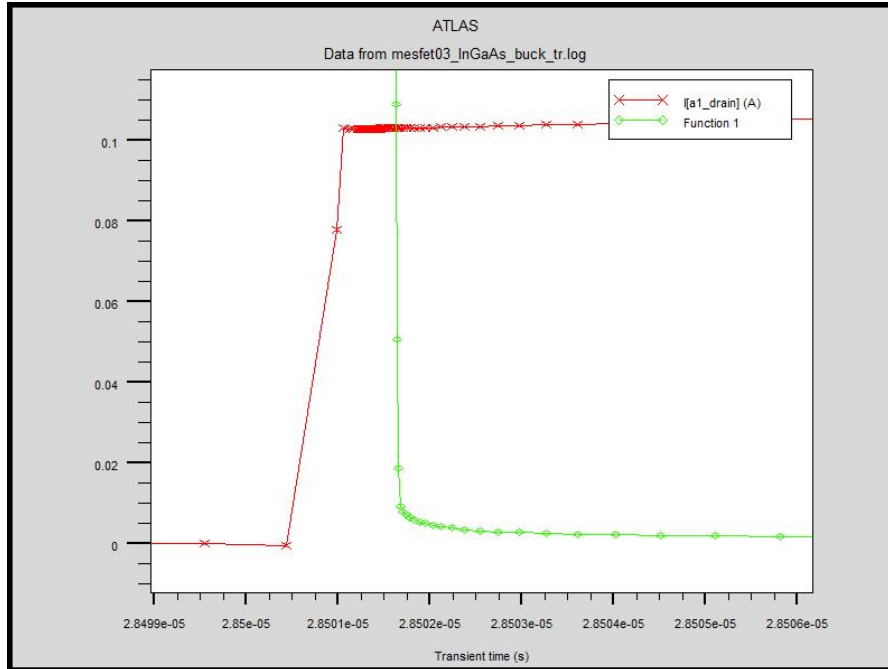
Figure 26. Turn on process of the switch

The power efficiency comparison between InGaAs LDMOS and Si LDMOS for buck converter can be seen from Figure 27. Buck converter using InGaAs LDMOS switch has slightly higher power efficiency than that using Si LDMOS. At 1 MHz, the power efficiency for InGaAs LDMOS case reaches 92.579%. For frequency higher than 100 MHz, both cases do not work correctly. The efficiency at high frequency range drops a lot and the gate drive power loss occupies a big portion of the total power loss.
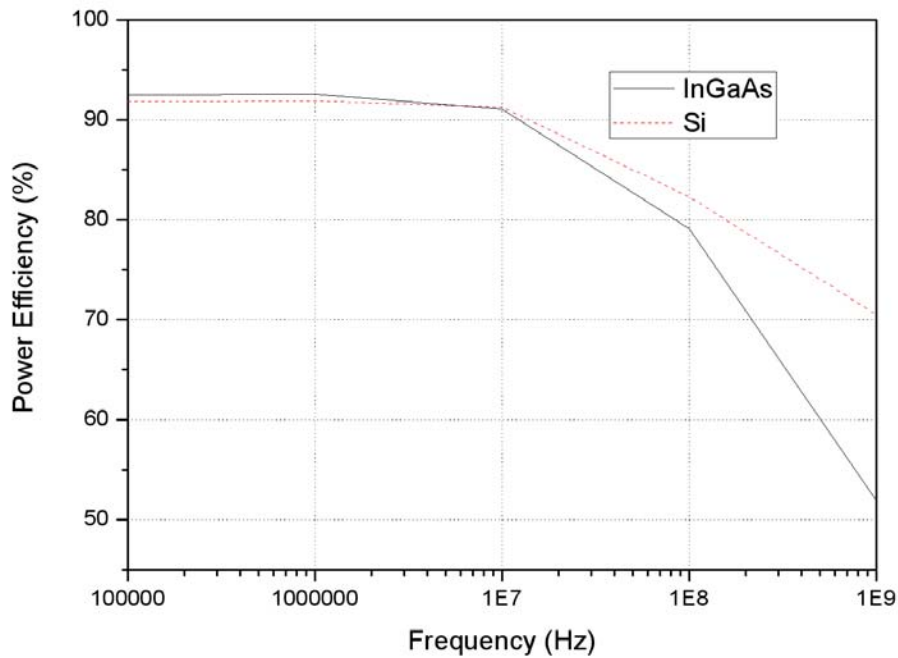
Figure 27. Power efficiency comparison for buck converter operating under different frequency

5.2.2 Synchronous Buck Converter

For this case, the power efficiency is increased because the diode is replaced by the active switch, which eliminates the almost 0.7V on voltage drop when diode is turn on. The reduced power loss due to low-side switch instead of diode leads to both higher power efficiency and more complicated control circuit.

The component value is similar to the above case. The inductance value of 10μH and capacitor value of 1μF is picked for circuit operating at 1 MHz. The circuit schematic

can be view in Figure 28. The power efficiency is less related to the duty cycle of the switch since both high-side and low-side switch use the same LDMOS device.
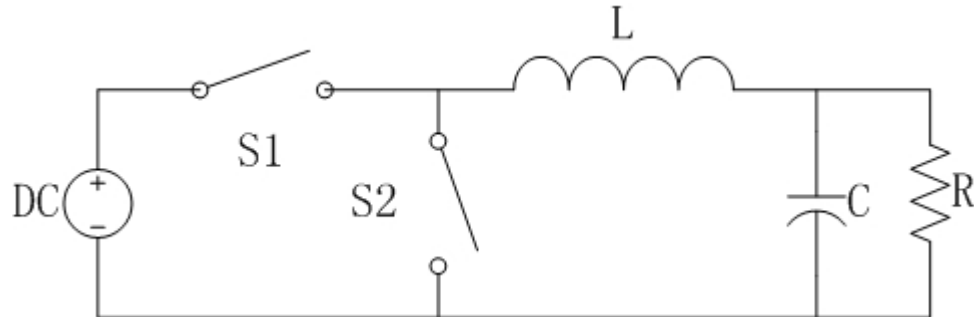
Figure 28. Schematic of synchronous buck converter

The operation frequency of the synchronous buck converter is swept from 100 KHz to 100 MHz in decade step increase. From Figure 29, it is seen that InGaAs LDMOS is better than Si LDMOS. The higher power efficiency is obtained at low frequency compared with single switch buck converter. For example, at 1 MHz, the power efficiency for InGaAs LDMOS synchronous buck converter is 99.373%, which is much higher than single switch buck converter. But with the frequency goes up, the power efficiency shows a rapid drop, which is mainly due to the gate charge limitation of the LDMOS switch. Under the same condition, InGaAs LDMOS beats Si LDMOS for higher power efficiency. For high frequency operation, it is necessary to optimize the structure of InGaAs LDMOS for smaller gate charge design.
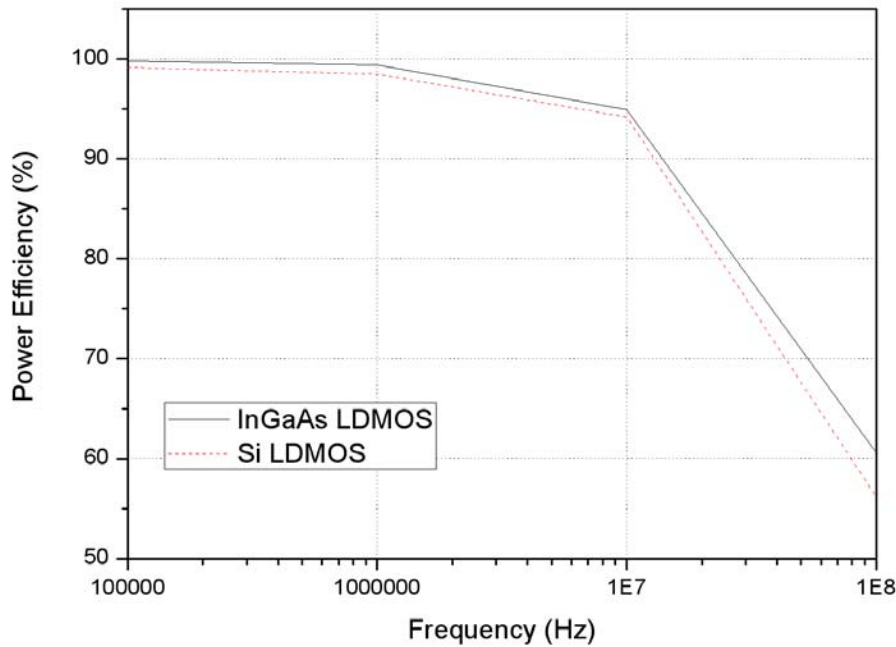
Figure 29. Power efficiency comparison for synchronous buck converter

5.3 Chapter Outline

In the DC-DC buck converter circuit, InGaAs LDMOS as high side switch shows the power efficiency of 92.579% at 1 MHz. It is better than the Si LDMOS under similar condition at low frequency. Also synchronous buck converter is studied, which has higher power efficiency for both InGaAs LDMOS and Si LDMOS switches. But as long as the high frequency operation is considered, both circuits show a big drop in power efficiency and large gate drive power loss is observed, which indicate the gate charge limitation of both LDMOS devices. Currently under low and median frequency operation,

InGaAs LDMOS is a better candidate for power applications. Future work is still under

way to further optimize the device for smaller gate charge design and thus high frequency

operations.

CHAPTER SIX: CONCLUSIONS

6.1 Accomplishment

In this work, an InGaAs LDMOS device is proposed. First of all, the basic LDMOS background and theory is reviewed, which including the basic transport equations used in TCAD tools, LDMOS current model, and self-heating effect. Then InGaAs material properties are described, its benefit is high electron mobility compared with silicon. The device structure design parameters are related with the performance, which is used to design the device structure in this work.

We suggest $In_{0.65}Ga_{0.35}As$ as substitute and propose a 0.5-µm channel-length $In_{0.65}Ga_{0.35}As$ LDMOS. Considered different gate dielectric constant, comparisons between InGaAs LDMOS and Si LDMOS are made in two ways, which are the same gate insulator thickness and the same gate capacitance. The on-resistance of the InGaAs LDMOS shows a big improvement with no degradation on breakdown voltage over Si LDMOS. Also it is indicated from these comparisons that FOM of InGaAs LDMOS shows a 91.9% improvement to that of Si LDMOS. The benefit of using InGaAs LDMOS as switch for power applications is studied further. Simple DC-DC buck converter is utilized to observe the performance of LDMOS. The InGaAs LDMOS switch is put into the buck converter circuit with operation frequency sweeping in the range from 100 KHz to 100 MHz. Also synchronous buck converter case is prepared and observed. At low and median frequency range, it turns out InGaAs LDMOS is better than its peer Si LDMOS device for power applications. But for high frequency, there is limitation in device gate

charge and large gate drive power loss will be introduced. Thus in order to operate in higher frequency, smaller device gate charge should be designed.

6.2 Future Work

The work in this thesis is not full picture yet. Further lab sample should be fabricated for real sample test and comparison for power application. Parameters like Qgd, Ron and BV should be extract from these experiments to support the theory and simulations done in this work. Also there will be a lot fabrication issue beyond expectation, especially material related issues. While in the process of overcoming the difficulty of process, novel ideas will emerge.

Except the fabrication is expected, further device optimization like better RESURF structure need to be considered for specific application, for example, high frequency power application. Also smaller gate charge, smaller on resistance, and higher breakdown voltage is always the key design goal in the device optimization.

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